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CHARACTERIZATION OF THE TRANSIENT BEHAVIOR OF A MESFET

Vesna Borelli, B.Eng.
Michel Bégin, M.Sc. A.
Fadhel. M. Ghannouchi, Ph. D.

Département de génie électrique

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Introduction

Communications technology at microwave frequencies requires integrated circuits with higher performances. Furthermore, for such applications as high-speed digital and analog circuits [1], GaAs has become a serious alternative to Si because of its superior qualities such as high f_t, excellent optical properties and high speed for the majority carriers. Trap levels [2-4], and especially the low thermal conductivity of the GaAs material [4, 5], cause non-negligible problems in obtaining accurate models for these devices. To study the transient behavior of a GaAs MESFET, two sets of measurements were made: pulsed I-V and pulsed RF. Pulsed I-V curves were obtained by pulsing Vds. The instantaneous S-parameters were measured using a Six-Port Network Analyzer (SPNA) operating in burst mode. These S-parameters were then used to extract the small-signal equivalent circuit elements. The results reveal the time dependence of some intrinsic parameters of the MESFET.

1 Modeling and Parameter Extraction

A small-signal equivalent circuit, proposed by A. Cappy [6] and shown in figure 1, was used to analyze the device behavior. This conventional equivalent circuit can be divided into two parts :

1- the intrinsic elements g_m, G_{ds}, C_{gs}, C_{gd}, C_{ds}, R_i and tau which are function of the bias conditions;

2- the extrinsic elements L_g, R_g, C_{pg}, L_s, R_s, R_d, L_d and C_{pd} which are independent of the bias conditions.

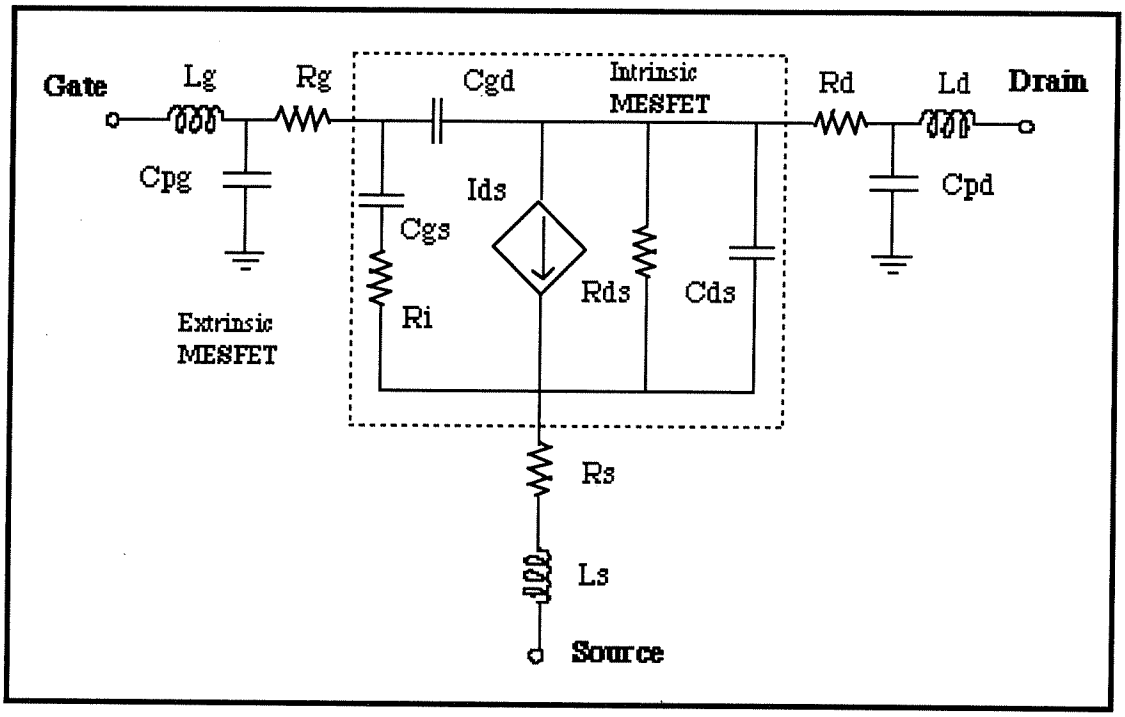


Fig. 1. Small-signal equivalent circuit of the MESFET.

Since the intrinsic device shows a PI topology, the admittance matrix has to be used to characterize its electrical properties. Therefore the problem is to determine the intrinsic y parameters from the experimental data, that is from the measured S-parameters of the extrinsic device. First, all the extrinsic elements have to be determined by the so-called cold modeling (where drain-to-source voltage Vds=0V). Then from the measured S-parameters, simple matrix manipulations allow to carry out the intrinsic admittance matrix. This can be done using the following procedure :

1- measurement of the S-parameters of the extrinsic device;

2- transformation of the S-parameters to impedance parameters and subtraction of the series elements L_g and L_d;

3- transformation of Z to Y parameters and subtraction of C_{pg} and C_{pd} that are in parallel;

4- transformation of Y to Z parameters and subtraction of R_g, R_s, L_s and R_d that are in series;

5- transformation of Z to Y parameters that corresponds to the desired matrix.

To determine the parasitic resistances, inductances and capacitances, the S-parameters are measured at a Vds of 0V. In this case the transistor is a non-linear symmetric device. First the parasitic gate, source and drain resistances and inductances are determined at a positively biased gate, so that the influence of the C_{pg} and C_{pd} parasitic capacitances is negligible. At these bias points the following simplified equations are valid:

$$Z_{11} = R_s + R_g + R_c/3 + nkT/qI_g + j\omega(L_s + L_g) \quad (1.1)$$

$$Z_{12} = Z_{21} = R_s + R_c/2 + j\omega L_s \quad (1.2)$$

$$Z_{22} = R_s + R_d + R_c + j\omega(L_s + L_d) \quad (1.3)$$

where R_C is the channel resistance at the applied gate voltage and nkT/qI_g is the differential resistance of the Schottky diode. As there are four unknown resistors and only three equations with corresponding real parts, one additional relation is required. To do this, different methods can be used [6]. The gate and drain capacitances C_{pg} and C_{pd} can be determined from S-parameter measurements at gate voltages below pinch-off using the following simplified equations:

$$\mathrm{Im}(Y_{11}) = j\omega(C_{pg} + 2C_b) \quad (1.4)$$

$$\mathrm{Im}(Y_{12}) = \mathrm{Im}(Y_{21}) = -j\omega C_b \quad (1.5)$$

$$\mathrm{Im}(Y_{22}) = j\omega(C_{pd} + C_b) \quad (1.6)$$

where C_b is the residual coupling capacitance from the gate to the source and drain region.

It has been showed that all the device parasitic elements can be measured when Vds is set to 0V. The intrinsic y parameters and the equivalent circuit elements of the MESFET can be carried out for any bias point using the procedure described above and finally solving the following equations:

$$C_{gd} = -\frac{Im(Y_{12})}{\omega} \tag{1.7}$$

$$C_{gs} = \frac{Im(Y_{11}) - \omega C_{gd}}{\omega}\left(1 + \frac{(Re(Y_{11}))^2}{(Im(Y_{11}) - \omega C_{gd})^2}\right) \tag{1.8}$$

$$R_i = \frac{Re(Y_{11})}{(Im(Y_{11}) - \omega C_{gd})^2 + (Re(Y_{11}))^2} \tag{1.9}$$

$$g_m = \sqrt{\left((Re(Y_{21}))^2 + (Im(Y_{21}) + \omega C_{gd})^2\right)(1 + \omega^2 C_{gs}^2 R_i^2)} \tag{1.10}$$

$$C_{ds} = \frac{Im(Y_{22}) - \omega C_{gd}}{\omega} \tag{1.11}$$

$$g_{ds} = Re(Y_{22}) \tag{1.12}$$

$$tau = \frac{1}{\omega}\arcsin\left(\frac{-\omega C_{gd} - Im(Y_{21}) - \omega C_{gs} R_i Re(Y_{21})}{g_m}\right) \tag{1.13}$$

2 Characterization of the MESFET

It is well known that the model accuracy depends on the characterization techniques. Here, three different measurement methods were used:

1-DC

2-pulsed I-V

3-pulsed RF

2.1 DC measurements

The drain-to-source current, Ids, versus Vds and Vgs was traced from experimental data and is shown in figure 2. From this figure, it can be seen that, for Vgs greater than -1V and for Vds greater than 2.5V, the Ids curves have negative slopes. This means that for increasing Vds the current decreases. As a consequence of this, the output conductance has a negative value, which is of no physical meaning. In order to explain this and to improve the equivalent model used for the MESFET, thermal effects have to be taken into account.

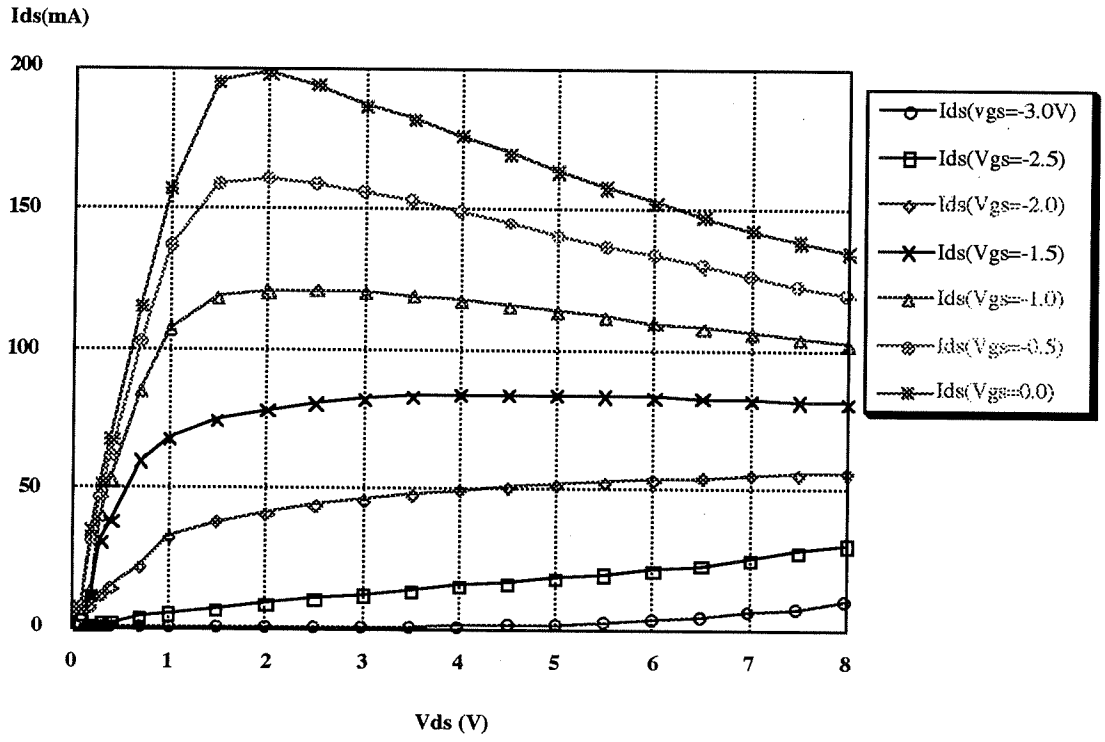


Fig. 2. DC characteristics of the MESFET

The Ids versus Vgs curves show a similar behavior: for increasing values of Vds greater than 2.5V, the Ids current decreases and then the transconductance gm decreases too, at these bias conditions.

2.2 Pulsed I-V measurements

In order to put in evidence the transient effects, pulsed I-V measurements were taken with the experimental setup shown in Figure 1. The voltage drop, due to the Ids current across a known resistor, was amplified and then measured with a digitizing oscilloscope. The resistor values were chosen to obtain a voltage gain of 10. Three pulses of different widths were used at several bias points.

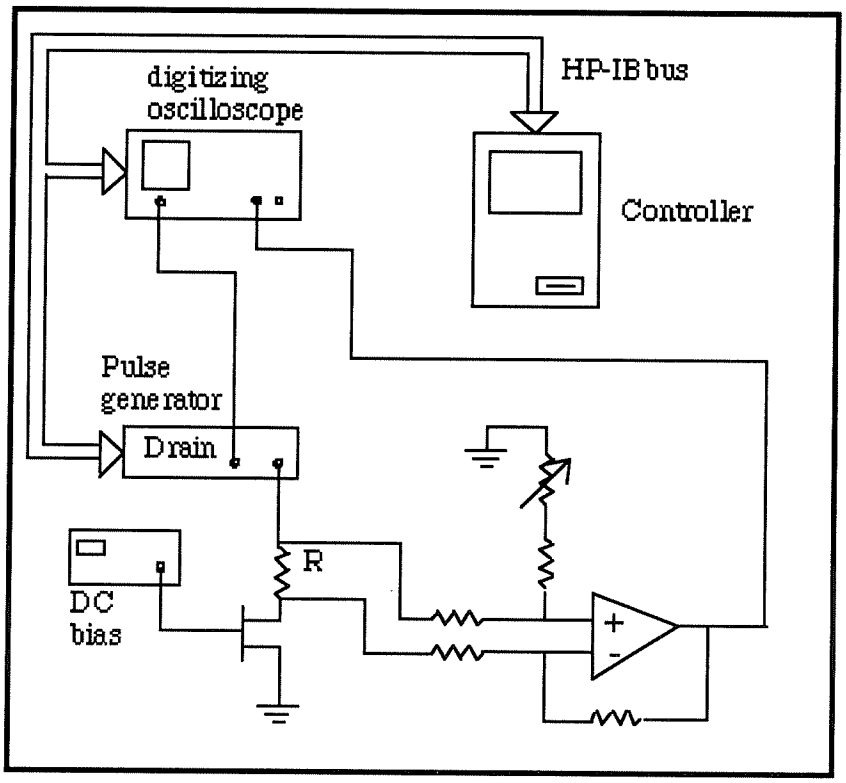
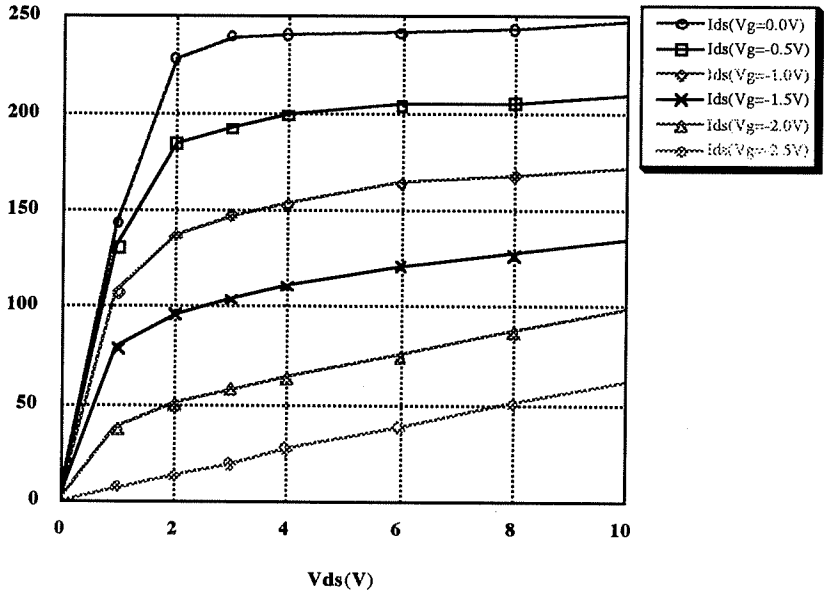


Fig. 3. Pulsed I-V measurement setup.

Figures 4a and 4b show the results at the beginning and the end of the pulse. It was

noticed that the slopes of the Ids curves versus Vds start beeing negative after the first 100μs.



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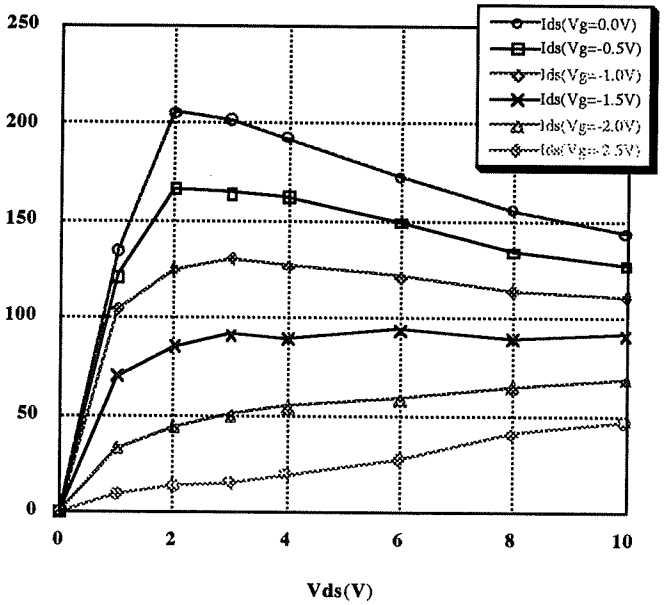


(b)

Fig. 4. Ids versus Vds (a) after 24μs (b) after 1.4s from the beginning of the pulse.

Moreover, the Ids values, in the different bias points, are greater than the corresponding DC values. They progressively decrease and it can be reasonably deduced that they will coincide with the DC values, once the steady state is reached.

2.3 Pulsed RF measurements

A SPNA in burst mode was used to study the pulsed behavior of the MESFET and to characterize the time response of the equivalent circuit parameters. The instantaneous S-parameters of the DUT, corresponding to different pulses, were measured. A SPNA is essentially made up of:

1- two six-port junctions;
2- eight linearized diode detectors;
3- a digitizing oscilloscope to record the waveforms at the output of the eight diode detectors;
4- a pulse generator;
5- a RF source.

The setup shown in figure 5 was used to characterize a medium power MESFET, a NE900189 (0.5μmx750μm), applying a burst of voltage at the drain while maintaining the gate bias constant. The MESFET was mounted on a test fixture and de-embedded using the TRL calibration method. Three different pulses of 1ms, 50ms and 1.5s width were used. The system was calibrated at the frequency of 2.3GHz. The measurements were made at the following bias points:

Vgs \ Vds	1.0	2.0	6.0	8.0	10.0
0.0	x	x	x	x	x
-1.5	x	x	x	x	x
-2.0	x	x	x		x
-2.5	x	x	x		x

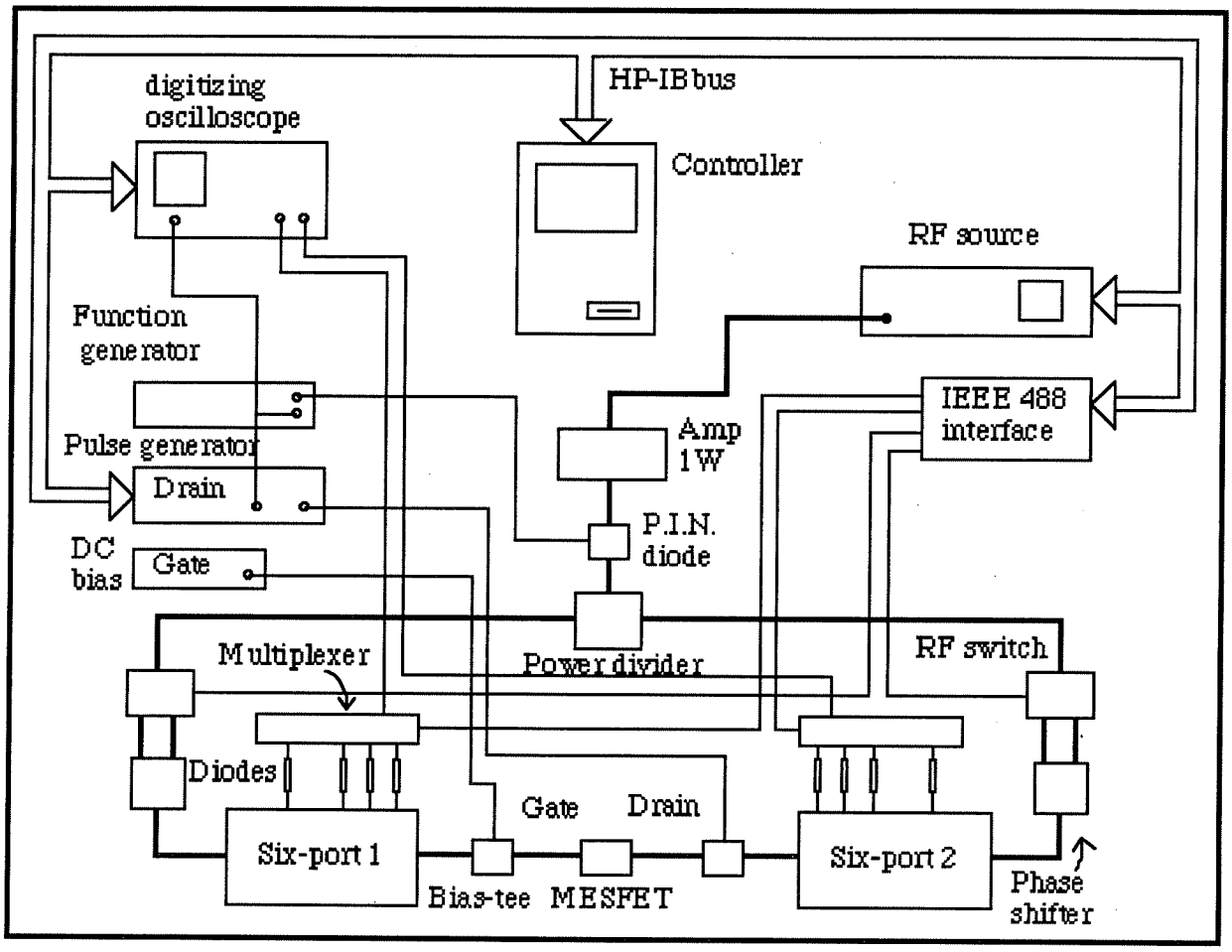


Fig. 5. Experimental setup used for the S-parameter measurements.

So the instantaneous S-parameters, at the different bias conditions, were measured. The technique described previously was used to strip the parasitic elements and to carry out the values of the intrinsic parameters of the equivalent circuit. This was made by the DCμWV program.

Figures 6a and 6b show the behavior of the intrinsic transconductance g_m. It is the most important among the non linear elements of the equivalent circuit. To first order, g_m is a function of gate bias only. The transconductance g_m increases as the bias of the gate is increased. But there is also a dependence upon Vds. For very low values of Vgs (around -2.5V), g_m increases for increasing Vds. For Vgs values greater than -2.0V, g_m increases for increasing Vds up to 6V, and then starts decreasing as Vds exceeds this value. This

can be explained considering the thermal effects on the Ids curves at these bias points. In figure 6a it is shown how g_m changes versus time. It can be seen that, at the very beginning of the pulse, g_m increases for increasing Vds and, at the end of the pulse, g_m increases and then decreases as Vds becomes greater than 6V.

Regarding G_{ds}, it is shown, in figure 7a, that it decreases for increasing Vds. At low Vds, G_{ds} increases as Vgs is increased. However, at higher values of Vds, it increases for increasing Vgs values from -2.5V to -2.0V and then G_{ds} decreases. This can be seen in figure 7b, and can be explained in terms of self-heating that becomes important for bias values in the saturation region at high gate voltages. In figure 7b the thermal effects allow to understand the higher percentage reduction versus time of G_{ds}, when Vgs is equal to 0V.

The main contribution to C_{gs} is due to the depletion region under the gate junction. The increase in the C_{gs} value, for increasing Vds and Vgs, can be explained referring to the depth and extension of the depletion region. Its behavior versus time is constant. See figures 8a and 8b.

C_{gd}'s main variation is related to the extension of the depletion region between the gate and the drain. In fact, for increasing Vds, C_{gd} decreases. Although the dependence upon Vgs is slighter, there is a decrease of C_{gd} for increasing Vgs. No time dependence was found (see figure 9).

The capacitance C_{ds} presents its typical behavior versus bias changes, that is C_{ds} increases for increasing Vds and decreasing Vgs. No significant time dependence has been found, except for high gate and drain voltages, where dissipation cannot be considered negligible as can be seen in figure 10.

According to the literature, we found out that it is particularly hard to extract the intrinsic

parameter R_i with accuracy. Decreasing R_i for increasing Vgs was obtained, as expected. For each Vgs value, R_i decreases as Vds increases. There is no evident time dependence as figure 11 shows.

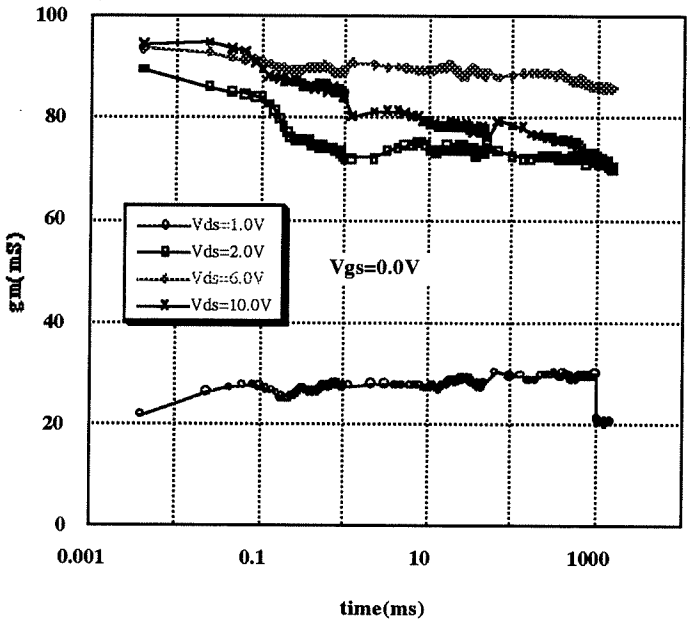
The intrinsic parameter tau is the transconductance time delay and corresponds to the transit time of the majority carriers from the source to the drain passing through the bias dependent region under the gate. It should be pointed out that tau decreases for increasing Vgs and Vds. The values obtained are larger than the expected ones, except those in the region of high Vds and Vgs. There is a weak increase versus time as is illustrated in figure 12.

It is clear from figure 13 that the bias nonlinearity of f_t is governed by the bias nonlinearities of g_m and C_{gs}.

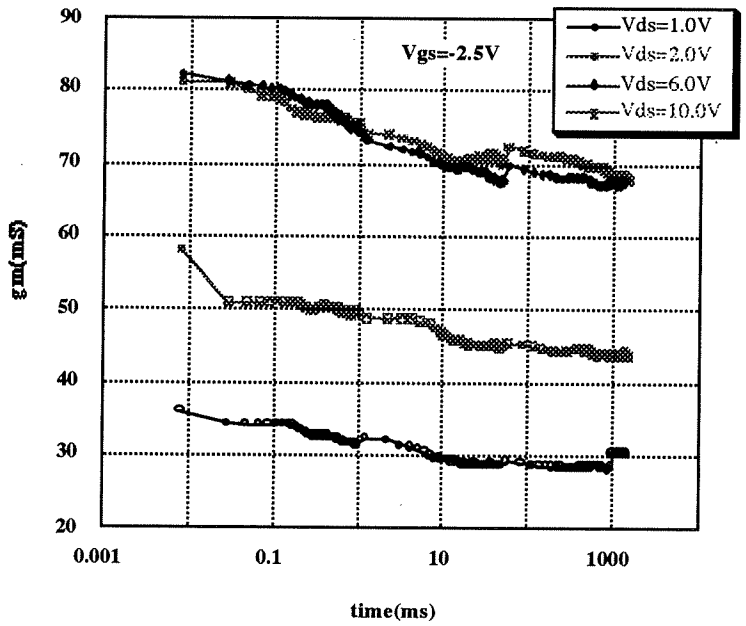
Finally, the S-parameters computed using the extracted parameter values, are in good agreement with the measured data, thereby validating the accuracy of the approach used.

Vds=6.0V Vgs=-1.5V

S-Par.	$\|S_{11}\|$	$\angle S_{11}$	$\|S_{12}\|$	$\angle S_{12}$	$\|S_{21}\|$	$\angle S_{21}$	$\|S_{22}\|$	$\angle S_{22}$
Meas.	0.71	-94.5	0.065	58.0	3.18	103.2	0.45	-72.5
Comp.	0.68	-87.2	0.063	53.6	3.26	65	0.41	-64.6

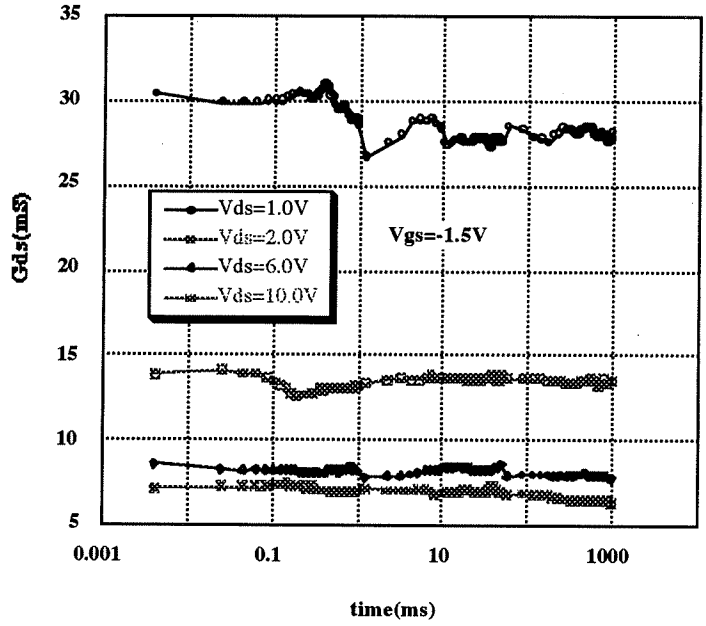


(a)



(b)

Fig. 6. Variation of g_m with time.



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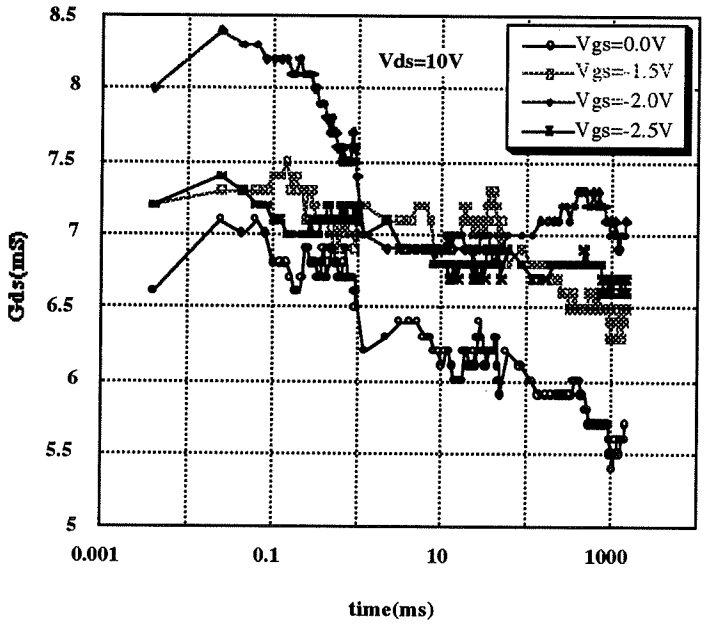
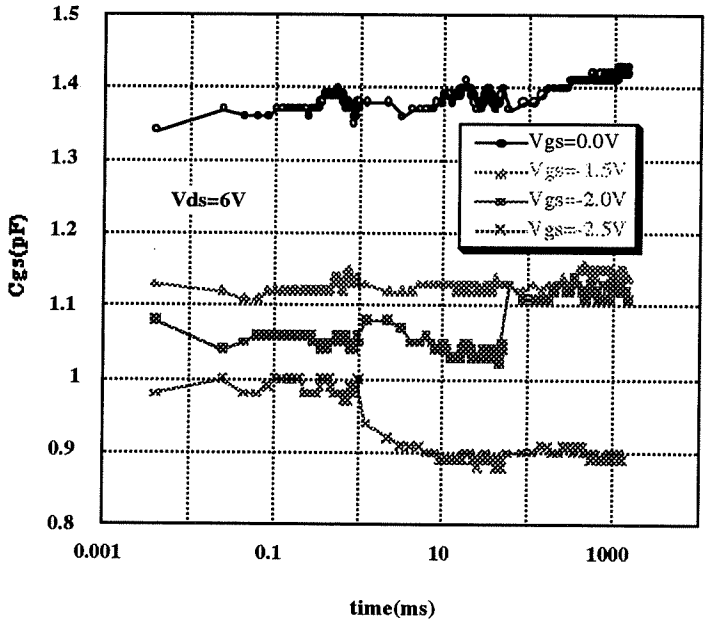


(b)

Fig. 7. Variation of G_{ds} versus time.



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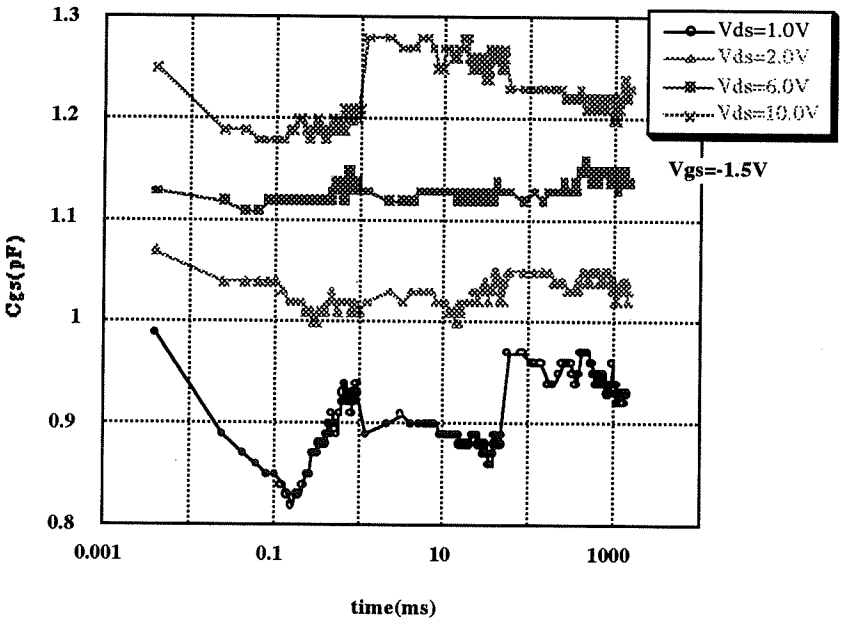

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Fig. 8. Variation of C_{gs} with time.

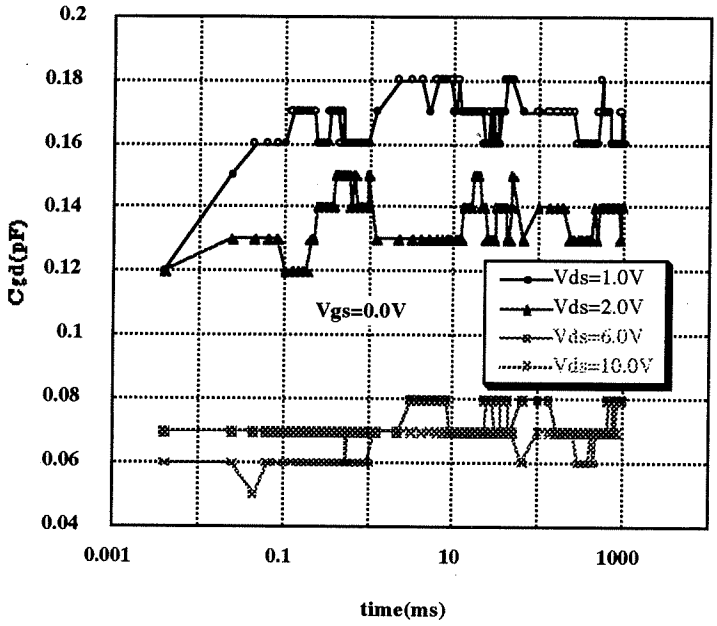

Fig. 9. Variation of C_{gd} versus time.

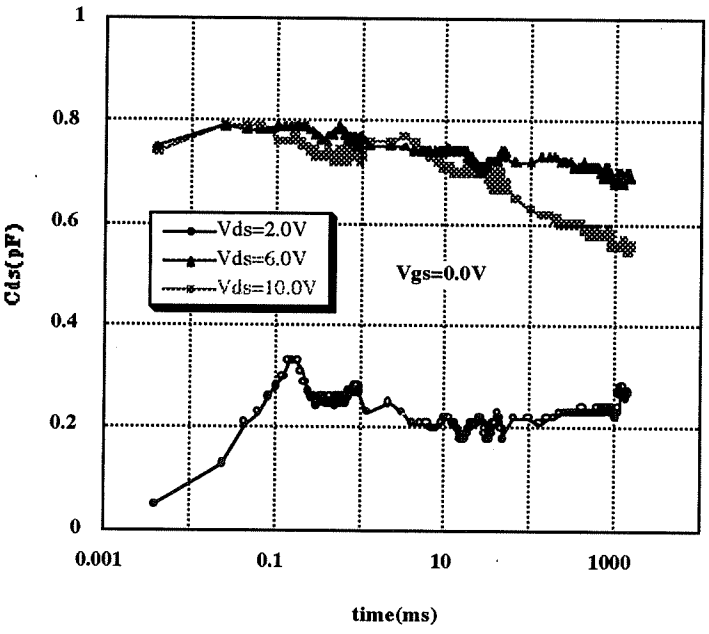

Fig. 10. Variation of C_{ds} with time.

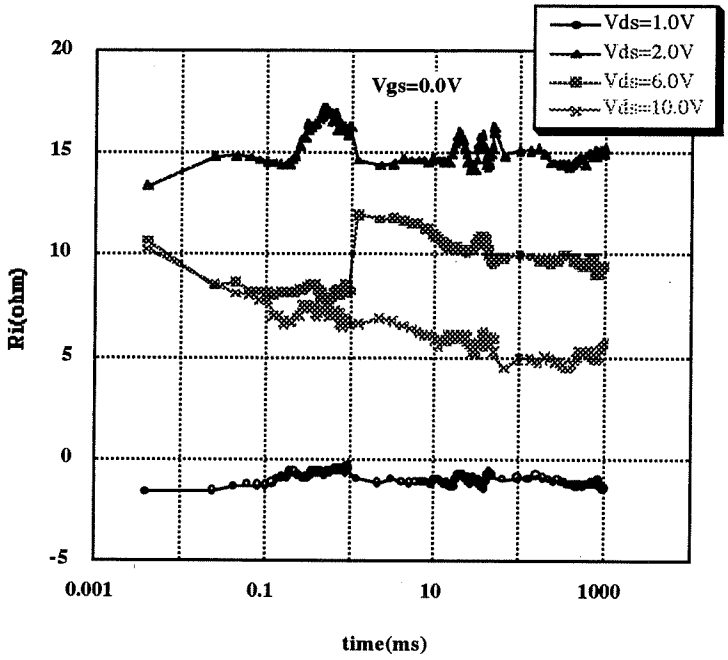

Fig. 11. Variation of R_i versus time.

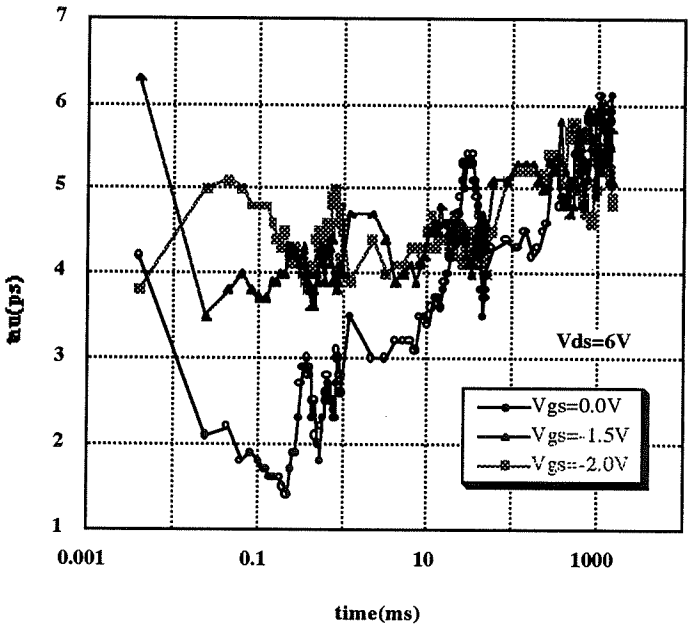

Fig. 12. Variation of tau with time.

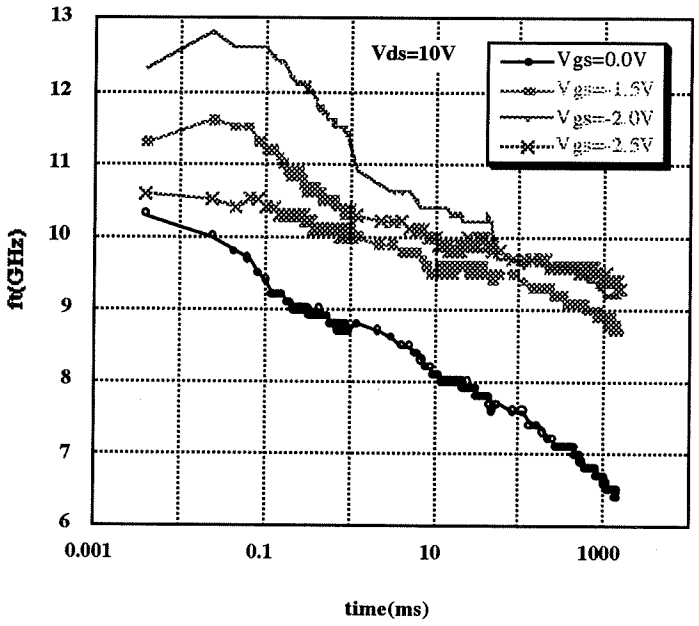

Fig. 13. Variation of f_t versus time.

Conclusion

The main purpose of this work was to study the transient behavior of the MESFET small-signal equivalent circuit elements. To do this a SPNA was used to measure the instantaneous S-parameters under burst drain bias and RF conditions. Self-heating effects were pointed out. The time independence of most of the intrinsic parameters allows the use of a simple model incorporating only a few time dependent elements to reproduce the effective device behavior.

Regarding the measurement setup, few recommendations should be made in order to improve the accuracy of the results. First, the vertical resolution (8 bits) of the digitizing oscilloscope, when used in single shot, was found to be the main limitation of the system. Second, the settling time of 1.5μs of the pulse generator prevents us from studying the behavior of the device at the very beginning of the pulse. Finally, other significant limitations are related to the inaccuracy of the parasitic extraction techniques and the analytical method used to compute the intrinsic elements of the equivalent circuit of the MESFET.

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