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A wide dynamic range programmable isolation voltage amplifier based on a Hall effect sensor

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Thèse présentée en vue de l'obtention du diplôme de *Philosophiæ Doctor*

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a été dûment acceptée par le jury d'examen constitué de :

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RÉSUMÉ

Depuis quelques années, la demande industrielle de circuit d'interface s'est spécialisée vers des architectures capables de tolérer des hautes tensions en mode commun. Les activités de recherche se sont alors orientées vers la conception d'amplificateurs d'isolation aptes à maintenir des caractéristiques performantes en présence de bruit mode commun. En dépit des récentes avancées dans le domaine, ces architectures complexes demeurent encombrantes, consomment beaucoup de puissance et de ce fait ne sont pas adaptées aux circuits d'interface multi-canaux.

Cette thèse présente pour la première fois un amplificateur d'isolation dont le principe de base repose sur un couplage par champ magnétique utilisant un capteur à effet Hall. Cette approche a permis de concevoir un amplificateur d'isolation compact et entièrement intégré, qui permet une architecture multi-canaux qui n'utilise que deux puces. L'amplificateur permet une isolation de 0.6 kV (V_{iso}), un taux de rejet en mode isolation de 120 dB pour les fréquences inférieures à 100 Hz et un rapport signal-bruit (SNR) de 86 dB mesuré avec un bande passante de 1 Hz. En comparaison avec les circuits existants, cette approche facilite la mise en boîtier, s'avère plus compacte en surface de silicium et consomme beaucoup moins. Tous les composants des circuits de tansmission et de réception sont intégrés dans une technologie CMOS 0.35 μm. De plus, l'ampli présente une erreur de non-linéarité de seulement 0.6 % provenant de la linéarité du capteur à effet Hall pour de faibles champs magnétiques. L'amplificateur permet de mesurer une tension différentielle ou un courant en y ajoutant une résistance shunt.

Le système d'isolation consiste en un pilote rail-rail et un modulateur hachoir pour le côté haute-tension (HV) de la puce. Le pilote possède un gain ajustable de façon à mesurer soit une tension ou soit un courant via une résistance shunt. Sur le côté basse tension de la puce (LV), on retrouve une bobine spirale intégrée, un capteur à effet Hall cruciforme optimisé, des références de tension et de courant, un amplificateur bas bruit (LNA), le démodulateur hachoir et un filtre anti-alias. Il possède également un amplificateur à gain programmable (PGA) afin d'adapter la sortie de l'amplificateur à un convertisseur analogique à numérique (ADC) ayant différentes gammes de tension à l'entrée.

Conséquemment à la méthode de modulation hachoir employée, le système requiert un circuit de recouvrement d'horloge. Ce circuit utilise le capteur à effet Hall côté récepteur et une bobine spirale

côté transmetteur. Comparé aux méthodes inductive, capacitive et optique, cette approche est plus compacte, permettant d'intégrer le circuit récepteur sous la bobine spirale.

Au cours de la thèse, trois circuits intégrés ont été fabriquées et testés. Ces travaux ont permis de publier deux articles de conférence et un article de revue, et deux autres articles de revue ont été soumis.

ABSTRACT

In response to the industrial need for a reliable, long life, and compact readout circuit capable of tolerating high common-mode voltages, many researchers and corporations have focused on adapting the isolation amplifiers (IA) to maintain robust performance in presence of common-mode noise. Despite all advances, yet they all suffer from being bulky, power-intensive, and complicated designs which makes them non applicable for multi-channel readout circuits.

In this thesis, we introduce the first reported isolation voltage amplifier based on magnetic sensors in which data isolation is achieved through the Hall-effect. Using this approach, we demonstrate a miniaturized and fully integrated IA capable of having multi-channel isolated readout circuits using only two dice. The fully integrated approach satisfies 0.6 kV of isolation working voltage (V_{iso}) and 120 dB of isolation mode rejection (IMR) for frequencies lower than 100 Hz, while achieving signal to noise ratio (SNR) of 86 dB in 1 Hz bandwidth. In comparison with similar products, the approach has minimal packaging complexity, consumes less dice area, and significantly reduces power consumption, which makes it suitable for multi-channel readout circuits and dense integration. Also, it has a good nonlinearity error of 0.6 % as a result of the linearity of Hall-effect sensors at low magnetic fields. This is the first demonstration of an approach compatible with multi-channel isolated sensing which stems from the small footprint of miniaturized transmit and receive (Tx/Rx) components as well as reduced power consumption. Finally, the design is capable of both shunt-based current sensing and differential voltage monitoring.

The implemented data transmission system consists of a rail-to-rail driver and chopper modulator for the high voltage (HV) side dice. The driver has an adjustable gain to make the design suitable for voltage and current sensing applications. Also, for the low voltage (LV) side's dice, an integrated spiral coil, optimized cross-shaped Hall-effect sensor, voltage/current references, a low noise amplifier (LNA), chopper demodulator, and anti-aliasing filter (AAF) are fabricated. The LV dice is equipped with a programmable gain amplifier (PGA) for versatile interfacing with an analog to digital converter (ADC) with different input ranges.

As a result of employed chopper modulator, a fully integrated approaches based on on-off keying (OOK) modulation was fabricated and tested to serve the clock-recovery of the design. This is a

first of its kind digital isolator that uses a Hall-effect sensor for the receiver circuit. Compared to inductive, capacitive, and optic, the approach has the smallest footprint or diameter of the on-chip transmitter coil and allows integration of the receiver circuit under the coil.

Three chips were fabricated and tested, 2-conference papers and 3-journal manuscripts were published or submitted to disseminate the contributions of this thesis.

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LIST OF SYMBOLS AND ABBREVIATIONS

AAF	Anti-aliasing filter
AC	Alternating current
ADC	Analog-to-digital converter
AlGaAs	Aluminium gallium arsenide
AM	Amplitude modulation
AMR	Anisotropic magnetic resistor
CMFB	Common mode feedback
CMOS	Complementary metal-oxide-semiconductor
CMRR	Common mode rejection ration
CMTI	Common mode transient immunity
CMN	Common mode noise
CT	Current transformer
CTR	Current transfer ratio
CTE	Coefficient of thermal expansion
CMV	Common mode voltage
DAC	Digital-to-analog converter
DC	Direct current
2DEG	Two-Dimensional Electron Gas
DIL	Dual in-line package
E_G	Energy bandgap
ESD	Electrostatic discharge
FBR	Full bridge rectifier
f_c	Carrier frequency

f_T	Cut-off frequency
GBW	Gain-bandwidth product
GA	Galvanic amplifier
GaAs	Gallium Arsenide
GaN	Gallium Nitride
gm	Transconductance
GMR	Giant magneto resistor
GR	Generation-Recombination
HBR	Half bridge rectifier
HF	High frequency
HPF	High pass filter
HV	High voltage
IA	Isolation amplifier
IC	Integrated circuit
IMR	Isolation mode rejection ratio
InGaAs	Indium gallium arsenide
INA	Instrumentation amplifier
IPT	Inductive power transfer
LF	Low frequency
LNA	Low noise amplifier
LV	Low voltage
MAGFET	Magnetic field effect transistor
MF	Magnetic field
MOSFET	Metal oxide semiconductor field-effect transistor

MR	Magneto-resistor
N_c	Effective electron density
ni	Intrinsic carrier concentration
NRC	Canadian National Research Council
N_v	Effective hole density
OOK	On-Off Keying
PCB	Printed circuit board
PGA	Programmable gain amplifier
PWM	Pulse width modulation
Q	Quality factor
QWHE/S	Quantum well Hall effect/sensor
RF	Radio frequency
RFID	Radio-frequency identification
RT	Room temperature
Si	Silicon
SoI	Silicon on Insulator
SiP	System in package
SNR	Signal to noise ratio
TC	Transient coefficient
TMR	Tunnel magnetoresistance
VGA	Variable gain amplifier
V_{iso}	Isolation working-voltage
V_N	Common mode noise
V_t	Thermal voltage noise

V_{th}	Threshold voltage
WBG	Wide bandgap

CHAPTER 1 INTRODUCTION

1.1 Problem statement

Several applications such as power monitoring of photovoltaic inverters, power system control and protection, and industrial sensor interface require electronics to operate in a high continuous working voltage (V_{iso}) of the monitoring units and withstand high common-mode voltage (CMV) surges including fault conditions and lightning strikes. In industries, like avionics, where numerous read out circuits are employed with their redundancies, it is critical that electronic components not only satisfy high-end standards but also keep small footprints and light weights.

Currently, avionic industries suffer from off package implementation that occupies lots of space and weight; because of various specifications of actuators and sensor interfaces, the employed electronics are non-uniform. Furthermore, the implemented electronics contain bulky and heavy inductors or transformers for electrostatic discharge (ESD) protection. A high degree of redundancy is built into the electronic installations to satisfy the high safety integrity level of the avionic industry, which further increases the consumed area. Therefore, an integrated design for harsh environmental conditions including high voltages (HV) of lightning strikes eliminates the need for bulky components for ESD protection. In addition, having a unique programmable front-end isolation amplifier (IA) capable of voltage and current monitoring of a wide range of sensor interfaces would unify designs, saves lots of space and wiring, lowers manufacturing costs, and consequently, decrease aircrafts' fuel consumption and maintenance costs.

1.2 Significance of the work

Several isolation amplifiers are proposed in the literature and are commercially available including inductive coupling [1, 2], acoustic/ultrasound coupling [3], optocouplers, and capacitive coupling [4]. All type of isolation barriers has been used for digital isolators with very robust noise performances. To benefit from digital transmission, the sensed signal first needs to be digitized using an ADC on the high voltage side of the amplifier. However, an ADC alone can consume high amount of power, which significantly increases the consumption of the amplifier. Therefore, if being employed in multi-channel readback circuits, the digitization solution comes with the price of a significant power consumption. In direct analog isolated data transmission, optocouplers are

the simplest solution with low nonlinearity and good isolation levels. However, they suffer from electrical and thermal stress which degrades their life span [5]; besides, being incompatible with CMOS processes, every isolated link requires a dedicated optocouplers which increases the total number of dices. Capacitive couplings have a very low signal resolution, and they transmit common-mode noise, which makes them unsuitable for analog data transmission. Inductive medium is the most robust means of analog data transmission which has an enlarged footprint due to the high-quality factor requirements of its transformer, and it consumes about one Watt of power, so its usage is still not applicable in multi-channel applications.

This thesis investigates the first reported IA that detects voltages and employs Hall-effect sensors as the analog signal receiver. Using this unique technique, Hall sensors can be utilized in voltage sensing and not be limited to magnetic field measurement or current sensing. Unlike capacitive data transmission that transmits common-mode noise (CMN), the coupling mechanism of Hall sensors is based on magnetic field and transmittance of the CMN noise is limited to parasitic capacitances, which further increases amplifier noise immunity. It also exhibits a better signal quality. The small size of the Hall sensor in the receiver circuitry, miniaturization of the magnetic field (MF) generator (i.e. on-chip coil), and lower consumption suggest that this approach could be utilized in readout circuits with multiple inputs. Unlike optocouplers that are not compatible with CMOS process, the proposed approach uses only two CMOS dice with no requirement for post processing. Finally, the reconfigurability feature suits the approach to be used in shunt-based current and differential voltage monitoring.

1.3 Research objectives and research work overview

The main objectives of this thesis are:

1. Proposing a first reported IA for voltage and shunt-based current sensing based on CMOS Hall-effect sensors.
2. Integrating a new Hall-based digital isolator for clock recovery circuit and showing its robustness by measuring the common-mode transient immunity (CMTI).

The specific objectives of the tasks are:

1. Optimizing sensitivity of cross-shaped Hall plates based on COMSOL simulation for maximized SNR.

2. Investigating system's isolation mode rejection (IMR) for HV surges and achieving isolation working voltage (V_{iso}) at the industrial standard level.
3. Minimizing power consumption and miniaturization of the design to be compatible for multi-channel isolated sensing with reduced packaging complexity and production costs.
4. Employing design and layout consideration to extend the bandwidth limit of AC Hall sensors.
5. Achieving the maximum possible signal quality from a single sensor.
6. Reconfigurability of the design for voltage and shunt-based current sensing as well as interfacing with ADCs with different input swing ranges.

1.4 List of publications

Journal paper:

Article 1: S. S. Mirfakhraei, Y. Audet, A. Hassan, and M. Sawan, "A Galvanic Isolated Amplifier Based on CMOS Integrated Hall-Effect Sensors", *IEEE Transactions on Circuits and Systems I: Regular Papers*, pp. 1-10, 2021, doi: 10.1109/TCSI.2021.3052476/

Article 2: S. S. Mirfakhraei, Y. Audet, A. Hassan, and M. Sawan, "A Small Footprint Digital Isolator based on CMOS Integrated Hall-effect Sensor", *IEEE* Journal of Sensors*: Regular Papers*, submitted (July 2021).

Article 3: S. S. Mirfakhraei, Y. Audet, A. Hassan, and M. Sawan, "A Fully Integrated Low-Power Hall-based Isolation Amplifier with IMR Greater than 120 dB", *IEEE Transactions on Circuits and Systems I: Regular Papers*, submitted (August 2021).

Conference proceedings:

S. S. Mirfakhraei, Y. Audet, M. Nabavi, B. Youness, M. Ali, A. Hassan, M. Sawan, "Wide Dynamic Range Front-End Programmable Isolation Amplifier using Integrated CMOS Hall Effect Sensor," in 2020 IEEE International Symposium on Circuits and Systems (ISCAS), Oct. 2020, pp. 1-5, doi: 10.1109/ISCAS45731.2020.9180574.

S. S. Mirfakhraei, Y. Audet, A. Hassan, M. Ali, M. Nabavi, and M. Sawan, "A CMOS MAGFET-Based Programmable Isolation Amplifier," in 2020 18th IEEE International New Circuits and

Systems Conference (NEWCAS), June 2020, pp. 9-13, doi: 10.1109/NEWCAS49341.2020.9159790.

1.5 Thesis outline

This Ph.D. thesis includes seven chapters. The first chapter (Introduction) discusses the motivation behind this research. The primary and specific objectives are presented in this chapter as well, in addition to the organization of the thesis and coherence of the articles with the research goals.

In chapter 2, we present a literature review of applications of isolation amplifiers and the developed arts or industrial products satisfying readout circuits. The advantages, challenges, and limitations of each technology are discussed in this chapter. This review introduces more specifically the problem formulation related to isolated data transfer devices in the integrated electronics.

Chapter 3 describes sections that are not reported as part of the articles toward the thesis. It describes considerations that are taken towards selecting among the available methodologies of sensor and coil implementation. Also, advantageous and disadvantages of possible approaches are verified by simulations.

Chapters 4, 5, and 6 include our three scientific articles. In the first article (chapter 4), we demonstrate a prototype showing the functionality of the idea with commercial products as well as integration of two sensors with their respective instrumentation amplifier (INA) in TSMC 65 nm technology. The linearity, step response, and signal quality of the design are measured, which verifies the design suitability for industrial applications.

In the second article (chapter 5), the first reported Hall-based digital isolator is developed to serve as clock recovery for the full system. Considerations towards preserving the bandwidth limit of the integrated CMOS Hall sensors are discussed. The digital isolator performances, including delay and bitrate as well as its robustness in presence of common mode noise, are measured.

In the third article (chapter 6), the full system integration and detailed design of each building block implemented in AMS 0.35 µm are presented. In this design, the signal quality of the system has been improved while power consumption is reduced. Isolation properties of the design including V_{iso} and IMR is discussed. Unlike the previous article (i.e. chapter 4) with an external miniature coil, in this fabrication, the integrated spiral coil generates the required MF which makes the design compact and allows multiple readback circuits to be fabricated using a single dice.

Finally, chapter 7 is general discussion and chapter 8 summarizes our contributions and achievements in this project. It also includes our recommendations to be taken for further improvements on the present design as well as our suggestions for the future direction of the current research.

1.6 Coherence of the articles with the research goals

This thesis follows the article-based format that includes papers produced as part of this Ph.D. research. Chapter 3 described simulation and design considerations that are taken towards selecting the sensor and coil. The proposed Hall-based IA is introduced in chapters 4, 5, and 6 including the device characterization, modeling, circuit design, validation, and implementation. Each one of the three chapters presents published or submitted research work. The articles are consistent with the research work in terms of complementarity and incrementality of the proposed contribution.

In the first article, validation of the proposed design is performed on TSMC 65 nm technology with minimal integration that includes a dual sensor with their respective INAs. The proposed idea involves several challenges in terms of sensor selection, bandwidth limit of the integrated Hall sensors, and magnetic field generation of coils. Optimization of the sensors' length and width toward maximum SNR is performed based on the sensitivity relation of the sensor. Sensor frequency response and nonlinearity error of the full amplifier circuit is measured. To generate the MF, a miniature coil is fabricated with a size that is suitable for packaging and glued on the chip.

As part of the fully integrated solution, in the second article, an isolated clock recovery with OOK modulation scheme is developed with the CMTI measurement setup and its test result. This is the first time that Hall sensors are utilized as a digital isolator, so design considerations for bandwidth preservation of CMOS Hall sensors as well as noise rejection analysis are described. The on-chip Tx coil diameter is the smallest among all inductive/capacitive digital isolators. Also, the miniature size of the Hall plate enables the receiver circuitry to be placed under the transmitter coil and next to the plate. This further minimizes the overall consumed chip area. Results that are not graphicly reported in this journal are included in the thesis appendix.

In the third article, a fully integrated solution is developed using AMS 0.35 µm technology. This is the first time that Hall sensors are being utilized in frequencies other than DC; therefore, in this integrated solution, the noise level of the Hall sensor pre-amplifier chain has been suppressed to an

adequate level to extract maximum SNR. COMSOL Multiphysics simulation is performed to further investigate and optimize sensors based on their contact size. The programmable gain amplifier (PGA) architecture is explained, and the dB-linear feature of the PGA is experimentally validated. The MF is generated using an integrated hexagonal spiral coil; therefore, as a final product, a PGA68 package containing driver and receiver dices is fabricated in AMS 0.35 µm that has no off-chip components. This proves the possibility of integration of multiple isolated readout circuits in a single package using only two dice. The article consists of the HV testing procedure and achieved amplifier's results including IMR, non-linearity error, and gain drift. The overall design has achieved an improved signal quality and reduced consumption due to integration. Clock recovery of the work is reported in the second article, and results that are not graphicly reported in this journal are included in the appendix section. The impact of clocking delay as well as duty cycle variation on the amplifier's output are also shown in the appendix section.

CHAPTER 2 LITERATURE REVIEW

2.1 High Common-Mode Voltage and Current Sensing

Applications such as power line monitoring and power system protection require current and voltage detection of the power line. These measurements take place in presence of a very high common-mode voltage and should satisfy industrial standards such as isolation working voltage (V_{iso}) of 600 Vrms, isolation mode rejection (IMR), and common-mode transient immunity (CMTI) of 10 $\frac{kV}{\mu s}$. Figure 2.1 shows available methodologies for high common-mode voltage power monitoring. These techniques are discussed in detail for the remaining of the review.

2.1.1 Isolation amplifiers

The main benefits of galvanic isolation are circuit protection, noise reduction, and high CMV operation, and CMN rejection, particularly those developed by ground loops. Signals with high common-mode or large spikes will damage electronics. An isolated amplifier is composed of two sides including an HV and an LV side. The HV side is directly connected to a sensing line and data is transmitted through an isolation barrier to the LV side. To prevent the ground loop, an isolated

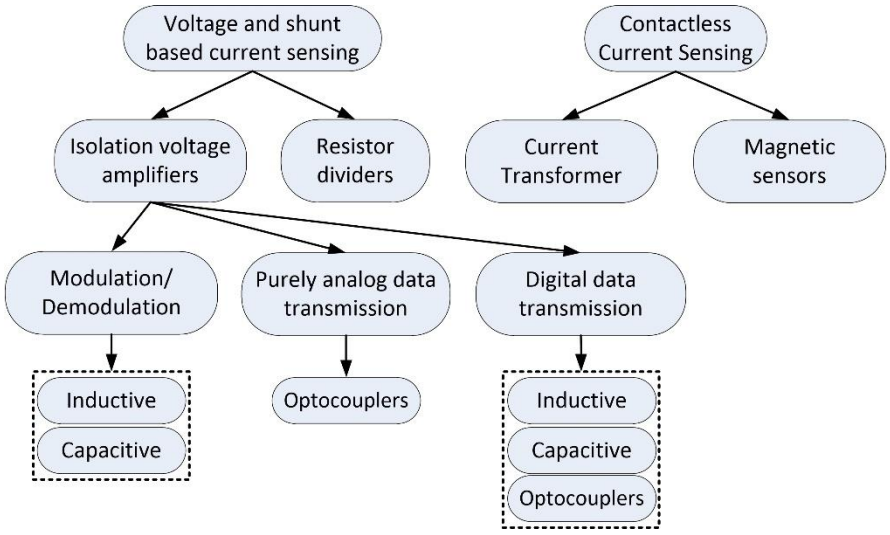


Figure 2.1 Voltage and current detection techniques in presence of high CMV

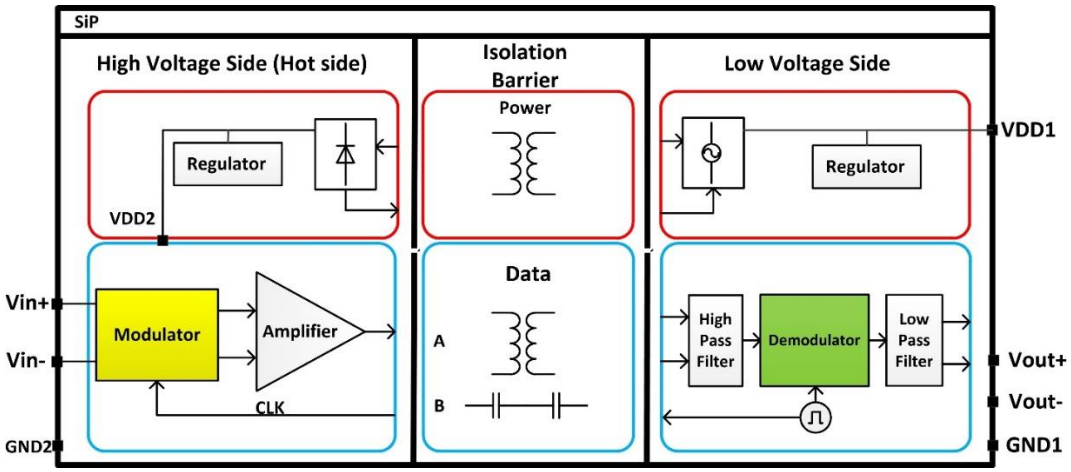


Figure 2.2 System in package solution of isolation amplifiers based on modulation techniques

DC-DC converter provides a floating supply for electronics on the HV side. The types of data transmission in isolated amplifiers divide them into two categories of analog transmission and digital isolator solutions.

2.1.1.1 Isolation amplifiers with analog data transmission

2.1.1.1.1 Isolation amplifier with modulation

The general architecture of the IAs with modulation and demodulation techniques is shown in Figure 2.2. The capacitive and inductive data links are the ones that so far are being employed in this approach.

Capacitive: Purely analog data transmission is a challenge for the capacitive link, as it transmits the HV side's CMN, ranging from 50 Hz to 400 Hz (supply noise) to 1.5 kHz of lightning strike noise [6]. Hence, the modulation technique is performed to separate the signal from the CMN, and the LV side's high pass filter (HPF) rejects the CMNs. So far, modulation schemes of pulse width modulation (PWM) [7] and amplitude modulation (AM) [8] are employed. Chopper modulation in the capacitive medium can be operated with no dedicated power supply on the HV side so it presents low power [9]; also, the capacitive galvanic barrier can be formed by process metal layers. This technique is highly useful in high-speed current sensing. Nevertheless, the analog capacitive data transfer suffers from a low resolution of 47 dB in 1 Hz bandwidth and transmittance of

CMN. To overcome this limit, PWM is employed [7]. The approach achieves an IMR of 140 dB and a very good nonlinearity error of 0.01%. Although the system has a better signal quality and supports power monitoring applications, it induces residual clock noise on the output signal.

Inductive medium: Mainly used for precision voltage and shunt-based current sensing and due to the four-terminal nature of the inductors, they exhibit very high IMR. As inductors can not transmit a DC signal, modulation is required to eliminate the need for bulky transformers. In contrast, achieving a good SNR in this technique imposes designers to employ a high-quality factor transformer, which is not possible on a millimeter scale, and leads to an enlarged overall design and huge power consumption of hundreds of milliwatts [8]. This makes them not suitable for multi-channel sensor interfaces. Few commercial products employing this technique are demonstrated in Table 2.1.

Table 2.1 Inductive isolation amplifier with analog data transmission available in market

	Modulation Frequency	BW (kHz)	Power	Package size in mm (X, Y, Z)	Product image
AD210	50 kHz	20	1.2W	(53,25,9)	
AD202/4	25 kHz	2-5	Min 75mW	(53.3,17.8,8.9)	
AD215	470 kHz	120	Min 1.2W	(54.6,8.3,21.4)	

2.1.1.1.2 Optocoupler

In optocoupler types of analog isolated amplifiers [10, 11] shown in Figure 2.3, while the input signal on D_1 generates a variable optical light intensity captured by the photodiode D_2, the emitted light through D_1 generates another current through D_3 that is fed back to the LED driver. Thus, nonlinearity of these photodiodes is canceled out through the feedback architecture. This is a very interesting alternative that eliminates clocking signal or carrier frequency; consequently, it removes

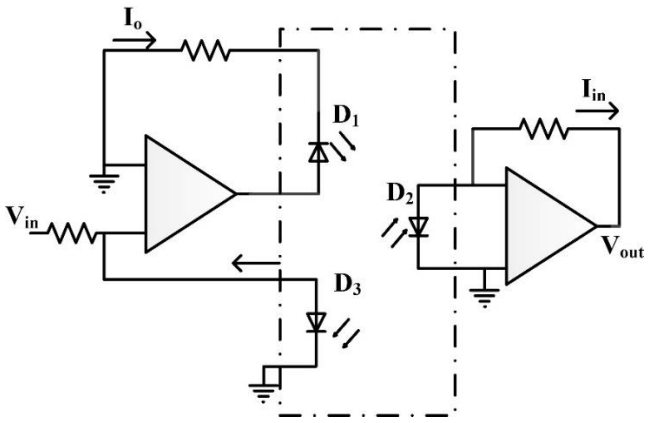


Figure 2.3 Analog isolation using optocouplers

the imposed clocking noises. Due to the optical nature of data transmission, this optocoupler isolator has a very high IMR, as there is no current leakage across the isolation barrier.

However, the current transfer ratio (CTR) $\frac{I_0}{I_{in}}$ is a parameter of all optocouplers that is weakened by their operating condition, electrical, and thermal stress [12]. Therefore, a linear relationship between the emitted light and the received photons as well as a long lifetime are the concerns in the optocoupler's type of isolation amplifiers. Furthermore, displacement damage subject to gamma radiation lowers the quantum efficiency of the optocouplers [13]. Finally, not compatible with the CMOS process, for every link an independent optocoupler dice is required which increases the total number of packaged dices in multichannel readout circuits and complicates packaging.

2.1.1.2 Digital-isolator-based amplifiers

Linearity of transmitted data over isolation barrier depends on common mode transient signal (i.e. surge) and frequency characteristic of the isolated barrier. Therefore, digitization is the most common way of data transmission that eliminates the nonlinearity error.

Figure 2.4 shows the overall architecture of all the digital isolation processes. First, a PGA adjusts the gain for the data converter stage. Then, an AAF filters signal to be prepared for the ADC. The two types of ADCs reported in literature and industry for this application are SAR [14] and sigma-delta modulator ($\sum\Delta$ ADC) [15, 16]. The digitized signal gets encoded using an available digital modulation technique and gets transmitted through the isolation barrier. In the receiver section, first, an HPF removes the supply and lightning strike noise. Then, the signal gets decoded.

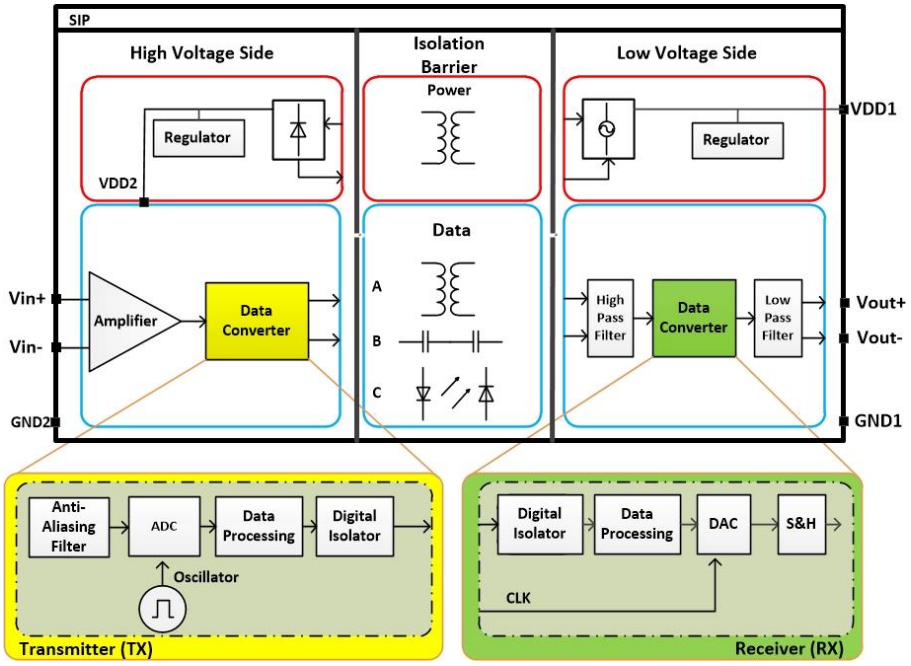


Figure 2.4 General architecture of an ADC-based isolation amplifier where digital isolator transmits the digitized serial data of the ADC and a DAC on the HV side reconstruct the analog signal

Finally, a DAC reconstructs the analog signal, and an analog filter generates the required output signal.

In all architectures of isolated amplifiers with digital data transfer or modulation/demodulation, clocking signals between the ADC and DAC or modulators and demodulators must be synchronized. As shown in Figure 2.4, for this purpose a separate channel is associated with transferring clock generated either in LV or HV side [14-16]. However, there are architectures in which the clock recovery is performed without a dedicated channel [17].

All types of isolation barriers including inductive [14, 15], capacitive [16], and optic [17] are used in digital data transmission. The robustness of the ADC-based isolation amplifiers in case of surge occurrence is measured by the CMTI of their digital isolators. Among the conventional isolation media, inductive link as a four-terminal device exhibits the most robust performance.

Sampling at the HV side allows high-resolution data to be transmitted to the LV side without being contaminated by imperfections of isolation barriers. However, an ADC alone can consume 100 mW of the HV side's power [14], which is not power effective. Also, the design covers a relatively large area for a single data link, and for a multi-channel readout circuit, it increases

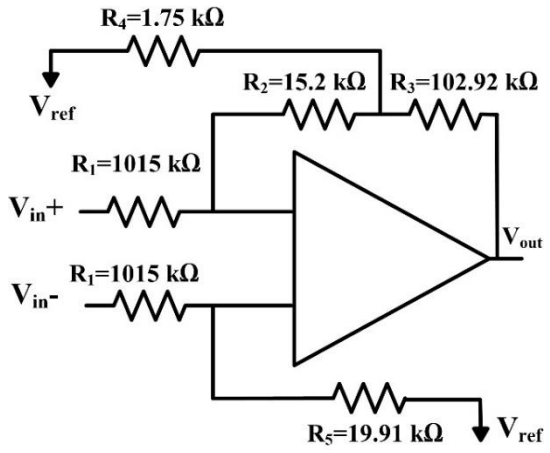


Figure 2.5 Internal divider architecture of AD8479 capable of tolerating 600 V of common-mode voltage

fabrication costs. Finally, modulation of power supply noise limits the amplifier linearity (resolution); therefore, during ADCs decision making time, the isolated power supply is halted to not contaminate the digitization process, which adds lots of complexity to the overall design.

2.1.1.3 RC Network

Figure 2.5 shows a high CMV resistive feedback amplifier topology designed for high CMV [18]. While not truly isolated, with lower cost and consumption, conventional resistor dividers allow these amplifiers to have high input impedance as well as high CMV. In resistive feedback configuration, the common-mode rejection ratio (CMRR) will be calculated as:

$$\mathrm{CMRR}=20\log((\mathrm{Gain}+1)\frac{100}{\%\mathrm{mismach}}) \qquad (2.1)$$

Therefore, to have a CMRR of 92 dB, these resistors must be laser trimmed to decrease their mismatch to 0.0025 %. Not only this process increases overall costs, but also it introduces additional capacitances on its dividers and feedback loop. Consequently, their CMRR is highly affected by the zeros located around 1 kHz in their common-mode gain. Also, these resistors must have a temperature coefficient (TC) of less than or equal to 3 ppm/°C [19].

Low signal quality is another drawback of divider architecture when being utilized in a shunt-based current sensing. Considering the unity gain high common-mode voltage amplifier of AD8479 [20],

Table 2.2 Comparison of industrial high CMV amplifiers suitable for voltage and current sensing

	Types		V_{iso} (kV)	CMRR (dB)	IMRR @60 Hz (dB)	CMTI $(\frac{kV}{\mu s})$	Input Noise $\left(\frac{nV}{\sqrt{Hz}}\right)$	Output Noise $\left(\frac{\mu V}{\sqrt{Hz}}\right)$	BW (kHz)	Power (mW)Total (HV/LV)
[7]	Analog	Capacitive	1.5	-	140	-	6	56	50	45-180
[8]		Inductive	1.5	100	120	-	20	-	120	870
[21]		Optic (1)	4.42	130	-	-	-	-	200	15<
[18]	Resistor dividers (Not isolated)		0.6	90		-	1600	-	310 (Gain = 1)	1.4-10.8
[22]	Digital	Capacitive	0.6	108	-	15	-	12.9	60	(27/22)
(1) The provided data is only for the optocoupler and does not include drivers. The blank parameters are defined by the added drivers.										

for a 100 mA of current using 0.1 Ω of resistance, amplifier output will be 10 mV while according to the product datasheet, it has 1.6 $\frac{\mu V}{\sqrt{Hz}}$ of input thermal noise. Therefore, the amplifier will have 75.9 dB of SNR in 1 Hz bandwidth which is not sufficient for many applications.

Capacitive coupling is another class of RC network mainly employed as instrumentation amplifier in biopotential signals acquisition that can sustain high CMV as input capacitors isolates the amplifier; however, they block DC signal, and they are not considered in this review. Table 2.2 provides a summary and comparison between important parameters of amplifiers capable of tolerating high CMV.

2.1.2 Contactless Current Monitoring

2.1.2.1 Current Transformer Based Solutions

The current transformer (CT) solution is a current measurement technique that converts the HV side current in the primary to a much lower current in the secondary (Figure 2.6). Then, this current will be converted to a voltage and undergoes further signal processing. Therefore, CT performs both signal scaling and isolation purposes. Also, CT can have a large output magnitude; therefore,

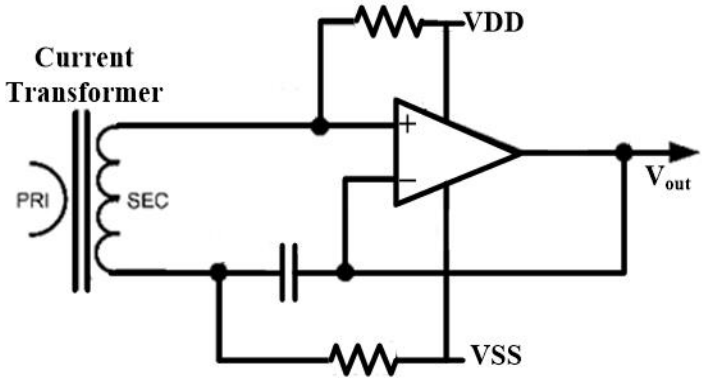


Figure 2.6 Typical CT-based current sensing

precise measurement can be performed. There exist other techniques including Rogowski coil and search coil that can be categorized as CT-based current sensing. A Rogowski coil, unlike a search coil, is equipped with ferrite or metal inside the airgap to increase the sensitivity of the coil with magnetic fluctuations and can detect smaller currents. However, this technique is limited to sensing only AC currents. A high DC magnetic field generated by DC current [23] can saturate the coil and sense DC signal, the transformer size becomes extremely bulky. Finally, frequency-dependent phase shift which is the coil's inherent feature needs to be corrected.

2.1.2.2 Magnetic Current Sensors

Discovered by Edwin Hall in 1879, they have been widely used in current and position sensors, magnetic fields, and speed measurements. When a thin conductive film is subjected to a magnetic field, it generates a voltage. This is shown in eq. (2.2):

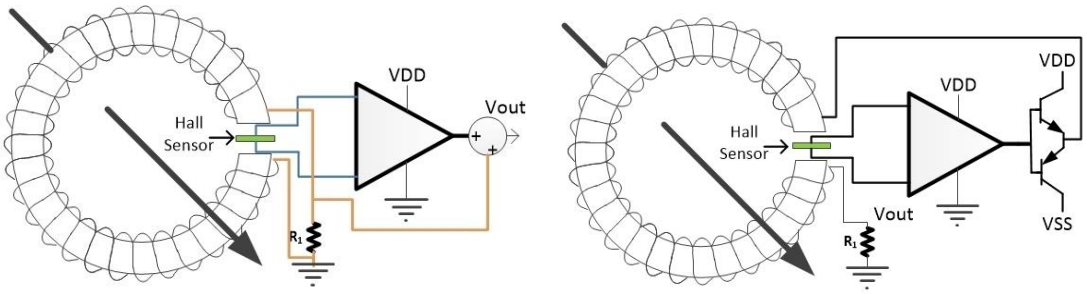
$$V_{Hall} = S_I IB \tag{2.2}$$

where 'I' is the biasing current, B is the perpendicular magnetic field, and S_I is the sensitivity of the Hall plate. Based on eq. (2.2), the generated voltage is linearly proportional to the magnetic field which is representative of an analog signal.

Although the performance of these Hall sensors varies between different designs, linearity [24] as well as sensing both DC and AC are the advantages of such sensors. Also, unlike the CT solution that introduces an inductive effect on the primary side or shunt sensing that adds resistivity to the sensing line, the direct sensing of Hall sensors does not introduce any distortion in sensing lines.

However, commercially available products, normally have a limited bandwidth of 20kHz [25, 26]. Melexis MLX91208 and Allegro A3163 known as wideband sensors have bandwidths of 250kHz and 120kHz [27, 28], respectively, while literature reported integrated and special process 2DEG quantum well Hall elements (QWHE) have a bandwidth of 1MHz and above [29-32]. To overcome the bandwidth limit, Figure 2.7 (a-b) combines the output of a magnetic sensor and a CT to achieve a wide bandwidth current measurement [33]. Here the Hall sensor is responsible for low frequency (LF) measurements and CT is responsible for high frequency (HF) current measurement. The added magnetic concentrator also increases flux density, which increases sensor sensitivity and lowers sensitivity toward external magnetic fields. The magnetic core in Figure 2.7 (a) can permanently be saturated due to high current and causing an absolute error of above 1% [33]. To compensate for the effect known as magnetic offset, output of Hall sensor in Figure 2.7 (b) act as error signal to generate an opposing flux. The technique greatly reduces thermal drift and make the linearity independent of magnetic flux. Although the combined Hall current sensor with CT solution demonstrates good resolution, linearity, and bandwidth, the final product is bulky in comparison with the traditional analog isolation amplifier and is limited for current monitoring. The other disadvantage is that for higher sensing currents, more power is required to compensate the saturated flux.

There are state-of-the-art and industrial Hall sensors where the sensor is placed on top of a shunt of current [28, 34] or a high current is diverted into the package [35, 36] and the magnetic field created by this high current is being sensed (Figure 2.8). However, their usage is limited for high current applications, and yet, similar to all the magnetic sensors, they are limited to current sensing.



(a) (b)

Figure 2.7 Combined Hall sensor with CT based solution: (a) open-loop implementation, and (b) closed-loop architecture to eliminate flux saturation

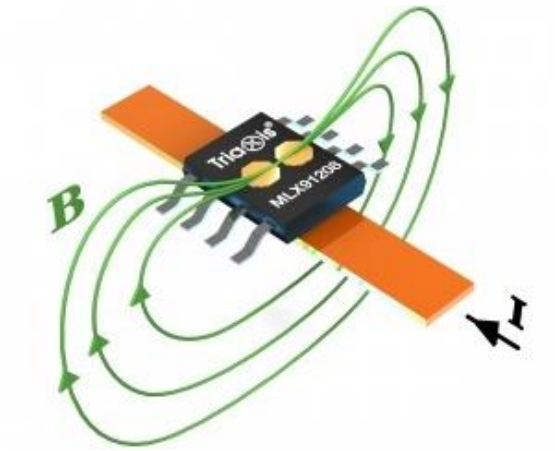


Figure 2.8 Open-loop current measurement using a magnetic field sensor that directly measures the field around a current-carrying conductor (MLX912018)

CHAPTER 3 METHODOLOGY

This thesis proposes a voltage isolation amplifier based on Hall effect sensor. A simplified architecture of the design is shown in Figure 3.1. A transmitter (Tx) drives a coil placed on top of Hall plate. Then, the generated magnetic field induces a deflecting voltage in the Hall plate, and the receiver circuitry processes the signal.

This chapter describes the methodology, simulations, and challenges involved toward the sensor and the coil selection. After defining the type of sensor and coil, their designs as well as Tx/Rx circuitries are explained explicitly in the following chapters.

3.1 Hall Effect Sensors

3.1.1 Sensitivity

So far, magneto-resistors (MR) including giant magneto-resistors GMR, anisotropic magneto-resistors (AMR), and tunnel magneto-resistors (TMR) [31, 37], Hall elements, fluxgates, and magneto inductances are the existing types of magnetic effects. All magnetic sensors can be utilized in applications where switching and comparison are required such as position sensors. In Hall sensors, which works based on Lorentz force, magnetic field sensitivity is perpendicular to biasing current. Magneto resistors are sensitive to the horizontal field and the resistivity of the sensor changes due to the applied field. The open-loop current sensor of MLX912018 (Figure 2.8) is an example of their application. Although in comparison with Hall sensors, magneto-resistors exhibit better sensitivity, in this thesis, Hall sensors are studied as they are sensitive to perpendicular MF.

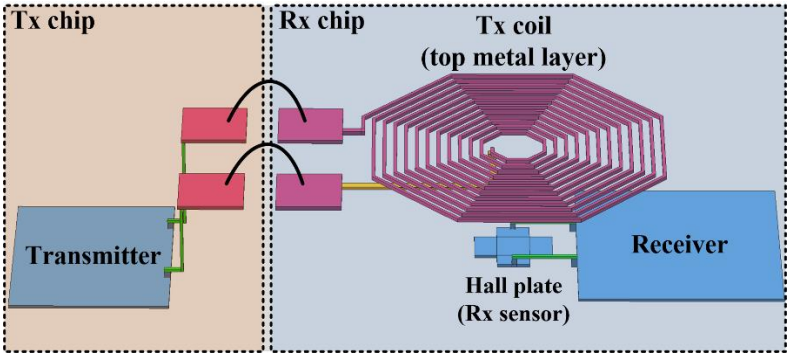


Figure 3.1 General architecture of the Hall-based isolator

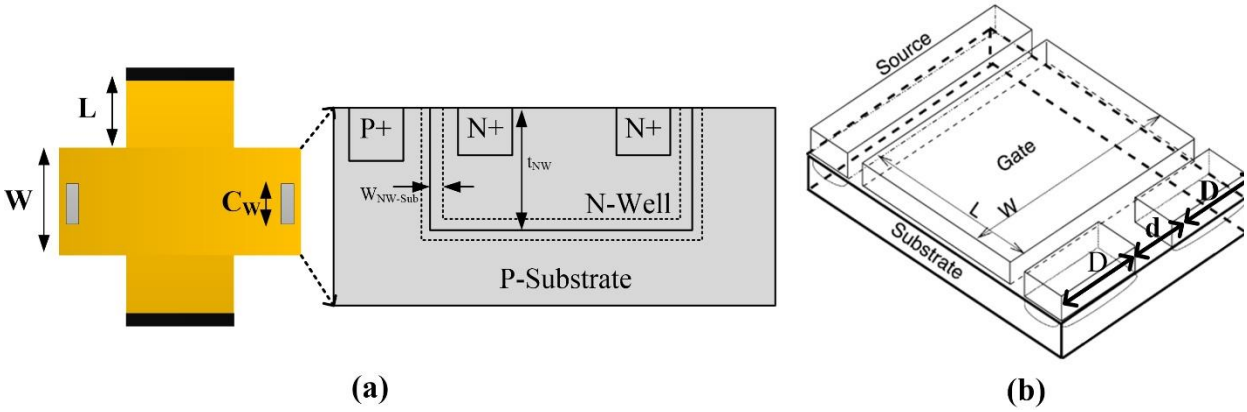


Figure 3.2 CMOS implementation of (a) cross-shaped Hall plate, and (b) MAGFET [38]

There exist two types of CMOS Hall sensors as shown in Figure 3.2, namely Hall plates and MAGFETs. A Hall plate is biased by a fixed current and generates a differential signal in form of voltage. MAGFETs are similar to normal transistors that have their drains/sources split in two [39], three [38], or more [40].

Sensitivity is a parameter measuring the effectiveness of Hall plates and is typically very low in silicon. This is defined as follows [41]:

$$S_I = \frac{G\, r_H(T)}{n(T)q(t_{NW}(T) - W_{NW-sub})} \tag{3.1}$$

$$G = 1 - 5.0267 \frac{\Theta}{\tan\Theta} e^{-\frac{\pi(W+2L)}{2\ W}} \tag{3.2}$$

Here, G is a geometric factor, r_H is the Hall coefficient, n is the doping concentration, T is the temperature in Kelvin, and t_{NW} is the N-Well thickness, and $W_{NW\text{-}Sub}$ is the depletion region between the N-Well and the substrate. As an important parameter, G depends on the ratio $\frac{L}{W}$ and the angle of the Hall plate Θ. As explicitly shown in [42], the increase in the plate size as well as the increase in $\frac{L}{W}$ will increase the current sensitivity. Also, following eq. (3.1), any decrease in effective thickness t_{NW} and doping level of Hall plate active layer increases the sensitivity. Usage of group 3 and 5 heterostructure Hall devices are becoming more popular because of their higher

sensitivity [43]. An ultra-sensitive Hall plate called 2DEG QWHE sensors using GaAs–InGaAs–AlGaAs with a minimum detectable field of 20 nT is an example of these heterostructure Hall devices [29]. Finally, the sensitivity can be improved by using magnetic concentrators [44] and increasing biasing current/voltage.

MAGFETs' sensitivity is calculated as follows [45]:

$$S_{MAGFET} = \mu_S \frac{L}{D + \frac{d}{2}} \tag{3.3}$$

where "L" is the effective length of differential pair, μ_S is the effective surface electron mobility, and "d" is the gap between drains, and "D" is the width of drains (Figure 3.2). Process surface electron mobility is given by:

$$\mu_s = \frac{\mu_r}{(1 + \frac{V_{gs}-V_{th}}{F1\ t_{ox}} + \frac{V_{ds}}{F3\ L_{eff}})} \tag{3.4}$$

Here, t_{ox} is the oxide thickness, F1 and F3 are the mobility attenuation factors, which is technology dependent, and μ_r is the low field mobility. The μ_r is given by the product of the effective surface mobility of the carriers in the inversion layer (μ_n) and the Hall scattering factor (r_H). In this case, one of the limiting factors for achieving high sensitivity silicon magnetic sensors is the relatively low silicon mobility [40], so using a semiconductor with higher mobility like Silicon on Isolation (SoI) can increase the sensitivity. The mobility equation shows that small-scaled technologies (lowering t_{ox}) results in lower μ_s and decreased sensitivity. Increasing L_{eff} can contribute to rise the μ_s while it also increases S_{MAGFET}. It was first shown by Kluge et al. [46] that narrowing drain contacts of MAGFETs increases their sensitivity, and the optimized shape called sectorial MAGFETs has the highest sensitivity[40].

3.1.2 Noise in Hall sensors

The output sensed voltage of a Hall plate is defined as:

$$V_{Out} = V_{Hall} + V_{offset+flicker} + V_{th} + V_{shot} + V_{GR} \tag{3.5}$$

where $V_{offset+flicker}$ is the Hall offset and flicker noise, V_{th} is the thermal noise, V_{shot} is the shot noise, V_{GNR} is the Generation-Recombination noise. Figure 3.3 demonstrates the spectral density behavior of these noises.

Flicker noise, Generation-Recombination, and offset

Flicker noise is conductivity modulating noise and generation-recombination (GR) noise is a result of the fluctuation in the number of quasi-free carriers in a device [47]. Flicker noise and GR have $\frac{1}{f}$ and $\frac{1}{f^2}$ decaying characteristics, respectively. More details on these noises can be found in [47].

At zero magnetic field, the voltage/current offset generated by misalignment, nonuniformity of dopant, and thermal drift appear at the output. This offset can be ameliorated by adding the current spinning or connection-commutation technique [48, 49] on the output side of the sensor and chopper amplifiers to remove the amplifier's offset. The current spinning is originally implemented to reduce the offset of silicon-based Hall sensor (SBHS) [50]. As shown in Figure 3.4, biasing current and sensing nodes are periodically switched in 90° [51] or 180° [52] rotations; consequently, offset is evenly distributed between amplifier nodes. Using this technique, large offsets of SBHS ranging from mT to tens of mT are decreased in a range of micro-Tesla. QWHS has an inherently lower offset, and by using the clock spinning technique, a very low offset of 20 nT is reported in the literature [49].

The four-phase clocking technique employed in the cross-shaped Hall sensor not only reduces DC offset but also decreases flicker noise and GR. Considering the corner frequency of these noises,

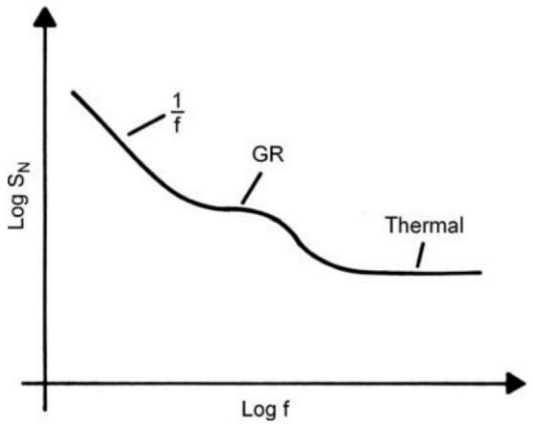


Figure 3.3 A typical noise spectrum in a Hall device [47]

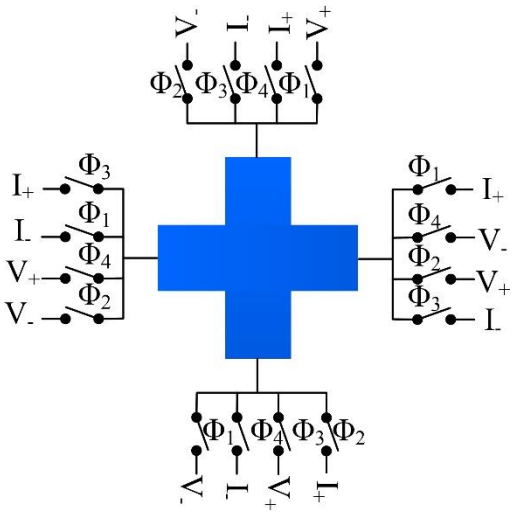


Figure 3.4 Clock spinning for DC offset cancellation

the right frequency can be selected for the four-phase clocking signal to smoothen the flicker noise [49]. The clock-spinning comes with two main disadvantages. First, the presence of transistor switches of clock spinning and chopper amplifier adds resistor between Hall plate and amplifier, which increase thermal noise and decrease sensitivity. Second, it introduces voltage spikes (ripples) at the output of the amplifier.

If Hall sensors are used for low field magnetic sensing in the range of μT and nT, the effect of earth magnetic field, also known as geomagnetic field, shall be considered. Depending on the geographical location of the sensor, the geomagnetic field ranges from 25 to 65 μT [53] which is in the sensing range of the Hall sensor. Therefore, the sensor must be calibrated depending on its location. Also, external magnetic noise such as the supply noise of wires can perturb the accuracy of the device. These drawbacks make them not suitable for mobile applications, including airplanes, where the sensor faces geomagnetic field variation.

Shot and thermal noise

Due to the resistive nature of the substrate on which a magnetic sensor of any kind including MAGFET and cross shape Hall plate being implemented, shot and thermal noise always exist. These noises are defined as:

$$I_s = \sqrt{2\, q\, I_{DC}} \tag{3.6}$$

$$I_t = \sqrt{\frac{4\, k_B\, T}{R}} \tag{3.7}$$

where I_s is shot noise, q is the electron charge, I_{DC} is biasing current, I_t is thermal current noise, k_B is Boltzmann constant, R is the channel resistance, and T is temperature. To investigate the impact of these noises and choose the right choice of sensor configuration between voltage and current mode, an analysis needs to be performed. Figure 3.5 (a-b) shows examples of magnetic sensors operating in current mode. SNR formula in current mode sensitivity for 1 Hz bandwidth will be calculated as:

$$SNR_I = 20 \log\left(\frac{S_{M/H}\, I_{DC}\, B}{I_S + I_t}\right) \tag{3.8}$$

where $S_{M/H}$ is the MAGFET or current mode Hall sensitivity and B is the perpendicular magnetic field. Assuming that the typical sensitivity value of MAGFETs operating at saturation mode at room temperature is 3.67 $\frac{\%}{T}$ [38] for 125 µm of length and 80 µm of width (Figure 3.5 (a)). For 1 mA of I_{DC} and 1 mT of B, 66.235 dB of SNR is expected.

The SNR formula for 1 Hz bandwidth of CMOS cross-shaped Hall effect sensors operating in voltage mode is:

$$SNR_V = 20 \log\left(\frac{S_I\, I_{DC}\, B}{V_S + V_t}\right) \tag{3.9}$$

where S_I is current related sensitivity, V_S is shot voltage noise, and V_t is thermal voltage noise. Typical CMOS Hall voltage sensitivity is 0.032 $\frac{V}{mA \times T}$ [54] and typical n-diffusion sheet resistance of 1 $\frac{k\Omega}{sq}$ is expected from a fabrication process. Shot noise appears either as a common mode signal or differential signal at voltage nodes of the sensor. The differential shot noise is negligible as a very low leakage current is passing through the gates of differential pairs that are connected to voltage nodes. Preamplifier's CMRR can attenuate the common mode shot noise, which is in the range of 17 $\frac{nV}{\sqrt{Hz}}$ signal. An amplifier with 40 dB of the CMRR attenuates the common mode noise

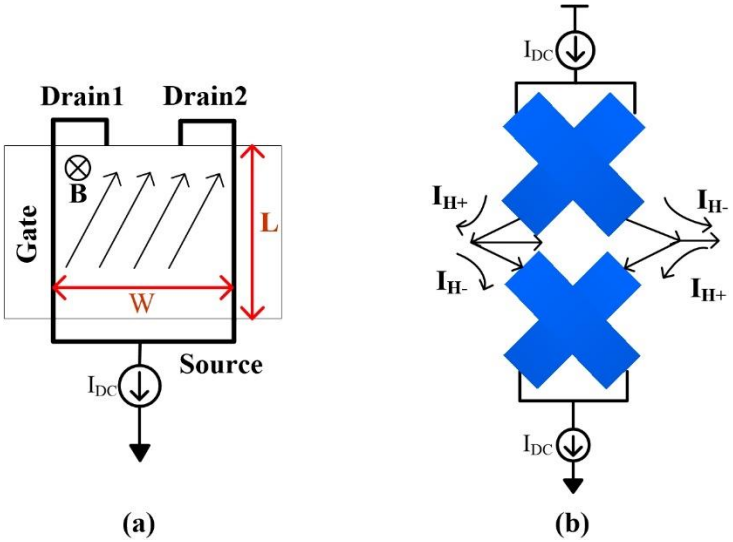


Figure 3.5 Magnetic sensors operating in current mode: (a) MAGFET and (b) cross shape Hall plate configured to operate in current mode

resulting from shot noise down to 0.17 $\frac{nV}{\sqrt{Hz}}$ and leaving the thermal noise as the dominant source of the noise. For the same 1 mA of I_{DC} and 1 mT of B, 78 dB of SNR is expected.

In case of Figure 3.5 (b) where the Hall sensor is biased in current mode [48], equation (3.8) is still valid. For purpose of comparison, the reported 1660 $\frac{V}{mA \times T}$ sensitivity [48] is divided by 109 dB of the designed amplifier's gain to obtain the combined sensors' *true* sensitivity that is 0.006 $\frac{V}{mA \times T}$. Therefore, for the 1mA of current, magnetic field of 1 mT, and Hall plate resistivity of $1\frac{k\Omega}{sq}$, 64 dB of SNR is expected by the Hall sensors operating in current mode.

A cascode stage can simply amplify MAGFET's signal; however as stated above, Hall plates have a better limit of detection [55]. Therefore, in this study, cross-shaped Hall plates are being utilized for the receiver element.

3.1.3 Temperature consideration

By taking derivative of the Hall plates sensitivity of eq. (3.1) with respect to temperature, the sensor temperature coefficient (TC) can be calculated as:

$$\alpha_{S_I} = \alpha_{r_H} - \alpha_n - \alpha_{teff} \tag{3.10}$$

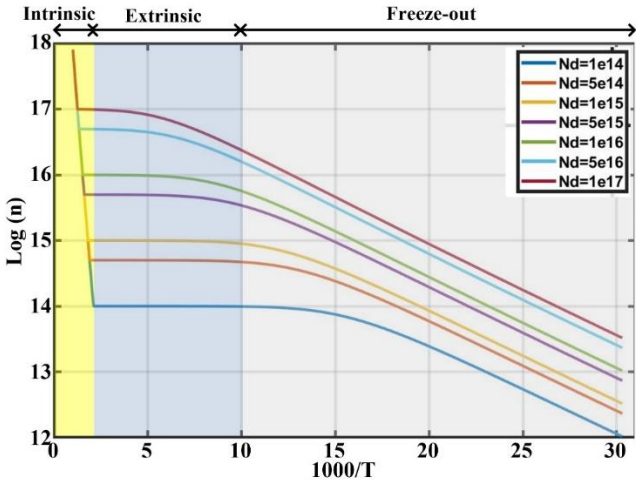


Figure 3.6 Carrier concentration respective with reciprocal temperature for different donner impurity concentrations

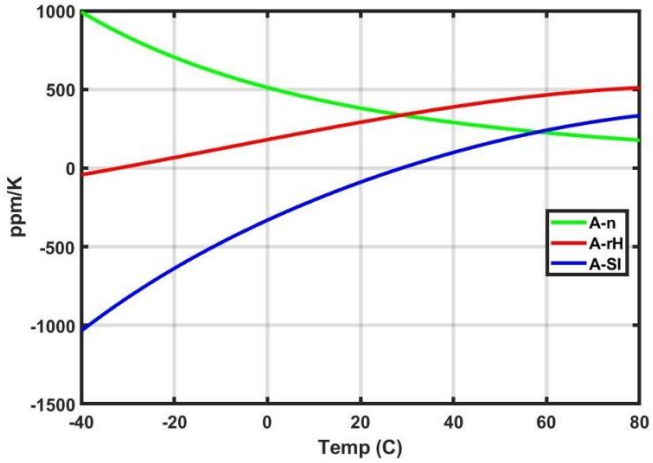


Figure 3.7 Temperature coefficient of r_H, n, and S_I are calculated for a process with $10^{17}cm^{-3}$ of doping impurity

where TC of the Hall coefficient, carrier concentration, and N-Well effective thickness are abbreviated as α_{r_H}, α_n, and α_{teff}. Using methodologies described by Paun et al. [56], the α_n of different doping concentration (N_d) are plotted in Figure 3.6. In the freeze-out region, the electron-hole pair is negligible and doner electrons are bound by the donor atoms, and in the intrinsic region carrier concentration increase with temperature. Temperature variation in the extrinsic region does not significantly vary the carrier concentration. It can be seen from the graph that technologies with lower N_d have an extended extrinsic region or lower temperature drift in the industrial temperature range.

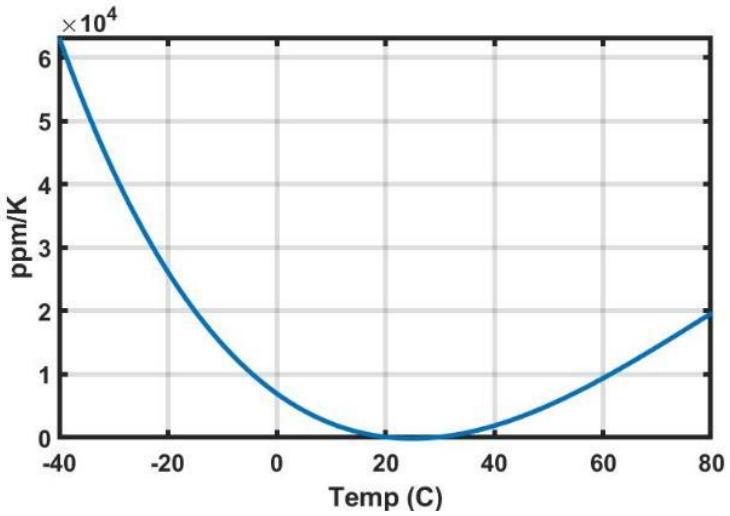


Figure 3.8 The calculated relative variation of the sensitivity related to the value at 300 K for a zero-stress mounting (silicon glue)

The α_{teff} depends on the packaging thermal expansion factor and in ceramic packaging with silicon glue (zero-stress mounting) the TC is considered null [57]. α_{r_H} is depicted from measurement results reported by Popoviū [58]. Based on these parameters, α_{S_l} for a process with N_d of $10^{17}cm^{-3}$ is calculated as shown in Figure 3.7. It can be depicted that the α_{S_l} has a zero-temperature drift at 27°. The overall sensitivity drift is demonstrated in Figure 3.8.

Knowing this response, active adjustment of the sensor's biasing current is a common practice to lower the drift. Also, Ajbl, et al. [51] introduced a novel active compensation approach based on an integrated coil that generates a reference magnetic field, and they could obtain 1% drift over the industrial temperature range.

3.2 Magnetic coil

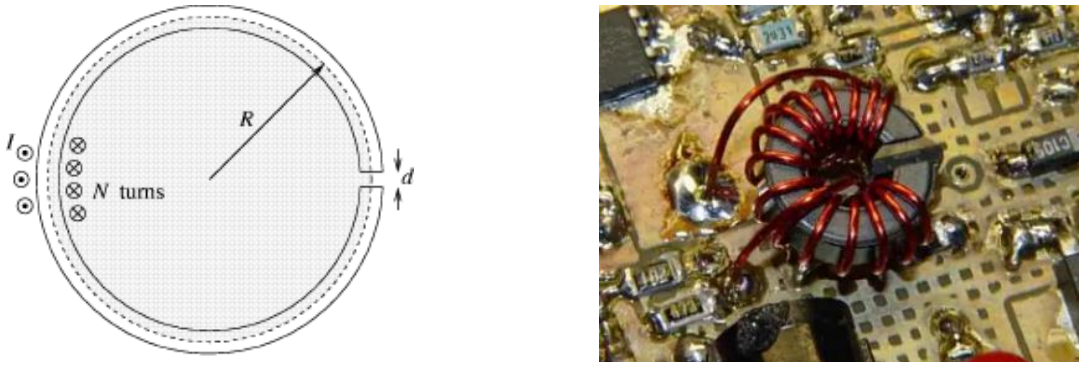
In magnetic current sensors, the strength of MF determines signal resolution, and for the purpose of this thesis, various means of MF generation are investigated.

In a C-shape toroid, shown in Figure 3.9 (a), a high permeability ferromagnet is surrounded by windings to generate high MF. The sensor is placed inside the toroidal airgap. C-Shape toroids are widely used in clamped current sensors [33] as they can create a strong uniform magnetic field. The flux inside the air gap is:

$$B = \frac{\mu_0 N I}{\frac{2\pi R}{\mu_r} + d} \tag{3.11}$$

where μ_0 is the magnetic permeability of free space, μ_r is the relative permeability of the toroid, "I" is the winding current, "N" is the number of turns, "R" is toroid radius, and "d" is toroid airgap as shown in Figure 3.9 (a). Following equation eq. (3.11), MF is significantly reduced due to the demagnetization of the air gap. To lower the air loss of magnetic field, the "R" and "d" of the toroid must be minimal. Unfortunately, ferrite material suffers from permeability change against variation in flux density. Another drawback is low μ_r of the ferrite rods for HF applications. An example of the implementation is shown in Figure 3.9 (b). An ANSYS Maxwell simulation is performed on the smallest commercially available toroid to determine inductance and MF generated inside the air gap for low current applications. In this simulation "R" is 1.65 mm, "N" is 93 turns, "I" is 5 mA, and "d" is 0.5 mm (Figure 3.10). Based on the simulation, the toroid has a magnetic field of 1 mT and a high inductance of 100 µH. However, due to the small size of the toroid and the small size of the airgap where sensor is placed, the toroid winding and chip wire bonding become a complicated process; so, fabrication and assembly costs increase.

Solenoids in the form of a miniature coil with a ferrite rod inside the air gap is another approach that can generate a reasonable magnetic field while the small footprint allows the approach to be packageable. The minimum diameter of commercially available RFID is 1 mm, so we designed a solenoid that fits this RFID. For 2 mA of current, the approach generates 2.5 mT of MF. This is explicitly explained in our work [59]. Although, the addition of the RFID rod inside the air gap increases the magnetic field at the cost of adding inductance, which is not suitable for higher modulation frequencies. Also, the coil increases the overall packaging area and cost. With no ferrite rod inside, with the same coil current, to achieve the same magnetic field, we could push the solenoid design to the limitation of industrial winding machines which is 30 µm of wire width (AWG 48) and inner diameter of 0.8 mm. This would decrease the inductance by 30% and significantly reduce the solenoid size to 1.2x1.2 mm^2. Finally, further miniaturization of the coil increases its manufacturing cost as specialized and very limited tooling machines exist for 10 µm wire sizes and inner diameters smaller than 0.1 mm. Also, engineering fees significantly increase.



(a) (b)

Figure 3.9 (a) Cross-section of a C-shape toroid, and (b) an example of implementation of a C-shape toroid [60]

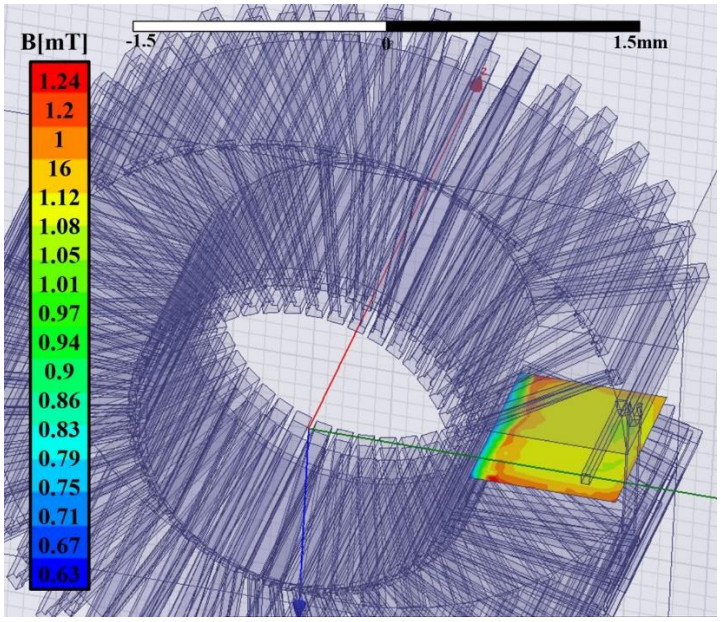


Figure 3.10 ANSYS simulation of a C shape toroid with 1.65 mm of radius showing the MF density at the air gap

As part of this thesis, the CMOS integrated spiral coils have been investigated. The thickness of the oxide layers from the top metal down to the substrate with respect to the diameter of the spiral coils is negligible. The central magnetic field of the stacked spiral coils can be calculated as:

$$B=MN\mu I\frac{\ln(\frac{D_o}{D_i})}{(D_o-D_i)} \tag{3.12}$$

where M is the number of used metal layers, N is the number of turns, I is the current, D_0 and D_I are the outer and inner diameters of spiral coils. These parameters are shown in Figure 3.11(a). The inductance of a single layer of the spiral coil will be calculated as:

$$L(\mu H)=\frac{r^2\ A^2}{30A\text{-}11D_i} \tag{3.13}$$

$$A=(D_i+N\ (d+S))/2 \tag{3.14}$$

For multi-layer spirals, considering inductors' mutual coupling, the overall inductance will be calculated as:

$$L=L_1+L_2+L_3...\pm 2M_{12}\pm 2M_{13}\pm 2M_{23} \tag{3.15}$$

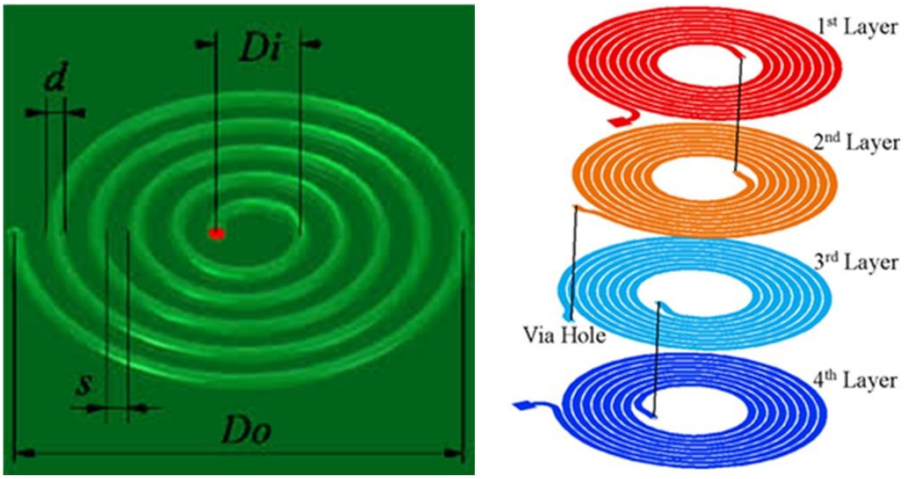
$$L=L_1+L_2+L_3...\pm 2K_{12}\sqrt{L_1\ L_2}\pm 2\sqrt{L_1\ L_3}\pm 2\sqrt{L_2\ L_3} \tag{3.16}$$

where S is the distance between windings, d is the wire diameter, and M_{ij} and K_{ij} are the mutual inductance and mutual coupling between i^{th} and j^{th} layer, respectively. Following the above equations, due to very small D_0 and small wire width, this approach is the smallest footprint with no packaging complexity that generates relatively high MF with a low inductance of nano Henry. To verify this hypothesis, ANSYS simulation shown in Figure 3.11(b) is performed for an integrated coil with a current of 1 mA, 5 metal layers of TSMC 65nm process, 21 turns, 0.5 µm wire spacing, 2 µm wire width, and 15 µm of D_0.

Despite these advantages, there is a trade-off between maximizing the field and maximum current density of the coil which limits the maximum MF. Moreover, there is always a limitation in the maximum isolation working voltage of IAs using multi-layer integrated spiral coils. SiO_2 is intermetal filling of the fabrication process including AMS 0.35 µm technology; it has a mean time to failure (MTTF) of 450 kV/mm [61] for 20 years of life time.

To elimination the thickness dependency and limit of isolation voltage to the intermetal filling thickness, we propose the flip-chip solution of Figure 3.12, such that all metal layers of one chip

(a)



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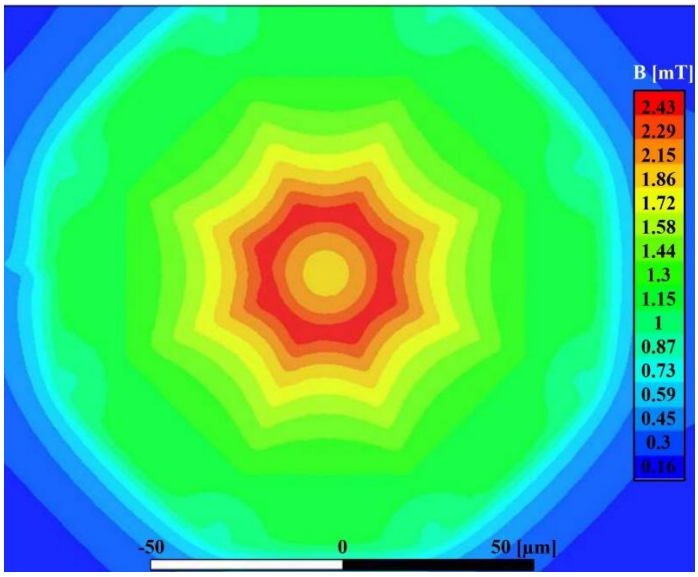


Figure 3.11 (a) CMOS integrated spiral coil configuration [62], and (b) ANSYS modeling and simulation of an integrated spiral coil implemented in a 65nm process with 1mA of current

are solely being used for the coil that is being placed on top of the sensor chip. In this way, the dual isolation barrier called reinforced isolation, which is a combination of SiO_2 barrier and the added polyimide layer and can satisfy 5kV galvanic isolation. ANSYS simulation of a 0.6x0.6 mm^2 coil using all four metal layers of AMS 0.35 µm technology in a square configuration, with 5 µm thick and 5 mA of current, is shown in Figure 3.13 (b) and achieves an inductance of 9 µH. One limitation of the proposed idea is the high thickness of the dice substrate. AMS 0.35 µm

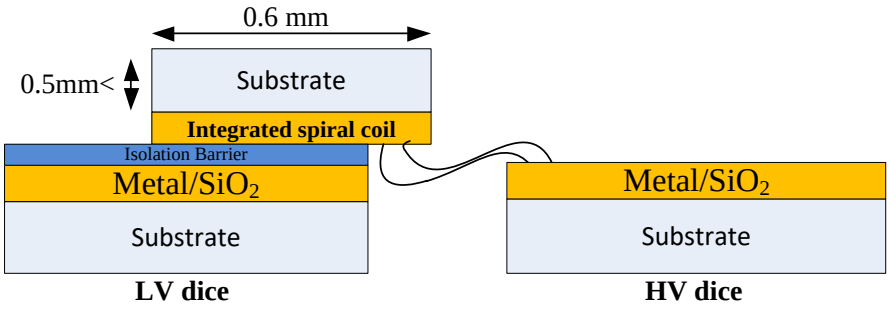
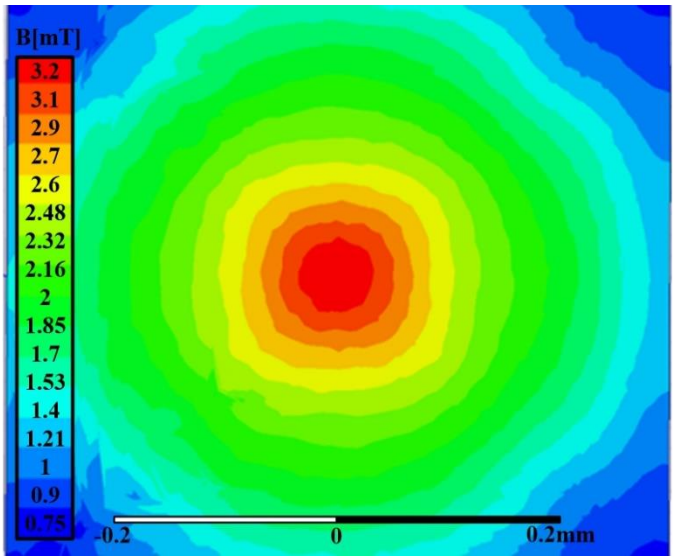


Figure 3.12 Side view of the flipped chip solution; here, the top left chip is the dice dedicated for the spiral coil

(a)



(b)

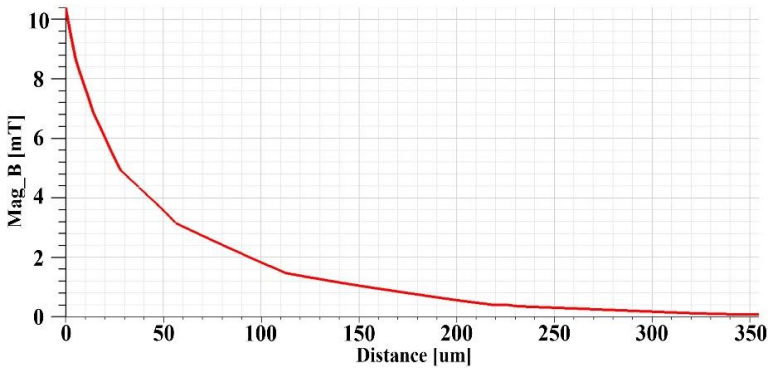


Figure 3.13 ANSYS modeling and simulation of (a) a planner field at 50 µm from the sensor's surface using integrated spiral coils implemented in the AMS 0.35 µm process, and (b) field attenuation respective with the axial distance

Table 3.1 Comparison of MF generating techniques

#	Technique	Field strength	Inductance	Practicality(1)	OD (mm)
1	C shape toroid	~1.23	100u	--	NA
2	Solenoid with ferrite rod inside	~1.5	200u	-	1.9
3	Solenoid with NO ferrite rod inside	~1.3	100u	+	0.9
4	Solenoid with sensor inside	~1	1m	+	4
5	Integrated Coil	~1.5	20n	++	0.25
6	Flipped chip Integrated Coil	~3	9u	+	0.8

(1) Any post processing or proprietary process, special packaging, special wire bonding techniques that increase the assembly cost, and off-chip integration reduces the practicality of the coil.

and TSMC 65 nm have 710 µm and 240 µm of thickness, which drastically decreases the MF as shown in Figure 3.13 (b); therefore, the chip needs to be flipped and soldered to the driver side which increases packaging cost (Figure 3.12). The MF is perpendicular at the center of the coil and Hall plates are only sensitive to vertical MF, so perfect alignment of coil dice and Hall sensor is required to fully capture all the created MF. The coil itself consumes 0.6x0.6 $mm^2$and further increasing the coil size does not have a significant effect on the perpendicular magnetic field; however, in post-fabrication steps, cutting the silicon plate for sizes smaller than 1x1 mm^2 is a challenging and costly process that should be taken into consideration. A summary of the available methodologies is provided in Table 3.1.

Limitation of available commercial IAs were discussed in section 2.1. This includes not only large area and high-power consumption that prevent the IAs from dense integration, but also short lifetime, low resolution, and limitation to current sensing. To overcome these drawbacks, we proposed to integrate magnetic sensors in IAs as the signal receiver. Among the various discussed magnetic sensors in section 2.2, CMOS Hall-effect sensors were depicted, as they do not require any post-processing like implementation of ferrite material in GMR/TMR. Also, they are sensitive to vertical magnetic field, and compatible with CMOS processes. To generate a high magnetic field, several scenarios were modeled by ANSYS simulation in section 2.3, and finally, the

integrated spiral coils were selected which further reduces the final cost due to no requirement of any special packaging and allows multichannel isolated sensing using only two dices.

3.3 Simulation tools

Schematic design and post-layout verification were challenging tasks. First, this is due to the absence of an EMI tool in Cadence, so a magnetic field source could not be generated. Second, the sensitivity of a sensor could not be defined by simulation tools prior to the measurement. To address these two issues, first, COMSOL simulation described in chapter 4 and 6 optimize the sensor size and determine the sensitivity of the sensor. Second, ANSYS Maxwell modeling and simulations for optimization of the coil size and determining the generated magnetic field was performed. These results were embedded as a VERILOG-A code in Cadence to convert the magnetic field to voltage for simulation purposes. Next, this code is combined with a resistor bridge model of the Hall plate reported by Xu and Pan [41]; then, the combined models is connected to the design schematic and post layout for functionality verification. Also, knowing that Cadence does not have a model to mimic the sensitivity drift of the Hall sensor, as explained in chapter 3 (section 1.3), the temperature behavior of the sensor is predicted. To compensate for the drift, the gain drift of the LV side amplifier chain is adjusted to oppose the sensitivity drift.

CHAPTER 4 ARTICLE 1: A GALVANIC ISOLATED AMPLIFIER BASED ON CMOS INTEGRATED HALL-EFFECT SENSORS

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This article addresses the first objective of this thesis, namely the investigation and validation of Hall-based isolation amplifier with minimal integration in the CMOS process TSMC 65nm. Also, the optimization objective toward maximizing sensitivity of Hall plate is validated in this manuscript. The manuscript was published in IEEE Transactions on Circuits and Systems - I as a Regular Paper in February 2021.

4.1 Abstract

A novel galvanic isolated amplifier based on CMOS integrated Hall sensors is presented in this paper. Two serially connected Hall-effect sensors are integrated along with their instrumentation amplifiers using the TSMC 65nm process. A printed-circuit board is employed to validate the proposed isolation amplifier by assembling the chip with chopper modulator, coil driver, miniature coil, variable gain amplifier, and anti-aliasing filter. Because of the miniaturized size of isolation components, this approach can be packaged in chip for industrial applications. This solution replaces the need of bulky/frequency dependent current transformers, complex isolation amplifiers with embedded analog to digital converters, and allows proposed sensors to be used in voltage and current sensing applications. The introduced prototype achieves an input referred offset of 1 mV, 50 dB full-scale signal-to-noise ratio in a 10 kHz bandwidth, and spurious-free dynamic range of 53 dB, while satisfying continuous isolation working voltage of 550 V.

Index Terms: Isolated amplifier, current/voltage sensing, galvanic isolation, chopper amplifier, magnetic coil, CMOS Hall sensor.

4.2 Introduction

Power monitoring applications such as power system control and protection need to simultaneously measure the load voltage and current. Such devices must continuously withstand in their working High Voltage (HV) environment for their lifetime and tolerate one-minute operation in presence of lightning surges, faults, or switching loads [63]. Additionally, they must have a fast response time to react to any aggression. Consequently, stringent industrial standards [63] verify their reliability over the required lifetime as well as satisfying important electrical safety features.

The principal technique employed in isolation/galvanic amplifiers (GA) is segregated ground loops and dividing the amplifiers into an HV side and a Low Voltage (LV) side. Therefore, the sensed voltage and current by the HV side must be transmitted to the LV side through an isolation medium. Figure 4.1 summarizes all available isolated voltage/current sensing techniques. Unlike current transformers (CT) and magnetic sensors including Hall sensors, giant magneto resistor (GMR), and anisotropic magneto resistors (AMR), which are restricted to current sensing, implementation of differential voltage amplifiers is not limited to voltage sensing and are extensively used in shunt resistor current sensing due to the shunt simple implementation and high frequency behavior.

In isolated differential amplifiers, data transmission is performed by modulation, digitization, or purely analog. Commonly used isolated media are capacitive [64], inductive [14], and optic [17]. Purely analog data transmission is a challenge for capacitive link, as it transmits the HV side's common mode noises ranging from 50 Hz to 400 Hz (supply noise) to 1.5 kHz (lightning strike noise) [6]. Hence, modulation and demodulation are performed to separate the signal from the

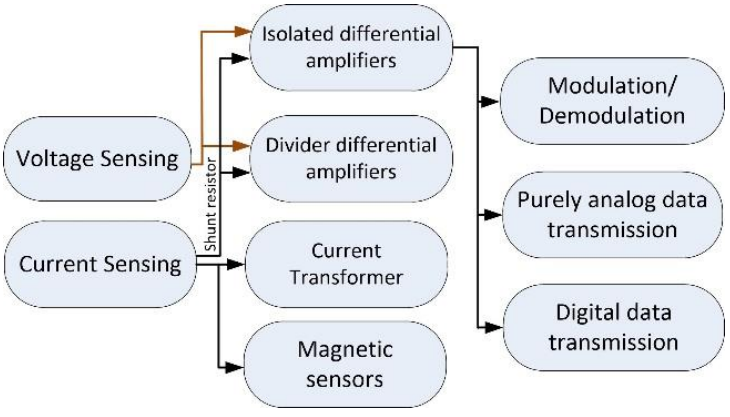

Figure 4.1 Available isolated voltage and current sensing

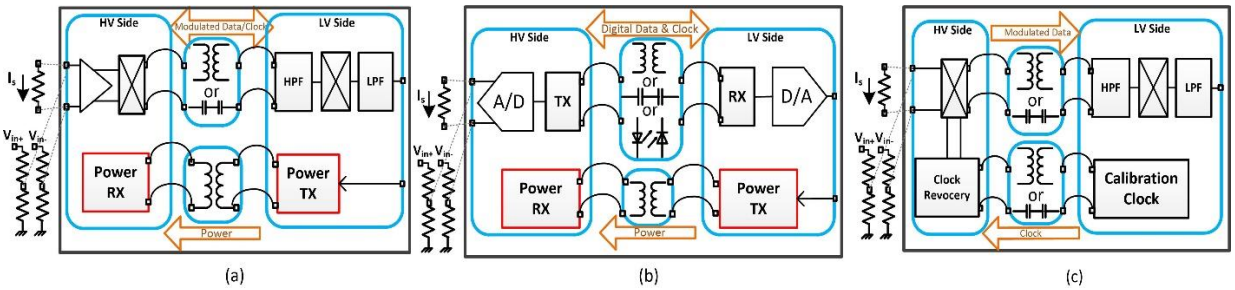

Figure 4.2 Isolation Amplifier based on Modulation/Demodulation (a) with active circuitry on the HV side, (b) based on digital isolator, and (c) all passive components on the HV side

common mode noise, and the LV side high pass filter rejects the common mode transient noise as in Fig. 2(a). So far, pulse width modulation (PWM) [7] and amplitude modulation (AM) [8] are employed in modulation/ demodulation types of GA. The PWM induces residual clock noise on the output signal. Also, in inductive medium, achieving a good Signal to Noise Ratio "SNR" imposes designers to employ a high-quality factor transformer which is not possible in millimeter scale, and lead to an enlarged overall design [8].

In parallel, the robust performance of digital isolators allows designers to use all types of isolation barriers as shown in Figure 4.2 (b), to overcome the previous limitations, and keep a high signal-to-noise ratio (SNR) [14, 64]. However, in addition to the transceiver and the receiver of the digital isolator, it comes at the cost of an additional analog-to-digital converter (ADC) on the HV side and a digital-to-analog converter (DAC) on the LV side. Despite the compactness and significant performance characteristics, the overall design is complicated and precise synchronization between ADC's sampling time and rectifier is needed.

In fully isolated or single supply isolation amplifiers, the power of HV side is supplied by the LV side as shown in Figure 4.2 (a-b). Therefore, the power consumption of the HV side will be the dominant part of the overall system's consumption. As shown in Figure 4.2 (c), in modulator/demodulator type, there are attempts to not use active components on the HV side, such that chopper switches are triggered by a passive recovery clock [9, 65]. However, the transformer-based GA is limited to current sensing [65], and the capacitive based GA has a limited resolution which makes it not suitable for high resolution applications [9]. The other drawback of all fully isolated amplifiers using digital communication is having high-power consumption on their HV side. For instance, the power consumption of one ADC on the HV side is around 100 mW [14].

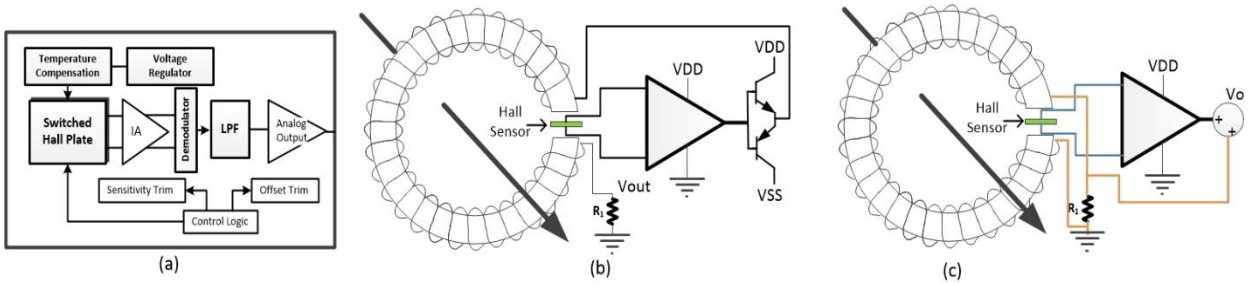

Figure 4.3 Isolated current sensing: (a) internal architecture of a typical Hall amplifier, (b) Hall current sensing using magnetic concentrator in closed loop configuration, and (c) combination of CT and Hall sensors for wide bandwidth current measurement

Analog data transmission with optocouplers is an attractive alternative that can reach a very good linearity of 0.1% and high isolation level of 5 kVrms [21]. However, they suffer from light-emitting diode (LED) shorter lifetime being caused by electrical and thermal stresses [5]; displacement damage subject to gamma radiation, also lowers the quantum efficiency of the optocouplers [13]. Other types of differential amplifiers that can tolerate HV conditions are resistor divider and capacitive coupling that are mostly used in biopotential amplifiers. However, both have not been discussed here because of not being truly isolated and DC blockage of signal, respectively.

In CT-based solution, AC current in the primary of the HV side is transformed to a smaller current on its secondary winding and converted to voltage using a burden resistor. Not capable of DC transmittance, this approach also suffers from bulky transformers for low-frequency signals [33].

While there have been limited efforts to configure Hall effects as voltage amplifiers [66, 67], they have been widely used in current and position sensors, magnetic field, and speed measurements [68]. High DC offset, 1/f noise, offset and sensitivity drift over temperature are of the concerns in deploying Hall sensors [66]. Consequently, every Hall current sensor amplifier integrates a Hall element, temperature-compensating circuitry, a small-signal high-gain amplifier, a clamped low-impedance output stage, and a proprietary dynamic offset cancellation technique as shown in Figure 4.3 (a) [35].

Typical CMOS Hall sensors are known for their low sensitivity. As a result, traditionally large C-shaped magnetic concentrator being clamped around wires, as shown in Figure 4.3 (b), is usually used [33]. In this configuration, the signal of the magnetic sensor generates a current signal opposing the offset magnetic field, and the remaining current will generate the signal related

current to produce the output voltage on R_1. However, the low bandwidth of the core material due to eddy losses and hysteresis, decreases the overall sensor's frequency response. To overcome the bandwidth limit, Figure 4.3 (c) combines the output of open-loop magnetic sensor and a CT to achieve wide bandwidth current measurement [33]. Although the Hall current sensor with concentrator demonstrates good resolution, linearity, and bandwidth, the final product is bulky in comparison with the traditional analog isolation amplifier. There are state-of-the-art and industrial Hall sensors that the sensor is placed on top of a shunt of current [28, 34] or a high current are diverted into the package [35, 36] and the magnetic field created by this high current is being sensed. However, their usage is limited for high current applications, and yet, similar to all the magnetic sensors, they are limited to current sensing.

Our response to these challenges is a Hall-based isolation amplifier capable of sensing shunt resistor voltage on the high voltage lines as well as differential voltage sensing. In this approach, the HV side is directly connected to the shunt resistor or differential voltage lines and generates a perpendicular signal dependent magnetic field to be sensed by the Hall sensors on the LV side. Consequently, it enables the Hall sensor to be utilized in voltage sensing applications, and the magnetic data transmission adds a galvanic medium to satisfy requisite isolation. Also, the analog-based approach eliminates the complications involved in using ADCs on the HV side and consequently conserves the overall system's power consumption.

The capacitive data transmission of Figure 4.2 (a & c) transmits electrical surges that has inherently low frequencies. To protect the amplifier from surges, the modulation/demodulation approach, as well as high pass filtering at the LV side, are performed. Although the isolation principle of an inductive link is realized by magnetic coupling, yet the planner inductors behave like parallel capacitor plates, and they suffer from surge transmission as well. Moreover, the modulation/demodulation approach comes with the benefit of lowering the transformer size in inductive coupling technique; nonetheless, limitation of the quality factor in small planner coils made the amplifier bulkier and power-hungry [8]. Also, inductive links are sensitive to electromagnetic interference [69]. Consequently, most of the integrated inductive links are used as digital isolators [14]. The purely magnetic-based approach of the Hall based isolation amplifier not only immunes the amplifier to surges but also require a smaller footprint transmitter coil with the advantage of generating more magnetic field with lower inductance while preserving consumption.

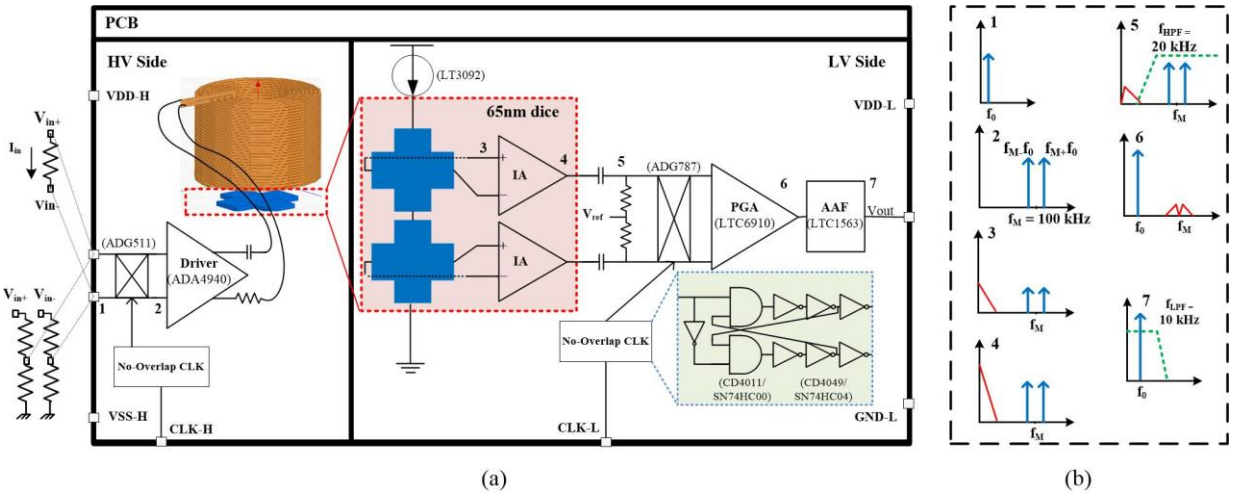

Figure 4.4 (a) Architecture of the Hall based isolated amplifier, and (b) signal spectrum at various stages of the amplifier

The remaining of this paper is organized as follows: the overall system architecture is described in Section II, coil, and sensor design criteria, and implementation of the instrumentation amplifier (INA) are also, described in this section. The measurement results and discussion are stated in Section III, and finally conclusion remarks and future works appear in Section IV.

4.3 Design and Implementation

4.3.1 Overview

The main architectural concerns of the proposed Hall based isolation amplifiers are a miniature coil with its driver, the twin CMOS Hall effect sensors with their respective INAs, and the Anti-Aliasing Filter (AAF). A schematic version of the Hall based isolation amplifier is shown in Figure 4.4 (a).

First, located on the HV side, chopper modulator displaces the input signal to a higher frequency band of 100 kHz. Second, a variable gain amplifier drives the miniature coil being placed on top of two serried CMOS Hall sensors with their respective INAs fabricated in 65nm chip. Consequently, the coil generates a signal dependent magnetic field to be sensed by the sensors and amplified by the integrated INAs. Then, implemented on the PCB, a passive high pass filter (HPF) with a cut-off frequency of 20 kHz eliminates the DC offset and attenuates the 1/f noise of the

combined sensors and INAs. Next, down converter chopper switches bring the signal back to the baseband region, and a programmable gain amplifier further adjusts the gain. Finally, the mirrored spectral components due to switching frequency and residual switching glitches are being filtered by an active low pass AAF.

The frequency spectrum of the GA is shown in Fig. 4 (b). The modulation/demodulation technique in graph 2 and 6 of Figure 4.4 (b) allows transmission of baseband input with signal's DC component to the Hall sensor without letting flicker noise as well as DC offset of the sensor and INA being merged with the received signal.

In comparison with similar works, at [66] CMOS Magfets are used as the sensing element which eliminates the need for instrumentation amplifiers and a cascode stage amplifies the deflected current due to magnetic field; however, minimum detectable magnetic field in CMOS Magfets is higher than CMOS Hall sensors [55]. Therefore, by using CMOS Hall sensors better detection of the magnetic field will be achieved.

Also, the structure presented in [67], allows single magnetic link to transfer analog data and no additional data link for clock recovery is needed; however, an external low-frequency magnetic field can perturb the amplifier's signal, and the modulation/ demodulation approach not only protects the amplifier from such noises, but also removes the necessity of an active offset canceler circuit.

4.3.2 Sensor Implementation

CMOS Hall sensors are known for low sensitivity. Therefore, optimum sizing to achieve the highest SNR is performed as follows. The Hall voltage related sensitivity is defined by:

$$S_V = \frac{G\,\mu_H}{N_{square}} \tag{4.1}$$

$$G = 1 - 1.045 e^{-\pi \frac{L}{W}} \tag{4.2}$$

where G is the geometry parameter [41], μ_H the Hall mobility, N_{square} the equivalent square number of N-Well sheet resistance, L the length, and W the width of the sensor. Knowing the sensitivity,

the sensor's biasing current, I, and the peak magnetic field of the coil, B, the peak voltage of the sensor is calculated as:

$$V_{peak}=S_I\,IB \tag{4.3}$$

To determine the noise power, flicker noise, as well as DC offset, is ignored due to the modulation technique. Also, value of shot noise of the tail current source is negligible and can be further attenuated by the amplifier's CMRR. Therefore, the main noise contributor on the output nodes of the sensor is thermal noise, which is calculated as:

$$\text{Noise}=\sqrt{4kTR_{eq}} \tag{4.4}$$

$$R_{eq}=(2\frac{L}{W}+\frac{2}{3})\,R_s \tag{4.5}$$

where R_{eq} is the equivalent resistor between voltage nodes of the sensor [41], k is Boltzmann constant and T is temperature in Kelvin. As shown in Figure 4.5, $\frac{L}{W}$ ratio of 0.58 results in the optimum SNR. Hence, the implemented sensor has 7.2 µm width and length of 12 µm. To reduce the 1/f noise and carrier surface loss, the sensor's top is covered with P^+ layer [54]. Table 4.1 summarizes the parameters used in the calculation which corresponds to the available technology and test setup.

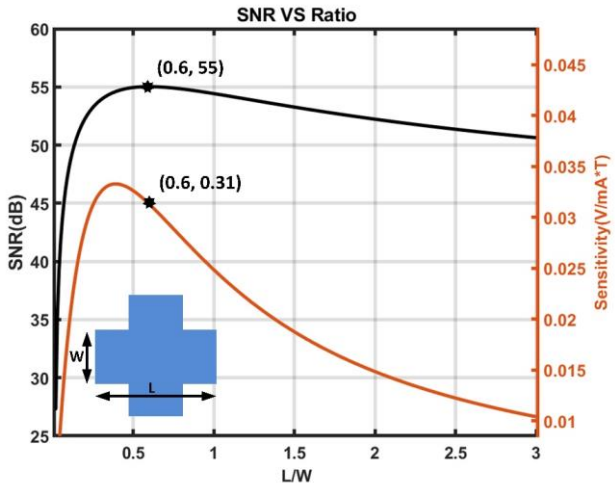

Figure 4.5 Calculated sensor's SNR and Sensitivity respective with L/W (1 mA biasing current and 2.5 mT of magnetic field)

Table 4.1 Model Parameters Based on the Available Technology and Field Strength of the Miniature Coil

Symbol	Parameter	Value
n [cm^{-3}]	Dopping Concentration	$2e^{17}$
I [mA]	Biasing Current	1
B [mT]	Peak Magnetic field of miniature coil	2.6
R_s	N-Well Sheet Resistance	1e3
t [µm]	N-Well Thickness	1
$\sigma\ [\frac{S}{m}]$	Conductivity	$\frac{1}{R_S t}$
μ_H	Hall Mobility	$\frac{\sigma}{nq}$

4.3.3 Miniature Coil

System's overall SNR is directly related to the strength of the magnetic field generated by the HV side's driver. Unlike the previous studies, in this work, the coil current is supplied by the HV side's driver; thus, to restrict the power consumption and maintain good SNR, a limited current should be fed to the coil for high magnetic field generation. On the other hand, the coil size must be minimized to make this design compatible with IC packaging, and miniaturization is another challenge that cannot be done using conventional concentrators.

One viable solution to have a compact design is using miniature coils. For such a reason, a small air gap solenoid coil is manufactured and to further increase magnetic field, a ferrite rod is centered at the coil's airgap. The coil will be placed directly on the sensor dice. Therefore, assuming zero gap between the coil and sensor die, the actual distance between the die's N-Well top and the coil's wire surface will be the sum of a 9.5 µm of coil isolator material plus 10 µm of dice intermetal isolation.

Figure 4.6 shows the magnetic field simulation of the described miniature coil using ANSYS Maxwell software at 17.5 µm distance from the coil. The coil generates a uniform peak magnetic field of 2.5 mT at the center for 2.5 mA of current. This allows the twin sensors to absorb identical magnetic field. The field strength relative to the coil's height is also shown in Figure 4.7.

Because of the complications involved in placing the dice in the coil center, the highest field of the coil cannot be captured, and we can only place the sensor on the coil's edges. The coil-ferrite specification is described in Table 4.2. Using the optimum sensitivity of Figure 4.5 and simulated axial magnetic field of Figure 4.7, Figure 4.8 demonstrates the relationship between SNR and magnetic field respective to axial distance. Although capturing the most magnetic field and achieving the optimum SNR stems from minimizing the coil-sensor distance, in applications with higher requirement of isolation level, adding layers of polyimide with 30 μm of thickness similar to [14] can increase the isolation voltage while loosing only 0.5 dB.

Table 4.2 External Miniature Coil Parameters

	Parameter	**Value**
Miniature coil	Inner diameter	1 mm
	Outer diameter	1.9 mm
	Height	1.9 mm
	Turns	270
	Wire width without isolator	50 μm
	Wire width with isolator	69μm
	Coating	Polyimide
	Enamel thickness	~10μm
	Wire type	AWG44-HY
Ferrite	Material	78
	Outer diameter	1mm
	Initial permeability	2000
	Relative permeability	48

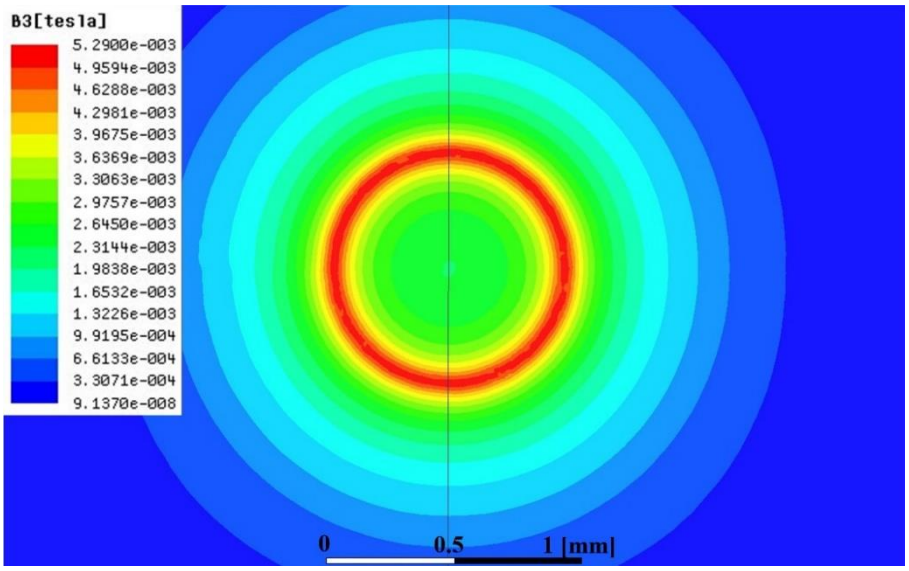

Figure 4.6 Simulated radial magnetic field at 17.5 µm distance from the bottom of the miniature coil with 2.5 mA of current

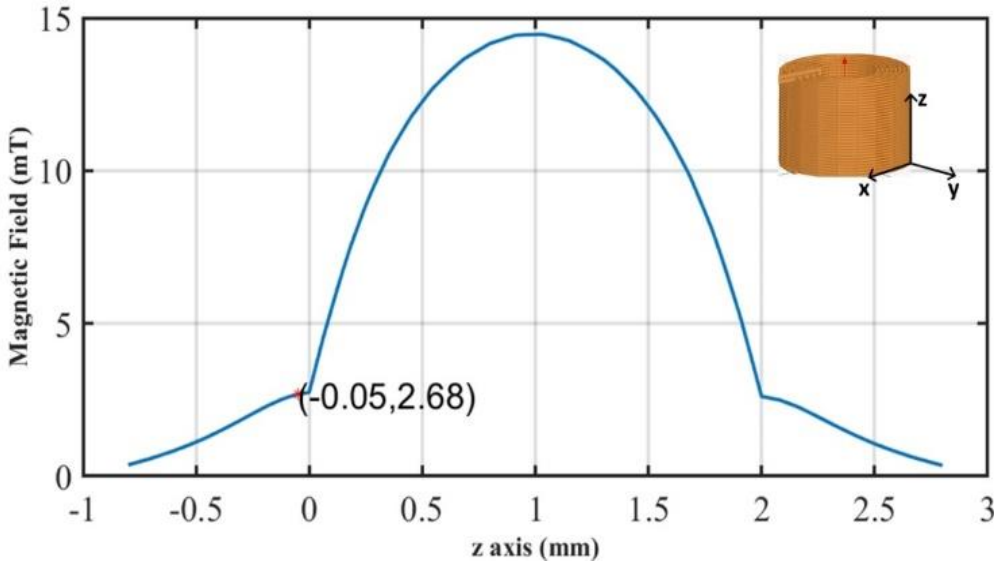

Figure 4.7 Simulation result of axial magnetic field of the miniature coil with 2.5 mA of current

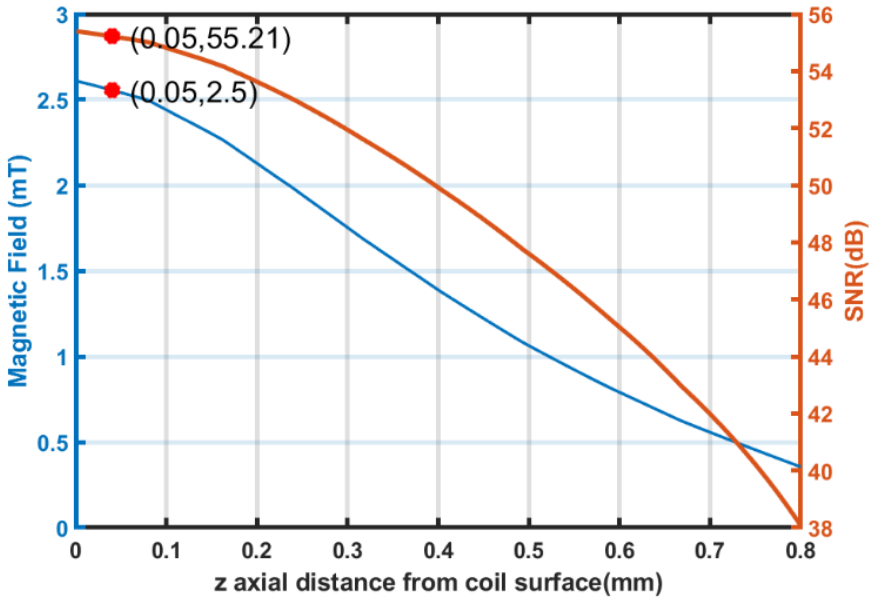

Figure 4.8 Variation of SNR and magnetic field respective with axial separation of the chip substrate where coil is located at the chip's surface

4.3.4 Driver Circuit

To preserve the overall system's linearity, the current passing the miniature coil must be linearly proportional to the input voltage. Considering the coil as a simple series model of relatively large inductance and low resistance, frequency response of the model would have a pole lower than the chopper frequency. This causes non-flat low pass response of the overall system. Moreover, offset of the driver injects a constant DC current to the coil that not only can saturate the coil, but also generates a DC field that would be sensed by the sensor.

Therefore, as shown on the HV side of Figure 4.4, using inductance of the miniature coil, a series RLC filter was created to ensure flat passband response and avoid a constant DC current injection through the coil. In this way, the maximum delivered current is also controlled. Finally, the gain of this stage must be tuned to adjust the deliverable coil's current for different input voltage ranges of shunt resistor current sensing or differential voltage sensing, so that maximum plausible magnetic field is delivered to the sensors in both sensing applications.

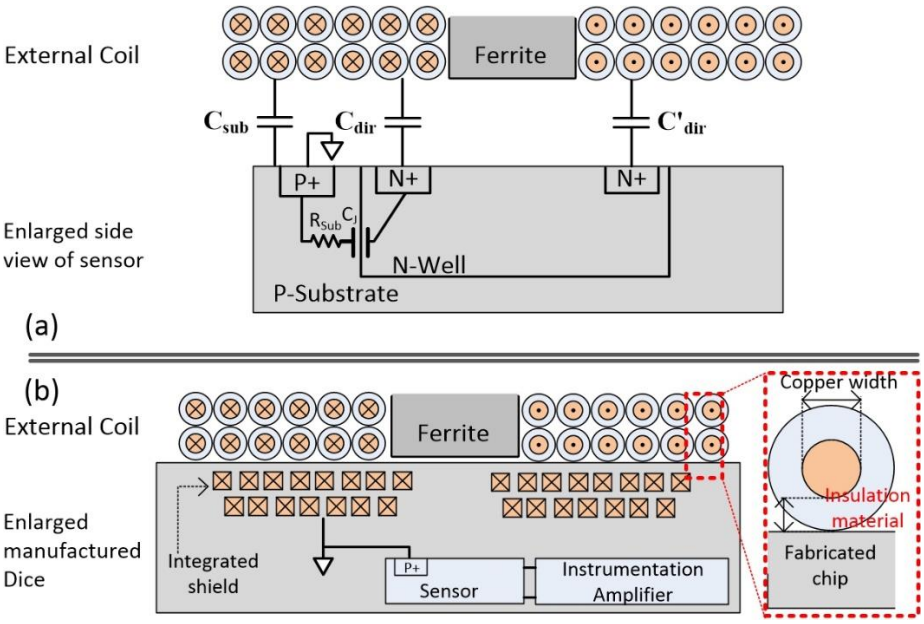

Figure 4.9 Coil placement: (a) side view of the miniature coil-sensor with the respective parasitic capacitances, and (b) side view of the miniature coil and shielded sensor

4.3.5 Instrumentation Amplifier Design

Coil placement on the sensor's top creates two types of parasitic capacitance. C_{dir} is capacitance between the coil and the integrated Hall sensor's metallic contacts and N-Well and C_{sub} is parasitic between coil and dice substrate, which both are shown in Fig. 9(a). This parasitic effect exhibits two types of noises, common and differential mode [70], so the sensor's output signal will be defined as the following:

$$V_{out} = V_{CM} + V_{diff\text{-}CC} + V_H \tag{4.6}$$

where, V_{CM} is common mode noise, $V_{diff-CC}$ is capacitively coupled differential voltage noise, and V_H is the Hall voltage generated by the magnetic field. Using eq (3), reported data of Table (I), and sensor's sensitivity of Figure 4.5, the sensor alone can induce a differential voltage of up to 75μV. Due to the small value of the input signal, damping and controlling the V_{CM} and $V_{diff-CC}$ are of great importance.

A typical approach in damping the V_{CM} of the CMOS Hall sensors is the placement of an instrumentation amplifier with a high Common Mode Rejection Ration (CMRR). Furthermore, as

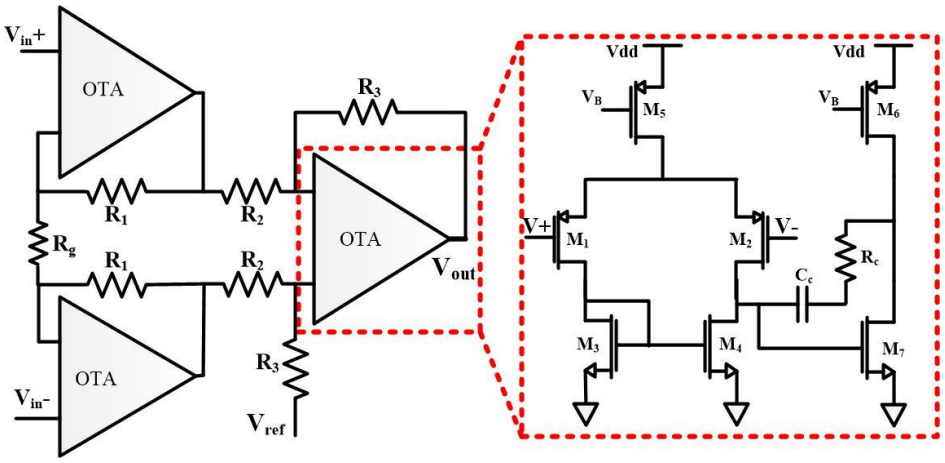

Figure 4.10 Topology of the integrated instrumentation amplifier

the Hall sensor does not have any driving capabilities, any capacitance on their signal node decreases their bandwidth [71]. Hence, an amplifier with high input impedance and no implemented input capacitance needs to be employed. For this reason, here a conventional IA with the architecture shown in Figure 4.10 has a CMRR of 90dB, 60 dB of gain, an input referred noise of 14 $\frac{nV}{\sqrt{Hz}}$, a cutoff frequency of 200 kHz, and gain-BW of 200 MHz is designed.

The $V_{diff-CC}$ is related to an asymmetry between the miniature coil and the Hall sensor as well as its connection. Such an inevitable asymmetry varies the C_{dir} parasitics, which imposes two distinct voltages on the sensor's nodes in Figure 4.9 (a). Addressing the $V_{diff-CC}$ is done by a proper layout. Accordingly, the instrumentation amplifier is placed at a close distance to the sensor, while the Hall signals' wire lengths are precisely matched. The other countermeasure considered for this noise is creating an integrated shield surrounding the sensors and partially the INA. The grounded shield creates a uni-potential plate that shields the sensor from the noises generated by mismatched capacitors between the external coil and sensor Figure 4.9 (b). The entire substrate that surrounds the N-Well perimeter of the sensor is also tied to the ground to minimize the variation in C_{sub}.

4.4 Measurement Results

A Hall based isolation amplifier is designed for voltage and current sensing using shunt resistors. The test bench setup and its dedicated PCB are shown in Figure 4.11 (a) and (b), respectively. The fabricated 65nm dice along with all off-chip components of the LV side are supplied by a 2 V

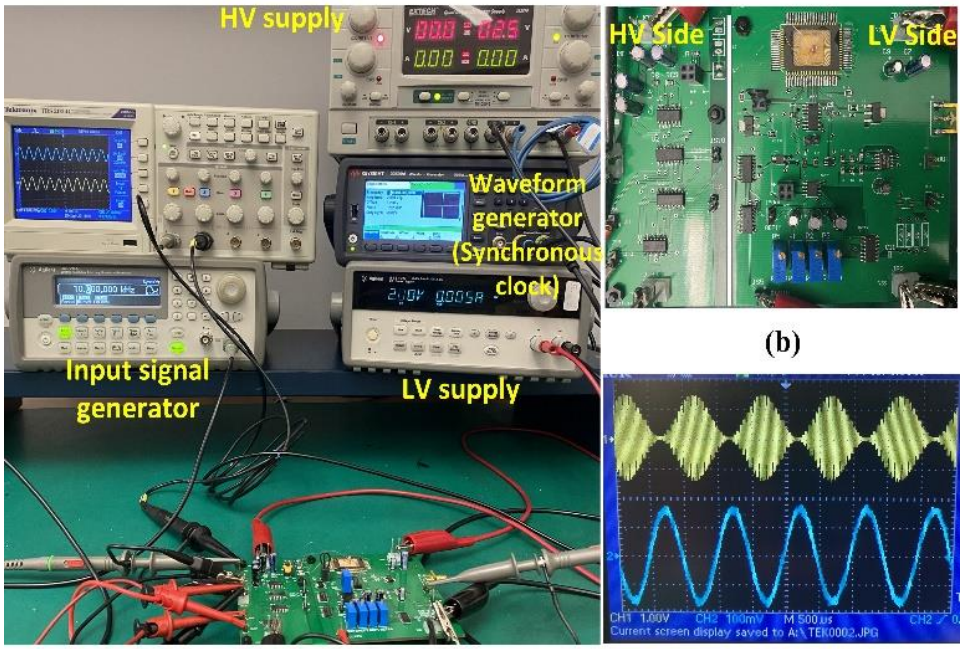

Figure 4.11 Experimental measurements: (a) test bench setup, (b) prototype PCB of the design, and (c) modulated current of the miniature coil measured from the 2 kΩ resistor being connected to the coil

supply while drawing 5 mA. The HV side of the PCB is supplied by ±2.5 V and consumes 20 mW approximately. The modulated current of the miniature coil being fed by the HV side's driver is shown in Figure 4.11 (c), which represents the modulated magnetic field of the coil.

On the HV side, AD4940 is chosen to drive the miniature coil for sufficient driving capability and rapid response. Chopper switches on both high and low side are implemented using commercially available multiplexers "ADG511 & ADG787", and the non-overlap clocks of Figure 4.4 (a) are created using NANDs "CD4011 & SN74HC00" and inverters "CD4049 & SN74HC04". Proper clocking signal between modulator and demodulator switches need to be precisely regulated. Any variation of duty cycle from 50% adds to system input referred offset; frequency mismatch causes harmonic and distorts the output signal. Moreover, the unadjusted clock phase causes signal attenuation; consequently, LV side switches must have an identical delay as the signal paths to avoid signal loss. Therefore, to address these concerns, an accurate switching operation is achieved by using the Keysight 33600A arbitrary waveform generator.

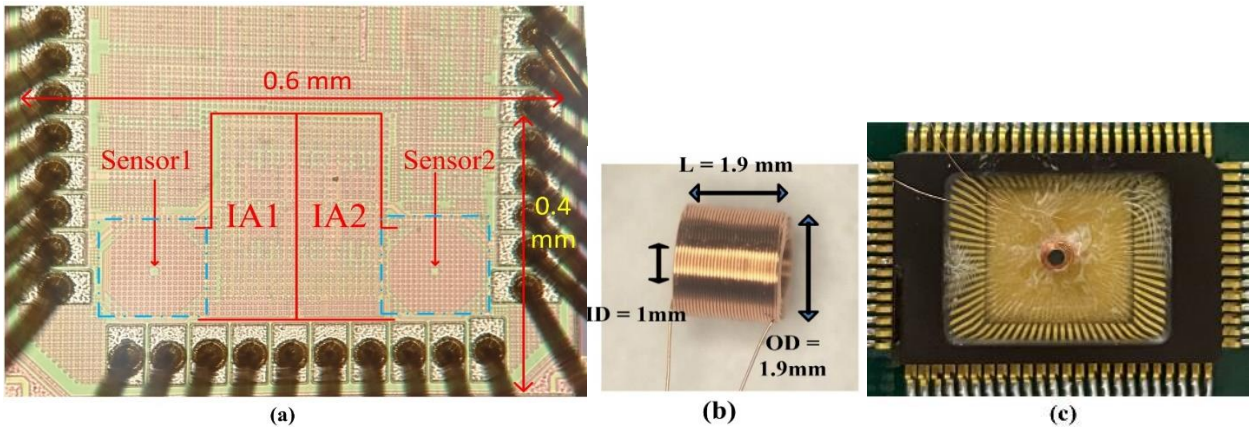

Figure 4.12 System in package view: (a) micrograph of the manufactured sensors and instrumentation amplifiers, (b) manufacture miniature coil, and (c) sensor package with coil glued on top of the dice

The fabricated chip using TSMC 65nm is shown in Figure 4.12 (a). This chip has 0.6 mm length and 0.4 mm height, and it consists of two sensors surrounded by metallic shield and corresponding INAs. The metallic shield is formed by 5 layers of hexagonal spiral coils with outer diameter of 150 µm and inner diameter of 15 µm leaving the central gap open for magnetic field entry. The initial purpose of the spiral coils was to generate a high integrated magnetic field; however, the measurement results revealed that the effect of differential capacitive coupling "$V_{diff-CC}$" explained in section II-E becomes dominant at frequencies above 50 kHz, and the amplified signal would not be purely magnetic based. Therefore, to have purely Hall effect without interference of capacitive coupling, the integrated spiral coil is used as a shield and is tied to ground, and an external miniature coil is utilized, as shown in Figure 4.12 (b). To double the sensitivity, the two implemented sensors are serially connected, and they generate 180-degree phase difference signals.

Distance from the on-chip miniature coil to the dice is directly and inversely proportional to RMS isolation voltage and SNR, respectively. That is, as the separation distance between the coil and die increases, magnetic field drastically attenuates. Consequently, to capture the most magnetic field, at 0.05 mm of Fig. 8, the coil is placed and glued on the chip top with a no-shrink/expand very low viscosity epoxy as depicted in Figure 4.12 (c).

The CMOS Hall elements have a bandwidth in the range of few megahertz [41]. To investigate the sensor and INA's bandwidth and sensitivity, a resonant technique as reported in [72] is employed.

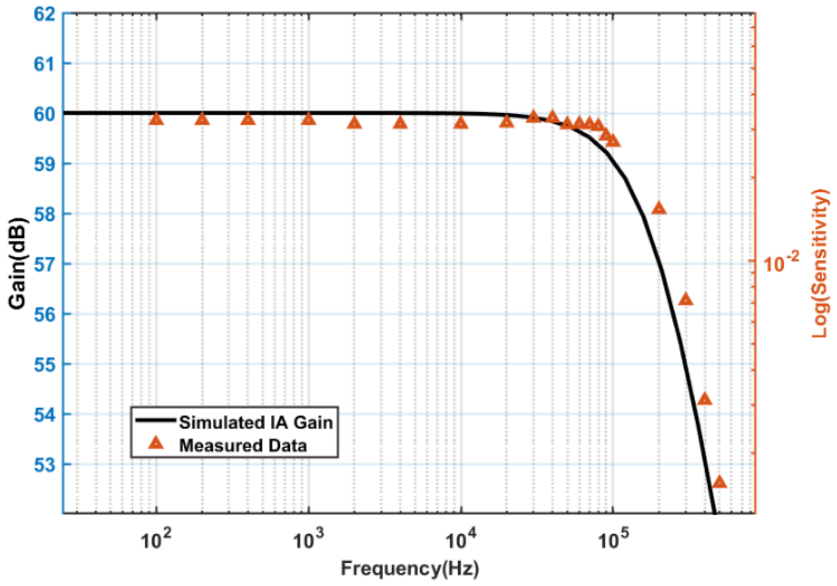

Figure 4.13 Simulated frequency response of the implemented IA compared with the measured frequency response of the combined integrated sensor and IA's sensitivity

First, the DC voltage sensitivity of a single sensor at 1mA biasing current is measured using the GMW 3472 Dipole Electromagnet generating a 4 mT of magnetic field. Next, on the measurement setup of Figure 4.12 (c), the miniature coil is connected to a signal generator, and a DC voltage that yields the same sensitivity is defined. Finally, for the same magnitude as of DC voltage, a resonant capacitor is serried with the miniature coil, and the signal generator frequency is tuned to achieve the maximum peak (resonant frequency) and the resonant frequency is recorded. The resulted sensitivity of the sensor at different frequencies is shown in Figure 4.13 and the single sensor's sensitivity of 0.032 V/mAT is bounded by the INA's bandwidth. The measured sensitivity complies with the calculated sensitivity reported in Fig. 5. Also, the sensor's output voltage that linearly varies with the biasing current is shown in Fig. 14. This confirms the purely resistive feature of the sensor. Additionally, the measured resistance between sensor voltage nodes is 850 Ω. Accordingly, following Figure 4.14, although increasing biasing current escalates sensor's sensitivity, having two sensors in series with 1 mA of current consumes 1.7 V of supply rail and sourcing more current is not possible.

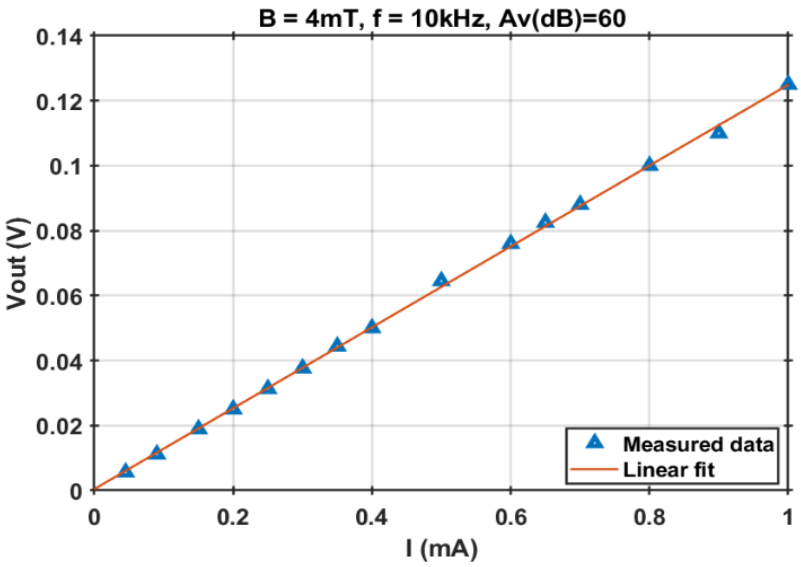

Figure 4.14 Sensor output voltage for different biasing currents

Having rapid response time in amplifiers' chain from the HV to LV side requires a sharp modulated signal before the demodulator choppers to preserve the signal amplitude. As a result, the modulation frequency must be chosen based on the slew rate and the bandwidth limit of the amplifiers' chain including the driver, sensors, and integrated INAs, as well as the input signal spectrum. Knowing the measured 200 kHz bandwidth of the combined implemented Hall-INA shown in Figure 4.13, 100 kHz is chosen as the chopping frequency. The 3 dB frequency of the HPF of Figure 4.4 is chosen to be 20 kHz to sufficiently attenuate the PGA "LTC6910" input signal from flicker noise and DC offset. The relatively low modulation frequency and the input signal bandwidth ranging from DC to 10 kHz obliged us to use a 4th order active low pass AAF filter which is realized in this test setup by the active filter IC "LTC1563".

The measured inductance and resistance of the manufactured coil with the ferrite rod inside are 0.25 mH and 12 Ω, respectively. To create a wide passband frequency response on the HV side, a capacitance of 50 nF and a 2 kΩ resistance are included in series.

In this Hall based GA, the coil-dice distance defines system's isolation level, and the aggression current must pass the magnetic barriers to break the amplifier's ground loops. The magnetic wire of the coil has polyimide insulation coating with 10 µm thickness, so considering zero distance between the die with its bond wires and surface of coil-copper's enamel, as shown in Figure 4.9(b),

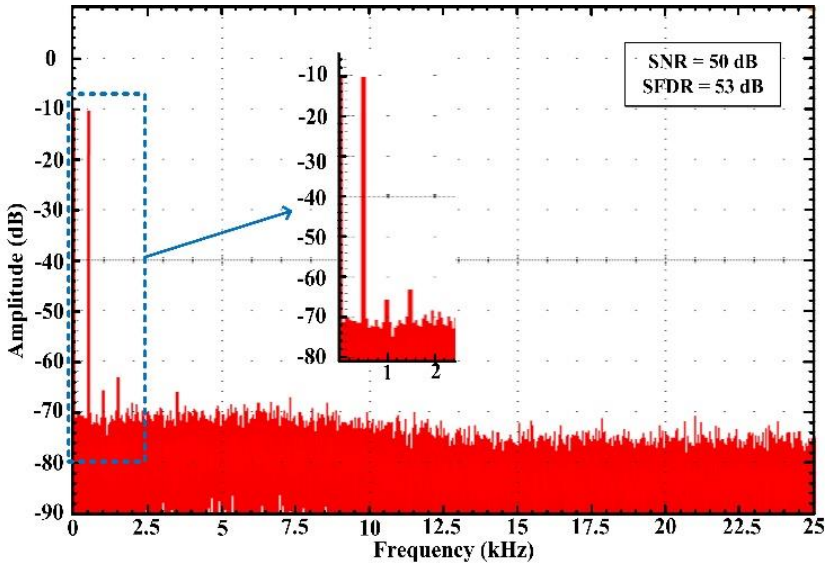

Figure 4.15 Output spectrum of a ±250 mV input signal at 500 Hz

minimum continuous isolation level of 550 V is guaranteed [73]. Therefore, this design benefits from a minimum of 0.55 kV of continuous isolation working voltage "V_{iso}", which can further be improved by increasing the polyimide barrier thickness.

The overall input referred offset of the design is 1 mV. The output spectrum of the amplifier attains an overall SNR of 50 dB within the 10 kHz bandwidth and an SFDR of 53 dB as shown in Figure 4.15. It can be seen from the spectrum graph that the modulation/demodulation approach has eliminated the 1/f noise from the output spectrum and based on 6 kV/V gain from Hall element to the output, the -72 dB of noise spectrum in signal band corresponds to amplified thermal's noise of the combined sensors and amplifiers.

The gain error for the output voltage swing of 0.1 to 1.9 V is shown in Figure 4.16 yielding a maximum nonlinearity error of 0.5%. In this measurement, employing least squares between differential input voltage (V_{in+} - V_{in-}) and differential output voltage (V_{out+} - V_{out-}), slope of the optimum line is defined. Then, nonlinearity is calculated as a fraction of half of the peak-to-peak value of differential output voltage deviation divided by the full-scale differential output voltage range. The measured amplifier's 5 µs propagation delay time in response to input step function is shown in Figure 4.17, which is sufficient for any over current conditions [14].

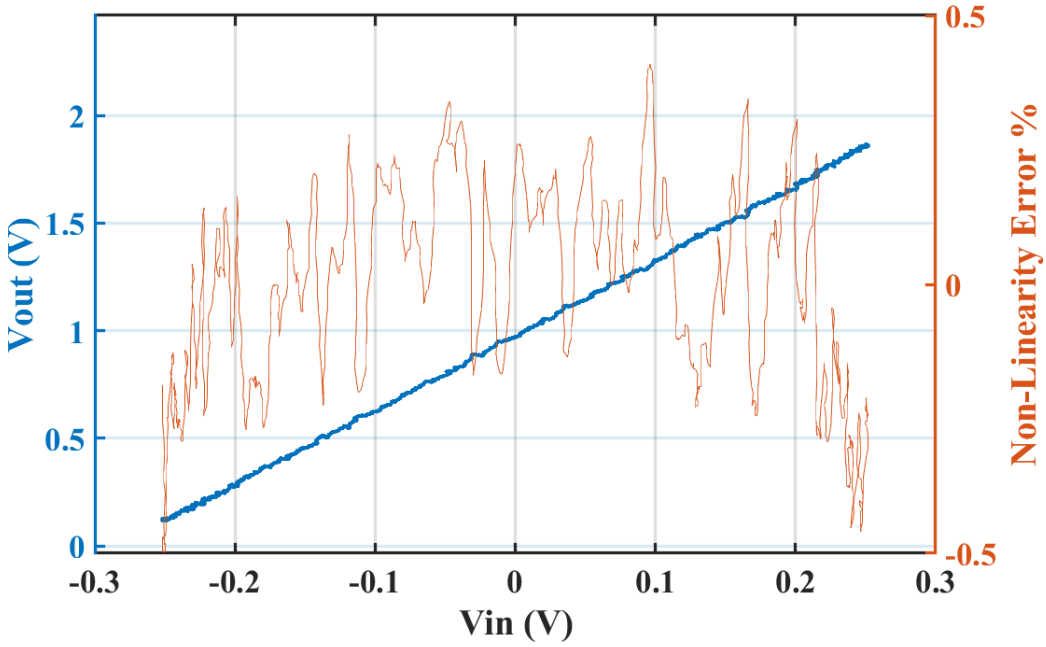

Figure 4.16 Amplifier's output nonlinearity error for input differential voltage of ±0.25 V

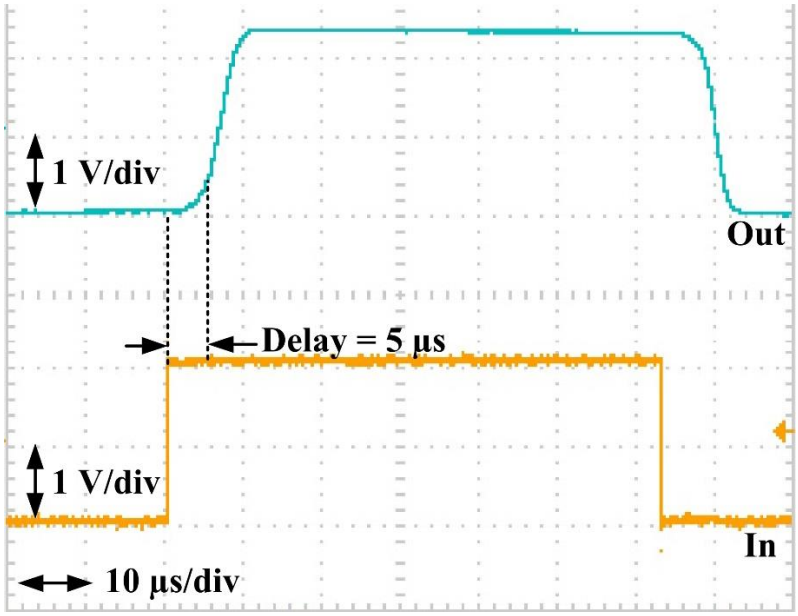

Figure 4.17 Step Response and Propagation Delay time

Table 4.3 summarizes the performance and the comparison with the state-of-the-art and industrial isolated amplifiers. Unlike conventional Hall sensor, high input impedance of the drivers shaped

the design to be capable of voltage and current sensing through shunt resistors. In this implementation, a dedicated external supply for the high side is required; thereafter, in comparison with the same category of amplifier (e.g. TLP7920 [17]), the Hall based GA has significantly conserved total consumption due to the elimination of the HV side's ADCs. Finally, the minimum V_{iso} of 550 V is assured and by benefitting from polyimide layer of commercially available technologies including 0.18 µm or adding 30 to 50 µm of polyimide layers by an external process, RMS isolation voltage can be further improved while losing about 0.5 dB of SNR as shown in Figure 4.8. Also, manufacturing coils with a smaller inner diameter and using thinner wires reduce its outer diameter such that the chip diameter is larger than the coil. Thereafter, the process of attaching the coil to the chip becomes easier and more adaptable to pick and place equipment.

Table 4.3 Performance Summary and comparison with prior-art works

Parameter	**Ma, et al. [14]**	**TLP7920 [17]**	**HLSR50 [34]**	**This Work**
Isolation Type	Inductive	Optic	Hall Effect	Hall Effect
Data Transmission	Digital	Digital	Analog	Analog
Sensing Application	Voltage/ Current	Voltage/ Current	Current	Voltage/ Current
V_{iso} [kV]	0.6	0.6	4.3	0.55<
Power [mW]	251.5	60 (HV side)/ 18.6 (LV side)	95	20 (HV side)/ 10 (LV side)
Input range	±0.3 V	±0.2 V	±125 A	±0.25-2.5 V
Vout non-linearity % @ minimum input range	0.5%	0.02%	0.5%	0.5%
Bandwidth [kHz]	200	230	400	10
Input offset	0.7 [mV]	0.73 [mV]	313 [mA]	1 [mV]
SNR [dB] @ bandwidth	71.9	-	59.1	50
SFDR [dB]	84.6	-	-	53
Propagation delay [µs]	5	2.8	-	5

4.5 Conclusion

To the authors' best knowledge, the reported work is a preliminary proof of concept of a novel approach in using Hall sensors as isolation amplifiers. A System in Package solution for analog isolation amplifier based on CMOS integrated Hall sensor is presented for voltage and shunt resistor current sensing, while satisfying minimum RMS isolation working voltage of 550 V. The isolated amplifier yields an input offset of 1 mV, overall SNR of 50dB with 10 kHz bandwidth, SFDR of 53 dB, and 5 µs propagation delay.

The author is currently working on improvement of the design. Using miniature coils with 10µm of wire diameter or special packaging having integrated coils can further improve the system's overall SNR and compactness. In application where higher SNR is required, 2DEG sensors, namely GaN, can be utilized. Sensor's sensitivity drift over temperature needs to be compensated, and all the off-chip components including PGA and filter can be integrated. Finally, for a complete isolation amplifier, a clock recovery with a tunable phase as well as an isolated power converter is needed.

CHAPTER 5 ARTICLE 2: A SMALL FOOTPRINT DIGITAL ISOLATOR BASED ON CMOS INTEGRATED HALL-EFFECT SENSOR

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As a part of a fully integrated system, a first reported Hall-based digital isolator for transmission of clocking signal from the HV to the LV side is designed and integrated in AMS 0.35 µm technology. The measurement results of the clock recovery are reported in this article and the manuscript was submitted to IEEE Sensor Journals in July 2021.

5.1 Abstract

Digital isolators have been widely used to protect low voltage electronics as well as human safety from high voltage surges. However, conventional isolation links suffer from occupying large chip areas. In this article, a novel small-size on-chip digital isolator for medium-bitrate application based on a CMOS integrated Hall-effect sensor is reported. With the proposed approach, the area of the transmitter coil is reduced to lower than 50% of conventional transformers. The architecture reduces the chip area in isolation amplifiers, power control units, DC-DC converters, and clock recovery circuits. It allows the integration of multichannel isolators using two custom integrated circuits with no post-processing. The tested prototype achieves a data transfer rate of 20 Mbps with above 12 kV/µs of common-mode transient immunity (CMTI). It has 900 V of continuous isolation working voltage, 27 ns propagation delay, and consumes 2.3 mA of static current.

Index Terms: Digital isolator, Galvanic isolation, CMOS Hall sensor, Gate driver, Integrated spiral coil.

5.2 Introduction

Magnetic field sensors are broadly utilized across various applications. Linear or angular position sensors, magnetic field measurements, and switches are examples of industrial applications. Employing their magnetic field sensing capability, the sensor usage is expanded to provide galvanic isolation. For instance, contactless current sensors (current transducers) replaces shunt based sensing with no drop out voltage and achieve a remarkable V_{iso} [74]. Magneto resistors, also been employed as digital isolators [75].

Isolated DC-DC converters, clock recovery of isolation amplifiers, power-over-ethernet, inter-integrated circuit (I^2C), and industrial programmable logic controllers (PLC) are applications that require the transmission of low to medium data rates over an isolation barrier. The digital isolators must satisfy stringent isolation standards including isolation working voltage (V_{iso}) and common-mode transient immunity (CMTI). Besides, reducing the number of chips and chip areas results in a low-cost product.

Figure 5.1(a) shows a system in package (SiP) of a typical fully integrated isolation amplifier (IA) based on an analog-to-digital converter (ADC) [14]. This IA employs three digital isolator links: (i) a link for isolated DC-DC converter, (ii) clock recovery, and (iii) data. As another application, Figure 5.1(b) shows a conventional three-phase motor driver. To avoid damaging the microcontroller unit (MCU) from HV pulses driving power transistor gates, the MCU needs to be isolated and six isolator links are required [76]. Therefore, integrating multiple isolator links in a small die can lower the consumed chip area and consequently the fabrication cost.

So far, all the isolation links including optic, capacitive, magneto resistor (MR), and inductive are employed in digital isolators. Despite unique isolation properties, optocouplers suffer from integration levels as they are made by GaAs whichcannot be integrated into a CMOS process. So, for every channel, a dedicated optocoupler chip is required. Also, optocouplers are prone to low lifetime due to electrical and thermal stress [5]. Capacitive digital isolators are highly integrable as capacitors can be formed by metal layers of a fabrication process, while the required isolation level is achieved using process silicon dioxide (SiO_2) available as intermetal fillings; laying out metal capacitors of both transmitter (Tx) and receiver (Rx) chips reinforces the isolation level. Besides, they require only two chips for any number of isolated links. However, transmitting of low-frequency signals requires an enlarged capacitor, so conventionally two data paths transfer the

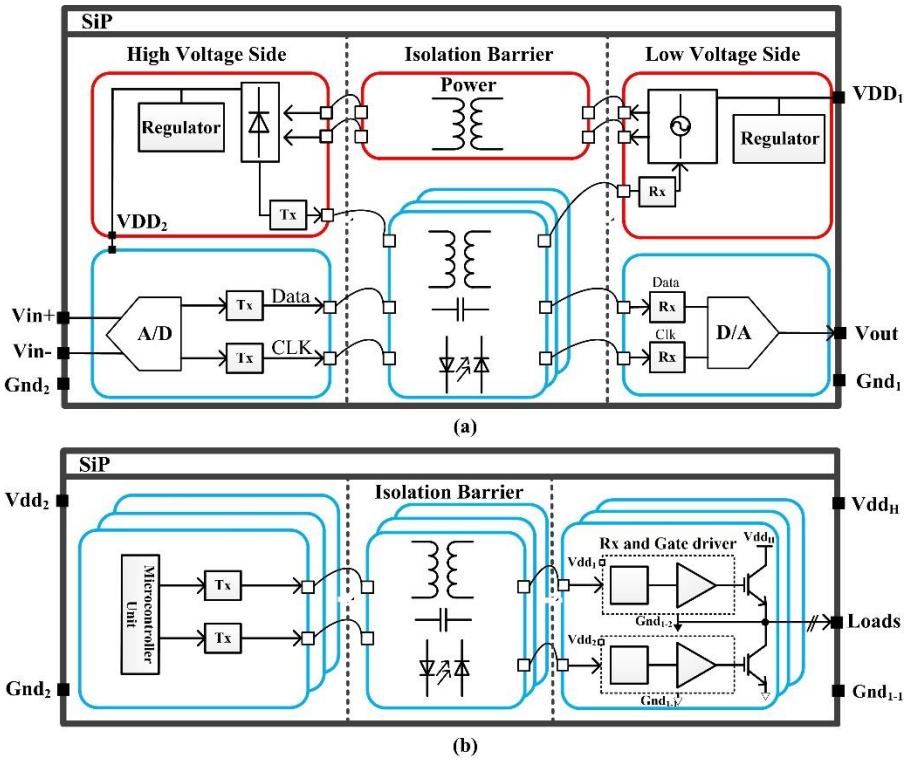

Figure 5.1 (a) Isolated amplifier based on analog to digital converter, and (b) typical motor drive system

digital signal, one using a modulation scheme for transmission of low bitrate (<100 kbps) signals and one channel for high bitrate (>100 kbps) signals. Consequently, the dual-channel capacitors increase chip area. Besides, as a two-terminal device, capacitive digital isolators suffer from transmission of common-mode transient noise (CMTN), and they have lower CMTI than transformers.

Most industrial digital isolators that are based on inductive links form the primary side of transformers on top of a polyimide isolator deposited as the last layer of the dielectric stack. The secondary side of the transformer is shaped by the top thick metal layer of the CMOS process [14]. The added deposition of the polyimide layer increases the cost and is not available in regular foundries. Although the on-chip transformer-based isolators are suitable for dense integration of multiple isolation channels in a microcontroller or gate driver chips, conventional technology still has the problem of considerably large transformer area.

Giant magnetoresistance (GMR) or tunneling magnetoresistance (TMR) technology are the magnetic sensors that have been studied for digital isolators implementation [75] and commercialized through NVE's patented IsoLoop spintronic technology. Regular foundries are incapable of deposition of ferrite/magnetic material in MR type of digital isolator, which increases the manufacturing cost. Employing CMOS Hall effect sensors could be more cost-effective.

This work presents an on-chip micro-transformer-based medium-speed digital isolator based on a Hall-effect sensor designed for dense integration. The rest of the paper is organized as follows: system architecture is explained in section II with the explanation of sensor and coil selection. Section III investigates the CMTI of the design. The measurement results and discussion are stated in Section VI, and finally, the conclusion and remarks appear in Section V.

5.3 Design and Implementation

5.3.1 System Architecture

Figure 5.2 (a) illustrates the digital isolator circuitry. First, located on the Tx chip, a Schmitt-trigger inverter conditions the digital input signal. Then, a 100 MHz bi-stable oscillator generates OOK modulation carrier frequency, and weighted inverters drive the integrated spiral coil located on the Rx chip. Next, a Hall-effect sensor placed under the coil center detects the signal, and three stages of amplification and passive high-pass filtering (HPF) amplify the modulated signal and filter the low-frequency noises, respectively. Each of the low-noise amplifiers (LNA) has a 35 dB gain. A 50 MHz of corner frequency is selected for each passive HPFs to attenuate the HV surges noises. The HPFs also remove flicker noises and DC offset of the combined sensor and amplification stages. Finally, a squarer circuit rectifies the modulated signal, and a comparator generates the output signal. The circuit schematic of each block is shown in Figure 5.2(b-f).

5.3.2 CMOS Hall Sensor

Although Hall effect sensors are widely known for their limited bandwidth, about THz theoretical bandwidth limit of Hall sensors is experimentally validated by Mittleman, et al. [77]. This high-frequency behavior of the Hall plates is subject to parasitic capacitances and the conventional inductive effect that severely limits the frequency response [58]. Therefore, design and layout considerations are applied to avoid inductive and capacitive effects. First, according to

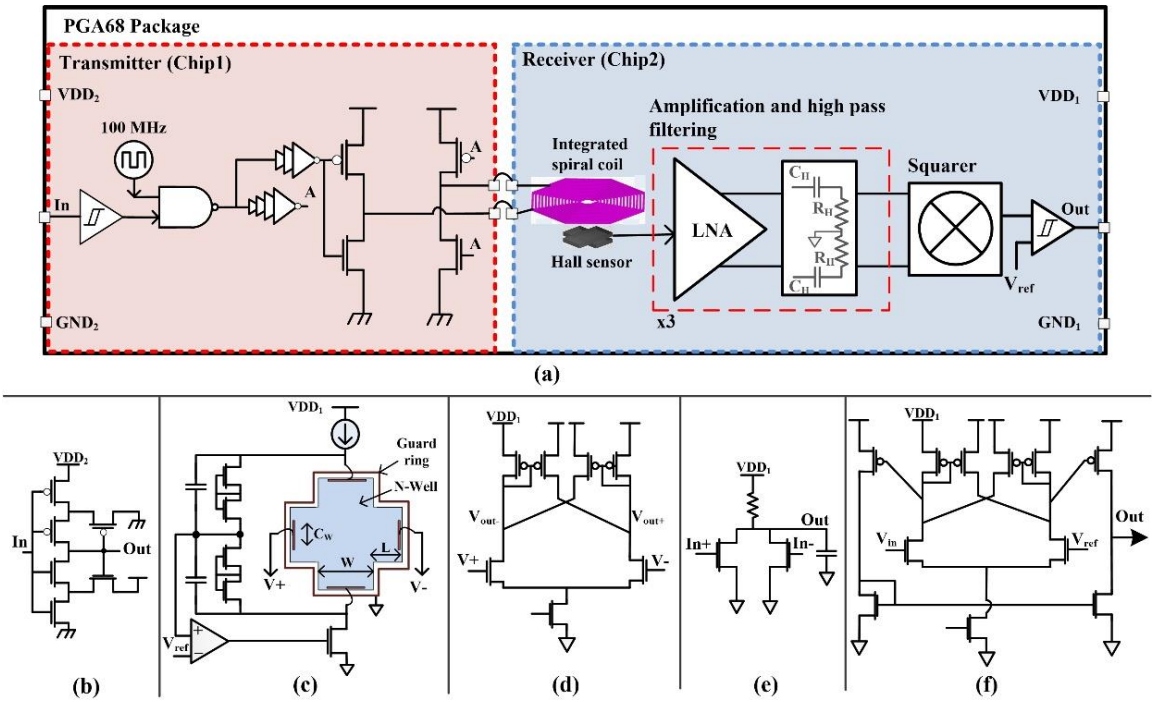

Figure 5.2 (a) Architecture of the proposed Hall-based digital isolator, (b) input Schmitt trigger inverter, (c) biasing circuit of the Hall sensor, (d) cross-coupled architecture of the sensor's preamplifier, (e) squarer circuit, and (f) output comparator

Figure 5.2(a), biasing voltage of the first amplifier stage must be provided by the sensor. Therefore, to avoid adding any capacitive load on the Hall voltage nodes, voltage reading of the common-mode feedback (CMFB) is performed from the biasing nodes of the Hall plate as seen in Figure 5.2(c). Second, the LNA must satisfy a low input gate capacitance as well as a wide bandwidth. For this purpose, the cross-coupled architecture of Figure 5.2(d) with NMOS input differential pairs are chosen. Third, to address the inductive effect and lowering wiring capacitance, the LNA is placed under the coil and 40 µm away from the Hall voltage contacts. The wiring between the sensor and the differential pair are the minimum width with equal distances and any loop is avoided to minimize the inductive effect and conserve the sensor bandwidth.

The CMOS Hall plate converts the orthogonal magnetic field to an electrical signal via the Lorentz force, so optimization toward sensitivity and minimization of the sensor's noise floor improves the signal quality of the sensor. Optimal sizing of a cross-shaped Hall effect sensor of Figure 5.2(c) relative to the width (W) and length (L) has been previously reported in [59]. The sensor is surrounded by a guard ring to eliminate noises induced by the P-substrate. The variation of

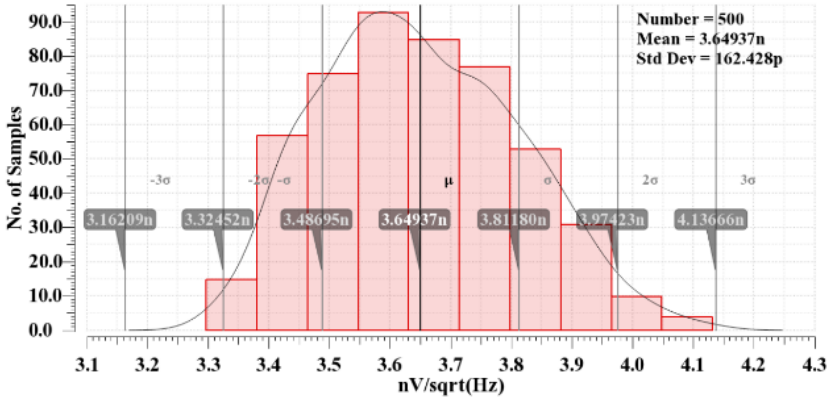

Figure 5.3 Cadence Monte Carlo simulation of the preamplifier's input referred noise

sensitivity to sensor area is described by Crescentini et al [78] and an enlarged area increases the sensitivity of the sensor. In contrast, reported by Xu and Pan [41], expanding sensor size, decreases the sensor's 3 dB bandwidth. Therefore, to avoid limiting the bandwidth of the sensor, a small sensor is designed with W of 19.3 µm and L of 11.2 µm. Large contact width of the signal nodes (C_W) shortens the voltage equipotential line deflection over the sensing nodes leading to a lower sensitivity. Therefore, a short contact size of 1.2 µm is depicted for the design.

To optimally capture the Hall voltage induced by the generated magnetic field, the first amplifying stage must have a low input-referred noise (VN_{in}). At the 100 MHz of modulation frequency, the dominant noise of the sensor is thermal. Knowing the process has N-Well sheet resistance of 1 kΩ/square and using the methodology described by Xu and Pan [41], the sensor has a resistivity of 1.6 kΩ and consequently 5.1 nV/$\sqrt{Hz}$ of thermal noise. Therefore, the LNA must be designed with a VN_{in} lower than this thermal noise to avoid contaminating the received signal. The designed cross-coupled structure of Figure 5.2(d) has a VN_{in} of 3.65 nV/$\sqrt{Hz}$ that can be observed from Figure 5.3.

5.3.3 Integrated Spiral Coil

Generating a magnetic field in Hall-based digital isolator involves several challenges. First, the Hall sensor signal quality is directly proportional to the field, so an adequate magnetic field is required to achieve a reasonable signal-to-noise ratio (SNR). Second, the coil behaves like a series of restive-inductive loads (i.e. a low pass filter); therefore, to avoid attenuating the carrier signal, the magnetic coil must have low inductance. Finally, the coil must have a small footprint to lower

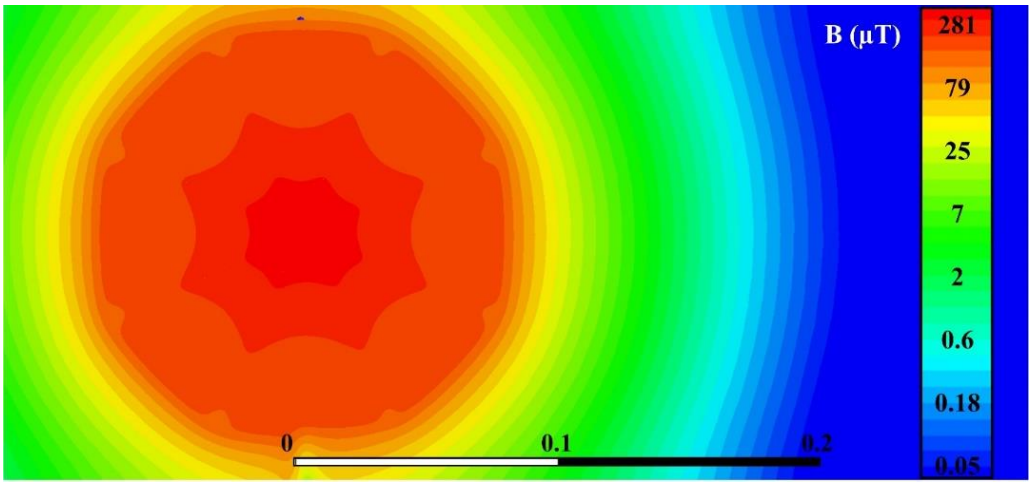

Figure 5.4 ANSYS simulation of magnetic field strength of the integrated spiral coil showing central magnetic field of 281 μT for 1 mA of current

the transceiver size, simplify packaging complexity, and reduce cost. Therefore, on top of the Hall plate, a single layer of integrated hexagonal spiral coil is fabricated using process top tick metal layer with specifications listed in Using the integrated coil approach, SiO_2, the intermetal filling of the CMOS process behaves as the isolation barrier. Following the reported mean time to failure of 450 V/μm for 20 years [61], and 2 μm of spacing between process second and the top metal layer, above 900 V of isolation working voltage (V_{iso}) is achieved in this design. Further increase of the V_{iso} can be obtained through a smaller process with a greater number of metal layers and consequently a thicker isolation barrier.

Table 5.1. To determine the field strength of the coil, an Ansys Maxwell simulation is performed for the peak current of 1 mA. Figure 5.4 shows 281 μT magnetic fields at the coil center where the sensor is located.

Using the integrated coil approach, SiO_2, the intermetal filling of the CMOS process behaves as the isolation barrier. Following the reported mean time to failure of 450 V/μm for 20 years [61], and 2 μm of spacing between process second and the top metal layer, above 900 V of isolation working voltage (V_{iso}) is achieved in this design. Further increase of the V_{iso} can be obtained through a smaller process with a greater number of metal layers and consequently a thicker isolation barrier.

Table 5.1 Parameters of the Integrated Spiral Coils

Parameter	Value
Number of turns	15
Turn spacing (μm)	2
Wire width (μm)	2.5
Inner diameter (μm)	22
Current density (mA/μm)	1.5
Outer diameter (μm)	158

To have multi-channel Hall-based digitally isolated links on the same dice, the Hall sensors must be in a cross-talk-free environment with respect to its neighbor coil. To determine the cross-talk-free distance, the output voltage of the sensor respective with the neighbor coil must be smaller than sensor thermal noise. The sensor output is defined as:

$$V_{diff} = S_I \, B \, I \tag{5.1}$$

where S_I is current-related sensitivity, B is the magnetic field, and I is sensor biasing current. Assuming S_I is 0.03 $\left(\frac{V}{mA.T}\right)$ [42] and I is 0.5 mA, any magnetic field lower than 0.34 µT generates a peak voltage lower than the sensor's thermal noise of 5.1 nV and cannot be detected. Based on Figure 5.4, multiple receiver sensors can be placed 200 µm apart from each other. Finally, based on simulation data, the coil has a self-resonance frequency of 4.2 GHz. If the predicted oscillation frequency occurs, it is higher than the LNAs' bandwidth at the Rx circuit and cannot get amplified. However, to avoid the self-resonance frequency limitation in higher bitrate applications, the Tx driver needs to be upgraded to not allow any current passes the coil when the input logic is low. This could be done by an LC tank oscillator or changing the Tx logic circuitry.

5.4 Analysis of Noise Rejection

Common-mode transient noises (CMTN) occurring between the grounds of the Tx and Rx side make the recovered digital signal not follow the input. The parasitic capacitance on the input node of the transmitter stores the charge and during HV surge causes the input inverter to follow the noise. Therefore, the Schmitt inverter protects the input from being contaminated by the CMTN.

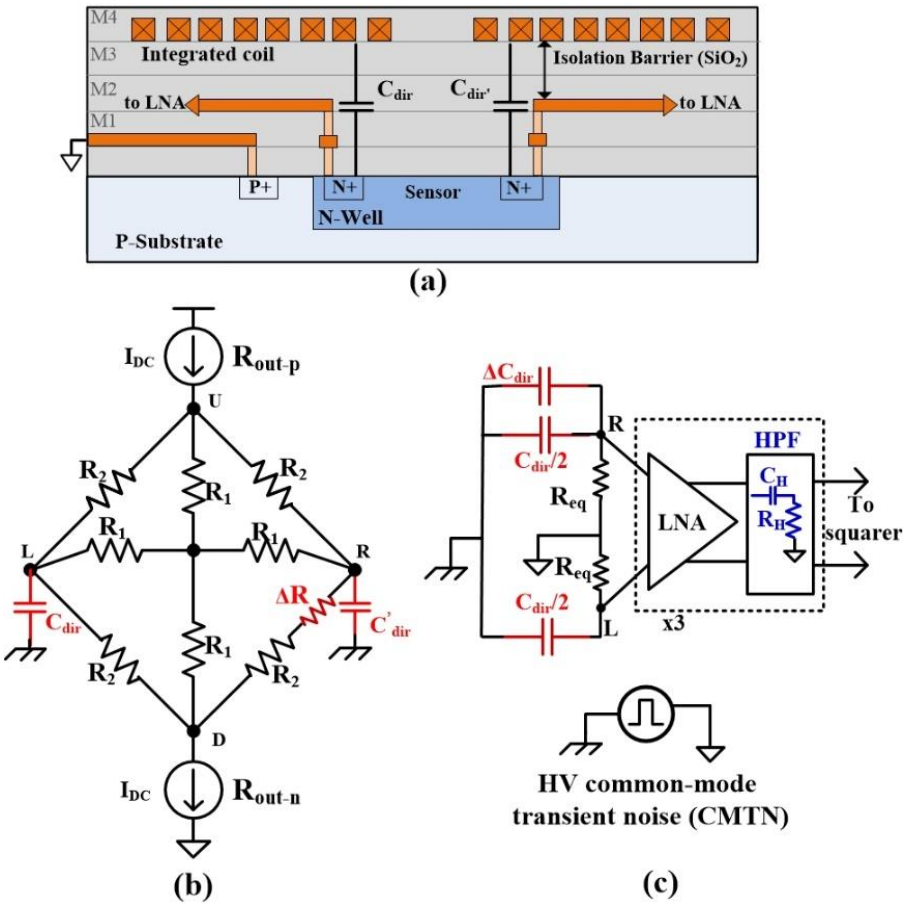

Figure 5.5 (a) Side view of the Rx dice showing parasitic capacitances between the integrated spiral coil and the Hall plate, (b) resistive model of the Hall plate with the parasitic capacitances , and (c) simplified schematic showing impact of the parasitic capacitances to the Rx circuit

Cross shape Hall plate sensors receive signals based on Lorentz force. Unlike the capacitive link, the different sensing mechanism comes with the advantage of not being sensitive to CMTN from the Tx side [14], [15]. However, miniaturization of the integrated magnetic coil with its close distance to the sensor form parasitic capacitances of C_{dir} and C'_{dir} as shown in Figure 5.5(a). To investigate in detail the effect of parasitic capacitances, the resistive model of the sensor depicted from Xu and Pan [41] with the parasitic capacitances is illustrated in Figure 5.5(b). The C_{dir} and C'_{dir} seen from the LNA nodes are not identical due to natural non-symmetry of the integrated spiral coils and it is assumed to have a difference of ΔC_{dir}. In Figure 5.5(b), ΔR models the sensor offset due to masking misalignment or nonuniformity of dopant [42] which is the main source of DC

offset in Hall effect sensors. Figure 5.5(c) shows a simplified AC model of the available parasitic between the LNA and CMTN of the Tx side. Following the methodologies described by Lyu, et al. [42], ΔR is lower than one ohm, so the effect of ΔR can be ignored, and R_{eq} is calculated as:

$$R_{eq}=(R_{out\text{-}p}+R_S)||(R_{out\text{-}n}+R_S) \tag{5.2}$$

Here, R_S is the Hall sensor resistance between voltage or current nodes, and $R_{out\text{-}p}$ or $R_{out\text{-}n}$ are output resistance of the tail current sources.

The main common-mode transient noise (CMTN) appears as a common-mode signal (N_{cm}); however, the ΔC_{dir} exhibits a differential noise (N_{dif}). Therefore, input noise voltage at the LNA is defined as:

$$CMTN= N_{cm}+N_{dif} \tag{5.3}$$

Next, the resulting output noise of the LNA is calculated as:

$$V_{out}^{LNA}=N_{dif}\, A_{dif}^{LNA} + N_{cm}\, A_{cm}^{LNA} \tag{5.4}$$

A_{dif}^{LNA} is the differential gain and A_{cm}^{LNA} is the common-mode gain of the LNA. Then, the V_{out}^{LNA} undergoes three stages of passive high pass filtering with capacitors of "C_H" and resistors of "R_H", and two stages of further amplification. Then, the input noise at the squarer will be calculated as:

$$V_{In}^{Squarer}=\left(\frac{S}{S+\frac{1}{C_H R_H}}\right)^3 \left(A_{dif}^{LNA}\right)^2 V_{out}^{LNA} \tag{5.5}$$

Following the post-layout simulation, C_{dir} and ΔC_{dir} are extracted to be 100 fF and 20 fF, accordingly. Also, A_{dif}^{LNA} is 35 dB and A_{cm}^{LNA} is -40 dB. Based on work presented by Xu and Pan [41], R_{eq} can be calculated as approximately 1 kΩ. By solving for poles and zeros, V_{out}^{LNA} has a high pass pole located at 8 GHz. Therefore, in total, the received noise on the squarer circuit is suppressed by fourth orders of HPF which three of them have 50 MHz and one has an 8 GHz of corner frequency. Post layout simulation for different signal stages of the Rx circuit for CMTN of

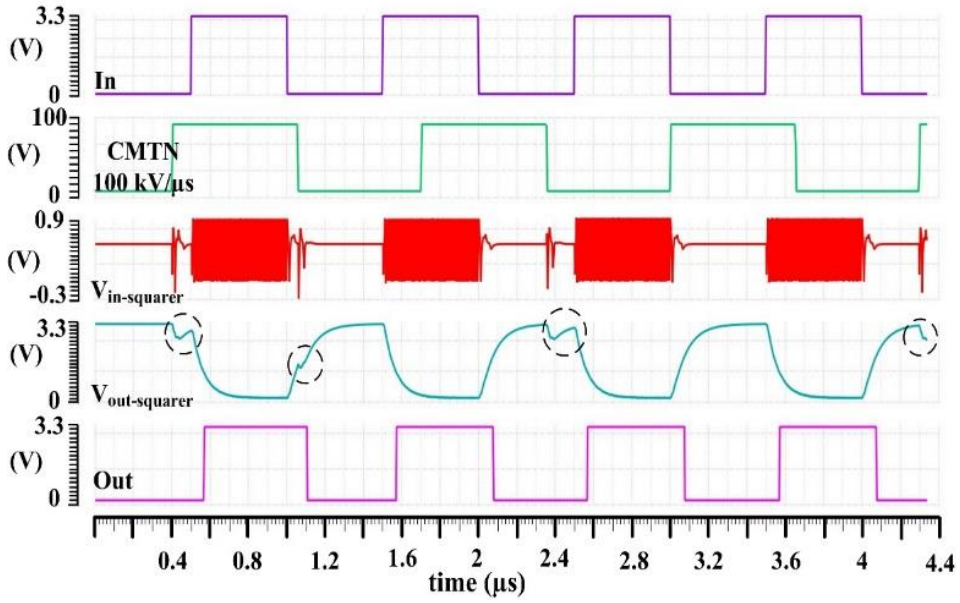

Figure 5.6 Post layout simulation showing isolator's signal flow in presence of 100 kV/µs of common-mode transient noises

100 V in 1 ns rise/fall time (100 kV/µs of slew rate) is shown in Figure 5.6. It can be seen from Figure 5.6 that the HPFs pass the OOK modulated signal while attenuate the CMTN to lower than 0.75 V of impulse noise. The reference voltage of the last HPF is selected to be 200 mV lower than the threshold voltage (V_{th}) of the squarer input NMOSs transistors. This results in approximately 0.58 V of peak impulse noise at the squarer's input that is lower than the V_{th}; therefore, it does merely affect the output squarer as circled in Figure 5.6. Finally, a hysteresis comparator eliminates the remaining CMTN effects and protect the output logic state.

5.5 Measurement Results

The Hall-based digital isolator with on-chip coil is composed of two dices. A micrograph of the packaged design along with the fabricated dices in AMS 0.35 µm technology is shown in Figure 5.7. Excluding pad area, the Tx and Rx circuits occupy an area of $100 \times 70\ \mu m^2$ and $265 \times 185\ \mu m^2$, respectively. The integrated spiral coil of the Tx circuit has an area of $156 \times 156\ \mu m^2$, 12 nH of inductance, and resistance. The integrated coil has 80 Ω of resistance and is connected in series with a 3 kΩ resistor to limit the coil peak current flow. The measured

sensitivity of the sensor is 0.032 $\frac{V}{mA \times T}$. Part of the Rx circuit is located under this coil to minimize the inductive effect as well as parasitic capacitance of wiring between the sensor and coil. A pad containing no metal-1 to metal-3 is considered for the coil connections and Rx circuits located under the coil are free from metal-3; therefore above 2 µm of SiO_2 enable the design to tolerate more than 0.9 kV of isolation voltage V_{iso}.

Figure 5.8 demonstrates the measurement setup being employed for the HV test of common-mode transient immunity (CMTI). An HV pulser being connected between the Tx and Rx grounds generates pulses with a peak-to-peak value equal to the HV DC supply. To measure a fully isolated environment, an off-package isolated DC-DC converter "RM-3.305S" is employed to power up the Tx side. The ground levels of the HV and LV-domain is oscillated with 630 V and 12 kV/µs slew rate common-mode voltage. The DEI PVX-4140 is equipped with a 1:1000 divider socket for monitoring the generated pulse since an oscilloscope cannot probe the high-voltage pulses. The CMTI test results for the rise and fall of transient noise during low and high output pulse are shown in Figure 5.9 and a CMTI of 12 kV/µs is achieved for the Hall-based digital isolator. Higher CMTI measurement could not be achieved in this article due to the limited voltage level of HV DC supply test equipment.

Current consumption variation respective with bitrate is demonstrated in Figure 5.10. For measurement purposes, in this work, connection between the Tx circuit and the integrated coil

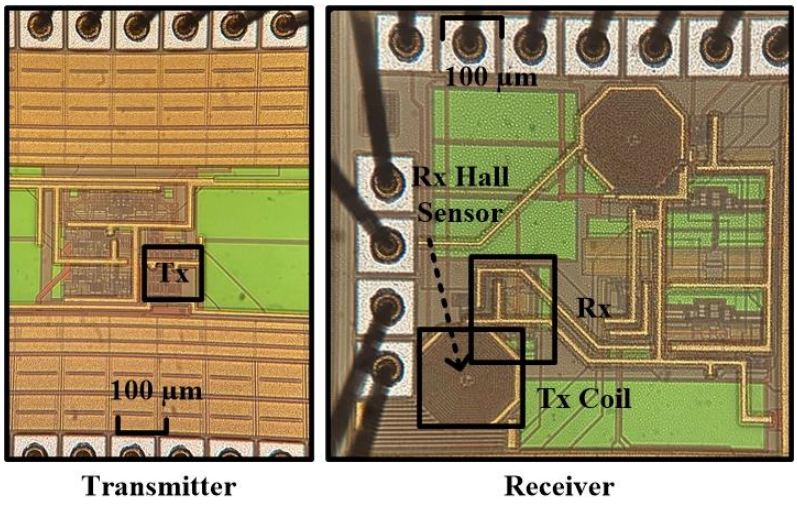

Figure 5.7 Micrograph of the transmitter and receiver chips

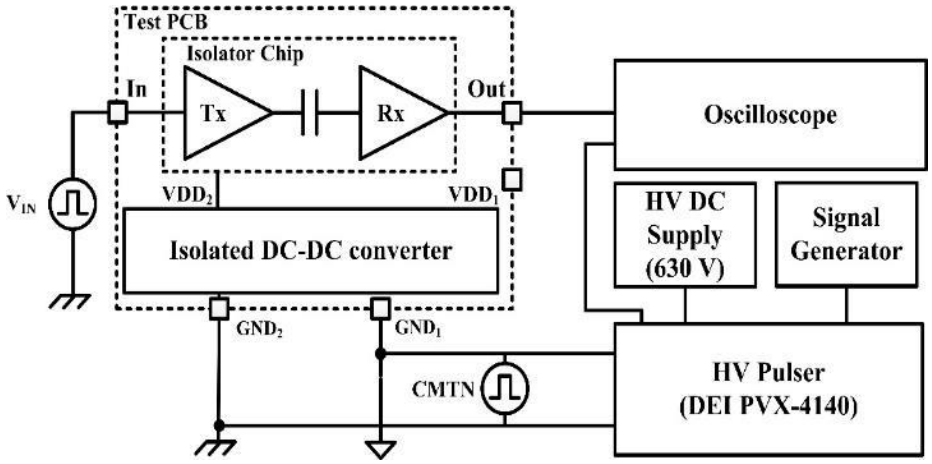

Figure 5.8 CMTI measurement setup

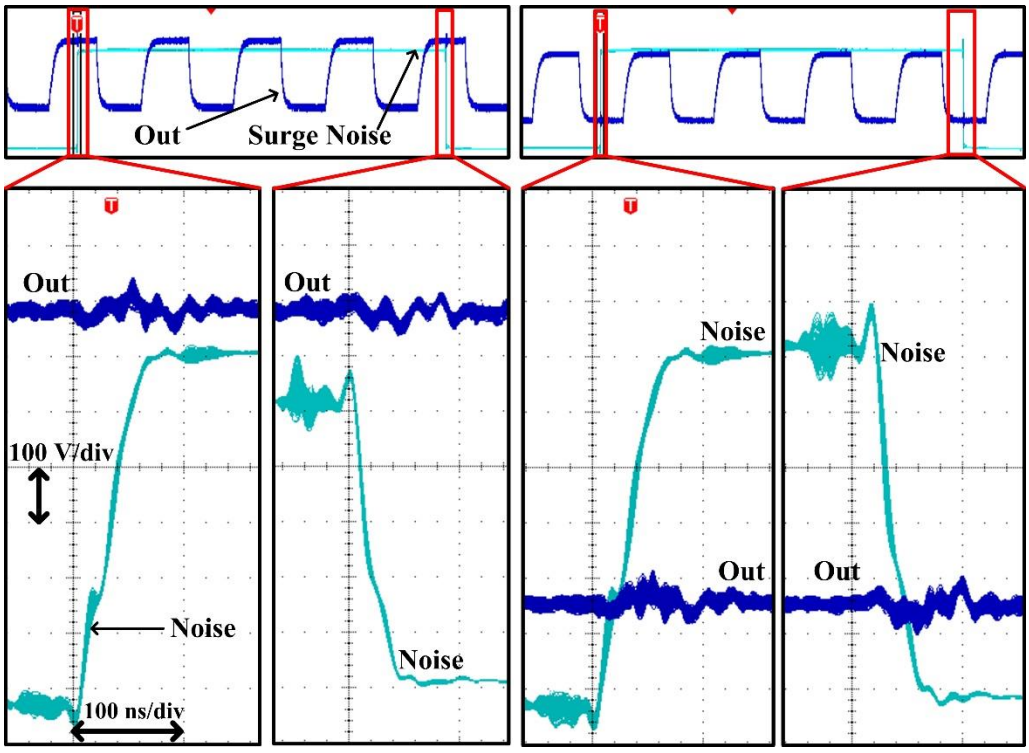

Figure 5.9 CMTI test result for rising and falling edge when output state is high or low

located on the Rx dice is made through the PCB of the measurement setup, which adds extra parasitic capacitance on the transmitter nodes. This has a great impact on the Tx consumption, particularly at high bitrates. The reported bitrate is measured at supply voltages of 3.3V and an input signal of 10-MHz square wave (equivalent to 20 Mbps toggle pattern).

Figure 5.11(a) demonstrates the variation of propagation delay respective to temperature. At room temperature, 27 ns propagation delay is obtained which varies with the rate of 20 $\frac{ps}{°C}$. Variation of the delay respective with supply range of Tx and Rx circuit is also shown in Figure 5.11(b-c). Increasing supply voltage on the Tx side forces more current through the coil and increases the magnitude of the received signal on the Rx side, so it decreases the delay. The achieved data rate, as well as delay, are bounded by the bandwidth of the LNA which limits the OOK modulation frequency, and further increasing of the modulation frequency can increase the bitrate and lower the delay.

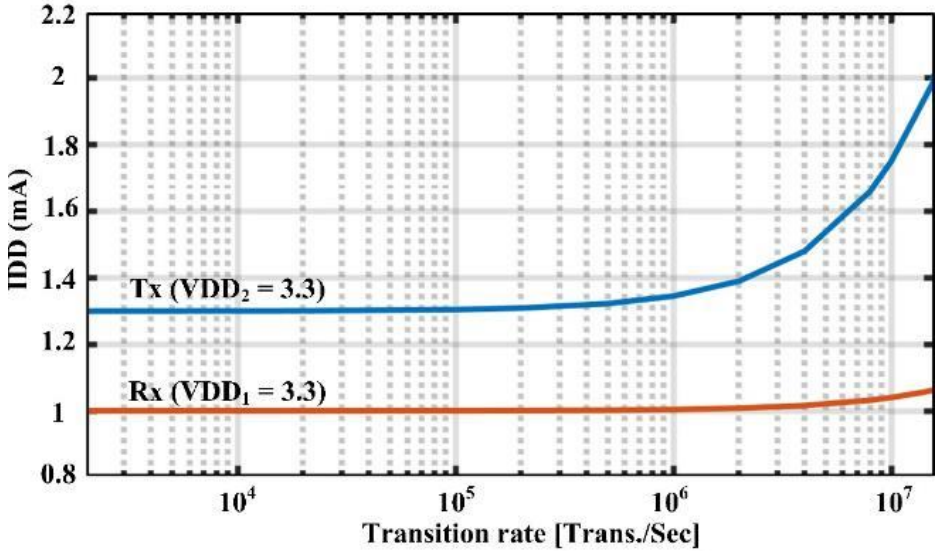

Figure 5.10 Current consumption versus bitrate for the Tx and Rx circuit

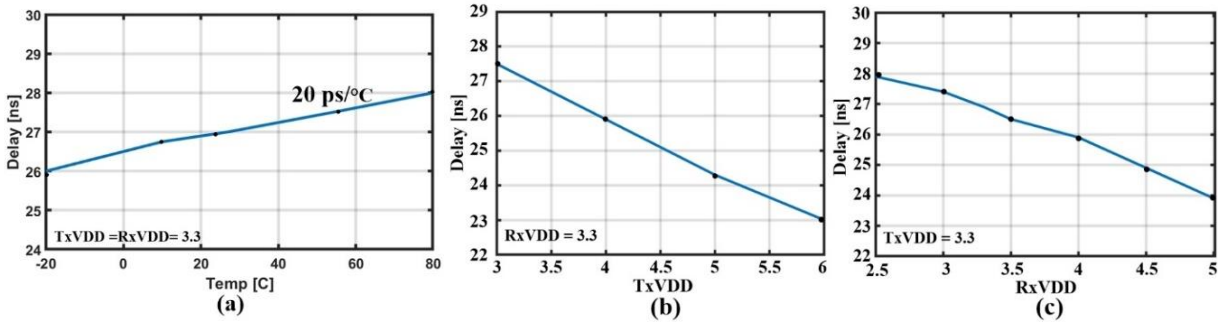

Figure 5.11 Propagation delay versus (a) temperature, (b) Tx supply variation, and (c) Rx supply range

The performance summary of the work is shown in Table 5.2. For purpose of comparison, medium-bitrate industrial products and the smallest transmitter size arts are selected. Kaeriyama et al. [79] presented the smallest on-chip coil for an inductive digital isolator. The reported Hall based digital isolator, in comparison with other arts, has the smallest transmitter area. Unlike transformer-based or capacitive-based isolators, this approach does not require a secondary coil or a capacitive plate and allows the Rx circuitry to be fabricated under the coil which further reduces the consumed area. These miniaturizations make the device suitable for multi-channel digital isolators. Unlike GMR/TMR-based digital isolator that uses layers of deposited ferrite material, this approach uses

Table 5.2 Performance Summary

Parameter	Kaeriyama, et al. [79]	ADuM131 [80, 81]	Si80xx [82]	ISO72X [83]	IL01x [84]	**This work**
Isolation Type	Inductive	Inductive	Capacitive	Capacitive	TMR	Hall Effect
Isolation material	SiO_2	Polyimide	SiO_2	SiO_2	-	SiO_2
Post Processing	No	Yes	No	No	Yes	No
# of Dies	2	3	2	2	-	2
Isolator size Ø [µm]	230	2x 500[(1)]	-	241[(1)]	-	156
Maximum bitrate [Mbps]	250	10	10	100-150	10	20
Propagation delay [ns]	5.9	20-60	40	10	25	27
CMTI $\left[\frac{kV}{\mu s}\right]$	35	35	50	50	50	12<
Architecture	Pulse Polarity	-	-	OOK	-	OOK
IDD (Tx+Rx) @ DC [mA][(2)]	1.6	2	1.98	4.3	0.3	2
IDD (Tx+Rx), @ 10 Mbps 15 pF load [mA] [(2)]	1.9	4.5	2.3	5.6	1.8	2.9

[(1)] Size is estimated based on chip photo.

[(2)] At $VDD_1 = VDD_2 = 3.3$

no post-processing, so no proprietary process is needed which makes it cost-effective.

Integration in a smaller process with more metal layers (i.e. 130 nm) helps reduce the coil area by doubling the layers of the integrated spiral coil to maintain the magnetic field strength; thicker oxide would also increase the V_{iso}, and inherently lower noise and supply voltage of smaller processes can reduce the power consumption. Finally, the silicon on isolator process helps isolate n-p substrates and avoids crosstalk in a multi-channel isolator.

5.6 Conclusion

To the author's best knowledge, the reported work is a proof of concept of an approach in using integrated CMOS Hall sensors in digital isolators. The proposed architecture serves applications including clock recovery, isolated DC-DC converter, and I^2C with the maximum bitrate of 20 Mbps. The miniature footprint of the transmitter coil as well as the miniature size of the Hall sensor that allows placement of the receiver circuitry under the coil are unique parameters that significantly reduced the CMOS area and make the approach suitable for multi-channel digital isolator and dense integration. The design achieves a CMTI of greater than 12 kV/µs with a propagation delay of 27 ns.

The applied methodology in sensor implementation enabled the sensor to receive the on-off keying (OOK) modulation frequency of 100 MHz which is beyond most of the reported frequency response of Hall sensors. Although the implemented approach is not yet suitable for high or ultra-high bitrate applications, further increase of the bitrate is achievable by the methodologies described in this article for conserving the Hall plate bandwidth and modification of the receiver circuitry.

CHAPTER 6 ARTICLE 3: A FULLY INTEGRATED LOW-POWER HALL-BASED ISOLATION AMPLIFIER WITH IMR GREATER THAN 120 dB

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This article presents the full integration of the Hall-based isolation amplifier implemented in AMS 0.35 µm technology. The sensor optimization is performed by a COMSOL finite element model (FEM). Magnetic field of the integrated coil is simulated by ANSYS and the crosstalk free distance for integration of multiple sensing unit is defined. Also, to satisfy the objective of isolated clock recovery design, a robust all-integrated Hall-based digital isolator is implemented (reported in chapter 4). The final products achieve a minimal power consumption with minimal footprint while using no post-processing and off-chip components. The manuscript was submitted to IEEE Transaction on Circuits and Systems as a Regular Paper in August 2021.

6.1 Abstract

A CMOS Hall-based fully integrated isolation amplifier for differential voltage sensing is presented in this work. The design is fabricated in AMS 0.35 µm CMOS process in which the high voltage (HV) side of the amplifier contains a coil driver while the low voltage (LV) side includes a Hall-effect sensor, low-noise amplifier, programmable-gain amplifier, filter, and chopper switches. Another Hall sensor performs digital isolation using on-off keying (OOK) technique for clock recovery. The fabricated chips are wire-bonded on a PGA68 package. The introduced prototype achieves above 120 dB of isolation mode rejection (IMR) at 60 Hz and operates at continuous isolation working voltage of 0.6 kV. It also has maximum nonlinearity of 0.6 %, an input-referred offset of 1 mV, a 40 dB full-scale signal-to-noise ratio in 40 kHz bandwidth, and a spurious-free dynamic range of 64 dB. The silicon area for each of the two separate dices employed

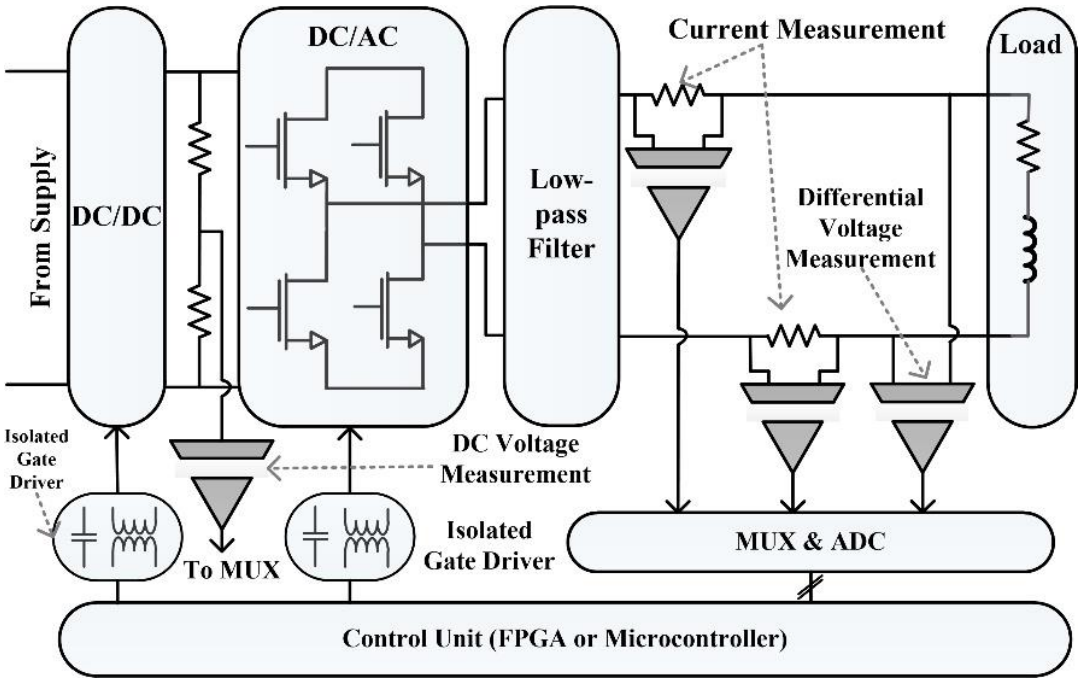

Figure 6.1 Block diagram of a sensor interface unit

for the LV and HV side of the isolation amplifier is 1 mm^2 with a power consumption of 9.9 mW and 7.6 mW, respectively. The achieved miniaturized size of the isolation components, as well as their significantly low-power consumption, ensure the suitability of the presented isolation amplifier for multi-channel readout circuit applications.

Index Terms: Isolation amplifier, voltage sensing, current sensing, galvanic isolation, chopper amplifier, digital isolator, integrated spiral coil, CMOS Hall sensor.

6.2 Introduction

Sensor interfaces are elemental in several applications including robotic, industrial control, and aerospace where delivering stable high power to sensors and actuators is required. Accordingly, voltages and currents delivered to these loads are monitored for further processing [85]. The environmental working conditions of these actuators enforce sensor interfaces to satisfy certain safety insulation standards such as surge withstand voltage and continuous isolation working voltage V_{iso} through their operating lifetime [63].

A typical sensor interface unit as shown in Figure 6.1 incorporates numbers of isolated voltage and current reading units. One unit could be employed to read the DC input level of the rectifier bridge and others to monitor the delivered power or detect a fault condition. One of the viable current reading techniques is based on combining a Hall-effect sensor with a current transformer (CT) as it can detect both DC and AC signals [33]. However, for applications where multiple input currents are being monitored, the overall packaging size becomes bulky due to the large footprint of the CT-Hall based sensing. Furthermore, being limited to current sensing, this approach obliges designers to employ other mechanisms including resistor divider or isolation amplifiers for voltage monitoring, which results in a non-uniform design. An attractive solution to unify designs is achieved by applying shunt-based current sensing which also has features including small footprint, rapid response, and DC monitoring [33]. To unify power monitoring designs, a programmable isolation amplifier can be employed for differential voltage and shunt-based current sensing.

Isolation amplifiers, which transmit digitized data across the isolation medium, are very advantageous in terms of signal resolution and bandwidth [14, 15]. However, a single analog to digital converter (ADC) on the high voltage (HV) side can consume a minimum of 100 mW of power [14] making them power-consuming for multi-channel voltage and current sensing applications, particularly if large bandwidths are not of interests. In the non-ADC type of isolation amplifiers (IA), analog data are transmitted over the galvanic medium either directly like optocouplers or after modulation. Other than simple design approaches, optocouplers have outstanding performance in terms of linearity, noise, and drift performance [21]. However, there are concerns regarding their effective lifetime due to electrical and thermal stresses [5]. The transformer-based approach employs modulation to transmit DC signal [86] where a good signal-to-noise (SNR) is obtained at a price of very high wattage and bulky designs as the transformer must be sized to achieve a high quality factor. This makes them not suitable for multi-channel sensor interfaces.

This paper presents an IA based on a on-chip spiral coil and CMOS Hall sensor, which is suitable for amplifying shunt-based current and differential voltage sensing. The remaining of this paper is organized as follows: Section II describes the overall system architecture including integrated spiral coils, optimization of the cross-shaped Hall-effect sensor, and clock recovery. The measurement results are stated in Section III, and conclusion remarks appear in Section IV.

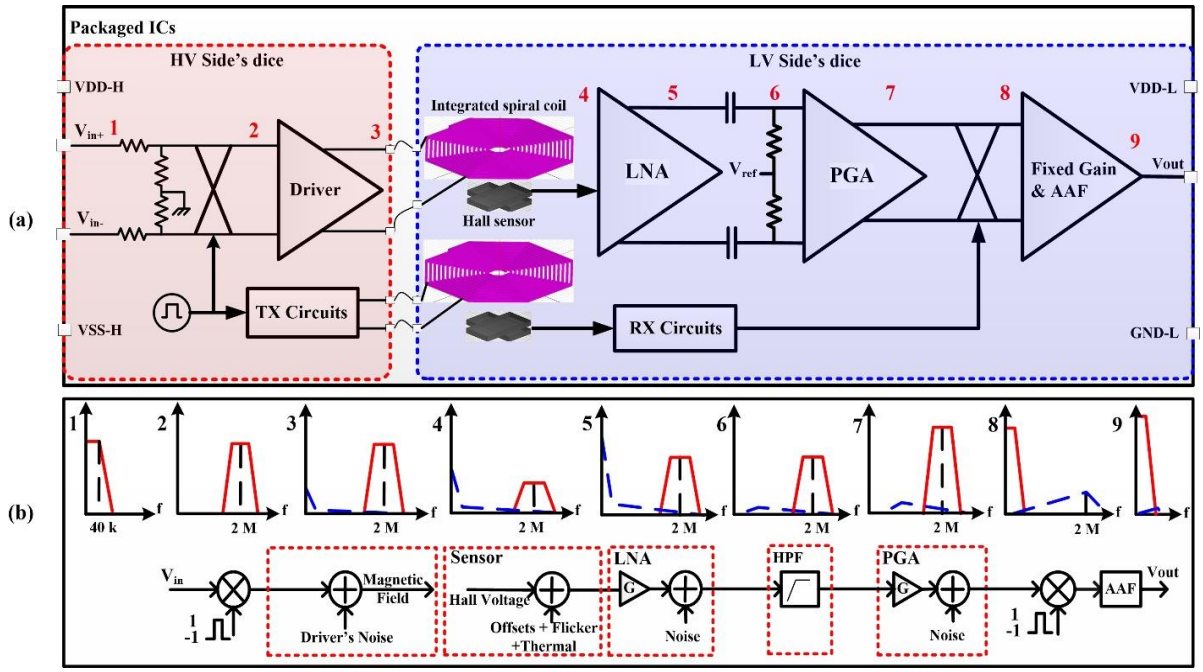

Figure 6.2 (a) Architecture of the proposed isolation amplifier, and (b) signal spectrum of the structure presented at different nodes

6.3 Design and Implementation

6.3.1 System Architecture

Figure 6.2(a) illustrates the proposed system-in package (SiP) solution that includes two dices where one integrates a driver circuit and the other a Hall-effect circuit with corresponding amplification stages. On the HV side's dice, the chopper switches formed by transmission gates chop input signal at 2 MHz and send it to the mid-band region. Then, an amplifier drives the integrated spiral coils formed by intermetal layers of the LV dice. The Hall sensor located under the center of the coil receives the transmitted magnetic field and generates a deflected voltage. Next, the sensed voltage goes through amplification stages starting from the low noise amplifier (LNA). The resulting amplified DC offset and flicker noise of the sensor are removed by the passive high-pass filter (HPF) with a 500 kHz cut-off frequency, and a programmable gain amplifier (PGA) tunes the signal to be suitable for the input dynamic range of an ADC. Then, a chopper demodulator brings the amplified signal back to the baseband region and a second-order anti-aliasing filter (AAF) attenuates the mirrored spectral components and switching overshoots. Finally, a clock recovery circuit using a Hall-effect sensor forms a digital isolator with on-off keying (OOK) modulator to transmit the clocking signal generated on the HV side to the LV side.

The frequency spectrum of the IA at different nodes along the analog modulation/demodulation chain is demonstrated in Figure 6.2(b). The modulation of node 2 and demodulation of node 8 allow the transmission of the baseband input signal without adding the DC offset and flicker noise of the amplifier's chain including the coil driver, Hall sensor, LNA, and PGA as shown in Figure 6.2(b) nodes 3-5. The high pass filtering of node 6 removes the DC offset and weakens the amplified 1/f noise of the sensor and LNA to protect the amplifier from saturation. Additionally, the chopper technique and the high-pass filtering, eliminate inherent offset drift of the Hall sensors and the DC geomagnetic field do not have any effect on the amplifier.

6.3.2 Driver Circuit

A high input impedance is needed for a shunt resistor current sensing application, so an instrumentation amplifier is chosen for the coil driver in Figure 6.3. In parallel, as the system overall SNR in this Hall-based isolated voltage sensing is proportional to the strength of the generated magnetic field, the magnetic coil must be sourced with a sufficient current to fulfill the required SNR of the application. As a result, the gain resistor (R_g) can be adjusted to deliver the required coil current for different differential input voltage ranges. Moreover, to preserve the current consumption of the HV side, a class AB output stage, that conducts only a half-wave signal, is employed for the output stage. For large input signals, the amplifier is connected to a resistor divider as shown in Figure 6.2(a), also rail-to-rail architecture is chosen for the input differential pairs of the driver amplifier. The driver circuit has an input-referred noise of 25 nV/$\sqrt{\text{Hz}}$ and a gain-bandwidth product of 40 MHz.

6.3.3 Integrated Spiral Coils

Creating a magnetic field in the Hall-based isolation amplifier involves several challenges. First, the amplifier's signal quality is directly proportional to the field, so an adequate magnetic field is required to achieve a reasonable SNR. Second, the coil behaves like a series of resistive-inductive loads (i.e. a low-pass filter); therefore, to avoid attenuating the carrier signal, the magnetic coil must have low inductance. Finally, the coil must have a small footprint to lower the packaging size, simplify packaging complexity, and reduce cost. Therefore, on top of the Hall plate, a double layer of integrated hexagonal spiral coil is fabricated with specifications listed in Table 6.1. To determine

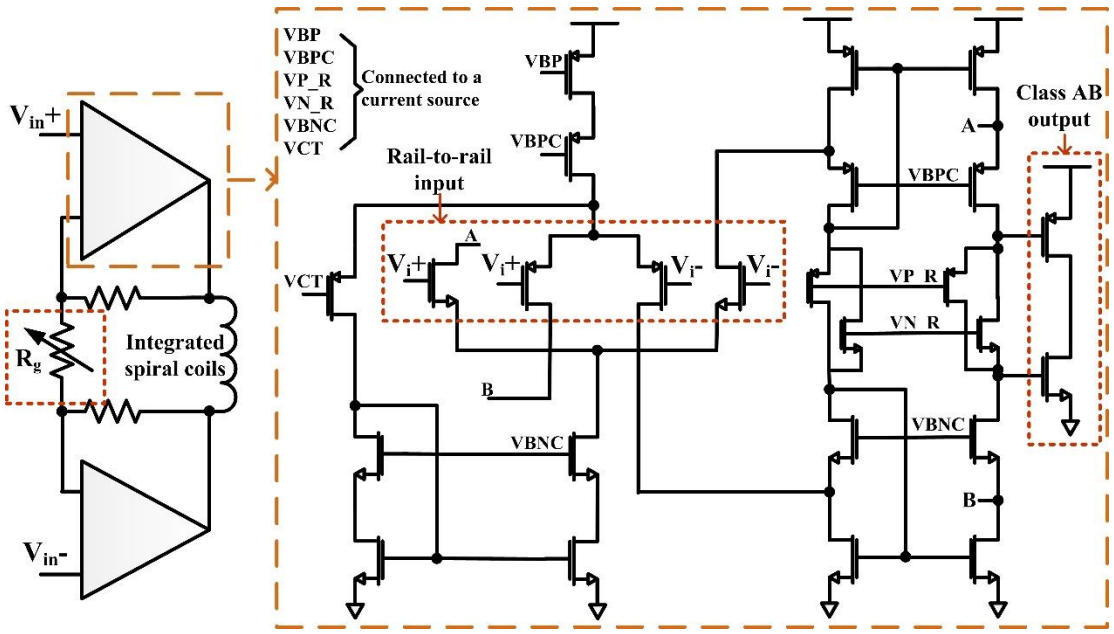

Figure 6.3 Schematic of the coil driver

the field strength of the coil, an ANSYS simulation is performed for the peak current of 2.5 mA, showing that the coil can generate a field of 1.25 mT according to the result of Figure 6.4(a). Besides, Hall plates are sensitive to perpendicular magnetic fields, and following Figure 6.4(b), the magnetic flux is vertical at the coil's center where the sensor is placed.

Having process CMOS oxide as an isolation barrier is a common industrial practice (e.g. Texas Instrument ISO72xx [83]). Based on the oxide deterioration profile reported in [61], one micron of oxide for a mean time to failure (MTTF) of 20 years has an isolation breakdown voltage of 0.45 MV/mm; further increase of V_{iso} can be obtained through a smaller process with a greater number of metal layers and consequently a thicker galvanic barrier. Doubling the number of serried spiral coils in such a process doubles the generated magnetic field strength and adds 6 dB to the SNR.

The other requirement from the Hall-based isolation amplifier is the ability to perform multi-channel isolated reading by placing several dices next to each other in the same package or using multiple transmitter coils in a single dice on the LV side. To determine this capability, the integrated Hall sensors must be crosstalk-free from the neighboring coils. For a 1 Hz bandwidth and an SNR of 95 dB, to place the sensor in a crosstalk-free distance, the far-field must be 95 dB lower than the adjacent coil; consequently, simulation of far-field strength of the integrated coil in

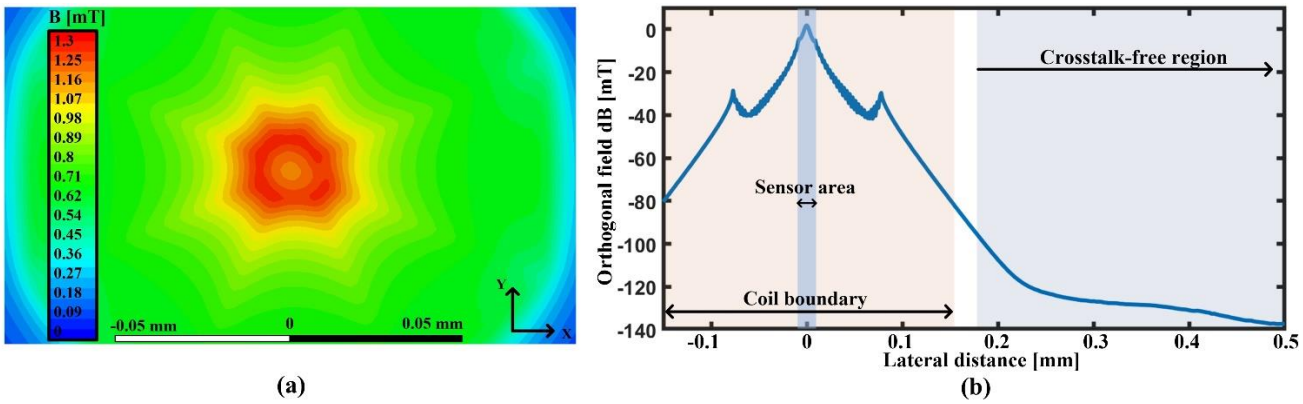

Figure 6.4 (a) ANSYS simulation showing magnetic field of the integrated spiral coil for 2.5 mA of current and at 5 µm distance, and (b) perpendicular field to the substrate area respective with lateral distance

Table 6.1 Parameters of the Integrated Spiral Coils

Parameter	Metal 3	Metal 4
Number of turns	22	15
Turn spacing (μm)	0.5	2
Wire width (μm)	2.5	2.5
Inner diameter (μm)	20	22
Current density (mA/μm)	1	1.5
Outer diameter (μm)	154	158

logarithmic scale is shown Figure 6.4(b). Based on this figure, multiple transmitter coils and receiver sensors can be placed 350 µm apart from each other.

6.3.4 Sensor Implementation

The Hall sensor converts the received magnetic field to an electrical signal via the Lorentz force, so optimization toward sensitivity and minimizing the noise floor improve the overall SNR of the system. Optimal sizing of cross-shaped Hall effect sensor respective with its width (W) and length (L) has been reported by Xu, et al. [87]. However, other parameters, including the contact width of the signal nodes (C_W) and the sensor area, contribute to the Hall sensitivity. The variation of the sensitivity with respect to the area is described by Crescentini, et al. [78]; however, based on Figure 6.4(b) orthogonal vector of the generated magnetic field to the sensor's surface attenuates when

the sensor's area becomes larger than the inner diameter of the integrated coil. Besides, reported by Xu and Pan [41], expanding sensor size, decreases the sensor's 3 dB bandwidth.

To investigate the relationship between sensitivity and contact size, a COMSOL simulation is performed using an anisotropic conductivity tensor σ modeled by a 3x3 matrix [88]:

$$\begin{bmatrix} \sigma_{xx} & \sigma_{xy} & \sigma_{xz} \\ \sigma_{yx} & \sigma_{yy} & \sigma_{yz} \\ \sigma_{zx} & \sigma_{zy} & \sigma_{zz} \end{bmatrix} = \begin{bmatrix} \frac{\sigma_0}{1+(R_H B\sigma_0)^2} & \frac{R_H B\sigma_0{}^2}{1+(R_H B\sigma_0)^2} & 0 \\ \frac{R_H B\sigma_0{}^2}{1+(R_H B\sigma_0)^2} & \frac{\sigma_0}{1+(R_H B\sigma_0)^2} & 0 \\ 0 & 0 & \sigma_0 \end{bmatrix} \quad (6.1)$$

where R_H is the Hall coefficient, σ_0 is the conductivity, and B is the magnetic field. Figure 6.5 shows the COMSOL simulation of the sensor sensitivity versus contact size. This simulation is performed based on the optimum ratio of L/W using methodologies described by Xu, et al. [87], for W and L of 19.3 µm and 11.2 µm, respectively. The current source contact sizes are equal to W. Based on Figure 6.5, minimizing C_W increases the sensor sensitivity, i.e., a wide C_W shortens the voltage equipotential line deflection over the sensing nodes, leading to a lower sensitivity. As a result, a narrow C_W of 1.2 µm is employed for the sensor contacts. Table 6.2 summarizes the process parameters being used in the simulation.

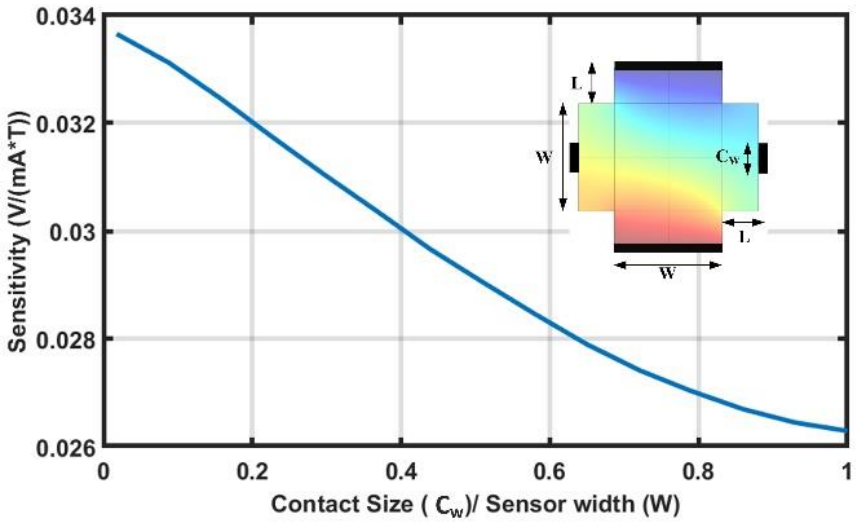

Figure 6.5 COMSOL simulation of the cross-shape Hall sensor respective with various signal contact size for an optimum L/W ratio. The biasing contacts are equal to the sensor's width and located at extremities of the arm

Table 6.2 Model Parameters of the COMSOL Simulation Based on the Available Technology and Field Strength of the Miniature Coil

Symbol	Parameter	Value
n [cm^{-3}]	Dopping Concentration	$1.28e^{17}$
I [mA]	Biasing Current	2
B [mT]	Peak Magnetic field of the miniature coil	1.25
R_s	N-Well Sheet Resistance	1e3
t [μm]	N-Well Thickness	2
σ_0 [$\frac{S}{m}$]	Conductivity	$\frac{1}{R_S\, t}$
R_H	Hall Coefficient	$\frac{1}{nq}$

6.3.5 Analog Receiver Circuitry

To ensure that Hall node voltages are within the input swing range of the LNA, common-mode feedback (CMFB) is employed as shown in Figure 6.6(a). Also, to avoid adding any capacitive load on the Hall signal nodes and limiting the bandwidth of the sensor, DC voltage reading of the CMFB branch is performed on the Hall current nodes.

CMOS Hall sensors have inherently a low sensitivity and a high DC offset. Hence, to optimally capture the Hall voltage induced by the generated magnetic field, the first amplifying stage must have a low input-referred noise (VN_{in}). Since the input signal of the LNA is at the modulation frequency of 2 MHz, the dominant noise of the sensor is thermal noise. Knowing that the sensor has a resistivity of 1.4 kΩ, 4.7 nV/$\sqrt{\text{Hz}}$ of thermal noise is expected from the sensor, so the amplifier must be designed to satisfy a VN_{in} of lower than the sensor's thermal noise at modulation frequency to not contaminate the received signal. Furthermore, the amplifier must have a sufficiently large bandwidth to not attenuate the received modulated signal. Considering these limits, available conventional instrumentation amplifier with triple operational amplifiers suffers

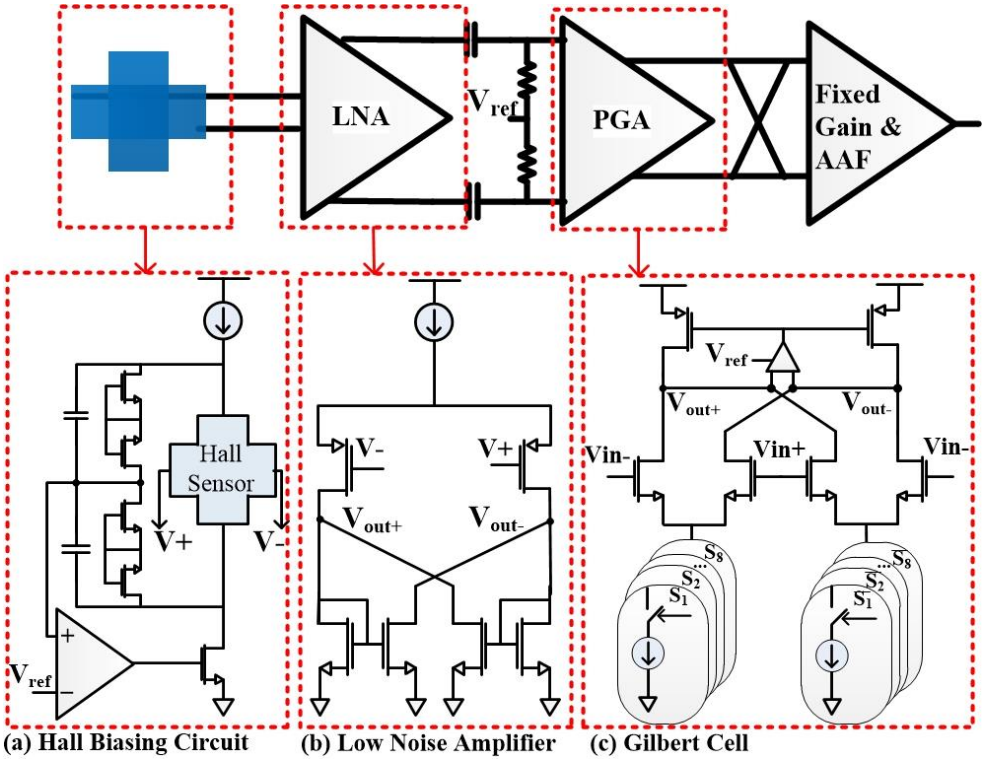

Figure 6.6 (a) Biasing circuit of the Hall plate, (b) structure of the cross-coupled preamplifier, and (c) topology of the integrated dB-linear PGA

from high consumption in large bandwidth. Moreover, the sensor does not have the driving capability, which dictates the amplifier to have a high input impedance. Therefore, amplifiers with capacitive coupling or feedback resistors attenuate the bandwidth spectrum of the Hall sensor. To satisfy the wide bandwidth as well as the high input impedance, a cross-coupled architecture is implemented as depicted in Figure 6.6(b). Due to the inherent low 1/f noise, PMOS transistors are selected as the differential pair for the architecture, and they are sized to have an input-referred thermal noise of 3 nV/$\sqrt{\text{Hz}}$. Also, without active offset canceler circuitry, direct amplification with the required high can saturates the amplifier. Therefore, a low gain of 26 dB is considered for the pre-amplifier stage. The designed cross-coupled architecture has 64 dB of CMRR and a 3-dB bandwidth of 10 MHz.

To adapt the output of the amplifier to ADCs with various input dynamic ranges or operating voltages, the LV side is equipped with a PGA. Also, the sensitivity of the sensor and the generated magnetic field of the miniature coil are not precisely quantified before the measurement, so the

PGA can compensate for these variations. Design constraints impose the PGA to have a constant and wide bandwidth for all gain stages as well as a high input impedance. Neither of these features could be obtained by the resistive or capacitive closed-loop topologies. As a result, a folded Gilbert cell of Figure 6.6(c) with active load is selected for this design. To achieve dB-linear gain variation using a 3-bit gain setting, a dB-linear function is obtained by varying tail current sources of the Gilbert cell branch. Current sources are switched by transmission gates, and they operate in parallel.

The output stage is composed of an impedance matching stage, a fixed gain amplifier, and an AAF. To properly filter the spurious signal resulting from the modulation/demodulation process, a second-order Butterworth AAF with a Sallen-Key topology and a 40 kHz cutoff frequency eliminates the clocking harmonics.

6.3.6 Hall-Based Digital Isolator

The integrable types of isolation barriers that are widely used as digital isolators are capacitive and inductive media. Capacitors, as two-terminal devices, transmit both signal and common-mode noises concurrently. However, the different coupling mechanism of transformers as 4-terminal devices achieves an intrinsically higher common-mode transient immunity (CMTI). An inductive digital isolator, using OOK approach achieves low propagation delay, EMI, and high noise immunity [89]. Self-resonant frequency is the efficient approach being used in the OOK modulator [14]. However, by miniaturizing the transformer size, the transmitter can have above GHz of self-resonance frequency. Although that will increase the bitrate of the digital isolator and minimizes the propagation delay, any added parasitic capacitance on the resonant nodes can damp the resonance frequency, so there will be a challenging consideration in wire-bonding, dice distances, and pad capacitances; however, such high bitrates are not required for this application. Consequently, in this design, an application-specific, novel Hall-based digital isolator using OOK modulation is employed.

Transferring an isolated clock across a galvanic barrier presents considerable challenges, as the transmitted and received clocking signals must be precisely synchronized. Figure 6.7 demonstrates the full clock recovery circuit in which the transceiver (Tx) is located on the HV side. First, an astable multivibrator generates a 64 MHz clocking signal as the carrier for the OOK modulation. Then, 5 stages of D flip-flop frequency dividers lower the frequency of the clocking signal and

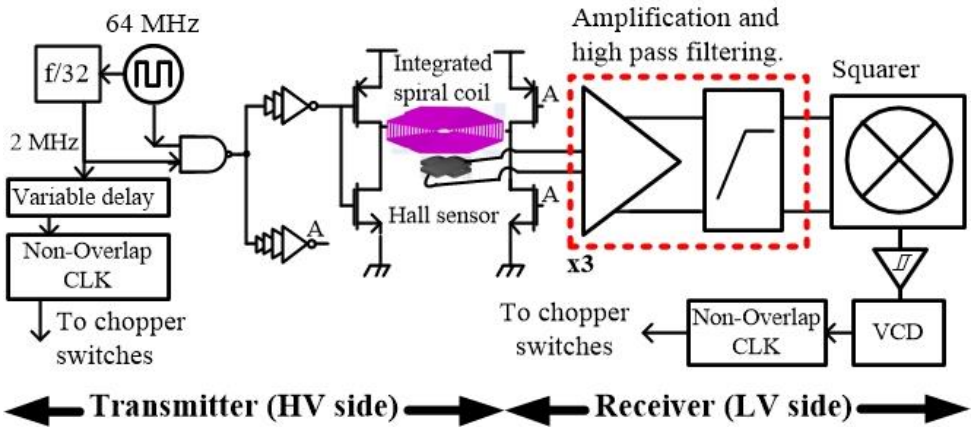

Figure 6.7 Structure of the Hall-based digital isolator using OOK modulator

modulate chopper switches. The weighted inverters drive the integrated spiral coil, and on the receiver side (Rx), the Hall-effect sensor detects the signal. Three stages of amplification and HPF amplifies the modulated signal and eliminates the low-frequency noises, respectively. Finally, a squarer circuit rectifies the modulated signal.

Due to the digital nature and lower required resolution in the receiver circuit, the coil and sensor can be fed by a much smaller current than the analog path. Therefore, to preserve power, the Hall sensor is biased by 0.5 mA of current, and the coil current is limited to 1 mA through a limiting resistor. For the same reason, the integrated coil has the same architecture as described in section II-C but is only formed by Metal-4 and leaving above 2 μm of SiO_2 for the isolation barrier. So, the digital isolated link can tolerate above 900 V of V_{iso}.

For any chopper circuit, it is essential to minimize the phase delay between modulator and demodulator switches, failing in adjusting the delay results in degraded amplifier's gain. Therefore, the propagation delay of the digital isolator must match the phase shift of the analog path that appears between the chopper modulator and demodulator at the 2 MHz modulation frequency. Sources of the phase shift are the driver and LV side's amplifiers. Although the digital isolator's propagation delay compensates the phase shift, on the demodulator side, a voltage-controlled delay (VCD) allows to match the phase shift and the propagation delay.

6.4 Measurement Results

The fully integrated Hall-based isolation amplifier composed of two dices is designed for voltage and current reading of industrial read-back circuits. A micrograph of the packaged design along with the fabricated dices in AMS 0.35 µm technology is shown in Figure 6.8. Each of the HV and LV dices has 1x1 mm^2. The HV-side is powered by a 2 V supply while drawing 3.8 mA, and the LV-side dice consumes 3 mA from a 3.3 V supply.

The sensor response to a variable magnetic field is shown in Figure 6.9. In this measurement, the output of the amplifier is measured at 2 MHz and 2.6 mT peak-to-peak magnetic field, and the process is repeated by decreasing the coil current. Based on the 80 dB gain of the amplifier's overall chain (i.e. LNA, PGA, and fixed gain stage) and 2 mA of biasing current, the sensor has a sensitivity of 0.032 $\frac{V}{mA \times T}$ which complies with the COMSOL simulation of Figure 6.5.

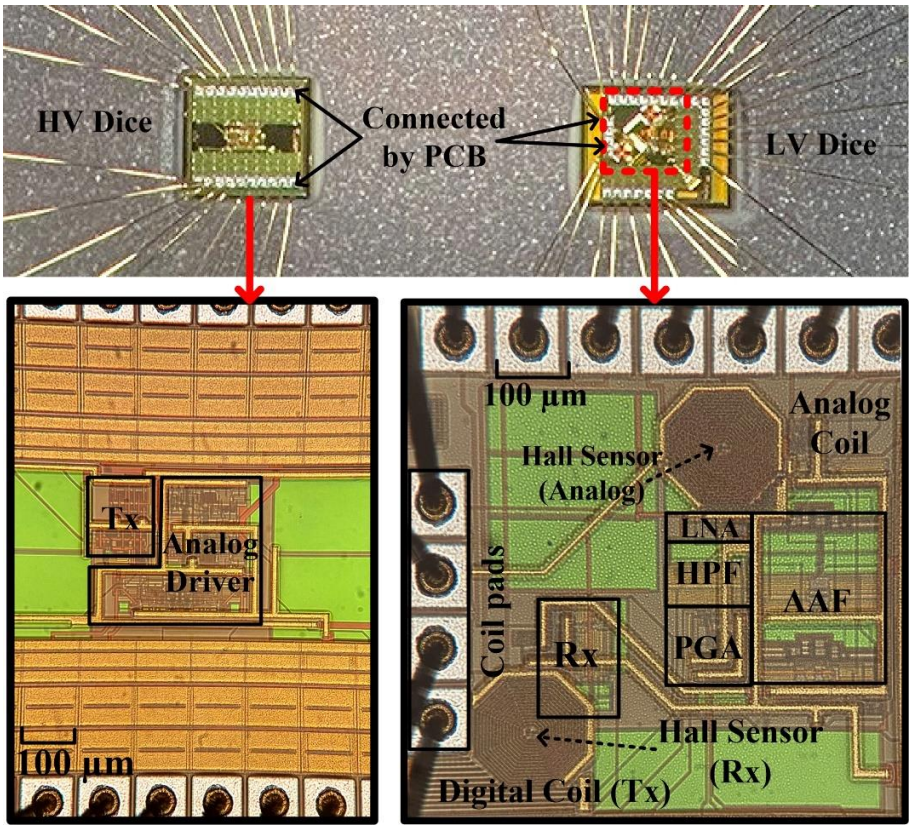

Figure 6.8 Micrograph of the packaged design using PGA68

The Hall-based approach of the proposed amplifier raises a concern regarding sensor saturation in presence of very high external magnetic noise. This saturation can be observed as sensitivity variation or amplifier's gain variation. To measure that, the uncapped package is placed inside GMW 3472 Dipole Electromagnet generating a 0.5 T of magnetic field and no sensitivity drift was observed. One reason is that CMOS Hall sensors are sensitive to more than one Tesla of fields. Also, the low gain of the LNA and high-pass filter protect the amplifier from saturation.

Figure 6.10 demonstrates the measurement setup being employed for HV tests including common-mode transient immunity (CMTI) and isolation mode rejection (IMR). An HV pulser being connected between the HV and LV grounds generates pulses with a peak-to-peak value equal to the HV DC supply. To measure a fully isolated environment, an off-package isolated DC-DC converter "RM-3.305S" is employed to power up the HV side. Any missing or addition of clocking cycle due to common-mode voltage transition momentarily distort the demodulated signal and results in faulty reading. Therefore, the digital isolator must sustain HV transient noises and a measured CMTI of 12 kV/µs is achieved for the Hall-based clock recovery while achieving 35 ns of propagation delay. Higher CMTI measurement could not be achieved in this article due to the limited voltage level of the HV DC supply test equipment. The measurement of the structure IMR is shown in Figure 6.11 and demonstrates above 120 dB of IMR for frequencies lower than 60 Hz.

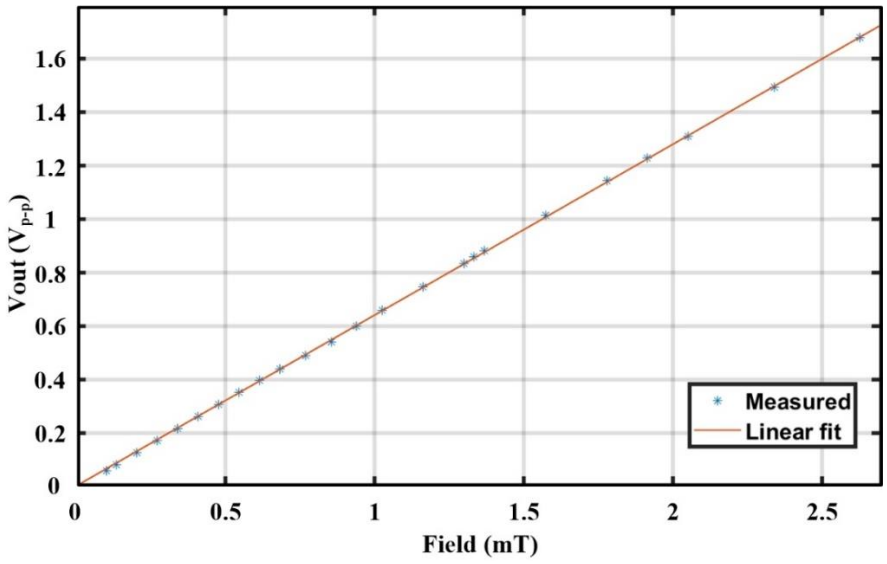

Figure 6.9 Output of the amplifier respective with magnetic field variation measured at 2 MHz of input signal with no modulation

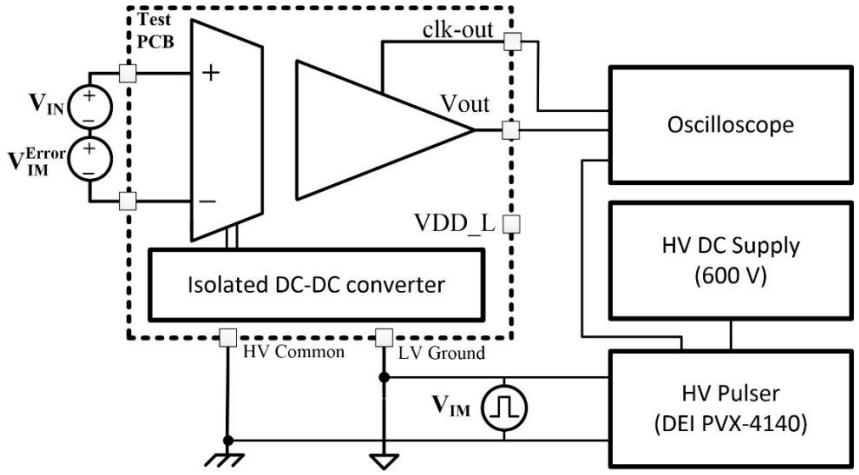

Figure 6.10 Measurement setup employed for HV testing

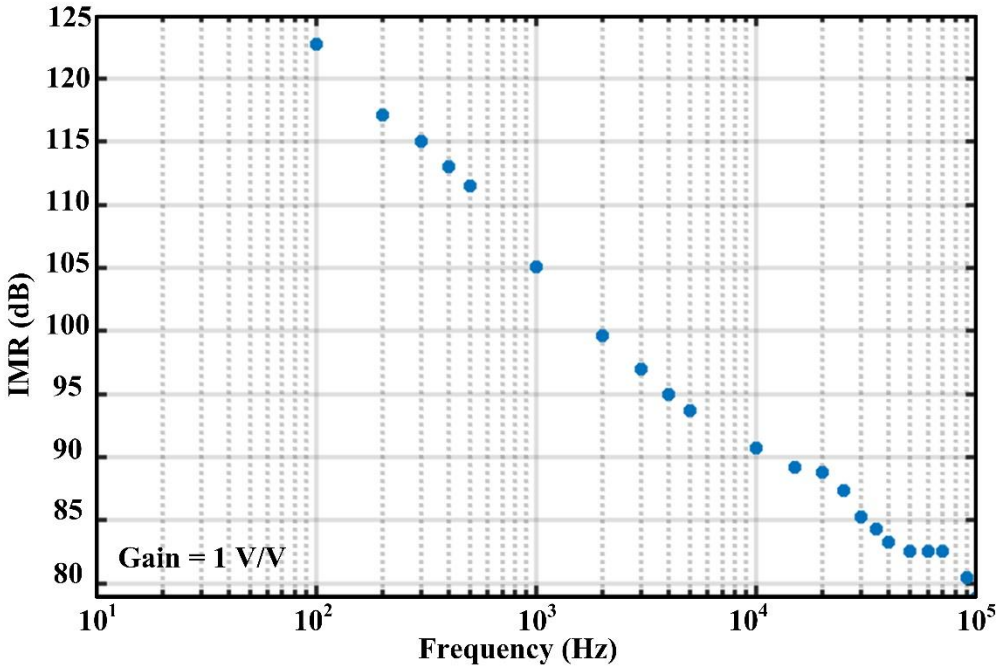

Figure 6.11 Measured isolation mode rejection ratio of the Hall-based isolation voltage amplifier

To characterize the PGA specification of the LV side, an identical test PGA is fabricated, and gain variation of 17 dB to 39.2 dB with 3.16 dB steps is achieved. The 3 bits of gain setting follows a

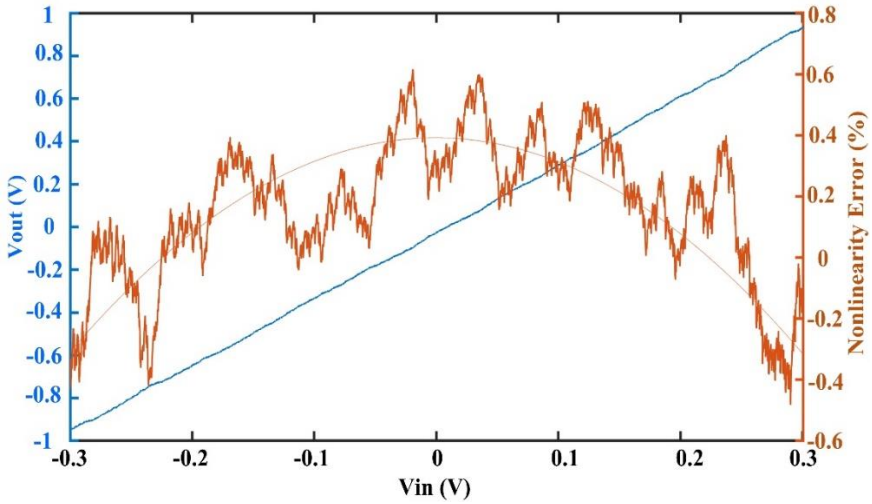

Figure 6.12 Output nonlinearity error for differential input voltage ranging from – 0.3 V to 0.3 V

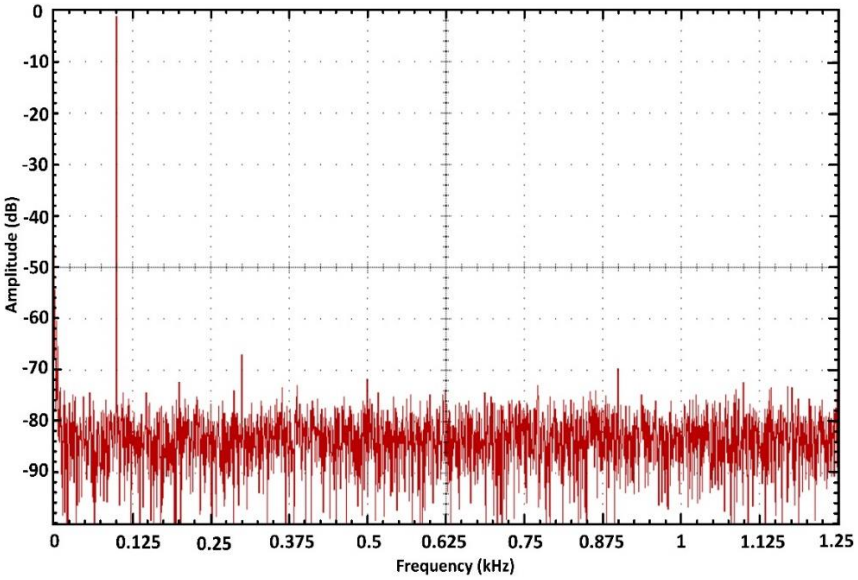

Figure 6.13 Output voltage spectrum of the amplifier for a ±300 mV input signal at 100 Hz

dB-linear function with a maximum 0.3 dB of nonlinearity. The measured overall input-referred offset of the design is 1 mV. Finally, the linear behavior of the Hall sensor with respect to magnetic field allows the amplifier to achieve a maximum nonlinearity of 0.6 %, as can be depicted in Figure 6.12.

The amplifier spectrum for ±300 mV of a 100 Hz input signal is shown in Figure 6.13 which shows an SNR of 86 dB in 1 Hz bandwidth with spurious-free dynamic range (SFDR) of 64 dB. It should be noted that the cumulative thermal noise of the sensor and LNA is about 5.5 nV/$\sqrt{\text{Hz}}$. This noise

is multiplied by a total gain of the amplifier's path approximately creates a -86 dB noise floor of the signal spectrum. Additionally, based on the spectrum graph, the 1/f noise generated by the sensor and the LNA is eliminated due to modulation/demodulation of the input signal.

Table 6.3 Performance Summary

	Tan, et al. [15]	AD210BN [86]	HLSR50-P/SP33 [34]	ISO124 [7]	**This work**
Voltage/ Current	Voltage/ Current	Voltage/ Current	Current	Voltage/ Current	**Voltage/ Current**
Type	Inductive (Digital-SAR)	Inductive (Analog)	Hall Effect	Capacitive (Analog)	**Hall Effect (Analog)**
Isolated supply	Yes	Yes	-	No	**No**
non-linearity %	-	0.01	0.8	0.01	**0.6**
V_{iso}[kV]	0.4	2.5	0.6	1.5	**0.6**
Power [mW] (1)	41.25 (Total)	>750 (Total)	62.7 (Total)	300/300 (HV/LV side)	**7.6/9.9 (HV/LV side)**
IMR @ 60 Hz [dB]	-	100<	-	140	**120<**
Input range [V]	±0.5	±15	±125 A	±5.5	**±2** (2)
Input offset	-	5 [mV]	0.25 A	20 [mV]	**1** [mV]
Bandwidth [kHz]	3.3	20	450	50	**40**
Output noise (3) [$\mu V/\sqrt{Hz}$]	3.3 (@500 mV input)	0.18	4	56	**52**
SFDR [dB]	80.75	-	-	-	**64**
Gain drift	10 $\frac{ppm}{°C}$	25 $\frac{ppm}{°C}$	200 $\frac{ppm}{°C}$	10 $\frac{ppm}{°C}$	**4 % (-20 to 80)**

(1) Power consumption of fully isolated amplifiers with isolated DC-DC converter is reported as "Total", otherwise, the HV and LV consumptions are separated.

(2) The input swing range is ±5 V with an HV supply voltage of 5 V.

(3) Output noise is based on 300 mV of input signal.

Table 6.3 compares the performance of the current work with the available commercial IAs and the state-of-the-art. Firstly, despite the superior performance of the amplifiers with digital isolators,

they all have high consumption owing to the placement of an ADC on the HV side [14]. Secondly, unlike Hall current sensors (e.g. HLSR50) that are limited to current measurement, this approach enables Hall sensors to be utilized for voltage monitoring as well as shunt-based current sensing. Due to various bandwidths and different representations of SNRs of the compared amplifiers, in this table, the amplifiers' resolution is compared by their output noise floor for a 1 Hz bandwidth and 300 mV of input signal. Although this work has a higher output noise compared to Tan, et al. [15] and AD210 [86], the proposed architecture yet can be used in applications with a less stringent resolution. Furthermore, usage of inductive links in IAs with modulated analog data transmission (e.g. AD210 [86]) is a challenge for multi-channel readout circuits because of the large size of transformers. The isolation amplifiers that are equipped with ADCs (e.g. Tan, et al. [15]) have a much smaller transformer diameter fabricated on a dedicated dice; however, they require polyimide as an isolator, which is not available in regular foundries. In contrast with others, this work does not require any off-chip isolator or proprietary process and it only uses two dices for data transfer. Considering these challenges, our design is an ideal solution for dense integration in multi-channel isolated sensor interfaces due to its simple design, low power consumption, and small footprint.

6.5 Conclusion

The present study demonstrates a CMOS Hall sensor-based analog isolation voltage amplifier for sensor interface units in a system-in-package setup. It was shown that the proposed design provides an isolation working voltage of 600 V with an isolation-mode rejection ratio of greater than 122 dB for frequencies lower than 60 Hz. Furthermore, an SFDR of 64 dB, overall SNR of 40 dB at 40 kHz bandwidth, and an input-referred offset of 1 mV were achieved in the current work. Additionally, the power consumption of this amplifier is 7.6 mW and 9.9 mW on the HV and LV side, respectively. The fully integrated configuration makes the presented isolation system a suitable candidate to support multi-channel readout circuits using only two dice and no external component.

CHAPTER 7 GENERAL DISCUSSION

Monitoring voltage and currents in application such as power monitoring of motor feeds and sensors are needed to optimize power efficiency, acquire sensor status, and fault detection. Such measurements can occur in presence of continuous high voltages and harsh environmental conditions such as lightning strikes. Adapting electronics to sustain such an environment can eliminates or reduce heavy and bulky ESD protection solutions and improves safety of the low voltage electronic. The available commercial products suffer from high power consumption and the possibility of dense integration owing to the large area of isolation components. Consequently, a small footprint programmable low-power IA preserves reliability and decreases the cost of current and voltage sensing units by eliminating ESD protection solutions. Also, the programmability feature makes the device suitable for various sensor interface units. Finally, by reducing the weight and size of electronics in applications involving transportation (e.g. airplane), the final product can optimize the fuel efficiency and reduces green gas emissions.

To benefit from the DC measurement capability of Hall-sensors, our initial proposed idea was to use a Hall-based isolation amplifier using a single channel with no modulation/demodulation technique, Mirfakhraei, et al. [59]. This was limiting the amplifier to operate in a fixed location as calibration due to the geomagnetic field was required; although integrated calibration (DC adjustment) circuitry is possible, it would come with complications and process dependencies. Therefore, chapter 3 presents the implementation and characterization of a prototype using modulation/demodulation with commercial products and a minimal CMOS integration. The robust measured results validated the proposed idea. However, not sensitive to geomagnetic field variation (tested with varying low external DC field), yet the LV side amplifiers were getting saturated due to a high gain of INA in presence of high external magnetic fields. Modifying the receiver circuitry, the fully integrated approach demonstrated in chapter 5, is not sensitive to high external DC field perturbations.

The computation time of transient simulation was also of the challenges that impeded in-depth verification of post layout of the full system; if not slowed down or interrupted by lack of memory, license interruption, server malfunction, etc. every millisecond of transient simulation (in liberal

mode) could take days of processing. For this reason, every block was independently fully characterized, and their behavior model was predicted.

External inductive/capacitive noise can be coupled with the Hall chip, bonding pads, wire bonding, and package pads; this was a set back we encountered during our first tape out where the Hall plate signal was directly connected to the package for measurement. After increasing the measurement frequency, the detected signal was not the result of the magnetic field of the miniature or integrated spiral coils. Signals resulting from the inductive coupling between the integrated/external coil and the Hall sensor could easily be misinterpreted as AC Hall signals. The Hall sensor, its connections to the amplifying stage, and even their current source can pick inductive voltage; a more severe effect was observed with the integrated coil. To suppress that effect, methodologies described in chapter 5 were employed. This includes minimizing wire length between sensor and the first amplification stage inside the chip, balancing wires' length, shielding the sensor surface, and utilizing guard ring around the sensor and its current sources. To verify that the inductive effect is not dominant, the measured sensitivity and the COMSOL result must match

EMI is another concern that may affect the sensor. To measure that, the chip is uncapped and is tested against high DC field as explained in chapter 6. The test is also conducted for a low frequency noise (<200 kHz) with a lower magnetic field of 5 mT. In both cases no sensitivity drift or effect was detected in the signal spectrum. However, to be commercialized, this product must satisfy the CISPR-22 EMI standard, and we have not validated the standard because of the limitation of our testing equipment. As a possible improvement solution, shielding of the dice can be achieved by selecting EMI resistant packages similar to the packaging technique employed for industrial current transducers.

The layout presents a couple of challenges as well. First, as stated before, there is no Hall model in Cadence; therefore, comparing layout versus schematic (LVS) of the full structure is not possible. Second, part of the preamplifier of the Hall sensor is located under the sensor, and isolation constraints forced us to perform routing solely by the first and second metal layer. Third, to satisfy isolation level, other than SiO_2 that fills vertical spacing between integrated coil and the low voltage designs, the pads of the LV side dice that are connected to the HV design must also be adequately spaced with respect to the LV pads. The filling between pads in an open cavity package is air which has a dielectric breakdown voltage of 3 kV/mm (dry air) [90]. Therefore, for a 600 V of isolation,

the pad openings which is connected to a wire bond and are usually patterned in aluminum must be 200 µm spaced.

The 40 kHz reported bandwidth of the work was aimed for a specific application. As tested in the Hall-based digital isolator reported in chapter 5, the modulation frequency of the amplifier could be increased. Therefore, by increasing the modulation frequency, order of the AAF, as well as modifying the coil driver and the amplification stages, the architecture bandwidth could be increased.

CHAPTER 8 CONCLUSION AND RECOMMENDATIONS

8.1 Contributions

The main contributions claimed in this thesis relate to the development of the first reported Hall-effect-based isolation amplifier. These contributions can be summarized as follows:

- We conducted in-depth investigations on the available magnetic sensor and the effect of different noises on the sensors. CMOS cross-shaped Hall plates are nominated for implementation in our application. To optimize the sizing of the sensor, the plate is modeled by COMSOL using an anisotropic conductivity matrix. Also, to optimize the magnetic field, various approaches are investigated by ANSYS simulation. Finally, the integrated spiral coil that has a miniature footprint, smallest inductance, high magnetic field, and no packaging issue was selected.
- As part of the design, a first reported Hall-based digital isolator for a clock recovery circuit was fabricated and tested that satisfies the CMTI of the commercially available products. This is the first time that Hall sensors are utilized in frequencies other than DC. As described in the review section (chapter 2), contactless current sensors use CT to extend the bandwidth limit of the Hall sensors; however, using the described methodology in Chapter 4, the area consuming CTs can be replaced by a secondary integrated AC Hall sensor.
- We proposed the first fully integrated Hall-based isolation voltage amplifier. The system performance and impact of HV noises are investigated by measurement. The results are promising as they show comparable IMR with available industrial products. The packaged product consumes less power compared with inductive, capacitive, and optical analog data transmission or ADC based solutions. The final product occupies significantly lower area while using only two dices with no post processing, which makes the approach suitable for multi-channel readout sensing. The added gain tunning feature not only allows the design to be employed in voltage and current sensing using shunt resistor, but also make it compatible for different swing range of ADCs.

8.2 Future work

Our planned future work is to further increase the SNR of the design by implementation in smaller gate-length technologies like 65 nm. A lower sheet resistance of the N-Well process could allow the sensor to be biased with a more current. Besides, smaller gate-length techs have 8-9 metal layers which can increase the MF strength of the integrated spiral coils for the same isolation level and further increase SNR. Also, a different configuration of sensors or increasing the total number of sensors improves the SNR of the design. If the thermal noise of each sensor is assumed to be uncorrelated, the SNR of the combined sensors is calculated as:

$$\mathrm{SNR} = 20\log\left(\frac{\mathrm{N}S_I B I_{DC}}{(V_t\sqrt{\mathrm{N}})\sqrt{\mathrm{BW}}}\right) = 10\log(\mathrm{N}) + 20\log\left(\frac{S_I B I_{DC}}{V_t\sqrt{\mathrm{BW}}}\right) \qquad (8.1)$$

Where N is the total number of sensors, V_t is the thermal noise level, S_I is the current sensitivity, I_{DC} is the biasing current, and B is the magnetic field. Therefore, adding three more sensors for a total of four sensors, increases the SNR by 6 dB.

Combining multiple readout circuit units in a single dice is another future task that is only applicable using the Hall-based approach. By properly spacing the Tx coil and Rx Hall sensor of each amplifier on the receiver dice (reported in chapters 5 and 6), crosstalk is reduced to a negligible level.

One additional step that can further increase the signal quality is transferring the designs to a 2DEG process like GaN, which not only has higher sensitivity, but also a lower sheet resistance that can significantly improve signal quality. Finally, we aim to implement a fully isolated prototype consisting of both Hall-based data isolation and an inductive DC-DC power converter.

REFERENCES

[1] M. Yamakawa, Y. Mizuno, J. Ishida, K. Komurasaki, and H. Koizumi, "Wireless power transmission into a space enclosed by metal walls using magnetic resonance coupling," *Wireless Engineering Technology*, vol. 5, no. 01, p. 19, 2014.

[2] H. Zangl, A. Fuchs, T. Bretterklieber, M. J. Moser, and G. Holler, "Wireless communication and power supply strategy for sensor applications within closed metal walls," *IEEE transactions on instrumentation measurement*, vol. 59, no. 6, pp. 1686-1692, 2010.

[3] T. J. Lawry, K. R. Wilt, J. D. Ashdown, H. A. Scarton, and G. J. Saulnier, "A high-performance ultrasonic system for the simultaneous transmission of data and power through solid metal barriers," *IEEE transactions on ultrasonics, ferroelectrics, frequency control*, vol. 60, no. 1, pp. 194-203, 2013.

[4] L. Huang, A. P. Hu, A. Swain, S. Kim, and Y. Ren, "An overview of capacitively coupled power transfer—A new contactless power transfer solution," in *2013 IEEE 8th Conference on Industrial Electronics and Applications (ICIEA)*, 2013: IEEE, pp. 461-465.

[5] *"Gauging LED lifetime in optocouplers"*. [Online]. Available: https://www.machinedesign.com/news/gauging-led-lifetime-optocouplers. Accessed: June 2021.

[6] C. A. McCreary and B. A. Lail, "Design of multiple stage avionics lightning protection for DC power input lines using a graphical user interface (GUI)," in *2013 IEEE International Symposium on Electromagnetic Compatibility*, Aug. 2013, pp. 177-181, doi: 10.1109/ISEMC.2013.6670404.

[7] *"ISO124: ±10-V Input, Precision Isolation Amplifier", Burr-Brown Products from Texas Instruments*. [Online]. Available: http://www.ti.com. Accessed: June 2021.

[8] A. Devices. *"AD215: 120 kHz bandwidth low distortion isolation amplifier"*. [Online]. Available: http://www.analog.com. Accessed: Sep. 2019.

[9] S. Takaya, H. Ishihara, and K. Onizuka, "18.7 A DC to 35MHz Fully Integrated Single-Power-Supply Isolation Amplifier for Current- and Voltage-Sensing Front-Ends of Power Electronics," in *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, Feb. 2020, pp. 298-300, doi: 10.1109/ISSCC19947.2020.9063124.

[10] AVAGO. *High-Linearity Analog Optocouplers*, July 2014.

[11] "Linear Optocoupler, High Gain Stability, Wide Bandwidth." Vishay Semiconductors. http://www.farnell.com/datasheets/2047031.pdf (accessed.

[12] F. Zhang, T. Zhao, C. Ma, and D. Pan, "4-port digital isolator based on on-chip transformer," *Journal of Semiconductors*, vol. 39, no. 11, p. 115003, 2018/11 2018, doi: 10.1088/1674-4926/39/11/115003.

[13] A. H. Johnston and B. G. Rax, "Proton damage in linear and digital optocouplers," *IEEE Transactions on Nuclear Science*, vol. 47, no. 3, pp. 675-681, 2000, doi: 10.1109/23.856497.

[14] S. Ma, J. Feng, T. Zhao, and B. Chen, "A Fully Isolated Amplifier Based on Charge-Balanced SAR Converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 6, pp. 1795-1804, 2018, doi: 10.1109/TCSI.2017.2767678.

[15] Z. Tan *et al.*, "A Fully Isolated Delta-Sigma ADC for Shunt Based Current Sensing," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 10, pp. 2232-2240, 2016, doi: 10.1109/JSSC.2016.2581800.

[16] T. INSTRUMENT. *AMC1301 Precision, ±250-mV Input, 3-µs Delay, Reinforced Isolated Amplifier*, AMC1301, 2016.

[17] *"Photocouplers Optically Isolation Amplifier, TLP7920,TLP7920F", TOSHIBA*. [Online]. Available: https://toshiba.semicon-storage.com/. Accessed: Feb. 2021.

[18] A. DEVICES. *Very High Common-Mode Voltage Precision Difference Amplifier*, AD8479, 2015.

[19] S. Wayne, "Finding the Needle in a Haystack: Measuring small differential voltages in the presence of large common-mode voltages."

[20] X. Liu, J. Yang, B. Qian, and L. Zhang, "Application Analysis of AD8479 in the Acquisition Unit of Electronic Current Transformer," *MATEC Web of Conferences*, vol. 160, p. 01002, 01/01 2018, doi: 10.1051/matecconf/201816001002.

[21] *"Designing Linear Amplifiers Using the IL300 Optocoupler", Application Note 50*. [Online]. Available: www.vishay.com. Accessed: June 2021.

[22] T. INSTRUMENT. "AMC1200-Q1Fully-DifferentialIsolationAmplifier." https://www.ti.com/ (accessed Apr. 2021.

[23] N. McNeill, N. K. Gupta, and W. G. Armstrong, "Active current transformer circuits for low distortion sensing in switched mode power converters," *IEEE Transactions on Power Electronics*, vol. 19, no. 4, pp. 908-917, 2004, doi: 10.1109/TPEL.2004.830075.

[24] J. E. Lenz, "A review of magnetic sensors," *Proceedings of the IEEE*, vol. 78, no. 6, pp. 973-989, 1990, doi: 10.1109/5.56910.

[25] Alegro. "A1324, A1325, and A1326_Low Noise, Linear Hall Effect Sensor ICs with Analog Output." https://www.allegromicro.com/ (accessed.

[26] HONEYWELL, "SS39ET/SS49E/SS59ET Series Linear Hall-effect Sensor ICs." [Online]. Available: https://www.honeywell.com.

[27] ALLEGRO, "A1362 Low Noise, High Precision, Programmable Linear Hall Effect Sensor IC With Advanced Temperature Compensation and High Bandwidth (120 kHz) Analog Output," April 26, 2019.

[28] MELEXIS. *MLX91208, "IMC-Hall® Current Sensor (Triaxis®Technology)"*. [Online]. Available: www.melexis.com. Accessed: June 2018.

[29] M. Sadeghi, J. Sexton, C. Liang, and M. Missous, "Highly Sensitive Nanotesla Quantum-Well Hall-Effect Integrated Circuit Using GaAs–InGaAs–AlGaAs 2DEG," *IEEE Sens. J.*, vol. 15, no. 3, pp. 1817-1824, 2015, doi: 10.1109/JSEN.2014.2368074.

[30] M.-A. Paun, J.-M. Sallese, and M. Kayal, *Hall Effect Sensors Design, Integration and Behavior Analysis*. 2013, pp. 85-97.

[31] Y.-N. Lin and C.-L. Dai, "Micro Magnetic Field Sensors Manufactured Using a Standard 0.18-μm CMOS Process," (in eng), *Micromachines (Basel)*, vol. 9, no. 8, p. 393, 2018, doi: 10.3390/mi9080393.

[32] H. Heidari, E. Bonizzoni, U. Gatti, and F. Maloberti, "A CMOS Current-Mode Magnetic Hall Sensor With Integrated Front-End," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 5, pp. 1270-1278, 2015, doi: 10.1109/TCSI.2015.2415173.

[33] S. Ziegler, R. C. Woodward, H. H. Iu, and L. J. Borle, "Current Sensing Techniques: A Review," *IEEE Sens. J.*, vol. 9, no. 4, pp. 354-376, 2009, doi: 10.1109/JSEN.2009.2013914.

[34] *"Current Transducer HLSR-P/SP33 series"*. [Online]. Available: http://www.lem.com. Accessed: June 2021.

[35] *ALLEGRO microsystems, "ACS714, Automotive Grade, Fully Integrated, Hall-Effect-Based Linear Current Sensor IC with 2.1 kVRMS Voltage Isolation and Low-Resistance Current Conductor"*. [Online]. Available: https://www.allegromicro.com/. Accessed: Aug. 2020.

[36] BROADCOM. *ACHS-719X, "Fully Integrated, Hall Effect-Based Linear Current Sensor IC with 3 kVRMS Isolation and Low-Resistance Current Conductor"*. [Online]. Available: www.broadcom.com. Accessed: July 2020.

[37] P. Ripka and M. Janosek, "Advances in Magnetic Field Sensors," *IEEE Sens. J.*, vol. 10, no. 6, pp. 1108-1116, 2010, doi: 10.1109/JSEN.2010.2043429.

[38] R. Rodriguez-Torres, E. A. Gutierrez-Dominguez, R. Klima, and S. Selberherr, "Analysis of split-drain MAGFETs," *IEEE Transactions on Electron Devices*, vol. 51, no. 12, pp. 2237-2245, 2004, doi: 10.1109/TED.2004.839869.

[39] Y. Audet and G. H. Chapman, "Yield improvement of a large area magnetic field sensor array using redundancy schemes," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 5, no. 1, pp. 28-33, 1997, doi: 10.1109/92.555984.

[40] N. Rezaei, R. Dehghani, A. Jalili, and A. Mosahebfard, "CMOS magnetic sensor with MAGFET," in *2013 21st Iranian Conference on Electrical Engineering (ICEE)*, 14-16 May 2013 2013, pp. 1-5, doi: 10.1109/IranianCEE.2013.6599582.

[41] Y. Xu and H.-B. Pan, "An improved equivalent simulation model for CMOS integrated Hall plates," (in eng), *Sensors (Basel)*, vol. 11, no. 6, pp. 6284-6296, June 2011, doi: 10.3390/s110606284.

[42] F. Lyu *et al.*, "Performance comparison of cross-like Hall plates with different covering layers," (in eng), *Sensors (Basel)*, vol. 15, no. 1, pp. 672-686, 2014, doi: 10.3390/s150100672.

[43] S. Koide, H. Takahashi, A. Abderrahmane, I. Shibasaki, and A. Sandhu, "High Temperature Hall sensors using AlGaN/GaN HEMT Structures," *Journal of Physics: Conference Series*, vol. 352, p. 012009, 2012/03/05 2012, doi: 10.1088/1742-6596/352/1/012009.

[44] Melexis. "CURRENT SENSORS REFERENCE DESIGN GUIDE." (accessed.

[45] E. Yosry, W. Fikry, A. El-Henawy, and M. Marzouk, "Compact model of dual-drain MAGFETs simulation," *Int. J. Electr. Commun. Comput. Eng.*, vol. 1, 01/01 2009.

[46] J. W. A. v. Kluge and W. A. Langheinrich, "An analytical model of MAGFET sensitivity including secondary effects using a continuous description of the geometric correction factor G," *IEEE Transactions on Electron Devices*, vol. 46, no. 1, pp. 89-95, 1999, doi: 10.1109/16.737446.

[47] R. S. Popovic, *Hall Effect Devices* (no. Book, Whole). Baton Rouge: CRC Press, 2003.

[48] H. Heidari, E. Bonizzoni, U. Gatti, and F. Maloberti, "A 0.18-µm CMOS current-mode Hall magnetic sensor with very low bias current and high sensitive front-end," in *SENSORS, 2014 IEEE*, 2-5 Nov. 2014 2014, pp. 1467-1470, doi: 10.1109/ICSENS.2014.6985291.

[49] V. Mosser, N. Matringe, and Y. Haddab, "A Spinning Current Circuit for Hall Measurements Down to the Nanotesla Range," *IEEE Transactions on Instrumentation and Measurement*, vol. 66, no. 4, pp. 637-650, 2017, doi: 10.1109/TIM.2017.2649858.

[50] P. J. A. Munter, "A low-offset spinning-current hall plate," *Sensors and Actuators A: Physical*, vol. 22, no. 1, pp. 743-746, 1990/06/01/ 1990, doi: https://doi.org/10.1016/0924-4247(89)80069-X.

[51] A. Ajbl, M. Pastre, and M. Kayal, "A Fully Integrated Hall Sensor Microsystem for Contactless Current Measurement," *IEEE Sens. J.*, vol. 13, no. 6, pp. 2271-2278, 2013, doi: 10.1109/JSEN.2013.2251971.

[52] S.-M. Lim and J.-S. Park, "A Low Noise Offset Cancellation Method for Improving Sensitivity of CMOS Hall Sensor," *Journal of Electrical Engineering & Technology*, vol. 14, no. 1, pp. 377-383, 2019/01/01 2019, doi: 10.1007/s42835-018-00031-7.

[53] G. International Association of *et al.*, "International Geomagnetic Reference Field: the eleventh generation," *Geophysical Journal International*, https://doi.org/10.1111/j.1365-246X.2010.04804.x vol. 183, no. 3, pp. 1216-1230, 2010/12/01 2010, doi: https://doi.org/10.1111/j.1365-246X.2010.04804.x.

[54] Y. Xu, H.-B. Pan, S.-Z. He, and L. Li, "A Highly Sensitive CMOS Digital Hall Sensor for Low Magnetic Field Applications," *Sensors (Basel)*, vol. 12, pp. 2162-74, Dec. 2012, doi: 10.3390/s120202162.

[55] A. Chovet, C. S. Roumenin, G. Dimopoulos, and N. Mathieu, "Comparison of noise properties of different magnetic-field semiconductor integrated sensors," *Sensors and Actuators A: Physical*, vol. 22, no. 1, pp. 790-794, 1990/06/01/ 1990, doi: https://doi.org/10.1016/0924-4247(89)80079-2.

[56] M. Paun, J. Sallese, and M. Kayal, "Temperature considerations on Hall Effect sensors current-related sensitivity behaviour," in *2012 19th IEEE International Conference on Electronics, Circuits, and Systems (ICECS 2012)*, 9-12 Dec. 2012 2012, pp. 201-204, doi: 10.1109/ICECS.2012.6463766.

[57] D. Manic, J. Petr, and R. S. Popovic, "Temperature cross-sensitivity of Hall plate in submicron CMOS technology," *Sensors and Actuators A: Physical*, vol. 85, no. 1, pp. 244-248, 2000/08/25/ 2000, doi: https://doi.org/10.1016/S0924-4247(00)00399-X.

[58] R. S. Popoviū, *Hall effect devices: R.S. Popoviū*, 2nd -- ed. (no. Book, Whole). Bristol, [Angleterre]: Institute of Physics Publishing, 2004.

[59] S. S. Mirfakhraei, Y. Audet, A. Hassan, and M. Sawan, "A Galvanic Isolated Amplifier Based on CMOS Integrated Hall-Effect Sensors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, pp. 1-10, 2021, doi: 10.1109/TCSI.2021.3052476.

[60] "Hall Effect Sensor: Toroid Winding Direction," ed.

[61] D. J. Dumin, *Oxide reliability : a summary of silicon oxide wearout, breakdown, and reliability*, [River Edge, NJ]: World Scientific, 2002.

[62] C. K. Lee, Y. P. Su, and S. Y. R. Hui, "Multilayer stacked coreless printed spiral winding inductor with wide frequency bandwidth," in *2009 IEEE Energy Conversion Congress and Exposition*, 20-24 Sept. 2009 2009, pp. 1002-1009, doi: 10.1109/ECCE.2009.5316322.

[63] *"IEC 61800-5-2", "Adjustable speed electrical power drive systems - Part 5-2: Safety requirements - Functional"*, 2016.

[64] *Texas Instrument, "AMC1301 Precision, ±250-mV Input, 3-µs Delay, Reinforced Isolated Amplifier"*. [Online]. Available: http://www.ti.com. Accessed: Apr. 2020.

[65] F. Rothan *et al.*, "A ±1.5% nonlinearity 0.1-to-100A shunt current sensor based on a 6kV isolated micro-transformer for electrical vehicles and home automation," in *2011 IEEE International Solid-State Circuits Conference*, Feb. 2011, pp. 112-114, doi: 10.1109/ISSCC.2011.5746242.

[66] S. S. Mirfakhraei, Y. Audet, A. Hassan, M. Ali, M. Nabavi, and M. Sawan, "A CMOS MAGFET-Based Programmable Isolation Amplifier," in *2020 18th IEEE International New Circuits and Systems Conference (NEWCAS)*, June 2020, pp. 9-13, doi: 10.1109/NEWCAS49341.2020.9159790.

[67] S. S. Mirfakhraei *et al.*, "Wide Dynamic Range Front-End Programmable Isolation Amplifier using Integrated CMOS Hall Effect Sensor," in *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, Oct. 2020, pp. 1-5, doi: 10.1109/ISCAS45731.2020.9180574.

[68] W.-c. Wang, "A Motor Speed Measurement System Based on Hall Sensor," in *Intelligent Computing and Information Science*, Berlin, Heidelberg, R. Chen, Ed., 2011// 2011: Springer Berlin Heidelberg, pp. 440-445.

[69] "Isolation Types and Considerations When Taking a Measuremen." [Online]. Available: https://www.ni.com/.

[70] M. Demierre, S. Pesenti, J. Frounchi, P.-A. Besse, and R. Popovic, *Reference Magnetic Actuator for self Calibration of a very small Hall Sensor Array*. Apr. 2002, pp. 39-46.

[71] M. M. Marco Crescentini, Aldo Romani, Marco Tartagni, Pier Andrea Traverso, "Bandwidth limits in Hall effect-based current sensors," vol. 6, no. 4, pp. 17-24, Dec. 2017.

[72] *High-Frequency Electromagnet Using Resonant Technique*. [Online]. Available: https://www.accelinstruments.com/Applications/WaveformAmp/Electromagnetic-Coil-Resonant.html. Accessed: Sep. 2020.

[73] *CnC Tech Industrial Cable and Connector Technology, "MW35C"*. [Online]. Available: https://www.cnctech.us/pdfs/MW-Specification-sheet.pdf. Accessed: Feb. 2021.

[74] R. P. Singh and A. M. Khambadkone, "Giant Magneto Resistive (GMR) effect based Current Sensing Technique for DC/DC Converters," in *IECON 2007 - 33rd Annual Conference of the IEEE Industrial Electronics Society*, 5-8 Nov. 2007 2007, pp. 1420-1425, doi: 10.1109/IECON.2007.4460150.

[75] J. Kim and S. Jo, "Modeling of giant magnetoresistance isolator for high speed digital data transmission utilizing spin valves," *Journal of Applied Physics - J APPL PHYS*, vol. 97, 05/15 2005, doi: 10.1063/1.1853913.

[76] S. K. Biswas, B. Basak, and K. S. Rajashekara, "Gate drive methods for IGBTs in bridge configurations," in *Proceedings of 1994 IEEE Industry Applications Society Annual Meeting*, 2-6 Oct. 1994 1994, vol. 2, pp. 1310-1316 vol.2, doi: 10.1109/IAS.1994.377589.

[77] D. Mittleman, J. Cunningham, M. Nuss, and M. Geva, "Noncontact semiconductor wafer characterization with the terahertz Hall effect," *Applied Physics Letters*, vol. 71, pp. 16-18, 1997.

[78] M. Crescentini, M. Biondi, A. Romani, M. Tartagni, and E. Sangiorgi, "Optimum Design Rules for CMOS Hall Sensors," *Sensors*, vol. 17, no. 4, 2017, doi: 10.3390/s17040765.

[79] S. Kaeriyama, S. Uchida, M. Furumiya, M. Okada, T. Maeda, and M. Mizuno, "A 2.5 kV Isolation 35 kV/us CMR 250 Mbps Digital Isolator in Standard CMOS With a Small Transformer Driving Technique," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 2, pp. 435-443, 2012, doi: 10.1109/JSSC.2011.2170775.

[80] *ADuM1310/ADuM1311 Triple-Channel Digital Isolators* [Online]. Available: https://www.analog.com/. Accessed: June 2021.

[81] A. Devices. *High Speed Digital Isolators Using Microscale On-Chip Transformers*. [Online]. Available: https://www.analog.com/. Accessed: June 2021.

[82] *Si80xx-1kV three to six-channel digital isolations*. [Online]. Available: https://www.silabs.com/. Accessed: June 2021.

[83] *ISO72x Single Channel High-Speed Digital Isolators Data Sheet Rev. L*. [Online]. Available: https://www.ti.com/. Accessed: June 2020.

[84] *IL01x Low-Power Digital Isolators*. [Online]. Available: https://www.nve.com/. Accessed: Jun 2020.

[85] M. Ali, N. Morteza, A. Hassan, M. Honarparvar, Y. Savaria, and M. Sawan, "A Versatile SoC/SiP Sensor Interface for Industrial Applications: Design Considerations," in *2019 31st International Conference on Microelectronics (ICM)*, 2019, pp. 40-43, doi: 10.1109/ICM48031.2019.9021286.

[86] *"AD210 Precision, Wide Bandwidth 3-Port Isolation Amplifier"*. [Online]. Available: www.analog.com. Accessed: June 2021.

[87] Y. Xu, X. Hu, and L. Jiang, "An Analytical Geometry Optimization Model for Current-Mode Cross-Like Hall Plates," (in eng), *Sensors (Basel)*, vol. 19, no. 11, p. 2490, 2019, doi: 10.3390/s19112490.

[88] I. N. Ruskova, E. E. Gieva, V. M. Yantchev, and M. H. Hristov, "COMSOL modeling of Hall sensors efficiency," in *2017 XXVI International Scientific Conference Electronics (ET)*, 2017, pp. 1-4, doi: 10.1109/ET.2017.8124384.

[89] R. Yun, J. Sun, E. Gaalaas, and C. Baoxing, "A transformer-based digital isolator with 20kVPK surge capability and > 200kV/µS Common Mode Transient Immunity," in *2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits)*, 2016, pp. 1-2, doi: 10.1109/VLSIC.2016.7573497.

[90] *"Dielectric Strength of Air"*, The Physics Factbook, 2000. [Online]. Available: https://hypertextbook.com/facts/2000/AliceHong.shtml. Accessed: July 2021.