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Anti-Series Varactor Network With Improved Linearity Performances in the Presence of Inductive and Capacitive Parasitics

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ABSTRACT This paper proposes a varactor-based circuit technique intended for amplitude and phase control, with improved linearity in the presence of parasitic capacitances and parasitic inductances. The mechanism causing linearity degradation in an anti-series varactor network that includes significant parasitic elements – a key aspect that, to our knowledge, has never been reported – is first studied using an analytical approach based on multi-tone excitation. It is demonstrated that simply optimizing the ratio of diode sizes is insufficient to circumvent this linearity degradation. The underlying linearity degradation concept serves as the basis for the introduction of a modified anti-series controllable capacitance, followed by a design and practical implementation. Experimental validations with multi-tone and modulated signals demonstrate improved linearity performances with respect to the state-of-the-art when parasitic capacitances and inductances are significant. Moreover, it is shown that the complete varactor-based circuit topology proposed here, which uses the proposed modified anti-series controllable capacitance in conjunction with a second-harmonic trap filter, constitutes a very attractive alternative to the state-of-the-art anti-series/anti-parallel topology, since it reduces the required number of diodes by a factor of 2. Measurements on discrete-component designs operating at 3.6GHz, hence with significant parasitic effects, demonstrate that the proposed circuit topology improves the 3rd order intermodulation distortion levels by 10.6dB and 6.6dB at output powers of 10dBm and 18dBm respectively, in comparison with the state-of-the-art topology. Measurements with a 16QAM modulated signal also show 3.9dB improvement in ACPR at 18dBm. These performances constitute improved state-of-the-art results in anti-series hyper-abrupt varactor-based electronic control.

INDEX TERMS Adjacent channel power ratio (ACPR), amplitude, anti-series, controllable, diode, distortion, intermodulation distortion (IMD), impedance, linearity, linearization techniques, magnitude, multi-tone, parasitic, phase, reconfigurable, spatially-fed antenna, transmitarray, tunable, varactor, variable.

I. INTRODUCTION

The aerospace industry is showing increasing interest in electronically reconfigurable antenna systems [1], [2]. This type of system provides opportunities for new functionalities which would ultimately facilitate the adaptation of satellites to the evolving market. Fig.1 is one such reconfigurable transmitarray (RTA) antenna system for satellite applications. The electronically controllable networks (highlighted in Fig.1) within each cell of the aperture array are key elements of this system. Solid-state varactor technologies are suitable for many of the tight specifications associated with the system of Fig.1, given their good reliability, their ease of control, their compatibility with fast switching speed, their compactness, their high energy efficiency, etc. However, it is also well known that solid-state varactor technologies are associated with limited linearity and power handling performances.

With regard to improving the linearity and power handling capability of varactor-based controllable networks, [3] introduces the concept of stacking two identical varactors

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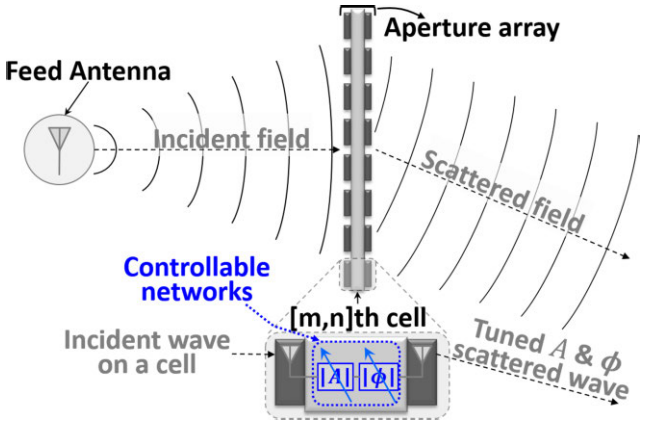


FIGURE 1. Schematic of an electronically controllable RTA system.

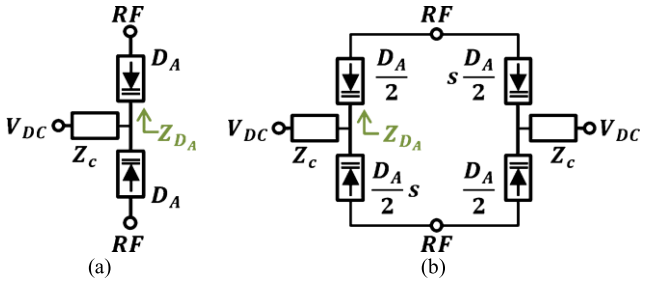


FIGURE 2. State-of-the-art highly linear varactor-based controllable impedance network where D_A is the varactor size. a) Matched anti-series-only topology b) Unmatched anti-series/anti-parallel topology.

of size D_A in an anti-series configuration by proposing the abrupt varactor-based topology in Fig.2a. This topology significantly improves circuit linearity by enabling a distortion-cancellation mechanism. Moreover, such series stacking of two varactors inherently enhances the power handling capability by sharing the RF voltage between two varactors. In the work of [4], the network's capacitance tuning range is broadened by using hyper-abrupt varactors, while the distortion-cancellation mechanism is made possible by using the anti-series/anti-parallel topology in Fig.2b and by optimizing the ratio (s) between the diode sizes, hence the ratio between their junction capacitances.

In the topologies proposed in [3], [4], the effectiveness of the distortion-cancellation mechanism relies on a center-tap impedance (Z_C in Fig.2), typically implemented with a resistor, higher than the diode's AC impedance (Z_{D_A} in Fig.2) for all frequency components (i.e. $Z_C \gg Z_{D_A}$ at all frequencies). The key factor dictating the required value of Z_C is the high value of Z_{D_A} at baseband frequencies, which are at significantly lower frequencies than the fundamental and harmonic frequencies (f_0, $2f_0$, $3f_0$, $\cdots$). Since the condition on Z_C is alleviated as the tone spacing is widened, [3], [4] topologies suit large-bandwidth RF applications and are referred as ''wide tone-spacing varactor stacks'' in the literature. On the other hand, for near-zero tone spacing (or modulation schemes including very low frequencies), the required infinitely high value of Z_C to comply with $Z_C \gg Z_{D_A}$ at baseband frequency is an important limiting factor, particularly for MMIC-only designs. With regard to increasing the value of Z_C at low frequencies, [4] implements Z_C using an anti-parallel diodes network which maintains the effectiveness of the distortion-cancellation mechanism for a simulated tone spacing as low as ∼100Hz. However, because of the possible current leakages through the diode-based Z_C network, yielding degraded linearity performances, this latter solution adds significant design complexities.

Whereas [3], [4] require high Z_C values at tone spacing near 0Hz, the topologies proposed in [5], [6] require $Z_C \ll Z_{D_A}$ at baseband frequencies and $Z_C \gg Z_{D_A}$ at the fundamental and harmonic frequencies. These center-tap impedance conditions, which are fulfilled by implementing Z_C with an inductance, makes [5], [6] topologies best suited for modulated signals including content near 0Hz. This shift on the conditions on Z_C is made possible by designing the topology in Fig.2a using exponentially doped diodes produced in Silicon on Glass (SoG) [5] and GaAs MMIC [6] processes. However, the condition $Z_C \ll Z_{D_A}$ at baseband frequencies restricts [5], [6] topologies to smaller bandwidth applications (e.g., [5] is limited to a tone spacing of ∼10MHz).

The work in [7] extends the use of exponentially doped diode technologies to a larger variety of RF applications by proposing a wide tone-spacing varactor stack based on the topology in Fig.2b. Note that this work is restricted by the same center-tap conditions as in [3], [4].

References [8], [9] further improve the power handling capability of anti-series topologies by sharing the RF voltage between an increased number of varactors. This is made possible by using multiple series-stacking of the topologies proposed in [4], [5]. The drawbacks with the topologies in [8], [9] are the use of an increased number of components or chip area, and a lower Q factor for the same targeted capacitance value. The work in [10], [11] also improves power capability by implementing the topology of Fig.2a in a GaN technology with a focus on the Q factor.

The key characteristics associated to the above works and that are demonstrated in the gigahertz frequency range ($\geq 1GHz$) are summarized in Table 1 and compared with our work, while taking into consideration the important aspect of L-C parasitics.

All the solutions in Table 1 are demonstrated at ∼2.15GHz or lower and are implemented either on SoG MMIC [12], GaAs MMIC or GaN MMIC technologies. The limited frequency of operation and MMIC integration aspects in these works are of particular importance. In these conditions, the *ideal* distortion-free behavior of anti-series topologies is made possible, in part because the effects of parasitics surrounding the diodes are negligible. In fact, the effects of parasitics on the linearity of anti-series varactor networks, to our knowledge, have never been reported.

The discrete-package varactors approach in this work translates into added constraints due to larger parasitics compared to MMIC technologies. As will be demonstrated in this

TABLE 1. Comparison of existing varactor-based anti-series topologies in the context of significant L-C parasitics.

Ref. / Year	Technology / Doping / Topology	Demonstrated with L-C parasitics	f_0 (GHz)	Diode count	Linearity/Power at min and max demonstrated TS				Key aspects not demonstrated
					Measurement type	Linearity level	Power or Voltage	TS (Hz)	
[4] / 2005	SoG MMIC / H-A / AS-AP (Fig.1b in [4])	NO✗	2	4✗	2-tone IMD3	~-60dBc	3V	100M	- Performances for a range of bias - Performances for a range of TS - Experimental linearity performances
[5] / 2008	SoG MMIC / EXP / AS Only	NO✗	2.14	2	2-tone IMD3	~-63dBc	16dBm	10k	- Performances for a range of bias - Linearity with complex modulation
						~-33dBc✗		99M	
[6] / 2010	GaAs MMIC / EXP / AS Only	NO✗	2	2	2-tone IMD3	~-59dBc	24dBm	2k	- Performances for a range of bias - Linearity with complex modulation
						~-40dBc✗		100M	
[7] / 2009	SoG MMIC / EXP / AS-AP (Fig.3a-b in [7])	NO✗	2	4✗	2-tone IMD3	~-35dBc✗	15dBm	5k	- Performances for a range of bias - Linearity with complex modulation
						~-94dBc		80M	
[8] / 2007	SoG MMIC / A / M-AS Only (Fig.3 in [8])	NO✗	2.14	4✗	2-tone IMD3	~-97dBc	21dBm	10k✗	- Performances for a range of bias - Linearity with complex modulation
						~-86dBc		100M	
[9] / 2008	SoG MMIC / EXP / M-AS Only	NO✗	2.14	4✗	2-tone IMD3	~-76dBc	26dBm	10k✗	- Performances for a range of bias - Linearity with complex modulation
						~-47dBc		80M	
[10] / 2012	GaN MMIC / A / AS Only	NO✗	1	2	2-tone IMD3	~-56dBc	27dBm	15M	- Performances for a range of bias - Performances for a range of TS - Linearity with complex modulation
[11] / 2019	GaN MMIC / A / AS Only	NO✗	1-2	2	CW✗ 3rd harm.	Harmonics only✗		N/A	- 2-tone linearity performances - Experimental linearity performances
This work	Discrete / Using AS Only with H-A✱	YES✱ (1st to demonstrate)	3.6✱	2✱	2-tone IMD3	-63dBc✱	10dBm	1k	Demonstrated in this work
						-62dBc	10dBm	120M	- Evaluated over full bias range ✱ Linearity with complex modulation
						-54dBc	18dBm	10M	
					16QAM✱	-56dBc	18dBm	10M	

Acronyms		Symbols for a qualitative comparison
A – Abrupt doping profile ACPR – Adjacent channel power ratio AS Only – Anti-series-only topology AS-AP – Anti-series/anti-parallel topology BW – Bandwidth CW – Continuous wave EXP – Exponential doping profile	f_0 – Frequency of operation GaAs – Gallium arsenide H-A – Hyper-abrupt doping profile M-AS Only – Multi-stack of AS Only SoG – Silicon on glass TS – Tone spacing	✗ Disadvantage with respect to this work ✱ Key improvements or new metrics in this work ~ Data estimated from a graphic

paper, the parasitics in discrete designs at 3.6GHz degrade significantly the linearity of anti-series varactor networks.

While many comparisons may be drawn with the prior-art, the objectives pursued in this work requires high linearity performances over a wide range of tone spacing, given that our application (Fig.1) uses complex modulation schemes. This aspect is compared in the column "Linearity/Power at min and max demonstrated TS" of Table 1. Also, the column "Diode count" highlights the importance of minimizing the number of varactors when a high-reliability discrete design is needed, as in our application. Moreover, a column highlights key aspects that were not demonstrated in these prior works, but which were demonstrated in our work.

The work presented in this paper investigates the linearity performance optimization of the varactor-based discrete design needed for the controllable network in the system illustrated in Fig.1. The analyses presented make use of the electrical characteristics of an off-the-shelf GaAs flip-chip varactor device only as numerical example and to allow experimental validation with a practical design using the same varactor. However, the proposed linearity improvement technique is not limited to this specific varactor and may be implemented using other hyper-abrupt varactors in flip-chip and discrete packages.

It is demonstrated, using multi-tone-based equations, that the linearity performance enhancement expected from the distortion-cancellation mechanism inherent to the anti-series networks in Fig.2, is severely degraded by the passive parasitics surrounding the varactors. Note that recent articles (e.g. [13]–[15]) employ varactor-based anti-series networks in various RF systems, which highlights their importance. However, they do not address the linearity degradation mechanism due to L-C parasitics in anti-series networks.

Moreover, it is shown that optimizing the ratio of diode sizes is insufficient to circumvent the linearity degradation due to parasitics.

Understanding the degradation of this distortion-cancellation mechanism in an anti-series-only network is the basis for the introduction of a *modified* anti-series network in

this paper. The complete hyper-abrupt varactor-based circuit topology pursued here yields many key improvements over the works listed in Table 1 and, to our knowledge, over all reported varactor-based anti-series topologies in the literature:

(i) It enhances the linearity performances despite the presence of parasitics surrounding the diodes. This allows operating varactor topologies at higher frequencies and is highlighted in Table 1 by $f_0 = 3.6GHz$ in our work using discrete components as opposed to the reported $f_0 \leq 2.14GHz$ in previous works based on MMIC approaches,
(ii) It offers an alternative to the anti-series/anti-parallel topology (Fig.2b) with the benefit of reducing by 2 the number of diodes. This is relevant in regards to cost and size for high volume products (e.g. wireless communication systems), and also for high-reliability systems (e.g. on-board satellite RF circuitry as in Fig.1).
(iii) It circumvents the linearity degradation that stems from the inductive effect of series transmission lines between the varactor-based network and external circuits. This facilitates the implementation of anti-series networks in various RF systems (e.g. phase-shifters, tunable filters, configurable amplifiers, etc.)

This paper is organized as follows. Section II begins with a summary of the theory behind the state-of-the-art anti-series topology. An analytical study is then presented to explain the mechanism of linearity degradation in an anti-series topology due to capacitive and inductive parasitics. Section III presents the proposed modified anti-series network, followed by the complete varactor-based topology introduced here. Formulations associated with this modified network and that allow theoretically predicting the possible linearity improvement, are also given. Section IV presents experimental results validating the linearity enhancement achieved with the complete varactor-based topology proposed in this paper, under 2-tone and 16QAM excitation schemes.

II. NONLINEARITIES IN ANTI-SERIES VARACTOR IN THE PRESENCE OF PARASITIC ELEMENTS

Varactor models commonly used by manufacturers include a series parasitic inductance (L_S) and a parallel parasitic capacitance (C_P). These components were not included in the state-of-the-art formulations presented in [3]–[5], [8], [16] to predict the nonlinearities generated by anti-series varactor networks. This constitutes a limitation under certain conditions.

Section II-A summarizes the theory in [4] predicting the nonlinearities generated by parasitic-free anti-series varactor networks. Section II-B then extends this theory by introducing new formulations to describe the generation of additional nonlinearities in the presence of significant C_P and L_S.

A. NONLINEARITIES IN PARASITIC-FREE ANTI-SERIES TOPOLOGY

In this subsection, we analyze the distortion mechanism in the parasitic-free anti-series-only circuits of [4], [7]. The analysis builds on the formulations presented in [4], to further highlight the nonlinear current generation mechanism for better clarity in this paper. This is necessary since frequent references to these currents will be made throughout the remainder of this paper and will be used for various numerical calculations.

1) ASSUMPTIONS MADE FOR ANALYSIS

It is worthwhile to explicitly mention the assumptions considered in the theory proposed in [4] and in this paper.

First, the analyses in [4] as well as in this paper are limited to a quasi-static representation of the weakly nonlinear function that describes the capacitance (in Farads) vs voltage: $C(V) = \frac{dQ}{dV}$ [3], [17]. This allows using a power series with scalar coefficients to define a nonlinear capacitance function $C(v_S)$ [3], [17] that represents the variation of the capacitance value with the instantaneous voltage defined by a time-dependent AC signal $v_s(t)$ (without DC) applied to it. For a given controllable nonlinear capacitance, any new DC bias voltage value or any increase in the amplitude of $v_s(t)$ requires a different $C(v_S)$ nonlinear function. Note that quasi-static representations of weakly non-linear capacitances have been demonstrated to properly predict the nonlinearities at large signal power levels (e.g. [18]).

Second, the nonlinear capacitance $C(v_S)$ is analyzed using the circuit in Fig.3 where the ideal 0Ω voltage source is given by (1). It is a 2 equal-tone signal of amplitude A and at angular frequencies ω_1 and ω_2.

$$v_S(t) = A \cdot \cos(\omega_1 t) + A \cdot \cos(\omega_2 t) \tag{1}$$

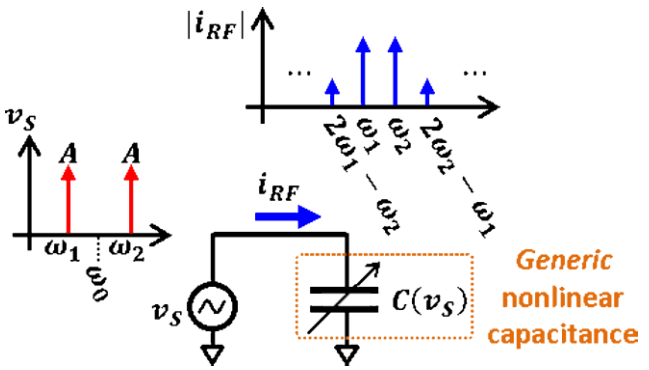


FIGURE 3. Circuit to analyze the nonlinear RF current (i_{RF}) generated by a nonlinear capacitance ($C(v_S)$).

In Fig.3, $v_S = 0V$ at all frequencies other than ω_1 and ω_2. In this ideal context, the only contributor to harmonics and intermodulation distortion (IMD) products in the RF current i_{RF} is the intrinsic nonlinear behavior of the capacitance $C(v_S)$ as no other component influences the distortions in i_{RF}.

In a practical implementation, the non-zero external impedances have an important effect on circuit linearity, an aspect that will be dealt with in section III-B.

2) NONLINEARITIES OF A GENERIC NONLINEAR CAPACITANCE

This subsection analyzes the nonlinear behavior of a *generic* nonlinear capacitance $C(v_S)$. In subsequent subsections, this generic $C(v_S)$ is appropriately substituted by specific varactor-based topologies under study. This allows analyzing the nonlinear behavior associated to a specific topology.

The nonlinear capacitance $C(v_S)$ in Fig.3 is modeled with the power series given by (2):

$$C\left(v_S\right) = C_0 + C_1 \cdot v_S + C_2 \cdot [v_S]^2 + \cdots + C_n \cdot [v_S]^n \quad (2)$$

As stated earlier, a new set of scalar coefficients C_0 to C_n is required with any new DC bias voltage or any increase in the amplitude of $v_s(t)$.

The nonlinear behavior of $C\left(v_S\right)$ within the circuit in Fig.3 is analyzed using nonlinearities of the RF current i_{RF}, which is calculated using (3a) [3], [17].

$$i_{RF}\left(t\right) = C\left(v_S\right) \cdot \frac{d\left[v_S(t)\right]}{dt} \quad (3a)$$

Substituting $C\left(v_s\right)$ given by (2) in (3a) gives (3b) [17].

$$i_{RF}\left(t\right) = \left(C_0 + C_1 \cdot v_S(t) + C_2 \cdot [v_S(t)]^2 + \cdots\right) \cdot \frac{d\left[v_S(t)\right]}{dt} \quad (3b)$$

By substituting $v_S(t)$ with its value in (1), (3b) becomes (4).

$$i_{RF}\left(t\right) = \begin{pmatrix} C_0 \\ +C_1 \cdot [A \cdot \cos\left(\omega_1 t\right) + A \cdot \cos\left(\omega_2 t\right)] \\ +C_2 \cdot [A \cdot \cos\left(\omega_1 t\right) + A \cdot \cos\left(\omega_2 t\right)]^2 + \cdots \end{pmatrix} \cdot \frac{d\left[A \cdot \cos\left(\omega_1 t\right) + A \cdot \cos\left(\omega_2 t\right)\right]}{dt} \quad (4)$$

A 3rd order expansion of (4) allows associating each capacitor coefficients (C_0, C_1, and C_2 of the power series in (2)) with the various frequency components in i_{RF} generated by $C(v_S)$. While higher-order contributors greater than the 3rd order are present in (4), their values are not considered in this paper for compactness of the equations. Besides, such higher-order terms have a significantly smaller effect on the overall circuit linearity.

Circuit linearity performances in this paper are measured using the intermodulation (IM) distortion products at the angular frequency $2\omega_2 - \omega_1$ or equivalently at $2f_2 - f_1$ ($IMD_{2f_2-f_1}$) [17]. The notation $IMD_{2f_2-f_1}$ is preferred over the common IMD3 notation since multiple IM products contribute to the level of distortion at $2f_2 - f_1$ in the simulation and experimental results.

After a 3rd order expansion of (4), the $IMD_{2f_2-f_1}$ levels in i_{RF}, which stem from the product of the 2nd degree term and the derivative term, are found to be:

$$IMD_{2f_2-f_1} = \frac{i_{RF}\left(2\omega_2 - \omega_1\right)}{i_{RF}\left(\omega_2\right)} = \frac{A^2 C_2\left(2\omega_2 - \omega_1\right)}{\omega_2\left(3A^2 C_2 + 4C_0\right)} \quad (5)$$

As can be seen in the numerator of (5), C_2 may be used to reduce or cancel the distortion at $2f_2 - f_1$ in a varactor-based controllable impedance network. The remainder of the analyses presented in this paper discusses various methods of minimizing the coefficient C_2 associated to tunable-capacitor elements that are built in the form of varactor-based networks. This will allow the study of $IMD_{2f_2-f_1}$ level reduction, depending on the parasitics included in the different embodiments that will be presented.

3) EXPRESSION FOR SELECTED OFF-THE-SHELF VARACTOR CAPACITANCE

For the targeted application illustrated in Fig.1, this work uses the off-the-shelf GaAs flip-chip varactor MA46H120 from MACOM [19] because of its wide capacitance tuning range and its low series parasitic resistance (R_S). Equation (6) is the expression of the nonlinear capacitance to voltage relationship given by the manufacturer and widely used in the literature. In (6), C_{j0} is the zero-bias junction capacitance, V_{DC} is the bias voltage of the varactor, v is the RF voltage across the varactor, V_J is the junction potential, and M is the grading coefficient.

$$C\left(V_{DC}, v\right) = \frac{C_{j0}}{\left(1 + \left[\frac{V_{DC}+v}{V_J}\right]\right)^M} \quad (6)$$

It is possible to reformulate (6) with the help of a Taylor series expansion (not shown here for conciseness) as a function of v, yielding a power series (as in (2)) with coefficients $C_n = C_0, C_1, C_2, \cdots$ that depend on V_{DC}, C_{j0}, V_J, and M. This expansion will be used in later sections.

4) FORMULATION FOR PARASITIC-FREE ANTI-SERIES NONLINEAR CAPACITANCE

This subsection analyzes the nonlinear behavior of the parasitic-free anti-series varactor topology shown in Fig.4.

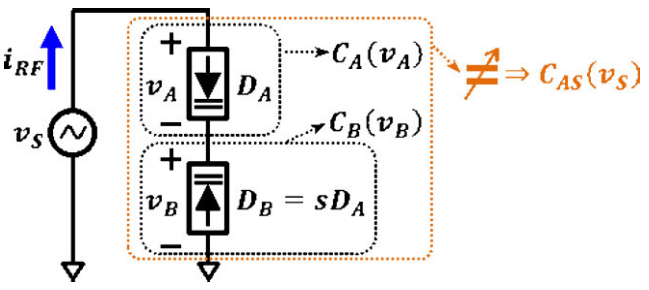


FIGURE 4. Circuit to analyze i_{RF} generated by the parasitic-free anti-series topology. As in Fig.2, varactors are biased at V_{DC} through a high impedance network Z_C (not shown for simplification).

The equivalent capacitance $C_{AS}\left(v_S\right)$ in Fig.4 is a stack of two nonlinear capacitances $C_A(v_A)$ and $C_B\left(v_B\right)$ with $v_S = v_A + v_B$, where v_A and v_B are the AC voltages across the capacitances C_A and C_B respectively. The only circuit elements present in $C_A(v_A)$ and $C_B\left(v_B\right)$ are the two varactors which are defined respectively by their different sizes D_A and D_B.

Also, D_A and D_B are related through the ratio s of their sizes, i.e. $D_B = sD_A$. $C_A(v_A)$ and $C_B(v_B)$ may be expressed with the power series given in (7) where $C_{An} = C_{A0}, C_{A1}, C_{A2}$ and $C_{Bn} = C_{B0}, C_{B1}, C_{B2}$ are dependent on the nonlinearities associated to $C_A(v_A)$ and $C_B(v_B)$ respectively.

$$C_A(v_A) = C_{A0} + C_{A1} \cdot v_A + C_{A2} \cdot [v_A]^2 + \cdots$$
$$C_B(v_B) = C_{B0} - C_{B1} \cdot v_B + C_{B2} \cdot [v_B]^2 + \cdots$$

With C_{A0}, C_{B0} determined from (6) as:

$$\begin{aligned} C_{A0} &= C_0 \quad C_{B0} = s \cdot C_0 \\ C_{A1} &= C_1 \quad C_{B1} = s \cdot C_1 \\ C_{A2} &= C_2 \quad C_{B2} = s \cdot C_2 \end{aligned} \tag{7}$$

The varactor associated to C_A is modeled with (6) and the coefficients $C_{An} = C_{A0}, C_{A1}, C_{A2}, \cdots$ are obtained with a Taylor series expansion of (6) as a function of v. The coefficients C_{Bn}, assuming the same type of varactor, are subsequently derived from C_{An} considering the scaling relationship $D_B = sD_A$. The values of C_{An} and C_{Bn} are given in (7).

Starting from the values of C_{An} and C_{Bn} in (7), the power series $C_{AS}(v_S)$ that describes the intrinsic nonlinear behavior of the topology in Fig.4 (in orange) is formulated with (8) (equivalent to (3) to (5) in [4]). Appendix details the derivation of the coefficients $C_{ASn} = C_{AS0}, C_{AS1}, C_{AS2}$ in (8). Note that C_0 is left unexpanded in (8) for conciseness.

$$C_{AS}(v_S) = C_{AS0} + C_{AS1} \cdot v_S + C_{AS2} \cdot [v_S]^2 + \cdots$$

where

$$C_{AS0} = \left[\frac{s}{s+1}\right] \cdot C_0$$
$$C_{AS1} = \left[\frac{s \cdot (s-1)}{(s+1)^2}\right] \cdot C_0 \cdot \left[\frac{M}{(V_J + V_{DC})}\right]$$
$$C_{AS2} = \left[\frac{1}{2} \cdot \frac{\alpha_2}{(s+1)^3}\right] \cdot C_0 \cdot \left[\frac{M}{(V_J + V_{DC})^2}\right]$$

with

$$\alpha_2 = s \cdot \left((M+1) \cdot s^2 + (-4M-1) \cdot s + M + 1\right) \tag{8}$$

Equation (8) allows computing the resulting $i_{RF}IMD_{2f_2-f_1}$ levels in the circuit of Fig.4. Equation (5) is used for this computation by substituting the coefficients $C_n = C_0, C_1, C_2$ with $C_{ASn} = C_{AS0}, C_{AS1}, C_{AS2}$.

In [4], the use of hyper-abrupt ($M \geq 1$) varactors is made possible by introducing the diode-size scaling parameter s (unmatched varactors) which allows designing for $\alpha_2 = 0$ in (8) to cancel C_{AS2}. By associating C_{AS2} to C_2 in the numerator of (5), it can be seen that this results in lower 3rd order distortions. Designing for $\alpha_2 = 0$ is achieved by solving for the required value of the diode-size ratio (s) with (9), as a function of the value M dictated by the choice of varactor.

$$s_{IDEAL} = \frac{1}{2} \cdot \frac{4 \cdot M + 1 + \sqrt{12 \cdot M^2 - 3}}{(M+1)} \tag{9}$$

However, unlike the technique in [3] which uses matched ($s = 1$) abrupt ($M = 0.5$) anti-series varactors and where *all* distortion components (i.e. related to $C_{AS1}, C_{AS2}, C_{AS3}$, etc.) are canceled, the technique using unmatched-size and hyper-abrupt varactors in [4] does *not* allow for a cancellation of all even-order and all higher odd-order (greater than 3rd order) distortion components. Moreover, the very presence of even-order distortion components in the varactor currents (i_{RF} in Fig.4) yields degraded linearity performances due to a secondary mixing mechanism caused by the presence of a non-zero source impedance connected to the anti-series network. In [4], this problem is overcome by introducing the anti-series/anti-parallel network (Fig.2b) to cancel all even-order as well as the 3rd order nonlinearities.

However, in practical implementations relying on hyper-abrupt varactor-based anti-series-*only* topologies, the non-cancellation of even-order distortion components constitutes a limiting factor. In that regard, a solution to minimize the effects of the secondary mixing mechanism in the presence of a non-zero source impedance, when using hyper-abrupt anti-series-*only* topologies has not been proposed. This paper proposes a technique to address this in section III-B.

B. NONLINEARITIES OF ANTI-SERIES TOPOLOGY IN THE PRESENCE OF SIGNIFICANT PARASITICS

The formulations in the literature so far (e.g. [4], [7]) are limited to parasitic-free varactors, and to the best of the authors' knowledge, the negative impact of parasitic capacitances and inductances on linearity in anti-series varactor topologies has never been reported.

In part 1) of this subsection, we demonstrate the detrimental effect of parallel parasitic capacitances in the distortion mechanism of unmatched hyper-abrupt varactor-based anti-series topologies by extending the preceding equations. Moreover, in part 2), the negative impact of series inductances on linearity is analyzed.

Fig.5 is the model of the GaAs flip-chip varactor MA46H120 considered in this paper [19]. This model includes three parasitic elements: a series resistance (R_S), a parallel linear capacitance (C_P), and a series linear inductance (L_S). The parameters listed in Table 2 are considered in the analyses that follow. Note that the parasitic capacitance C_P is expressed also as a normalized value with respect to C_{j0} (i.e. N_{CP} in %). Also note that, given $M = 2.256$, (9) yields $s_{IDEAL} \approx 2.71$.

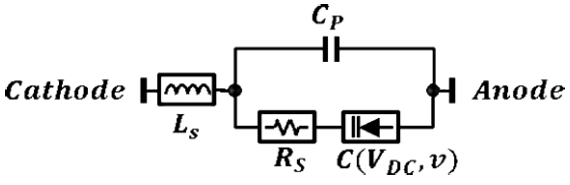


FIGURE 5. Model of the varactor MA46H120 including parasitics [19].

TABLE 2. MA46H120 varactor parameters.

C_{j0}	$1.09pF^{*1}$
V_J	$4.445V^{*1}$
M	2.256^{*1}
$C_P \,/\, \left[N_{CP} = \frac{C_P}{C_{j0}}(in\ \%)\right]$	$139fF^{*1} \,/\, [12.8\%]^{*2}$
R_S	$0\Omega^{*3}$
L_S	$\sim 300pH^{*4}$
s_{IDEAL}	2.71^{*5}
$V_{Turn-on}$	$0.5V^{*1}$
$V_{Breakdown}$	$-27.4V^{*1}$

[*1]Data provided in [19]. [*2] Highlights the significance of C_P relative to C_{j0}
[*3]Identified as 0.88Ω in [19] but is neglected in analytical analysis.
[*4]Estimated from experimental measurements. [*5]Computed with (9).

1) EFFECT OF PARALLEL PARASICITC CAPACITANCE ON LINEARITY

This subsection describes the intrinsic nonlinear behavior of an unmatched ($s > 1$) anti-series-only topology including parasitic capacitances (C_P). For the purpose of focusing on the effects of C_P on linearity, the varactor model in Fig.5 is considered with $C_P \neq 0F$, $L_S = 0H$ and $R_S = 0\Omega$.

Individually-packaged varactor components are considered in this work. Therefore, the size ratio s between the two varactors in Fig.6 is accounted for by using a first diode of size D_A connected in anti-series with a set of identical diodes in parallel (of size $D_B = s \cdot D_A$). As seen in Fig.5, the parasitic linear capacitance C_P is in parallel with the diode. Thus, paralleling s diodes also increases C_P by s. The resulting circuit for the analysis of the intrinsic nonlinear behavior of an anti-series-only topology including C_P is shown in Fig.6. The nonlinear capacitance $C_A(v_A)$ includes the nonlinear capacitance of the varactor of size D_A and its associated parasitic C_P, while $C_B\,(v_B)$ includes the circuit elements associated to $C_A\,(v_A)$, but scaled by s.

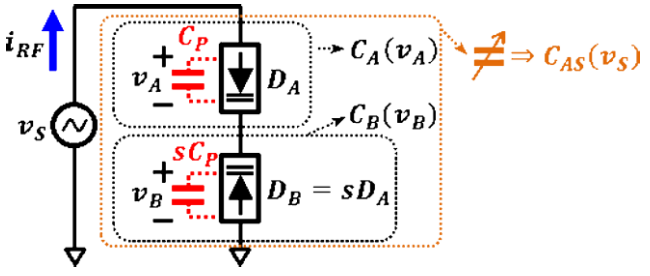


FIGURE 6. Anti-series-only topology including parallel parasitic capacitances (C_P). As in Fig.2, varactors are biased at V_{DC} through a high impedance network Z_C (not shown for simplification).

$C_A(v_A)$ and $C_B\,(v_B)$ are formulated with power series, this time including C_P, as in (10). The values of $C_{An} = C_{A0}, C_{A1}, C_{A2}$ and $C_{Bn} = C_{B0}, C_{B1}, C_{B2}$ in (10) are dependent on the circuit elements associated to $C_A(v_A)$ and $C_B\,(v_B)$ respectively, in Fig.6.

$$C_A\,(v_A) = C_{A0} + C_{A1} \cdot v_A + C_{A2} \cdot [v_A]^2 + \cdots$$
$$C_B\,(v_B) = C_{B0} - C_{B1} \cdot v_B + C_{B2} \cdot [v_B]^2 + \cdots$$

With

$$\begin{aligned} C_{A0} &= C_0 + C_P \quad C_{B0} = s \cdot (C_0 + C_P) \\ C_{A1} &= C_1 \quad C_{B1} = s \cdot C_1 \\ C_{A2} &= C_2 \quad C_{B2} = s \cdot C_2 \end{aligned} \tag{10}$$

In Fig.6, the resulting equivalent nonlinear capacitance $C_{AS}(v_s)$ (orange rectangle) is expressed by the power series (11), with coefficients $C_{ASn} = C_{AS0}, C_{AS1}, C_{AS2}$ that are derived in appendix, starting from the values of C_{An} and C_{Bn} in (10).

$$C_{AS}\,(v_S) = C_{AS0} + C_{AS1} \cdot v_S + C_{AS2} \cdot [v_S]^2 + \cdots$$

where

$$C_{AS0} = \left[\frac{s}{s+1}\right] \cdot (C_0 + C_P)$$
$$C_{AS1} = \left[\frac{s \cdot (s-1)}{(s+1)^2}\right] \cdot C_0 \cdot \left[\frac{M}{(V_J + V_{DC})}\right]$$
$$C_{AS2} = \left[\frac{1}{2} \cdot \frac{\alpha_2}{(s+1)^3}\right] \cdot C_0 \cdot \left[\frac{M}{(V_J + V_{DC})^2}\right]$$

with

$$\alpha_2 = s \cdot \left((M+1) \cdot s^2 + K \cdot s + M + 1\right)$$
$$K = M \cdot \frac{(-4 \cdot C_0 - C_P)}{(C_0 + C_P)} - 1 \tag{11}$$

We now focus on the $IMD_{2f_2-f_1}$ levels of RF current i_{RF} shown in Fig.6, which are computed with the help of (10) and appendix. It will be shown that these $IMD_{2f_2-f_1}$ levels are severely degraded due to the presence of parasitic C_P.

The computation of the $i_{RF}IMD_{2f_2-f_1}$ levels takes into account all the MA46H120 varactor parameters (Table 2), all the other circuit variables (Table 3) and a variable C_P value normalized with respect to C_{j0} ($N_{CP} = C_P/C_{j0}$ in %). The results are shown in Fig.7 for N_{CP} varying from 0.1% to 12.8%.

TABLE 3. Default circuit parameters to compute $i_{RF}IMD_{2f_2-f_1}$.

Varactors parameters	Parameters listed in Table II including $s = s_{IDEAL} \approx 2.71$ [*1]
RF voltage source	2-tone signal in (1) with: $A = 1V$, f_1 and $f_2 = f_0 \pm f_{ENV}$, $f_0 = 3.6GHz$, $f_{ENV} = 5MHz$ (spacing of 10MHz)
V_{DC} values	0V to 25V with steps of 0.1V
C_{An} and C_{Bn}	According to the topology analyzed

[*1] $s_{IDEAL} \approx 2.71$ computed with (9) is used since it remains a near-optimal value, and it allows evaluating the effect of a change in C_P only.

At an available power of $P_{AVS} = 18dBm$, the worst case $IMD_{2f_2-f_1}$ level in i_{RF} is about $-45dBc$ and corresponds to

the case $N_{CP} = 12.8\%$ with $V_{DC} = 0V$. However, for the purpose of simplifying comparisons between $IMD_{2f_2-f_1}$ performances in multiple conditions (ratio s, bias voltage V_{DC}, parasitics, etc.), all levels in Fig.7 are normalized such that the worst case with $N_{CP} = 12.8\%$ and $V_{DC} = 0V$ translates into $IMD_{2f_2-f_1} = 0dBc$. This allows setting a Figure of Merit (FoM) for linearity performance and which will be used throughout this paper, defined as the worst case linearity in dBc over the full range of the bias voltage V_{DC}. In Fig.7, it implies an FoM of $0dBc$ for $N_{CP} = 12.8\%$ (marker *(3)*), of $-13.9dBc$ for $N_{CP} = 2\%$ (marker *(2)*) and of $-37dBc$ for $N_{CP} = 0.1\%$ (marker *(1)*).

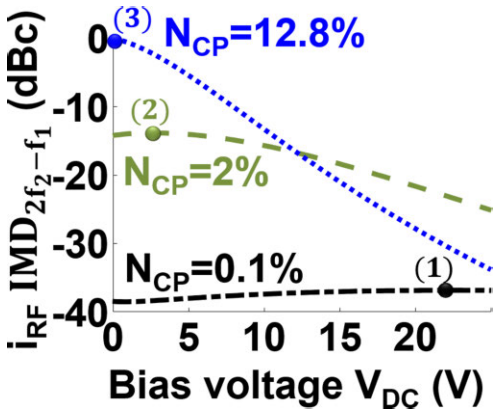


FIGURE 7. Computed $i_{RF}IMD_{2f_2-f_1}$ levels as a function of V_{DC} of the circuit in Fig.6. Note that markers (1) to (3) identify the *FoM* of each case of N_{CP}.

Note that $N_{CP} = 12.8\%$ stems from the choice of the varactor MA46H120 (Table 2). The linearity performances of the topology in Fig.6 implemented with this varactor is used for benchmarking purposes in this paper.

As can be seen in Fig.7, even when considering a hypothetical case with N_{CP} as low as 2%, the FoM improvement relative to the case $N_{CP} = 12.8\%$ is reduced by only $13.9dB$ (marker *(2)* with respect to marker *(3)*), which is a marginal improvement compared to the nearly-ideal case of $N_{CP} = 0.1\%$ (marker *(1)*). Therefore, in our applications where packaged varactors with $N_{CP} \approx 12.8\%$ are typical, relying on lower N_{CP} to improve linearity is not a solution.

This justifies the need for linearity improvement techniques for applications such as ours, to compensate the linearity degradation due to capacitive parasitics (C_P).

Next, the potential of compensating the linearity degradation due to C_P by varying s is evaluated.

The computations with $N_{CP} = 12.8\%$ show an FoM improvement of only $\sim 8.4dB$ relative to marker *(3)* (i.e. still significantly higher that marker *(2)*) when the scaling factor s is swept. This points to the inefficacity of simply adjusting the ratio of diode sizes s in the anti-series topology to compensate the negative effect of C_P on linearity. It is attributed to the dependence of α_2 on C_0 in (11), when C_P is present. While α_2 in (8) (C_P-free case) may be cancelled over the full range of the bias voltage V_{DC} with the proper scaling factor s, α_2 in (11) may only be cancelled over a narrow range of V_{DC} with a specific value of s, given the presence of C_0 in (11) and its dependence on V_{DC}. This is a serious limitation in this type of anti-series implementation, when a highly linear and controllable capacitance network with a wide tunable range is desired.

The above considerations demonstrate that the existing distortion cancellation technique applied to two unmatched series-connected hyper-abrupt varactors is *not effective* in the presence of significant parasitic capacitance C_P. This justifies the need for linearity improvement techniques. An improved anti-series-only network that allows improving the linearity performances in the presence of C_P is proposed in section III-A of this paper.

2) EFFECT OF SERIES PARASITIC INDUCTANCE ON LINEARITY

We now analyze the nonlinear behavior of an anti-series topology in the presence of series parasitic inductances. This analysis uses the varactor model in Fig.5 with $L_S \neq 0$, $C_P = 139fF$ ($N_{CP} = 12.8\%$) and $R_S = 0.88\Omega$.

Considering identical diodes in parallel, each represented by the network of Fig 5, the inductances in these networks may be combined in parallel using the symmetry principle to determine the equivalent inductance associated with the entire network of diodes. Moreover, this network of parallel diodes resulting in the size $s \cdot D_A$ may be augmented with an additional diode of size D_A to represent the anti-series topology, and the inductances in the resulting network may be summed as an equivalent series inductance L_{EQ}. The expression of L_{EQ} is given by (12). Note that (12) neglects any mutual inductance phenomena for simplification purposes but still adequately captures the negative impact of L_S on linearity.

$$L_{EQ} = L_S \cdot \left(\frac{s+1}{s}\right) \tag{12}$$

A single series equivalent inductance allows analyzing the effect of L_S on linearity in i_{RF} with the circuit in Fig.8 by substituting the non-zero series impedance Z_L with L_{EQ}. In Fig.8, the impedance seen by the voltage source v_s is identified as $Z_{TOT} = Z_L + Z_{CAS(v_{AS})}$ where $Z_{CAS(v_{AS})}$ is the impedance of $C_{AS}(v_{AS})$. Due to the presence of Z_L, the nonlinear capacitance $C_{AS}(v_{AS})$ expressed in (11) is no longer a function of the ideal source voltage v_S, but varies as a function of the AC voltage v_{AS}. This means that the analysis given in section II-B1, which includes the effect of parasitic capacitance C_P only, is not sufficient when $Z_L \neq 0$.

In the circuit of Fig.8, two mechanisms generate nonlinearities at the voltage node v_{AS}: (i) the intrinsic nonlinear behavior of the anti-series topology (section II-B1) and (ii) a secondary mixing mechanism, due to the presence of Z_L. This latter mechanism is mentioned in the literature (e.g. [4]), but only for an undefined non-zero source impedance Z_L.

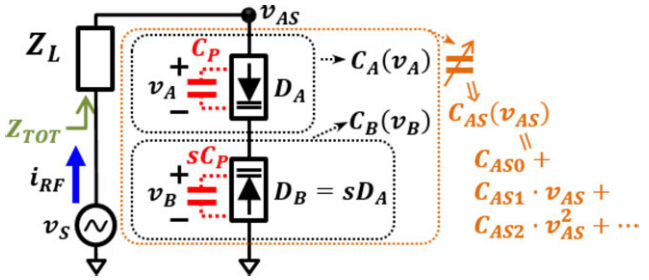


FIGURE 8. Anti-series-only topology including C_P driven by a non-zero source impedance Z_L. As in Fig.2, varactors are biased at V_{DC} through a high impedance network Z_C (not shown for simplification).

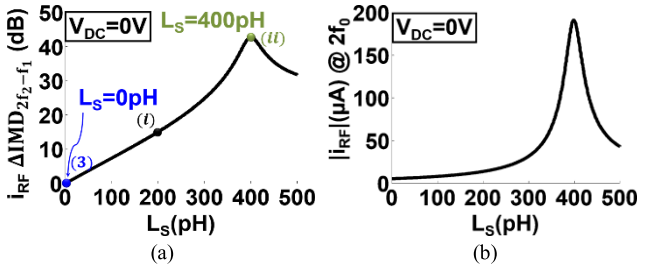


FIGURE 9. a) Increase of $i_{RF}IMD_{2f_2-f_1}$ level with L_S at a bias voltage of $V_{DC} = 0V$ b) $|i_{RF}|$ at $2f_0$ as a function of L_S at a bias voltage of $V_{DC} = 0V$.

Next, the secondary mixing mechanism in the presence of inductive Z_L is explained and its severe negative impact on linearity is demonstrated.

The intrinsic nonlinear behavior of the anti-series circuit generates nonlinear current components in i_{RF} in Fig.8, where v_S is the 2-tone excitation centered at f_0 defined by (1). These nonlinear i_{RF} current components, in turn, generate nonlinear voltage components at the node v_{AS} through the ohmic interaction between i_{RF} and Z_L. As a result, secondary mixing products occur, given the nonlinear voltage content of v_{AS} that is now present across the nonlinear capacitance ($C_{AS}(v_{AS})$). In our context, a key mixing product is the one between the fundamental voltage tones centered at f_0 (i.e. f_1, f_2) and voltage components in the vicinity of $2f_0$ (e.g. $2f_1$, f_1+f_2, $2f_2$) within v_{AS}. This yields additional contributors to $IMD_{2f_2-f_1}$ products (one example being the mixing product $2[f_2+f_1]-f_1 = 2f_2-f_1$). The simulations presented next will show that this secondary mixing mechanism is detrimental to linearity. The worst-case is when L_{EQ} and the capacitance network C_{AS} allow a series resonance in the vicinity of $2f_0$. This corresponds to $|Z_{TOT}|\ @2f_0 \rightarrow 0\Omega$ which allows significantly higher i_{RF} and v_{AS} components in the vicinity of $2f_0$. As a result, the contributors due to this secondary mixing mechanism further degrade the $IMD_{2f_2-f_1}$ levels.

The aforementioned explanation stating that the presence of inductive series parasitics (L_S) yields linearity degradation is confirmed by results from the simulation of the circuit in Fig.8 with Z_L substituted by L_{EQ}. In these harmonic balance simulations using ADS^{TM}, all the varactor parameters in Table 2 and all the circuit variables in Table 3 are considered, except for $A = 0.01V$ and a variable L_S (i.e. L_{EQ} is swept). Fig.9 presents conclusive results regarding L_S.

For performance evaluation, the highest $IMD_{2f_2-f_1}$ level obtained across the V_{DC} bias voltage range is considered as the linearity Figure of Merit (as defined in section II-B1).

All $IMD_{2f_2-f_1}$ levels in Fig.9 are normalized such that the case $L_S = 0pH$ with $V_{DC} = 0V$ (marker *(3)*) translates into $0dBc$. This also means that any linearity degradation compared to marker *(3)* is attributed to the presence of L_S.

Fig.9a plots the increase of $i_{RF}IMD_{2f_2-f_1}$ levels as a function of L_S with $V_{DC} = 0V$. It shows a significant degradation of $IMD_{2f_2-f_1}$ with an increasing L_S between $0pH$ and $\sim 300pH$. This is because an increasing L_S (and L_{EQ} according to (12)) in series with $C_{AS}(v_{AS})$ translates into a decreasing resulting reactance seen by v_S, hence an increasing i_{RF}, which in turn translates into an increasing RF voltage across each nonlinear junction capacitance within the varactor and consequently higher $IMD_{2f_2-f_1}$. The peak at $L_S \approx 400pH$ results from $L_{EQ} \approx 550pH$ (12) resonating at the frequency $2f_0$ with $C_{AS0} \approx 0.9$pF (computed with (11)) when $V_{DC} = 0V$. Fig.9b supports the above explanation. It shows that $|i_{RF}|$ at $2f_0$ reach a peak at the same L_S value as for the curve of Fig.9a, i.e. when resonance at $2f_0$ occurs.

The overall $IMD_{2f_2-f_1} - L_S$ relationship in Fig.9a demonstrates that the L_S associated to diode's technology and assembly (semiconductor technology, wire-bond or flip-chip connectivity, discrete diode devices or MMIC designs, etc.) has the potential of severely degrading circuit linearity and is a limiting factor in regards with the maximum frequency of operation of a given technology.

Moreover, the above analysis may be extended to series interconnect transmission lines presenting significant electrical lengths and which have a similar negative impact on linearity as with L_S. As a case example illustrated in Fig.10, a connection network used with the anti-series/anti-parallel topology (Fig.2b) inherently adds series parasitics between the two anti-series branches. If the electrical length of this connection network is significant (e.g. in a 3.6GHz design requiring discrete components on a PCB), the above analysis shows that this topology inevitably yield degraded linearity

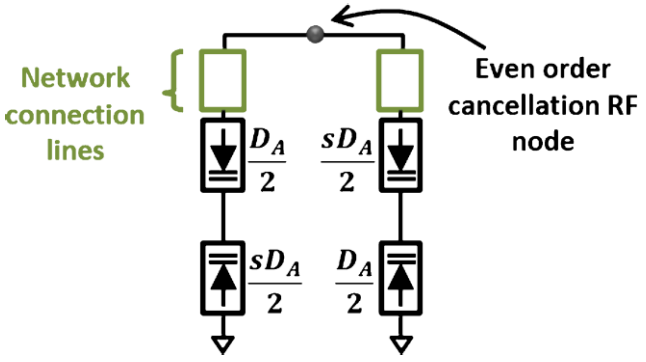


FIGURE 10. Anti-series/anti-parallel topology including significant series parasitics within the network connection lines.

performances. As a solution to minimize the effect of such connectivity network, an alternative to the anti-series/anti-parallel topology is proposed in section III-B.

III. PROPOSED MODIFIED ANTI-SERIES TOPOLOGY FOR IMPROVED LINEARITY IN THE PRESENCE OF PARASITICS

This section presents an improved anti-series-only topology introducing two major innovations. (i) It enhances circuit linearity of hyper-abrupt varactor-based controllable networks in the presence of significant parasitic parallel capacitance (C_P), and (ii) it desensitizes its linearity performances from source impedance loading effects without the necessity of doubling the number of required varactors as required in the state-of-the-art anti-series/anti-parallel topology (Fig.2b). Moreover, (ii) offers the additional advantage of minimizing the linearity degradation due to the connection network compared to the circuit in Fig.10. These two innovative concepts are presented in section III-A and section III-B respectively.

A. ANTI-SERIES-ONLY TOPOLOGY WITH ENHANCED LINEARITY PERFORMANCES IN THE PRESENCE OF C_P

The linearity enhancement of a varactor-based anti-series topology, as reported in the literature so far, is achieved through the optimization of the ratio between the diode sizes (s) to enable a 3rd order distortion cancellation. This was shown in section II-A4 by designing for $\alpha_2 = 0$ in (8), hence $C_{AS2} = 0$, yielding the ideal ratio $s = s_{IDEAL}$ as in (9). However, as demonstrated in section II-B1, this nonlinearity-cancellation mechanism is significantly impaired by the parasitic C_P, yielding poor overall linearity performances. The negative impact of C_P on linearity is significantly reduced with the *modified* anti-series network proposed here.

We first examine the underlying concept with the help of the circuit in Fig.11. It will be demonstrated that the linearity degradation due to C_P may be minimized with a compensation technique that allows adjusting the capacitance ratio between C_A and C_B, independently of s.

For the purpose of this demonstration, Fig.11 includes nonlinear capacitances $C_A(v_A)$ and $C_B(v_B)$ that may be tuned

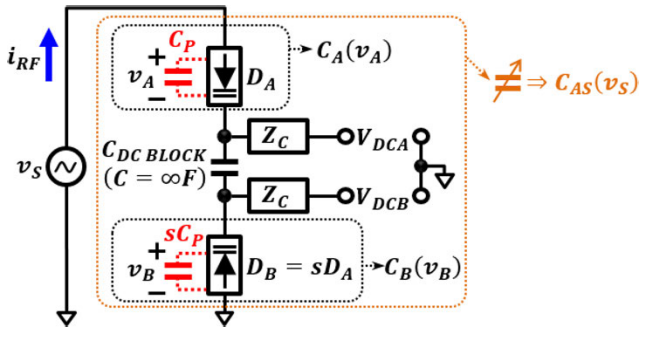


FIGURE 11. Dual-biased anti-series topology in the presence of C_P. D_A and D_B are biased at V_{DCA} and V_{DCB}, respectively, through a high impedance network Z_C. V_{DCA} and V_{DCB} are decoupled with C_{BLOCK} which has an ideal infinite impedance at DC and 0Ω at all other frequencies.

independently, thanks to the biasing of D_A and D_B with separated bias voltages (V_{DCA} and V_{DCB}). The ideal decoupling capacitance ($C_{DC\ BLOCK}$ in Fig.11) is necessary in this analysis to maintain an infinite impedance at DC and an ideal 0Ω at all other frequencies, including down to baseband frequencies (f_{ENV}). These hypothetical conditions allow maintaining an optimal capacitance ratio between C_A and C_B even in the presence of significant parasitics C_P, yielding enhanced linearity performances. This is shown next.

$$C_A(v_A) = C_{A0} + C_{A1} \cdot v_A + C_{A2} \cdot [v_A]^2 + \cdots$$
$$C_B(v_B) = C_{B0} - C_{B1} \cdot v_B + C_{B2} \cdot [v_B]^2 + \cdots$$

With

$$\begin{aligned} C_{A0} &= C_{0\alpha} + C_P \quad C_{B0} = s \cdot (C_{0\beta} + C_P) \\ C_{A1} &= C_{1\alpha} \quad C_{B1} = s \cdot C_{1\beta} \\ C_{A2} &= C_{2\alpha} \quad C_{B2} = s \cdot C_{2\beta} \end{aligned} \tag{13}$$

With the help of (13) and appendix, while considering the varactor parameters in Table 2 and all the other circuit variables in Table 3, the $IMD_{2f_2-f_1}$ levels of the RF current i_{RF} are computed. The objective of these computations is to minimize the distortions by optimizing the value of V_{DCB} for every given value of V_{DCA} over its full range. Fig.12a presents the optimal V_{DCB} bias voltage profile applied to the diode D_B as a function of V_{DCA}.

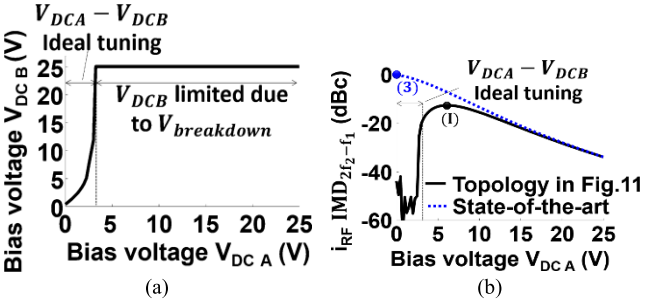


FIGURE 12. a) V_{DCB} vs V_{DCA} bias profile which optimizes circuit linearity b) i_{RF} $IMD_{2f_2-f_1}$ level (solid curve) of the circuit in Fig.11 when using the V_{DCB} vs V_{DCA} bias profile of a) benchmarked against the $IMD_{2f_2-f_1}$ level of the topology including C_P with S_{CP} = 12.8% (blue curve). Markers *(3)* and *(I)* identify the *FoM* of each curve.

Over the range of V_{DCA} values from $0V$ to $3.25V$ (identified as "$V_{DCA} - V_{DCB}$ ideal tuning" in Fig.12a), it is possible to select the optimal value of V_{DCB} to achieve maximal linearity improvement. Above $V_{DCA} = 3.25V$, the value of V_{DCB} that would enable optimal $IMD_{2f_2-f_1}$ cancellation is higher than the diode's breakdown voltage. Therefore V_{DCB} is kept fixed at $25V$ for $V_{DCA} \geq 3.25V$.

To evaluate the linearity improvement from the use of independent bias as in Fig.11 in the presence of $C_P = 139fF$ ($N_{CP} = 12.8\%$), the linearity performance (black curve in Fig.12b) associated with the optimal V_{DCB} vs V_{DCA} bias profile of Fig.12a is computed using the same normalization as in Fig.7 (i.e. marker (3) equal $0dBc$). Fig.12b therefore allows benchmarking the linearity *FoM* (as defined earlier)

of the topology in Fig.11 against the *FoM* of the anti-series topology in Fig.6 with identical $C_P = 139fF$ (the blue curves in Fig.7 and Fig.12 are the same).

It can be seen that in the range "$V_{DCA}-V_{DCB}$ ideal tuning", the $IMD_{2f_2-f_1}$ levels are improved by more than $\sim 40dB$. This demonstrates the feasibility of achieving excellent linearity improvement despite the presence of C_P, assuming the hypothetical case where a dual (separate) bias scheme as in Fig.11 is used. Above this ideal tuning range, the linearity improvement being less significant is due to the voltage breakdown limitation, which does not allow maintaining an optimal $V_{DCA} - V_{DCB}$ profile.

The topology in Fig.11 adds circuit complexities that make it prohibitive for a practical implementation (e.g. requiring $C_{DC\ BLOCK} = \infty$). However, the above analysis based on Fig.11 allows drawing an important conclusion.

The linearity improvement shown in Fig.12b is achieved with the V_{DCB} vs V_{DCA} bias profile of Fig.12a, which shows that the condition $V_{DCA} < V_{DCB}$ is required. Hence, a bias condition in Fig.11 where V_{DCB} is set at some DC voltage V_1, while V_{DCA} is set at a DC voltage $V_2 < V_1$ translates necessarily into $C_A|_{V_2} > \left[\frac{C_B|_{V_1}}{s} = \frac{sC_A|_{V_1}}{s} = C_A|_{V_1}\right]$ according to (6). It can be concluded then that the linearity degradation due to C_P may be reduced by increasing the capacitance of C_A relative to the capacitance of C_B. This must be achieved independently of the capacitance C_P, which does not vary with the bias voltage, and thus may not be achieved by adjusting the size ratio s. Moreover, in a practical implementation restricted to a unique bias voltage, it cannot be accomplished neither by setting $V_{DCA} \leq V_{DCB}$. Therefore, the solution proposed in this paper is to add a lumped capacitance in parallel with C_A.

It is worth recalling also that, although modifying the diode-size ratio s allows adjusting the ratio between C_A and C_B, the *FoM* improvement in the presence of C_P as a function of s can only be of limited value, as explained in section II-B1, hence does not substitute the proposed method of adding a lumped capacitance.

Based on the above conclusion, we propose in Fig.13 a modified anti-series-only network that improves significantly the linearity performances despite the presence of C_P, by providing a new degree of freedom to reach a greater range of C_A/C_B ratios, compared to only adjusting the ratio s. This is achieved by adding a lumped capacitance (C_{LIN}) in parallel with the smaller nonlinear capacitance C_A.

Next, we demonstrate through computations and simulations the linearity improvement with the addition of C_{LIN}. First, the power series $C_A(v_A)$ and $C_B(v_B)$ associated with the topology in Fig.13 is derived by adding C_{LIN} to the coefficient C_{A0} in (10), yielding (14).

$$C_A(v_A) = C_{A0} + C_{A1}\cdot v_A + C_{A2}\cdot [v_A]^2 + \cdots$$
$$C_B(v_B) = C_{B0} - C_{B1}\cdot v_B + C_{B2}\cdot [v_B]^2 + \cdots$$

With

$$C_{A0} = C_0 + C_P + C_{LIN} \quad C_{B0} = s\cdot(C_0 + C_P)$$

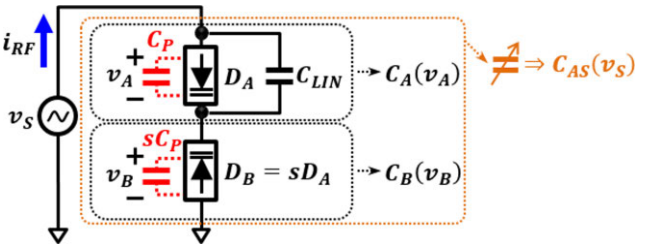


FIGURE 13. Proposed improved anti-series network. As in Fig.2, varactors are biased at V_{DC} through a high impedance network Z_C (not shown for simplification).

$$C_{A1} = C_1 \quad C_{B1} = s\cdot C_1$$
$$C_{A2} = C_2 \quad C_{B2} = s\cdot C_2 \tag{14}$$

$IMD_{2f_2-f_1}$ levels are now used to demonstrate the linearity improvement of the proposed topology in the presence of C_P compared to the well-known topology of Fig.6. The $i_{RF}IMD_{2f_2-f_1}$ levels of the circuit in Fig.13 are computed with appendix using the C_{An} and C_{Bn} coefficients given in (14) while considering the varactor parameters in Table 2, all the circuit parameters in Table 3, and a variable C_{LIN}.

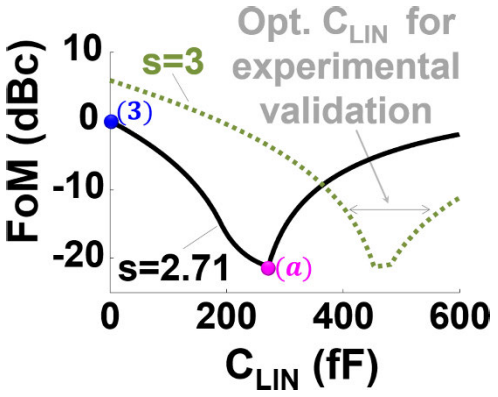


FIGURE 14. Computed *FoM* levels of the circuit in Fig.13 as a function of C_{LIN} for $s = s_{IDEAL} = 2.71$ (black curve) and for $s = 3$ (green curve). Markers *(3)* and *(a)* identify key *FoM* values.

Fig.14 plots the *FoM*, i.e. the highest $IMD_{2f_2-f_1}$ level over the full range of bias voltages, as a function of C_{LIN} for two scaling factor s : (i) for $s \approx s_{IDEAL} = 2.71$ as per Table 2 (black solid curve) and (ii) for $s = 3$ (green dashed curve). The case $s = 3$ reflects the diode ratio in the designs used for experimental implementation (section IV).

In Fig.14, all plotted *FoM* values on both curves are normalized such that the case $C_{LIN} = 0fF$ for $s = 2.71$ (marker *(3)*), which corresponds to the regular topology in Fig.6, translates into $0dBc$. Accordingly, any negative *dBc* value on these *FoM* curves represents an improvement attributed to our proposed technique over the state-of-the-art.

For the case of $s = 2.71$, the optimal value of C_{LIN} is $\sim 270fF$ (marker (a)) and corresponds to a $\sim 21dB$ improvement of the *FoM* compared to marker *(3)*. Therefore, the proposed modified network in Fig.13 brings a significant improvement of linearity in the presence of C_P.

Moreover, the case $s = 3$ in Fig.14 demonstrates that similar linearity performances to the case $s = 2.71$ may be achieved by properly adjusting C_{LIN}. Therefore, unlike in the topology in Fig.6, where linearity inevitably degrades as the value of the scaling factor differs from s_{IDEAL}, the topology proposed here offers greater flexibility on the value of s. This is of particular interest in a discrete component approach where the size ratio s is set by paralleling multiple diodes.

It is also worth mentioning that the proposed linearization technique is effective on a wide range of N_{CP} values and thus is applicable to other hyper-abrupt varactors. For instance, when the circuit in Fig.13 is implemented with the SMV2019 varactor from Skyworks^{TM} ($N_{CP} = 3.1\%$ and $S_{IDEAL} = 2.32$ due to a $M = 1.4$), the same numerical computations applied earlier yield an improvement of the FoM by $28dBc$ for $C_{LIN} = 120fF$. Similarly, with the SMV1231 varactor from Skyworks^{TM} ($N_{CP} = 23.4\%$ and $S_{IDEAL} = 3.19$ due to a $M = 5$), the same computations yield a FoM improved by $18dBc$ for $C_{LIN} = 980fF$.

B. DESENSITIZATION OF LINEARITY AGAINST EXTERNAL IMPEDANCE IN ANTI-SERIES-ONLY TOPOLOGY

It was shown in section II-B2 that linearity in an anti-series-only topology using hyper-abrupt varactors is significantly degraded when driven by a non-zero source impedance Z_L.

The complete varactor-based circuit topology proposed here circumvents this shortcoming, with key advantages over the state-of-the-art anti-series/anti-parallel topology (Fig.10) used for the same purpose. Our solution consists of cancelling all the even-order harmonics at the voltage v_{AS} (i.e. $v_{AS} = 0V$ around $2f_0$, $4f_0$, $\cdots$) with a quarter-wave shorted stub as illustrated with "$2f_0$ trap" in Fig.15. This circumvents the linearity degradation due to the well-known secondary mixing mechanism caused by a non-zero Z_L (section II-B2), when voltage exists at even-order harmonics.

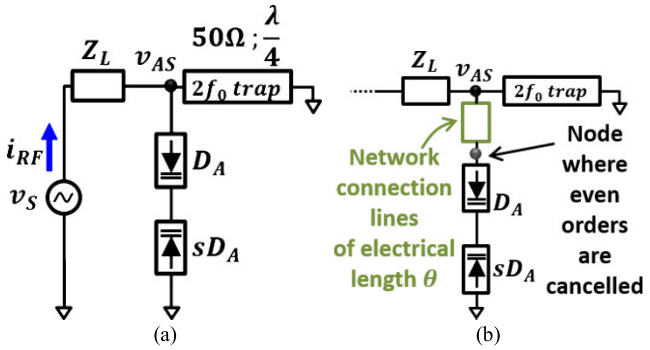


FIGURE 15. a) Anti-series topology including an even-order filter trap. b) Possible design optimization that allows mitigating the effect of series parasitics for better overall circuit linearity performances.

Our proposed technique has two benefits over the anti-series/anti-parallel topology. (i) It reduces the number of varactors by a factor of two and (ii) whereas in the anti-series/anti-parallel topology the linearity is inevitably degraded due to series-parasitics in the network connection lines (Fig.10 in sections II-B2), our technique circumvents this problem. Fig.15b illustrates the underlying concept where the cancellation of even-order harmonics takes place at the node connected to the varactor. This is made possible by adjusting the dimensions of the transmission line-based filter ("$2f_0$ *trap*") to account for the electrical length θ of the network connection lines and the loading effects of Z_L, thereby allowing to force $v_{2f_0} \approx 0V$ at this node.

IV. EXPERIMENTAL IMPLEMENTATION AND RESULTS

This section presents results from experimental measurements i) validating the improved linearity of the proposed anti-series topology in section III-A when benchmarked against a topology that does not use the proposed technique and ii) validating the complete varactor-based circuit topology proposed here, which makes use of an even-order harmonic trap.

A. DESCRIPTION OF FABRICATED CIRCUITS

This subsection describes the circuits fabricated for the linearity characterization of the anti-series-only topologies.

In the previous sections, the linearity is analyzed based on the currents i_{RF} (Fig.3). Given the difficulty of measuring i_{RF}, the distortions are accurately measured here using a hybrid coupler.

In part 1) of this subsection, the fabricated anti-series topologies are detailed. Then the devices under test (*DUTs*), each one comprising an anti-series network and a hybrid coupler, are described in part 2).

1) FABBRICATED ANTI-SERIES TOPOLOGIES

To demonstrate the linearity improvement of the proposed anti-series topology that includes C_{LIN} (referred to as $C_{AS\ NEW}$), it is benchmarked against an identical topology, but *without* C_{LIN} (referred to as $C_{AS\ REF}$). $C_{AS\ REF}$ and $C_{AS\ NEW}$ are designed with the following features and their schematics and photos are presented in Fig.16a, Fig. 16c and Fig. 16b, Fig. 16d respectively.

(iv) All varactor used are MA46H120 [19] (marker *(5)*).

(v) A 6:2 discrete varactor configuration is used so that the impedance tuning range meets the requirement in our application (Fig.1). At the same time it corresponds to a diode-size ratio (i.e. $s = 3$) in the vicinity of $s_{IDEAL} \approx 2.71$, as dictated by the choice of varactor and according to (9) and Table 2.

(vi) Unlike in other works that use twice the number of varactors (Fig.2b) to cancel even-order voltage harmonics, here we use our proposed technique (section III-B) with quarter-wave $2f_0$ *traps* (marker *(4)*).

(vii) The DC feed network (Z_C) is a line-up of a $100k\Omega$, a $22M\Omega$, and a $200M\Omega$ resistors (markers *(1)*, *(2)* and *(3)*). Moreover, the ground plane is slotted below the Z_C network to minimize the shunt capacitive parasitics.

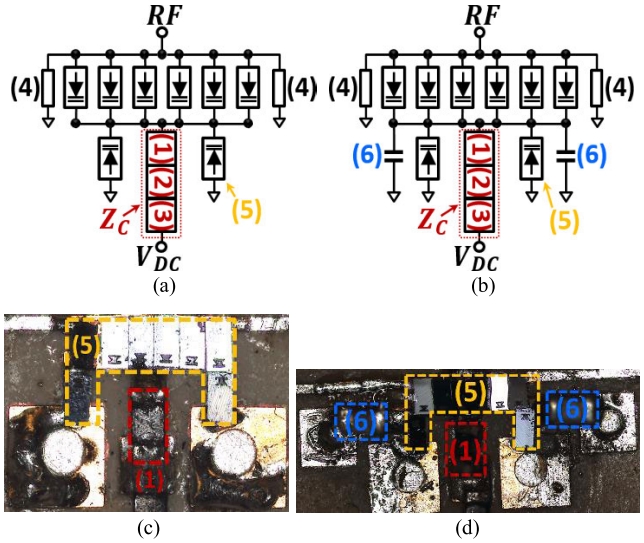


FIGURE 16. a) Schematic of $C_{AS\ REF}$ b) Schematic of $C_{AS\ NEW}$ c) photo of the fabricated network $C_{AS\ REF}$ showing a close-up of the diodes d) photo of the fabricated network $C_{AS\ NEW}$ showing a close-up of the diodes. Components: (1) 100kΩ 0402 resistor (2) 20MΩ 0402 resistor (3) 200MΩ 0805 resistor (4)∼100Ω; λ/4 transmission line (5) MA46H120 varactor model from MACOM [19] (6) C_{LIN} 0402 capacitance.

(viii) The linearity improvement technique proposed in section III-A is implemented in $C_{AS\ NEW}$ with lumped capacitances C_{LIN} (marker *(6)*). The two identical C_{LIN} account for the ratio of 6 : 2(*i.e.*2 × 3.1) such that a comparison may be drawn between the experimental linearity performances and the computed results presented in Fig.14.

2) FABRICATED DUTS

Fig.17a presents the schematic of the *DUTs* used to measure the linearity performances of $C_{AS\ REF}$ and $C_{AS\ NEW}$. In this network, the 50Ω−90° hybrid coupler equally divides the incoming RF power (red arrows) towards two identical anti-series topologies (C_{AS}), both of them implemented as $C_{AS\ REF}$ in one distinct *DUT*, and as $C_{AS\ NEW}$ in another distinct *DUT*. The distortions in the reflected signals (blue arrows) measured at the RF_{OUT} port are generated strictly by C_{AS}.

$C_{AS\ REF}$ and $C_{AS\ NEW}$ are implemented on the same 10mils CLTE ($\varepsilon_r = 2.98$) substrate. $C_{AS\ REF}$ implemented in DUT_{REF} (Fig.17b) serves as the reference linearity performance from the state-of-the-art, and $C_{AS\ NEW}$ implemented in DUT_{NEW} (Fig.17c) demonstrates the linearity improvement brought by the technique proposed here.

B. EXPERIMENTAL RESULTS

The linearity performances of DUT_{REF} and DUT_{NEW} are evaluated using two metrics. (i) $IMD_{2f_2-f_1}$ levels with a 2 equal-tone RF signal at frequencies $f_0 \pm f_{ENV}$ (Table 3) and (ii) Adjacent Channel Power Ratio (ACPR) levels with a 10 *MHz* 16 *QAM* RF signal centered at f_0 (Table 3) and a raised-cosine filter using a roll-off factor of 0.22.

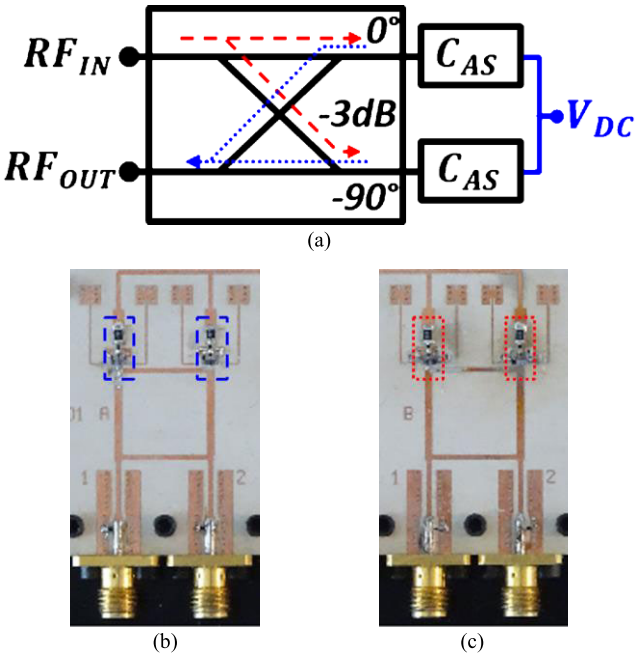


FIGURE 17. a) Schematic of the DUT b) Photo of the fabricated network DUT_{REF} where the blue line identifies C_{ASREF} c) Photo of the fabricated network DUT_{NEW} where the red line identifies C_{ASNEW}.

TABLE 4. Summary of key measurement results.

	$IMD_{2f_2-f_1}$ @ P_{OUT} =10dBm	$IMD_{2f_2-f_1}$ @ P_{OUT} =18dBm	ACPR @ P_{OUT} =18dBm	Demonstrated bandwidth
FoM with linearization technique (C_{LIN})	-62.2dBc	-47.3dBc	-56.2dBc	1kHz to 120MHz
FoM without C_{LIN}	-51.6dBc	-53.9dBc	-52.3dBc	N/A
Improvement	10.6dB	6.6dB	3.9dB	N/A

Results from these measurements are discussed in part 1) and part 2) and key results demonstrating improved linearity by the proposed topology are summarized in Table 4.

It is worth mentioning that VNA-based S-parameters measurements show that $S_{11} < -15dB$ and that $S_{21} < 1.2dB$ for both *DUTs*, over a large bandwidth, and for any bias voltage. This demonstrates that the mismatch and transmission losses are maintained very low, thereby guarantying an accurate measurement of the anti-series networks linearity based on the signals coupled to the RF_{OUT} port.

1) $IMD_{2f_2-f_1}$ LEVELS

The measured $IMD_{2f_2-f_1}$ levels at an output power (P_{OUT}) of 10*dBm* and at $P_{OUT} = 18dBm$ are shown in Fig.18a and Fig.18b respectively. In Fig.18, the blue curves correspond to DUT_{REF} and the black curves correspond to DUT_{NEW}. Also, to avoid any uncertainty, all levels lying below the minimum measurable level (light gray curve) are set equal to −75*dBc*.

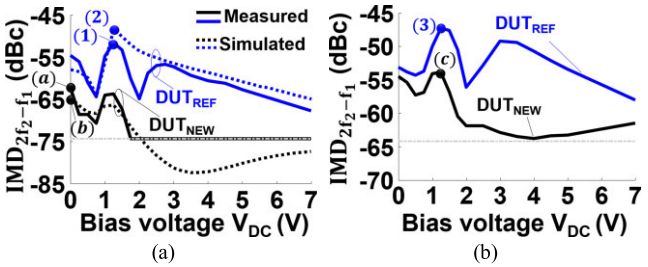


FIGURE 18. Simulated and measured $IMD_{2f_2-f_1}$ levels for DUT_{REF} (Fig.16a and Fig. 17b) and DUT_{NEW} (Fig.16b and Fig. 17c) for a tone spacing of 10MHz, a) at $P_{OUT} = 10dBm$ and b) at $P_{OUT} = 18dBm$. The light gray line identifies the minimum measurable level with the test setup.

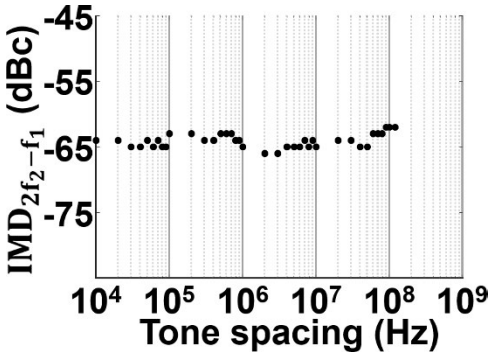


FIGURE 19. Measured $IMD_{2f_2-f_1}$ levels vs the tone spacing for DUT_{NEW} (Fig.16b and Fig. 17c) at $P_{OUT} = 10dBm$ and $V_{DC} = 1V$.

Using the same FoM as for the computations and simulations (section III), i.e. the worst-case $IMD_{2f_2-f_1}$ level over the full range of bias voltages, DUT_{NEW} demonstrates an improvement by 10.6dB at $P_{OUT} = 10dBm$ (difference between markers *(1)* and (a)) and an improvement of 6.6dB at $P_{OUT} = 18dBm$ (difference between markers *(3)* and (c)).

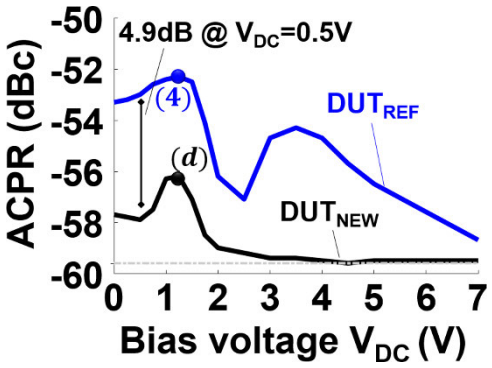
These levels for DUT_{NEW} were obtained for an experimentally optimized value of $C_{LIN} = 500fF$, which is in agreement with the range "Opt. C_{LIN}" identified in Fig.14. Moreover, the dashed curves in Fig.18a result from harmonic balance simulations performed in ADS^{TM} at $P_{OUT} = 10dBm$ with the same 2-tone RF signal using the nonlinear model (Fig.5) of the varactor MA46H120 implemented in the same two DUT designs, including electromagnetic simulations performed in Momentum^{TM} for the modelling of passive structures, i.e. the hybrid coupler, the transmission lines, and the components pads. Linearity optimization by simulation is reached with $C_{LIN} = 450fF$. Such excellent correlations between theory, simulations and measurements validate that the linearity improvements observed in Fig.18 are attributed to the proposed linearity improvement technique (section III-A) and also validate the proposed even-order cancellation technique (section III-B).

Fig.19 presents $IMD_{2f_2-f_1}$ levels over a tone spacing ranging from 1kHz to 120MHz, measured on DUT_{NEW} at $P_{OUT} = 10dBm$ and for $V_{DC} = 1V$. The absence of linearity degradation over the full tone spacing range demonstrates: i) that the DC feed network Z_C does not degrade linearity performances at a tone spacing as low as 1kHz and ii) that the proposed distortion-cancellation technique in the presence of L-C parasitics with the use of C_{LIN}, as well as the proposed "$2f_0$ trap" as an alternative to the anti-series/anti-parallel topology, are both effective at a tone spacing as wide as 120MHz.

2) ACPR LEVELS

Fig.20a plots the ACPR levels measured at $P_{OUT} = 18dBm$ where the blue and black curves correspond to DUT_{REF} and DUT_{NEW} respectively. Using the same FoM, $C_{AS\ NEW}$ demonstrates an improvement of the FoM by 3.9dB (difference between markers *(4)* and (d)).

Fig.20b is a screenshot of an ACPR measurement example for $V_{DC} = 0.5V$, where the yellow power spectrum



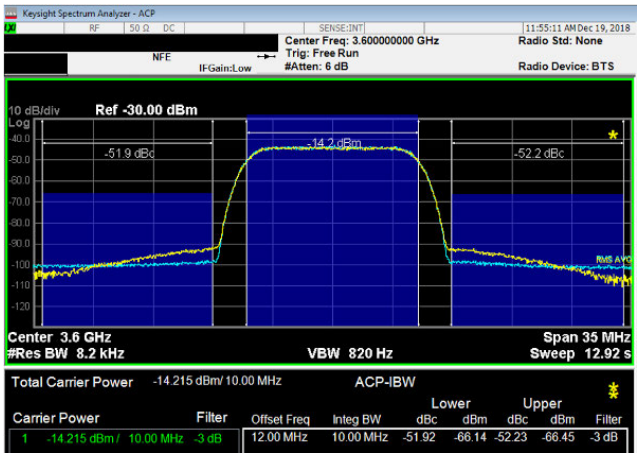


FIGURE 20. a) Measured ACPR levels for DUT_{REF} (Fig.16a and Fig. 17b) and DUT_{NEW} (Fig.16b and Fig. 17c) at $P_{OUT} = 18dBm$. The light gray line identify the minimum measurable level. b) Screenshot of measured output spectrums at $V_{DC} = 0.5V$ where the yellow and blue curves correspond to DUT_{REF} and DUT_{NEW} respectively. The signal is attenuated for equipment protection explaining that the power being shown is lower than 18dBm.

corresponds to DUT_{REF} and the blue spectrum corresponds to DUT_{NEW}. In Fig.20b, the displayed values $-51.9dBc$ and $-52.2dBc$ are related to DUT_{REF} and the blue curve represent an ACPR improvement by ~7dB, which is comparable to the ~5dB improvement identified in Fig.20a at $V_{DC} = 0.5V$.

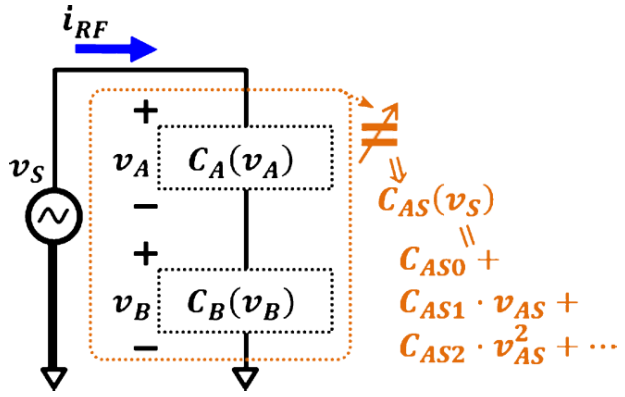


FIGURE 21. A generic anti-series topology showing all network's elements on the form of a power series for calculation purposes.

To the best of our knowledge, ACPR measurements have never been performed on hyper-abrupt anti-series topologies. This is relevant since it is difficult to comply with the condition $Z_C \gg Z_{D_A}$ (refer to Fig.2) for the content at low frequencies in such modulation schemes. It is thus interesting that (i) the high resistance Z_C network does not degrade significantly the linearity with such a modulation scheme and (ii) that the proposed anti-series topology combined with the proposed even-order cancellation technique improves performances with such complex modulated signals.

V. CONCLUSION

This paper studies the linearity performances of hyper-abrupt varactor-based anti-series-only topologies by focusing on the effect of the parasitics surrounding the varactors. First, the mechanisms causing linearity degradation due to the presence of parallel capacitance (C_P) and series inductance (L_S) parasitics – an aspect that to the best of the authors' knowledge has never been addressed in the literature – are demonstrated analytically using a multi-tone excitation. It is shown that this degradation may not be avoided simply by adjusting the diode size ratio. Based on these analyses, this paper proposes an improved anti-series-only network compensating the linearity degradation due to these parasitics, thereby significantly improving linearity performances compared to the state-of-the-art. Furthermore, the complete varactor-based topology introduced in this paper reduces the number of diodes by a factor of 2 compared to prior work by proposing an even-order harmonic filter, and is an attractive alternative to the well-known anti-series/anti-parallel topology. The proposed topology improves the $IMD_{2f_2-f_1}$ levels by 10.6dB and 6.6dB at output power levels of 10dBm and 18dBm respectively and also improves ACPR levels by 3.9dB in response to a 16QAM modulated signal at an output power level of 18dBm. The large signal linearity performances demonstrated at 3.6GHz in this paper constitute a significant improvement over the state-of-the-art. This is especially important for designs using discrete components, where parasitics are more predominant than in a MMIC approach. Although not shown here, simulations and experimental validations show that these results have only minimal impact on the tuning range of the reactance, hence the proposed techniques are suitable for applications such as Fig.1.

APPENDIX
CALCULATION OF THE NONLINEAR COEFFICENTS OF ANTI-SERIES TOPOLOGIES

This appendix gives the details to derive the coefficients $C_{ASn} = C_{AS0}, C_{AS1}, C_{AS2}$ of the nonlinear capacitance $C_{AS}(v_S)$ in power series (8) and (11) and to compute the coefficients in the power series (13) and (14). Equation (8) defines the intrinsic nonlinear behavior of the parasitic-free anti-series-only varactor topology in Fig.4. Equation (11) also defines the nonlinear behavior of the anti-series-only varactor topology, but this time including parallel parasitic capacitances C_P as shown in Fig.6. Equations (13) and (14) define the power series associated to the anti-series network using a dual bias scheme (Fig.11) and the improved anti-series network including C_{LIN} (Fig.13) respectively.

$$\begin{aligned} C_A(v_A) &= C_{A0} + C_{A1} \cdot v_A + C_{A2} \cdot [v_A]^2 + \cdots \\ C_B(v_B) &= C_{B0} + C_{B1} \cdot v_B + C_{B2} \cdot [v_B]^2 + \cdots \end{aligned} \quad \text{(A1)}$$

Reference [3] demonstrates the series-combination of $C_A(v_A)$ and $C_B(v_B)$ in Fig.21, resulting in (A2) and is repeated here for convenience, consistent with the terminology in the formulations of this paper. Equation (A2) includes the C_{ASn} coefficients of power series $C_{AS}(v_S)$ (in orange in Fig.21).

$$\begin{aligned} C_{AS}(v_S) &= C_{AS0} + C_{AS1} \cdot v_S + C_{AS2} \cdot [v_S]^2 + \cdots \\ C_{AS0} &= \frac{1}{P_0} \quad C_{AS1} = -\frac{2P_1}{P_0^3} \\ C_{AS2} &= \frac{3}{P_0^5} \cdot \left(2 \cdot P_1^2 - P_0 \cdot P_2\right) \end{aligned}$$

where

$$\begin{aligned} P_0 &= \frac{1}{C_{A0}} + \frac{1}{C_{B0}} \quad P_1 = -\frac{C_{A1}}{2 \cdot [C_{A0}]^3} + \frac{C_{B1}}{2 \cdot [C_{B0}]^3} \\ P_2 &= \frac{\frac{[C_{A1}]^2}{2} - \frac{C_{A0} \cdot C_{A2}}{3}}{[C_{A0}]^5} + \frac{\frac{[C_{B1}]^2}{2} - \frac{C_{B0} \cdot C_{B2}}{3}}{[C_{B0}]^5} \end{aligned} \quad \text{(A2)}$$

In (A2), the coefficients $C_{ASn} = C_{AS0}, C_{AS1}, C_{AS2}$ of power series $C_{AS}(v_S)$ are function of the terms P_0, P_1, and P_2, which themselves are function of coefficients C_{An} and C_{Bn} in (A1).

In this work, hyper-abrupt varactors ($M > 1$) and unmatched varactors ($s > 1$) including parasitics are considered. Accordingly, the C_{ASn} coefficients defining $C_{AS}(v_S)$ here are obtained simply through the substitution of C_{An} and C_{Bn} in (A2) by the appropriate capacitance terms.

For the cases of the parasitic-free anti-series varactor topology (section II-A4) and of the anti-series varactor topology including C_P (section II-B1), C_{A0}, C_{A1}, C_{A2} and C_{B0}, C_{B1}, C_{B2} are substituted as in (7) and (10) respectively.

For the cases of the dual biased scheme anti-series network and of the improved anti-series network including C_{LIN} (section III-A), C_{A0}, C_{A1}, C_{A2} and C_{B0}, C_{B1}, C_{B2} are substituted as in (13) and (14) respectively.

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