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UNIVERSITÉ DE MONTRÉAL

CMOS LOW VOLTAGE PREAMPLIFIER BASED ON 1/F NOISE CANCELLATION

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ÉCOLE POLYTECHNIQUE DE MONTRÉAL

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Ce mémoire intitulé :

CMOS LOW VOLTAGE PREAMPLIFIER BASED ON 1/F NOISE CANCELLATION

présenté par : YAMU HU

en vue de l'obtention du diplôme de : Maîtrise ès sciences appliquées

a été dûment accepté par le jury d'examen constitué de :

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M. MARCEL LAPOINTE,	Ph.D., membre

DEDICATE

To all my friends

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First, I would like to thank my advisor, Professor Mahamad Sawan, for his patient guidance and support during my stay at École Polytechnique de Montréal. In addition to providing guidance in microelectronic system design, he also provided help in technical writing and presentation style, and I found this guidance extremely valuable for me.

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RÉSUMÉ

L'utilisation des préamplificateurs analogiques de haute performance devient de plus de plus incontournable avec l'évolution rapide de la microélectronique. Celle-ci est due au fait que les préamplificateurs définissent le niveau minimum de signal pouvant être traité. Dans les applications à basse fréquence telles que les applications biomédicales, le facteur limite est le bruit 1/f et le décalage continue ou DC du circuit d'amplification. La décroissance rapide de la taille minimale des transistors en technologie CMOS, impose une contrainte additionnelle sévère à la conception des circuits analogiques de haute performance.

L'objectif principal de ce mémoire est la conception en technologie CMOS d'un préamplificateur possédant une bonne performance de bruit 1/f avec un niveau faible de la tension de décalage. Le circuit proposé est en mesure de fonctionner à basse alimentation puisqu'elle est destinée aux applications biomédicales.

Une analyse de la source de bruit aux basses fréquences en technologie CMOS a été effectuée. La technique de « CHopper Stabilisation (CHS) », qui est une méthode fréquemment utilisée pour réduire à la fois le bruit à basse fréquence ainsi que la tension de décalage, a été étudiée tant au niveau théorique qu'au niveau implementation VLSI. Le circuit de préamplification proposé fonctionne avec une alimentation de 1.8 V tout en présentant une large bande dynamique (0 à 1.8 V) et a été fabriqué dans un procédé

CMOS 0.35µm. Il est composé d'un circuit d'appariement d'horloge, d'un filtre passe-bas continu d'ordre 4 et d'un amplificateur d'instrumentation. Le gain DC de l'amplification est de 51 dB avec une bande passante de 4.5 kHz. Le bruit équivalent d'entrée est de l'ordre de 45 nV / $\sqrt{Hz}$. Le circuit occupe une surface approximative 1150×450 μm^2 et dissipe seulement 775 µW en simulation. Bien que le circuit a été originalement conçu pour les applications biomédicales, sa versatilité fait qu'il peut être utilisé dans des applications nécessitant la mesure de signaux basses fréquences de très faible amplitude.

ABSTRACT

Nowadays, with the ongoing development of microelectronics, high performance analog preamplifier plays a critical role in mixed-signal analog-digital interfaces. It often limits the minimum signal level that can be processed. For the low-frequency applications, such as implantable devices in biomedicine that require to monitor several neuromuscular activities, the main factors that limit the signal dynamic range are the flicker noise and the DC offset of the preamplifier. In addition, the ongoing downscaling of the CMOS technology introduces more difficulty on designing high performance analog circuits.

The aim of this master thesis is to design a CMOS preamplifier without being limited by its inherent flicker noise and DC offset, which allows handling smaller signals. Furthermore, apart from low-noise and low-offset, the circuit should work under a low-voltage supply since it is designed for an implantable stimulate application.

This thesis examines the noise sources and means to minimize their impact in CMOS technology used at low frequency. An emphasis is placed on providing noise minimizing solutions. Chopper Stabilization technique (CHS) is used to realize low-noise and low-offset. This thesis deals both with theoretical analysis and circuit implementations. The proposed circuit works under low power supply (1.8V), and has a wide common mode input range (0-1.8V). It features a 51dB gain with a bandwidth of 4.5 KHz. The equivalent input noise is about 45 $nV/\sqrt{Hz}$. The proposed preamplifier includes a

matching clock generator, a 4^{th} order continuous time low-pass filter and an instrumentation amplifier, and it has been implemented in a 0.35μm n-well CMOS process with an active die area of 1150×450 μm^2. The total data acquisition device consumes only 775 μW in simulation. Although the analog front-end preamplifier was originally designed for biomedical applications, it can be used for any low frequency application to monitor ultra low-amplitude signals.

CONDENSÉ EN FRANÇAIS

I. INTRODUCTION

Pour les applications de mesure de signaux, le bruit intrinsèque du système limite souvent la plage du signal d'entrée. Il existe deux sortes de sources de bruit dans un circuit MOS.

1. Le bruit thermique

Le bruit thermique dans un transistor MOS résulte du mouvement aléatoire des électrons. La densité du bruit peut être représentée par $N_{tw} = 4kT/gm$, qui est du bruit blanc.

2. Le bruit 1/f

Bien que l'origine de ce bruit est partiellement inconnue, il est possible de l'identifier par sa densité spectrale qui est inversement proportionnelle à la fréquence, comme le montre l'équation.

$$N_{1/f}(f) = \frac{K}{f^{\gamma}} \qquad \text{où, } 0.7 < \gamma < 1.3$$

Comme le bruit en 1/f est plus élevé que le bruit thermique à basse fréquence, le bruit en 1/f est particulièrement important dans les circuits MOS. La figure 1 illustre la densité spectrale de bruit typique d'un transistor MOS en fonction de la fréquence. Le bruit

thermique et le bruit en 1/f se croisent à la fréquence fa, qui est appelée fréquence de coin (corner frequency).

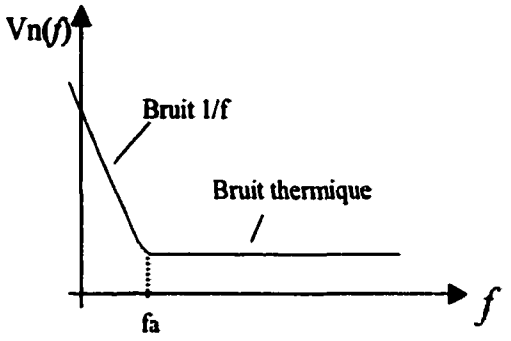


Figure 1. Densité spectrale de bruit typique d'un transistor MOS

Plusieurs applications nécessitent le traitement des signaux à basse amplitude tels que les dispositifs électroniques implantables dédiés à des applications biomédicales afin de coordonner les nombreuses activités neuromusculaires [1][2][3]. Parmi ces dispositifs, on retrouve le contrôleur de la vessie, dédié à la mesure du volume urinaire et à l'évacuation de l'urine par la stimulation électrique via des électrodes [1]. Le système implantable correspondant se compose par conséquent de trois parties principales, tel que présenté sur la figure 2: un processeur central (CP), un module de mesure du volume urinaire « Volume Monitoring Device (VMD) » et un micro-stimulateur.

Le module VMD prélève le signal nerveux qui contient l'information sur le volume de la vessie. Le schéma fonctionnel du VMD est illustré sur la figure 3. L'amplitude du signal nerveux V_n est généralement très basse, de l'ordre 1 à 10 μV [2][3], et souvent submergée par le bruit dans un amplificateur opérationnel conventionnel CMOS à deux

étages. Par conséquent, le signal doit être faiblement amplifié, tout d'abord par un amplificateur à faible bruit (LNA), afin de limiter le bruit 1/f et d'augmenter le niveau du signal au-dessus de celui du bruit de l'amplificateur d'instrumentation (AI). La sortie de l'AI est alors convertie en signal numérique et envoyée au bloc traitant le signal numérique.

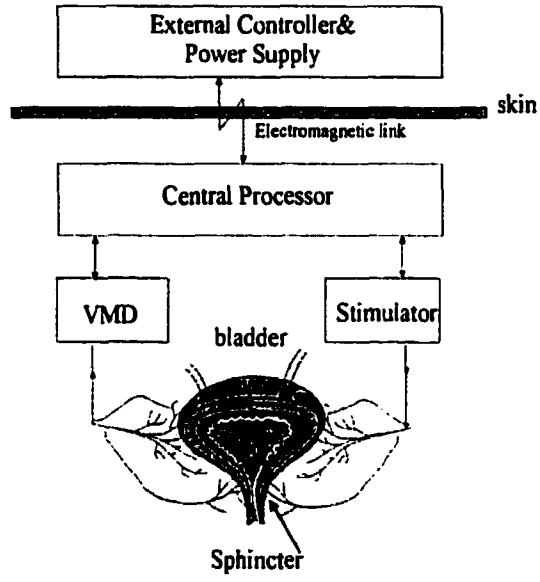


Figure 2. Schéma bloc simplifié du system globale dédié à la régulation de la vessie.

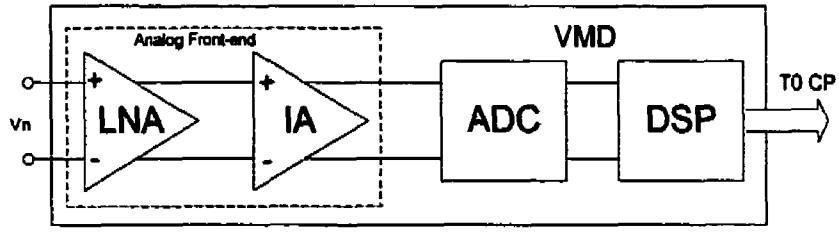


Figure 3. Schéma bloc du module VMD

La source dominante de bruit dans les applications de systèmes électroniques implantables est le bruit 1/f de l'étage différentiel d'entrée. La technologie récente utilisé

pour les masque et l'emploi de longueurs de transistors réduites associée à la réduction d'échelle tend généralement à augmenter le niveau du bruit 1/f [11]-[14]. Le bruit peut être réduit par un certain nombre de méthodes [4]-[10]. La technique de « CHopper Stabilisation (CHS) » est une méthode fréquemment utilisée pour réduire à la fois le bruit à basse fréquence ainsi que la tension de décalage due au "mismatch".

II. CARACTÉRISTIQUES DE LA TECHNIQUE DE STABILISATION CHOPPER

Cette dernière méthode tire profit d'une technique de modulation qui n'augmente pas le bruit à large bande ni le bruit blanc à bande de base. Ainsi le CHS est une méthode très pertinente pour le traitement des signaux en temps réel, tel que la surveillance des activités neuromusculaires dans les applications biomédicales.

Le principe de base du CHS est présenté à la figure 4. Le signal d'entrée $V_{in}(t)$ est modulé par un signal d'une onde carrée $m_1(t)$ à une fréquence f_{chop}. Après cette modulation, le spectre du signal d'entrée (V_{in}) est transposé aux fréquences des harmoniques impaires du signal $m_1(t)$. Il est alors amplifié par un amplificateur sélectif (SA) et démodulé par le signal $m_2(t)$, et cela transpose de nouveau le signal $m_1(t)$ à la bande initiale. Si le spectre du signal d'entrée est limité à la moitié de la fréquence de chopper, aucun chevauchement de signal ne se produira.

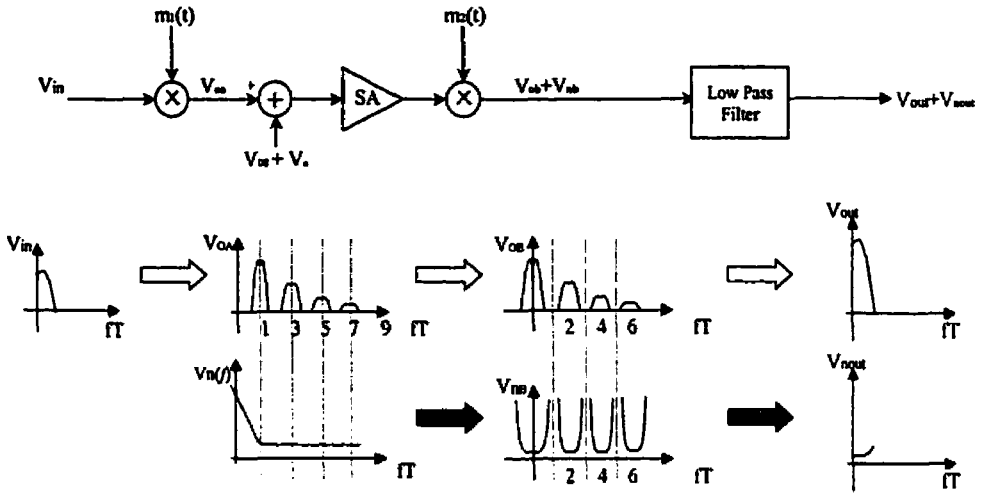


Figure 4. Principe de la technique CHS

Le bruit à basse fréquence ainsi que le décalage de tension de l'amplificateur (représentée par V_n et V_{os} respectivement sur la figure 4) sont modulés une première fois par le démodulateur et leurs spectres se retrouvent aux harmoniques impaires, laissant par le fait même le bruit blanc dans la bande de base. Après démodulation (soit une deuxième modulation), le signal est filtré passe-bas à la moitié de la fréquence de chopper. Ainsi, les signaux et le bruit à contenu fréquentiel élevé seront éliminés.

Quelques études sur la technique CHS ont été publiés récemment [4][5][6][7]. La partie critique du CHS est de concevoir un amplificateur sélectif optimal, qui amplifie non seulement le signal dans une bande de fréquence, mais peut également réduire le décalage résiduel (figure 5) provenant de l'horloge du modulateur d'entrée. Deux publications [5][6] ont démontré qu'un filtre passe-bande du deuxième ordre (BPF) sera un meilleur compromis entre la réduction du décalage et la complexité du circuit. Dans [5], l'effet de

la modulation CHS sur le bruit de l'amplificateur a été illustré en détail, mais le circuit utilisé était un filtre passe-bas de premier ordre au lieu d'un filtre passe-bande de second ordre, tel qu'il a été utilisé dans la pratique. Dans [6][7], les auteurs ont complété une autre étude sur le taux de rejet en mode commun (CMRR) et le décalage dans les CHS. Dans ce mémoire, plusieurs caractéristiques complémentaires et importantes du CHS sont fournis, et l'analyse du rapport de signal sur bruit (SNR) avec CHS et sans CHS est démontrée. Ceci afin de fournir un aperçu supplémentaire sur la réduction du bruit du signal par le filtre passe-bande du deuxième ordre. Les résultats ont été vérifiés par un modèle de comportement établi pour l'outil SIMULINK [28].

Le décalage résiduel

Le décalage en tension dans un amplificateur sélectif est quasi nul, car il a été décalé aux harmoniques impaires de la fréquence f_{chop}, puis filtré par le filtre passe bas (LPF). Mais les niveaux crêtes des signaux résultants du modulateur d'entrée présentent un décalage en tension résiduel après la seconde modulation, tel que présenté sur la figure 5. On démontrera que ce décalage résiduel est proportionnel au carré du taux (la constante de temps du niveau crête sur la période T du signal modulé), si un filtre passe-bande de deuxième ordre est choisi comme amplificateur sélectif. La constante de temps τ est égale à RC, où R est la résistance de la source du signal d'entrée et C est la capacité parasite de l'amplificateur.

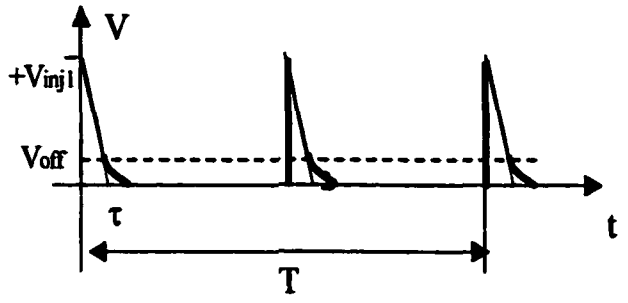


Figure 5. Le décalage résiduel

Les bruit thermique du CHS

Après que le bruit blanc soit passé par un filtre passe-bande de deuxième ordre, un bruit résultant à bande étroite est obtenu. Ceci augmente le SNR (CHS sur bruit blanc) de $16/\pi^2 = 1.62$ par rapport à un système sans CHS. Ce phénomène est dû au fait que le modulateur d'entrée présente un coefficient $k=4/\pi$ à la première harmonique qui est principalement la partie du signal restauré. Le signal augmenté améliore donc le SNR d'un taux de k^2.

III. IMPLEMENTATION DU CIRCUIT

1.Schéma bloc du circuit

Le VMD sera implanté dans le corps humain, ainsi toutes les composantes analogiques d'entrée incluant le générateur à horloge et le filtre passe bas devraient être entièrement intégrée sur une seule puce. Le schéma bloc simplifié du système est donné à la figure 6.

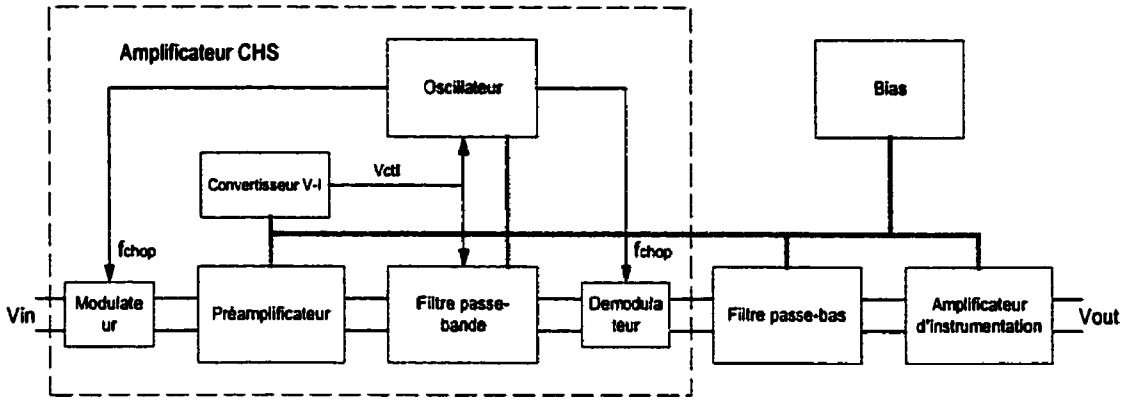


Figure 6. Schéma bloc de l'amplificateur d'entrée analogique

Dans notre application, l'amplificateur sélectif est réalisé par deux étages, un préamplificateur à large bande et faible bruit suivi d'un filtre passe-bande. Cette structure présente deux avantages: d'abord, une large gamme d'entrée en mode commun peut être réalisée en utilisant un OTA (Amplificateur Opérationnel à Transconductance) ayant une topologie rail à rail au premier étage, sans pour autant affecter la linéarité du filtre g_m-C (combinaison de cellules de transconductances et de condensateurs). En second lieu, la valeur de la transconductance d'entrée du BPF n'a pas besoin d'être très haute pour réaliser un gain DC élevé, d'où la non nécessité de compenser le décalage provenant de la paire d'entrée.

2. Le préamplificateur à faible bruit

Le préamplificateur est composé d'un OTA rail à rail suivi d'un étage à transimpédance. Le gain DC de l'amplificateur est égal au rapport de Gm1/Gm2, où Gm1 et Gm2 sont les valeurs des transconductances de l'OTA et de l'étage à transimpédance respectivement.

La largeur de bande de l'amplificateur est choisie élevée afin d'éviter qu'un faible gain ainsi qu'une distortion de la phase n'apparaisse dans le système. L'amplificateur rail à rail (plage d'entrée de 0V à VDD) à faible bruit est présenté à la figure 7. L'étage à transimpédance proposé utilise un étage à transconductance linéaire avec une rétroaction négative, tirant avantage de deux transistors en triode afin d'améliorer la linéarité.

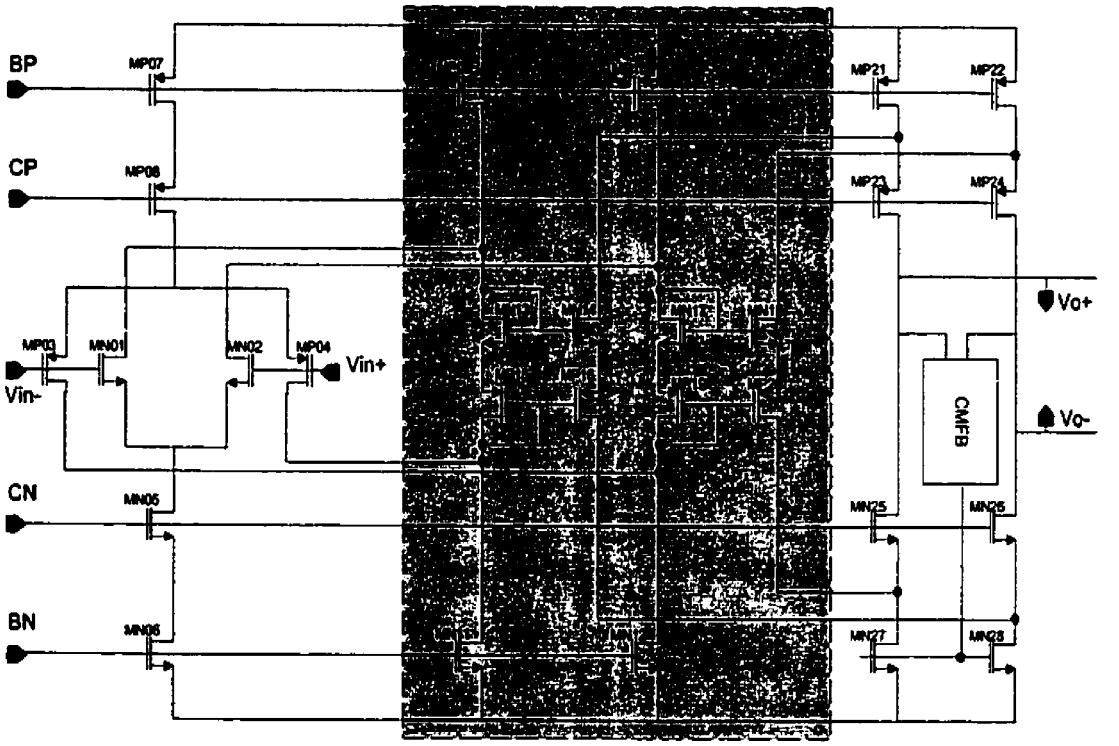


Figure 7. Schéma de l'amplificateur rail à rail

3. Le filtre passe-bande et l'oscillateur

Le deuxième étage de l'amplificateur sélectif est constitué d'un filtre Gm-C de 2ième ordre. La fréquence f_{chop} et la fréquence centrale sont doivent être égaler, et supérieures à

la fréquence de coin (corner frequency). Le facteur de qualité Q sera limité par la largeur de bande et est égal à 4. Ainsi la bande passante du signal peut aller jusqu' à 5 kHz. Le schéma bloc est présenté à la figure 8. Les cellules GM utilisent des étages à transconductance linéaire [22].

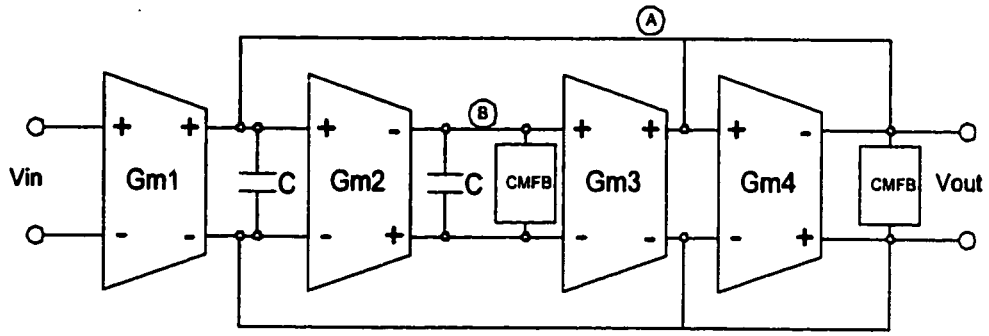


Figure 8. Schéma bloc du filtre passe-bande

En raison du manque de masses virtuelles et de nœuds à basse impédance, les filtres gm-C sont sensibles aux capacités parasites. Par conséquent, il est nécessaire d'ajouter un circuit de calibration automatique dans le filtre passe bande, pour verrouiller sa fréquence centrale f_c avec le f_{chop}. La calibration automatique des filtres continus a été analysée dans la littérature [21]-[26]. Mais pour l'amplificateur CHS, la valeur de la fluctuation du f_{chop} ne présentera pas d'impact significatif sur les performances du CHS. Donc, le point clé de la calibration dans le CHS étant de suivre la fréquence centrale du filtre, plutôt que de le fixer avec une horloge à référence. Ainsi nous pouvons utiliser un oscillateur intégré avec le filtre passe bande qui joue le rôle d'un générateur d'horloge f_{chop}. Deux structures identiques du circuit de résonance sont utilisées dans l'oscillateur et dans le filtre passe-bande. Cette structure réduira la complexité du système entier. Cela est particulièrement

important dans cette application, où l'horloge f_{chop} est générée sur la même puce. Le schéma de l'oscillateur est présenté à la figure 9.

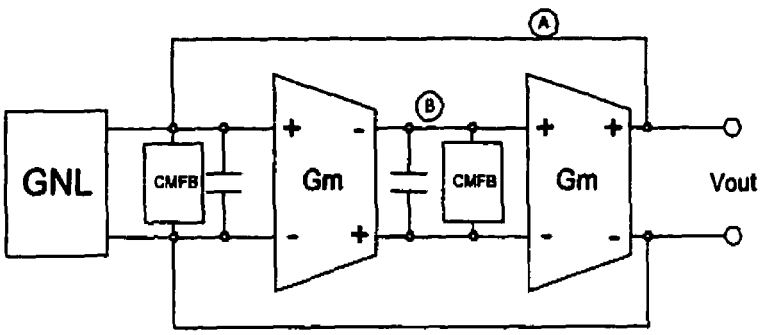
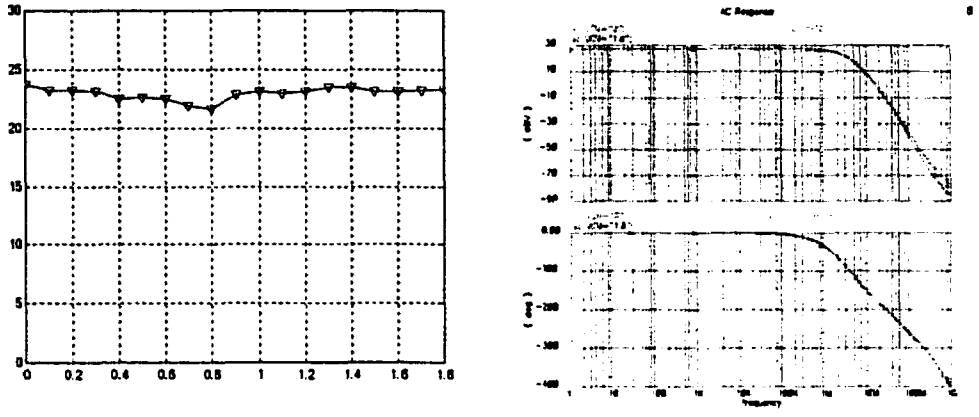


Figure 9. Schéma bloc de l'oscillateur

IV. SIMULATION ET RÉSULTATS EXPÉRIMENTAUX

Le design proposé du CHS a été implémenté et fabriqué en technologie CMOSP35 de la Société Canadienne en Microélectronique (SCM). Les résultats de mesure de l'amplificateur d'entrée rail à rail sont montrés sur la figure 10 a). La variation du Gm est inférieure à 5%, et les autres performances sont meilleurs que celle d'un OTA conventionnel rail à rail. La réponse en fréquence du préamplificateur à faible bruit est présentée sur la figure 10 b). Son gain DC est de 26 dB et la fréquence de coupure à -3dB est environ 1.2 MHz, beaucoup plus grande que le f_{chop} (47 kHz dans notre cas). La figure 11 montre le spectre du filtre passe bande. Un zéro supplémentaire apparaît en basse fréquence à cause de l'impédance de sortie finie de l'étage à transconductance. Le gain à la fréquence centrale est de 25 dB. Le gain de l'amplificateur sélectif incluant deux étages est de 51 dB. L'amplificateur d'instrumentation (AI) a été également intégré dans cette

puce. La structure de l'AI proposé par notre équipe PolySTIM a été illustrée dans [27]. L'AI permet de réaliser un taux de rejet en mode commun (CMRR) assez élevé sans calibration. Le bruit équivalent à l'entrée est de 45 nV/$\sqrt{Hz}$. La puissance consommée en simulation est de seulement 775 µW pour une alimentation de 3.3 V.



a) b)

Figure 10. Résultats de mesure de l'amplificateur d'entrée rail à rail

a) Variation du Gain b) Réponse en fréquence

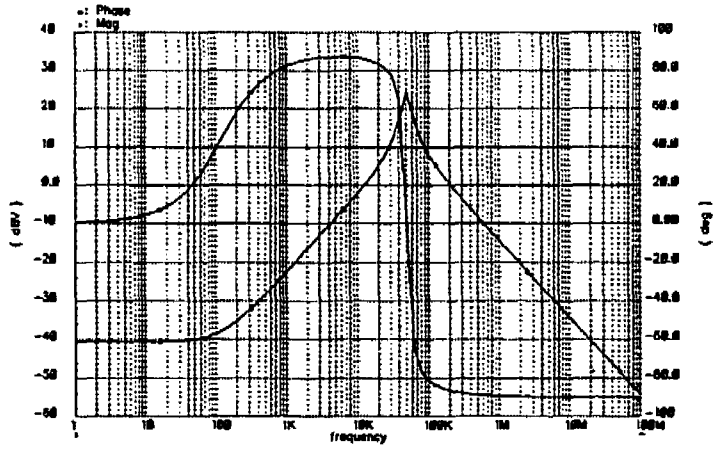


Figure 11. Simulation du filtre passe bande

V. CONCLUSION

La technique de modulation 'CHOPPER' a été choisie pour réduire le bruit à basse fréquence ainsi que l'offset au niveau de l'amplificateur opérationnel CMOS. La basse tension d'alimentation et la grande marge de tension en mode commun sont réalisées en utilisant le préamplificateur rail à rail à faible bruit au niveau du premier étage. Le système a été intégré dans la technologie CMOSP 0.35 μm. Cet amplificateur a été initialement conçu pour des applications biomédicales, toutefois il peut être employé pour des applications à basses fréquences pour traite des signaux de basse amplitude.

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LIST OF ABBREVIATIONS AND SYMBOLS

ABBREVIATIONS

ADC	Analog-to-Digital Converter
AZ	Autozero technique
BPF, BP	Band Pass Filter
CHS	Chopper Stabilization Amplifier
CMFB	Common Mode Feedback
CMOS	Complementary Metal Oxide Semiconductor
CMR	Common Mode Range
CMRR	Common Mode Rejection Ratio
CP	Central Processing
DOA	Differential Opamp
DSB	Double Sideband
DSP	Digital Signal Processing
GNL	Non Linear Transconductor
IA	Instrumentation Amplifier
IC	Integrated Circuit
LNA	Low Noise Amplifier
LPF, LP	Low Pass Filter
LTI	Linear Time Invariable
MCS	Maximum Current Select circuit

MOSFET	Metal Oxide Field Effect Transistor
NF	Noise Figure
NMOS	Channel-N Metal Oxide Semiconductor
OTA	Operational Transconductor Amplifier
PLL	Phase Lock Loop
PMOS	Channel-P Metal Oxide Semiconductor
PSD	Power Spectral Density
PSRR	Power Supply Rejection Ratio
RMS	Root Mean Square value
SA	Selective Amplifier
SNR	Signal to Noise Ratio
SOA	Single-end Opamp
SOC	System-On-Chip
VCF	Voltage Controlled Filter
VCO	Voltage Controlled Oscillator
VLSI	Very Large Scale Integration
VMD	Volume Measure Device

SYMBOLS

k	Boltzman Constant
T	Absolute temperature
μ	Channel mobility of MOSFET transistor
W	Width of MOSFET transistor
L	Length of MOSFET transistor
C_{ox}	Gate capacitance per unit area
λ	Output impedance constant of MOSFET transistor
γ	Body-effect constant of MOSFET transistor
Q	Quality Factor
i_d	Drain current of MOSFET transistor
g_m	Transconductance of MOSFET transistor
V_n	Low frequency noise voltage
V_{off}	DC offset voltage
f_{chop}	Chopper modulating frequency
f_c	Cut-off frequency
V_{eff}	Effective voltage of MOSFET transistor
V_{th}	Threshold voltage of MOSFET transistor
V_{sat}	Saturation voltage of MOSFET transistor (also named V_{eff})
V_{gs}	Gate-source voltage of MOSFET transistor
VDD	Positive supply voltage

VSS	Negative supply voltage
VCM	Common Mode voltage
r_{ds}	Drain-source resistance of MOSFET transistor

LIST OF ANNEXS

CHAPTER 1

INTRODUCTION

1.1 Motivation

With the continuous growth of microelectronic, the pervasiveness of digital circuits does not make the analog part diminish. On the contrary, it becomes a key factor for the increased pervasiveness of analog circuits in mixed signal chips. There are two main reasons for this: the need to interface the digital signal processing (DSP) part to the analog world and the need for analog-enhanced digital performance.

Advances in MOS technology in the past decades allow digital circuits to benefit more from the downscaling, however the new trends of the mixed-signal IC which include low voltage, low power, low noise, high-frequency operation and high-resolution make the analog IC designers job more difficult.

Sensors, detectors, and transducers are basic functions to the instrumentation and control fields, which translate the characteristics of the physical world into electrical signals. In recent years, new high-precision sensors and high-performance data acquisition systems have been developed. However all sensors have an offset or limiting noise level. The system designer must interface the sensor with electronic circuitry that contributes a

minimum of additional noise. To raise the signal to noise ratio (SNR), a high performance analog front-end signal conditioning stage must be designed.

Nowadays, more and more applications require an ultra low-amplitude signal measurement system, such as the implantable devices in biomedical applications intended to monitor several neuromuscular activities [1][2][3]. Among these devices, the bladder controller, dedicated to measure the volume of the urine and to stimulate via neural pathways the detrusor and sphincter muscle when necessary, is an important rehabilitation application [1]. The implantable part of the corresponding system consists of three main blocks as shown in figure 1.1: Central Processor (CP), Volume-Monitoring Device (VMD) and stimulator.

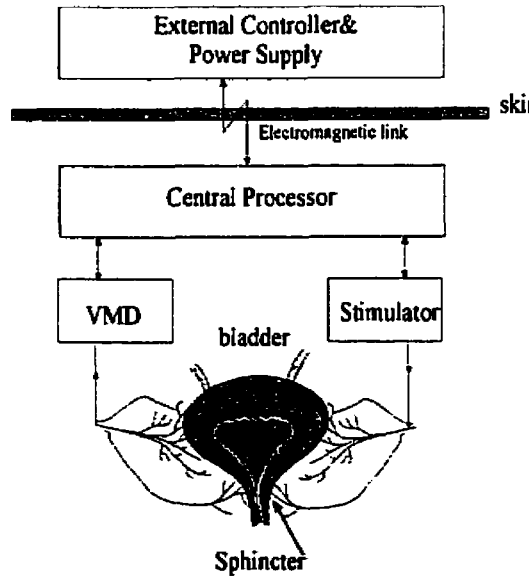


Figure 1.1 Simplified block diagram of the global system dedicated to bladder control

The VMD senses the nerve signal that contains information about volume of the bladder. The block diagram of the VMD is illustrated in figure 1.2. Nerve signal, of which the amplitude is very low and generally ranged from 1 to 10 μV [2][3], is submerged in the noise of a conventional CMOS two stages topology Opamp. Hence, the signal needs to be first weakly amplified by a Low Noise Amplifier (LNA), to overcome the 1/f noise, and to rise this signal above the noise level of the instrumentation amplifier (IA), which amplifies the signal with a programmable gain and rejects the common mode signal. The output of IA is then converted to digital signals and is sent to the Digital Signal Processing (DSP) block. At this level, the useful information is then extracted and sent to the CP block to analyze the data about the bladder volume, such as the filled volume percentage and estimation of time needed to fully filling the bladder.

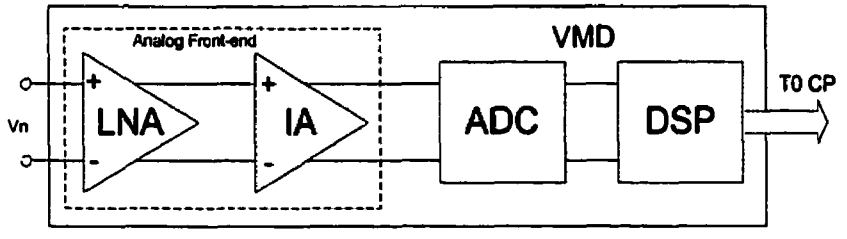


Figure 1.2 Block diagram of VMD

All functions of the implantable system must be integrated in one chip. Although it makes the analog part design more difficult, the single-chip solution offers several advantages:

- The size of the system is reduced, which is a very important characteristic in implantable system.

- The speed of operation can be increased. The analog and digital circuits do not have to communicate via off-chip interconnects, which are plagued by parasitic capacitances.
- The power dissipation is decreased.
- Other factors such as the design flexibility, the reliability and the system cost all benefit from system integration.

1.2 Research Goals

The primary aim of this master thesis is to design a low noise CMOS analog front-end amplifier, to overcome the low frequency noise and DC offset, when detecting signals on peripheral nerves. Note that it does not reduce the inherent noise of the electrodes, but it reduces the additional 1/f noise created by the circuits. Due to the special environment where the implantable system will be located, the analog front-end of the system, which includes the low-noise preamplifier and the instrumentation amplifier, must be low noise and have low DC offset. In addition, it must also meet the following characteristics:

- Low-supply voltage and low-power consumption, because the needed energy is transmitted from outside the body through the skin and should be minimized.
- High Power Supply Rejection Ratio (PSRR), since the variation of the power supply caused by the bi-directional link must not affect the stimulation operations.
- High Common Mode Rejection Ratio (CMRR) to overcome the relatively high common mode input voltage.

- Fully integrated device in a low-die-area in order to reduce the physical dimensions of the implant.

1.3 Thesis Organization

Following this chapter, chapter 2 provides an overview of the noise sources that exist in MOS amplifiers. The noise reduction techniques that include autozero (AZ) and chopper stabilization (CHS) methods will also be reviewed in chapter 2.

Chapter 3 focuses on presenting detailed characteristics and further analysis of the chopper stabilization technique. First an analysis method by virtue of a behavioral model in MATLAB/SIMULINK to simulate the chopper stabilization amplifier, will be introduced. Then the signal transfer function, signal to noise ratio (SNR), and non-ideality effects to the CHS will be further analyzed respectively and verified by the behavioral model.

In Chapter 4, low voltage requirements of the system are first examined. Then some elementary circuits which are compatible with low voltage operation are covered. Chapter 5 illustrates detailed circuit implementation of the needed blocks of a CHS amplifier, which include a modulator (demodulator), a rail-to-rail low noise preamplifier, a 2^{nd} order bandpass filter and an oscillator.

The simulation and measurement results of an experimental prototype chip are the subject of chapter 6. Some layout rules which are utilized to reduce mismatching are also discussed. Conclusions from this project and future work are presented in the last part of this thesis.

CHAPTER 2

NOISE IN CMOS INTEGRATED CIRCUITS

2.1 Introduction

Noise in integrated circuits is one of the most critical factors that determine the performance of integrated signal processing systems, such as ultra low-amplitude signal monitor, detector readout systems, transducer, AM/FM radio receivers, etc. It represents a lower limit of the electrical signal level that can be handled by an integrated circuit without significant deterioration in signal quality.

As the noise performance of any integrated system is determined by the noise characteristic of the integrated components, this chapter first presents a brief overview of the noise sources that exist in MOSFET transistors. Then the impacts of CMOS downscaling on system noise performance are discussed in the next section. The Autozero (AZ) and Chopper Stabilization (CHS) circuit techniques that reduce the low frequency noise and DC offset will be illustrated in the third section. The main previous works on two methods published by Enz (1996) and Menolfi (1997) will be briefly reviewed. The last section completes the literature review on the low noise amplifier design.

2.2 Noise sources in MOSFET transistors

Two important noise sources can be distinguished in a MOSFET transistor: the thermal noise associated with the conducting resistive channel and the flicker noise or so called 1/f noise. Other noise sources also exist in MOS transistors, such as the noise associated with the resistive poly-gate and the noise due to the distributed substrate resistance [34][43]. However for low frequency applications, it is sufficient to calculate and analyze the noise performance of circuits by considering only the thermal noise and the flicker noise. Thus the two noise mechanisms will be discussed in the following.

2.2.1 Channel Thermal Noise Mechanism

When a MOS transistor is in the "on" state, the current flowing between its drain and source is based on the existence of an inverse resistive channel between them. The inverse resistive channel is formed by the minority carriers of substrate under an appropriate gate control voltage. In analogy to a resistance, the random motion of the free carriers in the channel generates thermal noise at the device terminals. In the extreme case where there is no voltage potential difference between the drain and the source (V_{ds} = 0V), the inversed channel can be treated as a homogeneous resistance. According to the Nyquist theorem, the short circuit thermal noise current spectral density i_d is then given by [34]

$$i_d^2 = 4kTg_0 \qquad (2.1)$$

where k is the Boltzman constant, T represents the absolute temperature and g_0 denotes the channel conductance at zero drain-source voltage.

However, for analog applications, MOS transistors mostly operate in the saturation region, in which the channel can't be considered as a homogeneous resistance. In this case, the short-circuit drain current noise must be calculated by dividing the channel into a large number of small sections Δx, as shown in figure 2.1. For each section Δx, the output current noise which stem from the noise electromotive force generated in the section Δx, can be calculated separately, and finally be integrated along the whole channel to obtain the total drain current noise.

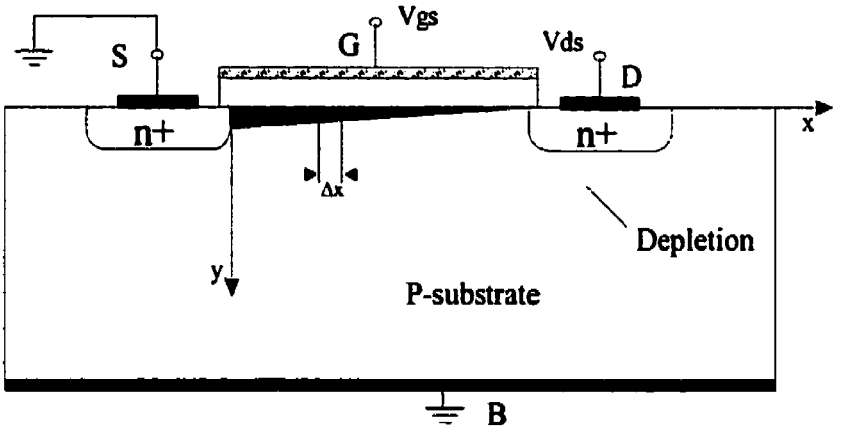


Figure 2.1 Cross section of NMOS transistor

The transistor drain current noise spectral density is derived by

$$i_d^2 = 4kT\frac{\mu^2 W^2}{L^2 I_{DS}}\int_0^{VDS} Q_n^2(V)dV = 4kT\frac{2}{3}g_m \qquad (2.2)$$

where W and L are the channel width and length respectively, μ is the effective channel mobility, I_{DS} is the drain-source current, $Q_n(x)$ represents the inversion channel charge per unit area and g_m is the transconductance of the MOSFET. Equation (2.2) predicts well the channel thermal noise behavior of MOSFET with negligible substrate effect.

2.2.2 Flicker (1/f) Noise in MOS Transistors

The 1/f noise phenomenon has been observed in almost all kinds of devices, from homogeneous metal films and different kinds of resistors to semiconductor devices and even chemical concentration cells. Among all active integrated devices, MOS transistor shows the highest 1/f noise due to its surface conduction mechanism. In spite of more than 30 years of research, the mechanisms involved in the 1/f noise of MOSFET transistor are not yet fully understood. Two main 1/f noise theoretical models exist: the carrier density or number fluctuation model (Δn model) and the mobility fluctuation model (Δμ model).

2.2.2.1 Number Fluctuation Model (Δn model)

In this model, the 1/f noise is believed to be caused by the random trapping and detrapping of the mobile carriers in the traps located at the Si-SiO_2 interface and within the gate oxide. Each trapping and detrapping event results in a Random Telegraph Signal (RTS) corresponding to a Lorentzian spectrum or generation-recombination spectrum. The superposition of a large number of such Lorentzians with a proper time constant

distribution results in the 1/f noise spectrum. The general expression for the spectrum of the drain 1/f current noise can be written by

$$i_d^2(f)_{1/f} = \frac{\mu q^2 I_{DS}}{L^2 C_{ox}} \frac{kTN_t}{\alpha f} \frac{1}{8} \ln\left[\frac{2}{2(\frac{V_{SAT}-V_{DS}}{V_{SAT}})^2 + (\frac{n_i}{n_{s0}})^2}\right] \tag{2.3}$$

where N_t is the trap density, α (=10^8 cm^{-1}) is the McWhorter tunneling constant, n_{s0} is the surface carrier concentration value at source side. In the saturation region where $V_{DS} > V_{SAT}$, equation (2.3) is reduced to

$$i_d^2(f)_{1/f} = \frac{\mu q^2 I_{DS}}{L^2 C_{ox}} \frac{kTN_t}{\alpha f} \frac{1}{16} \ln\left[\frac{\sqrt{2}n_{s0}}{n_i}\right] = \frac{K_F I_{DS}}{C_{ox} L^2 f} \tag{2.4}$$

where $K_F = \frac{\mu q^2 kTN_t}{\alpha} \frac{1}{16} \ln\left[\frac{\sqrt{2}n_{s0}}{n_i}\right]$

The transconductance of a MOS transistor in saturation is given by

$$g_m = \sqrt{2\mu C_{ox} \frac{W}{L} I_{DS}} \tag{2.5}$$

Combining (2.4) and (2.5), the equivalent input 1/f noise can be easily calculated as

$$v^2(f)_{1/f} = \frac{i_d^2(f)_{1/f}}{g_m^2} = \frac{K_F}{2\mu C_{ox}^2 WLf} = \frac{K_f}{C_{ox}^2 WLf} \tag{2.6}$$

where $K_f = K_F / 2\mu$. Note that according to equation (2.6) the flicker noise is only determined by the transistor channel area size and is independent of the DC bias condition. The expression (2.6) is widely used in 1/f noise analysis and in CMOS amplifier design.

2.2.2.2 Mobility Fluctuation Model ($\Delta\mu$ model)

In the mobility fluctuation model, the 1/f noise is assumed to be attributed to the fluctuation in mobility of free carriers when they collide with the crystal lattices. This model is described by the Hooge empirical equation [44]

$$\frac{i_{1/f}^2}{I^2} = \frac{\alpha_l}{N \cdot f} \tag{2.7}$$

where α_l is so called Hooge 1/f noise parameter, N is the total number of the free carriers in the device and I is the short circuit current through the device. Integrating over the whole channel the total 1/f noise power spectrum at saturation is obtained as [34]

$$i_{1/f}^2 = \alpha_l \frac{q\mu_f (V_{GS} - V_T) I_{DS}}{L^2 f} \tag{2.8}$$

Combining the equation (2.5) and (2.8), the equivalent input 1/f noise voltage spectrum density is then

$$v_{1/f}^2 = \frac{i_{1/f}^2}{g_m} = \alpha_l \frac{q\mu_f (V_{GS} - V_T)}{2\mu_{eff} C_{ox} WLf} \tag{2.9}$$

According to equation (2.9), the input referred 1/f noise voltage is directly proportional to the effective gate voltage V_{GS}-V_T, rather than being independent of it as in the Δn model. In this case, noise analysis and simulation is much more complex. Although the 1/f noise of the CMOSP35 technology used to implement the system is dependent on the DC bias condition, we will ignore this dependence to simplify the noise analysis.

2.2.3 Impact of scaling

The tendency to downscale the average feature size in today's CMOS, which is the leading edge technology world-wide, brings up continuous changes in the device processing and architecture. As the minimal device length is reduced by a factor K, in order to obtain a reasonable threshold voltage and to minimize short channel effects, one should modify the gate dielectric thickness and substrate doping density accordingly. This requires major technological changes, the development of new processing steps and the use of new lithographical techniques and equipment. As 1/f noise is strongly technology sensitive, the introduction of advanced processing steps may lead to observations which in many cases can hardly be predicted and/or modeled by the existing theories. But, it has been demonstrated, both theoretically and experimentally, that scaling a technology by a factor K (>1) increases the average noise level accordingly [11][12]. In addition, it has been observed that the noise dispersion (the sample-to-sample and wafer-to-wafer variation) increases significantly with scaling.

2.3 Low noise techniques

For implantable electronic system applications, the dominant noise source is often the 1/f noise component of the differential input stage. This component is directly proportional to the surface state density (N_t in equation 2.3) in the channel and inversely proportional to the gate area [10]. The 1/f noise can be reduced by a number of different methods.

- One approach is to simply make use of large input device geometries to reduce the 1/f noise associated with these devices. This approach has been widely used in the past, and works particularly well in process technologies that have a low level of surface states at the outset. For processes that have high surface state densities, however, this approach can give uneconomically large input transistor geometries for applications requiring extremely high dynamic range.

- The second approach is to use buried channel devices so as to remove the channel from the influence of surface states. This approach requires process steps which are not usually included in standard LSI technologies used to manufacture the needed circuits in high volume.

- The third approach is to make the input transistors be operated in the lateral bipolar mode that is compatible with CMOS process. The 1/f noise is strongly reduced because the minority carrier flow is pushed away from the oxide-silicon interface. But it is not well suited for high impedance requirements due to the bipolar transistor base current.

- The fourth approach is to use some special circuit techniques to reduce the 1/f noise and the offset. Popular approaches include the auto-zero technique (AZ) and the chopper stabilization technique (CHS). The latter is the main subject of this thesis.

The next section will review some details about the two circuit techniques, Autozero (AZ) technique and Chopper Stabilization (CHS) technique, to reduce the 1/f noise and DC offset. Readers are referred to [4][5][6][7] for a more comprehensive and in-depth review of the underlying concepts and related issues.

2.3.1 Autozero technique

2.3.1.1 Basic principle

The basic principle of the auto-zero technique is presented in figure 2.2. In the sampling phase ϕ_1, as illustrated in figure 2.3, the output in accordance with the noise V_n and the offset voltage V_{os} are sampled and stored. During this phase, the amplifier is disconnected from the signal path and its inputs are short-connected and set to an appropriate common-mode voltage. The sampled noise and offset value are stored by means of an analog or a digital method. Then, in the amplification phase ϕ_2, the input terminals of the amplifier are connected back to the signal source for amplification.

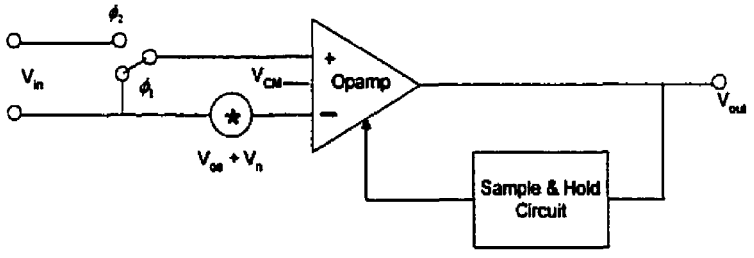


Figure 2.2 Basic principle of AZ technique

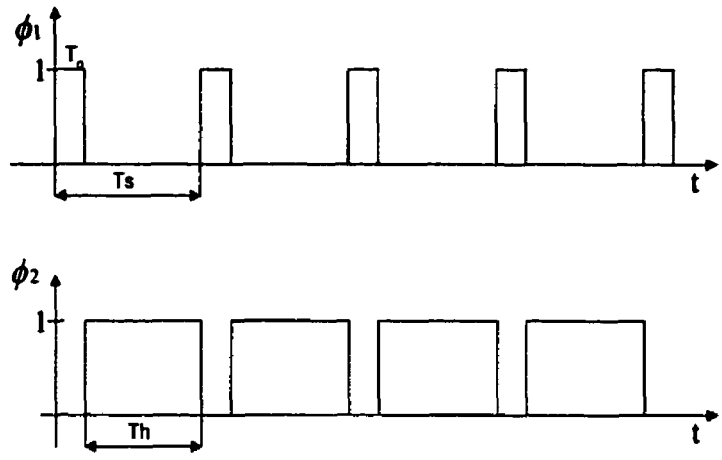


Figure 2.3 Autozero sample clocks

If the amplifier is used under the same conditions as during sampling, the instantaneous noise and DC offset can be compensated by the stored value in the sampling phase. Thus, ideally, the amplifier is free from offset. However, unlike the offset voltage, which can be considered as a constant, the amplifier's noise, and particularly its wide-band thermal noise component is time-varying and random. The efficiency of the AZ process for the low-frequency noise reduction strongly depends on the correlation between the noise sample and the instantaneous noise value from which this sample is subtracted.

2.3.1.2 The effect of AZ on the noise

Suppose the analog switch in sample-and-hold circuit is ideal (T_0=0), the sample-and-hold (S/H) process can be expressed as

$$y_s(t) = \sum_{n=-\infty}^{\infty} x(nT_s)h(t-nT_s) \qquad (2.10)$$

where y(t) and x(t) denote the output and input signals which correspond to V_{out} and V_{in} in figure 2.2 respectively, $x(nT_s)$ denotes the signal value ideally sampled at the time nT_s,

h(t) represents the hold signal which is a rectangular pulse of unit amplitude and duration T_s, defined as

$$h(t) = \begin{cases} 1 & 0 < t \le T_s \\ 0 & otherwise \end{cases} \tag{2.11}$$

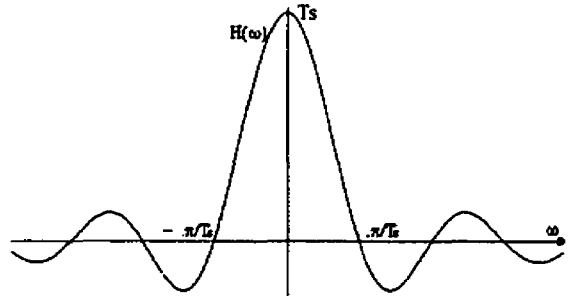
As the instantaneous sampled signal $x_s(t)$ can be written as

$$x_s(t) = x(t)\delta_{Ts}(t) = \sum_{n=-\infty}^{\infty} x(nT_s)\delta(t - nT_s) \tag{2.12}$$

According to (2.10) and (2.12), it can be derived that $y_s(t)$ is the convolution of $x_s(t)$ with the hold signal pulse *h(t)*, that is

$$y_s(t) = x_s(t) * h(t) \tag{2.13}$$

a)



b)

Figure 2.4 a) Hold phase signal and b) its spectrum

In the frequency domain, by using Fourier transform, we obtain

$$Y_s(\omega) = X_s(\omega)H(\omega) = \frac{1}{T_s}\sum_{n=-\infty}^{\infty} X(\omega - n\omega_s)H(\omega) \qquad (2.14)$$

where the spectrum $|H(\omega)| = T_s \frac{\sin(\omega T_s)}{\omega T_s}$ (2.15)

The signal h(t) and its spectrum are shown in figure 2.4. Note that the sampling-and-hold process is equivalent to passing an ideal sampled signal through a filter having the frequency response $G(\omega) = H(\omega)$.

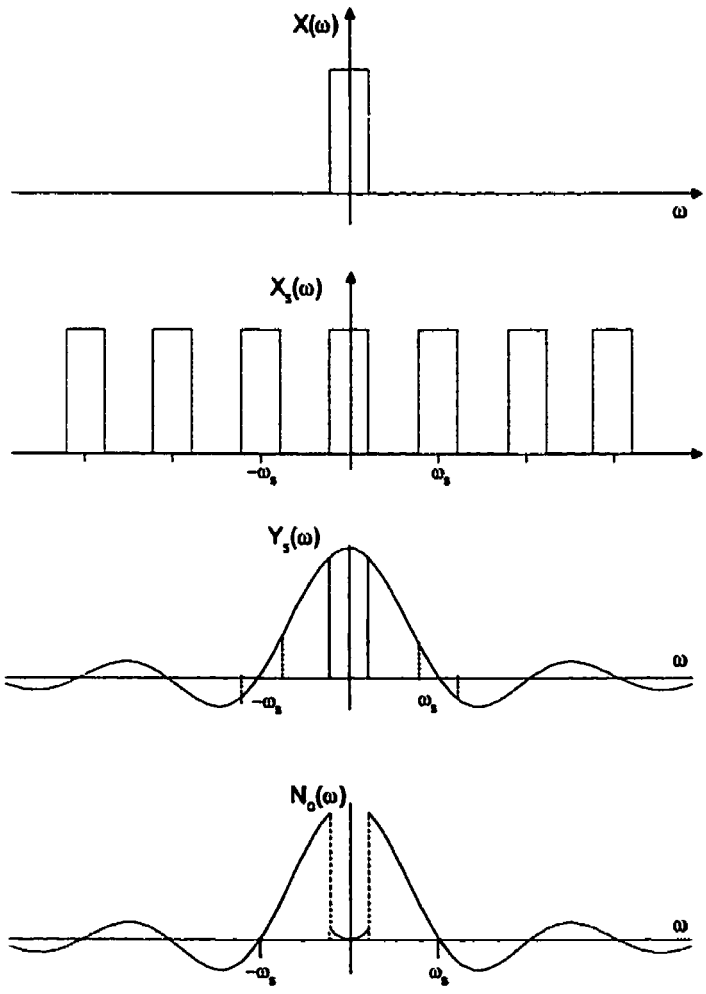


Figure 2.5 Spectrum representation of AZ

Thus the spectrum of the output noise with the autozero process can be expressed as:

$$N_o(\omega) = X(\omega) - Y_s(\omega) = X(\omega) - \frac{\sin(\omega T_s)}{\omega T_s} \sum_{n=-\infty}^{\infty} X(\omega - n\omega_s) \qquad (2.16)$$

Figure 2.5 illustrates a graphical interpretation of equation (2.16), with the assumed $X(\omega)$. It illustrates that the auto-zero technique effectively imposes a high-pass filters on the noise. For DC or very low-frequency noise, this results in an effective cancellation.

However, for the wide-band thermal noise, which has a spectrum wider than Nyquist frequency, the output noise spectrum foldover (aliasing) is inevitable. This can be understood clearly if we assume that the amplifier's wide-band noise is an ideally low-pass filtered white noise having bandwidth equal to F_B. The aliasing effect introduced by the sampling process in this case is illustrated in figure 2.6, which assumes that $F_B T_s = 2$. The original noise power spectrum is shifted by multiplying n of the sampling frequency and summed, resulting in a white noise of Power Spectrum Density (PSD) value approximately equal to $N \times S_0$, where N is the integer closest to the undersampling factor defined by $2F_B T_s$. Thus the output thermal noise PSD will be increased to [5]

$$S_{white}(f) = (2F_B T_s - 1) S_0 \sin c^2(\pi f T_s) \qquad (2.17)$$

If the undersampling factor $2F_B T_s$ is much larger than unity, the autozeroed white noise is thus dominated by the aliased broadband noise component.

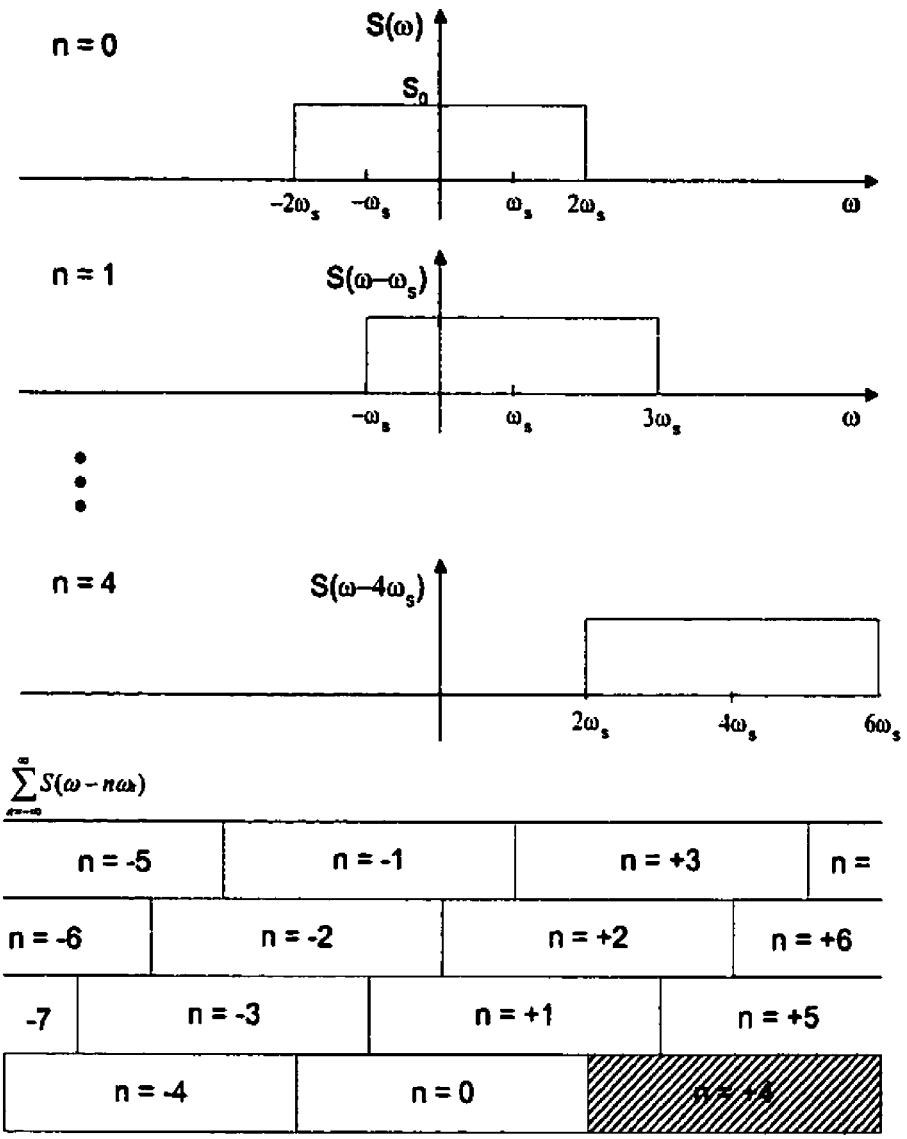


Figure 2.6 Increased white noise by aliasing

A similar analysis can be carried out for the 1/f noise, although 1/f noise has a narrow bandwidth, it still has a foldover component due to the aliasing of all the tails of the 1/f noise. It had been demonstrated that the aliasing increases log-arithmetically to $f_c T_s$ [5], rather than increasing proportionally as the white noise, thus the effect of aliasing on the 1/f noise is not as dramatic as that observed on the broadband white noise.

In conclusion, the auto-zero technique can effectively reduce the DC offset and low frequency noise, but at the cost of an increased white noise foldover component as well as 1/f noise.

2.3.2 Chopper Stabilization technique

An alternate approach to 1/f noise reduction is the CHopper Stabilization technique (CHS). This technique has been used for more than fifty years when the best DC performance was required. It was first used with vacuum tubes and mechanical relay choppers [10]. Recently, CHS has been used to reduce the low frequency noise and DC offset in CMOS technology.

2.3.2.1 Basic principle

The basic principle of CHS is reviewed in figure 2.7

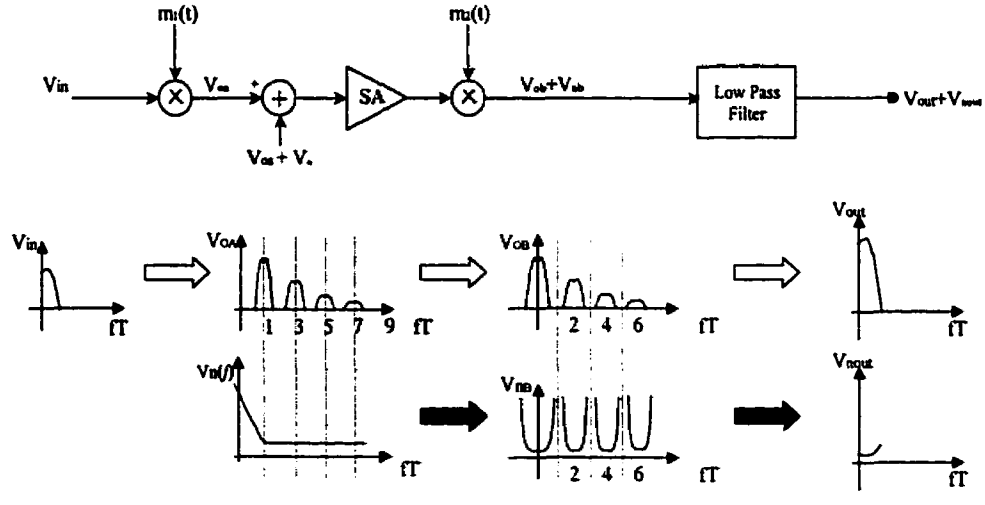


Figure 2.7 Principle of operation of the chopper stabilization technique

The input signal $V_{in}(t)$ is modulated by a square-wave signal $m_1(t)$ with frequency f_{chop}. After this modulation, the signal spectrum is transposed to the odd harmonic frequencies of the signal $m_1(t)$. It is then amplified by a selective amplifier (SA) and demodulated by signal $m_2(t)$ back to the original band. Suppose that the input signal has a spectrum limited to half the chopper frequency, then no signal aliasing occurs.

Modulating Signal $m(t)$ is a square wave function which is shown in figure 2.8. Its Fourier series and frequency spectrum are given in equations (2.18).

$$\begin{cases} m(t) = \dfrac{2}{\pi} \sum\limits_{\substack{n=-\infty \\ n\ \text{odd}}}^{+\infty} \dfrac{1}{n} \sin(2\pi n \dfrac{t}{T}) \\ M(f) = \dfrac{2}{j\pi} \sum\limits_{\substack{n=-\infty \\ n\ \text{odd}}}^{+\infty} \dfrac{1}{n} \delta(f - \dfrac{n}{T}) \end{cases} \tag{2.18}$$

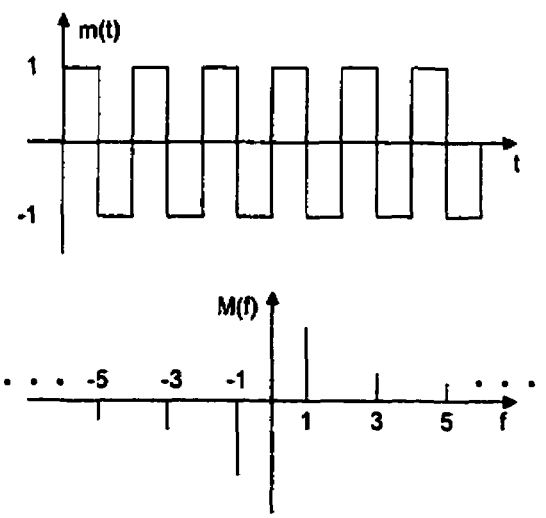


Figure 2.8 Modulation signal and its spectrum

Note that the low frequency noise and offset of the amplifier (represented by V_n and V_{os} respectively in figure 2.7) are only modulated once by the demodulator and translated to

the odd harmonics, leaving essentially white noise in the baseband. After demodulation, the signal is filtered at half the chopper frequency by a low pass filter, thus high-frequency components, which also include the 1/f noise and offset of the amplifier, will then be removed.

2.3.2.2 The effect of CHS on the amplifier noise

From the description of the CHS principle of operation, we know that the 1/f noise and DC offset will be reduced. However, the effect on thermal noise needs to be further discussed.

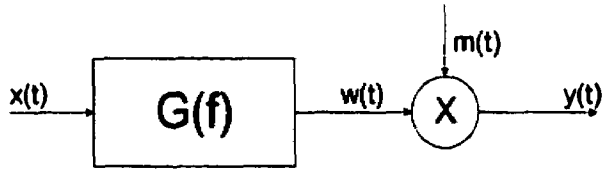


Figure 2.9 Noise modulation

The noise path is extracted from figure 2.7 as shown in figure 2.9, where *x(t)* represents the amplifier noise and DC offset, *y(t)* denotes its output. Enz presented in [4][5]: the power spectrum density (PSD) of the output white noise was

$$S_{white}(f) \approx S_{white}(0) = S_0 \cdot (1 - \frac{\tanh(\frac{\pi}{2} f_c T)}{\frac{\pi}{2} f_c T}) \qquad (2.19)$$

where S_0 represents the input thermal noise. The PSD is plotted in figure 2.10 against the white-noise bandwidth normalized to the chopper frequency. It shows that the chopper-modulated white noise power is always smaller than the power of the original white

noise. This implies that the CHS technique not only reduces the 1/f noise but also decreases the output thermal noise level.

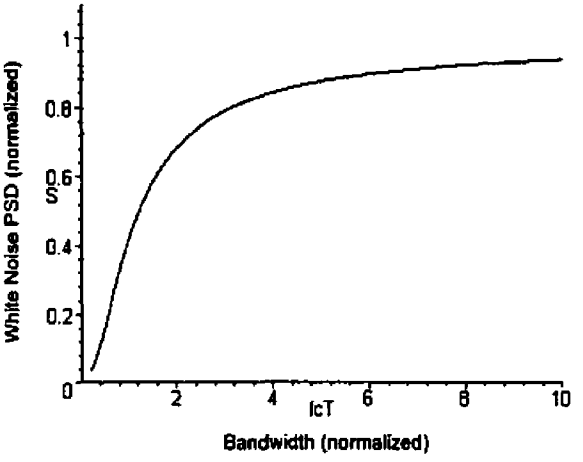


Figure 2.10 Chopper modulated white noise versus bandwidth

And according to [4][5]. the PSD of the output 1/f noise

$$S_{1/f}(f) \cong 0.8525 S_0 f_k T \tag{2.20}$$

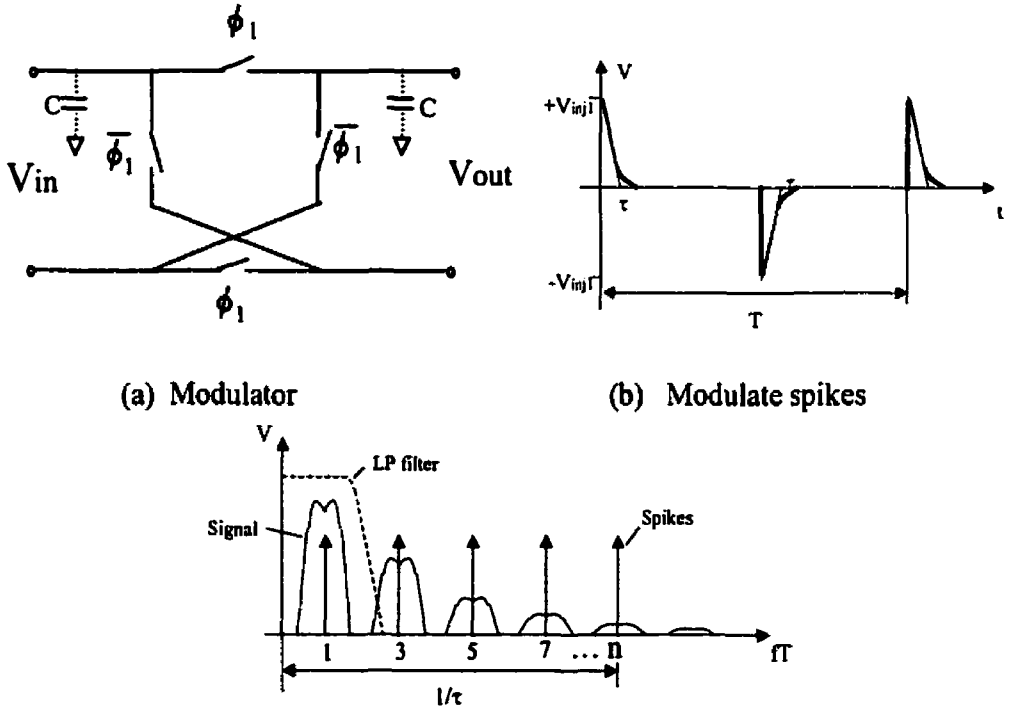
where f_k represents the chopper frequency.

2.3.2.3 Residual Offset

The inherent DC offset in the selective amplifier is completely removed, since it has been shift to the odd harmonics of the chopper frequency, and filtered by the low pass filter (LPF). In MOS circuits, the modulators are composed of four switches. It is inevitable that the charge injection through these switches, especially in the input modulator, will introduce a residual offset to the chopper amplifier. This charge injection and parasitic coupling cause spikes appearing at the input of the amplifier. Each time a MOS switch turns off, a certain amount of charge ΔQ flows into parasitic capacitors C, and causes a

"spike" with peak voltage $V_{inj} = \Delta Q/C$ as presented in figure 2.11. The time constant τ of the spikes has a value RC, where R represents the resistance of the input signal source.

This "spike" signal has a period of T ($1/f_{chop}$). Since the demodulation signal is also periodic with period T, a substantial part of this spike energy will be translated back to DC which result in a residual offsets. If care is taken to limit the time constant τ of those spikes to a value much smaller than T/2, most of the spike energy will remain on frequencies higher than the chopper frequency, as shown in figure 2.11 (c).



(a) Modulator

(b) Modulate spikes

(c) Spectrum of spikes and signals

Figure 2.11 Residual offset

The spectrum of the spike's signal is represented by impulses at the odd harmonics of the chopper frequency with an equivalent bandwidth proportional to $1/\tau$ and much larger than

f_{chop}. Meanwhile, figure 2.11 shows the spectrum of a modulated signal. Since the spectral envelope of the signal is inversely proportional to the frequency, the output signal after amplification and demodulation can be essentially reconstituted by its fundamental harmonic. This poses a problem of choosing an amplifier bandwidth in order to be capable of restoring the modulated signal while rejecting most of the spike's spectral components.

The spikes can be represented by the Fourier series [6]

$$x_{spike}(t) = \sum_{\substack{n=1 \\ odd}}^{\infty} \frac{4\tau}{T} V_{inj} \frac{1}{\sqrt{1+(n\omega\tau)^2}} \cos(n\omega t - \arctan(n\omega\tau)) \tag{2.21}$$

Amplified by the selective amplifier (SA), the spikes become

$$x_f(t) = \sum_{\substack{n=1 \\ odd}}^{\infty} A_n \cdot \frac{4\tau}{T} V_{inj} \frac{1}{\sqrt{1+(n\omega\tau)^2}} \cos(n\omega t - \arctan(n\omega\tau) + \phi_n) \tag{2.22}$$

where A_n and ϕ_n represent the amplitude and phase response of the SA at the frequency $n\omega$, respectively. Thus after demodulating, the residual offset can be written as:

$$\begin{aligned} V_{off} &= \Im_{LP}(x_f(t) \cdot m(t)) \\ &= \sum_{\substack{n=1 \\ odd}}^{\infty} A_n \cdot \frac{4\tau}{T} \cdot \frac{2}{n\pi} V_{inj} \frac{1}{\sqrt{1+(n\omega\tau)^2}} \cos(-\arctan(n\omega\tau) + \phi_n - \frac{\pi}{2}) \end{aligned} \tag{2.23}$$

where $\Im_{LP}$ represents an ideal low pass filter function having a cutoff frequency of one half of the modulation signal frequency f_{mod}. It illustrates that the effectiveness of the offset reduction depends on the transfer function of the selective amplifier.

It has been demonstrated that the 2nd order bandpass filter (BPF) is the best choice between offset reduction and complexity of the circuit [5][6]. Equation (2.24) presents the optimized residual offset of the CHS, which illustrates that in this case the residual offset is proportional to the square of the ratio between spike time constant τ and modulating signal period T.

$$V_{off} \approx 4A_0V_{inj}(\frac{2\tau}{T})^2 \qquad (2.24)$$

2.3.2.4 Comparison with AZ

Unlike the AZ process, the CHS approach does not use sampling techniques, but it is based on a modulation method. It does not alias the wideband noise, thus does not increase the baseband white noise. In addition, the amplifier is always connected with signal in CHS unlike in the autozero technique where during one of the phase the amplifier is disconnected. Furthermore, the AZ technique also suffers the charge injection, which result from the non-ideal MOS switches. Therefore the CHS is more effective for continuous time signal processing, such as monitoring the neuromuscular activities in the biomedical application. In this project we will take advantage of the chopper stabilization technique to reduce the 1/f noise and DC offset.

2.4 Low noise circuits within recent literatures

So far, a few papers have discussed the low noise circuit techniques. Timothy et al. [29] presented a compact low noise operational amplifier in 1.2 um digital CMOS technology,

which used the lateral PNP transistors as the input stage to reduce the 1/f noise. Due to the inherent low 1/f noise attribute of the bipolar transistor, the circuit features a input referred noise of 23.8 $nV/\sqrt{Hz}$ at 1 Hz, with a closed loop gain 20.8 dB, a minimum PSRR of 68 dB and a CMRR of 100 dB. It worked under a ±2.5 V supply. The chip area of the fabricated amplifier is 0.211 mm^2 only. However, the bipolar input stage of the amplifier makes it only suitable for applications that can tolerate its low input impedance, not applications like urine monitor system, where the source impedance is about 10k Ω [1].

Wong et al. introduced a switched differential Op-amp with low offset and reduced 1/f noise [10]. The authors proposed a dynamic technique for implementing fully differential op-amps (DOA) by time-sharing conventional single-output op-amps (SOA), which took advantages of the auto-zero technique to reduce the input DC offset and 1/f noise. The authors analyzed the reduction of offset and 1/f noise produced by the technique, unfortunately they did not mention its impact on the input thermal noise. The circuit was implemented using a 5-um polysilicon-gate CMOS process. The Opamp realized 52 dB gain with input noise density of 200 $nV/\sqrt{Hz}$ at 1k Hz. The offset was reduced to 0.4 mV. It worked under a ±5V power supply.

Enz discussed chopper stabilization to reduce the DC offset and 1/f noise of conventional monolithic CMOS opamp [4][5][29]. The author provided a detailed mathematical analysis of the effect on Opamp thermal noise, 1/f noise and the residual offset

introduced by a non-ideal modulator. The author also compared the CHS technique with the auto-zero technique. He demonstrated that CHS is more adaptable in continuous time signal applications than other known techniques. Furthermore, the authors pointed out that the critical part of CHS amplifier design is to use an optimized selective amplifier to reduce the residual offset. The selective amplifier presented in [5] made use of a 2nd order continuous time gm-C BP filter only. It realized a 56 dB DC gain, however an offset compensation circuit was necessarily associated with the high gm value of the input transconductor. Its equivalent input-referred noise was $47nV/\sqrt{Hz}$ under a 5V supply voltage.

Menolfi et al. presented further insight on the chopper stabilization technique to reduce the offset and the flicker noise [6][7]. The authors analyzed the residual offset in the time domain, and illustrated that a band-pass filter provides the best choice between the residual offset reduction and the circuit complication. The authors also suggested that the common mode rejection ratio can be improved by CHS. Moreover, a low noise amplifier based on the CHS technique has been implemented and used successfully in a thermoelectric infrared detectors. Two stages [6] and three stages [7] amplifiers were used as the selective amplifier respectively which allow to easily realize a high gain. The equivalent input-referred noise in the case of two stage amplifier was 15 $nV/\sqrt{Hz}$ [6]. The supply voltage was 5V and the power consumption was 3 mW.

Table 2-1 depicts a summary of those techniques and their respective performance.

	Timothy et al	Wong et al	Enz.	Menolfi et al
Key Words	Lateral BJT	Switched Opamp	CHS	CHS
Power Supply	±2.5 V	±5V	5V	5V
Utilize technology	1.2 um	5-um	SACMOS	1-um
Input referred noise	23.8 nV/$\sqrt{Hz}$ @ 1 Hz	200 nV/$\sqrt{Hz}$ @ 1k Hz	43 nV/$\sqrt{Hz}$	15 nV/$\sqrt{Hz}$
Input DC offset	N/A	0.4 mV	0.62μV	0.5μV
DC gain	20.8 dB	52 dB	56 dB	52 dB
Surface area size	0.211 mm^2	N/A	N/A	1260×1150 μm^2
Reference	[29]	[10]	[4][5]	[6]

Table 2.1 Main characteristics of reported low-noise preamplifiers

2.5 Conclusion

This chapter has reviewed the important concepts in the design of CMOS low noise circuits. First two dominant noise sources in MOSFET transistors were introduced. And the effect of downscaling of the CMOS technology on the system noise was presented. This was followed by a discussion on the two circuit low noise techniques. Based on the

comparison of two techniques, The CHS technique will be used in this project to reduce the low frequency noise and DC offset.

CHAPTER 3

CHOPPER STABILIZATION TECHNIQUE

3.1 Introduction

The basic principle of Chopper stabilization technique has been introduced in the last chapter and main previous CHS analysis works have been reviewed. It has also been illustrated that one of the critical parts of CHS is to design an optimized selective amplifier, which not only amplifies the signal to a high level, but also can reduce the residual offset that stems from the charge injections of the input modulator.

Enz and Menolfi both have demonstrated that making use of a 2^{nd} order bandpass filter (BPF) as the SA is the best compromise between offset reduction and complexity of circuit. However their analyses and conclusions of the effect of CHS on amplifier noise (equations (2.19) and (2.20)) were based on analyzing a 1^{st} order low-pass filter from the viewpoint of simplicity, rather than a 2^{nd} order BPF used in practice. Thus in this chapter, detailed discussions of the CHS amplifier with a 2^{nd} order BPF and illustration of its two supplementary characteristics of CHS will be given. The next section will first introduce a CHS behavior model that is built under SIMULINK toolbox in Matlab. The proposed model can be used to simulate the practical behavior of chopper stabilization technique in

a view of theory and mathematical consideration, so that we can use it to verify our analyses and conclusions later.

3.2 A CHS Behavior Model in MATLAB/SIMULINK

With the rapid evolution of the design technology, time-to-market is one of the crucial factors in the ultimate success of a component. Designers have, therefore, increasingly adhered to design methodologies and strategies that are more amenable to design automation and flexible analysis. Chopper stabilization technique has been known for a long time to realize high-precision DC gains with AC-coupled amplifiers and reduce the low frequency noise. However, its relatively complicated mathematical model which refers to twice frequency transforms and once non-ideal filter, makes that designing and optimizing the CHS circuit be a bewildering and tedious work. Moreover, the random attribute of the noise and other practical non-idealities in circuit implementation, further contribute to the complexity and difficulty of CHS analysis. These problems will be identified by the CHS behavior model built with MATLAB/SIMULINK.

3.2.1 Model Description

SIMULINK is a software package for modeling, simulating and analyzing dynamical systems. It supports linear and nonlinear systems modeled in continuous time, sampled time or a hybrid of the two. Figure 3.1 depicts the proposed CHS behavior model.

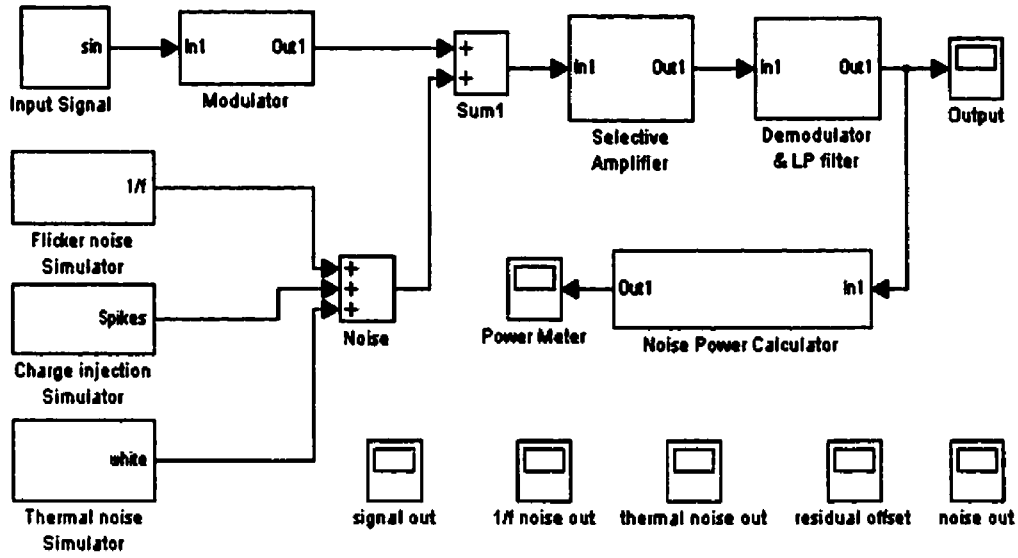


Figure 3.1 A CHS model in SIMULINK

The model includes several sub-modules, which take advantages of simplified mathematical model to approximate their real-world functions. Therefore, it can be used to analyze and optimize our circuit design. The model consists of the following parts.

3.2.1.1 Modulator

The mathematical function of an ideal modulator is given by

$$y(t) = x(t)m(t) \tag{3.1}$$

The equation can be realized by a switch controlled by a square wave block in SIMULINK as shown in figure 3.2. And the modulate frequency is able to be tuned by changing frequency of the square wave block.

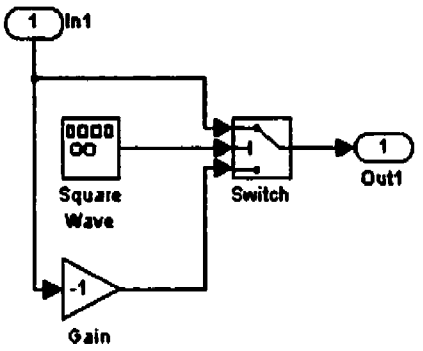


Figure 3.2 Modulator sub-system

3.2.1.2 Selective Amplifier

In practice, the operational amplifier has a very complex model. It is confined by its DC gain, bandwidth, slew rate, settling time etc. As the CHS amplifier is used in ultra low-amplitude application, some large signal model specifications such as slew rate and settling time can be neglected. An ideal transfer function model is enough to mimic an amplifier here. We make use of a 2^{nd} order bandpass filter transfer function as shown in figure 3.3. Its DC gain, quality factor Q and center frequency can be specified according to our requirements. For example in the figure 3.3, they are set as 1, 10 and 50k respectively.

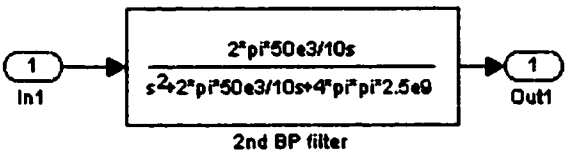


Figure 3.3 Selective Amplifier model

3.2.1.3 Demodulator & LP filter

The demodulator module is essentially similar to the modulator module when a 2nd BPF is chosen as the selective amplifier. The output LP filter is used to remove the high harmonics and the shifted flicker noise. Its cutoff frequency is specified at half of the modulating frequency. For more precision output, a 4th order butterworth LP filter is used.

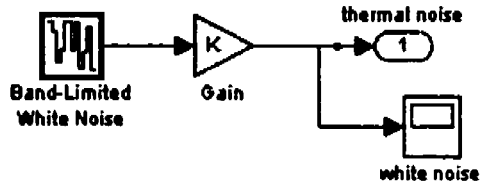
3.2.1.4 Noise & Offset Simulator

Although there are noise models of MOS transistor in the circuit simulators, such as HSPICE and SPECTRE, they can only be used to predict the noise power spectrum density (PSD) value of practical circuits. To observe the noise reduction by CHS, the best way is to simulate it with transient analysis. However in HSPICE and SPECTRE, it is not easy to mimic the input thermal noise and 1/f noise. Fortunately, the difficulty can be overcome easily in the proposed behavioral model.

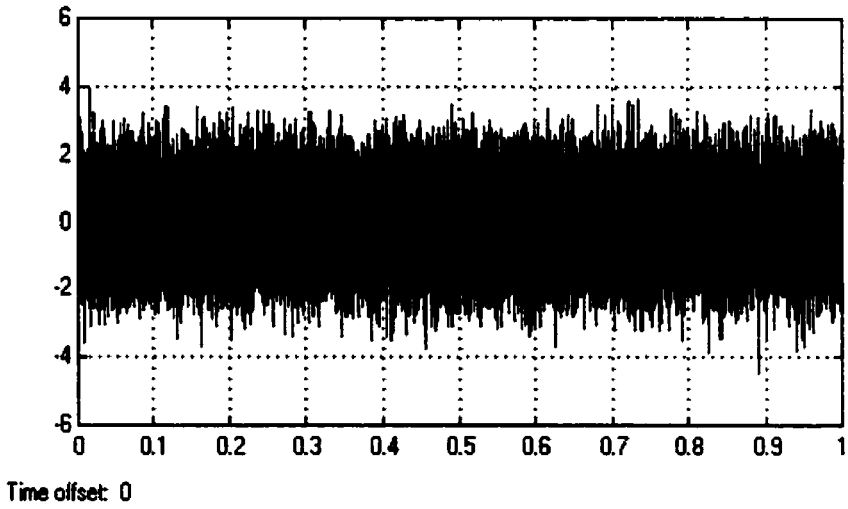
1) Thermal noise

As the emphases of noise analysis in the behavior model is to verify the noise reduction effect by CHS. It is not necessary to approximate the real noise values in circuit. Theoretically, continuous white noise has a correlation time of 0, a flat Power Spectral Density (PSD), and a covariance of infinity. The proposed thermal noise generator module is shown in figure 3.4-a. The band-limited white noise block generates a random sequence with a correlation time much smaller than the shortest time constant of the

system [28]. The gain block is used to adjust the level of the noise floor in the same order of the input signal. Figure 3.4-b presents the generated thermal noise.



a)



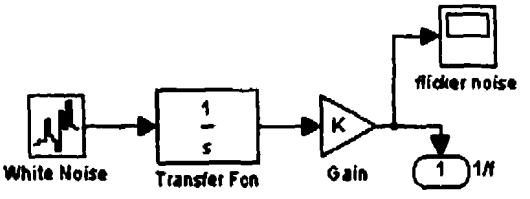
b)

Figure 3.4 a) Thermal noise module and b) generated thermal noise

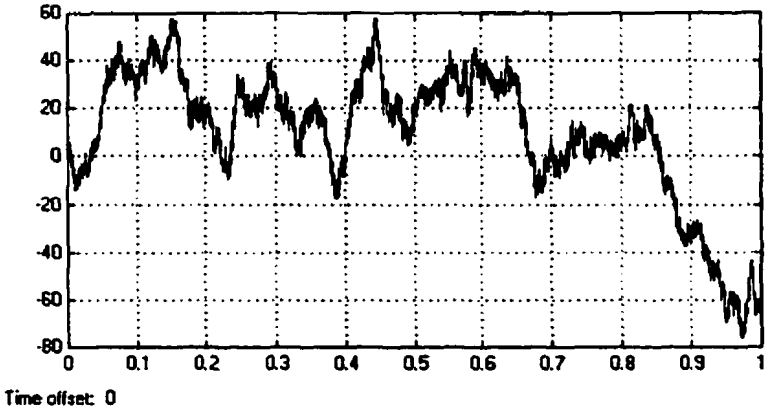
2) Flicker noise

As the integrator has a similar frequency characteristic with the spectrum of 1/f noise, we can use an integrated white noise to simulate the flicker (1/f) noise. The model is shown in figure 3.5-a. Again the gain block is used to limit its amplitude. As we know, the noise corner frequency of a CMOS circuit is the frequency when PSD of 1/f noise equals to the

PSD of thermal noise. Thus in this model, it will be possible to set the corner frequency by adjusting the gain block in 1/f noise and thermal noise modules. The generated flicker noise is shown in figure 3.5-b. The spectrums of white noise and flicker noise are depicted in figure 3.6. In this case, the corner frequency is close to 3 KHz.



a)



b)

Figure 3.5 a) Input noise module and b) generated input 1/f noise

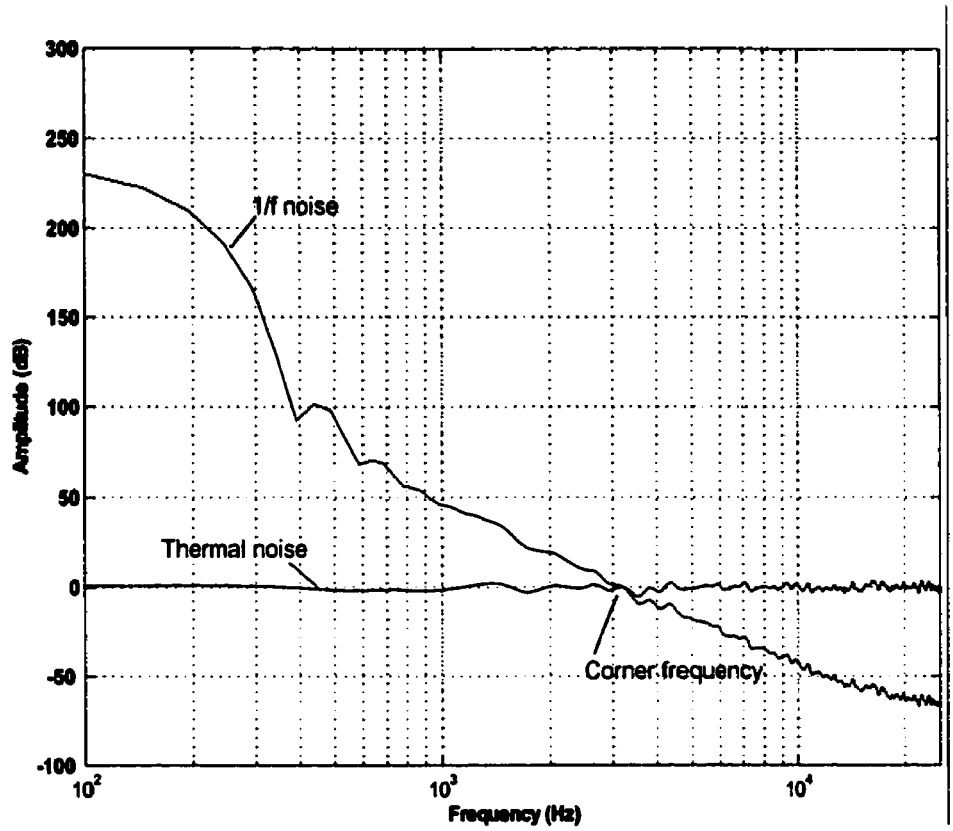
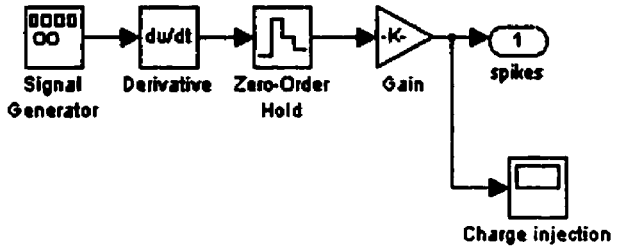


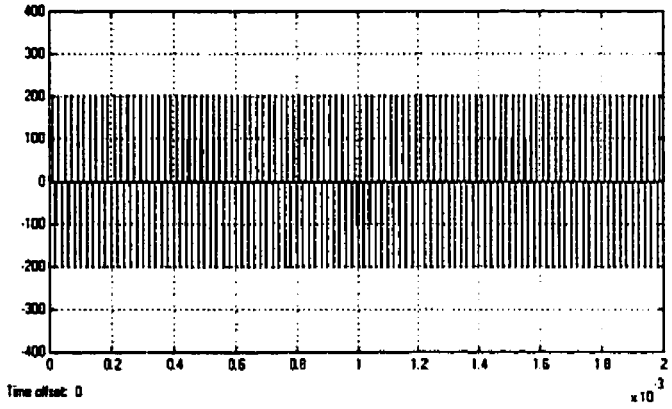
Figure 3.6 Spectrums of 1/f noise and white noise

3) Charge injection

The charge injection of CMOS switches in the modulator generates the spikes which lead to a residual offset in output. To evaluate the CHS performance, it is indispensable to simulate the charge injection phenomena in the proposed behavioral model. Figure 3.7-a presents the charge injection simulator module achieved by a derivative block. Here, the signal generator outputs a series of pulse signal. After passing through the derivative block, a spike series having the same frequency with the pulse signal is generated as shown in figure 3.7-b. The zero-order block is used to specify the time constant of charging.



a)



b)

Figure 3.7 (a) Charge injection simulator (b) modulator spikes

3.2.1.5 Noise Power Calculator

In order to evaluate the noise performance of CHS, the simulated noise output need to be further processed to calculate its power. The average noise power can be found by evaluating the integral

$$P_{noise} = \frac{V_{n(rms)}^2}{1\Omega} = V_{n(rms)}^2 = \frac{1}{T}\int_0^T V_n^2(t)dt \qquad (3.2)$$

The equation is realized by the noise power calculator module, as shown in figure 3.8, where u(1) represents input variable of the function.

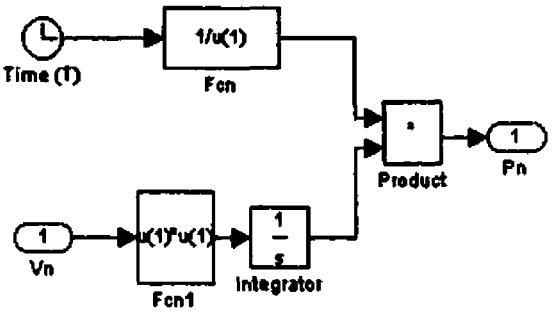


Figure 3.8 Noise power calculator module

3.2.2 Non-idealities Consideration

One impressive feature of the behavioral model is that it can conveniently simulate the effects of circuit non-idealities, such as tuning error between the modulating clock frequency (f_{chop}) and the center frequency (f_c) of SA, time delay of two modulating signals, etc. These non-idealities are represented by some parameters of module or the customized transfer function. For example, to simulate the effect due to the time delay between two modulating clocks, only a transport delay block in the demodulator model needs to be added. And the delay time can be set arbitrarily.

3.2.3 A Simulation Example

The figure 3.9 shows an example simulation result of the proposed behavior model. Suppose the input is a sinusoidal signal with a frequency of 1k Hz and an amplitude of 5 volt. The simulated thermal noise, input flicker noise and modulator spikes which were presented early are added to the input signal. The output of the CHS, consists of both

signal and noise contributions. As we expected, the significant input noises didn't make an impact on the output signal and the 1/f noise has been removed thoroughly. The time delay mainly comes from the output 4^{th} order lowpass filter.

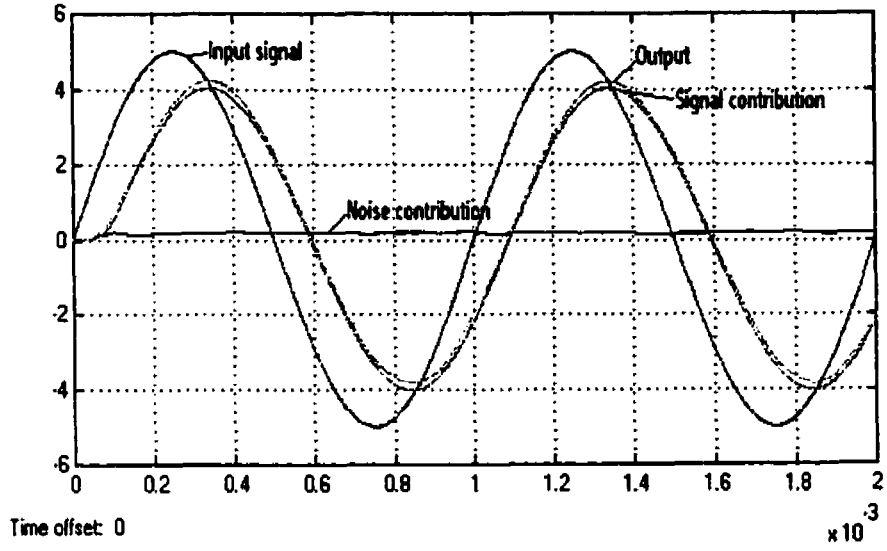


Figure 3.9 A simulation result of CHS model

Summarizing, the proposed model uses the blocks in SIMULINK and the custom Matlab functions to simulate the behavior of CHS. Comparing with the transistor level simulator, it does not consider so many second or third order issues. It is used to obtain information about the first-order requirements and is very useful to analyze the overall performance of a design. This method allows us to perform exhaustive behavioral simulations of the chopper amplifier. And it will be used to analyze the practical CHS amplifier as shown in the following section.

3.3 Supplemental analyses of CHS

3.3.1 Characteristics of CHS

Although the extensive discussion on CHS basic operation has been presented in [5][6]. Two complementary characteristics of CHS could be summarized as follows for a further understanding of CHS.

- **Amplitude modulation (AM).**

The modulated carrier can be represented by :

$$y(t) = x(t)m(t) = \sum_{\substack{n=-\infty \\ odd}}^{\infty} \frac{2}{n\pi} x(t)\sin(\frac{2n\pi t}{T}) = \sum_{\substack{n=-\infty \\ odd}}^{\infty} A_n(t)\sin(\frac{2n\pi t}{T}) \qquad (3.3)$$

where the carrier amplitude $A_n(t)$ is linearly related to the input signal x(t). And in this case, since $A_n(t)$ is proportional to the message signal x(t) and the proportionality is $\frac{2}{n\pi}$, the modulation is also named double-sideband (DSB) modulation. One important property of the DSB modulation, is that for demodulation, the demodulator signal should be in phase and frequency synchronism with the incoming carrier [42].

- **Quasi Linear Time-invariable (LTI) system**

The DSB modulation is a linear process because it satisfies the two conditions of linear system: additivity and homogeneity. But due to the fact that the output y(t) also depends on the carrier signal m(t) (3.4), it does not satisfy the delay property of a time-invariable system. Hence it is not a LTI system.

$$y(t-t_0)=x(t-t_0)m(t-t_0)\neq x(t-t_0)m(t)=\Im[x(t-t_0)] \tag{3.4}$$

However in the CHS amplifier, the input signal passes through two modulators and is filtered by a low-pass filter. When the signal bandwidth is limited to the half of the modulating signal (carrier) frequency, the output can be expressed as:

$$y(t)=\Im_{LP}[m(t)x(t)m(t)]=\alpha\cdot x(t) \tag{3.5}$$

where α is a coefficient constant in terms of frequency, which is independent of time. Note that the output will not be related to the carrier signal m(t) any more. Hence, in a limited bandwidth $f_{sig}<\frac{1}{2}f_{mod}$, CHS behaves like a quasi LTI system. All the approaches in LTI system can be used to analyze the signal processing in CHS, but can not be used to calculate noise performance.

3.3.2 Chopper amplifier with the 2nd order BPF

The chopper amplifier performance is dependent on the type of selective amplifier. In the present application, a 2nd order bandpass filter is chosen as the SA, whose transfer function can be expressed as:

$$G(f)=\frac{A\times Q}{1+jQ\dfrac{f^2-f_c^2}{f\cdot f_c}}. \tag{3.6}$$

where A denotes the gain of filter, f_c is the center frequency of the bandpass filter, Q represents the quality factor. In the following part, the chopper amplifier with the 2nd order BPF will be discussed in details.

3.3.2.1 Transfer Function in CHS

As CHS is a quasi LTI system, its transfer function exists in the limited bandwidth. Figure 3.10 presents the signal path of CHS. The output signal spectrum is given by

$$\begin{aligned} Y(f) &= \{[X(f) * M_1(f)] \cdot G(f)\} * M_2(f) \\ &= [(\frac{2}{\pi}) \sum_{\substack{n=-\infty \\ n\,\text{odd}}}^{+\infty} \frac{1}{n} X(f - \frac{n}{T}) \cdot G(f)] * [(\frac{2}{\pi}) \sum_{\substack{n=-\infty \\ n\,\text{odd}}}^{+\infty} \exp(-j2\pi n \frac{t_0}{T}) \frac{1}{n} \delta(f - \frac{n}{T})] \end{aligned} \tag{3.7}$$

where, T represents the period of the modulating signal, t_0 denotes the time delay between $m_1(t)$ and $m_2(t)$. Assume the two modulating signals $m_1(t)$ and $m_2(t)$ are synchronous, and the frequency is limited to one half of the modulating frequency, then the output signal spectrum can be rewritten as:

$$Y(f) = (\frac{2}{\pi})^2 X(f) \sum_{\substack{n=-\infty \\ n\,\text{odd}}}^{+\infty} \frac{1}{n^2} G(f - \frac{n}{T}) \tag{3.8}$$

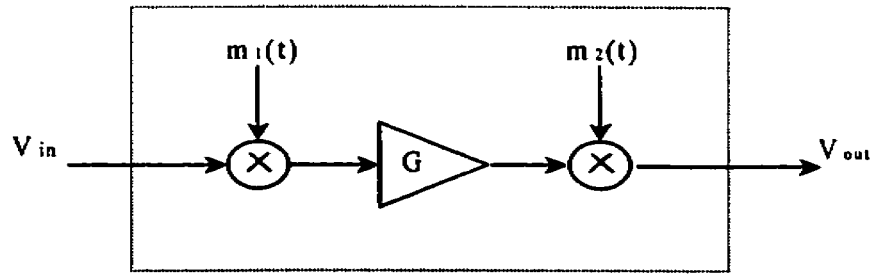


Figure 3.10 Signal path in CHS

The CHS transfer function can be derived from (3.8), and be rewritten using equation (3.6)

$$H(f)=\frac{Y(f)}{X(f)}=(\frac{2}{\pi})^2\sum_{\substack{n=-\infty\\ n\,odd}}^{+\infty}\frac{1}{n^2}G(f-\frac{n}{T})$$
$$=(\frac{2}{\pi})^2\sum_{\substack{n=-\infty\\ n\,odd}}^{+\infty}\frac{1}{n^2}\cdot\frac{A\cdot Q}{1+jQ\cdot\frac{(fT-n)^2-f_cT^2}{(fT-n)\cdot f_cT}} \qquad (3.9)$$

The numerical calculation result of the normalized H (f) magnitude is depicted in figure 3.11, where the center frequency of filter f_c is tuned equal to the chopper frequency ($f_cT=1$). Note that the modulation and demodulation only introduce a coefficient to the output signal. The normalized DC gain $(\frac{2}{\pi})^2\sum_{\substack{-\infty\\ odd}}^{\infty}\frac{n^2}{n^2+Q^2(n^2-1)^2}$ is approximately equal to $2\times(\frac{2}{\pi})^2=0.81$. It implies that the overall gain of CHS will lost about 20% because the selective amplifier rejected most part of harmonics. This is verified in the behavior model simulation result as was shown in figure 3.9. The bandwidth of signal equals $\frac{f_c}{2Q}$.

And the output signal power S_o is given by

$$S_o(f)=|H(f)|^2\,S_i(f)=(\frac{8}{\pi^2})^2 S_i(f)|\sum_{\substack{n=1\\ n\,odd}}^{+\infty}\frac{1}{n^2}\cdot\frac{1}{1+jQ\cdot\frac{(fT-n)^2-f_cT^2}{(fT-n)\cdot f_cT}}|^2 \qquad (3.10)$$

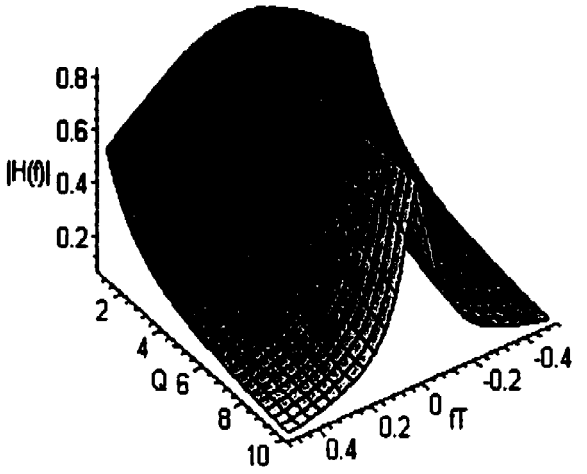


Figure 3.11 Transfer function of CHS

3.3.2.2 Modulated Noises

For the reason that the noises in CHS are only modulated once as was shown in chapter 2, the noise path is a time variable system, thus in strictly sense, the equation in LTI system

$$S_{yy}(f) = |H(f)|^2 S_{xx}(f) \tag{3.11}$$

can not be used to analyze the modulated noise system. Since it still satisfies the conditions of linear system, we can analyze the thermal noise and flicker noise respectively and superimpose their effect later.

1. Thermal noise

As was shown in chapter 2, the mean square thermal noise density can be represented as $N_{iw} = 4kTR$. After the white noise is passed through the 2nd order BPF (narrowband linear filter), a narrowband process is produced. The noise can be represented by the expression

$$n_w(t) = V(t)\cos[\omega_c t + \phi(t)] \tag{3.12}$$

where V(t) and $\phi(t)$ are random processes which are called the envelope function and phase function respectively, and ω_c denotes the center frequency of the BPF.

Equation (3.12) can be rewritten as

$$n_w(t) = V(t)\cos\phi(t)\cos\omega_c t - V(t)\sin\phi(t)\sin\omega_c t = n_c(t)\cos\omega_c t - n_s(t)\sin\omega_c t \tag{3.13}$$

where

$$n_c(t) = V(t)\cos\phi(t) \text{ (quadrature component)} \tag{3.14}$$

$$n_s(t) = V(t)\sin\phi(t) \text{ (in-phase component)} \tag{3.15}$$

Through the demodulator and low pass filter, the noise becomes

$$n_{ow}(t) = \Im_{LP}[n_w(t)\cdot\sum_{\substack{n=1\\ odd}}^{\infty}\frac{4}{n\pi}\sin(n\omega_c t)] \approx \frac{2}{\pi}\cdot n_s(t) \tag{3.16}$$

The output thermal noise power is given by [42]

$$N_{ow} = E[{n_{ow}}^2(t)] = \frac{4}{\pi^2}E[{n_s}^2(t)] = \frac{4}{\pi^2}N_{iw} \tag{3.17}$$

The thermal noise simulation result of CHS model is depicted in figure 3.12. The ratio between the input thermal noise and the output thermal noise (BPF) was about $\frac{\pi^2}{4}$ as we expected. And from equation (3.10) and (3.17) the output SNR is

$$(\frac{S}{N})_{ow} = \frac{S_o(f)}{N_{ow}} \geq \frac{(\frac{8}{\pi^2})^2 S_i(f)}{\frac{4}{\pi^2}N_{iw}} = \frac{16}{\pi^2}(\frac{S}{N})_{iw} \tag{3.18}$$

It can be arranged as

$$\frac{(S/N)_{ow}}{(S/N)_{iw}} \geq \frac{16}{\pi^2} \tag{3.19}$$

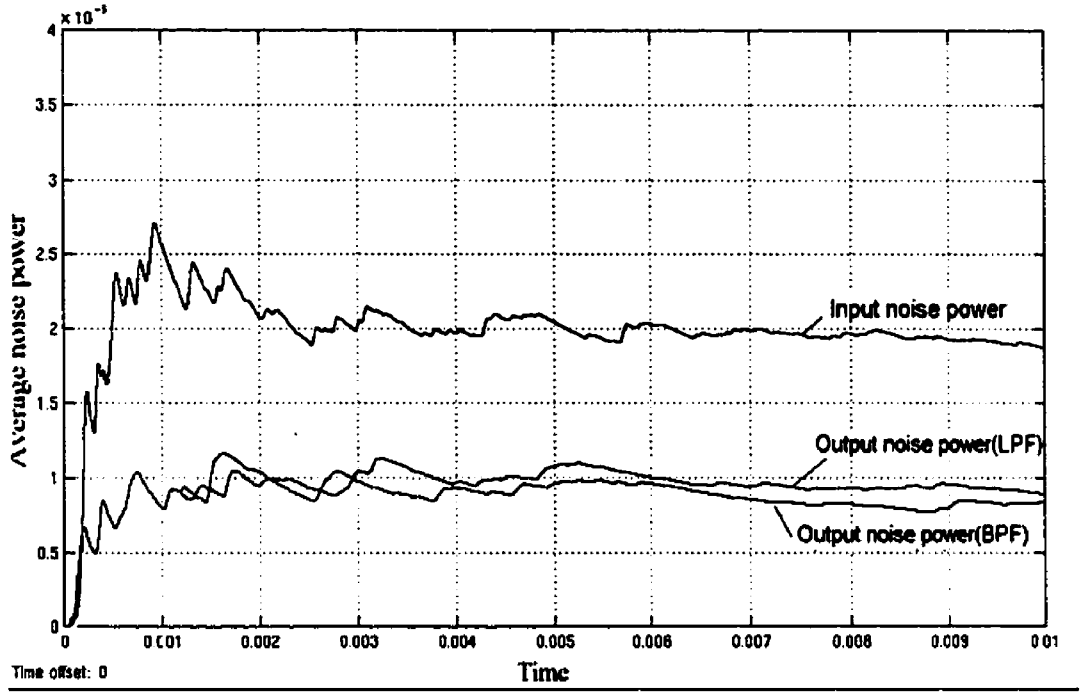


Figure 3.12 Thermal noise simulation

Thus, the thermal noise SNR with CHS has been increased to $\frac{16}{\pi^2} = 1.62$ times compare without CHS. It is not difficult to understand that: the modulator block just flip and flop the thermal noise whose sign is a random positive or negative, thus there is no effect on the overall PSD of the thermal noise. However for the signal, the input modulator introduces a coefficient $k=\frac{4}{\pi}$ to the first harmonic which composes the mainly part of the restored signal, the increased signal improves the SNR a ratio k^2. We notice that the output thermal noise with LPF as the selective amplifier is a little bit higher than the

noise power with BPF, as shown in figure 3.12. It is because that the thermal noise passing through the BPF has been filtered in lower sideband (LSB) more than in LPF.

2. Flicker noise

The origin and mechanism of flicker noise have been introduced in chapter 2, for simplified analysis, its PSD can be represented as

$$N(f)_{1/f} = \frac{K}{f^{\gamma}} \qquad \text{where: } 0.7 < \gamma < 1.3 \tag{3.20}$$

Without loss of generality, the parameter γ can be set as 1. The output 1/f noise power spectral density is derived by:

$$N_o(f)_{1/f} = V_{yy}^2(f)_{1/f} = KT \cdot \frac{4}{\pi^2} \left| \sum_{\substack{n=-\infty \\ n\ \text{odd}}}^{+\infty} \frac{1}{n^2} \cdot \frac{1}{|fT-n|} \cdot G(f - \frac{n}{T}) \right|^2 \tag{3.21}$$

As the noise PSD of chopper frequency $N(f_c)_{1/f} = \frac{K}{f_c} = KT$, we can rewrite (3.21) as

$$\begin{aligned} N_o(f)_{1/f} &= N(f_c)_{1/f} \cdot \frac{4}{\pi^2} \left| \sum_{\substack{n=-\infty \\ n\ \text{odd}}}^{+\infty} \frac{1}{n^2} \cdot \frac{1}{|fT-n|} \frac{1}{1+[Q \cdot \frac{(fT-n)^2 - f_cT^2}{(fT-n) \cdot f_cT}]^2} \right|^2 \\ &= N(f_c)_{1/f} \cdot A(f,Q) \end{aligned} \tag{3.22}$$

It illustrates that the output flicker noise at baseband can be represented by the input flicker noise at chopper frequency multiple a coefficient function $A(f,Q)$, which depends on the frequency and quality factor of BPF. Figure 3.13-a shows the numerical calculation result of the function $A(f,Q)$. Note that the output flicker noise has the maximum value at DC and inversely proportion with frequency because of the shape of

the BPF transfer function, its magnitude has been significantly reduced, around two times $N(f_c)_{1/f}$ only.

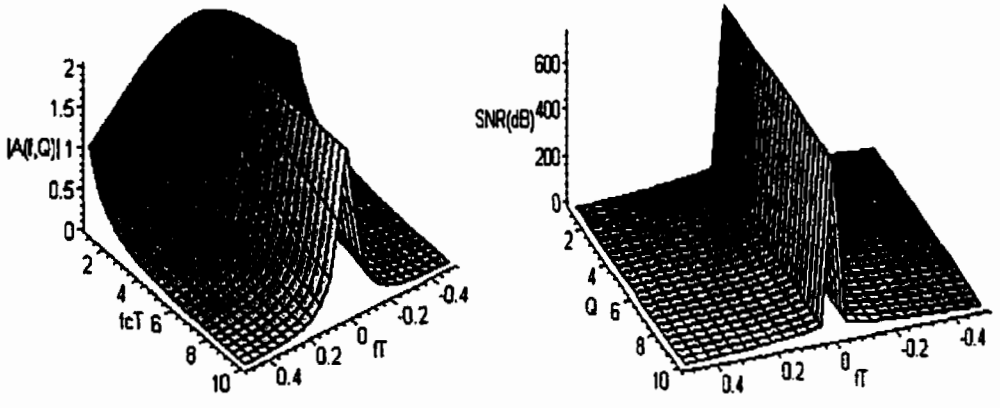
The output signal to flicker noise ratio (SNR) is given by

$$(\frac{S}{N})_o = \frac{S_o(f)}{N(f_c)_{1/f} \cdot A(f,Q)} = \frac{|H(f)|^2 S_i(f)}{N(f)_{1/f} \cdot fT \cdot A(f,Q)} \tag{3.23}$$

It can be arranged as

$$\frac{(S/N)_o}{(S/N)_i} = \frac{|H(f)|^2}{fT \cdot A(f,Q)} \tag{3.24}$$

which is shown in figure 3.13-b. We know that the flicker noise has been significant reduced, especially at low frequency region.



(a) Flicker noise coefficient function A(f,Q) (b) Improved signal to flicker noise ratio

Figure 3.13 Calculation result of flicker noise reduction

3.3.2.3 Frequency Tuning Error

Among the above analysis, the center frequency of BPF f_c is assumed to be locked at the chopper frequency f_{chop} ($f_cT=1$). However, in practice, it is unavoidable that there is a tuning error between f_{chop} and f_c. This tuning error will affect the signal transfer function,

as well as impact the residual offset. The CHS transfer function H(*f*) versus tuning value f_cT (equation (3.9)) is shown in figure 3.14, where the quality factor Q was set to 4. Since there is a tuning error between f_c and f_{chop}, the peak value of the transfer function appears at the tuning difference frequency $|f_c-f_{chop}|$, not at the DC level as the tuned case. And that the signal amplified away BPF center frequency f_c will cause more distortion.

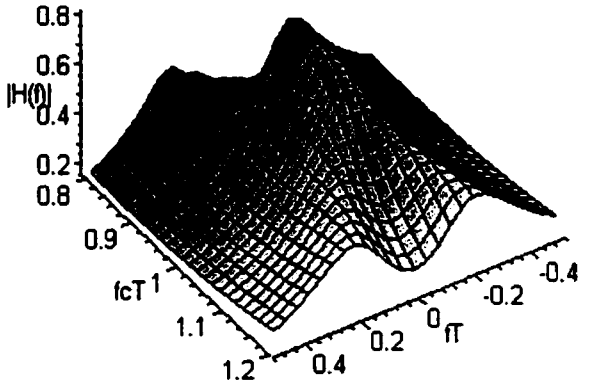


Figure 3.14 Transfer function variation due to the tuning error

In addition, the tuning error can result in more residual offset. The residual offset is dominated by the first harmonic spike and it is almost quadrature with the modulate signal in tuned case. The tuning error introduces an additional phase shift θ to the first harmonic spike. The equation (2.23) can be rewritten as:

$$V_{off} = \frac{2}{\pi}\frac{4\tau}{T}A_0V_{inj}\frac{1}{\sqrt{1+(\frac{2\pi\tau}{T})^2}}\sin(\arctan(\frac{2\pi\tau}{T})-\theta) \approx -\frac{2}{\pi}\frac{4\tau}{T}A_0V_{inj}\sin\theta+4A_0V_{inj}(\frac{2\tau}{T})^2\cos\theta \quad (3.25)$$

The introduced phase shift θ causes a significant increase of the residual offset since the first term is proportional to the $\frac{\tau}{T}$ rather than $(\frac{\tau}{T})^2$. Note that the negative phase shift may cause a negative DC offset. Figure 3.15 shows the simulated residual offset resulting from five different center frequencies.

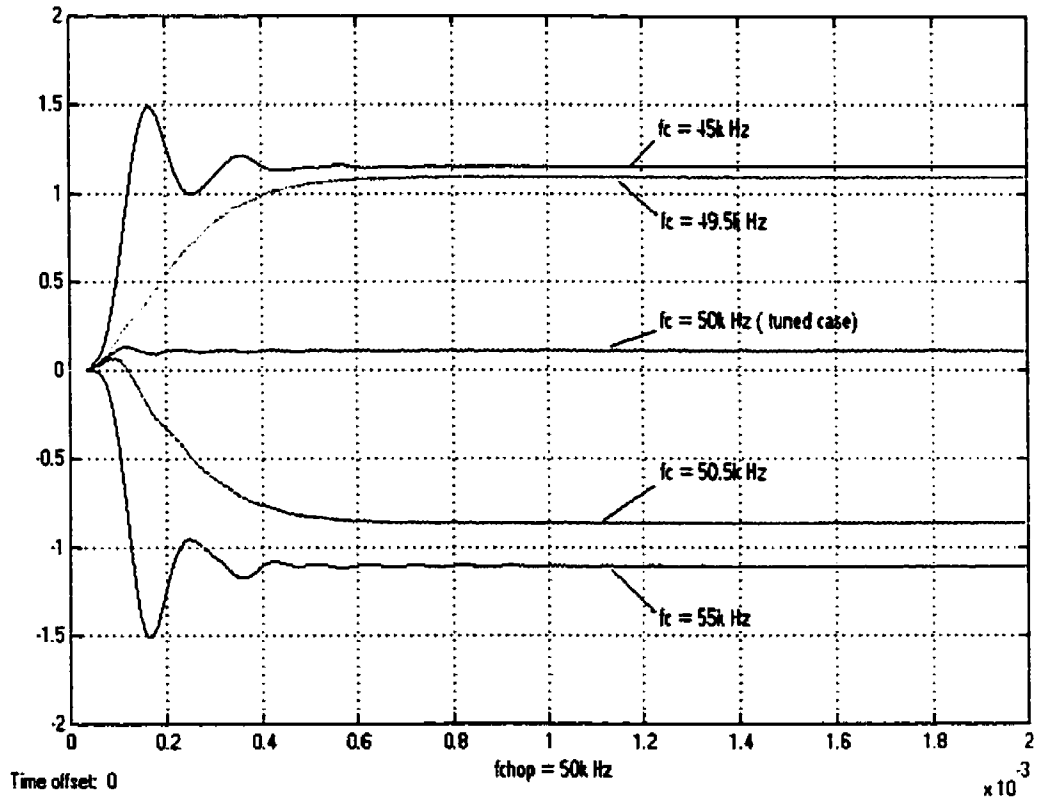


Figure 3.15 Residual offset versus tuning error

3.4 Summary

From the above analysis, we can conclude that the 1/f noise in CHS has been reduced effectively as we expected and the thermal noise after passing through the CHS has also been weakly reduced.

Trade-offs can be considered in the CHS amplifier design. From the view of noise performance, it requires high modulating frequency. But higher frequencies introduce more residual offset. Thus the best compromise is that choose the modulating frequency around the noise corner frequency where thermal noise becomes the dominant noise.

In addition, the selection of quality factor Q of the BPF needs to be considered. In theory, high quality factor reduces the residual offset. However, the high Q leads to large tuning error in practice, thus result in a large residual offset. On the other hand, the bandwidth of CHS is inversely proportional to Q. Therefore, in practice, a value of Q around 4 or 5 has to be considered.

CHAPTER 4

LOW VOLTAGE OPERATION & ELEMENTARY CIRCUITS

4.1 Introduction

In the previous chapters, the theory analyses and design considerations of chopper stabilization amplifier (CHS) have been presented. This chapter addresses some issues of practical implementation of this low-noise analog front-end preamplifier.

In the bladder control system, the VMD (analog front-end) will be integrated with the central processor (CP) on one chip. Like most mixed-mode VLSI systems, more than 80% of the circuitry in the electronic implant are digital circuits. The digital circuits can benefit a lot by reducing supply voltage from viewpoint of the power consumption. Nowadays, from the perspective of compatibility, it is a tendency to adopt the same low level voltage as power supply of the analog part of the mixed signal system. However, reducing the supply voltage results in a few significant impacts on the analog circuits when their performance is required high. First, the dynamic range of signal is shrunk directly with reducing of the power supply. Second, the drain-source voltage drop V_{ds}, and transistor effective voltage V_{eff} both have to be lowered in accordance with the decreasing of the supply voltage, which result in the output impedance and the gain bandwidth are decreased. Third, to reduce the thermal noise of transistors, they need

carry a larger DC current, which is limited by the low supply too. Thus, the trade-off between low power-supply and the circuit performances should be considered carefully.

We will discuss the minimum voltage requirements of the system in the next section. Then some elementary circuits that are used extensively in the system will be presented in left parts.

4.2 Voltage requirements of analog circuits

For the analog amplification circuits that operate in class A mode, all the transistors connected between VDD and VSS must be in "on" state to carry the quiescent current. The gate-source voltage of each transistor requires larger than its threshold voltage in order to ensure the transistor being active. Moreover, the transistors in analog circuitry normally need to work in deep saturation region to realize amplification. These requirements are reflected in (4.1) and (4.2).

$$V_{eff} = V_{gs} - V_{th} \geq \Delta V \tag{4.1}$$

$$V_{ds} \geq V_{eff} + \Delta V \tag{4.2}$$

where V_{gs}, V_{ds}, V_{th} denotes gate-source, drain-source and threshold voltage of the transistors respectively. Here ΔV denotes a voltage safety margin to accommodate the possible deviation corresponding to the variation of the process and environment temperature.

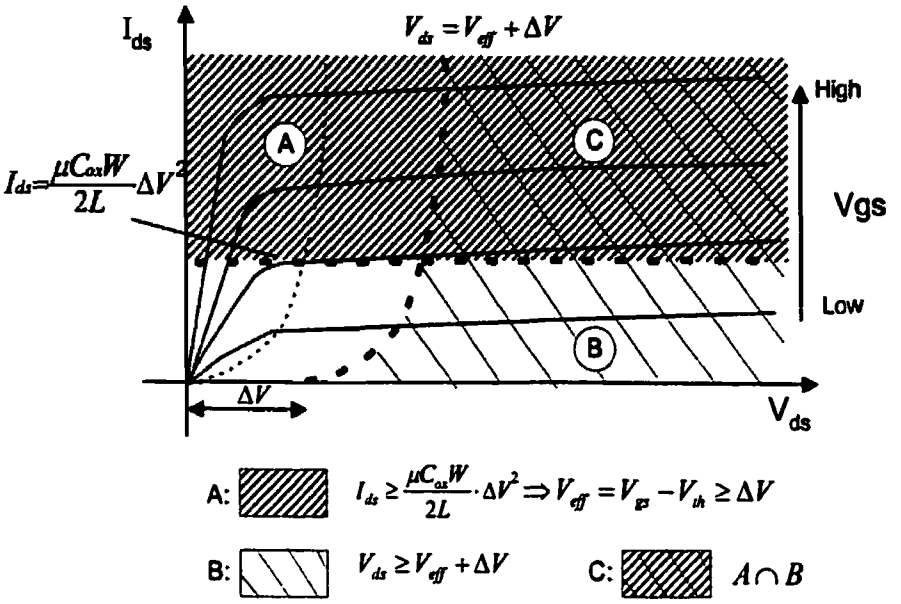


Figure 4.1 I-V characteristic of MOSFET transistor

As illustrated in figure 4.1, the transistor that operates in region C can bear a variation on both gate-source and drain-source voltages, thus ensure stable and robust operation of the transistor. The value of ΔV depends on the CMOS technology and the supply voltage. Corresponding with the 0.35μm technology which we used to implement this system, the typical value of ΔV is 100 mV, thus 200 mV is the minimum of V_{ds}.

To maximize the signal processing range in the low voltage supply, it is imperative to include a rail-to-rail input stage. Figure 4.2 illustrates voltage requirements of the design of the input stage. The common-mode input voltage range (CMR) of n-channel pairs is restricted as defined in equation (4.3)

$$V_{CMN} \geq V_{SS} + V_{gsn} + V_{dsn} \qquad (4.3)$$

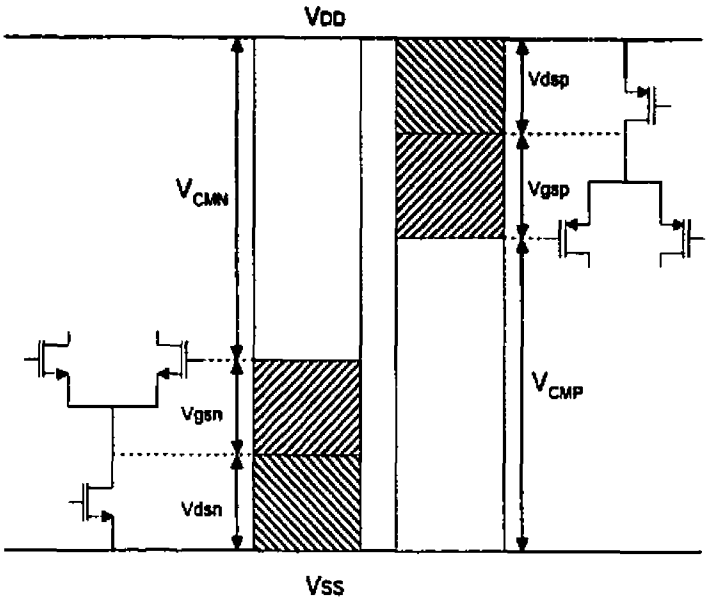


Figure 4.2 Common mode range of N-pair, P-pair

Similarly, the CMR of p-channel pairs is restricted to the range as

$$V_{CMP} \leq V_{DD} - V_{gsp} - V_{dsp} \tag{4.4}$$

To obtain a full rail-to-rail input range, we must combine both complementary stages and allow at least one of the stages to function. This requires

$$V_{CMP-\max} \geq V_{CMN-\min} \tag{4.5}$$

Substitute (4.3) and (4.4) into (4.5), we obtain

$$V_{DD} - V_{SS} \geq V_{gsp} + V_{thp} + V_{gsn} + V_{thn} = 2(V_{gs} + V_{ds}) \tag{4.6}$$

Formula (4.6) gives out the lowest limit to the supply voltage of the rail-to-rail input stages. The prototype chip of our system will be fabricated with a 0.35μm CMOS technology whose normal gate-source voltage can be down to 700 mV. Thus the power supply being specified in the system is

$$V_{DD} = 2(V_{gs} + V_{ds}) = 2(0.7 + 0.2) = 1.8V \quad (4.7)$$

Table 4.1 summarizes the specifications of the system design.

Table 4.1 Specifications of the system design.

Name	Value
Power supply	VDD = 1.8 V VSS = 0 V
General transistor length	Four times minimum length permitted by technology: 4×0.35μm = 1.4μm
Vds-sat	≥ 100m V
Vds	Double Vds-sat: ≥ 200mv

4.3 Basic circuits and functions

4.3.1 High swing current source/sink

The current source/sink is a basic block in CMOS IC design and is used extensively in analog integrated circuit design. Ideally, the output impedance of a current source/sink should be infinite and capable of generating or drawing a constant current over a wide range of voltage. Here, a kind of high swing current mirror is commonly used in the design.

Figure 4.3 presents the PMOS and NMOS current mirrors respectively. Their operation mechanism can be reviewed by the NMOS current mirror shown in part c) of figure 4.3. Suppose that all the transistors have good matching and equal W/L ratio, when they work under a deep saturation region, their drain current is written as:

$$I_D = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)(V_{gs} - V_{th})^2[1 + \lambda(V_{DS} - V_{eff})] \tag{4.8}$$

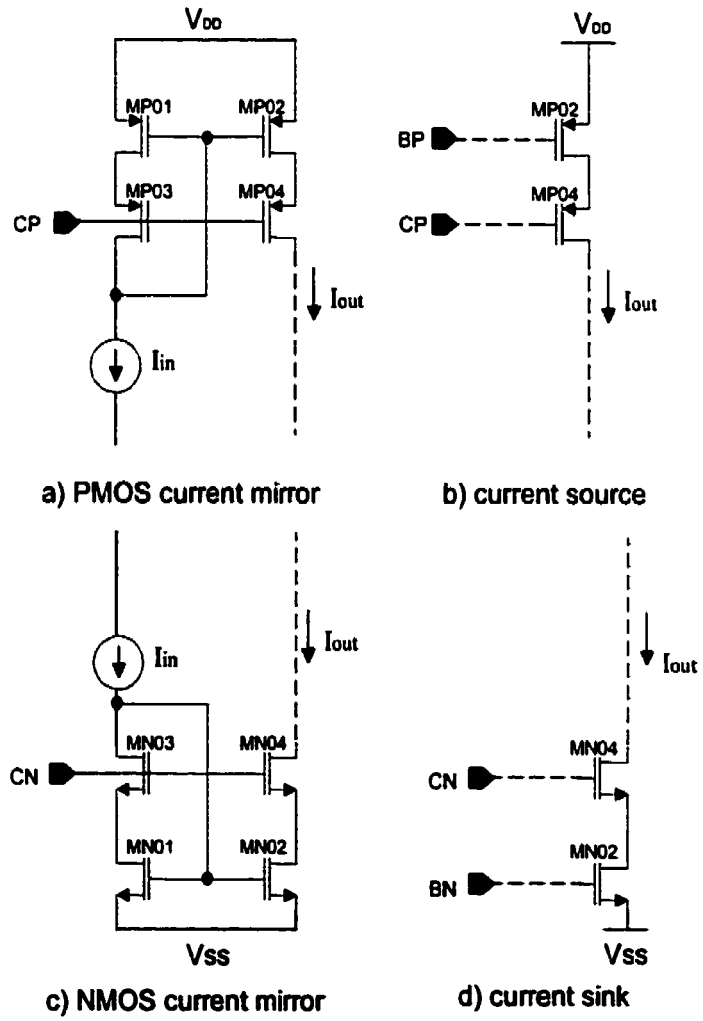


Figure 4.3 High swing current mirror

where the effective gate-source voltage (V_{eff}), is defined in equation 4.1. Note that the drain-source current of the transistor mainly depends on its gate-source voltage (V_{gs}). And the drain-source voltage V_{ds} has a second order effect with factor λ on the current. According to (4.8) we know that as long as their gate-source voltage V_{gs} and drain source voltage V_{ds} are equal, the two transistors MN01 and MN02 will carry exactly the equal current. The gate-to-source voltages of the two transistors have been forced equal by connecting their gates together. Furthermore, their drain-to-source voltages are approximately equal due to the appearance of transistors MN03 and MN04. Thus, the current mirror has very high precision. Note that the gate of MN01 is connected with the drain of MN03 rather than the drain of itself, the minimum dynamic voltage of the output can be down to $2V_{eff}$ rather than $V_{th}+2V_{eff}$ [35]. The output impedance and the output swing voltage the current mirror are summarized as:

$$Z_{out} = g_{m4} \cdot r_{ds4} \cdot r_{ds2} \tag{4.9}$$

$$V_{out-min} = V_{eff4} + V_{eff2} . \tag{4.10}$$

The label BN, CN, CP, BP in figure 4.3 represent the bias voltages of the circuit. And the labels will be used in all of the following chapters. They are generated by an on-chip bias circuit, which is described in the next section.

4.3.2 BIAS circuit design

As mentioned above, an on-chip bias circuit is needed to supply the biasing voltages to all the blocks of the system, which include a rail-to-rail amplifier, a 2nd BP filter, an oscillator and an instrumentation amplifier. Therefore, it is very important to make the

biasing circuit working stable. Figure 4.4 presents the biasing scheme of the prototype chip which eas adapted from [35].

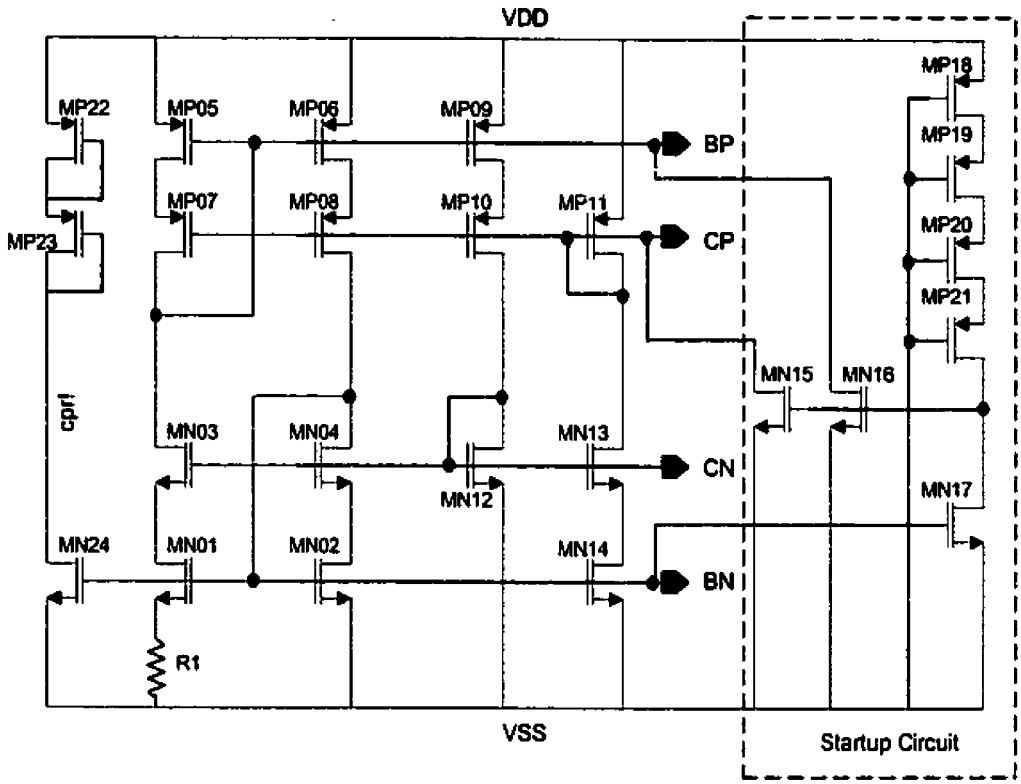


Figure 4.4 Schematic of biasing circuit

The main advantage of this biasing circuit is that it realizes a stabilized transconductance of each transistor. Assume the transistors MP05 and MP06 have the same ratio W/L, it results in both sides of the circuit having the same current due to the current mirror. The transconductance of transistor MN02 is given by:

$$g_{m2} = \frac{2(1-\sqrt{\frac{(W/L)_2}{(W/L)_1}})}{R_1} \tag{4.11}$$

Suppose the specified ratio, $(\frac{W}{L})_1 = 4(\frac{W}{L})_2$, is satisfied, we obtain

$$g_{m2} = \frac{1}{R_1}. \tag{4.12}$$

It demonstrates that the transconductance g_{m2} is determined by the resistor value R_1 only. It is independent of power-supply voltage, process and temperature variations. Note that not only g_{m2} but all other transconductances are stabilized, since currents of all transistor are derived from the same biasing network. Therefore, for all n-channel transistors, we have

$$g_{mi} = \sqrt{\frac{(W/L)_i I_{Di}}{(W/L)_2 I_{D2}}} \times g_{m2} \tag{4.13}$$

And for all p-channel transistors

$$g_{mi} = \sqrt{\frac{\mu_p (W/L)_i I_{Di}}{\mu_n (W/L)_2 I_{D2}}} \times g_{m2} \tag{4.14}$$

The high-swing cascade bias voltages are generated by transistors MN12 and MP11 respectively. It should be noted that the bias circuit can have a second stable state while all the currents are zero. To prevent this case, it is necessary to add a start-up circuit that is composed of transistors MN15~MP21 as presented in figure 4.4. The start-up module only affects the bias circuit when all currents in the loop are zero. In this case, MN17 is off. As the transistors MP18~MP21 operate as a high-impedance load that is always on, the gates of MN15 and MN16 are pulled high. These transistors then inject currents into the bias loop, which leads to the circuit to start up. Therefore MN17 becomes on, sinking all of the currents from MP18~MP21, pulling the gates of MN15 and MN16 low, and turning them off. Then, they will not affect the bias loop any more.

4.3.3 MOSFET switch

Analog switch is a basic component of the modulator. The high OFF-to-ON resistance ratio of MOSFET transistors makes them suitable for use in switching applications. As shown in figure 4.5, NMOS, PMOS and CMOS all can be used as switches. The largest voltage that an n-channel switch can pass is $V_{DD} - V_{thn}$, while the lowest voltage a p-channel switch can pass is V_{thp}. To obtain full rail-to-rail signal transmission, CMOS switch is one of the alternatives as long as the condition illustrated in equation (4.15) is satisfied.

$$V_{DD} > V_{thn} + V_{thp}. \qquad (4.15)$$

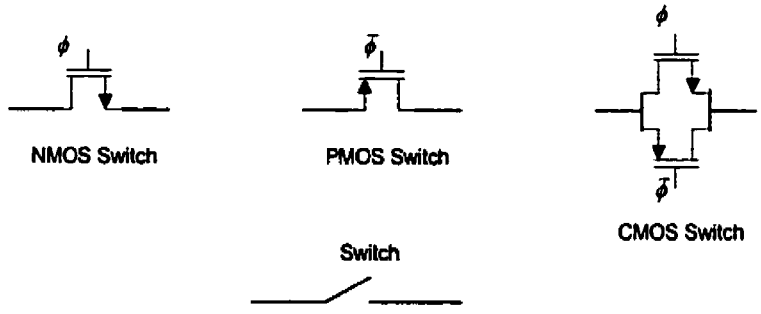


Figure 4.5 MOSFET switches

As discussed in 2.3.2, the charge injection, one of the non-ideal effects of MOS switches in input modulator, results in the residual offset at the output nodes of CHS amplifier. Therefore, the mechanism leading to charge injection in MOS switches and its minimization methods has to be analyzed. Figure 4.6 illustrates this charge injection phenomenon.

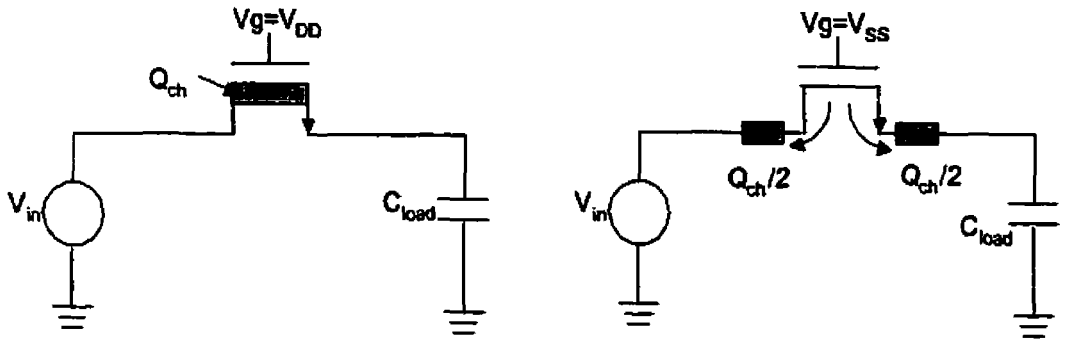


Figure 4.6 Charge in the NMOS transistor channel

- When MOS switch is on and its drain-source voltage V_{ds} is small, the charge under the gate oxide resulting from the inverted channel is approximated as:

$$Q_{ch} = C_{ox} \cdot W \cdot L \cdot (V_{GS} - V_{TH}) \tag{4.16}$$

- When the MOSFET turns off, this charge is injected onto the capacitor and into the voltage source V_{in}. Assume that V_{in} is a low-impedance source-driven node, the injected charge will have no effect on this node. However, the charge injected onto C_{load} results in a change in voltage across it. It has been shown, that if the clock signal turns off fast, the channel charge distributes fairly equally between the adjacent nodes [32]. Thus, half of the channel charge is distributed onto C_{load}. As the accumulated charge in n-channel and p-channel are electrons and holes respectively, the charge injection in n-channel and p-channel switch will result in negative and positive spikes correspondingly. Their amplitude, for instance in NMOS switch, can be calculated as:

$$\Delta V_{spike} = -\frac{Q}{C} = -\frac{C_{ox} \cdot W \cdot L \cdot (V_{GS} - V_{TH})}{2C_{load}} \tag{4.17}$$

Assume the clock swings is between V_{DD} and V_{SS}, we obtain

$$\Delta V_{spike} = -\frac{C_{ox} \cdot W \cdot L \cdot (V_{DD} - V_{in} - V_{TH})}{2C_{load}} \tag{4.18}$$

where V_{in} represents the input signal.

Substituting the threshold voltage expression into (4.18), yields

$$\Delta V_{spike} = -\frac{C_{ox} \cdot W \cdot L \cdot (V_{DD} - V_{in} - [V_{THN0} + \gamma(\sqrt{|2\phi_F| + V_{in} - V_{bulk}} - \sqrt{|2\phi_F|})]}{2C_{load}} \tag{4.19}$$

where V_{THN0} is the threshold voltage with zero V_{SB} (i.e. source-to-substrate voltage), γ denotes the body-effect constant and ϕ_F represents the electrostatic potential of substrate.

The equation (4.19) illustrates that the amplitude of spikes are dependent on the input signal V_{in} which is composed of common mode DC voltage V_{CM} and differential AC signal V_d, as

$$V_{in} = V_{CM} + v_d \tag{4.20}$$

In low amplitude signal applications, V_d is very small comparing with the amplitude of V_{CM} and ϕ_F. Therefore the distortion that is caused by charge injection can be neglected, however a significant residual offset should be considered as discussed in chapter 2.

One technique to reduce the charge injection error is to use a dummy switch as illustrated in figure 4.7. Here, a half size transistor with its drain and source shorted is placed in series with the desired switch M_1. When M_1 turns off, the dummy switch absorbs its

channel charge in output direction. Thus, the charge injection error can be cancelled to a first order [32].

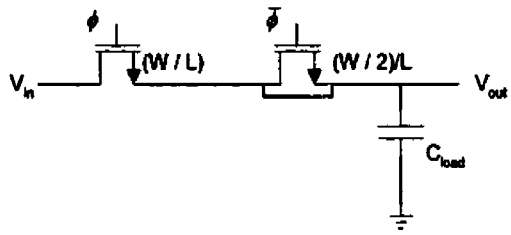


Figure 4.7 Charge injection cancellation using a half size dummy switch

Another technique is to use a CMOS switch where the n-channel transistor and p-channel transistor have the equal gate area size. According to (4.19), if the DC level of the input signal is exactly in the middle of rail-to-rail and the clocks supplying the two switches are fully complementary, the charge injections in n-channel and p-channel will be basically canceled by each other. However, the previous condition can not be satisfied in our case since the input common-mode voltage necessitates being able to vary from rail to rail. To realize a rail-to-rail modulator without depending on input signal level, a bootstrapped switch that is inspired from [30][31] can be used. The switch is conceptually a single NMOS transistor, as shown in figure 4.8.

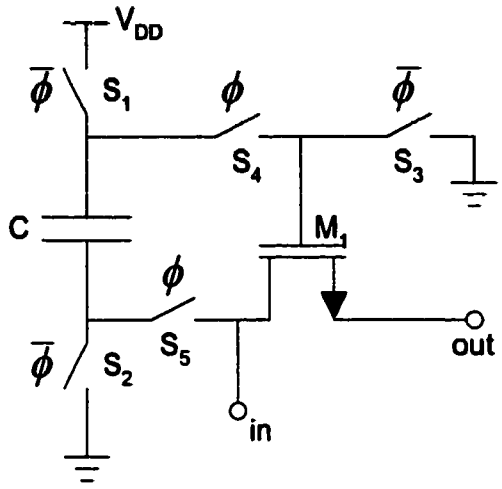


Figure 4.8 Bootstrapped MOS switch

- During the off phase, $\overline{\phi}$ is high. The switch S_3 discharges the gate of M_1 to ground. Meanwhile, V_{DD} is applied across capacitor C by the switches S_1 and S_2. And the switches S_4 and S_5 isolate the transistor M_1 from C while it is charging.

- In the ϕ phase, the switches S_1, S_2 and S_3 are off while the switches S_4, S_5 are on. The capacitor C whose voltage has been charged to V_{DD} on the previous phase behaves as a battery across the source-gate of the transistor M_1 during this phase. It turns on transistor M_1 and enables the gate of M_1 to track the input voltage shifted by V_{DD}, keeping the gate-source voltage unchanged regardless of the input signal. For example, if the input common mode voltage is at V_{DD} (1.8V), then the clock amplitude at the gate of M_1 will be up to $2V_{DD}$ (3.6V).

Comparing with the CMOS switches, the bootstrap switches have two advantages at the cost of more complexity. First, if the variation of the threshold voltage is ignored, the

charge injection of the switch is no more dependent on the input signal as well as the "on" resistance. Second, it is more suitable in low voltage applications since the power supply of system can be further down to 1V as long as it is higher than the threshold voltage of MOSFET transistors. Unlike the CMOS switches must satisfied the condition (4.15) to realize the rail-to-rail signal transmission.

4.3.4 Transconductor

A kind of linearity transconductor [22][35] that takes advantage of two triode region transistors as source degeneration resistor is commonly used in the continuous-time filter implementation. The schematic of transconductor is presented in figure 4.9. Its transconductance value is given by:

$$G_m = \frac{i_o}{v_1 - v_2} = \frac{1}{r_{s1} + r_{s2} + (r_{ds3} // r_{ds4})} \tag{4.21}$$

where r_{s1} represents the output impedance of transistor MP01 view from source terminal, $r_{s1} = \frac{1}{g_{m1}}$. The g_m of a saturated region transistor can be expressed as:

$$g_m = \sqrt{2\mu_p C_{ox}(W/L) I_D} \tag{4.22}$$

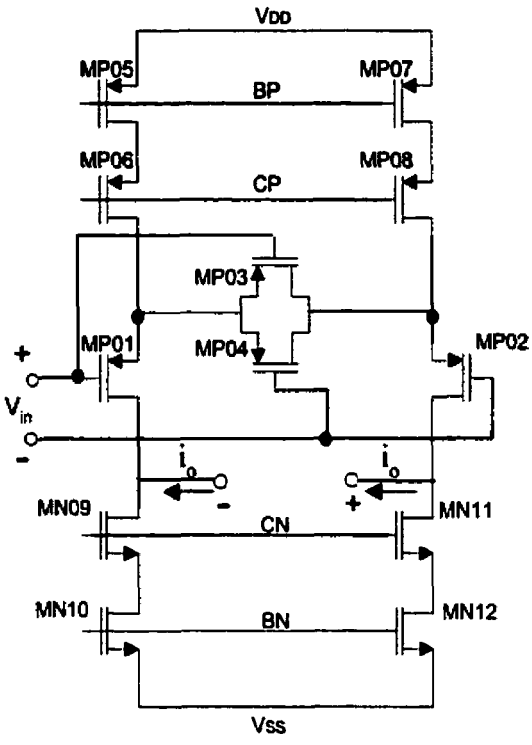


Figure 4.9 Linear transconductor circuit

And r_{ds3} denotes the conductance of transistor MP03 which works in triode region, $r_{ds3} = \frac{1}{g_{ds3}}$. The g_{ds} of a triode region transistor is given by:

$$g_{ds} = \mu_p C_{ox}(W/L)V_{eff} \tag{4.23}$$

Assume $g_{m1} = g_{m2}$ and $g_{ds3} = g_{ds4}$, the transconductance of the cell is written as

$$G_m = \frac{g_{m1}}{2} // 2g_{ds3} = \frac{4g_{m1} \cdot g_{ds3}}{g_{m1} + 4g_{ds3}}. \tag{4.24}$$

Note that varying bias conditions for the triode transistors further improve the linearity of the transconductor [35].

4.3.5 Common mode Feed-back (CMFB)

For the full differential signal circuitry, because of the increased symmetry, all common-mode signals and even-order distortions cancel out, except for the influence of component mismatches. It leads to lower distortion, higher common-mode rejection ratio (CMRR), and higher power supply rejection ratio (PSRR). However, as the signal is no longer referred to ground, the operating point of the circuitry cannot be stabilized with the differential feedback loop. A common-mode feedback loop (CMFB) is required to determine the output common-mode voltage and to control it to be equal to some specified voltage. Figure 4.10 shows the CMFB circuit that will be used in the rail-to-rail OTA, the 2nd BP filter and oscillator of the system. Transistors MP01 and MP04 sense the common mode voltage on the output nodes. Assume the common-mode signal which is higher than V_{CM} appeared, it results in both currents of transistors MP02 and MP03 increasing, then leads to the gate potential of the diode-connected MN13 increasing correspondingly. This voltage is feedback to control the current levels in the n-channel current sinks of the summing circuit in transconductor. Thus, both current sinks carried larger currents and bring the common mode voltage of output nodes back to value V_{CM}. The transistor MN11 makes use of the other sides of the differential pairs, which doubles the common mode gain of the circuit [35].

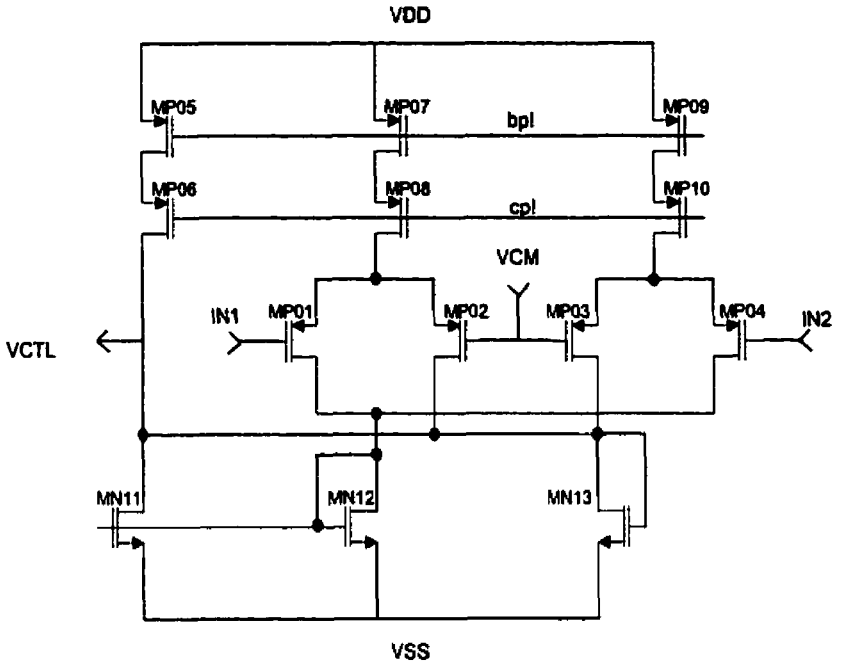


Figure 4.10 Common mode feedback circuit

4.4 Summary

This chapter mainly discussed the basic circuits which are commonly used to implement the analog front-end system. To be compatible with the digital circuit of the system, low voltage (1.8V) is adopted as the power supply of the analog circuit. The high swing current mirror and a stabled transconductance biasing circuit are used in the design. A bootstrapped switch is introduced to build the input modulator that can realize signal transmission from rail to rail. Source degenerated transconductor and common mode feedback (CMFB) are the basic components to form a continuous time filter and an oscillator.

CHAPTER 5

IMPLEMENTATION OF THE CHS MODULES

5.1 Introduction

The design aims at implementing a fully integrated system-on-chip (SOC) structure. Figure 5.1 illustrates the block diagram of the proposed topology, which includes two gain blocks: a CHS amplifier to reduce the low-frequency noise and DC offset, and an instrumentation amplifier (IA) to obtain a programmable gain and high common mode rejection ratio (CMRR). The system also involves other peripheral circuits, such as an on-chip bias circuit, a clock generator and an output low-pass filter.

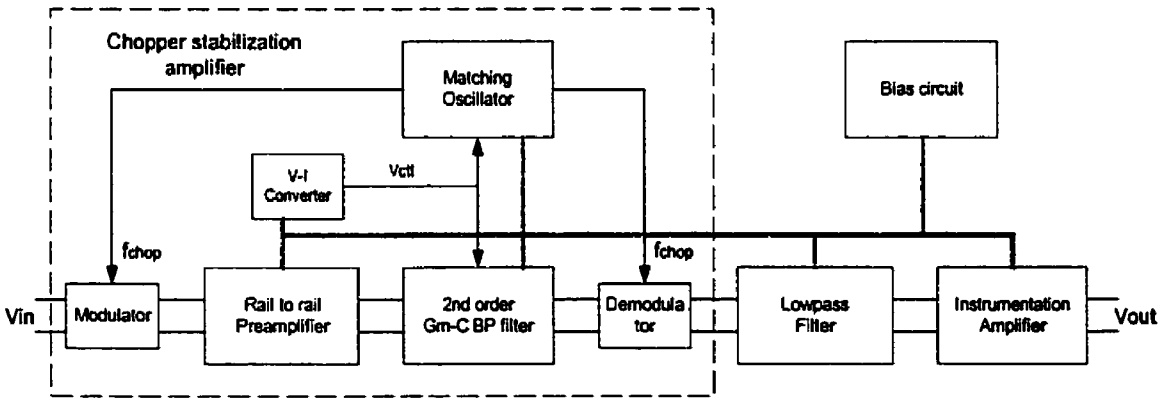


Figure 5.1 The block scheme of the analog front-end preamplifier

In the next section, the dominant noise source in a cascade amplifier system is analyzed. The rest parts of this chapter analyzes in detail the proposed circuit configuration.

5.2 Noise in Cascaded Stages

In the case that an amplifier is constituted by several stages, their noise performance can be analyzed with the model illustrated in figure 5.2. The Power Spectral Density (PSD) of the total input referred noise due to each stage is given by:

$$S_N(f) = \sum_{i=1}^{N} \frac{S_{N_i}(f)}{\prod_{k=1}^{i-1} |A_k(f)|^2} \tag{5.1}$$

When $|A_1(f)|^2 >> 1$, the expression (5.1) reduces to the first stage noise PSD $S_{N_1}(f)$. It implies that in the system, the main noise contribution is due to the input stage. The improvement of the amplifier noise performance is therefore reduced to the optimization of its input stage.

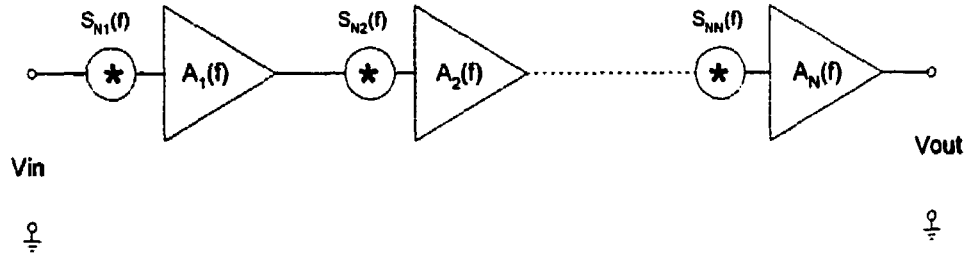


Figure 5.2 Noise sources of a cascade stage amplifier

5.3 Modulators

5.3.1 Circuit implementation

The basic idea of CHS is using modulation technique to reduce 1/f noise and DC offset. Thus the input modulator will be a critical part in the design of the CHS amplifier. The function of modulator is illustrated in figure 5.3.

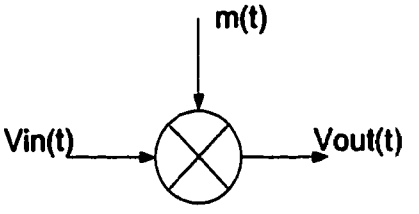


Figure 5.3 Modulator function block

$$V_{out}(t) = V_{in}(t) \cdot m(t) \tag{5.2}$$

The modulate signal m(t) is a square wave signal as presented in figure 2.8. The expression (5.2) can be rewritten as a discrete form

$$V_{out}(t) = \begin{cases} V_{in}(t) & \text{kT} < t < kT + \dfrac{T}{2} \\ -V_{in}(t) & \text{kT} + \dfrac{T}{2} < t < (k+1)T \end{cases} \qquad \text{k=1,2,.....}\infty \tag{5.3}$$

This function can be realized with four cross-coupled analog switches that are controlled by two non-overlap clocks having frequency (1/T), as shown in figure 5.4. The switch pairs S_1- S_3, S_2-S_4 transmit the signal in turn and reverse the sign during each half period so as to realize signal modulation.

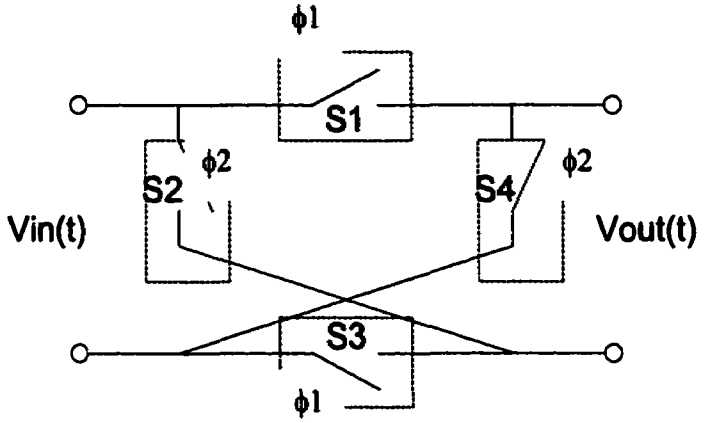


Figure 5.4 Modulator based on four switches

The input modulator needs the bootstrap switch introduced in the preceding chapter, to remove the effects caused by the varying common mode input voltage. The actual bootstrap switch is presented in figure A.2. Note that the two switches pair S_1-S_3 or S_2-S_4 (figure 5.4) can share one bootstrapped circuit respectively since their clock phases are exactly the same. As for the ultra-low-amplitude signal applications, the input AC signal is too small comparing with the clock signal, it will not result in the signal distortion or additional variation of charge injection. Furthermore, the dummy switch method is needed to minimize the residual charge injection.

5.3.2 Clock signals of Modulator

Four clock phases are needed to operate of the modulator: two non-overlap clocks ϕ_1, ϕ_2, and their complementary clocks $\overline{\phi}_1$, $\overline{\phi}_2$, which are shown in figure 5.5. To guarantee the modulator work normally, the clocks need satisfy the two requirements:

- The clock ϕ_1 and ϕ_2 can not be high simultaneously.
- When ϕ_1 is high, $\overline{\phi}_2$ can not be low.

The first one is satisfied as long as the two clocks are non-overlapped. The second condition requires the delay between two complementary clocks to be smaller than the propagation delay between two non-overlap clocks. The propagation delay is determined by the inverter chains in the non-overlap clock generator circuit, as shown in figure 5.6. The high performance complementary clocks can be obtained by a pseudo differential clock driver circuit as shown in figure A.17.

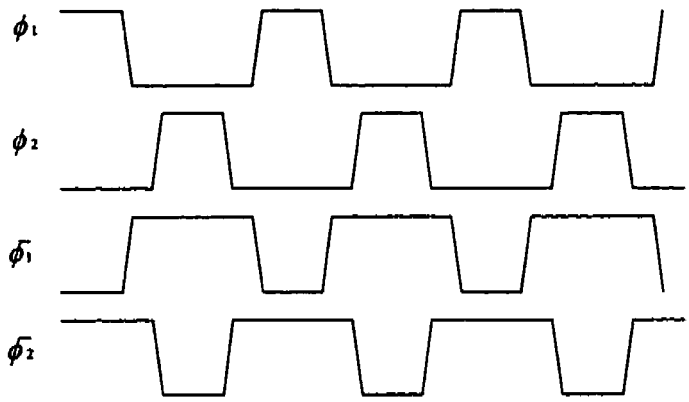


Figure 5.5 Clocks in the modulator

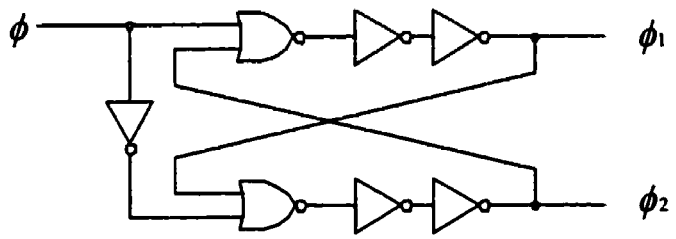


Figure 5.6 Non-overlap clock generator

5.3.3 Noise in Modulator

As the input modulator is the first block to process the weak input signal directly, its noise contribution needs to be minimized. From the previous analysis, the switches being

in "on" state can be thought as a resistor. Thus the thermal noise of switch can be modeled as a voltage source, $V_R(f)$, in series with a noiseless resistor, as shown in figure 5.7. With such an approach, the spectral density function, $V_R^2(f)$, is given by

$$V_R^2(f) = 4kTr_{ds} \tag{5.4}$$

where k is Boltzmann's constant, T is the temperature in Kelvins, and r_{ds} is the transistor drain and source resistance.

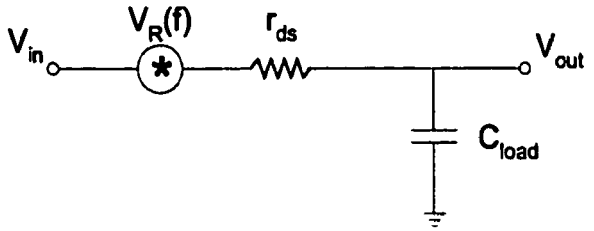


Figure 5.7 Noise model of the MOS switch in "on" state

As the transistor is in triode region, its drain-source resistance can be written as

$$r_{ds} = \frac{1}{\mu_n C_{OX}(W/L)(V_{gs} - V_{th})} \tag{5.5}$$

To reduce thermal noise, the resistance needs to be lowered through increasing the width-length ratio or the effective voltage of the transistor. Thanks to the usage of bootstrapped switch, the effective voltage (V_{gs}-V_{th}) has been maximized to (V_{DD}-V_{th}). Note that according to (5.4), a 1-kΩ resistor exhibits a root spectral density of 4.06 $nV/\sqrt{Hz}$ in thermal noise at room temperature (300K). The root spectral density is proportional to the square root of the resistance, we can also write

$$V_R(f) = \sqrt{\frac{r_{ds}}{1k}} \times 4.06nV/\sqrt{Hz} \qquad \text{for } 27°C \tag{5.6}$$

Normally, r_{ds} is smaller than 10K Ω. Thus the thermal noise exhibited in MOS switch is smaller than $12\,nV/\sqrt{Hz}$.

5.3.4 Demodulator

The structure of the demodulator is similar to the modulator one. However, as the input DC voltage of the demodulator can be fixed at a specified voltage, a simple NMOS switch instead of the bootstrapped switch can be used in the demodulator. And the same control clocks can be used in the demodulator as long as there is no phase shift introduced by the previous selective amplifier. The noise performance and charge injection of the demodulator are no longer critical to the system design, because the signal has been amplified much more and shifted back to the baseband.

5.4 Selective Amplifier

Note that the selective amplifier of the CHS presented in figure 5.1 is realized by two amplifiers, a wide-band low-noise rail-to-rail preamplifier followed by a 2nd order bandpass filter. The analysis and results based on equation (3.6) is still valid for the two stages selective amplifier. Since their transfer function can be expressed as follows:

$$G(f) = \frac{A_1}{1 + j\frac{f}{f_{c1}}} \times \frac{A_2 \times Q}{1 + jQ\frac{f^2 - f_{c2}^2}{f \cdot f_{c2}}} \tag{5.7}$$

where f_{c1}, f_{c2} are the cut-off frequencies of the two stages respectively. As f_{c1} is much larger than f_{c2}, in the range $f \ll f_{c2}$, the equation (5.7) can be rewritten as

$$G(f) = A_1 \cdot \frac{A_2 \times Q}{1 + jQ\dfrac{f^2 - f_{c2}^2}{f \cdot f_{c2}}} \tag{5.8}$$

There are two advantages of this kind of structure: First, a wide common mode input range can be obtained by means of a rail-to-rail OTA as the input stage, and the noise optimization can be limited in this stage only. Second, as the DC gain of CHS amplifier has been divided into two stages, the input transconductance of the BP filter does not need to be high. Thus, the compensation circuit, which is needed to reduce the offset stems from the high g_m input pair [29], can be removed.

5.4.1 Low noise preamplifier

The low-noise preamplifier consists of a rail-to-rail OTA followed by a transimpedance stage as shown in figure 5.8. The DC gain of this amplifier equals to G_{m1}/G_{m2}, where G_{m1} and G_{m2} are the transconductances of the two blocks respectively. The bandwidth of the amplifier should be high enough comparing with chopper frequency to ensure that little gain and phase distortion will be introduced to the system.

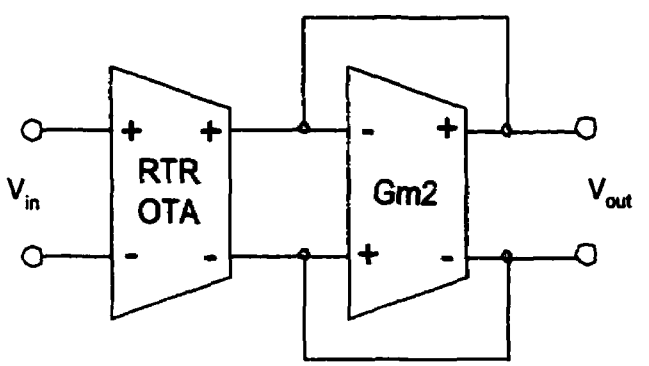


Figure 5.8 Block scheme of the preamplifier

5.4.1.1 Rail to Rail OTA

The input operational transconductor amplifier (OTA) transfers the voltage signal to a current level, which can be realized by conventional source-coupled pair. As discussed in section 4.2, to obtain the maximum dynamic range at low supply voltage, it is necessary to use a rail-to-rail input stage. As shown in figure 5.9, this can be implemented by placing N- and P-type differential pairs (MN01, MN02, MP03, and MP04) in parallel.

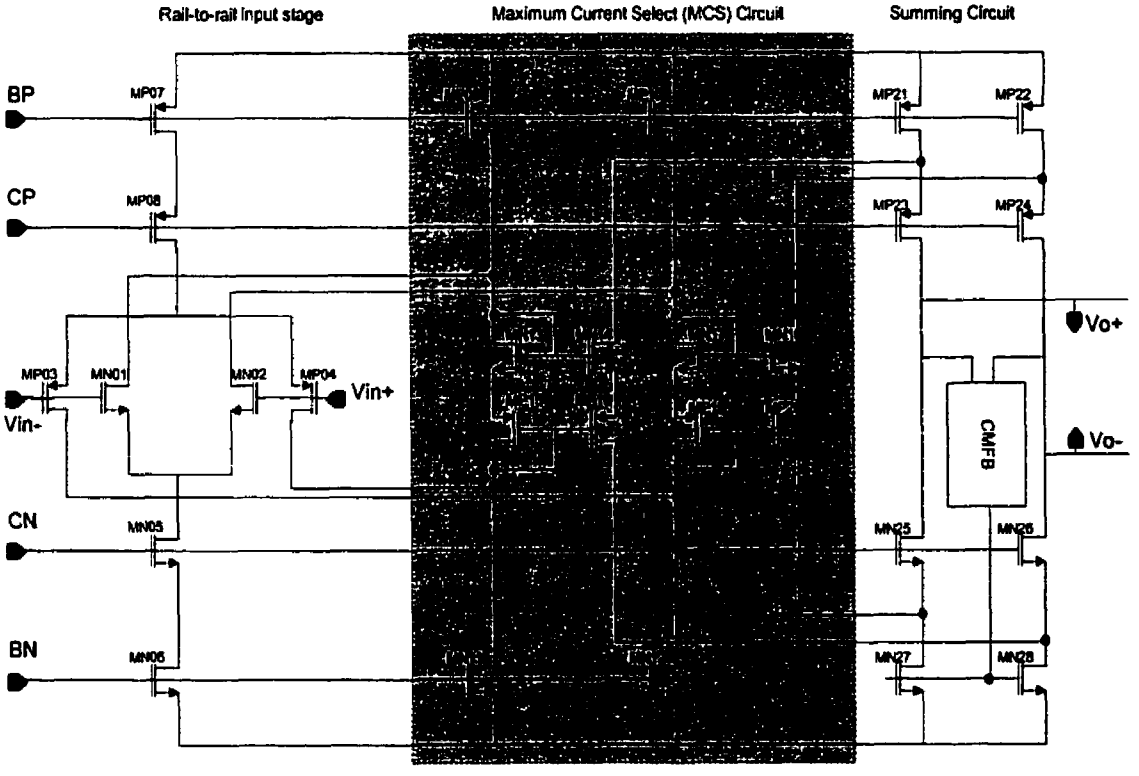


Figure 5.9 Rail-to-rail Operational Transconductor Amplifier (OTA)

Varying with the common mode voltage, three different operation areas can be distinguished, as shown in figure 5.10:

- Region I: The CMR is near the negative supply rail: signal transfer will take place only by the P-type differential pair.
- Region II: The CMR is in a region somewhere in the middle between the supply voltages; both the NMOS and PMOS differential pairs will be active.
- Region III: The CMR is near the positive supply rail: signal transfer will take place only by the N-type differential pair.

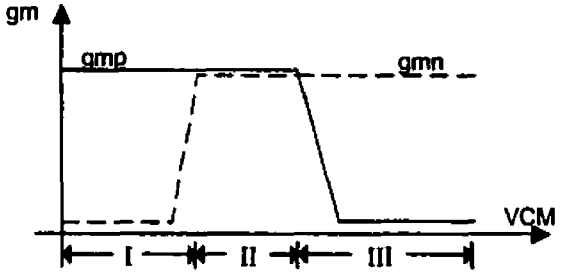


Figure 5.10 Gm of three regions

The transconductance (g_m) of both N and P pairs strongly depends on the common-mode input level because only in a region somewhere in the middle of the supply voltage will both differential pairs be active. Also the fully differential circuits necessitate to use a common mode feedback circuit (CMFB) at the output node of the OTA, which should fix the output node quiescent voltage. The CMFB circuit, through adjusting the gate-source voltage of transistors MN27 and MN28, controls the output node DC point. Thus in order to ensure the MN27 and MN28 working in saturation region, their carrying DC current should remain constant. In other words, the DC current that flows into the summing circuit of rail to rail OTA should be stable regardless of varying of the common mode input voltage.

The constant g_m value is obtained by two maximum current select (MCS) circuits, as shown in figure 5.9. Among them, the transistors MP09 (MP10) and MN11 (MN12), act as a current source or sink to supply a DC current to two floating current mirrors which composed by transistors MN13 ~ MN14 (MN17 ~ MN18) and MP15 ~ MP16 (MP19 ~ MP20).

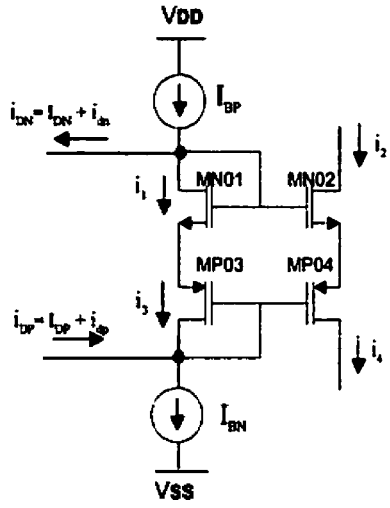


Figure 5.11 Maximum current select circuit.

The principle of the MSC is illustrated in figure 5.11. The input currents are represented by i_{DN} and i_{DP}, which come from the input N-pairs and P-pairs respectively. Suppose the common mode input voltage is near the negative rail, locating in the region I, where P-pair is on and N-pair is off. Their currents are expressed as

$$i_{DN} = I_{DN} + i_{dn} \approx 0 \tag{5.9}$$

$$i_{DP} = I_{DP} + i_{dp} = \frac{I_D}{2} + g_{mp} \cdot V_{id}, \tag{5.10}$$

According to the kirchhoff current law, at the node A and B, as shown in figure 5.11.

$$i_1 = I_{BP} - i_{DN} \approx I_{BP} \tag{5.11}$$

$$i_3 = I_{BN} - i_{DP} = I_{BN} - (\frac{I_D}{2} + g_{mp} \cdot V_{id}) \tag{5.12}$$

Apparently, i_1 must be equal i_3, thus leads to $I_{BP} \approx I_{BN} - (\frac{I_D}{2} + g_{mp} \cdot V_{id})$. However, I_{BP} is supposed to be equal I_{BN}. That means one of the two current sources will work as a load, it does not act as a constant current source or a current sink any more.

It can be explained by the I-V characteristic of a MOS transistor as shown in figure 5.12. Because the gate-source voltage of the two transistors are fixed, the drain current i_{ds} of the transistor can only move toward a smaller value when the transistor has worked in the saturation region. In this case the transistors MP09 an MP10 will lose their saturation status. Their operation points move from point A to point B. The MCS output current is given by:

$$i_{O1} = i_2 = i_4 = I_{BN} - (\frac{I_D}{2} + g_{mp} \cdot \frac{V_{id}}{2}) \tag{5.13}$$

Same situation happened at the other MCS. Its output current is

$$i_{O2} = I_{BN} - (\frac{I_D}{2} - g_{mp} \cdot \frac{V_{id}}{2}) \tag{5.14}$$

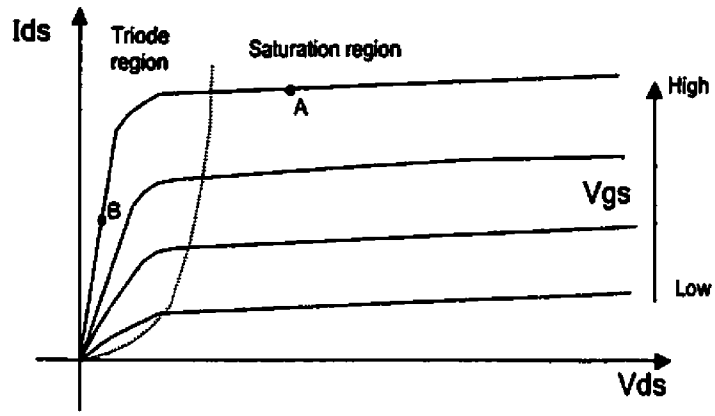


Figure 5.12 I-V characteristic of MOS transistor

Thereby the output g_m value of OTA in this case is obtained by

$$G_m = \frac{i_o}{V_{id}} = \frac{i_{o1} - i_{o2}}{V_{id}} = g_{mp}. \tag{5.15}$$

Similarly in the region II and III, the two different input currents will cause one of the current sources lost saturation. The OTA output current can be expressed as

$$i_o = i_{o1} - i_{o2} = g_{mn}(g_{mp}) \times V_{id} \tag{5.16}$$

In summary, the MCS circuit compares the two input currents, and outputs the maximum one. Provided that the g_{mn} and g_{mp} are tuned at the same value, the g_m value of OTA will be universal constant, as shown in figure 5.10. It should be noticed that no matter in which region the input pairs is located, the output DC bias current magnitude flows from the drain of transistor MN14, MP16, MN18 and MP20 will be always equal $I_B - \frac{I_D}{2}$. Thus the variation of CMR will not result in the change of the DC operation point of summing circuit.

5.4.1.2 Transimpedance

The transimpedance block is built by a negative feedback transconductor, as shown in figure 5.8. The transconductor can make use of the linear one introduced in 4.3. Its impedance equals $Z = \frac{1}{G_m}$.

5.4.1.3 Noise Analysis

Because there is no gain stage before the rail-to-rail preamplifier except one modulator, as discussed above, the system input referred noise is mainly determined by the noise of the preamplifier. Using figure 5.13, where all the transistors have been modeled with an equivalent voltage noise source, we can optimize the noise performance of the preamplifier. Provided that all noise sources are not correlated, the noise sources can be analyzed separately, then using superposition to calculate the overall noise. For more clarity, figure 5.13 shows N- input pair transistors only. The analysis of P-pair input stage would be similar to the N-pair counterpart.

- *Noises in input pair MN01 and MN02*

  As the noise sources of these two transistors (V_{n1} and V_{n2}) are connected in series with input signal, the gain of V_{n1} and V_{n2} is the same as the gain of the signal, which is

$$\frac{V_{no}}{V_{n1}} = g_{m1} Z_0 \qquad (5.17)$$

where V_{no} represents the output noise correspond the noise source V_{nI}. Z_0 represents the output impedance of the amplifier.

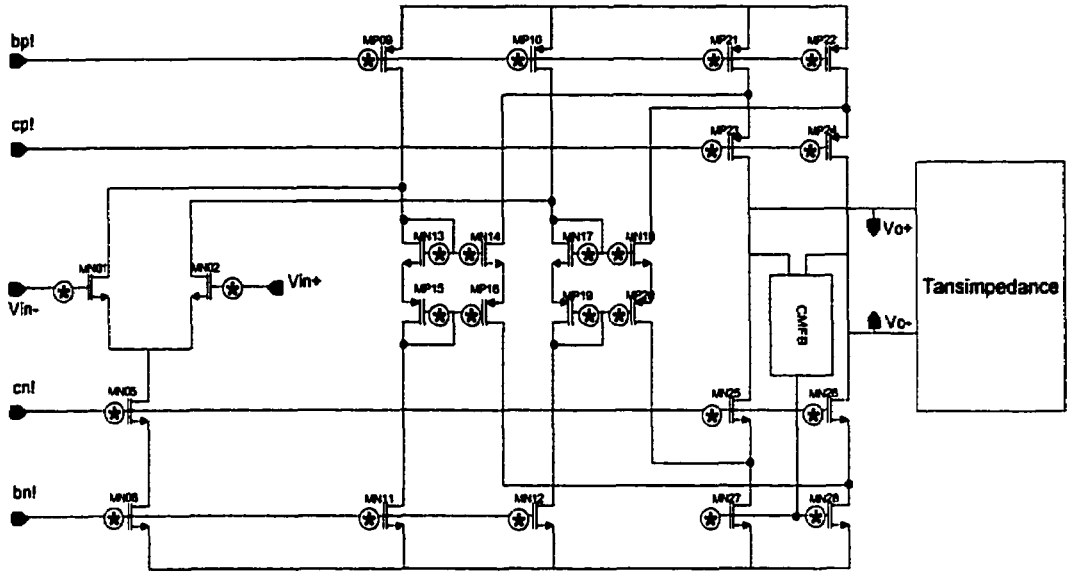


Figure 5.13 Noise model of the rail-to-rail OTA

- *Noises in current source MN05 and MN06*

  The noise sources in the gate of MN06 result in a noise drain source current $i_{dsn} = g_{m6} \cdot V_{n6}$. This current is divided into the two input transistors MN01 and MN02. Due to the symmetry in the circuit, this noise acts as a common mode voltage and is rejected by the high CMRR of the amplifier. Thus the noises can be ignored in that it is relatively very small compared to the others.

- *Noises in the cascade transistors (from MP23 to MN26)*

The noises of these transistors cause little variation of their drain currents since their source voltage potential varies simultaneously.

- *Noise in other transistors*

  The noises of these transistors introduces a noise current to the signal path. Hence, their noise gain at output node respectively is

  $\frac{V_{no}}{V_{ni}} = g_{mi}Z_0$, where g_{mi} is the transconductance value of each transistors.

The equivalent input referred noise can be obtained by

$$V_{neq} = \frac{V_{no}}{A_D} = \frac{\sum g_{mi} \cdot Z_0}{g_{m1} \cdot Z_0} = \sum \frac{g_{mi}}{g_{m1}} \qquad (5.18)$$

where A_D denotes the signal gain of the amplifier.

Apart from the OTA, the transimpedance and the common mode feedback circuit (CMFB) are also responsible for the noise contribution. Their noise analysis is similar to above analysis. From that, we know the noise performance of the preamplifier is dominated by several critical transistors in the circuit. To reduce their noise, two aspects should be considered. First, it is needed to enlarge their dimension both on width and length to lower their 1/f noise. Only when the 1/f noise is decreased, the corner frequency can be as small as we expected, for instance 10 kHz. Second, since the output noise of CHS will be eventually dominated by the thermal noise, it is need to reduce their thermal noise by increasing their carrying DC current and transconductance.

5.4.2 Second order BP filter design

The second stage of the selective amplifier is a 2nd order (biquad) band-pass gm-C filter. As discussed in chapter 2 and chapter 3, the filter is aimed at reducing the residual offset stems from the charge injection of the input modulator. The basic building block of gm-C filter is an integrator involving a transconductor and a capacitor. The block scheme of a fully differential 2nd order band-pass filter is presented in figure 5.14:

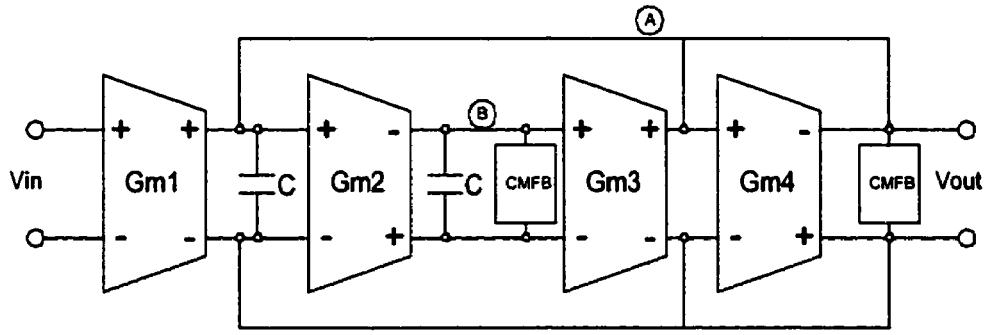


Figure 5.14 Block scheme of the biquad filter

The input transconductor G_{m1} converts input signal from voltage to current mode. Transconductors G_{m2} and G_{m3} constitute resonant stage which determines the center frequency of the filter. And transconductor G_{m4} is responsible for converting back the signal from current to voltage mode. The small signal model of the filter is presented in figure 5.15, where C_1, C_2 represent the parasitic capacitors of the two nodes.

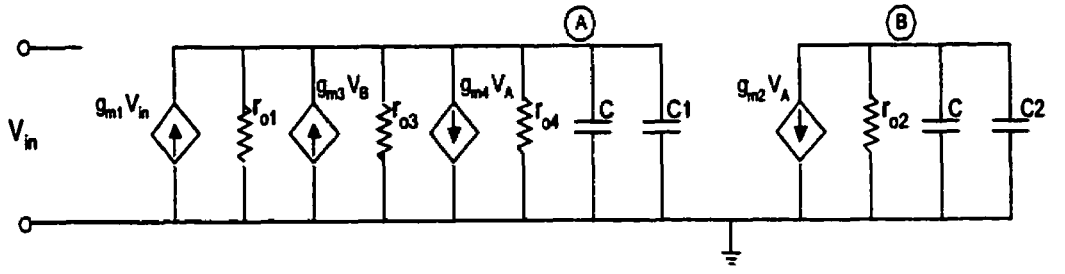


Figure 5.15 Small signal model of the filter

Nodes A, B represent filter's band-pass and low-pass outputs respectively. Their voltages can be expressed as

$$V_A = (g_{m1}V_{in} + g_{m3}V_B - g_{m4}V_A) \cdot \frac{1}{(s(C+C_1) + g_{o1} + g_{o3} + g_{o4})} \tag{5.19}$$

$$V_B = -g_{m2}V_A \cdot \frac{1}{(s(C+C_2) + g_{o2})} \tag{5.20}$$

where g_{oi} represents the output impedance of each transconductor.

From (5.19) and (5.20), the bandpass output transfer function can be found by:

$$A(s) = \frac{V_A}{V_{in}} = \frac{g_{m1}(sC_B + g_{o2})}{s^2 C_A C_B + s(C_A g_{o2} + C_B g_{m4} + C_B g_o') + g_{m3}g_{m2} + g_{m4}g_{o2} + g_o' g_{o2}} \tag{5.21}$$

where $C_A = C + C_1$, $C_B = C + C_2$ and $g_o' = g_{o1} + g_{o3} + g_{o4}$

Its zero and poles can be expressed as

$$z_1 = -\frac{g_{o2}}{C_B} \tag{5.22}$$

$$p_1, p_2 = -\frac{C_A g_{o2} + C_B(g_{m4} + g_o')}{2C_A C_B} \pm \frac{\sqrt{(C_A g_{o2} + C_B(g_{m4} + g_o'))^2 - 4C_A C_B(g_{m3}g_{m2} + g_{m4}g_{o2} + g_o' g_{o2})}}{2C_A C_B} \tag{5.23}$$

Equation (5.22) illustrates that an additional zero due to the finite output impedance of transconductor G_{m2} appears. However, it will not cause significant effects on the operation of the bandpass filter as long as it is much smaller than the center frequency of the filter. Suppose the integrator's capacitor C is much larger than the parasitic capacitors and two identical transconductors are used in the resonant stage, i.e. $g_{m2} = g_{m3} = g_m$, the equation (5.23) can be simplified as

$$p_1, p_2 = -\frac{g_{m4}}{2C} \pm \frac{\sqrt{g_{m4}^{\ 2} - 4(g_m^{\ 2} + g_{m4}g_{o2})}}{2C} \tag{5.24}$$

Figure 5.16 shows the poles and zero of the filter in the *s* plane.

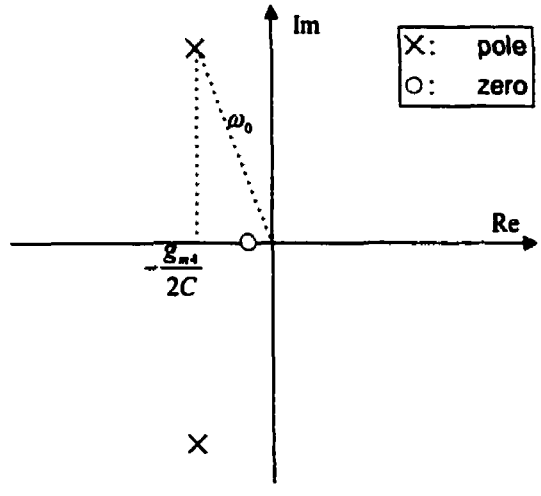


Figure 5.16 Poles and zero of the 2nd order BPF

Ignoring the additional zero, equation (5.21) can be rewritten as a standard biquad form

$$A(s) = \frac{A_0\omega_0 s}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{5.25}$$

where $\omega_0 \approx \sqrt{\frac{g_m^{\ 2} + g_{m4}g_{o2}}{C^2}}$ is the resonance frequency of the filter,

$Q = \frac{g_m}{g_{m4}}$ denotes the quality factor,

$A_0 = \frac{g_{m1}}{g_m}$ denotes the gain of the filter.

Note that the finite impedance of transconductor G_{m2} not only causes an additional zero, but also increases the resonant frequency of the filter. In addition, the choice of quality factor Q value has been discussed in chapter 3. Considering the tuning problem in practice, this value can be selected around 4 and 5. Transconductor and common mode feedback (CMFB) have been presented in (4.3). Their detailed schematics are given in Appendix A.

5.5 Automatic tuning & Matching Oscillator

Due to the lack of virtual grounds and low impedance nodes, the g_m-C filters are sensitive to the parasitic capacitors. The time constants of the filter depend on g_m/C ratios. These time constants are not well controlled in CMOS technologies because they are affected by the process parameter tolerances. These tolerances can be more than 30% if temperature variations, parasitic capacitors, bulk and other effects are included [36]. In addition to these aspects, the active filters are sensitive to the OTA finite parameters, e.g. parasitic poles and zeros and finite dc gain. The variations of g_m/C ratio can be corrected using a Phase Locked Loop (PLL). Usually there are two approaches, PLL based on voltage controlled filter (VCF) and PLL based on voltage controlled oscillator (VCO), to

build an on-chip automatic tuning circuit. The principles of the two techniques are briefly illustrated in figure 5.17.

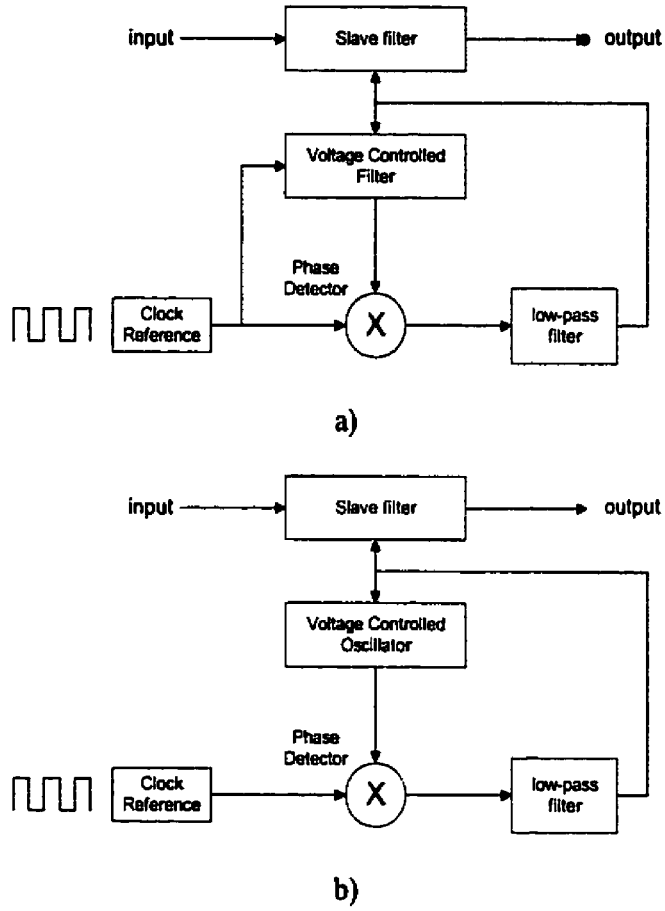


Figure 5.17 Automatic tuning techniques of the filter design based on

a) VCF b)VCO

In the PLL using a VCF technique, the voltage controlled filter is a replica of a section of the slave filter. The phase of the reference clock is compared with that of the VCF by the phase detector. The phase error is filtered out by the low-pass filter and fed back so as to adjust the transconductance of the OTAs involved in the master filter. Ideally, the loop is

locked when the phase of the band-pass filter output signal is equal to the phase of the reference signal.

In the PLL using a VCO technique, the important parameter is the frequency comparison instead of the phase comparison. Both the reference frequency and the oscillating frequency are compared by the phase detector. Similarly, the error voltage is filtered out by the low-pass filter and fed back to control the transconductance of the OTA. Under locked condition, the oscillating frequency of the VCO is tracked to the clock frequency.

Note that both techniques require an external reference clock and are based on the VCO or VCF being well matched with the slave filter. However, for the CHS amplifier, the deviation of modulating clock f_{chop} itself will not introduce significant impact on the performance of CHS. The critical point of tuning in CHS is to make the center frequency of BP filter tracking with f_{chop}, without affecting by process variation and environment temperature, rather than lock it with a reference clock. Hence, we can use an on-chip oscillator, as shown in figure 5.18, which is matched with the BP filter as the chopper clock generator.

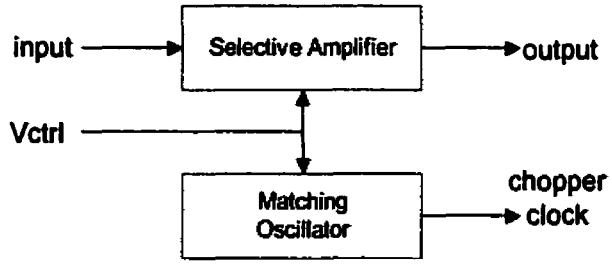
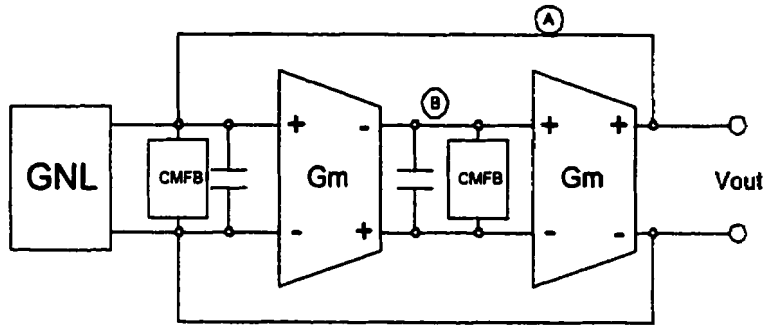
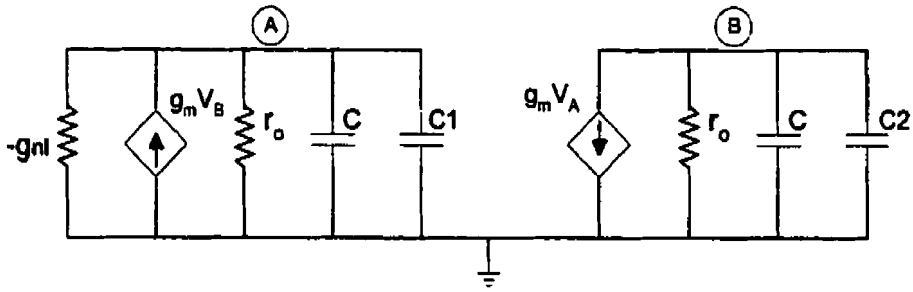


Figure 5.18 Matching oscillator to track with filter

The exactly same resonator structure is used in both parts. This structure will reduce the complexity of whole system, especially in this application, the chopper clock should be generated on chip. The proposed oscillator is shown in figure 5.19 a). The GNL block represents a nonlinear negative transconductor to ensure the oscillation and regulate the signal amplitude.



(a)



(b)

Figure 5.19 On-chip oscillator a) block scheme

b) Small signal model of the oscillator

The small signal model of the oscillator is illustrated in figure 5.19 b). Two node voltages can be written in:

$$\begin{cases} V_A = g_m V_B \cdot \dfrac{1}{sC_A + g_o - g_{nl}} \\ V_B = -g_m V_A \cdot \dfrac{1}{sC_B + g_o} \end{cases} \tag{5.26}$$

where g_o represents the output impedance of the transconductor, C_A and C_B represent the node capacitors which include the integrator capacitor C and the parasitic capacitors. Solving (5.26), the oscillation output can be expressed as

$$V_{out} = V_A = -g_m{}^2 V_{out} \cdot \frac{1}{(SC_A + g_o - g_{nl}) \cdot (SC_B + g_o)} \tag{5.27}$$

Rearranging (5.27), we obtain

$$V_{out} = \frac{s^2 C_A C_B + s(C_A g_o + C_B(g_o - g_{nl})) + g_o(g_o - g_{nl})}{s^2 C_A C_B + s(C_A g_o + C_B(g_o - g_{nl})) + g_o(g_o - g_{nl}) + g_m{}^2} \Delta V \tag{5.28}$$

where ΔV represents any deviation appeared in the signal path, which will cause the oscillation.

Their poles can be found in

$$p_1, p_2 = -\frac{C_A g_o + C_B(g_o - g_{nl})}{2C_A C_B} \pm j \cdot \frac{\sqrt{4C_A C_B(g_m^2 + g_o(g_o - g_{nl})) - (C_A g_o + C_B(g_o - g_{nl}))^2}}{2C_A C_B} \tag{5.29}$$

Ignoring the parasitic capacitors, and suppose that

$$C_A = C_B = C \tag{5.30}$$

Substitute (5.30) to (5.29), and omit the second order term of g_o

$$p_1, p_2 = -\frac{(2g_o - g_{nl})}{2C} \pm j \cdot \frac{\sqrt{C^2(4g_m^2 + 4g_o(g_o - g_{nl}) - (2g_o - g_{nl})^2)}}{2C^2} \tag{5.31}$$

$$= -\frac{(2g_o - g_{nl})}{2C} \pm j \cdot \frac{\sqrt{(4g_m^2 - g_{nl}^{\ 2})}}{2C} \tag{5.32}$$

Figure 5.20 illustrates the poles of the oscillator in the *s* plane. To ensure the oscillation, the poles should be located on the right half plane (RHP), which requires the following condition.

$$-\frac{(2g_o - g_{nl})}{C} \geq 0 \quad \Rightarrow \quad g_{nl} \geq 2g_o \tag{5.33}$$

And, the oscillator frequency can be found by

$$\omega = \frac{\sqrt{(g_m^2 - (\frac{g_{nl}}{2})^2)}}{C} \tag{5.34}$$

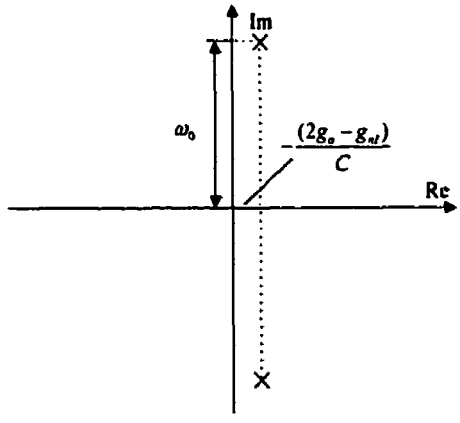


Figure 5.20 Poles of the oscillator

Note that the negative transconductance block inherently decreases the oscillator frequency from the desired value. To reduce the error, the value of g_{nl} should be as small as possible. For instance, if the error is required smaller than 1%, then

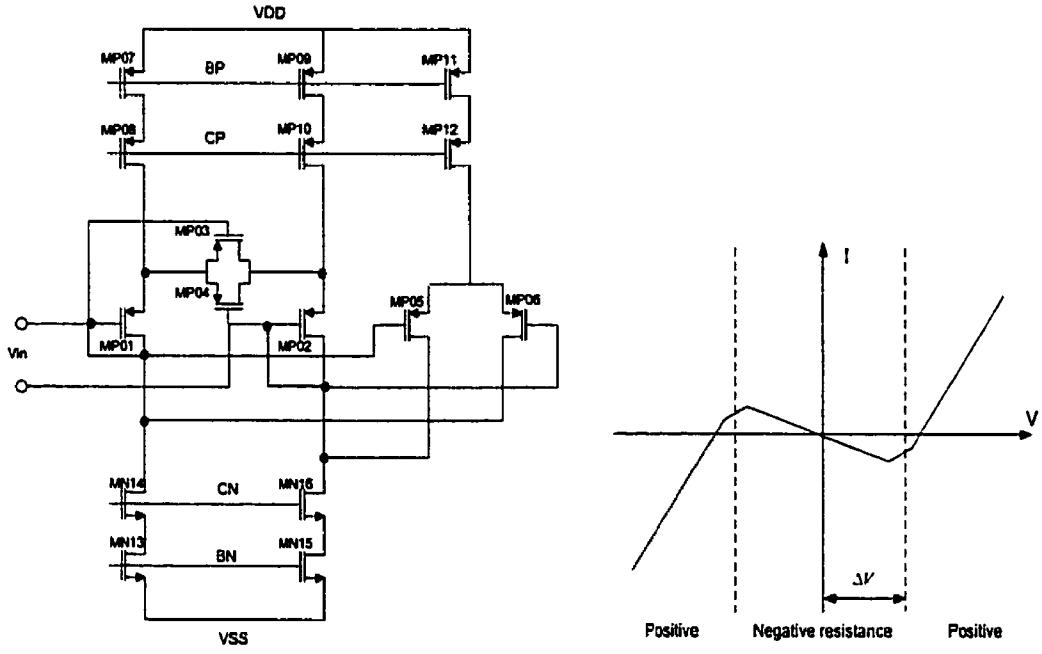
$$\omega = \sqrt{\frac{(g_m^2 - (\frac{g_{nl}}{2})^2)}{C}} > 0.99\frac{g_m}{C} \tag{5.35}$$

Solving it, we obtain

$$g_{nl} < 0.282 \cdot g_m \tag{5.36}$$

Thus, combine the condition (5.33), the g_{nl} should satisfy

$$2g_o \le g_{nl} < 0.282 \cdot g_m \tag{5.37}$$



a) b)

Figure 5.21 Non-linear transconductor (GNL) block a) schematic

b) I-V transfer characteristic

Figure 5.21 shows the actual implementation of the nonlinear conductance g_{nl} used for amplitude regulation in the two-integrator oscillator. To obtain the desired nonlinear characteristic, the cross-coupled MOS differential pair MP05 and MP06, is added to a linear transconductance stage connected in unity gain. For small signals, this circuit is equivalent to a negative conductance, as shown in figure 5.21 b). It will therefore ensure

oscillations build up when connected to the two-integrator loop which behaves like a passive LC resonant circuit. The amplitude of the oscillations increases until the current flowing through the nonlinear conductance GNL has no more components at the resonant frequency f_{chop} of the two-integrator loop [22]. A stable oscillation amplitude is obtained.

5.6 Summary

The chapter has presented the implementation of a chopper amplifier for low-frequency instrumentation applications. And a low noise preamplifier with rail-to-rail input stage is used as the first gain block in order to obtain the maximum common mode input range. To optimize the signal-to-offset gain, a 2^{nd} order band-pass filter based on the continuous-time filtering technique is chosen as the second stage of the selective amplifier. The modulating clock signal is generated by an on-chip oscillator tracking with the 2^{nd} order bandpass filter. Like in any other fully differential structure, a common mode stabilization circuitry must be included at each high impedance node to fix its DC potential to the desired value. The instrumentation amplifier and the low pass filter which further processed output signal of CHS are briefly explained in the Appendix D. A novel instrumentation amplifier based on current mirror approach instead of conventional resistor matching three-opamp IA has been adopted. It improves the common mode rejection ratio (CMRR) without requiring on-chip trimming.

CHAPTER 6

SIMULATION RESULTS AND EXPERIMENTAL PROTOTYPE

The proposed analog front-end preamplifier system has been implemented in 0.35 μm N-well technology. Appendix A illustrates the detailed schematic of each block. The circuits are simulated and analyzed by means of simulator HSPICE. The netlist files are attached in Appendix B.

6.1 Simulation Results

Bias & Operation point

As mentioned in chapter 4, having stable bias voltages in the circuit is one of the key factors to guarantee the success of the system. Figure 6.1 shows the simulation result of the biasing circuit. First, the start-up circuit inject the currents to the current mirror loop, make the biasing work. Then after around 100 ns, the biasing voltages were stable. The operation region of each transistor can be clarified by checking their drain-source voltage and effective voltage in the AC simulation HSPICE output file. Normally, all the transistors in the circuit should be in deep saturation region except the inverters and other digital cells. The power consumption of total system is 775 μW (This does not includes the switching power consumption of the modulators) .

Input Modulator

Figure 6.2 presents the bootstrapped clocks corresponding to two cases of common mode input voltages (0V, 1.8V) respectively. It illustrates that the 'high' state of the clock while the input voltage is at 1.8V can be up to approximately 3.5 V. The bottom curve shows the differential modulated signal. There are little spikes appearing. It is because that the spikes have been cancelled by the full differential mode. However, the mismatching of the transistors in reality will cause the spikes. The charge injection of the switch is reflected by the spikes appearing on the single-end signal as shown in figure 6.3. The magnitude is around 1.5 mV with 1p F capacitive load. The input referred noise spectrum of the modulator is 8.7 $nV/\sqrt{Hz}$ which is mainly contributed by the "on" resistors of MOS switch.

Low Noise Amplifier

Figure 6.4 shows the simulation result of the input range and g_m values of the rail-to-rail amplifier. The X-axis represents the common mode input voltage, the curve at the top illustrates the DC gain correspond it. The bottom curve illustrates the gm values of input P-channel and N-channel transistors respectively. It demonstrates that the input range is from 0 to 1.8 V and the variation of DC gain from rail to rail is limited in 5%, which is better than the performance of the conventional rail-to-rail amplifier. The frequency response of the amplifier is illustrated in figure 6.5. The DC gain equals to 26 dB and the –3 dB frequency is around 1.2 MHz, much larger than the center frequency f_{chop} (47 kHz in our case) of the bandpass filter.

Bandpass filter & Oscillator

Limited by the requirement of tuning and bandwidth, quality factor Q of the bandpass filter, which is determined by the transconductance ratio of G_{m2} and G_{m4}, is selected around 4. The center frequency is chosen around 50 kHz in order to guarantee it is larger than the noise corner frequency and ensure the signal having 5 kHz bandwidth. The figure 6.6 illustrates the simulation result of the magnitude and phase spectrum of the filter. The gain of center frequency equals 25 dB. Note that due to the finite output impedance of G_{m2}, an additional zero appears at low frequency (100 Hz).

The figure 6.7 presents the modulator clock signal generated by the matching oscillator. The clock frequency is around 47 kHz. The error between this frequency and the center frequency is around 6% due to the appearance of GNL block. The I-V transfer characteristic of GNL block is illustrated in figure 6.8.

For CHS simulation, a voltage source has been added between input modulator and amplifier to simulate the 1/f noise and DC offset of op-amp. The input signal, noise sources and output of CHS are presented in figure 6.9. From the simulation result, we see that the output signal is amplified and free from both 1/f noise and DC offset. Though the amplitude of noise is at the same order of signal. The simulated overall system input referred noise spectrum is 45 $nV/\sqrt{Hz}$. The characteristics of the system can be summarised in table 6.1.

Table 6.1 Simulation results of the proposed analog front-end

Characteristics	Simulation results
Power Supply	VDD = 1.8V,VSS = 0
Input range	0 ~ 1.8 V
Constant Gm	< 5%
Clock frequency	47 kHz
Signal bandwidth	< 5K Hz
DC Gain(not include the IA)	51 dB
CMRR	180 dB @ 1 KHz
PSRR	VDD: 92 dB @ 1 KHz
	VSS: 83 dB @ 1 KHz
Input referred noise	45 nV/$\sqrt{Hz}$
Input referred DC offset	< 1 μV
Total Harmonic Distortion (THD)	0.023% @ Vin=10μV
Power consumption (static)	775 μW

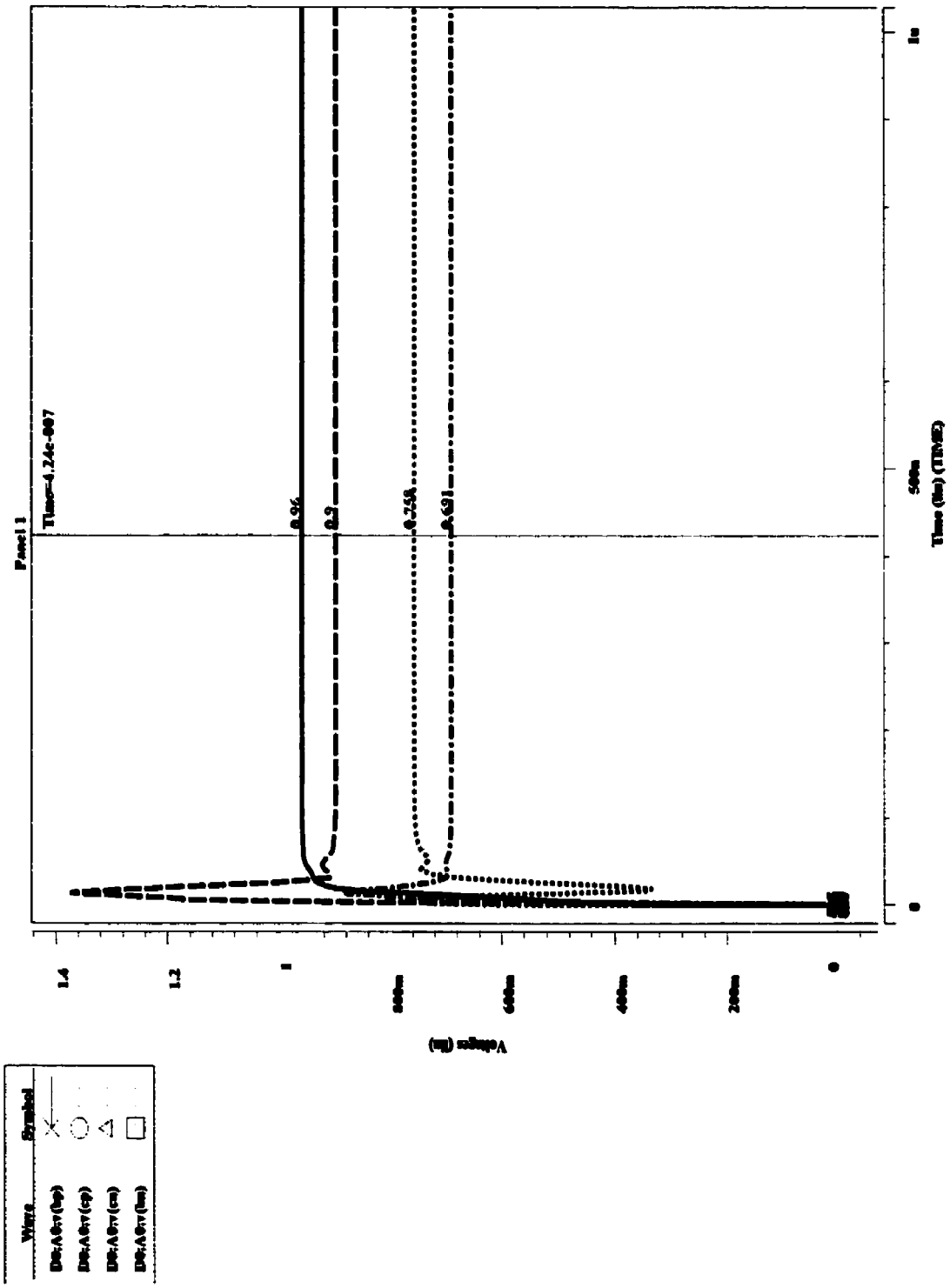


Figure 6.1 Bias Voltages

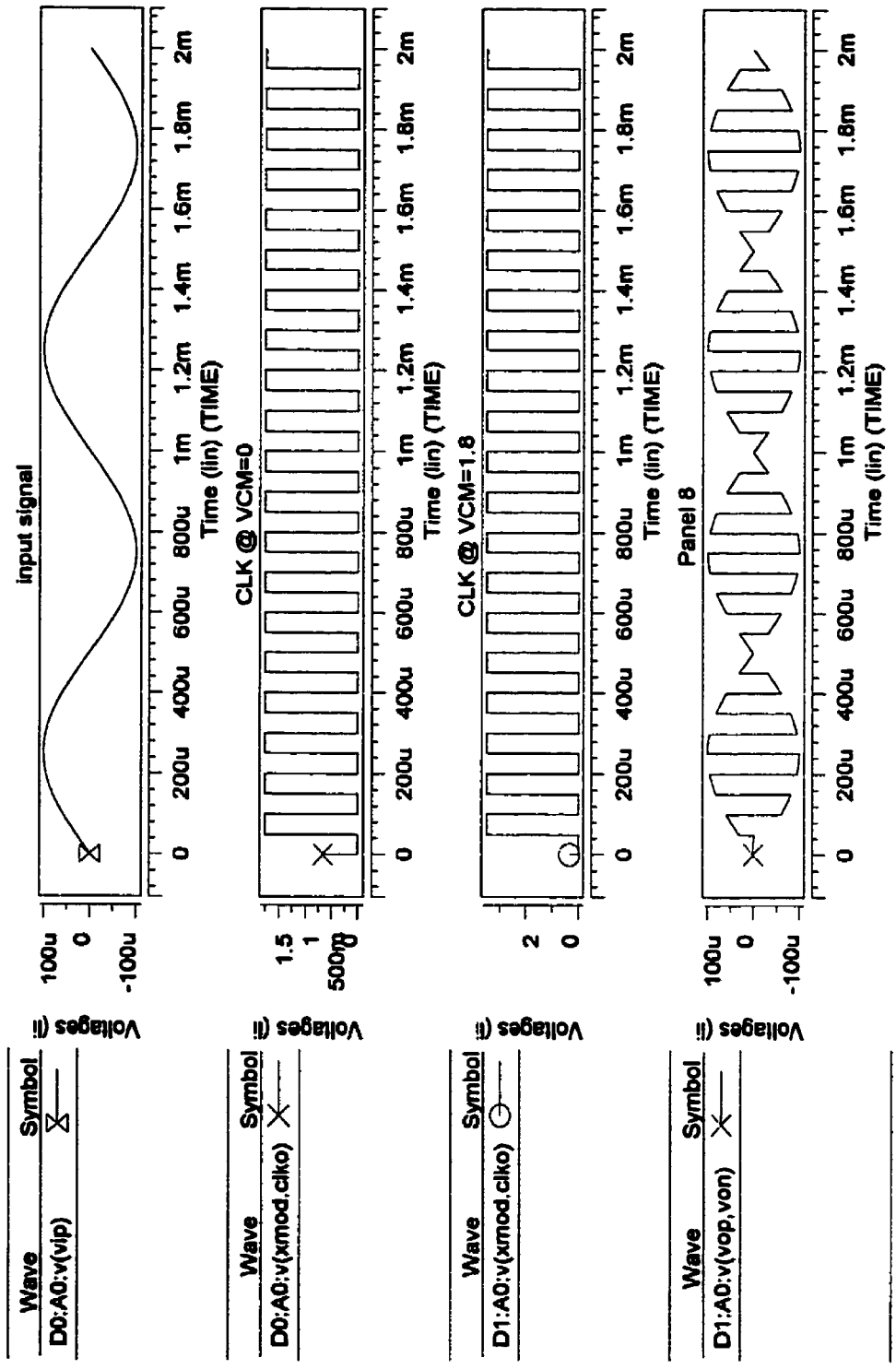


Figure 6.2 Input Modulator Simulation Result (1)

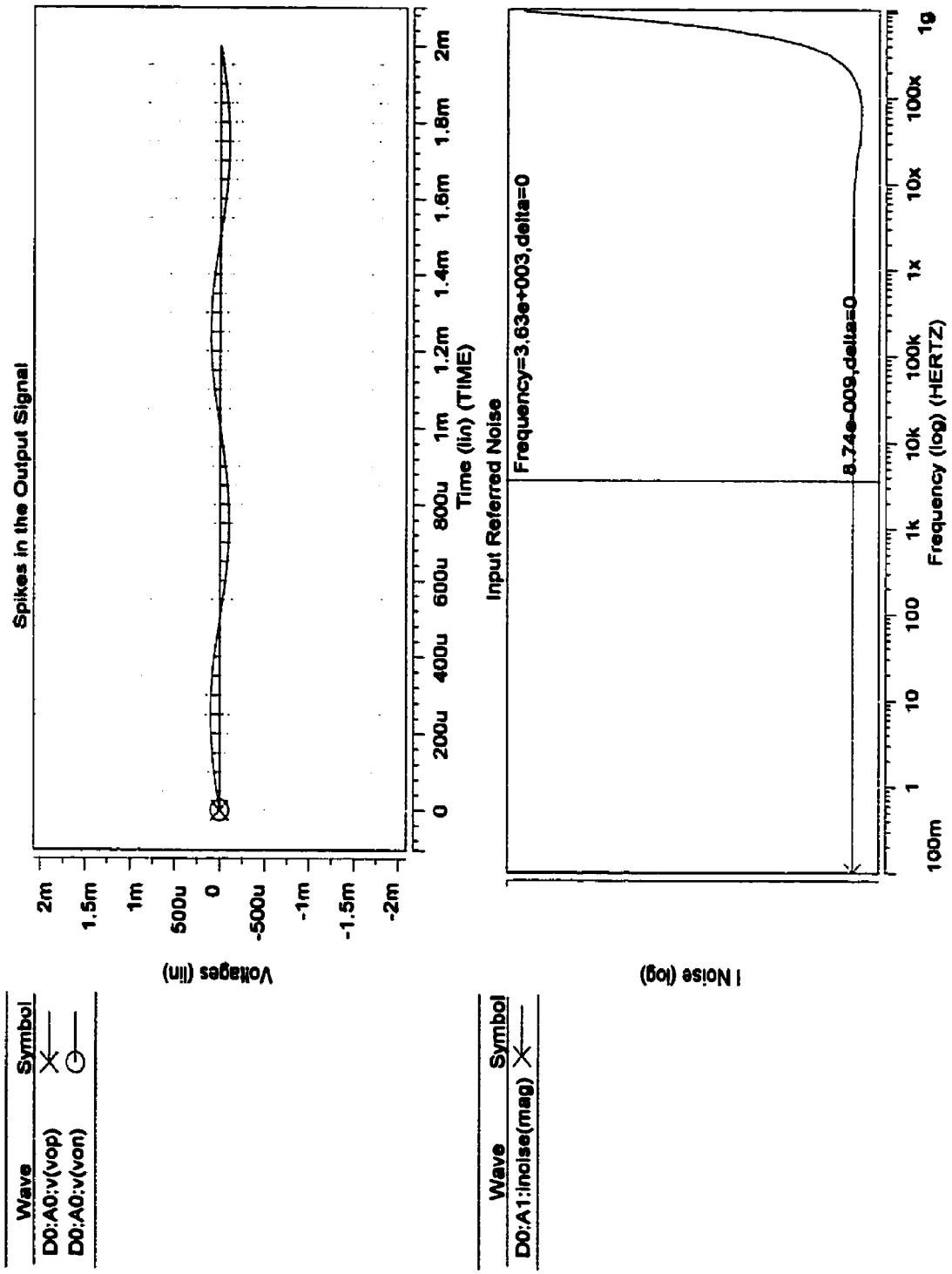


Figure 6.3 Input Modulator Simulation Result (2)

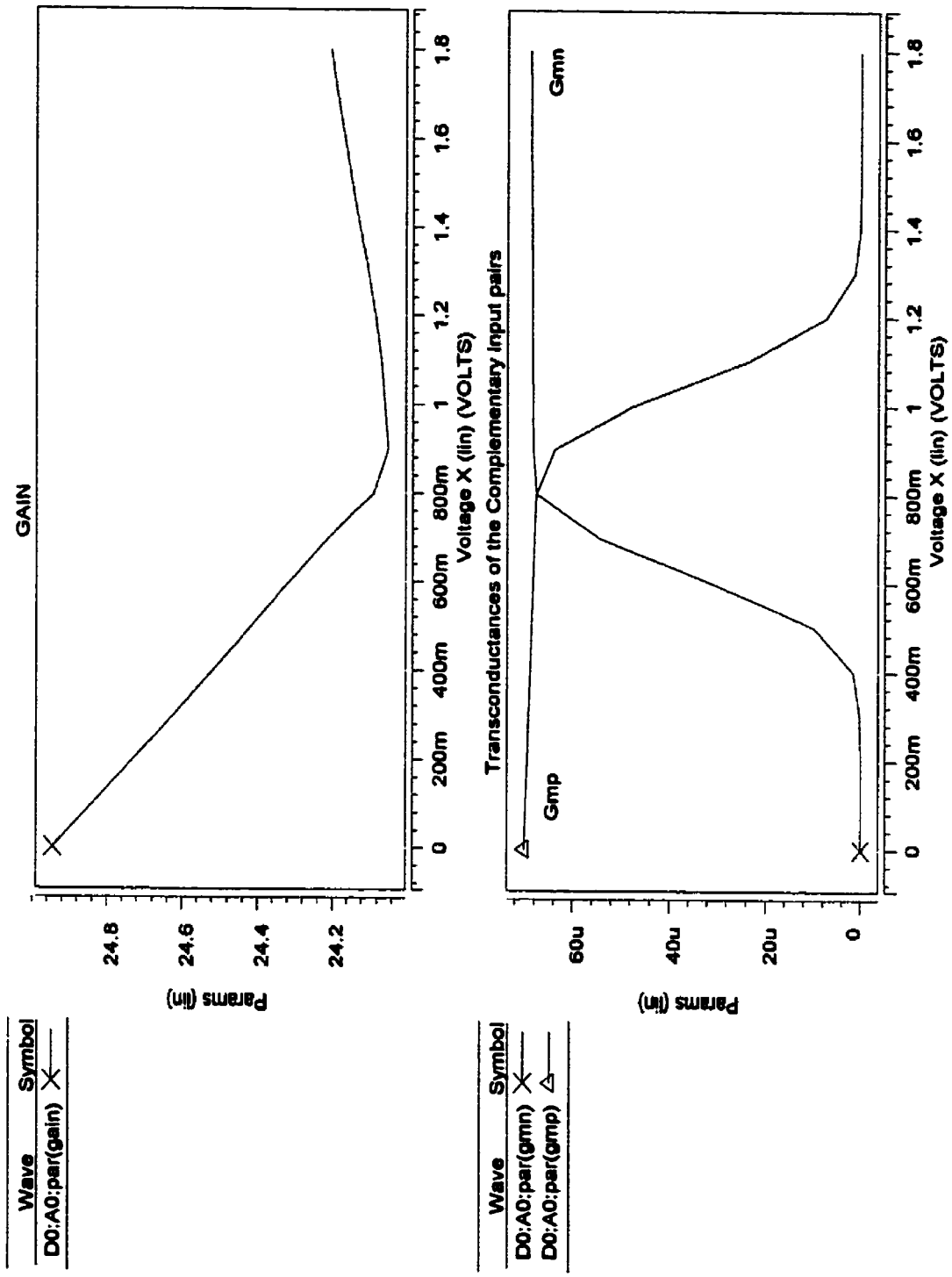


Figure 6.4 Constant Gm of the rail-to-rail OTA

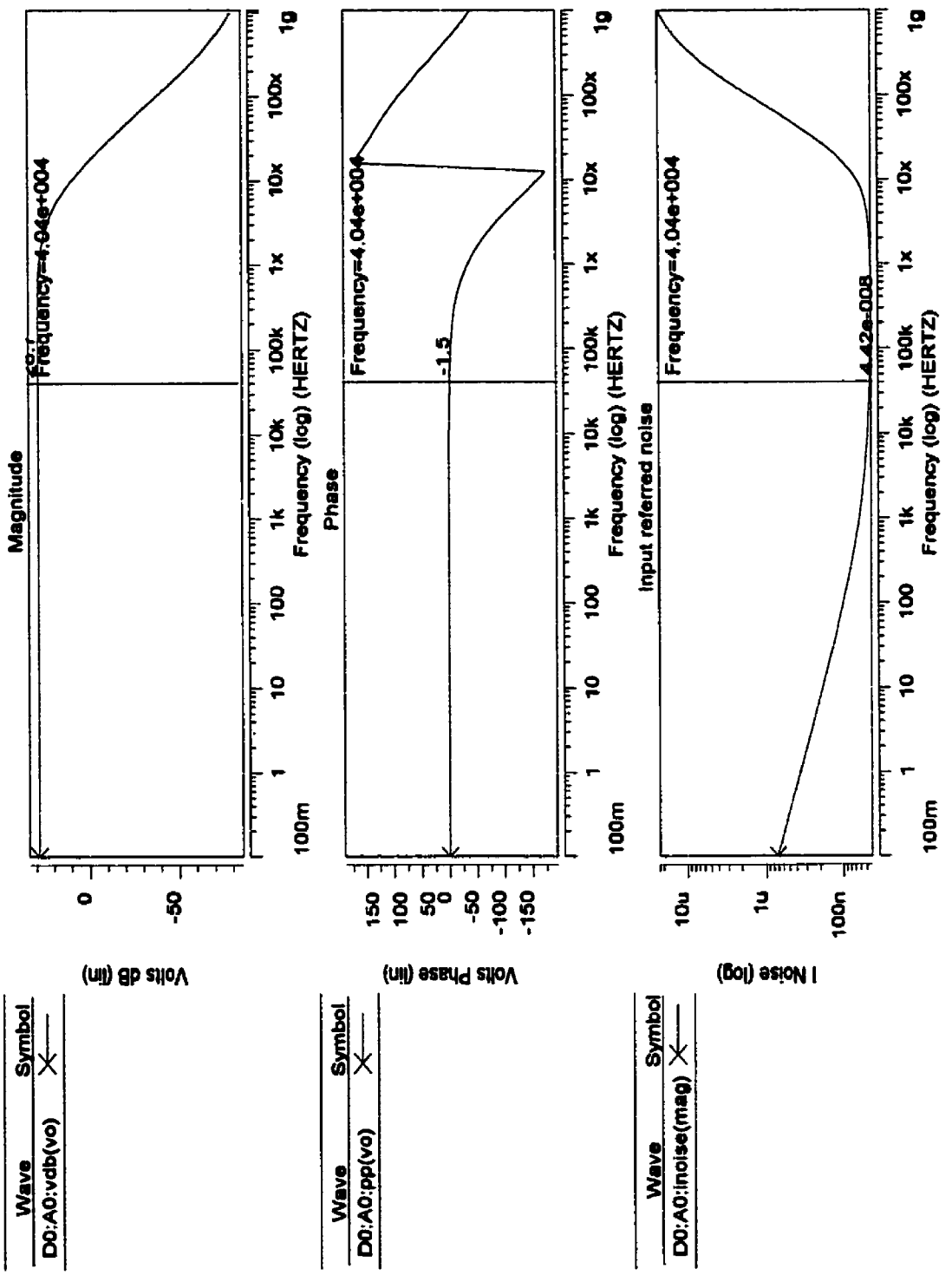


Figure 6.5 Low Noise Rail-to-rail Amplifier AC Response & Noise result

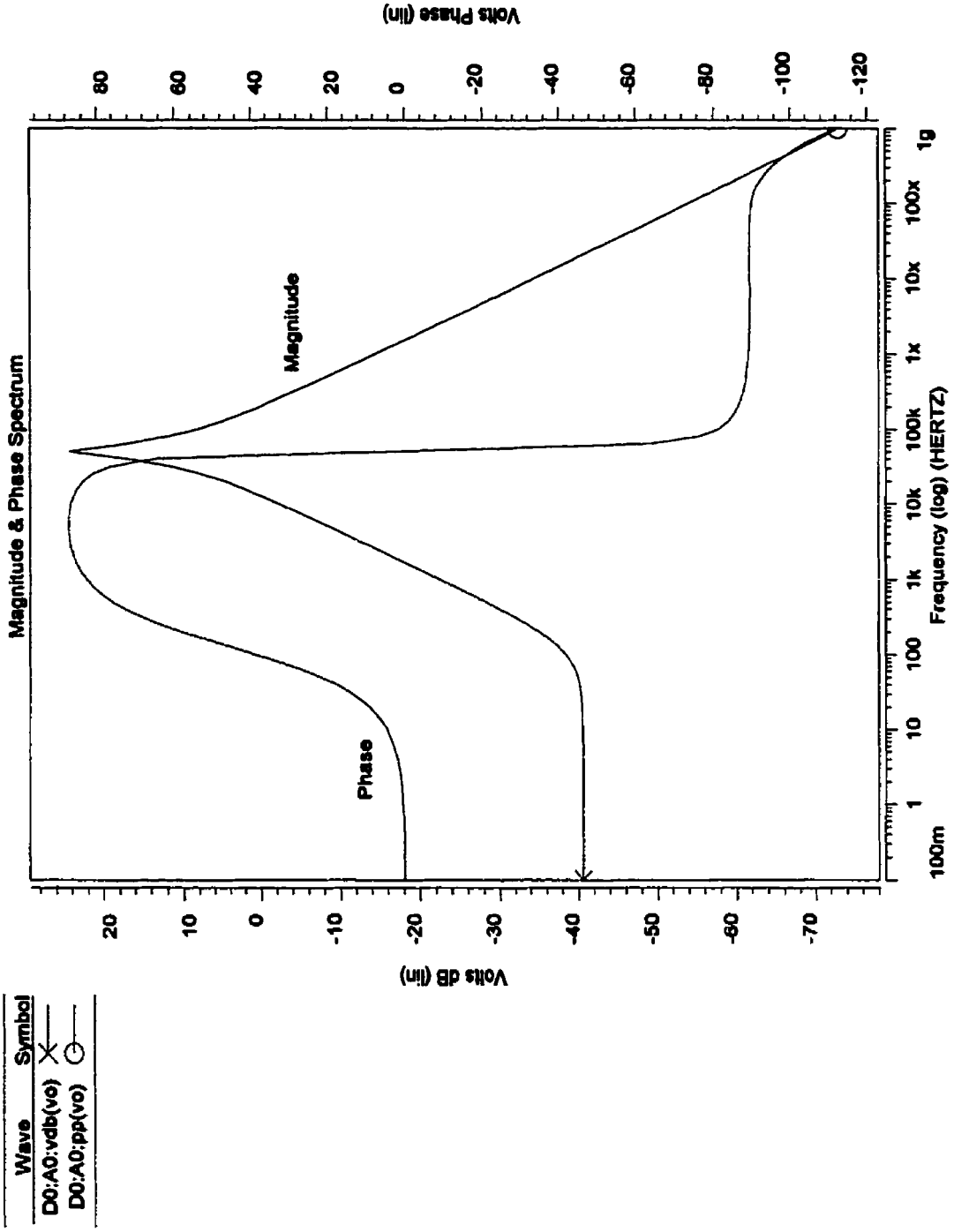


Figure 6.6 Magnitude and Phase Spectrum of the 2nd BPF

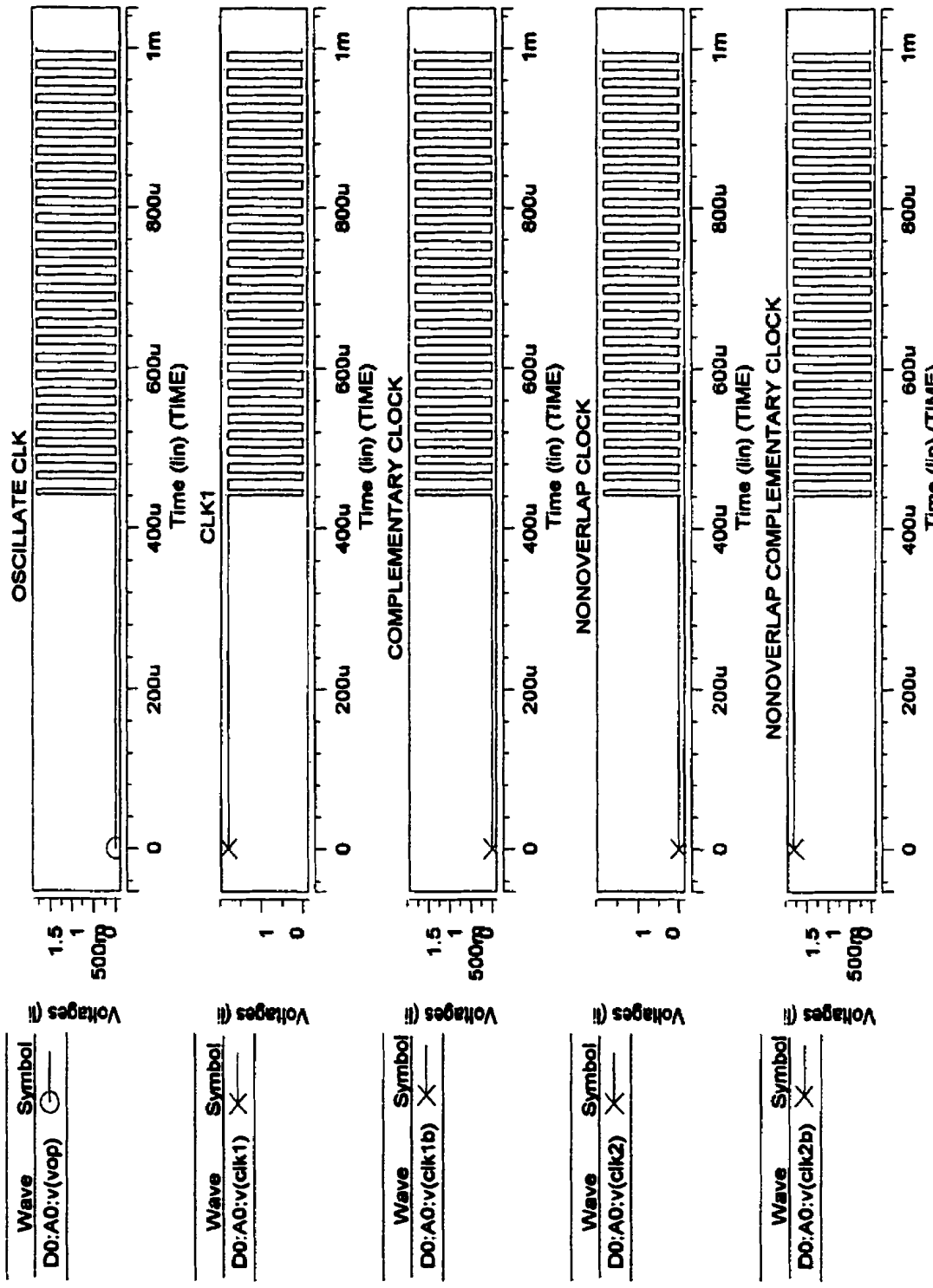


Figure 6.7 Clocks Generated by the Oscillator

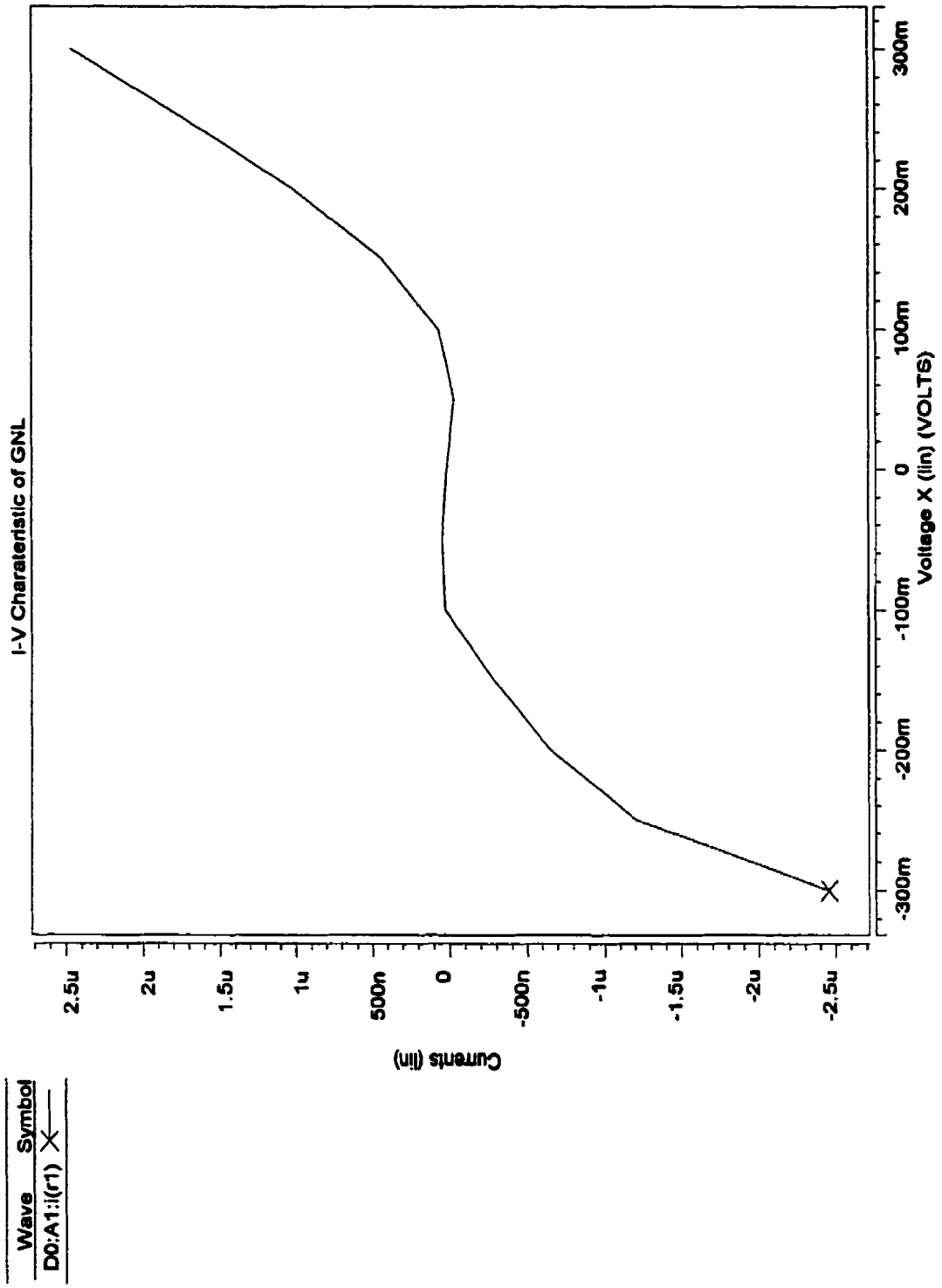


Figure 6.8 I-V Transfer Characteristic of the GNL

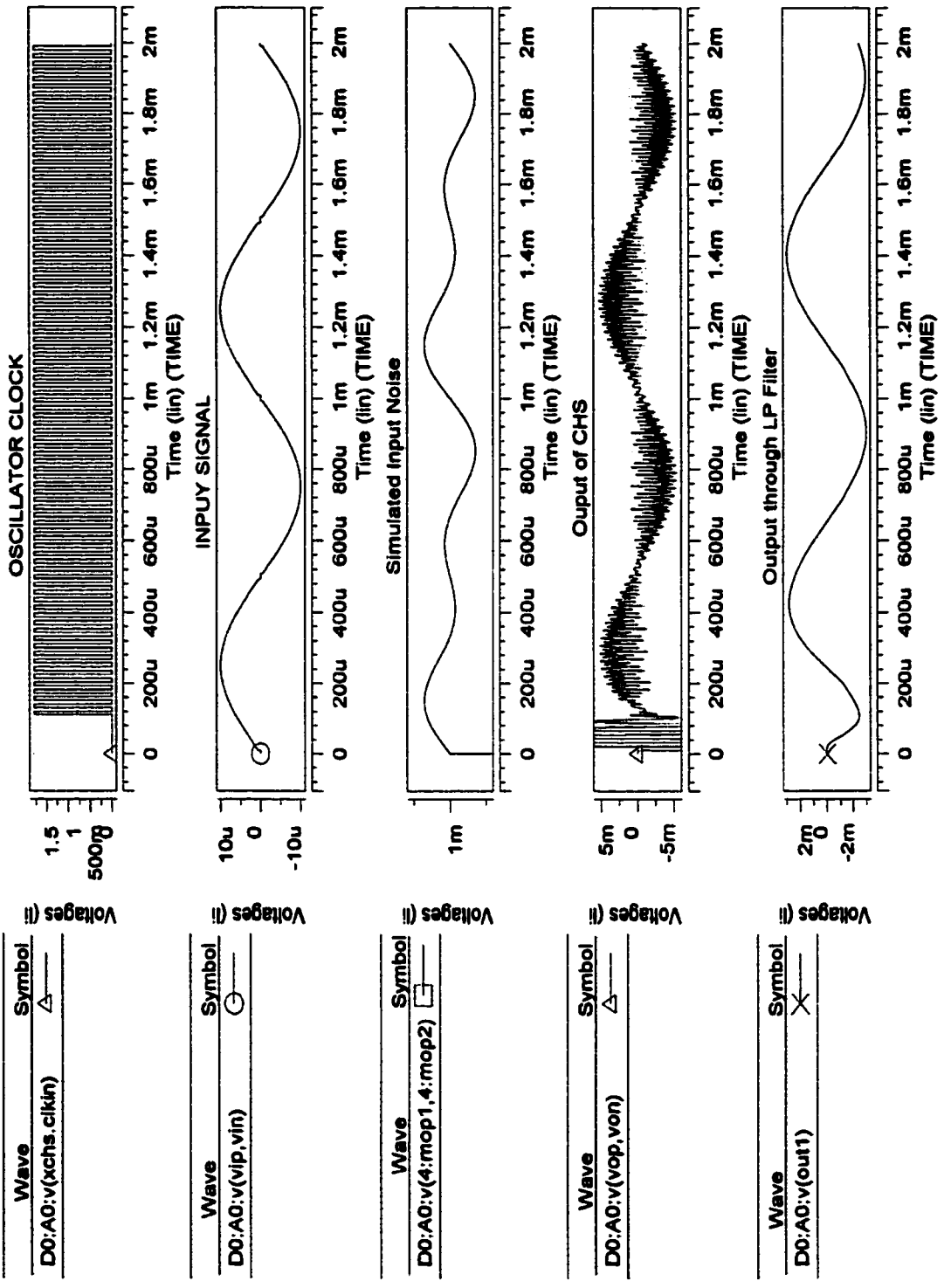


Figure 6.9 Simulation Result of the Chopper Amplifier

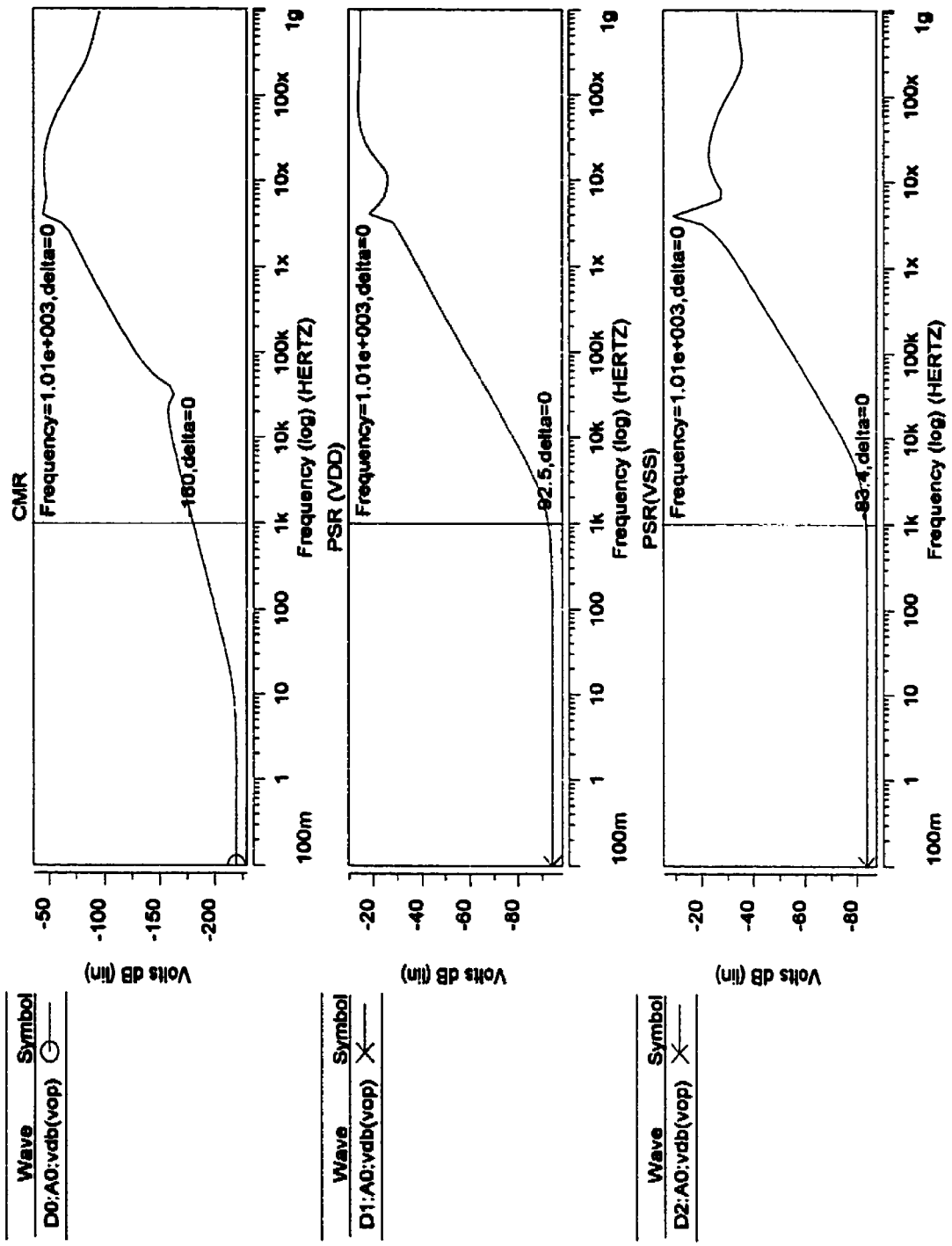


Figure 6.10 Simulation Result of CMR, PSR (VDD) , PSR (VSS)

6.2 Prototype chip

A prototype chip based on the above description was fabricated in a 0.35μm N-well CMOS technology. The layout of the analog front-end system was done manually under Cadence Virtuoso. To reduce unexpected effects caused by the circuit layout, several strategies were adopted for the experimental prototype chip.

All large width transistors in the circuit are split into parallel-connected small transistors. For example, layout of a split transistor (M=4) is illustrated in figure 6.11. The drain and source areas are shared between adjacent transistors. It highly improves the performance of the current mirrors, since the current ratio will equal the ratio between the multipliers of two transistors, if one ignores the effect of process gradients. There are two benefits with this kind of layout: First, it reduces the area, which also leads to the reduction of source and drain depletion capacitances; Second, it reduces the latch-up problem.

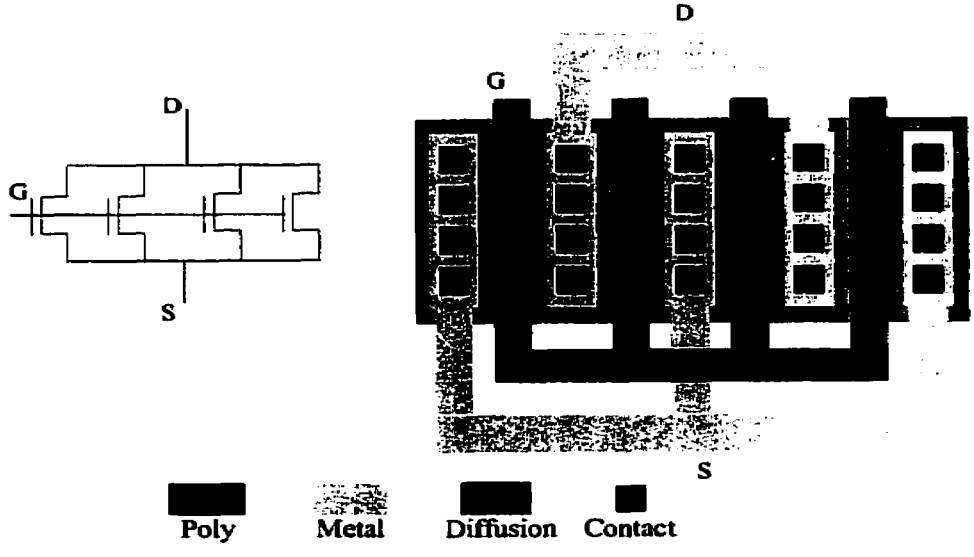


Figure 6.11 Layout of a split transistor (M=4)

For the transistor pairs that need good matching, the interdigitated or common centroid arrangement allows us to reduce the mismatch caused by the process gradient effect. The figure 6.12 illustrates the idea of interdigitated four-transistors pair which is commonly used in the design.

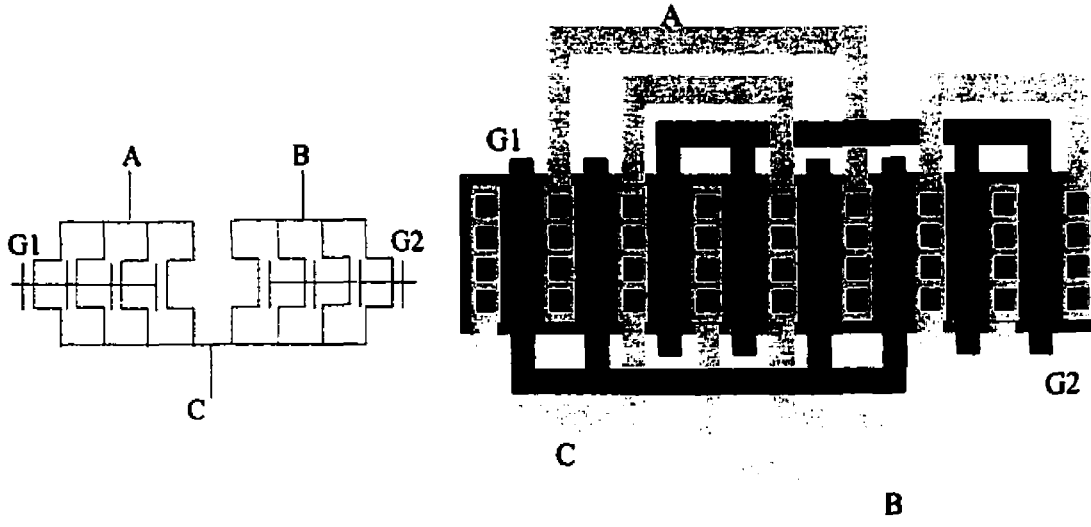


Figure 6.12 Layout of a differential pair with interdigitizing

In addition, the following rules are respected in the layout of the prototype chip:

- Use transistors with the same orientation;
- Respect the symmetries that exist in the electrical network as well as in the layout to limit offset;
- Minimize the source or the drain contact area by stacking transistors;
- Use low resistive paths (metal and not polysilicon) when a current needs to be carried to avoid parasitic voltage drop.

Finally, it should be noticed that as the tuning error between f_{chop} and f_c mainly comes from the mismatch of the resonant stage of the oscillator and the filter, the two resonant stages should be interdigitated to minimize the error. The layout of the whole CHS is depicted in figure 6.13. The core die size is 1150×450 μm^2. The detailed layouts of each block are presented in Appendix C. When the thesis was finished, the chip was still under testing. Some measurement results obtained are listed in table 6.2. The noise performance and the output offset were going to be tested.

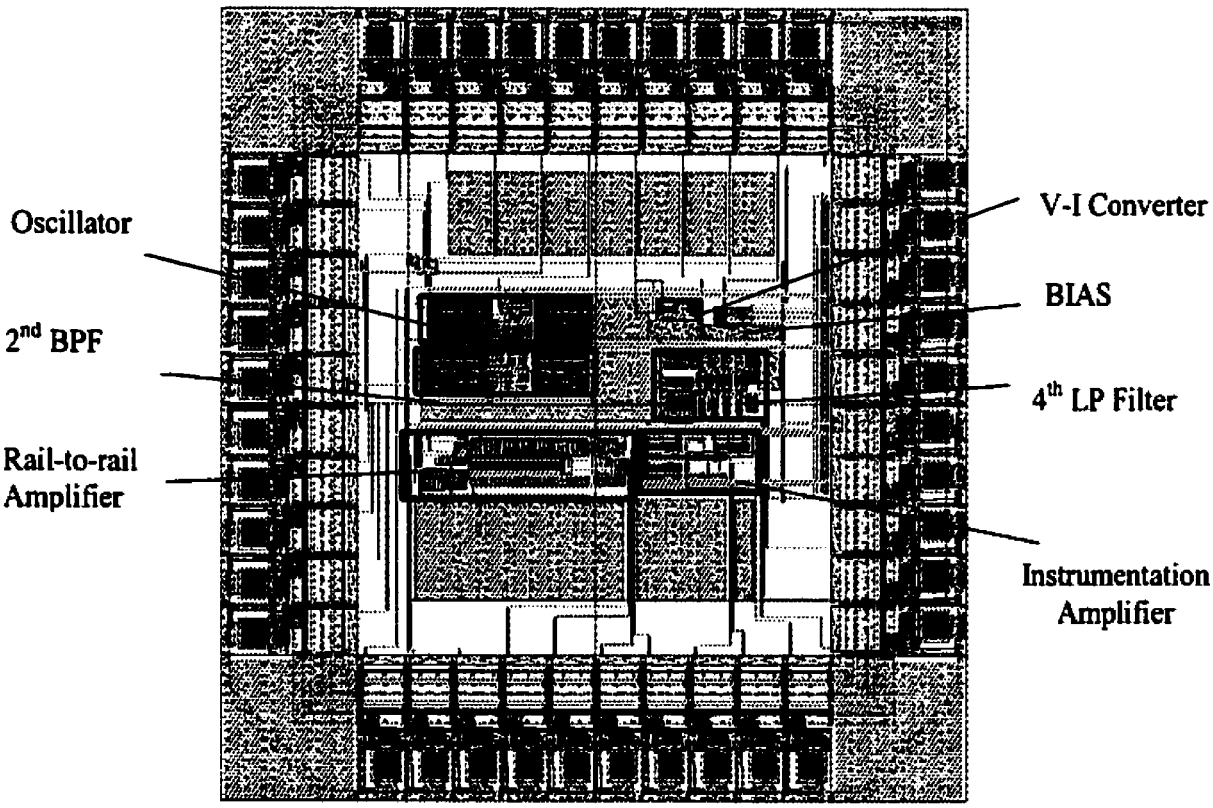


Figure 6.13 Layout of the Analog Front-end Amplifier

Table 6.2 Measurement results of the experimental chip

Power Supply	VDD = 1.8V,VSS = 0
Signal bandwidth	< 4.5K Hz
Oscillation frequency	37.6 K Hz
DC Gain of RTR Amplifier	26 dB
Variation of the Gm of OTA	< 5%
Center frequency of BPF	39.8 K Hz

CHAPTER 7

CONCLUSION

This thesis studies fundamental limitation to ultra low amplitude acquisition applications, which come from the low frequency noise and DC offset. The dominant noise sources of CMOS circuits in low frequency applications are discussed and two low noise techniques, Chopper stabilization (CHS) and Auto-Zero technique (AZ), are reviewed. Due to its continuous property and low thermal noise, the Chopper Stabilization technique (CHS) is chosen in our system to reduce the low frequency noise and DC offset.

To analyze the characteristics of CHS, we introduced a novel method that uses a behavioral model built by SIMULINK. Either the system consideration, such as selection of the selective amplifier, or the non-idealities of the circuit in practice, such as charge injection and tuning error, can be simulated and analyzed conveniently with this model. It is very helpful to optimize the CHS amplifier and thus save us the time to market. In addition, the behavioral model can be used to analyze other circuits.

Then, a fully integrated low-voltage analog front-end preamplifier dedicated to biomedical applications is described in detail. The low supply voltage and wide common mode input range are realized by using a bootstrapped modulator and a rail-to-rail low

noise preamplifier. Its residual offset is optimized by means of a 2nd order bandpass filter implemented on gm-C continuous filter structure. The high CMRR and PSRR are obtained by the fully differential structure and the use of a novel instrumentation amplifier. The output noise power spectral density of the front-end preamplifier is free from 1/f noise and the input referred noise spectral density is equal to $45nV/\sqrt{Hz}$. Although the analog front-end preamplifier was originally designed for biomedical applications, it can be used for any low frequency applications to monitor ultra low amplitude signals.

Based on the analysis and results reported above, the following projection can be made for future work to further improve the performance of the low noise amplifier.

- To overcome the voltage limits on the rail-to-rail input stage, input pairs working in weak inversion can be taken into account. A constant gm can be obtained by its linear voltage-to-current transfer characteristic. Consequently, the system power supply can be reduced to 1.2 V.

- To improve the signal dynamic range, a current-mode 2nd order bandpass filter can be considered to replace the voltage-mode filter. Thus the first stage just uses a rail-to-rail low noise operational transconductor amplifier (OTA) to transfer the input signal from voltage to current. If a wider signal bandwidth is required, a higher order bandpass filter is needed to reduce the distortion.

- To further improve the performance of the input modulator, a PMOS bootstrapped switch can be used to replace the NMOS counterpart. This is because in the n-well process, only the substrate of p-channel transistors can be tied to a voltage that differs from the supply voltage. Due to the zero source-bulk voltage difference, the threshold voltage of p-channel transistor will be independent of input voltage. Thus the variation of charge injection and the "on" resistance can be further decreased. Note that the demodulator also needs to be modified to ensure synchronous operation.

- The behavioral model can be further improved by including more customized blocks to accurately mimic the CHS behavior. For instance, the effect caused by the variation of duty cycle can be analyzed by introducing a periodic pulse signal superimposed on the ideal clock.

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ANNEX A

SCHEMATICS

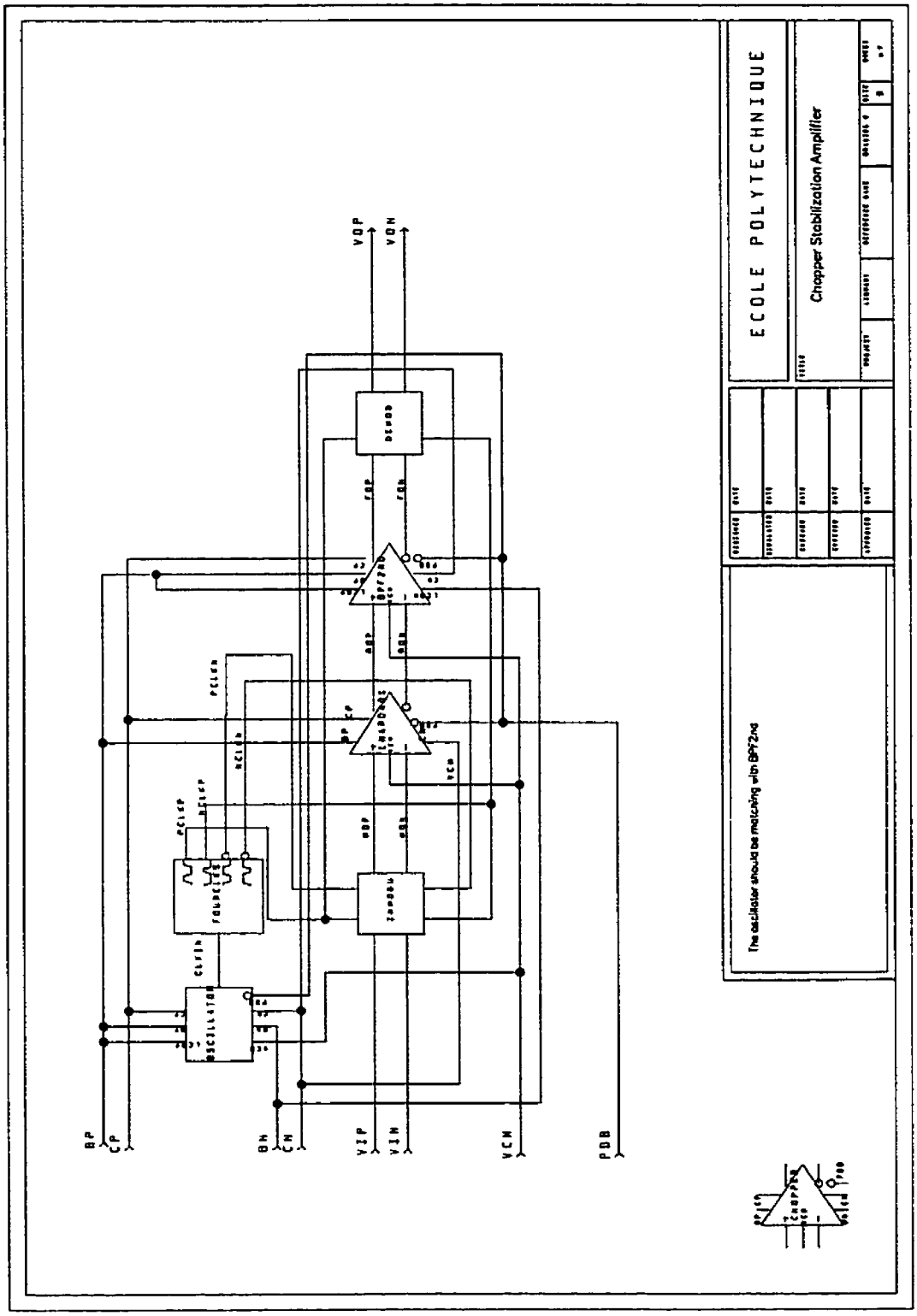

Figure A.1 Chopper Stabilization Amplifier

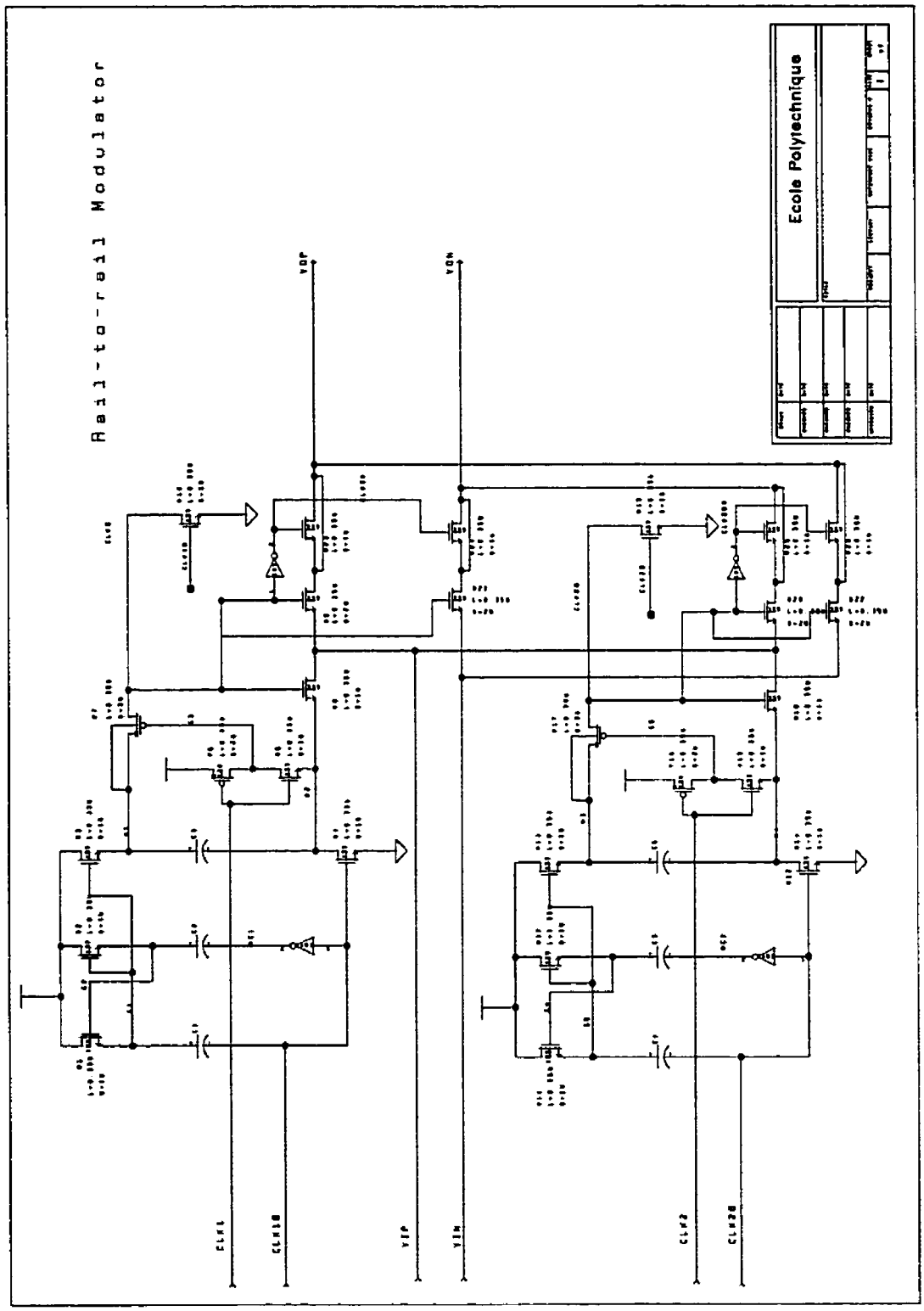

Figure A.2 Input Modulator Cell

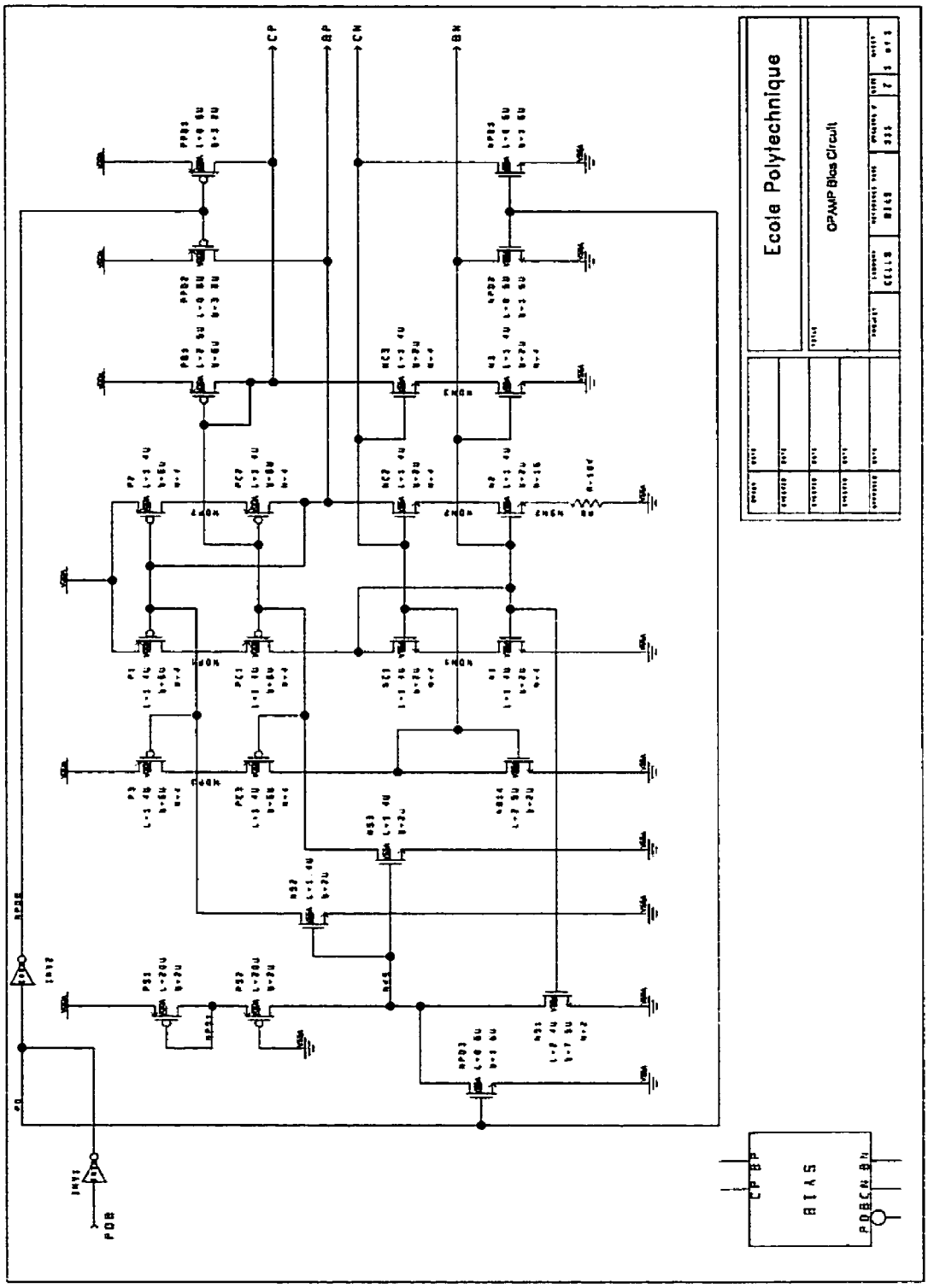

Figure A.3 BIAS Cell

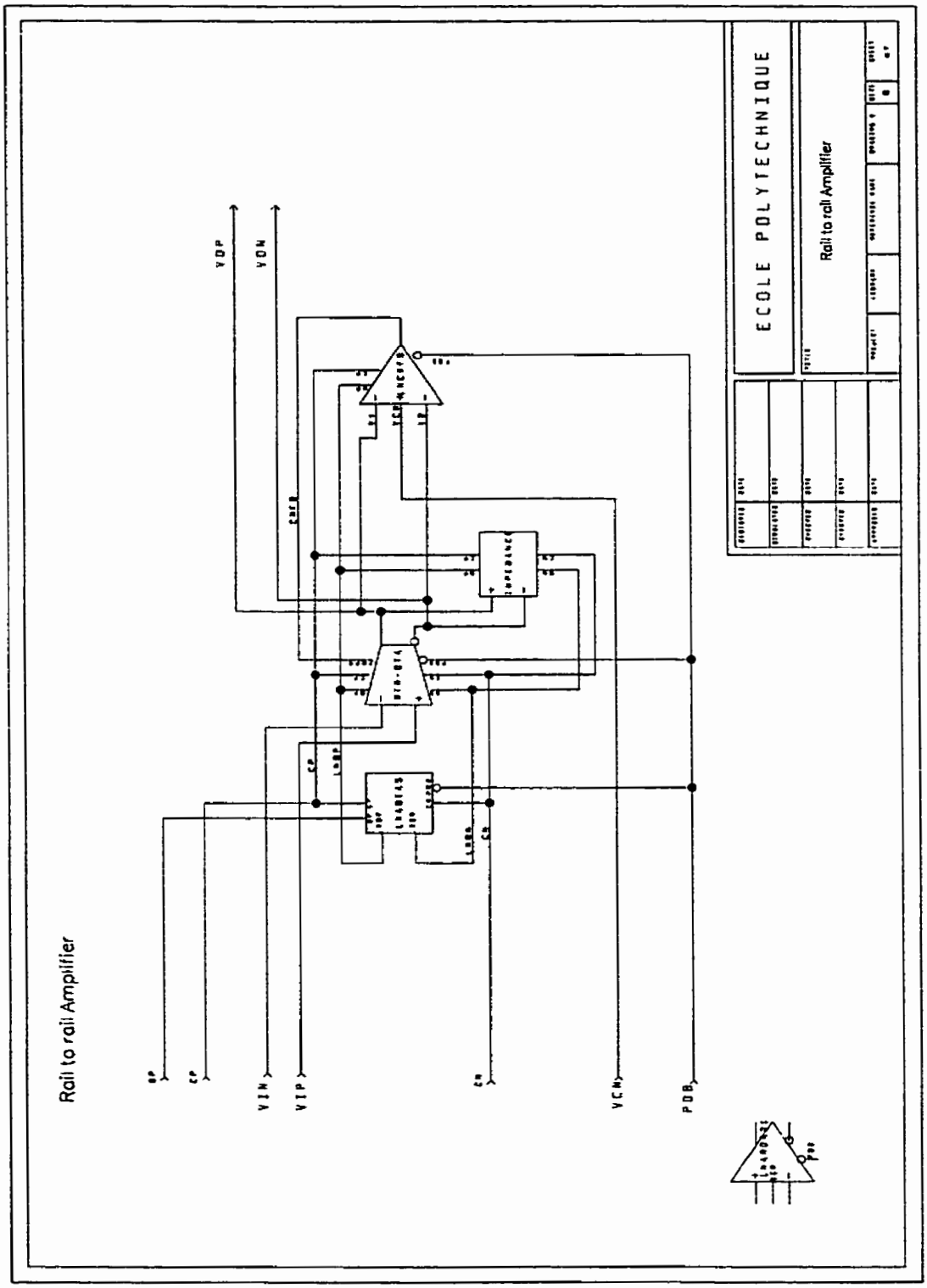

Figure A.4 Low Noise Rail-to-rail Amplifier Cell

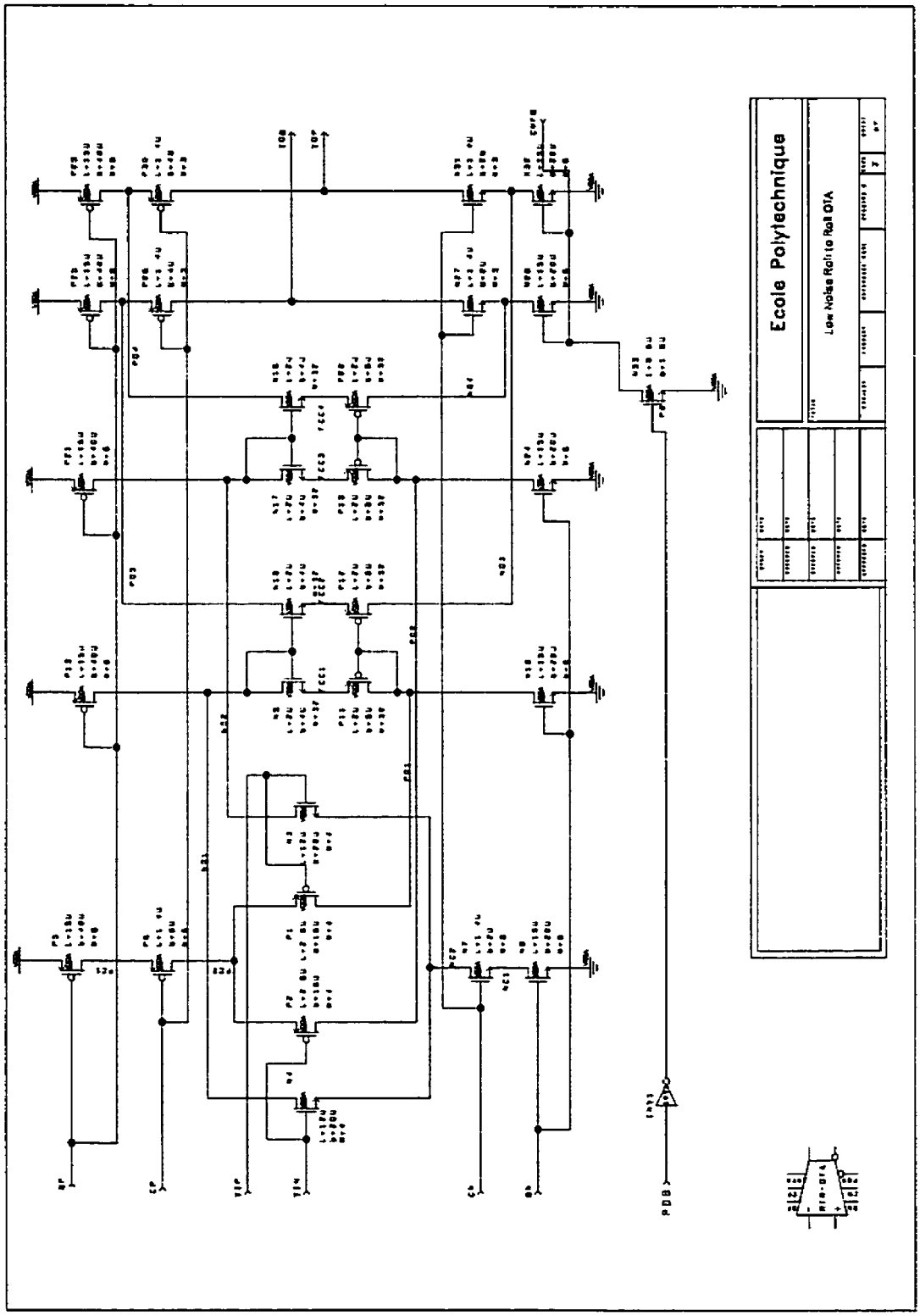

Figure A.5 Low Noise Rail-to-rail Operational Amplifier Cell

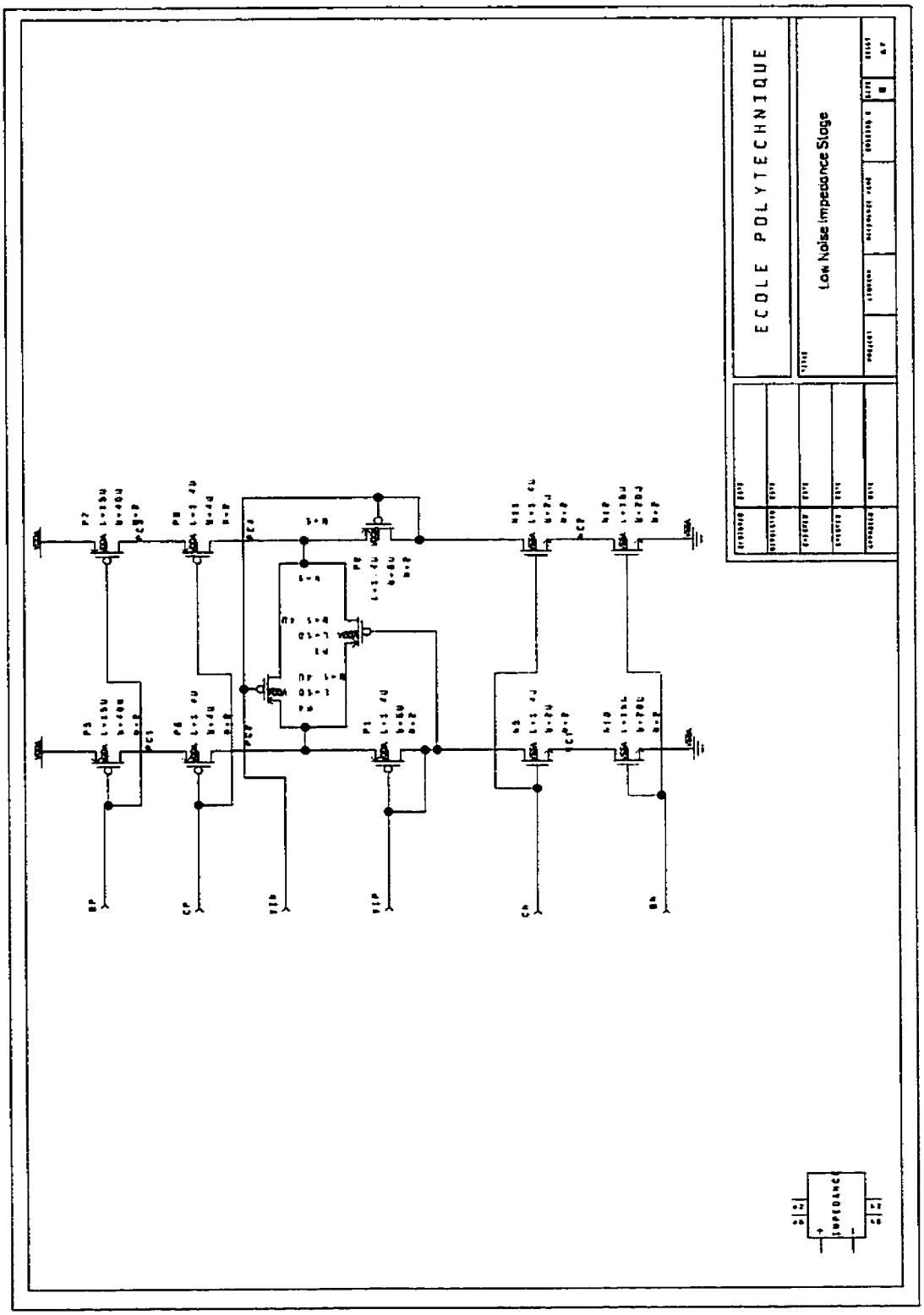

Figure A.6 Low Noise Impedance Cell

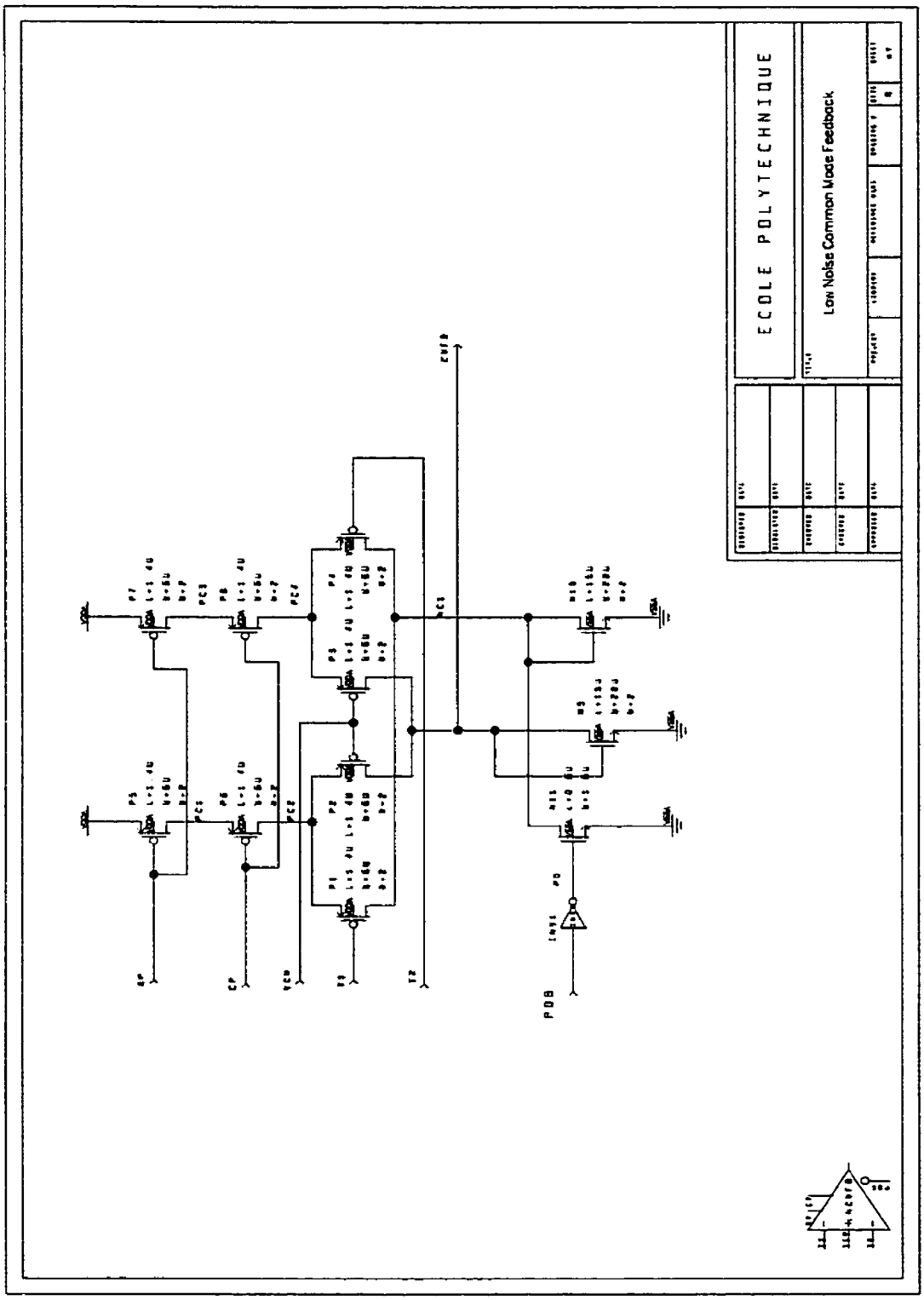

Figure A.7 Low Noise Common Mode Feedback Cell

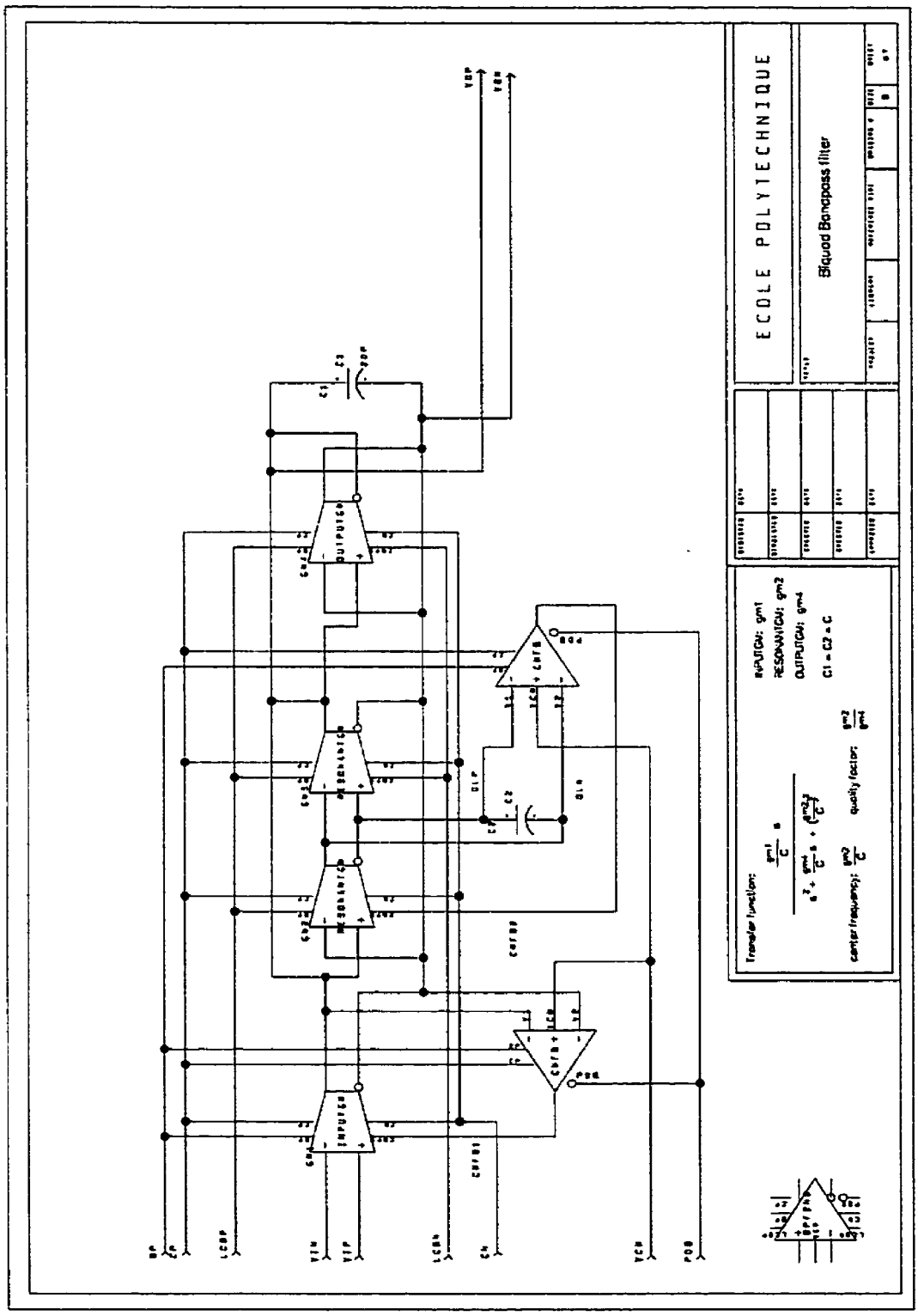

Figure A.8 Biquad Gm-C bandpass Filter Cell

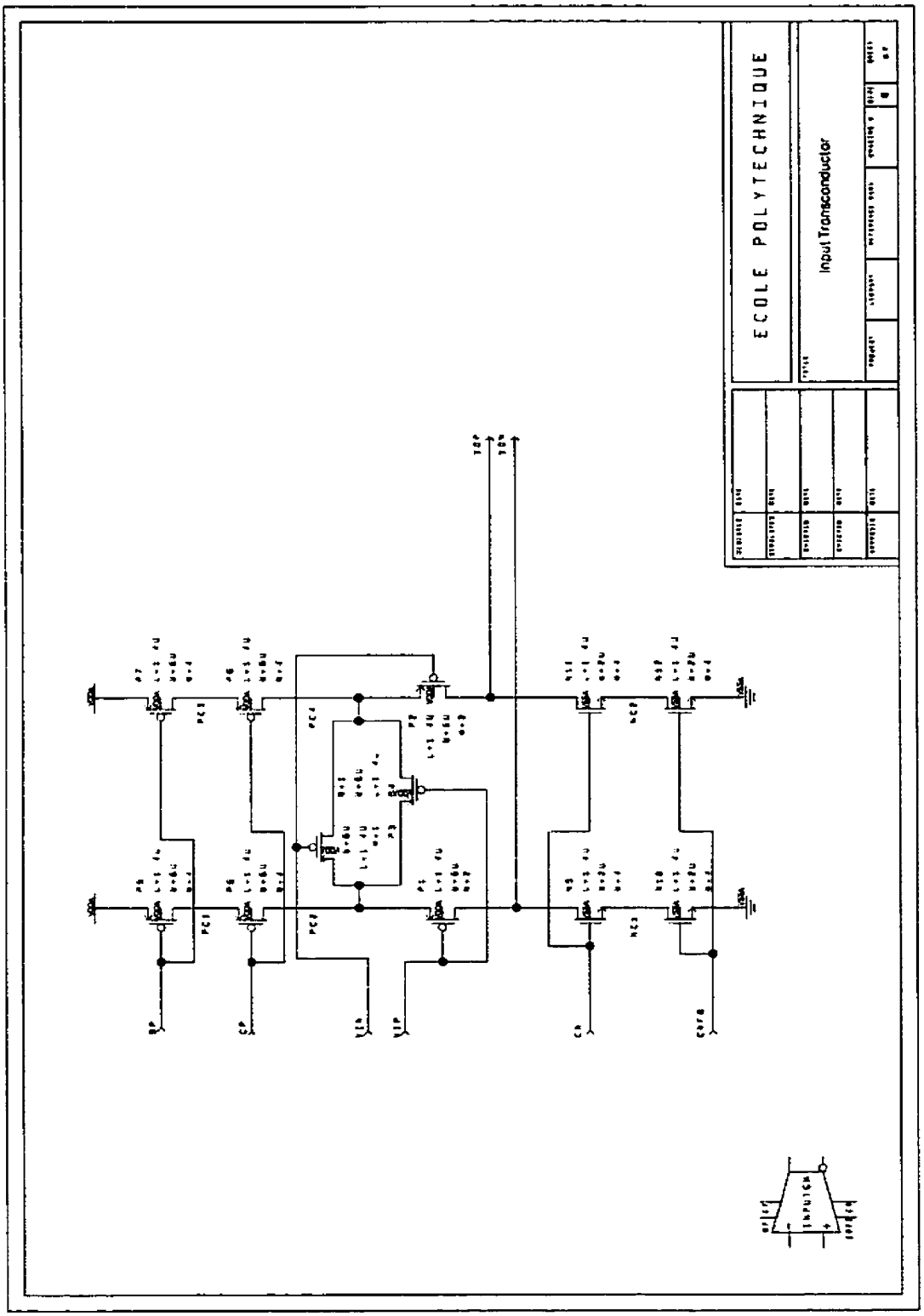

Figure A.9 Input Transconductor Cell

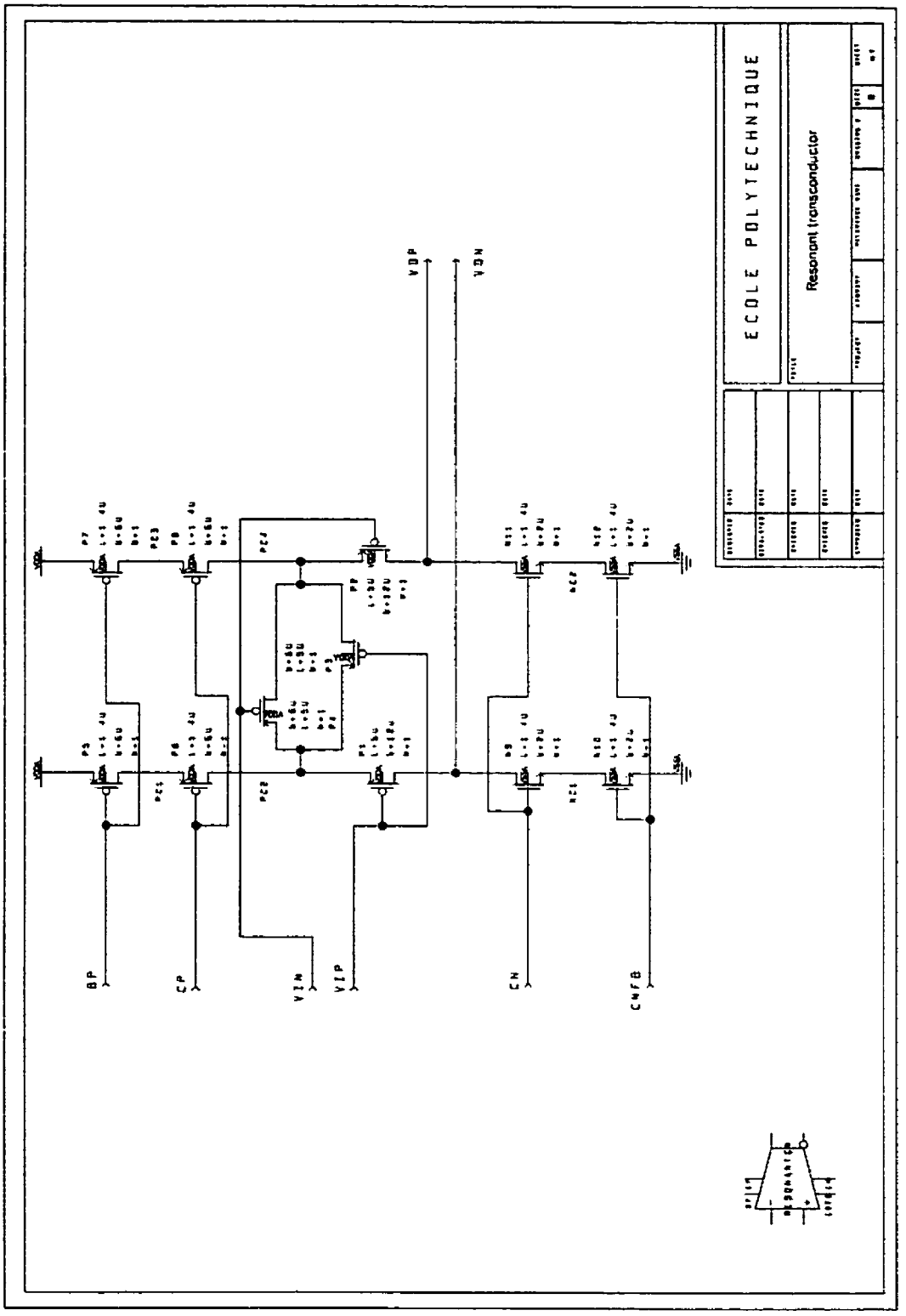

Figure A.10 Resonant Transconductor Cell

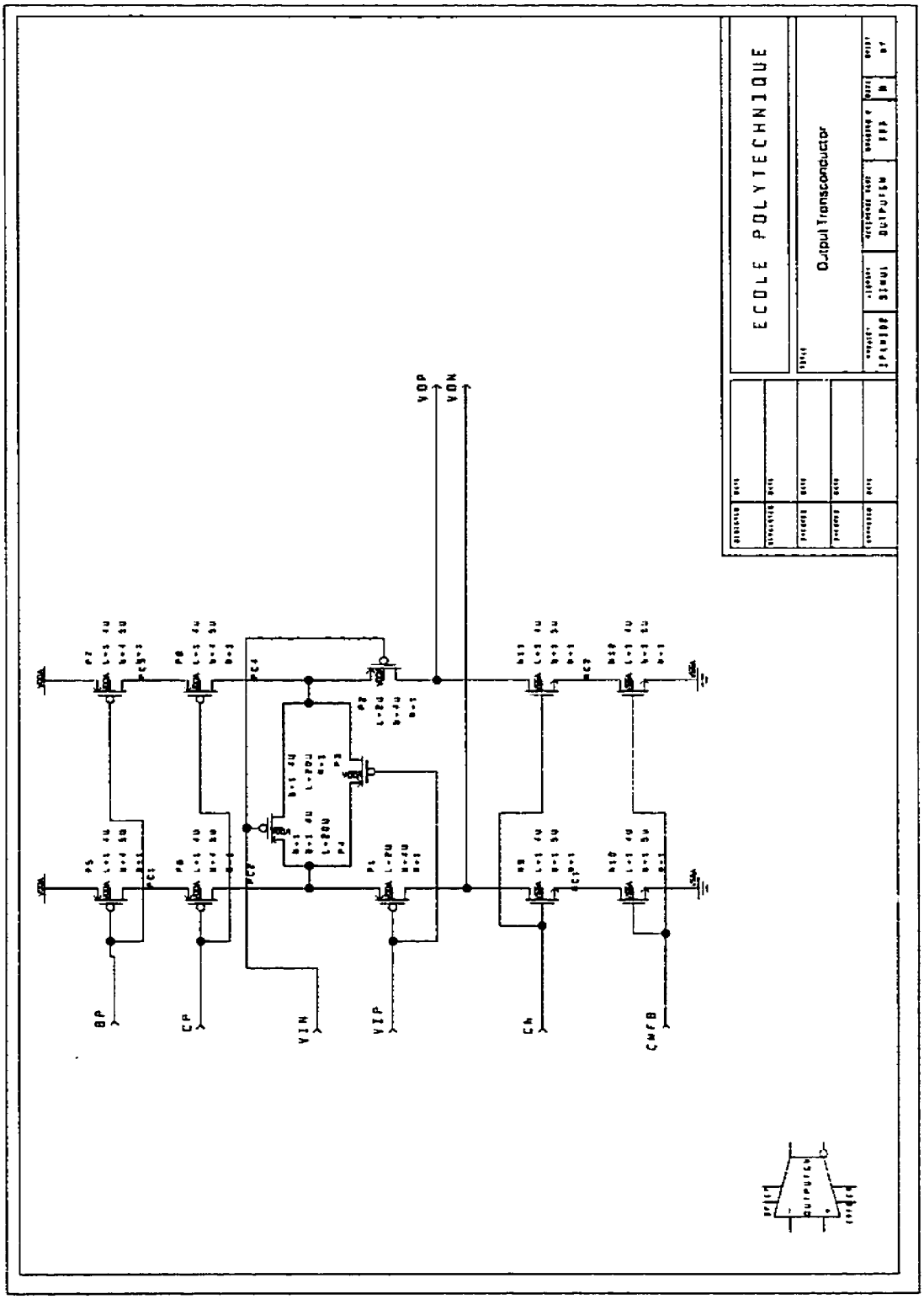

Figure A.11 Output Transconductor Cell

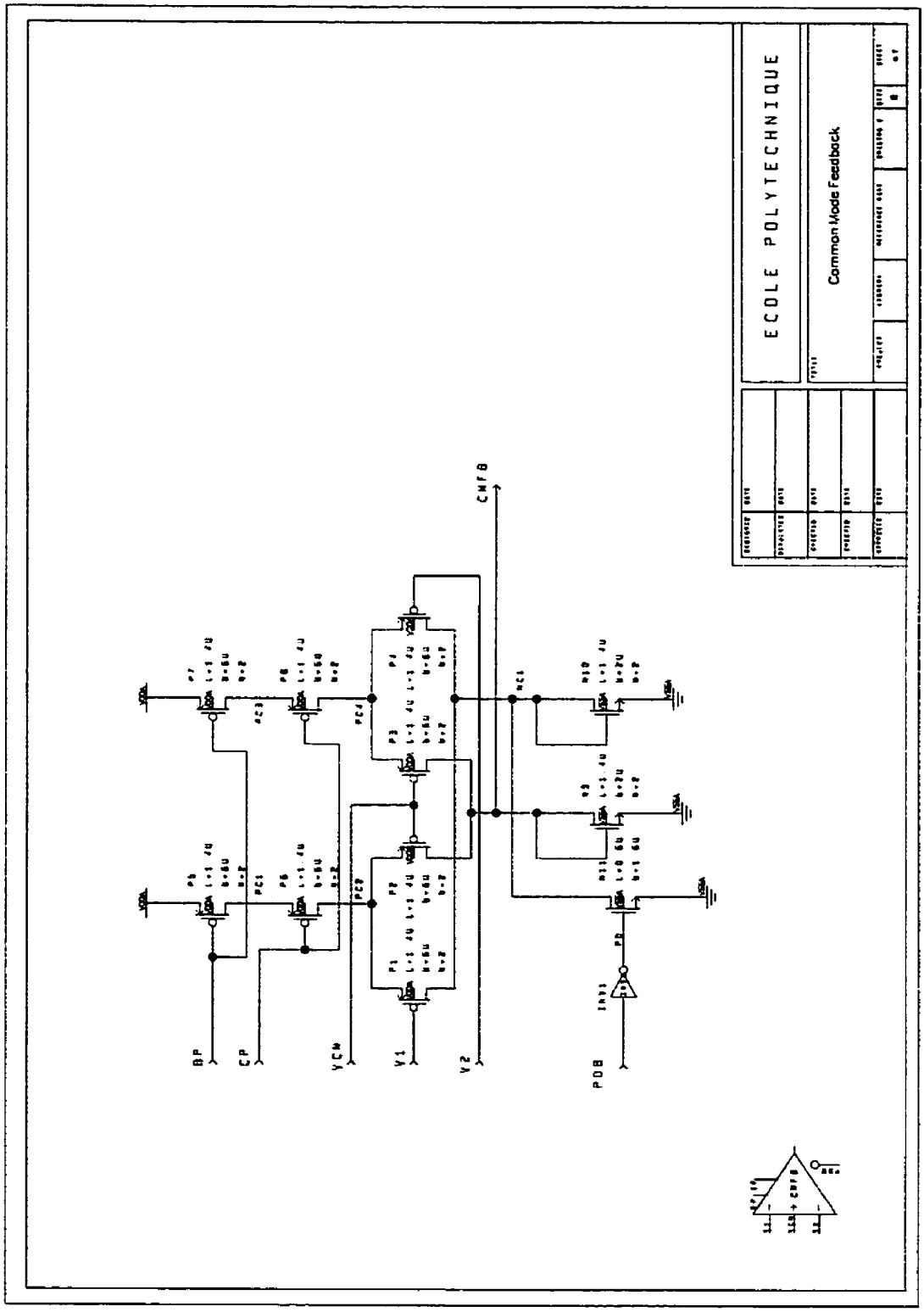

Figure A.12 Common Mode Feedback Cell

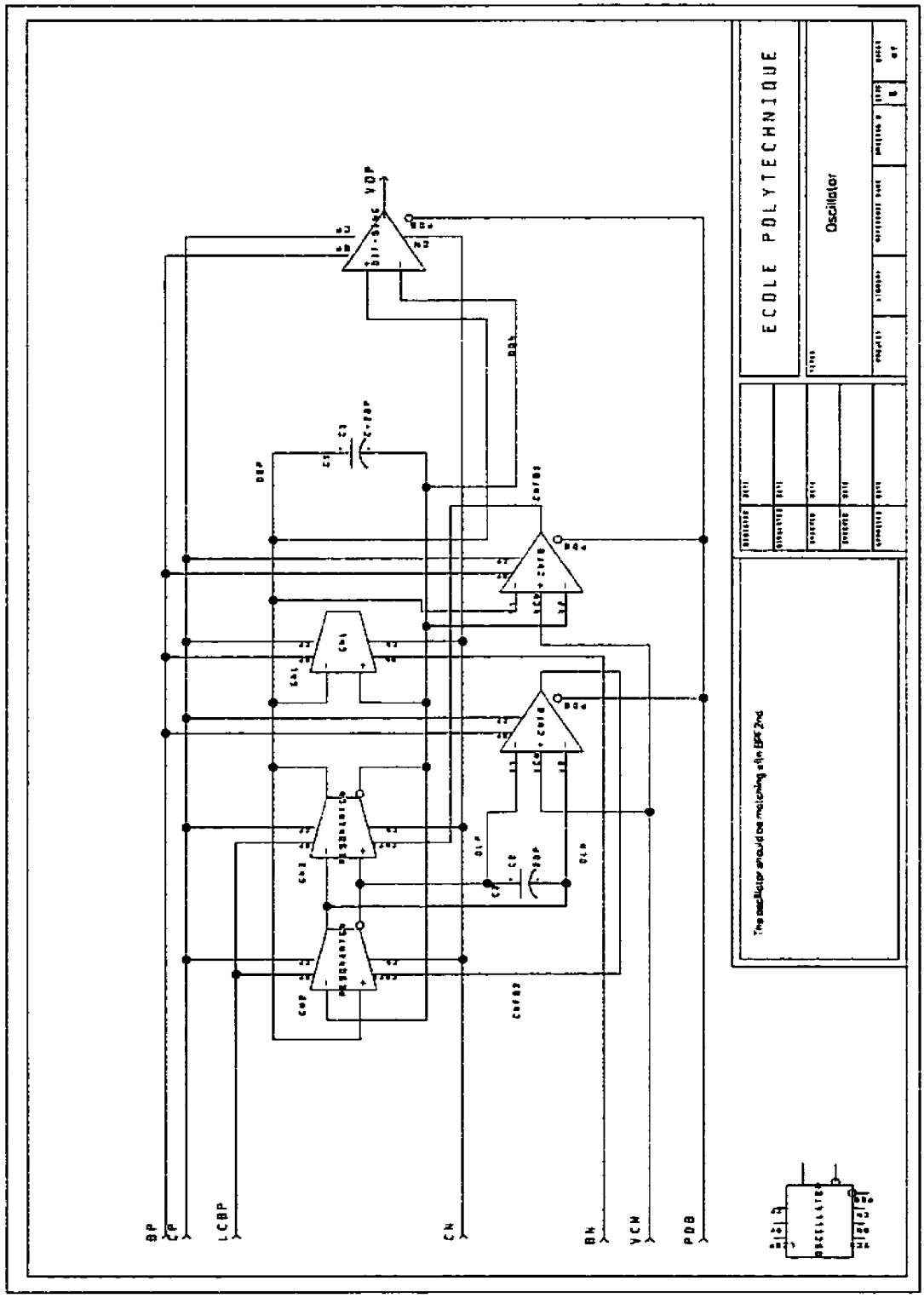

Figure A.13 Matching Oscillator Cell

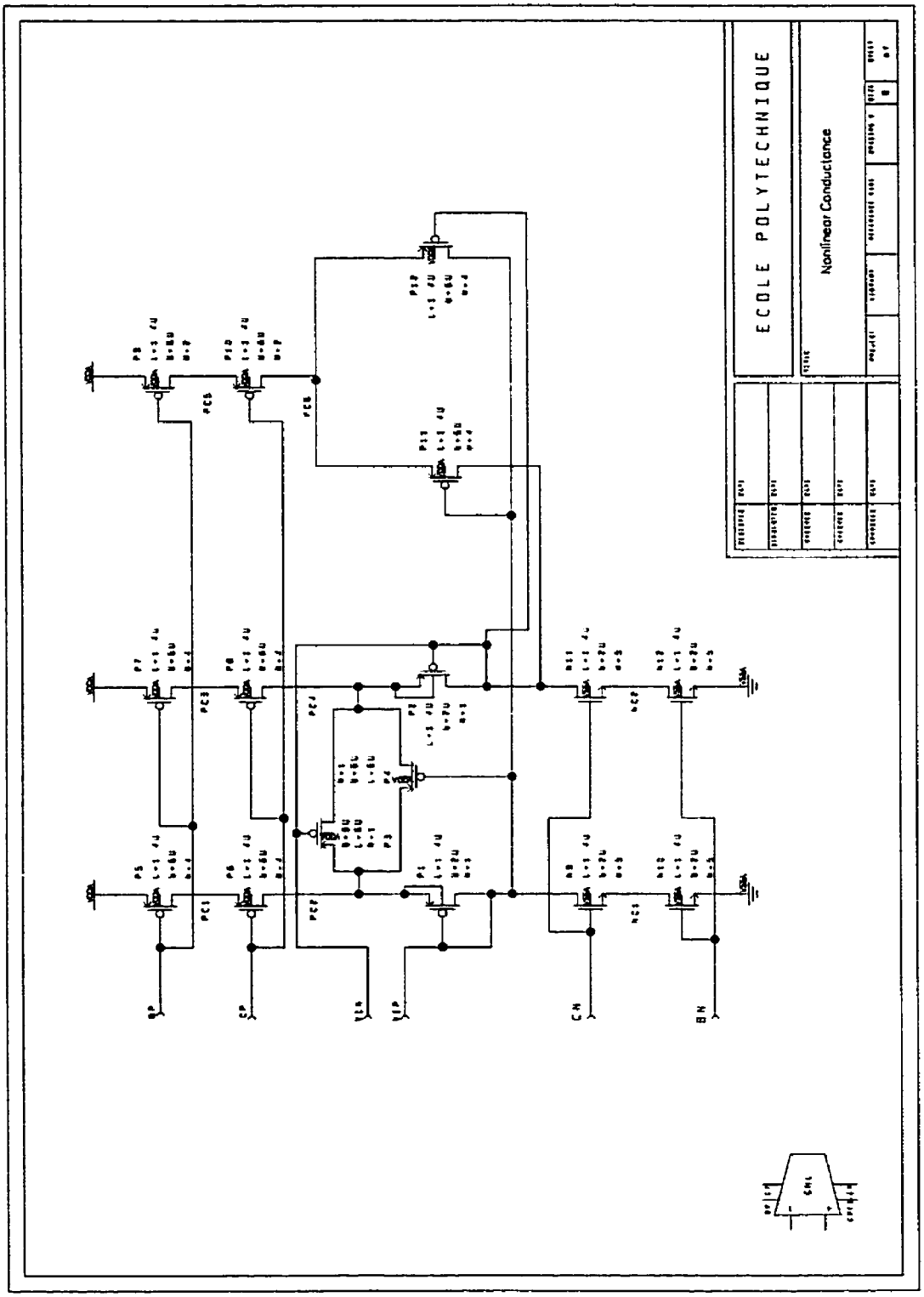

Figure A.14 Nonlinear Transconductor Cell

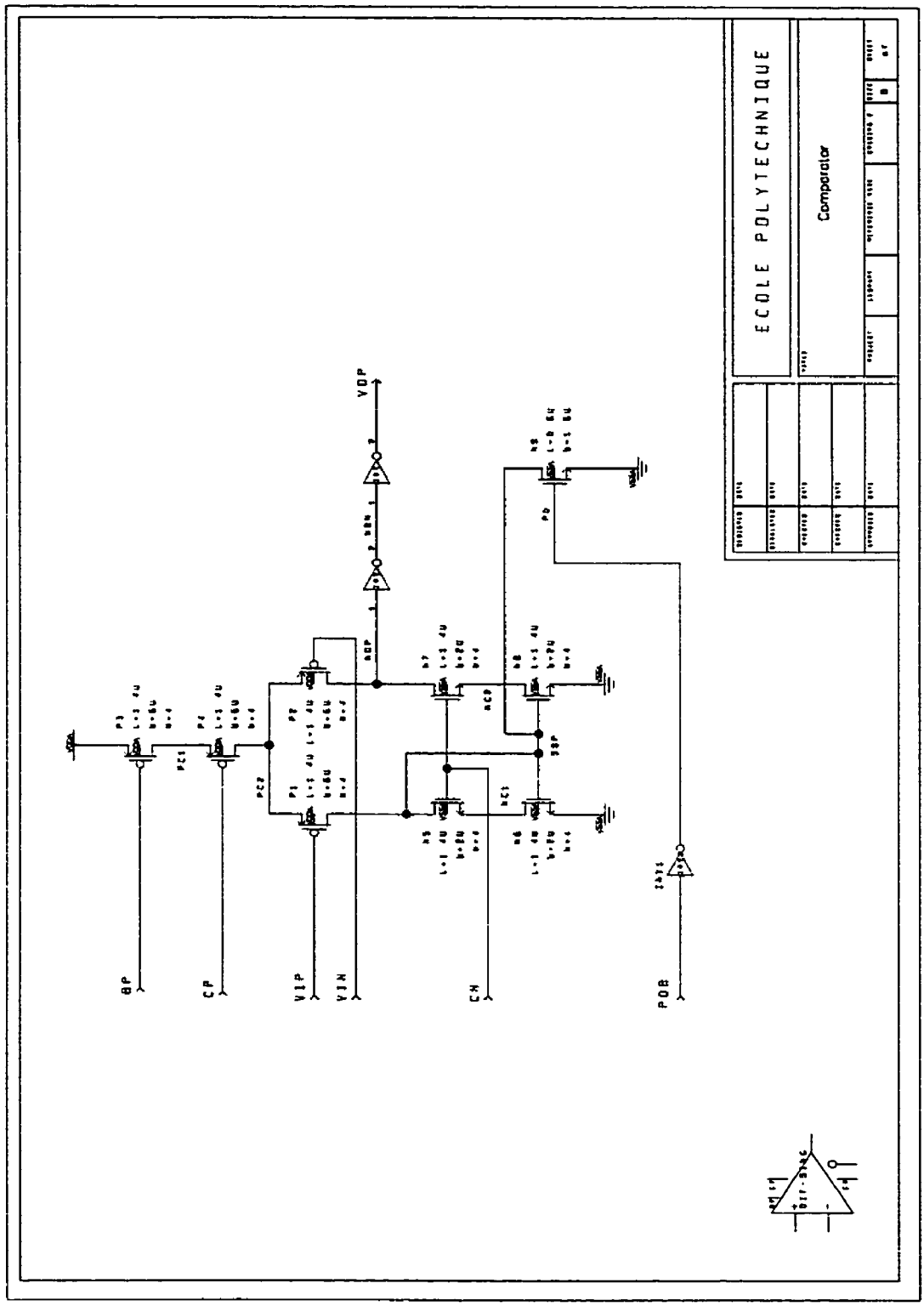

Figure A.15 Differential-to-Single Converter Cell

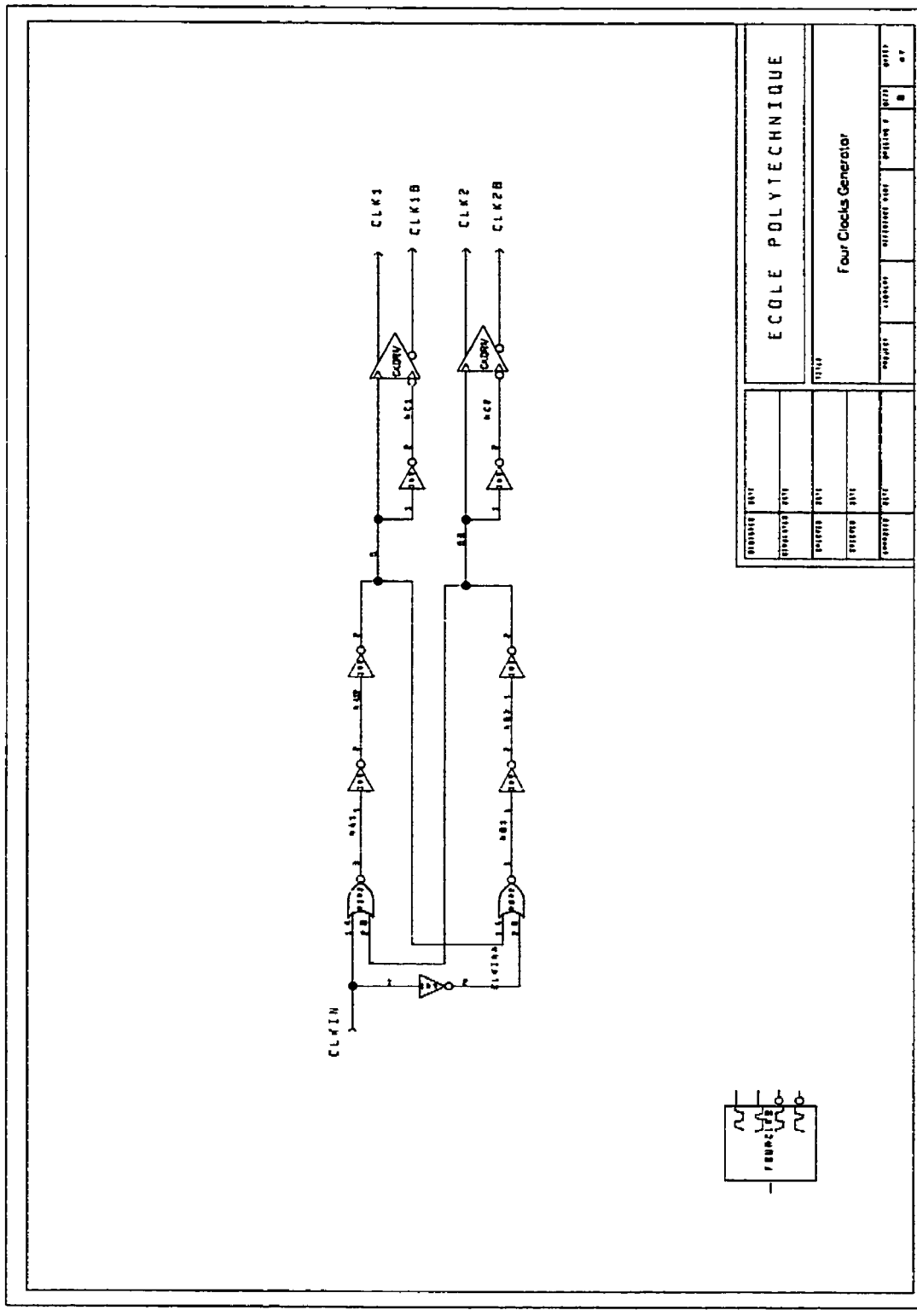

Figure A.16 Four Clocks Generator Cell

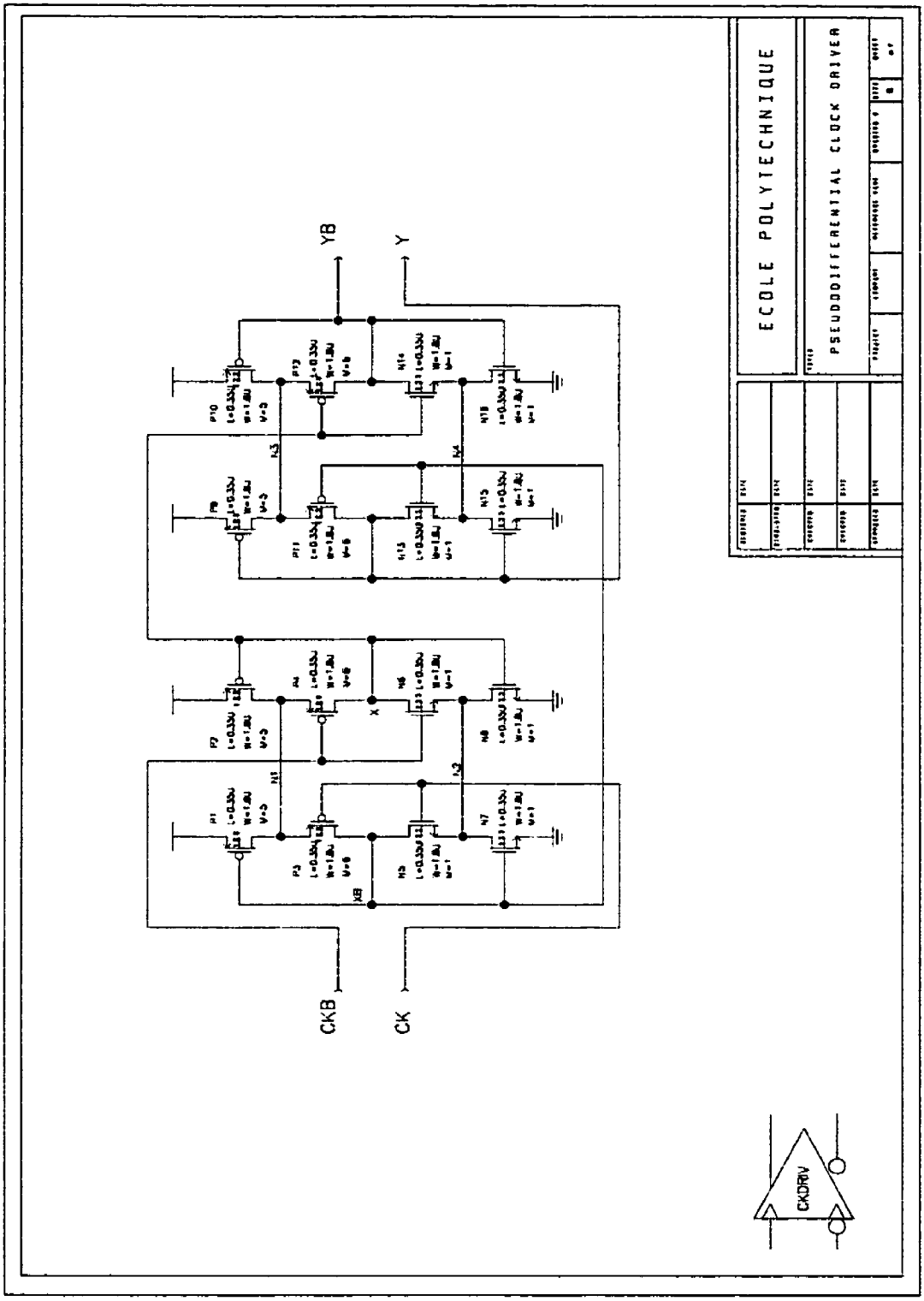

Figure A.17 Pseudo Differential Clock Driver Cell

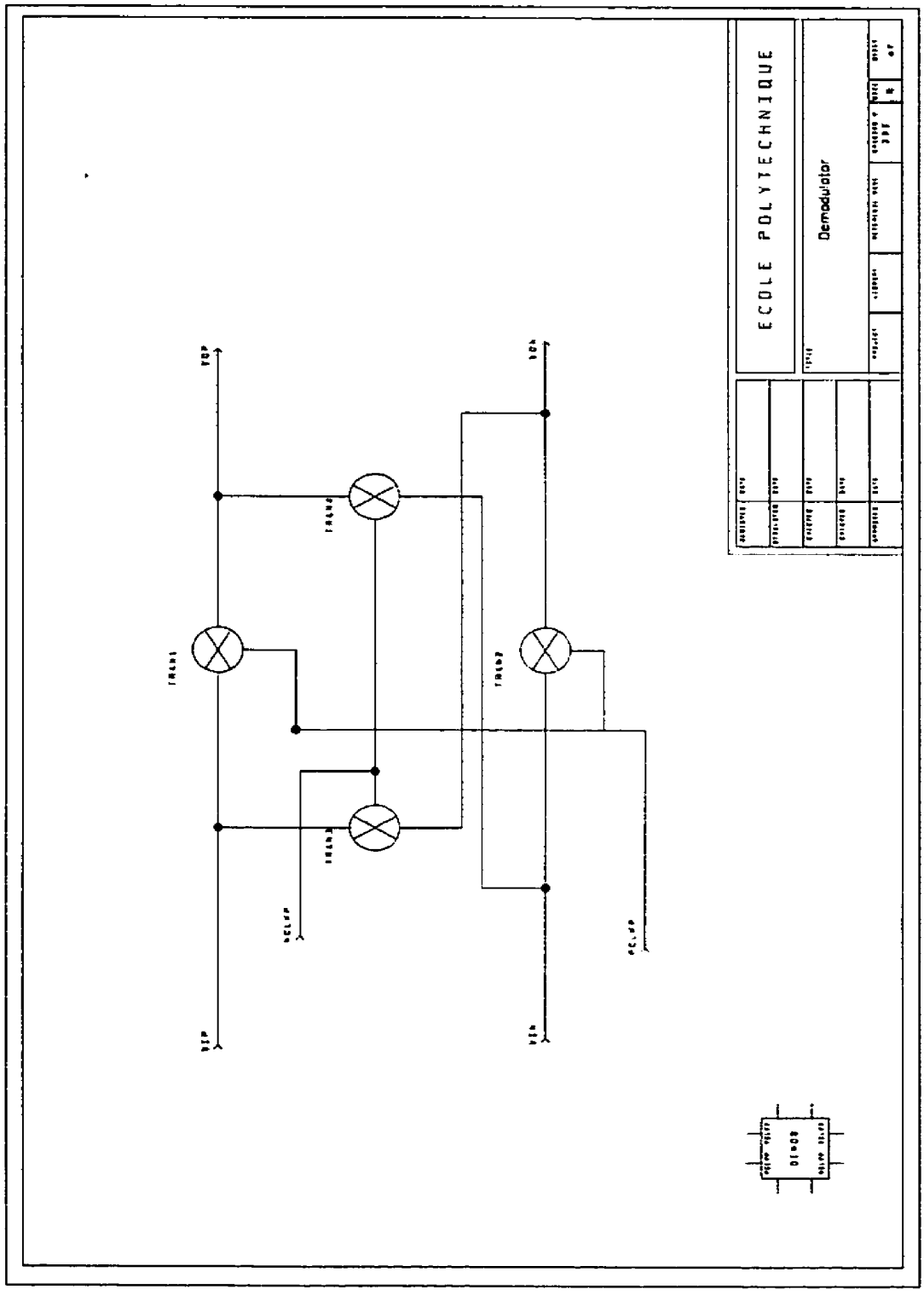

Figure A.18 Demodulator Cell

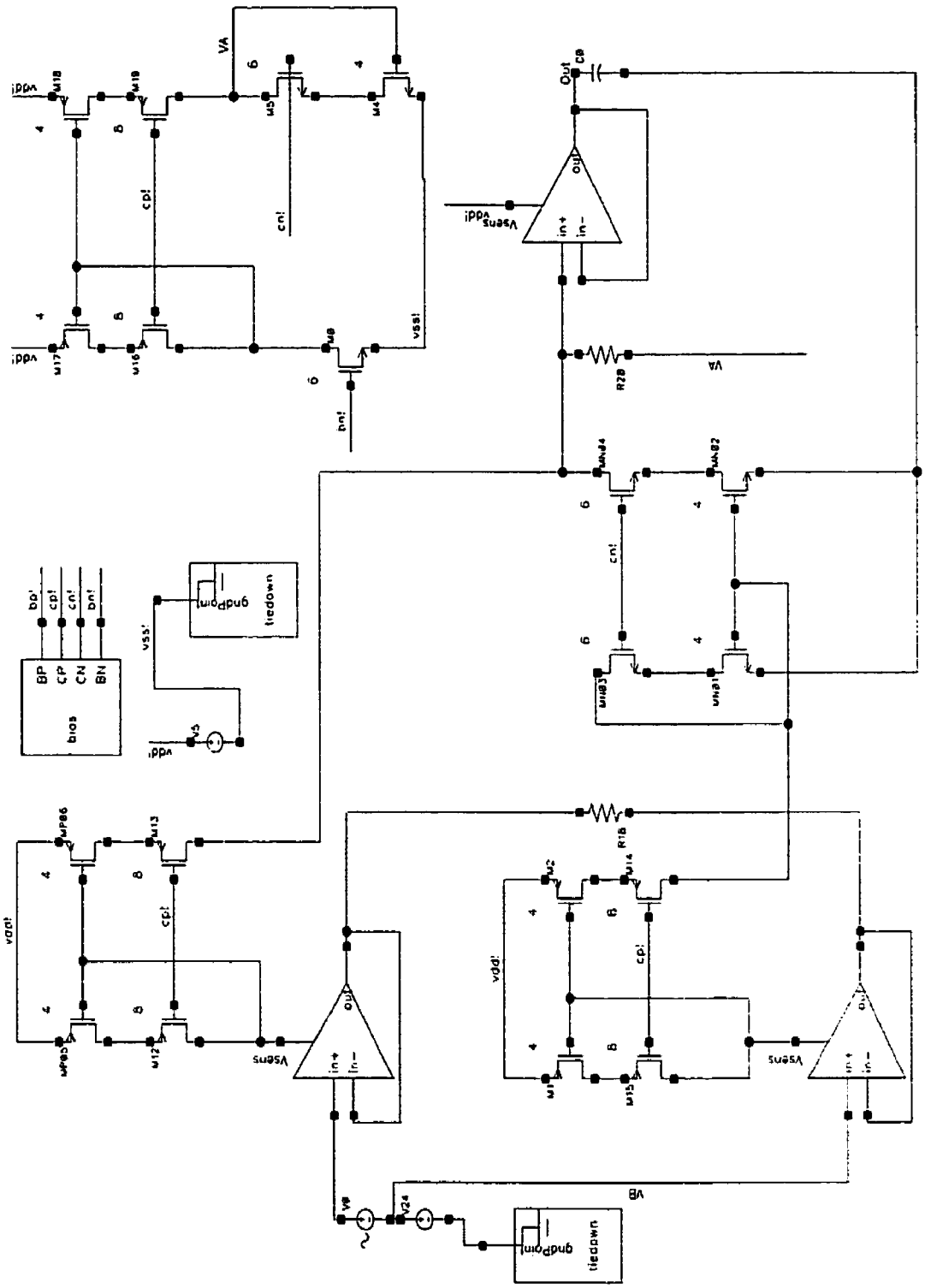

Figure A.19 Instrumentation Amplifier

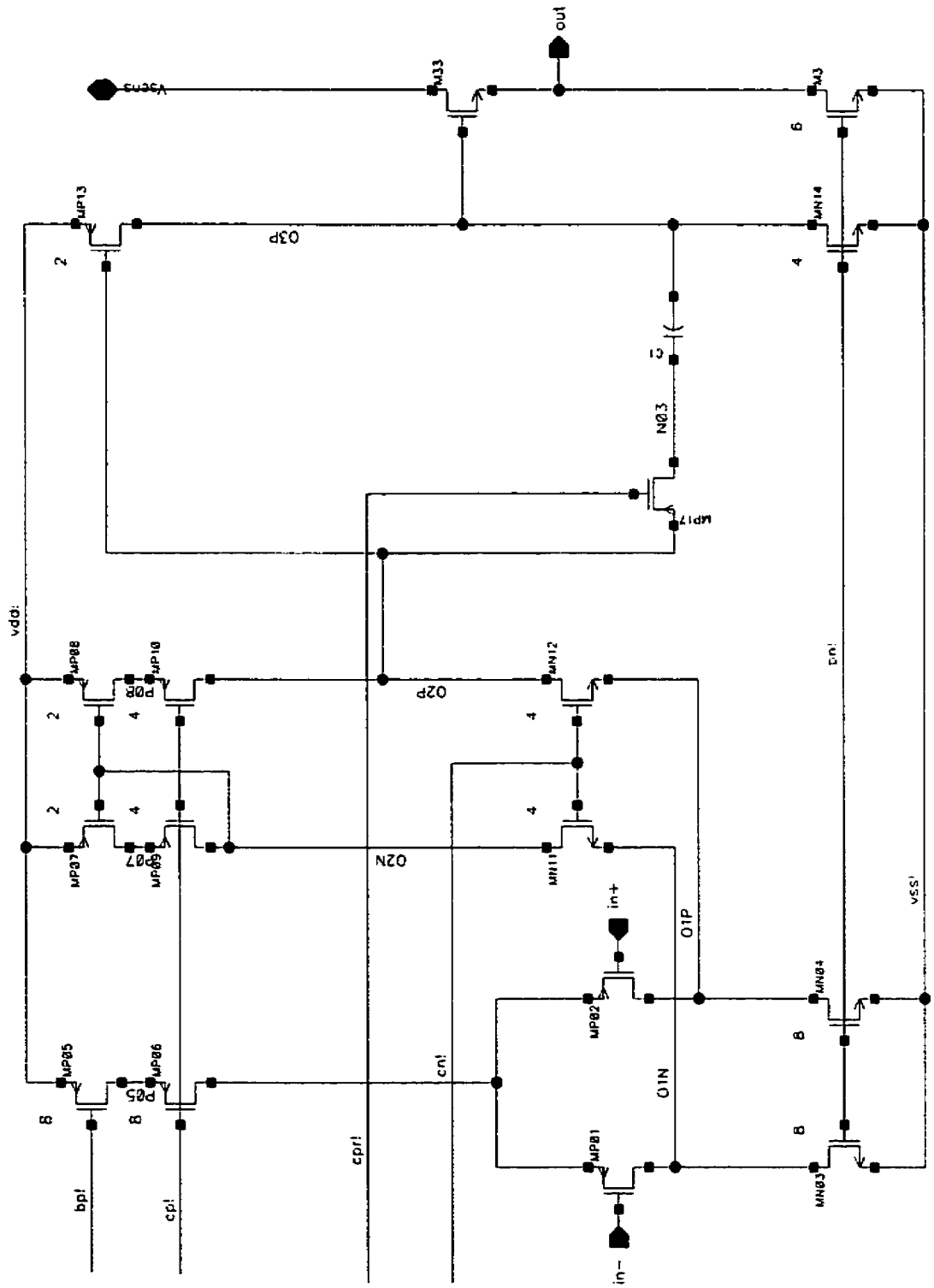

Figure A.20 OPAMP

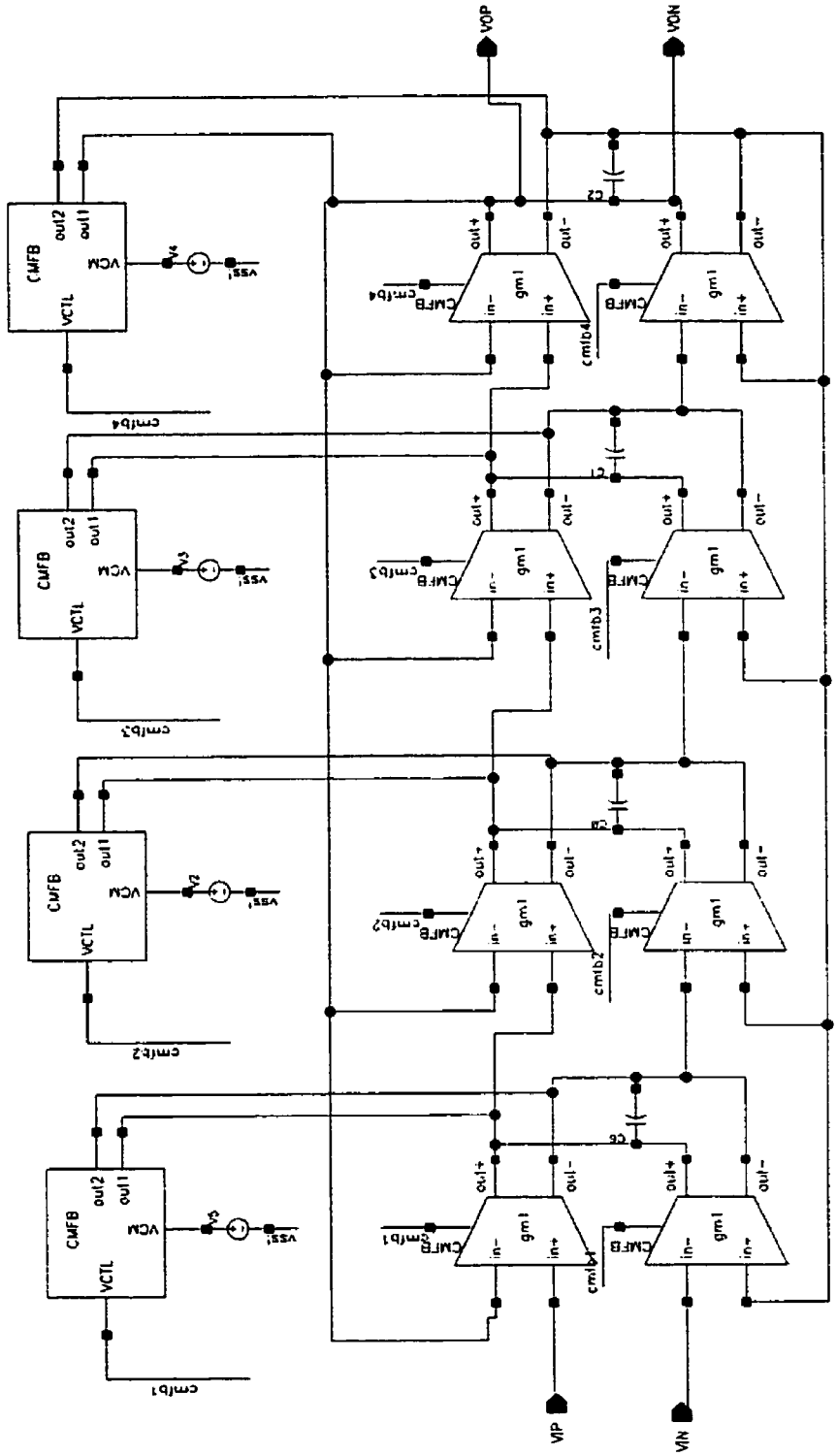

Figure A.21 4th order LP Filter

ANNEX B

HSPICE NETLIST FILE

```
* Project CHOPPER
* Powerview Wirelist Created with Version 6.3.1
*
*  Definition for project INVW
.SUBCKT INVW A YB
* CROSS-REFERENCE 1
* GND = 0
MP01 YB A VDDA VDDA PCH L=5U W=1.1U AS=1.1P AD=1.1P PS=4.2U PD=4.2U NRD=1.818 NRS=1.818
MN02 YB A VSSA VSSA NCH L=10U W=1.1U AS=1.1P AD=1.1P PS=4.2U PD=4.2U NRD=1.818 NRS=1.818
.ENDS

*  Definition for project RTR-OTA
.SUBCKT RTR-OTA BN BP CMFB CN CP PDB VIN VIP VON VOP
* CROSS-REFERENCE 1
* GND = 0
MP1 PO1 VIP PC2 VDDA PCH L=2.8U W=16U M=4 AS=16P AD=16P PS=34U PD=34U NRD=125M NRS=125M
MP2 PO2 VIN PC2 VDDA PCH L=2.8U W=16U M=4 AS=16P AD=16P PS=34U PD=34U NRD=125M NRS=125M
MN3 NO2 VIP NC2 VSSA NCH L=12U W=20U M=4 AS=20P AD=20P PS=42U PD=42U NRD=100M NRS=100M
MN4 NO1 VIN NC2 VSSA NCH L=12U W=20U M=4 AS=20P AD=20P PS=42U PD=42U NRD=100M NRS=100M
MP5 PC1 BP VDDA VDDA PCH L=15U W=40U M=6 AS=40P AD=40P PS=82U PD=82U NRD=50M NRS=50M
MP6 PC2 CP PC1 VDDA PCH L=1.4U W=6U M=6 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MN7 NC2 CN NC1 VSSA NCH L=1.4U W=2U M=6 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MN8 NC1 BN VSSA VSSA NCH L=15U W=20U M=6 AS=20P AD=20P PS=42U PD=42U NRD=100M NRS=100M
MN9 NO1 NO1 FCC1 VSSA NCH L=2U W=4U M=32 AS=4P AD=4P PS=10U PD=10U NRD=500M NRS=500M
MN10 PO3 NO1 FCC2 VSSA NCH L=2U W=4U M=32 AS=4P AD=4P PS=10U PD=10U NRD=500M NRS=500M
MP11 PO1 PO1 FCC1 VDDA PCH L=2U W=6U M=32 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP12 NO3 PO1 FCC2 VDDA PCH L=2U W=6U M=32 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP13 NO1 BP VDDA VDDA PCH L=15U W=40U M=6 AS=40P AD=40P PS=82U PD=82U NRD=50M NRS=50M
MN16 PO1 BN VSSA VSSA NCH L=15U W=20U M=6 AS=20P AD=20P PS=42U PD=42U NRD=100M NRS=100M
MN17 NO2 NO2 FCC3 VSSA NCH L=2U W=4U M=32 AS=4P AD=4P PS=10U PD=10U NRD=500M NRS=500M
MN18 PO4 NO2 FCC4 VSSA NCH L=2U W=4U M=32 AS=4P AD=4P PS=10U PD=10U NRD=500M NRS=500M
MP19 PO2 PO2 FCC3 VDDA PCH L=2U W=6U M=32 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP20 NO4 PO2 FCC4 VDDA PCH L=2U W=6U M=32 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP21 NO2 BP VDDA VDDA PCH L=15U W=40U M=6 AS=40P AD=40P PS=82U PD=82U NRD=50M NRS=50M
MN24 PO2 BN VSSA VSSA NCH L=15U W=20U M=6 AS=20P AD=20P PS=42U PD=42U NRD=100M NRS=100M
MP25 PO3 BP VDDA VDDA PCH L=15U W=40U M=6 AS=40P AD=40P PS=82U PD=82U NRD=50M NRS=50M
MP26 VON CP PO3 VDDA PCH L=1.4U W=4U M=3 AS=4P AD=4P PS=10U PD=10U NRD=500M NRS=500M
MN27 VON CN NO4 VSSA NCH L=1.4U W=2U M=3 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MN28 NO4 CMFB VSSA VSSA NCH L=15U W=20U M=6 AS=20P AD=20P PS=42U PD=42U NRD=100M NRS=100M
MP29 PO4 BP VDDA VDDA PCH L=15U W=40U M=6 AS=40P AD=40P PS=82U PD=82U NRD=50M NRS=50M
MP30 VOP CP PO4 VDDA PCH L=1.4U W=4U M=3 AS=4P AD=4P PS=10U PD=10U NRD=500M NRS=500M
MN31 VOP CN NO3 VSSA NCH L=1.4U W=2U M=3 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MN32 NO3 CMFB VSSA VSSA NCH L=15U W=20U M=6 AS=20P AD=20P PS=42U PD=42U NRD=100M NRS=100M
MN33  CMFB  PD  VSSA  VSSA  NCH  L=0.6U  W=1.6U  AS=1.6P  AD=1.6P  PS=5.2U  PD=5.2U  NRD=1.25
NRS=1.25
XINV1 PDB PD INVW
.ENDS

*  Definition for project LNCMFB
.SUBCKT LNCMFB BP CMFB CP PDB V1 V2 VCM
* CROSS-REFERENCE 1
* GND = 0
MP1 NC1 V1 PC2 VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP2 CMFB VCM PC2 VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP3 CMFB VCM PC4 VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP4 NC1 V2 PC4 VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP5 PC1 BP VDDA VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP6 PC2 CP PC1 VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP7 PC3 BP VDDA VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP8 PC4 CP PC3 VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MN9 CMFB CMFB VSSA VSSA NCH L=15U W=20U M=2 AS=20P AD=20P PS=42U PD=42U NRD=100M NRS=100M
MN10 NC1 NC1 VSSA VSSA NCH L=15U W=20U M=2 AS=20P AD=20P PS=42U PD=42U NRD=100M NRS=100M
MN11 NC1 PD VSSA VSSA NCH L=0.6U W=1.6U AS=1.6P AD=1.6P PS=5.2U PD=5.2U NRD=1.25 NRS=1.25
XINV1 PDB PD INVW
.ENDS
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* Definition for project INV2
.SUBCKT INV2 A YB
* CROSS-REFERENCE 1
* GND = 0
MP01 YB A VDDA VDDA PCH L=0.6U W=3.2U AS=3.2P AD=3.2P PS=8.4U PD=8.4U NRD=625M NRS=625M
MN02 YB A VSSA VSSA NCH L=0.6U W=1.6U AS=1.6P AD=1.6P PS=5.2U PD=5.2U NRD=1.25 NRS=1.25
.ENDS

* Definition for project LNABIAS
.SUBCKT LNABIAS BP CN CP LNBN LNBP PDB
* CROSS-REFERENCE 1
* GND = 0
MN1 NDN1 LNBN VSSA VSSA NCH L=15U W=20U M=2 AS=20P AD=20P PS=42U PD=42U NRD=100M NRS=100M
MP1 NDP1 BP VDDA VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MN2 NDN2 LNBN VSSA VSSA NCH L=15U W=20U M=2 AS=20P AD=20P PS=42U PD=42U NRD=100M NRS=100M
MP2 NDP2 LNBP VDDA VDDA PCH L=15U W=40U M=2 AS=40P AD=40P PS=82U PD=82U NRD=50M NRS=50M
MNC1 LNBN CN NDN1 VSSA NCH L=15U W=20U M=2 AS=20P AD=20P PS=42U PD=42U NRD=100M NRS=100M
MNC2 LNBP CN NDN2 VSSA NCH L=15U W=20U M=2 AS=20P AD=20P PS=42U PD=42U NRD=100M NRS=100M
MNPD2 LNBN PD VSSA VSSA NCH L=0.6U W=1.6U AS=1.6P AD=1.6P PS=5.2U PD=5.2U NRD=1.25
NRS=1.25
MPC1 LNBN CP NDP1 VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M
NRS=333.3M
MPC2 LNBP CP NDP2 VDDA PCH L=15U W=40U M=2 AS=40P AD=40P PS=82U PD=82U NRD=50M NRS=50M
MPPD2 LNBP NPDB VDDA VDDA PCH L=0.6U W=3.2U AS=3.2P AD=3.2P PS=8.4U PD=8.4U NRD=625M
NRS=625M
XINV1 PDB PD INVW
XINV2 PD NPDB INV2
.ENDS

* Definition for project IMPEDANCE
.SUBCKT IMPEDANCE BN BP CN CP VIN VIP
* CROSS-REFERENCE 1
* GND = 0
MP1 VIP VIP PC2 VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP2 VIN VIN PC4 VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP3 PC4 VIP PC2 VDDA PCH L=10U W=1.4U M=1 AS=1.4P AD=1.4P PS=4.8U PD=4.8U NRD=1.429
NRS=1.429
MP4 PC4 VIN PC2 VDDA PCH L=10U W=1.4U M=1 AS=1.4P AD=1.4P PS=4.8U PD=4.8U NRD=1.429
NRS=1.429
MP5 PC1 BP VDDA VDDA PCH L=15U W=40U M=2 AS=40P AD=40P PS=82U PD=82U NRD=50M NRS=50M
MP6 PC2 CP PC1 VDDA PCH L=1.4U W=4U M=2 AS=4P AD=4P PS=10U PD=10U NRD=500M NRS=500M
MP7 PC3 BP VDDA VDDA PCH L=15U W=40U M=2 AS=40P AD=40P PS=82U PD=82U NRD=50M NRS=50M
MP8 PC4 CP PC3 VDDA PCH L=1.4U W=4U M=2 AS=4P AD=4P PS=10U PD=10U NRD=500M NRS=500M
MN9 VIP CN NC1 VSSA NCH L=1.4U W=2U M=2 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MN10 NC1 BN VSSA VSSA NCH L=15U W=20U M=2 AS=20P AD=20P PS=42U PD=42U NRD=100M NRS=100M
MN11 VIN CN NC2 VSSA NCH L=1.4U W=2U M=2 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MN12 NC2 BN VSSA VSSA NCH L=15U W=20U M=2 AS=20P AD=20P PS=42U PD=42U NRD=100M NRS=100M
.ENDS

* Definition for project LNARDA01
.SUBCKT LNARDA01 BP CN CP PDB VCM VIN VIP VON VOP
* CROSS-REFERENCE 1
* GND = 0
XIMPEDANCE LNBN LNBP CN CP VON VOP IMPEDANCE
XLNABIAS BP CN CP LNBN LNBP PDB LNABIAS
XLNCMFB LNBP CMFB CP PDB VOP VON VCM LNCMFB
XRTROTA LNBN LNBP CMFB CN CP PDB VIN VIP VON VOP RTR-OTA
.ENDS

* Definition for project INPUTGM
.SUBCKT INPUTGM BP CMFB CN CP VIN VIP VON VOP
* CROSS-REFERENCE 1
* GND = 0
MP1 VON VIP PC2 VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP2 VOP VIN PC4 VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP3 PC4 VIP PC2 VDDA PCH L=1.4U W=6U M=1 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
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MP4 PC4 VIN PC2 VDDA PCH L=1.4U W=6U M=1 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP5 PC1 BP VDDA VDDA PCH L=1.4U W=6U M=4 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP6 PC2 CP PC1 VDDA PCH L=1.4U W=6U M=4 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP7 PC3 BP VDDA VDDA PCH L=1.4U W=6U M=4 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP8 PC4 CP PC3 VDDA PCH L=1.4U W=6U M=4 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MN9 VON CN NC1 VSSA NCH L=1.4U W=2U M=4 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MN10 NC1 CMFB VSSA VSSA NCH L=1.4U W=2U M=4 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MN11 VOP CN NC2 VSSA NCH L=1.4U W=2U M=4 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MN12 NC2 CMFB VSSA VSSA NCH L=1.4U W=2U M=4 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
.ENDS

* Definition for project CMFB
.SUBCKT CMFB BP CMFB CP PDB V1 V2 VCM
* CROSS-REFERENCE 1
* GND = 0
MP1 NC1 V1 PC2 VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP2 CMFB VCM PC2 VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP3 CMFB VCM PC4 VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP4 NC1 V2 PC4 VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP5 PC1 BP VDDA VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP6 PC2 CP PC1 VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP7 PC3 BP VDDA VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP8 PC4 CP PC3 VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MN9 CMFB CMFB VSSA VSSA NCH L=1.4U W=2U M=2 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MN10 NC1 NC1 VSSA VSSA NCH L=1.4U W=2U M=2 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MN11 NC1 PD VSSA VSSA NCH L=0.6U W=1.6U AS=1.6P AD=1.6P PS=5.2U PD=5.2U NRD=1.25 NRS=1.25
XINV1 PDB PD INVW
.ENDS

* Definition for project RESONANTGM
.SUBCKT RESONANTGM BP CMFB CN CP VIN VIP VON VOP
* CROSS-REFERENCE 1
* GND = 0
MP1 VON VIP PC2 VDDA PCH L=5U W=12U M=1 AS=12P AD=12P PS=26U PD=26U NRD=166.7M NRS=166.7M
MP2 VOP VIN PC4 VDDA PCH L=5U W=12U M=1 AS=12P AD=12P PS=26U PD=26U NRD=166.7M NRS=166.7M
MP3 PC4 VIP PC2 VDDA PCH L=5U W=6U M=1 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP4 PC4 VIN PC2 VDDA PCH L=5U W=6U M=1 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP5 PC1 BP VDDA VDDA PCH L=1.4U W=6U M=1 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP6 PC2 CP PC1 VDDA PCH L=1.4U W=6U M=1 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP7 PC3 BP VDDA VDDA PCH L=1.4U W=6U M=1 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP8 PC4 CP PC3 VDDA PCH L=1.4U W=6U M=1 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MN9 VON CN NC1 VSSA NCH L=1.4U W=2U M=1 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MN10 NC1 CMFB VSSA VSSA NCH L=1.4U W=2U M=1 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MN11 VOP CN NC2 VSSA NCH L=1.4U W=2U M=1 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MN12 NC2 CMFB VSSA VSSA NCH L=1.4U W=2U M=1 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
.ENDS

* Definition for project OUTPUTGM
.SUBCKT OUTPUTGM BP CMFB CN CP VIN VIP VON VOP
* CROSS-REFERENCE 1
* GND = 0
MP1 VON VIP PC2 VDDA PCH L=2U W=4U M=1 AS=4P AD=4P PS=10U PD=10U NRD=500M NRS=500M
MP2 VOP VIN PC4 VDDA PCH L=2U W=4U M=1 AS=4P AD=4P PS=10U PD=10U NRD=500M NRS=500M
MP3 PC4 VIP PC2 VDDA PCH L=20U W=1.4U M=1 AS=1.4P AD=1.4P PS=4.8U PD=4.8U NRD=1.429
NRS=1.429
MP4 PC4 VIN PC2 VDDA PCH L=20U W=1.4U M=1 AS=1.4P AD=1.4P PS=4.8U PD=4.8U NRD=1.429
NRS=1.429
MP5 PC1 BP VDDA VDDA PCH L=1.4U W=4.5U M=1 AS=4.5P AD=4.5P PS=11U PD=11U NRD=444.4M
NRS=444.4M
MP6 PC2 CP PC1 VDDA PCH L=1.4U W=4.5U M=1 AS=4.5P AD=4.5P PS=11U PD=11U NRD=444.4M
NRS=444.4M
MP7 PC3 BP VDDA VDDA PCH L=1.4U W=4.5U M=1 AS=4.5P AD=4.5P PS=11U PD=11U NRD=444.4M
NRS=444.4M
MP8 PC4 CP PC3 VDDA PCH L=1.4U W=4.5U M=1 AS=4.5P AD=4.5P PS=11U PD=11U NRD=444.4M
NRS=444.4M
MN9 VON CN NC1 VSSA NCH L=1.4U W=1.5U M=1 AS=1.5P AD=1.5P PS=5U PD=5U NRD=1.333 NRS=1.333
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MN10 NC1 CMFB VSSA VSSA NCH L=1.4U W=1.5U M=1 AS=1.5P AD=1.5P PS=5U PD=5U NRD=1.333
NRS=1.333
MN11 VOP CN NC2 VSSA NCH L=1.4U W=1.5U M=1 AS=1.5P AD=1.5P PS=5U PD=5U NRD=1.333
NRS=1.333
MN12 NC2 CMFB VSSA VSSA NCH L=1.4U W=1.5U M=1 AS=1.5P AD=1.5P PS=5U PD=5U NRD=1.333
NRS=1.333
.ENDS

* Definition for project BPF2ND
.SUBCKT BPF2ND BP CN CP LCBN LCBP PDB VCM VIN VIP VON VOP
* CROSS-REFERENCE 1
* GND = 0
C1 VOP VON 20P
C2 OLP OLN 20P
XCMFB1 BP CMFB1 CP PDB VOP VON VCM CMFB
XCMFB2 BP CMFB2 CP PDB OLP OLN VCM CMFB
XGM1 BP CMFB1 CN CP VIN VIP VON VOP INPUTGM
XGM2 LCBP CMFB2 CN CP VON VOP OLP OLN RESONANTGM
XGM3 LCBP LCBN CN CP OLN OLP VON VOP RESONANTGM
XGM4 LCBP LCBN CN CP VON VOP VOP VON OUTPUTGM
.ENDS

* Definition for project INV
.SUBCKT INV A YB
* CROSS-REFERENCE 1
* GND = 0
MP01 YB A VDDA VDD PCH L=0.35U W=3U AS=3P AD=3P PS=8U PD=8U NRD=666.7M NRS=666.7M
MN02 YB A VSSA VSS NCH L=0.35U W=1U AS=1P AD=1P PS=4U PD=4U NRD=2 NRS=2
.ENDS

* Definition for project INMODU
.SUBCKT INMODU CLK1 CLK1B CLK2 CLK2B VIN VIP VON VOP
* CROSS-REFERENCE 1
* GND = 0
MN1 VDD G2 G1 VSS NCH L=0.35U W=1U AS=1P AD=1P PS=4U PD=4U NRD=2 NRS=2
MN2 VDD G1 G2 VSS NCH L=0.35U W=1U AS=1P AD=1P PS=4U PD=4U NRD=2 NRS=2
MN3 VDD G1 N1 VSS NCH L=0.35U W=1U AS=1P AD=1P PS=4U PD=4U NRD=2 NRS=2
MN4 N2 CLK1B 0 VSS NCH L=0.35U W=1U AS=1P AD=1P PS=4U PD=4U NRD=2 NRS=2
MN5 G3 CLK1 N2 VSS NCH L=0.35U W=1U AS=1P AD=1P PS=4U PD=4U NRD=2 NRS=2
MP6 G3 CLK1 VDD VDD PCH L=0.35U W=2U AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MP7 CLKO G3 N1 N1 PCH L=0.35U W=3U AS=3P AD=3P PS=8U PD=8U NRD=666.7M NRS=666.7M
MN8 VIP CLKO N2 VSS NCH L=0.35U W=1U AS=1P AD=1P PS=4U PD=4U NRD=2 NRS=2
MN9 VOP CLKO VIP VSS NCH L=0.35U W=2U AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MN10 CLKO CLK1B 0 VSS NCH L=0.35U W=1U AS=1P AD=1P PS=4U PD=4U NRD=2 NRS=2
MN11 VDD G4 G5 VSS NCH L=0.35U W=1U AS=1P AD=1P PS=4U PD=4U NRD=2 NRS=2
MN12 VDD G5 G4 VSS NCH L=0.35U W=1U AS=1P AD=1P PS=4U PD=4U NRD=2 NRS=2
MN13 VDD G5 N3 VSS NCH L=0.35U W=1U AS=1P AD=1P PS=4U PD=4U NRD=2 NRS=2
MN15 G6 CLK2 N4 VSS NCH L=0.35U W=1U AS=1P AD=1P PS=4U PD=4U NRD=2 NRS=2
MP16 G6 CLK2 VDD VDD PCH L=0.35U W=2U AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MP17 CLKOB G6 N3 N3 PCH L=0.35U W=3U AS=3P AD=3P PS=8U PD=8U NRD=666.7M NRS=666.7M
MN18 VIP CLKOB N4 VSS NCH L=0.35U W=1U AS=1P AD=1P PS=4U PD=4U NRD=2 NRS=2
MN19 CLKOB CLK2B 0 VSS NCH L=0.35U W=1U AS=1P AD=1P PS=4U PD=4U NRD=2 NRS=2
MN20 VON CLKOB VIP VSS NCH L=0.35U W=2U AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MN21 VON CLKO VIN VSS NCH L=0.35U W=2U AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MN22 VOP CLKOB VIN VSS NCH L=0.35U W=2U AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MN23 VOP CLKON VOP VSS NCH L=0.35U W=1U AS=1P AD=1P PS=4U PD=4U NRD=2 NRS=2
MN24 VON CLKON VON VSS NCH L=0.35U W=1U AS=1P AD=1P PS=4U PD=4U NRD=2 NRS=2
MN25 VON CLKOBN VON VSS NCH L=0.35U W=1U AS=1P AD=1P PS=4U PD=4U NRD=2 NRS=2
MN26 VOP CLKOBN VOP VSS NCH L=0.35U W=1U AS=1P AD=1P PS=4U PD=4U NRD=2 NRS=2
C1 G1 CLK1B 1P
C2 G2 NC1 1P
C3 N1 N2 1P
C4 G5 CLK2B 1P
C5 G4 NC2 1P
C6 N3 N4 1P
M0 N4 CLK2B 0 VSS NCH L=0.35U W=1U AS=1P AD=1P PS=4U PD=4U NRD=2 NRS=2
X1I195 CLK2B NC2 INV
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X1I252 CLKO CLKON INV
X1I269 CLKOB CLKOBN INV
X1I5 CLK1B NC1 INV
.ENDS

* Definition for project CKDRIV
.SUBCKT CKDRIV CK CKB Y YB
* CROSS-REFERENCE 1
* GND = 0
MP1 N1 XB VDD VDD PCH L=0.35U W=1.8U M=5 AS=1.8P AD=1.8P PS=5.6U PD=5.6U NRD=1.111
NRS=1.111
MP2 N1 X VDD VDD PCH L=0.35U W=1.8U M=5 AS=1.8P AD=1.8P PS=5.6U PD=5.6U NRD=1.111
NRS=1.111
MP3 XB CK N1 VDD PCH L=0.35U W=1.8U M=6 AS=1.8P AD=1.8P PS=5.6U PD=5.6U NRD=1.111
NRS=1.111
MP4 X CKB N1 VDD PCH L=0.35U W=1.8U M=6 AS=1.8P AD=1.8P PS=5.6U PD=5.6U NRD=1.111
NRS=1.111
MN5 XB CK N2 VSS NCH L=0.35U W=1.8U M=1 AS=1.8P AD=1.8P PS=5.6U PD=5.6U NRD=1.111
NRS=1.111
MN6 X CKB N2 VSS NCH L=0.35U W=1.8U M=1 AS=1.8P AD=1.8P PS=5.6U PD=5.6U NRD=1.111
NRS=1.111
MN7 N2 XB VSS VSS NCH L=0.35U W=1.8U M=1 AS=1.8P AD=1.8P PS=5.6U PD=5.6U NRD=1.111
NRS=1.111
MN8 N2 X VSS VSS NCH L=0.35U W=1.8U M=1 AS=1.8P AD=1.8P PS=5.6U PD=5.6U NRD=1.111
NRS=1.111
MP9 N3 Y VDD VDD PCH L=0.35U W=1.8U M=5 AS=1.8P AD=1.8P PS=5.6U PD=5.6U NRD=1.111
NRS=1.111
MP10 N3 YB VDD VDD PCH L=0.35U W=1.8U M=5 AS=1.8P AD=1.8P PS=5.6U PD=5.6U NRD=1.111
NRS=1.111
MP11 Y XB N3 VDD PCH L=0.35U W=1.8U M=6 AS=1.8P AD=1.8P PS=5.6U PD=5.6U NRD=1.111
NRS=1.111
MP12 YB X N3 VDD PCH L=0.35U W=1.8U M=6 AS=1.8P AD=1.8P PS=5.6U PD=5.6U NRD=1.111
NRS=1.111
MN13 Y XB N4 VSS NCH L=0.35U W=1.8U M=1 AS=1.8P AD=1.8P PS=5.6U PD=5.6U NRD=1.111
NRS=1.111
MN14 YB X N4 VSS NCH L=0.35U W=1.8U M=1 AS=1.8P AD=1.8P PS=5.6U PD=5.6U NRD=1.111
NRS=1.111
MN15 N4 Y VSS VSS NCH L=0.35U W=1.8U M=1 AS=1.8P AD=1.8P PS=5.6U PD=5.6U NRD=1.111
NRS=1.111
MN16 N4 YB VSS VSS NCH L=0.35U W=1.8U M=1 AS=1.8P AD=1.8P PS=5.6U PD=5.6U NRD=1.111
NRS=1.111
.ENDS

* Definition for project NOR2
.SUBCKT NOR2 A B YB
* CROSS-REFERENCE 1
* GND = 0
MP01 N01 A VDD VDD PCH L=0.35U W=2U AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MP02 YB B N01 VDD PCH L=0.35U W=2U AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MN03 YB A VSS VSS NCH L=0.35U W=1U AS=1P AD=1P PS=4U PD=4U NRD=2 NRS=2
MN04 YB B VSS VSS NCH L=0.35U W=1U AS=1P AD=1P PS=4U PD=4U NRD=2 NRS=2
C01 N01 VDD 10FF
.ENDS

* Definition for project FOURCLKS
.SUBCKT FOURCLKS CLK1 CLK1B CLK2 CLK2B CLKIN
* CROSS-REFERENCE 1
* GND = 0
X1I30 QB NC2 CLK2 CLK2B CKDRIV
X1I31 QB NC2 INV
X1I32 Q NC1 INV
X1I35 Q NC1 CLK1 CLK1B CKDRIV
XINV1 CLKIN CLKINN INV
XINV2 NA1 NA2 INV
XINV3 NA2 Q INV
XINV4 NB1 NB2 INV
XINV5 NB2 QB INV
```

```
XNOR2A CLKIN QB NA1 NOR2
XNOR2B Q CLKINN NB1 NOR2
.ENDS

* Definition for project GNL
.SUBCKT GNL BN BP CN CP VIN VIP
* CROSS-REFERENCE 1
* GND = 0
MP1 VIP VIP PC2 PC2 PCH L=1.4U W=2U M=1 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MP2 VIN VIN PC4 PC4 PCH L=1.4U W=2U M=1 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MP3 PC4 VIP PC2 VDDA PCH L=6U W=6U M=1 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP4 PC4 VIN PC2 VDDA PCH L=6U W=6U M=1 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP5 PC1 BP VDDA VDDA PCH L=1.4U W=6U M=4 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP6 PC2 CP PC1 VDDA PCH L=1.4U W=6U M=4 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP7 PC3 BP VDDA VDDA PCH L=1.4U W=6U M=4 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP8 PC4 CP PC3 VDDA PCH L=1.4U W=6U M=4 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MN9 VIP CN NC1 VSSA NCH L=1.4U W=2U M=5 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MP9 PC5 BP VDDA VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MN10 NC1 BN VSSA VSSA NCH L=1.4U W=2U M=5 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MP10 PC6 CP PC5 VDDA PCH L=1.4U W=6U M=2 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MN11 VIN CN NC2 VSSA NCH L=1.4U W=2U M=5 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MP11 VIN VIP PC6 VDDA PCH L=1.4U W=6U M=4 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MN12 NC2 BN VSSA VSSA NCH L=1.4U W=2U M=5 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MP12 VIP VIN PC6 VDDA PCH L=1.4U W=6U M=4 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
.ENDS

* Definition for project DIF-SING
.SUBCKT DIF-SING BP CN CP PDB VIN VIP VOP
* CROSS-REFERENCE 1
* GND = 0
MP1 SBP VIP PC2 VDDA PCH L=1.4U W=6U M=4 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP2 NOP VIN PC2 VDDA PCH L=1.4U W=6U M=4 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP3 PC1 BP VDDA VDDA PCH L=1.4U W=6U M=4 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MP4 PC2 CP PC1 VDDA PCH L=1.4U W=6U M=4 AS=6P AD=6P PS=14U PD=14U NRD=333.3M NRS=333.3M
MN5 SBP CN NC1 VSSA NCH L=1.4U W=2U M=4 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MN6 NC1 SBP VSSA VSSA NCH L=1.4U W=2U M=4 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MN7 NOP CN NC2 VSSA NCH L=1.4U W=2U M=4 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MN8 NC2 SBP VSSA VSSA NCH L=1.4U W=2U M=4 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
MN9 SBP PD VSSA VSSA NCH L=0.6U W=1.6U AS=1.6P AD=1.6P PS=5.2U PD=5.2U NRD=1.25 NRS=1.25
X1I36 NOP NON INV
X1I37 NON VOP INV
XINV1 PDB PD INVW
.ENDS

* Definition for project OSCILLATOR
.SUBCKT OSCILLATOR BN BP CN CP LCBP PDB VCM VOP
* CROSS-REFERENCE 1
* GND = 0
C1 OOP OON 20P
C2 OLP OLN 20P
XCMFB1 BP CMFB2 CP PDB OLP OLN VCM CMFB
XCMFB2 BP CMFB1 CP PDB OOP OON VCM CMFB
XDIFSING BP CN CP PDB OON OOP VOP DIF-SING
XGM2 LCBP CMFB2 CN CP OON OOP OLP OLN RESONANTGM
XGM3 LCBP CMFB1 CN CP OLN OLP OON OOP RESONANTGM
XGNL BN BP CN CP OOP OON GNL
.ENDS

* Definition for project TRGATEDS
.SUBCKT TRGATEDS CLKN IN OUT
* CROSS-REFERENCE 1
* GND = 0
MN1 IN CLKN OUT VSSA NCH L=0.6U W=4U M=1 AS=4P AD=4P PS=10U PD=10U NRD=500M NRS=500M
MN2 OUT CLKB OUT VSSA NCH L=0.6U W=2U M=1 AS=2P AD=2P PS=6U PD=6U NRD=1 NRS=1
X1I41 CLKN CLKB INV
.ENDS
```

```
*  Definition for project DEMOD
.SUBCKT DEMOD NCLKP PCLKP VIN VIP VON VOP
* CROSS-REFERENCE 1
* GND = 0
XTRAN1 PCLKP VIP VOP TRGATEDS
XTRAN2 PCLKP VIN VON TRGATEDS
XTRAN3 NCLKP VIP VON TRGATEDS
XTRAN4 NCLKP VIN VOP TRGATEDS
.ENDS

XRTROP BP CN CP PDB VCM MON MOP RON ROP LNARDA01
XBPF BP CN CP BN BP PDB VCM RON ROP FON FOP BPF2ND
XMOD PCLKP PCLKN NCLKP NCLKN VIN VIP MON MOP INMODU
XCLKGEN PCLKP PCLKN NCLKP NCLKN CLKIN FOURCLKS
XOSC BN BP CN CP BP PDB VCM CLKIN OSCILLATOR
XDEMOD NCLKP PCLKP FON FOP VON VOP DEMOD
* DICTIONARY 1
* GND = 0
.GLOBAL VDDA
.GLOBAL VSSA
.GLOBAL VDD
.GLOBAL VSS
.OPTIONS INGOLD=2
.END
```

ANNEX C

LAYOUTS

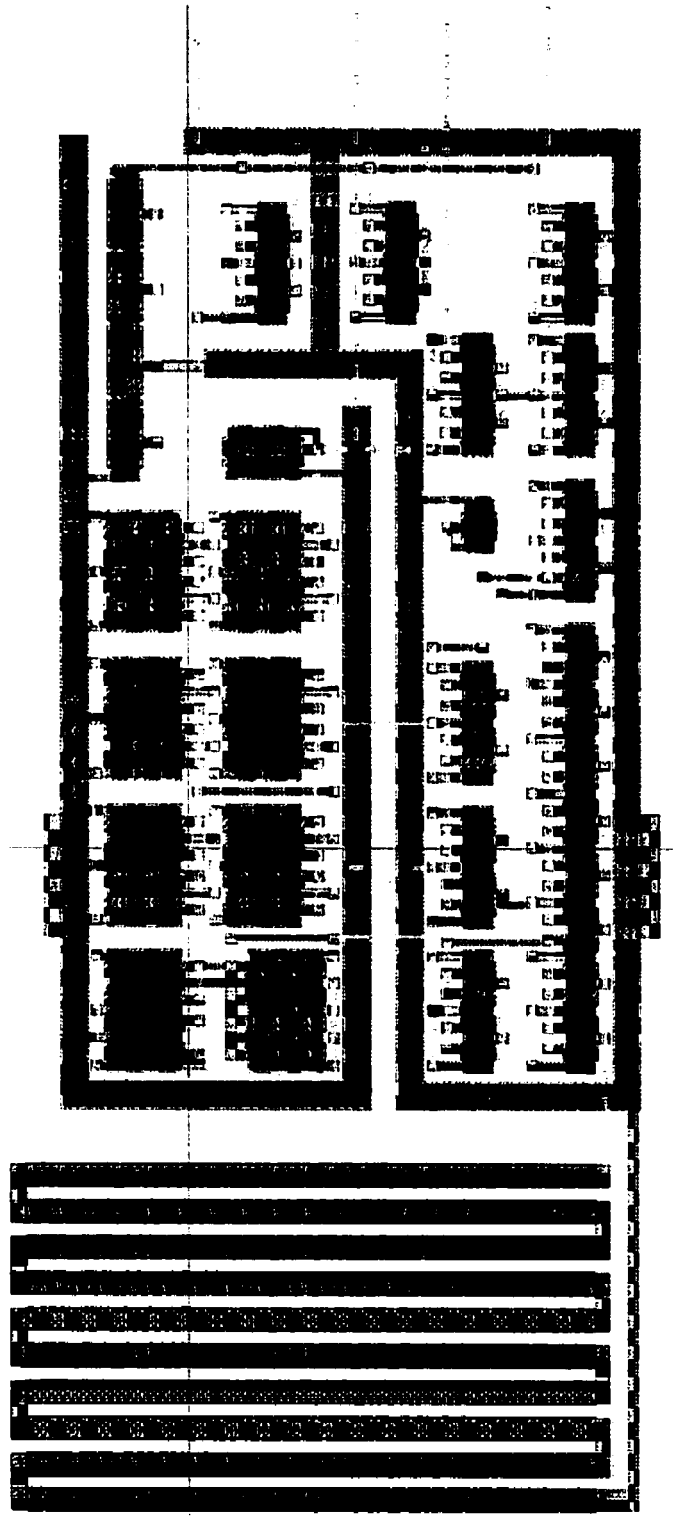

Figure C.1 BiAS

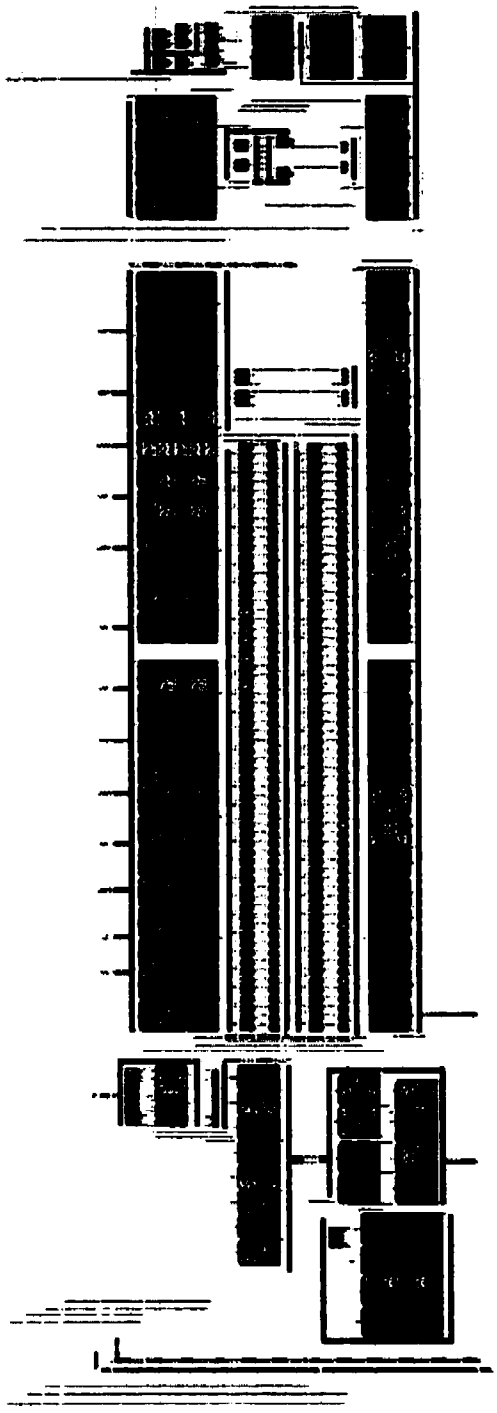

Figure C.2 Low Noise Amplifier

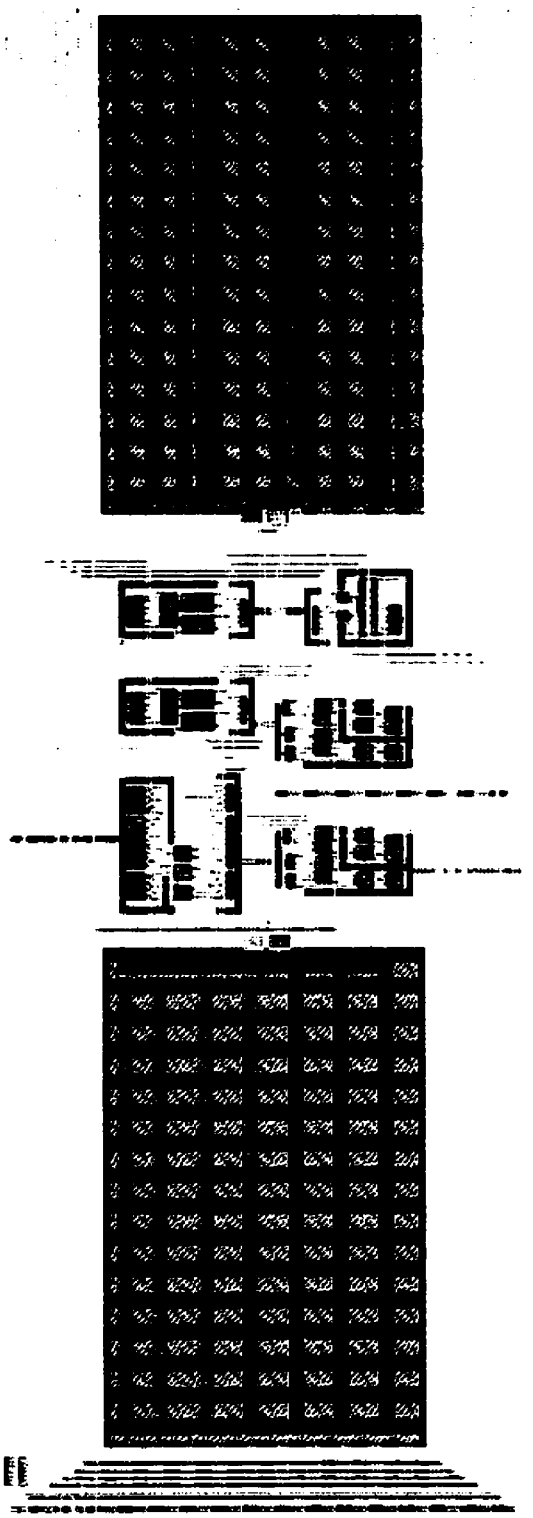

Figure C.3 Bandpass Filter

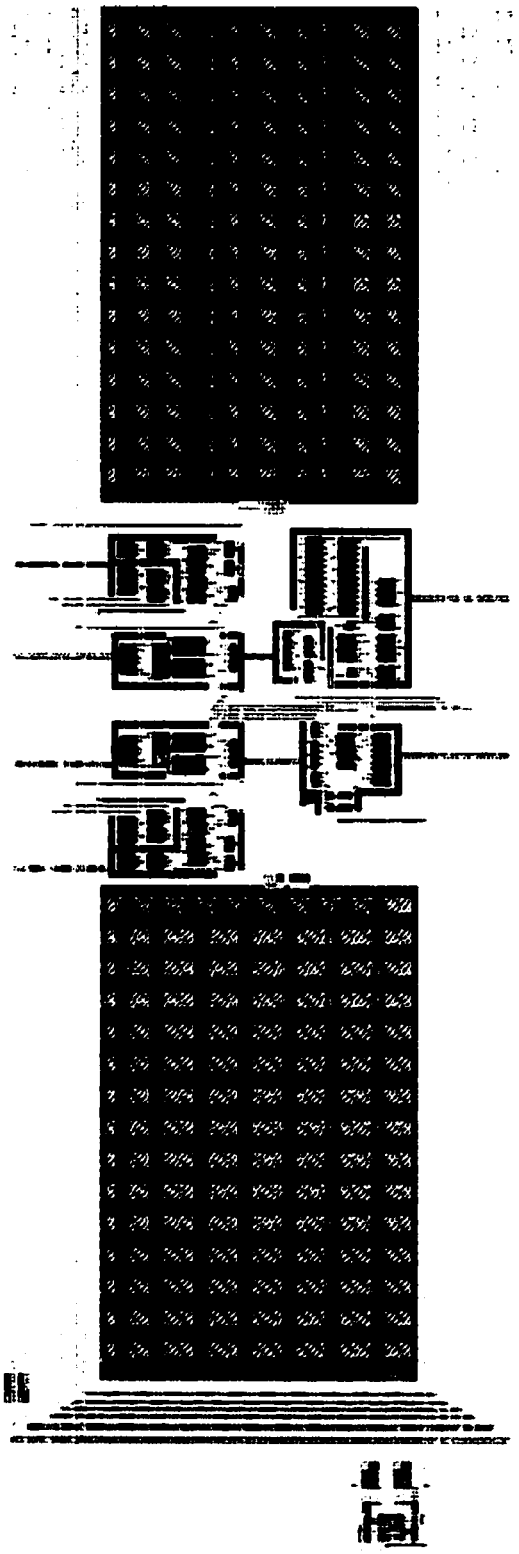

Figure C.4 Oscilator

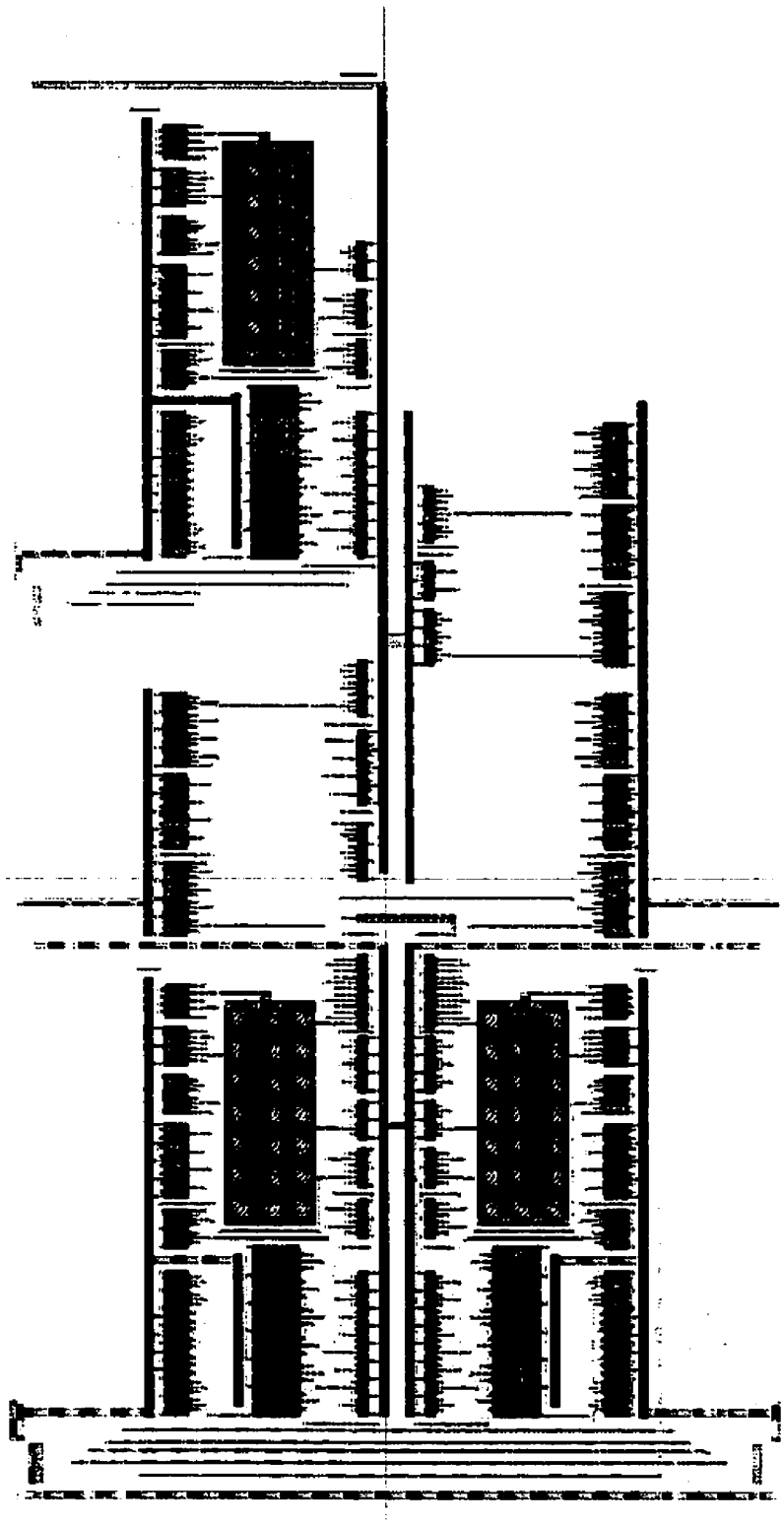

Figure C.5 Instrumentation Amplifier

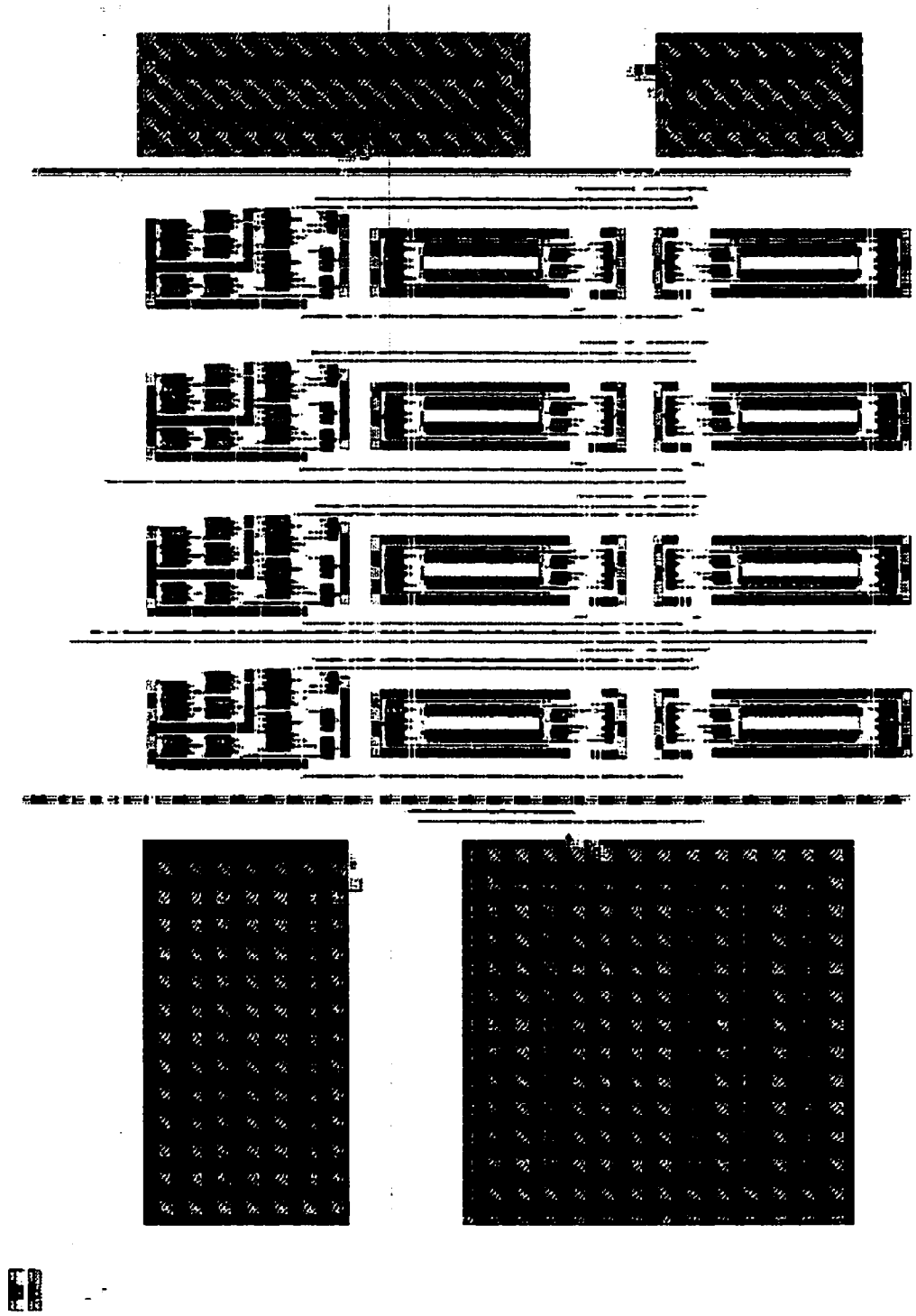

Figure C.6 4th order Lowpass Filter

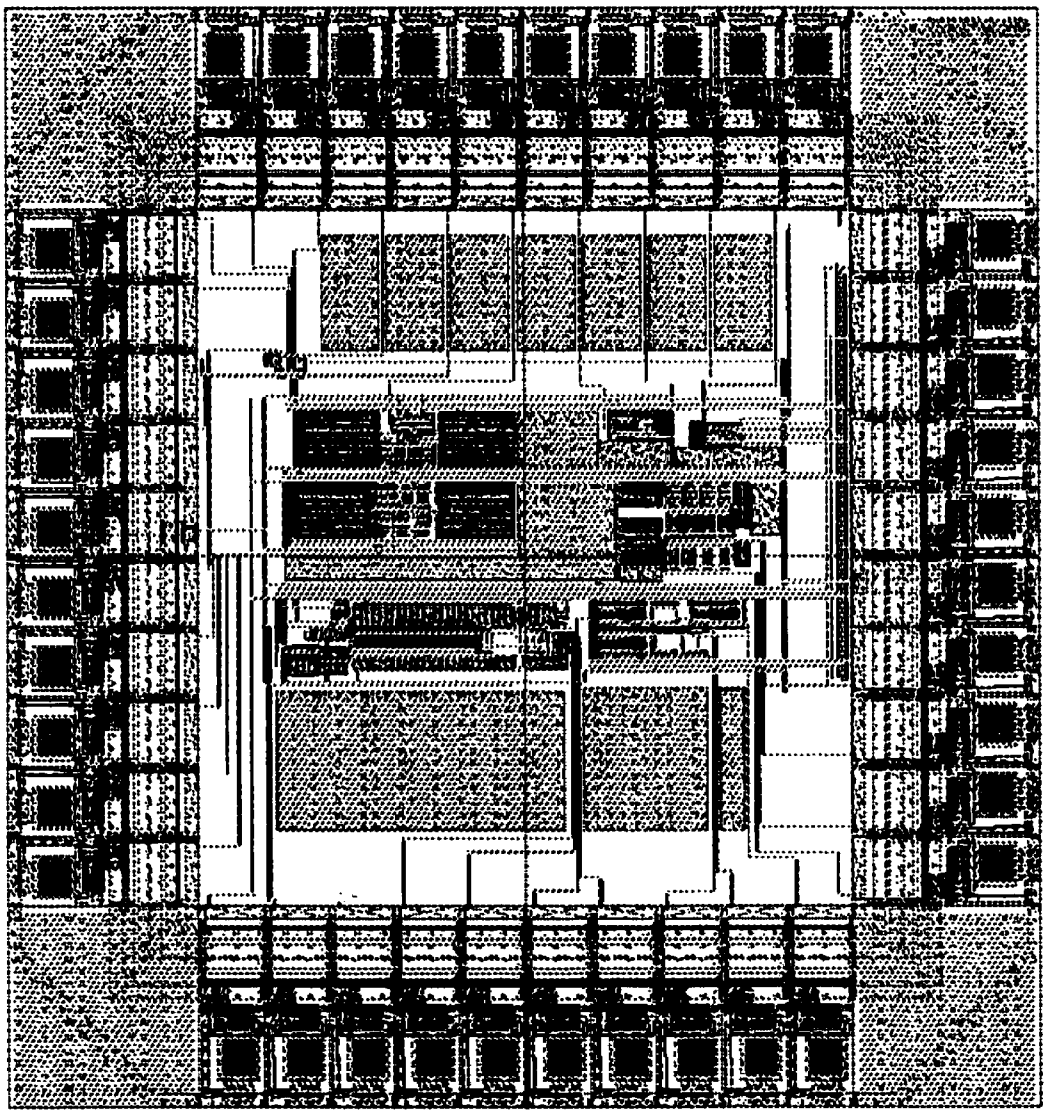

Figure C.7 Chip layout

ANNEX D

INSTRUMENTATION AMPLIFIER & OUTPUT LOW-PASS FILTER

Instrumentation amplifier

The instrumentation amplifier (IA) is an important component in a signal conditional circuit. The signal that output from CHS need to be further amplified by the IA. An amplifier with programmable gain, high input resistance and high CMRR is an instrumentation amplifier (IA). The most common configuration is the three-op-amp based differential amplifier [41]. A good CMRR performance is related to resistor matching. Some resistors must be trimmed accurately to reduce the common-mode gain hence increasing the cost of the IA. A kind of novel instrumentation amplifier has been proposed by Harb et. Sawan [27] whose structure is presented in figure D.1.

The current mirrors CM_1 and CM_2 measure the output stage current supply which is equal to the current flowing into the load resistor R_l ($I_R = I_l = -I_2$). The voltage gain can be found as [27]:

$$\frac{V_{out}}{V_{in}} = \frac{V_{out}}{V_+ - V_-} = 2 \times K = 2 \times \frac{R_g}{R_1} \qquad \text{(E.1)}$$

where R_g is the programmable gain resistor. The new design does not require the expensive on-chip resistance trimming because the CMRR depends on the current mirror. The detailed IA circuits are presented in Appendix A.

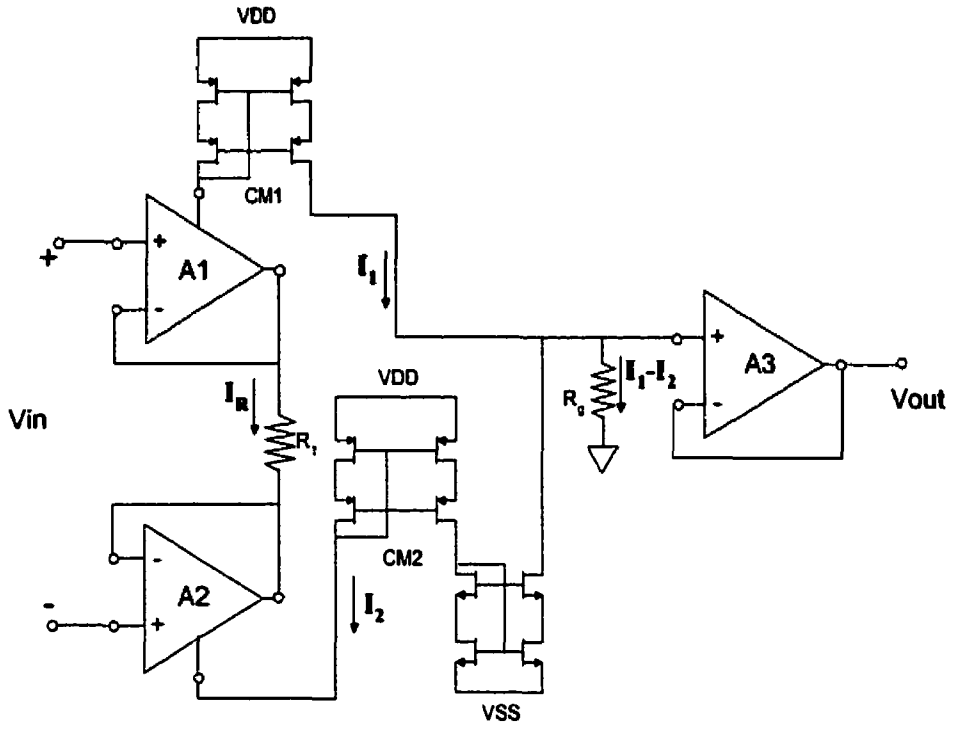

Figure D.1 Topology of the Instrumentation Amplifier (IA).

Output Low-pass filter

The output signal came from CHS contains all the harmonics and shifted flicker noise. To obtain a clean output, a low pass filter whose cut-off frequency is smaller than half of the modulating frequency is needed. Here, a 4^{th} order butterworth continuous filter with cut-off frequency 10 kHz is used. Its transfer function is presented in equation (E.2). The block scheme is shown in figure D.2. The same transconductor structure and common feedback circuit can be adopted. Detailed circuits are given in the Appendix A.

$$H(s)=\frac{10^{16}}{s^4+2.6131\times10^4 s^3+3.4142\times10^8 s^2+2.6131\times10^{12}s+10^{16}} \qquad \text{(E.2)}$$

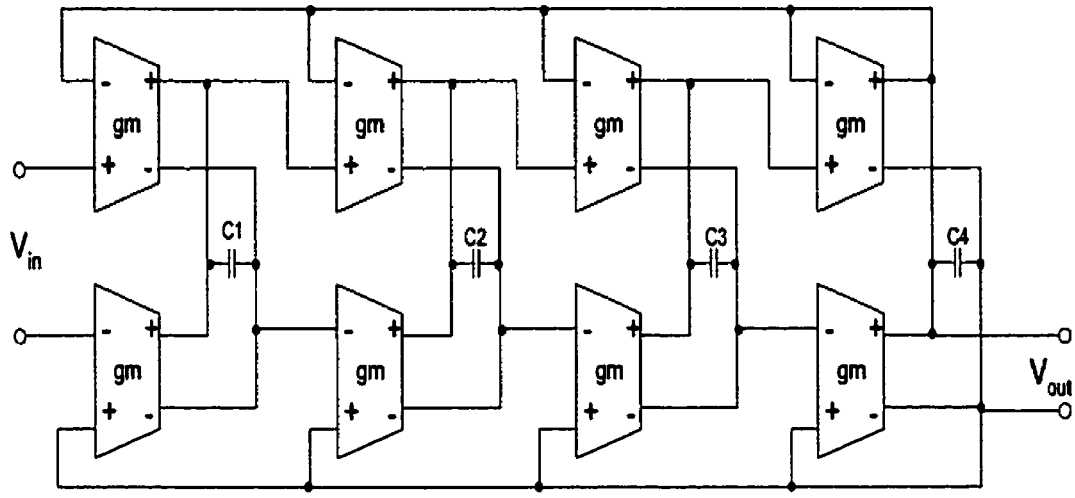

Figure D.2 Block Scheme of the 4th order LP filter