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PRECISION RAIL-TO-RAIL INPUT-OUTPUT OPERATIONAL AMPLIFIER USING LASER-TRIMMABLE POLY-SILICON RESISTORS IN STANDARD CMOS PROCESS

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Ce mémoire intitulé:

PRECISION RAIL-TO-RAIL INPUT-OUTPUT OPERATIONAL AMPLIFIER USING LASER-TRIMMABLE POLY-SILICON RESISTORS IN STANDARD CMOS PROCESS

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To my parents

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RESUMÉ

On retrouve les amplificateurs opérationnels de précision dans beaucoup d'applications, notamment sur des systèmes à base de détecteurs, sur des dispositifs industriels de commande et sur des amplificateurs d'instrumentation, bref partout où un niveau important d'exactitude dans la mesure est nécessaire. Un paramètre important d'un amplificateur de précision est la tension de décalage référée à l'entrée, qui détermine l'exactitude de la tension continue de sortie. Le mésappariement des composants critiques et le stress mécanique induit lors de l'encapsulation augmentent la tension de décalage. De plus, les variations de température provoquent une dérive de celle-ci. Afin de réduire cette tension indésirable, la plupart des amplificateurs commerciaux de précision emploient une technique d'ajustement de résistances. L'ajustement au laser en temps réel de résistances intégrées à même le circuit d'amplificateur est l'une de ces méthodes.

Ce mémoire porte sur un amplificateur opérationnel de précision à pleine gamme dynamique en entrée et en sortie ayant des résistances de silicium polycristallin (poly-silicium) ajustable par faisceau laser. Une méthode d'ajustement au laser de résistances de poly-silicium de type P tout à fait compatible avec les procédés de fabrication CMOS standard est employée. Une analyse de circuit est présentée pour développer une séquence d'ajustement des résistances de façon à réduire la tension de décalage sur toute la gamme dynamique de la tension d'entrée en mode commun, allant de V_{SS} à V_{DD}. Un circuit de polarisation robuste aux variations de la tension d'alimentation et au changement de température a été conçu pour permettre à l'amplificateur de fonctionner sur une gamme de -40^0C à $+85^0$C.

Le circuit a été fabriqué en technologie CMOS 0.18 µm de la TSMC et fonctionne à partir d'une alimentation simple de 3.3 V. Les résultats de tests sont présentés et démontrent son bon fonctionnement. Les résultats expérimentaux de la méthode de diminution de la tension de décalage par ajustement au laser de résistances en poly-silicium sont également présentés. La méthode employée sur cinq

échantillons montre une tension de décalage finale de moins de 30 μV pour une tension d'entrée mode commun centrée à 1.65 V et de 110 μV sur la toute la gamme dynamique de la tension d'entrée (3.3V) en mode commun.

ABSTRACT

Precision operational amplifiers have many applications in sensor-based systems found in industrial control and instrumentation devices, where a high degree of accuracy is needed for measurement. An important parameter of a precision amplifier is the input referred offset voltage, which is used to determine its DC accuracy. Device mismatch and package induced mechanical stress on the die have an influence on the input offset voltage. Furthermore, the temperature variations in the operating environment can affect the associated drift of offset voltage. These factors tend to limit the DC accuracy and the dynamic range of an amplifier utilized for high precision applications. To overcome this performance issue, most commercial precision amplifiers exploit an integrated circuit (IC) trimming technique that can reduce the initial input offset voltage. Continuous-time laser trimming of resistors at wafer level is one such IC trimming method.

The dissertation presents the design of a standalone precision CMOS rail-to-rail input-output (I/O) operational amplifier with embedded laser-trimable poly silicon resistors. The work investigates a method of laser trimming of P-type poly silicon resistors compatible with standard-CMOS processes for reducing the input offset voltage. An analysis is presented to develop the trimming sequence methodology in order to reduce the input offset voltage over the full input common mode range of a rail-to-rail input stage. An on-chip PTAT bias circuitry is also designed to maintain the performance of the amplifier over process variations and operate over a range of -40^0C to $+85^0$C.

The circuit is implemented using the TSMC 0.18 μm CMOS process and operates from a single supply of 3.3V. Test results have been presented and show a successful implementation of the amplifier at silicon level. Also, the experimental trimming sequence methodology has been proven successful. Laser-trimmed offset voltages of less than 30 μV at mid-supply and 110 μV over the entire input common mode range have been achieved for various samples of the amplifier.

CONDENSÉ EN FRANÇAIS

Introduction

Les deux principaux objectifs de ce travail ont été de 1) Concevoir un amplificateur opérationnel à pleine gamme dynamique en entrée et en sortie (de V_{SS} à V_{DD}) à base d'un procédé CMOS standard incluant un circuit de polarisation PTAT (Proportional-To-Absolute-Temperature); 2) minimiser la tension de décalage de l'amplificateur par une technique d'ajustement de résistances au silicium poly-cristallin (poly-silicium) à l'aide d'un rayon laser. Les résistances au poly silicium font partie du circuit d'amplification afin de réduire la tension de décalage et d'augmenter la précision de la tension continue (CC) de sortie lorsque l'amplificateur fonctionne en boucle fermée. Le procédé utilisé pour la fabrication, le CMOS 0.18 µm de la TSMC, comporte une couche de poly silicium, six couches de métal et la possibilité d'inclure des capacités de type MiM (Metal-Insulator-Metal). Ce projet de recherche a été accompli en collaboration avec la compagnie québécoise LTRIM Technologies, qui œuvrait dans le domaine des circuits analogiques de précision utilisant des résistances diffusées ajustables par faisceau laser [14, 35].

Problématique

La tension de décalage détermine la précision de la tension CC que l'amplificateur peut atteindre en sortie. Elle varie habituellement du microvolt au millivolt. Elle se définit comme étant la tension CC d'entrée que l'on doit appliquen, en mode différentiel, pour obtenir une tension CC nulle en sortie [37]. En pratique, cette tension de décalage n'est pas nulle même pour les amplificateurs opérationnels dont le circuit est entièrement intégré sur un même substrat. Ceci provient du fait que les composants intégrés actifs et passifs sont sujets à des variations des différentes propriétés des couches qui les composent dépendamment de leur position sur la puce. Ces variations affectent leurs caractéristiques électriques lors de la fabrication et sont critiques dans le cas des composants qui sont appariés comme, par exemple, la paire

de transistors d'entrée d'un étage différentiel et les miroirs de courant. Lors de la fabrication, ces variations se traduisent en non-uniformité dans l'épaisseur d'oxyde, dans les concentrations de dopant et dans les géométries, principalement due aux erreurs de photolithographie pour ces derniers. Elles sont de nature aléatoire et produisent des caractéristiques dissimilaires même pour des composants ayant été soigneusement appariés lors du dessin des masques. En jargon microélectronique ce phénomène est connu sous le nom de mésappariement de composants, '*device mismatch*' [28]. En plus du mésappariement, le stress engendré lors de la mise en boitier du circuit intégré accentue le mésappariement des caractéristiques électriques et peut augmente la tension de décalage. Ce phénomène peut cependant être minimisé en orientant adéquatement les composants appariés critiques lors du dessin des masques. À la section 1.3, l'effet du mésappariement sur une paire différentielle avec charge résistive est démontré. L'amplificateur est polarisé à l'aide d'une tension CC fixe, et des courants inégaux circulent dans les deux branches du au mésappariement des transistors. Cette différence dans les courants va produire en sortie une déviation du niveau CC par rapport à celui anticipé. La tension qui devra être appliquée à l'entrée pour compenser cette déviation est la tension de décalage. Cependant, cette déviation peut être grandement minimisée en ajustant la valeur des résistances de charge de façon à égaliser le mieux possible les courants dans les deux branches. Les fabricants d'amplificateurs opérationnels de précision utilisent des méthodes post-fabrication s'appliquant directement sur la puce pour réduire la tension de décalage. Dans ce travail, une méthode d'ajustement au laser des résistances fabriquées en silicium poly-cristallin a été exploitée pour réduire la tension de décalage d'un amplificateur opérationnel de précision.

Un élément de difficulté supplémentaire vient s'ajouter dans le cas des amplificateurs à pleine gamme dynamique. La tension de décalage varie selon la valeur de la tension CC mode commun (MC) appliquée à l'entrée. Un amplificateur à pleine gamme dynamique possède deux paires différentielles, une NMOS et l'autre PMOS connectées en parallèle. La tension de décalage dépend de quelle paire

différentielle est en opération PMOS, NMOS ou les deux, selon le niveau de tension MC à l'entrée. C'est dans ces circonstances qu'une méthode d'ajustement de la tension de décalage causée par les deux paires différentielles a été développée de façon à couvrir la totalité de la gamme dynamique MC d'entrée qui va de V_{SS} à V_{DD}.

Ajustement au laser des résistances de poly-silicium en CMOS standard

Il existe toute une panoplie de méthodes de réduction de tension de décalage. Elles sont décrites en détail à la section 1.3 en indiquant pour chacune les avantages et les inconvénients. Parmi les méthodes utilisées dans l'industrie, on retrouve le potentiomètre externe [7], la technique 'zener zapping' [9, 10, 12, 26], les résistances en couches minces [6, 11], les liens configurables [19, 26], les transistors à grille flottante[1, 27, 45] et les résistances diffusées [34, 41, 44]. Des méthodes utilisant des résistances au poly-silicium ont déjà été exploitées [3, 4, 39], mais contrairement à celle utilisée dans ce travail, aucune d'elles n'est compatible avec un procédé de fabrication CMOS standard. L'approche d'ajustement des résistances intégrées en poly-silicium utilisée dans ce travail est différente; les résistances sont ajustées grâce à un faisceau laser pulsé qui chauffe localement le poly-silicium situé au point focal. La fusion locale engendrée change la structure cristalline du silicium et a pour effet de diminuer sa résistivité à cet endroit et ainsi diminue la résistance totale. Aucun masque additionnel n'est requis, ce qui rend la méthode applicable a tout procédé CMOS standard. Des travaux de recherche portant sur les caractéristiques des résistances au poly-silicium ajustes au laser sont présentement en cours [13]. À la section 1.4, il est démontré que la réduction de décalage non seulement améliore la précision de la tension de sortie, mais augmente aussi la gamme dynamique et le taux de rejet en mode commun [16, 17].

Pratique de conception pour réduire le mésappariement

Les phases de conception de l'amplificateur de précision ainsi que le circuit de polarisation PTAT, impliquent l'appariement de transistors de certains éléments de

circuit tel que décrit à la section 2.1. L'appariement de composants est un sujet abondamment traité dans la littérature et basé sur les références [28, 31, 40], les principales règles à suivre sont détaillées :

1 Basés sur les équations (2.1) et (2.2), pour réduire le mésappariement dû aux variations aléatoires de la tension de seuil, V_T, et du facteur de courant, $\beta = \mu C_{OX}$ (W/L), les transistors appariés doivent avoir une grande surface active (WL). Ceci s'avère avantageux au niveau de la conception du dessin des masques, ce qui permet d'utiliser des techniques de centroïde commun et d'entrelacement.
2 Optimiser le point de polarisation des transistors selon la tension de sur-conduction (V_{GS}-V_T) ou le rapport g_m/I_{DS}.
3 Selon l'équation (2.3), le mésappariement des courants de drains d'un miroir de courant MOS peut être réduit en concevant le circuit avec un rapport g_m/I_{DS} faible ou une grande tension de sur-conduction (V_{GS}-V_T). En d'autres mots, polariser le miroir de courant dans la région de forte inversion améliore l'appariement.
4 Selon l'équation (2.4), pour réduire le mésappariement des tensions grille-source des transistors de la paire différentielle, il faut conserver un grand rapport g_m/I_{DS} ou une faible tension de sur-conduction (V_{GS}-V_T). Ceci implique que le point d'opération des transistors se situe dans la région de faible inversion.

L'amplificateur opérationnel CMOS et le circuit de polarisation PTAT

La topologie de l'amplificateur conçue dans ce travail possède une gamme dynamique à pleine tension d'alimentation autant en entrée qu'en sortie. C'est-à-dire qu'il fonctionne pour n'importe quelles tensions d'entrée et de sortie comprises entre le potentiel d'alimentation le plus positif, V_{DD} et le plus négatif V_{SS} [17]. L'étage d'entrée typique de ce type d'amplificateur est décrit à la section 1.4 et est présenté à la figure 1.7. L'étage d'entrée différentiel doit suivre les critères suivants [22] :

1. Pour atteindre en entrée la tension V_{DD}, une paire différentielle NMOS doit être utilisée afin que leur tension de drain puisse atteindre V_{DD}.
2. Pour atteindre en entrée la tension V_{SS}, une paire différentielle PMOS doit être utilisée afin que leur tension de drain puisse atteindre V_{SS}.
3. Pour que l'amplificateur fonctionne sur la pleine gamme dynamique, les courants des paires différentielles NMOS and PMOS doivent être additionnés et contrôlés de façon à ce que la transconductance, g_m, de l'étage d'entrée reste constante. L'étage de sortie à pleine gamme dynamique doit fonctionner en classe AB pour obtenir le maximum de tension crête à crête en sortie [20]. Une description générale des étages de sortie MOS en classe AB est donnée à la section 1.4 et des exemples sont montrés à la figure 1.8 a) et b). Le principe de base consiste à alimenter les grilles des transistors de sortie avec des signaux en phase. Ceci est accompli par des étages intermédiaires placés entre l'étage différentiel d'entrée et l'étage classe AB source-commune de sortie.

L'amplificateur opérationnel à pleine gamme dynamique d'entrée/sortie est présenté en détail à la section 2.2. L'amplificateur possède trois étages dans le but de limiter la complexité du circuit de compensation, tout en atteignant un gain CC en boucle ouverte de 40 dB par étage. Dans le cas général des amplificateurs à étages multiples cascadés, c'est habituellement l'étage d'entrée qui contribue majoritairement à la tension de décalage [29]. Dans ce contexte, la conception du premier étage est critique pour atteindre une bonne précision. Le diagramme schématique de la topologie proposée est illustré à la figure 2.4. L'amplificateur consiste en un étage d'entrée formé des transistors M1 à M12 et des résistances R1 à R8. Les résistances R1, R2, R7 et R8 sont ajustables par laser pour la réduction de la tension de décalage et les résistances R3, R4, R5 et R6 ont des valeurs fixes. Puisque l'étage d'entrée possède deux paires différentielles, son mode d'opération peut être divisé en trois parties. Quand le signal d'entrée MC possède une composante CC faible, seulement la paire PMOS est activée. Lorsque le niveau CC d'entrée arrive à mi-chemin entre V_{SS} et V_{DD}, les deux paires sont activées, puis lorsque le niveau CC

d'entrée se rapproche de V_{DD}, seulement la paire NMOS conduit. Les deux paires différentielles opèrent en région d'inversion faible de façon à avoir une relation linéaire entre le courant de polarisation et le g_m des transistors. L'opération en inversion faible couplée avec une large surface de grille et une faible tension de sur-conduction contribue à diminuer la composante de bruit 1/f [23]. Dans le but de conserver le g_m des transistors de la paire d'entrée constant sur toute la gamme dynamique, le circuit composé de la source de courant, M5, d'un transistor de transfert de courant, M6, et du miroir de courant, M7-M8, s'assure que la somme des courants de polarisation dans les deux paires différentielles PMOS (M1, M2) et NMOS (M3, M4) soit toujours la même quelque soit la tension MC d'entrée CC [20]. Le deuxième étage est composé d'un amplificateur différentiel simple formé par les transistors M13 à M17. Sa sortie est connectée au transistor M24 de l'étage classe AB en configuration source-commune. Un circuit d'interface constitué des transistors M18 à M22 convertit la tension de sortie du 2^e étage en courant de façon à polariser le transistor M23 en configuration source-commune [21]. Cette configuration permet aux signaux à la grille de M23 et M24 d'être en phase. Les transistors M18 à M20 représentent un circuit d'amplification large bande [30, 42] ayant un transistor connecté en diode comme charge active, pour permettre un décalage de tension CC. Le circuit complet de l'amplificateur est stable pour une charge de 500 pF en utilisant la technique de compensation 'Nested-Miller' [32, 38].

Le circuit de polarisation PTAT de l'amplificateur est détaillé à la section 2.4 et est illustré à la figure 2.11. Son fonctionnement est basé sur le principe qu'un courant est généré dans la résistance RBIAS dû à la différence de tension grille-source entre les transistors M19 et M20 [1]. Ceci est rendu possible en imposant un rapport (W/L) du transistor M19 plus grand que celui de M20. Ce courant est alors indépendant de la tension d'alimentation et ne dépend que de la température comme le montre l'équation (2.64) tirée d'une analyse simple au premier ordre. Le circuit de polarisation doit être entraîné dans l'état d'opération voulu grâce au circuit de démarrage composé des transistors M1 à M10. Les alimentations externes V1 et V2

sont requises par le circuit de démarrage. Le circuit de polarisation génère deux tensions précises VBIAS1 et VBIAS2 utilisées par l'amplificateur.

Les dessins des masques de l'amplificateur et du circuit de polarisation emploient pour les transistors et les résistances critiques, les techniques d'appariement dans les règles de l'art [18]. De plus, les transistors critiques des paires différentielles de l'étage d'entrée sont positionnés de part et d'autre de l'axe central de la puce où l'on retrouve le gradient de stress le plus faible. Une description détaillée des dessins des masques est présentée à la section 2.5 et le dessin complet est illustrée à la figure 2.13.

Méthodologie d'ajustement des résistances pour diminuer la tension de décalage

Une analyse détaillée justifiant la séquence d'ajustement des résistances est présentée à la section 2.3. L'analyse en mode courant de la séquence d'ajustement est basée sur la méthode employée pour réduire la tension de décalage des amplificateurs à pleine gamme dynamique à base de transistors bipolaires utilisant la technologie 'zener zap' [24]. La séquence d'ajustement est décrite ici selon deux scénarios possibles. Le premier scénario se présente lorsque la tension d'entrée MC est élevée de sorte que seulement la paire différentielle NMOS est activée. À l'opposé, le deuxième scénario se produit lorsque la tension MC est faible et seulement la paire PMOS est activée. Dans les deux cas, les effets engendrés par l'ajustement de la paire de résistances R7 et R8 et ceux engendrés par la paire R1 et R2 sont traités séparément. L'analyse montre que la tension de décalage causée par la paire PMOS, $V_{OS(P)}$, est plus sensible à l'ajustement des résistances R7 ou R8 que dans le cas de la tension causée par la paire NMOS, $V_{OS(N)}$. Lorsqu'une des résistances de la paire R1, R2 est ajustée, $V_{OS(N)}$ et $V_{OS(P)}$ sont affecter la même variation. La diminution de la tension de décalage globale se déroule en deux étapes :

Étape No. 1: Ajustement laser des résistances - R7 ou R8

On déduit de l'équation (2.55), que $V_{OS(P)}$ est trois fois plus sensible au changement infligé à la résistance R7 ou R8 que $V_{OS(N)}$. Cet ajustement est donc privilégié pour réduire $V_{OS(P)}$. Le rapport R7/R8 est varié en chauffant au laser R7 ou R8 jusqu'à ce que $V_{OS(P)}$ devienne approximativement égale à $V_{OS(N)}$. Cette étape permet de réduire la différence $|V_{OS(P)} - V_{OS(N)}|$ à presque 0 Volt. C'est la première étape dans le processus de réduction de la tension de décalage globale de l'amplificateur. Puisque lors de cet ajustement, $V_{OS(P)}$ est plus sensible que $V_{OS(N)}$, cette étape est réalisée pour une tension MC d'entrée qui permet d'avoir seulement la paire différentielle PMOS activé.

Étape No. 2: Ajustement laser des résistances - R1 ou R2

On déduit de l'équation (2.60), que l'ajustement des résistances R1 ou R2 influence de la même façon $V_{OS(P)}$ et $V_{OS(N)}$. Cet ajustement est réalisé lorsque la tension MC d'entrée et à mi-chemin entre V_{DD} et V_{SS} de sorte que les deux paires différentielles sont activées. L'ajustement de R1 ou R2 prend fin lorsque la tension de décalage visée est atteinte ou du moins le plus près possible.

Il existe huit cas possibles de variation de la tension de décalage en fonction de la tension MC d'entrée. Ces huit cas sont illustrés à la figures 2.8 et 2.9. Selon le cas, la résistance à ajuster au laser de chacune des paires R7 ou R8 et R1 ou R2 doit être identifiée. À cet effet, le tableau 2.1 identifie ces résistances pour chacun des huit cas et un organigramme des séquences d'ajustement est présenté à la figure 2.10.

Résultats

Les résultats de simulation post-dessin de masques et expérimentaux sont présentés au chapitre 3. Ils démontrent la fonctionnalité de l'amplificateur et l'efficacité de la méthode de réduction de la tension de décalage. La conception a été réalisée en prenant soin à chaque étape de minimiser les variations des niveaux de tension de polarisation CC en fonction des variations des paramètres du procédé

'corners' et de la température sur la gamme -40° C à 85° C. Les résultats démontrant la stabilité des niveaux de tension et du gain en boucle ouverte sont présentés aux tableaux 3.1 et 3.2 respectivement. Les résultats de simulation sont détaillés au tableau 3.3. L'amplificateur s'avère stable avec une marge de phase de 63° et un gain en boucle ouverte supérieur à 120 dB. La réponse à une onde carrée ne montre aucune trace d'oscillation, prouvant la stabilité du circuit. Un exemple simulé de séquence d'ajustement des résistances est présenté à la section 3.1.1. Cet exemple démontre l'utilisation du tableau 2.1 pour réduire efficacement la tension de décalage. Les mesures expérimentales ont été effectuées avec une charge de 470 pF et sont présentées à la section 3.2. Elles montrent la réponse de l'amplificateur à divers stimulus d'entrée : rampe de tension CC, sinusoïde et petite et grande amplitude d'onde carrée. Les résultats indiquent que l'amplificateur est fonctionnel et stable lorsqu'utilisé en suiveur. Les résultats expérimentaux d'annulation de tension de décalage sont présentés à la section 3.2.1. Les paramètres du laser utilisé pour ajuster les résistances au poly-silicium dopé P+ sont présentés au tableau 3.8. Les résultats de réduction de tension de décalage pratiqués sur cinq échantillons sont résumés au tableau 3.12.

Conclusion

Ce mémoire a présenté une nouvelle méthode d'ajustement au laser de résistances au silicium poly-cristallin fabriquée en technologie CMOS standard. Cette méthode a été mise en œuvre dans le but de réduire la tension de décalage d'un amplificateur opérationnel à pleine gamme dynamique d'entrée et de sortie. La séquence d'ajustement des paires de résistances développé analytiquement a été implémentée expérimentalement avec succès. L'algorithme d'ajustement des résistances développé par simulation, dans un premier temps, s'est avéré exact expérimentalement. Les résultats obtenus sur cinq échantillons après ajustement ont montré une tension de décalage inférieure à 30 μV pour une tension CC en mode commun située à mi-chemin entre V_{DD} et V_{SS}. De plus, une tension de décalage

inférieure à 110 μV a été obtenue sur ces mêmes échantillons et ce pour l'ensemble de la gamme dynamique d'entrée, de V_{SS} (0V) à V_{DD} (3.3V).

La majeure partie du travail expérimental effectué a été dédiée à la mise au point de la méthode d'ajustement au laser des résistances et des mesures avec précision des tensions de décalage pendant et après l'ajustement. Cependant, d'autres expérimentations pourraient être conduites pour évaluer, entre autre, le gain en boucle ouverte, la bande passante de gain unitaire et la distorsion harmonique totale. La dérive de la tension de décalage après ajustement en fonction de la température devrait aussi être mesurée. Ce type de mesure est très apprécié par les industriels et font l'objet de publications dans des revues d'envergure. Elles permettent de comparer la durabilité des différentes méthodes de réduction de tension de décalage.

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Singh, R.; Audet, Y.; Gagnon, Y.; Savaria, Y.; "Integrated Circuit Trimming Technique for Offset Reduction in a Precision CMOS Amplifier," Published in IEEE International Symposium on Circuits And Systems (ISCAS), May 2007

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LISTE DES ACRONYMES

CC	Courant Continu
CMOS	Complementary Metal Oxide Semiconductor
LASER	Light Amplification by Stimulated Emission of Radiation
MC	Mode Commun
MiM	Metal-insulator-Metal
NMOS	N-type Metal Oxide Semiconductor
PMOS	P-type Metal Oxide Semiconductor
PTAT	Proportional-To-Absolute-Temperature
TSMC	Taiwan Semiconductor Manufacturing Corporation

ABREVIATIONS

AC	Alternating Current
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common Mode Rejection Ratio
CPU	Central Processing Unit
DC	Direct Current
DUT	Device Under Test
FG	Floating Gate
Fig.	Figure
FF	Fast-Fast
FS	Fast-Slow
GPIB	General Purpose Bus Interface
IC	Integrated Circuit
ICMR	Input Common Mode Range
I/O	Input-Output
LASER	Light Amplification by Stimulated Emission of Radiation
MiM	Metal-Insulator-Metal
MOS	Metal Oxide Semiconductor
NMOS	N-type Metal Oxide Semiconductor

Nd: YAG	Neodymium-doped Yttrium Aluminium Garnet
PMOS	P-type Metal Oxide Semiconductor
PTAT	Proportional-To-Absolute-Temperature
SF	Slow-Fast
SS	Slow-Slow
TT	Typical-Typical
TSMC	Taiwan Semiconductor Manufacturing Corporation

CHAPTER 1
Introduction

This chapter introduces the motivation and objective of the thesis. It summaries a study of various input offset voltage trimming techniques applied to precision analog IC amplifiers. The chapter also presents an overview of rail-to-rail input-output CMOS amplifier. The chapter concludes presenting an outline of the thesis.

1.1 Motivation

This dissertation was performed in an industrial collaboration with LTRIM Technologies Inc., Quebec, Canada. LTRIM Technologies was involved in the design of analog circuits utilizing their patented laser trimmable diffused resistor [14, 35] in standard CMOS processes. This work intended to implement these laser-trimmable diffused resistors for the design of precision operational amplifiers similar to Linear Technology's LT1218/LT1219 BJT precision operational amplifiers [8] using trimmed resistors for reducing input offset voltage. This research further aimed at investigating laser trimming of poly-silicon resistors available in standard-CMOS process for designing precision amplifiers. This concept in due course of research work became the main motivation for designing and developing a standalone IC amplifier and reducing its input offset voltage by laser trimming of poly-silicon resistors embedded in the amplifier topology.

1.2 Objective

The objective of this thesis is to demonstrate the implementation and application of laser-trimmable poly-silicon resistors for reducing the offset voltage of precision operational amplifier in standard-CMOS process. The process technology used for this work is TSMC CMOS 0.18 μm. A high DC gain, low frequency rail-to-rail I/O operational amplifier was the design objective with integrating P+ poly-silicon resistors in its topology. This also required developing a methodology for trimming sequence such that the input offset voltage of a rail-to-rail differential amplifier can

be trimmed over the complete input common mode range (ICMR). This was needed since the input offset voltage for a rail-to-rail input stage varies over ICMR depending on which differential pair is active, PMOS, NMOS or both pairs. An input offset voltage of less than 100 μV over the full ICMR after laser trimming has been defined as a specification for the prototype operational amplifier designed for this work.

1.3 Input Offset Voltage Trimming Methods for Operational Amplifier

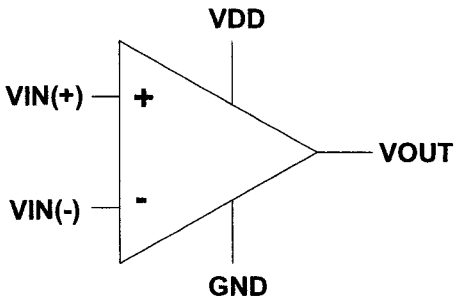


Fig 1.1: Operational amplifier symbolic representation

An ideal operational amplifier as shown in Fig. 1.1 is characterized by:

- Infinite open loop DC gain
- Infinite bandwidth
- Infinite input impedance i.e., no current flows into either inputs of the amplifier
- Zero output impedance i.e., amplifier is able to drive any load impedance to any voltage
- Zero output voltage when both input terminals are at same potential i.e., zero input offset voltage

Since this work is aimed at reduction of input offset voltage, the other amplifier parameters mentioned above are not discussed further. The term input offset voltage (V_{OS}) is defined as the DC voltage that must be applied between the two input terminals (inverting and non-inverting) of the operational amplifier to obtain zero DC volt at the output terminal [37]. In practice, the amplifier parameters deviate from the

ideal ones and this includes offset voltage, which is never zero. In other words, the output voltage is not observed to be zero volt, when two input terminals of the amplifier are at the same DC potential. Typically, an offset voltage is in the range of microvolts to millivolts. The polarity of offset voltage can be negative or positive, which varies from device to device (die to die) of the same wafer lot. The reason is the inherent device mismatch of the input stage transistors and other integrated circuit components in the amplifier during fabrication steps. Device mismatch occurs due to random variations in time-independent physical quantities (e.g., number of doping atoms under the gates of identical MOS transistors, oxide thickness variation, device dimension variations) and this leads to random differences between device characteristics [28, 40]. Also, there is a minor contribution of mechanical stress on the die during packaging. These factors have a combined effect on the drain currents flowing in the input stage of the amplifier. The bias currents are mismatched and flow unequally, which creates a difference in voltage appearing at the input terminals of the amplifier.

A simple PMOS differential pair with resistive load, RA and RB is shown in Fig. 1.2. For such a differential pair, T1 and T2 should be perfectly matched with each other in terms of their size (Width, W and Length, L) and the same condition applies for load resistors. As a result, bias or drain currents are equal for this differential pair i.e., ID1=ID2. This is an ideal situation. But due to device mismatch, W and L of T1 and T2 will vary, which will cause mismatch in their drain currents, ID1 and ID2. The mismatch in drain current is observed since it is a function of aspect ratio (W/L) of a MOS transistor. Here it is assumed that load resistors, RA and RB are perfectly matched though in reality, they too will experience mismatch. A difference in drain current values will cause the output DC value, VOUT to deviate from the expected value. It can be either higher or lower than the desired value after fabrication. Eventually, the output DC voltage accuracy of this differential amplifier gets affected.

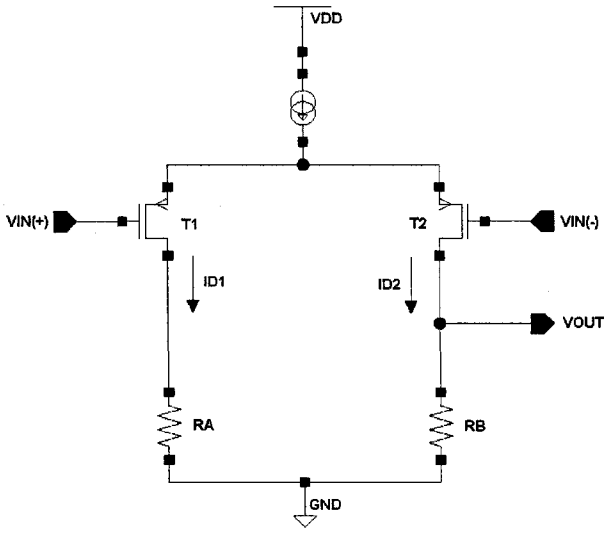


Fig 1.2: Basic MOS differential amplifier

Input offset voltage is one of most important specification identified in datasheets for commercial IC amplifiers. It is categorized as a DC parameter, which represents an internal error of the amplifier occurring due to device mismatches and packaging effects as mentioned earlier. This error is always present as the amplifier is powered on and the error is observable before, during and after any input signal is applied. In other words, input offset voltage determines how accurately the output DC voltage of the amplifier matches the ideal operational amplifier condition, as the input terminals are maintained at the same DC potential. Thus, the precision of an amplifier is identified by the magnitude of its input DC offset voltage, V_{OS}. Referring back to Fig. 1.2, trimming of load resistors can be performed to improve matching of currents in two legs of the differential amplifier, which reduces V_{OS} and thus improves DC accuracy. Considering a specific case for purpose of explanation, assuming ID1 is greater than ID2 due to mismatch, then RA can be reduced using trimming techniques to a lower value to eventually make ID1 equal to ID2. This condition is achieved by reducing the input offset voltage and measuring it until a desired value is attained. In essence, reducing offset voltage will tend to match the drain currents in the two legs of the differential amplifier. The following section describes some of the commercial offset voltage trimming techniques applied to operational amplifiers to improve its

precision and accuracy.

1.3.1 External Potentiometer

Even the classical LM741 BJT general-purpose operational amplifier by National Semiconductor included an offset voltage reduction feature [7]. This involved two trim-pads called "Offset Null" available to be connected to an external potentiometer to reduce the offset voltage. These offset trimming pads were connected to the input differential stage. For the sake of discussion, Fig. 1.3 shows the null pins in a MOS differential pair connected to an external potentiometer circuit represented by RP1 and RP2.

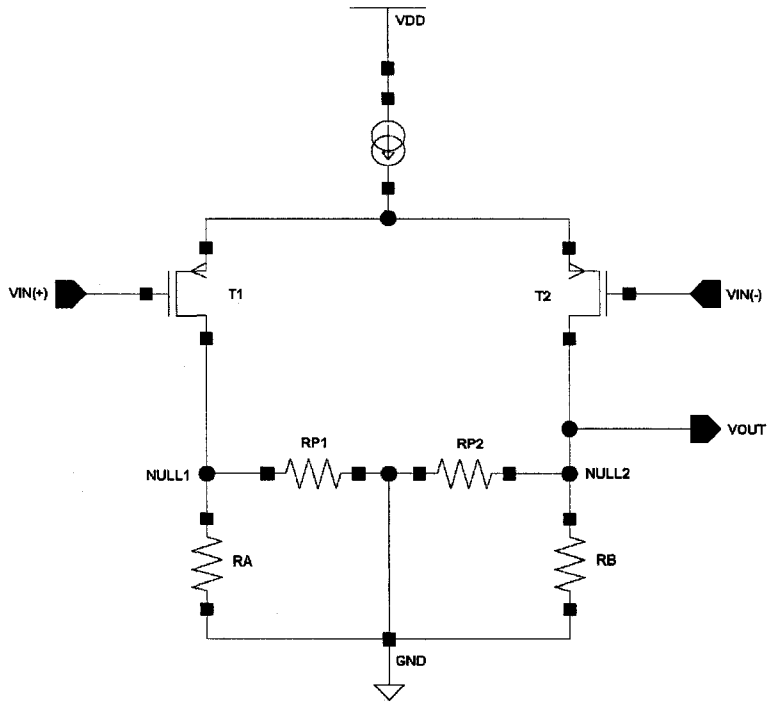


Fig 1.3: Basic MOS differential amplifier with external potentiometer resistors

The input offset voltage is measured by the difference in voltage between the two input terminals of the op amp, i.e., V_{OS} = VIN (–) – VIN (+) [36]. This measurement is defined for DC voltage values at VIN (–) and VIN (+) terminals of the differential pair. If V_{OS} is negative, then VIN (–) is smaller than VIN (+), so more resistance

needs to be added to the NULL2 pins (which ties to the inverting input branch) in order to produce more voltage at this node; thus, V_{OS} is less negative, and vice versa for the case of positive V_{OS}. Therefore, the absolute V_{OS} becomes smaller for a given temperature. This method of offset voltage trimming is applicable to all IC manufacturing processes like BJT, Bi-CMOS and CMOS. One of the drawbacks of this technique is that it always requires trim-pads that contribute to die area. The resistor temperature coefficient of the potentiometer must be given a careful attention as it can affect the drift of offset voltage over temperature. The external potentiometer is usually large in comparison to IC amplifier, which further occupies large space on board.

1.3.2 Zener Zapping

Zener zapping is the oldest IC trimming technique applicable to Bipolar processes [12,26]. It involves melting of a reverse biased P-N diode (Base-Emitter junction) by injecting a large current usually in the range of a single ampere. The mechanism involved here is avalanche breakdown of the bipolar transistor, which creates localized heating causing rapid metal migration between base and emitter metal layers. This makes a metallurgical short circuit connection across the P-N junction with a very low resistance of the order of few Ohms under proper bias conditions. Fig. 1.4 shows application of base-emitter junction diode or zener diode, which are connected in parallel with a string of resistors. Pads are included across each parallel resistor-diode network where a large voltage can be applied across a selected resistor-diode network. This process will selectively "remove" a particular resistor across which the zener diode is shorted. This reduces the net value of the series connected resistors. This type of resistor trimming is defined as zener-zapping. In the context of the MOS differential pair of Fig. 1.3, RA and RB can be designed as integrated parallel resistor-zener diode network connections as shown in Fig. 1.4 for offset voltage trimming [23].

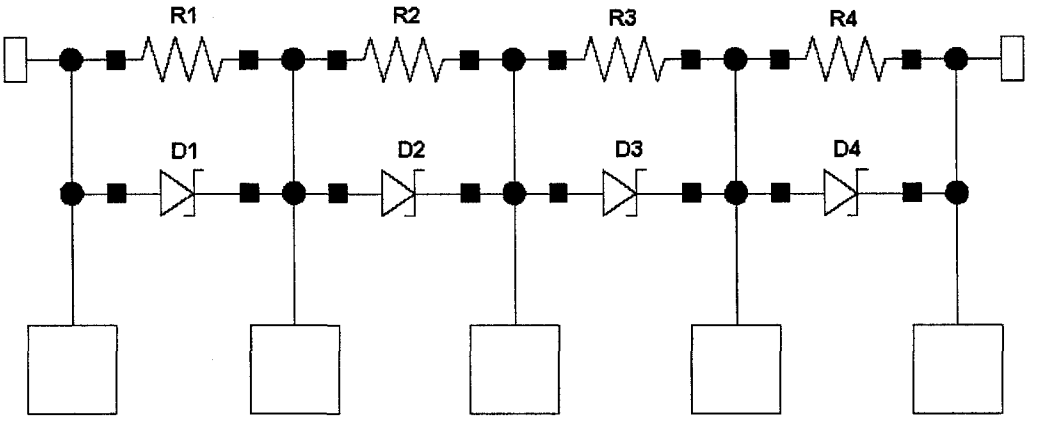


Fig 1.4: Zener zap trimming network

This kind of trimming is widely used for Bipolar and Bi-CMOS processes since zener diodes are easily available in such processes without adding any additional mask layer and cost. The technique also has a reasonable trimming resolution though its is discrete in steps. However, it also comes with some drawbacks which include large die area for trim pads connected to zener diodes, short life of test probe needles carrying ampere-range currents during zapping, offset variation due to on-chip heat waves and large currents required to implement this method make it unsuitable for low voltage designs. This technique is best implemented at wafer level in order to reduce package pin count. Area considerations reserve this method for large geometry processes where the trimming structures and probe pads make up a relatively small percentage of the overall die area. Some of the commercial precision amplifiers using this form of trimming method are OP07 [9] and OP200 [10] by Analog Devices.

1.3.3 Thin-Film Resistors

A thin-film resistor consists of materials like Nickel-Chromium (NiCr), Silicon-Chromium (SiCr) and Tantalum-Nitride (TaN). Thin-film thickness ranges between 10 nm and 100 nm. The actual resistance depends on the geometry and the property of the film material. Earliest reported thin-film resistor trimming [6] utilized Yttrium Aluminum Garnet (YAG) laser, which performed trimming by removing the material. The removal of the material is accomplished by making a laser cut into the resistor

area, causing the effective resistor width to be reduced. Another way to change the value of the resistor is by vaporizing small spots in the interior of a resistor. In both cases, the resistance value is increased since the overall area of the resistor is reduced. By controlling the path and speed of the laser beam, the resistor's value of a single resistor can be adjusted to very precise values. Thin-film resistors trimmed in such fashion have shown a change less than 0.1 percent in resistance over a period of several months. As an example, OPA27/37 [11] is an ultra-low noise precision operational amplifier manufactured by Texas Instruments (TI) that incorporates laser trimmed thin-film resistors for offset voltage reduction.

The laser trimming process is continuous and the thin-film resistors can be easily integrated as a circuit element. The trimming process does not require any parallel connections like zener-zapping. This avoids the need of any additional pads since trimming is performed at wafer level. On the other hand, such resistors require an additional manufacturing step that adds to the cost of production. The size of the trimming structures created due to a laser cutting of a thin-film resistor depends on the laser beam diameter, which does not scale with IC manufacturing processes.

1.3.4 Link Trimming

When a laser cutting or a high current injection is used to destroy a "shorted" connection across a parallel resistive element, it is called link trimming [19, 26]. The removal of the connection increases the equivalent resistance of the combined elements. Laser cutting works similar to laser trimming of thin films, the high local heat from the laser beam causes material changes which create a non-conductive area by cutting a metal or conductive poly-silicon connector. Metal layers may include aluminum (Al) and titanium-tungsten (TiW). This is somewhat opposite to zener-zapping where a short is created across a resistor, reducing the value of the resistor. Link trimming network consists of metal connections placed in parallel to series connected string of resistors. A circuit representation is shown in Fig. 1.5. The resistors are represented by R1, R2, R3 and R4 and link connections are denoted by L1, L2, L3 and L4. There are no special processing steps needed although the

manufacturing process may have to be tailored to the laser characteristics if laser cutting is used. With the high current injection method, trimming can be performed at the package level if required using pads for current injection.

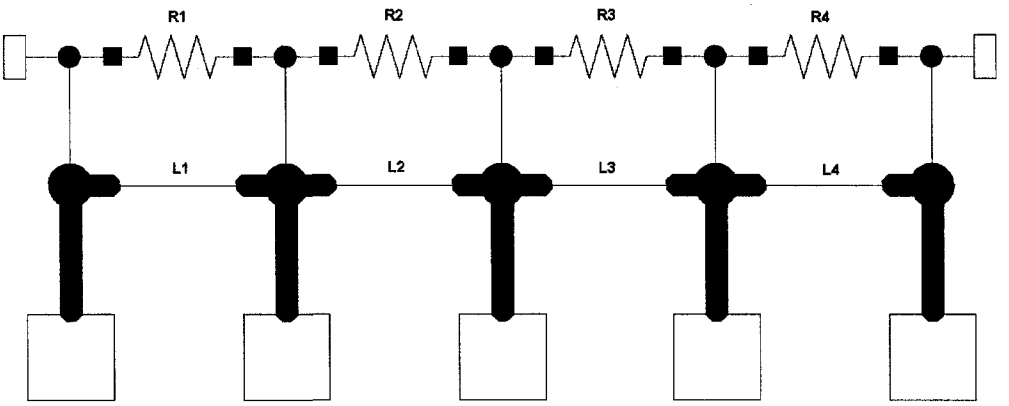


Fig 1.5: Link trimming network

The laser cutting of metal links doesn't require extra contact pads but the trim structures do not scale with the process feature sizes. This type of trimming cannot be performed in package level. The current trimmed version requires additional probe pads and it can require extra package pins for in-package trims. Like zener zapping, link trimming is discrete in operation. To improve the trimming resolution, additional link structures are required and proportionally increase the die area. Metal resistors used for link trimming require additional mask steps while poly-silicon resistors used for link trimming can easily adapt to a standard-CMOS process.

1.3.5 Floating Gate Transistor

A floating gate (FG) transistor is usually associated with digital storage devices like EEPROMs. Such a circuit element is used to store binary data to adjust voltage levels [27]. Floating gate transistor has also found application as a trimmable element in the area of analog circuits, which include voltage reference [1] and operational amplifiers [45]. A simplified schematic of a FG device is shown in the Fig. 1.6. It consists of two tunnel diodes, D1 and D2 and a MOS transistor, M0. A tunnel diode is a used to establish a fixed voltage at the gate of the MOS transistor, which is called a floating gate (FG) node. C_{FG} represents the equivalent FG capacitance at the gate of the transistor. During the programming phase, a fixed voltage can be set at the FG

node. The node voltage VP is raised which causes D1 to charge the FG node and by lowering the node voltage VN, D2 will discharge the FG node. Once the FG node reaches a specified voltage, both of these diodes, D1 and D2 are turned off by making VP and VN to 0 V. It results a fixed charge stored permanently at the FG node. The programming phase is identified as trimming of FG transistor in terms of its application to analog circuits. Such a transistor can be connected as loads in MOS differential pair topology of Fig. 1.2. The gate voltage of FG transistor can be adjusted to correct the drain current mismatch in the amplifier to reduce its input offset voltage.

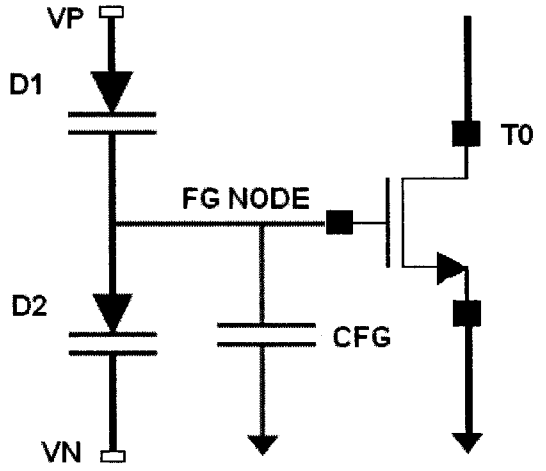


Fig 1.6: Floating gate circuit representation

The trimming can be overwritten; it is possible to periodically reprogram the FG device to account for long-term drifts or to modify system characteristics to meet new requirements. This kind of trimming can be performed at package level. The floating gate device is built using two overlapping poly-silicon layers, which is compatible with CMOS processes having dual poly-silicon layers.

1.3.6 Diffused Resistor

The diffused resistor consists of two highly doped p-type (or n-type) regions separated by a gap of n-type (or p-type). It can be considered as a gateless MOSFET where two highly doped regions are analogous to the source and drain regions and the channel is the gap region. The accuracy of this resistor can be precisely controlled by

applying a laser pulse on the gap region, which leads to melting of silicon substrate and results in diffusion of dopants from the two highly doped regions [44]. A laser trimmable diffused resistor has found application in design of voltage reference [41] and R-2R Digital-to-Analog Converters (DAC) [34]. The top layout view of N-type diffused resistor with different laser beam positions is shown in Fig. 1.7. The process of trimming involves a single laser pulse gap region between the diffused resistors at a distance, L_{PULSE}. The two highly doped regions have top nodes C and D connected to each other, thus forming a chain of two resistors in series between node A and B. Assuming there is enough energy in the laser pulse, its interaction with silicon results in melting of the two highly doped regions, causing dopant diffusion in the gap region that creates a low resistance path between them.

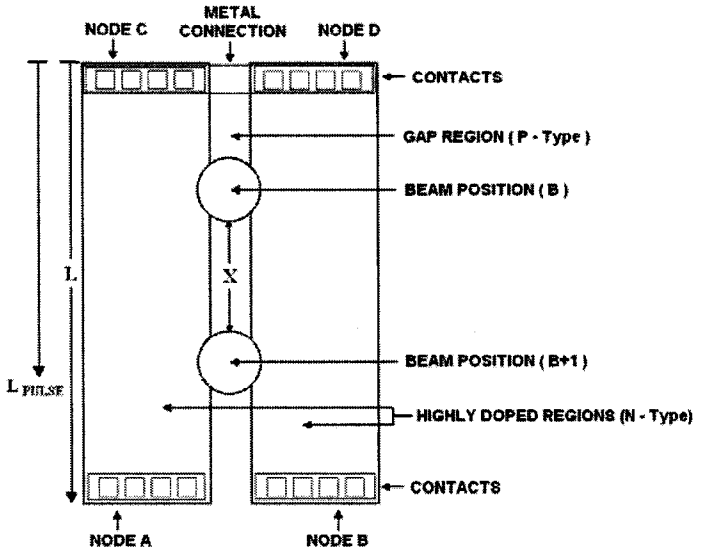


Fig 1.7: Diffused resistor with laser beam positions

This is electrically equivalent to making a short circuit connection between two identical segments of the highly doped regions. The overall resistance is lowered because the metallurgical short reduces the available length of the resistor. The beam positions are shown in Fig. 1.7 to demonstrate the path of laser as it traces during trimming operation. The term X represents the minimum spatial resolution between two distinct laser beam positions, B and B+1.

The advantage of using a diffused resistor is that it can easily form a part of the

integrated circuit like resistive elements for differential amplifier in Fig. 1.2. It does not require any additional mask since it is entirely compatible with standard CMOS and Bipolar processes. Similar to thin-film resistors, the size of the trimmable diffused resistor structure depends on the laser beam diameter, which does not scale with IC manufacturing processes.

1.3.7 Poly-silicon Resistor

Poly-silicon (poly-Si) resistors have been widely used in monolithic ICs because of their compatibility with CMOS IC manufacturing processes. A poly-Si can be manufactured with a wide range of resistance values. Such resistors also have been exploited for the purpose of trimming in high precision analog circuits. One of the methods to trim a poly-Si resistor is performed by laser link making [39]. The structure of the resistor can be constructed in a similar manner as the diffused resistor shown in Fig 1.6. In this case two poly-Si resistors connected in series are separated by a gap or un-doped area. The gap area is subjected to a laser pulse, which will cause lateral diffusion of the dopants creating a link between poly-Si regions. This is analogous to making a short circuit connection in a diffused resistor trimming using a laser pulse. The resistance of the poly-Si resistor is decreased as a consequence. Poly-Si resistor trimmed using laser link making method can be easily adapted to Bipolar and standard CMOS processes. Another method reported to perform trimming of poly-Si resistors is called pulse current trimming [3, 4]. This method is applicable to heavily doped poly-Si resistors with impurities (Arsenic, Boron or Phosphorous). The resistance of a heavily doped poly-Si resistor having 2-terminals is reduced by electrical means using short duration current pulses. The reduction in resistance is possible when a current density higher than a certain threshold value is applied. To satisfy conditions for trimming, the doping concentration of impurity should be higher than a threshold value of $1x10^{20}$ cm^{-3} and a current density threshold value should be higher than $1x10^{4}$ A/cm^{2}. This method of trimming is applicable at package level where trimming can compensate for change in resistance values due to die stress and process variations, similar to zener zapping. On the other hand, the requirement

for heavy doping of poly-Si resistor with impurities requires specialized processing steps. Secondly, trim pads are needed to inject current pulses that cost die area.

This thesis work employs laser-trimmable passivated poly-Si resistors with a different approach as compared to those described earlier. The poly-Si resistor is trimmed by local heating on the surface of the resistor using a laser pulse, which causes the surface to melt locally where the laser beam is focused. The melting due to heat creates a change in the crystalline structure of the resistor that reduces the resistivity of the poly-Si resistor. A change in the resistivity creates a proportional change in the value of resistance. The process of trimming using this concept tends to decreases the value of the resistance. Poly-Si resistors trimmed in this manner can be easily manufactured in a standard CMOS process. It requires no additional mask layer and it is compatible with standard CMOS process manufacturing steps. Also, it can easily form a part of monolithic integrated circuit as a circuit element similar to thin-film resistors. The characterization of trimmed poly-Si resistors is also the subject of current research [13].

1.4 Rail-to-Rail Input/Output Amplifiers

Rail-to-Rail Input/Output (I/O) amplifiers find applications for low supply voltage and portable analog IC designs to obtain maximum dynamic range and output signal swing. Low supply voltage designs with values of 5 V or less must use the complete power supply range to have a usable dynamic range. The usable span is an important value because it influences several parameters such as noise susceptibility, signal-to-noise ratio (SNR), and dynamic range. Operational amplifiers that have input and output stages using the complete span between positive and ground / negative supply voltage for signal conditioning are known as rail-to-rail I/O amplifiers [17].

The input voltage range or the ICMR is a function of the input circuit topology of an operational amplifier. In case of a PMOS input pair of a differential amplifier stage as shown in Fig. 1.2, ICMR includes the ground rail but the positive supply voltage is limited due to voltage drop across the fixed current source. The opposite

will be the case if an NMOS input pair differential amplifier is considered. In both cases, the ICMR with simple differential amplifier input stage is never rail-to-rail. From the circuit design point of view, the design of an efficient rail-to-rail input stage must satisfy the following requirements [22]:

- To reach the positive supply voltage rail, NMOS transistors must be used while maintaining their drain voltage close to supply voltage.
- To reach the ground or negative supply voltage rail, PMOS transistors must be used while maintaining their drain voltage close to ground or negative supply voltage.
- To obtain complete rail-to-rail operation, the signals through PMOS and NMOS input transistors must be added and processed such that the total transconductance, g_m of the input stage remains constant over the complete ICMR.

A rail-to-rail input stage operation can then be obtained by paralleling a NMOS (M1-M2) and PMOS (M3-M4) differential pair stage as shown in Fig. 1.8. The differential pair is connected to a common current summing stage for complete implementation of an input stage. The NMOS input stage operates when the ICMR is high and the PMOS input stage works under reverse conditions. Both differential input stages operate when the input voltage passes through the centre of the ICMR. Thus, a dual input stage differential amplifier tends to extend the ICMR relative to a simple differential amplifier.

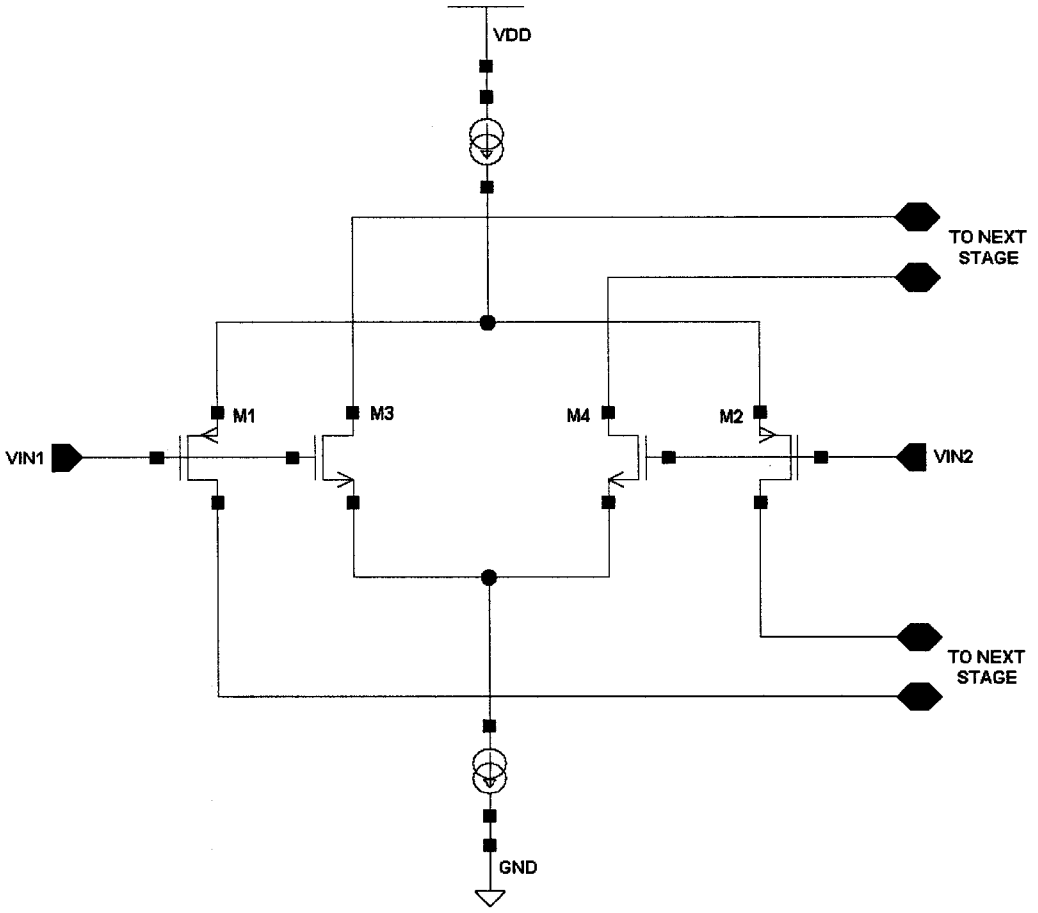
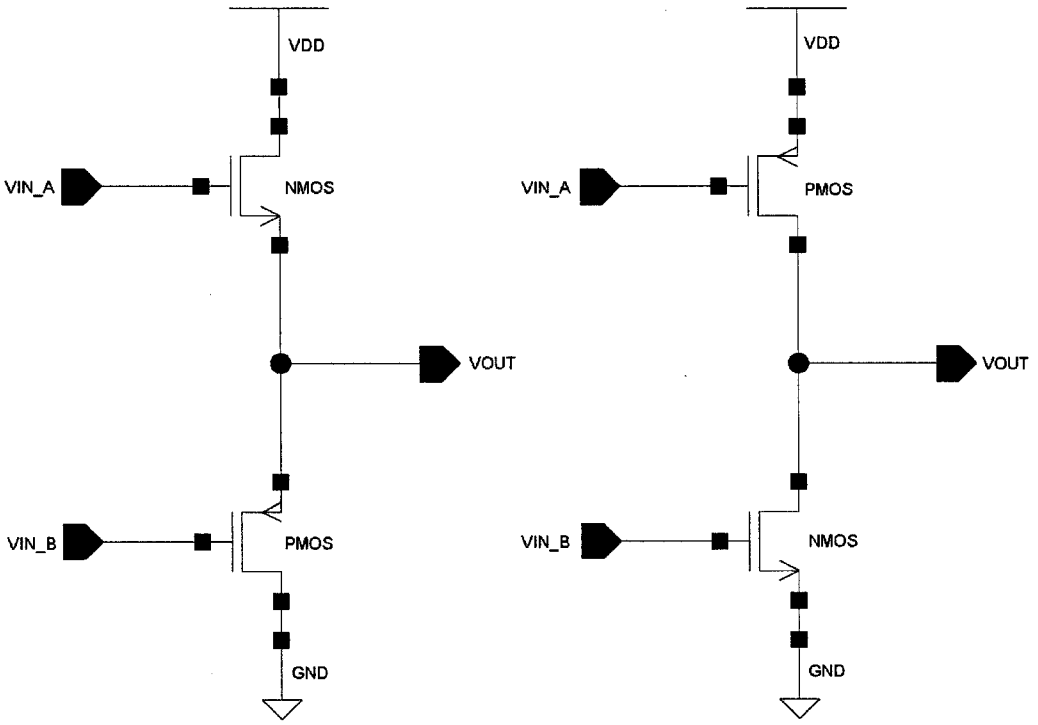


Fig. 1.8: Simplified schematic of a rail-to-rail differential input pair

To obtain a rail-to-rail output voltage swing, the output stage in a rail-to-rail amplifier is designed to operate in Class-AB mode [20]. The key requirement is that the output transistors are driven by two in-phase voltage signals. There are two cases of Class AB mode CMOS output stages shown in Fig. 1.9. The classical Class AB output stage shown in Fig. 1.9 (a) utilizes NMOS and PMOS common-drain output stages. The issue is that the output voltage swing can reach the supply rail within one gate-source voltage, which is an obstacle to achieve rail-to-rail output swing. Considering, the Class AB output stage shown in Fig. 1.9 (b), it consists of complementary output transistors using common source NMOS and PMOS connected with their drain terminals. The output voltage swing of this stage is almost rail-to-rail as it can reach either supply rail within one drain-source saturation voltage limit. For high DC value

of input signals, the drain current of NMOS output transistor is greater than the PMOS output transistor. This causes the output stage to pull down or sink current from the load connected to the output terminal of the stage.



(a) Common-drain stage **(b) Common-source stage**

Fig. 1.9: CMOS Class-AB output stages

On the other hand, for low value of DC input signals, the reverse occurs during which the output stage tends to push or source current into the load. The output stage shown in Fig. 1.9 (b) is generally used as an output stage for making rail-to-rail I/O amplifiers since it provides wider output signal swing response.

One of the earliest reported CMOS implementation of rail-to-rail input/output amplifiers was described in [22]. Rail-to-rail differential amplifiers require additional circuitry to maintain constant g_m over the ICMR. Without any g_m control stage, the g_m can vary by a factor of two over the ICMR. This will occur at the centre of the ICMR when both input pairs contribute their transconductance relative to the case when only

one of the differential pair is operating at low or high ICMR. A variation in g_m of the rail-to-rail input stage will lead to sub-optimal frequency compensation since the unity-gain bandwidth (UGB) of an amplifier is proportional to the g_m of the input differential stage [25]. In other words, the UGB will vary as the ICMR changes. A circuit that maintains constant-g_m for a rail-to-rail input stage is designed, based on the weak and strong inversion operation mode of the rail-to-rail input differential amplifier. This thesis work is restricted to use constant-g_m technique applied for weak inversion mode of differential pairs. To optimize for low frequency noise or 1/f noise, most input differential stages in CMOS amplifiers operate in weak inversion for precision analog applications [23]. This also allows making large differential pair transistors to reduce mismatch and have common centroid layout geometry. The constant-g_m stage used for this thesis work is described in Chapter 2. Several CMOS amplifiers with rail-to-rail I/O capability are available and an extensive treatment of such amplifiers with g_m stabilization over ICMR can be found in recent literature [20].

A rail-to-rail I/O amplifier finds wide usage as a voltage buffer (unity-gain configuration) where signal swing is an important parameter. Since the gain in a voltage buffer configuration is unity, a rail-to-rail output signal requires the input signal to be able to follow the output. A reduction of operating supply voltage will result in reduced maximum available dynamic range. In a precision analog system at low supply voltage of 5V or less, the operational amplifier must amplify the dc voltage level precisely. Errors in this area mainly result from input offset voltage (V_{OS}). This will eventually limit the dynamic range of the amplifier configured in unity-gain configurations. The dynamic range of the system is defined as the ratio of the largest output voltage to smallest output voltage [17]. The TLC271C (produced by TI) has a non rail-to-rail input and a rail-to-rail output stage operational amplifier, it operates at 5 V and has an input offset voltage of 1.1 mV. Its maximum output voltage swing at 5 V is 3.8 V_{P-P}. The dynamic range of the TLC271C is 20log (3800/1.1) = 71 dB in a unity gain configuration. On the other hand, TLV245x (also

produced by TI) has a rail-to-rail input and output with an input offset voltage of 20 μV. With rail-to-rail I/O feature, this amplifier has a maximum output voltage swing of 5 V_{PP} with a 5V supply. The dynamic range is 20 log (5000/0.02) = 108 dB. This shows how the dynamic range can improve for low supply voltage using a low offset voltage rail-to-rail I/O stage.

A rail-to-rail input stage V_{OS} varies as the input common mode voltage changes. This is not the case with a non rail-to-rail differential amplifier, for which the V_{OS} remains the same over the complete ICMR. In a rail-to-rail differential pair, the V_{OS} varies since there are two differential pairs connected in parallel. Both PMOS and NMOS differential pairs contribute to V_{OS} depending on values of the common mode voltage. At a high value of ICMR, only the NMOS stage contributes to V_{OS}, at low value of ICMR, only the PMOS stage contributes to V_{OS} and around mid-supply values of ICMR, both pairs contribute to V_{OS}. The two differential pairs usually have different offset voltages and this change in offset voltages contributes towards the common mode rejection ratio (CMRR). The CMRR of a differential amplifier can be stated in terms of input offset voltage as [16]

$$CMRR = \frac{\Delta V_{COMMON}}{\Delta V_{OS}} \tag{1.1}$$

where ΔV_{COMMON} and ΔV_{OS} represent the change in common mode input and offset voltage. From eq. (1.1), it follows that a large change in offset voltage will deteriorate the CMRR of the amplifier. The CMRR can be maximized by spreading the variation of input offset voltage over a large part of the ICMR. In case of a precision rail-to-rail I/O operational amplifier, reducing or trimming V_{OS} over the ICMR will improve the CMRR.

Offset voltage trimming techniques find usage in rail-to-rail I/O amplifiers suited for precision and low supply voltage applications. Based on the discussion presented earlier in this section, a reduction in offset voltage using trimming will enhance the accuracy, dynamic range and CMRR of the amplifier. The offset

trimming methods described in Section 1.3 are all applicable depending on manufacturing process, cost and application of the amplifier. Some of the industry standard precision rail-to-rail I/O amplifiers are LT1218/1219 by Linear Technology and OPA340 series by Texas Instruments. The LT1218/L1219 is built in a Bipolar process and utilizes laser-trimmed resistors for offset voltage trimming. OPA340 is manufactured in CMOS process and also utilizes laser-trimmed resistors for reduced offset voltage. Most industry standard precision amplifiers are manufactured with in-house semiconductor processes and utilize their process facilities (e.g. thin-film resistors, zener diodes) to trim offset voltage.

The objective of this work is to utilize standard-CMOS process for design of rail-to-rail precision amplifier and using available poly-silicon resistors. These poly-silicon resistors are integrated in the amplifier topology and will be subjected to laser trimming for V_{OS} reduction. The poly-silicon resistors form a part of the circuit and no additional circuitry is needed for offset voltage reduction.

1.5 Organization of the Dissertation

The thesis is organized in three chapters as outlined:

Chapter 2 presents the circuit and layout design of the CMOS rail-to-rail I/O operational amplifier. A mathematical theory and analysis is presented to determine the trimming sequence steps for reducing the input offset voltage over ICMR. A Proportional-To-Absolute-Temperature (PTAT) bias circuit design is presented to generate bias points for the amplifier. A start-up circuit for the bias circuit is also described.

Chapter 3 presents the post-layout simulation results to verify the basic parameters (DC Gain, Bandwidth, Phase Margin, Slew Rate, and Settling Time) of the amplifier before chip submission. The simulation results also include process corners and temperature variation analysis. Test results are presented to show the amplifier functionality in terms of DC and transient tests. Experimental results also demonstrate offset voltage trimming sequence to verify the trimming methodology developed during this thesis.

Chapter 4 is the last chapter of the dissertation, which concludes this work and presents future work that can be performed related to this thesis.

CHAPTER 2

Design of a Precision CMOS Operational Amplifier and PTAT Bias Generator

This section describes the design of a multistage operational amplifier with a rail-to-rail input-output capability. It presents the trimming sequence method applied to a CMOS rail-to-rail differential input stage to reduce the input offset voltage over the common mode voltage range. It is also imperative to have reduced variability of circuit characteristics over process and temperature changes. With this issue in consideration, a CMOS bias generator was designed to reduce the variations of the circuit parameters over a temperature ranging from -40^{0}C to +85^{0}C. The layout design and post-layout simulation results of the complete circuit including the amplifier and bias circuit is presented.

2.1 Precision Analog Circuit Design Considerations

Most precision analog circuit design is governed by the matching properties of similar components. Though matching of devices is an important issue addressed at layout level, it must be first tackled at the circuit level. Matching is a widely reported subject in literature [28, 31, 40] and based on literature review of device mismatch, circuit design considerations are summarized below which were instrumental in shaping this work.

1. Mismatch of two MOS transistors is characterized by random variations of the difference between their threshold voltages, V_T and current factor, $\beta = \mu C_{OX}(W/L)$. The Pelgrom model [40] is followed here for MOS transistor matching. The random variations have a normal distribution with an average value of zero and a variance depending on MOS active area which is a product of gate width, W and gate length, L. Mathematically, the model can be stated as

$$\sigma^2(\Delta V_T) = \frac{A_{VT}^2}{W.L} \tag{2.1}$$

$$\sigma^2\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_\beta^2}{W.L} \tag{2.2}$$

The equations (2.1) and (2.2) are approximations where A_{VT} and A_β are proportionality constants which depend on the process technology. Matching is also a function of distance between any matched devices and the corresponding term is not shown in the above equations. For the present design, all matched transistors are closely placed during layout. Published literature has shown that the correlation coefficient between V_T and β mismatch is very low and for this reason, the two terms are considered to be independent of each other. In order to reduce variations due to V_T and β mismatch, matched transistors are designed to have a large active area (W. L) at the circuit level. This also is advantageous for layout design using various matching techniques like common-centroid and interdigitated patterns.

2. Matching is also dependent on biasing point and can be classified for voltage and current biased blocks. Most analog circuits will constitute such building blocks. An example of a voltage-biased block is a current processing circuit (current mirror) and for a current biased block is a voltage processing circuit (differential pair). These blocks have been widely used for the design of the operational amplifier and the PTAT bias circuit included in this thesis.
3. For a voltage biasing block as shown in Fig. 2.1, the transistors T1 and T2 are biased from the same gate-source voltages and the drain-source current is a dependent term. Here, the difference in drain to source current of T1 and T2 is the major source of error i.e. $\Delta I_{DS} = I_{DS1} - I_{DS2}$:

$$\left(\frac{\sigma(\Delta I_{DS})}{I_{DS}}\right)^2 = \left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 + \left(\frac{g_m}{I_{DS}}\right)^2 \sigma^2(\Delta V_T) \tag{2.3}$$

Eq. (2.3) indicates that to maintain low drain-source current mismatch, transistors should be biased to have a low g_m/I_{DS} ratio, which will reduce the contribution of V_T mismatch. For the present case, β factor mismatch will dominate. Transistors should also be designed to have large active areas so as to both minimize V_T and β mismatch for Eq. (2.3). Thus, the drain current mismatch can be reduced by designing for lower g_m/I_{DS} ratio or a large gate overdrive (V_{GS}-V_T) voltage or biasing the transistor towards strong inversion region. A current mirror should be biased towards strong inversion region to have improved matching for precision analog design.

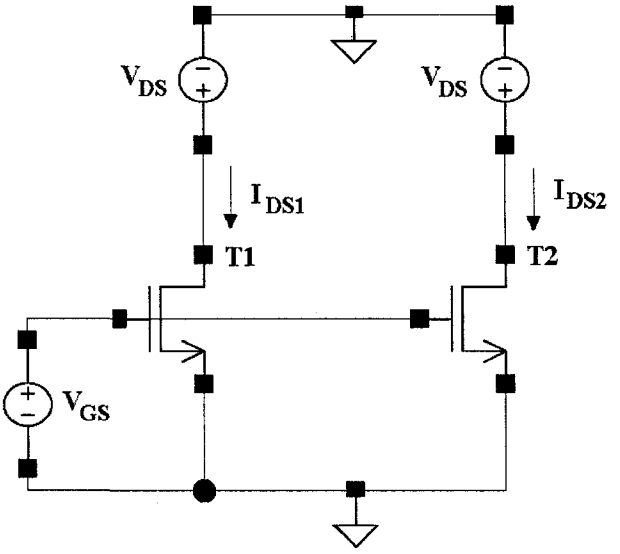


Fig. 2.1: Voltage biased block

4. For a current biased block as shown in Fig. 2.2, the error source is mainly due to the difference in gate-source voltages of T1 and T2 i.e., $\Delta V_{GS} = V_{GS1} - V_{GS2}$ as gate-source voltage is a dependent variable and the drain-source current is fixed,

$$\sigma^2(\Delta V_{GS}) = \sigma^2(\Delta V_T) + \left(\frac{1}{\left(\frac{g_m}{I_{DS}}\right)^2}\right)\left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 \qquad (2.4)$$

Eq. (2.4) suggests that to maintain low gate-source voltage mismatch, transistors should be biased to have a high g_m/I_{DS} ratio that will reduce the contribution of β mismatch. For the present case, the V_T factor mismatch will dominate. Again, transistors should also be designed to have large active areas so as to both minimize V_T and β mismatch for Eq. (2.4). To obtain reduced gate-source voltage mismatch, transistor should have higher g_m/I_{DS} ratio or a low gate overdrive (V_{GS}-V_T) voltage by biasing the transistor towards weak-inversion region. Thus, a differential pair should be biased towards weak inversion region to have improved matching for precision analog design.

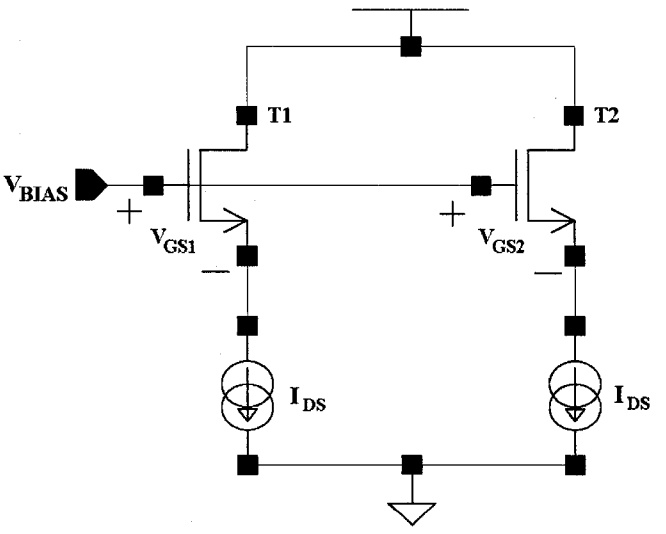


Fig. 2.2: Current biased block

The mismatch equations presented in this section are valid for all regions of operations.

2.2 CMOS Rail-to-Rail I/O Operational Amplifier Design

Device mismatches between MOS transistors and any passive components in an operational amplifier topology pose a challenge to circuit design in terms of accuracy and precision. It is this effect that appears as an offset voltage at the input terminals of the amplifier. The amplifier designed for this work is targeted to have a large gain similar to most industry standard precision amplifiers of approximately 120 dB [8, 23]. A large open loop DC gain is required to have a low DC gain error for the amplifier for close-loop operations. So, the number of amplification stages required to achieve a very large gain needs to be identified. Usually, BJT precision amplifiers utilize two stages of amplification to obtain a DC gain of 120 dB. On the other hand, for CMOS precision amplifiers, this is not case. The first reason is that the DC gain of a single stage BJT amplifier is higher than a single stage MOS transistor amplifier [25, 42]. Also, the intrinsic transconductance of a BJT is higher than a MOS transistor, which contributes to higher gain [47]. The intrinsic transconductance of MOS transistor varies based on the region of operation. It exhibits highest intrinsic transconductance in weak inversion region, yet it is relatively less as compared to a BJT. Secondly, for an ideal operational amplifier, the DC value of the output voltage should follow the DC value at input. This situation can be observed for an amplifier utilized in unity gain configurations for voltage buffering application. But in practice, the output DC value deviates from the input DC value leads generate the input offset voltage for the amplifier. Device-mismatch due to process-induced variations is the major contributing factors to cause the DC value to deviate. This condition tends to limit the accuracy of circuit response. In this context, a Figure of Merit (FOM) called DC accuracy, Acc_{DC}, is defined which is a measure of accuracy of a circuit. It is described as the variation of input offset voltage of an amplifier, V_{OS} or the threshold voltage mismatch of input stage transistors with reference to the maximum input RMS voltage, V_{IN_RMS}. For a typical MOS differential voltage amplifier, the Acc_{DC} for the output value of the amplifier has been mathematically described in detail in [29] and stated as,

$$A_{CC_{DC}} = \frac{V_{IN\_RMS(MAX)}}{3\sigma(V_{OS})} = \frac{V_{OUT\_PP}.\sqrt{WL}}{6\sqrt{2}.A_{VT}.A_{DC}} \tag{2.5}$$

Here V_{outPP} is the maximum output voltage swing which corresponds to supply voltage value, VDD (V), WL is the product of the width, W and the length, L of the transistor, A_{VT} is the process technology parameter and A_{DC} is the DC gain of the amplifier. The equation (2.5) is only used for the purpose of obtaining an insight into a trade-off that exists between the accuracy of the amplifier, its DC gain and area of the input stage transistors. It suggests that a very high DC gain for a differential amplifier stage will tend to lower the value of DC accuracy if all other parameters are maintained the same. Considering the issue of ability to obtain DC gain from a MOS amplifier relative to a BJT amplifier and dc accuracy parameter for MOS differential amplifier, three stages of amplification is chosen where each stage has a moderate DC gain of 40 dB approximately to achieve a 120 dB open loop DC gain. The amplifier design is also restricted to three amplifying stages in order to limit the complexity in stabilising a higher number of stages. Second, we need to identify which stage of the cascaded amplifier will contribute the most towards the input offset voltage. For a cascaded multiple stage voltage amplifier design as shown in Fig. 2.3, it is usually the input stage that is the main source of input offset voltage.

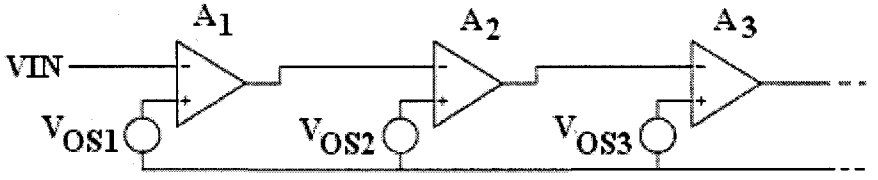


Fig. 2.3: Cascaded amplifier stages [29]

The equivalent input referred offset voltage is given as:

$$\sigma(V_{OSeq}) = \sqrt{\sigma^2(V_{OS1}) + \left(\frac{\sigma(V_{OS2})}{A_1}\right)^2 + \left(\frac{\sigma(V_{OS3})}{A_1.A_2}\right)^2 + \ldots.} \tag{2.6}$$

This relationship [29] shows that the input or the first stage of a cascaded amplifier is critical for precision design. The signal level is small at the input of the amplifier and mismatch effect combined with noise will limit the smallest signal that can be amplified. The input stage must be well matched at the layout level to minimize the effect of process gradients.

The schematic of the proposed topology of a three-stage operational amplifier are shown in Fig. 2.4. The amplifier consists of a rail-to-rail input stage formed with transistors M1 to M12 and load resistors R1 to R8. The load resistors R1, R2, R7, R8 are laser trimmable resistors utilized during offset voltage trimming and R3, R4, R5, R6 are fixed resistors. Since there are two differential pairs in the input stage, their operation is defined on the basis of which differential pair is operating. The operation of the input stage can be divided into three different states based on the input DC voltage of the signal. At low value of input DC voltage, the PMOS differential pair is turned ON, at mid-supply value of DC voltage, both PMOS and NMOS differential pairs are turned ON and at high values of DC input voltage, only the NMOS differential pair is turned ON. Both differential pairs, NMOS and PMOS, are operating in weak-inversion region. In this region the transconductance, g_m of a common-source MOS transistor acting as an amplifier is linearly proportional to the drain current, I_D [20] given by

$$g_m = \frac{I_D}{nV_{TH}} \tag{2.7}$$

Here n represents the sub-threshold slope factor which is between 1 and 2 (1.48 for NMOS and 1.53 for PMOS in TSMC 0.18 um process), V_{TH} = kT/q denotes the thermal voltage where k is the Boltzman constant, q is the electronic charge and T is the temperature in Kelvin. The total trans-conductance when both differential pairs are operating is given as $g_{m\,TOTAL} = g_{mP} + g_{mN}$. In the event, when only one of the pairs is operating, g_{mTOTAL} will also change corresponding to which pair is operating. To maintain g_{mTOTAL} relatively constant in order to have a constant DC gain over

ICMR, a current steering stage [20] is used with the input stage. It consists of current source, M5, a current steering transistor, M6 and a 1:1 current mirror M7-M8. The function of a current steering stage is to maintain a constant sum of tail currents to the PMOS and NMOS differential input transistors as the ICMR changes. This tends to provide a constant $g_{m\ TOTAL}$ for the input stage. If a low value of ICMR voltage is applied to the differential pairs, the bias current from M5 flows only in the PMOS input pair since the NMOS input pair transistors are not operating. At mid-supply input DC values, the current steering transistor, M6 diverts a part of the bias current from M5 and feeds it through the current mirror, M7-M8 to the NMOS input pair. Applying Kirchhoff's current law at the drain of M5, the sum of the tail currents to both differential pairs is equal to the bias current from M5. Further raising the ICMR voltage, M6 diverts current from M5 though the current mirror, M7-M8 into the NMOS input pair while the PMOS pair is turned off. The equation of the DC gain for the input stage based on two port model [16] is given as

$$A_{DC1} = G_m.R_{OUT} \tag{2.8}$$

where G_m and R_{OUT} are given as

$$G_m = g_{mM1} + g_{mM4} \tag{2.9}$$

$$R_{OUT} = \left\{ g_{mM12}.rout_{M12}\left(\frac{rout_{M4}.(R6+R8)}{rout_{M4}+R6+R8}\right) \| \, g_{mM10}.rout_{M10}\left(\frac{rout_{M1}.(R2+R4)}{rout_{M1}+R2+R4}\right)\right\} \tag{2.10}$$

The equation of R_{OUT} is developed by referring to the analysis of a folded cascade amplifier in [16] and applied here to a rail-to-rail amplifier stage. In this case, transistor M12, resistors R6 and R8 and transistor M4 make one pair of folded cascode stage. Similarly, transistor M10, resistors R2 and R4 and transistor M2 make another pair of folded cascode stage. Their equivalent output impedances appear in

parallel at the drains of M10 and M12 and this condition is represented by eq. (2.10) which gives the output impedance for a rail-to-rail amplifier. The input stage is followed by a second stage consisting of a simple differential amplifier stage formed by transistors M13-M17. The DC gain for this stage [30] is given as

$$A_{DC2} = \frac{g_{mM14}}{g_{dsM15} + g_{dsM17}} \tag{2.11}$$

The output of the second stage is connected to common source transistor M24 in the output stage. An intermediate stage consisting of transistors M18-M22 is used which translates the voltage output of the second stage into current mode to bias M23 to operate as a common source stage [21]. This configuration allows AC signal paths at the gates of M23 and M24 to be in the same phase. In the intermediate stage, M18-M20 is a wideband amplifier stage [30, 42] with diode connected load acting as a buffer. The bias current from current source M18 is equally divided between M19 and M20. Current mirrors M20-M21 and M22-M23 have a ratio of 1:1. An approximate equation of DC gain for this stage is given as [30]

$$A_{DC3} \approx \frac{g_{mM19}}{g_{mM20}} \tag{2.12}$$

and finally the small signal equation for DC gain of the Class AB output stage consisting of M23 and M24 is given as [2]

$$A_{DC4} = \frac{g_{mM23} + g_{mM24}}{g_{dsM23} + g_{dsM24}} \tag{2.13}$$

The output stage is designed to drive a capacitive load of 500 pF. The complete amplifier is stabilized by using the Nested-Miller compensation technique proposed in [32, 38]. The capacitors C2 and C3 and resistors R9 and R10 form an internal

compensation network. C1 is used to roll-off the gain of the first stage in order to avoid any zero that could affect the performance of the amplifier in the frequency band of interest.

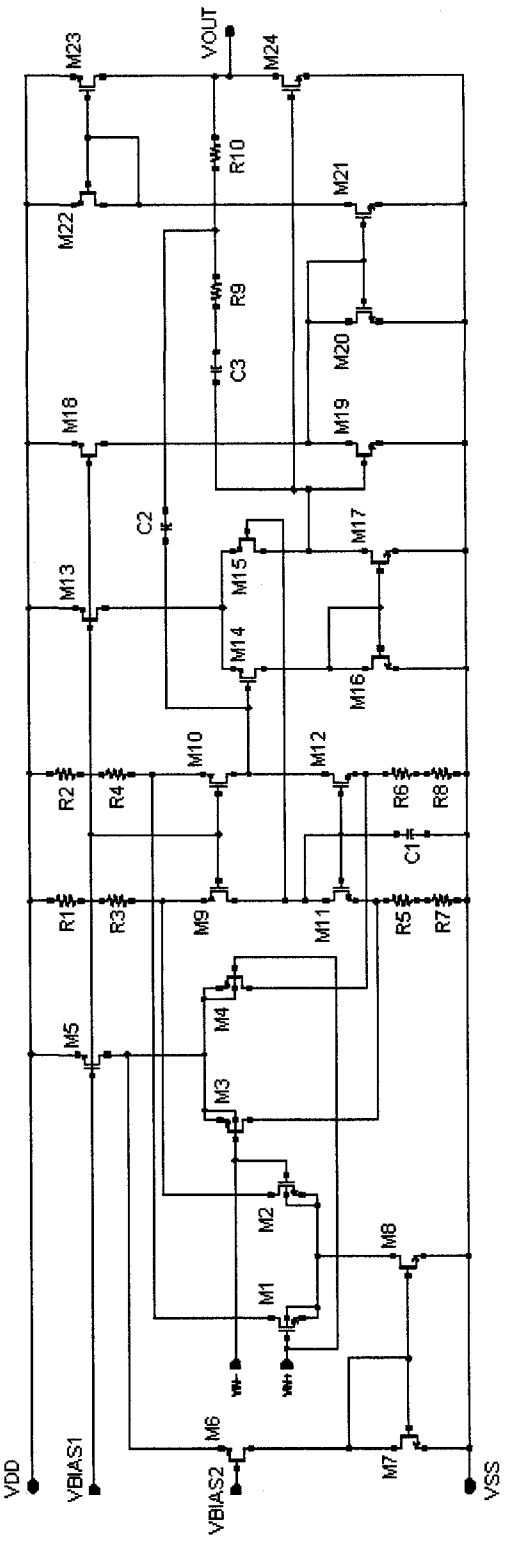


Fig. 2.4: Schematic of the proposed operational amplifier topology

2.3 Effect of Load Resistor Trimming on Offset Voltage

The input stage of the amplifier is shown separately in Fig. 2.5. In this section the effect of varying the value of trimmable load resistors R1, R2 and R7, R8 on offset voltage at the output of the rail-to-rail differential input stage amplifier is considered. This method of analysis is based on the work described in [24] which shows trimming offset voltage of industrial BJT rail-to-rail amplifier using zener zap pads. The value of all resistors R1, R2, R3, R4, R5, R6, R7 and R8 are equal. The analysis is carried out with a current mode method where it is assumed that an output current I_{OUT} is flowing into the drain terminals of M10 and M12, if a non-zero offset voltage exists.

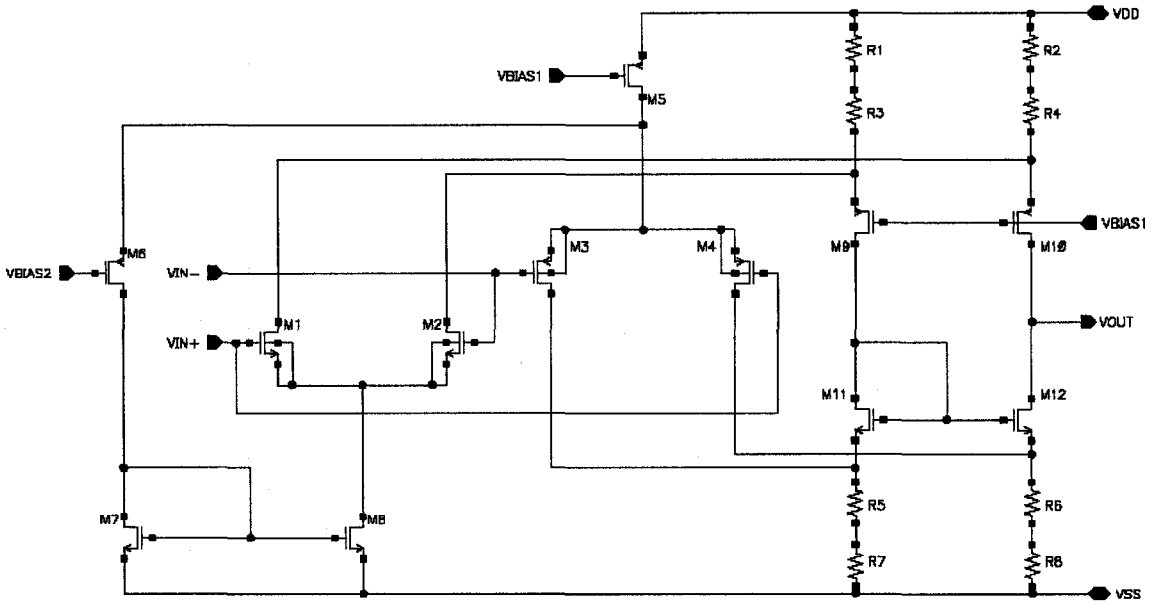


Fig. 2.5: Input stage of the CMOS rail-to-rail operational amplifier

Applying KCL at drain terminals of M10 and M12,

$$I_{OUT} = I_{M12} - I_{M10} \tag{2.14}$$

VBIAS1 is a constant DC voltage provided to bias M5, M9 and M10. For M9-M10, due to biasing constraint and equal value of resistors,

$$V_{SG9} = V_{SG10} \tag{2.15}$$

The tail current M5 is defined to be equal to 2I and this current is divided equally between the NMOS and PMOS differential pairs depending on their operating state. Since all resistors in the input stage are of equal value, it is considered for analysis:

$$V_{R1} = V_{R2} \tag{2.16}$$

or

$$I_{R1}.R1 = I_{R2}.R2 \tag{2.17}$$

$$V_{R7} = V_{R8} \tag{2.18}$$

or

$$I_{R7}.R7 = I_{R8}.R8 \tag{2.19}$$

Case 1: NMOS Differential Pair is ON and PMOS Differential Pair is OFF

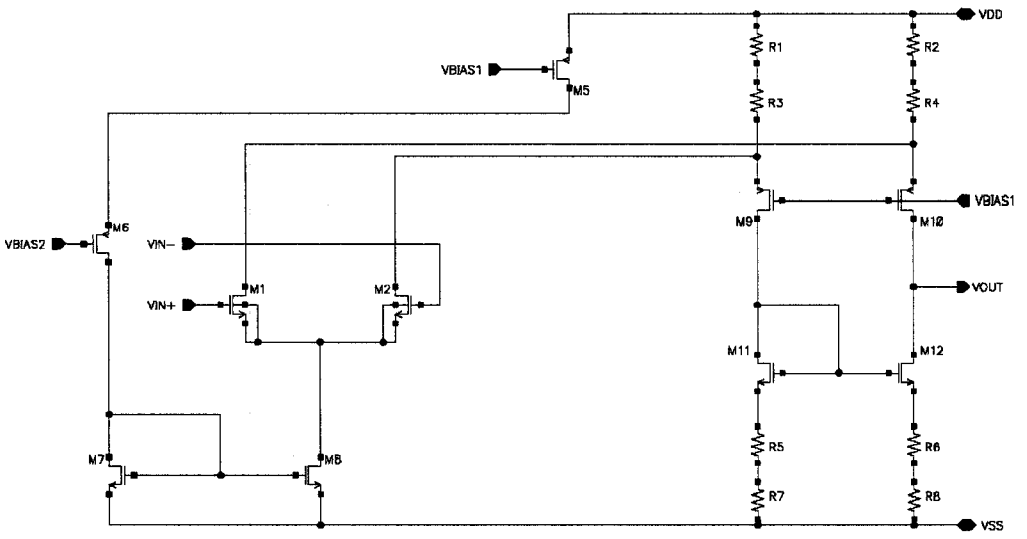


Fig. 2.6: Input stage with NMOS differential pair turned ON

This condition occurs when the ICMR voltage is at a high value during which only NMOS differential input transistors are operating and PMOS transistors are turned OFF. The circuit while NMOS pair is ON is as shown in the Fig. 2.6 forming a folded-cascode differential amplifier with NMOS input. The current distribution equation in the input stage during this circuit condition is given as follows,

$$I_{M5} = I_{R1} = I_{R2} = 2I \tag{2.20}$$

$$I_{M6} = I_{M7} = I_{M8} = 2I \tag{2.21}$$

$$I_{M1} = I_{M2} = I \tag{2.22}$$

$$I_{R7} = I_{R8} = I \tag{2.23}$$

First, the effect of trimming on R1 and R2 is considered assuming no trimming on R7 and R8. Solving for I_{M12} in eq. (2.14),

$$I_{M12} = I_{M11} = I_{M9} = I_{R1} - I_{M2} \tag{2.24}$$

$$I_{M12} = I_{R2} \cdot \frac{R2}{R1} - I_{M2} \tag{2.25}$$

$$I_{M12} = 2I_{R8} \cdot \frac{R2}{R1} - I \tag{2.26}$$

$$I_{M12} = 2I_{R7} \cdot \frac{R7\ R2}{R8\ R1} - I \tag{2.27}$$

$$I_{M12} = 2I \cdot \frac{R7\ R2}{R8\ R1} - I \tag{2.28}$$

Solving for I_{M10} in eq. (2.14),

$$I_{M10} = I_{R2} - I_{M1} \tag{2.29}$$

$$I_{M10} = I_{R1} \cdot \frac{R1}{R2} - I \tag{2.30}$$

$$I_{M10} = 2I \cdot \frac{R1}{R2} - I \tag{2.31}$$

Substituting the values of I_{M12} and I_{M10} in eq. (2.14), it gives

$$I_{OUT} = 2I \cdot \frac{R7\ R2}{R8\ R1} - 2I \cdot \frac{R1}{R2} \tag{2.32}$$

Now, the effect on trimming R7 and R8 is considered

$$I_{OUT} = I_{M12} - (I_{R2} - I_{M1}) \tag{2.33}$$

$$I_{OUT} = I_{R8} - (2.I_{R8} - I) \tag{2.34}$$

$$I_{OUT} = -\left(I_{R7} \cdot \frac{R7}{R8} - I\right) \tag{2.35}$$

Using the Superposition Principle [43], which states that, "If cause and effect are linearly related, the total effect of several causes acting simultaneously is equal to the sum of the effects of the individual causes acting one at a time." Then the total I_{OUT} is the sum of Eq. (2.32) and (2.35) defined as

$$I_{OUT} = 2I\left(\frac{R7\,R2}{R8\,R1} - \frac{R1}{R2}\right) - I\left(\frac{R7}{R8} - 1\right) \tag{2.36}$$

Case 2: PMOS Differential Pair is ON and NMOS Differential Pair is OFF

This condition occurs when the ICMR voltage is at a low value during which only PMOS differential input transistors are operating and NMOS transistors are turned OFF. The circuit while PMOS pair is ON is as shown in the Fig. 2.7 forming a folded-cascode differential amplifier with NMOS input. The current distribution equation in the input stage during this circuit condition is given as follows,

$$I_{M5} = I_{R1} = I_{R2} = 2I \tag{2.37}$$

$$I_{M3} = I_{M4} = I \tag{2.38}$$

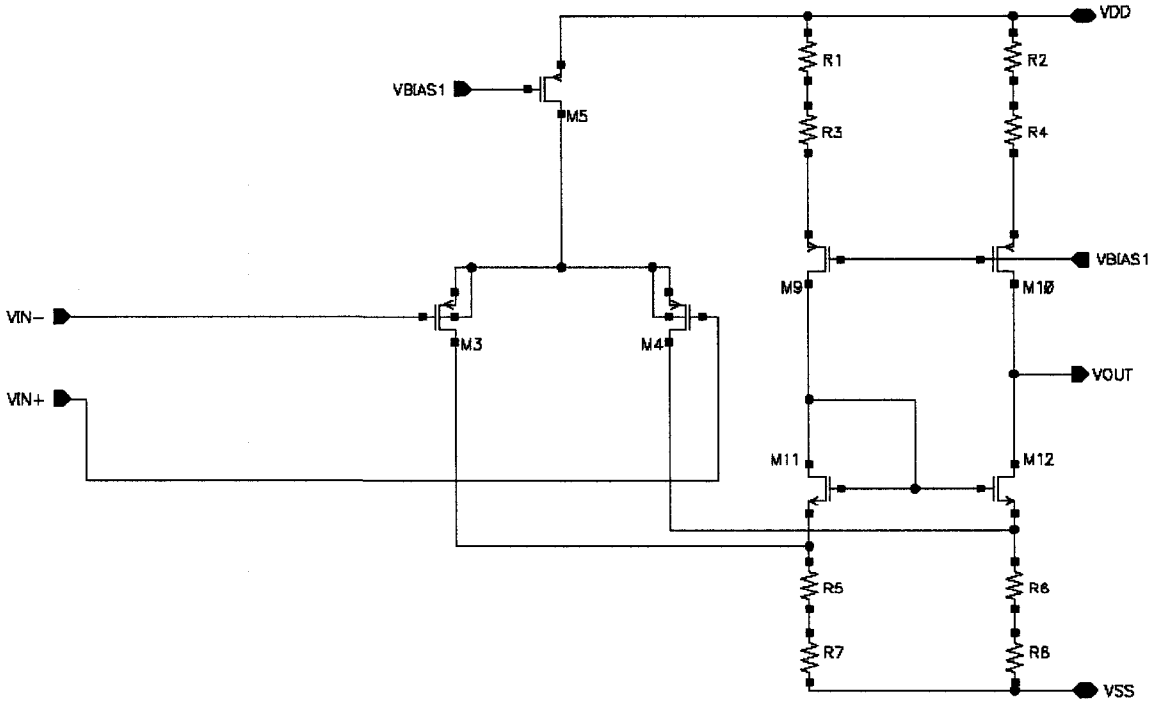


Fig. 2.7: Input stage with PMOS differential pair turned ON only

$$I_{R7} = I_{R8} = 3I \tag{2.39}$$

In this analysis, similar equation is derived as (2.36). Solving for I_{M12} in eq. (2.14),

$$I_{M12} = I_{R8} - I_{M3} \tag{2.40}$$

$$I_{M12} = I_{R7}.\frac{R7}{R8} - I \tag{2.41}$$

$$I_{M12} = (I_{R1} + I_{M4}).\frac{R7}{R8} - I \tag{2.42}$$

$$I_{M12} = I_{R2}\left(\frac{R7\,R2}{R8\,R1}\right) + I_{M4}\left(\frac{R7}{R8}\right) - 1 \tag{2.43}$$

$$I_{M12} = 2I\left(\frac{R7\,R2}{R8\,R1}\right) + I\left(\frac{R7}{R8}\right) - 1 \tag{2.44}$$

Solving for I_{M10} in eq. (2.14),

$$I_{M10} = I_{R2} = I_{R1}.\frac{R1}{R2} = 2I.\frac{R1}{R2} \tag{2.45}$$

Substituting the values of I_{M12} and I_{M10} in eq. (2.14) from eq. (2.44) and eq. (2.45) respectively,

$$I_{OUT} = 2I\left(\frac{R7\,R2}{R8\,R1} - \frac{R1}{R2}\right) + I\left(\frac{R7}{R8} - 1\right) \tag{2.46}$$

The two equations (2.36) and (2.46) differ from each other by the sign of the second term. This show that an adjustment in the value of resistors R7 or R8 will have an influence on I_{OUT} depending on which differential pair is in operation. Based on the same equations, an adjustment in the value of resistors R1 or R2 in the first term will affect I_{OUT} which is independent of which differential pair is operating. The presence of the R7 and R8 with R1 and R2 in the first term of the equations indicates that the adjustment in the value of resistors is inter-related.

2.3.1 Interpretation of the Offset Voltage Trimming Analysis

The equations (2.36) and (2.46) derived earlier are re-written here for further analysis and interpretation. The term I_{OUT} in these two equations has been represented as I_{OUT_NMOS} and I_{OUT_PMOS} to define equations for NMOS and PMOS folded cascode differential pairs, respectively. The condition when only NMOS differential pair is operating, I_{OUT} has been derived as

$$I_{OUT\_NMOS} = 2I\left(\frac{R7\,R2}{R8\,R1} - \frac{R1}{R2}\right) - I\left(\frac{R7}{R8} - 1\right) \tag{2.47}$$

and for condition when only PMOS differential pair is operating, I_{OUT} has been derived as

$$I_{OUT\_PMOS} = 2I\left(\frac{R7\,R2}{R8\,R1} - \frac{R1}{R2}\right) + I\left(\frac{R7}{R8} - 1\right) \tag{2.48}$$

For eq. (2.47) and (2.48), considering the situation that the upper load resistors, R1 and R2 are perfectly matched leading to the ratio R1/R2 and R2/R1 equal to unity and R7 or R8 is varied such that the ratio R7/R8 is not unity. This condition can be stated as

$$\frac{R1}{R2}=\frac{R2}{R1}=1 \tag{2.49}$$

$$\frac{R7}{R8}=X \tag{2.50}$$

Substituting for the values from eq. (2.49) and (2.50) in eq. (2.47) gives

$$I_{OUT\_NMOS}=2I\,(X-1)-I\,(X-1) \tag{2.51}$$

$$I_{OUT\_NMOS}=I\,(X-1) \tag{2.52}$$

and substituting for the values from eq. (2.49) and (2.50) in eq. (2.48) gives

$$I_{OUT\_PMOS}=2I\,(X-1)+I\,(X-1) \tag{2.53}$$

$$I_{OUT\_PMOS}=3I\,(X-1) \tag{2.54}$$

Comparing eqs. (2.52) and (2.54) indicates that a change in the ratio of R7/R8 will affect I_{OUT} by a factor of three times more for PMOS folded cascode differential pair than NMOS folded cascode differential pairs. A correlation can be drawn from eqs. (2.52) and (2.54) given as

$$I_{OUT\_PMOS}=3.\,I_{OUT\_NMOS} \tag{2.55}$$

This shows that I_{OUT_PMOS} is three time more sensitive to any changes in the ratio, R7/R8, relative to I_{OUT_NMOS}. Next in this analysis, it is considered that R7 and R8 are perfectly matched and R1 or R2 are changed in eqs. (2.47) and (2.48) such that the ratio R1/R2 and R2/R1 is not unity. This can be mathematically stated as

$$\frac{R7}{R8} = 1 \tag{2.56}$$

$$\frac{R2}{R1} = Y \tag{2.57}$$

Substituting for the values from eq. (2.56) and (2.57) in eq. (2.47) gives

$$I_{OUT\_NMOS} = 2I\left(Y - \frac{1}{Y}\right) \tag{2.58}$$

and substituting for the values from eq. (2.56) and (2.57) in eq. (2.48) gives

$$I_{OUT\_PMOS} = 2I\left(Y - \frac{1}{Y}\right) \tag{2.59}$$

Equations (2.57) and (2.58) show that IOUT_PMOS and IOUT_NMOS represent same values, respectively and this leads to

$$I_{OUT\_PMOS} = I_{OUT\_NMOS} \tag{2.60}$$

This shows that for a matched pair of resistors R7 and R8, a change in the ratio of R1 and R2 will have the influence on the term I_{OUT} by the same factor for PMOS and NMOS folded cascode differential pair.

To summarize, the current-mode trimming analysis presented above has been interpreted in terms of voltage-mode for reducing the offset voltage of a rail-to-rail amplifier. For such an input differential pair, the input offset voltage, V_{OS} will vary according to three different states of operation depending on the DC value of the input signal – Only PMOS pair is ON (high common mode), both NMOS and PMOS pairs are ON (mid-supply common mode) and only NMOS pair is ON (lower

common mode). Let $V_{OS(P)}$ and $V_{OS(N)}$ represent the individual offset voltage for P and N type folded cascode differential stages respectively. When both pairs are operating, the total offset voltage, V_{OS} is due to contribution of both $V_{OS(P)}$ and $V_{OS(N)}$. Broadly, the trimming is performed in two steps as outlined:

STEP No. 1: Laser Trimming of Lower Load Resistors - R7 or R8

It is deduced from eq. (2.55), that $V_{OS(P)}$ is three time more sensitive to changes in R7 or R8 than $V_{OS(N)}$. So, trimming is preferred to produce a change in $V_{OS(P)}$. The ratio R7/R8 is adjusted by laser-trimming R7 or R8 until $V_{OS(P)}$ becomes approximately equal to $V_{OS(N)}$. This step is equivalent to reducing the difference $|V_{OS(P)} - V_{OS(N)}|$ to near zero volts. This is the first step involved in trimming the offset voltage of the amplifier. Since the sensitivity of $V_{OS(P)}$ is more than $V_{OS(N)}$, so trimming at low common mode DC value is performed keeping only the PMOS differential pair in operation.

STEP No. 2: Laser Trimming of Upper Load Resistors - R1 or R2

It is determined from eq. (2.60), trimming of R1 or R2 which will cause both $V_{OS(P)}$ and $V_{OS(N)}$ to be influenced by the same amount. This step involves trimming at mid-supply common mode voltage when both PMOS and NMOS differential input pairs are operating. The trimming is performed until a target value of the offset voltage is attained.

The possible cases that can be observed for an un-trimmed input offset voltage, V_{OS}, over common mode input voltage range, V_{IN}, during experimental verification at wafer level are shown in Fig. 2.8 and 2.9. At lower common mode voltages, offset voltage due to PMOS differential pair, $V_{OS(P)}$ dominates while at higher common mode voltage, offset voltage due to NMOS differential pair, $V_{OS(N)}$ dominates. For the input voltages centered on mid-supply values, both PMOS and NMOS differential pair contribute to the total value of input offset voltage. It must be noted that the choice of resistors to be trimmed depends on the polarity of the DC offset voltage. So, the initial step should be to determine the polarity of offset voltage before applying any trimming sequence. As shown in Fig. 2.8 and 2.9, the offset

voltage curve can possibly lie in the positive quadrant, negative quadrant or in between the two quadrants. There are two special cases 7 and 8 in Fig. 2.9 which shows that $V_{OS(N)}$ and $V_{OS(P)}$ are approximately the same. Under this situation, there is no need to trim the lower of resistors, R7 and R8, as $V_{OS(P)}$ and $V_{OS(N)}$ have similar values. These two cases will not require Step No. 1 for trimming as described previously where one of the lower resistors is trimmed. Only upper resistors, R1 or R2 are trimmed from Step No. 2. Based on eight possible cases of untrimmed offset voltage versus input voltage range, Table 2.1 shows resistor selection guidelines for trimming the offset voltage. This data is obtained by creating these eight cases during DC simulations of the amplifier topology shown in Fig. 2.4 and using the equations (2.36) and (2.46). The simulation set-up utilized non-inverting unity gain configuration to obtain offset voltage curves similar to the eight cases. The input range involved sweeping it from 0 to supply voltage, VDD. Finally, a flow chart is shown in Fig. 2.10 describing a generalized method used for trimming. It should be used with reference to offset curve cases and resistor selection table to determine resistors to be trimmed.

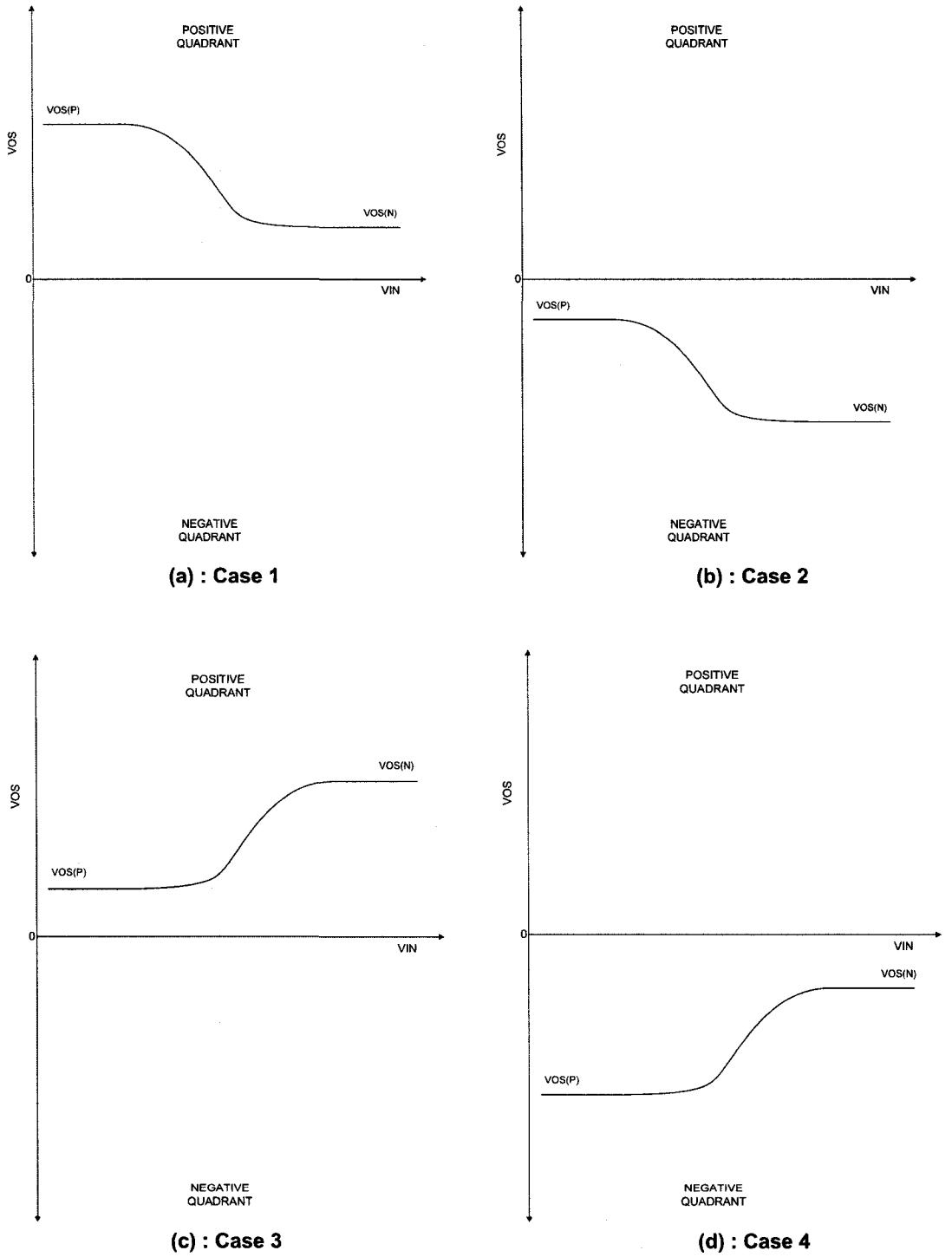


Fig. 2.8: Un-trimmed input offset voltage curve cases over ICMR

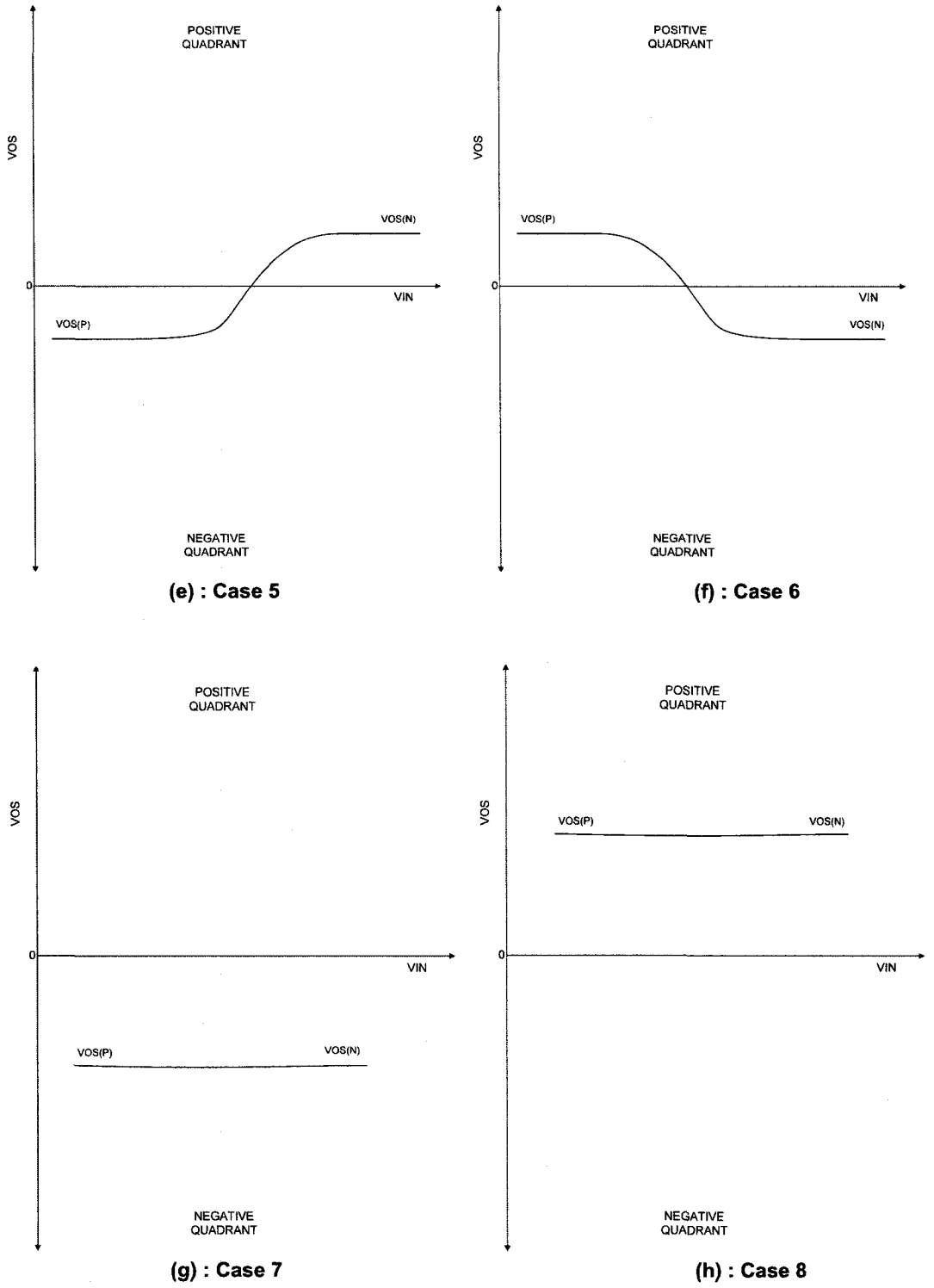


Fig. 2.9: Un-trimmed input offset voltage curve cases over ICMR

Table 2.1: Resistor selection for input offset voltage trimming sequence over ICMR

Untrimmed V_{OS} Case	Step No. 1	Step No. 2	Remarks
1	Trim R7	Trim R2	Trim R7 to lower $V_{OS(P)}$ down to $V_{OS(N)}$. Trim R2 to lower both $V_{OS(P)}$ and $V_{OS(N)}$.
2	Trim R7	Trim R1	Trim R7 to lower $V_{OS(P)}$ down to $V_{OS(N)}$. Trim R1 to raise both $V_{OS(P)}$ and $V_{OS(N)}$.
3	Trim R8	Trim R2	Trim R8 to raise $V_{OS(P)}$ to $V_{OS(N)}$. Trim R2 to reduce both $V_{OS(P)}$ and $V_{OS(N)}$.
4	Trim R8	Trim R1	Trim R8 to raise $V_{OS(P)}$ to $V_{OS(N)}$. Trim R1 to raise both $V_{OS(P)}$ and $V_{OS(N)}$.
5	Trim R8	Trim R2	Trim R8 to lower $V_{OS(P)}$ down to $V_{OS(N)}$. Trim R2 to lower both $V_{OS(P)}$ and $V_{OS(N)}$.
6	Trim R7	Trim R1	Trim R7 to raise $V_{OS(P)}$ till to $V_{OS(N)}$. Trim R1 to raise both $V_{OS(P)}$ and $V_{OS(N)}$.
7	----	Trim R1	Trim R1 to raise both $V_{OS(P)}$ and $V_{OS(N)}$.
8	----	Trim R2	Trim R2 to lower both $V_{OS(P)}$ and $V_{OS(N)}$.

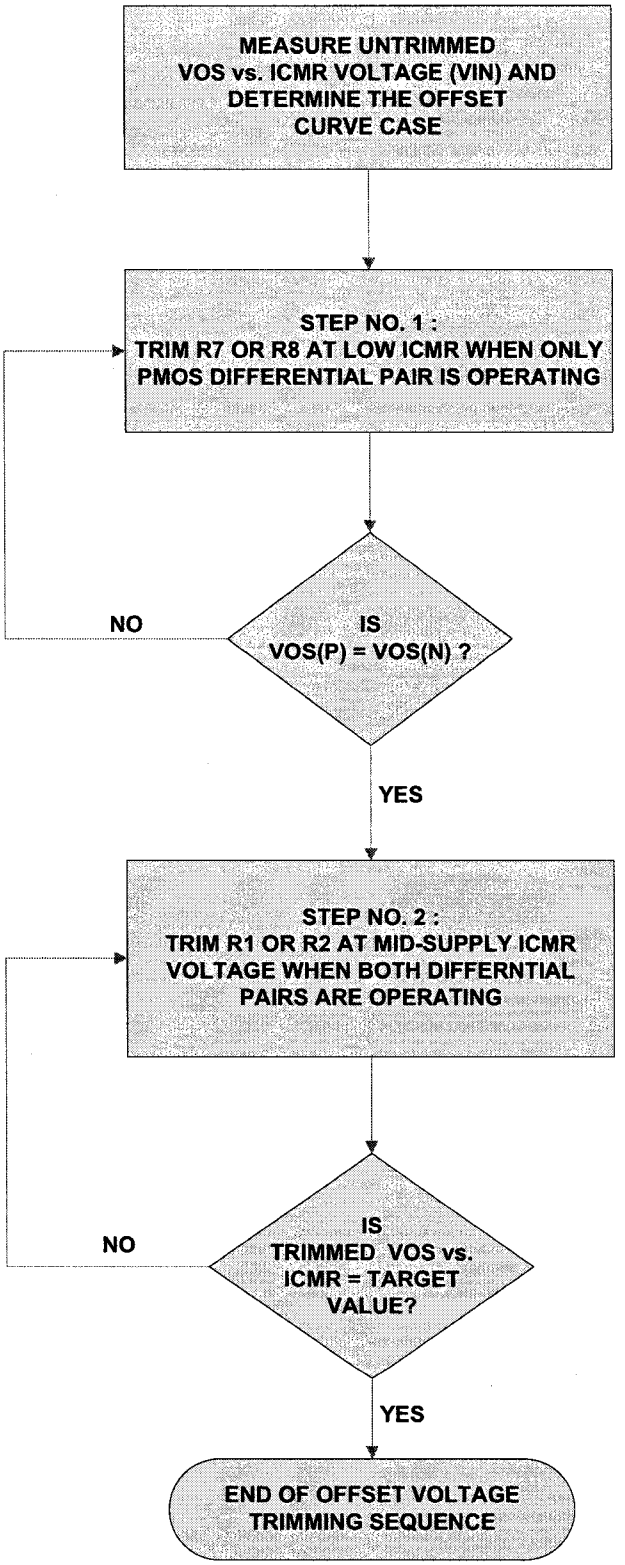


Fig. 2.10: Flow-chart for input offset voltage trimming sequence steps over ICMR

2.4 CMOS PTAT Bias Circuit Design

A CMOS Proportional-To-Absolute-Temperature (PTAT) bias circuit for the amplifier is shown in Fig. 2.11, where M11 to M22 forms the biasing core which is a variant of the topology described in [1]. M11, M12, M14, M15 and M16 form the NMOS wide swing cascade current mirror. M17, M18, M19, M20 and M22 form the PMOS wide swing cascade current mirror. M16 and M22 are diode connected transistors to provide biasing voltage to cascode transistors M15, M14 and M17, M18, respectively. The wide-swing cascode current mirrors are used to minimize the dependence of drain voltage on currents since it has high output impedance [25].

The operation of this circuit is based on the principle that a current is generated due to the difference in V_{GS} of M19 and M20 that develops across the resistor R_{BIAS} [33]. This is achieved by designing Width/Length (W/L) ratio of M19 larger than that of M20. In this case, the ratio for M19 is two times the ratio of M20. Transistors M19 and M20 operate in sub-threshold region. M19 and M20 carry the same drain currents and this condition is imposed by the PMOS wide swing current mirror, therefore, the larger device, M19, has a smaller value of V_{GS} than the smaller device, M20. This difference in V_{GS} appears across the resistor R_{BIAS}. These conditions, coupled with the wide swing current mirror M11-M15, produce a current flowing through R_{BIAS} which is a function of temperature only, independent of supply variation. Applying Kirchhoff's law around the loop formed by M19, M20 and R1,

$$V_{GS20} = V_{GS19} + I_{BIAS}. R_{BIAS} \tag{2.61}$$

For a MOS transistors operating in weak inversion, the drain current is approximately given by an exponential relationship given by [25, 30]

$$I_D \quad I_O \left(\frac{W}{L}\right) e^{\left(\frac{V_{GS}}{nV_{TH}}\right)} \tag{2.62}$$

Here n represents the sub-threshold slope factor, V_{TH} = kT/q denotes the thermal voltage where k is the Boltzman constant, q is the electronic charge and T is the temperature in Kelvin. The values of V_{GS} can then be expressed as

$$V_{GS} = nV_T \ln\left(\frac{I_D}{I_O(W/L)}\right) \tag{2.63}$$

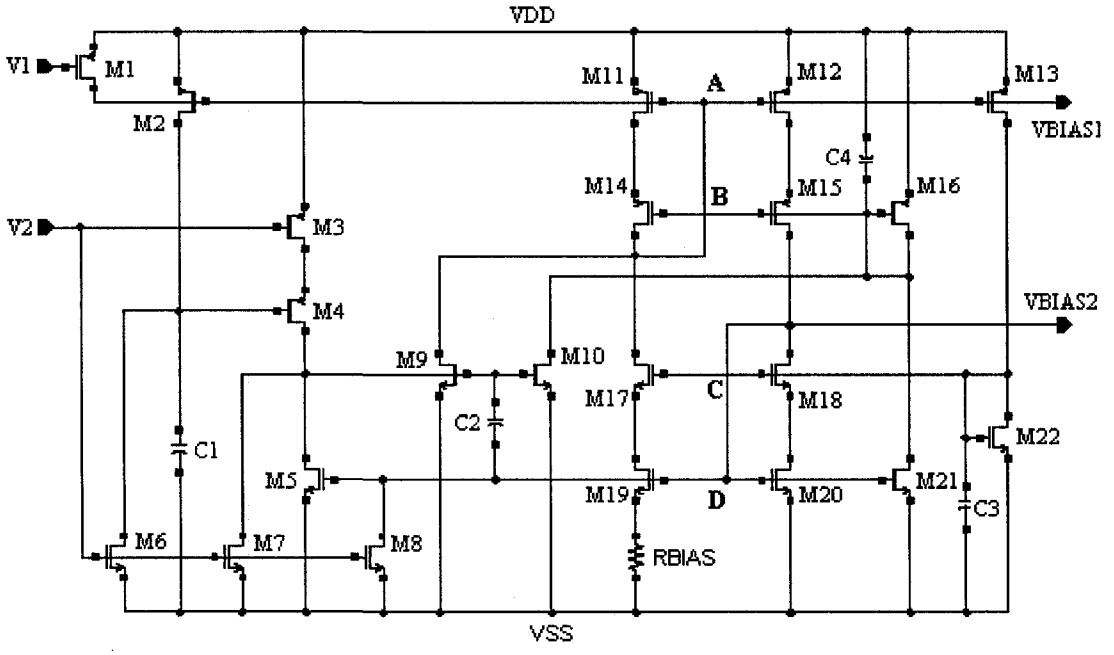


Fig. 2.11: CMOS PTAT Bias Circuit

M19 and M20 operate in sub-threshold region which carry equal drain currents, then substituting for the values of V_{GS20} and V_{GS19} in eq. (2.61) based on eq. (2.63) will lead to

$$I_{BIAS} = \frac{nV_{TH}\ln(M)}{R_{BIAS}} \tag{2.64}$$

Here M is the ratio, which is greater than one given as

$$M = \left(\frac{W}{L}\right)_{19} \Big/ \left(\frac{W}{L}\right)_{20} \tag{2.65}$$

Eq. (2.64) denotes that I_{BIAS} is proportional to T while other terms are numerical constants, hence the name PTAT (Proportional-To-Absolute-Temperature) bias circuit. This statement is correct to first order approximation and the biasing current value, I_{BIAS}, is expected to shift over process variations caused during fabrication of R_{BIAS}. The requirement of PTAT bias circuit is governed by the fact that the differential pairs used in the amplifier topology of Fig. 2.4 are operating in weak-inversion mode. A MOS transistor as an amplifier has its trans-conductance, g_m given by Eq. (2.7) which is inversely proportional to temperature. Therefore, using a PTAT biased drain current as defined by Eq. (2.64) will tend to make g_m independent of temperature to first order. This also helps to stabilize unity gain bandwidth variation over temperature as g_m variations are minimized [23].

In order to maintain a single operating state for the biasing core, a start-up circuit is implemented with transistors M1 to M10. V1 and V2 are external supply voltages applied to keep the start-up circuit in operation. V1 is set to VDD and V2 is set to GND for start-up circuit to operate in ENABLE mode. This is because there is a possible stable state in which the bias currents are zero. The start-up circuit is required to affect the bias loop only when all the currents in the bias loop are zero. Under zero bias conditions, all currents in the bias core are zero. Nodes A and B stay at VDD and nodes C and D stay at GND. M5 and M2 is in turned-off state. The initial charge on the capacitor, C1 is zero or the voltage across the capacitor is zero. M3 is biased at 0 V while M4 observes 0 V at its gate due to the initial voltage across the capacitor. So, M3-M4 act as high impedance loads that are turned ON. As a result, the gates of M9-M10 are pulled high, since M5 is non-conducting. M9-M10 start conducting that will inject current into the bias loop by pulling down the gates of M11-M12 and M14-M15. This causes a current to flow in the bias core pulling up the gate of M5 and turning it ON. This creates a DC current path through M3-M4 which

will cause the gate voltage M9-M10 to fall eventually to zero causing them to turn OFF. On the other hand, the instant when M11-M12 are turned ON, M2 is also tuned ON which sinks current from VDD into the capacitor, C1, charging it until VDD. As C1 is charged until VDD, it eventually turns OFF M4 blocking any DC path through M3.

During the DISABLE operating mode, V1 is set at 0 V turning M1 ON causing the gate voltage of M2 to pull up at VDD. V2 is set at VDD value causing M6, M7, M8 to turn ON and pulling down the drain voltage to GND. These conditions will turn OFF the bias core. The circuit has two biasing voltages, VBIAS1 and VBIAS2 corresponding to node A and D which are used to generate bias points for the amplifier. The node voltages inside the PTAT bias circuit are a shown in Fig. 2.12 when the supply voltage is ramped from 0 to 3.3 V. It illustrates that the node voltages reach their stable biasing points.

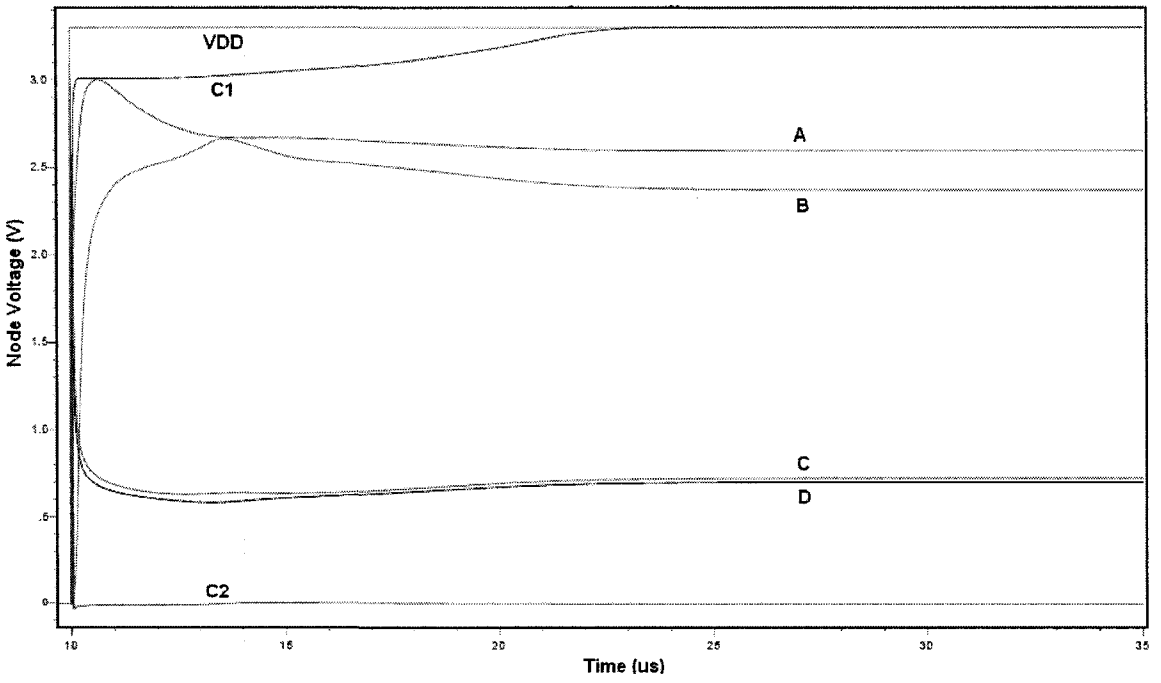


Fig. 2.12: Node voltages in PTAT bias circuit for supply voltage ramp

2.5 IC Layout Implementation

The layout of the operational amplifier and the bias circuit has been implemented using 1P6M (Single Poly layer and Six Metal layers) TSMC CMOS 0.18 μm process technology. Once matching considerations are taken care of during circuit design, the next important phase is layout design. A bad layout design will contribute to higher mismatches between devices, leading to a higher input offset voltage for the amplifier. The layout of the amplifier with the bias circuit is shown in Fig. 2.13.

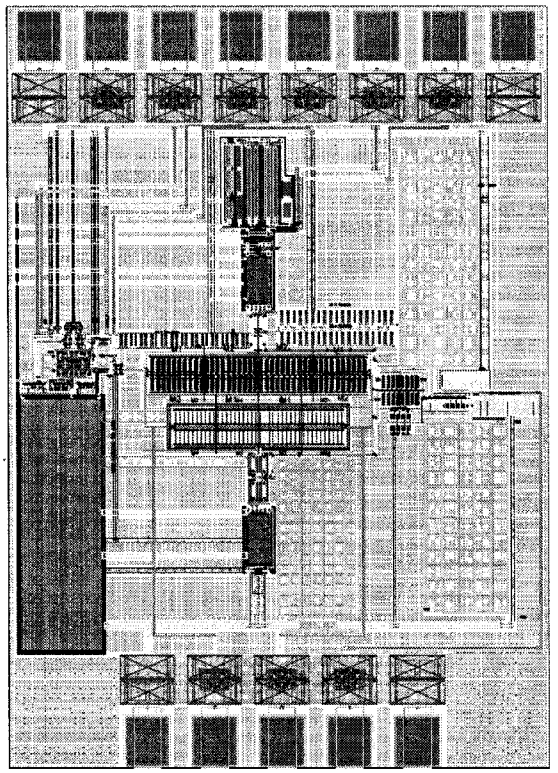


Fig. 2.13: Layout of the fabricated chip

All critically matched devices including those in the amplifier and the bias generator are designed with state-of-the-art layout matching techniques applied to transistors and resistors [18]. Good device matching is essential to reduce or cancel variations due to the manufacturing process. Identical transistors that constitute a part

of differential pairs and current mirrors are highly susceptible to mismatches and for this reason, matched pairs with large area transistors are designed with a common centroid layout. For the bias part, the wide-swing current mirrors are laid out as common centroid layout for a configuration shown in Fig. 2.14. For a PMOS wide-swing current mirror, the matching critical pairs are M11-M12 and M14-M15. To minimize bulk-source voltage mismatch for cascode transistors, M14 and M15, both transistors are built in separate Hot N-wells so that their bulk and source nodes are connected to each other. A Hot N-well is defined as a well not connected to VDD and it is left floating. Referring to Fig. 2.13, M11-M12 corresponds to A-B layout and M14-M15 corresponds to C-D setup on layout. For the case concerning, NMOS wide swing current mirror, transistor pair M17-M18 is matched on layout that corresponds to a layout style shown in Fig. 2.15. Transistors M19 and M20 are not matched as M19 is designed in Deep N-well so as to maintain zero bulk-source voltage drop like M20 which is built in p-substrate. The resistor R_{BIAS} of 200 KΩ is laid out in a serpentine fashion.

The transistors in the amplifier are also matched especially for the input stage, the matching is critical as it has the highest contribution to offset voltage. First the differential pairs of the input stage, both transistor pairs M26-M27 and M29-M30 are laid in a common centroid style as shown in Fig. 2.16.

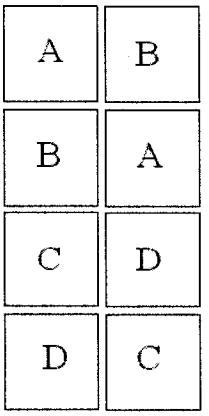


Fig. 2.14: Layout configuration

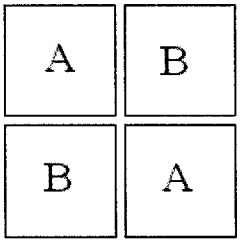


Fig. 2.15: Layout configuration

The PMOS differential pair (M29-M30) is built in Hot N-well and the NMOS differential pair (M26-M27) is built in Deep N-well. This allows them to have zero bulk-source voltage dependence and also isolates them from any substrate noise. The transistor pairs M31-M32, M33-M34, M37-M38 and M39-M40 are all based on the common centroid layout configuration as shown earlier in Fig. 2.15. The matching of current mirror pairs M42-M43 and M45-M46 is relatively relaxed since the output stage contributes the least towards the offset voltage. The layout here involves unit-matching principle [2] which involves creating geometrically equivalent components by drawing them as identical units adjacent to each other. The passive elements of the rail-to-rail input stage, the P+ poly-resistors are also matched and follow an interdigitated common centroid layout pattern as depicted in Fig. 2.17.

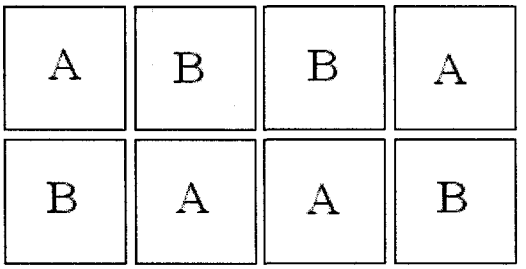


Fig. 2.16: Layout configuration

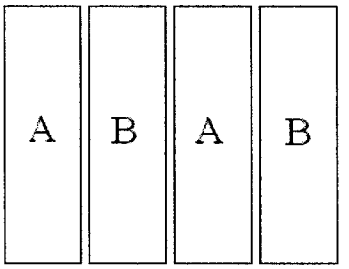


Fig. 2.17: Layout configuration

The following statements outline basic analog layout considerations followed for the amplifier and the bias circuit design:

1. Large area devices are built from unit sized elements [25].
2. Distance between the matched elements is kept to a minimum as allowed by the topology and the design rules of TSMC 0.18 μm CMOS process.
3. To maintain similar environment around matched elements, dummies were utilized [18, 30].
4. Critically matched transistors of the input differential stage are placed on the die's center axis where low stress gradients occur to minimize sensitivity to die stress due to packaging [5].

5. MOS transistors exhibit different motilities in different orientations. So, same orientation of devices to be matched is maintained throughout the design such that the current flows in the same direction [30].
6. Identical metal fill patterns are placed surrounding the matched elements especially for the input differential transistors [46].
7. Resistors are designed with relaxed design rules to improve matching between them [48].

CHAPTER 3

Simulation Results and Experimental Verification

This chapter describes the simulation results of the extracted layout of the operational amplifier and PTAT bias circuit. The simulation results present the response of the integrated amplifier circuit over process corners and temperature range of -40^0C to $+85^0$C. Simulation results are presented to demonstrate steps for trimming the input offset voltage (V_{OS}) over Input Common Mode Range (ICMR) for the proposed amplifier topology. The chip is fabricated in single-poly, six metal, MiM capacitor TSMC 0.18 μm process technology with 40-pin DIP package. The amplifier test results obtained during experimental verification of the chip are presented along with offset voltage trimming using P+ poly resistors.

3.1 Simulation Results

In this section, post-layout results are presented to verify the functionality of the amplifier before fabrication. The primary task followed during schematic design phase was to maintain the stability of DC operating points over process and temperature variations. After this, AC parameters were verified as per specifications. The simulations were performed using spectre. The supply voltage used is 3.3 V. The dc output voltage values for the amplifier under process and temperature variations are shown in Table 3.1. These DC operating points indicate the variation in the output DC value of the amplifier under device-matched conditions. It is imperative for a robust design that there should not be a very large deviation in DC operating point values over process and temperature variations. This is followed by simulation DC gain values over process and temperature variations. Table 3.2 indicates the DC gain (dB) values at 1 KHz.

Table 3.1: Operating point values for output DC node voltage (V) over process and temperature

TEMP. (^{0}C)	TT	SS	FF	FS	SF
25	1.650	1.871	1.765	1.642	2.003
85	1.774	1.999	1.862	1.741	2.123
-40	1.530	1.743	1.670	1.546	1.884

Table 3.2: DC operating point values for DC gain (dB) over process and temperature

TEMP. (^{0}C)	TT	SS	FF	FS	SF
25	123.0	124.8	111.9	116.0	119.6
85	120.0	122.4	109.6	113.7	117.1
-40	125.4	127.0	114.3	118.2	121.9

The results from Table 3.1 and 3.2 show variations of DC points and DC gain over process corners and a wide temperature range. The plots for DC gain and phase margin for Typical-Typical (TT) process corner are given in Fig. 3.1 and Fig. 3.2 to demonstrate the stability of the amplifier. A phase margin of approximately 63^0 has been achieved. In order to demonstrate the operation of the rail-to-rail input feature

using the current steering stage, Fig. 3.3 shows a plot of variation of the low frequency gain measured at 1 KHz over the entire common mode input voltage range from 0 to 3.3 V. These results, performed for all process corners, indicate a uniform trans-conductance control. Fig. 3.4 indicates simulated large signal response of the amplifier with a square wave input signal 3.3 V_{P-P} and simulated slew rate for the amplifier is 0.24 V/μs. Fig. 3.5 shows simulated small signal response of the amplifier with a square wave input signal 100 mV_{P-P} and simulated settling time for the amplifier is 2.8 μs. The small signal square wave response also indicates the stability of the amplifier indicating it is closer to critically damped case [30] and shows no ringing corresponding to 63^0 phase margin.

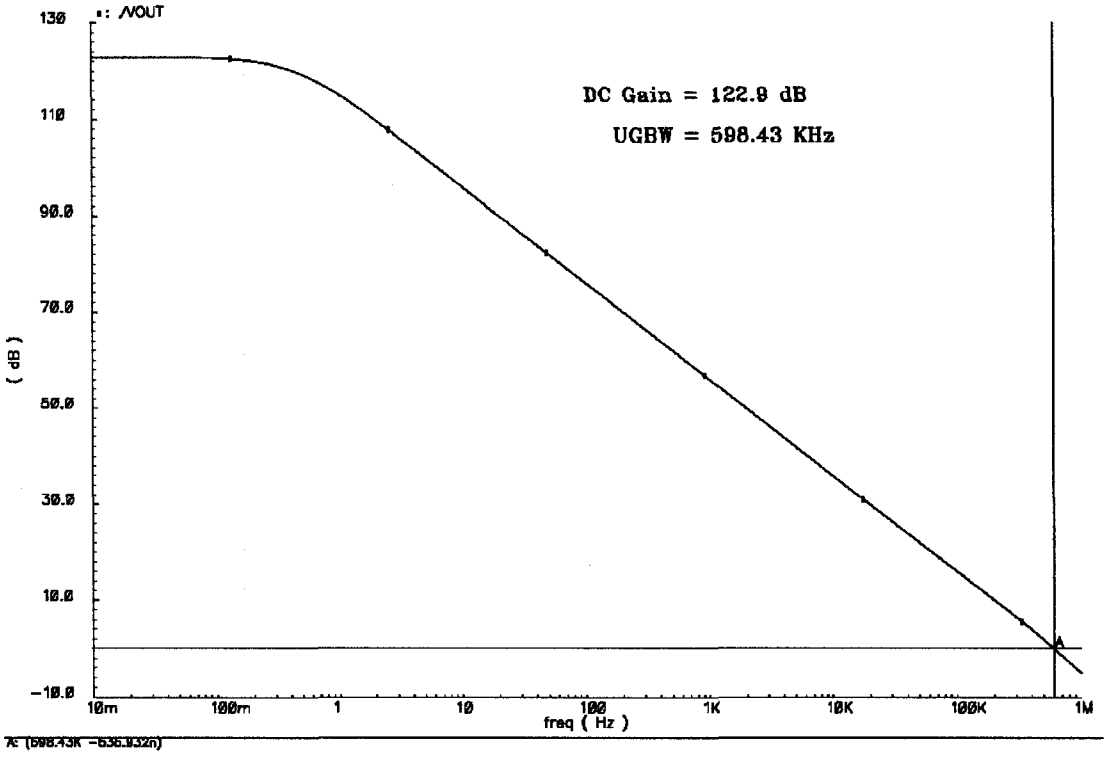


Fig. 3.1: Simulated DC gain of the amplifier at T = 25 ^{0}C for TT process corner

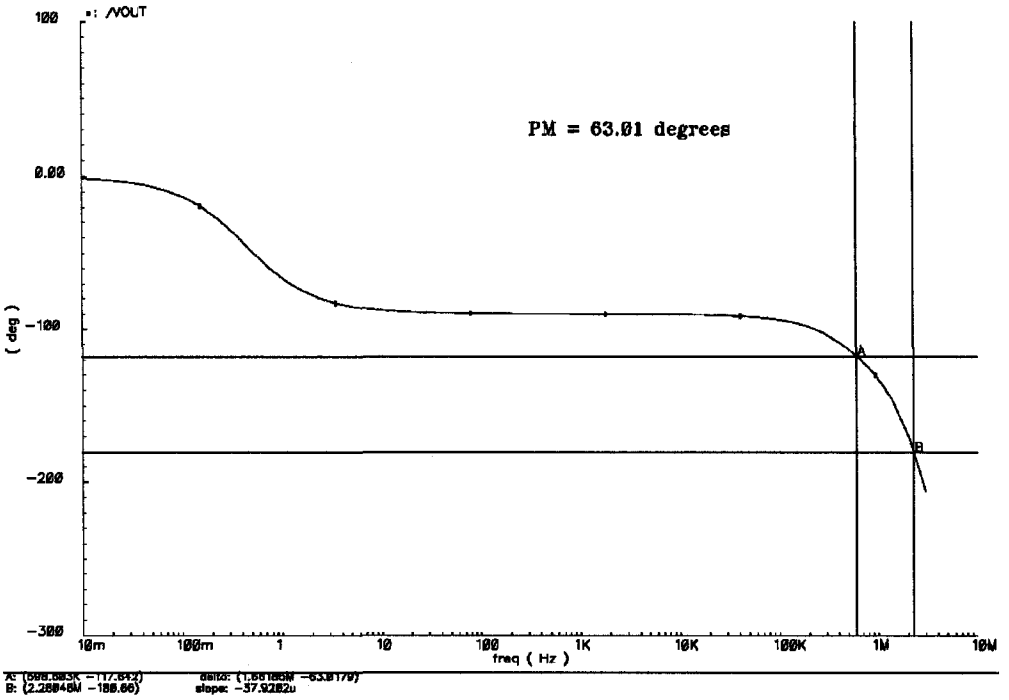


Fig. 3.2: Simulated phase margin of the amplifier at T = 25 ^{0}C for TT process corner

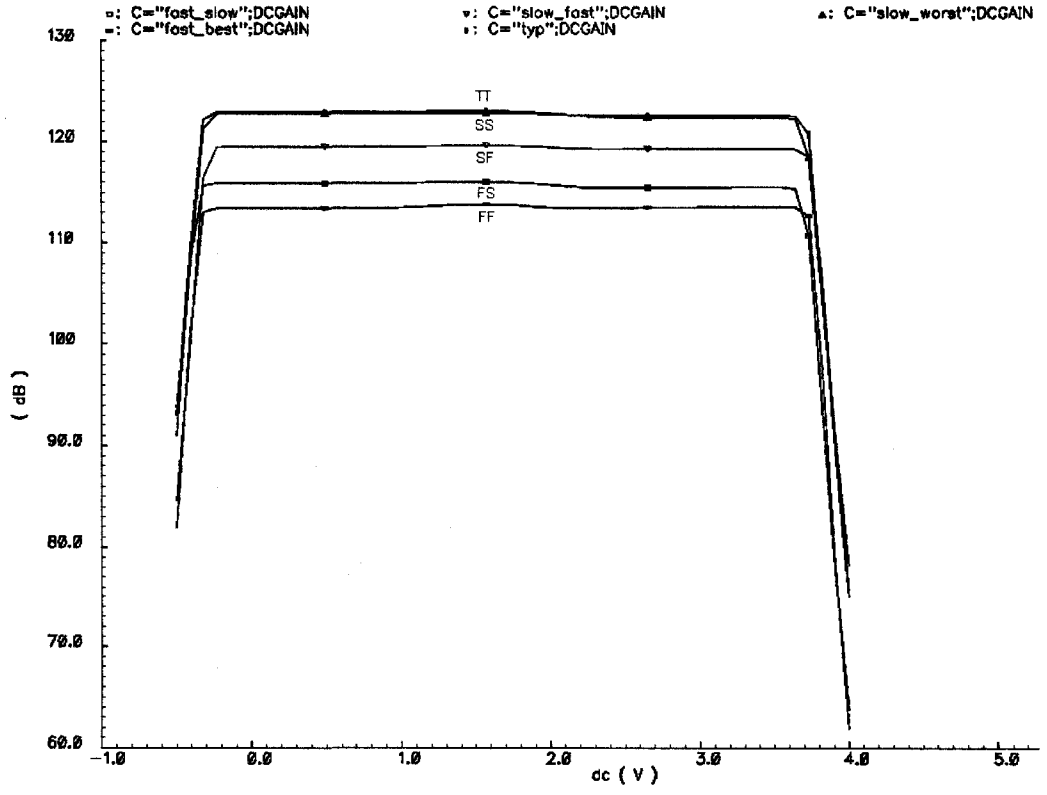


Fig. 3.3: Simulated DC gain at 1 KHz over ICMR (0 V – 3.3 V)

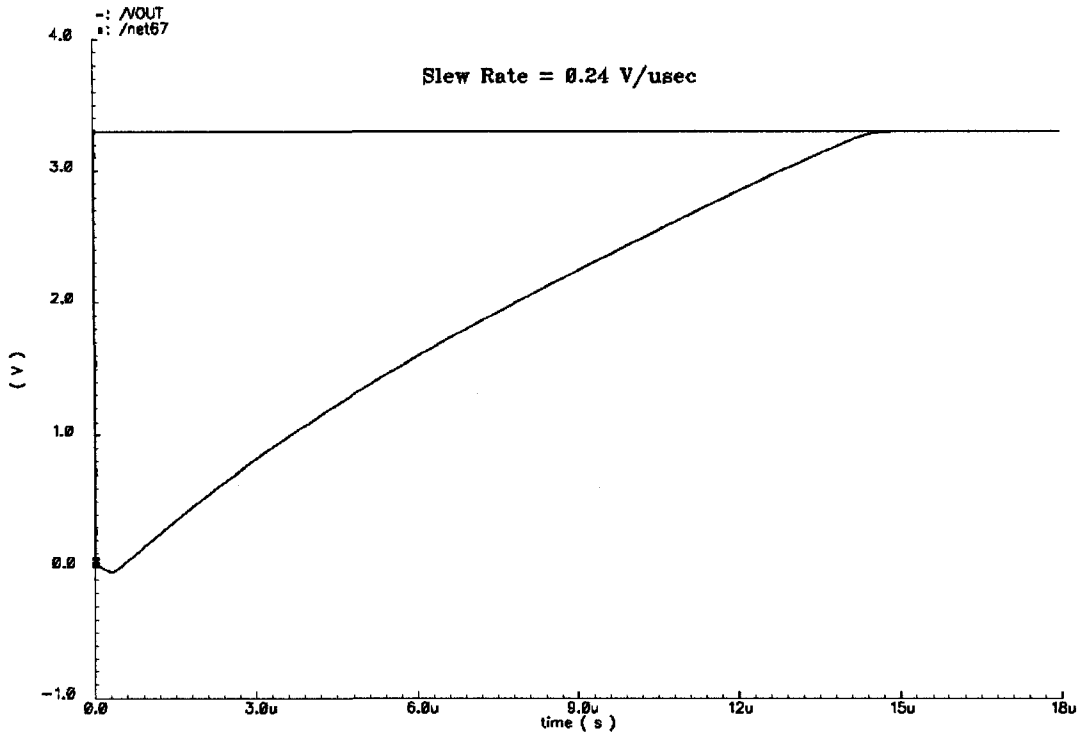


Fig. 3.4: Simulated slew rate of the amplifier at T = 25 ^{0}C for TT process corner

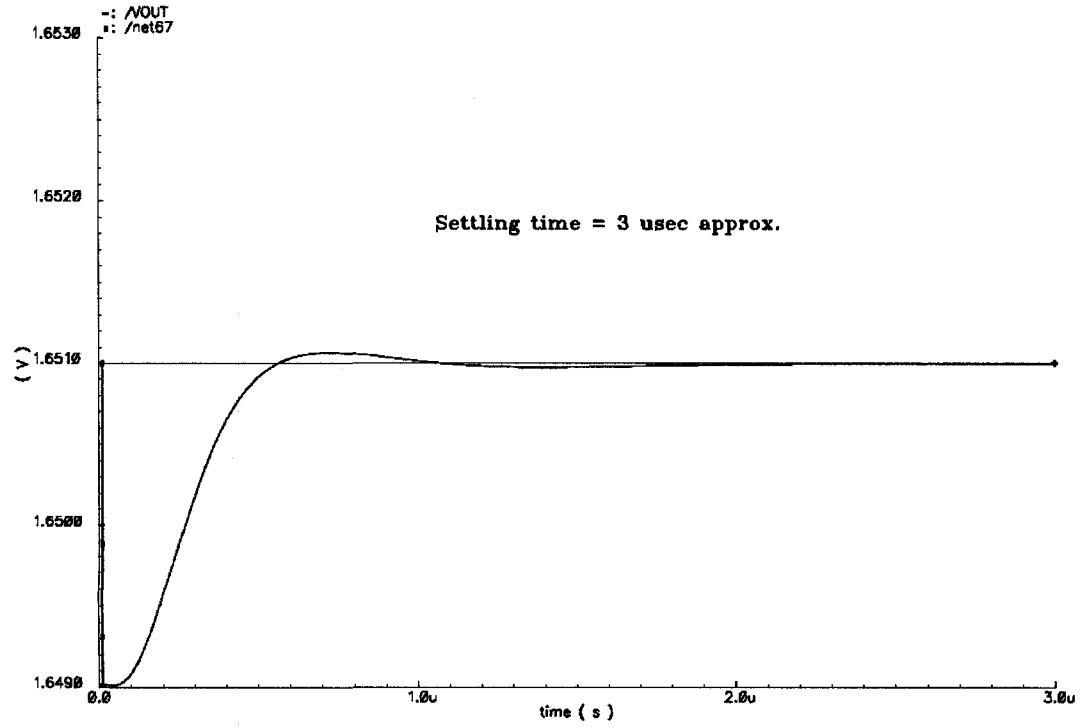


Fig. 3.5: Simulated settling time of the amplifier at T = 25 ^{0}C for TT process corner

The simulated results presented here are summarized in a tabulated format in Table 3.3 along with power and current consumption values. These reported values are for a Typical-Typical (TT) process corner at 25 ^{0}C.

Table 3.3: Parameters of the amplifier at T = 25 ^{0}C for TT process corner simulation

PARAMETER	VALUE
Supply Voltage (V)	3.3
DC Gain (dB)	122.8
Phase Margin (^{0})	63.01
Slew Rate (V/μs)	0.24
Settling Time (μs)	3.0
Total Current Consumed (μA)	180
Power (μW)	594

3.1.1 Simulation Results to Demonstrate Offset Voltage Trimming

The simulation results in this section demonstrate the influence of laser trimming of trimmable load resistors in the input stage of the amplifier on the input offset voltage. The laser trimming of a resistor is modeled as reducing the value of the resistor during simulations. The value of the resistor is reduced to observe its influence on input offset voltage. Based on the analysis presented in Chapter 2, simulation results are presented to support the theoretical analysis for trimming sequence of offset voltage. There are various cases of untrimmed offset voltage versus ICMR. To demonstrate offset voltage trimming, a simulated example is presented for a particular case of offset voltage curve characteristic over ICMR. Though one case is shown here, all other cases of untrimmed offset voltage over ICMR are equally applicable.

To create the offset voltage, the aspect ratios of PMOS and NMOS differential pairs in the input stage are changed by a small amount. The offset voltage is measured by configuring the amplifier in unity-gain set-up. Fig. 3.6 shows a simulated example of an initial untrimmed offset voltage over ICMR. This corresponds to Case 3 from

Fig. 2.8 in Section 2.3 of Chapter 2. The untrimmed offset voltages at different values of common mode voltage are tabulated in Table 3.4.

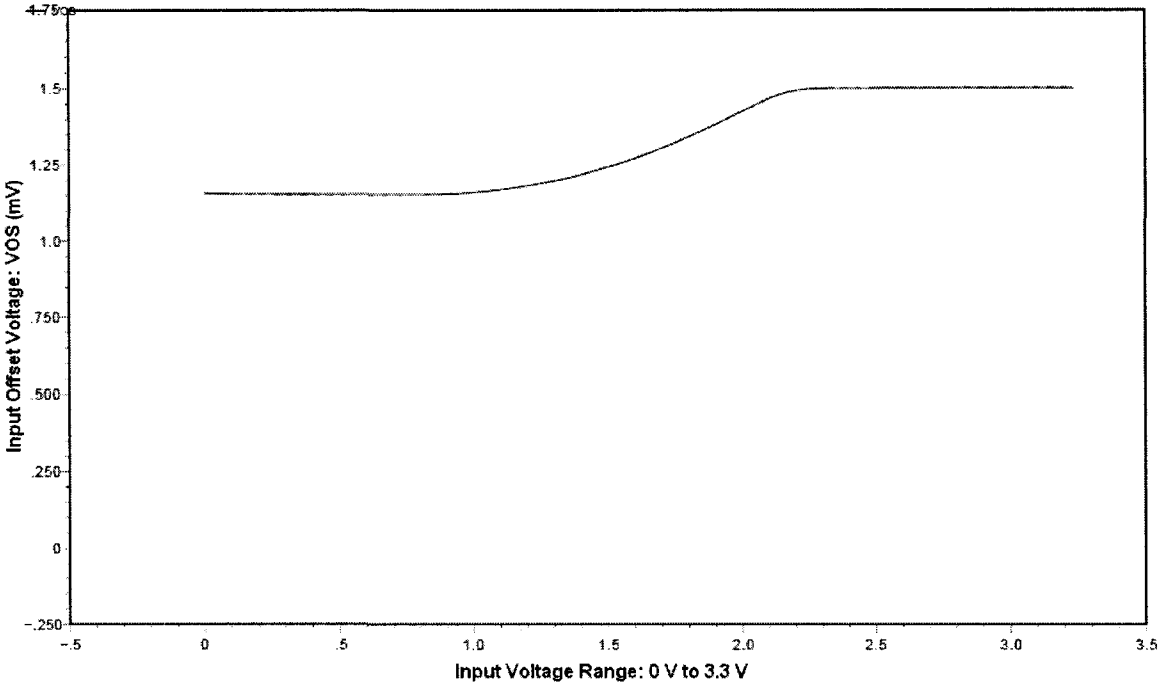


Fig. 3.6: Simulated un-trimmed input offset voltage over ICMR

Table 3.4: Simulated un-trimmed input offset voltage at various DC input voltages

ICMR	UN-TRIMMED OFFSET VOLTAGE (V_{OS})	VALUE (mV)
Low	PMOS Differential Pair ON: $V_{OS\,(P)}$	1.15
Mid-Rail	PMOS & NMOS Differential Pair ON: $V_{OS\,(P)} + V_{OS\,(N)}$	1.28
High	NMOS Differential Pair ON: $V_{OS\,(N)}$	1.51

With reference to Step 1 from the trimming procedure given in Fig. 2.10 and the resistor selection table outlined in Table 2.1, the value of the resistor R8 is reduced to raise $V_{OS(P)}$ close to the value of $V_{OS(N)}$ maintaining only PMOS differential stage turned ON and NMOS differential stage turned OFF i.e. biasing the input stage at lower DC voltage of common mode input range (0.45 V). Simulated plot is shown in Fig.3.7 where two offset voltages from both differential pairs are approximately the same.

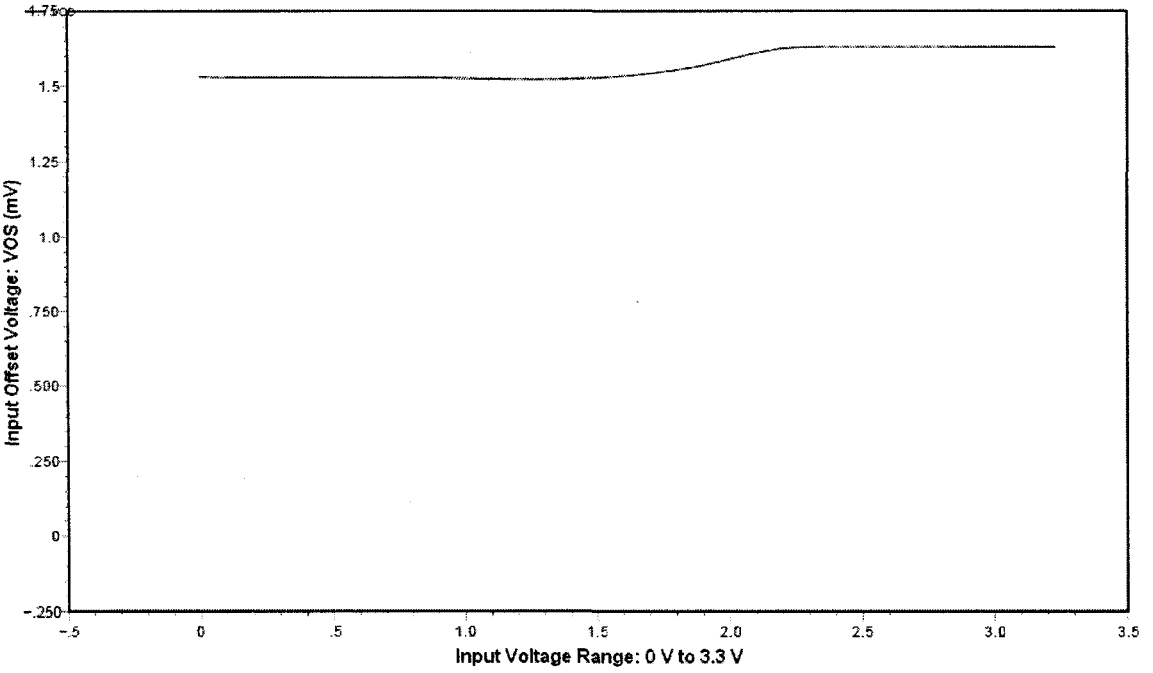


Fig. 3.7: Simulated trimmed input offset voltage over ICMR after Step 1

The results for this trimming step are shown in Table 3.5. The resistor R8 is reduced from 5 KΩ to 4.97 KΩ. The PMOS input offset voltage V_{OSP} is raised to 1.52 mV by reducing the resistance of resistor R8 so as to reduce the difference between $V_{OS\,(P)}$ and $V_{OS\,(N)}$. It is observed from this simulation, that as the value of $V_{OS(P)}$ is raised, the part of the offset voltage contributed when both differential pairs are ON is also raised and a minor increment of $V_{OS\,(N)}$ is observed.

Table 3.5: Simulated results for trimmed input offset voltage after Step 1 of trimming

ICMR	TRIMMED OFFSET VOLTAGE (V_{OS})	VALUE (mV)
Low	PMOS Differential Pair ON: $V_{OS\,(P)}$	1.52
Mid-Rail	PMOS & NMOS Differential Pair ON: $V_{OS\,(P)} + V_{OS\,(N)}$	1.53
High	NMOS Differential Pair ON: $V_{OS\,(N)}$	1.63

After following Step 1, the offset is trimmed as per Step 2 of Fig. 3.10 where the input DC bias voltage is set at mid-rail value of 1.65 V. At this ICMR voltage, both differential pairs contribute to offset voltage. The resistor R2 is reduced from 5 KΩ to 4.82 KΩ to reduce the offset voltage at mid-rail to 60.5 μV. The offset voltages due to each differential pair are also reduced i.e., both $V_{OS(P)}$ and $V_{OS(N)}$ move in the same direction. The results are presented in Table 3.6 and the simulated plot for the trimmed offset voltage is shown in Fig. 3.8. These offset voltage trimming steps were performed at temperature, T = 25 ^{0}C. The issue of offset voltage drift is also addressed since the amplifier is specified to operate over a range of temperature from -40^{0}C to +85^{0}C. The offset voltage drift is measured as average drifts over the specified temperature range to simplify testing and specifications. The drift measurement is usually made at an intermediate point of the temperature range, followed by two end point tests. The two separate drifts are computed and their magnitudes are averaged to define the average offset voltage drift over temperature [15].

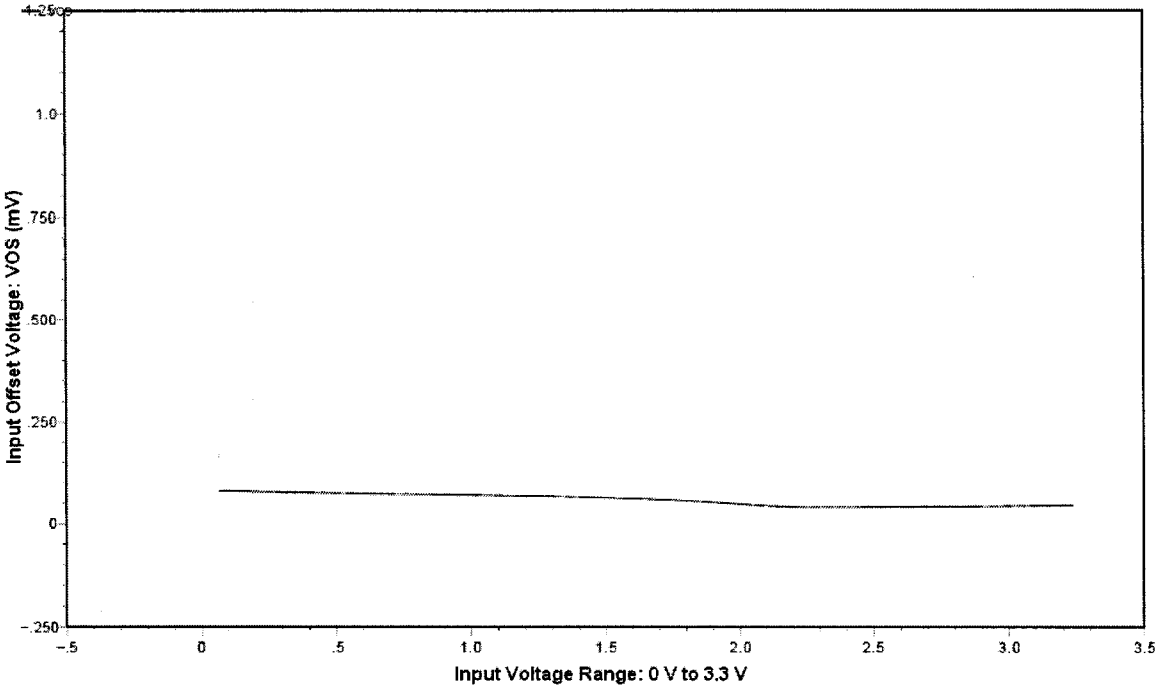


Fig. 3.8: Simulated trimmed input offset voltage over ICMR after Step 2

Table 3.6: Simulated results of trimmed input offset voltage after Step 2 of trimming

ICMR	TRIMMED OFFSET VOLTAGE (V_{OS})	VALUE (μV)
Low	PMOS Differential Pair ON: $V_{OS\,(P)}$	75.3
Mid-Rail	PMOS & NMOS Differential Pair ON: $V_{OS\,(P)} + V_{OS\,(N)}$	60.5
High	NMOS Differential Pair ON: $V_{OS\,(N)}$	42.1

This procedure is performed to avoid averaging two large but opposing drifts over various portions of the specified temperature range. The average of a U-shaped drift curve would be deceptively small if only end points are taken into account. The input offset voltage drift as a function of temperature is represented as

$$\left(\frac{dV_{OS}}{dT}\right)_{AVERAGE} = \frac{\left|V_{OS}(T_1) - V_{OS}(25^0 C)\right| + \left|V_{OS}(T_2) - V_{OS}(25^0 C)\right|}{\left|T_1 - T_2\right|} \qquad (3.1)$$

where the specified operating temperature range for the amplifier is from T_1 = -40 ^{0}C to T_2 = +85 ^{0}C and the intermediate temperature is 25 ^{0}C. The offset voltage drift is usually specified at mid-supply DC value which in this case is 1.65 V for 3.3 V supply.

The R_{BIAS} resistor in the PTAT Bias circuit as shown in Fig. 2.11 in Chapter 2 can be implemented using a poly-silicon or a diffused resistor. A poly-silicon resistor has a negative temperature coefficient and a diffused resistor has positive temperature coefficient as identified in TSMC 0.18 μm CMOS process. The choice of R_{BIAS} resistor film in the PTAT Bias circuit can influence the offset voltage drift over temperature. To demonstrate this issue, drift curves for untrimmed and trimmed input offset voltage are plotted in Fig. 3.9 and Fig. 3.10, respectively. These curves are for the case when the R_{BIAS} resistor in the Bias circuit is implemented using a P+ poly-silicon resistor. This is followed by offset voltage drift curves for the case when a diffused resistor is used in the Bias circuit. The plots for drift curves are shown for untrimmed and trimmed input offset voltage in Fig. 3.11 and Fig. 3.12, respectively. The offset drifts are calculated as per Eq. 1 and summarized in Table 3.7 for two kinds of resistor that can be used to implement the PTAT Bias circuit. It also shows offset voltage drift is reduced when laser trimming is performed. In case of poly-silicon resistor in the bias circuit, drift is reduced from 3.12 μV/ ^{0}C to 1.37 μV/ ^{0}C

and for a diffused resistor in the bias circuit, it is reduced from 3.44 μV/ ^{0}C to 0.99 μV/ ^{0}C.

Table 3.7: Simulated input offset voltage drift values over temperature (- 40^{0}C to + 85^{0}C)

R_{BIAS} Resistor Film	Un-trimmed V_{OS} Drift (μV/ ^{0}C)	Trimmed V_{OS} Drift (μV/ ^{0}C)
Poly-silicon	**3.12**	**1.37**
Diffused	**3.44**	**0.99**

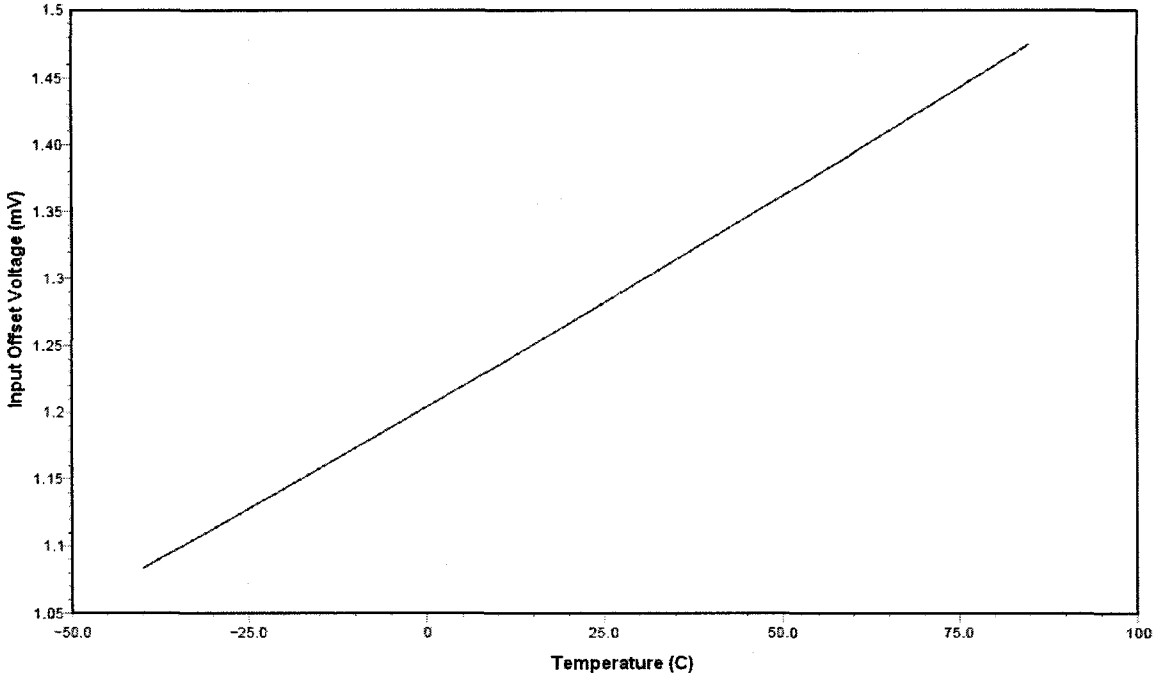


Fig. 3.9: Simulated un-trimmed offset voltage drift curve for R_{BIAS} implemented as P+ poly-resistor

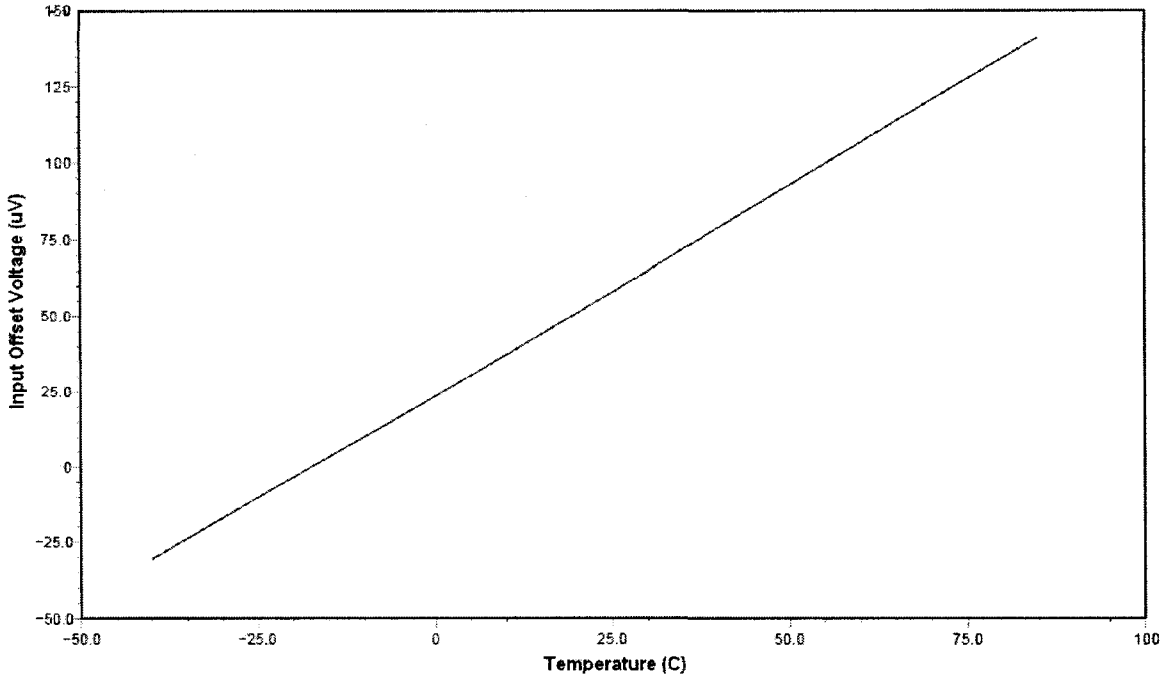


Fig. 3.10: Simulated trimmed offset voltage drift curve for R_{BIAS} implemented as P+ poly-resistor

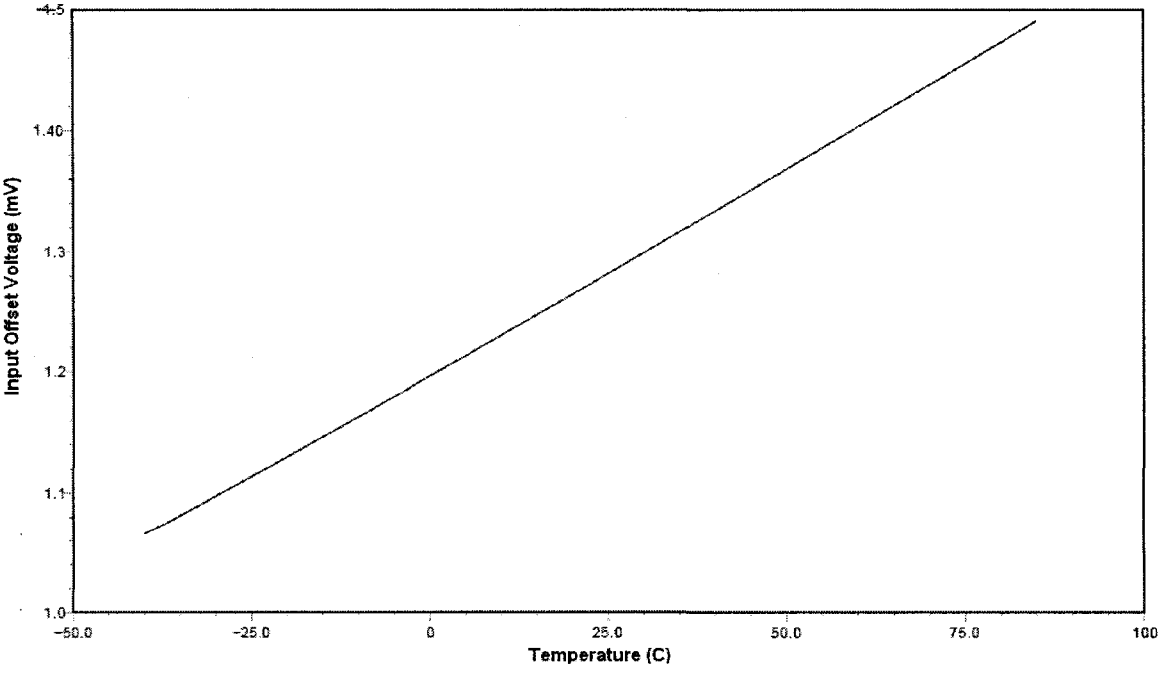


Fig. 3.11: Simulated un-trimmed offset voltage drift curve for R_{BIAS} implemented as diffused resistor

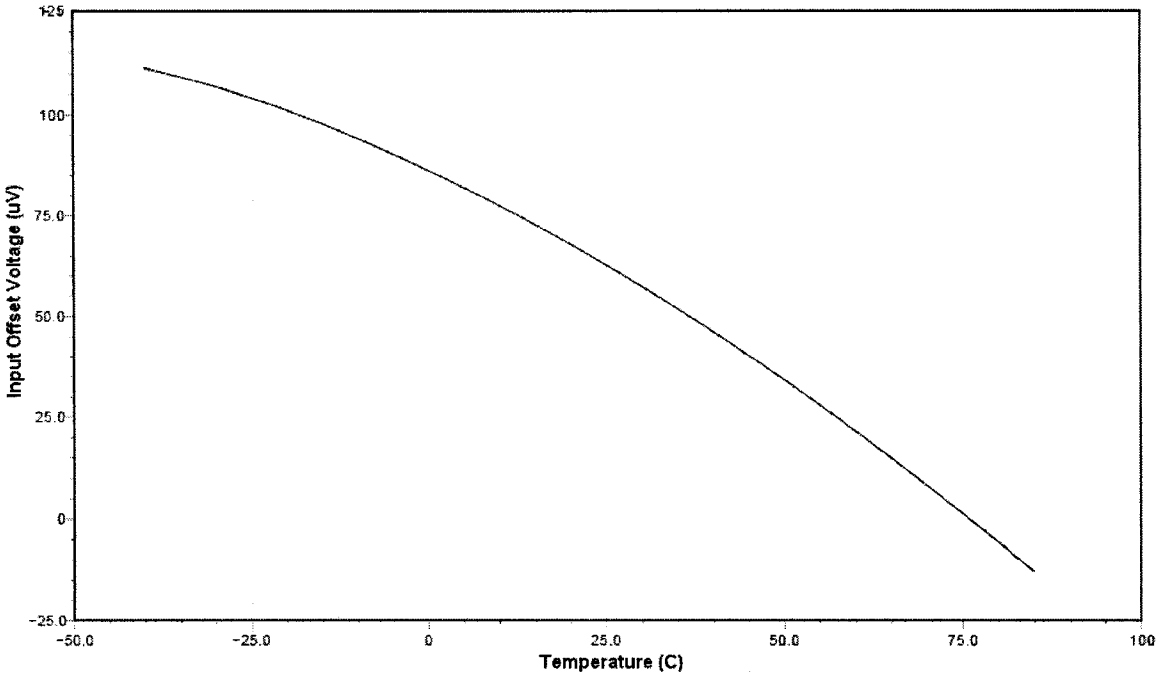


Fig. 3.12: Simulated trimmed offset voltage drift curve for R_{BIAS} implemented as diffused resistor

3.2 Experimental Results

The test-set up used for experimental results involves the rail-to-rail amplifier configured in non-inverting unity gain. This configuration is used to determine the functionality of the amplifier in terms of DC and transient response. For the purpose of the test, the chip was mounted on a Printed Circuit Board (PCB). The instruments utilized are the Agilent E3631A DC Power Supply for bias, supply and ground voltages, the Tektronix TDS754 Digital Oscilloscope for measurement of the amplifier DC and transient response, the Agilent 33250A Arbitrary Function Generator for sine-wave and square-wave generation and the Keithley 2002 Precision Multi-meter for measurement of DC values. The test results show that the expected functionality was achieved for the amplifier. The DC power supply of 3.3 V is used and a discrete capacitor of 470 pF was used as an external load. The measured results are described as follows:

- Fig. 3.13 shows measured DC input sweep response of the amplifier. The non-inverting input of the amplifier was swept from 0 V to 3.264 V shown by curve C1 and the output DC response attained is from 0 V to 3.237 V as shown.
- Fig. 3.14 shows measured sine wave response from the amplifier. A sine-wave of 3.302 V_{P-P} at 1 KHz was applied at the input shown by curve C2 and the output sinusoid response measured is 3.285 V_{P-P} (Curve C1). Fig. 3.9 and Fig. 3.10 demonstrate the rail-to-rail output swing capability at the output of the amplifier with a capacitive load.
- Fig. 3.15 (a) shows measured transient response for a large signal square wave response. A square wave of 3.308 V_{P-P} at 1 KHz is applied at the input shown by curve C2. The output response is slew-rate limited as shown by curve C1. The measured slew rate is 0.22 V / μs approximately. Fig. 3.15 (b) shows enlarged view of the Fig. 3.15(a)
- Fig. 3.16 (a) depicts the measured transient response for a small signal square wave. A square wave of 100 mV_{P-P} at 1 KHz is applied at the input shown by curve C2 while the output response is shown by curve C1. Fig. 3.16 (b) shows an enlarged view of Fig. 3.16 (a). This measurement was performed to determine the stability of the amplifier [30], which shows no ringing in the response of the amplifier.

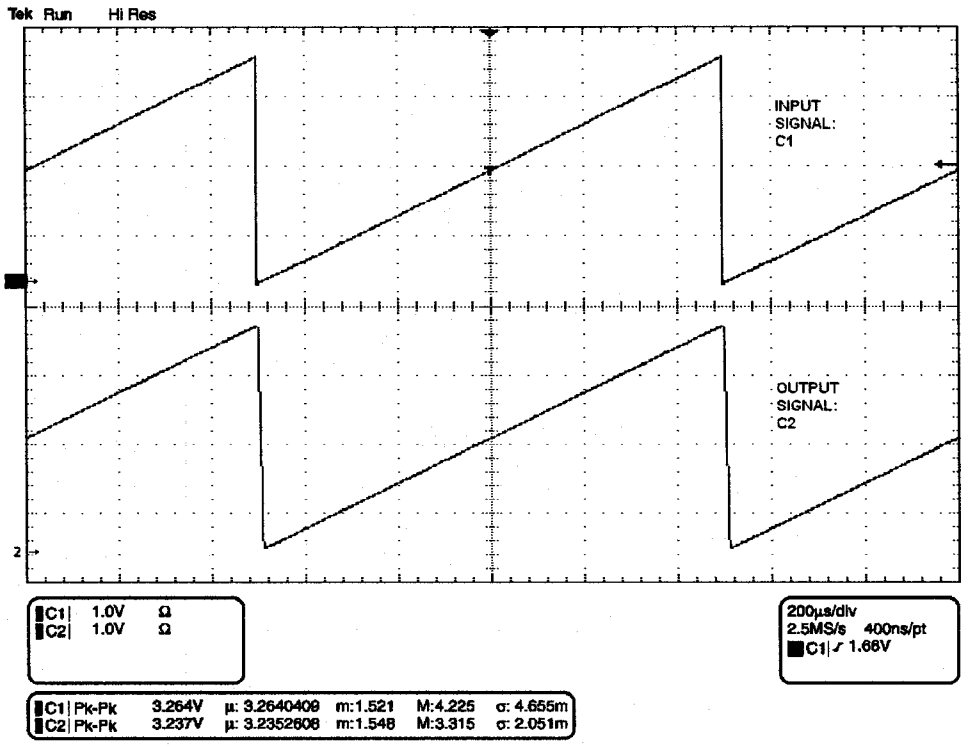


Fig. 3.13: Measured DC transfers characteristics of the input common-mode range

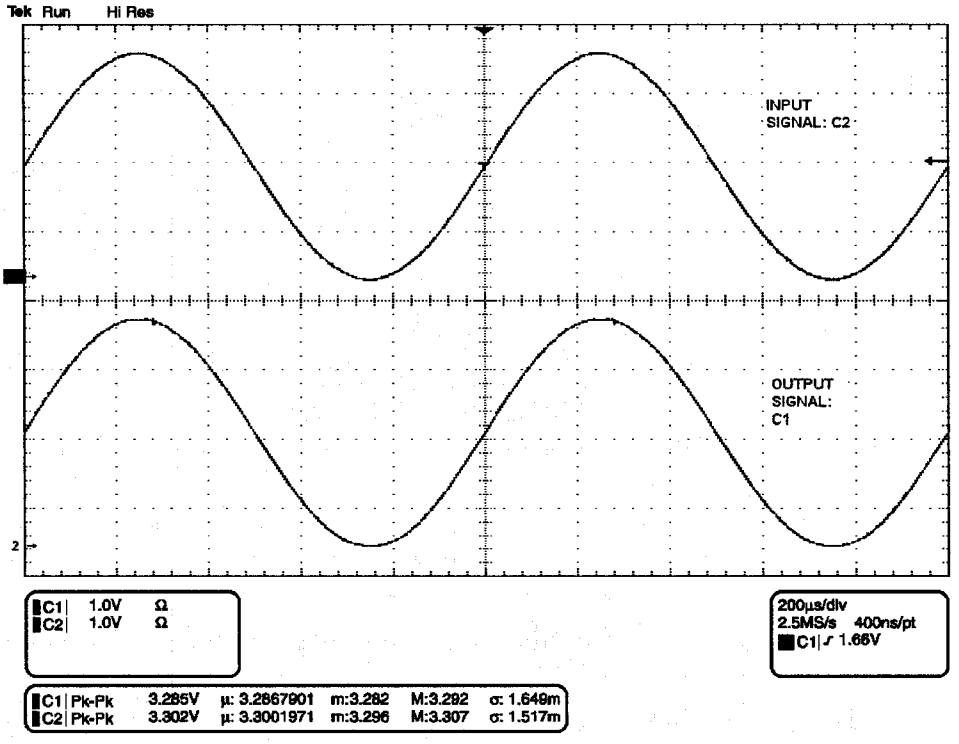
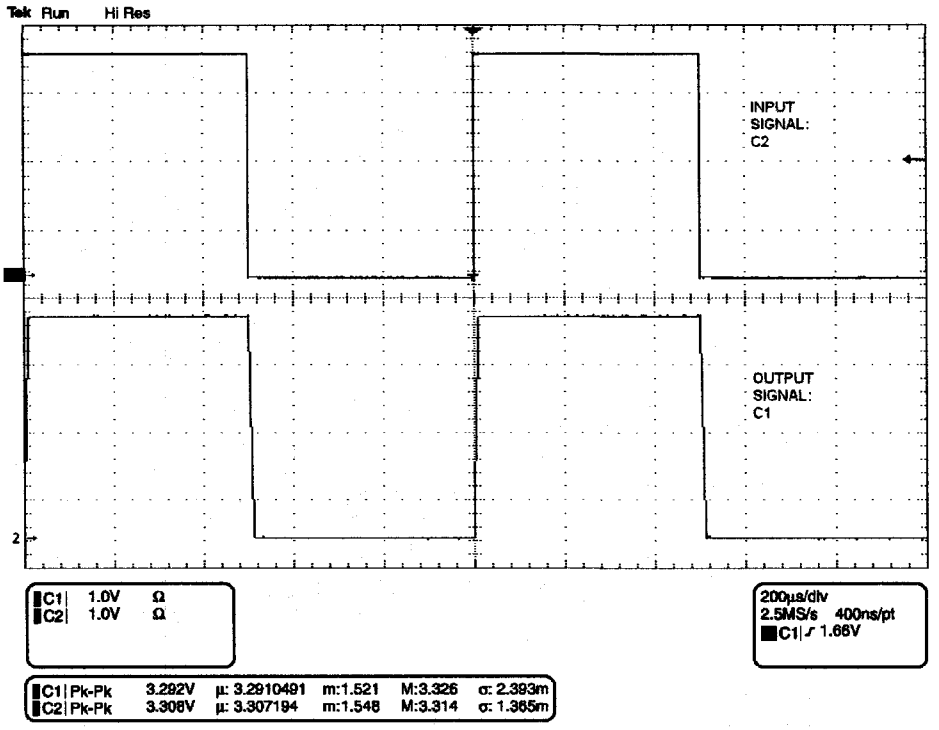
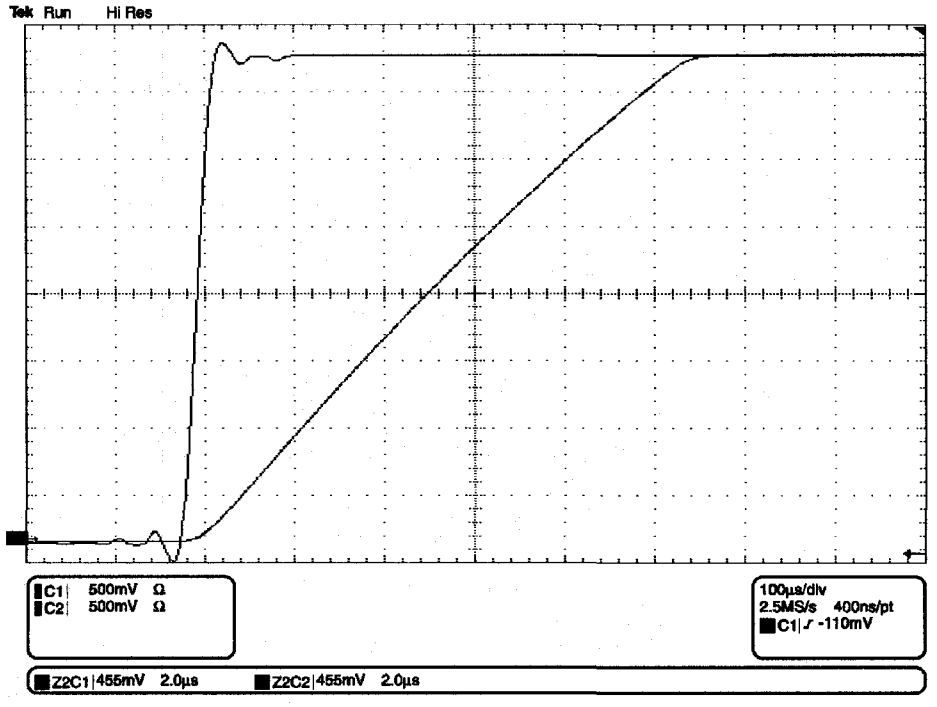


Fig. 3.14: Sine-wave response with input signal amplitude 3.3 V_{P-P} @ 1 KHz

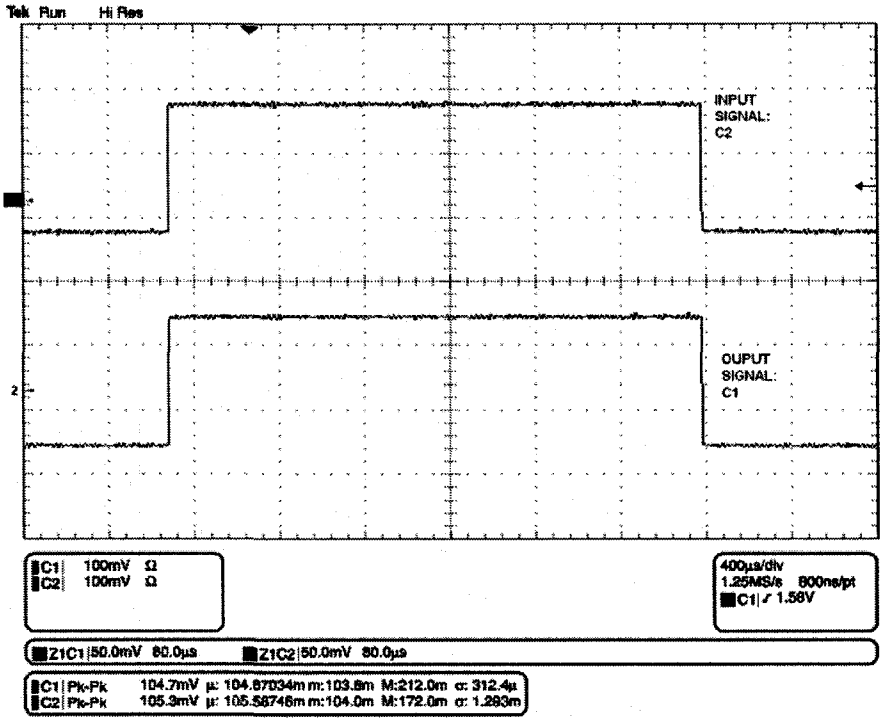


(a)

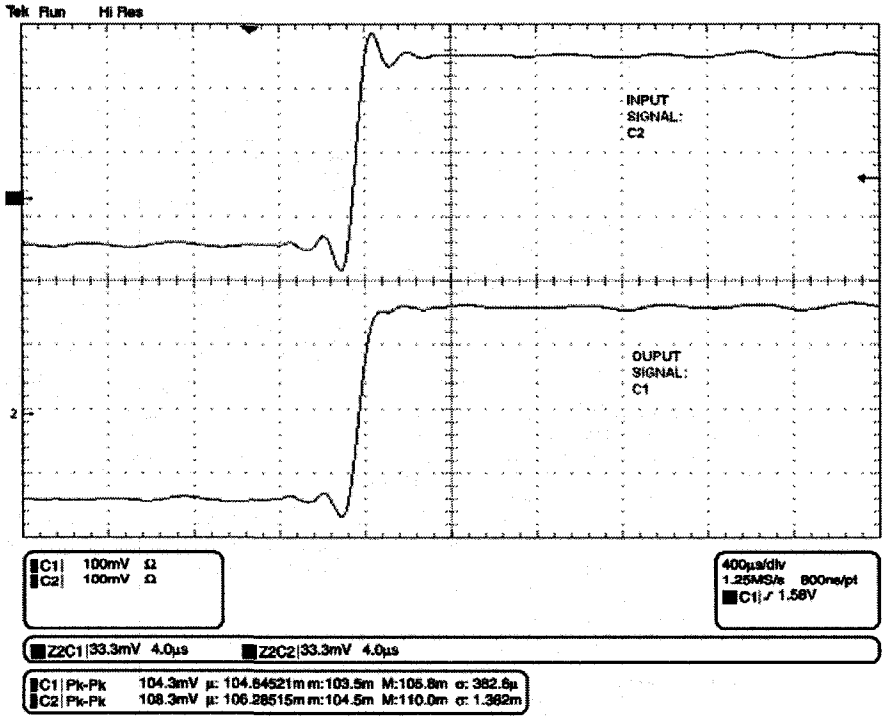


(b)

Fig. 3.15: (a) Measured transient response with large signal input (b) Zoomed-in view



(a)



(b)

Fig. 3.16: (a) Measured transient response with small signal input (b) Zoomed-in view

3. 2.1. Laser Trimming of Poly-Resistors for Offset Voltage Reduction

In this section, experimental results on offset voltage reduction are shown while performing laser trimming of P+ poly resistors as load resistors in the rail-to-rail input amplifier stage. The laser trimming is performed using the Nd-YAG laser. As proposed in Chapter 1, the local heating due to the laser pulse creates a melted spot at the surface of the poly-resistor. At this location on the surface, the crystalline structure of the resistor undergoes a change, which is accompanied by reduction in the value of resistance for the P+ poly-resistor. The trimming of V_{OS} involves iterative steps during which melted spots are created on the surface of the resistor and the resistance value is decreased with each step. The test set-up parameters during experiments with laser used for trimming P+ poly-resistors are tabulated in Table 3.8. These parameters were obtained during experimental optimization process, which creates a stable change in the value of the poly-resistor after trimming.

Table 3.8: Laser equipment set-up values for trimming of P+ poly resistor

Laser power consumed	**0.6 – 0.8 W (Box);** **0.2 – 0.3 W (Chip)**
Laser pulse time-period	**290 – 300 ns**
Time difference between each laser pulse	**96 ns**

In Table 3.8, "Box" represents the power as indicated on the laser controller, which is the total output power of the laser and "Chip" means the power that reaches the test-chip as the laser traverses through the acousto-optic modulator that is about 25%-30% of the total power. The operational amplifier is configured in unity gain set-up for offset voltage measurement and trimming as shown in Fig. 3.17. The Device Under Test (DUT) is the amplifier designed and fabricated for this thesis work. The

amplifier has a load of 473 pF discrete capacitor at its output terminal. The input of the DUT is connected to a Keithley 2400 Source and Measurement Unit designated as Multi-meter A while the output of the DUT is connected to Keithley 2002 Precision Multi-meter. The Multi-meter A is used to generate a voltage ramp sweeping from 0 V to 3.3 V with a specified number of steps and the Multi-meter B is connected to measure the output DC voltage value corresponding to the input value during the sweep process. Both multi-meters are interfaced with a GPIB cable connected to a Central Processing Unit (CPU), which is a desktop PC processing a MATLAB code.

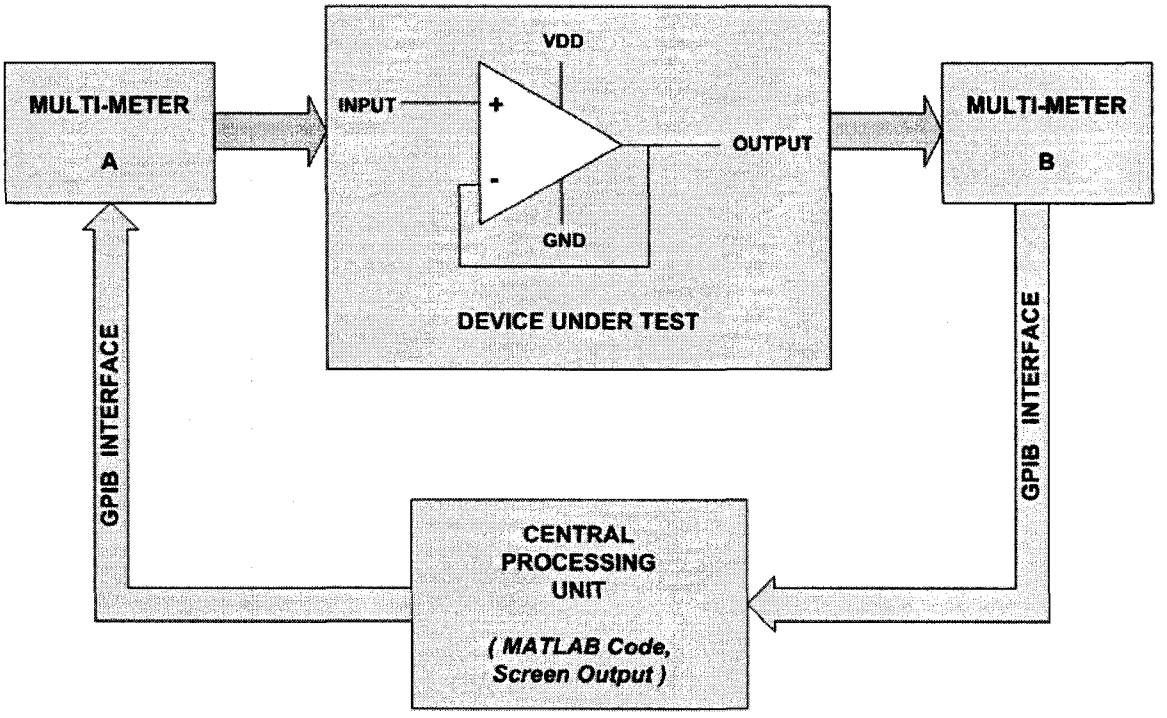


Fig. 3.17: Offset voltage measurement test set-up

The voltage sweep is generated using the MATLAB code where the increment steps are also specified. The code records the OUTPUT terminal voltage of the DUT, V_{OUTPUT} and INPUT terminal voltage of the DUT, V_{INPUT}. The output plot consists of offset voltage, V_{OS} as a function of input voltage sweep, V_{INPUT}. The offset voltage, V_{OS} is defined as a difference of V_{OUTPUT} - V_{INPUT}. The experimental results on offset

voltage trimming are presented for five different samples of the amplifier denoted as OPAMP1, OPAMP2, OPAMP3, OPAMP4 and OPAMP5. For OPAMP1, the values of untrimmed offset voltages at various parts of the common mode are shown in Table 3.9 which were obtained by readings from Multimeter B and verified using MATLAB plot of Fig. 3.18. The un-trimmed offset voltage ranges approximately between -0.18 mV to +0.21 mV over common mode voltage sweep and the curve response corresponds to Case 5 from Fig. 2.9 (e) in Chapter 2.

Table 3.9: Measured un-trimmed input offset voltage at various ICMR values

ICMR	UN-TRIMMED OFFSET VOLTAGE (V_{OS})	VALUE (mV)
Low	**PMOS Differential Pair ON: $V_{OS\,(P)}$**	**-0.178**
Mid-Rail	**PMOS & NMOS Differential Pairs ON: $V_{OS\,(P)} + V_{OS\,(N)}$**	**+0.060**
High	**NMOS Differential Pair ON: $V_{OS\,(N)}$**	**+0.211**

Now using the trimming steps and flowchart described in Chapter 2 and the resistor selection Table 2.1, $V_{OS(P)}$ is trimmed while maintaining the PMOS differential pair in operation at low common mode voltage of 0.45 V. The P+ poly-resistor R8 is trimmed until $V_{OS(P)}$ is approximately equal to $V_{OS(N)}$. The multimeter readings obtained during this phase of trimming are shown in Table 3.10. This completes Step 1 of trimming sequence and its MATLAB result shown in Fig. 3.19 where $V_{OS(P)}$ lies in the same plane as $V_{OS(N)}$.

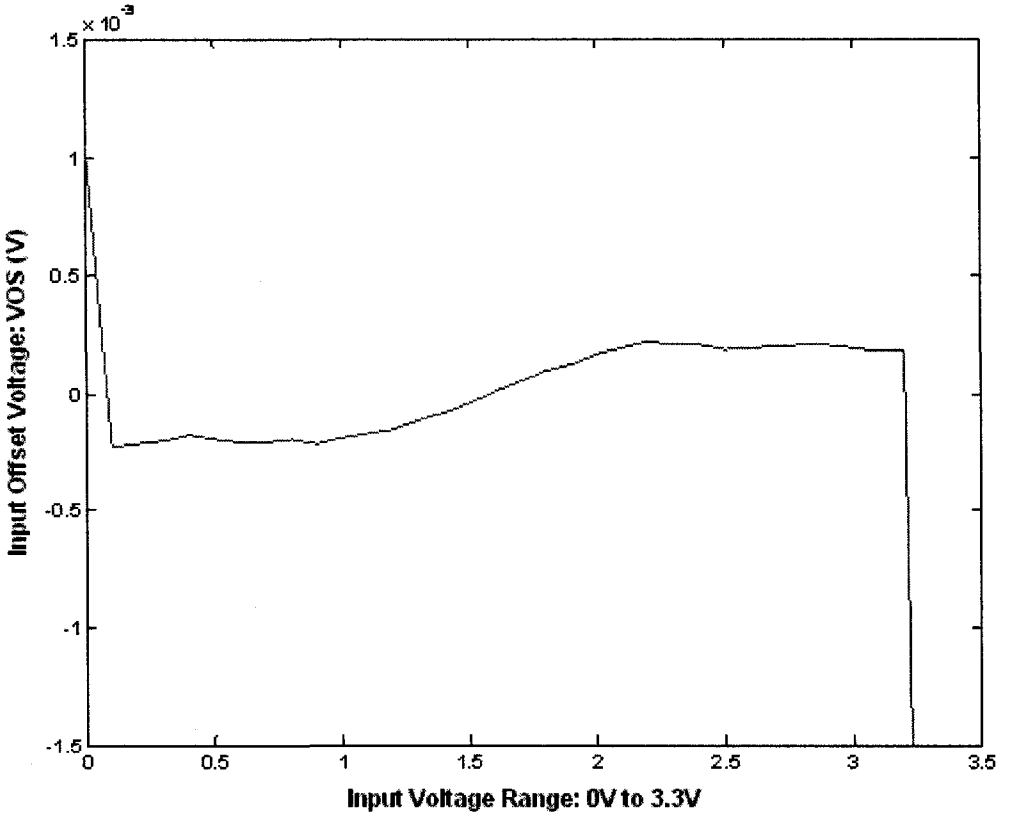


Fig. 3.18: OPAMP1 - Measured un-trimmed input offset voltage over ICMR

Table 3.10: Measured trimmed input offset voltage over ICMR after step1 of trimming

ICMR	UN-TRIMMED OFFSET VOLTAGE (V_{OS})	VALUE (mV)
Low	PMOS Differential Pair ON: $V_{OS\,(P)}$	+0.193
Mid-Rail	PMOS & NMOS Differential Pairs ON: $V_{OS\,(P)} + V_{OS\,(N)}$	+0.205
High	NMOS Differential Pair ON: $V_{OS\,(N)}$	+0.213

Next process is Step 2 of trimming sequence during which R2 is trimmed. The trimmed V_{OS} lies between -25 μV to +50 μV over the common mode voltage range. The measured readings from Multimeter B are presented in Table 3.11 and MATLAB plot result in Fig. 3.20 and a close up view in Fig. 3.21. Further results are presented for more samples of the amplifier. For sample, OPAMP2, Fig. 3.22 shows the un-trimmed offset voltage ranging between +0.1 mV to + 0.5 mV over common mode range. The trimmed offset voltage plot after Step 2 is presented in Fig. 3.23 where the input offset voltage is between -30 μV to +30 μV. The results for only trimmed offset voltage curves are presented for the remaining samples of the amplifier over ICMR. The trimmed V_{OS} for OPAMP3 lies between -40 μV to +40 μV as shown in plot of Fig. 3.24. In case of OPAMP4, it lies between -50 μV to +60 μV as shown in Fig. 3.25 and for OPAMP5, it lies between +80 μV to -20 μV as shown in Fig. 3.26. The measured results for trimmed offset voltage at mid-supply and over ICMR are summarized in Table 3.12 for five samples of the amplifier after Step No. 2 of trimming.

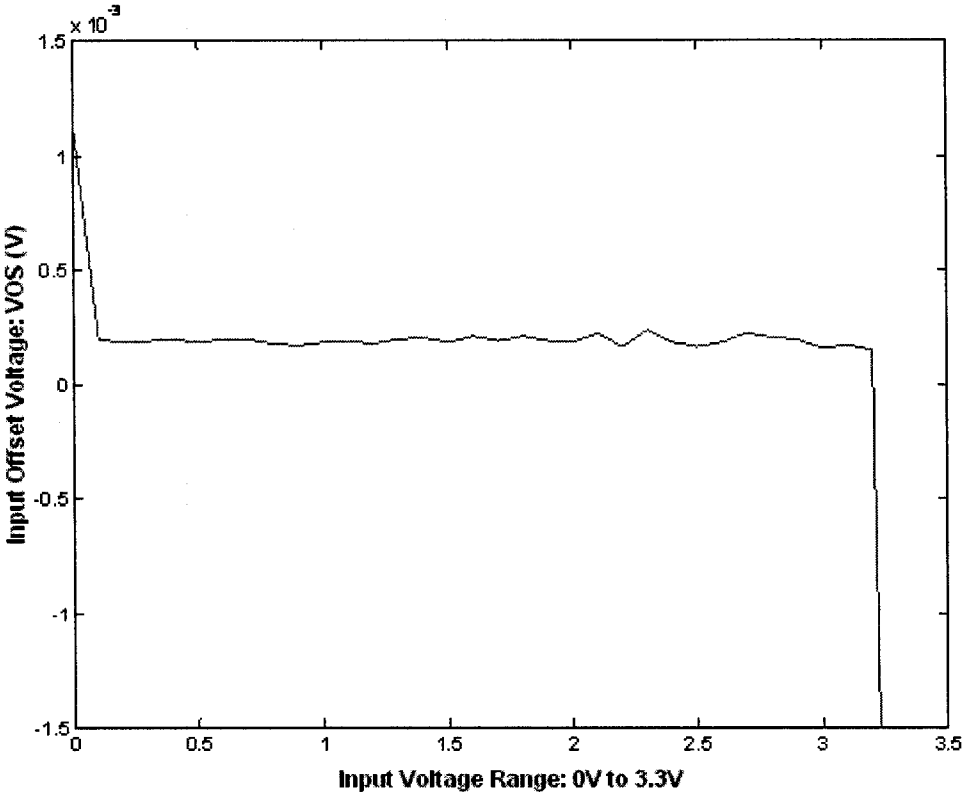


Fig. 3.19: OPAMP1 - Measured trimmed input offset voltage over ICMR after Step 1

Table 3.11: Measured trimmed input offset voltage over ICMR after Step 2 of trimming

ICMR	TRIMMED OFFSET VOLTAGE (V_{OS})	VALUE (μV)
Low	PMOS Differential Pair ON: $V_{OS\,(P)}$	-15.95
Mid-Rail	PMOS & NMOS Differential Pairs ON: $V_{OS\,(P)} + V_{OS\,(N)}$	+17.0
High	NMOS Differential Pair ON: $V_{OS\,(N)}$	+43.6

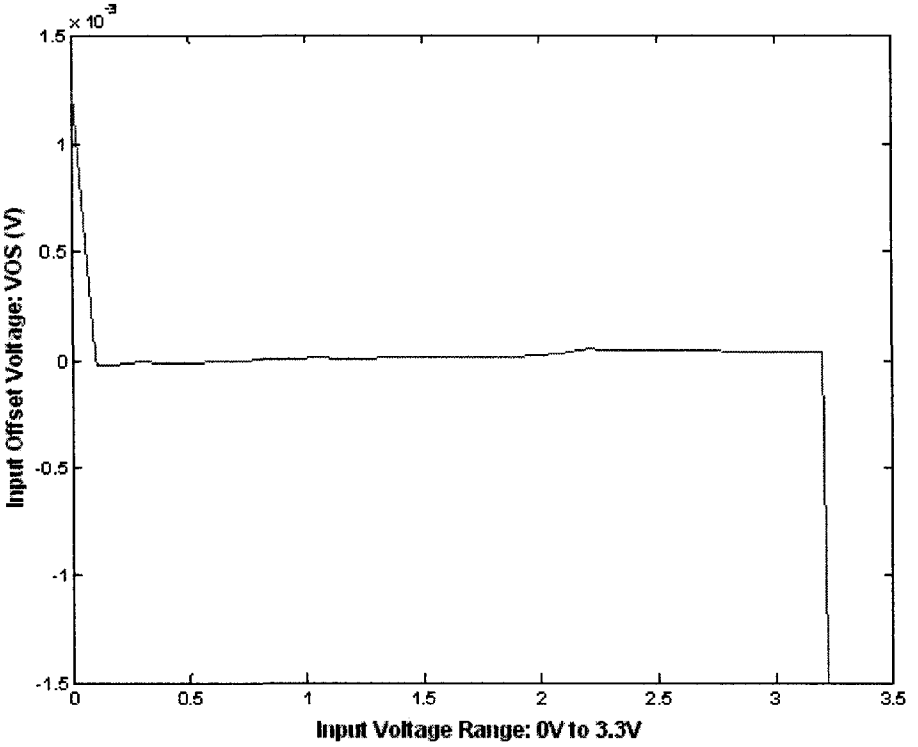


Fig. 3.20: OPAMP1 - Measured trimmed input offset voltage over ICMR after Step 2

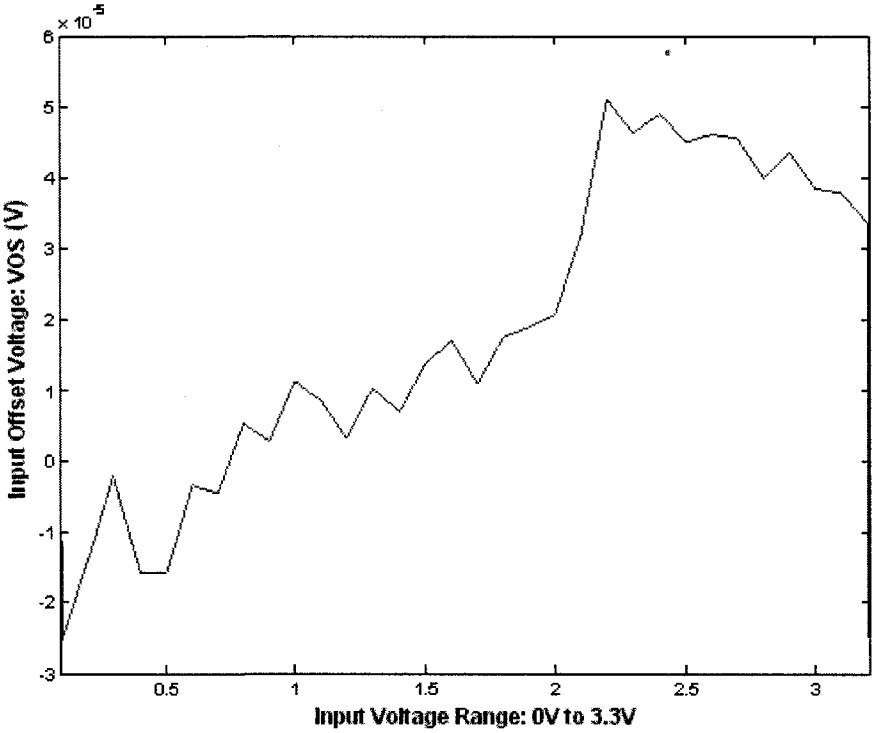


Fig. 3.21: OPAMP1- Zoomed-in view of Fig. 3.20

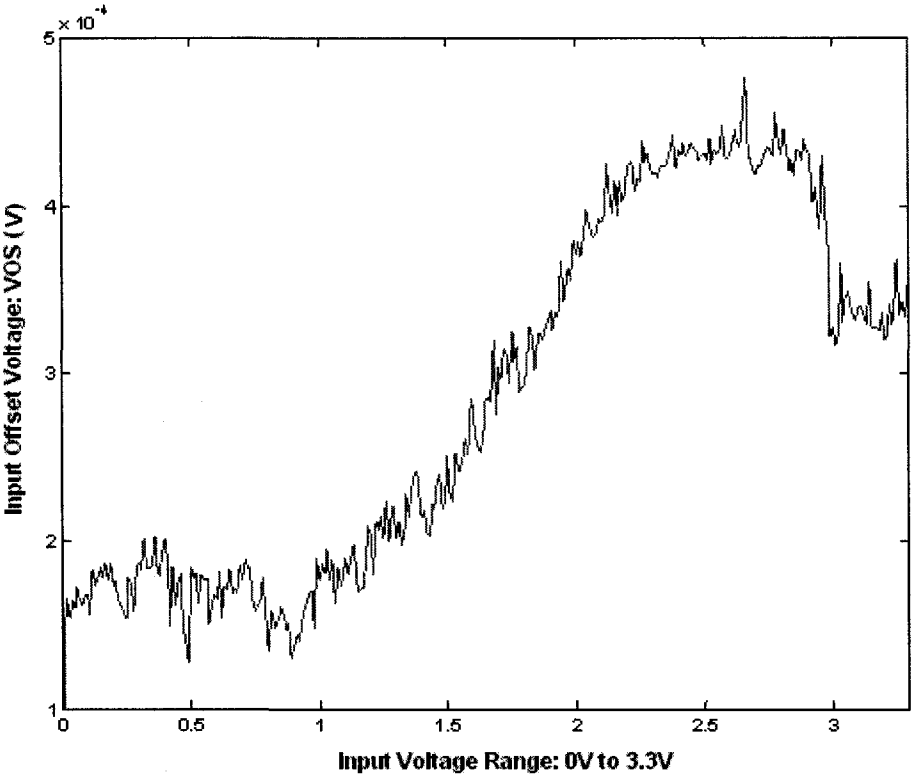


Fig. 3.22: OPAMP2 – Measured un-trimmed input offset voltage over ICMR

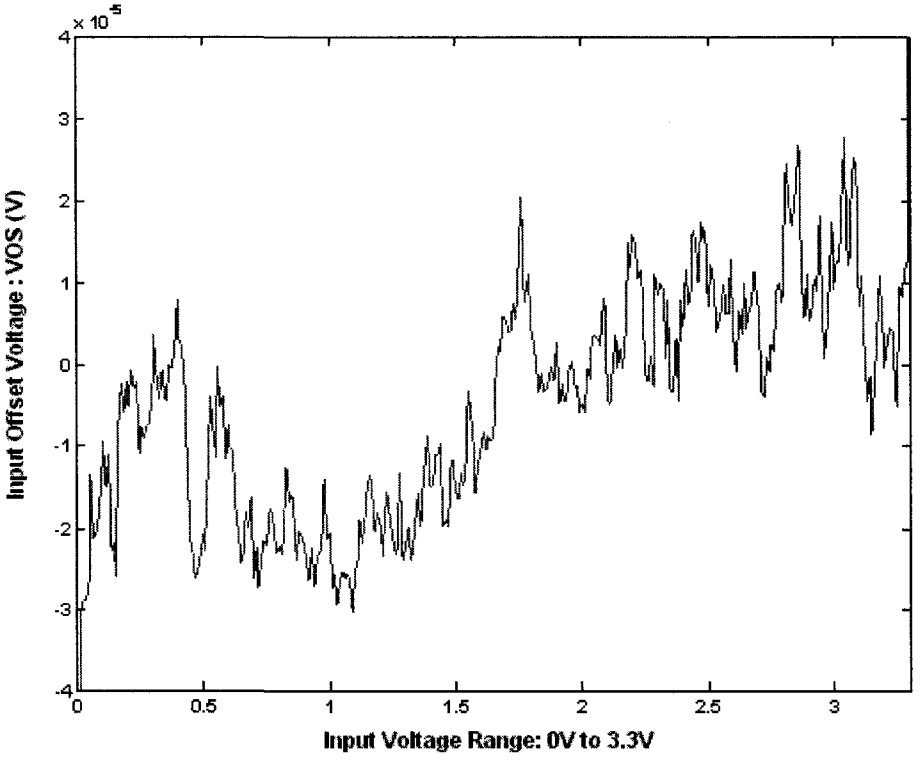


Fig. 3.23: OPAMP2 – Measured trimmed input offset voltage over ICMR after Step 2

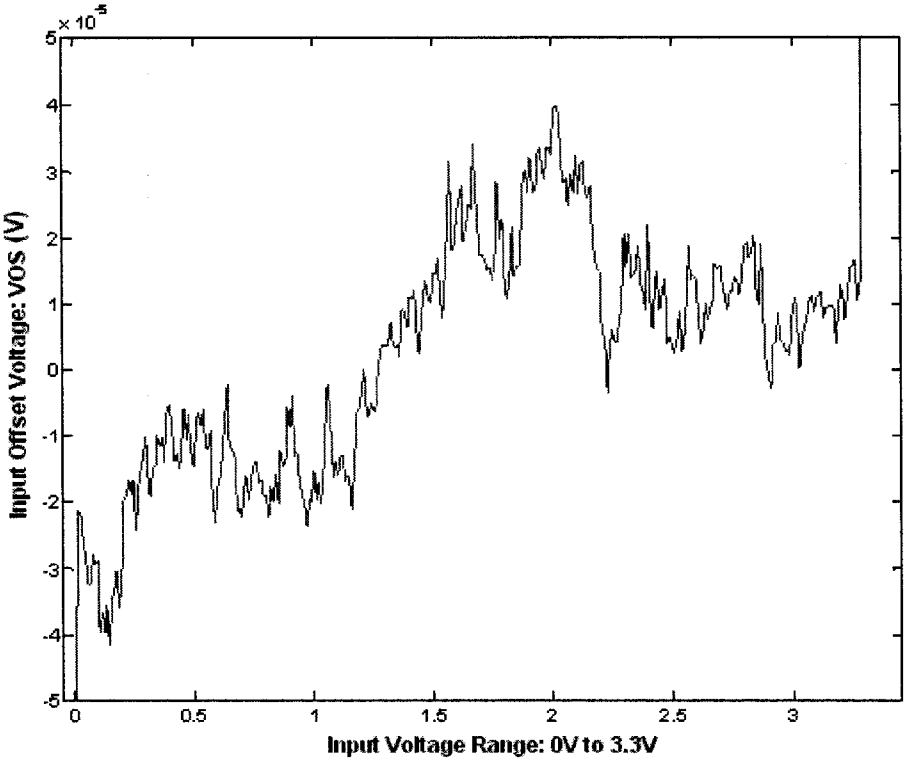


Fig. 3.24: OPAMP3 - Measured trimmed input offset voltage over ICMR after Step 2

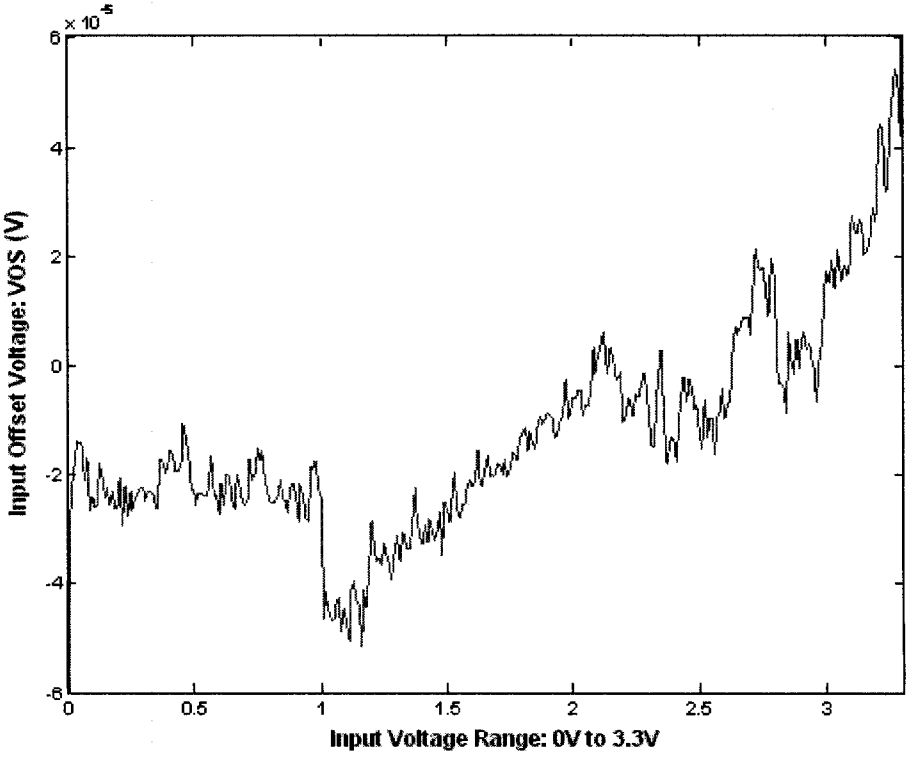


Fig. 3.25: OPAMP4 - Measured trimmed input offset voltage over ICMR after Step 2

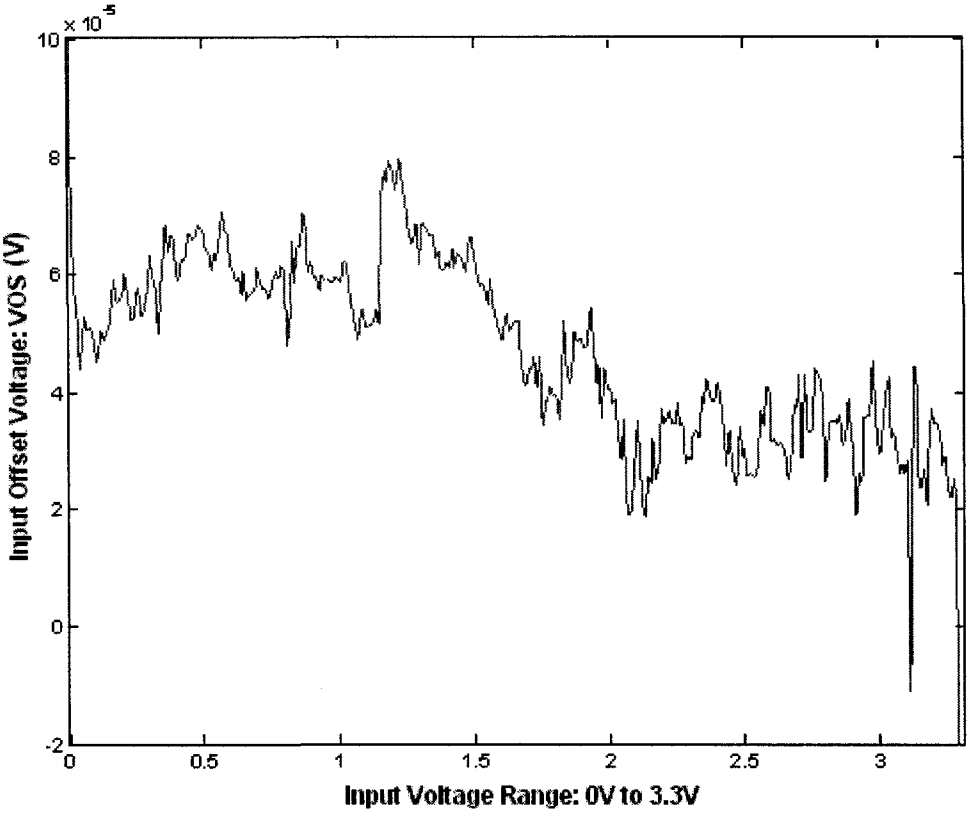


Fig. 3.26: OPAMP5- Measured trimmed input offset voltage over ICMR after Step 2

Table 3.12: Measured results for trimmed input offset voltage at mid-supply and over ICMR for 5 samples of amplifier

SAMPLE	TRIMMED V_{OS} (μV) @ MID-SUPPLY (1.65 V)	TRIMMED V_{OS} (μV) OVER ICMR (0 – 3.3 V)
OPAMP1	+17	-25 to +50
OPAMP2	-15	-30 to +30
OPAMP3	+25	-40 to +40
OPAMP4	-20	-50 to +60
OPAMP5	+50	+80 to -20

CHAPTER 4
Conclusion and Future Work

This chapter summarizes this dissertation and gives an insight into future work that can be performed associated with this thesis.

4.1 Thesis Summary

This thesis demonstrates a method to trim poly-silicon resistors available in standard CMOS processes and its application to precision analog ICs. A three-stage operational amplifier topology has been designed which has laser trimmable poly-silicon resistors. These resistors form a part of the circuit as load elements. A PTAT bias circuit has also been designed to generate DC bias points for the amplifier. The complete circuit was implemented at silicon level. The mathematical analysis developed for offset trimming sequence for a CMOS rail-to-rail amplifier input stage has been successfully implemented. The offset voltage trimming steps during experimental phase show a good correspondence to the theoretical and simulations analysis for offset trimming. Though trimmed rail-to-rail amplifiers are available in the market, yet a comprehensive mathematical analysis describing the offset voltage trimming methodology for a rail-to-rail CMOS differential amplifier is not published in the literature. This thesis work intends to bridge this gap and it is learned that trimming a rail-to-rail differential input stage is an altogether different method from a simple differential input stage, as it requires a careful selection of load elements that can be trimmed. To facilitate the trimming sequence, possible offset voltage curve cases have been identified and provided along with a resistor selection table. The offset voltage trimming over ICMR is performed in two steps. During the first step of trimming sequence, it is identified that the offset voltage of the PMOS differential pair is 3 times more sensitive compared to the offset voltage of the NMOS pair. Therefore, trimming the lower pair of trimmable load resistors is performed such that it affects the change in the offset voltage of the PMOS differential pair. This is the

key aspect of trimming sequence during which the offset voltage of the PMOS input pair is trimmed so that it becomes equal to the NMOS pair offset voltage. This is followed by the second step of trimming during which the upper trimmable load resistors tend to have the same impact on offset voltages of PMOS and NMOS input pairs. In addition to developing an input offset voltage trimming methodology for CMOS rail-to-rail amplifiers, this thesis work also demonstrated the ability to trim poly-silicon resistors available in standard CMOS processes by local heating at the surface of the resistor using a laser pulse.

The closed loop configuration results during the experimental phase have shown a successful silicon level implementation of the amplifier. The measured input DC sweep and sine wave response show a rail-to-rail input and output signal processing capability of the amplifier. The large signal response of the amplifier demonstrates the slewing capability and the small signal response has shown no ringing behavior indicating the amplifier is stable in closed-loop configuration. The device matching issues were addressed both at circuit and layout level. This was important to have an untrimmed offset voltage as low as possible before any trimming of offset voltage can be applied. A large untrimmed offset voltage can influence the size of the resistors to be trimmed for reducing offset voltage. The method of laser trimming presented in the thesis creates melted spots where the surface of the resistor undergoes a change in its crystalline structure. This method causes a decrease in the value of the resistance. So, in case of a large untrimmed offset voltage, it will require larger surface area to create multiple spots in an iterative manner to attain the target value of trimmed offset voltage. The analog circuit and layout design skills used during the design phase have resulted in less than 1 mV untrimmed offset voltage over the ICMR as measured during testing period for all the samples. The reduction of input offset voltage of the amplifier has been experimentally demonstrated using laser trimming of poly-silicon resistors, which is in correspondence with theoretical, and simulation analysis. There is no additional circuitry needed for offset trimming. As observed from experimental results, the

method of trimming poly-silicon resistors utilized during this work is completely compatible with standard CMOS processes. There were no additional masks used during the manufacturing process to implement such method of laser trimming. The results obtained for trimmed offset voltage shows that the trimmed offset voltage is less than 30 μV at mid-supply for 5 trimmed amplifier samples. Among all five amplifier sample, input offset voltages were trimmed to be less that 110 μV over the ICMR from 0 V to 3.3 V.

The trimmed offset voltage for the samples of the amplifier showed almost negligible drift over the ICMR when tested after a period of 6 months. Such experiments were performed to determine the stability of trimmed resistors and its influence on input offset voltage. Most of the experimental efforts done during this work were directed towards trimming the offset voltage of the amplifier. However, experiments are needed to determine open loop DC gain of the amplifier and unity gain-bandwidth. To observe the influence of trimming on the CMRR, it should be measured before and after trimming to determine its improvement. Also, the Total Harmonic Distortion (THD) measurement will be useful to further characterize the amplifier. One of the most important parameters remaining to be measured is offset voltage drift over a specified temperature range. This will further allow this work to draw comparisons with reported low offset, low drift precision CMOS amplifiers using different methods of trimming techniques.

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APPENDIX

Singh, R.; Audet, Y.; Gagnon, Y.; Savaria, Y.; "Integrated Circuit Trimming Technique for Offset Reduction in a Precision CMOS Amplifier," Published in IEEE International Symposium on Circuits And Systems (ISCAS), May 2007

Integrated Circuit Trimming Technique for Offset Reduction in a Precision CMOS Amplifier

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Abstract—**This article presents an application of a recently reported IC trimming technique using laser diffused resistors to reduce the input referred offset voltage of a precision amplifier. A three stage precision CMOS operational amplifier topology is proposed utilizing laser-trimmable diffused resistors for post-fabrication trimming. The amplifier is designed to operate over an industrial temperature range (-40°C to +85°C) including process corners and utilizes an on-chip CMOS bias generation circuit to maintain a robust performance. The results of post-layout simulation of the complete circuit are summarized. The effects of the trimming technique on the input offset voltage of the amplifier are described. The circuit is designed using the TSMC 0.18µm CMOS process and operates from a single supply of 3.3 V.**

I. INTRODUCTION

Precision amplifiers find many applications in sensor based systems utilized for industrial control and instrumentation devices where a high degree of accuracy is needed. An important parameter of a precision amplifier is the input referred offset voltage which determines its DC accuracy. Device mismatch and package induced stress have an effect on the input offset voltage, and temperature changes in the surrounding environment influence the associated drift of offset voltage. These factors tend to limit the DC accuracy and dynamic range of an amplifier utilized for high precision applications. To overcome this performance issue, most commercial precision amplifiers exploit an IC trimming technique which can lower the initial input offset voltage. Continuous-time laser trimming of resistors at wafer level is one such IC trimming method which is used for offset reduction in precision amplifiers.

In the following sections, an application of a new laser trimmable diffused resistor [1] is discussed. The article proposes an architecture of a three-stage precision rail-to-rail CMOS amplifier with a high DC gain. It exploits laser-trimmable diffused resistors for reduction of input referred offset voltage of the amplifier. The laser diffused resistor is completely compatible with standard CMOS fabrication steps and does not require any specialized processing.

The trimmable structure consists of two highly-doped p-type (or n- type) regions separated by a gap of n-type (or p-type). It can be considered as a gateless MOSFET where two highly-doped regions are analogous to the source and drain regions and the channel forms the gap region. The accuracy of this resistor can be precisely controlled by applying a laser pulse on the gap region which leads to melting of silicon substrate and results in diffusion of dopants from the two highly-doped regions. The description of the proposed amplifier topology is presented in section II followed by the results of post-layout simulation in section III. Simulation of the trimming effect of diffused resistors for offset reduction is shown in section IV.

II. PROPOSED AMPLIFIER ARCHITECTURE

The amplifier design is restricted to three amplifying stages in order to limit the complexity in stabilizing a higher number of stages, while simultaneously achieving high open loop DC gain. The amplification stages were designed to offer a DC gain of approximately 100 V/V per stage. For low drift, it is imperative to have reduced variability of circuit characteristics over process and temperature changes. With this issue in consideration, a CMOS bias generator was designed to reduce the variations of the circuit parameters over an industrial temperature range of -40°C to +85° C.

For a general multiple stage amplifier design, it is usually the input stage that is the main source of input offset voltage [2]. In this context, the input of the first stage is critical for precision design. All critically matched devices including those in the amplifier and the bias generator are designed with state-of-the-art layout matching techniques applied to transistors and resistors [3]. Large area devices have been designed to minimize device parameter variations. Critically matched transistors of the input differential stage are placed on the die's central axis where low stress gradients occur in order to minimize sensitivity to die stress [4].

The details of the proposed topology of a three-stage operational amplifier are shown in Fig. 1. The amplifier consists of a rail-to-rail input stage formed with transistors M23 to M34 and resistors R2 to R7 acting as load.

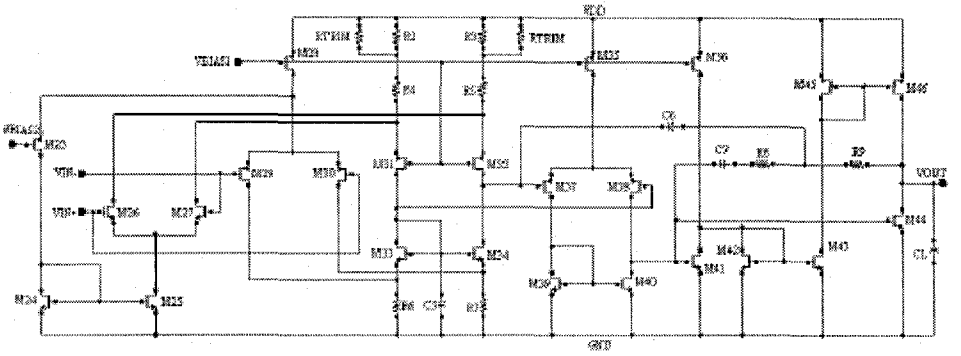

Figure 1. Schematic of the proposed three stage trimmable precision amplifier.

For a folded cascode complementary input stage, in order to minimize distortion, it is important to keep the overall gain of the first stage or transconductance, g_m, of the input pair constant over the complete common mode input voltage range. This is achieved by operating the MOS input pair in the sub-threshold region, where the g_m is proportional to the drain current [5]. The g_m control for the input stage is governed by a current source M28, a current switch M23 and a current mirror M24-M25 [5]. The input stage also incorporates the laser trimmable diffused resistors, R_{TRIM}, for the purpose of reducing the offset voltage of the amplifier. The second amplifying stage consists of a simple differential pair amplifier formed by M35 and M37 to M40. This is followed by a complementary output stage [6] which consists of M36 and M41 to M46 that can drive a large capacitive load. The complete amplifier is stabilized by using the Nested-Miller compensation technique proposed in [7]. The capacitors C6 and C7 and resistors R8 and R9 form the internal compensation network. C5 is used to roll-off the gain of the first stage in order to avoid any zero that could affect the performance of the amplifier in the frequency band of interest.

A CMOS Proportional-To-Absolute-Temperature (PTAT) bias circuit for the amplifier is shown in Fig. 2, where M11 to M22 forms the biasing core which is a variant of the topology described in [8]. The operation of this circuit is based on the principle that a current is generated due to the difference in V_{GS} of M19 and M20 that develops across the resistor R1. This is achieved by designing Width/Length (W/L) ratio of M19 larger than that of M20. In this case, the ratio for M19 is two times the ratio of M20 and both transistors operate in sub-threshold region. These conditions, coupled with the wide swing current mirror M11-M15, produce a current flowing through R1 which is a function of temperature only and independent of supply voltage variation. However, the biasing current value is also bound to shift over process parameter variations. In order to maintain a single operating state for the biasing core, a start-up circuit is implemented with transistors M1 to M10. V1 and V2 are external supply voltages applied to keep the start-up circuit in operation. The circuit has two biasing voltages, VBIAS1 and VBIAS2. Fig. 3 shows the layout of the prototype chip with amplifier and bias circuit submitted for fabrication.

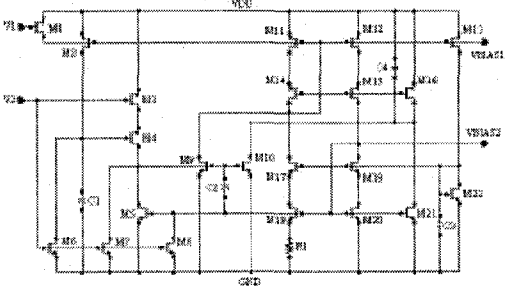

Figure 2. Schematic of bias generator

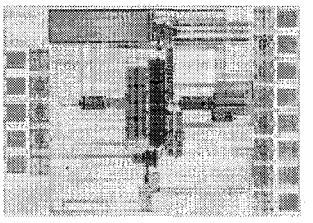

Figure 3. Layout of the proposed amplifier

III. POST-LAYOUT SIMULATION RESULTS

To design a precision amplifier, it is necessary that the circuit characteristics remains robust for all process corners and the desired operating temperature range before trimming can be applied for offset reduction. The complete circuit is simulated for a load capacitance of 500 pF using SPECTRE simulator with BSIM3v3 models. The circuit utilizes a single supply of 3.3V and is designed in the TSMC 0.18μm CMOS process. In order to demonstrate

the operation of the rail-to-rail input feature, Fig. 4 shows a plot of variations in the low frequency gain, post-layout simulated at 0.01 Hz over a common mode input voltage range from 0 to 3.3 V. These results, obtained for all process corners, indicate a uniform g_m control. To minimize distortion, the gain must remain fairly constant over the common mode input range. The simulation was performed for a temperature of 25 ^{0}C and similar results were obtained for the complete operating temperature range (-40^{0}C to +85^{0}C). Table 1 shows the specifications of the amplifier over the temperature range for a Typical-Typical process corner. These simulations indicate low variation of different amplifier specifications over a wide temperature range. Table 2 shows the variability of the specifications over all five process corners at 25^{0}C. These results confirm that a robust architecture is achieved while maintaining low power consumption.

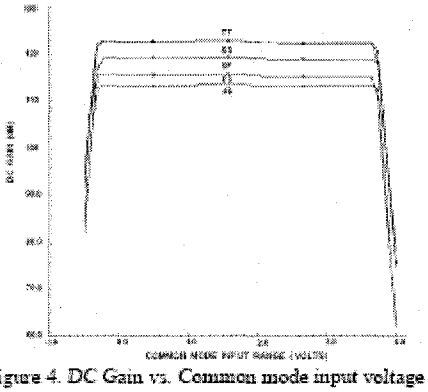

Figure 4. DC Gain vs. Common mode input voltage

Table 1: Results for Typical-Typical (TT) process corner

Temperature (^{0}C)	- 40	+ 25	+ 85
Gain (dB)	125.4	123.0	120.4
Phase Margin (^{0})	67.37	62.87	59.39
GBW (kHz)	741.5	628.1	551.0
Power (mW)	0.54	0.55	0.57

Table 2: Simulation results at T = 25^{0}C

Process	TT	SS	FF	FS	SF
Gain (dB)	123.0	124.8	111.9	116.0	119.6
Phase (^{0})	62.87	61.77	66.30	66.36	60.92
GBW (kHz)	628.1	589.1	684.5	613.9	650.2
Power (mW)	0.55	0.66	0.52	0.62	0.55

IV. TRIMMING FOR OFFSET REDUCTION

If the trimmed resistor is to achieve a specific target value in order to adjust the input offset voltage, the physical length, L, of the diffused resistor must be determined appropriately. The diffused resistor is shown in Fig. 5. Let MAX ($V_{OS\text{-}UNTRIMMED}$) be the maximum offset voltage before trimming that can be corrected and $V_{OS\text{-}TRIMMED}$ is the target value of the offset voltage after trimming. The process of trimming involves a single laser pulse in the gap region between the diffused resistors at a distance, L_{PULSE}. The two highly doped regions form the diffused resistors that have top nodes C and D connected to each other, thus forming a chain of two resistors in series between node A and B. Assuming there is enough energy in the laser pulse, its interaction with silicon results in melting of the two highly doped regions, causing dopant diffusion in the gap region that creates a low resistance path between them. This is electrically equivalent to making a short circuit connection between two identical segments of the highly doped regions. This process produces a change in the resistance value of R_{TRIM}. For this design, N+ diffusion resistors have been used. This single laser pulse is generated by a laser beam positioning system that has a minimum resolution in a given direction. The minimum spatial resolution between two distinct laser beam positions, B and $B+1$ is called X. Assuming a linear relationship between laser pulse position and the resulting offset voltage after trimming, the physical length of the diffused resistor L is given by

$$L \geq \frac{Max(V_{OS\text{-}UNTRIMMED})}{2V_{OS\text{-}TRIMMED}} \cdot X \qquad (1)$$

Still assuming linearity, the position at which the laser beam for trimming must be placed in the gap between the diffused resistors is approximately given by

$$L_{PULSE} \cong \frac{V_{OS\text{-}UNTRIMMED}}{V_{OS\text{-}TRIMMED}} \qquad (2)$$

The above analysis is correct to first order and a more elaborate work on this subject is underway to determine L_{PULSE}.

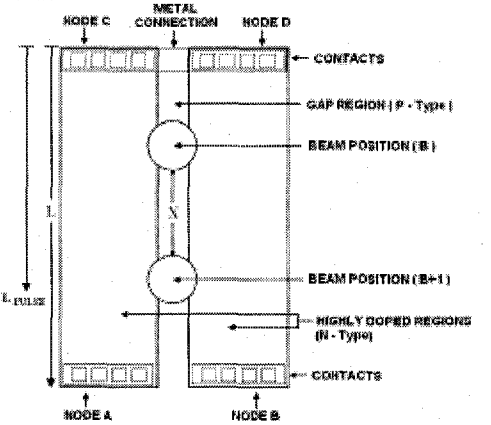

Figure 5. Diffused resistor (R_{TRIM}) with beam positioning

To trim the input offset voltage to few tenths of a microvolt, the test circuit configuration must not introduce errors greater than the offset voltage. For the proposed architecture of the amplifier, a closed loop non-inverting configuration has been used for offset voltage measurement and adjustment [9]. The input referred offset voltage is modeled as a voltage source, V_{OS} at the non-inverting input of the amplifier for the purpose of simulation. The input referred offset voltage for a non-inverting configuration can be expressed as

$$V_{OS} = (V_{OUT} - V_{CM}) / A_{CL} \qquad (3)$$

where V_{OUT} is the output DC voltage, V_{CM} is the common mode input voltage and A_{CL} is the closed loop gain. The V_{OS} expression may have a positive or negative value that determines which R_{TRIM} resistor will be subject to trimming. The effect of offset adjustment by trimming the resistors R_{TRIM} on V_{OS} has been plotted in Fig. 6. The temperature coefficient of the diffused resistor R_{TRIM} is taken into account while performing any simulations. The plot shows different values of $V_{OS\text{-}TRIMMED}$ obtained for corresponding values of R_{TRIM}. Table 3 shows an example of conditions before and after trimming. It demonstrates that initial offset voltage of +2 mV was reduced to a target value of +70.9 μV while trimming R_{TRIM} from 20KΩ to 1KΩ. The offset is adjusted for a V_{CM} = 1.65 V or mid-supply value when both PMOS and NMOS differential pairs are operating. The input offset voltage will vary over the entire common mode voltage range, depending upon which differential pair is active, NMOS or PMOS or both [10,11]. To maintain a low offset voltage variation over a wide common mode would require an additional pair diffused resistors connected with the lower resistor R6 and R7 similar to R2-R5 and R_{TRIM} connection. This configuration has not yet been incorporated in the proposed amplifier topology.

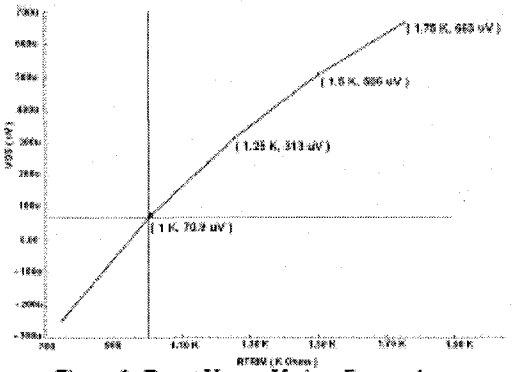

Figure 6. Target V_{OS} vs. Various R_{TRIM} values

Table 3: Trim conditions at T = 25°C (V_{CM} =1.65 V)

CONDITION	NO-TRIM	POST-TRIM
R_{TRIM} *(Parallel with R2=1K)*	20 KΩ	1 KΩ
V_{OS}	+2 mV	+70.9 μV

V. CONCLUSION

The circuit description of a proposed precision CMOS amplifier and PTAT bias generator was presented. It was shown that amplifier characteristics are tolerant to process variations, supply and temperature changes. Simulations also showed the application of laser trimmable diffused resistors to reduce the input referred DC offset voltage. A prototype chip has been submitted for fabrication to validate the precision amplifier functionality and the effect of the laser trimmed diffused resistors.

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