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MULTIPHASE SHORT-CIRCUIT ANALYSIS SOLVER IN PHASE DOMAIN USING A MODIFIED-AUGMENTED-NODAL ANALYSIS APPROACH

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Ce mémoire intitulé :

MULTIPHASE SHORT-CIRCUIT ANALYSIS SOLVER IN PHASE DOMAIN USING A MODIFIED-AUGMENTED-NODAL ANALYSIS APPROACH

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RÉSUMÉ

Ce mémoire présente un nouvel algorithme qui a pour objectif de calculer les valeurs de court-circuit en utilisant une méthode d'analyse nodale-modifiée-augmentée (MANA). L'intérêt principal de cette méthode est la résolution de réseaux de distributions qui sont complexes et déséquilibrés. Cependant, cette méthode peut être appliquée à la résolution de réseaux équilibrés, déséquilibrés, radiaux et bouclés, et de façon générale aux réseaux de distribution et de transport.

La contribution significative de cette recherche est le développement d'une méthode générale capable de résoudre des fautes parallèles, des fautes séries et des fautes simultanées sur divers barres du réseau tout en évaluant les courants de contributions sur l'ensemble des appareils constituants le réseau multi-phasé. De plus, ce document présente un algorithme de résolution du court-circuit sur toutes les barres du réseau avec une méthode efficace combinée avec un solveur robuste et performant pour des systèmes linéaires à matrices creuses non-symétriques.

La méthodologie proposée est de définir les modèles des équipements typiques que l'on retrouve dans les réseaux de distribution, soit les sources de postes, les transformateurs à deux enroulements, les transformateurs à trois enroulements, les machines synchrones, les machines à inductions, les lignes couplées, les câbles et les appareils de protections et de sectionnement. Par la suite, on tente de développer des algorithmes pouvant résoudre les systèmes multi-phase complexes et déséquilibrés. Enfin, une aperçue des techniques de résolution directes de systèmes linéaires est étudiée pour réduire le temps de calculs pour la résolution du problème de court-circuit.

Les modèles et les algorithmes ont été validés en comparant les résultats avec des références publiées. Les résultats démontrent une bonne précision numérique des modèles et une robustesse des algorithmes. La performance de la résolution demeure cependant une recherche importante à poursuivre.

ABSTRACT

This dissertation presents a new algorithm for the calculations of short-circuit currents in multiphase power systems using the modified-augmented-nodal analysis (MANA) approach. The main focus of this method is to solve complex unbalanced distribution systems. However, the proposed method is also applicable to balanced, unbalanced, radial and highly meshed secondary networks or transmission systems.

The main contribution of this research is the development of a general method able to compute shunt, series and simultaneous fault currents at fault locations with the evaluation of contributing currents on all network devices using a multiphase circuit representation. It also presents how to compute short-circuit currents at any system location with an efficient method combined with a high-performance and robust package for large sparse asymmetric linear systems.

The proposed methodology starts by defining typical models of devices in the distribution system, such as substation sources, two-winding transformers, three-winding transformers, synchronous machines, induction machines, overhead electromagnetic coupled lines, cables, switching devices and protective devices. Then, short-circuit algorithms are developed to solve multiphase complex unbalanced systems. An overview of sparse linear equation direct solution methods is also presented for the objective of computational time reduction in large scale systems.

The models and algorithms are validated using published references. The validation tests cases have shown good numerical accuracy and robustness on small and large networks. The performance remains an issue for large networks and further research remains to be contributed on this particular aspect.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST of NOTATION and ABBREVIATIONS

(1.1)	Equation 1.1
[1]	Reference 1
$\mathbb{C}$	Complex number
$\boldsymbol{D_c}$	MANA Dependency functions matrix
E_{N-LL}	Nominal line-to-line voltage
$\boldsymbol{I_d}$	MANA Unknown currents in dependent voltage source vector
$\boldsymbol{I_n}$	MANA Nodal currents injection vector
$\boldsymbol{I_s}$	MANA Unknown currents in zero impedance element vector
$\boldsymbol{I_v}$	MANA Unknown source current vector
$\boldsymbol{S_c}$	MANA Adjacency matrix of zero impedance type devices
$S_{cc-1\emptyset}$	Single-phase short-circuit power
$S_{cc-3\emptyset}$	Three-phase short-circuit power
$\boldsymbol{S_d}$	MANA Adjacency matrix of infinite impedance type devices
$\boldsymbol{V_b}$	MANA Voltage sources vector
$\boldsymbol{V_c}$	MANA Voltage sources adjacency matrix
$\boldsymbol{V_n}$	MANA Unknown node voltages vector
$\boldsymbol{Y_n}$	MANA Linear network admittance matrix
Z_0	Complex zero sequence impedance
Z_1	Complex positive sequence impedance
Z_2	Complex negative sequence impedance
ANSI	American National Standards Institute
BCBV	Branch-to Current to Bus-Voltage matrices
BIBC	Bus-Injection to Branch-Current matrices
CCLRC	Council for the Central Laboratory of the Research Councils
CTs	Current transformers
Delta	Ungrounded delta connection or system
DER	Distributed Energy Resources

DG	Distributed Generation
DMS	Distribution Management System
EMTP-RV	Electromagnetic Transients Program Restructured Version
EPRI	Electric Power Research Institute
GMR	Geometrical Mean Radius
IEEE	Institute of Electrical and Electronic Engineers
LG	Single Line-To-Ground Fault
LL	Line-To-Line Fault
LLG	Double Line-To-Ground Fault
LLL	Three-Phase Fault
LLLG	Three-Phase-To-Ground Fault
MANA	Modified-Augmented-Nodal Analysis
MNA	Modified Nodal Analysis
PES	Power Engineering Society
PTs	Potential transformers
p.u.	Per-Unit
rhs	Right-Hand Side
SPICE	Simulation Program with Integrated Circuit Emphasis
TCC	Time-Current Characteristic
UPEC	University Power Engineering Conference
X/R	Inductive per resistive ratio
Y	Wye ungrounded connection or system
Yg	Wye grounded connection or system

CHAPTER 1. **INTRODUCTION**

1.1. Overview

This dissertation presents a new algorithm for the calculation of short-circuit currents in multiphase network using the modified-augmented-nodal analysis (MANA) approach [1]–[3]. The main focus of this method is to solve complex unbalanced distribution systems. However, this method is also applicable to balanced, unbalanced, radial, highly meshed distribution and transmission systems. Furthermore, this method is oriented towards applications in distribution and transmission system planning and operation. This presentation is assuming linear network components. Furthermore, it considers deactivated dynamic controls for planning short-circuit studies (e.g. LTC).

The computation of short-circuit currents for distribution and transmission systems has been traditionally accomplished by the application of the method of symmetrical components [4]-[8] in sequence network domain. For balanced three-phase systems, this method has shown precise results since the symmetrical transformation theorem is accurate for balanced systems (continuously transposed transmission lines, balanced loads, and balanced generation and transformation components). Since distribution feeders are inherently unbalanced systems, the method of symmetrical components exhibits significant approximations. The validity of the short-circuit study using sequence networks can be seriously jeopardised when considering complex configurations in the distribution system, such as phase merging topology, single-phase distributed generation (DG), single-phase two wire configurations and atypical transformer configurations (YNOdo and DOdo).

Switching and protective devices are largely represented in systems for contingency analysis and reliability analysis. These zero impedance devices can be cumbersome for a matrix based short-circuit solver.

Since the accuracy of short-circuit analysis has a direct impact on protection and coordination studies and on the reliable operation of distribution systems, a general multiphase

method should replace the traditional sequence network based method used in many short-circuit software packages. Therefore, the target of this project is to introduce a general approach and generic modeling capabilities to solve complex unbalanced networks. With the high penetration of distributed energy resources (DER) in the distribution system, there has been a surge of interest in three-phase (or multiphase) short-circuits analysis, since these models encounter severe limitations in sequence domain. This is the area of study and thus the scope of this research.

1.2.Research Objective and Methodology

1.2.1. Objective

The objective of this research is to develop an algorithm for calculating short-circuit currents for complex unbalanced distribution systems using the MANA method. This method fully respects actual network components of distribution and transmission systems and reduces the necessity of pre- and post- processing tasks in the implementation of the algorithm. Although the presented method is of a general nature and is suitable for transmission systems or other highly meshed systems (e.g. secondary distribution networks), the main focus of this research is on unbalanced distribution systems.

1.2.2. Methodology

The methodology followed in this research considers several steps. The first step is the modeling of all distribution components in MANA representation.

Once all the devices are modeled in a specified formulation method, the second step is to develop the algorithms for short-circuit analysis. The solution of MANA equations requires the usage of sparse matrix packages. Such linear algebra packages must be capable of solving large, sparse and unsymmetrical matrices. Hence, the selection of a high-performance, robust, memory efficient package is strongly related to the research presented in this work.

The validation of short-circuit calculations presented in this work is based on recognized benchmarks. These validation benchmarks were selected for different purposes. The first tests were used to validate the device models and the general algorithm. A balanced network solution

was selected and compared with a published reference [5]. To validate unbalanced networks, results for the 13-bus feeder from IEEE [9] developed by the Distribution Test Feeder Working Group, part of IEEE Power and Energy Society (PES) Distribution System Analysis Subcommittee, are presented and compared to the solutions submitted by the working group. Finally, performance tests were conducted comparing two known solvers, KLU and MKL PARDISO.

1.3.Report Outline

Chapter One presents an overview of the research orientation and provides information on the objectives and the methodology used for this research project.

Chapter Two presents a literature review for short-circuit calculation methodologies and numerical solutions. The scope and limitations of these techniques are also discussed. A comprehensive description of the MANA method is presented as well.

Chapter Three focuses on distribution network devices represented in the MANA formulation.

Chapter Four presents different fault models using the MANA formulation and the algorithms for four different types of analysis. The four analysis types are: short-circuit current on all single phase and three-phase buses and nodes, shunt fault on a specific bus with fault flow, series fault on a specific bus with fault flow and simultaneous fault on several buses and lines with fault flow.

Chapter Five presents validation test cases used for testing the presented solution methods.

Chapter Six presents conclusions and recommendations for further research.

1.4.Research Contribution

The major contribution of this research is the development of methods able to:

- Compute shunt fault, series fault and simultaneous fault currents at fault locations with the evaluation of contributing currents on all network devices using multiphase circuit representation;

- Compute short-circuit currents at all locations of a system with an efficient method designed for system planning and operation purposes;

- Solve any type of network configuration: radial, highly meshed, phase-merging, three-phase, single phase, large (more than 10 000 bus) systems;

- Solve with a high-performance, robust, memory efficient and easy to use package for large sparse unsymmetrical linear systems and possibly ill-conditioned networks;

- Adequately represent practical devices in distribution systems, such as substation sources, two-winding transformers, three-winding transformers, electronically coupled generators, synchronous machines, induction machines, overhead electromagnetic coupled lines, cables, shunt inductances, switching and protective devices etc.

An additional contribution of this research project is the benchmarking and testing of several high-performance sparse linear solvers for circuit simulation.

It is noted that all the above contributions are within the context of specialized short-circuit analysis tools used for power system design and operation. The short-circuit currents are calculated in steady-state phasor domain. Such tools are designed for quick and multiple location fault calculations, protection and coordination analysis. This presentation contributes to the improvement and generalizations of traditional short-circuit analysis tools.

CHAPTER 2. **SHORT-CIRCUIT ANALYSIS**

2.1. Literature Review

Short-circuit analysis consists of calculating fault currents and voltages primarily for the determination of protection and coordination time-current characteristic (TCC) [10]. It is traditionally performed using symmetrical sequence networks [4]-[8]. Sequence networks have been utilized mostly for balanced transmission systems and can provide an exact solution with fast computational performance and reduced memory usage. The nodal admittance matrix (Y_{Bus}) formulation is the most widely used method for formulating network equations for short-circuit calculations. It can be found in most power system reference books. The nodal impedance matrix (Z_{Bus}) [11][12] building algorithms based on graph theory and topological particularities are also used for finding short-circuit currents. The compensation method is a computational scheme for simulating the effects of changes in the values of a network's passive elements. It uses the admittance matrix to compute short-circuit currents in the sequence domain [13] [14]. A post processing is necessary to compute source contributions and protective device currents.

The distribution system is an unbalanced network. Therefore, short-circuit analysis based on multiphase unbalanced network representation is unavoidable. With the development of faster computers and with the availability of more precise system data in power utilities, it is necessary and technically affordable to perform short-circuit analysis using detailed multiphase representation. In addition, the interconnection of three-phase and single-phase distributed generation has increased the importance of multiphase analysis [15]. The complexity of some configurations such, as phase-merging and atypical transformer connections (YNOdo, for example), require a phase domain analysis approach in order to provide an accurate solution.

Considering the radial structure of a distribution feeder, an equivalent three-phase impedance matrix method was developed with the capability to incorporate different types of faults [16][17]. Achieving the advantages of high performance, robust convergence and accuracy for radial systems, another method based on two matrices, the bus-injection to branch-current matrix (***BIBC***) and the branch-to current to bus-voltage matrix (***BCBV***), was developed to solve

various types of single or simultaneous unsymmetrical faults [18]-[20]. The ladder iterative technique, also known as the backward/forward sweep technique, is also a method used for computing short-circuit values for unbalanced distribution systems [21][22]. This technique can encounter some convergence issues when dealing with ungrounded transformer connections and delta type systems. Furthermore, the ladder iterative technique addresses only radial and weakly meshed networks. An approach in phase domain representation oriented towards applications in distribution system operation analysis using a nodal admittance matrix was developed in [23]. This technique can compute cross country (two faults affecting the same circuit) and triple double-line-to-ground faults. It also takes into considerations load and generator contribution by performing a load flow prior to solving the short-circuit analysis. As stated by the author of [23] the transformer models used in this method are non-trivial since they are based on the classical Y_{Bus} representation. Also, zero impedance devices, such as protective devices and switching devices, must be removed in a pre-treatment process.

In this dissertation, a general multiphase short-circuit analysis technique capable of solving any type of structured network is presented. This technique is based on the MANA formulation [1]-[3].

The classical nodal analysis formulation has some important disadvantages when modeling the power system. One of the disadvantages is the inability to incorporate ungrounded voltage sources. This issue has been addressed by using modified nodal analysis (MNA) [24]. Hence, extra equations for voltage sources were added to the linear system. Assuming a nodal admittance model for every component is a significant limitation. An ideal transformer model and zero impedance devices do not have an admittance matrix formulation. The MANA formulation can eliminate various classical nodal and MNA limitations.

The MANA method models transformer and other power system devices using circuit based relations, thus respecting the actual circuit components. It reduces pre-processing and post-processing by avoiding matrix manipulations and by retaining zero impedance elements and different source type current contributions [2]. The solution technique uses a sparse matrix solved by employing LU factorization algorithms.

2.2.Modified-Augmented-Nodal Analysis

The MANA expands the MNA formulated in the mid 1970's. The general MANA formulation uses the following symbolic formulation [3][25]:

$$\begin{bmatrix} \boldsymbol{Y_n} & \boldsymbol{V_c} & \boldsymbol{D_c} & \boldsymbol{S_c} \\ \boldsymbol{V_r} & \boldsymbol{V_d} & \boldsymbol{V_{VD}} & \boldsymbol{S_{VS}} \\ \boldsymbol{D_r} & \boldsymbol{D_{DV}} & \boldsymbol{D_d} & \boldsymbol{S_{DS}} \\ \boldsymbol{S_r} & \boldsymbol{S_{SV}} & \boldsymbol{S_{SD}} & \boldsymbol{S_d} \end{bmatrix} \begin{bmatrix} \boldsymbol{V_n} \\ \boldsymbol{I_v} \\ \boldsymbol{I_d} \\ \boldsymbol{I_s} \end{bmatrix} = \begin{bmatrix} \boldsymbol{I_n} \\ \boldsymbol{V_b} \\ \boldsymbol{D_b} \\ \boldsymbol{S_b} \end{bmatrix} \tag{2.1}$$

This formulation is used for steady-state and time-domain solutions in EMTP-RV [26]. A more simplified approach given by the following equation is used in this presentation

$$\begin{bmatrix} \boldsymbol{Y_n} & \boldsymbol{V_c} & \boldsymbol{D_c} & \boldsymbol{S_c} \\ \boldsymbol{V_c^t} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \boldsymbol{D_c^t} & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \boldsymbol{S_c^t} & \mathbf{0} & \mathbf{0} & \boldsymbol{S_d} \end{bmatrix} \begin{bmatrix} \boldsymbol{V_n} \\ \boldsymbol{I_v} \\ \boldsymbol{I_d} \\ \boldsymbol{I_s} \end{bmatrix} = \begin{bmatrix} \boldsymbol{I_n} \\ \boldsymbol{V_b} \\ \mathbf{0} \\ \mathbf{0} \end{bmatrix} \tag{2.2}$$

It is also used only in steady-state phasor domain solution.

In the above equation:

$\boldsymbol{Y_n}$: linear network admittance matrix

$\boldsymbol{V_c}$: voltage sources adjacency matrix

$\boldsymbol{D_c}$: dependency functions matrix

$\boldsymbol{S_c}$: adjacency matrix of zero impedance type devices

$\boldsymbol{S_d}$: adjacency matrix of infinite impedance type devices

$\boldsymbol{V_n}$: vector of unknown nodal

$\boldsymbol{I_v}$: vector of unknown voltage source currents

$\boldsymbol{I_d}$: vector of unknown currents in dependent branch functions

$\boldsymbol{I_s}$: vector of unknown currents in zero impedance element vector

$\boldsymbol{I_n}$: vector of nodal current injections

$\boldsymbol{V_b}$: vector of known source voltages

The following theory taken from [1] is repeated here for convenience and relations to further developments.

2.2.1. Independent Voltage Sources

If a voltage source is connected between any two nodes *k* and *m*, then:

$$v_k - v_m = v_s \tag{2.3}$$

where $v_s \in \boldsymbol{V_b}$. This places a 1 in column *k* and a -1 in column *m* of the voltage source equation in $\boldsymbol{V_c}$. If the voltage source is numbered as *q* in the list of voltage sources, then

$$\boldsymbol{V_c^t}(q,k) = 1 \tag{2.4}$$

$$\boldsymbol{V_c^t}(q,m) = -1 \tag{2.5}$$

$$\boldsymbol{V_c}(k,q) = 1 \tag{2.6}$$

$$\boldsymbol{V_c}(m,q) = -1 \tag{2.7}$$

$$\boldsymbol{V_b} = v_s \tag{2.8}$$

Equations (2.4) and (2.5) are used to account for the voltage source relation (2.3). Equations (2.6) and (2.7) stand for the sum of currents exiting the nodes *k* and *m*.

2.2.2. Ideal Transformer Model

An ideal transformer model consists of one dependant voltage source and a dependent current source. It is shown in Figure 2-1.

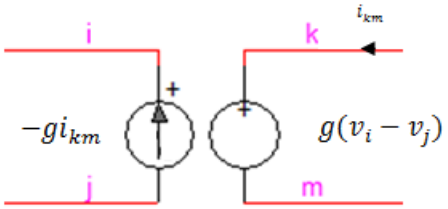


Figure 2-1 Two-Port Ideal Transformer Representation

It can be represented using the equation:

$$v_k - v_m - gv_i + gv_j = 0 \tag{2.9}$$

where g is the turn ratio. This model is equivalent to the traditional ideal transformer representation shown in Figure 2-2. This last representation will be used in this document.

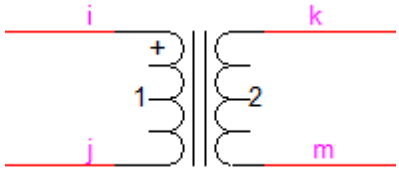


Figure 2-2 Traditional Ideal Transformer Representation

If an ideal transformer model is numbered as q in the list of dependent branch functions, then its contribution is:

$$\boldsymbol{D_c^t}(q,k) = 1 \tag{2.10}$$

$$\boldsymbol{D_c^t}(q,m) = -1 \tag{2.11}$$

$$\boldsymbol{D_c^t}(q,i) = -g \tag{2.12}$$

$$\boldsymbol{D_c^t}(q,j) = g \tag{2.13}$$

and:

$$\boldsymbol{D_c}(k,q) = 1 \tag{2.14}$$

$$\boldsymbol{D_c}(m,q) = -1 \tag{2.15}$$

$$\boldsymbol{D_c}(i,q) = -g \tag{2.16}$$

$$\boldsymbol{D_c}(j,q) = g \tag{2.17}$$

2.2.3. Zero and Infinite Impedance Elements

If a zero impedance element is connected between two arbitrary nodes *k* and *m*, the unit can be considered as an ideal closed switch. It can be represented by the equation:

$$v_k - v_m = 0 \tag{2.18}$$

For the switch numbered *q* in the list of switches:

$$\boldsymbol{S_c^t}(q,k) = 1 \tag{2.19}$$

$$\boldsymbol{S_c^t}(q,m) = -1 \tag{2.20}$$

$$\boldsymbol{S_c}(k,q) = 1 \tag{2.21}$$

$$\boldsymbol{S_c}(m,q) = -1 \tag{2.22}$$

$$\boldsymbol{S_d}(q,q) = 0 \tag{2.23}$$

If an infinite impedance element is connected between two arbitrary nodes *k* and *m*, then it can be considered as an ideal open switch. It can be represented by the equation:

$$i_{km} = 0 \tag{2.24}$$

For the switch numbered q in the list of switches:

$$\boldsymbol{S_c^t}(q,k) = 0 \tag{2.25}$$

$$\boldsymbol{S_c^t}(q,m) = 0 \tag{2.26}$$

$$\boldsymbol{S_c}(k,q) = 0 \tag{2.27}$$

$$\boldsymbol{S_c}(m,q) = 0 \tag{2.28}$$

$$\boldsymbol{S_d}(q,q) = 1 \tag{2.29}$$

CHAPTER 3. MANA MODELS FOR MULTIPHASE DEVICES

This section presents the detail models for the distribution devices. To ease the comprehension of the models, each device is presented by a general matrix following the equation (2.2). These matrices (e.g. $\boldsymbol{Y_n}$ or $\boldsymbol{V_c}$) represent a sub matrix of the whole system.

3.1. Substation

A substation is modeled by an equivalent source. In the distribution system, it is modeled as an ideal source with an equivalent impedance. The equivalent impedance is generally given in sequence domain. The sequence impedances are based on three-phase short-circuit power, line-to-ground short-circuit power and the reactance over resistance (X/R) ratio:

$$S_{cc-3\emptyset} = \frac{E_{N-LL}^2}{|Z_1|} \tag{3.1}$$

$$S_{cc-1\emptyset} = \frac{3 \cdot E_{N-LL}^2}{|2Z_1 + Z_0|} \tag{3.2}$$

Where:

$S_{cc-3\emptyset}$: three-phase short-circuit power

$S_{cc-1\emptyset}$: single-phase short-circuit power

E_{N-LL} : nominal line-to-line voltage

Z_1 : complex positive sequence impedance

Z_0 : complex zero sequence impedance

By solving equation (3.1), we find the module of the complex positive sequence. By knowing the X/R ratio Z_1 can be determined. The zero sequence impedance is then computed by using equation (3.2). The negative sequence (Z_2) impedance is assumed to be equal to Z_1 due to

balanced system representation. These impedances are then converted into phase domain using Fortescue transformation [7]:

$$Z_s = \frac{1}{3}(Z_0 + 2Z_1) \tag{3.3}$$

$$Z_m = \frac{1}{3}(Z_0 - Z_1) \tag{3.4}$$

Where:

Z_s : Self Impedance of a continuously transposed line

Z_m : Mutual Impedance of a continuously transposed line

The phase admittance matrix of the source can be defined as:

$$\boldsymbol{Y_{source}} = \begin{bmatrix} Z_s & Z_m & Z_m \\ Z_m & Z_s & Z_m \\ Z_m & Z_m & Z_s \end{bmatrix}^{-1} = \begin{bmatrix} Y_s & Y_m & Y_m \\ Y_m & Y_s & Y_m \\ Y_m & Y_m & Y_s \end{bmatrix} \tag{3.5}$$

Distribution substations are generally three-phase systems. For any type of three-phase source (Yg, Y, and Delta) with an impedance connected between the nodes *k* and *m*, the equivalent linear admittance matrix is found as:

$$\boldsymbol{Y_n} = \begin{bmatrix} & k_a & k_b & k_c & m_a & m_b & m_c \\ k_a & Y_s & Y_m & Y_m & -Y_s & -Y_m & -Y_m \\ k_b & Y_m & Y_s & Y_m & -Y_m & -Y_s & -Y_m \\ k_c & Y_m & Y_m & Y_s & -Y_m & -Y_m & -Y_s \\ m_a & -Y_s & -Y_m & -Y_m & Y_s & Y_m & Y_m \\ m_b & -Y_m & -Y_s & -Y_m & Y_m & Y_s & Y_m \\ m_c & -Y_m & -Y_m & -Y_s & Y_m & Y_m & Y_s \end{bmatrix} \tag{3.6}$$

Equation 3.6 can be also written in a compact form:

$$\boldsymbol{Y_n} = \begin{bmatrix} \boldsymbol{Y_{source}} & -\boldsymbol{Y_{source}} \\ -\boldsymbol{Y_{source}} & \boldsymbol{Y_{source}} \end{bmatrix} \tag{3.7}$$

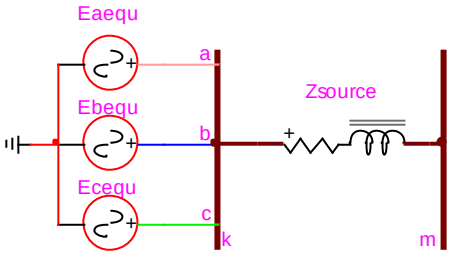


Figure 3-1: Yg Substation Source Configuration

For a Yg type of source shown in Figure 3-1, the voltage sources adjacency matrix and voltage source vectors are found by inspection:

$\boldsymbol{V_c}$ is a 6 x3 matrix:

$$\boldsymbol{V_c} = \begin{bmatrix} & q_1 & q_2 & q_3 \\ k_a & 1 & 0 & 0 \\ k_b & 0 & 1 & 0 \\ k_c & 0 & 0 & 1 \end{bmatrix} \tag{3.8}$$

$\boldsymbol{V_b}$ is a 3 x1 vector:

$$\boldsymbol{V_b} = \begin{bmatrix} & 1 \\ q_1 & E_{aequ} \\ q_2 & E_{bequ} \\ q_3 & E_{cequ} \end{bmatrix} \tag{3.9}$$

where:

E_{iequ} : Equivalent positive sequence voltage for phase i, i = a,b,c

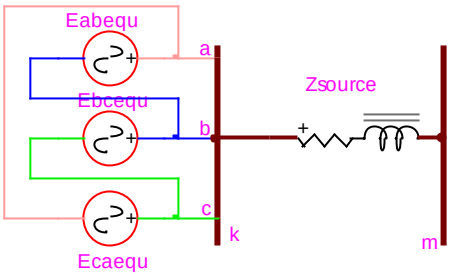


Figure 3-2: Delta Substation Source Configuration

For Delta type of source shown in Figure 3-2, the linear admittance matrix is the same as for the Yg. The voltage source adjacency matrix and the voltage source vector are found by inspection:

$\boldsymbol{V_c}$ is a 6 x3 matrix:

$$\boldsymbol{V_c} = \begin{bmatrix} & q_1 & q_2 & q_3 \\ k_a & 1 & 0 & -1 \\ k_b & -1 & 1 & 0 \\ k_c & 0 & -1 & 1 \end{bmatrix} \tag{3.10}$$

$\boldsymbol{V_b}$ is a 3 x1 vector:

$$\boldsymbol{V_b} = \begin{bmatrix} & 1 \\ q_1 & E_{aequ} - E_{bequ} \\ q_2 & E_{bequ} - E_{cequ} \\ q_3 & E_{cequ} - E_{aequ} \end{bmatrix} \tag{3.11}$$

These matrices and vectors are inserted into the main network equations using node number mapping. If the source impedance is null, we can replace the the impedances with closed switches:

$\boldsymbol{S_c}$ would then be a 6 x3 matrix:

$$\boldsymbol{S_c} = \begin{bmatrix} & m & n & o \\ k_a & 1 & 0 & 0 \\ k_b & 0 & 1 & 0 \\ k_c & 0 & 0 & 1 \\ m_a & -1 & 0 & 0 \\ m_b & 0 & -1 & 0 \\ m_c & 0 & 0 & -1 \end{bmatrix} \tag{3.12}$$

$\boldsymbol{S_d}$ would then be a 6 x3 matrix:

$$\boldsymbol{S_d} = \begin{bmatrix} & m & n & o \\ m & 0 & 0 & 0 \\ n & 0 & 0 & 0 \\ o & 0 & 0 & 0 \end{bmatrix} \tag{3.13}$$

3.2. Voltage Regulators

Voltage regulators are autotransformers with a voltage regulation apparatus. Commonly, they can adjust taps for a range of -10% to 10% with 32 taps, for example. Hence, each step would represent 0.75 V on a 120V base. There are two types of regulators standardized by the American National Standards Institute: ANSI type A and ANSI type B. The ANSI type A regulator has the taps on the load side and the ANSI type B regulator has the taps on the source side.

Voltage regulators are normally single-phase or three-phase devices. Three-phase devices are either connected in Delta or Yg and the 3 phases have the same tap numbers. The taps of single-phase devices can be controlled individually. Single-phase devices connected on 1 or 2-phase sections are Yg. Single-phase devices connected on 3-phase sections can be either Yg, open Delta or closed Delta (lagging or leading). For short-circuit analysis, it is accepted to consider the voltage regulator as a zero impedance element [27].

For the ANSI type A regulator, voltage ratios are given by:

$$a_R = 1 + \left(\frac{max_{buck} + max_{boost}}{NbOfTaps}\right) \cdot \frac{Tap}{100} \tag{3.14}$$

Where:

a_R : Voltage ratios

max_{buck} : Maximum voltage buck in percent (e.g. -10%)

max_{boost} : Maximum voltage boost (e.g. +10%)

$NbOfTaps$: Number to taps (e.g. 32)

Tap : Operation tap

For the ANSI type B regulator, voltage ratios are given by:

$$a_R = \frac{1}{\left[1 - \left(\frac{max_{buck} + max_{boost}}{NbOfTaps}\right) . \frac{Tap}{100}\right]} \quad (3.15)$$

Single-phase or three-phase closed delta devices have the same model. The only difference is that the voltage ratio of each phase may be different for single-phase devices. The detailed model for closed Delta lagging configuration is shown in Figure 3-3. For a closed Delta lagging voltage regulator between the nodes *k* and *m*, MANA matrices are found by inspection:

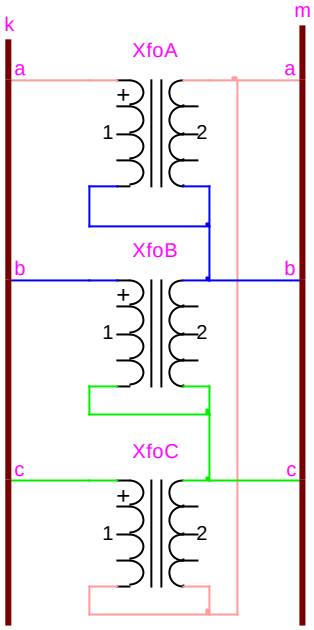


Figure 3-3: Closed Delta Lagging Configuration

The regulator impedance is neglected; hence there is no value in $\boldsymbol{Y_n}$

$\boldsymbol{D_c}$ is a 6 x 3 matrix

$$\boldsymbol{D_c} = \begin{bmatrix} & q_1 & q_2 & q_3 \\ k_a & -a_{RA} & 0 & 0 \\ k_b & 0 & -a_{RB} & 0 \\ k_c & 0 & 0 & -a_{RC} \\ m_a & 1 & 0 & a_{RC} - 1 \\ m_b & a_{RA} - 1 & 1 & 0 \\ m_c & 0 & a_{RB} - 1 & 1 \end{bmatrix} \tag{3.16}$$

The detailed model for closed Delta leading configuration is shown at Figure 3-4. For a closed Delta lagging voltage regulator, MANA matrices are found by inspection:

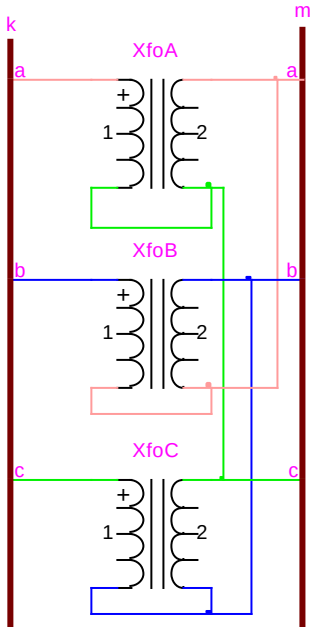


Figure 3-4: Closed Delta Leading Configuration

The linear admittance matrix is the same as for the lagging configuration.

$\boldsymbol{D_c}$ is again a 6 x 3 matrix given by

$$\boldsymbol{D_c} = \begin{bmatrix} & q_1 & q_2 & q_3 \\ k_a & -a_{RA} & 0 & 0 \\ k_b & 0 & -a_{RB} & 0 \\ k_c & 0 & 0 & -a_{RC} \\ m_a & 1 & a_{RB} - 1 & 0 \\ m_b & 0 & 1 & a_{RC} - 1 \\ m_c & a_{RA} - 1 & 0 & 1 \end{bmatrix} \tag{3.17}$$

The model for single phase Yg regulator is shown at Figure 3-5. For a Yg regulator between nodes *k* and *m* we can find a general matrix representation for the active phase *x* , the active phase (e.g. A).

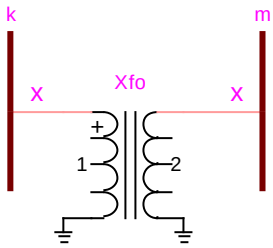


Figure 3-5: Single-Phase Yg Configuration

If n is the number of the active phase, then $\boldsymbol{Y_n}$ is a 2n x 2n empty matrix

$$\boldsymbol{Y_n} = \begin{bmatrix} & k_x & m_x \\ k_x & 0 & 0 \\ m_x & 0 & 0 \end{bmatrix} \tag{3.18}$$

$\boldsymbol{D_c}$ is a 6 x 3 matrix

$$\boldsymbol{D_c} = \begin{bmatrix} & q_1 & q_2 & q_3 \\ k_a & -a_{RA} & 0 & 0 \\ k_b & 0 & -a_{RB} & 0 \\ k_c & 0 & 0 & -a_{RC} \\ m_a & 1 & 0 & a_{RC}-1 \\ m_b & a_{RA}-1 & 1 & 0 \\ m_c & 0 & a_{RB}-1 & 1 \end{bmatrix} \tag{3.19}$$

The same formulation can be addressed to the open Delta configuration.

3.3. Transformers

Three-phase two-winding transformer banks and single-phase two-winding transformers can be found in distribution system. Different configurations can be used for several different purposes. For example, the most common substation transformer connections in North-American utilities are the Yg-Delta (YNd1 or YNd11) connection for economical reasons and protection issues. Furthermore, connections can be selected based on the type of load served by the utility.

Hence, to feed simultaneously single-phase loads and tri-phase loads, Delta-Yg (Dyn1 or Dyn11) is commonly used [28]. Three winding transformers are also used in substations.

A third winding can be used to feed main local substation loads. To lower the voltage at the service point, single-phase distribution transformers (e.g.120/240V) are installed near the utility clients. These types of transformers greatly outnumber the multiphase ones. Transformers can be also connected as autotransformers. Connecting the high-voltage terminal to the low-voltage terminal can create a step-up autotransformer.

The number of different types of transformers is too high to be provided in this document. Nevertheless, no known connections seem to cause a problem to be implemented in the MANA format. The transformer types that have been modeled for this research project are:

1. Three-phase two-winding transformer with connections shown in Table 3-1
2. Three-phase three-winding transformer
3. Distribution transformer (120/240V)

Table 3-1: Three-Phase Transformer Common Connections

Connection	Connection Code
Yg-Yg	YNyn0
Y-Y	Yy0
D-D	Dd0
Y-D	Yd1
Yg-D	YNd1
D-Y	Dy1
D-Yg	Dyn1
D-Z	Dzn0
Yg-Z	YNzn1
Yo-Do	YNOdo1
Do-Do	DOdo0
Y-Yg	Yyn0
Yg-Y	YNy0

3.3.1. Two-Winding Three-Phase Transformers

There are three-types of three-phase two winding transformers based on their construction and conception:

1- Three-phase banks of single units

2- Three-phase shell type

3- Three-phase core type

Other considerations when modeling the transformer are the line tap changer regulator unit, the grounding impedances, the magnetizing branch, the phase shift and the center taps.

Sequence impedances (Z_1 and Z_0) can be found on the nameplate of the transformer and are generally in per-unit (p.u.) or in percent. The X/R ratio is also available for both sequences. Negative sequence impedance is assumed to be equal to positive sequence. The general model for a transformer unit can be represented by the following circuit:

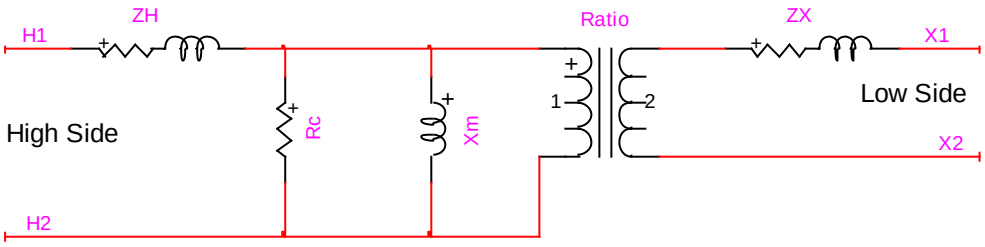


Figure 3-6: General Transformer Model

The Ratio parameter shown in Figure 3-6 can be defined by the nameplate high side/low side voltage and integrating high side/low side fix tap and LTC. For three-phase shell type transformers and single- phase transformers, the magnetization branch (X_m) and the core losses (R_c) are neglected [5]. For three-phase core transformers, a zero-sequence magnetizing branch is included for common configurations (YNyn, YNy and Yyn). Total transformer impedance is represented by the sum of primary and secondary p.u. impedances. The model is then simplified to its simplest scheme shown in Figure 3-7:

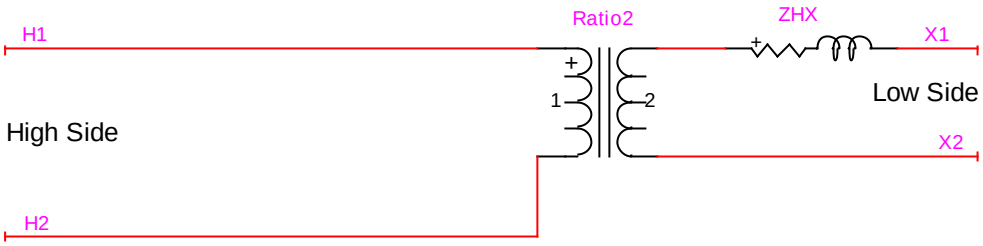


Figure 3-7: Simplified Transformer Model

The three-phase shell type transformer can have different sequence impedances reflecting a mutual effect between phases. For the three-phase single unit transformer, the positive and zero sequence impedances are equal. Thus, there are no mutual effects. This simplifies the linear admittance matrix by setting all mutual admittance to zero. Nevertheless, the MANA model for both transformer types can be generalized using a single model. Consider the connection (YNyn0) seen in figure 3-8 and based on equations 3-3 to 3-7, we find the general formulation:

$\boldsymbol{Y_n}$ is a 11 x 11 matrix:

$$\boldsymbol{Y_n} = \begin{array}{c} \\ k_a \\ k_b \\ k_c \\ m_a \\ m_b \\ m_c \\ n_a \\ n_b \\ n_c \\ o \\ p \end{array} \begin{array}{c} \begin{array}{ccccccccccc} k_a & k_b & k_c & m_a & m_b & m_c & n_a & n_b & n_c & o & p \end{array} \\ \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & Y_{sHX\_1} & Y_{mHX} & Y_{mHX} & -Y_{sHX\_1} & -Y_{mHX} & -Y_{mHX} & 0 & 0 \\ 0 & 0 & 0 & Y_{mHX} & Y_{sHX\_2} & Y_{mHX} & -Y_{mHX} & -Y_{sHX\_2} & -Y_{mHX} & 0 & 0 \\ 0 & 0 & 0 & Y_{mHX} & Y_{mHX} & Y_{sHX\_3} & -Y_{mHX} & -Y_{mHX} & -Y_{sHX\_3} & 0 & 0 \\ 0 & 0 & 0 & -Y_{sHX\_1} & -Y_{mHX} & -Y_{mHX} & Y_{sHX\_1} & Y_{mHX} & Y_{mHX} & 0 & 0 \\ 0 & 0 & 0 & -Y_{mHX} & -Y_{sHX\_2} & -Y_{mHX} & Y_{mHX} & Y_{sHX\_2} & Y_{mHX} & 0 & 0 \\ 0 & 0 & 0 & -Y_{mHX} & -Y_{mHX} & -Y_{sHX\_3} & Y_{mHX} & Y_{mHX} & Y_{sHX\_3} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & Y_{Hg} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & Y_{Xg} \end{bmatrix} \end{array} \tag{3.20}$$

where:

Y_{sHX_i} : Self admittance seen on the low side for unit i, i = 1,2,3

Y_{Hg}/Y_{Xg} : Grounding admittance for high side and low side

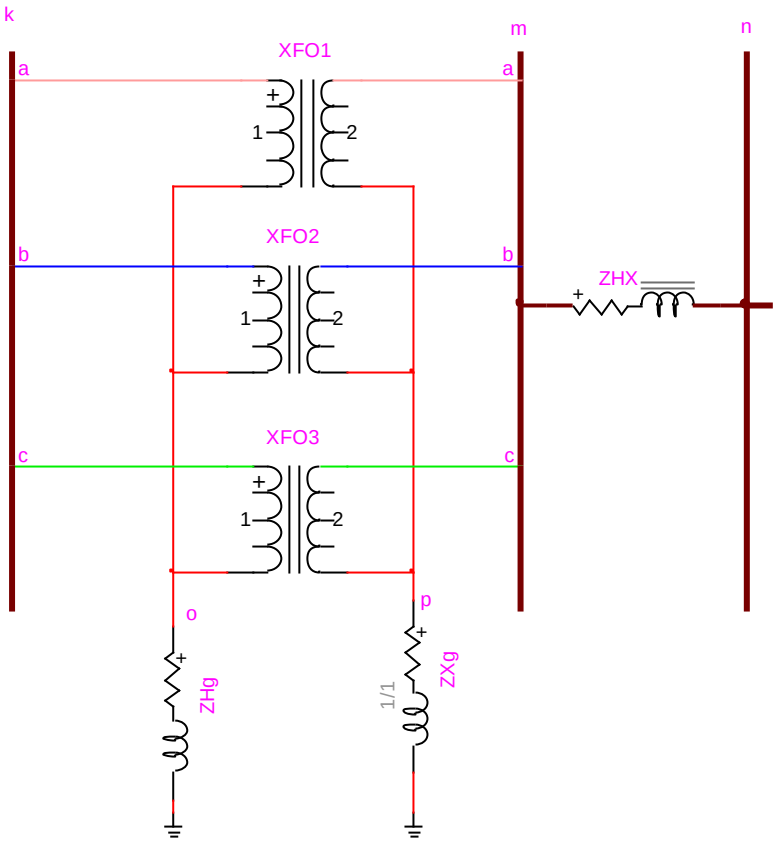


Figure 3-8: YNyn0 Shell Type and Single Phase Unit Transformer

$\boldsymbol{D_c}$ is an 8 x 3 matrix:

$$\boldsymbol{D_c} = \begin{bmatrix} & q_1 & q_2 & q_3 \\ k_a & -g_1 & 0 & 0 \\ k_b & 0 & -g_2 & 0 \\ k_c & 0 & 0 & -g_3 \\ m_a & 1 & 0 & 0 \\ m_b & 0 & 1 & 0 \\ m_c & 0 & 0 & 1 \\ o & g_1 & g_2 & g_3 \\ p & -1 & -1 & -1 \end{bmatrix} \tag{3.21}$$

where:

g_i : Turn ratio for ideal transformer i, i = 1,2,3

The equivalent phase circuit for the three-phase core-form transformer is different from the shell-form type. The zero sequence impedance is generally different from the positive sequence

impedance. Furthermore, the exciting impedance of the zero sequence impedance is in the range of 30-300% and should not be neglected [29]. A tertiary winding is then modeled to take into consideration this effect as shown in Figure 3-9.

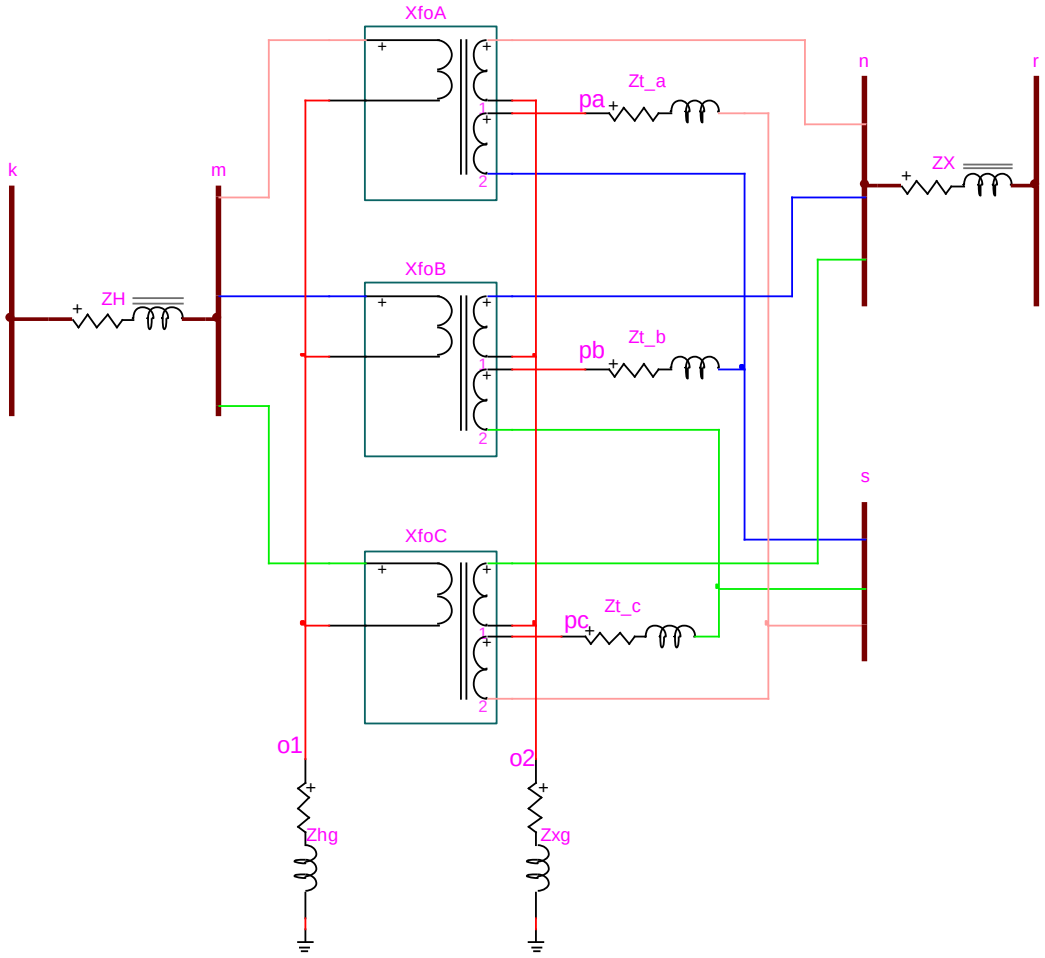


Figure 3-9: Three-Phase Core Type YNyn0 Transformer Model

Due to the large size of $\boldsymbol{Y_n}$, it will be presented using submatrices.

$\boldsymbol{Y_H}$ is a 8 x8 matrix:

$$\boldsymbol{Y_H} = \begin{bmatrix} & k_a & k_b & k_c & m_a & m_b & m_c & o_1 & o_2 \\ k_a & Y_{sH} & Y_{mH} & Y_{mH} & -Y_{sH} & -Y_{mH} & -Y_{mH} & 0 & 0 \\ k_b & Y_{mH} & Y_{sH} & Y_{mH} & -Y_{mH} & -Y_{sH} & -Y_{mH} & 0 & 0 \\ k_c & Y_{mH} & Y_{mH} & Y_{sH} & -Y_{mH} & -Y_{mH} & -Y_{sH} & 0 & 0 \\ m_a & -Y_{sH} & -Y_{mH} & -Y_{mH} & Y_{sH} & Y_{mH} & Y_{mH} & 0 & 0 \\ m_b & -Y_{mH} & -Y_{sH} & -Y_{mH} & Y_{mH} & Y_{sH} & Y_{mH} & 0 & 0 \\ m_c & -Y_{mH} & -Y_{mH} & -Y_{sH} & Y_{mH} & Y_{mH} & Y_{sH} & 0 & 0 \\ o_1 & 0 & 0 & 0 & 0 & 0 & 0 & Y_{Hg} & 0 \\ o_2 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & Y_{Xg} \end{bmatrix} \tag{3.22}$$

$\boldsymbol{Y_X}$ is a 6x6 matrix:

$$\boldsymbol{Y_X} = \begin{bmatrix} & n_a & n_b & n_c & r_a & r_b & r_c \\ n_a & Y_{sX} & Y_{mX} & Y_{mX} & -Y_{sX} & -Y_{mX} & -Y_{mX} \\ n_b & Y_{mX} & Y_{sX} & Y_{mX} & -Y_{mX} & -Y_{sX} & -Y_{mX} \\ n_c & Y_{mX} & Y_{mX} & Y_{sX} & -Y_{mX} & -Y_{mX} & -Y_{sX} \\ r_a & -Y_{sX} & -Y_{mX} & -Y_{mX} & Y_{sX} & Y_{mX} & Y_{mX} \\ r_b & -Y_{mX} & -Y_{sX} & -Y_{mX} & Y_{mX} & Y_{sX} & Y_{mX} \\ r_c & -Y_{mX} & -Y_{mX} & -Y_{sX} & Y_{mX} & Y_{mX} & Y_{sX} \end{bmatrix} \tag{3.23}$$

$\boldsymbol{T_t}$ is a 6 x6 matrix:

$$\boldsymbol{Y_t} = \begin{bmatrix} & p_a & p_b & p_c & s_a & s_b & s_c \\ p_a & Y_t & 0 & 0 & -Y_t & 0 & 0 \\ p_b & 0 & Y_t & 0 & 0 & -Y_t & 0 \\ p_c & 0 & 0 & Y_t & 0 & 0 & -Y_t \\ s_a & -Y_t & 0 & 0 & Y_t & 0 & 0 \\ s_b & 0 & -Y_t & 0 & 0 & Y_t & 0 \\ s_c & 0 & 0 & -Y_t & 0 & 0 & Y_t \end{bmatrix} \tag{3.24}$$

$\boldsymbol{Y_n}$ is a 20 x20 matrix:

$$\boldsymbol{Y_n} = \begin{bmatrix} \boldsymbol{Y_H} & \boldsymbol{0} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{Y_X} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{0} & \boldsymbol{Y_t} \end{bmatrix} \tag{3.25}$$

$\boldsymbol{D_c}$ is a 14 x6 matrix:

$$\boldsymbol{D_c} = \begin{bmatrix} & q_1 & q_2 & q_3 & q_4 & q_5 & q_6 \\ m_a & -g_1 & 0 & 0 & -g_2 & 0 & 0 \\ m_b & 0 & -g_1 & 0 & 0 & -g_2 & 0 \\ m_c & 0 & 0 & -g_1 & 0 & 0 & -g_2 \\ n_a & 1 & 0 & 0 & 0 & 0 & 0 \\ n_b & 0 & 1 & 0 & 0 & 0 & 0 \\ n_c & 0 & 0 & 1 & 0 & 0 & 0 \\ p_a & 0 & 0 & 0 & 1 & 0 & 0 \\ p_b & 0 & 0 & 0 & 0 & 1 & 0 \\ p_c & 0 & 0 & 0 & 0 & 0 & 1 \\ s_a & 0 & 0 & 0 & 0 & 0 & -1 \\ s_b & 0 & 0 & 0 & -1 & 0 & 0 \\ s_c & 0 & 0 & 0 & 0 & -1 & 0 \\ o_1 & g_1 & g_1 & g_1 & g_2 & g_2 & g_2 \\ o_2 & -1 & -1 & -1 & 0 & 0 & 0 \end{bmatrix} \tag{3.26}$$

Every transformer connections of Table 3-1 can be formulated in the MANA format in the same way exposed in this section.

3.3.2. Three-Winding Three-Phase Transformer

Three-winding transformers are considered to be three-phase devices and shell-type transformers. Their MANA model is very close to two-winding core-type transformers. Any of the 3 windings can be configured as Y, Yg, Delta and Zig-Zag. The general MANA representation of an ideal three-winding transformer is shown in Figure 3-10:

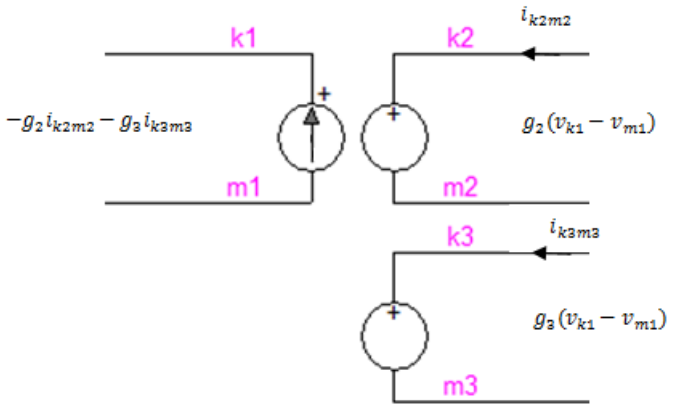


Figure 3-10: Ideal Three-Winding Transformer MANA Model

The MANA model requires the primary impedance on the primary side, the secondary impedance on the secondary side and the tertiary impedance on the tertiary side, all in ohms.

3.3.3. Distribution Transformer

The distribution transformer is used to lower the voltage from the medium voltage (2.4kV to 44kV) level to the secondary network voltage level, typically (120V to 600V). The low voltage side is composed of three-wire connections including the mid-tap connected to ground. Referenced by Lloyd transformation, the equivalent model for distribution transformer is detailed is shown in Figure 3-11 and detailed in [30]:

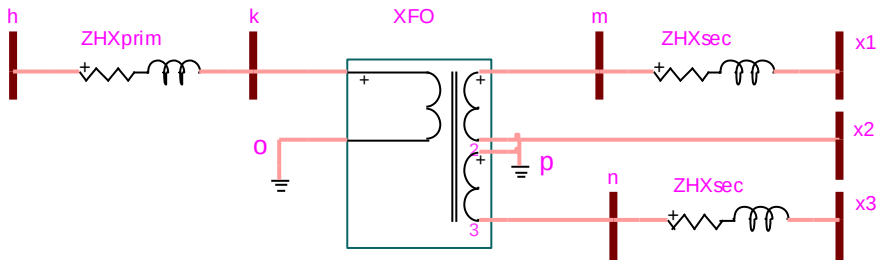


Figure 3-11: Distribution Transformer Model Based on Lloyd Transformation

The MANA model can then be represented with matrices similar to the three-phase transformer connections.

3.4.Machines

Machines can be divided into two groups: synchronous machines and induction machines. Computing their subtransient impedances can be performed through several complex equations based on Park's transformation for synchronous machines and on equivalent circuits for induction motors. It is not the purpose of this research to compute such impedances. This document presents the MANA models to handle three-phase synchronous machines and induction machines taking into consideration their connection and internal impedances.

Machines are handled in the same manner as substations described in section 3.1. Thus, their MANA models are equivalent voltages sources behind subtransient impedances. The connection, the mutual coupling, the grounding impedances and the pre-fault currents constitute the main differences with the substation case.

3.4.1. Synchronous Machines

Synchronous machines can be divided into two groups: synchronous generators and synchronous motors. Their MANA models are the same. Three connections can be found using those types of machines: Yg, Y and Delta. Their nameplate impedances are generally in sequence or in direct/quadrature axis data derived from equivalent circuits. Furthermore, Z_1 is generally not equal to Z_2. Considering the sequence impedance, the following equations are used to convert into phase domain:

$$\boldsymbol{Z_{gen}} = \frac{1}{3}\begin{bmatrix}1 & 1 & 1\\ 1 & a^2 & a\\ 1 & a & a^2\end{bmatrix}\begin{bmatrix}Z_0 & 0 & 0\\ 0 & Z_1 & 0\\ 0 & 0 & Z_2\end{bmatrix}\begin{bmatrix}1 & 1 & 1\\ 1 & a & a^2\\ 1 & a^2 & a\end{bmatrix} \tag{3.27}$$

where:

$a = 1\angle 120°$

The phase matrix is a cyclic matrix of the form:

$$\boldsymbol{Z_{gen}} = \begin{bmatrix}Z_x & Z_y & Z_z\\ Z_z & Z_x & Z_y\\ Z_y & Z_z & Z_x\end{bmatrix} \tag{3.28}$$

This matrix is one of the only few that cause an unsymmetrical impedance matrix. This fact has an impact on the selection of the mathematical linear algebra solver.

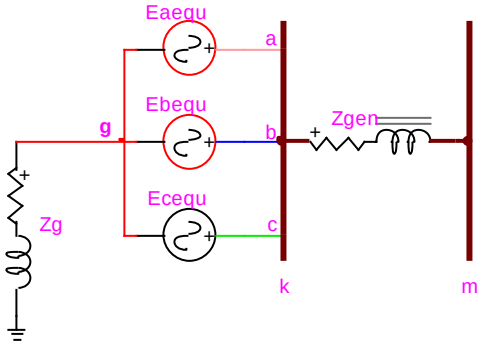


Figure 3-12: Yg Synchronous Machine Model

Based on equations (3.5) and (3.6), following this notation, the general model for Yg machine shown in Figure 3-12 is:

g : index of node g (internal)

k_i : index of node k, i = a, b, c for phase ABC (internal)

m_i : index of node m, i = a, b ,c for phase ABC

q_i : general index, i = 1,2,3…represents the number of single elements

$\boldsymbol{Y_n}$ is a 7 x7 matrix:

$$\boldsymbol{Y_n} = \begin{bmatrix} Y_g & \mathbf{0} \\ \mathbf{0} & \boldsymbol{Y_{coupled}} \end{bmatrix} \tag{3.29}$$

where:

$$Y_g = Z_g^{-1} \tag{3.30}$$

In a detailed format:

$$\boldsymbol{Y_n} = \begin{bmatrix} & g & k_a & k_b & k_c & m_a & m_b & m_c \\ g & Y_g & 0 & 0 & 0 & 0 & 0 & 0 \\ k_a & 0 & Y_x & Y_y & Y_z & -Y_x & -Y_y & -Y_z \\ k_b & 0 & Y_z & Y_x & Y_y & -Y_z & -Y_x & -Y_y \\ k_c & 0 & Y_y & Y_z & Y_x & -Y_y & -Y_z & -Y_x \\ m_a & 0 & -Y_x & -Y_y & -Y_z & Y_x & Y_y & Y_z \\ m_b & 0 & -Y_z & -Y_x & -Y_y & Y_z & Y_x & Y_y \\ m_c & 0 & -Y_y & -Y_z & -Y_x & Y_y & Y_z & Y_x \end{bmatrix} \tag{3.31}$$

$\boldsymbol{V_c}$ is a 7 x3 matrix:

$$\boldsymbol{V_c} = \begin{bmatrix} & q_1 & q_2 & q_3 \\ g & -1 & -1 & -1 \\ k_a & 1 & 0 & 0 \\ k_b & 0 & 1 & 0 \\ k_c & 0 & 0 & 1 \\ m_a & 0 & 0 & 0 \\ m_b & 0 & 0 & 0 \\ m_c & 0 & 0 & 0 \end{bmatrix} \tag{3.32}$$

$\boldsymbol{V_b}$ is a 3 x1 vector:

$$\boldsymbol{V_b} = \begin{bmatrix} & 1 \\ q_1 & E_{aequ} \\ q_2 & E_{bequ} \\ q_3 & E_{cequ} \end{bmatrix} \tag{3.33}$$

Similar MANA models are derived for Y and Delta connections shown in Figure 3-13 and Figure 3-14

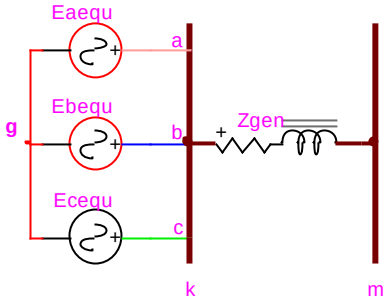


Figure 3-13: Y Synchronous Machine Model

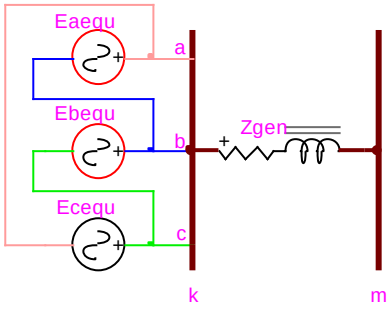


Figure 3-14: Delta Synchronous Machine Model

The main difference between the motor and the generator will be in the calculation of the equivalent internal voltages. Those voltages are based on the pre-fault conditions and can be calculated using a Load Flow analysis. Since generators are power delivering elements and the motor power consuming elements, the currents will not have the same angle, thus will not result in the same equivalent voltages. The general equation is:

$$\boldsymbol{E_{equ} = E_{LF} + Z_{gen} I_{LF}} \quad (3.34)$$

where:

$\boldsymbol{E_{LF}}$: Load Flow phase voltages at machine location

$\boldsymbol{I_{LF}}$: Load Flow phase currents at machine location

3.4.1. Induction Machines

The three-phase induction machine model is based on its equivalent single phase circuit shown in Figure 3-15 which takes into consideration winding power losses (R_s, R_r), leakage reactance (X_s, X_r), hysteresis and eddy current losses (R_m) within the core, reactive power losses (X_m) and operating slip (s). It has been modeled as a Y or Delta synchronous machine with the following modifications: the internal impedance has no coupling effect, thus only self impedance that is equal to the subtransient impedance derived from its equivalent circuit

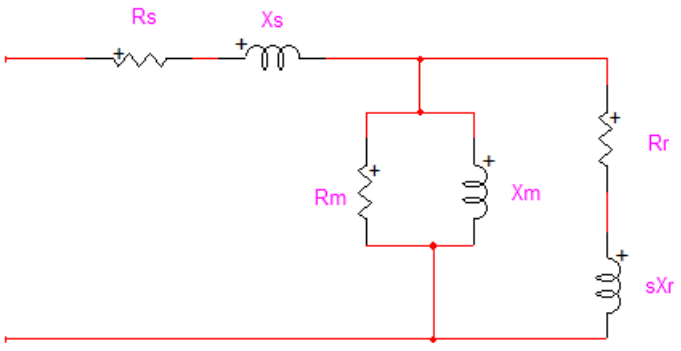


Figure 3-15: Induction Machine Equivalent Circuit

3.5.Switching and Protective Devices

Protecting civilians and workers is one of the most important objectives when designing electrical systems. Switching and protective devices are largely used in the distribution system. Such devices are generally considered as zero impedance elements since there are present to protect the system and not to interfere with the power flow. Removing those devices prior to

running a short-circuit analysis can be cumbersome. For arc-flash and protection and coordination analysis, evaluating the currents at those protective devices is necessary to properly select ratings. Common devices used in distribution systems are:

- Main protection: reclosers, relays, breaker, fuses
- Main switching devices: switches, sectionalizer, switchgear
- Other: instrument transformers such as current transformers (CTs), potential transformers (PTs) and network protector

For a switching device or protective device connected between two arbitrary nodes k and m, when if the switch is closed, it is needed to use a 1 in row *k* and a –1 in row m of the switch equation line in $\boldsymbol{S_c}$. For the switch numbered q_i in the list of switches for *n* phase devices:

$$\boldsymbol{S_c}(k, q_i) = \quad 1 \tag{3.35}$$

$$\boldsymbol{S_c}(m, q_i) = -1 \tag{3.36}$$

$$\boldsymbol{S_d}(q_i, q_i) = \quad 0 \tag{3.37}$$

If the switch is open:

$$\boldsymbol{S_c}(k, q_i) = \quad 0 \tag{3.38}$$

$$\boldsymbol{S_c}(m, q_i) = 0 \tag{3.39}$$

$$\boldsymbol{S_d}(q_i, q_i) = \quad 1 \tag{3.40}$$

For example, considering a 3 phase switch between the nodes *k* and *m* presented in Figure 3-16, when phases A and B are closed and C is open:

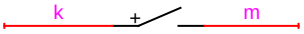


Figure 3-16: Switching and Protective Devices Model\

$\boldsymbol{S_c}$ is a 6 x3 matrix:

$$\boldsymbol{S_c} = \begin{bmatrix} & q_a & q_b & q_c \\ k_a & 1 & 0 & 0 \\ k_b & 0 & 1 & 0 \\ k_c & 0 & 0 & 0 \\ m_a & -1 & 0 & 0 \\ m_b & 0 & -1 & 0 \\ m_c & 0 & 0 & 0 \end{bmatrix} \tag{3.41}$$

$\boldsymbol{S_d}$ is a 3 x3 matrix:

$$\boldsymbol{S_d} = \begin{bmatrix} & q_a & q_b & q_c \\ q_a & 0 & 0 & 0 \\ q_b & 0 & 0 & 0 \\ q_c & 0 & 0 & 1 \end{bmatrix} \tag{3.42}$$

3.6.Lines and Cables

An overhead line impedance matrix can be computed using Carson's equations [31]. Earth can be modeled as an infinite, uniform solid with a flat uniform upper surface and a constant resistivity. Any end effects introduced at the neutral grounding points are not large at power frequencies, and are therefore neglected [4][5][32]. This method is valid for low frequency systems and is mostly used in distribution systems. Conductor's geometrical mean radius (GMR) and diameter are used as parameters.

Earth can be also modeled as a complex ground return plane. The model was initially proposed to approximate Carson's infinite series equation for the whole range of frequencies and

for the multi-layer ground returns [33]. Conductor's internal diameter and external diameter are used instead of the GMR.

A cable impedance matrix can be computed in a similar fashion. The calculation may differ depending on the type of cable. Typical cables types are multi-wire concentric neutral, shielded and unshielded cables. Most calculation can be found in the same literature as for overhead lines.

The shunt admittance calculation for overhead lines is different for cables since they are unshielded conductors. The shunt admittance matrix for overhead line is calculated using the method of images describe in most references [5][32]. When calculating the shunt admittance matrix of the cables, the dielectric constant, the internal insulation radius and the internal sheath radius must be considered.

Traditional three phase conductors and one neutral are found in most distribution systems, resulting into a 4 x 4 matrix. Assuming a multi-wire neutral, the Kron reduction method reduces the matrix into a 3 x 3 matrix. The detailed model can be shown in Figure 3-17.

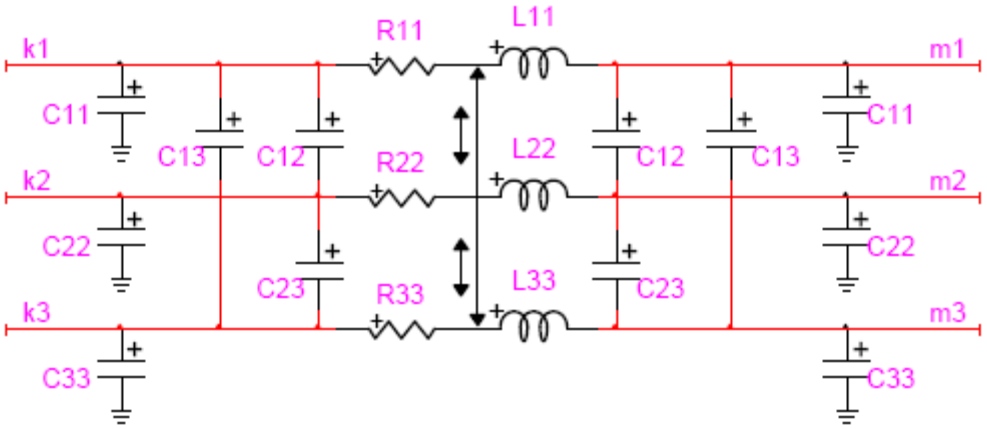


Figure 3-17: Detailed Line Model

Given the impedance matrix of the line or cable, we can compute the admittance matrix:

$$\boldsymbol{Y_{serie}} = \begin{bmatrix} Z_{aa} & Z_{ab} & Z_{ac} \\ Z_{ba} & Z_{bb} & Z_{bc} \\ Z_{ca} & Z_{cb} & Z_{cc} \end{bmatrix}^{-1} = \begin{bmatrix} Ys_{aa} & Ys_{ab} & Ys_{ac} \\ Ys_{ba} & Ys_{bb} & Ys_{bc} \\ Ys_{ca} & Ys_{cb} & Ys_{cc} \end{bmatrix} \quad (3.43)$$

Given the shunt admittance matrix representing the line charging, the MANA format can be

determined.

$$\boldsymbol{Y_{shunt}} = \begin{bmatrix} Ysh_{aa} & Ysh_{ba} & Ysh_{ac} \\ Ysh_{ba} & Ysh_{bb} & Ysh_{bc} \\ Ysh_{ca} & Ysh_{cb} & Ysh_{cc} \end{bmatrix} \tag{3.44}$$

Following this notation, we find:

k_i : node *k* on phase i = a,b,c

m_i : node *m* on phase i = a,b,c

$\boldsymbol{Y_n}$ is a 2n x 2n matrix for n phase line:

$$\boldsymbol{Y_n} = \begin{bmatrix} \boldsymbol{Y_{kk}} & \boldsymbol{Y_{km}} \\ \boldsymbol{Y_{mk}} & \boldsymbol{Y_{mm}} \end{bmatrix} \tag{3.45}$$

where:

$$\boldsymbol{Y_{kk}} = \boldsymbol{Y_{serie}} + \frac{\boldsymbol{Y_{shunt}}}{\mathbf{2}} \tag{3.46}$$

$$\boldsymbol{Y_{mm}} = \boldsymbol{Y_{kk}} \tag{3.47}$$

$$\boldsymbol{Y_{km}} = -\boldsymbol{Y_{serie}} \tag{3.48}$$

$$\boldsymbol{Y_{mk}} = \boldsymbol{Y_{km}} \tag{3.49}$$

For example, considering a 3 phase line between the nodes *k* and *m*, the contribution into the $\boldsymbol{Y_n}$ matrix is a 6 x 6 matrix formed of four 3 x 3 matrices which the 2 distinct matrices are.

$$\boldsymbol{Y_{kk}} = \begin{bmatrix} & k_a & k_b & k_c \\ k_a & Ys_{aa} + \frac{Ysh_{aa}}{2} & Ys_{ab} + \frac{Ysh_{ab}}{2} & Ys_{ac} + \frac{Ysh_{ac}}{2} \\ k_b & Ys_{ab} + \frac{Ysh_{ab}}{2} & Ys_{bb} + \frac{Ysh_{bb}}{2} & Ys_{bc} + \frac{Ysh_{bc}}{2} \\ k_c & Ys_{ca} + \frac{Ysh_{ca}}{2} & Ys_{cb} + \frac{Ysh_{cb}}{2} & Ys_{cc} + \frac{Ysh_{cc}}{2} \end{bmatrix} \tag{3.50}$$

and

$$\boldsymbol{Y_{km}} = \begin{bmatrix} & m_a & m_b & m_c \\ k & -Ys_{aa} & -Ys_{ab} & -Ys_{ac} \\ k_b & -Ys_{ba} & -Ys_{bb} & -Ys_{bc} \\ k_c & -Ys_{ca} & -Ys_{cb} & -Ys_{cc} \end{bmatrix} \tag{3.51}$$

3.7. Electronically Coupled Generators

The electronically coupled generators (ECG) can be modeled like the synchronous generators but with Z_2 considered as infinite. This model is really an approximation for the representation of different models. It is not the purpose of this document to elaborate models for the ECG. The reader interested in ECG models based on different configurations and control schemes can refer to [34]-[36]. Nevertheless, the modeling of ECG will require additional efforts to represent the particularity of power electronics. The development of models for the ECG is subject to further research.

3.8. Other Devices

Other devices that compose the distribution system can me modeled in a similar fashion:

- Shunt and series capacitors and reactors
- Spot and distributed loads
- Harmonic filters
- Grounding transformers
- Two-Winding and three-winding autotransformers

CHAPTER 4. SPARSE MATRIX SOLVER

4.1. Overview

Solving equation (2.2) to compute the short-circuit currents can become very time consuming if inappropriate tools are used in the numerical solution process. The first observation is that the matrix form for the MANA method is a structurally unsymmetrical sparse matrix with complex values. A sparse matrix contains primarily a very large number of zeros in its elements. Methods to solve sparse linear equations can be classified under two categories:

1. Direct methods
2. Indirect or iterative methods

Furthermore, when selecting a solver, other considerations should be based on the following criteria:

- Ability to solve unsymmetrical sparse matrix with complex values
- Performance of main features (e.g. factorization)
- Memory management (e.g. in core or out core)
- Interfacing simplicity
- Supported by development group

In March 2009, a list of available software for solving sparse linear systems via direct methods was published in [37]. The name of the packages, the type of factorization (e.g. LU, Cholesky), type of supported matrices (e.g. unsymmetrical, Hermitian) and other important information is detailed for more than 40 packages. To assist in finding the proper solver, the Council for the Central Laboratory of the Research Councils (CCLRC) from the United Kingdom has performed a numerical evaluation of sparse direct solvers [38].

After consulting both reports, two solvers have been selected based on the above criteria list:

1. Intel MKL PARDISO
2. KLU

Consider the linear set of equations on a matrix format equation (4.1). This linear system can represent equation (2.2).

$$\boldsymbol{Ax = b} \tag{4.1}$$

To focus on the type of matrix found in power systems, let's recall the matrix attributes for the linear system below:

Table 4-1: General Attributes of Matrix A

Attributes of A	**Justification**
Sparse	Matrix contains primarily zero values
Square	n x n matrix
Complex	Matrix elements are complex numbers
Structurally symmetric*	If $a_{i,j} \neq 0$, then $a_{j,i} \neq 0$ for all *i* and *j*

*Note that if ($a_{i,j} = a_{ji}$). for all *i* and *j*, the matrix is only structurally symmetric. A symmetric matrix for complex values must be Hermitian ($a_{i,j} = \bar{a}_{ji}$).

Before starting with the description of the two solvers, a brief review of sparse linear equation direct method solving techniques is presented here based on [39].

4.2.Sparse Linear Equation-Direct Methods

There are two main steps in solving the system:

1. Factorization

2. Forward and backward substitution

However, for performance and accuracy issues, a pre and post-treatment are sometimes necessary depending on the nature of the matrix:

1. Pre-Treatment: Permutation, reordering and scaling

2. Post-Treatment: Iterative refinement

An overview of each step is presented below.

4.2.1. Pre-Treatment: Permutation, Reordering and Scaling

Consider a sparse matrix A with a density plot shown in Figure 4-1. A total of 84 non-zeros elements are present.

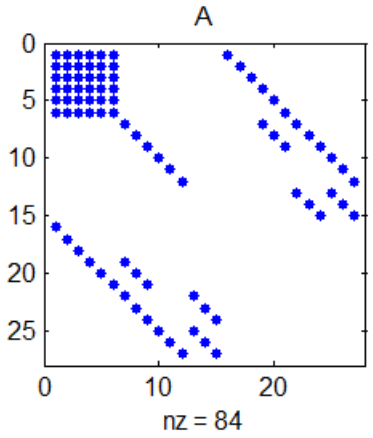


Figure 4-1: Density Plot of Matrix A

Performing a LU factorization on this matrix will result into a total of 198 non-zero elements as shown in Figure 4-2. Since there is a direct link between the number of non-zero elements and the computational time, there is an interest in finding a fill-reducing ordering scheme.

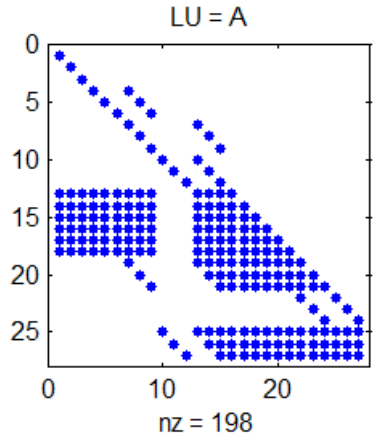


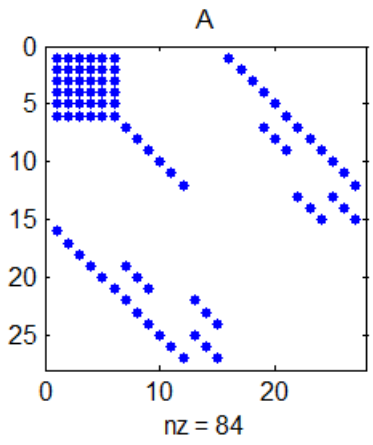
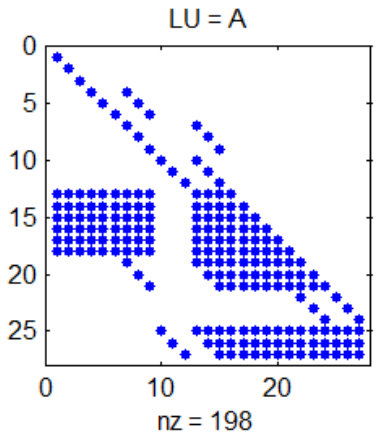
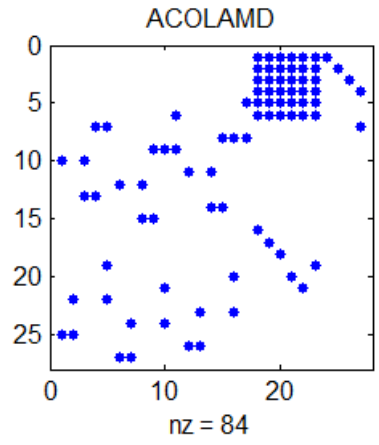
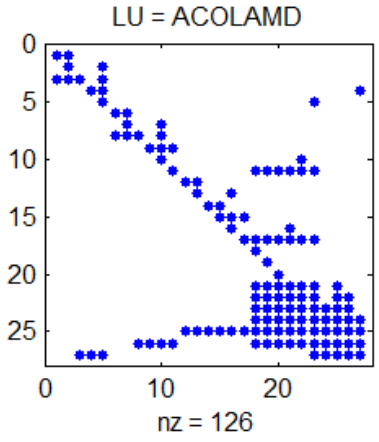
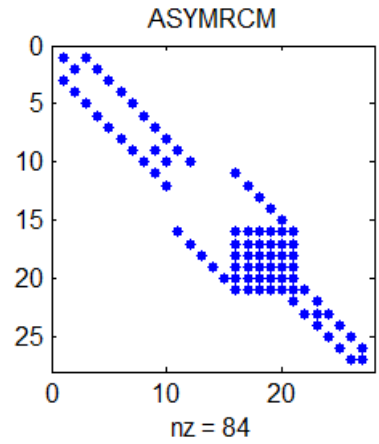
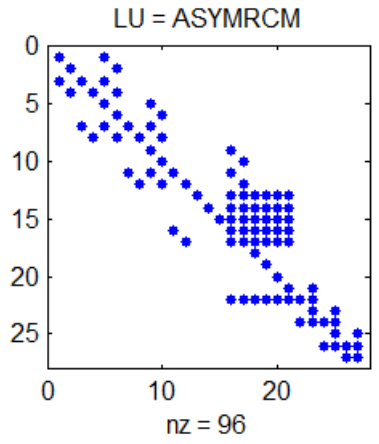
Figure 4-2: Density Plot of Matrix A=LU

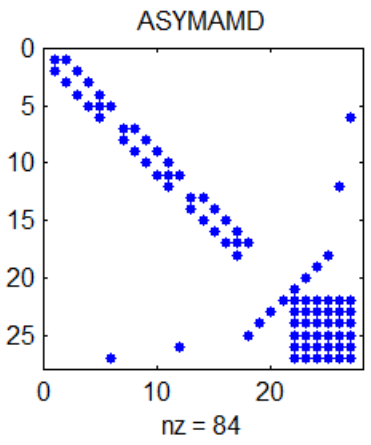
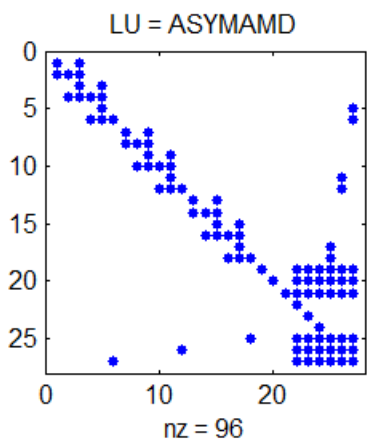
Linear software solvers contain multiple permutation algorithms to reduce the filling in a factorized matrix. For example, Matlab [40] offers multiple functions:

- colamd : Non Symmetric approximate minimum degree
- symamd : Symmetric approximate minimum degree
- symrcm : Reverse Cuthill-Mckee

Table 4-2 presents the effects of using those permutation techniques on the above matrix.

Table 4-2: Permutation Techniques

Technique	Density Plot	Density plot of LU	Solve
No Permutation			t=0.43s
COLAMD			t=0.39s
SYMRCM			t=0.32s

SYMAMD			t=0.34s

The table demonstrates the effect of permutations and the impact on the forward/backward substation step (Solve column) computing time.

Mathematicians have recently pursued the challenge to find the most optimal permutation techniques based on electrical circuit matrices that have unique characteristics [41]. The results of this research lead to the block triangular form (BTF) permutation algorithm used in the KLU solver.

The scaling process consists of multiplying the original matrix by two diagonal matrices. The norm of the matrix is then not modified. The scaling can be done to rows or columns. The objective of the scaling algorithm is to improve (i.e., reduce) the condition number of the matrix [42]. The final system of equations is represented as:

$$(\mathbf{PRAQ})\boldsymbol{Q^T x} = \mathbf{PR}\boldsymbol{b} \qquad (4.2)$$

where:

P : Row permutation matrix

R : Scaling matrix

Q : Column permutation matrix

4.2.2. Factorization

The factorization step is the decomposition of the matrix into a canonical form (standard form) in the objective of reducing the number of operations for the next steps of the solving process. Table 4-2 presents a summary of standard factorizations methods for square complex matrices.

Table 4-3: Factorization Methods for Square Complex Matrices

Matrix Structure	**Factorization**	**Matrix Representation**
Hermitian (Symmetric), Positive Definite	Cholesky	$\boldsymbol{A = U^T U}$ $\boldsymbol{A = LL^T}$
Hermitian (Symmetric), Indefinite	LDL'	$\boldsymbol{A = LDL'}$
Structurally Symmetric or Unsymmetric	LU	$\boldsymbol{A = LU}$

The factorization is done in two steps: symbolic factorization and numerical factorization. The first step determines the non-zero structure and prepares the data for the numerical factorization. The second step computes the factorization sub-matrices (e.g. L and U).

During the process of performing numerical factorization, some solvers can perform pivoting perturbation strategies when they cannot factorize super-nodes [39]. It then replaces near zero value pivots to a value proportional to the machine precision, typically called epsilon (ε). This technique can then solve under rank systems of equations encountered in ungrounded systems (e.g. Delta systems). Without this process, the solver cannot solve the linear system or provides an inaccurate solution caused by an ill-conditioned matrix.

4.2.3. Forward and Backward Substitution

Solving equation (4.1) using LU factorization decomposes the matrix into two matrices:

$$\boldsymbol{LUx = b} \tag{4.3}$$

where:

$$\boldsymbol{L} = \begin{bmatrix} l_{11} & 0 & \cdots & 0 \\ l_{21} & l_{22} & & 0 \\ \vdots & & \ddots & \vdots \\ l_{n1} & l_{n2} & \cdots & l_{nn} \end{bmatrix} \tag{4.4}$$

$$\boldsymbol{U} = \begin{bmatrix} u_{11} & u_{12} & \cdots & u_{1n} \\ 0 & u_{22} & & u_{2n} \\ \vdots & & \ddots & \vdots \\ 0 & 0 & \cdots & u_{nn} \end{bmatrix} \tag{4.5}$$

Solving the system is done in two steps:

$$\boldsymbol{Ly} = \boldsymbol{b} \tag{4.6}$$

$$\boldsymbol{Ux} = \boldsymbol{y} \tag{4.7}$$

The forward substitution is the process of solving the first step, equation (4.6). The backward substitution is the process of solving the second step, equation (4.7). Some solvers [37] provide parallel forward/backward substitution solving, which in some case might be faster than sequential solving.

4.2.4. Post-Treatment: Iterative Refinement

The iterative refinement is done in the forward/backward substitution step. Solvers using pivoting perturbation strategies find approximate solutions and measure the error produced by such replacement. An iterative process is used to correct the solution and find an accurate solution.

4.3.MKL PARDISO

The Intel MKL Parallel direct solver (PARDISO) is based on the PARDISO solver [42]. It provides functions to solve real or complex, symmetric, structurally symmetric or non-symmetric, positive definite, indefinite or Hermitian sparse linear system of equations. It utilizes Intel MKL BLAS and LAPACK library and uses shared-memory parallelism to improve numerical

factorization performance. It has some reordering, permutation and scaling capabilities to reduce non-zero elements in matrix A. It uses symbolic and numerical factorization based on the type of matrix (e.g. LU method for unsymmetrical matrices). It has the capability to solve multi-right hand side systems. One of the main distinctions between other solvers is the boosting of ill-conditioned matrices and a small pivot perturbation technique built in the solver. An iterative refinement is used to reduce the error factor in the presence of ill-conditioned and under rank matrices.

The solver was selected for its flexibility and its capability to solve under ranked matrix systems (e.g. delta systems). This is being done with the pivot perturbation technique that is being done during the solving process. Hence, no pre-treatment is necessary to handle under ranked systems. Such pre-treatment consists of manually integrating a small perturbation (e.g. ε = j1e-10) on the diagonal elements of the $\boldsymbol{A}$ matrix. This modification is equivalent of placing small reactive elements on the system, hence representing line charging effect due to capacitive effect between the system components and the earth. This is true for the $\boldsymbol{Y_n}$ part of the matrix. For the other sub-matrices of matrix $\boldsymbol{A}$, it has no physical explanation should only be seen as a mathematical strategy.

4.4.KLU

KLU is another sparse linear system solver [41]. Its particularity is the upper block triangular form permutation taking advantage of the structure of power systems. It has been initially designed for the Simulation Program with Integrated Circuit Emphasis (SPICE) [43] engine used for electronic circuit simulations. This solver is also integrated into the OPEN-DSS [44] simulation software developed by the Electric Power Research Institute (EPRI).

The solver was selected for its main features and for its permutation method adapted to power system. When using this solver, manual pivot perturbation is required in order to correct and solve rank deficient systems.

CHAPTER 5. MANA SHORT-CIRCUIT ALGORITHM

5.1.MANA Fault Models

5.1.1. Shunt Fault

When using the MANA method, faults are represented by ideal switches. This section gives the matrices needed to compute the usual 5 fault types: single line-to-ground (LG), three-phase (LLL), line-to-line (LL), double line-to-ground (LLG) and three-phase to ground (LLLG) faults. Only sub matrices $\boldsymbol{S_c}$ and $\boldsymbol{S_d}$ need to be modified to insert fault equations. The same could have been done by modifying the $\boldsymbol{Y_n}$ matrix, but that is time consuming and requires lengthy manipulations. The idea is to apply a fault to the existing network without manipulating or renumbering the existing A matrix. Fault impedances Z_f and Z_g will be represented following the standards shown in Figure 5-1

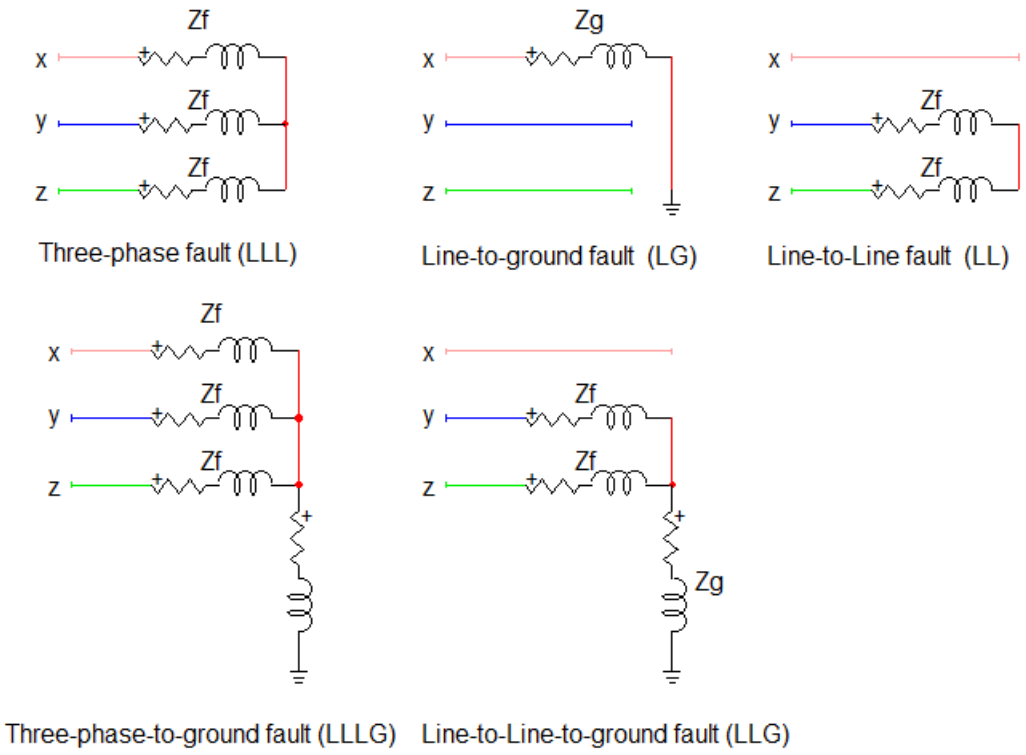


Figure 5-1: Shunt Fault Representation with Impedance

In the following models, faulted buses will be named *x, y, z*. They can be afterwards associated with phases *a, b, c* in the desired order. This is done to show that the fault can be easily

applied on any phase(s), which greatly extends the capabilities of packages based on symmetrical components. The least amount possible number of switches is used to build the smallest matrices possible. Finally, the equations below also work if one or both impedances are zero.

The MANA LG fault model can be represented in Figure 5-2:

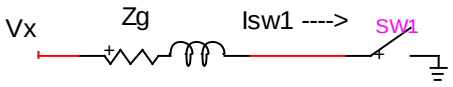


Figure 5-2: MANA LG Fault Model

A LG fault on bus *x* requires the following equation to be true:

$$V_x - Z_g \cdot I_{SW1} = 0 \tag{5.1}$$

Following this notation, we find:

k_i : faulted node on phase i = x and y

q_i : general index, i = 1,2,3…represents the number of single elements

$$\boldsymbol{S_c} = \begin{bmatrix} & q_1 \\ k_x & 1 \end{bmatrix} \tag{5.2}$$

$$\boldsymbol{S_z} = \begin{bmatrix} & q_1 \\ q_1 & -Z_g \end{bmatrix} \tag{5.3}$$

Fault current I_x will be equal to I_{SW1}.

The MANA LL fault model can be represented using Figure 5-3:

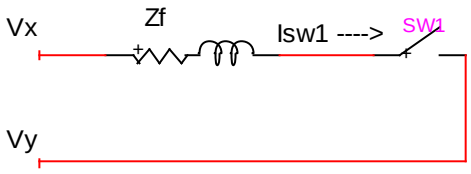


Figure 5-3 MANA LL Fault Model

A LL fault between buses *x* and *y* requires the following equation to be true:

$$V_x - Z_f \cdot I_{SW1} - V_y = 0 \tag{5.4}$$

Following this notation, we find:

k_i : faulted node on phase i = x and y

q_i : general index, i = 1,2,3…represents the number of single elements

$$\boldsymbol{S_c} = \begin{bmatrix} & q_1 \\ k_x & 1 \\ k_y & -1 \end{bmatrix} \tag{5.5}$$

$$\boldsymbol{S_d} = \begin{bmatrix} & q_1 \\ q_1 & -Z_f \end{bmatrix} \tag{5.6}$$

Fault currents $I_x = I_{SW1}$ and $I_y = -I_{SW1}$.

The MANA LLL fault model is shown in Figure 5-4.

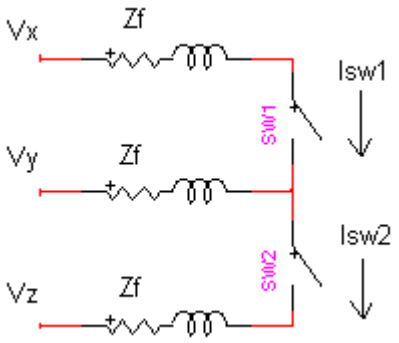


Figure 5-4 MANA LLL Fault Model

A LLL fault between nodes *x*, *y* and *z* requires the following equations to be true:

$$V_x - V_y - (2Z_f \cdot I_{SW1}) + (Z_f \cdot I_{SW2}) = 0 \tag{5.7}$$

$$V_y - V_z - (2Z_f \cdot I_{SW2}) + (Z_f \cdot I_{SW1}) = 0 \tag{5.8}$$

Following this notation, we find:

k_i : faulted node on phase i = x, y

q_i : general index, i = 1,2,3…represents the number of single elements

$$\boldsymbol{S_c} = \begin{bmatrix} & q_1 & q_2 \\ k_x & 1 & 0 \\ k_y & -1 & 1 \\ k_z & 0 & -1 \end{bmatrix} \tag{5.9}$$

$$\boldsymbol{S_d} = \begin{bmatrix} & q_1 & q_2 \\ q_1 & -2Z_f & Z_f \\ q_2 & Z_f & -2Z_f \end{bmatrix} \tag{5.10}$$

Fault currents $I_x = I_{SW1}$, $I_y = (-I_{SW1} + I_{SW2})$ and $I_z = -I_{SW2}$.

The MANA LLG fault model can be represented using Figure 5-5:

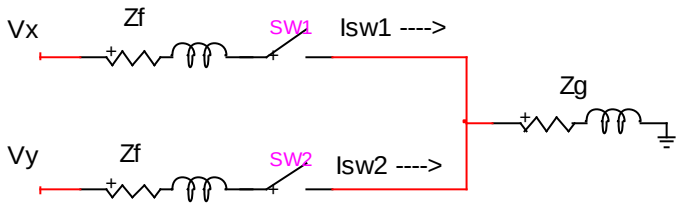


Figure 5-5 MANA LLG Fault Model

A LLG fault between buses *x* and *y* requires the following equations to be true:

$$V_x - (Z_f + Z_g) \cdot I_{SW1} - Z_g \cdot I_{SW2} = 0 \tag{5.11}$$

$$V_y - (Z_f + Z_g) \cdot I_{SW2} - Z_g \cdot I_{SW1} = 0 \tag{5.12}$$

Following this notation, we find:

k_i : faulted node on phase i = x, y

q_i : general index, i = 1,2,3…represents the number of single elements

$$\boldsymbol{S_c} = \begin{bmatrix} & q_1 & q_2 \\ k_x & 1 & 0 \\ k_y & 0 & 1 \end{bmatrix} \tag{5.13}$$

$$\boldsymbol{S_d} = \begin{bmatrix} & q_1 & q_2 \\ q_1 & -Z_f - Z_g & -Z_g \\ q_2 & -Z_g & -Z_f - Z_g \end{bmatrix} \tag{5.14}$$

Fault currents $I_x = I_{SW1}$ and $I_y = I_{SW2}$.

The MANA LLLG fault model can be represented using Figure 5-6:

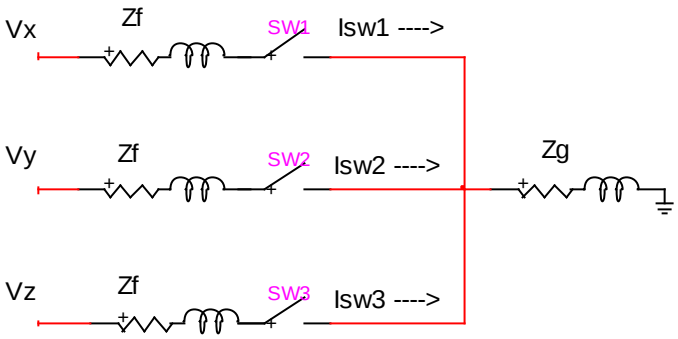


Figure 5-6 MANA LLLG Fault Model

A LLLG fault on bus *x*, *y* and *z* requires the following equations to be true:

$$V_x - (Z_f \cdot I_{SW1}) - Z_g(I_{SW1} + I_{SW2} + I_{SW3}) = 0 \tag{5.15}$$

$$V_y - (Z_f \cdot I_{SW2}) - Z_g(I_{SW1} + I_{SW2} + I_{SW3}) = 0 \tag{5.16}$$

$$V_z - (Z_f \cdot I_{SW3}) - Z_g(I_{SW1} + I_{SW2} + I_{SW3}) = 0 \tag{5.17}$$

Following this notation, we find:

k_i : faulted node on phase i = x, y, z

q_i : general index, i = 1,2,3…represents the number of single elements

$$\boldsymbol{S_c} = \begin{bmatrix} & q_1 & q_2 & q_3 \\ k_x & 1 & 0 & 0 \\ k_y & 0 & 1 & 0 \\ k_z & 0 & 0 & 1 \end{bmatrix} \tag{5.18}$$

$$\boldsymbol{S_d} = \begin{bmatrix} & q_1 & q_2 & q_3 \\ q_1 & -Z_f - Z_g & -Z_g & -Z_g \\ q_2 & -Z_g & -Z_f - Z_g & -Z_g \\ q_3 & -Z_g & -Z_g & -Z_f - Z_g \end{bmatrix} \tag{5.19}$$

Fault currents $I_x = I_{SW1}$, $I_y = I_{SW2}$ and $I_z = I_{SW3}$.

5.1.2. Series Fault

The series fault arises in the distribution system when a deficient contact or connection occurs. It can also be related to the opening action of a breaker based on inappropriate protection relay behavior. They can lead to the formation of electric arcs at the fault location [45].

There are three types of series faults: 1-phase open, 2 phases open and asymmetrical impedances series fault, also known as unequal series impedance fault. Series faults are traditionally handled in a cumbersome matter with complex Thevenin equivalents [4]. The MANA method has a relatively simple way of handling such faults by applying a small modification to original matrix formulation. In this document the models are represented for a three-phase line neglecting shunt capacitive component since the overhead lines are considered relatively short for distribution systems.

When studying a series fault, three sets of data are relevant:

- Series fault impedance: Z_a, Z_b and Z_c
- Type of fault: 1-phase open (a, b or c), 2 phases open (a-b, b-c, c-a) or asymmetrical impedances series fault
- Location of the fault l on the line

The one-phase open fault on phase x of line o connected between nodes m and n shown in Figure 5-7 can be represented schematically as:

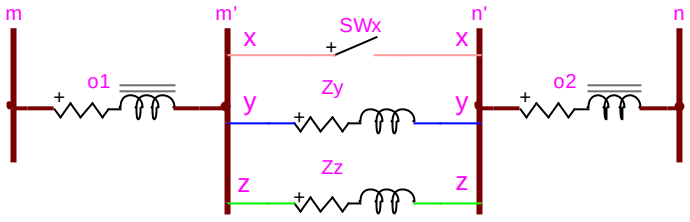


Figure 5-7: One-Phase Open Fault on Phase x

The original impedance matrix of line *o* is:

$$\boldsymbol{Z_o} = \begin{bmatrix} Z_{aa} & Z_{ab} & Z_{ac} \\ Z_{ba} & Z_{bb} & Z_{bc} \\ Z_{ca} & Z_{cb} & Z_{cc} \end{bmatrix} \tag{5.20}$$

If l = 0, then closed switches are added between *m* and *m'*, whereas if l = 1, closed switches are added between *n* and *n'*. The impedance matrices of the two equivalent lines become:

$$\boldsymbol{Z_{o1}} = l \cdot \boldsymbol{Z_o} \tag{5.21}$$

$$\boldsymbol{Z_{o1}} = (1 - l) \cdot \boldsymbol{Z_o} \tag{5.22}$$

The switch on phase *x* between *m'* and *n'* is open, whereas Z_y and Z_z are the fault impedances. If Z_y and/or Z_z are 0, they are replaced by closed switches.

The two-phase open fault on phases *x* and *y* of line *o* connected between nodes *m* and *n* can be represented schematically as in Figure 5-8:

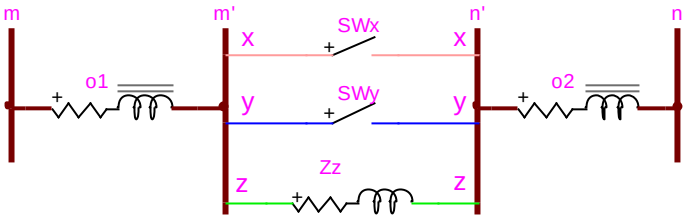


Figure 5-8: Two-Phase Open Fault on Phase x and y

The switches on phases *x* and *y* between *m'* and *n'* are open, whereas Z_z is the fault impedance. If Z_z is 0, it is replaced by a closed switch.

The asymmetrical fault impedance on line *o* connected between nodes *m* and *n* shown in Figure 5-9 can be represented schematically as:

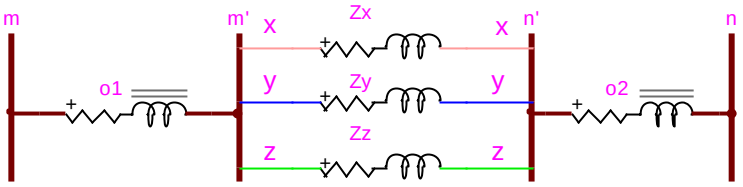


Figure 5-9: Asymmetrical Series Fault on Phase x, y and z

Z_x, Z_y and Z_z are the fault impedances. If Z_x Z_y and/or Z_z are 0, they are replaced by closed switches.

Assuming that the ***A*** matrix of the original network has already been built, it is possible to modify a few of its sub matrices, specifically parts of $\boldsymbol{Y_n}$ and $\boldsymbol{S_c}$/$\mathbf{S_d}$, in order to simulate a series fault.

5.1.3. Simultaneous Faults

The simultaneous fault is the event of multiple faults occurring simultaneously. Such events can occur naturally by accidental operator manipulations. Usually, only two simultaneous faults are studied for practical reasons; the joint probability of multiple faults occurring at the same time is inversely proportional to the number of faults [4].

The MANA method does not have any limitations for any combination of shunt and series faults. Hence, the traditional cases of interest can be handled for faults occurring at arbitrary locations A and B:

- Shunt fault at A and shunt fault at B
- Shunt fault at A and series fault at B
- Series fault at A and series fault at B
- Series fault at A and shunt fault at B

While only two simultaneous faults are generally studied, the MANA method can model a large number of faults by inserting impedance fault models into the MANA matrices.

5.2. Short-Circuit Algorithm

When performing a short-circuit analysis for planning purposes, many assumptions are made. Those assumptions are generally used to facilitate the data collections and are based on nominal or typical system values (e.g. LTC are at nominal taps). Typical assumptions are [5]:

1- Only subtransient fault current is considered;

2- All non-rotating impedance loads are neglected. Hence, power loads, shunt capacitors and line charging effects are neglected;

3- Machines and DGs pre-fault currents are neglected and represented as constant source voltages behind sub transient impedances;

4- Nominal voltages are set at each bus (e.g. 1 p.u.);

5- Transformers and regulators are set at nominal tap;

When performing a short-circuit analysis in a quasi-real time simulation or for operations, for example in a Distribution Management System (DMS), pre-fault currents provided from passive and active elements should not be neglected [23]. Hence, prior to running the short-circuit analysis, a load flow analysis is performed to compute network voltages and pre-fault currents. Internal voltages for substations and machines are calculated to take into consideration pre-fault contributions. Power loads, shunt capacitors and line charging effects as taken into account in the prior load flow and in the MANA models. For this type of analysis, the convergence and execution time are important aspects.

5.2.1. Fault Flow Algorithm

The Fault Flow analysis is the process of analyzing one or multiple faults on selected buses and observe fault contributions on network sections. For this type of analysis, critical buses are selected and contributions, such as protective devices, generators and sources are observed as points of interest. The algorithm presented below is suitable for shunt, series and simultaneous fault analysis. This type of analysis is generally used when specific nodes/buses needs to be

analyzed and not necessarily the entire network. For example, the following software analyses module uses a fault flow algorithm: Arc Flash, Minimum Fault, Protection & Coordination and Transient Stability analysis [46]. The general algorithm is presented in the Figure 5-10.

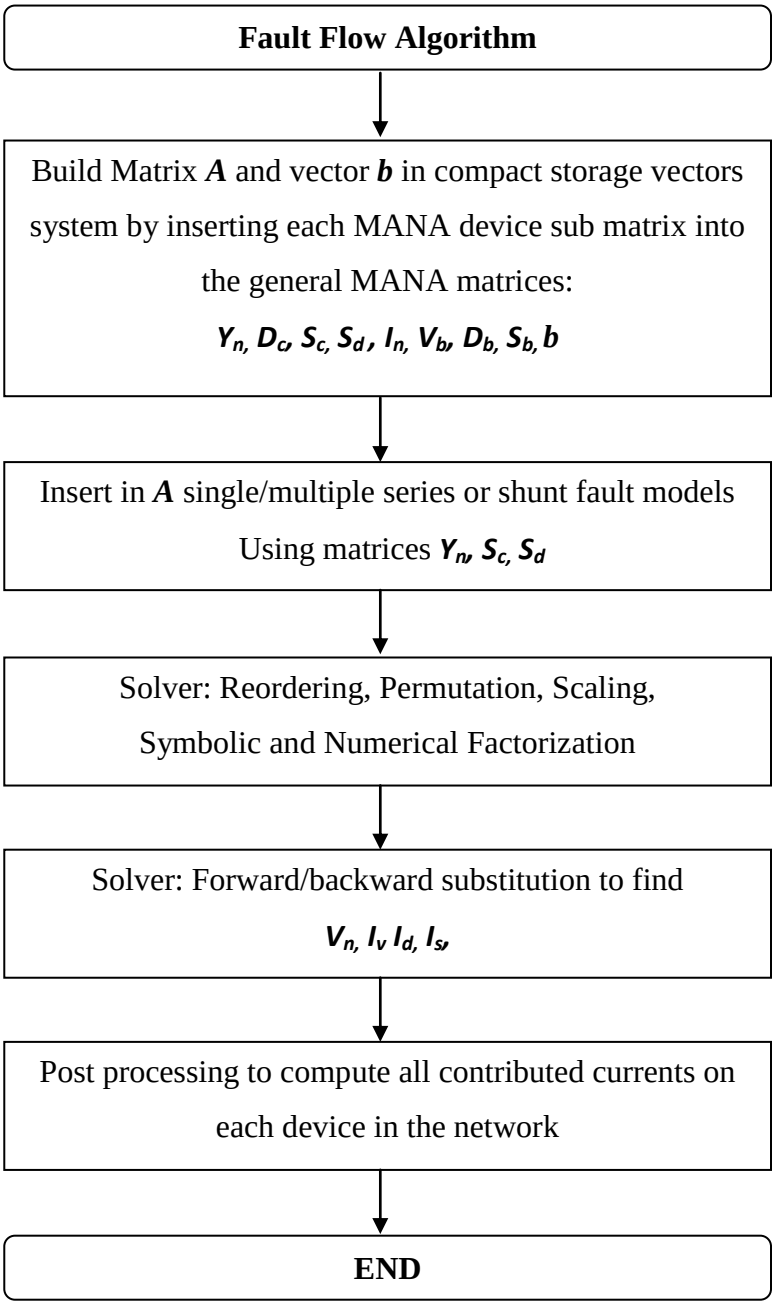


Figure 5-10: Fault Flow Algorithm

This algorithm requires only 1 factorization step and 1 forward/backward substitution step. It is not iterative and the solution is found directly. Most of the devices do not require post-processing calculations to compute current contributions. The solution of the linear system gives directly the substations, machines, transformers, switching and protective devices current contribution. Other devices such as overhead line shunt capacitors and all devices that are modeled only by an admittance matrix demand a post-processing step.

For example, consider overhead lines represented by typical pi circuits shown in Figure 5-11. Currents can be computed through the resistance and reactance segment of the line (*k* to *m*), through the sending end capacitance (*k* to ground) and through the receiving end capacitance (*m* to ground).

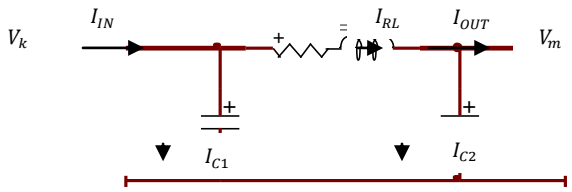


Figure 5-11: Overhead Line Pi Circuit

The currents through the RL segment of the line are given by the following equation:

$$\boldsymbol{I_{RL} = Y_{serie} \cdot (V_k - V_m)} \tag{5.23}$$

$\boldsymbol{Y_{serie}}$ is defined at equation (3.43). $\boldsymbol{I_{RL}}$ is a n x 1 vector and $\boldsymbol{V_k}$ and $\boldsymbol{V_m}$ are n x 1 vectors of the sending and receiving end voltages taken from the results vector x. The currents through the sending end capacitance, where $\boldsymbol{I_{C1}}$ is a n x 1 vector, are:

$$\boldsymbol{I_{C1} = \frac{Y_{shunt}}{2} \cdot V_k} \tag{5.24}$$

The currents through the receiving end capacitance, where $\boldsymbol{I_{C2}}$ is a n x 1 vector, are:

$$\boldsymbol{I_{C2} = \frac{Y_{shunt}}{2} \cdot V_m} \tag{5.25}$$

The input currents $\boldsymbol{I_{IN}}$, a n x 1 vector, are:

$$\boldsymbol{I_{IN} = I_{RL} + I_{C1}} \tag{5.26}$$

Finally, the output currents $\boldsymbol{I_{OUT}}$, also a n x 1 vector, are:

$$\boldsymbol{I_{OUT} = I_{RL} - I_{C2}} \tag{5.27}$$

5.2.2. Short-Circuit Summary Algorithm

The short-circuit summary is the process of computing the 5 types of shunt fault values on all system buses. This analysis is the most often used algorithm by distribution planners and network operators. There are several methods to compute such values but some are more time consuming. For *n* types of faults and *m* buses on the network, the first method (M1) shown in Figure 5-12 would be to repeat for *n x m* times the Fault Flow algorithm. The number of different operations is presented in Table 5-1.

Table 5-1: Number of Operations for Short-Circuit Method M1

Critical Steps of Algorithm	**Number of operation**
Build MANA matrices ***A*** and ***b***	1
Modify ***A*** to insert shunt fault type (e.g. LLL)	*n x m*
Reordering, Permutation, Scaling and Factorization	*n x m*
Forward/backward substitution	*n x m*
Post processing to compute all contribution currents	*n x m*

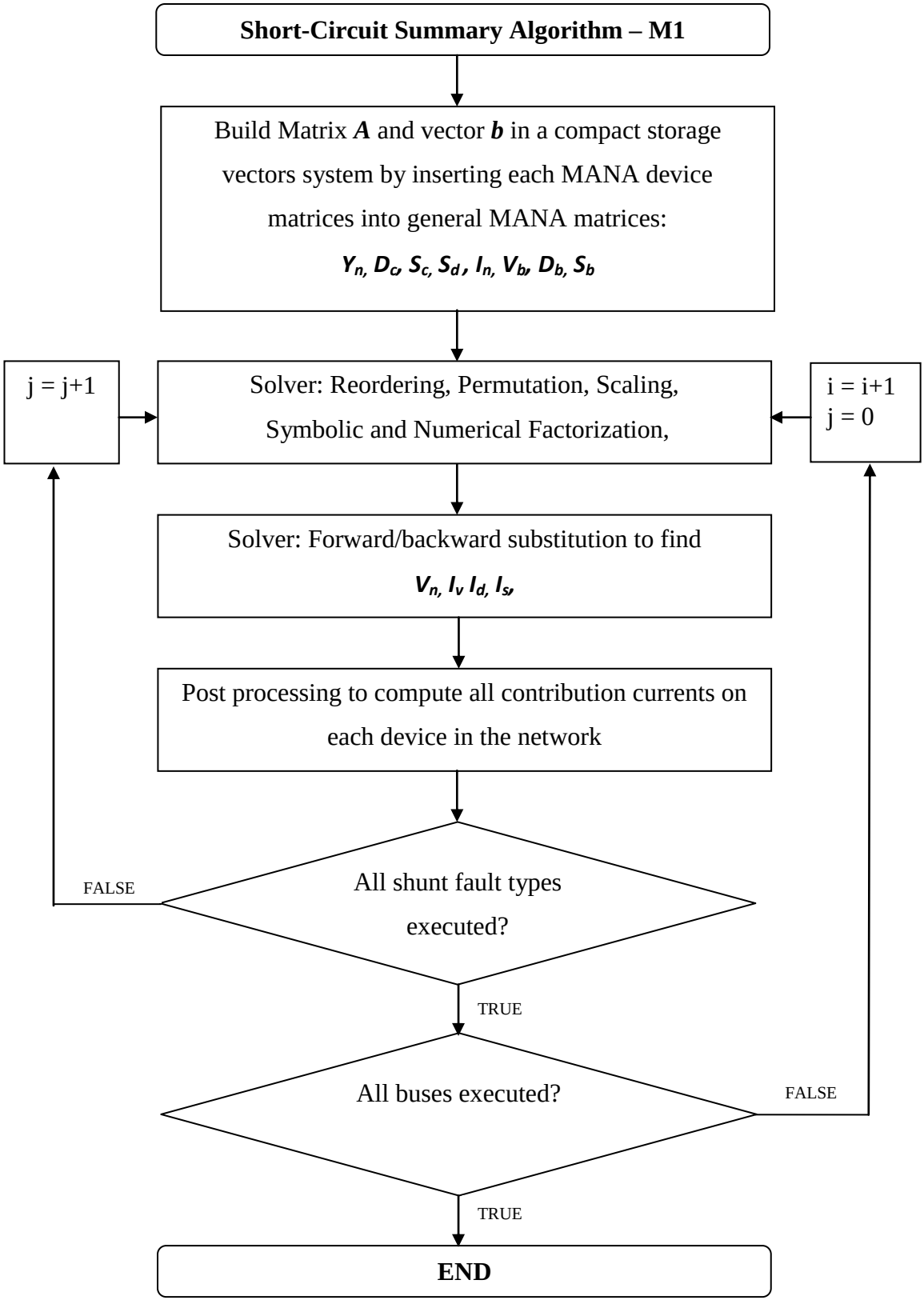


Figure 5-12: Short-Circuit Algorithm Method 1

The method 1 (M1) computes the short-circuit value at a specific bus/node for a specified shunt fault (e.g. LLL). Hence, in order to compute all short-circuit values at each node for all five types, an iterative process of rebuilding the matrices for each fault type and for each fault location is necessary. Although this process is a rigid approach, it is very time consuming since factorization must be repeated at each step.

An alternative method (M2), shown in Figure 5-13 is to calculate the inverse of network matrix $\boldsymbol{A}$ to compute the Thevenin impedance for each bus. This technique is traditionally used when solving with sequence nodal admittance matrices [5]. The inverse calculation using the transpose of the cofactors matrix (adjugate matrix) is not used as it would not be an efficient calculation method for large networks [47]. Instead, for a $m\ x\ m$ matrix, a method for solving m times the linear system applying a value 1 in a multiple vector $\boldsymbol{b}$ is the equivalent for finding the inverse. It is the equivalent of injecting 1A at each bus ($\boldsymbol{I_n}$) and solving the modified-augmented-nodal system. The solution vector $\boldsymbol{x}$ which originally contained partially voltage bus solutions ($\boldsymbol{V_n}$) will now contain Thevenin impedance ($\boldsymbol{Z_{Th}}$). Using this technique, the number of different operations is presented in Table 5-2.

Table 5-2: Number of Operations for Short-Circuit Method M2

Critical Steps of Algorithm	**Number of operation**
Build MANA matrices $\boldsymbol{A}$ and $\boldsymbol{b}$	1
Modify A to insert shunt fault type (e.g. LLL)	*0*
Reordering, Permutation, Scaling and Factorization	*1*
Forward/backward substitution	m
Post processing to compute current at buses	$n\ x\ m$

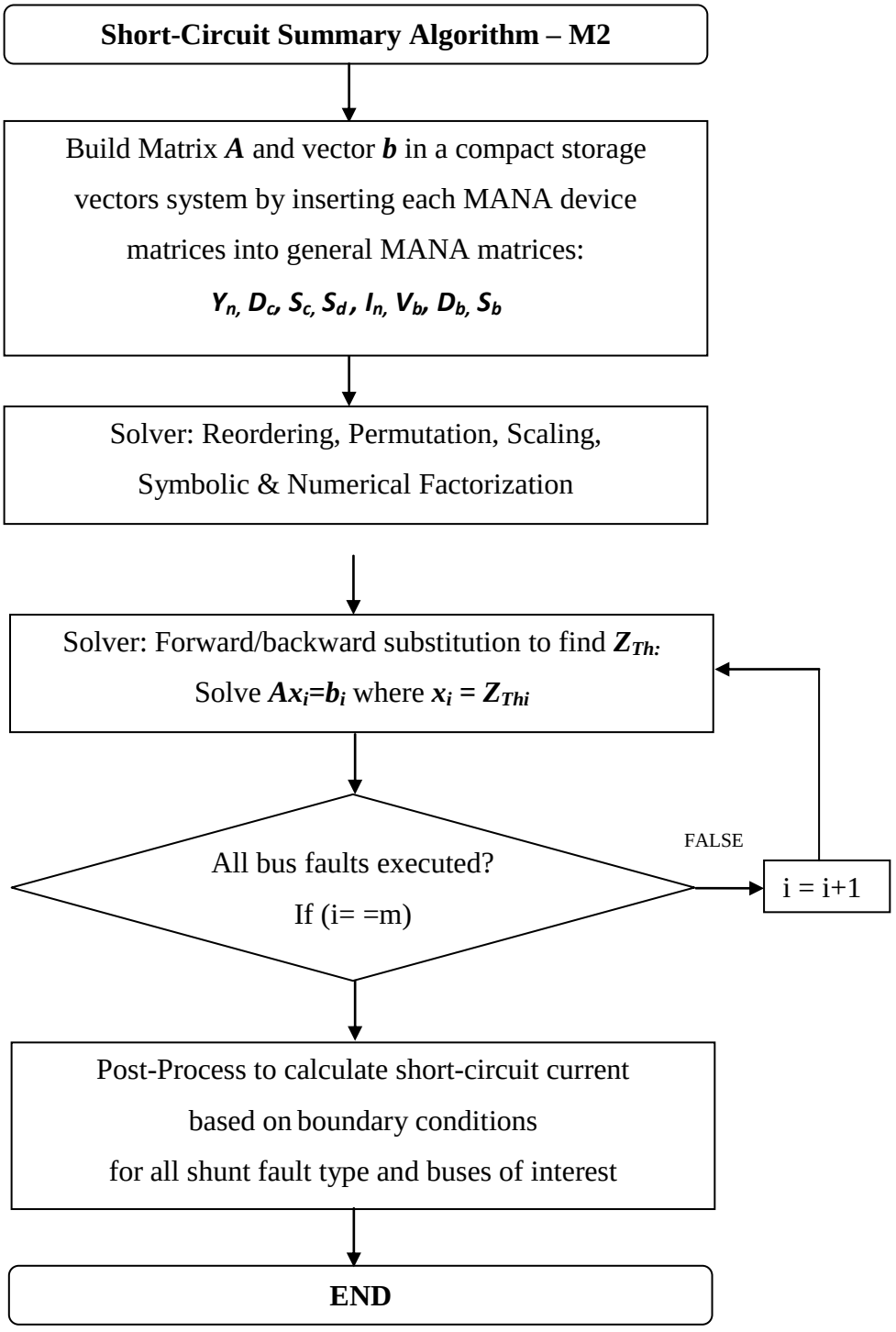


Figure 5-13: Short-Circuit Algorithm Method 2

The M2 algorithm is more efficient than M1 to compute short-circuit values for all nodes/buses in a network since it reduces the number of factorization steps. While computing the short-circuit values for all nodes/buses in the network is often the objective of the short-circuit summary analysis, the algorithm M2 can offer the possibility to only compute the short-circuit value at a specific node/bus. In this case, only the matrix index of interest should solve the current injection. For example, if there is no need to compute short-circuit values on all nodes/buses representing the MANA model of a transformer (e.g. grounding bus), then no injection should be done on this particular bus.

When using the M2 algorithm, the fault type is not modeled in the $\boldsymbol{A}$ matrix. The objective is to compute the $\boldsymbol{Z_{Th}}$ ($\boldsymbol{Z_{BUS}}$) matrix and to calculate in a post process the short-circuit value at each node/bus.

An *m* x *m* linear system with *s* right-hand sides (RHSs) can be written as:

$$\boldsymbol{Ax} = \boldsymbol{b} \tag{5.28}$$

With $\boldsymbol{A} \in \mathbb{C}^{m \times m}$, $\boldsymbol{x} \in \mathbb{C}^{m \times s}$, $\boldsymbol{b} \in \mathbb{C}^{m \times s}$

It can also be represented by the following multiple right-hand side expression:

$$\boldsymbol{AX} = \boldsymbol{B} \tag{5.29}$$

where:

$$\boldsymbol{A} = \begin{bmatrix} \boldsymbol{Y_n} & \boldsymbol{V_c} & \boldsymbol{D_c} & \boldsymbol{S_c} \\ \boldsymbol{V_c^t} & \boldsymbol{0} & \boldsymbol{0} & \boldsymbol{0} \\ \boldsymbol{D_c^t} & \boldsymbol{0} & \boldsymbol{0} & \boldsymbol{0} \\ \boldsymbol{S_c^t} & \boldsymbol{0} & \boldsymbol{0} & \boldsymbol{S_d} \end{bmatrix} \tag{5.30}$$

$$\boldsymbol{X} = \begin{bmatrix} Z_{Th11} & \cdots & Z_{Th1i} & \cdots & Z_{Th1n} \\ \vdots & \ddots & & & \vdots \\ Z_{Thi1} & & Z_{Th1ii} & & Z_{Th2n} \\ \vdots & & & \ddots & \vdots \\ Z_{Thn1} & \cdots & Z_{Thni} & \cdots & Z_{Thnn} \end{bmatrix} \tag{5.31}$$

$$\boldsymbol{B} = \begin{bmatrix} 1 & \cdots & 0 & \cdots & 0 \\ \vdots & \ddots & \vdots & & \vdots \\ & & i = 1 & & 0 \\ & & \vdots & \ddots & \vdots \\ 0 & \cdots & 0 & \cdots & 1 \end{bmatrix} \tag{5.32}$$

Only buses of interest are used to populate the matrix $\boldsymbol{B}$. Hence, the size of $\boldsymbol{B}$ is equal to the single phase node of interest. If all the nodes are of interest, for a *m* node network, $\boldsymbol{B}$ is the a *m* x *m* matrix. Matrix $\boldsymbol{X}$ has the same size as $\boldsymbol{B}$. One of the differences between the multiphase M2 algorithm and the traditional sequence calculation of the $\boldsymbol{Z_{Th}}$ matrix is that only part of $\boldsymbol{X}$ represents true multiphase Thevenin impedances. Only injection of rows containing the admittance model will result into Thevenin impedances. Also, Multiphase Thevenin impedance useful for the different short-circuit type can be of different sizes:

- 3 x 3 matrix for LLL and LLLG
- 2 x 2 matrix for LL and LLG
- 1 x 1 vector for LG

While the Fault Flow algorithm results were node voltages and voltage source and zero impedance element currents, the results obtained by solving the multi linear systems from the M2 algorithm are Thevenin impedances. Hence, to compute the short-circuit values, the post-processing will be different than for the one described for the Fault Flow algorithm. Using the same convention as in Figure 5-1 and where the neutral point is *N*, we evaluate the boundary equations and find a linear set of equations to solve the short-circuit current values.

For an LLL fault the boundary conditions are

$$I_X + I_Y + I_Z = 0 \tag{5.33}$$

$$V_X - Z_{XX} \cdot I_X - Z_{XY} \cdot I_Y - Z_{XZ} \cdot I_Z - Z_F \cdot I_X = V_N \tag{5.34}$$

$$V_Y - Z_{YY} \cdot I_Y - Z_{YX} \cdot I_X - Z_{YZ} \cdot I_Z - Z_F \cdot I_Y = V_N \tag{5.35}$$

$$V_Z - Z_{ZZ} \cdot I_Z - Z_{ZX} \cdot I_X - Z_{ZY} \cdot I_Y - Z_F \cdot I_Z = V_N \tag{5.36}$$

Reordering the equations, we compute the LLL short-circuit current:

$$\boldsymbol{I_{LLL} = Z_{Equ} V} \tag{5.37}$$

where:

$$\boldsymbol{Z_{Equ}} = \begin{bmatrix} Z_{XX} - Z_{YX} + Z_F & Z_{XY} - Z_{YY} - Z_F & Z_{XZ} - Z_{YZ} \\ Z_{XX} - Z_{ZX} + Z_F & Z_{XY} - Z_{ZY} & Z_{XZ} - Z_{ZZ} - Z_F \\ 1 & 1 & 1 \end{bmatrix} \tag{5.38}$$

$$\boldsymbol{V} = \begin{bmatrix} V_X - V_Y \\ V_X - V_Z \\ 0 \end{bmatrix} \tag{5.39}$$

For the LG fault case the boundary conditions are

$$I_Y = I_Z = 0 \tag{5.40}$$

$$V_X - Z_{XX} \cdot I_X - Z_G \cdot I_X = 0 \tag{5.41}$$

Reordering the equations, we compute LG short-circuit current:

$$I_X = \frac{V_X}{Z_{XX} + Z_G} \tag{5.42}$$

For LL fault the boundary conditions are:

$$I_Y = -I_Z \tag{5.43}$$

$$V_Y - Z_{YY} \cdot I_Y - Z_{YZ} \cdot I_Z - \frac{Z_F}{2} \cdot I_Y = V_N \tag{5.44}$$

$$V_Z - Z_{ZZ} \cdot I_Z - Z_{ZY} \cdot I_Y - \frac{Z_F}{2} \cdot I_Z = V_N \tag{5.45}$$

Reordering the equations, we compute LL short-circuits current:

$$I_Y = \frac{V_Y - V_Z}{Z_{YY} + Z_{ZZ} - Z_{YZ} - Z_{ZY} + Z_F} \tag{5.46}$$

$$I_Z = -I_Y \tag{5.47}$$

For LLG fault the boundary conditions are:

$$V_Y - Z_{YY} \cdot I_Y - Z_{YZ} \cdot I_Z - Z_F \cdot I_Y = V_N \tag{5.48}$$

$$V_Z - Z_{ZZ} \cdot I_Z - Z_{ZY} \cdot I_Y - Z_F \cdot I_Z = V_N \tag{5.49}$$

$$Z_g \cdot (I_Y + I_Z) = V_N \tag{5.50}$$

Reordering the equations 5.47, 5.48 and 5.49, we compute LLG short-circuit currents:

$$\boldsymbol{I_{LLG}} = \boldsymbol{Z_{Equ}} \boldsymbol{V} \tag{5.51}$$

where:

$$\boldsymbol{Z_{Equ}} = \begin{bmatrix} Z_{YY} + Z_F + Z_G & Z_{YZ} + Z_G \\ Z_{ZY} + Z_G & Z_{ZZ} + Z_F + Z_G \end{bmatrix} \tag{5.52}$$

$$\boldsymbol{V} = \begin{bmatrix} V_Y \\ V_Z \end{bmatrix} \tag{5.53}$$

For the LLLG fault case the boundary conditions are:

$$V_X - Z_{XX} \cdot I_X - Z_{XY} \cdot I_Y - Z_{XZ} \cdot I_Z - Z_F \cdot I_X = V_N \tag{5.54}$$

$$V_Y - Z_{YY} \cdot I_Y - Z_{XY} \cdot I_X - Z_{YZ} \cdot I_Z - Z_F \cdot I_Y = V_N \tag{5.55}$$

$$V_Z - Z_{ZZ} \cdot I_Z - Z_{XZ} \cdot I_X - Z_{YZ} \cdot I_Y - Z_F \cdot I_Z = V_N \tag{5.56}$$

$$Z_G \cdot (I_X + I_Y + I_Z) \tag{5.57}$$

Reordering the equations 5.53, 5.54, 5.55 and 5.56, we compute LLLG short-circuit currents:

$$\boldsymbol{I_{LLLG} = Z_{Equ} V} \tag{5.58}$$

where:

$$\boldsymbol{Z_{Equ}} = \begin{bmatrix} Z_{XX} + Z_F + Z_G & Z_{XY} + Z_G & Z_{XZ} + Z_G \\ Z_{YX} + Z_G & Z_{YY} + Z_F + Z_G & Z_{YZ} + Z_G \\ Z_{ZX} + Z_G & Z_{ZY} + Z_G & Z_{ZZ} + Z_F + Z_G \end{bmatrix} \tag{5.59}$$

$$\boldsymbol{V} = \begin{bmatrix} V_X \\ V_Y \\ V_Z \end{bmatrix} \tag{5.60}$$

These boundary equations are necessary to compute the short-circuit summary. These linear equations can be solved directly since the sizes of the matrices are relatively small and they are well conditioned.

CHAPTER 6. VALIDATION TESTS CASES

To validate multiple networks, the Fault Flow algorithm presented in Figure 5-11 and the Short-Circuit Summary Method 2 algorithm presented in Figure 5-14 has been implemented into the power engineering software CYME v5.04 [47]. The short-circuit results found by both algorithms are practically equal (differences of less than 1e-8). Hence, only one value is presented in the results. Contribution current is calculated using the Fault Flow Algorithm.

6.1.5 Bus System

The following benchmark [5] example is used to validate the following elements for a balanced network:

- Substation, generators, lines and transformer models
- Fault Flow and Short-Circuit Summary algorithm M2

This example is numbered 9.8 in [5]. A bolted LG fault is applied on buses 1 to 5 (one at a time). In the reference, Tables 9.4 and 9.5 give us the overall fault current, the current contributions and the voltages on all the buses. These results are given for every faulted bus. Figure 6.1 shows the network assembled in the software CYME.

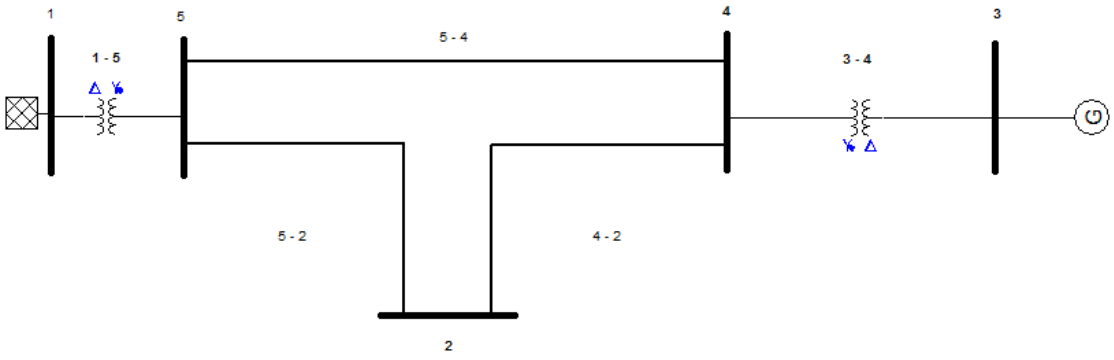


Figure 6-1: One Line Diagram for 5 Bus System

The system data is presented in the following tables:

Table 6-1: Substation and generator data for 5 Bus System

Bus	**X_0 [p.u.]**	**$X_1 = X_{d\text{-}sub}$ [p.u.]**	**X_2 [p.u.]**	**X_g [p.u.]**
1	0.0125	0.045	0.045	0
3	0.05	0.0225	0.0225	0.0025

Table 6-2: Line Data for 5 Bus System

Bus-Bus	**X_0 [p.u.]**	**X_1 [p.u.]**	**X_2 [p.u.]**
2-4	0.0125	0.045	0.045
2-5	0.05	0.0225	0.0225
4-5	0.075	0.025	0.025

Table 6-3: Transformer data for 5 Bus System

Low Voltage Bus	**High Voltage Bus**	**Leakage Reactance [p.u.]**	**Neutral Reactance [p.u.]**
1 (Delta)	5 (Y_g)	0.02	0
3 (Delta)	4 (Y_g)	0.01	0

For a single line-to-ground fault current on phase A, Table 6-4, 6-5 and 6-6 summarize the contributions on each line and transformer sections for each phase.

Table 6-4: Contribution of Fault Current for phase A for the 5 Bus System

Fault Bus	Contributions to Fault Current					
	GEN / Line / OR / TRSF	Bus-to-Bus	Current			
			Phase A			
			CYME [A]	Reference [A]	Reference [p.u.]	Diff(%)
1	G1	GRND_1	132455.09	132433.66	34.41	0.02
	T1	5_1	44685.91	44683.37	11.61	0.01
2	L1	4_2	862.17	862.03	5.151	0.02
	L2	5_2	1503.75	1503.52	8.984	0.02
3	G2	GRND_3	216435.04	216287.40	56.19	0.07
	T2	4_3	31216.73	31239.40	8.11	0.07
4	L1	2_4	291.63	291.61	1.742	0.01
	L3	5_4	1749.8	1749.68	10.46	0.01
	T2	3_4	7342.42	7342.43	43.88	0.00
5	L2	2_5	438.61	438.57	2.621	0.01
	L3	4_5	2631.65	2631.40	15.72	0.01
	T1	1_5	3986.3	3986.26	23.82	0.00
					Max.Diff (%)	0.07

Table 6-5: Contribution of Fault Current for phase B for the 5 Bus System

Fault Bus	Contributions to Fault Current					
	GEN / Line / OR / TRSF	Bus-to-Bus	Current			
			Phase B			
			CYME [A]	Reference [A]	Reference [p.u.]	Diff(%)
1	G1	GRND_1	22342.95	22337.84	5.804	0.02
	T1	5_1	22342.95	22337.84	5.804	0.02
2	L1	4_2	18.84	18.84	0.1124	0.02
	L2	5_2	18.84	18.84	0.1124	0.02
3	G2	GRND_3	15608.37	15619.69	4.055	0.07
	T2	4_3	15608.37	15619.70	4.055	0.07
4	L1	2_4	74.72	74.72	0.4464	0.00
	L3	5_4	448.3	448.31	2.679	0.00
	T2	3_4	523.02	523.03	3.125	0.00
5	L2	2_5	112.37	112.37	0.6716	0.00
	L3	4_5	674.23	674.23	4.029	0.00
	T1	1_5	786.6	786.59	4.7	0.00
					Max.Diff (%)	0.07

Table 6-6: Contribution of Fault Current for phase C for the 5 Bus System

Fault Bus	Contributions to Fault Current					
	GEN / Line / OR / TRSF	Bus-to-Bus	Current			
			Phase C			
			CYME [A]	Reference [A]	Reference [p.u.]	Diff(%)
1	G1	GRND_1	22342.95	22337.84	5.804	0.02
	T1	5_1	22342.95	22337.84	5.804	0.02
2	L1	4_2	18.84	18.84	0.1124	0.02
	L2	5_2	18.84	18.84	0.1124	0.02
3	G2	GRND_3	15608.37	15619.69	4.055	0.07
	T2	4_3	15608.37	15619.70	4.055	0.07
4	L1	2_4	74.72	74.72	0.4464	0.00
	L3	5_4	448.3	448.31	2.679	0.00
	T2	3_4	523.02	523.03	3.125	0.00
5	L2	2_5	112.37	112.37	0.6716	0.00
	L3	4_5	674.23	674.23	4.029	0.00
	T1	1_5	786.6	786.59	4.7	0.00
					Max.Diff (%)	0.07

Results show a maximum difference of 0.07%. This is acceptable knowing that the reference provides p.u. results with 2 digit precision. Since contributing fault currents are derived from voltages, we conclude that bus voltages are also validated.

6.2.IEEE 13-Node Test Feeder

The IEEE 13-Node Test Feeder is one of several test feeders provided by the IEEE PES Distribution System Analysis Subcommittee [9]. The tests feeders are intended to evaluate the accuracy and capability of power system software to solve unbalanced distribution systems. Figure 6-2 shows the system modeled in CYME. Results have been compared with the Subcommittee results. The Subcommittee has used the following software packages to create the benchmark:

1- WindMil by Milsoft Utility[48]

2- Radial Distribution Analysis Package (RDAP) [49]

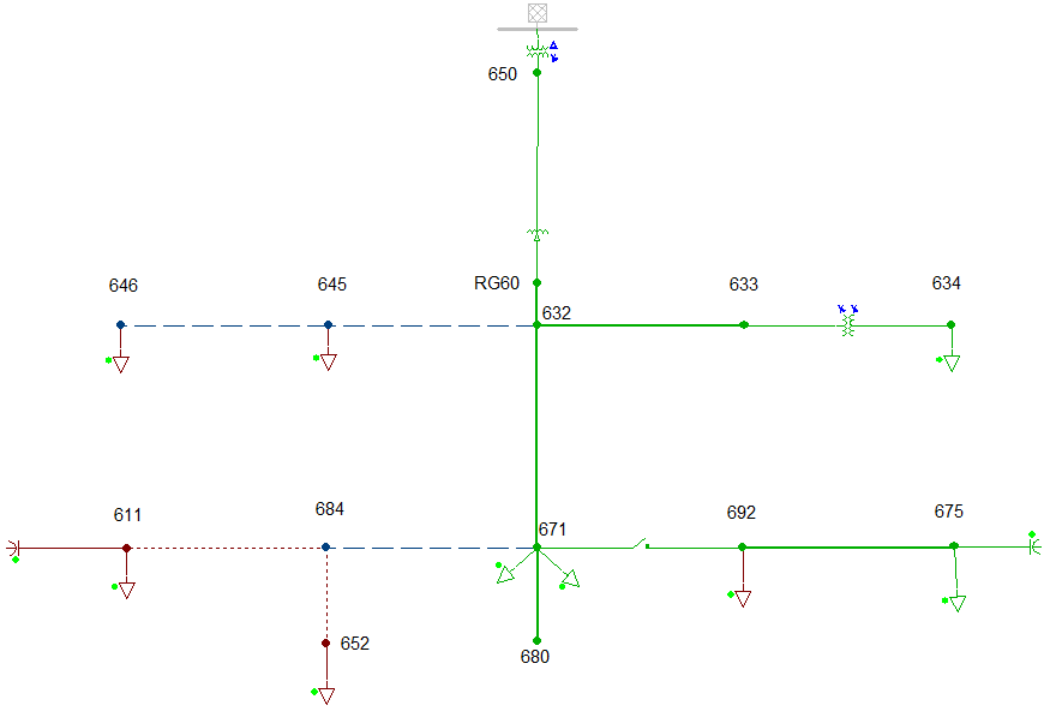


Figure 6-2: IEEE 13-Node Test Feeder

The common assumptions presented in section 5-2 and uses in distribution planning short-circuit analysis are considered to compute short-circuit currents. The results found for the short-circuit summary are presented in Table 6-7, Table 6-8 and Table 6-9. They match with an error less than 0.1% for all short-circuit types.

Table 6-7: Short-Circuit Summary method for LLL, LG and LLLG Faults

Short-Circuit Currents - IEEE 13 Node - Units [A]										
		Three-Phase Fault (LLL)			Single Line-To-Ground Fault (LG)			Three-Phase To-Ground Fault (LLLG)		
Nodes	Phases	A	B	C	A	B	C	A	B	C
Sub	ABC	13700.1	13700.1	13700.1	10952.7	10952.7	10952.7	13700.1	13700.1	13700.1
RG60	ABC	8416.0	8416.0	8416.0	8478.7	8478.7	8478.7	8416.0	8416.0	8416.0
692	ABC	3350.0	3271.3	2964.6	2196.2	2156.8	2173.8	3317.0	3267.9	3009.5
684	AC	0.0	0.0	0.0	2019.4	0.0	2001.7	0.0	0.0	0.0
680	ABC	2909.4	2839.3	2549.6	1851.8	1817.0	1832.0	2880.2	2836.7	2589.5
675	ABC	3075.8	3041.4	2754.9	2076.8	2049.9	2057.5	3044.6	3041.2	2792.9
671	ABC	3350.0	3271.3	2964.6	2196.2	2156.8	2173.8	3317.0	3267.9	3009.5
652	A	0.0	0.0	0.0	1795.6	0.0	0.0	0.0	0.0	0.0
650	ABC	8416.0	8416.0	8416.0	8478.7	8478.7	8478.7	8416.0	8416.0	8416.0
646	BC	0.0	0.0	0.0	0.0	2516.4	2524.1	0.0	0.0	0.0
645	BC	0.0	0.0	0.0	0.0	2806.4	2817.7	0.0	0.0	0.0
634	ABC	15275.2	15134.7	14719.9	13045.9	12961.4	12985.5	15190.0	15149.1	14795.7
633	ABC	4149.8	4023.0	3802.3	2950.4	2910.2	2921.6	4115.2	4028.1	3836.9
632	ABC	4800.7	4704.7	4392.0	3495.3	3444.3	3466.3	4758.6	4697.9	4449.1
611	C	0.0	0.0	0.0	0.0	0.0	1852.0	0.0	0.0	0.0

Table 6-8: Short-Circuit Summary for LLG Faults

Short-Circuit Currents - IEEE 13 Node - Units [A]										
		Double Line-To-Ground Fault (LLG)								
		Fault on AB			Fault on BC			Fault on CA		
Nodes	Phases	A	B	C	A	B	C	A	B	C
Sub	ABC	12311.4	13093.7	0.0	0.0	12311.4	13093.7	13093.7	0.0	12311.4
RG60	ABC	8445.9	8449.6	0.0	0.0	8445.9	8449.6	8449.6	0.0	8445.9
692	ABC	3091.1	3006.9	0.0	0.0	2778.8	2685.1	2822.4	0.0	2892.0
684	AC	0.0	0.0	0.0	0.0	0.0	0.0	2616.4	0.0	2644.7
680	ABC	2676.6	2610.2	0.0	0.0	2383.3	2306.8	2435.1	0.0	2489.0
675	ABC	2820.8	2815.0	0.0	0.0	2576.9	2531.0	2647.2	0.0	2658.6
671	ABC	3091.1	3006.9	0.0	0.0	2778.8	2685.1	2822.4	0.0	2892.0
652	A	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
650	ABC	8445.9	8449.6	0.0	0.0	8445.9	8449.6	8449.6	0.0	8445.9
646	BC	0.0	0.0	0.0	0.0	3051.7	3057.0	0.0	0.0	0.0
645	BC	0.0	0.0	0.0	0.0	3405.6	3367.7	0.0	0.0	0.0
634	ABC	14309.4	14484.9	0.0	0.0	14003.3	14056.1	14356.1	0.0	14150.6
633	ABC	3799.7	3728.4	0.0	0.0	3547.8	3456.5	3636.7	0.0	3673.6
632	ABC	4486.9	4333.9	0.0	0.0	4164.4	4008.1	4152.8	0.0	4283.5
611	C	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0

Table 6-9: Short-Circuit Summary for LL Faults

Short-Circuit Currents - IEEE 13 Node - Units [A]										
		Line-To-Line Fault (LL)								
		Fault on AB			Fault on BC			Fault on CA		
Nodes	Phases	A	B	C	A	B	C	A	B	C
Sub	ABC	11864.7	11864.7	0.0	0.0	11864.7	11864.7	11864.7	0.0	11864.7
RG60	ABC	7288.4	7288.4	0.0	0.0	7288.4	7288.4	7288.4	0.0	7288.4
692	ABC	2938.0	2938.0	0.0	0.0	2599.5	2599.5	2734.8	0.0	2734.8
684	AC	0.0	0.0	0.0	0.0	0.0	0.0	2517.6	0.0	2517.6
680	ABC	2554.5	2554.5	0.0	0.0	2238.5	2238.5	2364.1	0.0	2364.1
675	ABC	2707.3	2707.3	0.0	0.0	2423.0	2423.0	2531.4	0.0	2531.4
671	ABC	2938.0	2938.0	0.0	0.0	2599.5	2599.5	2734.8	0.0	2734.8
652	A	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
650	ABC	7288.4	7288.4	0.0	0.0	7288.4	7288.4	7288.4	0.0	7288.4
646	BC	0.0	0.0	0.0	0.0	2881.6	2881.6	0.0	0.0	0.0
645	BC	0.0	0.0	0.0	0.0	3191.0	3191.0	0.0	0.0	0.0
634	ABC	13235.0	13235.0	0.0	0.0	12781.8	12781.8	13056.2	0.0	13056.2
633	ABC	3585.8	3585.8	0.0	0.0	3298.3	3298.3	3469.0	0.0	3469.0
632	ABC	4194.7	4194.7	0.0	0.0	3835.7	3835.7	3982.0	0.0	3982.0
611	C	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0

It is interesting comparing these values with traditional sequence network based $\boldsymbol{Y_{Bus}}$ method. CYME has also a sequence component algorithm method based on [4]-[6]. The maximum error is 7.4%. Since the substation impedance is provided in sequence, both multiphase and sequence methods compute the same values. The error seems to be proportional to the distance of the node from the substation. The error should increase if the traditional assumptions are not considered. Hence, calculating the short-circuit in operations using those assumptions can lead to large erroneous values.

Table 6-10: Short--Circuit Summary using Sequence Method

Short-Circuit Currents - IEEE 13 Node - Units [A] Sequence Method						
		LLL	LG	LLLG	LLG	LL
Nodes	Phases	A	A	A	A	A
Sub	ABC	13700.1	10952.7	13700.1	12311.4	11864.7
RG60	ABC	8416.0	8478.7	8416.0	8445.9	7288.4
692	ABC	3176.2	2175.5	3176.2	2913.0	2750.7
684	AC		2002.7	2922.3	2661.4	2530.8
680	ABC	2747.0	1833.5	2747.0	2508.8	2378.9
675	ABC	2943.2	2061.3	2943.2	2679.9	2548.9
671	ABC	3176.2	2175.5	3176.2	2913.0	2750.7
652	A		1783.7			
650	ABC	8416.0	8478.7	8416.0	8445.9	7288.4
646	BC		2526.6		3117.2	2967.1
645	BC		2820.2		3491.7	3298.8
634	ABC	15036.4	12997.5	15036.4	14151.3	13021.9
633	ABC	3980.4	2927.3	3980.4	3669.3	3447.1
632	ABC	4617.5	3468.5	4617.5	4305.4	3998.9
611	C		1852.8			

Table 6-11: Maximum Difference between Phase and Sequence Method

Maximum difference Phase vs Sequence						
		LLL	LG	LLLG	LLG	LL
Nodes	Phases	A	A	A	A	A
Sub	ABC	0.0%	0.0%	0.0%	6.4%	0.0%
RG60	ABC	0.0%	0.0%	0.0%	0.0%	0.0%
692	ABC	6.7%	1.0%	5.3%	6.1%	6.8%
684	AC		0.8%		5.4%	0.5%
680	ABC	7.2%	1.0%	5.7%	6.7%	7.4%
675	ABC	6.4%	0.8%	5.1%	5.3%	6.2%
671	ABC	6.7%	1.0%	5.3%	6.1%	6.8%
652	A		0.7%			
650	ABC	0.0%	0.0%	0.0%	0.0%	0.0%
646	BC		0.4%		2.1%	2.9%
645	BC		0.5%		3.6%	3.3%
634	ABC	2.1%	0.4%	1.6%	2.4%	1.6%
633	ABC	4.5%	0.8%	3.6%	3.6%	4.0%
632	ABC	4.9%	0.8%	3.6%	4.2%	4.9%
611	C		0.0%			

6.3.Performance Tests

The performance of the resolution process of the short-circuit analysis is important for commercial use of the algorithms presented in this document. To investigate the performance, the resolution time for the KLU solver and the MKL solver were compared for the different system sizes. The tested algorithm is the Short-Circuit Summary algorithm M2. The systems are interconnected and constitute a single system. Hence, starting from an original 5110 matrix size system shown in Figure 6-3, larger systems were created by interconnecting the same network with a random loop point.

Figure 6-3: System for Performance Test

The tests were performed using a computer with Windows 7 64 bits, Intel Core 2 Quad (Q9550) at 2.83 Ghz with 4 GB RAM.

The distribution network consists of mostly overhead lines, protection devices and distributed loads. It can be found in the sample network provided by the engineering software CYME [47].

Table 6-12: KLU vs MKL PARDISO Resolution Time

System	Buses	Matrix Size	Short-Circuit Time [s]	
			KLU	MKL PARDISO
1	1223	5110	2.1	6.8
2	2445	10217	8.4	23.6
4	4889	20431	34.4	113.9
8	9777	40859	183.3	510.9
16	19553	81715	815.1	6235.8

The results shown in Table 6-12 confirm the advantage of the triangular block permutation strategy used by KLU. The KLU resolution time is faster than MKL PARDISO by an approximate factor of 3. These resolution times are problematic when integrating short-circuit algorithms in a commercial software. Rule of thumb is that over 10 seconds, the users are irritated by the resolution time. Since distribution feeders can be over 10 000 buses, the users' threshold is surpassed.

The Figure 6-4 illustrates the high performance of KLU versus MKL PARDISO. To focus on the values, the MKL PARDISO results for the 16 bus network system have been removed. To overcome the performance issues, further investigations in solver options need to be performed. During this research project, investigations were conducted evaluating the multiple right-hand side (rhs) feature of MKL PARDISO. Even with parallelization of the process using an OpenMP approach, the results have shown poor performances.

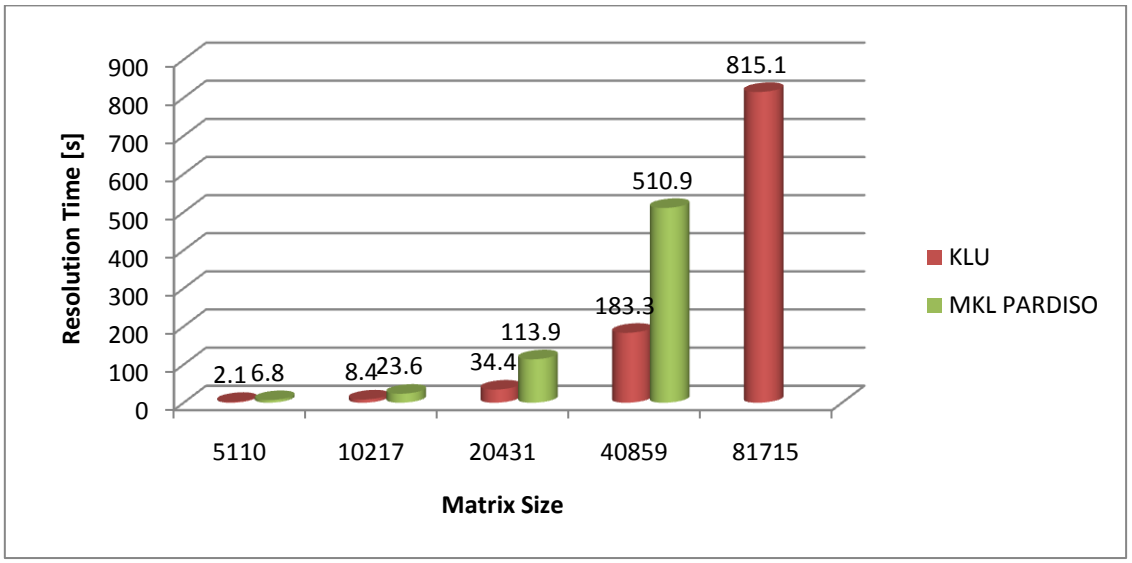


Figure 6-4: Short-Circuit Resolution Time as a Function of Matrix Size

A test conducted on two sample matrices with 10 non-zeros elements per rows for two different sizes, shows that for relatively small matrices, the resolution time is even greater when using parallel multiple right-hand side option. It seems that preparing the data for parallel resolution takes more time than actually solving the system in sequential mode. Higher size matrices perform better. Hence, for very large matrices (over 50 000), there might be an interest for using this feature.

Table 6-13: Multiple Rigth-Hand Side Test Results

5000 x 5000	
rhs	Time [s]
1	9,734
2	33,14
4	19,734
8	15,687
16	13,203
32	12,406
64	12,531
128	15,734

20000 x 20000	
rhs	Time [s]
1	248,932
2	659,347
4	415,055
8	306,088
16	260,636
32	239,574
64	232,651
128	259,808

When solving the short-circuit summary with the current injection method, similar to calculating the inverse matrix, there are numerous calculations that are done that are not necessary to obtain the short-circuit values. Hence, another strategy that could be used to solve

the performance issue is using algorithms that solve only the selected inversion of a sparse matrix. These algorithms are under development and should be integrated in solvers in the next few years [46]. These algorithms can compute selected values of the vector $\boldsymbol{x}$ of the injection current method by applying efficient factorization on matrix $\boldsymbol{A}$. This will truly reduce the computation time since the forward/backward step is no longer necessary.

After testing the same matrices presented in Table 6-12 on a prototype performing the partial inverse (SellINV method [46]), Table 6-14 presents the performance results comparing the short-circuit algorithm M2 with the partial inverse method.

Table 6-14: Performance Results Comparing KLU, MKL PARDISO and SellINV

System	Buses	Matrix Size	Short-Circuit Time [s]		
			KLU	MKL PARDISO	SellINV
1	1223	5110	2.1	6.8	< 2
2	2445	10217	8.4	23.6	< 2
4	4889	20431	34.4	113.9	< 2
8	9777	40859	183.3	510.9	< 2
16	19553	81715	815.1	6235.8	6

Furthermore, Table 6-15 presents results from an additional test done using only SellINV on a 78209 node system. For this case, the time has been separated for the 4 main blocs for solving the short-circuit:

Table 6-15: Performance Results for SelllINV method on a 78209 node system

Solving Steps	Short-Circuit Time [s]
	SellINV
Preparing the data	16
Building the matrices	45
Solving the system	3
Post Process	57
TOTAL:	121

Table 6-14 and 6-15 truly demonstrates the strength of this new algorithm!

CHAPTER 7. **CONCLUSION**

The present research work demonstrated the implementation of algorithms to solve short-circuit analysis for complex unbalanced distribution systems using the multiphase modified-augmented-nodal analysis method. The method has been implemented in commercial engineering analysis software CYME v5.04 to handle radial, highly meshed, phase-merging, three-phase, single phase and large (> 10 000 bus) systems. Typical MANA models for devices in the distribution system were presented. The documented devices are substation sources, two-winding transformers, three-winding transformers, electronically coupled generators, synchronous machines, induction machines, overhead electromagnetic coupled lines, cables and switching and protective devices. Two main algorithms were presented. The first algorithm, Fault Flow algorithm, was used to compute shunt, series and simultaneous fault currents at fault locations with the evaluation of contributing currents on all network devices using multiphase circuits. The second algorithm, Short-circuit summary, was used to compute short-circuit currents at all locations of the system with an efficient method oriented for planning and operation purposes. Two high-performance, robust, memory efficient and easy to use package solvers for large sparse asymmetric linear systems and ill-conditioned networks were presented highlighting their main features. Performance remains an issue for the Short-circuit summary algorithm. Further research must be conducted in this area.

The validation results show that the algorithms and device MANA models provide accurate results. Furthermore, we have demonstrated the capability of handling complex configurations such as phase-merging topology and single phase DG.

Further research should also include the integration of other network devices, such as electronically coupled generators MANA models

The overall objectives have been reached.

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