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UNIVERSITÉ DE MONTRÉAL

HYBRID MICROFLUIDIC CMOS CAPACITIVE SENSORS FOR LAB-ON-CHIP APPLICATIONS

Ebrahim Ghafar-Zadeh

DÉPARTEMENT DE GÉNIE ÉLECTRIQUE

ÉCOLE POLYTECHNIQUE DE MONTRÉAL

THÉSE PRÉSENTÉE EN VUE DE L'OBTENTION

DU DIPLÔME DE PHILOSOPHIAE DOCTOR (PH.D.)

(GÉNIE ÉLECTRIQUE)

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Cette thèse intitulée

HYBRID MICROFLUIDIC/CMOS CAPACITIVE SENSORS FOR LAB-ON-CHIP APPLICATIONS

Présentée par: Ebrahim Ghafar-Zadeh

en vue de l'obtention du diplôme de Philosophiae Doctor

a été dûment acceptée par le jury d'examen constitué de :

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M. CHODAVARAPU Vamsy, PhD, membre externe

Dedicated to my wife

Masoomeh

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ABSTRACT

The recent advances in lab-on-chip (LoC) technology offer the prospect of rapid, automated biological assays or procedures in analytical chemistry through miniaturized devices. The rapid response, portability, and ease-of-use make LoCs suitable for operation in real-world conditions, spanning a wide array of health and life science applications such as the diagnosis of genetic disorders or the testing of food and water supplies for contamination. The development of biochips is a major thrust of the rapidly growing biotechnology industry, and involves a multidisciplinary research effort encompassing microfluidics, microelectronics and biochemistry.

CMOS based capacitive sensors have recently received significant attention for biochemical testing applications such as DNA detection, antibody-antigen recognition and cell monitoring. In this thesis, we address this challenging issue by proposing hybrid microfluidic/CMOS capacitive sensor suitable for the aforementioned applications. A new high-precision charge-based sensor system is presented to detect the minute capacitance variations resulting from the presence of biochemical solutions/solvents in microchannel. We also propose a low temperature and low complexity direct-write microfluidic packaging procedure to implement the microfluidic channels on the top of CMOS sensor chip. The implementation and experimental results are demonstrated using organic solvents with known dielectric constants in order to reveal the viability of the proposed hybrid LoC platform for capacitive detection.

It is recognized by the researchers in the field that the custom design of a generic capacitive sensor system should be taken into account for LoC applications. Of course, this new multidisciplinary approach is in its early stage of development and it needs huge effort to transition from this level of research to the optimum design and implementation of fully automated sensor systems.

RÉSUMÉ

Les développements récents de la technologie de laboratoire-sur-puce (Laboratory-on-Chip : LoC) proposent des analyses ou des procédés biologiques rapides et automatiques en chimie analytique à travers des dispositifs miniaturisés. Leur réponse rapide, portabilité, et facilité d'utilisation rendent les LoCs convenables pour opérer dans des conditions réelles, pour beaucoup d'applications de santé et de sciences de la vie comme le dépistage de maladies génétiques ou les tests de contamination de nourriture et d'eau. Le développement des biopuces est un immense défi dans l'industrie de la biotechnologie en expansion rapide. Ceci comprend un effort de recherche multidisciplinaire incluant la microfluidique, la microélectronique et la biochimie.

Dans cette thèse, notre intérêt se porte sur l'aspect d'ingénierie des LoCs, et en particulier sur le développement d'un capteur hybride microfluidique/CMOS comme premier pas vers un LoC complètement intégré. Cependant, plusieurs LoCs basés sur la technologie CMOS ont été proposés récemment pour diverses applications, mais la technologie de laboratoire-sur-puce elle-même est encore dans sa phase préliminaire. Ce travail concerne l'intégration de structures microfluidiques avec de la microélectronique. Les composants microfluidiques sont requis pour injecter l'analyte vers les sites de détection. Nous relevons ce défi avec un procédé microfluidique d'écriture directe qui est utilisé pour la première fois sur une puce CMOS. Nous proposons aussi un capteur capacitif basé sur la charge pour détecter les petits changements de capacité induits par

la présence de bioparticules dans le canal. Bien que beaucoup de capteurs capacitifs aient été publiés pour maintes applications, peu d'intérêts ont été accordés envers un système dédié à la détection capacitive d'un liquide sur la surface d'une puce CMOS. Pour cela, nous proposons trois architectures de puces avec des niveaux de complexité différents en CMOS 0.18 µm. Chaque puce capteur est incorporée avec de la microfluidique pour la détection d'analytes. Nous démontrons la viabilité du système proposé pour les applications de LoC pour différents solvants organiques avec différentes constantes diélectriques.

Le capteur capacitif proposé, ainsi que la structure microfluidique faite par d'écriture directe, offrent les avantages d'une basse complexité et d'une grande flexibilité pour différents types d'applications de LoC comme la détection d'ADN, la reconnaissance de virus et l'analyse de cellules.

CONDENSÉ EN FRANÇAIS

I. INTRODUCTION

Les LoCs semblent avoir un avenir prometteur en tant que capteurs miniaturisés pour la mesure et la détection rapides et automatiques d'une gamme diversifiée d'analytes cliniques et environnementales. Une plateforme de LoC comprend de la microfluidique, des électrodes de détection et des interfaces microélectroniques (voir Fig. 4.1). Les composantes microfluidiques, tel que les canaux, les valves et les pompes dirigent et manipulent des fluides biologiques ou biochimiques. La fine pointe de la recherche sur l'intégration des microfluidiques en microélectronique est de nos jours, centralisée sur la fabrication de composants microfluidiques en tant que partie du procédé de fabrication microélectronique sur tranches plutôt que sur des puces encapsulées électriquement [PAL04]. Rasmussen et al, à titre d'exemple, ont réalisé des canaux microfluidiques sur une puce fabriquée en se basant sur des procédés conventionnels de micro-usinage de surfaces [RAS01]. D'autres efforts de la part de Masteranglo et al montrent le micro-usinage de surfaces polymères pour fabriquer les canaux microfluidiques sur la surface d'un circuit intégré CMOS [MAN97]. Chartier et al ont publié une méthode de fabrication d'une structure microfluidique intégrée sur une puce CMOS basée sur les polymères avec une technique de gaufrage à chaud [ICH03]. En effet, un LoC basé sur la

technologie CMOS requiert un boîtier microfluidique efficace pour protéger la circuiterie des analytes biologiques et biochimiques. Cet aspect, qui est souvent négligé par les applications de LoC CMOS, est incontournable pour diriger les fluides vers les capteurs pour être analysés. Idéalement, l'encapsulation microfluidique doit être le résultat d'un procédé à basse température avec soudure fiable et hermétique. La fuite des analytes des composants microfluidiques risque d'augmenter les résistances et capacités parasites, modifiant alors les caractéristiques du circuit. Nous traitons ce problème aussi en proposant un procédé de fabrication microfluidique d'écriture directe [GHA07g]. Ce procédé fiable et robotisé est utilisé pour implémenter les microcanaux sur une puce de capteurs capacitifs.

Les capteurs capacitifs CMOS ont récemment attiré l'attention des chercheurs œuvrant dans le domaine de LoC pour tests biochimiques, tel que la détection d'antigènes par liaison d'anticorps (ex. la détection de virus [BAL05], l'analyse cellulaire [ROM05], la reconnaissance d'ADN [SON06] ainsi que la détection chimique). Les applications de LoC complètement intégrés de la sorte exigent un capteur microfluidique/CMOS-capacitif hybride. Dans cette thèse, nous relevons ce défi en proposant une matrice de capteurs capacitifs implémentée avec le procédé CMOS et intégrée avec des canaux microfluidiques (voir Fig. 4.1). Une couche de détection biofonctionnalisée spécifique à chaque application pourrait être formée sur les sites de détection pour des fins de détection sélective – mais ceci n'est pas le cas pour le présent travail.

Jusqu'à maintenant, plusieurs techniques de lecture de données employant des stratégies différentes ont été publiées pour des systèmes de capteurs capacitifs autonomes (ex. accéléromètre basé sur les systèmes microélectromécaniques). Par contre, la littérature ne parle pas trop de la conception sur mesure de LoC à capteurs capacitifs. Les capteurs capacitifs pour les applications de LoC n'exigent pas la détermination d'une seule valeur pour la capacité de détection, mais toutefois de pouvoir distinguer le comportement du dispositif plutôt en présence qu'en absence d'analyte dans le canal microfluidique. Les valeurs des capacités statiques avant et après l'injection d'analyte sont extraites à partir de mesures dynamiques de capacités pour la plupart des applications [VAK06]. Pour cela, les techniques basées sur la moyenne peuvent être employées de façon simple et efficace. Cette complexité réduite se révèle être un atout pour la conception et l'implémentation de grandes matrices de capteurs capacitifs [PRA07]. En effet, l'implémentation d'une grande matrice de capteurs sur une seule puce implique une petite empreinte de plots pour le circuit. Ceci écarte l'option d'utiliser une approche basée sur les amplificateurs opérationnels qui occuperaient une grande surface.

La mesure de capacité basée sur la charge (MCBC) est une méthode simple proposée pour la première fois en 1998 pour les mesures de capacités d'interconnexions inférieures à un femto-Farad dans les puces CMOS [SYL98]. À cause de la basse complexité, de la surface réduite, et de la haute précision, cette méthode de mesure statique s'est avérée être la préférée pour satisfaire les exigences des capteurs capacitifs

de LoC. Parmi les rares travaux sur la mesure de capacité basée sur la charge pour les capteurs capacitifs, Guiducci et al ont réussi à détecter l'ADN par le biais de circuiterie externe à la puce et d'électrodes intégrées [GUI04]-[STA07].

Cet thèse se concentre sur les noyaux-MCBC complètement intégrés, pour applications de LoC. Pour montrer l'applicabilité de la MCBC pour les capteurs capacitifs, une puce de test (PT1) a été implémentée initialement avec une grosse électrode interdigitée connectée à une seule paire n/pMOS (Fig. 4.1). Puisque la mesure de capacité basée sur la charge utilise l'instrumentation externe, elle ne peut pas être appliquée directement aux capteurs intégrés. Pour cela, un circuit complémentaire (PT2) a été conçu est implémenté dans un procédé CMOS. Cette puce comprend une électrode interdigitée et des circuits d'interface pour convertir la capacité en tension. Par la suite, une matrice d'électrodes interdigitées et d'autres circuits de calibration ont été implémentés dans une puce PT3. Nous avons également conçu et développé d'autres circuits pour incorporer tout le système de capteurs sur une puce.

Les solvants organiques avec des constantes diélectriques connues offrent une bonne alternative pour modéliser la variation de capacité suite à un changement diélectrique à proximité de sites de détection. Nous caractérisons le capteur hybride proposé et montrons sa viabilité pour les applications de LoC en utilisant des substances chimiques contenant le la dichlorométhane, de l'acétone et du méthanol.

Le reste de ce condensé est organisé comme tel. La section II décrit l'analyse et la conception de circuits d'interface pour les noyaux-MCBC. La section III décrit le

procédé de fabrication microfluidique d'écriture directe. Les procédures d'expérimentation et les résultats se trouvent dans la section IV. Cette section est suivie d'un résumé qui fait l'objet de la section VI.

II. CIRCUIT D'INTERFACE À NOYAU- MCBC

Trois architectures de puces avec différents niveaux de complexité sont discutées dans cette section.

A. Banc d'essai de caractérisation capacitive

La structure MCBC est utilisée dans PT1 pour mesurer le changement de capacité en deux étapes. La Fig. 4.1 montre une électrode connectée à la masse et une autre connectée aux drains de la paire n/pMOS. La première étape consiste à enregistrer le courant de charge I_1 à travers un ampèremètre CC (A) pour un canal vide. Par la suite, le total des capacités parasites (C_0) associées aux transistors MOS et aux électrodes peut être représenté par l'équation suivante.

$$I_1 = f \cdot V_{dd} \cdot C_0 \tag{1}$$

où f et V_{dd} sont la fréquence des signaux à impulsions et la tension d'alimentation respectivement. Pour la seconde étape, une solution est injectée dans le microcanal et le courant de charge (I_2) est enregistré. Comme le montre l'Eq. 2, ce courant est proportionnel à la sommation de C_0 avec la variation de capacité ΔC.

$$I_2 = f \cdot V_{dd} \cdot (C_0 + \Delta C). \tag{2}$$

C_0 et ΔC peuvent alors être déduits des Eqs. (1) et (2) pour une valeur particulière de *f*.

Il est important de mentionner que cette puce peut servir de méthode simple pour la caractérisation capacitive de capteurs de laboratoires-sur-puce. Cette procédure de caractérisation sert à extraire les changements de capacité ainsi que les capacités parasites générées. Les données extraites pourraient alors servir de modèle simplifié pour la conception et l'optimisation de circuits intégrés dédiés à des applications de laboratoire-sur-puce. Des outils de CAO basés sur les éléments finis, tel que FEMLab, sont typiquement utilisés pour l'analyse de telles variations de capacité. Cependant, en plus des dimensions physiques, la modélisation d'applications de la sorte nécessite beaucoup de données préliminaires, tel que des données physicochimiques et des traitements qui sont rarement disponibles. Donc, une méthode de caractérisation expérimentale qui pourrait établir des analyses précises en se basant sur des données préexistantes serait un atout.

B. Capteur capacitif intégré

Pour remplacer le dispositif de mesure externe (A dans la Fig. 4.1) avec des circuits intégrés, la première étape a été d'implémenter un capteur capacitif et de concevoir un circuit d'interface dans PT2.

- *Analyse*

L'unité de base du circuit d'interface proposé (UCI) est illustrée dans la Fig. 4.2. Dans ce circuit, un miroir de courant composé de M_3 et M_4 est utilisé pour détecter et amplifier le courant de charge (I_S), qui est converti en tension dans le condensateur

d'intégration (C_{in}). Une fois que le signal $\phi 1$ est bas, la tension sur C_S (V_S) commence à augmenter en suivant l'Eq. (3).

$$C_S \frac{dV_S}{dt} = K_x \cdot (V_{gs} - V_{TP})^2 \tag{3}$$

où K_x dépends des paramètres du procédé, et V_{gs} et V_{TP} sont la tension entre la grille et la source et la tension de seuil d'un transistor à effet de champ à canal p respectivement. Aussi, les résistances d'activation de M_1 et M_2 ont été négligées. En remplaçant V_{gs} par $V_{dd} - V_S$ dans (3), et en considérant $V_S = 0$ à $t = 0$ (décharge) quand $\phi 1$ et $\phi 2$ sont hauts, Vs est donné par l'Eq. 4

$$V_S = (V_{dd} - V_{TP}) - \frac{(V_{dd} - V_{TP})C_S}{K_x (V_{dd} - V_{TP})t + C_S}. \tag{4}$$

Tel que montré par cette équation et par la Fig. 4.2, et en supposant que les courants de charge transitoires auraient assez de temps pour s'établir durant la période de l'onde carrée, V_S augmentera en conséquence jusqu'à une valeur d'une tension de seuil à court de la tension d'alimentation. À ce point, M4 est bloqué. Dans ce cas, la tension à travers le condensateur d'intégration est

$$V_{out} = \frac{W_4 / L_4}{W_3 / L_3} \cdot \frac{(\Delta C + C_0)}{C_{in}} \cdot V_S. \tag{5}$$

où W_4/L_4 et W_3/L_3 sont les rapports largeur/longueur de M_4 et M_3 respectivement. Il est clair que la gamme dynamique de V_{out} reste limitée puisque $Co >> \Delta C$. Pour cela, une empreinte du circuit d'interface est utilisée pour générer un courant de référence I_R. Comme le montre la Fig. 4.2, ce courant est reflété au nœud de sortie à travers un autre

miroir de courant et soustrait I_S. À cause de sa symétrie et de son opération différentielle, V_{out} est exprimé par l'Eq. 6

$$V_{out} = \frac{\Delta C}{C_{in}}(V_{dd} - V_{TP}) + V_{off}. \tag{6}$$

La tension de décalage résiduelle V_{off} est en principe due au défaut d'appariement des miroirs de courant et des circuits de MCBC. Pour réduire l'effet de cette erreur, un miroir de courant ajustable est utilisé, tel que montré dans les Figs. 4.3a et 4.3b. Pour chaque entrée numérique D1-Dm ($D_{1\text{-}m}$) montrées dans la Fig. 4.3b, un certain courant (I_R) est tiré de M_{C1}-M_{Cm} qui ont des rapports largeur/longueur donnés par l'Eq. 7.

$$\frac{W_{13}}{L_{13}} = 2 \cdot \frac{W_{C1}}{L_{C1}} = 2^2 \cdot \frac{W_{C2}}{L_{C2}} \ldots = 2^m \cdot \frac{W_{Cm}}{L_{Cm}} \tag{7}$$

Pour cette architecture, les données de l'entrée numérique sont générées à partir d'un circuit externe à la puce qui sera décrit dans la section suivante. Aussi, tel que montré dans la Fig. 4.3a, pour améliorer l'excursion de tension de la sortie V_{out} et pour réduire la fuite de C_{in}, notamment pour les impulsions d'horloge à basse fréquence, un miroir de courant à large excursion de tension, wide-swing, (M_5-M_{10}) est utilisé à la place du simple miroir de courant dessiné avec des lignes découpées dans la Fig. 4.3a. D'un autre côté, M_{14} et M_{15} forment un amplificateur à source chargée qui isole le nœud d'intégration des capacités parasites des étages subséquents. Il faut signaler que la tension V_{off} est éliminée automatiquement par la soustraction de deux mesures consécutives précédant et suivant l'injection d'analyte. Par la suite, elle n'a aucun effet important sur la précision de la détection capacitive.

C. Système de détection capacitif

Tel que montré par la Fig. 4.4, un système de détection a été conçu et incorporé dans PT3 ayant quatre électrodes interdigitées comme condensateurs de détection (C_{S1}-C_{S3}) et de référence (C_R), trois UCIs, un miroir de courant ajustable (voir Fig. 4.3), et un simple ampli-tampon à gain unitaire. Cette puce nécessite des signaux d'entrée-sortie analogiques (V_{out}, V_a, V_b and V_c) et numériques ($D_{1\text{-}m}$). Pour cette architecture, les électrodes de détection sont sélectionnées par des lignes d'adressage numérique S_1, S_2 et S_3 ($\check{S}$), tandis que la logique de contrôle englobe la réinitialisation et les signaux d'horloges ϕ1-ϕ2.

Une procédure de calibration est préalablement nécessaire à l'injection d'analyte en repérant la valeur optimale des données d'entrée $D_{1\text{-}m}$. Pour cela, un module externe à la puce est commandé pour commencer la calibration du capteur avant la prise d'une mesure. Ce module est implémenté dans une plateforme FPGA comprenant un convertisseur analogique-numérique (CAN). La sortie numérique du CAN ($\tilde{U}$) est employée comme critère de décision dans l'algorithme de calibration exécuté par le module externe à la puce. Pour chaque période de l'horloge ϕ1, si V_{out} dépasse une tension de seuil (V_{th}), $D_{1\text{-}m}$ est incrémenté jusqu'à ce que la valeur requise soit atteinte. Les rapports largeur/longueur de M_{C1}-M_{C8} indiquent qu'I_R est initialement inférieur à I_S, ce qui implique que le procédé de calibration commence toujours avec une valeur de V_{out} supérieure à V_{th}. La Fig. 4.4 montre que $D_{1\text{-}m}$, $\check{S}$ et les horloges (ϕ1 and ϕ2) sont fournis par en module externe à la puce implémenté dans un FPGA (AFS600, Actel). Le

signal numérique ($\tilde{U}$) est finalement capté et mémorisé dans l'ordinateur.

D. CAN dédié et efficace

Pour un capteur complètement intégré, il est nécessaire de concevoir un circuit de lecture de données pour l'enregistrement et pour des traitements plus poussés. Dans cette section, suite à notre circuit à noyau-MCBC, nous présentons un CAN simple et efficace conçu en ajoutant quelques dispositifs additionnels au circuit d'interface. Ôtons la réinitialisation (Reset) de la Fig. 4.2 et laissons V_{out} s'élever à chaque période, tel que montré par la Fig. 4.6. V_{out} est comparé à une tension de référence (V_R) et la sortie du comparateur (ζ) est utilisée pour commander l'interrupteur Sw1 qui est placé en série avec une source de courant I_ζ (voir Fig. 4.2 et Fig. 4.3b). Cette configuration met en vedette un simple CAN de premier ordre avec une entrée CC d'un-bit. Ce circuit numérique de lecture de données est implémenté avec un procédé CMOS utilisant un comparateur de tensions track and latch [VAK06] relié au circuit d'interface déjà expliqué. Les simulations suivant le dessin des masques (post-layout) montrent des flux d'impulsions différents pour différentes valeurs de ΔC (Fig. 4.8). Tel que montré par la Fig. 4.8, la moyenne de chaque séquence (le nombre de uns par le nombre d'impulsions dans chaque séquence) est proportionnel à ΔC. Suite à ces résultats, nous pouvons déduire que le CAN à bas coût proposé est similaire à un convertisseur sigma-delta conventionnel à entrée CC.

III. PROCÉDÉ DE FABRICATION MICROFLUIDIQUE PAR ÉCRITURE DIRECTE

Nous détaillons dans cette section l'encapsulation microfluidique proposée. Le procédé comprend six étapes décrites dans le texte suivant et illustrées dans la Fig. 4.1.

A. L'encapsulation des plots de connexion et des fils

Préalablement au début des trois étapes du procédé de fabrication microfluidique par écriture directe, les conducteurs doivent être couverts pour éviter le contact direct avec les fluides dans les canaux. Pour cela, une résine d'époxy partiellement polymérisée (Epon 828, Shell Chemical) est dispensée (Champion 8200 dispenser, Creative Automation Co.) sur la puce encapsulée pour encapsuler les fils de connexion. À cause de la tension superficielle et de la haute viscosité de l'époxy mi-polymérisé, celui-ci coule aisément autour des fils de connexion mais s'arrête prêt des pastilles (pads). La puce sans boîtier reste alors découverte – ce qui est nécessaire pour la détection. Les points de la trajectoire (x,y,z) de déposition d'encre doivent être initialement mesurés et programmés dans le système dispensateur commandé par un robot.

B. Déposition d'encre

De l'encre organique ayant une consistance de pâte (un mélange de vaseline et de cire microcristalline [GHA07i]) est extrudée (Ultra® 2400, EFD Inc.) à travers une microbuse pour être ensuite déposée sur le substrat. Pendant l'extrusion, un robot de micro-positionnement (Model I&J 2200, I&J FISNAR Inc.) déplace la buse à travers la trajectoire désirée (partie A, section II). Cette structure d'encre sacrificielle (Fig. 5.1b montre un filament d'encre) garde sa forme durant l'encapsulation d'époxy de la section

E. Les paramètres suivant doivent être modulés pour contrôler ce procédé : la pression d'air (P) appliquée pour extruder l'encre à travers la microbuse, la vélocité de la microbuse en mouvement sur la trajectoire (v), la hauteur relative entre la buse et le substrat (H) et la fraction microcristalline du mélange d'encre organique (M).

C. Connexion fluidique

À la suite du procédé de déposition d'encre, les armatures fluidiques à micro-échelle sont placées et fixées aux endroits requis près de l'encre déposée sur la puce avec quelques gouttes de colle thermofusible. Une déposition additionnelle d'encre fugitive de l'armature est nécessaire pour remplir l'espace entre le filament d'encre et la connexion fluidique, ainsi que pour prévenir l'infiltration de l'époxy dans l'armature durant le procédé d'encapsulation (voir "gap" dans la Fig. 5.1c).

D. Barrage fugitif

Un autre procédé de déposition d'encre est entrepris dans la surface de contour prédéfinie de l'encapsulation d'époxy. Ce barrage fugitif peut être retiré facilement pendant l'étape d'enlèvement de l'encre (f).

E. Procédé d'encapsulation et de remplissage d'encre

Dans cette étape, une résine d'époxy à basse viscosité est dispensée sur l'encre déposée à l'intérieur de la surface de contour d'encapsulation. La polymérisation de la résine s'effectue à température ambiante, en 24 heures. Ce procédé d'encapsulation d'époxy crée un lien puissant et hermétique sur la surface irrégulière de la puce sans boîtier. Il est aussi possible qu'un canal découvert peut être créé en utilisant un volume réduit

d'époxy. Ce type de canaux est nécessaire pour la déposition des couches de post-détection sélective et pourrait être recouvert plus tard.

F. Enlèvement d'encre et injection d'analyte

L'encre fugitive est fondue à ~75°C et propulsée sous une faible dépression ou sous la pression de l'air. Ensuite, de l'eau chaude est injectée dans le canal pour enlever les résidus d'encre. Suite à cette étape, une solution analyte peut être injectée directement dans le microcanal fabriqué sur la puce microélectronique pour des fins de détection.

IV. Montage de mesure, fabrication de puce et microfluidique

Dans cette section, nous décrivons la fabrication des puces, le montage de mesure et l'encapsulation microfluidique.

A. Fabrication de puces

Les puces microélectroniques de capteurs (PT1, PT2, PT3) ont été fabriquées par la Taiwan Semiconductor Manufacturing Company (TSMC) avec le procédé CMOS 0,18 micron. Les Figs. 3.9a et 4.10a et 4.10b montrent les microphotographies des deux puces. Il faut mentionner que la technique de gravure de pastilles dans le procédé CMOS a été utilisée pour enlever les couches de passivation entre les doigts des électrodes pour augmenter la sensibilité [GHA07g]. Nous pouvons observer cela ainsi que le manque d'uniformité du à cette technique de gravure dans l'image MEB (Fig. 4.10d). Tel que vu dans la Fig. 4.10d, le condensateur d'intégration C_{in} et le miroir de courant ajustable occupent la moitié de la surface du circuit d'interface; cependant, il n'est pas nécessaire de les répliquer si nous avons une matrice de capteurs capacitifs. De plus, les dimensions

des électrodes de détection C_S dans PT1 et PT2, ainsi que les électrodes de détection et de référence (C_R, C_{S1}, C_{S2} and C_{S3}) dans TP3 sont montrées dans le Tableau 4.1 (TP2 dans ce Tableau) pour $W_1=W_2=W$.

B. Procédé de fabrication microfluidique par écriture directe (PFED)

Suite à ce procédé (PFED), les canaux fluidiques sont construits sur les puces de capteurs (PT1, PT2 et PT3). L'image obtenue avec le microscope optique des microcanaux sur PT2 et sur la plateforme hybride microfluidique/PT1 sont l'objet des Figs. 3.9b et 5.4.

C. Montage de mesure multidisciplinaire

Tel que montré par la Fig. 3.12, un microscope stéréoscopique est utilisé pour observer la solution qui est injectée par une pompe seringue dans l'orifice d'entrée du canal microfluidique. Simultanément, l'oscilloscope (Digital Phosphor Oscilloscope, TD57154, Tektronix) surveille le V_{out} périodique. Il a déjà été évoqué qu'une plateforme FPGA soutient la puce de capteur pour l'enregistrement de données et pour aider à trouver les conditions de mesure optimales.

V. RÉSULTATS DE MESURE

Les simulations suivant le dessin des masques (post-layout), les caractéristiques électriques, ainsi que les résultats des tests chimiques sont présentés dans cette section.

A. Simulations

Des simulations post-layout avec SpectreS ont été utilisées pour valider l'architecture

présentée dans cette section (voir Fig. 4.2) et pour atteindre la performance optimale. La Fig. 3.7a montre la forme d'onde de la tension de sortie de l'intégrateur C_{in} durant le cycle d'horloge pour plusieurs ΔCs. Tel que prévu, V_{out} augmente rapidement à une valeur proportionnelle à ΔC. La linéarité de la variation de V_{out} (ΔV_{out}) par rapport à ΔC est soulignée dans la Fig. 4.5 qui est en accord avec l'Eq. (6). Il faut signaler que l'extraction des capacités post-layout donne $C_0 \approx 70.2$fF pour chaque électrode de référence et de détection (C_R et C_{S1}-C_{S3}).

Cette figure montre qu'un changement de 20% W_1, W_2 et W_5-W_8 affecte de façon substantielle V_{off} avec aucun changement dans la sensibilité. Cependant, il est prévisible que les défauts d'appariement de W_3 et W_4, affectent V_{off}, ainsi que la sensibilité. Bien sûr une configuration similaire à la calibration peut être utilisée pour compenser cette erreur en ajustant le gain de courant (M_3-M_4). Ces simulations considèrent un gain de courant de 10 avec un condensateur d'intégration de 1,2 pF. D'ailleurs, d'après les résultats de simulation, pour $C_{in} < 250$fF, V_{out} ne suit pas l'Eq. (6) [GHA05a]. Ceci peut être possiblement attribué à des capacités parasites sur ce nœud. Les résultats de simulation dans la Fig. 4.5 montrent l'importance de l'annulation du décalage pour obtenir une gamme dynamique pleine gamme pour la sortie. Ils montrent aussi que la sensibilité du circuit d'interface est d'environ 530mV/fF, à C_0=70 fF.

B. Caractérisation d'électrode de détection

Suite à la discussion dans la section II-A et aux étapes de mesure de PT1, le courant de charge différentiel (I_1-I_2) par rapport à la fréquence pour quatre trois solutions est donné

dans la Fig. 4.11a. Ces solutions sont utilisées pour mesurer les variations de capacité. Ces solvants sont le dichlorométhane, l'acétone, le méthanol et l'eau déionisée. Les constantes diélectriques des ces solutions sont 9,1, 20,7, 30,4 et 80,4 respectivement à 69°F. Il faut dire que la conductivité du dichlorométhane comme solvant non-polaire est presque nulle et les basses conductivités de l'eau DI (0.04 μS/cm) et de l'acétone (0.02 μS/cm) peuvent être négligées. Dans ce travail, V_{dd} garde sa valeur maximale (1,8V) et la fréquence est variée jusqu'à quatre décades pour montrer la linéarité de l'Eq. (1) pour la caractérisation de capacité dynamique. Pour cette large gamme de fréquences, les résultats de mesures sont montrés sur des échelles logarithmiques. Les droites parallèles dans la Fig. 4.11b sont en accord avec l'Eq. (8) qui est déduite des Eqs. (1) et (2).

$$\log(I_2 - I_1) = \log f + \log(V_{dd} \cdot \Delta C) \tag{8}$$

Alors, le changement de capacité (ΔC) associé à chaque solution peut être extrait de la continuation de ces courbes. D'ailleurs, dans cette représentation logarithmique, pour les différentes solutions, la largeur de l'origine (A, B, C et D) est différente tandis que la pente de ces courbes est la même. La Fig. 4.11b montre le ΔC extrait par rapport à la constante diélectrique. Chacune des valeurs mesurées dans la Fig. 4.11b est obtenue par le moyennage des cinq mesures répétées de suite suivies par une procédure de nettoyage (voir la section IV-B).

Des mesures similaires sont prises pour extraire C_0 pour cinq échantillons de puces avec aucune solution introduite sur les électrodes (Fig. 4.11c). La différence entre les C_0 extraites des différentes puces peut être le résultat de l'irrégularité de la gravure de

pastilles (pad-etching) (voir Fig. 4.10d.) et/ou la tolérance du procédé CMOS. Ces résultats témoignent que PT1 peut être utilisée comme capteur à complexité réduite pour laboratoires-sur-puce.

B. Tests chimiques

Suite à la procédure de calibration établie dans la section II-B avec un microcanal vide, V_{off} est minimisé. Bien sûr, pour un V_{off} plus bas plus que huit bits de calibration (D1-D8) doivent être considérés dans la conception de circuit. Tel que prévu, V_{out} augmente (f=1kHz) quand les électrodes interdigitées sont exposées à des solutions diélectriques (dichlorométhane et méthanol) et diminue pendant la période de décharge (voir Figs. 4.12a-b). La tension CC de V_{out} peut être réglée à travers V_c (voir Fig. 4.2b).

Un procédé de nettoyage avec eau chaude, insufflation d'air et traitement de température est fait entre les mesures avant la réinjection de solution. Pour évaluer le temps de réponse du capteur, la moyenne des données enregistrées de trois électrodes est enregistrée pendant 50 secondes. Cette procédure est répétée pour différentes solutions avec des procédures de nettoyage entre les mesures. La Fig. 4.13 montre qu'une fois l'analyte est introduit dans l'électrode de détection, la tension correspondante apparait à la sortie du capteur aussi vite que permis par le circuit d'interface. Dans ce travail, la variation brusque de la sortie du capteur dans la Fig. 4.13 est due à la mesure directe de l'analyte sans ajouter une couche de détection sur les électrodes de détection. Par exemple, l'utilisation d'une couche de détection PEUT pour la détection chimique dans

la phase gazeuse cause une sensibilité linéaire pour une gamme dynamique plus large de concentrations d'analytes et donc une réponse plus lente du capteur [HAG02]. Alors, avec une couche de détection additionnelle, le temps de réponse peut dépasser celui des résultats montrés dans cette section.

Dans un autre test, ΔV_{out} correspondant à C_{SI} devient 650mV et 800mW pour l'injection de DW et d'eau saline conductrice respectivement. Au fait, pour les constantes diélectriques plus élevées (constante diélectrique de DW $\approx$ 80.5), nous prévoyons un ΔV_{out} plus élevé. Mais pour le cas de l'eau saline injectée, le ΔV_{out} élevé est du à l'effet d'une grosse capacité parasite à travers la couche de passivation [GHA07h].

Il est important d'évoquer que la plupart des solutions biologiques sont ioniquement conductrices; cependant, pour les applications mentionnées plus tôt (ex. reconnaissance d'anticorps-antigènes, détection d'hybridation, etc.), après les réactions biologiques correspondantes, un nettoyage avec une solution non-conductrice (ex. Méthanol [STA06]) et parfois un traitement de température [BAL05], sont effectués pour préparer le capteur pour une mesure purement capacitive. Il peut être utile de prendre avantage du comportement de ce capteur envers les solutions conductrices pour surveiller si le procédé de rinçage est performé parfaitement et donc si le capteur est prêt pour une mesure capacitive, ou bien si quelques ions existent encore – ce qui nécessiterait plus de préparation.

VI. CONCLUSION

Nous avons décrit quelques circuits d'interface pour des capteurs capacitifs statiques utilisés pour la détection avec laboratoire-sur-puce. Une MCBC à complexité réduite et haute précision a été utilisée pour un capteur capacitif CMOS laboratoire-sur-puce. Les capteurs capacitifs basés sur la MCBC ont été implémentés dans le procédé CMOS 0.18μm pour la détection de liquide dans un microcanal. De plus, nous avons démontré avec succès les résultats expérimentaux utilisant des solutions chimiques standards pour montrer la viabilité du capteur hybride Circuit Intégré/Microfluidique proposé pour maintes applications tel que la surveillance d'analyte dans le canal, la microfluidique numérique, la détection cellulaire par analyses anticorps-antigènes, les micromatrices d'ADN complètement électroniques, ainsi que la détection de gaz chimique et de solvant organique pour la surveillance environnementale. Les circuits d'interface à bas coût proposés offrent de bonnes alternatives aux matrices de capteurs capacitifs complètement intégrées qui sont indispensables pour les laboratoires-sur-puce. Nous avons aussi présenté d'autres circuits (actuellement en étape de fabrication) fondés sur cette méthode basée sur la charge pour encapsuler le système capteur entier dans la même puce.

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LIST OF ABBREVIATIONS

ADC	Analog to Digital Converter
CBCM	Charge Based Capacitance Measurement
CE	Electrophoresis
CIEF	Charge-Injection-Induced Error-Free
CMOS	Complementary metal–oxide–semiconductor
CVC	Capacitance to Voltage Converter
DAC	Digital to Analog Converter
DEP	Dielectrophoresis
DNA	Deoxyribonucleic Acid
DWFP	Direct Write Fabrication Process
ESD	Electrostatic Discharge
ELISA	Enzyme Linked Immunosorbant Assay
FPGA	Field Programmable Gate Array
ISFET	Ion-Sensitive Field Effect Transistor
ITO	Indium Tin Oxide
LoC	Laboratory-on-Chip
MEMS	Micro-Electro-Mechanical Systems
MOSFET	Metal-Oxide-Semiconductor-FET
PCR	Polymerase Chain Reaction
PEUT	Polyetherurethane
SC	Switch Capacitor
SEM	Scanning Electron Microscope
SPRS	Surface Plasmon Resonance Sensor
TC	Test Chip
TSMC	Taiwan Semiconductor Manufacturing Company
UIC	Unit of Interface Circuit

LIST OF SYMBOLS

μm	Micrometer
ξ	One-bit DAC input bit
ε_r	Dielectric constant
Φ_i ($i=1,2,3,4$)	Clock pulses
$S_{\Delta V/\Delta C}$	Sensitivity of output voltage versus ΔC
ΔV_{out}	Output voltage variation
ΔC	Capacitance variation
A_I	Current gain
A_V	Voltage gain
C	Capacitance
C_{in}	Integrating capacitance
C_R	Reference capacitor
C_S	Sensing capacitor
D_i ($i=0,1,..$)	Calibration bits ($D_{1\text{-}m}$)
f	Clock pulse frequency
I	Current
I_R	Reference current
I_S	Sensing current
I_ξ	One-bit DAC current
$K\Omega$	Kilo-ohm
$L_i (i=1,2,..)$	Channel length
MHz	Megahertz
M_i ($i=1, 2...$)	Transistors
ms	millisecond
N	Period of output sequence

P	Performance factor of sensor
q_n	Output sequence
R	Resistance
$\check{U}$	Decoded output sequence
V	Volt
V_R	Reference voltage
V_{out}	Output voltage
V_{th}	Threshold voltage
V_{off}	Offset voltage
V_{dd}	Power supply voltage
W_i (i=1,2…)	Channel width

THESIS ORGANISATION AND CONTRIBUTIONS

1.1 Overview

The growing number of chronic diseases such as cancer, the absence of specific and efficient treatments for several viral and bacterial diseases and the absence of efficient and fast method of environmental monitoring has created the need of rapid identification and diagnosis. Lab-on-Chip is a sophisticated method to produce real-time, multiple and highly sensitive analysis at the point-of-care, while providing for doctors and patients. This multidisciplinary research approach calls for a convergence of microelectronic and microfluidic technologies with conventional techniques in biochemistry. Standard CMOS process is a technological platform to realize such LoC systems offering the advantages of well studied circuits and embedded sensors/actuators. The research work in this thesis is focused on a CMOS capacitive sensor integrated with microfluidic channels for LoC applications.

1.2 Research contributions

The main contributions on this thesis have already been reported in several peer-reviwed scientific journals and international conferences. In this section a summary of these contributions is put forward.

We presented in [GHA05a] and [GHA05d] new design methodologies for charge based capacitive sensors. Based on the discussions reported in these papers, the charge based capacitance measurement can be used for LoC applications and the process mismatch error is not a limitating factor in detecting minute capacitance variation resulting for the

biochemicals in proximity of sensing electrodes. Of course this error should be cancelled using a calibration procedure to improve the dynamic range of sensor's output as discussed in [GHA06b]. Also, in [GHA07g], an array of capacitive sensors was reported using CBCM structure. The measurement results of our proposed core-CBCM sensor circuit were also reported in [GHA07b]. We have already reported a complete capacitive sensor system design including a simple ADC for LoCs in [GHA07b].

A new microfluidic packaging method was presented in [GHA05b], [GHA06a]. We reported the direct-write assembly as an efficient method for the fabrication of microfluidic structure on CMOS chip. In the later report, the advantages of DWFP for creating of three dimensional microfluidic components have been discussed.

Since this thesis is organised based on the published or submitted journal papers, we will provide the details of these articles in chapter 1-5. A complete list of our contributions in this thesis can also be seen in our references [GHA05]-[GHA07].

1.3 Thesis organisation

In chapter 1, we put forward a comprehensive literature review of CMOS based sensors/actuators, in particular on-chip capacitive sensors for LoC applications. The main objective of this review is to highlight the engineering aspects of LoC applications by exploiting the advantages of CMOS process, microfluidic fabrication techniques and classical biochemistry. We present the main methodology of our approach using direct-write microfluidic fabrication process and the primary design of our proposed CMOS capacitive sensor in Chapter 2.

Chapter 3 reports the analysis of the proposed sensor chip for conductive and non-conductive solutions. We demonstrate the experimental results of implemented sensor chip using different chemical solvents in this chapter. In chapter 4, we put forward on the design, implementation and testing of two sensor chips with different levels of complexity. The first chip is a capacitive test-bed suitable for on-chip characterization purposes where the second chip features an array of capacitive sensors along with required calibration circuitries. In chapter 5, the six-step direct-write microfluidic packaging procedure is described. We demonstrate the experimental results and introduce unique advantages of DWFP for LoC applications in this chapter. Finally, the conclusion of this thesis is presented in chapter 6.

Chapter 1

METHODS AND APPLICATIONS OF CMOS-BASED LOCS

1.1 Introduction

The recent advances in CMOS based LoCs with a focus on capacitive sensors for biochemical diagnostics and environmental monitoring are reviewed in this section. The CMOS-based capacitive sensors consisting of interface circuits and microfluidic components along with functionalized sensing electrodes are detailed for the most important LoC applications. This literature review submitted to the " Journal of Analog Integrated Circuit and Signal Processing, Springer". This paper is reproduced as follows.

1.2 CMOS Based Capacitive Sensor Laboratory-on-Chip: A Multidisciplinary Approach

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ABSTRACT

In this paper, we review the recent advances of CMOS-based capacitive sensors for Lab-on-chip (LoC) applications. LoC design is a multidisciplinary approach of adapting classical biochemical assays to a miniaturized platform by exploiting advances in microelectronic and microfluidic technologies. By offering low cost and integrated devices, CMOS based LoCs could be amenable to a large number of biological and biochemical assays for disease diagnostics and biotechnology in the near future. While an exhaustive, all-encompassing review of CMOS-based LoCs is beyond the scope of this review, we have focused on the design and implementation of CMOS-based capacitive sensor LoCs for the most important biochemical applications. For each application, the corresponding biochemical sensing layer, interface circuit and microfluidic packaging technique are discussed based on the recent literature studies.

Keywords: CMOS, Capacitive Sensor, Lab-on-Chip, Bio-functionalized sensing layer, Microfluidic Packaging.

I. INTRODUCTION

A holistic system-based approach to LoC design seamlessly integrates microfluidic, microelectronic with biochemical reagents and reaction on a miniaturized platform. LoCs have attracted the attention of researchers for the miniaturization of biological assays for several applications such as point of care, disease diagnostics and in-situ environmental monitoring [1]. Fully automated LoCs would allow the advantages of rapid, low cost, portability, easy handling and low sample consumption. Additionally, standard CMOS

process offers the advantage of highly precise on-chip active circuits, embedded sensors/actuators and, as such, is a good alternative to play essential roles for the sensing of bioparticles. Owing to the exponential shrinkage of minimum feature sizes, today it is possible to design complex integrated circuits of the size of a cell to readout the output signals of capacitive sensors.

Many efforts have been made on implementation of biochips with a massive parallelism for DNA detection. The first DNA chip or so-called microarray commercialized by Affymetrix (GeneChip® Technology) in the late 1980s could be considered the first applicable Lab-on-chip for diagnostic purposes. An optical scanner is usually used to readout the microarrays. Nowadays, in addition to DNA microarrays, several types of microarrays such protein and antibody microarrays are in the market today and being used for diagnostics or clinical researches. A labelling procedure is frequently performed to bind a suitable fluorescence molecule to the fragment of DNA strand for visualization. As the scanner and relevant processing steps for labelling are expensive, a large effort is devoted to the development of electrical read-out devices which avoid tagging of the DNA target molecules [2]. Such fully electronic DNA detection would significantly enhance portability, as well as on-site sensing, and data processing. Capacitive sensor is recognized as the best alternative for such label free DNA detection [3]. In addition to DNA detection application with huge market potential, capacitive sensors have successfully been used for other LoC applications such as cellular monitoring, chemical sensing and antibody-antigen recognition [4-6].

To date, several capacitive readout techniques with different levels of complexity have been reported for autonomous MEMS based capacitive sensor (MBCS) systems (e.g. accelerometer [7]) but there is a little published literature on the custom design of an on-chip capacitive sensor for LoC applications. Indeed, the design strategy for LoC capacitive sensors differs from that of many other well established MBCS. As an example, for long term and continues sensing in a MBCS, a built-in self calibration module should be incorporated to correct the accumulating errors, whereas LoC capacitive sensors neither suffer from such a problem, nor need such a built-in module. Actually, in these applications, the sensing capacitances in the presence rather than in the absence of analyte are extracted through a differential procedure. For this, a capacitive sensor for LoC applications can be implemented through a simple architecture. This simplicity is an important issue for the design and implementation of a large capacitive sensor array [8] which is not the case of a MBCS application with only one single sensing capacitor.

Until now, several papers presented the fabrication of different types of microfluidic components for LoC applications using surface and bulk micromaching procedures on silicon and glass [9]. But, in this review, the emphasis is placed on low temperature microfabrication processes to build microflouidic devices on CMOS chips without any additional corrosive chemical solutions to damage the underlying circuits. A CMOS-compatible microfluidic fabrication process should be performed on dedicated chip in order to direct biological analyte toward sensing/actuating sites and also to protect the

remaining circuitry and pads from direct contact to solution. It should be mentioned that this protection is necessary to avoid superfluous parasitic capacitance and resistances which might convert the circuit design characteristics.

A generic hybrid IC/microfluidic capacitive sensor is illustrated in Fig. 1.1 including microfluidic components to direct the fluid toward sensing sites, functionalized sensing electrode to transduce the biological quantities into capacitance changes and finally microelectronic devices to detect the minute capacitance changes. Table I presents a summary of published articles on CMOS-based capacitive sensors for LoC applications. Of course, in the recent years, a variety of capacitive techniques have been put forward for the detection of bioparticles, but only a few articles reported the fully design and implementation of CMOS-based capacitive sensors for bio-particle detection purposes. More details about this table are given in the next sections.

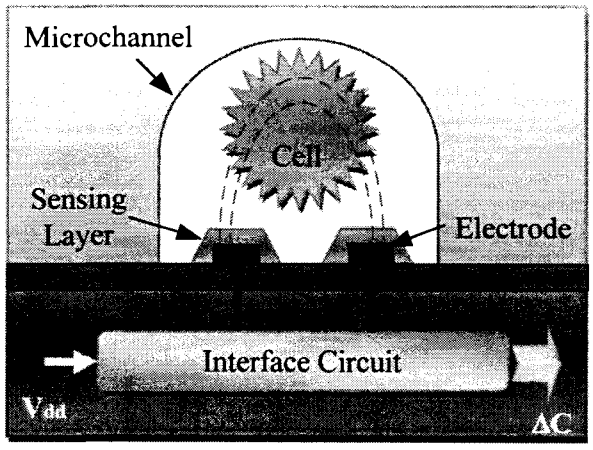


Figure 1.1. An illustration of hybrid microfluidic/ CMOS capacitive sensor for LoC applications (Vdd and ΔC are the power supply and sensing capacitance variation respectively).

Table I: A summary of CMOS based capacitive sensor LoCs reported in the recent years

Application	Sensing Electrode	Circuit	Microfluidic	CMOS	Year	Ref.
Cell Monitoring	Top Most metal layer, passivation layer	Switch Capacitor	Adhesive technique	0.5μm	2007	[19]
Cell localization	Top Most metal layer, passivation layer	Switch Capacitor	Adhesive technique	0.35μm	2004	[8], [33]
Virus detection	Thick metal layer, silicon oxide insulation layer, antibody immoblization	[1]DRAM Method	Rapid Prototyping	1.5μm	2005	[17]
DNA detection	Gold electrode, DNA immobilization	Core CBCM	Rapid Prototyping	0.5μm	2006	[15]
DNA detection	Gold electrode, DNA immobilization	[3]Basic Method	Rapid Prototyping	0.18μm	2007	[22]
Organic solvent sensor	Top Most metal layer, pad-etched passivation layer, PEUT layer	Switch Capacitor	Adhesive technique	1.2 μm	2002	[20]
Organic solvent sensor	Top Most metal layer, pad-etched passivation layer	Core CBCM	[2]DWFP	0.18μm	2007	[21]

1 Random Access Memory, 2 Direct-Write Microfluidic Fabrication Process

The remainder of this paper is organised as follows. In section II, the formation of bio-chemo-functionalized coatings on sensing electrodes is discussed for four important applications. The recent published design methodologies of capacitive interface circuits for LoC applications are put forward in section III. A review of microfluidic packaging techniques for CMOS sensors ia presented in section IV. This section is followed by a brief summary in section VII.

II. DIRECT BIO- CHEMICAL FUNCTIONALIZED SENSING ELECTRODES

In this section four different types of capacitive affinity biosensors are discussed. For

each instance, the biological/chemical principle, practical considerations and limiting factors on CMOS process are put forward.

A. Hybridization Detection

The genetic information is stored in DNA double-helical molecules confined in cell nuclei. A DNA code is a long and detailed message that instructs the cell how to make its vital proteins. Each code consists of sequences of four building blocks (A, G, C, T). Prior to reading out the DNA codes, several biological procedures should be accomplished to prepare the DNA sample from the cells as shown in Fig. 1.2. These procedures include cell pre-filtering, fractionation, and focusing in order to separate rare cells (e.g., cancer [10]) from a blood sample and make them ready for bursting. Thereafter, the DNA strands are extracted from the cells (cell lysis) followed by other molecular procedures (e.g. amplification, fragmentation and labelling [11]) to make the sample ready for DNA hybridization.

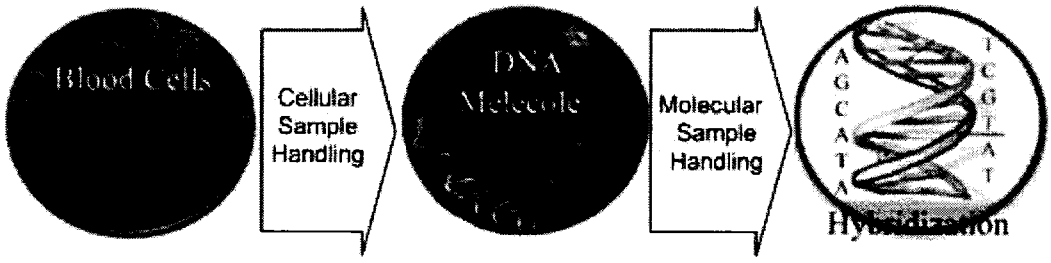


Figure 1.2. Simplified diagram of sequential steps of a genetic diagnostic system.

The hydrogen bonding of two complementary single strands of DNA such as *AGCATA* and *TCGTAT* is called hybridization. Thus, a double-stranded DNA or so-called renaturation process occurs at specific temperature and salinity conditions. In this

process, the known strands are immobilized on a substrate (also called DNA probe) and the unknown strands wander up and down in the sample solution until stopping beside the according probes. The hybridization bond is specific hence hybridization serves as a sequence detection mechanism (see Fig. 1.3a).

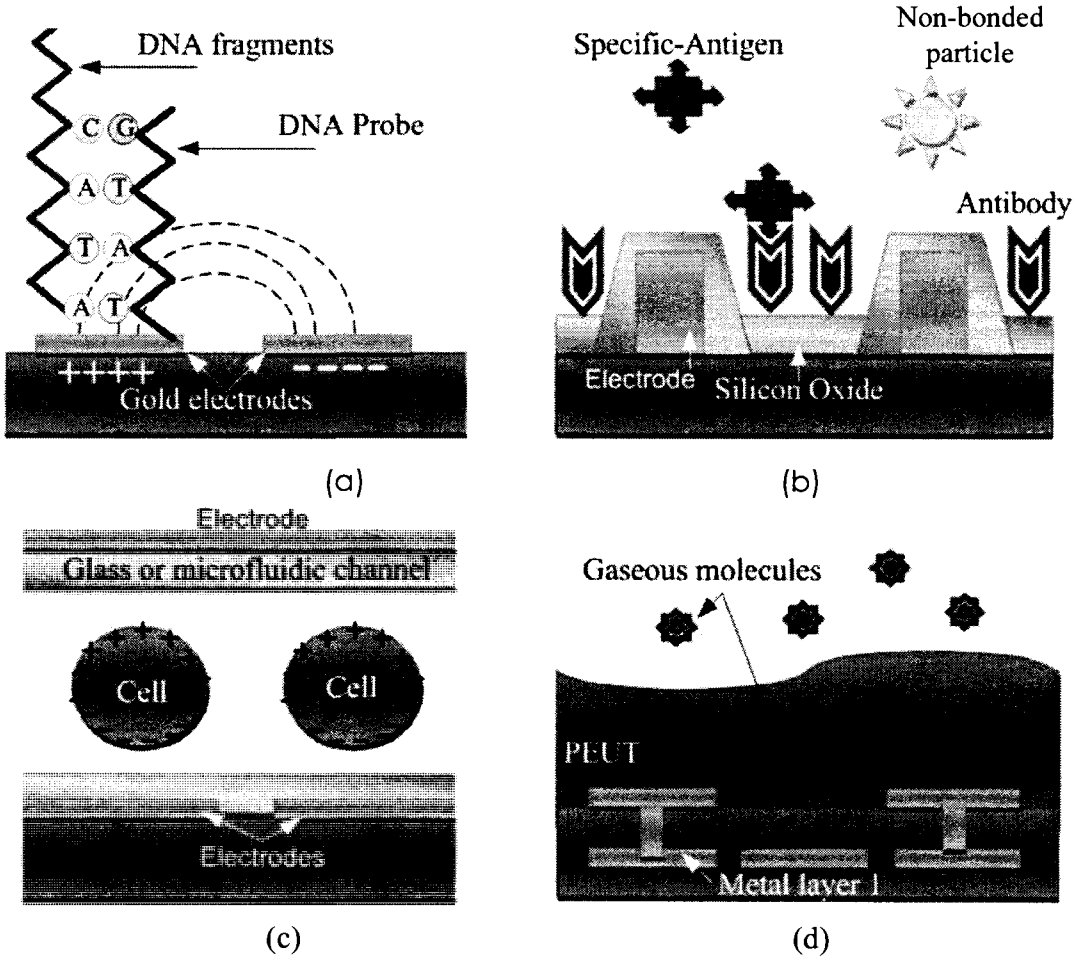


Figure 1.3. Capacitive sensor LoCs: (a) DNA detection, (b) antibody-antigen recognition, (c) cell monitoring and (d) quasi interdigitated electrodes for chemical sensing.

The presence of a double strand in the mixture can be detected optically by fluorescence tags which already labelled onto the input DNA molecules.

However, a decrease in the electrochemical capacitance of an electrode-solution interface after exposing to unknown fragments can also be detected through a low complexity capacitive sensor. Among the efforts to use capacitive sensor for DNA detection, Berggren et al. demonstrated a capacitance variation between 1 mF/cm^2 and 20 mF/cm^2 on the functionalized gold electrodes with 26-base-long oligonucleotides, complementary to the targets [12]. Also Guiducci et al presented a sensing method with two electrodes instead of three electrodes in conventional electrochemistry (counter, reference and ground electrodes) [13]. As a follow up of this work, they reported the realization of an array of gold electrodes and subsequent readout circuitry on CMOS process [14]. For this, a low temperature sputtering method was used to realize gold electrodes on CMOS chips. It should be mentioned, that there are some efforts to immobilize DNA on other materials included in standard CMOS process such as silicon dioxide [15], however, still the direct immobilization of DNA on standard CMOS is an unmet challenging issue to the best of our knowledge.

B. Antibody-antigen recognition

Antibodies are proteins deployed by the immune system to identify and neutralize foreign bodies, such as viruses. A small region at the tip of each antibody is extremely variable, allowing millions of antibodies with slightly different tip structures to exist. Each of these variants can bind to a different target, known as an antigen. When an

antigen binds to an immobilized antibody layer (e.g., unti-human transferrin [16]) on a substrate, a modulation occurs in thickness or dielectric constant parameters that can be detected through a capacitive sensor (see Fig. 1.3b). Of course, surface plasmon resonance sensor (SPRS) is a well established optical method to detect the mass variation resulting from antibody-antigen interaction [17], however, the realization of a technically complicated SPRS on standard CMOS process has not been reported. Moving toward a low complexity approach, Balasubramanian et al performed a capacitive method to detect viruses through standard enzyme linked immunosorbant assay (ELISA) [6]. The antibodies were immobilized on silicon dioxide where thick metal layer's option in CMOS was used to increase the sensitivity of detection. Also, a temperature treatment was performed prior to sensing in order to decrease the ionic conductivity around the sensing sites.

C. Cellular activity monitoring

It has been recognized in bio-electrochemistry studies that the morphological states of biological cells have strong correlation with their electrical properties and also the existing membrane potential can be considered as an indication of living cells [18]. Stomashekar et al reported a CMOS capacitive sensor for cell monitoring based on above mentioned bio-electrochemical observations. As seen in Fig. 1.3c, a surface charge density is carried by living cells [19]. These charges are moved once exposed to an electrical field resulting to a dipole moment. The contact of cells with the passivation layers on top of single electrodes as well as created dipole moment are significantly

detected by a capacitance change (e.g., 1fF capacitance variation on 400 μm^2 electrode [19]). In another effort, a cell detection method has been reported for cell localization using an array of parallel electrodes- one common electrode covering the microfluidic structure, and an array of addressable electrodes on top of a CMOS chip [8].

D. Organic solvent sensors

The detection of organic solvents is critical to monitoring of food, drug, soil and water samples, owing to the toxicity of such chemicals. The different dielectric constants values of solvent can obviously be used as selectivity and/or sensitivity factor for capacitive detection of solvents. Also, a low electrical conductivity is expected for most polar solvents (e.g., [5]). This property can be considered an advantage for capacitive sensors. In addition, the insulation of sensing electrodes drastically decrease the leakage current (due to low conductivity of solvents) and consequently improve the capacitive sensing property. Furthermore, sometime a polymer sensing layer is used on top of electrodes as an interface between electrodes and solvent. Therefore, for gaseous solvents, the density of diffused molecules and consequently the dielectric constants of insulation layer above the electrodes will proportionally vary with respect to the concentration of solvents.

Hagleitner et al proposed a CMOS capacitive sensor for the detection of toluene and ethanol using polyetherurethane (PEUT) as the polymeric sensing layer [20]. As shown in Fig. 1.3d, a quasi interdigitated electrode was employed for higher sensitivity purposes. For this, the passivation layer from the top and in between the electrodes is removed and replaced with PEUT. Another metal layer was used as a stop layer for pad-

etching of passivation layers in between the electrodes. In another effort, Ghafar-Zadeh et al reported a capacitive sensor LoC implemented through 0.18 μm CMOS process for the detection of organic solvents (liquid phase) such as dichloromethane and methanol without any other sensing layer [21].

Based on above discussions, capacitive sensors have an enormous scope of applications in medicine and biotechnology by detecting thousand types of virus, bacteria or organic solvents as well as millions of DNA fragments. These high demand applications could be essential technology drivers for batch production and continued research for new diagnostic devices. Of course, for each application, it is required to implement a specific readout circuit with subsequent sensing layer in order to individually validate the capacitive approaches for different applications and characterize the sensors for further optimization possibilities. This requirement opens a new and extensive field for microelectronic circuit and system designers to contribute in developing this emerging hybrid technology.

II. CAPACITIVE READOUT CIRCUITS FOR LOCS

High-resolution interface circuits in the literature have mostly been reported using switched-capacitor circuitries to realize the capacitance to voltage converter (CVC) along with sigma delta modulators for autonomous sensing systems such as accelerometers [7]. As already mentioned, for a biological or chemical detection, a different interface circuit should be designed and implemented. Such an interface circuit often features an array of

capacitive sensors with addressable sensing electrodes to detect sub femto Farad capacitance changes ΔC (e.g., ΔC=0.2 fF [8]) corresponding to each sensing site. For this, a low complexity and small area interface circuit is required for high spatial resolution sensor arrays. In this section, we describe the circuit topology of the capacitive sensor chips implemented in CMOS process for LoC applications.

A. Basic readout technique

This measurement technique is simply based on the capacitance charging and discharging principle. As shown in Fig. 1.4, a reference current (I_{ref}) is applied to the electrodes in push or pull mode through switches SW1 and SW2.

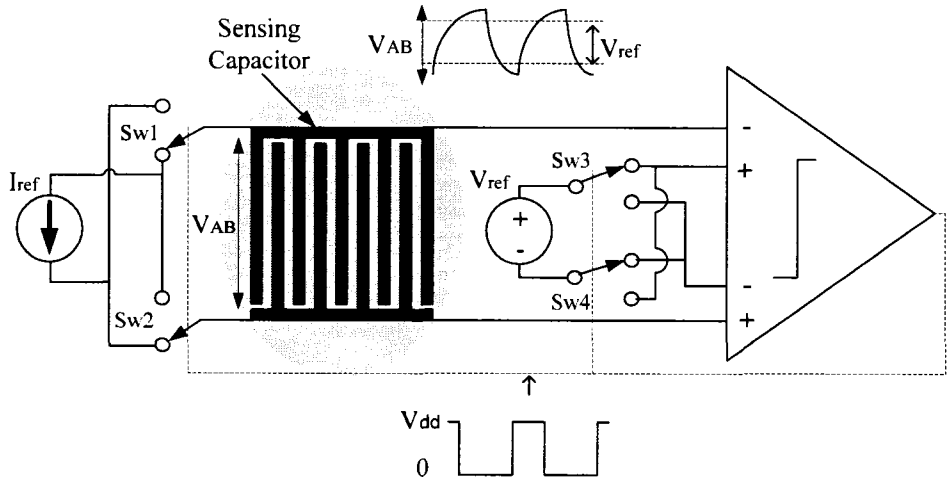


Figure 1.4. Schematic of basic capacitive readout circuit.

This therefore results in a transient voltage waveform on the sensing electrodes. Once, this voltage becomes higher than a reference voltage (V_{ref}), the directions of reference

current and voltage are reverted simultaneously through SW1-SW4. The time constant of this sensing electrode (see Fig. 1.4) is dominated by the capacitive electrode-solution interface. This method was successfully applied by Stagni et al for DNA detection using 0.18 μm CMOS process [22].

B. Core-CBCM methods

The charge based capacitance measurement (CBCM) method was originally proposed as an accurate technique for the characterization of interconnects capacitance in deep submicron CMOS ICs [23]. Fig. 1.5 shows the principle of operation in which two signal pulses (Φ1 and Φ2) are applied to two pairs of n/pMOS transistors in order to frequently charge and discharge the sensing C_S and reference capacitor C_R. Based on this method, the subtraction of charging/discharging currents I_S and I_R measured through high precision DC ammeters is proportional to $\Delta C=C_S-C_R$.

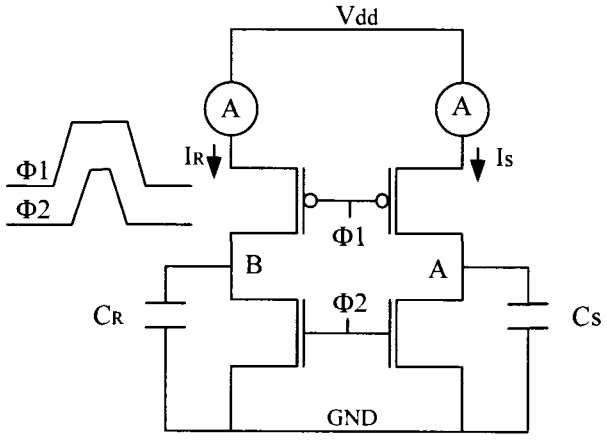


Figure 1.5. Schematic of CBCM structure.

When similar devices are used on both sides of the CBCM structure, the parasitic capacitances associated by M1-M2 are removed through the capacitance subtraction. However, the initial version of CBCM suffers from mismatch and charge injection errors, it was modified in new topologies such as the charge-injection induced error free (CIEF) structure [24]. In order to employ CBCM for DNA detection, Guiducci et al described an integrable readout circuitry using discrete electronic devices [25]. As shown in Fig. 1.6a, the discharging current is conducted through node A into integrating capacitor C_{in} where an opamp keeps a zero voltage on the source of nMOS transistor (M2). Following this work, in order to realize an array of capacitive DNA sensors in a single CMOS chip, they developed an on-chip sensor to detect the presence of DNA on gold electrodes. Fig. 1.6b shows a new CBCM structure with a sensing capacitor in between the drains of transistors, four clock pulses $\Phi 10$, $\Phi 11$, $\Phi 20$ and $\Phi 21$ along with additional p and n channel transistors (Q1-Q4) to exploit full voltage range. In this bridge topology, $\Phi 20$ is applied with a short delay with respect to $\Phi 10$. Additionally, an off-chip circuit including an opamp and a resistor (R) is employed to convert the current signal (I_S) into a readable voltage by a PC [26], with appropriate values of DC biases V^+ and V^-.

As for a fully integrated capacitive sensor, an on-chip circuit is a key requirement. For this, Ghafar-Zadeh et al designed and implemented an on-chip core-CBCM interface circuit suitable for LoC applications [21]. In their proposed circuit, the charging currents of involved CBCM structure are amplified and subtracted before converting to a voltage

in the output node. A linear output response against input capacitance variation (ΔC) was successfully demonstrated through simulation and experimental results.

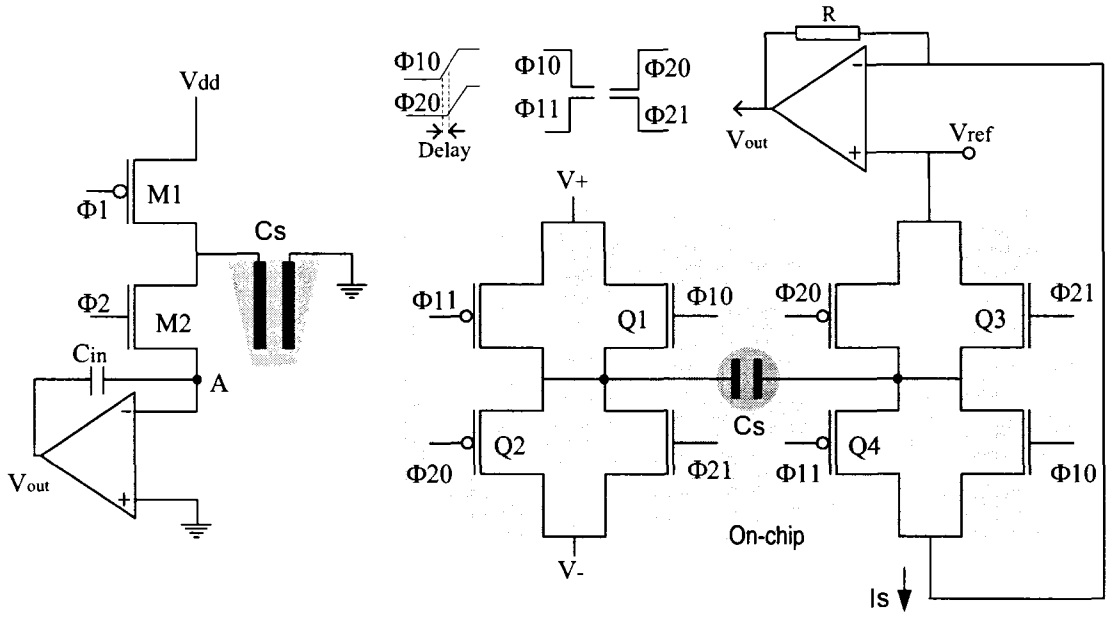


Figure 1.6. A core-CBCM capacitive DNA detection: (a) Off chip realization, (b) on chip realization of new CBCM structure.

C. Switch-capacitor sensing circuit

Switch capacitor (SC) techniques are widely used for different applications especially MBCS. Through these techniques, Guerrieri et al. developed a capacitive sensor array for fingerprint recognition [27] which was later modified for on-chip bioparticle localization [6]. Fig. 1.7 shows a schematic of this circuit including an opamp to maintain the node "A" grounded and therefore the flowing charge toward integrating capacitor proportional to the sensing capacitor. The dynamic range of output voltage of this design is increased by an appropriate value of C_C shown in this figure.

In another effort, Hierlemann et al put forward an integrated capacitive sensor including a second-order sigma delta modulator. This work relies on a differential readout voltage between sensing and reference capacitors, the latter being insensitive to injected chemicals. All the parasitic issues (e.g., temperature drift and aging) affect the reference and sensing capacitor in the same way and therefore cancel out.

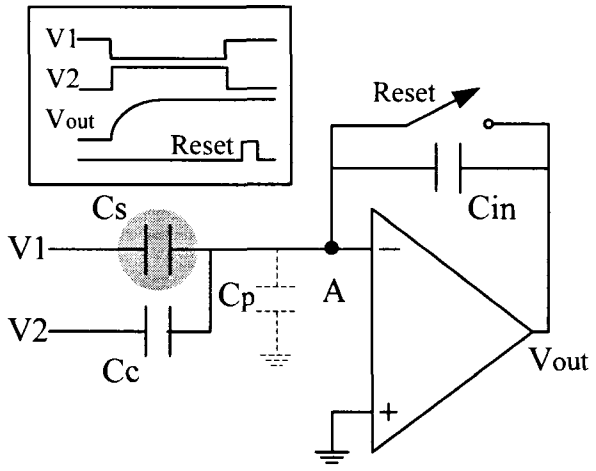


Figure 1.7. Schematic of a conventional SC-based capacitive sensor (C_p is a parasitic capacitance in a MBSC, see chapter 3).

III. MICROFLUIDIC PACKAGING METHODS

The different microfluidic packaging techniques particularly used for CMOS based LoC are discussed in this section.

A. On-chip micromachining procedures

Surface micromachining is one of conventional micromachining techniques which has been reported for on-chip microfluidic fabrication purposes. In this technique, a

conformably deposited material is formed over a sacrificial layer which is subsequently removed by etching to yield a micro- channel or structure. Through this technique, Mastrangelo et al reported the fabrication of plastic capillaries ranging from 0.5-100μm on standard CMOS chip [28].

Another effort for on-chip microfluidic fabrication was performed by Rasmussen et al without using addition material deposition [29]. A shallow microchannel was realized using a standard metal layer (Aluminum) inside the CMOS chip. In fact, using traditional CAD tools, a metal layer is selected and patterned on top of a sensing site as shown schematically in Fig. 1.8a. This conductor (and vias) plays the role of sacrificial layer which is etched using 80% phosphoric acid, 5% nitric acid, 5%acetic acid, and 10% water (see Fig. 1.8b). This procedure was successfully employed to create a monolithic integration into microelectronic interface circuit sensing the flow rate of liquid. A deep microchannel can also be fabricated through opening windows on top of a chip and by using different etchant along with multi metal layers [29].

Recently, Lee et al proposed an IC/Microfluidic hybrid microsystem for 2D magnetic manipulation of individual biological cells [30]. A spin-coated and patterned polyimide was formed on the SiGe IC as the sidewalls of a microfluidic channel. Thereafter, a glass cover slip is sealed on top of the channel sidewalls followed by connecting to inlet and outlet fluidic tube in order to circulate the biological solutions in microfluidic system. This low temperature method can similarly be applied on CMOS sensors for other LoC applications.

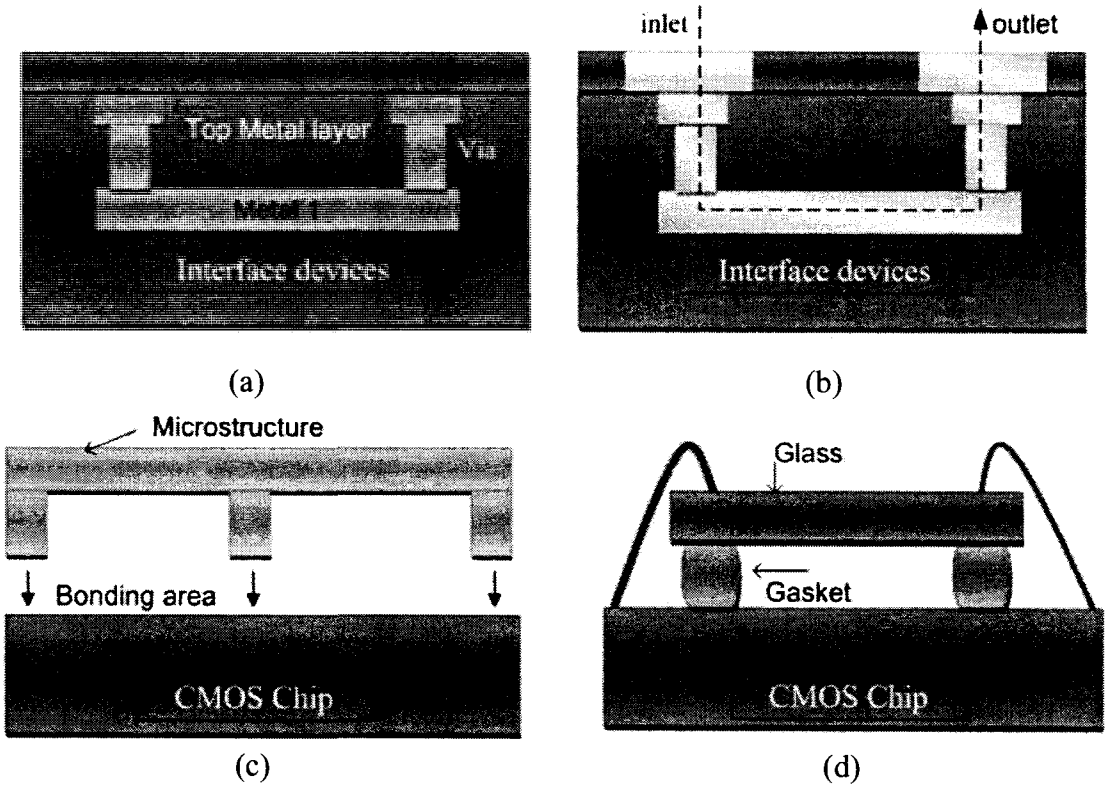


Figure 1.8. On-Chip cmos/microfluidic techniques: microchannel realization through CMOS process (a) before etching and (b) after etching along with an (c) adhesive microfluidic process and a (d) rapid prototyping method.

As these conventional micromachining procedures are labour intensive and expensive, less attention has been paid on these procedures in comparing with adhesive methods.

B. Adhesive methods

A microfluidic structure can be fabricated through a variety of polymeric techniques and adhesively bonded onto CMOS chips using glue or low temperature plasma bonding (see Fig. 1.8c) [31]. It is obvious that by using other bonding techniques with high temperature and/or high voltages, no electronic components can be present on the substrate. Polymer based materials are widely employed using replication techniques.

Three most common replication techniques are injection molding, hot embossing and casting. Mastrangelo et al implemented several epoxy microfluidic devices such as nozzle-diffuser pump and temperature control systems for LoCs through casting and molding processes [32]. Also, hot embossing allows the high precision replication of features from a mould insert into thermoplastic materials. Chartier et al. successfully achieved the fabrication of a polymer-based microfluidic structure through hot embossing and integrated to a CMOS based LoC for bioparticle detection and manipulation [33]. In addition, a follow-up paper describes the fabrication of microfluidic networks on the same CMOS-based system using a dry film resist [34].

A problem associated with these techniques is that adhesive methods can not guarantee a hermetic bonding for all kinds of solutions flowing through the microfluidic structure fabricated on a rough-surface CMOS chip.

C. Rapid prototyping techniques

One important reason to fabricate or bond a microfluidic structure on the top of an IC is to cover the chip by an insulation layer with an opening to access the sensing/actuating electrodes. An epoxy based packaging could be a fast and simple method to do this task. A programmable dispensing system (e.g., Champion 8300 dispenser) is often employed to extrude the epoxy from a nozzle onto predetermined points on sensor chip. By using flip-chip packaging technique, it could also be possible to cover the sensor chip by another covering chip. Medoro et al reported a rapid prototype using simply laboratory devices (see Fig. 1.8d) to create a well on top of dielectrophoresis electrodes for cell

manipulation [35]. Obviously, the rapid prototyping techniques can not be applied for precision applications with a large number of wells and microchannels.

D. Direct-write microfluidic fabrication process (DWFP)

The DWFP is a three-step process- a past-like ink deposition as the sacrificial layer, epoxy dispensing to encapsulate the ink filament and finally, ink removal using vacuum and hot water (see Fig. 1.9) [36].

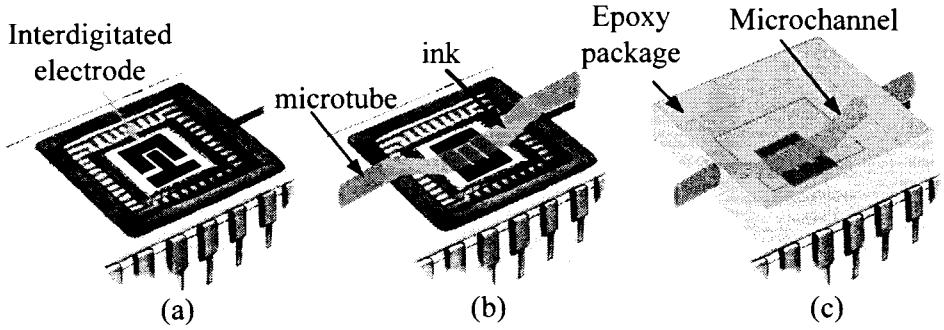


Figure 1.9. Illustration of an on-chip microfluidic packaging procedure using direct-write assembly technique: (a) before packaging, (b) after ink deposition, (c) after epoxy encapsulation and ink removal.

A mixture of petroleum jelly and microcrystalline is used as a fugitive ink which preserve its shape during the process. A three axis robot carries the nozzle along the desired trajectory of ink deposition [37]. This technique has successfully been employed to implement a microfluidic channel on CMOS sensor chip [38].

One common problem among bonding techniques (adhesives and non-adhesives) is the formation of microvoids at the bonding interface. These microvoids can cause the leakage of fluids from microchannel. In general, to avoid microvoids, a surface roughness

within 5 Å and wafer flatness on the order of 5 μm [39] are needed. An important advantage of DWFP against other techniques is the polymerization of epoxy on chip which creates a strong and hermetic bonding without such fabrication errors.

IV. SUMMARY

In this paper we reviewed the recent significant progresses for capacitive detection LoCs. In this survey, we concentrated on capacitive sensor lab-on-chips realized through CMOS process. Three important requirements of such sensor systems including functionalized sensing layer, microfluidic packaging and interface circuit were discussed and the important applications were introduced. It is believed that CMOS capacitive sensors will play a critical role for fully electronic diagnostics due to increasing demands for such low complexity devices.

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Chapter 2

HYBRID MICROFLUIDIC/CMOS PLATFORM

2.1 Introduction

This chapter concerns the implementation of a new platform for LoC applications consisting of a capacitive sensor chip incorporated with microfluidic channel. The design and post-layout simulation results of the proposed capacitive sensor are demonstrated using 0.18 μm CMOS process. In this chapter, DWFP is also presented for the construction of microfluidic channel on CMOS chip. The experiental results are thereafter demonstrated to illustrate the applicability of this technique for LoC applications. This work published in "Journal of Sensors and Actuators A: Physical, Elsevier" is reproduced as follows.

2.2 Novel Direct-Write CMOS-Based Laboratory-on-Chip: Design, Assembly and Experimental Results

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ABSTRACT

In this paper, we propose a Laboratory-on-Chip (LoC) integration technique based on a novel electro-fluidic implementation and packaging procedure for blood-based diagnostics. A LoC-based diagnostic tool is a complex hybrid system consisting of various electrical, fluidic, and biochemical components which are connected electrically and through microfluidic channels on a single platform. The microfluidic structure is performed through a direct-write assembly technique while the conventional wire bonding is used to make the required electrical connections. The microelectronic part of the proposed LoC put forward a high precision capacitive sensor carried out in TSMC's 0.18 μm CMOS process. Experimental results allow us demonstrating the capability of the proposed direct-write microfluidic fabrication process (DWFP) in building polymer-based microfluidic structures on the top of CMOS chips. In addition, the preliminary results of the proposed capacitive sensor show a sensitivity of 250 mV/fF with a noise level equivalent to less than 10 aF where the existing parasitic capacitances can be much larger.

Keywords: Lab-on-chip; Capacitive sensor; CMOS; Direct-write assembly; Microfluidic; Packaging.

I. INTRODUCTION

Multidisciplinary research in life sciences and engineering has led to the emergence of Laboratory-On-Chip (LoC) devices. LoC refers to the miniaturization of analytical

procedures for the detection and analysis of chemical and biochemical substances, on a micro-scale platform. LoCs are promising for many biomedical and environmental applications including the detection of pathogens such as viruses, bacteria and certain proteins for medical diagnostics [1]. Also LoC can be used for quantification of biomolecules like glucose, triglycerides, cholesterol that reside in blood, automated microsystems for genetic diagnosis, portable sensors for food safety and environmental monitoring (e.g. the detection of bacteria in water or food) [2].

Biomolecular and cellular analysis of blood has many clinical and research applications. Among various promising applications, cellular diagnostics can be performed on a small chip. In a way, LoC represents a new generation of impedance spectrometry flow cytometers [3] which may offer new data for cell-based diagnostics, not found in traditional optical flow cytometry. Over the last years, research efforts have been carried out on the miniaturization of chips for DNA analysis and molecular diagnosis using microarrays, with products now available on the markets (e.g. Gene-chip from Affymetrix Inc). While DNA or any other molecular markers have already isolated, purified and characterized through traditional protocols in molecular biology, less attention has been paid to automation and miniaturization of these procedures. Therefore, LoC can not only be used for cell-based diagnostics purposes but can also pave the way for molecular diagnostics through assaying of DNA and proteins extracted from blood cells. The cell preparation is a key link for a full automated diagnostic system along with other cell-based diagnostics. A blood LoC-based diagnostic tool would play an integral

role in the development of a comprehensive, automated diagnostic system. Such a system would be portable, field-deployable and allow for real-time monitoring of biomedical parameters. Recent published techniques based on dielectrophoresis (DEP) in microscale such as dielectrophoretic cell separation, manipulation, levitation, rotation and fractionation, have also attracted the attention of many researchers in microelectronics [4]. Gascoyne et al proposed a programmable diagnostic instrument based on dielectrophoretic sample handling. They successfully demonstrated many of the standard procedures in cellular biology such as cell sorting, focusing, detection, manipulation and cell lysis.

A key role of microelectronics in these procedures, in addition to offering a precise bioparticle sensor, would be to create a non-uniform, time-variant, reliable, precise and controllable electrical field in order to such dielectrophoresis manipulation. Among the techniques proposed by various researchers, Medoro et al have, for the first time, demonstrated the dielectrophoretic manipulation on CMOS [5]. In addition, they developed a capacitive and optical sensor realized on CMOS circuitry. CMOS standard technology can offer active circuit, programmability and processing. Localization of cells is necessary to determine the points to create dielectrophoretic force. This localization can be carried out by integrated capacitive sensors. Moreover, cell suspensions need microfluidic channels along with virtual channel created by dielectrophoretic forces, for continuous flow.

So far, an extensive variety of techniques has been employed to realize the fabrication of microfluidics for cellular and molecular applications [6]. And also, a number of techniques have been published about the CMOS-compatible microfluidic fabrication [7], but only a few papers reported the results of a biological application using CMOS-based microfluidic hybrid systems. Mastrangelo et al demonstrated a polymer surface micromachining to fabricate the microfluidic channels on a previously processed CMOS integrated circuit, which contained the control, detection, drive, and communication electronic modules [8]. In another attempt, for the fabrication of capillary electrophoresis (CE) and Polymerase Chain Reaction (PCR) devices, they developed a low cost epoxy microcasting technique [9]. Chartier et al reported the design of a polymer-based microfluidic structure fabricated through hot embossing, using an adhesive bonding [10]. This design was then integrated in a microelectronic chip, as described by Medoro et al [5]. It should be noted that most of the recent microfluidic techniques are based on polymers because they offer many advantages including low cost, fabrication flexibility and biocompatible with several biomedical applications.

The increasing need for 3D microfluidic devices has been widely recognized for LoC systems. To date, several efficient, but expensive and complex techniques such as LIGA have been developed to fabricate such fluidic structures [11]. Direct-write assembly is a high efficiency, low complexity and can be used for the fabrication of 3D microfluidics or the integration of fluidic or electronic chips from different technologies [12].

In addition to biological cells in blood, molecules such as glucose, cholesterol, triglycerides, disease-causing antigens and hormones can provide valuable information in medical diagnostics. This would require a biosensor that includes a bioelectrode with a biochemically-functionalized surface (such as an enzyme) to selectively recognize and bind to the biomolecule in the blood and a conducting interface, such as polypyrrole or carbon nanotubes, to immobilize the sensing molecule and transduce this biochemical interaction to an electric signal. Such electrochemical electrodes, in addition to above mentioned task, can offer a noninvasive technique for monitoring metabolic activity in single cells by detecting the extracellular metabolic gradient [13].

Since capacitive sensors represent important building blocks of LoC diagnostic tool for the detection of bioparticles, we focus in section II on novel highly sensitive circuit topology and sensing electrode design which are both realized onto CMOS process. Also, in this section, the design and simulation results of proposed capacitive sensor are demonstrated and discussed as the microelectronic part of LoC system. The novel polymer-based DWFP technique is presented in section III, which also deals with the implementation procedure, fabrication results, and advantages of this technique to construct novel LoC systems. In this section, we first introduce our experimental procedure and some of our microfluidic fabrication results, and then some experimental considerations of DWFP for integration and packaging purposes on a LoC system are discussed. In Section IV, this paper is concluded with a brief discussion of a fully automated LoC system fabricated through different technologies.

II. HIGH-SENSITIVITY CAPACITIVE SENSOR

The proposed capacitive sensor consists of sensing electrodes followed by an interface circuit as shown in Fig. 2.1a. The performance (P) of a capacitive sensor can be defined in equation (1)

$$P = \frac{\delta C}{C_{eq}} \tag{1}$$

where δC is the variation of input sensing capacitance (C) resulting from existing bioparticles exposed to sensing electrode, and C_{eq} is the equivalent sensing capacitance. For a single and differential output capacitive sensor:

$$C_{eq-single} = \delta C + C \tag{2a}$$

$$C_{eq-differential} = \delta C + \sigma C \quad . \tag{2b}$$

In equation (2b) ,$C_{eq\text{-}differential}$ includes σC which is an error, resulting from the difference between initial values of a sensing capacitance and a reference one. Therefore, for single and differential capacitive sensors, P results in equations (3a) and (3b).

$$P_{single} = \frac{\delta C}{\delta C + C} \approx \frac{\delta C}{C} \tag{3a}$$

$$P_{differential} = \frac{\delta C}{\delta C + \sigma C} \tag{3b}$$

P_{single} is very small due to the small variation of sensing capacitance δC in compared with C, but $P_{differential}$ can be high if σC is cancelled, using a calibration technique.

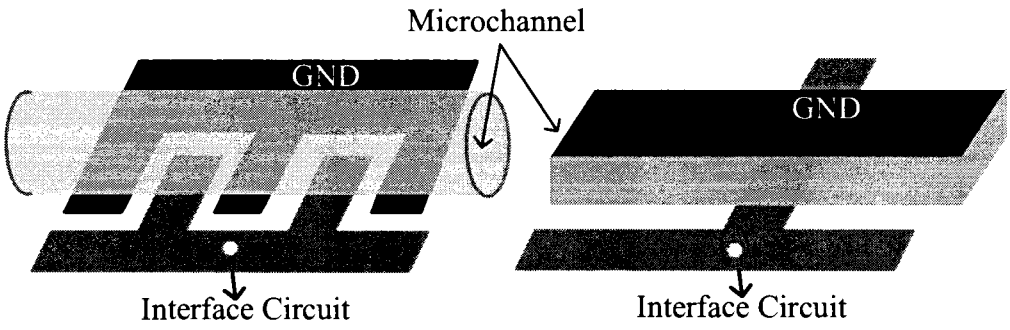


Figure 2.1. Schematic representation of sensing electrodes incorporated with a microchannel: (a) interdigitated electrode, (b) configuration presented in [5].

The sensitivity (S_v) of an integrated capacitive sensor is defined as follows:

$$S_v = \frac{\delta V_{out}}{\delta C} \tag{4}$$

where V_{out} is the output signal of corresponding interface circuit and δV_{out} shows its differential variation. The value of S_v depends on the characteristics of the both sensing electrode and interface circuit.

A. Capacitive sensing electrodes

Few designs of sensing electrodes for bioparticle detection on CMOS process have been reported in the literature. Fig. 2.1b shows a sensing capacitance created between an electrode designed in the uppermost metal layer of CMOS chip, covered with passivation layers, and a conductive lid [5]. A non-standard process using fiber optic as spacer between two electrodes was carried out to realize this sensing electrode.

A schematic representation of our proposed interdigitated capacitive sensor is shown in Fig. 2.1a. As an advantage of this technique, there is no need for extra post-processing to create an extra electrode onto a fabricated chip in standard technology. The design and implementation of the sensing electrode has been carried out in Virtuoso layout editor using a thick metal 6 and "Pad" mask layer. As shown in Fig. 2.2a, in standard CMOSP18 technology, the passivation layers stacked in the last step of process can be removed using this mask layer which decreases C due to less insulating passivation layers between the conductors of the electrodes (Fig. 2.2b). The mask removal also increases δC as a result of more space for the presence of bioparticles between electrodes.

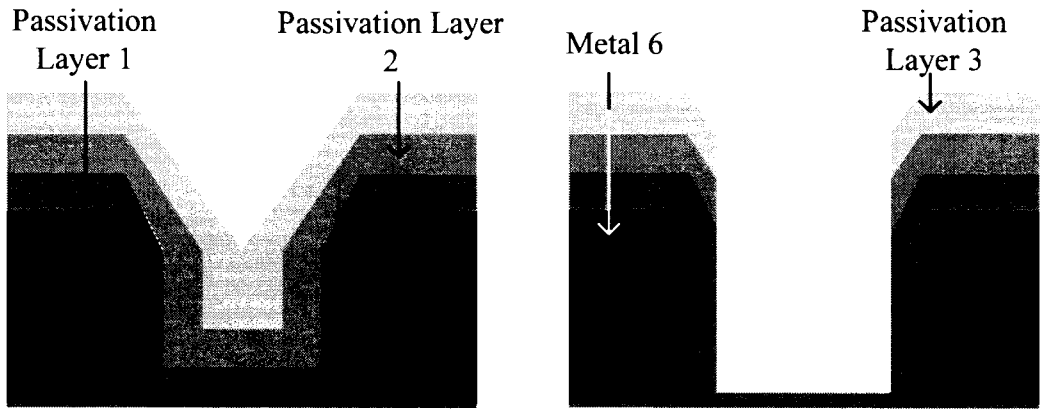


Figure 2.2. Passivation layers: (a) onto CMOSP18 (TSMSC), (b) after using removal process through pad-etch technique.

B. Interface circuit topology

We have recently reported a capacitive sensor for bioparticle detection using charge-based capacitance measurement [14, 15]. The simplified block diagram of the proposed

capacitive sensor circuit and complete interface circuit topology are depicted in Fig. 2.3 and Fig. 2.4 respectively. As shown in equation (5), the difference between the DC components of two charging currents I_1 and I_2 is proportional to ΔC where V_{dd} and f are power supply voltage and frequency of $\Phi 1$ and $\Phi 2$ respectively (see Fig. 2.4).

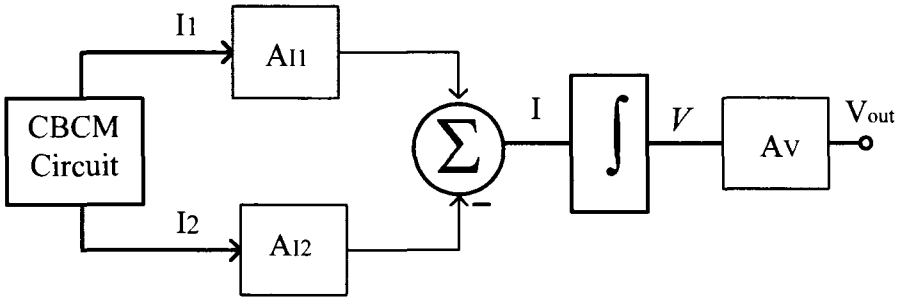


Figure 2.3. Simplified block diagram of proposed capacitive sensor.

$$\Delta I = I_1 - I_2 = \Delta C \cdot f \cdot V_{dd} \tag{5}$$

where ΔC is a differential capacitance between all parasitic and sensing capacitances standing on nodes A and B (see Fig. 2.4). Due to a fully symmetrical and differential structure, the output voltage of the proposed circuit is almost independent of the initial value of C. In this circuit, two current mirrors (M5-M6 and M7-M8) amplify (A_I) the charging currents I_1 and I_2 and the third current mirror (M9-M10) is employed to transfer I_2 to node C. Then, the resulting ΔI is converted to voltage by integrating capacitor C_{int}, and consequently this voltage (M11-M12) is buffered through the output stage (A_v).

C. Sensitivity optimization and circuit simulation results

The output voltage of the proposed capacitive sensor is given by equation (6) where V is a DC offset voltage resulting largely from parasitic capacitors [14]:

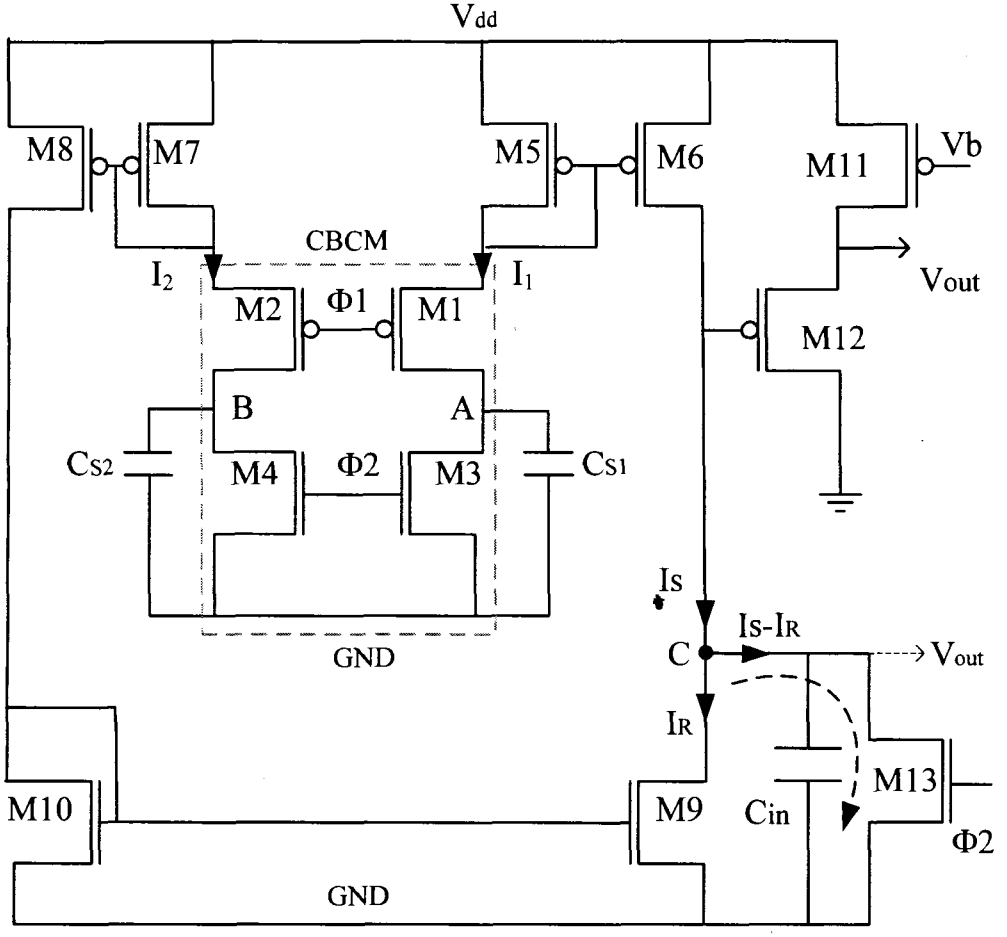


Figure 2.4. Proposed capacitive interface circuit topology.

$$V_{out} = \frac{\Delta C}{C_{\text{int}}} \cdot A_I \cdot V_{dd} + V \tag{6}$$

However, based on equations (4) and (6), it seems that A_I and C_{int} are the only two effective parameters on the sensitivity. Further simulations (Spectre S and Cadence) allowed to determine that the channel length (L) of transistors M9-M10 along with A_I are major parameters regarding this issue. This is because the channel length of transistors M9-M10 affects the output impedance seen from node "C". Therefore, the

critical parameters are identified as the gain of current mirrors A_I and L for a given range of C and ΔC.

D. Layout implementation of interface circuit and electrodes

The implemented layout of our proposed circuit includes two similar sensing electrodes and other devices schematically shown in Fig. 2.4. Microelectronic circuits are often plagued with parasitic capacitor; hence the need to design a high sensitivity sensor with the ability to detect less than 1 fF is a challenging issue. Of course, the smaller dimensions of devices the weaker their parasitic capacitances. Post layout simulation in the section of simulation and experimental results ensure us about the right functionality of the interface circuit in existing large environmental parasitic capacitances.

Along with the already discussed capacitive sensor, a large interdigitated electrode using metal layer 6 is also embedded in the same chip. This electrode is considered to investigate dielectrophoresis (DEP) handling in the microchannel fabricated through DWFP technique onto CMOS chip. The CMOS layout design rules allow making a sub-micro conductor in order to generate the required non-uniform electrical field. It is obvious, such precise electrical fields along with a grounded electrode on top of microchannel (e.g. conductive epoxy or Indium Thin Oxide layer [10]) can strengthen DEP forces with precision for LoC applications.

E. Capacitive sensor calibration

Even though, the interface circuit shown in Fig. 2.4 is symmetrical between two sensing electrodes, we can not expect such a balanced structure after fabrication, packaging

and/or integration with microfluidic channel. For example, microfluidic channel made of epoxy is not completely uniform at both ends of the electrodes resulting in two different parasitic capacitances on electrodes. Based on the previous discussions, σC is involved in ΔC, and ΔC is proportional to ΔI. Therefore, in order to cancel σC, the DC offset component of ΔI can be varied to remove this DC offset while there is no analyte in channel. After the fabrication of sensor chip, by assuming a constant value for V_{dd}, there is no any variable parameter except the sensing capacitance exposed to analyte. Therefore, an off-chip potentiometer can be connected to the source of M8 in order to adjust the DC offset included in ΔI. Consequently, the effects of all unwanted parasitic capacitance can approximately be removed. The calibration of this highly capacitive sensor is necessary, because the extraneous σC may positively or negatively increase the DC offset of ΔI (and V_{out}) and it may subsequently alter the circuit characteristics to an unstable state.

III. DIRECT-WRITE FABRICATION PROCESS

Direct-write assembly is a robotic deposition technique used to produce layer-by-layer microscale structures composed of filaments with either cylindrical, hexagonal or square cross sections [16-18]. The filaments are formed during the extrusion of a paste-like material through a micronozzle and deposited on a substrate in order to build planar or three-dimensional (3D) structures. The deposition of a fugitive organic ink scaffold was followed by the infiltration of an uncured epoxy resin. After polymerization of such a

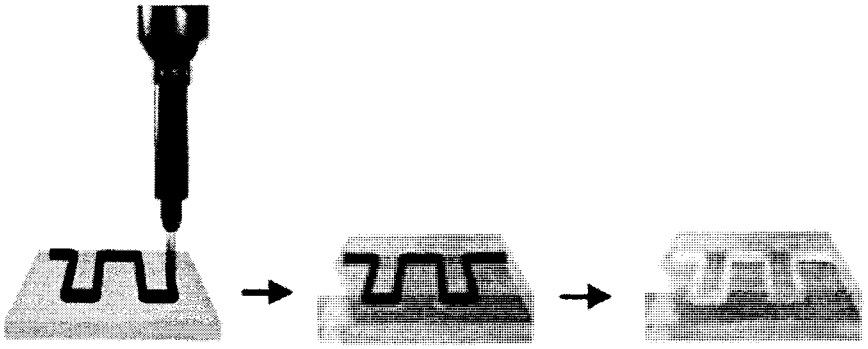
resin, the ink was extracted at a moderate temperature in order to obtain the desired microfluidic network (Fig. 2.5). The DWFP was employed to fabricate complex polymer-based 3D microfluidic structures [19]. The compatibility between DWFP and standard CMOS technology was also previously demonstrated [10].

A. Experimental procedure

A robotic apparatus (Model I&J 2200, I&J FISNAR Inc.) controlled by a computer (JR Points, I&J FISNAR Inc.) was used to perform the deposition pattern. The air-operated dispensing system (Model 2400, EFD Inc.) was used to extrude the fugitive binary organic ink [20] through different micronozzles (10, 100 and 200 μm inner diameters). The ink was either deposited onto a microscope slide or CMOS chip. During the deposition, the speed of the nozzle's motion was 1 mm/s and the extrusion pressure was experimentally determined. An optically clear epoxy resin (Epoxide 835, Epoxitech Inc.) was poured to encapsulate the deposited ink filaments and cured at room temperature. Then, the part was heated to ~75°C in order to melt the ink and an air pressure (100 kpa) was applied at the inlet of microfluidic channel to remove the melted ink. Robot speed and dispensing pressure, obtained experimentally (microscope slide as substrate, 100μm nozzle and petroleum jelly included 25 % microcrystalline wax) are 1mm/s and 10 kpa respectively.

The required set-up system and materials for DWFP are not expensive and there is no need to deal with laborious and complex infrastructure relevant to microfabrication clean rooms. For this, DWFP can be a good choice for researchers studying the chemical or

biological aspects of LoC without contributing in microfluidic or micoelectronic research areas.



(a) (b) (c)

Figure 2.5. Schematic representation of DWFP technique: (a) ink deposition, (b) encapsulation in epoxy, (c) ink extraction

B. CMOS integrated circuit compatibility

DWFP is compatible with standard CMOS technology because it is a low temperature technique with no destructive chemical solution to damage underlying microelectronic circuitries. In addition, DWFP enables the direct fabrication and integration of microfluidic components on top of CMOS chips. Indeed, with other techniques [8]-[9], microfluidic components are first fabricated and subsequently bonded to the chip, requiring careful alignment. DWFP avoids misalignment errors resulting from the adhesive bonding procedure.

IV. RESULTS AND DISCUSSIONS

In this section, the simulation results of proposed interface circuit, along with experimental results of microfluidic channel are presented and discussed.

A. Post layout interface circuit simulation

The transient output voltage of the interface circuit (Fig. 2.4) are simulated by Spectre S, in Cadence for different values of input sensing capacitances (C_{S1}) as shown in Fig. 2.6. And also, the linear relation between the output voltage and input sensing capacitances of this sensor circuit is highlighted in Fig. 2.7. As shown in these figures, this design results in sensitivity equal to 250 mV/fF. Also, in the frequencies lower than 25 MHz, the simulated noise is less than 40 μV which is equivalent to 10 aF. As illustrated in Fig. 2.8, the small values of C_{int} (Less than 100fF) do not increase the sensitivity due to the comparable parasitic capacitors on node "C" (see Fig. 2.4).

The implemented layout (Virtuosos, Cadence) of the interface circuit along with its sensing electrode are shown in Fig. 2.9. In this figure, sensing electrode (A) is exposed to flowing bioparticles where reference electrode (B) is not. Therefore the differential effect of presence and non-presence of a bioparticle is indicated in output voltage V_{out} arising from one of bonding pads.

B. Finite element modeling and simulation results

In order to characterize and optimize the interface sensor, an estimation of ΔC and C is required. The extracted capacitance using Virtuoso layout editor indicates that the induced capacitances between top plates of neighboring electrodes has not been involved in the calculations while those are the most influential parameter of an interdigitated electrode. For this, the sensing electrode was modeled and simulated in COMSOL Multiphysics, resulting in a ΔC equal to 1fF.

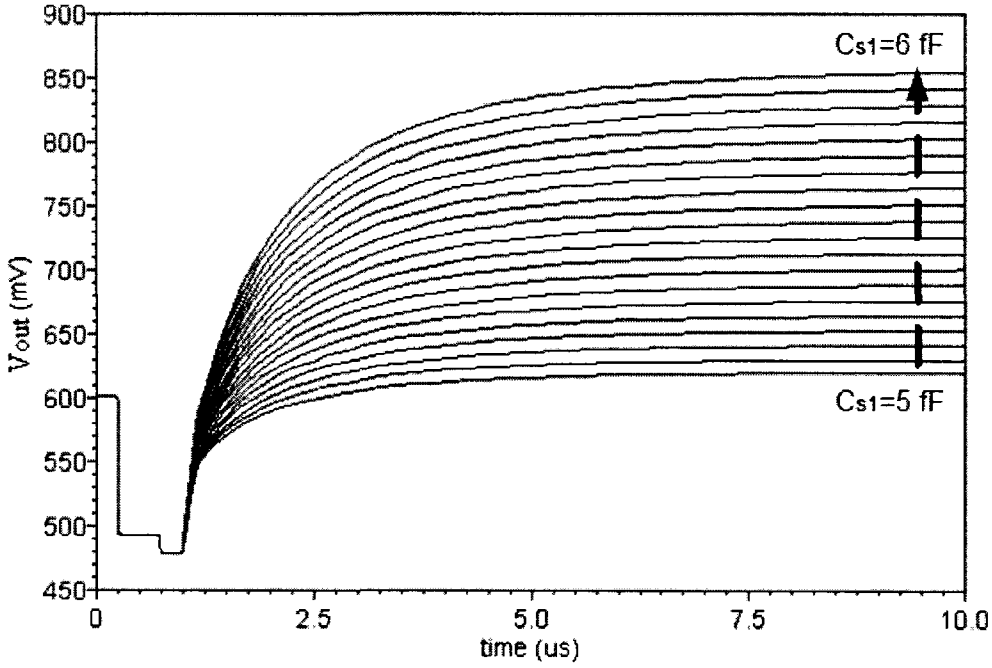


Figure 2.6. Output voltage versus time for different values of C_{S1}.

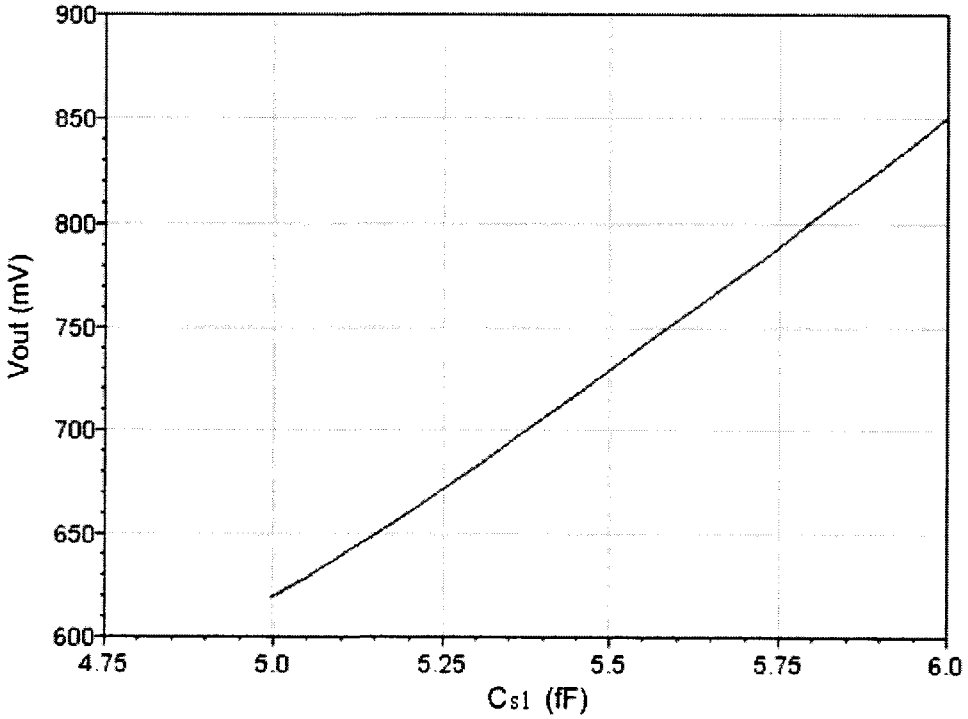


Figure 2.7. Output voltage versus C_{S1}.

C. Fabrication of Microchannel

Microchannels and 3D microreservoirs were fabricated on glass and CMOS chip substrates as a feasibility study of CMOS based LoC systems. Optical and UV microscope images (BX61, Olympus) of a 100 μm microchannel are shown in Fig. 2.10. Top view images were captured after the ink deposition, the matrix infiltration and the ink extraction. No significant deformations of the ink filament were observed during and after the matrix infiltration.

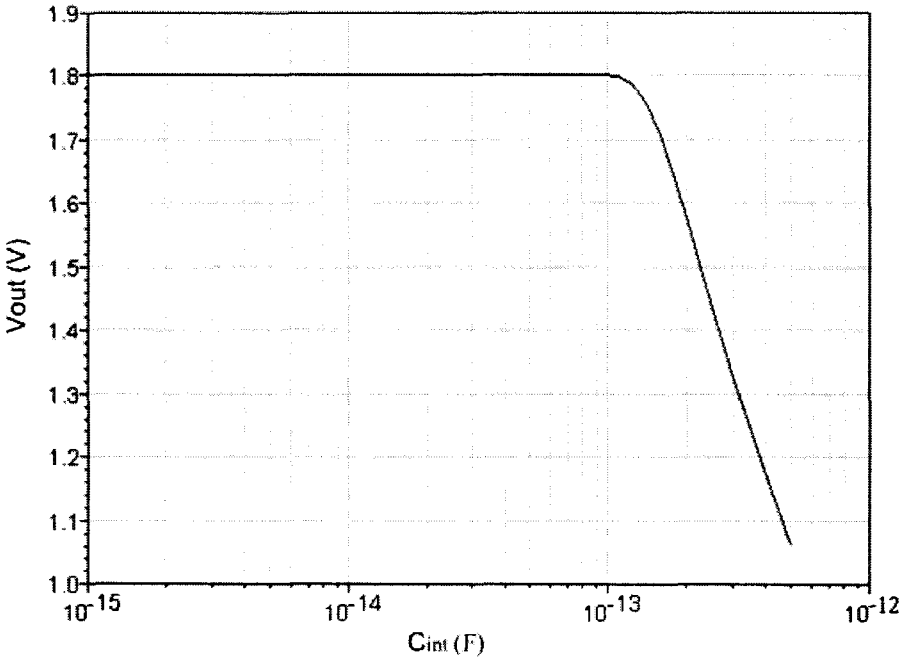


Figure 2.8. Output voltage versus Cint.

D. On-chip microchannel fabrication process

A microfluidic fabrication and fluidic connection processes are performed on an electrically packaged CMOS chip. The alignment of the ink deposition process over the

desired features of the CMOS chip is performed manually. First, the CMOS chip is fixed onto the microrobot platform.

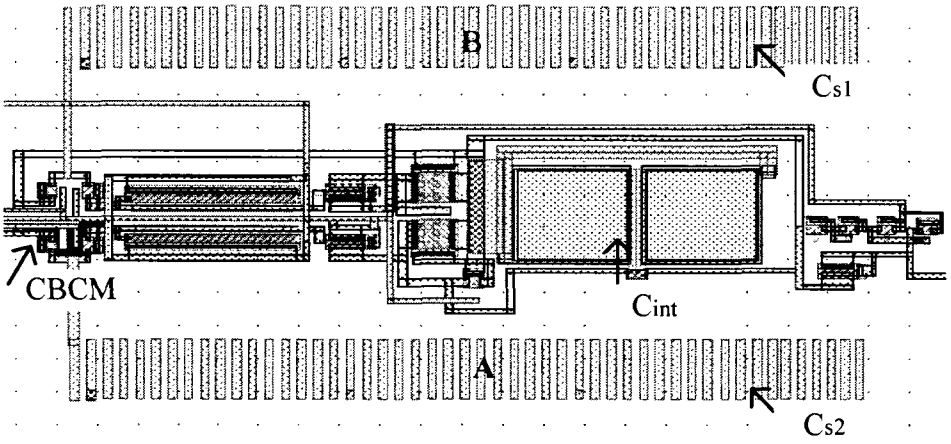


Figure 2.9. Layout of proposed circuit.

Then, a small tip needle (10 μm, World Precision Inc.) is moved by the microrobot, set in manual mode, at specific locations over the substrate (e.g., sensing electrodes) while the alignment is visually performed using a stereomicroscope. The *x*, *y* and *z* coordinates of the points of the deposition trajectory are determined and recorded into the trajectory file. For the fabrication of the straight microchannel shown in Fig. 2.11, the deposition started at one edge of the CMOS chip, crossed over the sensing electrodes and ended at the other edge of the chip. The minimum feature size of this sensing electrode is approximately the same size as the micronozzle tip used during this alignment technique. The observation error E is estimated at 4 μm when using the stereomicroscope (SZX7, Olympus Inc.) for the manual alignment. In addition, the microrobot step size D is 10 μm (Model I&J 2200). Thus, the alignment accuracy is (D+E)/2 or ~7 μm (see Appendix

A). Optical microscope image of the microelectronic CMOS chip shown in Fig. 2.11 indicates the compatibility between electrical and fluidic packaging.

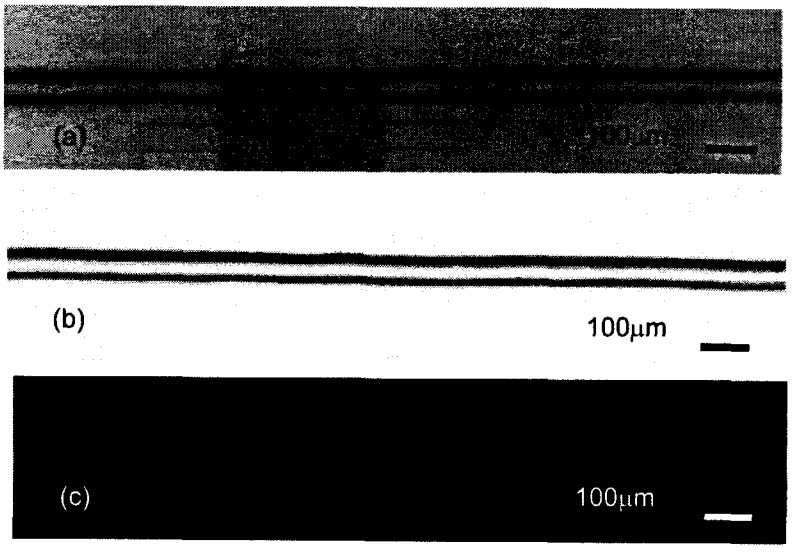
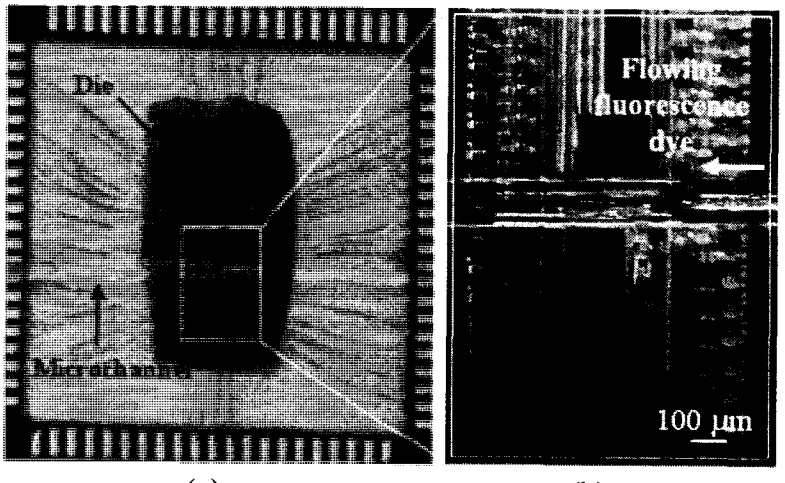


Figure 2.10. Microscopic images of 100 μm microchannel: (a) filament ink, (b) filament ink inside epoxy, (c) UV image of fluorescent dye filled in microchannel.



(a) (b)

Figure 2.11. Microfluidic fabrication on electrical packaged chip (a) over view, (b) close-up view of die.

The microchannel crossing die is zoomed in Fig. 2.11b. The simultaneous fabrication and integration of microchannel on top of a CMOS chip was performed in two steps: epoxy deposition to fill the spaces around die covering the bonding wires and simultaneous fabrication and integration of microchannel by DWFP. Fig. 2.13d shows the microchip after performing the first step. As shown in this figure, the microchip die is still uncovered by epoxy resin.

E. Discussion

Microfluidics fabrication, integration and fitting connection can be simultaneously performed onto microelectronic loose die or chip. We demonstrated the flexibility of DWFP for CMOS based LoC as shown in Fig. 2.12. The microchannel is fabricated by DWFP on top of the microelectronic chip suitable for the bioparticle sensing purposes. In a LoC system, there are two kinds of packaging: electrical and fluidic. Electrical packaging can be performed using conventional techniques such as wire bonding or flip chip. Thereafter, DWFP provide microfluidic components and inlet/outlet fittings.

In most of microelectronic packaging labs, programmable dispensing system (Champion 8300 dispenser in our Polystim neurotechnologies Laboratory) is one of important conventional packaging facilities already available. DWFP could potentially be performed with such programmable dispensing systems since they offer similar functionality. The diameter of the microchannel is directly proportional to the inner diameter of the micronozzle used during the deposition procedure. The minimum inner diameter of commercially available nozzles fabricated in metal and glass are 100 μm

(EFD Inc.) and 100 nm (World Precision Instruments Inc.), respectively. However, smaller glass tips are fragile and tend to break under the high extruding pressure and during accidental contact with the substrate surface.

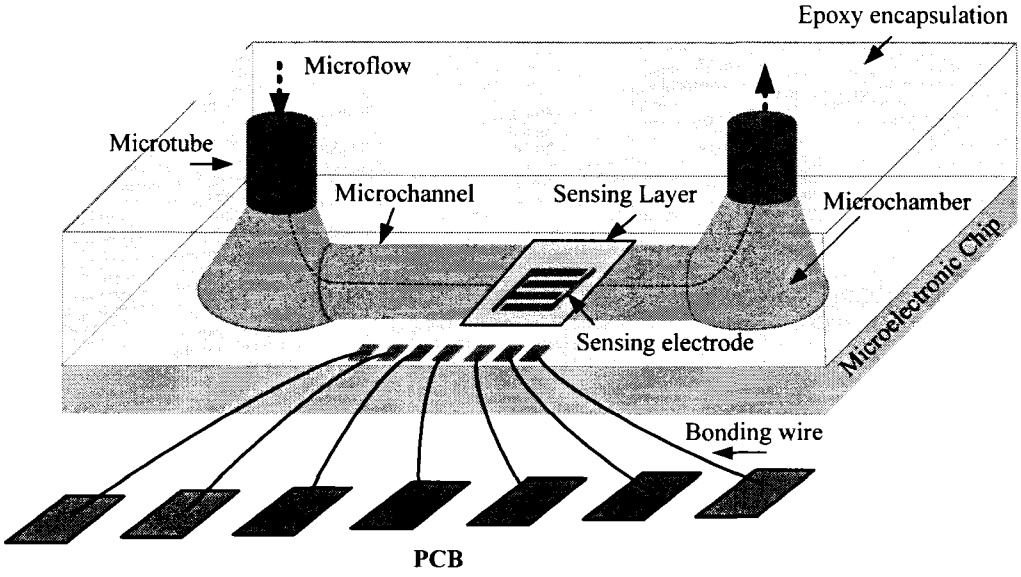


Figure 2.12. Schematic representation of full integration and packaging of LoC system.

The DWFP of microchannels at the micron and sub-micron scales will require the design of sturdy custom-made nozzles [18] combined with high extrusion pressure and precise motion of the robotic apparatus. For the creation of sub-micron LoC devices, piezoelectric nanopositioning xyz stages could be used for the deposition and alignment with the CMOS chip.

In addition to microfluidics and microelectronics, for a fully automated cell preparation and analysis, there are needs to DEP and biosensing electrodes for dielectrophoretic handeling and biological detection (Polypyrrole/glucose oxidase enzyme). But, the size of

such electrodes usually is a few centimetres [21] which are not justified to be realized on expensive standard semiconductor technologies. Therefore, these electrodes can be fabricated in their conventional technologies and then integrated and packaged to microelectronics with the proposed LoC integration technique presented in our research work. The fluidic connection is an important issue in microfluidic system and is performing based on different conventional techniques. Conventional fluidic fitting techniques such as tubing [22] or screwing [23] can not be implemented along with microfluidic fabrication. Therefore, there are needed to extra processes adopting micro-channel to such standard fittings. DWFP allows the simultaneous fabrication of microfluidics and connection to standard fittings. Fig. 2.13a shows the first step of fluidic connection by DWFP: the installation of the fitting close to ink filament. Thereafter the extruded ink from fitting creates the connection to microchannel (Fig. 2.13b). Then the connection site along with ink filaments is covered with epoxy. The existing fugitive ink inside the fitting can be easily removed during ink removal process.

DWFP can be performed on a wide variety of substrates (e.g., different materials and physical surface properties). Fig. 2.13c shows an optical side view image microscope of a deposited ink filament spanning between two substrates of different heights. This image demonstrates the flexibility of DWFP in the fluidic packaging process with different heights in the trajectory of deposition. This flexibility is a very important advantage of DWFP which makes it a powerful technique for fluidic integration and packaging of LoC system.

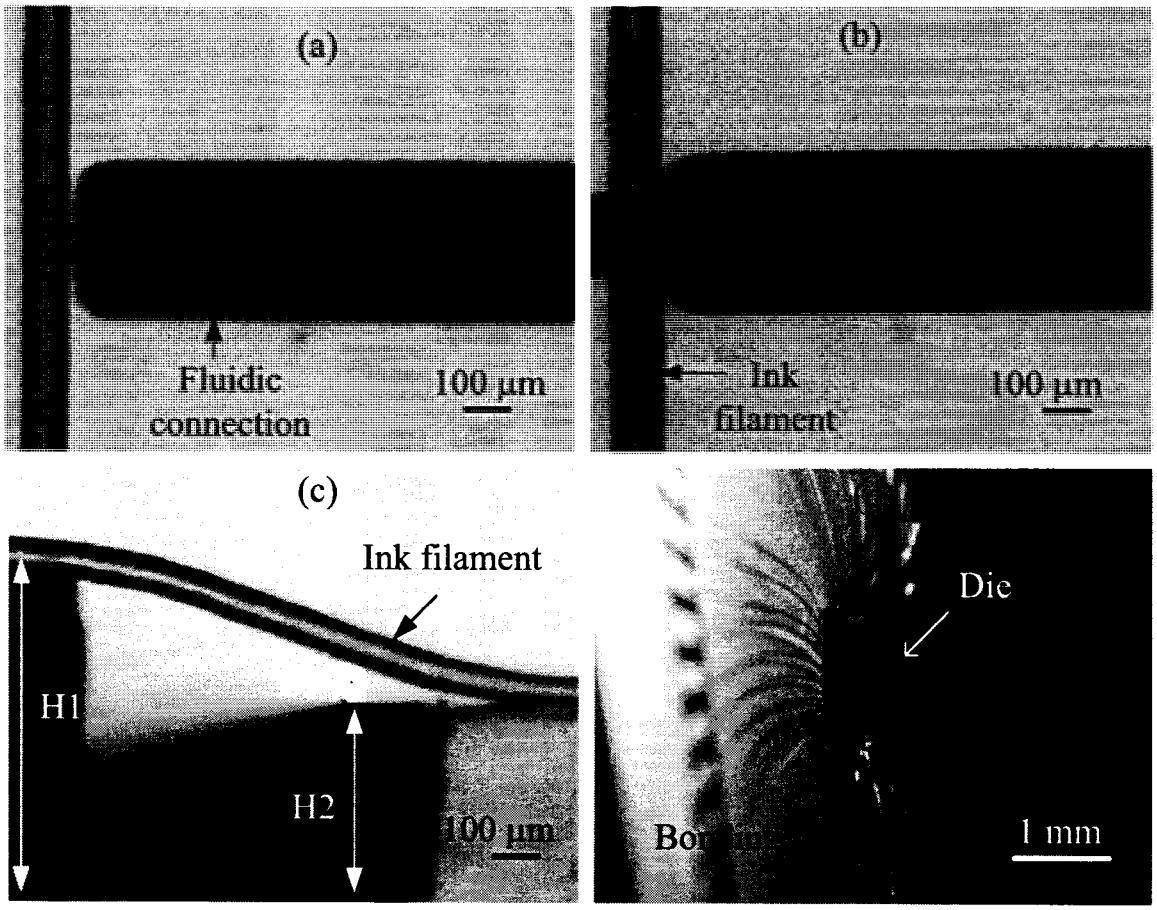


Figure 2.13. Optical microscope images of (a) the fugitive ink and fitting, (b) deposited ink from fitting, (c) ink deposition between two substrates in different heights, (d) epoxy resin surrounding the die.

V. CONCLUSION

DWFP can play a key role for the fluidic packaging of microfabricated chips implemented by standard technologies (e.g., microelectronics, microfluidics) for highly integrated LoC systems. The critical parameters of DWFP are determined by the nozzle's inner diameter and the precision of robotic system which are as important in this process as the microlithography process in conventional microfabrication technologies. As the

creation of sub-micron fluidic channels is essential for many of biomedical applications, our future work will attempt to achieve microfluidic structures with smaller feature sizes. We described a highly linear capacitive sensor to detect the capacitive variations as small as 10 aF. The simulation results were demonstrated and discussed in order to validate the functionality of this new interface circuit topology for such a high-precision application. This sensor chip is under fabrication by TSMC (Taiwan Semiconductor Manufacturing Corporation) using 0.18 μm CMOS process.

APPENDIX A

The total magnification of the stereomicroscope used (SZX7, Olympus Inc.) is 250X. The minimum observable feature size with the naked eye is assumed to be 1mm and the observation error E is then 4 μm (i.e., 1 mm/250). While the micronozzle is moved along one direction to reach a desired location as shown in Fig. 2.14, two points (i.e., A and B) can be defined at the limit of the position uncertainty of distance $x1$ and $x2$, respectively. The relations between $x1$ and $x2$ are

$$x1 + x2 = D \tag{A1}$$

$$x1 - x2 < E \tag{A2}$$

The expressions (A1) and (A2) can also be expressed by

$$x1 < (E + D) / 2 \tag{A3}$$

$$x2 > (D - E) / 2 \tag{A4}$$

Therefore, the maximum alignment error along one axis is approximately $(D+E)/2$ or 7 μm (D is the step size of robot).

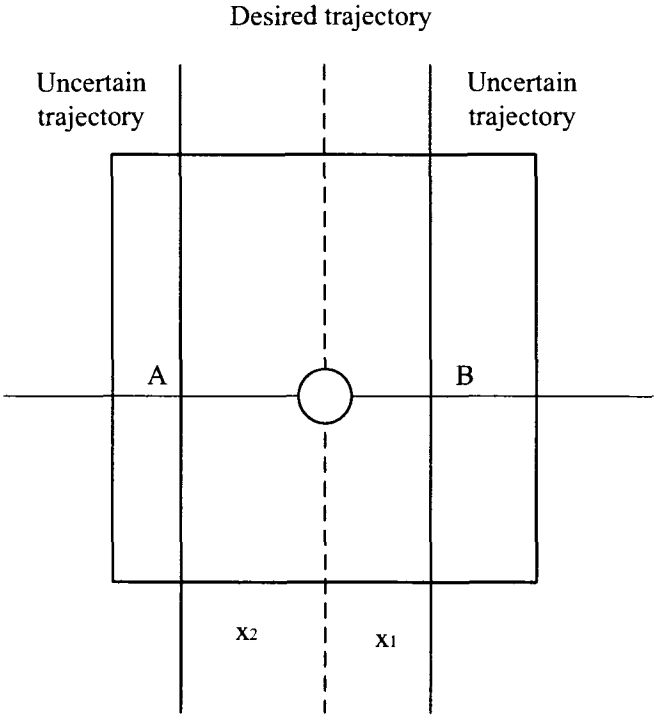


Figure 2.14. Estimation of alignment error.

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Chapter 3

CMOS BASED CAPACITIVE SENSOR FOR LOCS

3.1 Introduction

As discussed in Chapter 3, the proposed capacitive sensor maintains the advantages of low-complexity and high-sensitivity for the detection of non-conductive solvents in microchannel. In this chapter, the behaviour of this sensor is analyzed and discussed against both conductive and non-conductive solutions. Thereafter, the simulation and experimental results of fabricated chip are demonstrated using different chemical solvents. This work published in "Journal of Sensors and Actuators A: Physical, Elsevier" is reproduced in the following pages.

3.2 A 0.18-μm CMOS Capacitive Sensor Lab-on-Chip

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[1]Polystim Neurotechnologies Laboratory (Polystim), Department of Electrical Engineering, Ecole Polytechnique de Montreal. [2]Center for applied research on polymers and composites (CREPEC), Department of Mechanical Engineering, Ecole Polytechnique de Montreal. Published in: Sensors and Actuators A: Physical, SNA 6032, 2007.

ABSTRACT

In this paper, we put forward a capacitive sensor for Lab-on-Chip applications using a charge based capacitance measurement (CBCM) method. This simple and highly sensitive capacitive sensor is implemented in the TSMC 0.18 CMOS process to which we incorporate microfluidic structures for chemical sensing. The post-layout simulation, fabrication and preliminary Lab-on-Chip testing results are also reported.

Keyword:Microfluidic packaging, CMOS, capacitive sensor, Lab-on-Chip, Direct-write fabrication process.

I. INTRODUCTION

CMOS-based Laboratory-on-Chip (LoC) continues to command the attention of researchers for the miniaturization and automation of biological assays and procedures in chemical analysis. High-performance CMOS processes have been successfully applied for such embedded sensing devices as photodiodes for bioluminescence detection, ISFETs for pH sensors, parasitic bipolar transistors for temperature measurements and capacitive electrode arrays for cellular analysis [1-4]. Additionally, several post-processing sensing devices, such as thermally- and magnetically-actuated cantilevers, have been developed in CMOS technology for chemical analyses [5]. All these sensing devices have been integrated with high-precision circuitry for signal conditioning and further data processing. To date, several CMOS-based capacitive sensors have been

successfully developed for LoC applications, for example as digital microfluidics, antigen detection through antibody binding, and cellular analysis [6-8]. In these sensors, one or both electrodes of each sensing capacitor (with variation in dielectric coefficient) are realized on the topmost metal layer of the CMOS process. The second grounded electrode of sensing capacitors can also be coated atop a microfluidic channel, preferably transparent for visualization purposes (e.g. ITO).

A conventional interface circuit of a capacitive sensor consists of an operational amplifier and an integrating capacitor C_{in} as shown in Fig. 3.1 (see Fig. 1.7). The charge injected into the sensing capacitance C_S is transferred to C_{in} through the high impedance node of the opamp - which in turn leads to a linear relation between the opamp output and C_S:V_o $=V_a \cdot (C_S/C_{in})$, where V_a is the charging voltage amplitude. In this figure, the capacitance C_C is used to increase the dynamic range of interface circuit against input capacitance changes. C_{in} should typically be small to increase the output voltage, but it cannot be less than inherent parasitic capacitances, thus limiting the sensitivity of this interface circuit. The parasitic capacitance C_p (due to wire bonding) is cancelled through opamp with negative feedback where in CMOS capacitive sensors consisting of sensing electrodes, this parasitic capacitance doesn't exist. The amplifier flicker noise can be cancelled by correlated double sampling but the thermal noise sources of the amplifier and switches is sampled at node A and aliased into based-band frequency range and resulting in lower interface circuit resolution [9]. So far, several types of high resolution Sigma Delta ($\Sigma\Delta$) ADCs using switched-capacitor techniques have been reported as a digital readout device

adopting such capacitive sensors [9]. Recently, charge-based capacitive measurement (CBCM) technique has been reported as an accurate technique for the characterization of interconnects capacitance in deep submicron CMOS ICs [11]. So far, several papers that further develop on this work have been published, while also introducing new applications of CBCM such as particle and DNA detections [12-13]. The low complexity CBCM is also a good alternative for capacitive sensor arrays. We have already reported a CMOS based LoC using direct-write microfluidic fabrication process (DWFP) [14]. Here, we for the first time, report the analysis and measurement results of our proposed hybrid system against chemical solutions and discuss the practical considerations.

The remainder of the paper is organised as follows. In section II, we describe the proposed capacitive sensor and evaluate its sensitivity against five chemical analytes. The simulation and experimental results are given in section III. In section IV, the main design and fabrication considerations are briefly discussed, followed by a conclusion in section VI.

II. CAPACITIVE SENSOR

In this section, we describe the proposed capacitive sensor including interdigited electrodes and an interface circuit.

A. Interdigitated electrodes

Until now, several types of sensing electrodes have been reported in CMOS process for chemical and biological applications. Hierlemann et al reported the implementation of

quasi interdigitated electrodes using two top most metal layers for capacitive gas detection [5]. In another effort, the thick metal electrodes covered with silicon oxide passivation layer were employed for virus detection [7]. A capacitive sensor array including a common ground electrode on the top of microfluidic packaging was reported for cell analysis [3].

Herein, two interdigitated sensing and reference capacitors have been realized through CMOS process on the topmost metal layer. Using so-called pad-etch in this process; the passivation layers between the fingers of interdigitated sensing electrodes have been removed in order to increase the dynamic range of sensor. The created parasitics (δC_1, δC_2, δC_3, δC, δR) and their equivalent impedance in the presence of an analyte sample are shown in Figs. 3.2a and 3.2b, respectively. In the presence of a non-conductive analyte, R is considered very large which results in $C_{eq} = C_2 \| C_3 \| C$ where C (the analyte) $<<C_1$ (the passivation layer). But, in the case of ionically-conductive solution, R is assumed to be negligible and thus $C_{eq} = C_2 \| C_3 \| C_1$. It should be mentioned that the interdigitated reference electrode (covered by epoxy in the proposed platform) is used as the reference capacitor (C_R). An estimation of C_2, C_3 and C for a nonconductive analyte ($C<<C_1$) is given in section III-A using Cadence and FEMLab CAD tools.

B. Interface circuit

As shown in Fig. 3.3, the proposed capacitive sensor includes the CBCM block, charge amplifiers A_{I1} (M5-6) and A_{I2} (M7-10), integrator (C_{in}), and voltage buffer. The response of this circuit to non-conductive and conductive fluids in the channel above interdigitated

sensing capacitor is presented.

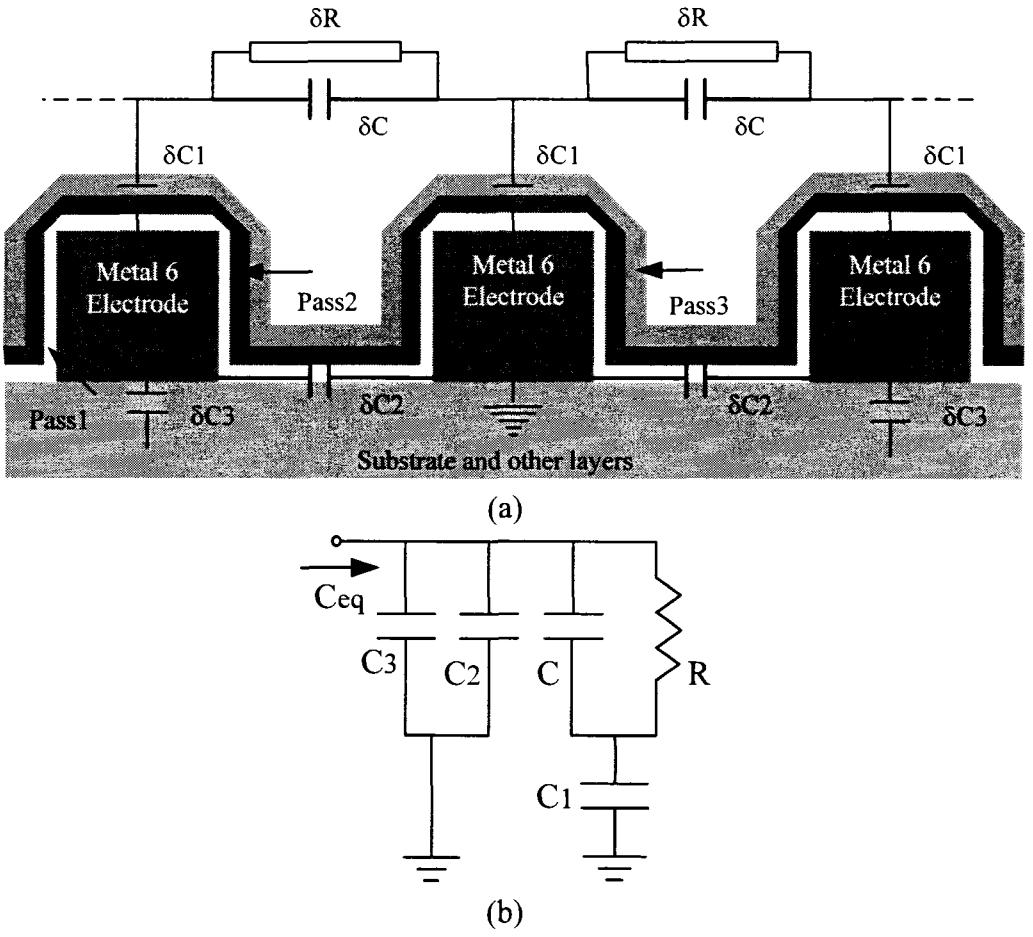


Figure 3.2. Illustration of (a) parasitics generated on top of CMOS chip (δC and δR are the partial parasitic capacitance and resistance respectively) and (b) its equivalent circuit.

1) Non-conductive fluids: Based on previous discussions, the equivalent capacitor of interdigitated sensing electrodes for a non-conductive solution is $C_S = C_2 + C_3 + C$ where C_R is the same for conductive or non-conductive solutions. The output voltage (V_{out}) in this case is obtained from Eq. (1)

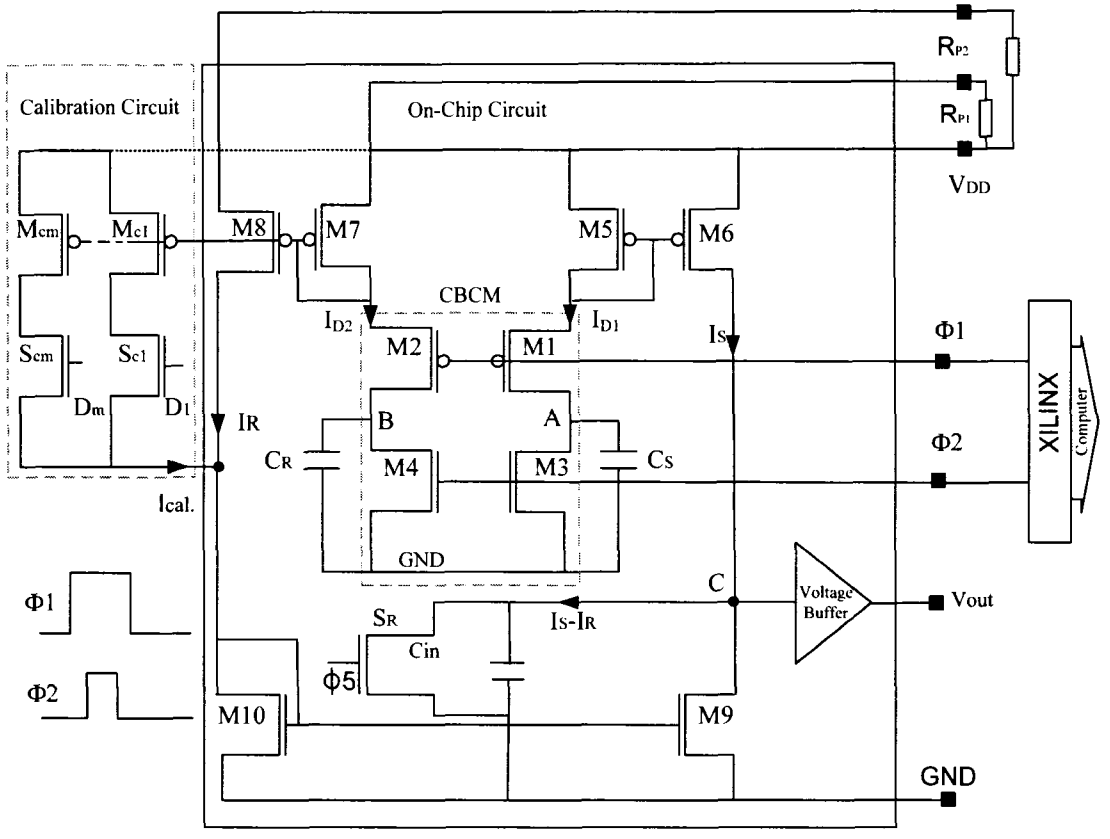


Figure 3.3. A schematic of fabricated interface circuit external connections and a switching calibration circuit.

$$V_{out} = \frac{C_{T1}}{C_{in}} \cdot A_{I1} \cdot V_{dd} - \frac{C_{T2}}{C_{in}} \cdot A_{I2} \cdot V_{dd} + V_{off} \tag{1}$$

where $V_{dd} = V_{DD} - V_{TP}$. V_{DD}, V_{TP} and V_{off} are the power supply, threshold voltage of P-channel transistors and output offset voltages, respectively and also, the switch-on and switch-off resistances of M1-M4 have been discounted. $C_{T1} = C_A + C_S$ and $C_{T2} = C_B + C_R$ are considered the equivalent capacitances seen from points A and B where C_A and C_B are the parasitic capacitances created by M1-M4. Eq. (1) can be rewritten in Eq. (2).

$$V_{out} = \frac{C_{T1} - C_{T2}}{C_{in}} \cdot A_{I1} \cdot V_{dd} + V'_{off} \tag{2}$$

where the equivalent output offset voltage V'_{off} is obtained from Eq. (3)

$$V'_{ooff} = \frac{C_{T2}}{C_{in}} \cdot (A_{I1} - A_{I2}) \cdot V_{dd} + V_{off} \quad . \tag{3}$$

In the circuit design proposed by Evans et al., they use two integrating capacitors instead of C_{in} and a differential voltage amplifier instead of unity gain current amplifier (M9-M10) [12]. In contrast, our proposed design offers a robust interface circuit against the value of parasitic capacitances C_{T1} and C_{T2} which are expected to be larger in CMOS processes of 0.18 microns and less. This is because, as seen in Eq. (2), the integrated voltage V_{out} is proportional to (C_{T1} - C_{T2}) and not to C_{T1} or C_{T2} individually which is the case in [12]. Therefore, in our proposed interface circuit, the voltage dropped in C_{in} will not destabilise the current amplifier transistor M6 from its active region for a wide range of these parasitic capacitances. By assuming C_{T1} = C_{T2}, the sensitivity of proposed capacitive sensor versus $\Delta C = C_{T1} - C_{T2}$ can be obtained from Eq. (4)

$$S_{\Delta V/\Delta C} = \frac{\Delta V_{out}}{\Delta C} = \frac{V_{dd} \cdot A_{I1}}{C_{in}} \tag{4}$$

where $S_{\Delta V/\Delta C}$ and ΔV_{out} are the sensitivity and the variation of output voltage. In order to maximize $S_{\Delta V/\Delta C}$, A_{I1} and C_{in} are assigned higher and lower parameter values respectively. C_{in} can not be less than the inherent paracitic capacitance seen in node C [15], but, one-stage current mirror amplifier of this design can easily be extended to a

multiple stage amplifier for higher A_{I1} and consequently higher sensitivity. In this design, V_{DD} keeps at its maximum value which is 1.8 V in 0.18 CMOS process.

It should be mentioned, ΔC is very low (see Fig. 3.4) and it can be considered as a limiting factor in on-chip capacitive sensor LoCs. Even though, the larger electrodes create higher ΔC; sometimes, it is preferred to use an array of small sensing electrodes instead in order to decrease the incorporated parasitic capacitances, thereby to allow higher current gain A_{I1} and A_{I2}.

2) Conductive fluids: Let us use the general model shown in Fig. 3.2b to obtain the output voltage for t>0

$$V_{out} = \frac{C_1}{C_{in}} \cdot A_{I1} \cdot V_{dd} \cdot (1 - \frac{C}{C + C_1} e^{-\frac{t}{R(C_1 + C)}}) + V''_{off} \tag{5}$$

where V''_{off} is obtained from Eq. (6)

$$V''_{off} = \frac{(C_2 + C_3 + C_4)}{C_{in}} \cdot A_{I1} \cdot V_{dd} - \frac{(C_2 + C_3)}{C_{in}} \cdot V_{dd} \cdot A_{I2} + V''_{off} . \tag{6}$$

As seen in Eq. (6), the resistivity of the analyte (R) does not affect V_{out} for t>>0. Therefore, for the fluids of different conductivities, $V_{out} = A_{I1} \cdot C_1 \cdot V_{dd}/C_{in} + V_{off}$ for t>>0 and the sensor can be used as a detector of similar conductive fluids. It is however apparent that the equivalent resistance of such fluids is included in the time constant $\tau = RC_1$ in Eq. (5), which with the appropriate circuitry ($V_{out} \approx A_{I1} \cdot C \cdot V_{dd}/C_{in} + V_{off}$ for $t \leq 3\tau$) can be exploited for sensing purposes. The selectivity of the sensor against conductive or

non-conductive solutions could be explored through the deposition of appropriate sensing layer.

5) Calibration procedure: As seen in Eqs. (3) and (6), offset voltages can be adjusted by A_{I2}. These offset voltage compensations are necessary to increase the dynamic range of interface circuit. For this, a variable A_{I2} can be simply realized using two potentiometers R_{P1} and R_{P2} as shown in Fig.3.3. This simple solution has been used for the offset compensation in our fabricated chip; however, as discussed in part A of section V, a linear and on-chip circuit can be used instead for high precision applications. It is obvious that the transistor mismatches, parasitic capacitance mismatches, temperature variations and light absorption by semiconductor through transparent microfluidic structure can be considered the main factors of this offset voltage.

III. SIMULATION AND EXPERIMENTAL RESULTS

The simulation and experimental results of the proposed CMOS-based sensor and microfluidic components are put forward in this section.

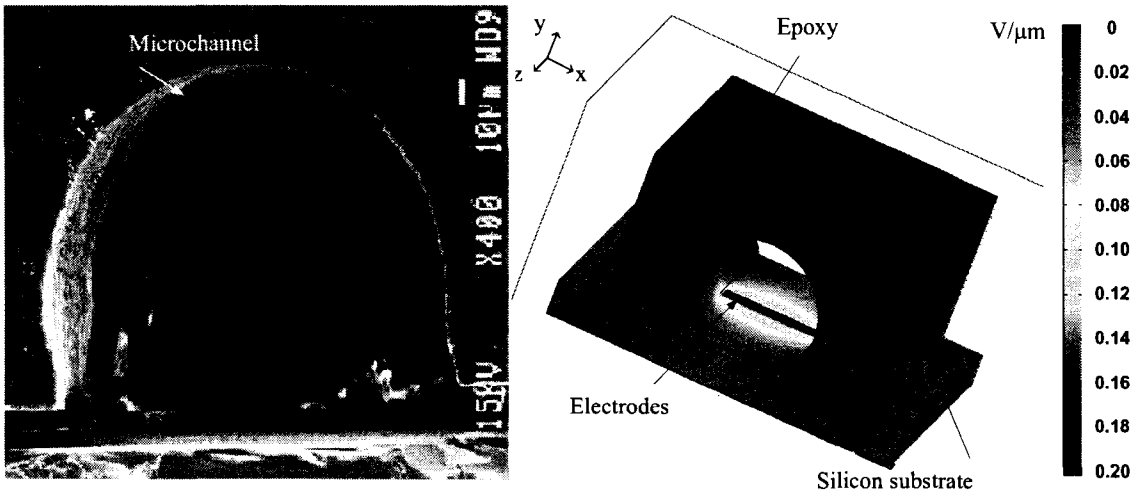
A. Modelling and simulation

The capacitive variation of interdigitated capacitor versus the thickness of a non-conductive liquid film (dielectric constant $\varepsilon_r = 9$) is simulated using a finite element software package - FEM-lab (Multiphysics COMSOL). These electrodes are embedded in the channel with a cross sectional shape similar to the shape observed experimentally. Fig. 3.4a shows a SEM image of the cross-section of a microchannel fabricated through

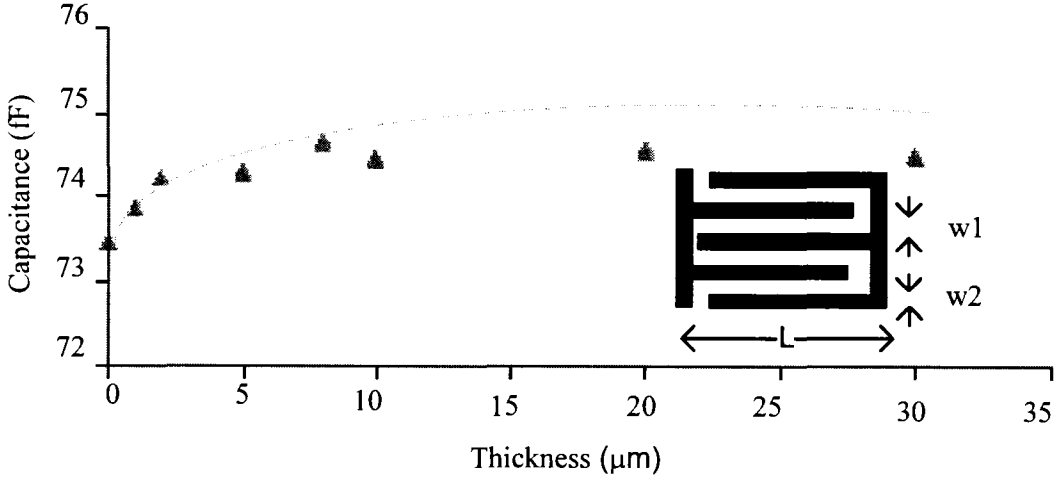
DWFP. Based on the simulation results shown in Fig. 3.4b, the dynamic range of this device is less than 1fF corresponding to only 3-microns variations of non-conductive film thickness. So, the volume of a non-conductive analyte can be scaled through a microchannel with height less than 3 μm. Of course, based on these results, it is apparent that the microchannels with large depth (or diameter in this paper) would not affect the equivalent capacitance of the sensing electrode.

The static parasitic capacitances can precisely be obtained using Cadensce. For this, two interdigitated electrodes as the same size of sensing electrode which was modeled in FEMLab (Fig. 3.4b) are implemented in Cadence; therefore, the extracted parasitic capacitances C_2 and C_3 are equal to 150fF and 25fF. A comparison between ΔC (1 fF) and the summation of parasitic capacitances C_3+C_2 ($\approx$175fF) can obviously reveals the need for a high resolution interface circuit in such on-chip capacitive sensors. It should be mentioned that the interdigiaited sensing electrodes consist of 20 fingers, so that the width (w1) and length (L1) of each finger are equal to 5 and 30 μm respectively. Also, the distance (w2) in between the fingers is 5μm. The maximum value of electrical field is around 0.2V/μm (very close to electrodes) while a differential potential equal to 1 volt is applied to the electrodes. For this, the modulation of capacitance can be performed in the region very close to sensing electrodes.

The variation of V_{out} (t=95 ms) versus temperature is also simulated through SpectreS in Cadence and shown in Fig. 3.5.



(a) (b)



(c)

Figure. 3.4. Simulation and modeling results of interdigitated capacitive electrodes (a) SEM image of microchannel fabricated through direct write process, (b) the FEMLAB model of microchannel and (c) the simulation results of extracted capacitance in between the electrodes for different thickness value of thin layer of liquid in channel.

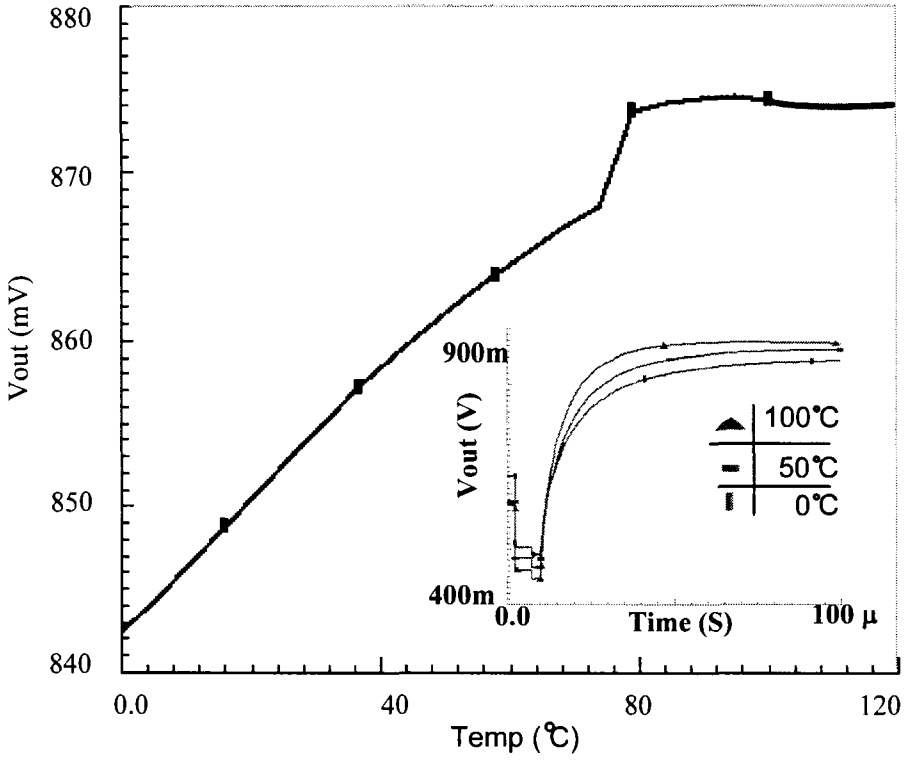


Figure 3.5. Simulation results of V_{out} variations versus temperature. The transient responses for 0, 50 and 100°C are shown in the inset.

This figure displays only a 33 mV deviation in V_{out} for a wide range of temperatures (0-120 °C). In reality however, the temperature variations of the fluid inside the channel atop the chip cannot surpass this voltage deviation. As already mentioned, a simple calibration technique can be applied using R_{P1} and R_{P2} to compensate such errors. In Fig. 3.6, the variation of V_{out} (t = 95 ms) versus R_{P1} and R_{P2} are displayed. Based on these results, the output voltage can be varied for different values of R_{P1} or R_{P2}. Also, V_{out} versus time for input differential capacitances ($\Delta C = C_S - C_R$) ranging from 0 to 3 fF are

displayed in Fig. 3.7. However, based on FEM simulation predictions of interdigitated capacitor in this design, $\Delta C \leq 1fF$.

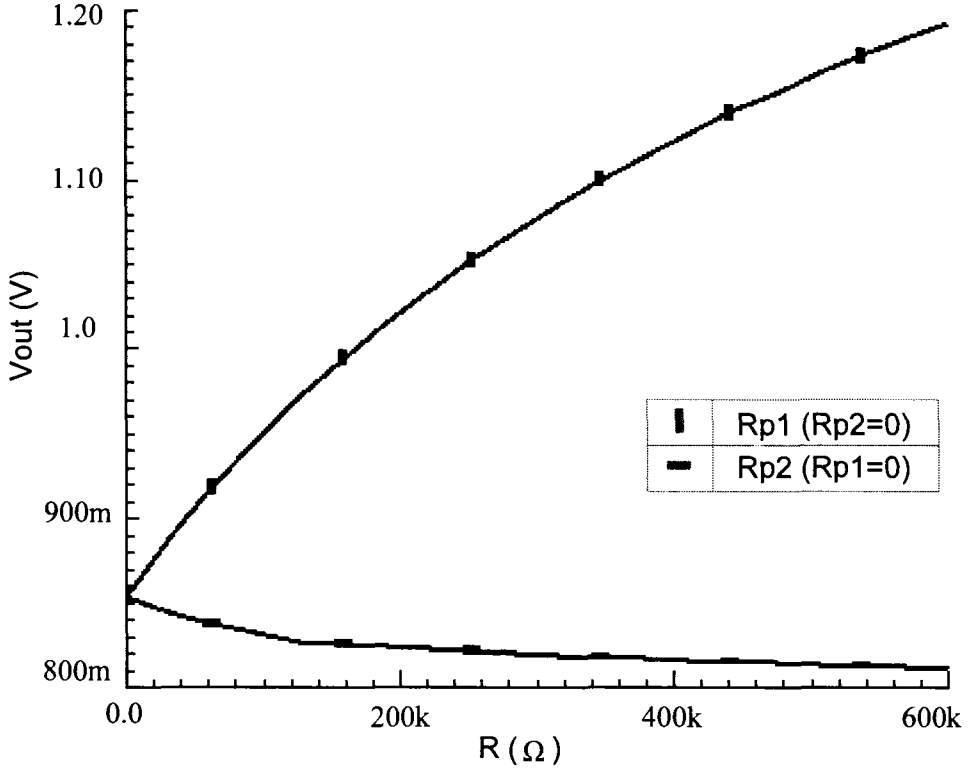


Figure 3.6. Simulation results of V_{out} variations versus Rp1 and Rp2.

B. Fabrication

The microelectronic chip has been fabricated by Taiwan Semiconductor Manufacturing Company's (TSMC) 0.18 micron CMOS process. A SEM image of the interdigitated sensing electrodes is shown in Fig. 3.8a. The interconnections between the fingers of these electrodes are achieved through the underlying metal layers and the passivation layers between these fingers have been removed using pad-etch process.

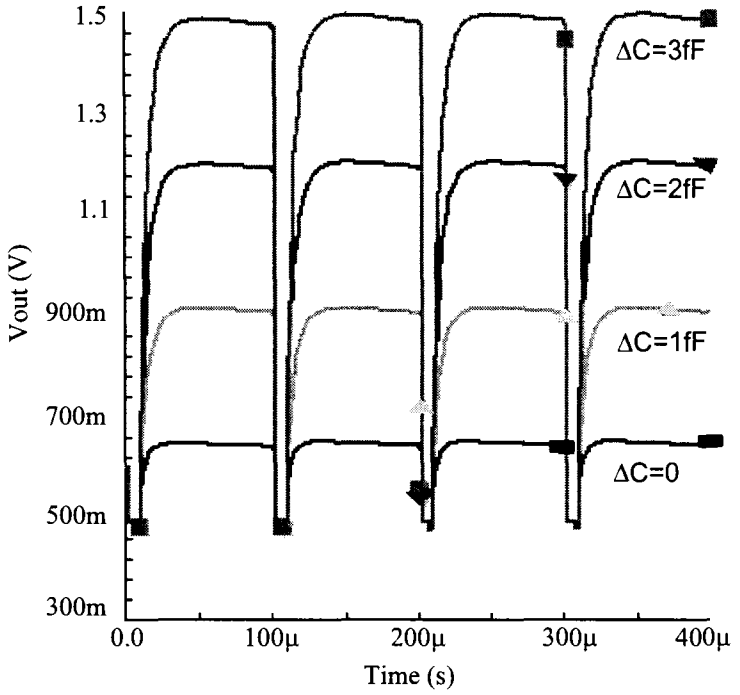
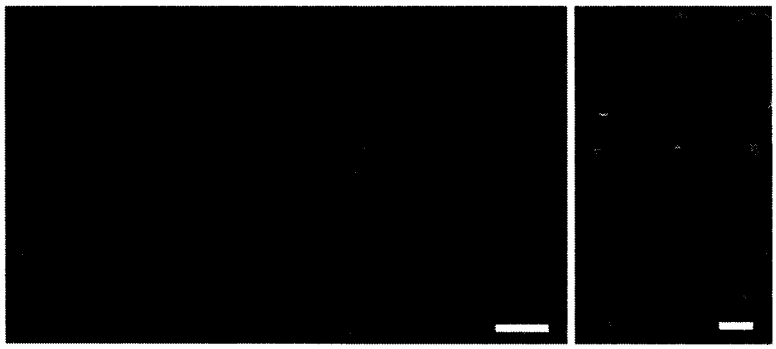


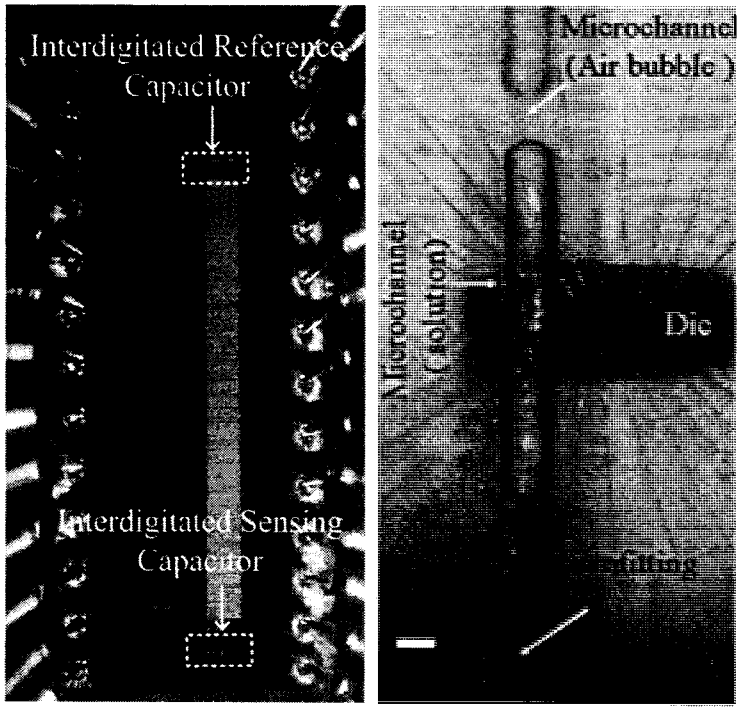
Figure 3.7. Simulation results of V_{out} versus time for different values of ΔC.

Also, as shown in Fig. 3.8b, pad-etch can be used to precisely pattern the passivation layers on CMOS chip. The created components can be sealed using low temperature bonding techniques [16] for high precision microfluidic applications. The packaged chip (40DIP-786 MOSIS) has been protected from electrostatic discharge (ESD) which is an important issue to be considered for DWFP as a soft post-processing. An optical microscope image of the top view of die including sensing and reference electrodes and interface circuits are shown in Fig. 3.9a. Following the direct-write microfluidic packaging procedure, a microchannel has been implemented on top of the proposed integrated sensor as shown in Fig.3.9b.



(a) (b)

Figure 3.8. Chip fabrication results: (a) SEM image of interdigited electrode realized on CMOS chip, (b) SEM image of a patterned passivation layers on CMOS chip (scale bar, 20 μm).



(a) (b)

Figure 3.9. Optical microscopic images of (a) loose die including interdigitated sensing and reference electrodes and (b) microfluidic channel with interdigitated sensor (scale bar 150 μm).

C. Preliminary sensing

A programmable interface system (SPARTAN-3, Xilinx) based on the field programmable gate array technology (FPGA) has been used to generate Φ_1, Φ_2 (Fig. 3.10a) at different frequencies and examine them on the integrated sensor. The desired frequency is 10 kHz. A stereo microscope is used to observe the solution injected in the channel while the oscilloscope (Digital Phosphor Oscilloscope, TD57154, Tektronix) measures V_{out}.

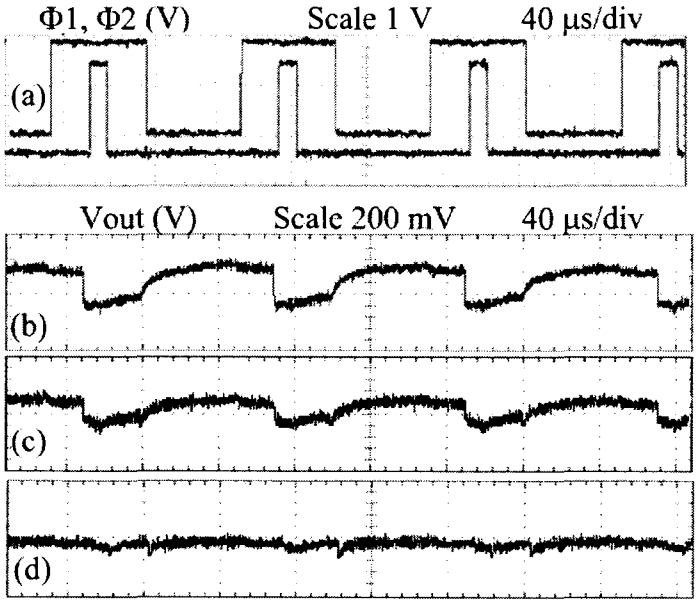


Figure 3.10. Measurements of (a) clock pulse and (b)-(d) V_{out} for different values of Rp1

As shown in Figs. 3.10b-d, while pulse signals Φ1 and Φ2 are high, V_{out} is low and when Φ1 and Φ2 get low, V_{out} increases. V_{out} of an empty channel is shown in Fig.10b where R_{p1}=100 and R_{p2}=0 kΩ. As shown in Figs. 3.10c-d, this signal is calibrated with a R_{P1} equal to 50 kΩ and 1 kΩ where R_{p2}=100 kΩ. An output voltage deviation was observed due to light exposure from the optical microscope light source. This error output voltage

was also compensated using the off-chip Rp1. Fig. 3.11a and 3.11b show the V_{out} variations for two different fluids injected in the microchannel which has been integrated to the capacitive sensor. As expected from the previous discussions, the change in output voltage for a non-conductive analyte (dichloromethane: ε_r =9.1) is ΔVout≈250 mV and the voltage buffer of the sensor is saturated for model biomacromolecule ΔVout ≈800 mV.

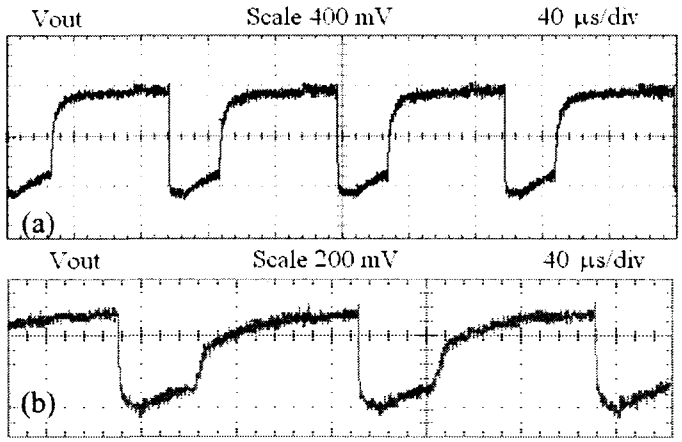


Figure 3.11. Measurements of V_{out} for (a) a model analyte (polyelectrolyte) and (b) dichloromethane solution in microchannel.

It should be mentioned that the interface circuit (except buffer) is not biased. For better experimental flexibility to measure the variation of output voltage of capacitive sensor and also to show the stability of results, an analog to digital converter part (TLC0820) along with other discreet components have been employed in connection with FPGA platform. This off-chip circuitry is incorporated to record the sensor's output and calculate the average of recorded samples for 2 seconds starting from the time that the channel is filled by a non-conductive solution and visually inspected through a

microscope. Fig. 3.12 shows the measurement set-up including FPGA platform and ADC board.

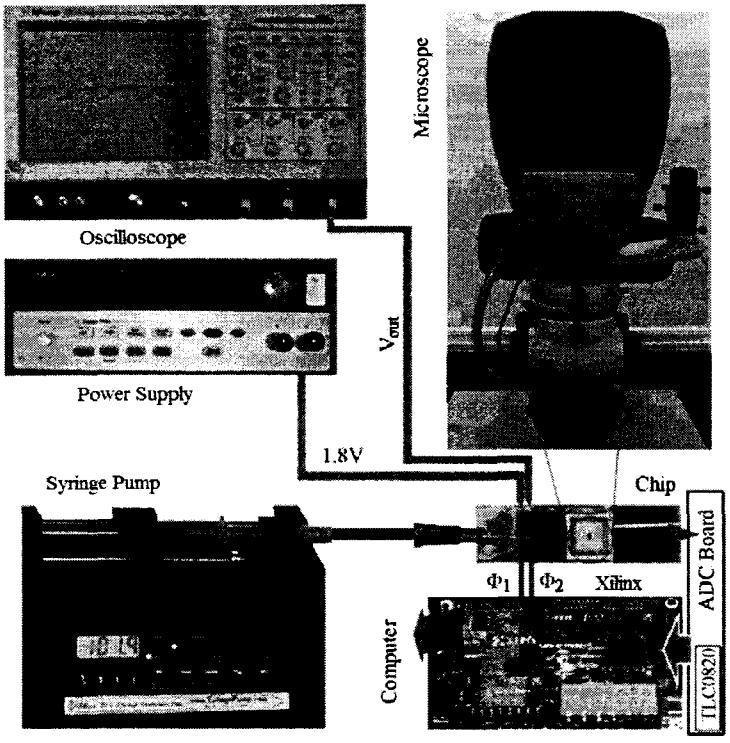


Figure. 3.12. Measurement set-up of proposed capacitive sensor LoC.

In order to demonstrate the viability of proposed capacitive sensor for LoC applications, three different solutions with known dielectric constants in addition to dichloromethane are used. These solvents are acetone, methanol and deionised water (DW). The dielectric constants of these solutions are 20.7, 32.6 and 80.4 respectively at 69°F. Also, a reliable cleaning procedure is performed before each measurement including water rinsing of microchannel, pre-heating treatment and air blowing into channel using an air dispensing system. This cleaning procedure assures there is no remnant in channel to change the output offset voltage. Fig. 3.13 shows the measurement results for aforementioned

solutions. As seen in this figure, ΔV_{out} is not exactly propotional to dielectric constant of analyte. This is due to C1 which is in series with C.

The stability of measurements is revealed in Table 3.1 while dichloromethane is injected in channel and the measurement is repeated for several times. In between the measurements, the cleaning procedure is performed and the channel is filled again with the solution. The error between the results could be negligible using a high resolution ADC instead of employed 8-bit ADC part. A summary of sensor specifications is presented in Table 3.2.

Table 3.1. Sensor response against dichloromethane in microchannel for several iterations.

≠	ΔV_{out} (V)	≠	ΔV_{out} (V)
1	0.2308	6	0.2295
2	0.2325	7	0.2304
3	0.2316	8	0.2317
4	0.2269	9	0.2285
5	0.2231	10	0.2297

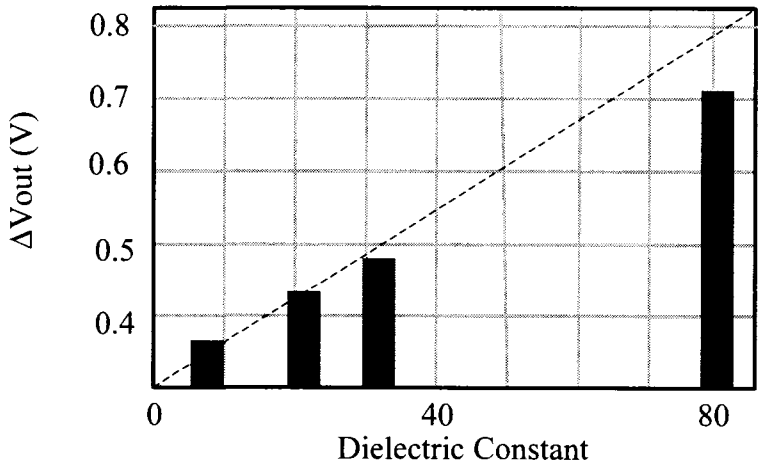


Figure 3.13. Sensor's response for different solutions.

Table 3.2. A summary of chip specifications.

Fabrication Process	0.18 μm CMOS TSMC
Power Supply (V_{DD})	1.8 V
Electrode (C_S and C_R) Area	100×30 μm^2
Interface Circuit Area	100×35 μm^2
Sensitivity ($S_{\Delta V/\Delta C}$)	≈ 230 mV/fF

IV. DISCUSSION

Certain design considerations of the capacitive sensor as well as some experimental issues of the microfluidic packaging procedure and important applications.

A. Sensor considerations

As already mentioned in sections III and IV, the offset voltage (V_{off}) of the fabricated sensor fluctuates owing to the residual analyte in the microchannels, thus affecting the precision and dynamic range of the sensor. Based on results presented in this paper, off-chip resistors do not compensate this error linearly and furthermore, it is not practical to use this technique with several capacitive sensors on a single chip. Instead, a highly-precise adjustable current mirror like the one shown in Fig. 3.3 would be more appropriate In this figure, the M_{C1}-M_{Cm} transistors along with M_7 are emploied to adjust the current reference I_R corresponding to digital input data $D_0 \ldots D_n$ [17] (see chapter 5).

B. Important applications

A CMOS based capacitive sensor LoC, from engineering point of view, consists of three different parts- microfluidic components for fluidic regulations, the sensing layer for

transducing the biological quantities to capacitance changes and finally on-chip capacitive measurement system for sensing of the capacitive changes. To date, so many different biochemical sensing layers such as immobilised antibodies [7] to recognise antigens or PEUT [5] layer to detect ethanol and toluene have been employed on capacitive sensors, but less attention has been placed on a complete and integrated LoC capacitive sensor. In this paper, much emphasis has been placed on the implementation of capacitive sensor and microfluidic channel as two important requirements for all CMOS based capacitive sensor LoCs. This device without any additional sensing layer can be used for dielectric measurement purposes. It is obvious, for selectively detection of any solution or bioparticle, extra sensing layer formation should be performed.

In addition to above mentioned applications, the detection of liquid in microfluidic structure is considered as the most important need for automation of a LoC system. Our proposed system, not only is capable to detect the presence of liquid through capacitive sensor, but also, can give an estimation of dielectric constant of non-conductive solution exposed to sensing electrodes. Furthermore, the conductive solutions can be recognized in this hybrid IC/microfluidic system as discussed and shown in sections II-B-2 and Fig. 3.13 respectively. For a continuation of our work on microfluidic procedures and CMOS capacitive sensor, the integration of a biochemical-functionalizing layer such as hydrogel is an important issue. The hydrogel formed in-situ in the channel or chamber can be exposed to a drop of acid producing a volume change in the hydrogel. This shrinking produces a mechanical deformation of the polypyrrole electrode coated atop the hydrogel

thus leading to a change of capacitance in sensor. Thus a hydrogel actuator can be converted to a hydrogel sensor through mechanoelectric transduction. More recently, this reversible volume change phenomenon has been exploited to introduce a novel method of biochemical detection by capacitively transducing the volume change [18-19]. High precision CMOS capacitive sensor incorporated with this moulded hydrogel structure is a good alternative for such hydrogel-actuated based biosensors.

V. CONCLUSION

We described a CMOS based capacitive sensor for LoC applications. The simulation and preliminary experimental results of the proposed microfluidic CMOS capacitive sensor are demonstrated with different chemical materials including polyelectrolyte hydrogel, dichloromethane, methanol, aceton and DI water. This capacitive sensor, in conjunction with microfluidic components and the formation of appropriate bio-functionalised layer, form an effective and versatile platform for chemical and biological Laboratory-on-chip applications. The implementation of a capacitive sensor array along with an on-chip sigma-delta ADC as a continuation of this work is currently under way.

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Chapter 4

CORE-CBCM CAPACITIVE SENSOR ARRAY FOR LOCS

4.1 Introduction

As mentioned in chapter 1, the capacitive sensor LoCs don't require a self-calibration module due to the differential method of measurement during the analyte injection. Instead, LoC capacitive sensors are always suffer the offset error resulting from mismatch process, remnant in micochannel and/or mechanical artifices. For this, a simple calibration method is integrated with the interface circuit as discussed in chapters 3 and 4. Additionally, two different charge based capacitive sensors with different level of complexity are realized in 0.18 μm CMOS process. The post-layout simulation and experimental results are demonstrated and discussed in this chapter. This work will appear in "IEEE Transaction of biomedical circuits and systems" as reproduced as follows.

4.2 A Hybrid Microfluidic/CMOS Capacitive Sensor Dedicated to Lab-on-Chip Applications

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Accepted to be published in: IEEE Transaction on Biomedical Circuits and Systems, 2007

ABSTRACT

A hybrid microfluidic/IC capacitive sensor is presented in this paper for highly integrated Lab-on-Chips (LoCs). We put forward the design and implementation of a charge based capacitive sensor array in 0.18 micron CMOS process. This sensor chip is incorporated with a microfluidic channel using direct-write microfluidic fabrication process (DWFP). The design, construction as well as experimental results are demonstrated using four different chemical solutions with known dielectric constants. The proposed highly sensitive CMOS capacitive sensor (≈530mV/fF) along with low complexity DWFP emerges as clear favourite for LoC applications.

Index Terms - CMOS technology, capacitive sensor, Lab-on-Chip, Microfluidic packaging.

VI. INTRODUCTION

CMOS-based capacitive sensors have recently attracted significant interest for a range of biochemical testing LoCs such as antigen detection through antibody binding (e.g., virus detection [1]), cellular analysis [2-3], DNA recognition [4] and chemical sensing [5]. A hybrid microfluidic/CMOS capacitive sensor is recognized as an important requirement for such fully integrated LoC applications. In this paper, we address this challenging issue by proposing an array of capacitive sensors implemented in CMOS process and integrated with microfluidic channel (see Fig. 4.1). An application-specific

biofunctionalized sensing layer could be formed on the sensing sites for selectively detection purposes which is not the case of this paper.

Up to date, several readout techniques with different design strategies have been reported for autonomous capacitive sensors systems (e.g. MEMS based accelerometer [6]) but there is a little published literature on custom design of on-chip capacitive sensor LoCs. Capacitive sensors for LoC applications do not require determining a single value of the sensing capacitance, but to distinguish between the device behavior in the presence rather than in the absence of analyte in microfluidic channel. In fact, the static capacitance values prior and after analyte injection are extracted deviating from dynamic capacitive measurement in the most of applications [7]. For this, the average based techniques can effectively be employed with much more simplicity. This low complexity is an important issue for design and implementation of large capacitive sensor arrays [3]. Actually, the implementation of a large array of sensing circuits on one die implies a small circuit footprint. This precludes the use of most operational amplifier -based circuits, which occupy a large area. Charge based capacitance measurement (CBCM) is a simple method which was originally proposed in 1996 for sub-femto Farad interconnects capacitance measurements in deep CMOS chip [8]. Due to low complexity, low area and high precision, this static measurement method emerged as the clear favourite for meeting the present requirements in capacitive detection LoCs. Among very few works using CBCM for capacitive sensors, Guiducci et al. reported DNA detection through an off-chip circuitry along with integrated electrodes [9]-[10]. In this paper, emphasis is

placed on fully integrated core-CBCM capacitive sensors suitable for LoC applications. In order to show the applicability of CBCM for capacitive sensors, a test chip (TC1) is initially implemented featuring a large interdigitated electrode in connection to only one n/pMOS pair (Fig. 4.1). As CBCM utilizes external instrumentation, it cannot be applied directly for integrated sensors. For this, a complementary circuit is designed and implemented in CMOS process (TC2).

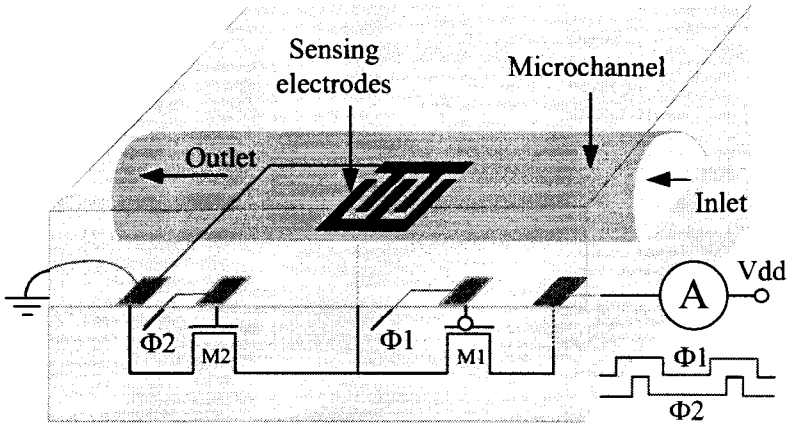


Figure 4.1. Schematic of a hybrid Microfluidic/CMOS capacitive sensor using CBCM method.

This sensor chip includes an array of interdigitated electrodes and interface circuits for capacitance to voltage conversion. Further designs and developments are also discussed and demonstrated to embed the whole sensor system on chip.

A microfluidic packaging process should be performed for all aforementioned LoC applications, through a low temperature process with a reliable and hermetic bonding. We have already reported this challenging issue by proposing a direct-write microfluidic

fabrication process (DWFP) [11]. This reliable and robotic-based process is employed to implement microchannels on wire-bonded capacitive sensor chip.

Organic solvents with known dielectric constants are good alternative to model the capacitive variation due to dielectric change in proximity of sensing sites. We characterize the proposed hybrid sensor and show its viability for LoC applications through such chemical solutions including dichloromethane, acetone and methanol.

The reminder of this paper is organized as follows. In section II, the analysis and design of core-CBCM interface circuits is described. In section III, further developments on the proposed circuit are put forward. The experimental procedures and results including microfluidic packaging are discussed and demonstrated in sections IV and V respectively. These sections are followed by a summary in section VI.

VII. CORE-CBCM INTERFACE CIRCUIT

The designs of two sensor chips with different levels of complexity are described in this section.

A. Capacitive characterization test-bed

CBCM structure is employed in TC1 in order to measure the capacitance changes in two steps. As shown in Fig. 4.1, one electrode is grounded and another one is connected to drain sides of n/pMOS pair. At the first step, the charging current I_1 is recorded through DC Ammeter (A) while the channel is empty. Therefore, the combination of all parasitic

capacitances (C_0) related to MOS transistors and electrodes is obtained by Eq. (1).

$$I_1 = f \cdot V_{dd} \cdot C_0 \tag{1}$$

where f and V_{dd} are the frequency of pulse signals and power-supply voltage respectively. At the second step, the solution is injected into microchannel and the charging current (I_2) is recorded. As seen in Eq. 2, this current is proportional to the combination of C_0 and the consequence capacitance variation ΔC.

$$I_2 = f \cdot V_{dd} \cdot (C_0 + \Delta C). \tag{2}$$

Therefore, C_0 and ΔC could be obtained through Eqs. (1) and (2) with a given value of f. It is worth pointing out that this chip can be used as a simple method for the characterization of capacitive LoC sensors. Through this characterization procedure, the input capacitance variation and contributed parasitic capacitances are extracted. These extracted data could be used as a simplified model for design and optimization of on-chip circuits dedicated to LoC applications. Finite element based CAD tools such as FEMLab are conventionally applied for per-assessment of such capacitance changes. However, in addition to physical dimensions, the modeling of such applications requires a lot of preliminary data, such as physicochemical data and processing which are seldom available, thus, an experimental characterization method that would carry out analyses accurately without relying on previously available data is highly desirable. We believe that CBCM is the best alternative for this purpose.

B. On-chip capacitive sensor

In order to replace the external measurement device with an on-chip circuitry, an interface circuit is designed and implemented in TC2.

- *Analysis*

The basic unit of proposed interface circuit (UIC) is illustrated in Fig. 4.2. In this circuit, a current mirror, composed of M_3 and M_4, is used to sense and amplify the charging current (I_S), which is converted into voltage in integrating capacitor (C_{in}). Once $\Phi 1$ is low, the voltage on C_S (V_S) starts rising rapidly following Eq. (3).

$$C_S \frac{dV_S}{dt} = K_x \cdot (V_{gs} - V_{TP})^2 \tag{3}$$

where K_x also depends on the parameters of process and V_{gs} and V_{TP} are the gate source voltage and the threshold voltage of p channel MOSFET respectively. Also, the switch-on and off resistances of M_1 and M_2 have been discounted. By substituting $V_{dd} - V_S$ instead of V_{gs} in (3), and considering $V_S = 0$ at $t = 0$ (discharging) when $\Phi 1$ and $\Phi 2$ are high, Vs is obtained by Eq. 4

$$V_S = (V_{dd} - V_{TP}) - \frac{(V_{dd} - V_{TP})C_S}{K_x (V_{dd} - V_{TP})t + C_S}. \tag{4}$$

As seen in this equation and Fig. 4.2, by assuming the charging current transients to have the sufficient time in order to settle during the period of the square wave, V_S will consequently rise to within one threshold voltage of the power supply at which point M4 is cut-off. In this case, the voltage on integrating capacitor is

$$V_{out} = \frac{W_4 / L_4}{W_3 / L_3} \cdot \frac{(\Delta C + C_0)}{C_{in}} \cdot V_S \cdot \tag{5}$$

where W_4/L_4 and W_3/L_3 are aspect ratios of M_4 and M_3 respectively.

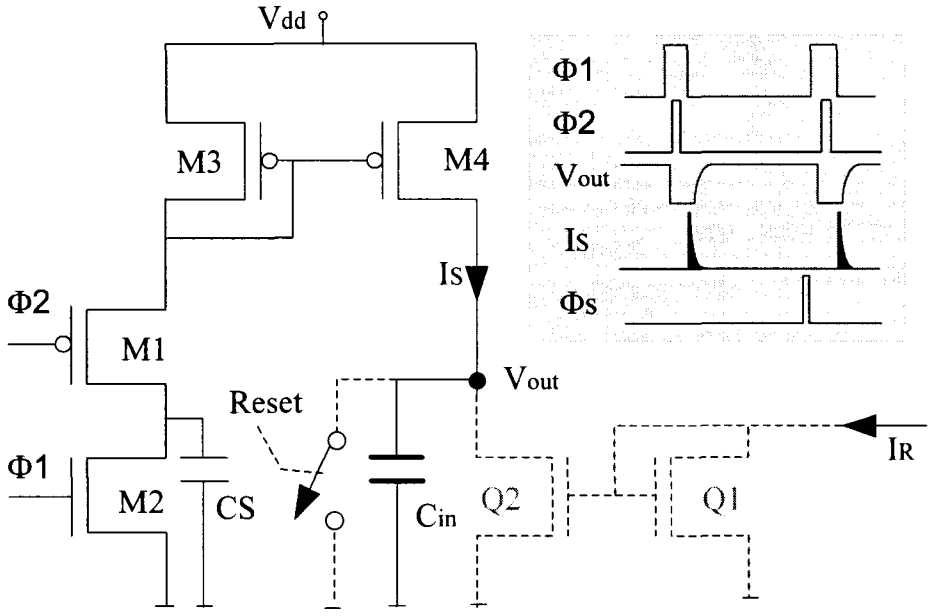


Figure 4.2. Illustration of the proposed BIC along with the waveform of clock pulses, sensing current Is and sensor response Vout (As discussed in section II, B, Φs is the sampling clock pulse).

It is obvious that the dynamic range of V_{out} remains limited due to $Co>>\Delta C$. For this, a replica of interface circuit is used to generate a reference current I_R. As shown in Fig. 4.2, this current is mirrored into output node through another current mirror and subtracted from I_S. Thanks to its symmetry and differential operation, V_{out} is expressed by Eq. 6

$$V_{out} = \frac{\Delta C}{C_{in}}(V_{dd} - V_{TP}) + V_{off} \cdot \tag{6}$$

The residual offset voltage V_{off} is mainly due to mismatch error of current mirrors and CBCM circuits. In order to minimize the effect of this error, an adjustable current mirror is employed as shown in Figs. 4.3a and 4.3b. Corresponding to each digital input D1-Dm ($D_{1\text{-}m}$) shown in Fig. 4.3b, a given current (I_R) is drawn from M_{C1}-M_{Cm} with aspect ratios given in Eq. 7.

$$\frac{W_{13}}{L_{13}} = 2 \cdot \frac{W_{C1}}{L_{C1}} = 2^2 \cdot \frac{W_{C2}}{L_{C2}} \ldots = 2^m \cdot \frac{W_{Cm}}{L_{Cm}} \tag{7}$$

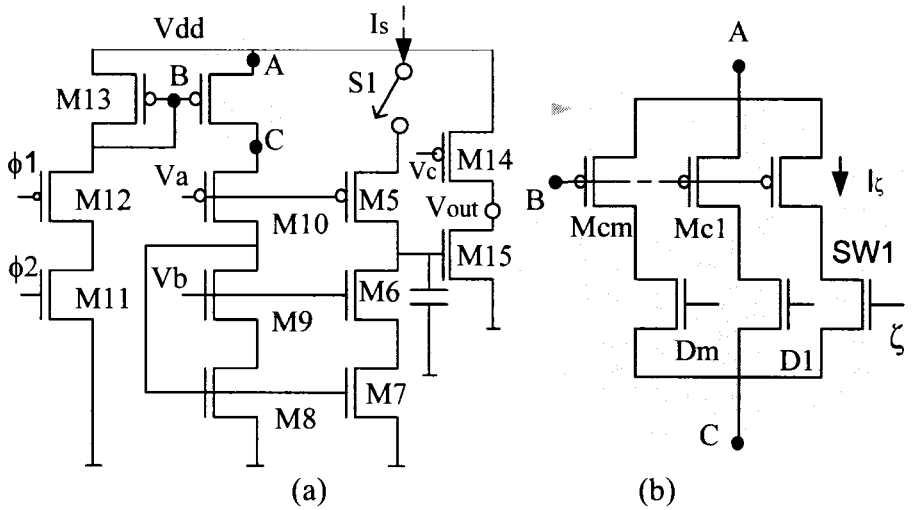


Figure 4.3. Adjustable current mirror: (a) wide swing current mirror and I_R generator, (b) digital current trimming (For Sw1 and ζ see section III).

In this design, the digital input data is generated in an off-chip circuitry as it will be described in next section. Furthermore, as shown in Fig. 4.3a, in order to improve the swing of output voltage V_{out} and minimize the leakage from C_{in} especially for low frequency clock pulses, a wide swing current mirror (M_5-M_{10}) is used instead of simple

current mirror shown by dot-dash lines in Fig. 4.2.

On the other hand, M_{14} and M_{15} form a source follower amplifier which buffers the integrating node from any stray capacitance of subsequent stages. It should be mentioned that V_{off} is automatically eliminated in the subtractions of two subsequent measurements prior and after analyte injection. Therefore it has no significant effect on the accuracy of capacitive detection.

- **Capacitive Sensor System**

As shown in Fig. 4.4, the sensor system embedded in TC2 features four interdigitated electrodes which are used as the sensing (C_{S1}-C_{S3}) and reference (C_R) capacitors, three UICs, an adjustable current mirror (see Fig. 4.3), and a simple unity voltage buffer.

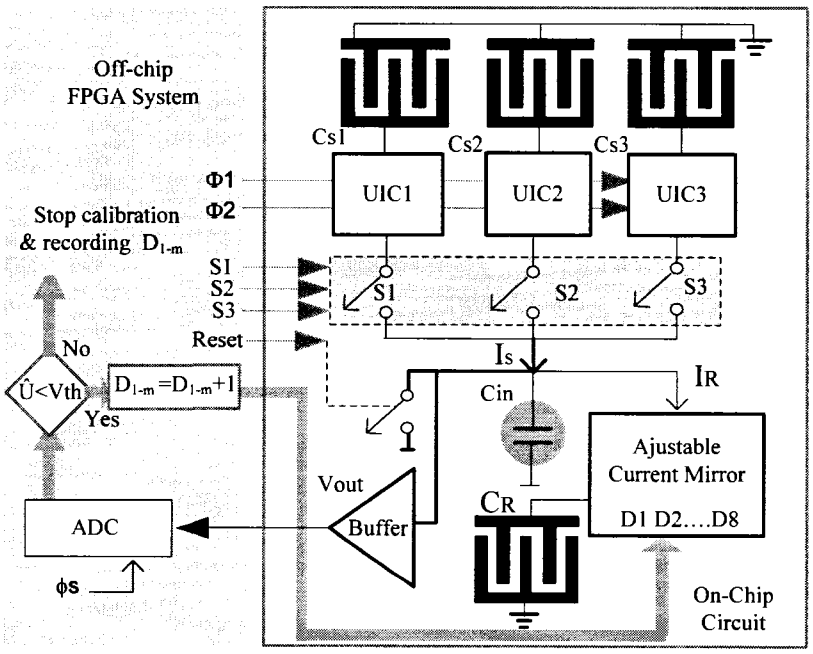


Figure 4.4. On-chip and off-chip architecture circuitries : TC2 and supporting FPGA system for calibration.

This chip requires both analog (V_{out}, V_a,V_b and V_c) and digital ($D_{1\text{-}m}$) I/O signals. In this design, sensing electrodes are selected using digital addressing lines S_1, S_2 and S_3 (Š) while, control logic includes reset and clock signals Φ1-Φ2.

Prior to analyte injection, the calibration procedure should be performed through finding the optimum value of digital input data $D_{1\text{-}m}$. For this, an off-chip module is commanded to start the sensor calibration before performing a measurement. This supporting module is realized in a FPGA platform including an analog to digital converter (ADC). The digital output of ADC (Ũ) is used as decision criterion in the calibration algorithm realized by the off-chip module. In each period of clock Φ1, if V_{out} is larger than a threshold voltage (V_{th}), $D_{1\text{-}m}$ is incremented until it reaches the desired value. Based on the considered aspect ratios of M_{C1}-M_{C8}, initially I_R is less than I_S, so the calibration process always starts with a value of V_{out} larger than V_{th}.

As seen in Fig. 4.4, $D_{1\text{-}m}$, Š and clocks (Φ1 and Φ2) are supplied by off-chip module implemented in FPGA (AFS600, Actel). The digital signal (Ũ) is finally acquired and stored in a PC.

- **Simulations**

Post-layout simulation using SpectreS was accomplished in order to validate the design presented in this section and look for optimal design performance. The output voltage waveform of the integrator C_{in} during the clocking cycle has already been reported [11] for a range of ΔCs. The linearity of V_{out} variation (ΔV_{out}) versus ΔC is emphasised in Fig. 4.5 that is in good agreement with Eq. (6).

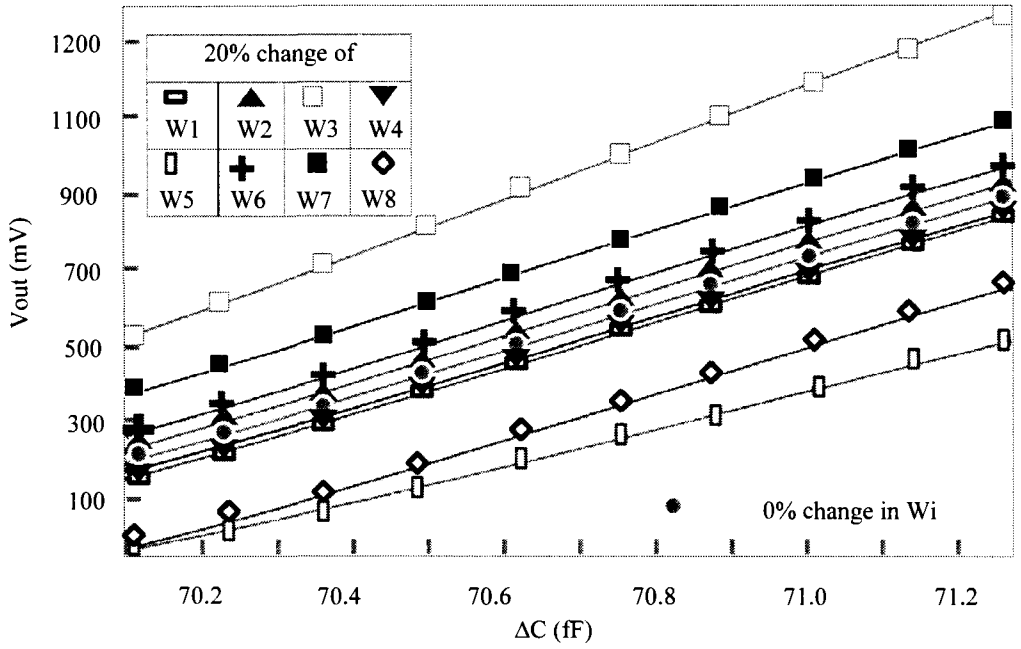


Figure 4.5. Variation of simulated V_{out} versus □C for different mismatch errors (20% change of a transistor's width) .

It should be mentioned that based on the post-layout capacitance extraction $C_0 \approx 70.2$fF for each reference and sensing electrodes (C_R and C_{S1}-C_{S3}). As shown in this figure, 20% change of W_1, W_2 and W_5-W_8 significantly affect V_{off} with no change in sensitivity. However, it is predictable that the mismatch errors of W_3 and W_4 affect on V_{off}, and sensitivity as well. Of course, a configuration similar to calibration one can be used to compensate this error by adjusting the current gain (M_3-M_4). These simulations have been carried out for a current gain of 10 with an integrating capacitor of 1.2 pF. In fact, based on simulation results, for $C_{in} < 250$fF, V_{out} does not follows the Eq. (6) [12-13]. This can likely be due to stray capacitances on this node. Referring to simulation results

in Fig. 4.5, it can be revealed how offset cancellation is important to obtain full output dynamic range. Also, based on the simulation results, the sensitivity of interface circuit is around 530mV/fF, of course for C_0=70 fF.

III. EFFICENT DEDICATED ADC

For a fully integrated sensor, it is required to design a digital readout circuit for recording and further processing purposes. In this section, following our proposed core-CBCM circuitry, we present a simple and still efficient ADC circuit which is realized with only a few more devices added to interface circuit. Let us remove "Reset" from Fig. 4.2 and allow V_{out} to step up in each period as shown in Fig. 4.6.

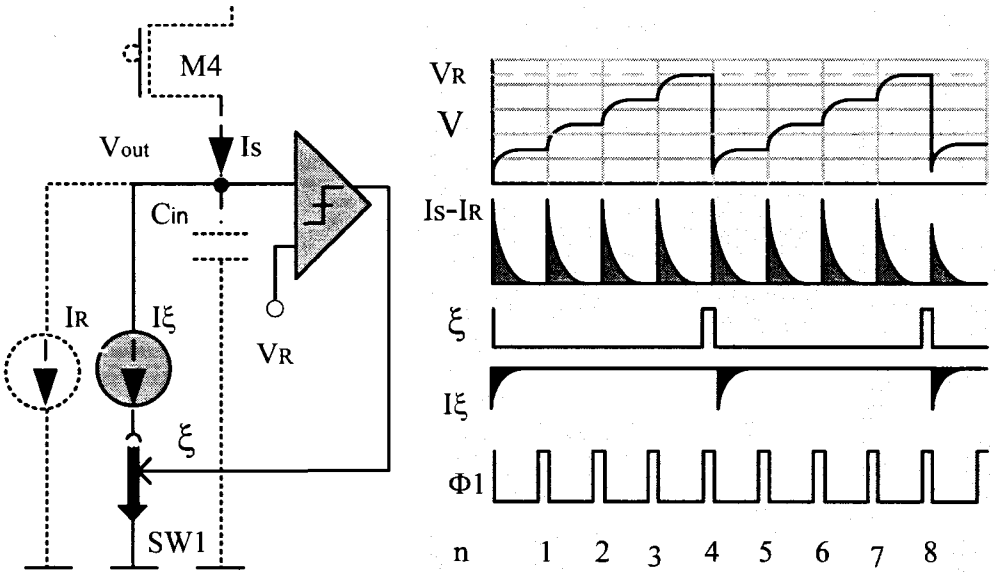


Figure 4.6. Proposed charge based sigma delta capacitive sensor and corresponding waveforms.

Vout is compared with a reference voltage (V_R) and the output of comparator (ζ) is used to command switch SW1 which is in series with a current source I_ζ as shown in Figs. 4.6 and 4.3b. This configuration features a simple one-bit DC input first-order ADC. This digital readout circuit is implemented in CMOS process using a track and latch voltage comparator as shown in Fig. 4.7 [14] in connection with already discussed interface circuit. This track and latch comparator consists of a differential amplifier (M28 and M16) sensing the input differential voltage.

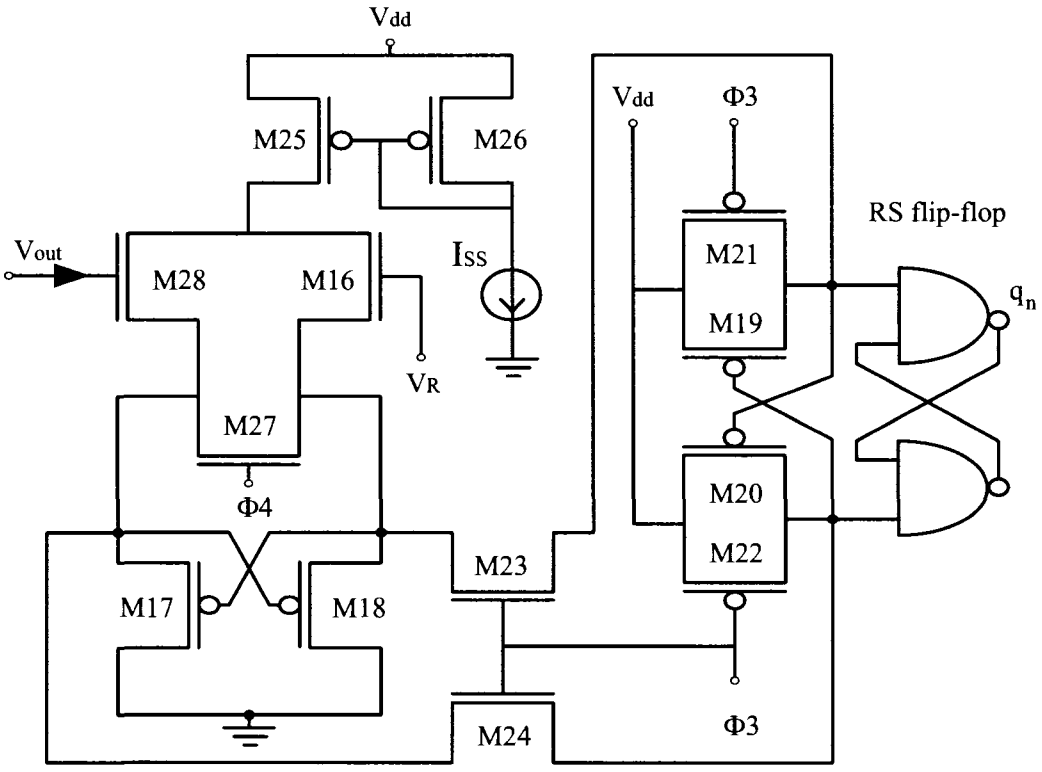


Figure 4.7. Implemented voltage comparator incorporated with ΣΔ modulator.

The logic states of M19-20 results from the generated drain current on M28 and M16 where Φ3 is high and Φ4 is low. Once Φ3 becomes high, the regenerative process starts on M19-20 resulting from initializing M17-18 logic states. RS flip-flop operates as a latch to save the logic states of M19- M20 during one clock pulse period. The post-layout simulations show different pulse stream for different values of ΔC as illustrated in Fig. 4.8.

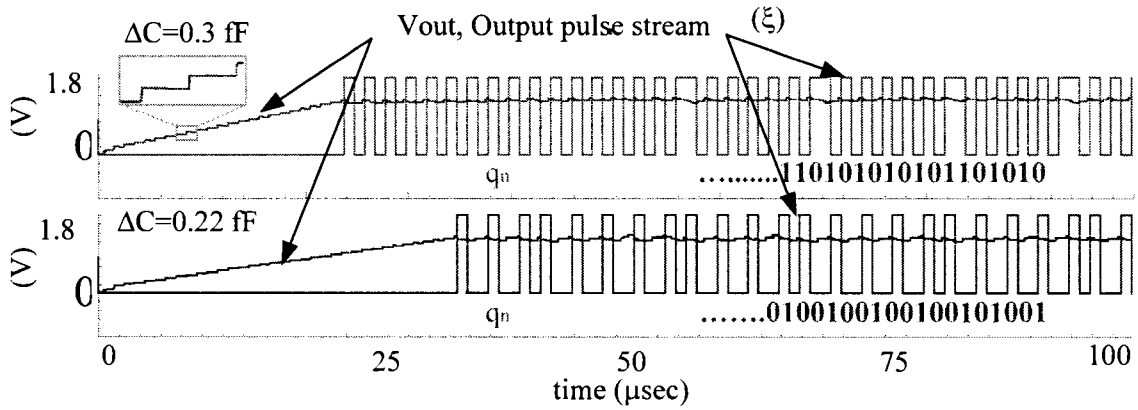


Figure 4.8. Simulation results of proposed sigma delta capacitive sensor.

As seen in Fig. 4.9, the average of each sequence (the number of one's per the number of pulses in each sequence) is proportional to ΔC. Based on these results, it can be concluded that the proposed low cost ADC is similar to conventional DC input sigma delta.

VIII. EXPERIMENTAL PROCEDURES

In this section, chips fabrication, measurement set-up and microfluidic packaging process are put forward and demonstrated.

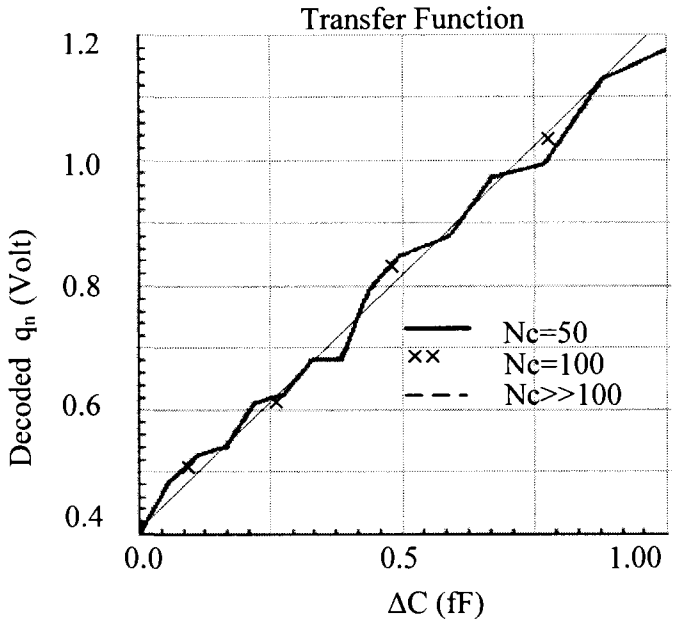


Figure 4.9. Sensitivity of decoded output sequence of proposed ΣΔ versus input ΔC.

A. Chip fabrication

The microelectronic sensor chips (TC1, TC2) were fabricated by Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 micron CMOS process. Figs. 4.10a-b show the microphotograph of both chips. It should be mentioned that pad-etch technique in CMOS process has been used to remove the passivation layers in between the electrodes fingers in order to increase the sensitivity [12]. This issue along with the non-uniformity due to this etching technique is shown in SEM image (Fig. 4.10c). As seen in Fig. 4.10d, integrating capacitor C_{in} and adjustable current mirror occupy half of interface circuit area; however, it does not require to be repeated in array of capacitive sensors.

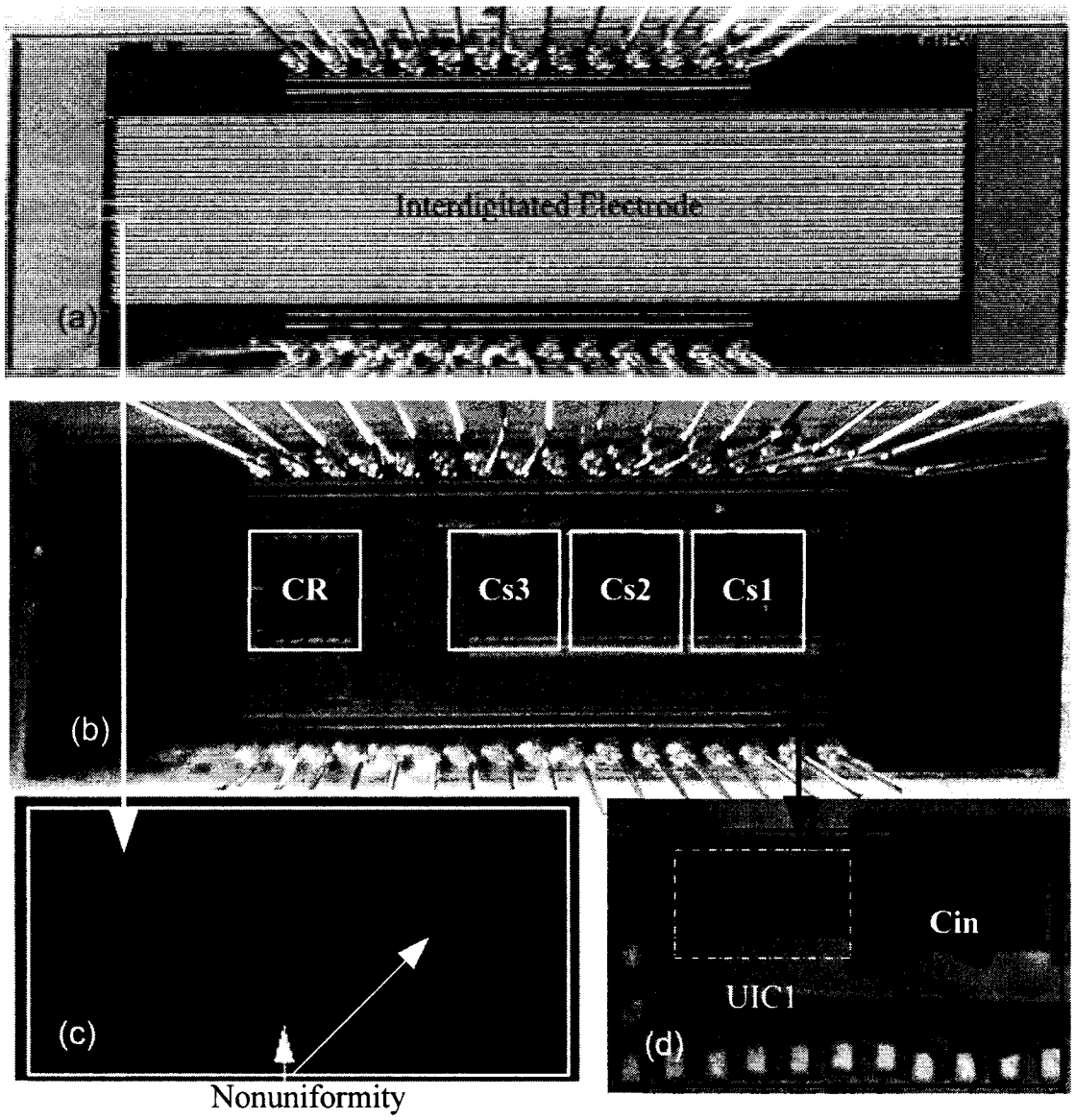
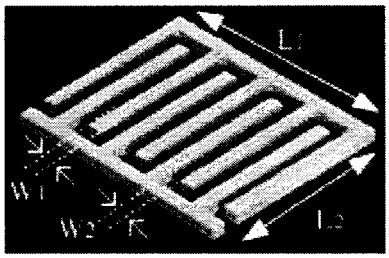


Figure 4.10. Chip fabrication results: optical microscope images of (a) TC1 and (b) TC2 along with (c) SEM images of interdigitated electrode, and (d) optical microscopic image of interface circuit layout (UCI1 is the first unit of capacitive interface circuit , see sectionII-B).

Also, the dimension of sensing electrodes C_S in TC1 and sensing and reference electrodes (C_R, C_{S1}, C_{S2} and C_{S3}) in TC2 are shown in Table 4.1 where $W_1=W_2=W$.

Table 4.1: Dimensions of interdigitated electrode in both fabricated chips (All geometries are in μm scale).

	TC2	TC1
L1	100	2500
L2	100	720
W	10	9



B. Direct-write microfluidic fabrication process

It is a threefold process: sacrificial paste-like ink deposition through a micronozzle on substrate on chip, encapsulation of ink filaments with liquid epoxy and ink extraction in a moderate temperature (75°C) and light vacuum after the hardening of epoxy [11]. Following this procedure, the microfluidic channels are constructed on sensor chips (TC1- TC2).

C. Multidisciplinary measurement set-up

A stereo microscope is used to observe the solution which is injected by a syringe pump into the inlet of microfluidic channel. Simultaneously, the oscilloscope (Digital Phosphor Oscilloscope, TD57154, Tektronix) monitors the periodic V_{out}. As already mentioned, a FPGA platform support the sensor chip for data recording and help the search for optimum measurement conditions.

IV. MEASUREMENT RESULTS

The electrical characterization along with chemical testing results is presented in this section.

A. Sensing electrode characterization

Referring to the discussion in section II-A and following measurement steps of TC1, the differential charging current (I_1-I_2) versus frequency for four solutions are obtained and given in Fig. 4.11. These solvents are used to measure the capacitance changes. These solvents are dichloromethane, acetone, methanol and deionized water (DW). The dielectric constants of these solvents are 9.1, 20.7, 30.4 and 80.4 respectively at 69°F.

It should be mentioned that the conductivity of dichloromethane as non-polar solvent is almost zero and the low conductivities of DI water (0.04 μS/cm), acetone (0.02 μS/cm) and methanol (0.12 μS/cm) can be discounted. In this work, V_{dd} keeps at its maximum value (1.8 V) and the frequency is varied up to four decades in order to demonstrate the linearity and viability of Eq. (1) for dynamic capacitance characterization. For this wide frequency range, the measurement results are revealed in logarithmic scales. The parallel straight lines in Fig. 4.11a are in agreement with following Eq. (8), which has been resulted from the combination of Eqs. (1) and (2).

$$\log(I_2 - I_1) = \log f + \log(V_{dd} \cdot \Delta C) \tag{8}$$

Therefore, the capacitance variation (ΔC) associated with each solution could be extracted from the continuing of these curves. In fact, in this logarithmic demonstration,

for different solutions the width of origin (A, B, C and D) is different while the slopes of these curves are as the same.

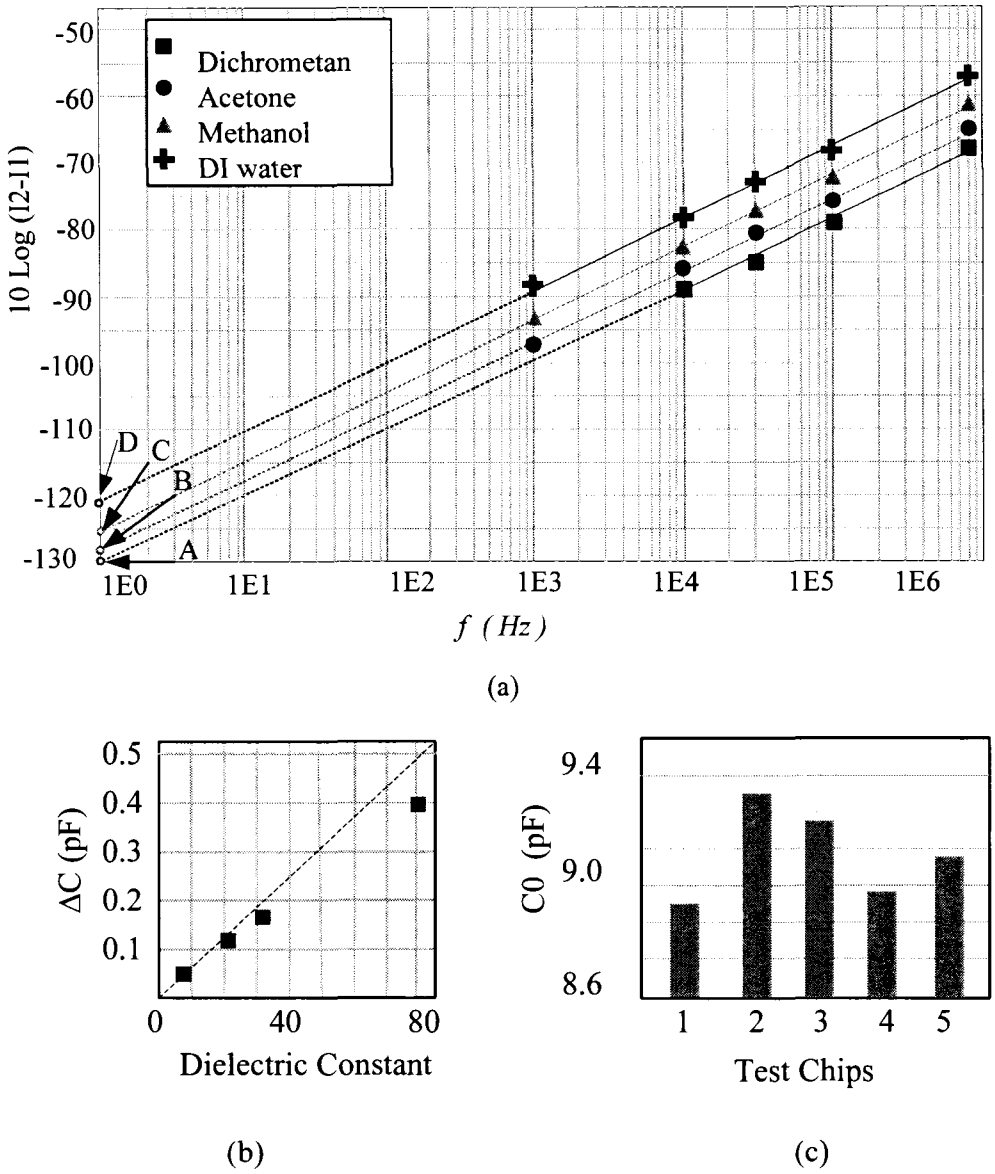


Figure 4.11. Measurement results: (a) differential current versus frequency for four different solutions, (b) the capacitance variation of chip versus dielectric constant and (c) the parasitic capacitance of 5 different chips.

.Fig. 4.11b shows the extracted ΔC versus dielectric constant. Each measured value in Fig. 4.3a is obtained from the average of 5 times repeated measurements followed by a cleaning procedure (see section IV-B).

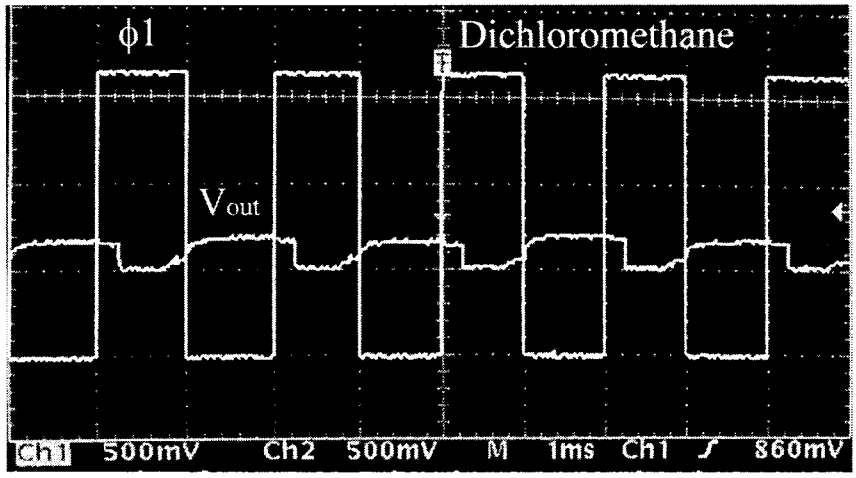
Similar measurements are performed to extract C_0 for five chip samples when no solution has been introduced on the electrodes (Fig. 4.11c). The difference between the extracted C_0 from different chips could be due to non-uniformity of pad-etching (see Fig. 4.9c) and/or CMOS process tolerance. Based on these results, TC1 can be used as low complexity sensor chip for LoCs.

B. Chemical testing

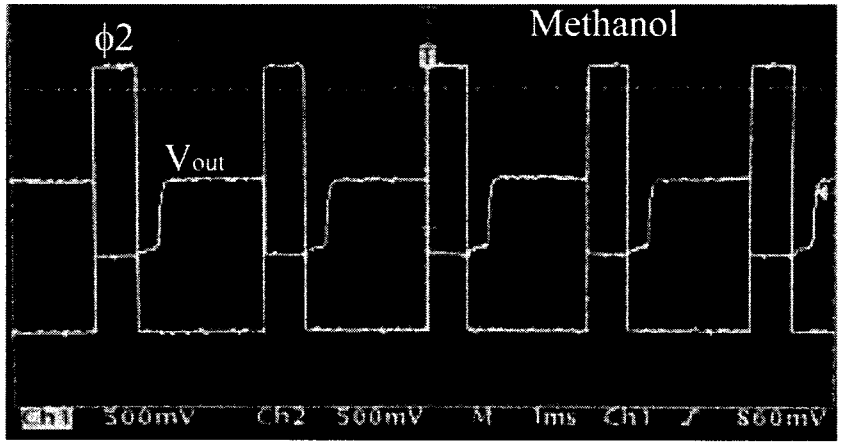
Following the calibration procedure discussed in section II-B while microchannel is empty, V_{off} is minimized. Of course, for lower $V_{off,}$ more than eight calibration bits (D1-D8) should be considered in circuit design. As anticipated, V_{out} rises up (f=1kHz) when the interdigitated electrodes are exposed to dielectric solutions (Dichromethan, and Methanol) and falls down during discharging period as shown in Figs. 4.12a-b. DC voltage of V_{out} can be adjusted through V_c (See Fig. 4.3a).

A cleaning procedure with hot water, air blowing and temperature treatment is performed in between the measurements prior to reinjection of solution. In order to evaluate the response time of sensor, the average of recorded data from three electrodes is recorded during 50 seconds. This procedure is repeated for different solutions with cleaning procedure in between the measurements. As shown in Fig. 4.13, once the analyte introduced to sensing electrode, the corresponding voltage appeared in the output

of sensor as fast as the speed of interface circuit. In this work, the sharp output variation of sensor in Fig. 4.13 is due to direct measurement of analyte without extra sensing layer on top of sensing electrodes. For example, using PEUT sensing layer for chemical detection in gas phase causes a linear sensitivity for a wider dynamic range of analyte concentration and consequently slower response of sensor [4].



(a)



(b)

Figure 4.12. Measurement results: Vout when a channel is filled with (a) Dichloromethane, and (b) Methanol.

Therefore, with additional sensing layer, the response time can be more than the results shown in this section.

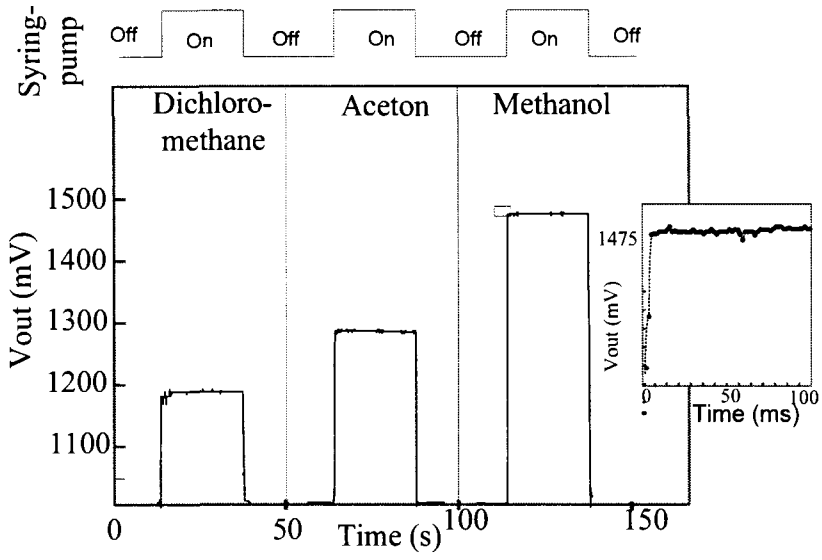


Figure 4.13. Testing results: recorded V_{out} when the channel is, empty (after calibration), filled with Dichloromethane, Acetone and methanol (Dielectric constant of Methanolis is nearly 32.4 at 77 °F).

In another test, ΔV_{out} correspond to C_{S1} become 650mV and 800mV for injected DW and conductive saline water respectively. Actually, the higher dielectric constant (Dielectric constant of DW $\approx$ 80.5), the higher ΔV_{out} is anticipated. But, in the case of injected saline water, higher ΔV_{out} is due to the effect of a large parasitic capacitance across the passivation layer [15]. It is worth to mention, that most of biological solutions are ionically conductive, however for aforementioned applications (e.g. Antibody-Antogen recognition, Hybridization detection, etc.), after the corresponding biological reactions,

washing with a non-conductive solution (e.g. Methanol [9]) and sometime temperature treatment [3], are performed in order to prepare the sensor for a purely capacitive measurement. It could be beneficial to take the advantage of this sensor's behaviour against conductive solution in order to monitor if the above mentioned rinsing process is performed perfectly and the sensor is ready for capacitive measurement or still some ions exist and consequently further preparations are needed.

VI. CONCLUSION

We described an interface circuit for static capacitive sensors which is used for LoC detections. A low-complexity and high-precision CBCM was employed as CMOS capacitive sensor Lab-on-Chip. Also, a core-CBCM capacitive sensor was implemented in 0.18μm CMOS process for liquid detection in micro-channel. Additionally, we successfully demonstrated the experimental results using standard chemical solutions in order to reveal the viability of the proposed hybrid IC/microfluidic sensor for so many applications such as in-channel analyte monitoring, digital microfluidics, cellular detection through antibody-antigen assays, fully electronic DNA microarray as well as chemical gas sensing and organic solvent detection for environmental monitoring. This simple and low cost interface circuit also offers a good alternative for fully integrated capacitive sensor arrays which are highly required for LoCs. We also discussed and demonstrated further circuitry (under fabrication process) based on this charge based approach in order to embed the sensor system entirely in the same chip.

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Chapter 5

DIRECT-WRITE MICROFLUIDIC PACKAGING

5. 1 Introduction

Following the discussions on the DWFP in chapter 3, this chapter presents a six-step microfluidic packaging procedure for highly integrated LoCs. Based on this procedure, the microfluidic components can be performed on different types of substrates including wire-bonded chip and printed circuit board (PCB) using the conventional digital dispensing system. The advantages of this method in fabricating three dimensional microfluidic components are also described and demonstrated through the experimental results. The contents of this chapter will appear in "IEEE Transactions on Advanced Packaging ". This paper is reproduced in the following pages.

5. 2 A Microfluidic Packaging Technique for Lab-on-Chip Applications

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ABSTRACT

In this paper, we address the often-neglected challenges of microfluidic packaging for biochemical sensors by proposing an efficient direct-write microfluidic packaging procedure. This low-cost procedure is performed through a programmable dispensing system right after a routine electronic packaging process. In order to prove the concept, the experimental results of implemented hybrid system incorporating microelectronics and microfluidics are also presented and discussed.

Index Terms—Microfluidic packaging, CMOS, Integrated capacitive sensor, Lab-on-Chip, Direct-write fabrication process.

I. INTRODUCTION

Laboratory-on-Chips (LoCs) hold immense promise as miniaturized sensors for rapid, automated sensing and measurement of a range of clinical and environmental analytes. Recently, several CMOS-based LoCs have been successfully developed for biological sensing applications such as living cell analysis, bioluminescence detection, pH sensing and organic solvent measurements[1]-[4].

All the aforementioned applications would require efficient microfluidic packaging to protect circuitry from the biological and chemical analytes as well as the external environment. Microfluidic packaging is also critical to direct the fluids towards the sensors for analysis. Ideally, these microfluidic packaging components (e.g., micro-channels, -chambers, -fittings, -valves, - pumps) should be performed through a low

temperature process with a reliable and hermetic bonding. The leakage of analytes (especially of charged molecules as is the case with many bioanalytes) from microfluidic components may increase the parasitic capacitances or resistances and thus affect the circuit characteristics. Conventionally, microfluidic packaging is performed using chemically-inert epoxy to cover the bonding wires, pads or to underfill the flip-chips with an opening for free access of analytes [5].

Since the thrust of current sensor development has been towards developing versatile platform technologies that could be adapted for a range of analytes, much of the current research centers on the incorporation of microchannels through micromaching processes onto the CMOS sensors [6-8]. Less attention has been paid to incorporating microfluidic components after chip fabrication procedures. Among those working with fabricated chips are Chartier et al. who have reported the fabrication of a polymer-based microfluidic structure through hot embossing and integrated to a CMOS based LoC for bioparticle detection and manipulation [9]. In addition, a follow-up paper describes the fabrication of microfluidic networks on the same CMOS-based system using a dry film resist [10]. Standard, mutually-compatible platforms, may allow CMOS-based LoC technologies to transition from a laboratory prototype to a ready-to-use product in the near future. With this in mind, we have already reported on the direct-write microfluidic fabrication process (DWFP) for the creation of microchannels atop a sample CMOS chip [11]. This polymer-based microfluidic fabrication procedure is threefold: sacrificial paste-like ink deposition through a micronozzle, encapsulation of ink filaments with

liquid epoxy, and ink extraction after the hardening of epoxy [12-13]. For this, a three-axis robot along with a dispensing device is used to extrude ink architecture (in one-, two- or three-dimensions) onto pre-determined sites on the substrate (e.g., silicon wafer, microelectronic die or PCB).

Fluid dispensing processes are widely employed in several applications of electronic packaging such as die encapsulation, surface mounting, and flip chip assemblies [14]. DWFP can be considered a new application of the dispensing process which can be performed in a conventional laboratory environment using standard packaging equipment. The microfluidic procedure described in this paper has been performed on a capacitive sensor fabricated in CMOS technology, so as to demonstrate the feasibility and compatibility of this novel procedure for CMOS-based microfluidic applications.

The remainder of the paper is organized as follows. In section II, we elucidate the DWFP for the fluidic packaging of microelectronic chips. Thereafter, the simulation and experimental results are given in section III. In section IV, the main fabrication considerations are briefly discussed, followed by a conclusion in section V.

II. MICROFLUIDIC FABRICATION PROCEDURE

We elaborate the proposed microfluidic packaging procedure in this section. This procedure consists of six steps which are described below and shown in Fig.5.1.

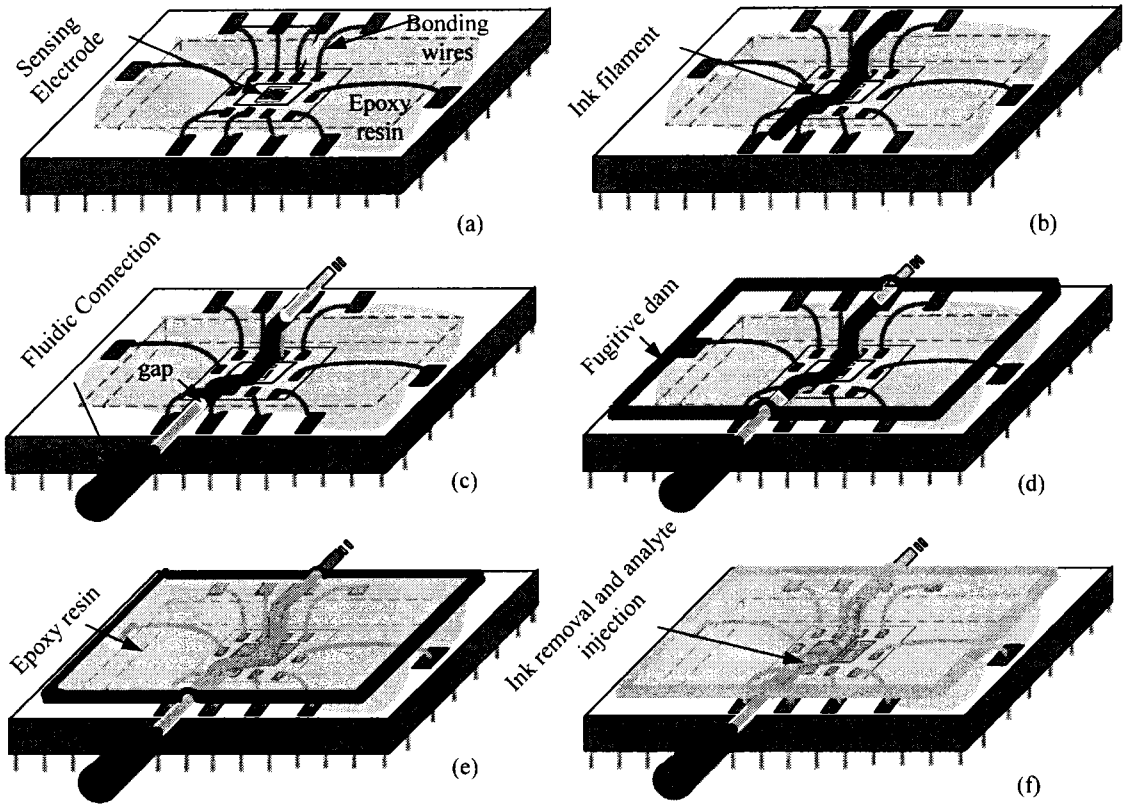


Figure. 5.1. Microfluidic packaging procedure: (a) wire bonding encapsulation, (b) ink deposition, (c) fluidic connection, (d) fugitive dam, (e) fugitive ink encapsulation and (f) ink removal and analyte injection.

A. Encapsulation of bonding pads and wires

Before starting the three-step direct-write microfluidic fabrication process, the conductors should be covered so as to avoid direct contact with fluids in the channels. For this, a partially cured epoxy resin (Epon 828, Shell Chemical) is dispensed (Champion 8200 dispenser, Creative Automation Co.) on the packaged chip in order to encapsulate the bonding wires. Due to surface tension and high viscosity of the semi-cured epoxy, it naturally flows around the bonding wires but stops near the pads (see Fig. 5.2d).

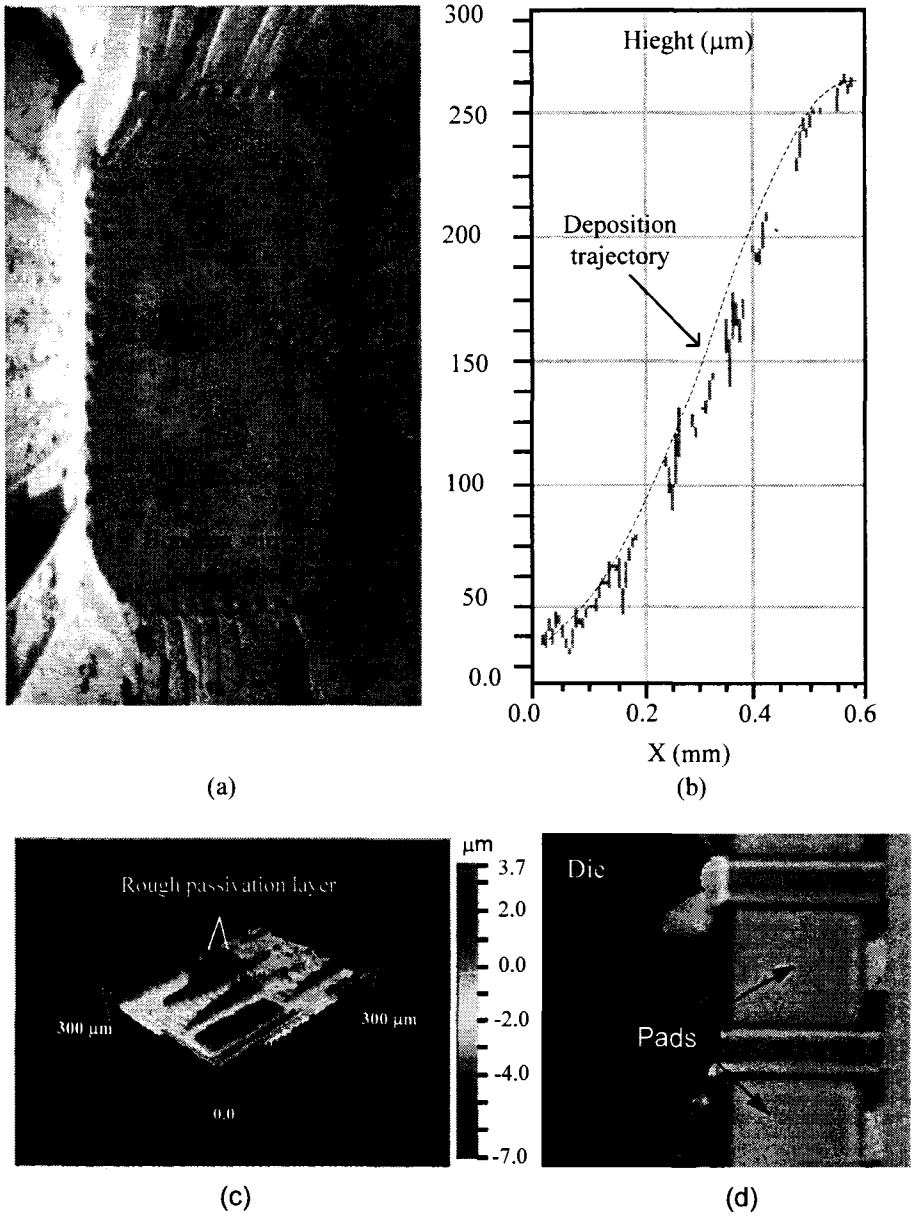


Figure 5.2. Trajectory recognition for ink deposition: (a) top view SEM image of a chip after wire bonding encapsulation, (b) height measurements starting from the mark x on the chip (a), (c) laser profiler image of the chip (in the middle of chip) shown in (a) and laser profiler image of bonding pads which stop the flowing epoxy resin.

Therefore, the loose die remains uncovered which is required for sensing purposes. In Fig. 5.2a, the SEM image of a chip (top view) with encapsulated bonding wires is displayed. This chip was covered with a thin layer of gold for better visualization. It should be mentioned that, this step can be ignored with a particular arrangement of pads with an open space for ink deposition.

The trajectory points (x,y,z) of ink deposition should initially be measured and programmed into the robot-driven dispensing system. This trajectory path should precisely pass over the sensing electrodes. For this, a high precision optical profiler (WYCO, Veeco Inc.) is used to measure the height (z) of the different trajectory points (x,y). The height profile along the desired trajectory is shown in Fig. 5.2b. The envelope of this curve can be used as the z-coordinate of the ink deposition trajectory. It should be mentioned, we have already proposed another manually alignment technique for the same purpose in [11].

B. Ink deposition

A paste-like organic ink (mixture of petroleum jelly and a microcrystalline wax [13]) is extruded (Ultra® 2400, EFD Inc.) through a micronozzle and deposited on the substrate. During the extrusion, a micro-positioning robot (Model I&J 2200, I&J FISNAR Inc.) moves the nozzle across a desired trajectory (part A, section II). This sacrificial ink structure (Fig. 5.1b shows an ink filament) preserves its shape during epoxy encapsulation in section E. The following parameters should be modulated to control this process: the air-pressure (P) applied to extrude the ink through the micronozzle, the

velocity of the moving micronozzle over the trajectory (v), the relative height between the nozzle and substrate (H) and the microcrystalline fraction of the organic ink mixture (M).

C. Fitting connections

Following the ink deposition process, the microscale fluidic fittings (nozzle or tube) are placed and fixed at desired locations close to the deposited ink on the chip using a few drops of hot glue. An extra deposition of fugitive ink from the fitting is necessary to fill the space between the ink filament and fluidic connection and furthermore, to prevent the infiltration of epoxy into the fitting during the encapsulation process (see"gap" in Fig. 5.1c).

D. Fugitive dam

Another ink deposition process is performed in the pre-defined boundary of epoxy encapsulation. This fugitive dam can easily be removed during the ink removal step (F).

E. Ink encapsulation and filling process

In this step, a low viscosity epoxy resin is dispensed on the deposited ink within the encapsulation boundary. Curing of the resin occurs at room temperature, within 24 hours. This epoxy encapsulation process creates a strong and hermetic bond on the uneven surface of loose die (see Fig. 5.2c).

It is obvious, an open-top channel can be performed by using less volume of epoxy. This type of channels is required for post sensing layer deposition which can be capped afterward.

F. Ink removal and analyte injection

The fugitive ink is melted at ~75°C and expelled under light vacuum or air pressure. Thereafter, hot water is injected through the channel to remove the ink remnants. Just after this step, an analyte solution can be directly injected into the fabricated microchannel onto microelectronic chip for sensing purposes.

III. EXPERIMENTAL RESULTS

A. Chip Fabrication and testing result

In order to validate the proposed microfluidic procedure, a capacitive sensor chip has been implemented in 0.18 μm CMOS process and incorporated into a microfluidic channel fabricated through DWFP [4]. A SEM image of the interdigitated sensing electrodes is shown in Fig. 5.3.

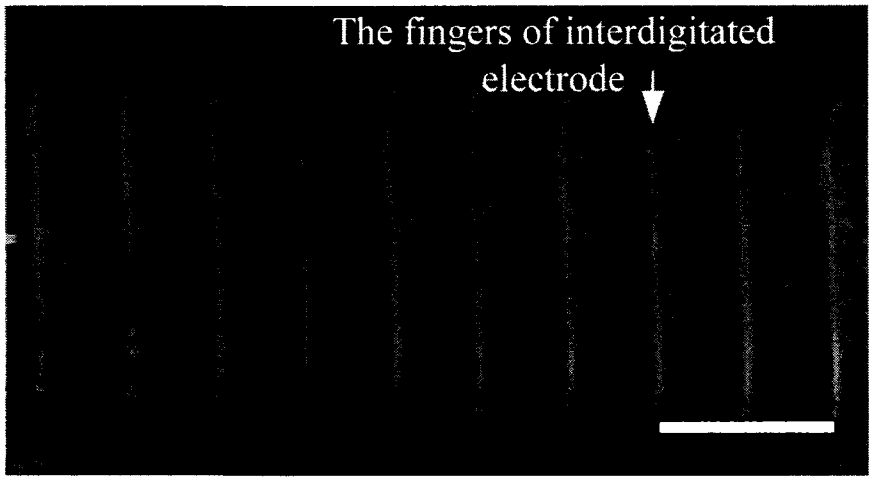


Figure 5.3. SEM image of interdigited electrode realized on CMOS chip from top view of 45° angle (scale bar 10 micron).

The interconnections between the fingers of these electrodes are achieved through an underlying metal layer 5 and the passivation layers between these fingers have been removed. This sensor chip was fabricated by TSMC and wire bonded by MOSIS using the package 40DIP-786. We have successfully reported the chemical testing results using the proposed microfluidic packaging procedure. along with ionically conductive poly (sodium acrylate) gel and an organic solvent [4]

B. CMOS chip microfluidic packaging

In order to deposit a fine and continuous 100-μm ink filament, the variable parameters are adjusted to P=250 kPa, V= 1.5 mm/s, H= 100 μm. M=40 wt%. Following the direct-write microfluidic packaging procedure, a microchannel has been implemented on top of CMOS sensor as shown in Fig. 5.4.

C. Three dimensional microfluidic components

DWFP is a low-temperature, low-cost process which can be used to implement microfluidics with complex and unique geometries. For example, helical microchannel, cylindrical microchamber and conic microchamber can be implemented through DWFP as shown in Figs. 5.5 to 5.7. Fig. 5.5a displays a microscopic image (Dynoscope, Lynex, Vision Engineering) of a helical microchannel filled with a coloured liquid. For this, a filament ink has been deposited on a rotating micronozzle. The encapsulation and ink removal processes are performed as discussed in section II. As shown in Fig. 5.5b, the rotating speed ω and displacement speed v play key role in this process. Helical

microchannels can be used as microscale mixers, centrifuge, fractionation or counter-current chromatography for biochemical sample processing and analyses.

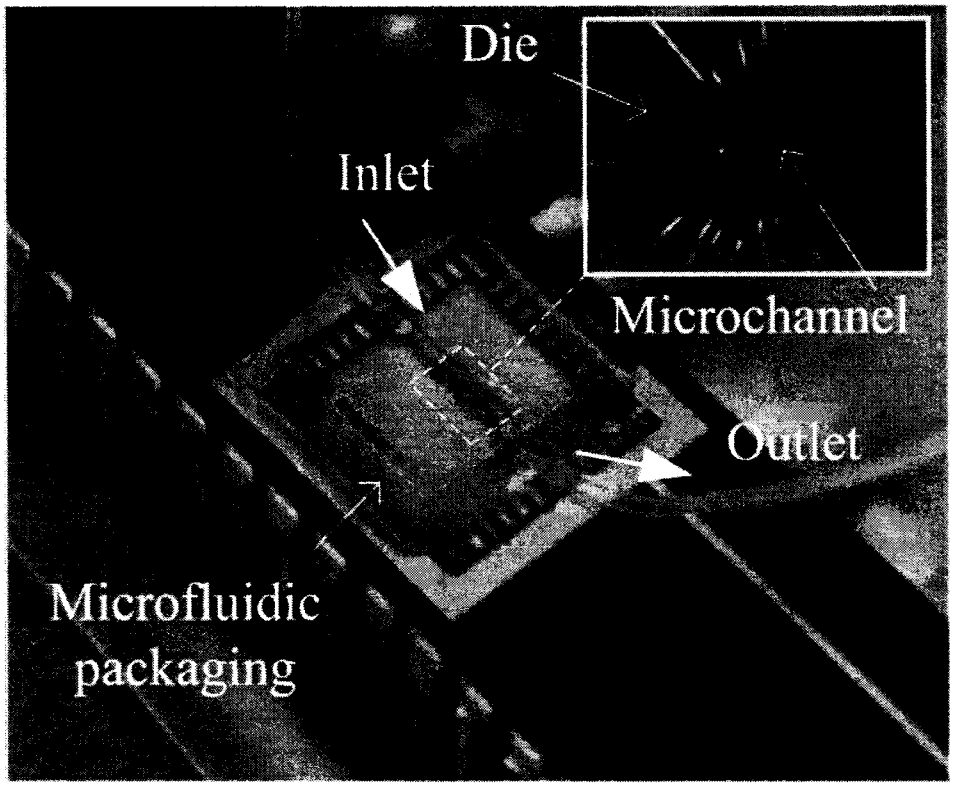
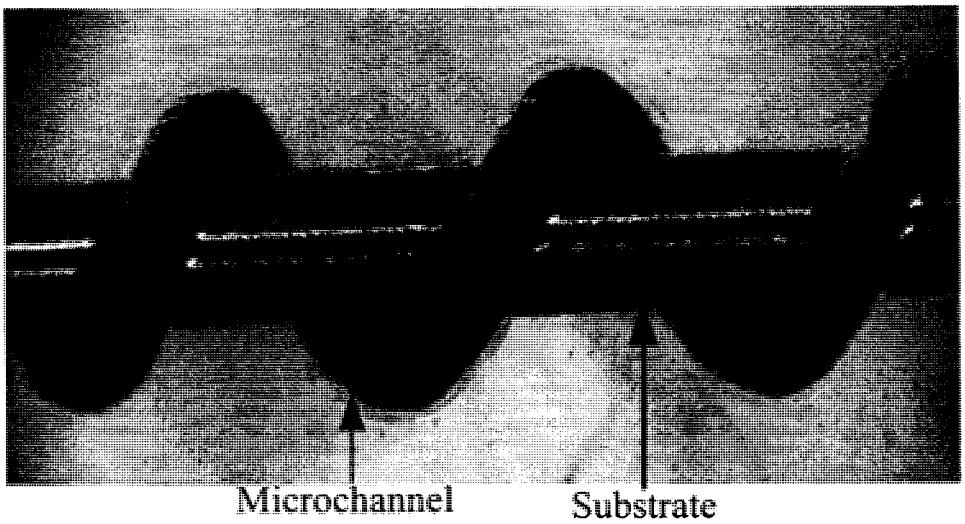
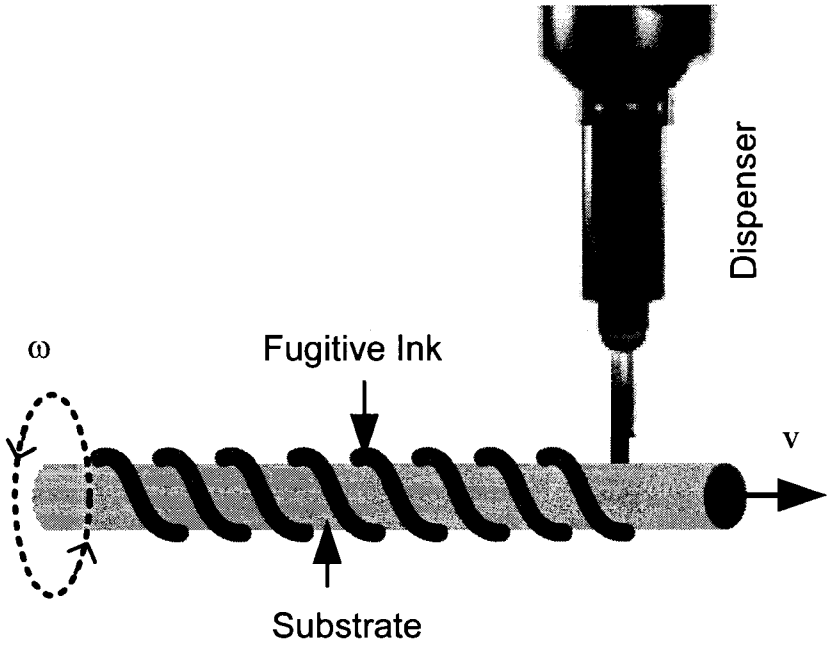


Figure 5.4. Micrograph of hybrid test structure including CMOS chip and microfluidic packaging (This platform is embedded in a shielding box during measurement).

Figures 5.6a and 5.6b show an ink architecture and corresponding cylindrical microfluidic device which is filled with a fluorescent dye. For the implementation of this microfluidics, the robot is programmed to pursue a helical path while the dispensing system extrudes the fugitive ink.

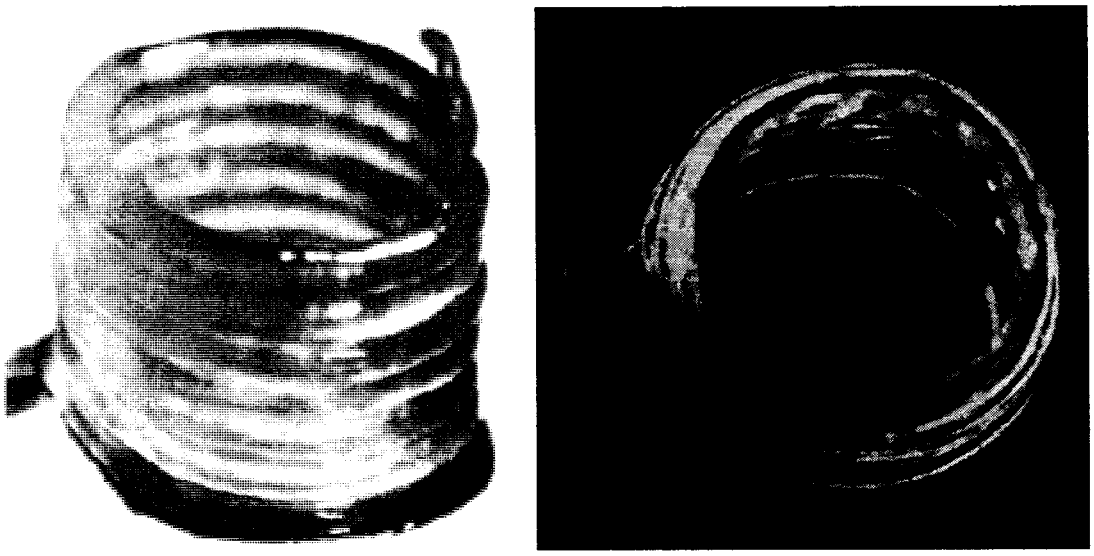


(a)



(b)

Figure 5.5. Helical microchannel embedded in side a clear epoxy: (a) optical microscope image of microchannel filled with a coloured liquid, (b) schematic of deposition set-up (scale bar, 100 μm).



(a) (b)

Figure 5.6. Optical microscope images of (a) cylindrical ink architecture and (b) corresponding microchamber filled with fluorescent dye (outer diameter of cylinder, 2mm).

Also, the optical microscope image of a conic microfluidic chamber is shown in Fig. 5.7a. The illustrations of ink deposition trajectory, stacked layers and the optical microscopic image of the corresponding ink architecture of this conic microfluidic chamber are shown in Figs. 5.7c, 5.7d and 5.7b respectively. In this figure also, the UV microscopic image of implemented microfluidic chamber with the same geometry of Fig. 5.7d but less volume of epoxy is shown in Fig. 5.7e. In another effort, filled-in cylindrical ink architecture is implemented and its optical microscopic image is shown in Fig. 5.7f. In addition to the above mentioned advantages, this technique can be used for water cooling of chip and printed circuit board. Fig. 5.8 shows a microchannel fabricated on a

printed circuit board. Several microchannels can be performed on PCB or chip to play the role of a cooling layer.

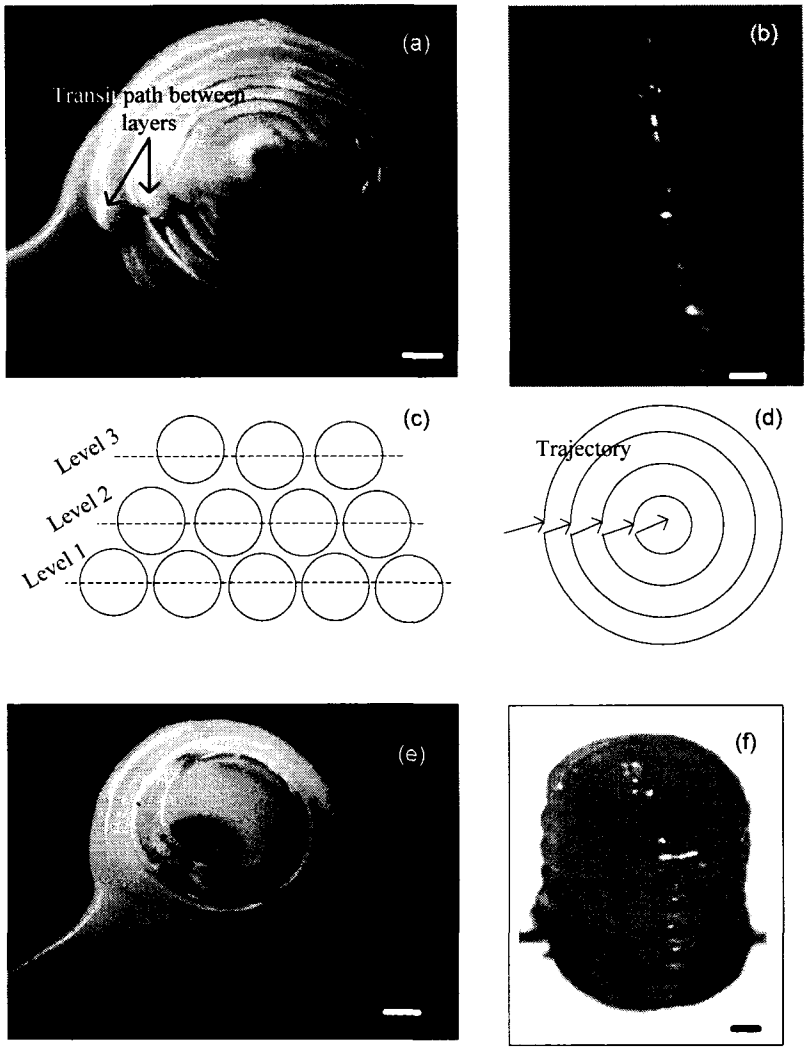


Figure 5.7. Conic and cylindrical microreservoir: (a) conic microfluidic chamber, (b) conic ink architecture, (c) stacked layers (b) trajectory of ink deposition, (e) conic microfluidic chamber with less epoxy and (d) filled in cylindrical ink architecture (scale bare 200 micron).

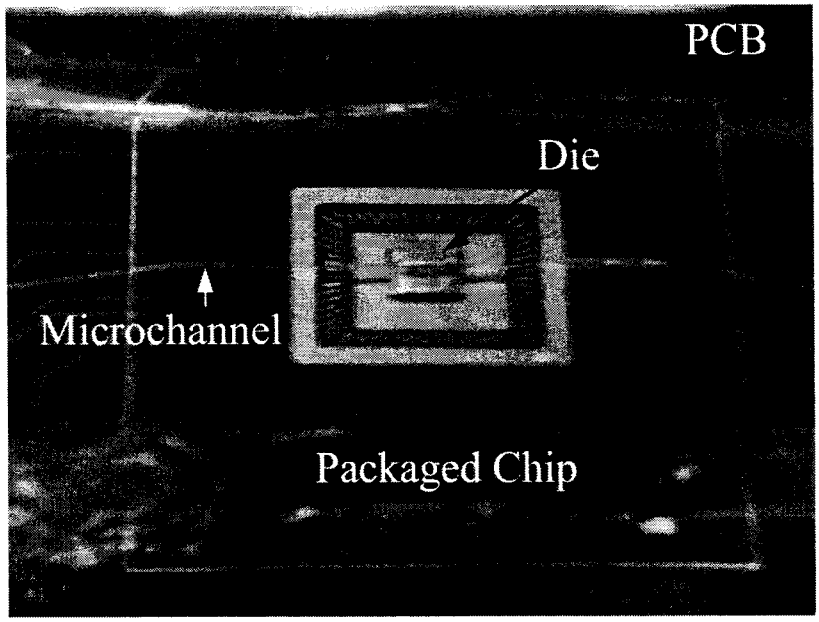
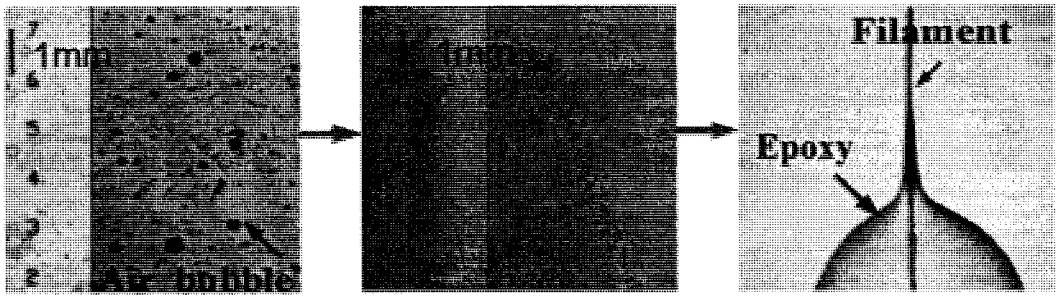


Figure 5.8. Optical microscope images of a microchannel implemented through the proposed technique in an transparent epoxy on a package and printed circuit board and filled with a coloured liquid for better visualization.

IV. DISCUSSION

DWFP can be easily adapted to conventional dispensing process for fluidic packaging of LoC integrated sensors. To date, the dispensing processes of several fluids are studied [24] but the modeling of fugitive ink dispensing process is still in its infancy. With appropriate rheological models of the ink, liquid epoxy and pre-gel solutions, the complex microfluidic components could be optimized and implemented through an automated and programmable DWFP. The minimum radius of the channels fabricated by DWFP is dependant on the inner diameter of the micronozzle. The size of commercially

available metalic micronozzles, with a metal tip (EFD Inc.), is around 100 μm. The fabrication of nozzles with different shapes and cross-sections for dispensing process has already been reported [25].



(a) (b) (c)

Figure. 5.9. Epoxy preparation and deposition (a) before degassing, (b) after degassing and (c) during deposition.

Of course, by using the nozzles with different geometries and cross sections, it could be possible to implement different microchannels. This issue can be considered to connect the large fluidic connections to the channel. Also, the implementation of smaller channel in proximity of sensing site offers the advantage of low sample consumption and high sensitivity. In addition to above mentioned issues, the degassing of prepared epoxy is critical for high-precision applications. Fig. 5.9 shows the role of the degassing which is performed in a vacuum chamber.

V. CONCLUSION

We described a novel microfluidic packaging procedure for LoC applications based on the ink and epoxy dispensing processes. This low temperature, flexible direct-write

fabrication process can be a good alternative for the fabrication fluidic packaging and other required microfluidic components (e.g., microchamber) onto microelectronic sensors. The experimental results of the proposed microfluidic packaging procedure on already implemented CMOS capacitive sensor are demonstrated with a polyelectrolyte hydrogel and dichloromethane in order to proof of concept. Furthermore, several advantages of DWFP for fabrication of three dimensional microfluidic structures on different substrates such as PCB were demonstrated and discussed.

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Chapter 6

CONCLUSION AND FUTHER WORK

Herein, we conclude this thesis by a review of our contributions along with offering some suggestions for future works.

A. Contributions

1. Design and implementation of three different capacitive sensors with different level of complexity in CMOS technology as broken into the following points:
   - Proposing a new core-CBCM design methodology for capacitive sensors
   - Proposing a simple current-based calibration procedure for cancelling the output offset voltage.
   - Proposing an array of capacitive sensors using CBCM structure as a building block.
   - Proposing a dedicated sigma delta analog to digital converter adopting with the main core-CBCM interface circuit and showing the post layout simulation results.
   - Implementing the sensor chips in 0.18 CMOS process and successfully testing through organic solvents.
2. Proposing a direct-write microfluidic procedure for CMOS based LoCs as detailed as follows:

- Construction of microfluidic structure on packaged chip in a six-step procedure.
- Fabrication of three dimensional structures suitable for LoC applications.

B. Recommendation for the further developments

It is obvious, for a new approach like CMOS based LoC there are so many important considerations from different aspects of this approach. Herein, we mention some of these issues based on our studies and experiments on this thesis.

- Design a generic and fully integrated capacitive sensor dedicated for LoC application: Nevertheless, for each LoC application, a particular bio-functionalized sensing layer is required; the interface circuits to detect the capacitance variation can be implemented through similar design strategy.
- Investigation of different CMOS compatible sensing layers for different applications: It is the main requirement of any highly sensitive sensor to be incorporated with a sensing layer functionalized chemically or biologically right after the fabrication of CMOS chip through standard procedures.
- Increasing the precision of direct-write microfluidic fabrication process: we believe the following issues should be taken into account for the future works:

- Design and fabrication of the micronozzle with smaller inner diameter and different cross-section shape rather than available commercial nozzles which have been used in this project.
- Modeling of the ink extrusion as the function of temperature, nozzle's dimensions, the speed of nozzle carried by 3D robot, the height between substrate and nozzle and the percentage of microcrystalline in fugitive ink is very important need for reproducibility and batch production purposes through DWFP.

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