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ÉCOLE POLYTECHNIQUE DE MONTRÉAL

EVALUATION OF DELAY MISMATCH DUE TO PROCESS VARIATIONS IN CMOS INTEGRATED CIRCUITS

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Ce mémoire intitulé:

EVALUATION OF DELAY MISMATCH DUE TO PROCESS VARIATIONS IN CMOS INTEGRATED CIRCUITS

Présenté par: Bo Zhou

en vue de l'obtention du diplôme de : Maîtrise ès sciences appliquées

a été dûment accepté par le jury d'examen constitué de:

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M. KHOUAS Abdelhakim, Ph.D., directeur de recherche

M. SAWAN Mohamad, Ph.D., membre

DEDICATE

I would like to dedicate this master thesis to my husband and my daughter.

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Special thanks to my family, for their encouragement and support over the past several years during my master research in Polytechnique.

RÉSUMÉ

Les fluctuations des paramètres des composants dues aux variations du procédé de fabrication (VPF) posent certains problèmes lors de la conception de circuits intégrés CMOS, particulièrement en ce qui concerne les technologies submicroniques (90 et 65nm). Dans le domaine numérique, les effets des variations à l'intérieur d'un même dé sur les performances du circuit sont devenus un défi important lors de la conception. D'ailleurs, ces dernières sont beaucoup plus complexes et difficilement mesurables que les effets des variations d'un dé à un autre. À ce jour, il n'existe aucun modèle reconnu pour les caractériser, c'est pourquoi beaucoup de travaux restent à faire dans ce domaine.

Ce mémoire explore des méthodes de caractérisation des effets des VPF sur les délais de propagation en évaluant les délais des cellules à délai et le délai de mésappariement à l'aide d'un oscillateur en anneau (OA). Un circuit de mesure est par la suite présenté, incluant la conception, les résultats de simulation et l'implémentation.

Dans ce mémoire, le DM entre les différentes cellules à délai est tout d'abord introduit et certains circuits d'application affectés par ces disparités sont présentés. Ensuite, certains concepts reliés aux VPF sont présentés et leur impact théorique sur les performances du circuit est étudié. Ceux-ci nous amèneront à faire une revue des méthodes existantes d'analyse et de caractérisation des VPF avec des circuits de mesure, afin de faire ressortir leurs défauts. Une architecture d'un circuit de mesure basée sur un OA modifié est donc proposée. Cette nouvelle structure de mesure est utilisée pour quantifier le délai de propagation ainsi que le délai de mésappariement dans un OA en mesurant uniquement la période (fréquence) de chaque OA avec un équipement de test standard.

Les considérations de conception et d'implémentation reliées à la création d'une architecture symétrique ainsi que les effets des interconnexions dans le dessin de masque sont analysés en

détails dans ce mémoire. Les résultats de simulation au niveau circuit avant et après placement-routage ont montré la faisabilité et la précision de notre méthode. Le circuit proposé a été implémenté avec la technologie CMOS 0.18um et peut être facilement réutilisé pour les technologies submicroniques. La nouvelle technique proposée pour la caractérisation des effets des VPF sur délais permettra donc d'aider le concepteur à résoudre les problèmes de gestion de la variabilité des processus de fabrication dans la création de nouveau design.

ABSTRACT

The consideration of device fluctuation is an important theme in designing CMOS integrated circuits, particularly on the deep submicron technology (90 and 65 nm). In digital circuit, effect of intra-die variations on performances of circuit especially becomes important consideration in design. However, since intra-die variation is much more complex and difficult to measure than inter-die variations, until now, there is no acknowledged model to describe it comprehensively, although many works engage in this topic.

This master thesis investigates method of characterizing the effect of die-to-die and intra-die variations on propagation delays by evaluating single cell delay and delay mismatch in Ring Oscillator (RO). A test circuit is presented including its design, simulation and implementation. Single cell delay mismatch will first be introduced and typical application circuits suffering from this delay mismatch will be discussed as well. And then, the master thesis will study some knowledge relating to process variations and analyze theoretically this variation impact on performances of integrated circuits. Next, some previous works will be reviewed about process variations analysis and characterization methods with test circuits, and their possible drawbacks will be reported. After that, a proposed test architecture, which is based on modified RO, is presented. This novel test structure can be used to evaluate propagation delay and delay mismatch in RO by only measuring period (frequency) of each RO with conventional frequency measurement equipment.

The design considerations and implementation along with creating symmetrical architecture and interconnect effect in the layout are also investigated in detail in this master thesis. Both pre-layout and post-layout simulation results indicate the accuracy and the feasibility of our method. The test chip was implemented with TSMC 0.18um CMOS technology; it's easily reused for submicron technologies. The proposed technique to characterize the effect of process variations

on delays can help designers to solve the problems caused by process variability in their new circuit design.

CONDENSÉ EN FRANÇAIS

Les nouvelles technologies de fabrication de circuits intégrés permettent d'intégrer un nombre de plus en plus élevé de transistors, ce qui permet d'avoir des circuits de plus en plus performants et à moindre coût. Ces nouvelles technologies ont l'avantage d'augmenter les fréquences d'utilisation, mais les effets des variations du procédé de fabrication (VPF) sur les délais ne diminuent pas dans les mêmes proportions, ce qui fait que les performances des circuits deviennent très sensibles aux fluctuations de l'environnement d'utilisation et du procédé de fabrication. Ces dernière années, et avec la diminution croissante des dimensions des transistors, ces variations deviennent des causes de plus en plus fréquentes de non fonctionnement des circuits. Il est donc très important de bien caractériser ces variations afin d'en tenir compte dans la conception de circuits intégrés, en particulier pour les technologies submicroniques (90 et 65 nm). Il existe deux types de VPF : les variations à l'intérieur d'un même dé (VIMD) et les variations d'un dé à un autre (VDA). Dans le domaine numérique, la caractérisation des effets des VPF sur les performances d'un circuit est devenue un défi important. En particulier, la caractérisation des effets des VIMD qui est beaucoup plus complexe et difficile à réaliser que pour les VDA. À ce jour, il n'existe aucun modèle reconnu pour la caractérisation de ces variations, et beaucoup de travaux restent à faire dans ce domaine. Un exemple des conséquences des VIMD sur les circuits intégrés est le délai de mésappariement (DM) qui représente la différence moyenne des délais des cellules dans une même chaîne à délai.

Ce travail de recherche a pour objectif la conception et la fabrication d'un circuit permettant de mesurer les effets des VPF sur les délais de propagation des cellules utilisées dans les chaînes à délai. Un nouveau circuit de caractérisation et de mesure du DM dans une chaîne à délai a été proposé. Ce circuit est réalisé à l'aide d'un oscillateur en anneau (OA) configurable qui permet de

réaliser plusieurs boucles d'oscillations qui ne différent que d'une seule cellule à délai. Les résultats de simulation obtenus démontrent la faisabilité de cette technique.

Au début de ce mémoire, nous présenterons en détail le DM ainsi que quelques applications typiques qui sont sensibles au DM. Nous expliquerons ensuite les principes de base théoriques de l'analyse des effets des VPF sur les performances des circuits. Une étude comparative des travaux antérieurs rapportés dans la littérature est présentée. Par la suite, le nouveau circuit de caractérisation et de mesure des délais de propagation du DM est présenté. Les considérations de conception et d'implémentation reliées à la création d'une architecture symétrique et au dessin de masque sont aussi étudiées en détails dans ce mémoire. Deux architectures de test basées sur un OA modifié sont suggérées; celle présentant une structure symétrique avec un faible facteur d'erreur a été conservée et implémentée. Pour une analyse plus complète des effets des VIMD sur les délais de propagation et le DM, des résultats de simulation de notre circuit après placement-routage et avec la technologie CMOS 0.18um sont présentés. En dernier, la stratégie de test pour le prototype ASIC du circuit de mesure, ainsi que le diagnostic et l'analyse de la puce fabriquée sont expliquées. La conclusion et les travaux futurs sont discutés.

Problématique

Dans plusieurs applications numériques tels que les convertisseurs de temps à numérique et les circuits de synthèse d'horloge, la précision de ces circuits dépend du délai de propagation de chaque élément de la chaîne de traitement. Le DM peut causer des erreurs qui affectent la résolution des convertisseurs de temps à numériques et conduit à l'apparition d'artefacts dans le spectre fréquentiel des circuits de synthèse de fréquence. La majorité des convertisseurs temps à numérique a période d'horloge de référence sont conçus avec une chaîne à délai composée d'éléments logiques. Avec ces types de circuits, un intervalle de temps est mesuré avec une

résolution qui dépend de la différence des délais de propagation entre deux éléments logiques. L'exactitude de la mesure dépend donc fortement de l'exactitude du délai de propagation dans les éléments logiques utilisés. Ainsi, dans ces cas-ci, une condition cruciale de la conception est de pouvoir caractériser avec une grande précision les délais de propagation des éléments logiques en tenant compte des variations des délais dues aux VPF.

Dans les circuits de synthèse d'horloge, comme les circuits partielle-N, un OA est habituellement employé pour produire le signal d'horloge désiré. Cependant, le DM entre les cellules causé par les VPF et les différences entre les interconnexions cause l'incertitude de synchronisation de l'horloge synthétisée, menant au problème du "jitter". Par conséquent la caractérisation avec précision des délais des cellules à délai et du DM dans une même chaîne de délai est très importante.

Le DM d'un circuit est principalement causé par le mésappariement des structures dû aux VPF lors de la fabrication du circuit. Afin d'atténuer ces variations qui causent des erreurs dans le signal de sortie, le DM de chaque cellule de la chaîne de traitement du circuit doit être pris compte. Le concepteur doit donc estimer l'influence des DM et proposer des circuits robustes dont la sortie est moins sensible aux VPF.

Revue de littérature

Dans les premiers travaux pour caractériser le DM dû aux VPF, on a utilisé des structures de test avec des OA pour faire l'analyse statistique de la moyenne des délais des cellules [13] [25] Ces solutions utilisent un nombre assez élevé d'OA sur la puce de test et la caractérisation se fait par la mesure de la fréquence des OA. Bien que ces méthodes soient efficaces pour caractériser la variabilité d'un lot à un autre, la période mesurée de l'OA est basée sur le délai moyen des cellules composant la chaîne d'un OA et ne tient pas compte des variations du délai propre à

chaque cellule. De ce fait, cette méthode mesure les effets des VDA sur le DM et il n'y a aucune estimation de l'impact des VIMD sur les performances du système.

Une autre approche pour trouver le DM a été rapportée dans [12] [16] [19]. La méthode, désignée par test de la densité du code (TDC), est basée sur des mesures statistiques. En utilisant le TDC dans le but de réaliser une précision élevée, un nombre élevé d'événements est à générer, ce qui implique un nombre important de compteurs sur la puce et donc une surface de silicium plus grande. Une structure de test basée sur la mesure directe du délai la différence dans la même cellule a été rapportée dans [2]. La structure proposée permet de mesurer de légère différence de délai dans chacune des cellules de délai (Figure 3.3). Bien que ces structures permettent de mesurer la différence entre deux délais de propagation d'une même cellule, elles ne peuvent mesurer que les effets des VIMD.

Méthodes de mesure du délai d'une cellule

Au cours des dernières années, beaucoup de recherche ont été menées sur la mesure du délai dans le but de caractériser les VPF que ce soit sur la puce elle même ou entre plusieurs puces. Les chaînes à délai et les OA sont le plus souvent utilisés, Les chaines à délai sont composées d'une chaîne d'une même cellule mise en cascade. Chaque cellule a le même délai de propagation et est utilisée pour augmenter le délai de propagation de la chaîne. L'OA est composé d'un nombre pair de cellules identiques ayant un délai donné. Il n'a pas besoin d'une source d'excitation à son entrée et permet de générer un signal périodique dont la période est deux fois la somme des délais des cellules composant l'OA. Parmi les avantages des chaines à délai et des OA, on peut citer le fait qu'ils sont facilement implémentables sur la puce et sensibles aux VPF particulièrement aux variations de la longueur de la grille des transistors. Des mesures montrent une sensibilité élevée entre la variation de la longueur de la grille et le délai de propagation [24]. La variation de la

géométrie de la grille est la principale cause de la dégradation de la vitesse des circuits. De plus les OA permettent de générer le délai de propagation désiré sans aucun signal d'entrée (ce qui est idéal pour notre application) et sont utilisés pour générer le signal d'horloge sur la puce.

Circuit de mesure proposé

Une caractérisation complète des effets des variations spatiales et des mésappariements de géométries sur les circuits fabriqués exigerait la capacité de mesurer le délai de propagation au travers de chaque cellule avec la résolution de temps de l'ordre du picoseconde. Les portes logiques de taille minimum en technologie CMOS 0.18µm ont des délais de propagation de l'ordre de 50 picosecondes. Il n'est donc pas possible de mesurer ce délai directement à l'aide d'instruments de mesure conventionnels. Notre but est de concevoir un circuit basé sur un OA qui nous permettra de mesurer les délais de propagation de façon indirect. L'idée principale pour l'OA modifié est d'utiliser plusieurs oscillateurs qui sont couplés. Il est possible de mesurer la période des différents OA, et ensuite en se basant sur les relations qu'on a entre les différents OA, on pourra déduire le délai de propagation pour chaque cellule à délai

Tout d'abord, une structure de mesure simple a été conçue. En utilisant un réseau de commutateurs il est possible d'ajouter des éléments de délais un par un (Figure 3.4). Chaque oscillateur a donc une cellule de délai en plus que l'oscillateur précédent. En mesurant la période de chaque oscillateur (T_1, T_2, T_n...) et en faisant la différence entre les périodes des oscillateurs adjacents, on obtient le délai de la cellule ajoutée :

$$D_n = \frac{1}{2}(T_n - T_{n-1})$$

Malheureusement, les résultats de simulation après placement routage ont montré que cette structure n'est pas symétrique. Cela signifie que les cellules n'ont pas les mêmes charges

capacitives et résistives. D'ailleurs, la dernière cellule de chaque OA est reliée à un nombre différent de cellules à délai, c'est.-à-dire dans le $n^{ième}$ (n = 1 à N) oscillateur (Figure 3.7), la dernière cellule relie $(N-n)^{ième}$ autres cellules. Ces deux facteurs font que les oscillateurs sont exposés à des capacités différentes, ce qui engendre des différences dans les délais de propagation même dans la situation idéale (sans VPF). Par conséquent, les délais observés représentent non seulement la disparité d'une cellule à une autre due aux VPF mais incluent également d'autres facteurs propres à la structure du circuit.

Basé sur la structure de test simple présentée, nous avons proposé un circuit de mesure améliorée. L'architecture proposée est une structure re-configurable comportant une série de M oscillateurs de N cellules à délai. Afin de créer une certaine dépendance entre les oscillateurs, des portes de transmission (PT) sont utilisés comme interrupteurs pour choisir les cellules de délai à utiliser dans l'oscillateur sélectionné. Le schéma du circuit de mesure proposé est montré à la figure.3.8. Nous appelons cette architecture la structure de mesure avec oscillateur modifiée. Pour sélectionner un oscillateur, il est possible d'utiliser les interrupteurs de commande SW. Un autre groupe de portes de transmission dénotées par S est utilisé pour choisir les cellules à utiliser. Le premier oscillateur est composé des N premières cellules, N étant une valeur entière positive et impaire. Ceci est accompli en reliant les interrupteurs S_1, S_2, ... S_{N-1}et SW_1 et en gardant les autres interrupteurs ouverts. De la même façon, un deuxième oscillateur peut être configuré en enlevant la première cellule de délai de l'oscillateur courant et en connectant la $(N+1)^{ème}$ cellule à l'autre extrémité de l'oscillateur. Le processus de reconfiguration peut continuer jusqu'à ce que le dernier oscillateur ait la $(M)^{ème}$ cellule de délai comme premier élément et $(N-1)^{ème}$ cellule comme dernier élément. Par conséquent, chaque oscillateur est composé de seulement N cellules, choisies pour former un OA. Dans la structure simple mentionnée ci-dessus, chaque oscillateur a différents éléments de délai, tandis que dans cette structure améliorée, tous les oscillateurs sont

constitués d'un même nombre d'éléments. C'est simplement les cellules qui les composent qui sont différentes. Notre technique de mesure du délai d'une cellule tire profit de la différence entre ces cellules.

Calcul du délai d'une cellule simple à partir de la période d'un OA

Pour déterminer le délai d'une cellule simple, on se base sur la relation de la période d'un OA qui est donnée par:

$$P_{RO} = 2\sum_{i=1}^{N} D_i$$

P_{RO} est la période d'un OA, D_i est le délai d'un élément constituant l'OA et N est le nombre de cellules de délai dans l'OA.

On suppose que la structure de mesure proposée contient un nombre M d'OA et que chaque OA est constitué de N cellules à délai. Suivant cette formule, la période de chaque OA est déterminée par la somme des délais des cellules composant l'OA. Par exemple, la période du premier OA est exprimée par la relation:

$$P_1 = 2\sum_{i=1}^{N} D_i$$

La période du second OA est:

$$P_2 = 2\sum_{i=2}^{N+1} D_i$$

Et ainsi de suite, jusqu'au dernier, le $M^{ème}$ OA, qui est constitué de la dernière cellule (M) plus les (N-1) premières cellules. La période de ce dernier OA est donnée par :

$$P_M = 2(D_M + \sum_{i=1}^{N-1} D_i)$$

Le délai de chaque cellule et en conséquence le DM peut être déduit en combinant les équations des périodes des M OA. La valeur moyenne et la déviation standard sont utilisées pour caractériser les fluctuations des délais d'une cellule à une autre et le DM.

$$\mu = \frac{1}{M}\sum_{i=1}^{M} D_i$$

$$\sigma = \sqrt{\frac{1}{M}\sum_{i=1}^{M}(D_i - \mu)^2}$$

Un autre paramètre, appelé coefficient de variation (CV), est utilisé pour caractériser les effets de VPF sur les délais. Ce paramètre sans unité, exprimé en pourcentage, représente la déviation relative sur la valeur moyenne. Il est utilisé pour comparer les DM entre différents circuits ayant des délais différents.

$$CV = \frac{\sigma}{\mu}100\%$$

Dans cette structure, il est très important de vérifier une certaine relation entre le nombre de cellules de délai dans chaque OA et le nombre d'OA dans cette structure. En supposant que chaque OA a N cellules et que le nombre total d'OA dans cette structure est M, alors, il faut que la différence entre M et N soit un nombre impair, et inférieur à (N+1). Autrement, si la différence est un nombre pair, on n'obtient aucun résultat, et si la différence est plus grande que (N+1), on ne pourra mesurer que le délai de certaines cellules, et donc le DM obtenu sera partiel.

Considérations des effets du dessin de masque

Dans le circuit proposé, nous utilisons deux groupes de portes de transmission, ce qui engendre un grand nombre d'interconnections inégales dans le dessin de masque, et en conséquence la différence des longueurs d'interconnections (DLI) devient une source importante du délai de mésappariement. Plusieurs topologies de dessin de masque ont été proposées afin d'analyser les

effets des DLI sur le DM (Figure 4.7, Figure 4.9 et Figure 4.11). Les résultats de simulation ont montré que la topologie II engendre un DM plus petit que les deux autres topologies. Nous avons donc choisi cette topologie pour implémenter le circuit de mesure et pour simuler les effets des dimensions des transistors et du nombre de cellules dans l'OA sur le DM.

Résultats

Nous avons comparés le DM pour l'OA modifié proposé à l'OA normal (sans PT) avec les mêmes déviations de la taille des transistors utilisés. Les résultats sont présentés dans les tableaux 4.1 et 4.2 qui montrent que les rapports de CV du DM dans le circuit proposé à celui dans l'OA normal sont presque constants, indépendamment des tailles des transistors et de la valeur des déviations. Le DM mesuré avec la structure proposée représente le DM dans l'OA normal, et la structure proposée peut donc être utilisée pour caractériser les effets des VIMD dans un OA conventionnel.

Les simulations au niveau circuit après placement-routage ont été faites pour différentes topologies du dessin de masque. Ensuite, nous avons choisis la topologie présentant le plus faible DM pour étudier les délais des cellules et le DM dans des architectures avec différentes tailles de transistor et différents nombres de cellules. Tous les résultats obtenus sont montrés dans les tableaux 4.5, 4.6 et 4.7. En augmentant la taille des transistors, on augmente les délais des cellules et le DM. Cependant, on remarque que l'augmentation du DM est moins importante que l'augmentation des délais des cellules. Par conséquent, le coefficient de variation du DM et en conséquence les effets des VPF diminueraient avec l'augmentation de la taille des transistors. Fondamentalement, avec l'augmentation du nombre des cellules utilisés, le délai des cellules augmenterait en raison de l'augmentation des longueurs des interconnexions, mais, le CV du DM n'augmente pas beaucoup, particulièrement dans le cas de petites VPF, car c'est l'effet du dessin

de masque qui est dominant. Parfois, l'effet des interconnexions peut annuler l'effet des VPF (Tableau 4.7).

Dans le dessin de masque, l'utilisation dans des secteurs de haute densité d'interconnexion, de différentes couches de métal peut réduire de façon significative les capacités parasites d'interconnexion et en conséquence les délais des cellules et les effets des interconnexions sur les délais (Tableau 4.8).

Conclusion

Nous avons proposé un nouveau circuit de caractérisation des DM dues aux VPF et aux DLI dans le dessin de masque. L'idée principale de notre circuit de mesure est de concevoir un OA configurable qui permet de réaliser plusieurs OA qui ne différent que de deux cellules à délai. La mesure des fréquences d'oscillation des différents OA nous permet d'extraire les délais exacts de chaque cellule et le DM entre les différentes cellules à délai. L'utilisation d'un OA dans un circuit de mesure du DM n'est pas une idée nouvelle, mais contrairement aux circuits existants qui ne mesurent que les effets des VDA sur les délais de propagation des cellules, l'avantage principal de notre circuit est qu'il permet de mesurer les effets des VDA, des VIMD, et des DLI sur les délais des cellules. Malheureusement, le prototype fabriqué n'a pas fonctionné, mais les résultats de simulation au niveau circuit avant et après placement-routage ont montré la faisabilité et l'exactitude de notre méthode. La validation du circuit a été réalisée en utilisant la technologie CMOS 0.18um, mais le circuit proposé peut facilement être réutilisé pour les technologies submicroniques (90 et 65 nm) pour lesquelles la gestion de la variabilité des processus de fabrication est un problème critique dont il faut tenir compte. En effet, pour ces technologies submicroniques les VPF peuvent avoir un impact important sur les performances et le rendement du circuit fabriqué

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LISTE DES ACRONYMES

CV	Coefficient de Variation
DLI	Longueurs d'interconnections
DM	Délai de Mésappariement
OA	Oscillateur en Anneau
PT	Porte de Transmission
VDA	Variations d'un Dé à un Autre
VIMD	Variations à l'Intérieur d'un Même Dé
VPF	Variations du Procédé de Fabrication

ABREVIATIONS

ADC	Analog-to-Digital Converter
CMP	Chemical Mechanical Polishing
CD	Critical Dimension
CMOS	Complementary Metal Oxide Semiconductor
CQFP	Ceramic Quad Flatpack
CV	Coefficient Variation
DDFS	Direct Digital Frequency Synthesis
DDPS	Direct Digital Period Synthesis
DFF	D-Flip-Flop
DFT	Design for Test
DLL	Delay Locked Loop
IC	Integrated Circuit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-Type Metal Oxide Semiconductor
PCB	Printed Circuit Board
PLL	Phase Locked Loop
PMOS	P-Type Metal Oxide Semiconductor
PVT	Power Supply Voltage and Temperature
RO	Ring Oscillator
TDC	Time to Digital Converter
TG	Transmission Gate

VCDL	Voltage Control Delay Line
VDL	Vernier Delay Line
WYSIWYG	What You See Is What You Get

CHAPTER 1

INTRODUCTION

This chapter introduces the motivation and goal of test chip methodology. It presents the importance of characterizing process variations and the effective method to evaluate delay mismatch due to process variations by performing measurement for a test circuit. Meanwhile the organization of this master thesis is also outlined.

1.1 Motivation

CMOS (Complementary Metal Oxide Semiconductor) technologies stepping into micro and nano-scale range makes it possible to create low power, high speed, and more reliable microelectronic-based products. However for designers and researchers, this technologies advance means also great challenges, in design, fabrication and testing.

For designer, downscaling in the feature size not only makes device itself complex, it also makes process variations unnegligible. CMOS processes and variants have come to dominate, so that as of 2006 the vast majority of integrated circuit manufacturing by dollar volume is on CMOS processes" [7].

The process variations can be divided into two categories: inter-die (die-to-die) and intra-die (within-die) variations. Inter-die variations indicate variability between dies, wafers and lots, which affect equally on every device on a chip. Conversely, intra-die variations produce a non-uniformity of electrical characteristics across the chip [11]. We also call this non-uniformity within the chip "mismatch".

At present, the performances of both digital and analog CMOS integrated circuits depend heavily upon the foundry ability to fabricate transistors with matched electrical behavior. Random variations inherent to the fabrication process steps result in intra-die variations between transistors designed to be nominally identical. This impedes the ability of the designer to achieve exact timing delay, voltage or current. The mismatch resulting from process variations is a limiting factor for both analog and digital ICs. For example, mismatch causes threshold voltage variations between nominally identical CMOS transistors. According to Pelgrom's model [26], we have:

$$\Delta V_T = \frac{K}{\sqrt{WL}} \tag{1.1}$$

where W and L are the width and length of the MOS transistor channel area, and K is a process constant supplied by the manufacturer in the process data sheets. It is evident from equation that the threshold variation will increase as transistor area decreases.

Device parameter mismatch is inversely proportional to the area of the transistor and therefore becomes increasingly important as the dimensions of transistors are reduced. A circuit design that is sensitive to mismatch must therefore uses larger devices than the minimum size allowed by the process rules (the master thesis will verify the rule in Chapter 3 through simulation results). In addition, circuit designers should account for die-level random process variations in simulations to ensure sufficient design margin to achieve high yields. Mismatch measurement on the circuit die itself would be useful in validating the simulations of the design margin and allow for rapid problem identification if circuit performances are not satisfied.

In digital circuit, the shrinking of transistor size makes it possible that the system runs at the rate of Gigahertz, thus timing accuracy becomes more and more important. That would mean the constraint for timing accuracy is stricter. Timing uncertainty due to process variations may induce

jitter in the system. For example, if the clock rate of the system is 100MHz, the effect of 100ps jitter is only 1% of the clock rate, but if the clock rate is 1GHz, the effect of this 100ps jitter would be 10%. Two key characteristics of clock signal, both jitter and clock skew are suffered from timing uncertainty. This timing uncertainty due to the weak routing information during early stage of design flow, the lack of accurate timing models for logic components and interconnects and the effect of process variations on propagation delay [28]. Accurate timing analysis models are dependant on the reliable characterization to process variations.

1.1.1 Timing uncertainty in frequency timing synthesis circuit

The typical application circuits suffered from timing uncertainty are many frequency synthesis circuits. Frequency synthesis is often used in digital designs, utilizing direct digital frequency synthesis (DDFS) or fractional-N synthesis techniques. The common method of either technique takes advantage of ring oscillators (RO) combining with programmable divider or accumulator to generate desired output frequency. With this synthesis method, each cell delay of RO may influence the accuracy of output. Thus device mismatch due to process variations causes deviation in time delay, leading to timing uncertainty to output.

Now we use an application circuit, Direct Digital Period Synthesis (DDPS) circuit to explain the timing uncertainty caused by process variations. A DDPS circuit [4] is a new architecture used to produce clock signals in television applications. It is expected to produce a clean clock signal. The diagram of DDPS circuit is shown in Figure 1.1. The transition generator of the DDPS uses a RO to generate copies of the clock signals that are equally delayed from each other. The transition selector in turn selects these equally phase shifted clocks according to the output of the phase accumulator. Ideally, these signals are equidistant. However, with the existing delay mismatch among the identical elements due to inevitable process variations, the individual signal edges are slightly misplaced from their expected timing values, causing jitter in the output signal.

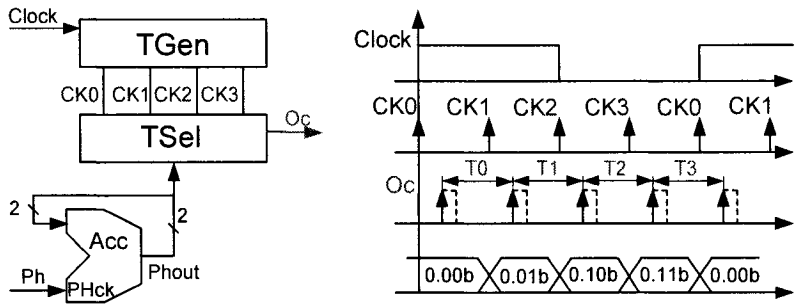


Figure 1.1 Block and timing diagram of DDPS circuit [4]

Delay mismatch due to process variations is one of the sources of spurious frequencies in this DDPS circuit. Another source relating to accumulator truncation has been characterized and modeled in [14]. Figure 1.2 displays spurs in spectrum of output frequency. In this figure, excluding fundamental frequency, spurs with relatively higher magnitudes and longer period are caused by accumulator truncation, while the smaller ones with high density are due to delay mismatch between single delay cells. Also, substrate and power supply noise are possible sources of such spurs, which are analyzed in [30].

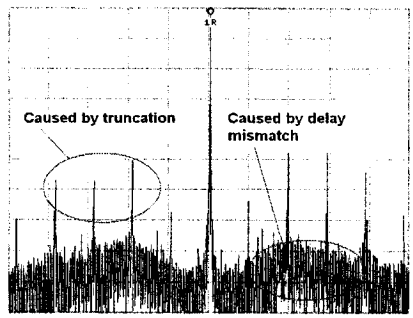


Figure 1.2 Spurs of output frequency in DDPS [4]

Since the delay mismatch is one of sources of jitters in DDPS circuit, we need to characterize this delay mismatch to find methods to reduce its effect. And this is also one of motivations of this project. It should be emphasized that the delay mismatch to be evaluated is the delay differences

between neighbor cells in the same RO, not the average delay of an RO, and it can only be obtained by measuring delays of each delay cell. The main goal of this work is not to measure the average single cell delay which is well done in previous works, but it is to measure mismatch between single cells delay.

1.1.2 Delay mismatch in Vernier Delay Line

In recent years, researchers have designed various schemes to perform on-chip measurement and time calibration. Many works have been engaging in improving the resolution of the measurement circuits. However, the resolution was always more than one gate delay until the emergence of the Vernier Delay Line (VDL) technique. This technique completes the breakthrough in timing measurement techniques, which makes it possible to measure interval time less than one gate delay. Now VDL is widely used in Time to Digital Converter (TDC) circuits [6] [10], which is one of the timing measurement techniques.

The typical architecture of VDL (Figure 1.3) uses two delay chains (t1 and t2 represent delay time of each delay element) feeding into the clock and data lines of a series of D-Latches [6].

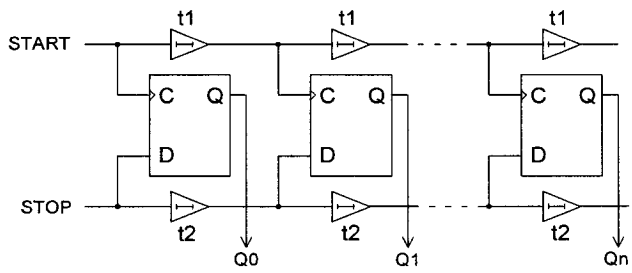


Figure 1.3 Schematic of VDL [6]

The delay time to be measured is the timing difference between START and STOP signals. If the interval time to be measured is D, the delay of a buffer in the upper delay chain is t_1, while that in the lower chain is t_2. We set up $t_1 > t_2$, then we have the timing diagram of VDL shown in Figure

1.4. As the START and STOP signals propagate in their respective delay chains. The timing difference between them will be less and less until this difference changes from positive to negative, so that the output of D-latch Q will change its state, from "0" to "1".

For example, in Figure 1.4, assuming $t_r = t_1 - t_2$, for the input of the first D-latch, the rising edge of clock signal (C) arrives earlier than that of data signal (D). The timing difference is $Tx_0 = D$. Therefore Q_0 is low. In the second D-latch, after propagation in delay element, the timing difference between C and D decreases as $Tx_1 = D - t_r$. In turn, in the third D-latch, the timing difference between C and D would be $Tx_2 = D - 2t_r$ ... until passing through $(n+1)^{th}$ delay elements. T_x in this D-latch is $Tx_n = D - nt_r$, at which the STOP signal catches up with the START signal. That means $Tx_n \leq 0$, and then the state of Q_n will rise to high at the rising edge of Clock signal. In this stage, the $D = nt_r$, which is the time delay between START and STOP, with a resolution of t_r.

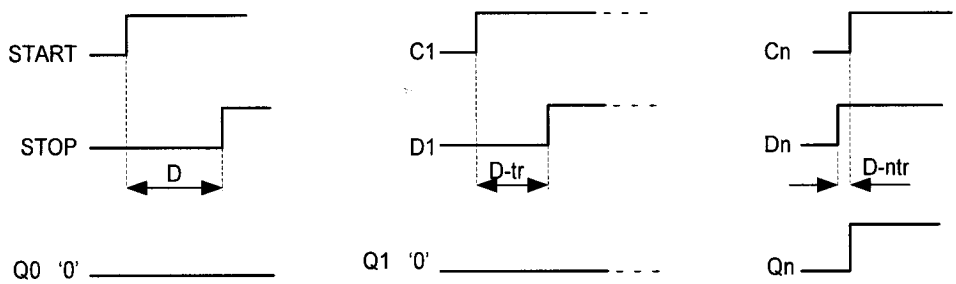


Figure 1.4 Timing diagram of Vernier Delay Line [6]

Because t_r is the difference delay between two delay elements, the VDL technique can measure timing difference with a resolution of less than single gate delay in the given process technology. However, as the measurement depends on the delay differences between two gates, the time resolution is strongly dependent on matching of pairs of delay elements, which is the most critical

drawback of VDL structure. The delays mismatch due to device and interconnect variations makes it impossible to get exactly same delay elements whose delay times are t1 or t_2.

Hence we need to characterize delay mismatch due to process variation and layout under certain technology and get accurate results that can be used to analyze circuits in design stage so as to reduce the effect of such mismatch. On the other hand, if designers do not account for the negative effects of delay mismatch, unpredictable behavior could result.

1.1.3 Clock skew

Another characteristic, closely related to process variations, is clock skew (Figure 1.5). On-chip clock skew is a function of device, interconnect, and device parameter variations. To equalize line lengths, a common practice is the use of a balanced clock network. That means using the same delay elements and equalizing the effects of interconnect resistance. However device parameter variations are still unavoidable leading to delay mismatch between delay elements that causes clock skew.

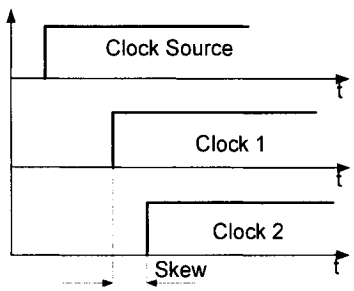


Figure 1.5 Clock skew

From testing results in studying a 1GHz microprocessor [18], a maximum clock skew of 34 ps due to the asymmetry of clock trees, 40-62 ps of skew due to interconnect variations and a tremendous 83 ps of skew due to poly critical dimension (CD) variations. Since variations in poly CD translates directly into variations in channel length of MOS transistor, hence device variation

must be taken into account for clock skew. In order to reduce the skew, many works focus on using same delay element and equalizing effect of interconnect resistance, however delay mismatch due to device variation makes clock skew inevitable. A high clock skew can potentially cause timing violation and even functional failures. Therefore, in timing analysis method, it is very important to estimate delay variability accurately.

1.2 Thesis goal

On-chip measurement is one of the major challenges in recent years for characterizing process variability. Although we have statistic models to carry out corner, worst case and Monte Carlo simulations to predict inter-die process variations, with the development of CMOS technologies, these models should be improved constantly. On the other hand, with transistor sizes shrinking, the systematic and random intra-die fluctuations of channel length have exceeded the inter-die fluctuations. Thus, intra-die fluctuations are growing threat to the performance and functionality of future gig scale integration [3]. However, since this kind of variation is much more complicated than inter-die variations, about how this intra-die process variations impact on circuit characteristics, until now we haven't had an acknowledged model to quantify it.

In order to predict variation in process so as to reduce its effects on CMOS integrated circuit, an effective way is designing one or more test circuits. From these test circuits we may extract most critical parameters that highly influence circuit performances. Furthermore, we may create a statistical analysis model to describe those parameter variations accurately. Moreover, these test circuits should be able to be upgraded easily for next generation technology. This kind of model has being expected by designers for a long period of time. The designed circuit in this master thesis is used to investigate delay mismatch mentioned in the section 1.1, verify critical

parameters causing delay mismatch and relationships between these parameters and delay mismatch.

The goal of this master thesis is to develop such a test structure that we can use to obtain useful experimental data from it only by performing simple measurement. From data measurement, we can analyze delay mismatch due to both inter-die and intra-die process variations, especially, spatial intra-die variations, characterize effects of delay mismatch on performance of digital circuit such as DDPS, TDC and other timing measurement circuits. Also, the analyzing results can be used as an important reference for timing analysis method in digital circuits. It requires that the measurement results for the circuit can represent process variations obviously and distinctly, be accurate, and be easy to extract parameters from obtained data. It is a really challenge to measure delay mismatch due to intra-die delay variations because the delay differences are too small and hard to capture. However the results will provide useful data for us to estimate how the delay mismatch impact on circuit and it will no doubt largely improve design quality.

For this master thesis, the test structure is based on ring oscillators. The device variation analyses only focuses on gate-length and interconnect variation, which are two dominant factors causing delay mismatch. Although using ring oscillator to characterize variation is not a new concept, there are many previous works engaging in analyzing intra-die variations by measuring average delay of each dependent ring oscillator, however we take advantage of different method in delay measurement by measuring single cell delays and delay mismatch between adjacent cells in a RO instead of average delay. This point of view will be explained in detail in Chapter 3. The single cell delay is obtained only by measuring period of series of related RO with the same structures. Moreover the chip measurement procedure can be completed by using simple lab equipment such

as signal generator and oscilloscope, without using a large and special probe station and equipment.

1.3 Organization of thesis

This master thesis is composed of six chapters. The content includes design, analysis, implementation and test of modified ring oscillator test structure. This chapter (Chapter 1) outlines the motivation and goal of the master thesis, the importance of intra-die variation characterization and its benefit to circuit design. Chapter 2 introduces theory of process variations and computer tools for statistic analyzing process variations. Chapter 3 discusses the main previous works on on-chip measurement of delay mismatch and intra-die variation characterization and presents a novel test structure for single cell delay measurement including digital control circuit. Chapter 4 explains test chip implementation with powerful computer aided design tools and layout consideration. Layout optimization and post layout simulation results are also explained in this chapter. In Chapter 5, we focus on the test procedures, test equipment, chip debugging and diagnosis. The final chapter, Chapter 6, summarizes the important issues of the master thesis. Besides, the master thesis contribution and possible future work are also provided in Chapter 6.

CHAPTER 2

PROCESS VARIATIONS IN CMOS INTEGRATED CIRCUITS

Integrated circuits have always been susceptible to process variations. Even though significant advances have been made to reduce process variations, silicon manufacturers have not been able to keep up with technology scaling. As no manufacturing process can ever be perfect, chip designers should give a certain margin to their design with compliance to the fabrication techniques. Considering process variations makes design stage simulation results of circuit performances closer to real results so that designers can adjust their designs to accommodate to variations, reducing negative effects due to process variations. The importance of understanding process variations and their impacts on circuit performances is directly related to design quality and manufacturing yield.

2.1 Sources of process variations

Process variations are caused by non-ideal conditions in manufacturing, like mask misalignment, etching errors, variations in doping concentrations, etc, which cause physical size variation in both device and interconnect. As a result, electrical parameters such as resistance, capacitance and voltage threshold vary a bit from nominal/designed values, thus impact on circuit performances. In general, there are three factors that affect circuit performances: device variations, interconnect variations and environmental variations. Device and interconnect variations can be further divided into two categories: inter-die and intra-die variations. Inter-die variations are largely independent of design implementation and we already have worst-case

model to analyze it. While intra-die variations are dependent on the design implementation (layout) and for which no general effective modeling and analysis methodologies yet exist [21]. This master thesis focuses on device and interconnects variations, especially the device variation, which is the most important factor causing intra-die variation.

2.1.1 Device variations

Due to process variations, device parameters present difference from die to die which results in difference in electrical characteristics from circuit to circuit, this is called inter-die variations. Intra-die variations, however, means the fluctuation occurs between devices in the same die, which may degrade the circuit performance or even cause failure of the circuit. There are also, of course, lot-to-lot and wafer-to-wafer variations. However for higher performance chips, inter-die and intra-die variations have a significant impact on their performances [3].

One source of inter-die variations is non-uniform resist thickness across the wafer, which is random from wafer to wafer, but deterministic within the wafer. The inter-die variations present the fluctuation in characteristics between chips assuming uniform characteristics within a chip. Inter-die variations, which equally affect on device inside a chip, can be considered as global shifts in characteristics from die to die, and normally present systematical feature. These global shifts in circuit characteristics are directly related to manufacturing yield.

Intra-die variations are highly caused by process fluctuation, especially with the downscaling of MOSFET dimension in the deep sub-micron technology. Comparing to inter-die variations, intra-die variations present both systematic and stochastic features. Aberration in the stepper lens is one of sources of systematic intra-die variations. It is an intrinsic effect since it cannot be eliminated by external control of conventional manufacturing processes. Besides, placement of doping atoms in the device channel region, which varies randomly and independently from device to device, is an example of source of stochastic intra-die variations [3]. The sources of intra-die

variations imply that this kind of variations present both systematic and random properties. Moreover, they are inevitable.

Traditionally, inter-die fluctuations have been the main concern in CMOS digital circuit designs, and the intra-die fluctuations have been neglected. With the decreasing of device sizes and chip area, Intra-die process variations increase substantially leading to much more effects on circuit performances. Intra-die fluctuations become a growing threat to the circuit performances.

2.1.2 Interconnect variations

In integrated circuits, the metal interconnects often act as load resistance, capacitance and inductance. Similar to device variations, dimensions of metal interconnects can also produce variations. The 3-dimension variations (metal line length, width, thickness and space between lines both in the same layer and different layers) lead to different electronic properties, which directly affect the circuit performances. In manufacturing process, the major sources of interconnect variations are from chemical mechanical polishing (CMP) and line width variations. There is no acknowledged model to characterize them until now. However the effect of interconnect would be more important as the combination of technology scaling and clock frequencies increasing. According to the simulation results for a variety of technologies, reported in [21], length of interconnect is not scaling down as fast as effective length of transistor (L_{eff}), which recalls the influences of interconnect would be increasing as CMOS technology advances.

2.1.3 Environmental variations

Besides those factors mentioned above, power supply voltage and temperature (PVT) also affect electrical performances of circuits. For example, power supply noise would cause jitter in PLL, leading to variation of phase alignment. Propagation delay in CMOS circuit would vary with the

temperature fluctuation and power supply voltage variations. PVT factor is highly design dependent and exhibit timing constants.

2.2 Effects of process variations on circuit performances

Most of effects of process variations on digital circuits are related to timing. In many digital circuits such as Delay Locked Loop (DLL) and Time-to-Digital Converter (TDC) involving delay chains composed of identical delay elements, the mismatches in the propagation delay of individual delay elements cause timing uncertainty. In DLL circuits, a Voltage Control Delay Line (VCDL) that consists of several tunable delay cells is used to generate multiple phases of the low frequency clock, which are combined into one high frequency clock. The stochastic mismatch between the cell delays causes clock skew of the intermediate clock phases, leading to spurious peaks in the output frequency spectrum of the output signals. Similarly, the delay-chain-based TDC circuits such as the Vernier Delay Line (VDL) time measurements are achieved with a timing resolution that depends on the propagation delays of the delay cells in the chain. Any delay mismatch between delay cells affects the circuit resolution, degrading the accuracy of the measurement. In synchronous circuit, delay mismatch is one of sources causing clock skew.

On the other hand, in analog and mixed-signal circuit design, such as analog-to-digital converter (ADC), mirror current source, bandgap voltage regulator, etc, the transistor mismatch plays a major role in limiting the performance of many precision analog integrated circuits.

Since device mismatch is caused by physical parameter mismatch during process, it is necessary to understand how parameter fluctuations affect on electrical parameters. This master thesis concentrates on delay mismatch because it is one of the most critical problems in today's high speed digital circuit, therefore we only concern parameters related to gate propagation delay, which cause delay mismatch directly.

2.2.1 Statistical model to stochastic parameter variability

Physical parameters of MOSFET transistors, which experience process variations, include gate-length (L_{gate}), gate-width (W_{gate}), doping concentration (N_{ch}), and oxide thickness (T_{ox}). Since all these physical parameters are both size and bias independent, the parameters can be characterized by the area according to the Pelgrom's law [26] for the intra-die statistical model, which is widely used for recent studies on the matching analysis. Thus five parameters can be modeled as:

$$\sigma^2(\Delta L) = \frac{A_{\Delta L}^2}{WL^2} \tag{2.1}$$

$$\sigma^2(\Delta W) = \frac{A_{\Delta W}^2}{W^2 L} \tag{2.2}$$

$$\sigma^2(T_{ox}) = \frac{A_{T_{ox}}^2}{WL} \tag{2.3}$$

$$\sigma^2(N_{CH}) = \frac{A_{N_{CH}}^2}{WL} \tag{2.4}$$

ΔL and ΔW represent deviations of gate length and gate width. Parameters such as $A_{\Delta L}$, $A_{\Delta W}$, A_{NCH} and A_{Tox} are process-dependent constants. The function of $\sigma(Parameter)$ indicates the standard deviation of the parameter to its mean value. The model is based on the assumption that within a limited area on a wafer, such as within a chip or a small circuit, the variations are treated as normal distribution. For the variation over the whole wafer, however, it is not expressed as a normal distribution due to the existence of the systematic variability [26]. From these equations, we notice under a certain technology, intra-die variations (mismatch) will increase with the gate area shrinking. Pelgrom model is applied for stochastic variability. However it models systematic fluctuation as a linear gradient across the die. Figure 2.1 displays the gradient gate length distribution across a wafer [24].

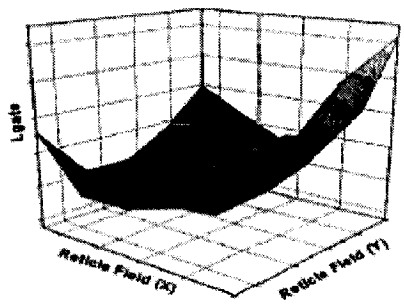


Figure 2.1 Gradient gate length distribution across a wafer [24]

The horizontal field (with x and y directions) represents die position in the wafer, and vertical field illustrates gate length. From this figure we can see that in the center of the wafer, gate length is the most closed to its mean value. The closer the die locates to the edge of the wafer, the larger deviation of gate length occurs. In this master thesis, we treat parameter variations within a circuit as normal distributions.

2.2.2 Delay mismatch

Every transistor on charging/discharging path influences the propagation delays. Parameter fluctuations caused by intra-die variations result in gate delay mismatch in transistors. So transistors with exactly same nominal/designed sizes have different delays, which is delay mismatch. Delay mismatch exists in many application circuits, inducing all kinds of unsatisfied performances. In digital circuits, this delay mismatch may cause clock uncertainty or clock skew. Many physical parameters of transistor experience process variations. We have to determine which are critical ones causing delay mismatch. We start from analyzing delay of a buffer with two inverters. Complex expressions of propagation delay of inverter in [1] [8] [9] imply its high dependence on process parameters, such as device size, junction capacitances, p-n junction

potential, etc. In order to link transistor physical parameters to the gate delay, we use a compact model [24] to describe single inverter delay as:

$$D = \frac{C_L V_{dd}}{n}(I_{dn}^{-1} + I_{dp}^{-1}) \tag{2.5}$$

where D is inverter delay, C_L is load capacitance, I_{dn} and I_{dp} are drain currents of NMOS and PMOS, V_{dd} is supply voltage and n is a constant. C_L is fixed by parasitic junction capacitance (C_{junc}) and gate capacitance (C_{gate}) of the following inverter [29]. Because the parasitic C_{junc} is very small, we assume that C_L almost equals to C_{gate}(both gate capacitances of NMOS and PMOS). In this circuit, we also assume that we use the same length for both NMOS and PMOS transistors. Hence C_L is given by:

$$C_L \approx C_{gate} = C_{gate.N} + C_{gate.P} = C_{ox} L_{gate}(W_{gate.n} + W_{gate.p}) \tag{2.6}$$

where L_{gate} is transistor gate length, $W_{gate.n}$ is NMOS transistor width, $W_{gate.p}$ is PMOS transistor width, and C_{ox} is capacitance of a unit area which can be expressed by:

$$C_{ox} = \frac{\varepsilon_{rsio_2}\varepsilon_0}{T_{ox}} \tag{2.7}$$

where T_{ox} : oxide thickness

ε_{rsio_2} : relative permittivity of SiO2

ε_0 : permittivity of free space

ε_{rsio_2} and ε_0 are constants. Therefore, C_{ox} is only dependent on T_{ox}.

For deep sub-micron MOS device, the saturation current in equation (2.5) can be described by universal empirical equation [24]:

$$I_{sat} \approx L_{gate}^{-0.5} T_{ox}^{-0.8}(Vdd - V_{th}) \tag{2.8}$$

Hence

$$I_{dn}^{-1} \approx L_{gate}^{0.5} T_{ox}^{0.8} (Vdd - V_{th,n})^{-1} \quad (2.9)$$

$$I_{dp}^{-1} \approx L_{gate}^{0.5} T_{ox}^{0.8} (Vdd - V_{th,p})^{-1} \quad (2.10)$$

From the equations (2.5) to (2.10), we obtain an equation to describe inverter-based delay:

$$D = K \cdot L_{gate}^{1.5} \cdot T_{ox}^{-0.2} \cdot (W_n + W_p) \cdot [(V_{dd} - V_{th,n})^{-1} + (V_{dd} - V_{th,p})^{-1}] \quad (2.11)$$

where K is a lumped process-specified constant. If we only consider bias independent parameters, from equation (2.11), we get to know that fluctuations in L, W and T_{ox} of a transistor may cause different gate delay. Therefore, they are critical parameters that cause delay mismatch. This equation also indicates gate length is the dominant parameter to gate delay. The gate delay dependent on length by order of 1.5, T_{ox} by order of –0.2 and width by order of 1.

2.2.3 Critical parameter analysis

The relationship of transistor gate delay to its physical parameters (L, W and T_{ox}) is described in approximation formula (2.11), which shows that gate length may induce the most delay deviation if all parameters have the same fluctuation. However fluctuations of different parameters are different in the real process technique. In order to analyze effects of these critical parameters on delay mismatch, we use the delay chain shown in Figure 2.2. The delay chain is formed by cascade inverters. Each inverter consists of one NMOS and one PMOS transistor. The load capacitance of the current inverter equals to the gate capacitance of the next inverter.

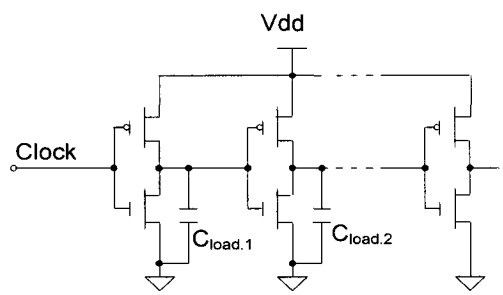


Figure 2.2 Delay chain consisted of digital inverters

Given an ideal clock to its input, delay chain will transmit the clock with certain delay. In this simulation, we used minimum size of NMOS transistors, that is L=0.18μm, W=0.5μm. for PMOS, L=0.18μm and W=2μm. We set up standard deviation for each critical parameter individually, and carry out Monte Carlo simulation to analyze the delay variations affected by parameter fluctuations.

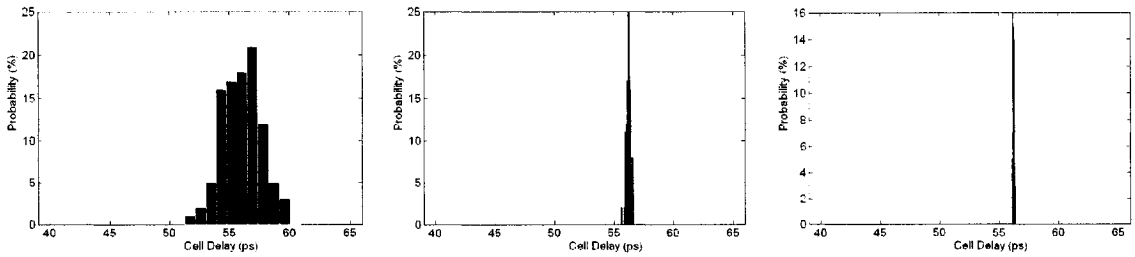
The only goal of these simulations is to find out the dominant parameter inducing delay mismatch among the three critical parameters, but not to evaluate the exact values of delay variations, so only the average delay in the delay chain is computed. Parameter deviations for each parameter (L, W and T_{ox}) are set up according to the technology data provided by TSMC under 0.18μm CMOS technology. Table 2.1 gives mean values (μ) and standard deviations (σ) of delay for different parameter fluctuations. The mean values of average cell delay are almost same with three parameter fluctuations; however, the standard deviations under the three circumstances are quite different. Fluctuation in transistor length can cause a very large delay deviation. Therefore, the effect of transistor length is much larger than that of other parameters.

Table 2.1 Average cell delay variations

Parameter	μ (ps)	σ (ps)
L_{gate}	56.23	1.77
W_{gate}	56.23	0.06
T_{ox}	56.21	0.2

Figure 2.3 displays histogram of simulation result. From this figure, the conclusion is made that gate length is a dominant factor causing delay mismatch, whereas the fluctuation in gate width causes the smallest deviation of delay. One of the reasons that effects of gate width deviations

due to process variations is very small is that gate width is designed much larger than gate length, leading to little affected by process variations.



a) b) c)

Figure 2.3 Effect of critical parameters on delay mismatch;
a) gate length effect; b) oxide thickness effect; c) gate width effect

Since in actual circuit, gate width is usually much larger than gate length, so it is not affected by process variation as much as length. Moreover, in the fabrication process, T_{ox} is generally better controlled than the other parameters. Thus in this master thesis only length's deviations has been considered for delay mismatch. The scatter plot in Figure 2.4 illustrates relationship between inverter delay and gate length. This figure indicates that the small variation on gate length may cause gate large enough delay deviation that affect on circuit performance.

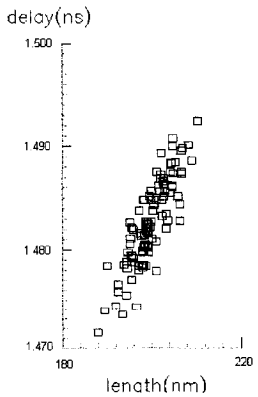


Figure 2.4 Inverter delay vs. gate length

2.2.4 Analysis of channel length variation

In traditional semiconductor manufacturing, integrated circuit (IC) layout patterns are printed onto a silicon wafer using light projected through a mask or reticle [27]. For earlier process technologies, the ratio of target resolution to optical resolution remained above or at least at unity of wavelength. Since the device feature sizes become much smaller than the wavelength of the light source used in optical lithography, newer process technologies are created with a resolution well below the wavelength of light used to project the IC layout pattern. Therefore, optical distortions, which have traditionally been ignored due to the light wavelength being larger than the feature size, can no longer be neglected. These distortions create patterns on silicon that are substantially different from the drawn layout for the sub 0.18 micron technology using a higher wavelength light source.

The optical distortions induce highly non-linear in every chip-manufacturing step and an old "What you see is what you get" (WYSIWYG) paradigm does not work anymore. That would mean, in sub-wavelength regime, layout is not equal to mask, and printed on wafer silicon image differs from the mask pattern [15]. This under wavelength of light feature size make the transistor length becomes the most important physical parameter that experiences the optical distortion.

2.3 Statistical analysis in CADENCE

Statistical analysis is a powerful method for estimating production yield. Throughout the statistical simulation, we can use the data analysis features to examine how manufacturing tolerances affect the overall production yield of design. If it is necessary, we can then change our design to improve the yield.

In CADENCE, there are two methods to simulate circuit performance under realistic variations in process: Corner Analysis and Statistical Analysis (Monte Carlo Analysis).

Corner Analysis uses 3σ-boundaries of main process parameter technique. This is a simple way to carry out a statistical analysis. It takes a set of n model parameters, which are assumed to have the largest deviation from nominal values (boundary) and simulate the effects on the circuit performance, first makes one simulation run with the nominal values and then perform an analysis of the circuit performance to the variation of every process parameter. Then a fast and a slow model parameter set can be built with the ±3σ values of the parameters. General estimations to many applications are NMOS and PMOS slow devices (SS), NMOS and PMOS fast devices (FF), NMOS slow and PMOS fast devices (SF), and NMOS fast and PMOS slow devices (FS). Adding power and temperature factors to corners analysis, we can carry out what is called worst-case analysis. Parameter fluctuations in device can be deviation in length (DXL), width (DXW), threshold DVTH, oxide thickness (T_{ox}), and many parasitic capacitances. With this method the boundaries of performance can be determined very roughly. The result of this type of simulations can be very inaccurate, because only a few parameters of the whole simulation model parameter sets are used and the rest of the model parameters are set to their nominal values. Another source of errors is that it would neglect the correlation between many model parameters.

Another statistic analysis technique is Monte Carlo Simulation. It allows multiple simulations with varying parameter values according to their distributions described in the model. It uses principal components as dependent variables, which will be varied randomly by a normal, logarithm or uniform distribution. This type of simulation can get accurate result, but it takes much CPU time.

For this Monte Carlo statistical analysis, the most important thing is to create an enough accurate model to demonstrate the distributions of both process variations (inter-die variations) and device mismatch (intra-die variations) for each parameter.

Regarding the parameter distributions over the whole sampled data and over the wafer surface, the following assumption will be drawn for statistical analysis:

In intra-die variation investigation, most of model parameters can be approximated by a Gaussian distribution function. This has additionally been confirmed by analyzing some key-parameters from the production database of the fabrication where the test wafers have been produced.

The Monte Carlo statistical analysis would give better results if we carry out sufficient number of simulations with statistical variations of the device parameters modeled directly. Monte Carlo analysis predicts product yield before production by enabling early statistical analysis. The selectable variation type (process and mismatch) enables us to simulate performance deviation of circuit affected by either inter-die or intra-die variations. When "Process" variation is selected, all transistors will be assigned same parameter deviations at a time, and random deviations values will be generated from run to run according to the process section of statistical file. When "Mismatch" variation is selected, transistors are assigned random deviation values according to mismatch section of statistical file. It generates reports for measurements, including probability-density histograms; probability; statistical data, such as mean values and standard deviation and scatter plots which are useful for verifying either interactions between different statistical data sets or dependencies between parameters and circuit performances. Monte Carlo simulations are used to perform statistical analysis in this master thesis.

CHAPTER 3

MEASURING SINGLE CELL DELAY AND DELAY MISMATCH

The previous chapter describes the sources of process variation and its effects on the circuit performance, especially the effects on the delay. This chapter will discuss how to measure single cell delay and delay mismatch due to process variations with test circuits.

At first, this chapter will give a review of previous works on delay mismatch measurement, and then describe proposed test circuit, which is used to measure cell delay and delay mismatch. Two ring oscillator based test architectures will be presented. The first architecture represents the basic idea of the cell delay measurement but its unsymmetrical feature limits its feasibility. The second one is improved and proposed structure, which overcomes the drawback of the first one. Digital control circuit, which ensures the test structure to work properly, will be also described in this chapter.

3.1 State of the art

3.1.1 Introduction

Any new technology in process would mean new challenges in design and test. As polysilicon gate lengths have decreased below the wavelength of light used in the optical lithography process, the importance of intra-die fluctuations in channel length have become more than inter-die fluctuations, especially in CMOS digital circuit design including memory, microprocessor and

other application circuits [17] [20]. Considering intra-die variations in design techniques is required to improve the yield and performance in scaled technologies.

Accurate estimation of intra-die variation effect on circuit is related to realization of robust design and manufacturing yield. Traditionally, only inter-die variation has been concerned in timing analyzing methods. Intra-die variation has only been considered as a certain percentage of 15%-20%, which now is found inaccurate [23]. On the other hand deep sub-micron technologies exhibit a new intra-die variability pattern. Many previous works consider intra-die variation as stochastic, however, recently research shows that it presents both systematic and stochastic.

Hence characterizing process variations, especially the intra-die variation, with a new pattern is becoming important. It can provide accurate evidence to timing analyzing technology.

In digital circuit, one source of timing uncertainty is delay mismatch due to intra-die variations. Therefore measuring delay and analyzing delay mismatch is an effective way to characterize intra-die variations. There are three main approaches to measure on-chip delays: using external probes to measure the signals of interest, using e-beams to observe electrical signals, and using on-chip measurement techniques. The main drawbacks of probes are intrusiveness and handling complexity that limit the number and the accuracy of the delay measurements. E-beam techniques, on the other hand, are much less intrusive but much more expensive. Therefore their practical application is limited as well. Both limitations are overcome, in principle, by on-chip measurement techniques. On-chip measurement takes advantages of both economy and accuracy. First, measurement equipment can be placed as close as possible to the test structure, thus improving the signal to noise ratio, secondly, delay measurements can be performed in the actual operating conditions and third, only low-cost external instrumentation is required [16].

In recent years, researchers have designed various structures to perform delay measurement in order to characterize inter-die and intra-die process variations. Delay chain and ring oscillator

(RO) are mostly used to study the propagation delay and delay mismatch due to process variations. Delay chain can be composed by multiple cascaded copies of the same delay elements. Hence each element has the same propagation delay, and delay is amplified through the delay chain. RO is a closed-loop delay chain, which must be composed of odd number of cells. It does not need any source of input but can create periodic signal by oscillation whose period is twice of the sum of each delay cell (Figure 3.1).

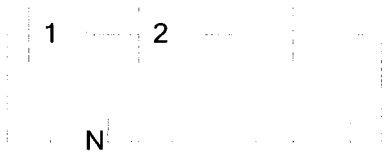


Figure 3.1 Ring oscillator composed by inverters

$$P_{RO} = 2\sum_{i=1}^{N} D_i \tag{3.1}$$

where P_{RO} is the period of the RO and D_i is the delay of the i^{th} cell.

The advantages of delay chains and RO include that they are easy to be created on-chip and highly sensitive to process variations, especially to gate length variation in process. Collected data from an actual state-of-the-art fabrication facility revealed that significant systematic spatial intra-chip variability of MOS gate length leads to large circuit path delay variation. Analysis shows that the spatial gate length variation is the main cause of large circuit speed degradation [24].

In practice, RO make it possible to measure average cell delay as the ratio of the overall delay (period) to the number of cells in the structure. For example, if the period of a ring oscillator composed by N cells is T, then we can say that average single cell propagation delay is T/2N. The result is the average propagation delay of the cells in the structure that can be used to evaluate the cell performance in the typical-case.

3.1.2 Previous work

Earlier attempts for characterizing the delay mismatch due to process variations involve test structures with RO because its cell delay is very sensitive to process variations. Carrying out statistical analysis with RO can get evident and useful data to characterize intra-die variations. Solutions reported in [13] [25] put large number of ring oscillators on test chips, and characterize variation performance by measuring RO frequencies (or periods), which in fact represent the average delay of delay cells. Although such method is efficient to characterize variability through a wafer and systematic variation inside circuit, period of the RO is based on the sum delay values of all delay elements, hiding individual properties of delays in each cell. Hence thorough estimation and characterization of the intra-die process variations and mismatch may not be obtainable, using such methods.

Another approach to find out delay mismatch in delay cells referred as code density test and random sampling was reported in [12] [16] [19]. They perform a statistical test on the line to the same signal by a large number of sampling, and then correct the individual cell delay mismatch according to the test results. Figure 3.2 displays the random sampling approach described in [16]. For a delay cell with input signal, it gives rise to a periodic output signal. Voltage of input and output are represented as V_{in} and V_{out} in the figure.

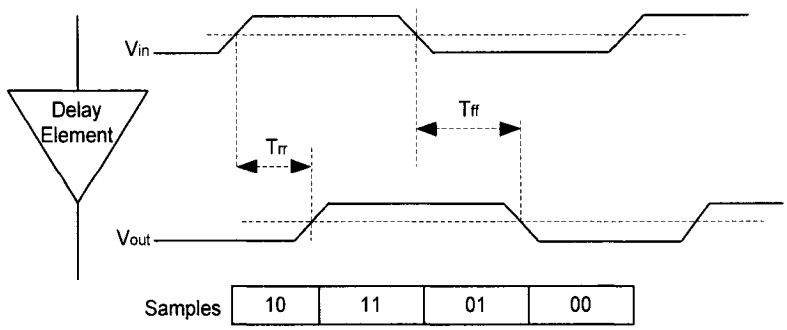


Figure 3.2 Illustration of random sampling approach [16]

When sampling the values of V_{in} and V_{out} at a random time instant, they obtain two Boolean random variables S_{in} and S_{out} respectively. The probability Pr (S_{in} =1, S_{out} =0) is proportional to the propagation delay of a rising edge through the cell. That would mean, the longer the propagation delay, the higher the probability of sampling the two waveforms when the input signal is already high but the output signal is still low.

$$\Pr(S_{in}=1, S_{out}=0)=\frac{T_{rr}}{T} \tag{3.2}$$

Where T_{rr} is the rising edge propagation delay and T is the period of signal.

The key issue is the probability, which can be estimated from a random sample of N independent elements by computing the relative frequency of event S_{in} =1, S_{out} =0, denoted by F (1, 0).

$$F(1,0)=\frac{N(1,0)}{N} \tag{3.3}$$

So that the rising edge propagation delay can be obtained from event counts.

$$Trr \cong \frac{N(1,0)}{N}T \tag{3.4}$$

This method is based on statistical measurement of device under test. According to the theory of random sampling, the higher the value of N is, the higher the accuracy of F (1, 0) would be. Using such type of approach and in order to achieve high precision, large number of events has to be generated [16]. The generation of such large number of events in turn would require large number of counters for each cell. Under 0.18um CMOS technology, delay mismatch between 2-transistor inverters may reach as small as a few picoseconds, requiring a sub-picoseconds measurement resolution. Using code density test to characterize the delay mismatch would need quite considerable number of counters, making this technique area consuming.

A test structure based on direct measurement of the delay mismatch between single cells was reported in [2] proposing a solution to measure slightly different delays in each delay cell. The

basic test structure is using a ring oscillator composed of controllable CMOS inverters that may exhibit two different propagation delays (Figure 3.3) of the same cell, depending on the control values of a digital control signal.

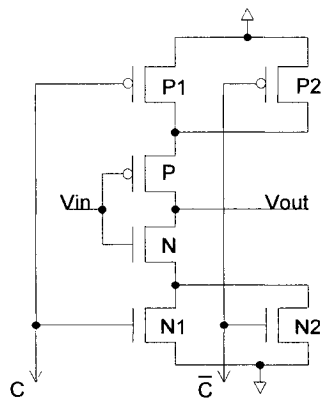


Figure 3.3 Architecture of measuring slightly different delays in each delay cell

When the control signal C = 0, the delay cell is consisted of P1, P, N and N2, the propagation delay is T_0, on the other hand, when C=1, the delay cell is consisted of P2, P, N and N1, the propagation delay is $T_0 + dT$. If the two periods of corresponding ROs are measured, the difference between the two propagation delays of each cell can be obtained from the RO period's difference. Since each cell has its own control signal, the incremental delay of any cell can be individually measured by providing the proper configuration of control bits. Although this direct measuring test structure can measure the incremental delay, i.e., the difference between the two propagation delays in the same cell cannot be used to characterize the delay mismatch between any two given cells. Measuring propagation delay mismatch in the same delay cell is not enough to analyze significant intra-die variations, which are spatial dependant.

3.1.3 Proposed single cell delay measurement

A thorough characterization of the effects of systematic and random variations and on circuit performance would require the capability of measuring single-cell propagation delays with sub-nanosecond time resolution. Therefore it is necessary to design a test circuit, which could be used to obtain real single cell delays in a RO, so as to characterize effects of both systematic and random variations on circuit performance accurately and thoroughly. Since gate delay (with minimum size) under 0.18um technology is about 50 picoseconds, it would require the measuring resolution of the circuit to be able to reach the order of a picoseconds or sub-picoseconds, obviously it's impossible to measure it directly. On the other hand, using normal ring oscillators which measure average delay hardly reach the target either. In this master thesis we use modified RO to realize the single cell delay measurement. The basic idea of the modified RO structure is using a series of related ROs instead of using independent ones. Since RO period relies on the total cell delays, if the relations between different RO periods are made properly, then single cell delays can be derived by only measuring periods of all of these RO, which is very easy to get only using general measuring equipment.

We will present two different modified RO test architectures: the simple one and the improved one. The relationships between ROs in the simple structure are very simple, and cell delays can be obtained by RO period differences directly. But the symmetry of this simple structure is not satisfactory. The improved structure is designed for overcoming the drawback of the simple one; it is a completely symmetrical structure. However, the relationships between ROs in improved structure are relatively complicated, and cell delay derivation is a longer computing procedure than that in simple one.

3.2 Simple modified RO test structure

In this structure, delay cells are added to RO one by one. That means each RO is composed by the cell delays which are formed the previous RO plus one more cell. The simple modified RO structure is shown in Figure 3.4.

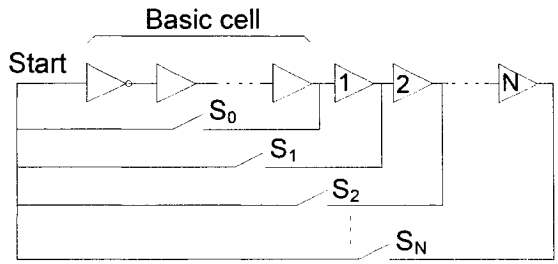


Figure 3.4 Architecture of simple modified RO

The architecture of simple modified RO consists of a few of basic cells plus N delay cells under test. Basic cells consist of five inverters, which are the least cells forming RO. N delay cells are controlled through a switching network (S_0, S_1, S_2 ... S_N). Here we use transmission gates (TG) to act as switches. Each delay cell is formed by two inverters (Figure 3.5), which makes sure that cell stage of each RO is odd number.

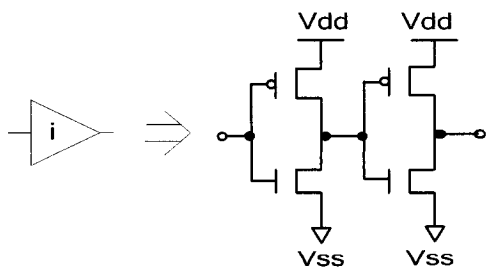


Figure 3.5 Schematic of single delay cell in simple modified RO

The switching network is used to select RO for the period to be measured. Each time, we select only one switch to be on and all the others are off, so that a RO is formed. Next step we select

next adjacent switch to be on and turn off the previous one. At this time, the RO has one more delay cell than the previous RO. The different periods between these two ROs represents the delay of the added cell. For example, if S_0 is set to on, then RO_0 is formed, which consists of basic cells only. The measured period (T_0) of RO_0 is relied on sum of delays of basic cells. If S_1, rather then S_0, is on, the measured period (P_1) is the period of a RO_1, which is composed by the basic cells plus cell 1, turning on S_2 forms RO_2, get period of P_2, and so on. The difference between P_1 and P_0 represents two times the delay of cell 1, difference between P_2 and P_1 represents two times the delay of cell 2, etc. Thus the delay of each cell (D_i) is given by:

$$D_i = \frac{1}{2}(P_i - P_{i-1}) \quad (1 \le i \le N) \tag{3.5}$$

In this structure, we add delay cell one by one and calculate their delay by measuring each RO period. The delay mismatch between the selectable adjacent cells is given by following: D_1-D_2, D_2-D_3 ... D_{N-1}-D_N. In the ideal situation, all the selectable cells should have exactly the same delay, therefore there would be no delay mismatch, in other words, delay mismatch should be zero. However, we cannot get equal cell delays with this method, even in the ideal case (same device without process variations and interconnect effects). Table 3.1 shows the transient simulation results for schematic.

Table 3.1 Delay increment in simple modified RO

RO number	RO Period Pi (ps)	Cell Delay Di (ps)
Basic RO	761	NA
RO1	973	106
RO2	1150	88.5
RO3	1320	85
RO4	1485	82.5
RO5	1652	83.5
RO6	1810	79
RO7	1964	77
RO8	2100	68

In this table, the first column represents RO number. RO_0 consists of basic cells only, RO_1 consists of basic cell plus cell 1, RO_2 consists of basic cells plus cell 1 and cell 2, and so on. The second column gives the period of each RO. P_0 to P_8 are displayed from the second row of this column to the last row. According to equation 3.4, single cell delays are derived and shown in the third column (from the row 3 to the last row are D_1 to D_8). From the third column we notice that single cell delays are not identical as it is expected. This unequal cell delay is due to the fact that this structure is not symmetrical structure. Although we add one delay element at each step, however cell structures are different from one RO to the other. The non-uniform of cell delays in this structure is displayed in Figure 3.6.

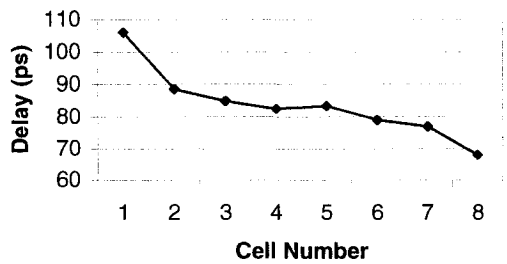


Figure 3.6 Single cell delays in simple modified RO

Unsymmetrical structure says delay elements in a RO are not same. Three are both basic cells and appending cells for each RO, an appending cell includes transmission gate connected, while basic cells don't connect to such TG. From Figure 3.4, we notice that every delay cell is connected to one switch, except the first cell (in "Start" node) which is connected to each of the N switches; whereas no switch is connected to the output of other basic cells. If we only consider the effect of a transmission gate as a resistor (R_{TG}) when it is on, its effect as capacitor (C_{TG}) when it is off and capacitance loaded by next unselected cell as C_{load}, for a RO consisted of basic cells plus n appending cells, the schematic of approximated RC model is shown in Figure 3.7, which displays

that the ring oscillator is not balanced; all of cells have the different load capacitance and resistance. If n^{th} RO is selected, for example, the cell n connects to R_{TG}. However if the last RO (Nth RO) is selected, the cell N connects only R_{TG} without C_{load} from unselected cells. That's the reason why the last cell delay in Figure 3.6 presents much smaller than other cells. Moreover, the last cell of each RO connects to different number of delay cells. For example, for RO_1, the last cell connects (N-1) serial delay cells, whereas for RO_2, the last cell connects (N-2) such delay cells. These two factors make load capacitors different between different ROs, which induce delay variation even without process variations.

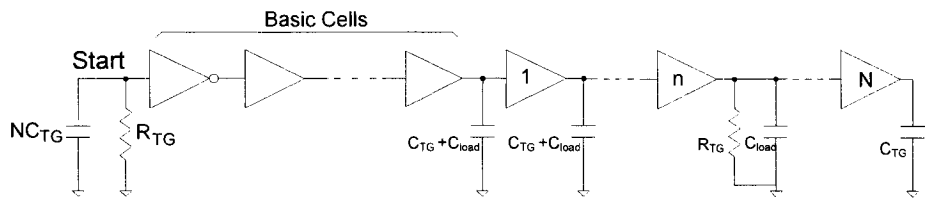


Figure 3.7 Approximated RC model of simple modified RO

Therefore, the differences in delay represent not only cell-to-cell mismatch due to process variations in device but also other factors. Hence we cannot use this structure to characterize delay mismatch due to process variations, because delay mismatch caused by process variations may less than that caused by unbalanced structure itself.

3.3 Improved modified RO test structure

Based on the simple test structure described in the previous subsection, an improved architecture of test structure is presented [31]. In the simple structure, related ROs are composed of different number of delay cells, while in the improved structure, these related ROs possess the same number of delay cells. Moreover, transmission gates are also used to perform delay cell control.

3.3.1 Architecture

Now the key point for the single cell delay measuring structure is to always keep the whole structure balanced. If all of ROs are composed of the same cell numbers, the structure will become completely symmetrical, which may overcome the drawbacks of simple modified RO. An improved structure is shown in Figure 3.8 [31].

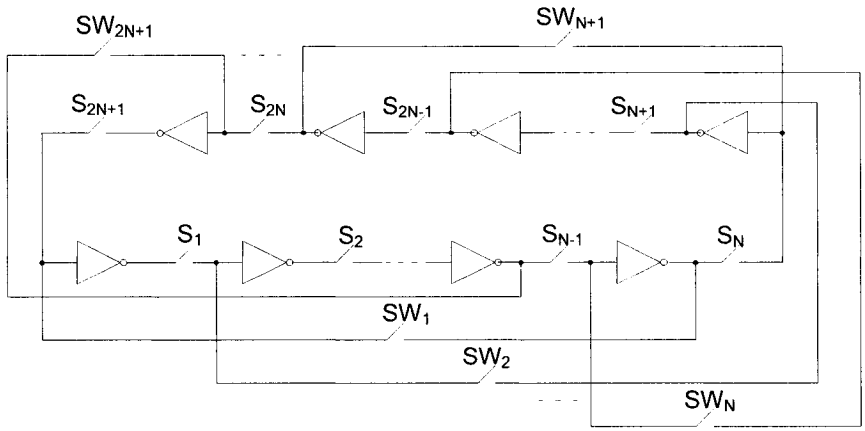


Figure 3.8 Architecture of modified RO [31]

In this structure, we use the (2N+1) inverters, where N is a positive odd number. However these inverters are not connected directly like in normal RO, they are connected to each other through a group of transmission gates denoted as S in Fig.3.8, which act as switches. The S group of switches (S_1 to S_{2N+1}) selects delay cell to be in use for the selected RO. However any ring oscillator is never formed by all of 2N+1 delay cells. Each time, only N delay cells are selected to form a RO. Therefore another group of transmission gates denoted as SW should be used to decide the first and the last cells of each RO. By changing the configurations of S and SW switches, we will get different RO. In this case, the number of RO we can realize is 2N+1.

3.3.2 Principle of the test circuit

Now we explain in detail the principle of the test circuit shown in Fig. 3.8. We start from RO_1, which is composed of the first N cells. In this case, S_1 to S_{N-1} is set to on, while other S switches are set to off so that those inverters, inverter 1 to N, are connected together. Also SW_1 is set to on at the same time, while other SW switches are set to off, so that inverter 1 connects to inverter N and RO_1 is formed. In order to switch to the next RO, S_1 is set to off to remove the first cell of RO_1 and the corresponding switch S_N is set to on to add a new cell to the last cell of RO_1. At the same time, corresponding SW switches are set correctly (turn off SW_1 and turn on SW_2). So far, those cell 2 to cell N+1 form RO_2. The switching goes on until to the last RO, RO_{2N+1} which consists of cell 2N+1 and cell 1 to cell N-1. Hence each RO has N inverters and N transmission gates in this structure, and all of the ROs would have the same number of stages with the same type of components.

The notations S_1, S_2.... S_{2N+1} and SW_1, SW_2 ....SW_{2N+1} refer to the switches as well as their control signals. In this structure, the delay of single cell is not only relied on an inverter, it is also dependent on the delay of the transmission gate connected to the output of the inverter. An inverter and a transmission gate form delay element in a delay cell.

3.3.3 Calculation of single cell delay and delay mismatch

In order to derive single cell delay and delay mismatch from RO periods in the improved test structure, a simple example is given to explain the computation procedure. Assuming N=5, we have eleven delay cells and each RO consists of five delay cells, which is the least cell number possible for RO. So the structure forms eleven ROs all together. According to common formula of RO period calculation, RO period is decided by sum of delays of all delay cells. Hence for RO_1, which consists of cell 1 to cell 5, its period (P1) can be expressed as:

$$P1 = 2(D1 + D2 + D3 + D4 + D5) \tag{3.6}$$

where Di denotes the delay of cell i. Similarly, RO_2 is formed by cell 2 to cell 6, so its period P2 is:

$$P2 = 2(D2 + D3 + D4 + D5 + D6) \tag{3.7}$$

and so on, until the last one, RO_{11}, which is formed by cell 11 and cell 1 to cell 4?

.
.
.

$$P7 = 2(D7 + D8 + D9 = D10 + D11) \tag{3.12}$$

$$P8 = 2(D8 + D9 + D10 + D11 + D1) \tag{3.13}$$

.
.
.

$$P11 = 2(D11 + D1 + D2 + D3 + D4) \tag{3.16}$$

Arranging these eleven equations above as current equation minus the next one, that is (3.6)-(3.7), (3.7)-(3.8)... (3.15)-(3.16), (3.16)-(3.6), we obtain:

$$D1 - D6 = \frac{1}{2}(P1 - P2) \tag{3.17}$$

$$D2 - D7 = \frac{1}{2}(P2 - P3) \tag{3.18}$$

.
.
.

$$D6 - D11 = \frac{1}{2}(P6 - P7) \tag{3.22}$$

$$D7 - D1 = \frac{1}{2}(P7 - P8) \tag{3.23}$$

.
.
.

$$D10 - D4 = \frac{1}{2}(P10 - P11) \tag{3.26}$$

$$D11 - D5 = \frac{1}{2}(P11 - P1) \tag{3.27}$$

To arrange equations (3.17) to (3.27), we start from (3.17) + (3.22), (3.18) + (3.23)... (3.26) + (3.27), and the following equations can be obtained:

$$D1 - D11 = \frac{1}{2}[(P1 - P2) + (P6 - P7)] \tag{3.28}$$

$$D2 - D1 = \frac{1}{2}[(P2 - P3) + (P7 - P8)] \tag{3.29}$$

$$D3 - D2 = \frac{1}{2}[(P3 - P4) + (P8 - P9)] \tag{3.30}$$

$$D4 - D3 = \frac{1}{2}[(P4 - P5) + (P9 - P10)] \tag{3.31}$$

$$D5 - D4 = \frac{1}{2}[(P5 - P6) + (P10 - P11)] \tag{3.32}$$

$$D6 - D5 = \frac{1}{2}[(P6 - P7) + (P11 - P1)] \tag{3.33}$$

Then make (3.17) + (3.23), (3.18) + (3.24) ... until (3.21) + (3.27), other five equations can be obtained:

$$D7 - D6 = \frac{1}{2}[(P1 - P2) + (P7 - P8)] \tag{3.34}$$

$$D8 - D7 = \frac{1}{2}[(P2 - P3) + (P8 - P9)] \tag{3.35}$$

$$D9 - D8 = \frac{1}{2}[(P3 - P4) + (P9 - P10)] \tag{3.36}$$

$$D10 - D9 = \frac{1}{2}[(P4 - P5) + (P10 - P11)] \tag{3.37}$$

$$D11 - D10 = \frac{1}{2}[(P5 - P6) + (P11 - P1)] \tag{3.38}$$

Equations (3.28) to (3.38) give delay difference between adjacent cells. That is cell-to-cell delay mismatch we need to get. It represents intra-die variations directly and accurately.

In order to characterize inter-die variations, single cell delays in more than one circuit have to be known. The following derivation is to get single cell delays, which can be obtained by arranging above equations. First of all, get the delay differences between cell 1 and other cells from (3.28) to (3.38). Using (3.29)+(3.30) get D3-D1; using (3.29)+(3.30)+(3.31) to get D4-D1; using (3.29)+(3.230)+(3.31)+(3.32) to get D5-D1, and so on, then we have:

$$D3 - D1 = \frac{1}{2}[(P2 - P4) + (P7 - P9)] \tag{3.39}$$

$$D4 - D1 = \frac{1}{2}[(P2 - P5) + (P7 - P10)] \tag{3.40}$$

$$D5 - D1 = \frac{1}{2}[(P2 - P6) + (P7 - P11)] \tag{3.41}$$

$$D6 - D1 = \frac{1}{2}(P2 - P1) \tag{3.42}$$

$$D7 - D1 = \frac{1}{2}(P7 - P8) \tag{3.43}$$

$$D8 - D1 = \frac{1}{2}[(P2 - P3) + (P7 - P9)] \tag{3.44}$$

$$D9 - D1 = \frac{1}{2}[(P2 - P4) + (P7 - P10)] \tag{3.45}$$

$$D10 - D1 = \frac{1}{2}[(P2 - P5) + (P7 - P11)] \tag{3.46}$$

$$D11 - D1 = \frac{1}{2}[(P2 - P6) + (P7 - P1)] \tag{3.47}$$

We have already known the difference between cell 2 and cell 1 in equation (3.29). Next, by adding D1-D1=0 to the group of equations above, then adding them up, we will get:

$$\sum_{i=1}^{11} Di - 11D1 = \frac{1}{2}[9(P2+P7) - 2(P1+P3+P4+P5+P6+P8+P9+P10+P11] \quad (3.48)$$

where $\sum_{i=1}^{11} Di$ is the total delay of delay cells (D_{sum}), which can be obtained by adding up the first eleven equations all together, that is (3.6) +... + (3.16). Therefore the total cell delay can be expressed as:

$$D_{sum} = \sum_{i=1}^{11} Di = \frac{1}{10}\sum_{i=1}^{11} P_i \quad (3.49)$$

Then D1can be derived from (3.48) and (3.49):

$$\begin{aligned} D1 &= \frac{1}{11}[\sum_{i=1}^{11} Di + \frac{1}{2}(2P1 - 9P2 + 2P3 + 2P4 + 2P5 + 2P6 - 9P7 \\ &\quad + 2P8 + 2P9 + 2P10 + 2P11)] \quad (3.50) \\ &= \frac{1}{110}[11(P1+P3+P4+P5+P6+P8+P9+P10+P11) - 44(P2+P7)] \end{aligned}$$

Hence, the delay of the first cell is got, and then by using relations between D1 and other cells, which are expressed in (3.28) and (3.38) to (3.46), we can calculate delays of other cells as well. The most important thing in this structure consists in the relationship between the number of delay cells in each RO and the number of RO in the structure. Assuming that the number of delay cells in each RO is N and the total number of RO in the structure is M; it requires that the difference between M and N must be:

1) an even number;

2) no more than N+1.

Otherwise, if the difference is an odd number, no results can be obtained; on the other hand, if the difference is larger than N+1, only part of cell delay and cell-to-cell delay mismatch instead of all can be obtained. In the master thesis, we use M=2N+1 in all of structures.

In fact, all these calculations described above can be carried out automatically in software tools such as EXCEL. Table 3.2 illustrates the procedure of calculations in detail. Here N=7, therefore, there are fifteen RO in the structure.

Table 3.2 Calculation of single cell delay and delay mismatch

Period (ps)		(Pi-Pi+1)/2		Di-Di+1		D1-Di (ps)		Di (ps)	
P1=	1685,91	D1-D8=	1,615	D1-D2=	0,715	D1-D1=	0	D1=	121,06429
P2=	1682,68	D2-D9=	-0,42	D2-D3=	-0,22	D1-D2=	0,715	D2=	120,34929
P3=	1683,52	D3-D10=	-0,71	D3-D4=	1,115	D1-D3=	0,495	D3=	120,56929
P4=	1684,94	D4-D11=	-0,92	D4-D5=	-1,74	D1-D4=	1,61	D4=	119,45429
P5=	1686,78	D5-D12=	0,19	D5-D6=	0,79	D1-D5=	-0,13	D5=	121,19429
P6=	1686,4	D6-D13=	0,145	D6-D7=	0,485	D1-D6=	0,66	D6=	120,40429
P7=	1686,11	D7-D14=	-0,34	D7-D8=	0,47	D1-D7=	1,145	D7=	119,91929
P8=	1686,79	D8-D15=	-1,27	D8-D9=	-1,32	D1-D8=	1,615	D8=	119,44929
P9=	1689,33	D9-D1=	-0,295	D9-D10=	-0,51	D1-D9=	0,295	D9=	120,76929
P10=	1689,92	D10-D2=	0,93	D10-D11=	0,905	D1-D10=	-0,215	D10=	121,27929
P11=	1688,06	D11-D3=	-0,195	D11-D12=	-0,63	D1-D11=	0,69	D11=	120,37429
P12=	1688,45	D12-D4=	1,55	D12-D13=	0,745	D1-D12=	0,06	D12=	121,00429
P13=	1685,35	D13-D5=	-0,935	D13-D14=	0	D1-D13=	0,805	D13=	120,25929
P14=	1687,22	D14-D6=	-0,145	D14-D15=	-0,46	D1-D14=	0,805	D14=	120,25929
P15=	1687,51	D15-D7=	0,8	D15-D1=	-0,345	D1-D15=	0,345	D15=	120,71929
Psum=	25298,97					15D1-Dsum	8,895	Dsum=	1807,0693
Dsum=	1807,0693								

3.4 Delay mismatch analysis

In the proposed test structure, delay mismatch which is obtained by computation method can be used to analyze the effects of both process variations and layout on delay. This master thesis uses the mean value (μ) and standard deviation (σ) of single cell delays to describe cell delays and delay mismatch. For an N-cell test structure, the μ and σ of cell delays are expressed as:

$$\mu = \frac{1}{N}\sum_{i=1}^{N} D_i \tag{4.1}$$

$$\sigma = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(D_i - \mu)^2} \tag{4.2}$$

where D_i is the i^{th} cell delay an N the number of delay cells. The master thesis also uses another parameter, coefficient of variation (CV), to measure the effects of delay mismatch on circuit performance. CV, which is also called relative deviation, is defined as the ratio of the standard deviation to the mean value. This non-unit parameter is expressed as a percentage, which represents the relative standard deviation to mean value. It can be used to compare the effects of delay mismatch on circuit performance between different designs which have different cell delays.

$$CV = \frac{\sigma}{\mu}100\% \tag{4.3}$$

3.5 Validation

3.5.1 Validation of symmetry

In order to verify that the improved modified RO structure is a completely symmetrical structure, transient simulations are performed with 11-cell architecture. All of transistor lengths in the circuit are 0.36um. In the ideal condition (without effect of process variations and unbalance routing capacitance), we've got exactly the same period (1706.45ps) to eleven ROs. That is:

$$P1 = P2 = P3 = ... = P11 = 1706.45ps$$

Using our method to calculate cell delays, we've got uniform delay to these eleven cells.

$$D1 = D2 = D3 = ...D11 = 170.645ps$$

Figure 3.9 shows the part of transient simulation results for the 11-cell structure (only seven RO results are displayed in the figure).

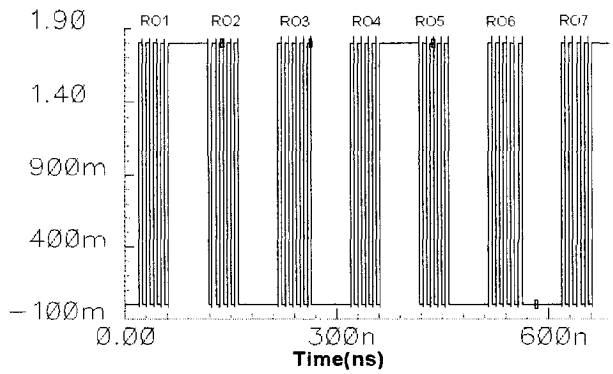


Figure 3.9 Transient simulation results for 11-cell structure

This result indicates that in the ideal situation, all delay cells in this circuit have exactly the same delay. If any delay mismatch will be measured with this circuit, the mismatch must be caused by unbalanced load capacitance in layout and process variations in both device and interconnect.

3.5.2 Validation of computation

To validate the single cell delay computation, simulation has been carried out to compare cell delays obtained by simulator to that obtained by our method. Here we use a 15-cell structure; therefore each RO is composed by 7 delay cells. In the 15-cell structure, all of transistors are assigned different gate lengths from one to others, so that each cell would have different delays. First, we get periods of 15 RO from simulator, and then derive cell delays of 15 delay cells with our method. Next, on the waveform of simulation result, we use markers to read cell delays directly. From simulation, we get waveforms of both input and output, shown in Figure 3.10. We put trace markers on four simulated points. Delay between rising of input and falling of output is

denoted as D_{rf}, and delay between falling of input and rising of output is denoted as D_{fr}. The average of D_{rf} and D_{fr} is the cell delay.

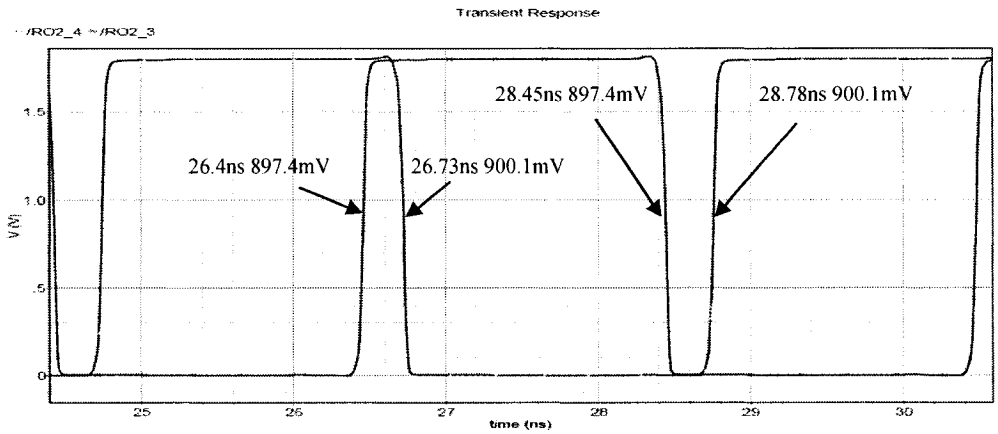


Figure 3.10 Transient simulation result of cell delay

Then we compared 15 cell delays between these two methods. Simulator evaluates these delays directly in waveforms. Figure 3.11 shows cell delays obtained by these two methods.

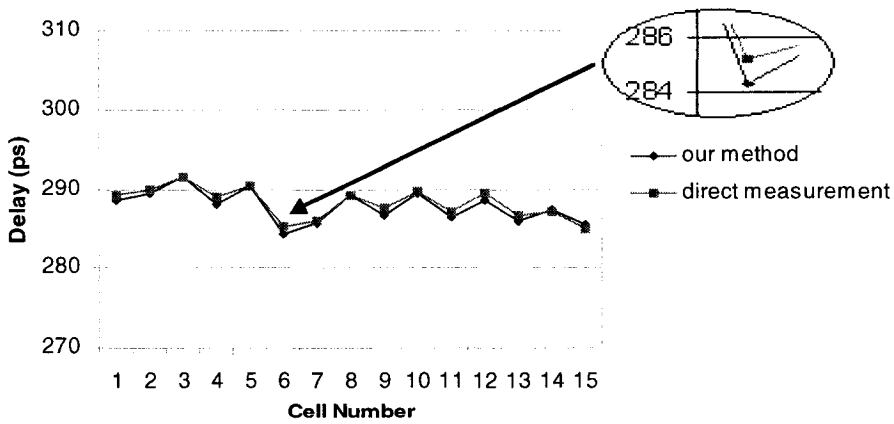


Figure 3.11 Validation of proposed delay computation method

From the figure we notice that two methods get almost same results. The maximum difference is in cell 6 which is 1 ps or so. This difference is due to resolution. For example, in direct

simulation method, we should take four points to put markers for each cell, input rising and output falling points, input falling and output rising points, however it's impossible to locate markers at the same voltage levels, which causes errors.

Overall, cell delay obtained by our computation method is the same as by simulation. Hence the proposed test architecture with computation method is applicable to evaluate single cell delay and delay mismatch in RO.

3.6 Digital control circuit

3.6.1 Introduction

In order to characterize cell delay mismatch in different size devices and different cell numbers, we designed a test chip where three sets of modified ROs are put. First series, RO1, is a 31-cell structure with minimum transistor sizes (NMOS W/L=0.5μm/0.18μm, PMOS W/L=2μm/0.18μm), second series, RO2, is a 15-cell structure with bigger sizes (NMOS W/L=2μm/0.36μm, PMOS W/L=8μm/0.36μm) and the third one, RO3, is 15-cell structure, with transistor sizes as NMOS W/L=2μm/0.18μm, PMOS W/L=8μm/0.18μm. Figure 3.12 displays the architecture of ROs under test and their control diagram.

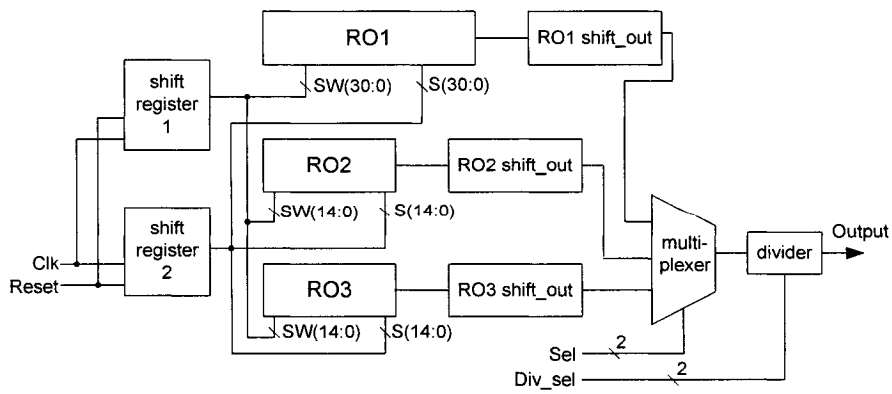


Figure 3.12 Block diagram of test chip

The digital control circuit can be divided into two parts: the first part produces control signals (S(30:0) and SW(30:0)) to control switches. They are indicated as shift register 1 and shift register 2 in Fig. 3.12. The second part is used to control the outputs of the three series of ROs, including three shift_out circuits, multiplexer and divider as shown in the block diagram.

3.6.2 Shift registers

In the first part of the control circuit, two feedback shift registers (FSR) are used to generate SW and S control signals to control TG. The register 1 generates control signals to control SW TG and the register 2 generates signals to control S TG. If 31-cell RO1 series is selected, they are 31-bit register; if 15-cell RO2 or RO3 series is selected, they turn to 15-bit ones. The difference between the two registers consists in quite different initializations.

When the two registers are set to 31-bit registers, the values of SW30 and S30 feed back to SW0 and S0 in shift operation. Whenever the register is reset, the initial value is set to each D-flip-flop (DFF). The initial value of register 1 is: SW(30:0) = "10...0", which means only SW30 is set to '1' while other bits are set to '0'. Hence when the first "Clk" signal comes, this '1' shifts to the first DFF, which makes the first SW TG on. In the register 2, the initial values of the first 13 bits (from S0 to S12) and the last bit (S30) are set to '1' and other bits are set to '0'. Hence when the first "Clk" signal comes, the first 14 bits (S(13:0)) are set to '1' which selects the first 15 delay cells. When the two registers are set to 15-bit registers, SW14 and S14 feed their values back to SW0 and S0 respectively in shift operation. Values of SW(30:15) and S(30:15) always remain '0'. In the register 1, the initial value of SW(14:0) is "100...0", which ensures SW0 is set to '1' when the firs "Clk" comes. In the register 2, the initial values of the first 6 bits (from S0 to S4) and the last available bit (S14) are set to '1' and initial values of other available bits (from S5 to S13) are set to '0', which ensures the first 6 bits are set to '1' at the first shift operation.

Figure 3.13shows diagram of shift register 1. 31 D-flip-flops give rise to control signals to SW0-SW30. The bit control is realized by 2-bit control signal "Sel", by which three multiplexers are controlled. If "Sel" is "00", multiplexer 1 selects output of FF30 to feedback to the input data of FF0, so that this is a 31-bit shift register. Multiplexer 2 makes all flip-flops connect to normal "Reset" (from external reset circuit). Otherwise multiplexer 1 chooses the output of FF14 (SW14) as a feedback, at the same time, multiplexer 2 resets FF15 to FF30 to be low. In this case, the register has only 15 available bits. Multiplexer 3 sets up different initial values corresponding to bit control. In RO series under test, only one RO will be selected at one time, which requires only one SW to be high while others to be low.

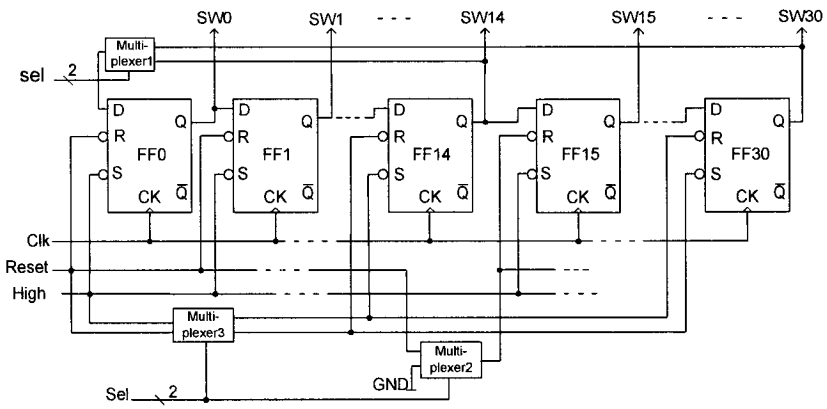


Figure 3.13 Block diagram of shift register 1

As shown in the Figure 3.13, if the register is configured as a 31-bit register, in FF30, R terminal connects to "High", and S terminal connects to normal "Reset", which ensures that whenever the register is reset, FF30 will be set to '1', this '1' will shift to FF0 when the first "Clk" coming and will shift this '1' to the next bit whenever a "Clk" coming. The setting of FF14, on the other hand, is exactly opposite to the situation in FF30. That would mean, if the register is configured as 15-bit register, FF14 is set to '1' when circuit is reset and this '1' will shift in the 15 bits. Table 3.3

shows configuration of register 1. Where "R" and "S" indicate Reset and Set terminals in DFF, and "Reset" represents the external reset signal.

Table 3.3 Configuration of shift register 1

	FF0-FF13	FF14		FF15-FF29		FF30	
Sel		**00**	**others**	**00**	**others**	**00**	**others**
R	Reset	Reset	1	Reset	0	1	0
S	1	1	Reset	1	1	Reset	1

The configuration of the first 14 DFF (from FF0 to FF13) are identical whether the register is set to 31-bit or 15-bit. When the register is set to 31-bit (Sel= "00"), the configuration of other 16 DFF (from FF14 to FF29) are the same as the first 14 ones and FF30 is set when the register is reset. When the register is set to 15-bit (Sel= "others"), the "R" terminals of last 16 DFF (from FF15 to FF30) are set to '0', which means these 16 DFF are not available in this case and the 15th DFF (FF14) is set when the register is reset. Simulation result for both 31-bit and 15-bit of registers 1 are shown in Figure 3.14 and Figure 3.15, where rst_an is reset signal. The latter one displays that value of '1' is only shift in the first fifteen bits, SW15 to SW30 always keep '0'.

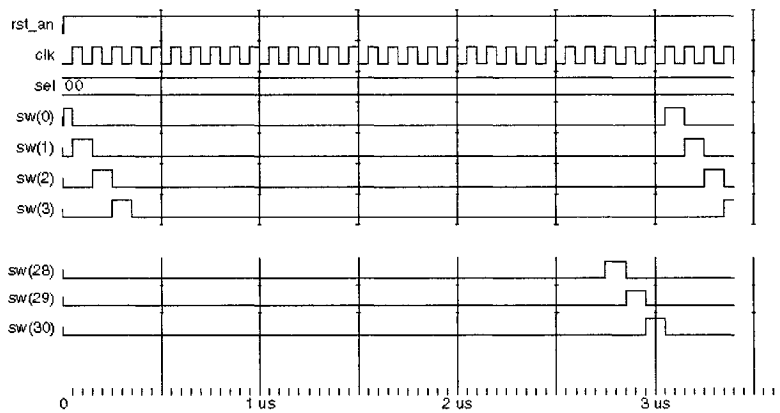


Figure 3.14 Timing diagram of 31-bit shift register 1

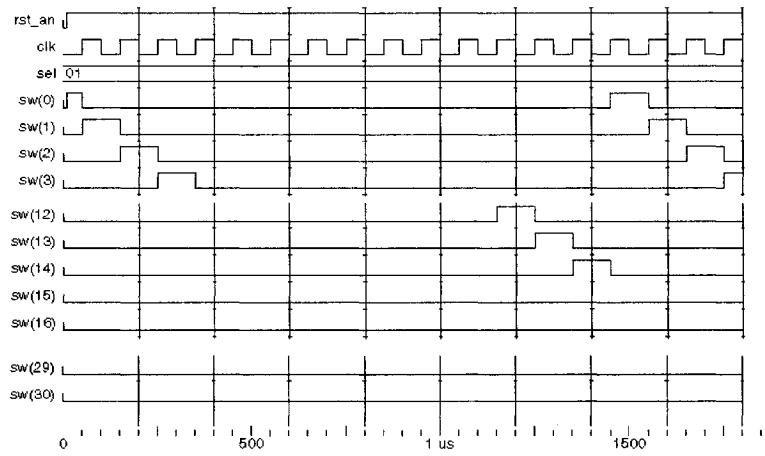


Figure 3.15 Timing diagram of 15-bit shift register 1

Shift register 2, produces S0 to S30, which is similar to shift register 1, but their initial values are different. Shift register 2 generates signals deciding which cell is selected. If RO1 series is selected, then each RO is composed by 15 cells, which requires 14 TG to be on, hence 14 bits in the register 2 should be at '1'at the same time; otherwise, RO2 or RO3 is selected, each RO is formed by 7 delay cells, which requires that six bits of the register should generate '1' at the same time. The block diagram of shift register 2 is shown in Figure 3.16. The register 2 also consists of 31 DFF. If "Sel" is set to "00", 31-cell structure will be selected, 14 DFF will produce '1' at the same time. Otherwise, 15-cell structure is selected, only six DFF give rise to '1' at the same time.

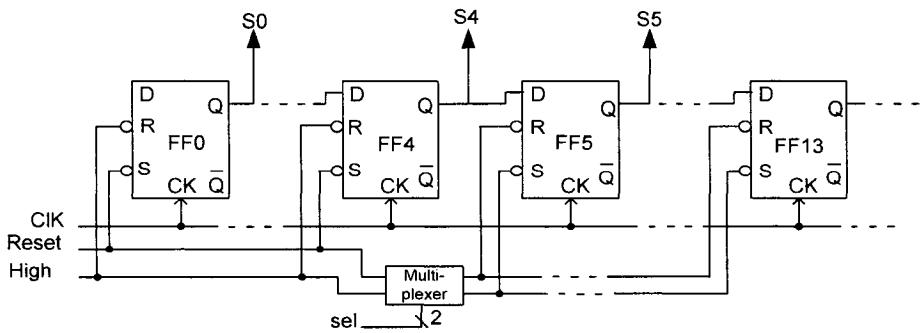


Figure 3.16 Block diagram of shift register 2

Table 3.4 illustrates the configuration of shift register 2 configuration. The initial value of the first 5 bits (FF0 to FF4) is '1' in reset state whether the register is set to 31-bit or 15-bit. The initial value of 14th bit (FF13), however, is always set to '0'. When the register is set to 31-bit register, that is Sel= "00", the initial values of FF5 to FF12 and FF30 are set to '1', and the values of FF14 to FF29 are set to '0'. Therefore there are always six continuous bits with the value of '1' in the register. On the other hand, when Sel= "others", FF5 to FF13 are set to '0' in the reset state, the last available bit (FF14) is set to '1'. When the first 'Clk' coming, the register right shift 1 bit , therefore, the first 6 bits (FF0 to FF5) turn to be '1', remaining other bits to '0'. Other bits (FF15 to FF30) remain to '0', and never take part in the shift operation.

Table 3.4 Configuration of shift register 2

	FF0-FF4	**FF5-FF12**		**FF13**	**FF14**		**FF15-FF29**		**FF30**	
Sel		00	others		00	others	00	others	00	others
R	1	1	Reset	Reset	Reset	1	Reset	0	1	0
S	Reset	Reset	1	1	1	Reset	1	1	Reset	1

Figure 3.17 and Figure 3.18 are simulation result for 31-bit and 15-bit S shift register respectively. In 15-bit shift register 2, FF15 to FF30 are always "0".

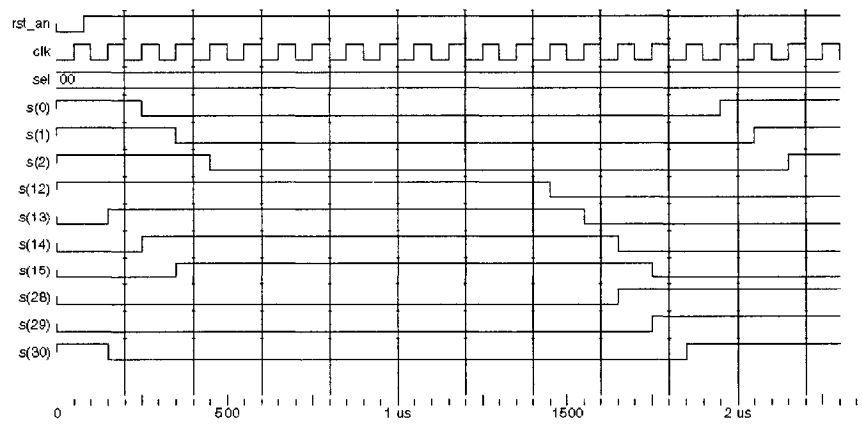


Figure 3.17 Timing diagram of 31-bit shift register 2

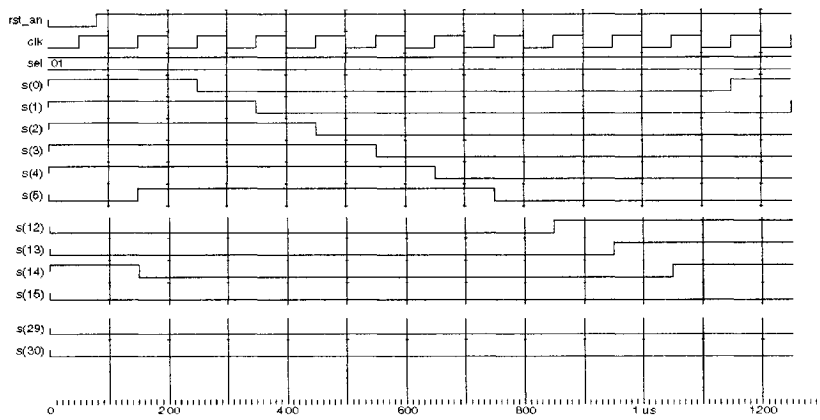


Figure 3.18 Timing diagram of 15-bit shift register 2

3.6.3 Multiplexer

In the second part of digital circuit, RO1, RO2 and RO3 shift_out circuit in Figure 3.12 are in fact three multiplexers. They shift RO signals out synchronized with SW signals. For example, when 31-cell series of RO1 is selected by "Sel" signal, we have 31 ROs: RO1_0 to RO1_30. The signal of RO1_0 will be sent to Out1 only if the transmission gate SW0 is closed. Similarly, for any RO, the signal of RO1_n will be sent to Out1 only if SWn is closed. They are the same cases as in RO2 and RO3. Diagram of shift_out circuits are displayed in Figure 3.19.

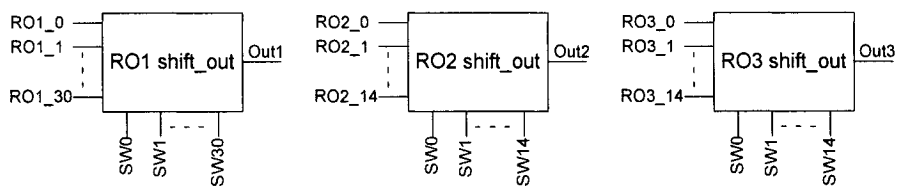


Figure 3.19 Block diagram of shift _out circuit for three series of RO

Figure 3.20 displays the port level circuit of RO_1 shift_out circuit. It is composed by 31 AND gates and 31 OR gates.

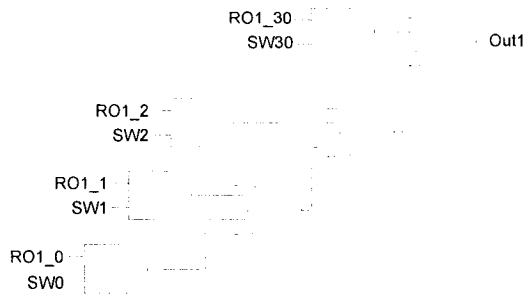


Figure 3.20 Gate level of RO1 shift_out circuit

Three series of ring oscillators RO_1, RO_2 and RO_3 are selected by setting up control signal "sel" as "00", "01" and "10" respectively.

Since we use only one shift_out circuit in one series for all outputs of ROs, the different interconnect lengths in the layout may cause different propagation delay for each RO signals, but it does not affect the ROs' frequencies, it only produces different phase shifts for every RO.

We use another multiplexer to select which series of RO to be measured. As shown in Fig. 3.20, the multiplexer is controlled by "Sel". If Sel is set to "00", Data_in select Out1 as output of the multiplexer; if Sel is set to "01", Data_in will take the signal from Out2, and it will take signal from Out3 when control signal "sel" is set to "10".

3.6.4 Divider

In order to perform measurement by general equipment, we use frequency divider to decrease frequencies of output. Figure 3.21 shows divider block diagram. Frequency range of those three series of RO is from 150MHz to 500MHz, a multiplexer controlled by 2-bit signal "Div" is used to select decreasing times as 2, 4, 8, and 16 respectively, therefore it could decrease the fastest RO below 50MHz. Here, Data_in from the multiplexer described in section 3.4.3 is used as

synchronized signal in divider, its frequency is decreased and turn to be final output to be measured.

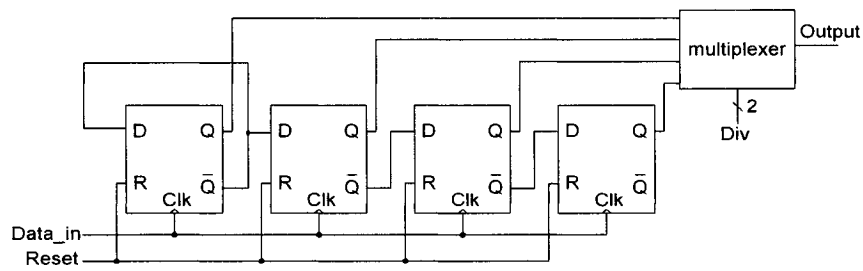


Figure 3.21 Divider Circuit

3.7 Conclusion

This chapter gives detail descriptions to test circuit for single cell delay measurement, which are based on modified RO. Simple modified RO test structure is not symmetrical structure, from which we cannot get satisfied information about delay mismatch due to process variations. Proposed modified RO test structure is complete symmetrical one, which makes it possible to characterize delay mismatch due to process variations. The computation results are almost the same as the simulation results, which validate the computation method. Two parts of digital control circuits ensure three series of modified RO to work properly and the final signals to be measured by general equipment easily.

CHAPTER 4

DESIGN IMPLEMENTATION

Chapter 3 describes the proposed test structure to measure single cell delay by means of modified ring oscillators, including RO structure and its digital control circuit. This chapter will outline design implementation related to both design and layout, including TG effects, layout implementation and delay mismatch investigation in the test structure through large amount of post-layout simulations. In the meantime CAD tools aiding the design (schematic and layout) are introduced.

4.1 Design consideration

Comparing with the normal RO, this test structure uses TG to perform control to delay cells. In order to verify that the delay mismatch in the proposed test structure can reflect the mismatch in a normal RO and that the computation technique is enough accurate, this section will investigate the TG effects in the test structure; it will also explain the importance of buffers on the output stage of RO.

4.1.1 Comparing delay mismatch between conventional RO and modified RO

In many application circuits, RO is consisted of odd number of delay cells; each cell has an inverter only. However, in the modified RO structure presented in the Chapter 3, each delay cell is formed by an inverter and a conducting TG connecting to neighbor inverters (S switches in Fig. 3.8). It is important to find the relationship of delay mismatch between normal RO and modified RO. If this relationship exists, delay mismatch obtained with the proposed structure can represent the mismatch situation in normal RO, which is mostly used in application circuits. In order to

reveal this relationship, simulations were performed for both 15-cell modified RO structure and 7-cell normal RO individually. The same transistor sizes were used for both inverters and TG in all simulations described in this subsection. Also, the same transistor length deviations were applied to both normal RO and modified RO respectively. Here standard deviations were set up to transistor length as 1.8 nm, 3.6 nm and 9 nm. For 15-cell modified RO, Monte Carlo simulation was performed to get periods of the 15 RO, then single cell delays and delay mismatch were obtained by using computation method presented in Chapter 3. For 7-cell normal RO, using transient analysis, single cell delays are obtained directly from simulation. Then the mean values (μ) and standard deviation (σ) of delays were used to compare cell delays and delay mismatch in the two RO structures and CV was used to compare the effects of parameter variations on delay in these two circuits.

Table 4.1 illustrates simulation results for both modified RO and normal RO structures, where all transistor length was 0,24 μm, transistor width was 0.5um for NMOS and 2um for PMOS. With the increasing of the transistor length deviation, cell delays in both ROs increase a little bit, but not significantly; the increasing of delay mismatch is almost proportional to transistor length fluctuation; hence values of CV increase also. In this table, the ratio of CV in modified RO to normal RO is almost a constant value no matter what the length deviation is.

Table 4.1 Delay mismatch comparison (L=0.24um)

Length Deviation (nm)	**Modified RO**			**Normal RO**			CV_1/CV_2
	μ_1(ps)	σ_1 (ps)	CV_1 (%)	μ_2 (ps)	σ_2 (ps)	CV_2 (%)	
1.8	170.6	3.3	1.93%	54.8	0.56	1.02%	1.89
3.6	170.9	6.4	3.74%	55	1.1	2.00%	1.87
9	171.6	16.3	9.50%	55.1	2.8	5.08%	1.87

Then the next group of simulation was performed for the two structures, following the same procedure as description above. The only difference is that the transistor length was doubled to 0.48μm. Table 4.2 displays the result with the larger transistors.

The overall delay mismatch in Table 4.2 is smaller than that shown in

Table 4.1 because of using larger transistor size. In this table, the ratios of CV1/CV2 are much close even with different transistor length deviation; furthermore they are almost same as the ratios in

Table 4.1.

Table 4.2 Delay mismatch comparison (L=0.48um)

Length Deviation (nm)	Modified RO			Normal RO			CV_1/CV_2
	μ_1 (ps)	σ_1 (ps)	CV_1 (%)	μ_2 (ps)	σ_2 (ps)	CV_2 (%)	
1.8	423.5	4.4	1.04	145.2	0.8	0.55	1.89
3.6	423.8	8.1	1.91	145.4	1.5	1.03	1.85
9	424.8	20.8	4.90	145.9	4.0	2.7	1.81

From these simulation results, we can conclude that the relative delay deviations obtained with the proposed test circuit are proportional to those in a normal RO regardless of the transistor sizes and length deviations. Thus delay mismatch in the test structure can represent the mismatch situation in normal RO, and the test structure can be used to characterize intra-die process variations in normal RO as well. Delay mismatch in normal RO can also be deduced from the measurement results with the modified RO test structure. By measuring a number of test chips, inter-die variations can also be evaluated.

4.1.2 Effects of "off" TG

It should be mentioned that these different delays are obtained based on the assumption that only an inverter and the TG connecting between the current inverter and its next inverter are considered as a delay cell, and delays of only selected inverters and conducting TG are taken into

account in the formula of computation method in Chapter 3. As a matter of fact, all of the "off" transmission gates (OTG) connecting to the selected inverters also influence the actual period of the RO. The equivalent resistances of OTG are considered as infinite, while their diffusion capacitances (junction capacitances) still exist as load capacitances to output of inverters [2] [12]. All these devices influence the actual period of the RO. If we consider the effect of OTG, the relation between two RO periods becomes more complicated.

Taking an 11-cell structure as an example, all of the components influencing the period of the 1st RO are shown in Figure 4.1. Among them, all OTG locating outside RO in the figure (e.g. $SW_2 \ldots SW_5$) would affect delay cells but were not considered in the computation method.

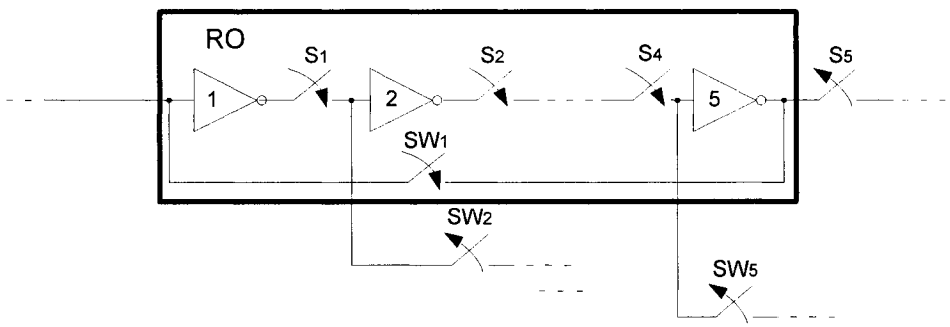
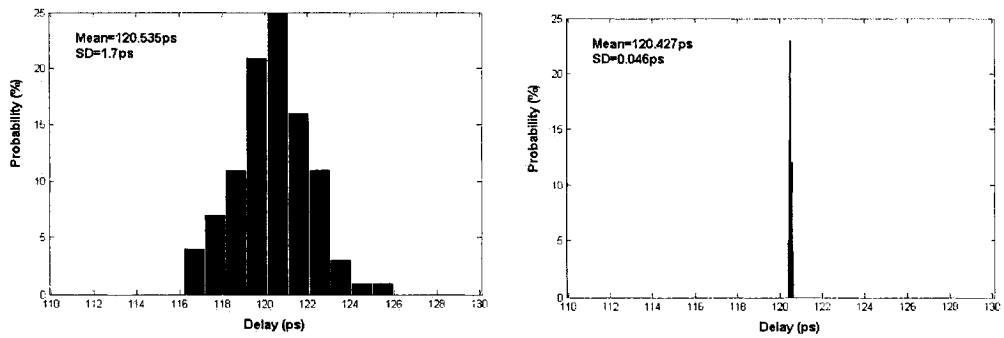


Figure 4.1 Components influencing the 1st RO period in 11-cell structure

In the ideal situation, the effect of OTG should be equal for each RO; therefore their effects would be cancelled when calculating RO period differences. However due to process variations, the effects of OTG would be different from one RO to the other. In order to analyze the effects of OTG, Monte Carlo simulations have been carried out with an 11-cell structure, using minimum transistor sizes for both inverters and switches. For statistical simulations, we only setup variations in transistor length, since it is the main source of delay mismatch. We assume that these length variations are following a normal (Gaussian) distribution and the same standard deviation (1.8 nm) of the transistor lengths is used for both delay cells and OTG. The distribution

of cell delays caused by transistor length fluctuation in the delay cells and OTG are depicted in Figure 4.2 a) and Figure 4.2 b) respectively.



a) b)

Figure 4.2 Delay mismatch due to transistor length fluctuation; a) in delay cells; b) in OTG

From the figure, we can see that the maximum delay deviation induced by transistor length variation in delay cells is as large as 1,7 ps, whereas it is only 0,046 ps by transistor length variations in OTG. That means that under certain process variation, device parameter variation in delay cells is the dominant factor that cause delay mismatch in the circuit. Although OTG connecting to selected inverters may influence RO period, they cause little delay mismatch due to process variations. Hence the effect of OTG could be cancelled when calculating period differences in the computation procedure. Thus the computation method presented is well applicable to single cell delay measurement and delay mismatch characterization. Therefore, the delay mismatch obtained using this test structure mainly represents delay variations caused by delay cells, which is in fact what we are interested in.

4.1.3 Effect of buffer on the RO output

The output of each delay cell is first connected to a buffer and then to a multiplexer as illustrated in

Figure 4.3. This buffer is put on the output of RO, which buffers the oscillator signals to the outside world, so that the frequency of RO would not be influenced by outside circuit, e.g. by extraneous loading on the ring oscillator.

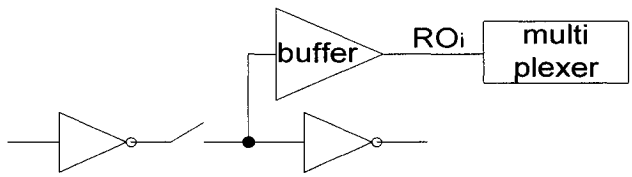


Figure 4.3 A buffer used on the output of each delay cell

Without this buffer, a long interconnection tapping a node on the ring oscillator would create additional loading on the RO. Another reason using this extra buffer is that without the buffer, the totally different distances of interconnection in the multiplexer would also cause delay differences between oscillators in the structure, which result in error measurement. The obtained delay mismatch is not only caused by process variations in the RO but also caused by unbalanced interconnect between RO and other circuits. If the buffer is used, the unbalanced interconnect in other circuits may lead to signal delays only, but it may not influence the periods of RO. Although the buffer may introduce a slight delay to RO, however it has little effect on delay mismatch compared to the variations in inverters.

4.1.4 Simulation results

This section demonstrates delay mismatch analysis method utilizing the proposed test structure. The goal of simulations in this section is not to predict the actual delays and delay mismatch

inside die, but to estimate delay mismatch and its trends under different parameter fluctuations and different transistor sizes. Delay mismatch discussed in this section were only due to process variations on transistor parameters. Layout effects were not considered. The given parameter variation doesn't represent the value of variation in the actual process.

First, a group of simulations were performed for 15-cell RO structure. In this circuit, NMOS transistor size is W/L=2um/0.36um, while PMOS size is W/L=8um/0.36um. Normal distribution to gate length was setup with deviation of 1.8nm, 3.6nm and 9nm respectively. Monte Carlo analysis gave rise to three groups of random values following the different deviations. If the transistor length of inverter is defined as a parameter as Linv, transistor length of SW switch is defined as Lsw and length of S switch is Ls, one of model files using for Monte Carlo analysis states is following:

```
simulator lang=spectre
library monteclib
section param
parameters Linv=0.36e-6
parameters Lsw=0.36e-6
parameters Ls=0.36e-6
endsection param
section stats
statistics {
        mismatch {
                vary Linv   dist=gauss std=1.8e-9
                vary Lsw    dist=gauss std=1.8e-9
                vary Ls     dist=gauss std=1.8e-9
                }
}
endsection stats
endlibrary monteclib
```

This model file defines Spectre as the used simulator; transistor length of inverter, S and SW TG as variable parameters, whose nominal values are 0.36um; their variations are all Gaussian distribution; and their standard deviations are 1.8nm.

Single cell delay can be calculated by simulating periods of all fifteen RO. Figure 4.4 illustrates cell delays under different length variations.

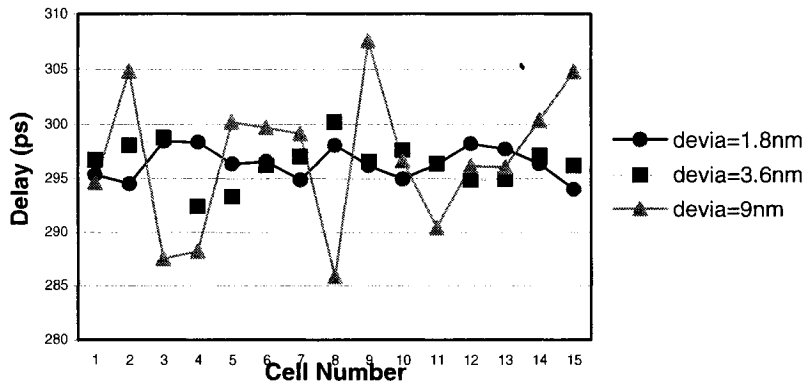


Figure 4.4 Single cell delay variation due to gate length fluctuation

Delay deviations (standard deviation of single cell delays) under 1.8nm, 3.6nm and 9nm length variations are 1.82ps, 3.6ps and 6.28ps. Obviously, when length variation is small, delay mismatch is almost linear to length variations; with the length fluctuation increasing, this linear relation is not valid.

Another group of simulation is carried out with different transistor sizes. We also use 15-cell structure, with transistor length 0.18um, 0.36um and 0.9um respectively. Gate length deviation is setup as 1.8nm, 3.6nm, 9nm and 18nm to each circuit, and cell delays are deduced by following the automatic calculating procedure. Since absolute cell delays are different with different transistor sizes, we use CV to compare the effect of delay mismatch. Table 4.3 gives CV for different transistor sizes and different length deviations, from which some conclusions are made:

1) If only length effects are considered, assuming no deviations in other parameters, the delay mismatch CV is not linear to the gate length fluctuations. The delay mismatch increases not as fast as the increasing of length fluctuation

2) The effect of length fluctuations on delay mismatch is inversely proportional to device size; smaller transistors are more susceptible to process variations.

Table 4.3 Delay mismatch CV for different transistor sizes and different length deviations

Length Deviation	Transistor Length (μm)		
	0.18	*0.36*	*0.9*
1.8nm	1.02%	0.62%	0.28%
3.6nm	1.8%	1.06%	0.5%
9nm	3.53%	2.12%	0.92%
18nm	7.08%	4.26	2.03%

4.2 Design flow

The overall design can be divided into two parts: RO structure and digital control circuit. The design flow is shown in Figure 4.5. In RO structure realization, CADENCE IC design tools are used to create all of schematic, layout, extract netlists and perform simulations. Analog Design Environment is used to compose schematic; Virtuoso is used to draw layout. Spectre and SpectreS are the simulators that carry out transient and Monte Carlo simulations. In digital control circuit realization, VHDL is used to complete RTL coding, which is compiled and synthesized by Design Analyzer of Synopsis. ModelSim5.8 is used to perform behavior simulation and timing analysis. The layout of the digital circuit is extracted in Encounter and then is imported to Cadence. After the layout of the two parts completed, they are combined together in one chip. For design rules checking (DRC), DivaDRC library is used for local check. However, at Canadian Microelectronic Corporation (CMC), CalibreDRC library is used to check design rules.

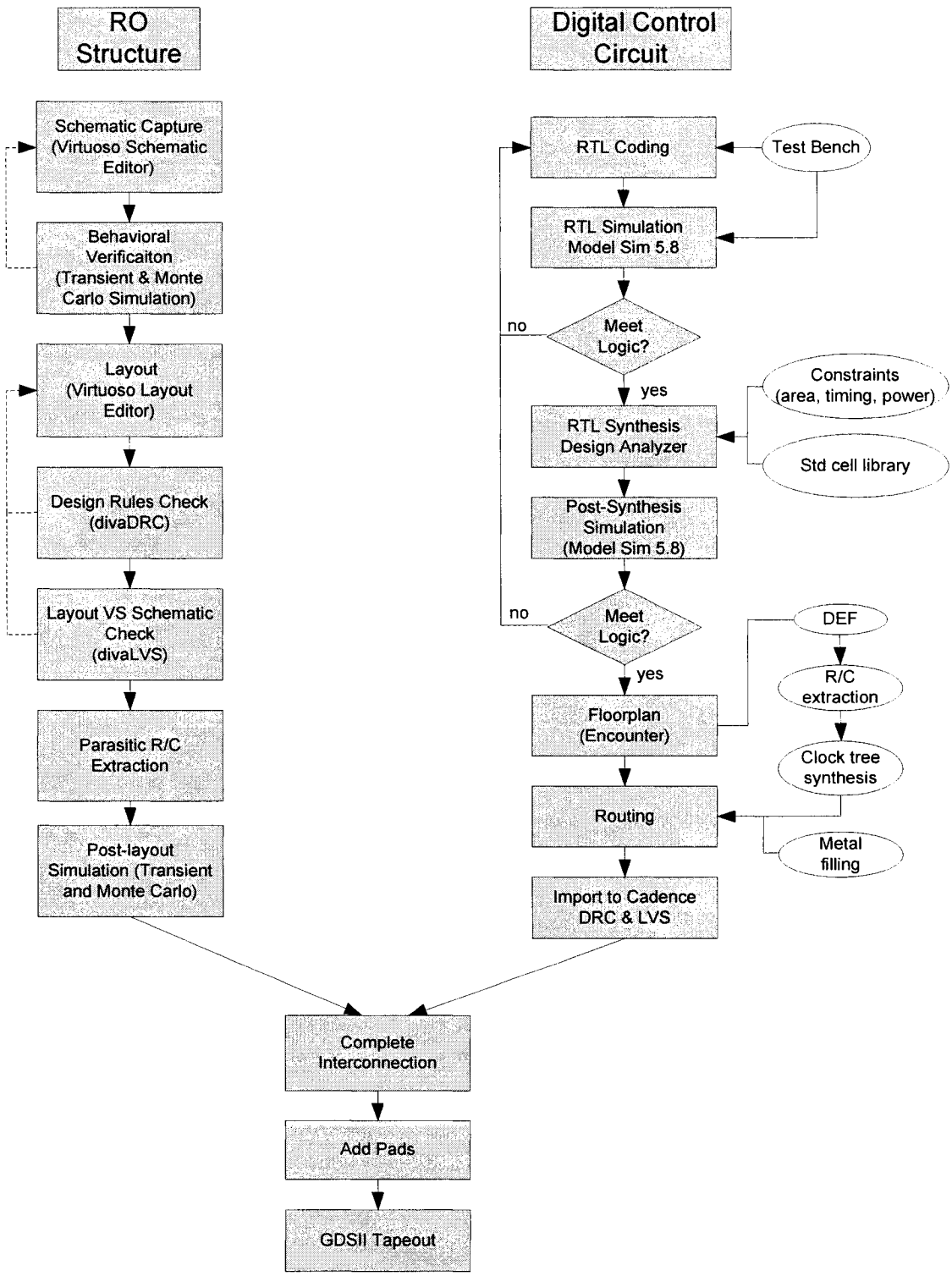


Figure 4.5 Design flow of test chip

4.3 RO layout structures

In the test chip, there are three series of RO. The first RO is 31-cell structure with minimum transistor length and width for NMOS. The second one is 15-cell structure with twice minimum transistor length and twice minimum width for NMOS. The last one is also 15-cell structure but with minimum length and twice minimum width for NMOS. All these RO have the same transistor length for both PMOS and NMOS, the widths of PMOS transistors are four times as that of NMOS.

Simulation results in Chapter 3 revealed that the test structure is completely symmetrical. However, after layout, the unbalanced interconnect wires may induce inevitable delay mismatch between delay cells. In application circuit, we always expect the structure which has the smallest delay mismatch due to layout. Moreover, we also expect the parasitic capacitance of interconnect could be small, because this smaller capacitance will in turn cause less delay mismatch due to interconnects. All of the following layouts are designed for the 15-cell architecture with minimum transistor sizes. This section presents three layout structures, from which we select one option with minimum delay mismatch to implement our test chip.

4.3.1 Type-I layout structure

Considering effects of spatial variation in intra-die process variations, type-I layout structure is designed as shown in Figure 4.6, in which the cell-to-cell delay mismatch is able to represent this spatial variation. In this structure, all 15 inverters and 30 TG are put on one line. Only the output buffers are put on another line. This design may lead to long interconnect. The layout is shown in Figure 4.7. This layout structure forms a dense interconnect area in the bottom of device, which may produce large and complex parasitic capacitance influencing cell delay. This complex and unequal capacitance causes delay mismatch between cells.

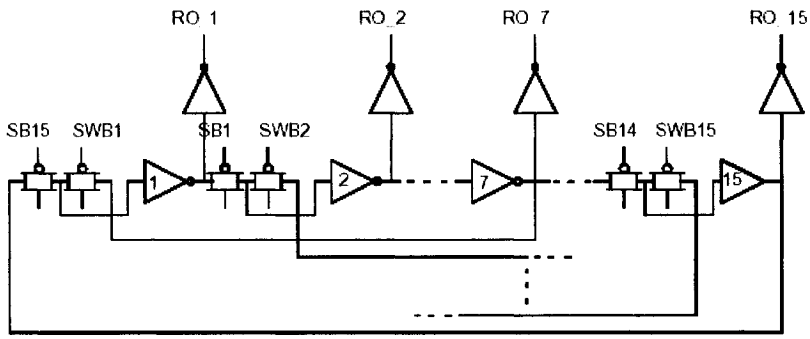


Figure 4.6 Component placement in type-I layout structure

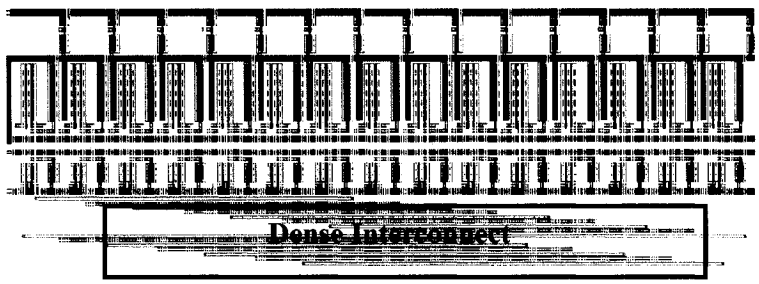


Figure 4.7 Layout of type-I Structure

4.3.2 Type-II layout structure

In order to shorten interconnects, we design another structure, type-II layout structure, in which inverters and TG are placed in two lines (as shown in Figure 4.8).

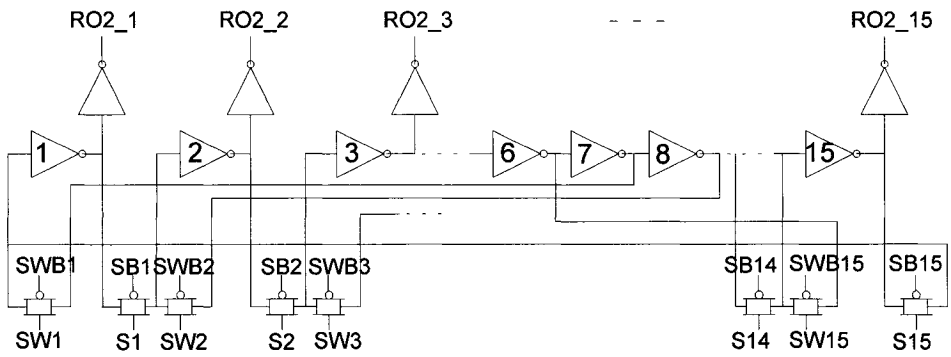


Figure 4.8 Component placement in type-II layout structure

The layout of this structure is shown in Figure 4.9. The dense interconnect area locates between inverters and TG. Comparing to type-I structure, interconnect wires are shorter, but they present higher density and more complicated. Interconnect in two lines include not only wires between inverters and SW TG but also between inverters and S TG.

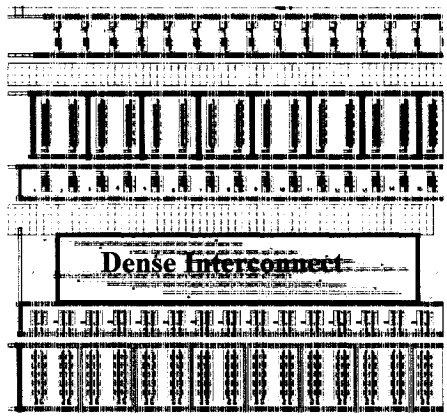


Figure 4.9 Layout of type-II structure

4.3.3 Type-III layout structure

Considering layout structure of ring oscillator in many applications, another layout structure (structure III) has also been designed which is displayed in Figure 4.10 the inverters are placed in two lines surrounded by transmission gates that are located inside the ring. Figure 4.11 shows the layout of this structure. This structure would form two areas of dense interconnect.

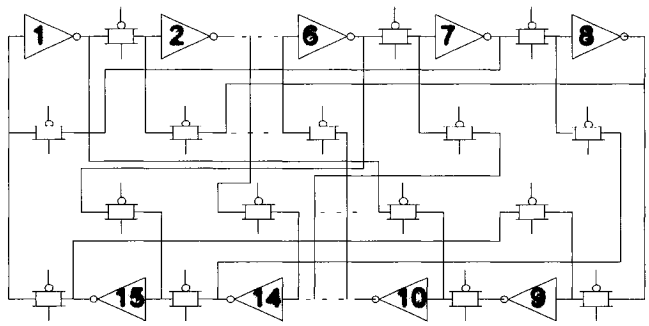


Figure 4.10 Component placement in type-III layout structure

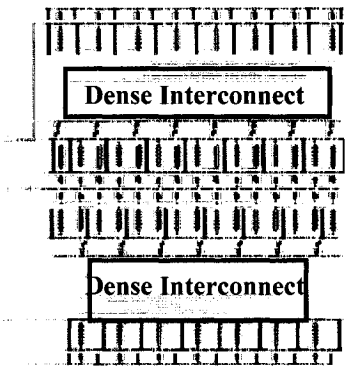


Figure 4.11 Layout of type-III structure

Simulation results for these three layout structures will be analyzed in section 4.6. The structure with the smallest delay mismatch will be selected to be used to carry out further simulations.

4.3.4 RO Power Grid

Power supply is a very important issue in RO structure layout. One reason is that power supply voltage is directly related to the frequency of RO, in order to measure reliable frequency (period) of RO, it is mandatory that power supply voltage for each RO in the same series must be as equal as possible. Another consideration for power supply is the very common sense, that is designer should make effort to reduce power consumption of circuit. These two considerations are related to metal wire in power grid.

Physical wires in integrated circuits contain parasitic resistance and capacitance associated with them and even exhibits inductive characteristics at very high frequency. The most relevant parasitic component characteristic to the power grid issue is resistance. The power consumption by wire resistance is expected to be as small as possible in design. It is well known that wire resistance relates to its dimension and its metal resistivity, which is fixed for a certain metal. The resistance is proportional to its length, while it is inversely proportional to its width.

For one series of structure, for example, the first series-RO1, thirty-one delay elements are supplied by the same power. Because those elements are placed in a row instead of a column, it is impossible to distribute a completely balanced power network. In order to reduce the unbalance effect, the power supply pads are put as center of the RO as possible.

On the other hand, considering power consumption, lower resistivity metal layers are considered. Among the metal layers in the used layout technique, the lowest layers, metal 1 and metal 2, have relatively lower resistivity. Hence metal 1 and metal 2 are used to be power supply wires of RO in the test chip. The distance of interconnects between RO and power supply pads should be as short as possible, because this distance distributes resistance through the power supply wire. When a RO works, it consume amount of current from power supply, resulting in voltage drops (VR). Therefore actual power supplying to RO may be lower than actual power supply applied. Figure 4.12 shows placing power supply pads close to power wire of RO.

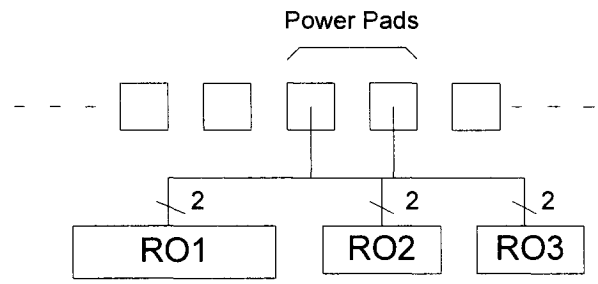


Figure 4.12 Assigning power supply pads close to RO power wires

4.3.5 Antenna Rules in Layout

Since this design use TSMC CMOS0.18um technology, the layout must respect the design rules for this technology which specify geometry rules, antenna rules, metal density rules, etc. Here the antenna rules are described in detail because this is a typical violation in this design.

The "Antenna Rules" deal with process induced gate oxide damage caused when exposed polysilicon and metal structures [5]. It is also called "Process-Induced Damage Rules". When a

metal wire connecting to a transistor gate is plasma-etched, it can charge up to a voltage sufficient to break down thin gate oxides. The metal can be connected to diffusion to provide a path for the charge to be discharged. In the design, control signals of TG come from digital part, which are generated by shift register as described in chapter 3. They are connected to transistor gates of inverters. The long metal interconnections lead to antenna problem. The design rule normally defines the maximum ratio of metal area to gate area such that charge on the metal will not damage the gate. The ratio in the technology we use is 100:1.

There are layout techniques to help deal with antenna ratio rules. Figure 4.13 shows a typical fix to an antenna violation, known as "cut and link" method. If metal 1 connects to gate terminal of transistor, its length would exceed the limit, we can use short links from metal1 to metal2 and back to metal1 connecting to gate. In this design, this method is applied

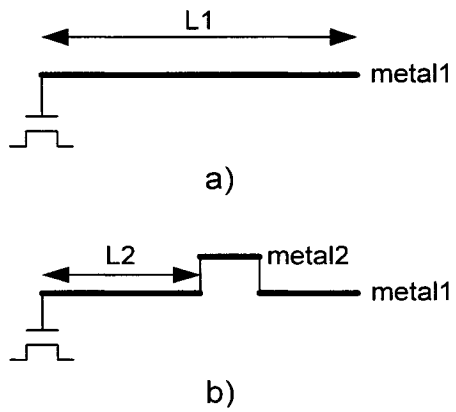


Figure 4.13 "Cut and Link" method to moderate antenna rule's effect;
a) antenna rule violation; b) "cut and link" method

An alternative method is to attach source/drain diodes to problem nets as shown in Figure 4.14. These diodes can be simple junctions of n-diffusion to p-substrate rather than transistor source/drain regions.

Figure 4.14 Adding antenna diode to moderate antenna rule's effect

The first method, "cut and link", is used in the test chip because of a large amount of long wires connecting S and SW TG to transistor gates. The second method, adding antenna diode, need more space than the first method,

4.4 Digital part realization

In VHDL coding, the top-level entity is "digital_control". The input/output architecture of digital_control is illustrated in Figure 4.15

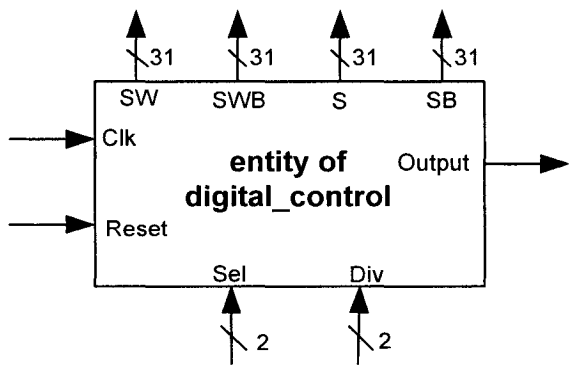


Figure 4.15 Architecture of digital control entity

Under digital_control entity, there are four sub-entities: shift_registor, shift_out, multiplexer (mux) and divider. Among them, shift register and divider are synchronous module with the same reset signal but different clocks, while shift_out and mux are combination circuits. An overall architecture of digital control circuit is displayed in Figure 4.16. RTL coding is used to realize

this architecture which was synthesized by TSMC 0.18 CMOS Technology (compiled by standard cell in vst_n18_sc_tsm_c4_wc library).

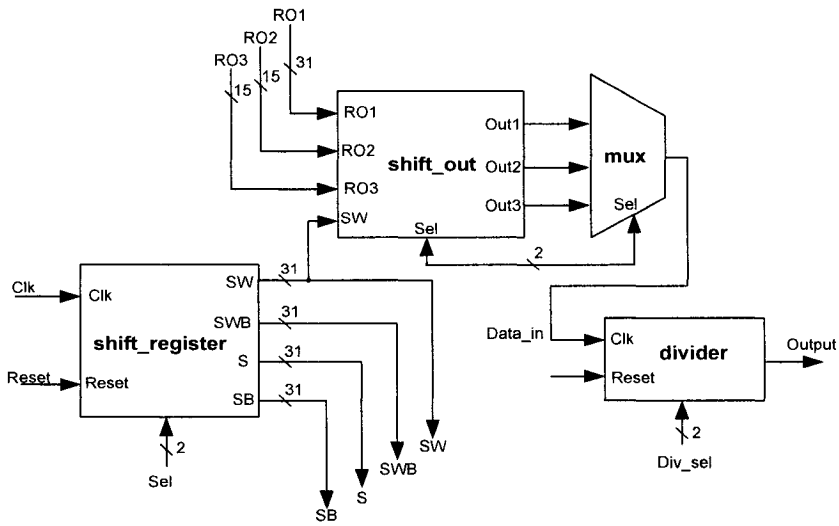


Figure 4.16 Overall architecture of digital control circuit

Since a large amount of flip-flops connect to single clock signal in the synchronized circuit (shift register, for example), drive strength and clock skew have to be considered. Tree-clock (shown in Figure 4.17) were created and inserted in physical design stage. The major task of clock-tree design is to develop the interconnect geometry that connects the clock to all the cells on the chip that are needed to synchronize with the system clock. In clock-tree design, the major concerns are minimizing clock skew and optimizing clock buffers to meet skew specifications and minimize clock-tree power dissipation.

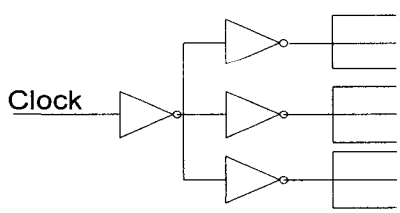


Figure 4.17 Structure of clock-tree

In this design, Clock Tree Synthesis (CTS) tools with Cadence's Gate Ensemble place-and-route tools are used to make automatic clock-tree synthesis and placement to chips. CTS cluster the clocked cells and match interconnect-RC delay for balanced-tree routing, creating an output file annotated to the circuit file that the router use. After routing, the output file (.cts) can be applied to post-layout simulation.

4.5 Test chip on top-level

Figure 4.18 shows the top-level block diagram of the test chip. Three series of RO and digital control part are connected together with seventeen pads. A dummy of poly is placed in the left bottom of the chip to meet requirement of layer density of process technique.

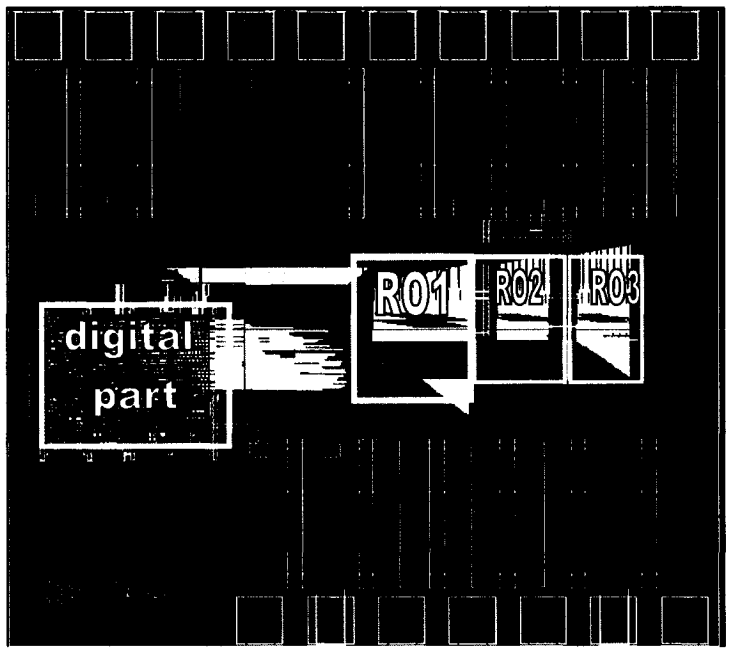


Figure 4.18 Top-level layout of test chip

We use two sets of power supplies to separate supply of RO from that of digital part (VDD1, VSS1 and VDD2, VSS2). Input signals "CLK", "RESET", "SEL(1:0)" and "DIV(1:0)" use

digital input pads "Output", "SW(14)_out" and "SW(31)_out" use digital output pads. Both of them use buffers to enhance their power of drive.

I/O pads assignment are illustrated in Table 4.4. Among them, SW(14)_OUT and SW(30)_OUT act as test points to make sure if shift register works well and creates correct control signals. Power supply for RO is separated from that for digital part. Hence the test chip will be easy to use for testing delay variation caused by power supply. The pad library used is tpz973g, version 100, processed by TSMC 0.18um Logic Salicide.

Table 4.4 Assignment of chip I/O pads

Pad No.	I/O Name	Pad name	Description
1	RESET	PDIDGZ	Input pad
2	DIV(0)	PDIDGZ	Input pad
3	DIV(1)	PDIDGZ	Input pad
4	OUTPUT	PDO02CDG	CMOS output pad
5	VDD_RING	PVDD2DGZ	For I/O cells power supply
6	VSS_RING	PVSS2DGZ	For I/O cells power supply
7	VSS1	PVSS1DGD	For core cells power supply
8	VDD1	PVDD1DGD	For core cells power supply
9	SW(14)_OUT	PDO02CDG	CMOS output pad
10	SW(30)_OUT	PDO02CDG	CMOS output pad
11	VSS_RING	PVSS2DGZ	For I/O cells power supply
12	VDD_RING	PVDD2DGZ	For I/O cells power supply
13	SEL(0)	PDIDGZ	Input pad
14	SEL(1)	PDIDGZ	Input pad
15	CLOCK	PDIDGZ	Input pad
16	VSS2	PVSS1DGD	For core cells power supply
17	VDD2	PVDD1DGD	For core cells power supply

4.6 Post-layout simulation results

This subsection analyzes delay mismatch in the three layout structures presented on section 4.4, using Monte Carlo simulation. Subsequently, a structure with the lowest delay mismatch will be selected to analyze delay mismatch related to transistor sizes and cell numbers in the RO. The goal of the analysis is to provide valuable information to reduce the effect of delay mismatch in application circuit design.

All simulations in this subsection are post-layout ones under TSMC 0.18um CMOS Technology. The exactly same simulation procedure was followed for all structures. Layout was extracted with parasitic capacitances in Virtuoso of CADENCE. In Monte Carlo process file, length deviation (standard deviation) was setup as 0, 1.8 and 3.6 nanometers respectively, which means that simulations were performed in three cases: without process variations, small parameter variations and large variations. Note that when length deviation is set to 0 nm, the delay mismatch is only caused by layout effects. The nominal length values used for each test case are described in the corresponding sub-sections. Each simulation was carried out for 100 runs, and for each run, random length values were assigned to transistors by the simulator based on the Gaussian distribution defined by the chosen deviation and nominal length values. From the simulation results, all RO periods were obtained and then the computation method was used to obtain single cell delay and delay mismatch.

4.6.1 Delay mismatch vs. layout structures

Figure 4.19 shows single cell delays of three layout structures with the 3.6 nm length deviation. In this case, delay mismatches are caused by both non-uniform interconnect and length deviations due to process variation. Type-I structure has the smallest cell delay and cell delays are the largest in type-III structure.

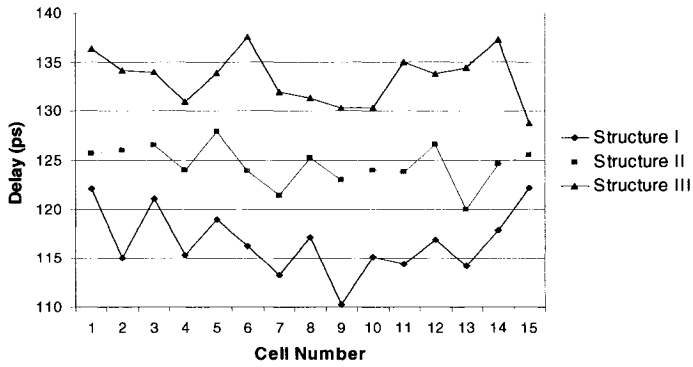


Figure 4.19 Single cell delays in three layout structures (Length deviation =3.6nm)

Table 4.5 gives delay mismatch in detail for the three structures. We performed simulations in three different cases: without process variation, small length variation and large length variation. From this table, we notice that in general, delay mismatch in structure I is larger than that in two others. Comparing structures II and III, delay deviations in two structures are much closer. However, from the view of parasitic capacitance, interconnect in structure II induces smaller capacitance, resulting in smaller average cell delay in this structure. Therefore, structure II is selected to implement the test chip. It is also used to perform the following simulations in this subsection.

Table 4.5 Delay mismatch vs. layout structures

Length	**Struct. I**		
Deviation	**μ (ps)**	**σ (ps)**	**CV (%)**
0nm	117.11	2.33	1.99
1.8nm	116.98	2.35	2.00
3.6nm	116.67	3.22	2.76
	Struct. II		
	μ (ps)	**σ (ps)**	**CV (%)**
0nm	124.74	***1.19***	0.95
1.8nm	124.82	***1.79***	1.43
3.6nm	124.56	***2.00***	1.60

	Struct. III		
	μ (ps)	σ (ps)	CV (%)
0nm	133.18	1.49	1.12
1.8nm	133.19	1.88	1.40
3.6nm	133.32	2.57	1.93

4.6.2 Delay mismatch vs. transistor sizes

This section analyzes the effects of delay mismatch for different transistor sizes. Since type-II is the structure with the smallest delay mismatch as described in the previous subsection, it was chosen to carry out Monte Carlo simulations for three 15-cell architecture with transistor lengths as 0.18um, 0.36um and 0.72um respectively. The obtained single cell delays and delay mismatches are tabulated in Table 4.6. It illustrates that enlarging the transistor length increases the single cell delay. Furthermore, larger circuit area may increase unbalanced interconnect which will lead to more delay mismatch, and even so at the presence of no process variations. However, the relative deviation decreases. That is, the increase in mismatch is less than the increase in cell delays. Therefore, the effects of delay mismatch would decrease with the transistor size increasing.

Table 4.6 Delay mismatch vs. transistor sizes

Length	**L=0.18um**		
Deviation	**μ (ps)**	**σ (ps)**	**CV (%)**
0nm	115.71	1.83	1.58
1.8nm	115.66	2.44	2.11
3.6nm	115.25	1.53	1.32
	L=0.36um		
	μ (ps)	**σ (ps)**	**CV (%)**
0nm	281.34	3.43	1.22
1.8nm	281.62	3.45	1.22
3.6nm	280.67	4.23	1.51

	L=0.72um		
	μ (ps)	σ (ps)	CV (%)
0nm	766.7	6.59	0.86
1.8nm	767.1	6.4	0.83
3.6nm	765.7	7.38	0.96

This situation can be explained by using an approximated equation. Assuming all of parameters are constant except of gate length. Hence inverter delay can be expressed as function of gate length [24]:

$$D = kL_{gate}^{1.5} \tag{4.4}$$

Hence the relation between delay mismatch (standard deviation of delay) and gate length can be expressed as:

$$\sigma_D = \sqrt{Var\{D\}} = 1.5kL_{gate}^{0..5} \tag{4.5}$$

where k is a constant. If gate length increases N times, the cell delay would increase $N^{1.5}$ times, while the delay mismatch increases $N^{0.5}$ times, therefore, the increasing rate of relative deviation would be:

$$\frac{N^{0.5}}{N^{1.5}} = \frac{1}{N} \tag{4.6}$$

This is only approximate equation. The simulation results indicate the fact that the increase in mismatch is indeed less than the increase in cell delays. Therefore, the delay mismatch CV or saying, the effects of delay mismatch, would decrease with the transistor size increasing.

Note that in the case of L=0.18um, when length deviation is 3.6nm, the deviation of the delay becomes smaller. That means the effect of process variation may mitigate the delay mismatch caused by interconnect.

4.6.3 Delay mismatch vs. number of cells

In order to investigate the dependence of delay mismatch on the number of cells in the RO, Monte Carlo simulations were also conducted on ring oscillators with different number of cells with a single transistor length of 0.36um. The numbers of cells were chosen to be 11, 15 and 31. The obtained results are illustrated in Table 4.7.

Table 4.7 Delay mismatch vs. the RO number of cells

Length Deviation	RO_11 μ (ps)	RO_11 σ (ps)	RO_11 CV (%)
0nm	281,34	3,43	1,22
1.8nm	281,62	3,45	1,22
3.6nm	280,67	4,23	1,51
	RO_15		
	μ (ps)	**σ (ps)**	**CV (%)**
0nm	280,28	4,3	1,5
1.8nm	283,77	5	1,76
3.6nm	283,01	4,94	1,75
	RO_31		
	μ (ps)	**σ (ps)**	**CV (%)**
0nm	305,84	3,98	1,3
1.8nm	305,98	4,06	1,33
3.6nm	304,86	6,8	2,23

Basically, with the increasing number of cells, the delay would increase largely because of an increase in interconnects. However, delay mismatch does not increase as much as the delay increases, especially in the case of smaller process variation, as the effect of layout on latter is dominant when process variation is minor. Moreover, with increasing the number of cells, the length of wire increases at the same time, therefore cell delay increases. Since the unbalance in interconnects and the delay deviation (standard deviation) are both proportional to the wire length, there will be no change in the relative deviation of cell delay.

In summary, delay mismatch in RO highly relies on layout and process variations. When designing application RO circuit, there is a direct trade-off between circuit area and delay mismatch. Larger transistor sizes imply larger circuit area, but lead to small relative deviation of delay which may decrease the effect of delay mismatch on the circuit.

4.6.4 Interconnect effect

In the circuit layout, interconnects play important role in both cell delay and delay mismatch. Decreasing parasitic capacitance would no doubt reduce cell delays as well as delay mismatch due to interconnect. Capacitance formed by metal wires is determined by wire area and distance between them. For a certain structure, both length and width of metal wires are unchangeable, which means the wire area is fixed. Therefore the only thing we can do is to increase the distance between wires. However, increasing adjacent wire space in the same layer would enlarge the area of the circuit. Using wires in different layers is an efficient way to reduce parasitic capacitance without increasing the circuit area. Figure 4.20 illustrates this wire modification. In Figure 4.20 a), all parallel wires are put in metal 3, which will lead to large parasitic capacitance. After modification, neighbour wires are put in metal 1 and metal 3 respectively as shown in b).

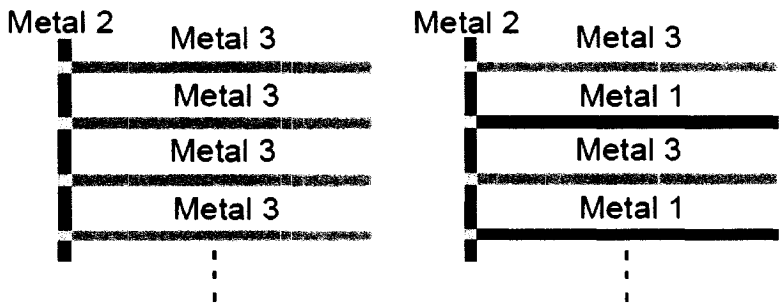


Figure 4.20 Resolution to high density wire;
a) closed wires in the same layer; b) closed wires in different layers

In the three types of layout structures, large amount of wires focus on dense interconnect area. Wire modification was made in this area. Simulations were performed with the three types of structures to compare cell delays before and after the modification. Cell delays and delay mismatch in these two cases are shown in Table 4.8. Before modification, all parallel wires are in the same layers. While after modification, these wires are put in the different layers. Therefore, the distance between two neighbor wires in the same layer is doubled, leading to much less interconnect capacitances. Hence delay mismatch in three structures are much reduced, especially in type-I structure where the wire length is very long. In this case, inter layer dielectric (ILD) turns to be an important factor producing parasitic capacitance.

Table 4.8 Delay mismatch comparison before and after layer modification

Struct.	Before modification			After modification		
	μ (ps)	σ (ps)	CV (%)	μ (ps)	σ (ps)	CV (%)
I	308,1	10,74	3,48	280,3	4,3	1,53
II	305,9	5,924	1,94	292	2,1	0,72
III	316	4,898	1,56	311,1	2,64	0,85

The ILD effect can be explained by using the post-layout simulation result for type-II layout structure. After extracting layout with parasitic capacitances, RO periods were computed by simulation, then 15 cell delays were derived and are shown in Figure 4.21. In this case, delay mismatch is only caused by unbalanced interconnection in layout, because no process variations were assigned to transistors.

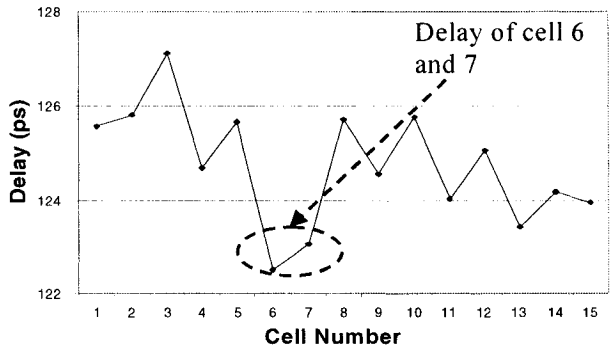


Figure 4.21 Delay mismatches due to interconnect parasitic capacitances

In Figure 4.21, cell delays present some interesting features: delays of cells 6 and 7 are much smaller than those of the other cells. This feature can be explained according to the diagram of interconnection shown in Figure 4.22.

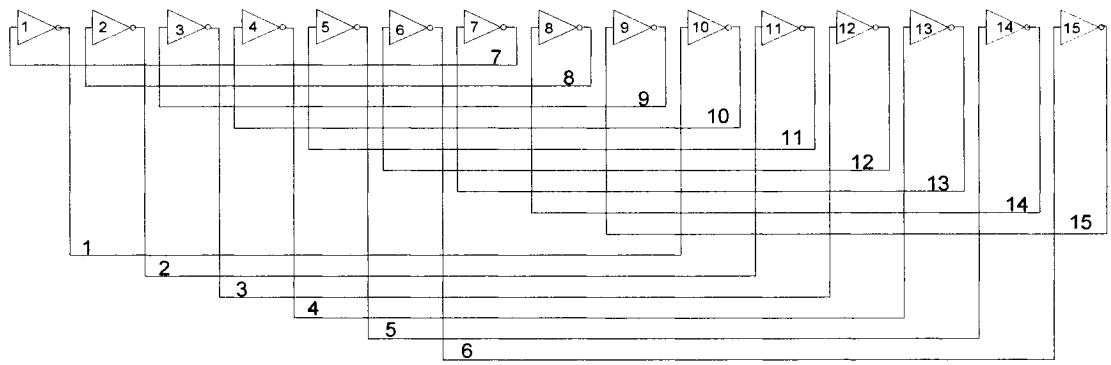


Figure 4.22 Diagram of interconnection in the type_II layout structure

The line numbers in Figure 4.22 represent the cell number whose output drives the line. For example, the line marked as "7" would indicate that this line is driven by the output of the 7^{th} cell. All marked lines in the figure form two ILD capacitances with both their up and down wires, except of lines 6 and 7 which are the first and last lines. These two lines form only one ILD capacitance with their one neighboring wires. Hence cells 6 and 7 would drive smaller load ILD

capacitors, which lead to a smallest cell delays in the architecture. Besides ILD capacitance, metal wires in the same layer (for example, line 8 and 10) and vertical wires shown in the figure also form parasitic capacitances. This complicated situation makes the cell delays to present other features, like cell 3 possessing the largest delay, cell 13 possessing the relatively small delay, and so on. However, the most important feature is that less ILD capacitances in line 6 and 7 make delays of cells 6 and 7 much smaller delays than those of the other cells. Therefore, ILD capacitance has significant effect on the cell delays

4.7 Conclusion

The single cell delay and delay mismatch obtained from the modified RO based test structure can accurately represent the process variations and somehow represent the delay mismatch in normal RO. Buffers on the output of RO protect RO from the influence of outside circuit. In the layout implementation, the antenna rules are very important to this design for many long metal wires connecting to transistor gates. "Cut and Link" method is used to solve the antenna violation in the master thesis.

Delay mismatch is quite linked to process variations and layout. A good layout structure relies on strict balance of interconnect between cells. With increasing transistor sizes, delay mismatch may also increase, but the relative deviation of delay will decrease, which means that the effect of process variation on delay mismatch will decrease. This gives a trade-off between circuit area and delay mismatch when designing application circuits. When jitter due to single cell delay mismatch is the main concern in the circuit, it is necessary to increase transistor sizes to decrease the effect of process variations on the delay mismatch. Changing cell number may be considered to get desired cell delays, especially when the variation values are small.

In the layout, using different layer wires in high density interconnect areas can significantly reduce the cell delay caused by interconnect parasitic capacitance, which can highly reduce the effects of interconnect variations on delay. In this case, the effect ILD parasitic capacitance turns to be the most important consideration in the layout.

CHAPTER 5

TEST STRATEGY

The chip was fabricated with TSMC 0.18um CMOS technology and bonded with CQFP 44 packaging. This chapter describes the main test procedure including printed circuit board design for testing, typical measuring equipment used. Test accuracy, chip diagnosis and debug strategy are also discussed in the chapter. These test and diagnosis issues provide experience for the future test chip improvement.

5.1 Printed Circuit board for testing

The pin assignment of the packaged chip is shown in Figure 5.1. Besides power supply, there are six inputs and three outputs all together.

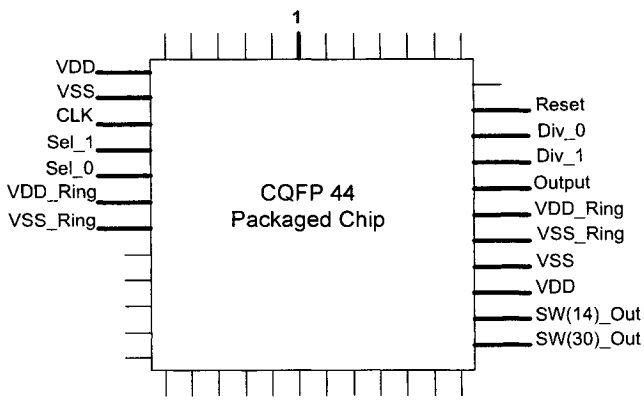


Figure 5.1 Pin assignments for packaged chip

In this figure, "Reset" and "CLK" are global reset and clock signals for shift registers. "Sel_0" and "Sel_1" are 2-bit boolean values which control the RO series to be selected. "Div_0" and "Div_1" are also 2-bit boolean values to select frequency dividing times. For outputs,

"SW14_Out" and "SW(30)_Out" are outputs of 15th and 31st bit shift register respectively, while "Output" is the output signal from the ring oscillator to be measured.

It's generally considered bad design practice to leave unconnected CMOS inputs floating. Unconnected inputs have a tendency to bang between input thresholds (V_{IL} and V_{IH}). The result is that the internal transistors would spend a long time switching unnecessarily. Not only does this contribute to noise in the system, but also it consumes real power. Hence, in the test board, dip switch shown in Figure 5.2 is used to provide boolean values to realize input signals. In addition, it avoids any input point floating. If the switch is "off", the controlled input signal would fall to "low" through a 10kΩ resistor; if the switch is "on", the controlled input signal would be "high". For Reset signal, a simple debouncing circuit shown in Figure 5.3 is used to eliminate shaking.

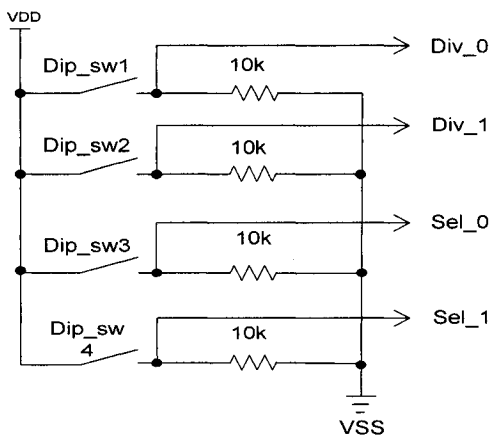


Figure 5.2 Using dip switch to generating input control signals

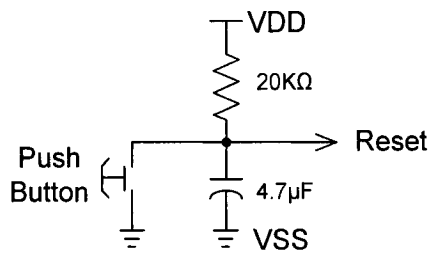


Figure 5.3 Simple debouncing circuit providing reset signal

For CLK signal, a pulse generator circuit is used to give pulse input signal. Figure 5.4 displays pulse generator applied to CLK. Each time, toggling the switch Clk_sw would generate a clock pulse; then the shift register 1 and 2 shift forward for one bit, which means that the current RO stop oscillating and the next RO is activated. An alternative to CLK generating circuit is by applying a continuous square wave signal provided by signal generator to provide CLK signal and perform continuous measurement to one series of RO. Figure 5.5 is a layout of PCB designed with ORCAD.

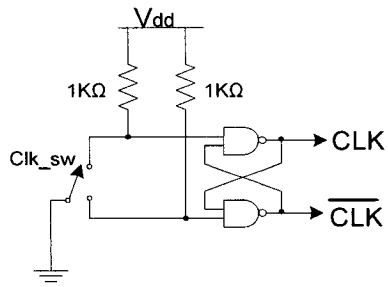


Figure 5.4 Pulse generators applied to CLK

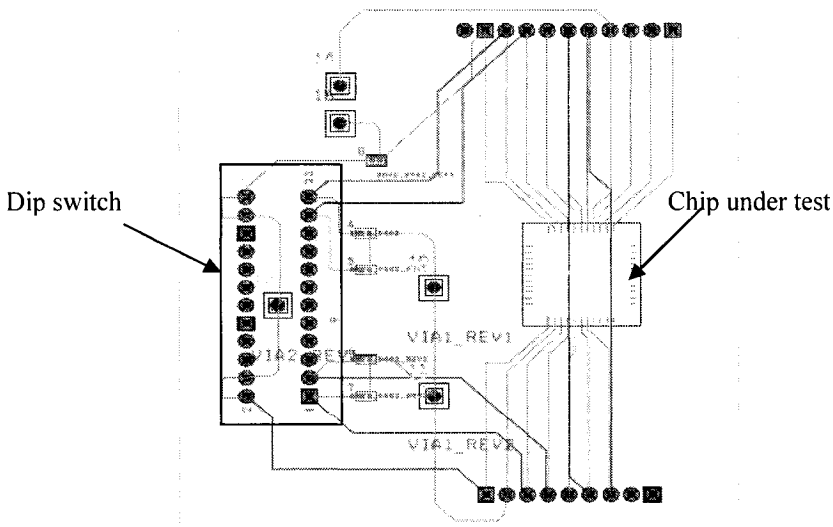


Figure 5.5 PCB layout for chip testing

5.2 Test procedure

First of all, before activating RO, 4-bit input control signal should be set up by configuring dip switches. For example, if RO1 is to be measured, and 16 times of frequency divider is to be used, then dip_sw1 and dip_sw2 should be "on" , dip_sw3 and dip_sw4 should be set to "off" which means Sel control signal is configured as "00" and Div control signal is configured as "11". Secondly, pushing the reset button resets the circuit. Next, toggling the clock switch gives a clock to shift register. The first RO in RO1 would oscillate, and the period of output signal can be measured by oscilloscope. If we toggle the clock switch again, then the second RO in RO1 would oscillate, its oscillating signal would pass through multiplexer and divider to the output. If other series of RO is to be measured, we can just reconfigure the dip switches.

It is important to activate single oscillator once a time. First of all, it would ensure that only one oscillator can go through frequency divider and give output signal at one time. Secondly, it would reduce power supply noise. A free running oscillator can induce significant noise on its power supply because of the numerous transitions its inverter makes [29]. The accuracy of the ring oscillator frequency depends on a clear power supply. Any deviations in the power supply can result in unwanted fluctuations in RO frequency. 2-bit boolean value of "Sel" control signals ensures that only one series is selected at one time. Pulse signal applying to CLK ensures that only one output of SW shift register (SW0-SW31) can be at '1', others would remain '0'. These control signals guaranty that no more than one RO is activated at the same time.

5.3 Measuring accuracy

The measurement for the test chip is quite simple. Only an oscilloscope is necessary to measure the period of ROs. Here digital phosphor oscilloscope-TDS 7154 is used to carry out period

measurement. The TDS 7154 oscilloscope provides at most 100GHz measuring frequency, 50Gs/second sampling rate, and period test accuracy is expected to 0.1%.

As mentioned in Chapter 4, the output signal frequency is scaled down by a factor of 16 by using a 16-stage frequency divider circuit. The period for the signals out of the frequency divider was observed to be 25ns, 28ns and 95ns for RO_3, RO_2 and RO_1 respectively, making the TDS 7154 oscilloscope suitable to be used for test measurements. With measurement range 20ns to 100ns, the measurement resolution would be 20ps-100ps (0.1% accuracy). With the 100 ps resolution at the output of the divider circuit, the real resolution for the period of the RO is given by 100ps /16 = 6.25 ps at most. Therefore, the minimum measured value for the total cell delay of RO1 is expected to be about 6.25ps /2 ≈ 3 ps. With 20 ps resolution, the minimum value for total cell delay of RO2 and RO3 is about **20 / (16*2) *≈0.6 ps.*** However, if divider accuracy is considered, the measurement resolution for cell delay would be lower than the above calculation values.

5.4 Chip analysis

Test result shows the control signal SW14 and SW31 are very unstable. In some of packaged chips, there are no output control signals at all. The possible reason is there isn't enough electrostatic discharge (ESD) protection in circuit inputs, especially the clock input.

In CMOS technology, MOSFET constant electric field scaling theory scales the dimensions of the transistor to maintain the same electric field across the oxide film. However, as operating voltages are lowered and gate oxides are thinned, input/output of MOS devices become more and more sensitive to electrical overstresses from the outside world, which do not scale at all with Moore's law [5]. As a result, ESD has a tendency to jump the isolative gaps etched into the metal film, ESD protection to MOSFET plays a profound role in the ESD robustness of the transistor as shown in Figure 5.6.

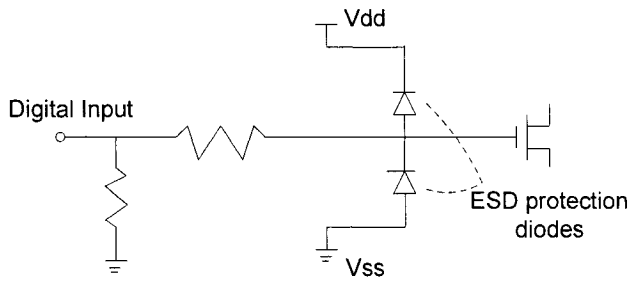


Figure 5.6 ESD protection diode

Besides, a bit of caution should be used when selecting resistors for use in circuits that may be subjected to ESD. It turns out that plain old carbon-composition axial-leaded resistors are the best. Surface-mount resistors have problems with hot spots forming in the metal film when subjected to ESD. These hot spots are caused by non-uniform current densities flowing in the metal film. The net result is that the resistor can be permanently damaged by ESD events. Unfortunately, all of resistors used in PCB are all surface-mount resistors.

The strategy of debugging the circuit, which does not function as expected, is to take steps to isolate the problem. The circuit gets split up into the smaller sub-circuits in design stage, and these sub-circuits will individually be tested for functionality. If a sub- circuit is tested and works as intended, then next step will be taken to diagnose error lying somewhere else. The output pads SW14_Out and SW31_Out are designed for these basic debugging steps to be applied to the test chip. These two outputs may indicate if the shift registers work properly. Applying continuous clock signal to the test chip instead of pulse signal, SW(14)_Out was triggered to "high" every fifteen clock as shown in Figure 5.7, which verify that shift register 1 works well. In fact the test chip should have more test points for shift register 2 and RO outputs. However they haven't been set up due to pad limitation. To improving the design and to enhance the DFT ability, we consider changing 4 input pads, Sel (1:0) and Div (1:0), as analog input pads, which can save much space, so that more test pads can be put. Besides, in this prototype, the output frequency is more than 50

MHz, because the maximum frequency divider designed is only 16 times. CQFP package have to be used, which leads to inconvenient for testing. If the dividing times are augmented, like 64 times or more, the output frequency would decrease to less than 1 MHz, and then the chip can be bonded with DIP package which make it easy to test on bread board.

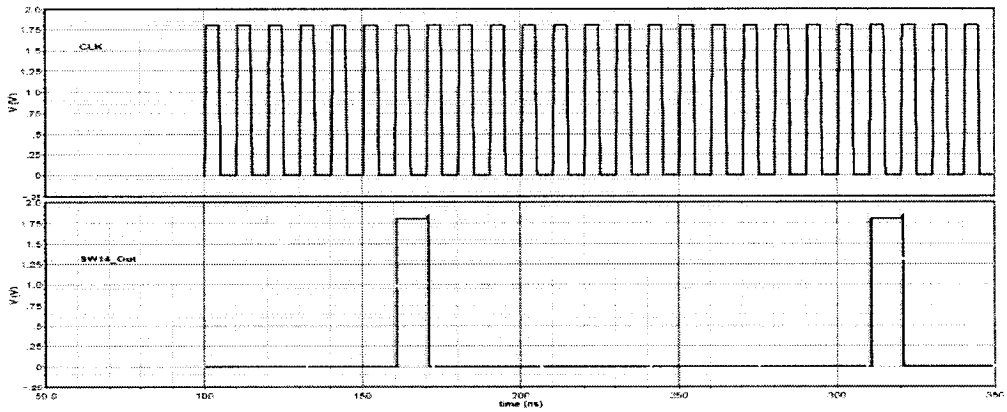


Figure 5.7 Test result for the 15th bit of shift register 1

5.5 Summary

Many test issues are discussed in this chapter. To avoid input point floating in CMOS circuit, dip switch is used to configure input control signals; to prevent shaking for the circuit reset, a debouncing circuit is applied to reset switch. Some test issues should be considered in design stage. Although the ESD protection is considered in standard pad, more attention should be paid in the design and the PCB or breadboard for chip testing.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

This chapter summarizes the important points presented in this master thesis; submits the possible improvement to test chip and describes potential future work.

6.1 Thesis summary

The increasing difficulty in controlling the uniformity of critical process parameters in the smaller devices makes the electrical properties of such scaled devices much less predictable than in the past. Timing uncertainty due to this process variation is one of the most challenging issues in the design of today's digital integrated circuits. Dealing with timing uncertainty imposes the use of conservative delay models and large time margins that lead to over-size designs and make it difficult to reach the performance limits of the target technology. For example, traditionally, only the effect of die-to-die fluctuations have been the main concern in CMOS digital circuit design, and the effect of within-die fluctuations have been neglected or considered as constant, which is found inaccurate. Therefore, in recent years, many published paper intended in within-die variation evaluation. Most of delay measurement circuits are designed based on RO because its cell delay is highly sensitive to process variation.

The simple modified RO architecture is an initial idea to measure single cell delay. Adding delay elements one by one, and then from RO periods difference, delay of each element can be obtained. However, simulation results testify that this structure is unsymmetrical. Even in ideal simulating circumstance, it cannot give satisfied result.

In the improved architecture, given single RO with N delay elements, the overall structure is composed of 2N + 1 delay elements, providing 2N+1 individual RO that are selected in circular manner controlled by switches. Each RO can be obtained by disconnecting the first element from the current RO and appending an extra delay element at the end of the RO. This process can continue until the last RO - $2N+1^{th}$ RO. A total number of 2N+1 RO structures are obtained by reconfiguring the modified RO architecture. The corresponding switches control the configuration of a particular RO.

The modified RO architecture allows characterizing the mismatch in the consisted delay elements simply by measuring the corresponding periods of the 2N+1 ring oscillators, without knowing the propagation delay of the individual delay elements. In fact, by performing some mathematical manipulations, the propagation delay of each delay cell can be found from the measured periods. This is the most important advantage of this proposed test methodology.

In layout of this modified architecture, interconnects are much more unbalanced than that in the circuit with normal RO. It is difficult to keep interconnects balance because of the circle like structure, whereas the wires in layout are only allowed to be horizontal and vertical directions.

6.2 Contribution of the thesis

The common practice of measuring delay mismatch due to intra-die process variation is to design a test structure basing on ring oscillator. However, most test circuits focus on analyzing frequency data to average delay of delay cells, no circuit involves in single cell delay and cell-to-cell delay mismatch measurement. This master thesis describes the design and implementation of a test circuit of a feasible modified RO based test chip fabricated in the TSMC 0.18um CMOS process. The test chip can be used to characterize process variations by analyzing single cell delay and cell-to-cell delay mismatch in a modified ring oscillator.

Using single cell delay of a RO to characterize intra-die variation is much accurate than using average delay of delay cells, because the single cell delay in a RO represents both systematic and random variations within a die exactly and thoroughly. On the other hand, in many application circuits, such as fractional-N synthesis circuit, TDC and VDL etc, it is just the timing uncertainty between single delay elements that degrades circuit performance: produces jitter and spur, and limits measurement resolution. This test chip can provide valuable reference data for analyzing cell delay mismatch. With the analyzing results, designers can predict the performance of application circuits. Tightening the margins can enable designer to focus their efforts on meeting or exceeding performance specifications. It also gives possibility to find efficient method to reduce the effect of delay mismatch in the future.

Another advantage of the delay mismatch obtained from test circuit represents mainly single cell delay mismatch between delay cells inside ring. Process variation in either connected buffer or control circuit has little effect on measurement results, though connected buffer induces slight delay to RO. However, this slight delay also exists in many application circuits.

Finally this technique of intra-die variation analysis can be applied to study impact on emerging interconnect and layout-induced variation. The completion of this master thesis has opened doors to investigating work in the study of process variation.

The completion of this master thesis has open up many issues relating to improving both design and measuring methods. A number of different series of RO can be implemented to investigate interconnect and layout-induced variation. Although some analysis methods have been performed on the frequency data to investigate device variation, more analysis methods like power supply voltages variation, can be developed and conducted on the test chip due to the fact that power supply of RO is separated from control circuit in the test chip. Moreover, the test chip can be imported into new and emerging semiconductor technologies.

6.3 Improved chip strategies and future work

This test chip features three series of RO that explore gate-length variation, as addressed in Chapter 5. Each series of RO has different sizes; however, within one series, inverters and transmission gates have the same size. If we enlarge gate length of transmission gates, delay mismatch in modified RO will be closer to the situation in normal RO.

In this test circuit, it doesn't have enough test points (only SW14 and SW31) because of the limited the number of pads, which makes the chip difficult to test. Testability features are a means of making a circuit more controllable and observable. While less test points makes it uneasy to observe and evaluate defects of circuit. For example, some of chips have correct signal of SW14, but no signal of output. In this situation, which part of circuit causes the problem, other incorrect signals from shift registers or defect of dividers? If space allows, the best way is to create extra test points in the shift register 2, output of RO directly, before and after frequency divider, so that every critical node in the circuit can be measured and tested.

The completion of this master thesis has open up many issues relating to improving both design and measuring methods. A number of different series of RO can be implemented to investigate interconnect and layout-induced variations.

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APPENDIX

"Measurement of Delay Mismatch Due to Process Variations by Means of Modified Ring Oscillators" Published in IEEE International Symposium on Circuits and Systems (ISCAS), May 2005

Measurement of Delay Mismatch Due to Process Variations by Means of Modified Ring Oscillators

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***Abstract* — A novel and effective test circuit to measure cell-to-cell delay mismatch due to process variations is presented. A fully digital control circuit that efficiently realizes the technique is also described. The proposed test structure is realized by a series of modified ring oscillators that minimize factors of inaccuracy. The results of a simulation using 0.18μm CMOS technology show the feasibility of the technique. This test structure can be beneficial in thoroughly characterizing the effects of systematical process variations inside the chip.**

I. INTRODUCTION

Systematical intra-die process variation is a variability pattern, which was newly investigated in recent years. Before, intra-die variations were considered as stochastic variations with no spatial dependence [1]. Deep sub-micron technologies, however, exhibit a new intra-die variability pattern. In addition, a number of previous methods for statistical timing analysis (including conventional worst-case timing analysis) propose intra-die delay variability at constant ratios of about 15% to 20%, which have been found to be over-conservative [2]. In a digital circuit, two of the most common negative effects of intra-die process variations are clock skew and clock non-linearity. Performances of digital circuits such as directly digital period synthesis DDPS and other digital clock synthesis circuits are highly affected by the delay mismatch due to intra-die process variations. One of the major source of spurs in DDPS circuits is the mismatch between delays of the cells in the same delay line [3]. This delay mismatch also becomes the main drawback of typical on-chip timing measuring methods such as Vernier Delay Line (VDL) technique [4]. Data collected from a state-of–the-art fabrication facility revealed that a significant and systematic intra-die variability of MOS gate lengths leads to large circuit path delay variations in an advanced 0.18um CMOS process [5]. Proper characterization of this variability will provide an accurate timing analysis method for designers, so that they can analyze and improve their design by reducing substantially the effects of variability. In this paper, we present a test structure that uses a series of modified ring oscillators (RO) dedicated to the high accuracy measurement of cell-to-cell delay mismatch. This test structure can be beneficial in thoroughly characterizing the effects of systematical process variations inside the chip.

The paper is organized as follows. In section II, we introduce what are common practices as well as the basic idea of the modified RO test structure and a simple architecture. The proposed modified RO structure and digital control circuits are presented in section III and IV. Section V analyzes the feasibility of the test circuit by presenting simulation results using 0.18μm CMOS technology. Section VI presents our main conclusions.

II. COMMON PRACTICE IN DELAY ANALYSIS

Characterization of the propagation delay fluctuations due to process variations is usually done with RO, because of their easy on-chip realization and high sensitivity to process variations. Moreover, the period T of a RO, which can be measured easily, is a function of all the delays of cells inside the ring. For an N-cell RO, the period can be expressed as:

$$T = 2 \times \sum_{n=1}^{N} D_n \qquad (1)$$

where D_n is the propagation delay of the n^{th} cell.

If we use, as in the case of most existing circuits [6], multiple independent RO to measure intra-chip variation, the average delay provided by the oscillators on the chip hides the effects of local process fluctuations and mismatch. Although a direct measurement test structure presented in [7] can measure the incremental delay, i.e., the difference between the two propagation delays of the same cell, it cannot measure the delay difference between any two given cells. Propagation delay mismatch measurement in the same delay cell cannot exhibit the significant intra-die variations, which are spatial dependant

The basic idea of the modified RO structure shown in Fig. 1 is that instead of using independent RO, we use multiple relational RO. This creates relations between the different RO. This architecture consists of N delay cells that are controlled through a switching network (S_0, S_1, S_2 ... SN). Each delay cell consists of a series of two inverters. The switching network is used to select the correct number of RO stages for the period to be measured. For example, if S_0 is on, the measured period (T_0) corresponds to the period of a RO composed of only the basic cells. If S_1, rather then S_0, is on, the measured period (T_1) is the period of a RO composed of the basic cells and cell 1. The delay (D) for each cell is given by:

$$D_n = \frac{1}{2}(T_n - T_{n-1}) \quad (1 \le n \le N) \qquad (2)$$

The delay mismatch between the different selectable cells is given by: D_1-D_2, D_2-D_3 ... D_{N-1}-D_N. In an ideal situation, all the selectable cells should have exactly the same delay, which would mean that delay mismatch is zero. Unfortunately, the simulation results show that delays of those cells are not equal, as displayed in Table 1. This is due to the fact that this structure is not symmetrical.

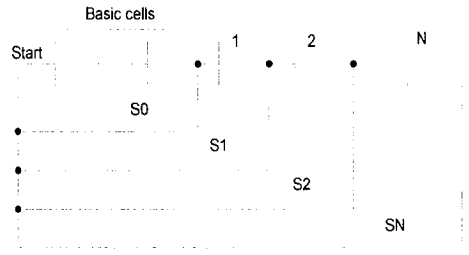

Figure 1. Architecture of simple modified RO

From Fig. 1, we notice that every delay cell is connected to one switch, that the "Start" node is connected to each of the N switches, and that no switch is connected to basic cells. Moreover, the last cell of each RO is connected to different number of delay cells, e.g. in n^{th} (i =1 to n) RO, the n^{th} cell connects (N-n) serial delay cells. These two factors induce delay variation even in the ideal situation (without process variation). Therefore, the differences in delay represent not only cell-to-cell mismatch but other factors as well.

TABLE I Delay increment in simple modified RO

Delay Cell Number	RO Period (ps)	Cell Delay (ps)
0	1036.1	N/A
1	1332.9	148.4
2	1611.5	139.3
3	1882.9	135.7
4	2151.0	134.1
5	2417.4	133.2

III. PROPOSED TEST STRUCTURE

In this paper, we upgrade the structure shown in Fig. 1 so that it becomes completely symmetrical, and overcomes the drawbacks mentioned above. In the simple structure mentioned in the previous section, each RO has different delay cells, whereas in this improved structure, we use the same number

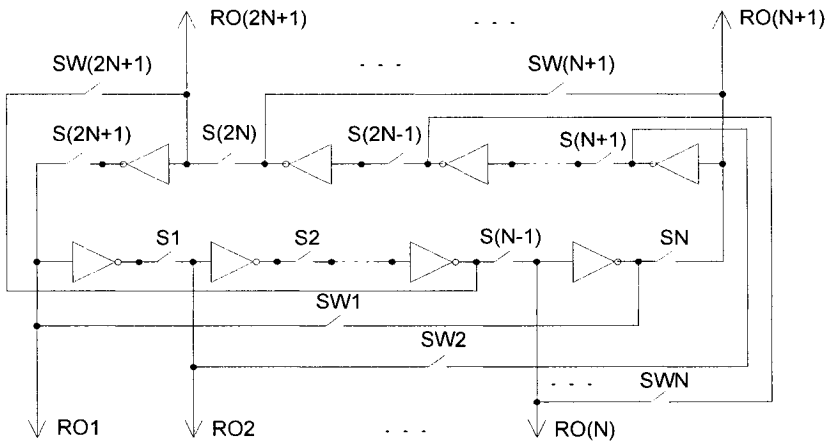

Figure 2. Achitecture of proposed modified RO

of delay cells, but change one cell from one RO to the other.

We use (2N+1) inverters to form a ring. These inverters are not connected directly, but through transmission gates, which act as switches (Fig. 2). By changing the configurations of switches we can realize (2N+1) RO. Each RO has N inverters and N transmission gates. RO_1 is composed of the first N inverters, S_1 to S_{N-1} and SW_1 is "on", while the remaining switches are "off". In order to switch to the next RO, the first cell of the current RO needs to be removed (the first switch is set to "off") and a new cell needs to be added, so that all of the RO will have the same number of stages. The notations S_1, S_2....S_N and SW_1, SW_2 ....SW_N refer to the switches as well as the control signals. A delay cell of delay D is formed of an inverter and a transmission gate. The period T_n of the n^{th} RO is given by:

$$T_n = 2\sum_{k=n}^{n+N-1} D_k \qquad (n=1\ to\ 2N+1) \qquad (3)$$

In fact, (3) includes 2N+1 equations. Arrange these equations by $T_n - T_{n+1}$; we get a series of different delays D_{diff_n} (for n=1 to 2N+1):

$$D_{diff\_n} = D_n - D_{n+N} = \frac{1}{2}(T_n - T_{n+1}) \qquad (4)$$

Equation (4) also includes the number of 2N+1 sub-equations. Arrange (4) by:

$$D_{diff\_1} + D_{diff\_N+1},\ D_{diff\_2} + D_{diff\_N+2},\cdots$$

$$D_{diff\_N+1} + D_{diff\_2N+1}$$

Then:

$$D_{diff\_1} + D_{diff\_N+2},\ D_{diff\_2} + D_{diff\_N+3},\cdots$$

$$D_{diff\_N} + D_{diff\_2N+1}$$

We obtain:

$$D_n - D_{n+1} = \frac{1}{2}[(T_{n+2} - T_{n+1}) + (T_{N+n+2} - T_{N+n+1})] \qquad (5)$$

Equation (5) gives the cell-to-cell delay mismatch. It may respond to spatial intra-die delay variations directly and accurately. In this structure, the relationship between the cell count of each RO and the number of RO is very important. If each RO has N cells, there must be at most 2N+1 RO in total. Otherwise, only some of the cell-to-cell delay mismatches can be obtained.

IV. DIGITAL CONTROL CIRCUIT

The signals to control the switches of the test structure are generated by a digital control circuit, which is shown in Fig. 3. Ideally, this control circuit has no effect on the measured delays.

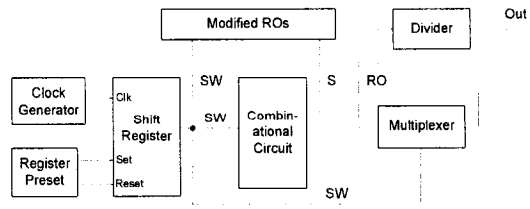

Figure 3. Diagram of digital control circuit

The control circuit is composed of a clock generator, a shift register and a combination logic circuitry. The clock is used for the shift register.

The parallel output of the register is used to control switches SW_1 to SW_{2N+1} as well as a multiplexer that selects the output. A "Register Preset" module is used to initiate the register at "100..." on power-up. Combinational logic is used to generate the control signals of switches S_1 to S_{2N+1}. It can consist of a series of N-input OR gates, which in fact are broken into several 4-input OR gates in order to keep gate delay as small as possible. In order to be able to carry out the measurement using common equipment, a divider is used to decrease the frequency of the circuit output.

V. SIMULATION RESULTS

All the simulations are done with 0.18μm CMOS technology. For Monte-Carlo simulations, we only focus on the variations in device sizes, since it is the main cause of delay mismatch. Moreover, we assume that the size variations follow a normal (Gaussian) distribution, and we use 1, 2 and 5 % of minimal size variations. The notations ΔL and ΔW refer to variations of 1% of minimal length and width, respectively. For confidential reasons, we can not give the used values of ΔL and ΔW. We know that in actual process variations, we can expect other size variations and distributions. The goal of this work is not to predict the intra-die delay mismatch, but to show the accuracy of our delay mismatch measurement structure.

We tested 11-cell architecture. In the ideal case (without process variations), the simulation results indicate that all the 11 RO have exactly the same period (1706.45ps), which means this architecture is completely symmetrical.

It should be mentioned that with this architecture, a single cell delay is composed of the delays of an inverter and a transmission gate. Monte Carlo simulations were performed with different size values following a normal distribution, where deviations are ΔL, 2ΔL, 5ΔL and ΔW, 2ΔW and 5ΔW for lengths and widths respectively. The size mismatch exists both in inverters and in transmission gates. The length of transistor we use is 0.24μm. The width of PMOS and NMOS transistors are 4μm and 1μm respectively. From the simulation results of period for each RO, we use equation (3), (4) and (5) to calculate cell-to-cell delay mismatch between the 11 cells. We then deduce the mean (μ) and standard deviation (σ) of delay.

The percentage of delay variation is expressed by the ratio of standard deviation to mean value:

$$Var = \frac{\sigma}{\mu} \tag{6}$$

Next, we remove all transmission gates, use only inverters and assign the same size variations to transistors in order to obtain the single cell delay variations without transmission gates. Table II shows that under the same size variations, the delay variations with transmission gates are almost twice as large as those without transmission gates. This is valid for different size deviations.

We then double the size of transistors, both lengthwise and widthwise. We use the same size deviations as described above and perform the same simulations. Table III displays the result with large transistors. From Table III, we notice that with transistor size increasing, all of delay variations are decreased. Moreover, modified RO to normal RO delay variation ratios are almost the same, regardless of the assigned size deviation.

From the simulation results, we conclude that no matter what transistor size is used, the delay variations obtained with our test circuit are proportional to those in a normal RO.

TABLE II Delay mismatch with small transistors

Size Deviation	Inverter +TG			Inverter only		
	μ (ps)	σ (ps)	Var	μ (ps)	σ (ps)	Var
ΔL,ΔW	170.6	3.3	1.93%	54.8	0.56	1.02%
2ΔL,2ΔW	170.9	6.4	3.74%	55	1.1	2.00%
5ΔL,5ΔW	171.6	16.1	9.38%	55.1	2.8	5.08%

a. TG: Transmission Gate

TABLE III Delay mismatch with large transistors

Size Dev.	Inverter +TG			Inverter only		
	μ (ps)	σ (ps)	Var	μ (ps)	σ (ps)	Var
ΔL ΔW	423.5	4.4	1.04%	145.2	0.8	0.55%
2ΔL 2ΔW	423.8	7.9	1.86%	145.4	1.5	1.03%
5ΔL 5ΔW	424.8	19.8	4.66%	145.9	4.0	2.74%

a. TG: Transmission Gate

We can thus use this test circuit to characterize delay mismatch due to intra-die process variations for the modified RO and then deduce the exact delay mismatch for the normal RO formed by inverters only.

VI. CONCLUSION

The main difference between this test structure and previous circuits is that the RO under test are not independent. While switching from one RO to the next, one delay cell is removed and another is added, while all the other cells remain. The period difference between these two RO represents the delay mismatch between the removed cell and the added one. With this structure, we can measure intra-die propagation delay variations with high accuracy. When used with a large number of different dies, this circuit can also be used to measure die-to-die delay variations. Compared with previous work, this new test structure can measure the effects of both local fluctuation and spatial dependant variation of the process. This test circuit will be implemented with different modified RO and used to characterize the delay mismatch and their effects on the spurs in the DDPS circuit.

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