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UNIVERSITÉ DE MONTRÉAL

DIGITAL BACKGROUND CALIBRATION FOR PIPELINED AND TIME-INTERLEAVED ANALOG-TO-DIGITAL CONVERTERS

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Cette thèse intitulée:

DIGITAL BACKGROUND CALIBRATION FOR PIPELINED AND TIME-INTERLEAVED ANALOG-TO-DIGITAL CONVERTERS

présentée par: Elsankary Kamal

en vue de l'obtention du diplôme de Philosophiae Doctor

a été dûment acceptée par le jury d'examen constitué de:

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To all my beloved

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RÉSUMÉ

L'apparition rapide, de nos jours, de différentes normes pour les systèmes de télécommunications a conduit au besoin de développer de nouvelles architectures de convertisseurs analogiques-numériques (CAN) à grande largeur de bande et à haute résolution. Parmi ces architectures, on retrouve les CAN pipelines qui présentent un bon compromis entre la surface du silicium occupée, la consommation de puissance et le débit de conversion. De plus, dans la plupart des architectures des CAN, la précision est limitée par l'appariement réel des éléments analogiques, nominalement à taille égale, et par le gain fini des amplificateurs opérationnels (ampop) résultant de la diminution de la tension d'alimentation. Cependant, la résolution de l'appariement et la précision du gain de l'ampop sont loin d'être conformes aux caractéristiques exigées par les CAN actuellement. Aussi, le mésappariement dans les canaux parallèles, utilisés pour concevoir des CAN pipeline à grande vitesse, et temporellement entrelacés, crée des distorsions non-désirées dans la bande passante. Ces distorsions doivent être évitées ou compensées.

Quant à la technologie de fabrication de CAN, le CMOS (Complementary Metal-Oxide Semiconductor) submicronique présente la solution la plus prometteuse pour l'intégration de système sur une seule puce (System-on-Chip - *SoC*). Cette intégration permet la réduction de la surface et de la puissance des circuits numériques plus rapidement qu'elle se permet pour les circuits analogiques. Par conséquence, la solution d'employer des techniques de calibration numérique afin d'améliorer la performance des CAN implémentés en technologie CMOS est devenue très attirante et convaincante.

Dans cette thèse, nous présentons de nouvelles méthodes et circuits numériques opérant en arrière plan dédiés à calibrer des CAN pipelinés et temporellement entrelacés.

Les nouvelles contributions proposées dans cette recherche sont récapitulées comme suit:

- Une nouvelle méthode d'échantillonnage, implémentée dans le domaine numérique, dédiée à surmonter les limitations des CAN temporellement entrelacés. Dans cette méthode, une permutation numérique aléatoire totale, pour n'importe quel nombre des canaux du CAN, peut être obtenue en échangeant aléatoirement la distribution des échantillons entre chaque groupe de deux CAN et en effectuant la rotation parmi ces différents groupes.
- Une technique de calibration aveugle surmontant les non-linéarités résultant du mésappariement de la capacité et du gain fini de l'ampop dans le CAN pipeline de 1.5-bit/étage, sans affecter ni la vitesse ni la gamme dynamique du signal d'entrée du CAN.
- Une nouvelle technique de calibration numérique obtenue en adoptant une injection de la tension de calibration imprécise opérant en arrière plan pour compenser la non-linéarité dans le CAN pipeline de multi-bits/étage.
- Un prototype de CAN 10-bit, 100 MS/s, pipeline de deux canaux temporellement entrelacés et implémentés dans la technologie CMOS standard de 0.18 μm, est présenté avec ses résultats expérimentaux. Le mésappariement du gain statique entre les canaux est compensé par la méthode de corrélation basée sur l'injection de la tension, tandis que le mésappariement du gain dynamique est réduit en utilisant la technique d'échantillonnage insensible au biais (skew) de l'horloge.

L'analyse et les résultats de ces méthodes proposées prouvent leurs capacités afin de réduire les limites technologiques et d'accroître la performance de ce CAN lorsqu'il est implémenté avec des technologies CMOS submicroniques

ABSTRACT

The fast emergence of different standards for telecommunication systems has urged the need for high-resolution wide-bandwidth analog-to-digital converters (ADCs) to accommodate nowadays applications. On the other hand, pipelined ADCs offer an excellent trade-off between die area, power consumption and throughput among the various available ADC architectures. In most ADCs, the accuracy is limited by the actual matching of nominally equal-sized passive elements and the finite operational amplifier (opamp) gain stemming from power supply voltage reduction. These matching accuracy and opamp gain are far from being compliant with the up-to-date required specifications. Moreover, mismatches in the parallel ADCs' channels, used to form a wide bandwidth time-interleaved ADC (TIADC), create unwanted in-band distortions that have to be compensated.

Knowing that the CMOS technology presents the most promising solution for SoC (System on Chip) designs and that the digital circuits scale faster than the analog circuits, using digital techniques to improve the performance of CMOS type ADC has become very attractive.

In this thesis, the following new research contributions associated with the digital background calibration of high-performance time-interleaved and pipelined ADCs are presented:

- Sampling method to improve spurious free dynamic range of TIADC. Firstly, the mathematical background describing the effect of randomizing the samples among the ADC channels in TIADC was analyzed and consequently a digitally

oriented implementation, amenable to integration in deep submicron technology, was proposed.

- Digital blind background calibration method for 1.5b-per-stage pipelined ADC without affecting the speed or the input dynamic range was presented. In this method, a simple modification to the conventional MDAC allowed the ADC to toggle between different configurations to create a reference signal used to calibrate blindly the ADC in the background.
- Multi-bit-per-stage pipelined ADC calibration using imprecise voltage injection and correlation-based background calibration with duration shortening. By injecting subtractive voltages in a modified conventional multi-bit MDAC and performing correlation based successive coefficient measurements, a background calibration was achieved.
- A prototype of two-channel 10-bit, 100 MS/s time-interleaved ADC was designed and fabricated in 0.18μm CMOS technology. The front-end S/Hs circuits of this ADC were modified to enable the injection of calibration voltage to compensate for the static gain-mismatch. Dynamic gain-mismatch was reduced by applying skew-insensitive sampling.

Analysis and experimental results of the new methods demonstrated their effectiveness to improve significantly pipelined and time-interleaved ADCs performances.

CONDENSÉ EN FRANÇAIS

1. Introduction

L'apparition rapide, de nos jours, de différentes normes pour les systèmes de télécommunications a conduit au besoin de développer de nouvelles architectures de convertisseurs analogiques-numériques (CAN), à grande largeur de bande et à haute résolution, destinés à des applications à haute vitesse [MIT00]. Parmi ces architectures, on trouve les CAN pipelines [LEW87] qui présentent un des meilleurs compromis entre la surface de la puce, la consommation de la puissance et le débit de conversion parmi toutes les architectures des CAN. Cependant, l'augmentation de la vitesse au-delà des limites des technologies d'intégration nécessite que la fréquence d'échantillonnage de l'interface analogique-numérique soit ainsi accrue en employant des CAN pipelines multiples et temporellement entrelacés [SUM01]. Aussi, dans la plupart des architectures des CAN, la précision est limitée par l'appariement réel des éléments analogiques, nominalement à taille égale, et par le gain fini de l'amplificateur opérationnel (ampop) résultant de la diminution de la tension d'alimentation. Cependant, la résolution de l'appariement et la précision du gain de l'ampop sont loin d'être conformes aux caractéristiques exigées à ce jour. D'ailleurs, le mésappariement dans les canaux parallèles utilisés pour implémenter un CAN pipeline à grande vitesse, et temporellement entrelacés, provoque des distorsions non-désirées dans la bande passante qui doivent être évitées ou compensées.

Quant à la technologie de fabrication de CAN, le CMOS (Complementary Metal-Oxide Semiconductor) submicronique présente la solution la plus prometteuse pour l'intégration de système sur une seule puce (System-on-Chip - *SoC*). Cette intégration permet la réduction de la surface et la puissance des circuits numériques plus rapidement qu'elle se permet pour les circuits analogiques. Par conséquence, la solution d'employer des techniques de calibration numérique afin d'améliorer la performance des CAN implémentés dans la technologie CMOS est devenue très attirante et convaincante.

Dans cette thèse, nous présentons de nouvelles méthodes et circuits CMOS de calibration numériques opérant en arrière plan qui sont dédiés à calibrer le CAN afin d'en réduire les limitations technologiques et d'accroître les performances.

Cette thèse est divisée en sept sections. Après une brève introduction, la section 2 présente une revue de la théorie de base des CAN pipelines et temporellement entrelacés. Dans la section 3, une nouvelle méthode d'échantillonnage, dédiée à surmonter les limitations des CAN temporellement entrelacés, est présentée. Une technique de calibration «aveugle» opérant en arrière plan pour réduire les non-linéarités provenant du mésappariement de la capacité et du gain fini d'ampop dans le CAN pipeline de 1.5-bit/étage est présentée dans la section 4. La section 5 couvre une nouvelle technique de calibration numérique opérant en arrière plan compensant la non-linéarité dans le CAN pipeline de multi-bits/étage. Un prototype de CAN pipeline de deux-canaux temporellement entrelacés et implémentés dans la technologie CMOS 0.18 μm est présenté ainsi que ses résultats expérimentaux dans la section 6. Finalement, la conclusion et des recommandations pour des travaux futures terminent ce travail dans la

section 7. Notons que toutes les références aux figures aux équations et aux indications bibliographiques dans ce document réfèrent au texte de cette thèse en anglais.

2. Problèmes de la conception des CAN pipelines et temporellement entrelacés

2.1 CAN pipeline

La figure 2.1 illustre le diagramme bloc d'un CAN pipeline général utilisant P étages. Dans cette structure pipelinée, la conversion est répartie sur plusieurs étages mis en cascade. Chaque étage (excepté le dernier représentant uniquement un CAN type flash), le signal d'entrée est d'abord quantifié en utilisant un CAN de résolution réduite (sub-CAN - SCAN), ensuite la sortie du code numérique est convertie à nouveau à un signal analogique en utilisant un convertisseur numérique-analogique à basse résolution (sub-CNA - SCNA). Ce signal analogique quantifié est alors soustrait du signal d'entrée, ayant pour résultat un résidu qui est amplifié par une valeur G égale à $2n$, où n représente la résolution d'étage. Ensuite, ce résidu est transmis à l'étage suivant et le processus est répété.

Un étage avec une résolution n fournit un mot numérique de $n+1$ bit qui est transmis au bloc numérique de correction d'erreurs. Ce dernier contient des registres à décalage et des circuits numériques de correction. La redondance d'un symbole binaire dans chaque étage est habituellement désignée sous le nom de redondance de 0.5 bit. Ainsi, un étage avec une résolution de 1-bit et un symbole binaire redondant par étage est décrit comme un module à 1.5 bit/étage. Cette redondance compense le décalage du comparateur utilisé dans le SCAN [LEW87].

L'avantage principal de la conversion en plusieurs étages pipelines est l'augmentation du taux de la conversion, puisqu'il y a une conversion complète à chaque période de l'horloge. En outre, la taille de la puce est réduite puisque la résolution est linéairement liée au nombre d'étages pipelinés.

Dans la réalisation d'un CAN pipeline par des circuits à capacités commutées, les opérations du SCNA, incluant la soustraction, et l'amplification sont conjointement combinées et désignées sous le nom du CAN multiplicateur (CNAM). Le SCAN est composé du CNA flash et d'un encodeur numérique. Un étage pipeliné, basé sur le CNAM à 2.5 bit/étage est illustré dans la Fig. 5.3.

La tension du résidu reliée à l'étage *i* peut être dérivée par l'éq. (5.1). Tels que $C_T = C_f + C_1 + C_2 + C_3$, $G_C = C_T/C_f$, et $G_A = 1/(1+1/Af)$ dont A représente le gain DC de l'ampop, f représente le facteur de rétroaction donné par $f = C_f/(C_T + C_p)$, C_p représente la capacité parasite connectée à la masse virtuelle et V_{os} représente la tension de décalage. La sortie du SCNA est donnée par $V_{daci} = ((d_1.C_1 + d_2.C_2 + d_3.C_3)/C_T) \cdot V_R$, où V_R représente la tension de référence et d_i représente la sortie numérique du SCAN dont $d_i \in \{-1, 0, 1\}$ et $d = \sum_{i=1}^{3} d_i$.

La figure 5.3(b) illustre le tracé du résidu d'un CNAM réel de 2.5-bit donné par l'éq. (5.1) et comparé à celui idéal. Cependant, la non-linéarité du SCNA et l'erreur du gain entre étages introduisent le mésappariement dans les sauts du résidu aux différentes bornes du code numérique d_i. Ces erreurs produisent des discontinuités dans la relation d'entrée-

sortie du CNA non-calibré et par conséquent provoquent des distorsions harmoniques qui vont dégrader considérablement la performance du CNA.

2.2 CAN temporellement entrelacé

Figure 3.1 illustre un diagramme bloc du CAN temporellement entrelacé (CAN-TE). Chaque canal du CAN (CNA_1, CNA_2, ..., CNA_M) opère, respectivement, à une phase d'horloge parmi M (CK_1, CK_2, ..., CK_M) et au taux d'échantillonnage f_s/M, où M et f_s désignent, respectivement, le nombre de canaux parallèles du CNA et la fréquence globale de l'échantillonnage. Idéalement, tous les canaux du CNA-TE possèderaient la même fonction de transfert.

Malheureusement, n'importe quel mésappariement entre les canaux du CAN-TE mène à une dégradation de la performance de la linéarité. En particulier, les mésappariements de décalage, du gain et du biais de l'horloge (skew) engendrés dans les canaux parallèles sont imprévisibles et ils produisent des distorsions harmoniques dans la bande passante du signal d'entrée. Ces distorsions empirent la plage dynamique exemptée des parasites (Spurious Free Dynamic Range - *SFDR*) et par conséquent dégradent la performance du rapport signal sur bruit et la distorsion (Signal to Noise and Distortion Ratio - *SNDR*).

2.3 Calibration des CAN pipelines et temporellement entrelacés

Plusieurs techniques de calibration ont été proposées afin de surmonter les limitations reliées à la technologie et d'accroître la linéarité des CAN pipelines et temporellement entrelacés. Cependant, chaque méthode présente des avantages et des limitations. La

méthode d'avant plan [SUM02a] par exemple, interrompt l'opération normale du CAN. Quant à la méthode de la moyenne de l'erreur [CHI04a], elle augmente la résolution tout en diminuant la bande passante du CAN. Aussi, l'addition d'un signal de calibration avec le signal d'entrée [JEW97] entraîne une diminution de la gamme dynamique utile du convertisseur. Cependant, l'ajout des convertisseurs et des circuits analogiques [CHU04b] augmente largement la complexité et le coût du CAN. Dans les sections suivantes, nous présentons de nouvelles méthodes et techniques de calibration du CAN pipeline et temporellement entrelacé surmontant les limitations de ces méthodes existantes.

3. **Nouvelle méthode d'échantillonnage pour les CAN-TE à large bande**

L'échantillonnage à un taux élevé peut être réalisé par plusieurs canaux d'un CAN pipeline (section 2.2). Cependant, les mésappariements entre les canaux du CAN infligent un modèle de distorsion additif et périodique à la sortie du CAN-TE. Dans ce qui suit, M et $T = 1/f_s$ représentent, respectivement, le nombre des canaux en parallèles et la période de l'échantillonnage globale du CAN-TE.

Quand un signal d'entrée de forme d'ondes sinusoïdale, de fréquence f_{in} et d'amplitude A_0, est appliqué à l'entrée du CAN-TE et que les erreurs du gain et de décalage sont présentées en ajoutant des termes dépendants du canal a_m et d_m, respectivement; le spectre du signal résultant à la sortie du CAN-TE est donné par l'éq. (3.1). Cette équation montre que les erreurs du gain et de décalage présentent des raies indésirables, centrées aux fréquences $kf_s/M \pm f_{in}$ et kf_s/M.

Par exemple dans le cas d'un CAN à quatre canaux, la sortie de CAN-TE est une séquence constituée des échantillons prélevés à partir de chaque canal dans l'ordre suivant : CAN_1, CAN_2, CAN_3, CAN_4, CAN_1, etc. Cette séquence périodique crée des raies centrées aux fréquences $kf_s/4 \pm f_{in}$ et $kf_s/4$. Dans ce qui suit, nous étudierons les raies produites par l'erreur de décalage d_m, et nous considérons l'étude d'un CAN à quatre canaux. Pour $k = 1$, nous avons des raies ayant des valeurs centrées à $f_s/4$ donnée par l'éq. (3.3) (figure 3.3(a)). Ces raies centrées à $f_s/4$ et aux autres fréquences dégradent le SFDR à des valeurs intolérables.

Cependant, dans le but de réduire la concentration des raies reliée à ces fréquences, une certaine permutation à l'intérieur de la séquence $d_0d_1d_2d_3$ est requise. Par exemple, cette permutation peut être de l'ordre de $d_0d_2d_1d_3$ ou n'importe quel autre ordre de permutation. Tout d'abord, si nous effectuons une permutation aléatoire des échantillons à l'entrée du CAN-TE, nous devons remplacer M dans l'éq. (3.1) par la période de cette séquence aléatoire. En d'autres termes, si un générateur de nombre binaire pseudo-aléatoire de période P est employé afin de contrôler cette permutation aléatoire, les séquences qui se répètent périodiquement, pour chaque N échantillons égal à $4P$, sont donc obtenues et la période de la DFT donnée par l'éq. (3.1) deviendra $N = 4P$. Et par conséquent, l'erreur du mésappariement est distribuée d'une manière que nous pouvons trouver d_i/N dans chaque direction et ce qui réduit ainsi la somme due à ce mésappariement à la fréquence $f_s/4$ ($k=M/2$), comme illustré dans la figure 3.3 (b) où P_{ij} sont données par l'éq.(3.5). Quand N est élevé, ces P_{ij} sont presque égales à $P/4$ pour chaque valeur de i et la somme de l'erreur due à chaque mésappariement est réduite au

minimum. Une technique pour mettre en application une permutation aléatoire presque complète concerne à ajouter plusieurs CAN aux M canaux du CAN-TE. Par conséquent, à un instant donné, deux CAN peuvent être disposés à recevoir deux échantillons aléatoirement choisis du signal d'entrée.

Ici nous proposons une solution de permutation aléatoire complète qui ne nécessite pas une complexité matérielle analogique supplémentaire mais en revanche, elle est basée sur des circuits numériques simples. Premièrement, supposons que nous pouvons permuter aléatoirement entre d_0 et d_1 et également entre d_2 et d_3 pendant une longue période d'échantillons de valeurs N. En effectuant cette procédure, les séquences comme ($d_0d_1d_2d_3$, $d_1d_0d_2d_3$, $d_0d_1d_3d_2$, etc..) peuvent être obtenues. Pour $f = f_s/4$, les raies sont distribuées dans chaque direction comme montré dans la figure 3.3(c).

Cette permutation aléatoire élimine complètement la raie centrée à la fréquence $f = f_s/2$ puisqu'il existe des erreurs d_i dans toutes les directions. Quant à la fréquence $f_s/4$, une grande réduction des raies est obtenue dans tous les cas sauf $d_0.d_1 > 0$ et $d_2.d_3 > 0$, dont les raies ne sont pas réduites. Cependant, afin d'obtenir une permutation aléatoire totale, nous proposons d'effectuer une technique de rotation des positions des CAN. Par exemple, au lieu d'avoir une séquence répétée à chaque N échantillons comme ($d_0d_1d_2d_3$, $d_1d_0d_2d_3$, $d_0d_1d_3d_2$,..), on peut s'arranger à avoir des séquences différentes.

Pour cela, on divise les N échantillons périodiques en quatre ensembles, le premier ensemble d'éléments peut disposer la même séquence à savoir ($d_0d_1d_2d_3$, $d_1d_0d_3d_2$), tandis que le deuxième ensemble peut être obtenu en tournant simultanément les positions de deux couples des deux CAN, résultant d'une nouvelle séquence ($d_2d_3d_0d_1$, $d_3d_2d_1d_0$), et

ensuite, on permute deux fois les deux séquences précédentes durant les N échantillons. En effectuant cette procédure, les erreurs du mésappariement d_i sont distribuées dans toutes les directions, et par conséquent, une réduction considérable de l'erreur totale est produite (figure 3.3 (d)). Cette réduction sera similaire à celle obtenue à partir de la permutation aléatoire complète des séquences. Cependant, le nombre des rotations effectuées, qui est égal à quatre dans cet exemple, est largement petit comparé au nombre N d'échantillons.

En effet, une permutation numérique aléatoire totale pour n'importe quel nombre de canaux du CAN peut être obtenue en permutant aléatoirement uniquement la distribution des échantillons entre chaque groupe de deux CAN et en effectuant la rotation parmi ces différents groupes. L'analyse et les résultats prouvent que cette méthode proposée peut être adaptée jusqu'a 5%pp de mésappariement de gain et un mésappariement de décalage atteignant $\pm V_R/10$ tout en préservant une performance de 10 bits de SFDR

4. Calibration «aveugle» opérant en arrière plan pour les CAN pipelines

Ces dernières années, l'architecture pipelinée des circuits à capacités commutées émergeait comme une approche particulièrement attrayante afin de réaliser des CAN type Nyquist ayant une moyenne-à-haute résolution et un moyen-à-haut taux de conversion. L'architecture 1.5-b/étage, où $n = 2$ avec un symbole binaire redondant, est généralement utilisée pour maximiser le taux de conversion tout en offrant une consommation raisonnable de puissance. Dans une implémentation pratique, le résidu analogique V_{i+1} de l'étage i d'un CAN pipeline utilisant 1.5-b/étage est exprimé par l' éq. (4.2). Dans cette

équation, $C_1/C_2 = 1+\alpha_i$, α_i représente le mésappariement de la capacité, ε_i représente l'erreur due au gain fini de l'ampop, et V_{ofi} représente la tension de l'offset. Prenant uniquement en considération le mésappariement de la capacité, l'éq. (4.2) peut être exprimée par l'éq. (4.3).

Cette valeur est numérisée par la partie restante du CAN de l'étage i à l'étage P (figure 4.1) dont le résultat est donné par l'éq.(4.4), où $D[V]$ dénote la valeur numérique de V.

La soustraction de l'éq. (4.4) par la valeur numérique de V_i générée par l'étage i, ($D[D_iV_r]$), comme illustrée dans la figure 4.1, donne l'éq. (4.5) où g_1 et V_g sont donnés par les équations (4.6) et (4.7).

Maintenant, en échangeant le rôle de C_1 et C_2, l'éq. (4.5) devient être exprimée par l'éq. (4.8) où g_2 est donné par l'éq. (4.9). En permutant l'étage i à une fréquence $f_s/2$ entre les deux configurations obtenues à partir de la permutation de rôle de C_1 et C_2, comme illustré dans la Fig.4.2, la tension V_g est considérée d'être échantillonnée par un CAN-TE à deux canaux où le premier canal possède un gain g_1 et le deuxième possède un gain g_2.

Basé sur la théorie du CAN-TE [CON93], la différence des gains g_1 et g_2 entre les deux canaux créera une image centrée à la fréquence $kf_s/2 \pm f_{in}$ dans le spectre du signal V_{gd} où f_{in} dénote la fréquence du signal V_g donnée par l'équation (4.7) et f_s dénote la fréquence d'échantillonnage. Le spectre du signal numérique V_{gd} est donné par l'éq. (4.10). Cette équation indique qu'un signal sinusoïdal de fréquence f_o possédera une image à la fréquence $f_{im}=f_s/2-f_o$.

Les auteurs dans [JAM02] présentent une méthode pour égaliser le gain dans un CAN-TE à deux canaux. Dans cette méthode la sortie du CAN, dans notre cas V_{gd}, est multipliée par $(-1)^n$ et le signal V_{gdc} est obtenu. Cette multiplication déplacera l'image centrée à la fréquence f_{im} à f_o et le signal d'entrée centrée à la fréquence f_o à f_{im}. La multiplication de V_{gd} par V_{gdc} dans le domaine temporel résultera à une composante DC proportionnelle au mésappariement du gain. En multipliant ensuite cette composante DC par *mu* et à l'aide d'un intégrateur, un signal *R(n)* proportionnel au mésappariement du gain est extrait. Ce signal, $R(n)$ multiplie le gain g_2 afin de forcer l'élimination de l'image. À l'équilibre, $R(n)$ convergera vers la valeur g_1/g_2. Ce rapport de gain est employé afin de corriger le mésappariement de la capacité et le gain fini de l'ampop.

Des simulations ont été effectuées afin de vérifier l'efficacité de cette nouvelle technique de calibration opérant en arrière plan. Un mésappariement de la capacité de 3% et une tension de décalage du comparateur de $\pm V_R/10$ ont été ajoutés dans tous les étages d'un CAN pipeline de 15 bits.

Un signal sinusoïdal à amplitude pleine échelle et de fréquence égale à 1/20 la fréquence d'échantillonnage (f_s) a été appliqué à l'entrée du CAN avant et après le calibrage. Cependant, avant la calibration, le SNDR est de l'ordre de 43.9 dB, ayant pour résultat un nombre de bits effectifs (Effective Number Of Bit - *ENOB*) égal à 7 bits, et un SFDR de l'ordre de 47 dB. Aussi, après la calibration le SNDR devient de l'ordre de 89.3 dB, correspondant à un ENOB de 14.5 bits, et par conséquent, le SFDR est amélioré jusqu'au 103 dB.

5. Calibration numérique en arrière plan en utilisant l'injection de tension imprécise

Pour des CANs pipelines de haute résolution, la conversion de plusieurs bits par étage diminue généralement la consommation de puissance [CLI96]. Ceci est principalement dû au fait que la conversion de plusieurs bits par étage réduit considérablement le nombre total d'étages nécessaires.

Ainsi, comme mentionné dans la section 2.1, la non-linéarité du SCNA et l'erreur du gain entre étages introduisent le mésappariement dans les sauts du résidu aux différentes bornes du code numérique comme illustré dans la Fig. 5.3. Cependant, en mesurant précisément la valeur des sauts $G_A(C_i/C_f)V_R$ dans le résidu et en employant l'équation (5.2), la sortie du résidu devient linéaire si elle se référera à l'entrée de l'étage *i* en dépit des erreurs produites du SCAN et du gain fini de l'ampop.

Après cette correction en utilisant l'éq. (5.2), le CAN, composé maintenant de l'étage *i* et les étages suivants, est linéaire avec un gain global $G_A \cdot G_C$. Dans la technique de calibration proposée, le terme $G_A(C_i/C_f)V_R$ est mesuré à partir de différentes valeurs de C_i afin de permettre la correction en utilisant l'éq. (5.2).

Un schéma du CNAM de 2.5-bit utilisant le calibrage proposé est illustré dans la Fig. 5.4. La modification apportée au CNAM par rapport au conventionnel est l'ajout d'une capacité supplémentaire C_4 et de quelques circuits de contrôle numérique. En outre, la tension $V_1 \cdot P_N$ est échantillonnée par la capacité de rétroaction C_f quand ϕ_1 est élevée, tel

que P_N est un signal pseudo-aléatoire alternant entre 0 et 1. La capacité C_4 est utilisée au lieu de C_f pour échantillonner la tension d'entrée quand ϕ_1 est élevée.

En effectuant cette procédure, une tension égale à $G_A \cdot V_1$ est injectée dans la sortie du résidu. Cependant, afin de ne pas trop limiter la plage de tension allouée pour la correction de la tension de décalage du SCAN, la tension V_1 doit être suffisamment petite. Pour cette raison, une tension $V_2 \cdot P_N$ est échantillonnée par la capacité C_4 dans la phase suivante où la phase ϕ_2 est élevée. En injectant ces tensions suivant cette procédure, une tension est prélevée à la sortie du résidu de l'étage sous-calibrage est donnée par l'éq. (5.3). Tel que $G_C = (C_1 + C_2 + C_3 + C_4)/C_f$ et V_{o1} désigne le terme restant dans la tension V_o qui représente la sortie du résidu dans l'absence des tensions injectées.

En effectuant une corrélation entre la valeur numérisée $D[V_o]$ de la sortie du résidu V_o et P_N, le terme $\Delta V = G_A \cdot (V_1 - (C_4/C_f)V_2)$ est mesuré. De plus, le terme $G_A(C_4/C_f)V_R$ est obtenu par l'injection des tensions de calibration et en effectuant des mesures successives des coefficients. En effet, pour mesurer le premier coefficient (g_1), la tension V_1 est choisie égale à $(K-1)V_R/K$ et la tension V_2 est égale à V_R, où K est un entier pair. Dans ce cas, le terme égal à g_1, représentant le premier coefficient, serait mesuré. Aussi, pour mesurer le 2ieme coefficient (g_2), la tension V_1 est choisie égale à $(K-1)V_R/K$ et la tension V_2 est égale à $(K-2)V_R/K$. Ainsi, pour mesurer le coefficient g_{K-1}, la tension V_1 est choisie égale à V_R/K et la tension V_2 est égale à $2 \cdot V_R/K$. Et finalement, pour mesurer

le coefficient g_K, la tension V_1 est choisie égale à V_R/K et la tension V_2 est reliée à la masse. Le terme $G_A(C_4/C_f)V_R$ est obtenu par l'éq. (5.8).

La même procédure est répétée pour chaque capacité dont les multiplexeurs illustrés dans la Fig. 5.4 choisissent la capacité correspondante à la valeur à mesurer et acheminent sa ligne de contrôle numérique à une capacité de remplacement.

Des simulations ont été effectuées afin de vérifier l'efficacité de la technique proposée de calibrage dans un CAN pipeline de 14-bit. Un mésappariement de la capacité de ±0.2%, une tension de décalage du comparateur de $\pm V_R/12$ et un gain DC de l'ampop de l'ordre de 60 dB ont été ajoutés dans tous les étages.

Un signal sinusoïdal à amplitude pleine échelle et de fréquence égale à 1/20 la fréquence d'échantillonnage (f_s) a été appliqué à l'entrée du CAN de 14-bit avant et après la calibration. Nous avons obtenu avant la calibration un SNDR de l'ordre de 64 dB, ayant pour résultat un ENOB égal à 10.3 bits, et un SFDR de l'ordre de 68.4 dB. Après le calibration, le SNDR devient de l'ordre de 84 dB, ayant pour résultat un ENOB égal à 13.7 bits, et par conséquent, le SFDR s'est accru à 98 dB.

6. CAN-TE pipeline à 2 canaux de 10-b et 100-MÉ/s

Dans cette section, un CAN–TE pipeline à deux canaux, conçu et fabriqué dans la technologie CMOS standard 0.18µm, est présenté. Le diagramme bloc de ce CAN proposé est illustré dans la Fig. 6.1. Chaque canal possède à l'entrée un échantillonneur-bloqueur (É/B) d'une large bande passante et implémenté en employant une architecture de neuf étages pipelinés en cascade d'une résolution de 1.5-bit-par-étage. Cependant,

chaque étage est composé d'un CNAM suivi d'un CAN complètement différentiel d'une résolution de 1.5 bit-par-étage.

Cependant, le mésappariement du gain statique entre les canaux est compensé en utilisant la méthode de calibration opérant en arrière plan basée sur l'injection de la tension sans affecter la gamme d'entrée du CAN comme présenté dans la section 3. De même, le mésappariement du gain dynamique, due à l'établissement incomplet de la tension à la sortie de l'É/B, est réduit en employant la technique d'échantillonnage insensible au biais de l'horloge, appliquée au premier étage de chaque canal du CAN pipeline.

Ainsi, afin de réduire la consommation de la puissance et la surface de la puce, le partage de l'ampop entre deux étages consécutifs du CAN pipeline est employé. Les commutateurs additionnels dédiés à réaliser le partage conventionnel de l'ampop engendrent des capacités supplémentaires à l'entrée de l'ampop. En conséquence, ces capacités supplémentaires accumulées avec les capacités disposées à l'entrée de l'ampop ne sont jamais remises à zéro entre les échantillons ce qui introduira une non-linéarité dans le CAN. Afin de réduire la non-linéarité du CAN, nous proposons un ampop à quatre entrées dont chaque CNAM dispose deux entrées désignées. Cet ampop proposé est illustré dans la Fig. 6.5. Cet ampop est implémenté en utilisant une architecture complètement différentielle à deux étages d'amplification avec une compensation type Miller. Cet ampop fournit à la fois une performance au niveau du gain DC de l'ordre de 78 dB et au niveau de la fréquence du gain unitaire de l'ordre de 400 MHz.

Le convertisseur est implémenté et fabriqué dans la technologie CMOS de TSMC standard 0.18µm. Ce CAN consomme 76 mW et occupe une surface de 3.6 mm^2. La Fig. 6.15 présente le spectre de la sortie du CAN avant et après le calibrage. Le signal d'entrée, appliqué à ce convertisseur, est un signal sinusoïdal en pleine échelle de 1.6Vpp et de fréquence (f_{in}) de 3.99 MHz telle que la fréquence de l'échantillonnage (f_s) est égale à 100 MHz. Avant la calibration, le SNDR et le SFDR mesurés étaient de l'ordre de 48dB et 57dB, respectivement. La performance est limitée par l'existence des raies de distorsion, due au mésappariement de l'offset, de l'ordre de -57dBc à la fréquence $f_s/2$ d'une part et d'autre part due au désappareillement du gain de l'ordre de -61dBc à la fréquence $f_s/2$-f_{in}. Après la calibration, le SNDR et le SFDR sont améliorés à 57dB et à 69dB, respectivement. Le tableau 6.2 récapitule les performances mesurées.

7. Conclusion et recommandations

Dans cette thèse, nous avons examiné la calibration numérique opérant en arrière plan de CNA pipeline et temporellement entrelacé. Les nouvelles contributions proposées dans cette recherche ont été présentées et sont récapitulées comme suit:

- Une nouvelle méthode d'échantillonnage, implémentée dans le domaine numérique, dédiée à surmonter la limitation de CAN temporellement entrelacé.
- Une technique de calibrage «aveugle» surmontant les non-linéarités provenant du mésappariement de la capacité et du gain fini de l'ampop dans le CAN pipeline de 1.5-bit/étage, sans affecter ni la vitesse ni la gamme dynamique du signal d'entrée du CAN.

- Une nouvelle technique de calibrage numérique obtenue en adoptant une injection de la tension de calibration imprécise opérant en arrière plan compensant la non-linéarité dans le CAN pipeline de multi-bits/étage.
- Un prototype de CAN pipeline de deux canaux temporellement entrelacés, et implémenté dans la technologie CMOS standard de 0.18 μm est présenté avec ses résultats expérimentaux. Le mésappariement du gain statique entre les canaux est compensé par la méthode de corrélation basée sur l'injection de la tension tandis que le mésappariement du gain dynamique est réduit en utilisant la technique d'échantillonnage insensible au biais de l'horloge.

Finalement, nous présentons certaines recommandations pour des recherches futures reliées à la conception du CAN pipeline, temporellement entrelacé de haute performance:

- Étudier la limitation pratique liée à la consommation de la puissance des CAN, et développer une architecture et des circuits mixtes afin d'atteindre la limite optimale de cette consommation. Une solution destinée à réduire cette dernière peut être réalisée en substituant l'ampop par un circuit analogique imprécis nécessitant une faible consommation de puissance. Un tel circuit peut être basé sur un circuit passif à capacité commutée à faible linéarité. Les méthodes proposées dans cette thèse peuvent être utilisées pour calibrer les non- linéarités des CAN basés sur cette sorte des circuits imprécis.
- Vérification expérimentale des méthodes proposées, en particulier la méthode de calibration «aveugle» grâce à sa faible complexité d'intégration au niveau des circuits analogiques et sa performance prometteuse.

- Dans le SoC à haute densité d'intégration, le couplage des circuits numériques avec les modules analogiques génère un bruit se propageant dans les substrats communs. Ce phénomène de propagation est appelé le couplage de substrat. Malheureusement, ce couplage de substrat dégrade l'intégrité des signaux analogiques dans les circuits mixtes en y injectant des perturbations de l'ordre des centaines de millivolts durant les transitions de l'horloge. Pour cette bonne raison, la modélisation de l'effet de ce bruit sur la performance du CAN et la proposition de solution est un sujet de recherche vivement recommandé.

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LIST OF ABBREVIATIONS

ADC	Analog-to-Digital Converter
BPF	Bandpass Filter
CDS	Correlated Double Sampling
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
DCR	Direct Conversion Receiver
DNC	DAC Noise Cancellation
DNL	differential nonlinearity
DFCA	DAC and Feedback Capacitor Averaging
DFT	Discrete Fourier Transform
DRR	Digital Radio Receive
FS	Full-Scale
GEC	Gain Error Correction
ICM	Input Common Mode
IF	Intermediate Frequency
INL	integral nonlinearity
IR	Image Reject
LMS	Least Mean Square
LNA	Low Noise Amplifier
LSB	Least Significant Bit
MDAC	Multiplying Digital-to-Analog Converter
MNC	Mismatch Noise Cancelling
MSB	Most Significant Bit
PRBG	Pseudo-Random Bit Generator number
RF	Radio Frequency

SADC	Sub Analog-to-Digital Converter
SCM	Successive Coefficient Measurement
SCV	Subtractive Calibration Voltage
SDAC	Sub Digital-to-Analog Converter
SD-CGC	Subtractive Dither-Continuous Gain Correction
SDR	Software Defined Radio
SFDR	Spurious Free Dynamic Range
S/H	Sample and Hold
SMA	SubMiniature version A
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
SoC	System on Chip
TIADC	Time-Interleaved ADC
TSMC	Taiwan Semiconductor Manufacturing Company

LIST OF SYMBOLS

α_i	Capacitor mismatch
Δ	Quantization error
ϕ_1	Sampling phase
ϕ_2	Amplifying phase
μm	Micrometer
σ^2	Variance
A	Finite opamp gain
C_p	Virtual ground parasitic capacitance
dB	Decibel
dBm	dB referenced to one milliwatt
d_i	Digital output code
E[ ]	Expected value
f	Feedback factor
f_s	Sampling frequency
g_m	Gate small-signal transconductance
G_A	Interstage gain due to the finite opamp gain
G_C	Interstage gain due to sub-DAC
G_i	Interstage gain of stage i
MHz	Megahertz
MS/s	Mega-sample-per-second
n	Stage resolution
N	Number of bits
V_{daci}	SDAC analog output of stage i
V_{i+1}	Output residue of stage i
V_{os}	Input-referred offset voltage

V_R	Reference voltage
T	Time
V	Voltage
W	Watt

Chapter 1

INTRODUCTION

1.1 Trends and Motivation

The continuous growth of demand for wireless communications has led to the proliferation of different standards. The highly competitive market demands low-cost, low-power, and small form-factor devices. This calls for the development of single-chip receivers capable of adapting to the various communication standards, preferably in low-cost technologies [LI02]. New transceiver architectures are evolving toward enabling software defined radio (SDR) to allow global roaming for wireless users.

The ideal SDR receiver [MIT00] has very few analog stages: the only analog components are the antenna, the bandpass filter (BPF), the low noise amplifier (LNA), and the analog-to-digital converter (ADC) as illustrated in Fig. 1.1.

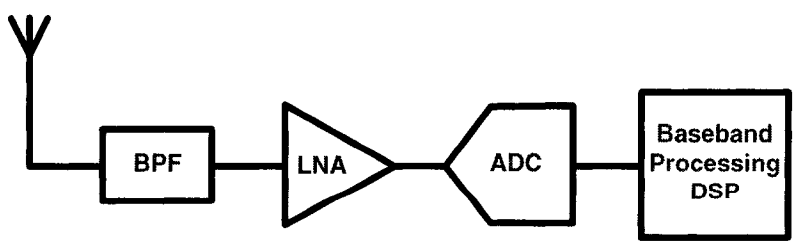

Figure 1.1: An ideal SDR receiver.

In this architecture, analog-to-digital conversion is achieved immediately at the radio frequency (RF) in order to process the signal completely in the digital domain. In

addition to the difficulty concerning the design of wide bandwidth LNAs and antennas, this architecture puts stringent requirements on the analog-to-digital converter (ADC). To sample directly the RF input signals, which can rise to several giga-hertz, an ADC capable of handling signals ranging from –120 dBm to –30 dBm is needed [BUR00]. An ADC with sampling rate of several gigahertz and a dynamic range around 90 dB is far from being realized due to technological, technical, and fundamental physical limitations with today's technologies. Moreover, the configurability of the receiver means that its front-end interface should be highly adjustable. This configurability is difficult to obtain at the analog side of the receiver and for this reason it should be transferred to the digital domain. Thus, the most promising nowadays solutions for receivers are the digital radio receiver (DRR) and the direct conversion receiver (DCR) [MIR00], shown in Figs. 1.2 and 1.3 respectively.

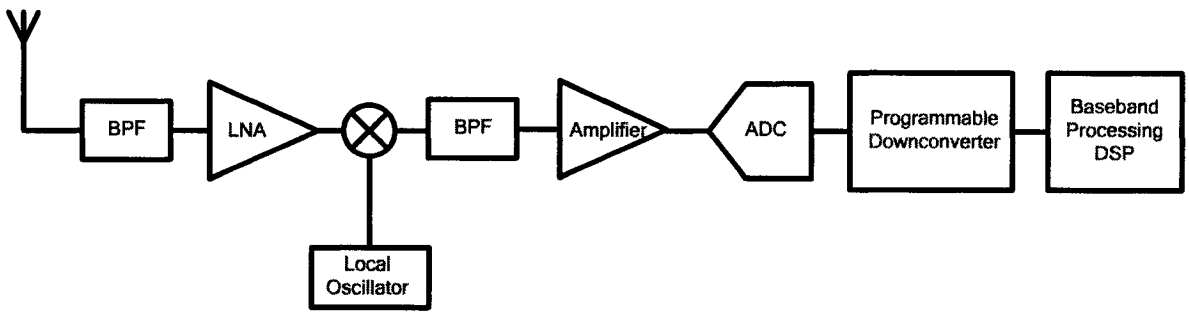

Figure 1.2: The digital radio receiver architecture employing IF-sampling.

In DRR, the ADC samples the overall spectrum allocated to the system at an intermediate frequency (IF) selected upon a compromise between selectivity and sensitivity of the receiver. It is desirable to choose a high IF to reduce the requirements

on the image reject (IR) filter to make it implementable on-chip. For a sufficiently high IF, the band selection filter can play the role of IF filter as well [RAZ97].

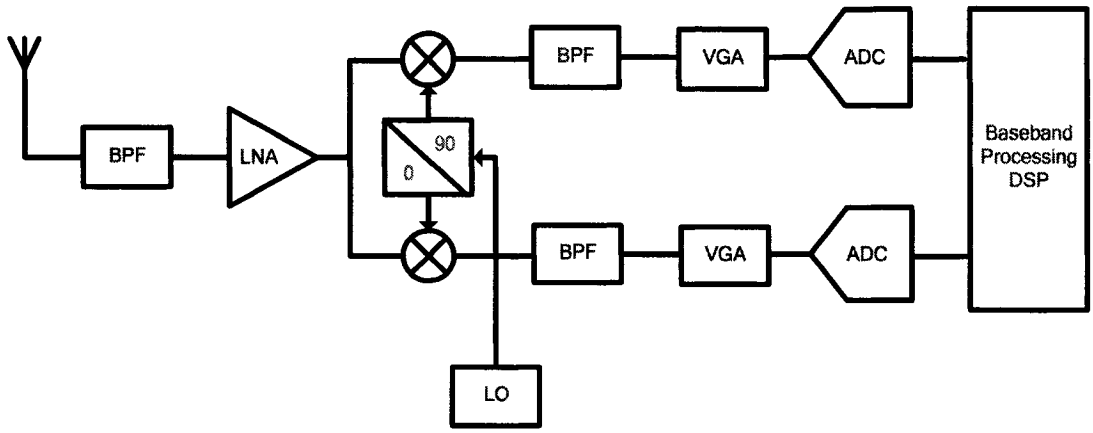

Figure 1.3: The direct conversion architecture.

The programmable downconverter (Fig. 1.2) deals with down conversion, channelization and sample rate adaptation. This kind of receiver overcomes some problems of the DCR architecture such as dynamic dc offset, flicker noise and second-order intermodulation. Also this DRR has the advantage of avoiding I and Q mismatches in DCR. However, this technique requires a fast and high resolution ADC that is currently limiting its utilization almost to base stations only. Providing wide bandwidth, high resolution and low power ADC, the DRR architecture becomes also a viable solution for mobile receivers.

In DCR, the desired channel is centered at zero frequency (DC), which relaxes the sampling frequency required from the ADC. Solving the shortcomings of the DCR could make it the most favorable solution for mobile receivers.

Since signal processing functions are moved to the digital domain, where all nonidealities of the analog domain can be avoided, the ADC stage has become a key

bottleneck in these developments. Therefore in DRR and DCR, ADCs with specifications ranging between 50 to 200 MS/s, and 10 to 14 bits with high spurious free dynamic range (SFDR) are required.

Since the complementary metal oxide semiconductor (CMOS) technology permits the free mixture of analog and digital functions owing to its inexpensive fabrication process and its superiority for the digital applications, CMOS is the best technology for the SoC (System on Chip) design that enables single chip transceivers.

On the other hand, pipelined ADCs offer an excellent trade-off between die area, power consumption and throughput among all the ADC architectures [LEW87]. For this reason the pipelined ADC in CMOS technology is the perfect choice for DRR and DCR receivers. Moreover, to increase the speed beyond the technological limit of the CMOS technology: the sampling frequency of the analog-to-digital interface can be increased by using multiple ADCs that are time interleaved [SUM01].

1.2 Research Problem

In the following paragraphs we will state the major limitations facing the implementation of the high dynamic range wide-bandwidth pipelined ADCs in CMOS technologies:

A. In most ADCs, the accuracy is limited by the actual matching of nominally equal-sized analog elements (resistors, capacitors, or current sources). This matching accuracy is far from being compliant with the up-to-date required specifications. To improve matching between components, their geometrical sizes and therefore the area

of the circuit increases. Large analog elements (e.g. capacitors) limit the speed of the ADC and increase also its power consumption.

B. The supply voltage of digital CMOS circuits is decreasing to minimize the power consumption per logic cell. In addition, the shrinking of device dimensions lowers the maximum allowed supply voltage. While high-performance ADCs rely on fast and high gain operational amplifiers (opamps), lowering the supply voltage reduces the available signal swing and makes the design of high gain opamp topologies with many stacked transistors unfeasible. One way to overcome this problem is to use multistage opamps with nested Miller-effect compensation. Although such opamps can give large enough gains, they slow down the frequency compared to simple single-stage structures.

C. To achieve higher sampling rates, parallelism can be introduced to multiple ADC channels to form a single wide bandwidth time-interleaved ADC (TIADC). In CMOS technology, TIADCs using pipelined ADCs for the parallel channels represent the most suitable solution to obtain high frequency and resolution simultaneously. Mismatches in the parallel ADCs channels create unwanted in-band distortions that have to be avoided or compensated. For nowadays configurable receivers, the digital channel selection is performed after digitizing the whole utilized spectrum, with wide bandwidth high dynamic range TIADC needed to support a large number of wireless standards. Channel selection after the ADC will increase the signal-to-noise ratio (SNR) but it cannot overcome distortion in the ADC bandwidth, which makes the SFDR a very important parameter to feature the efficiency of an ADC for

telecommunication applications. TIADCs, as we mentioned earlier, suffer from in-band distortions that undermine the SFDR performance.

The aforementioned problems motivate the development of calibration methods to compensate for the technological limitations and enhance the ADCs performance. Knowing that the digital circuits in current deep submicron technologies scale faster in terms of power and area compared with the analog circuits, digital solutions to improve ADC performance are now very attractive.

1.3 Research Contributions

The contributions presented in this thesis have been reported in several journals and conferences as summarized below.

- We presented, in [ELS03] and [ELS04a], a new sampling method to overcome the limitation of time-interleaved analog-to-digital converters (TIADC). Ideally in TIADC all the channels would have the same transfer function. In fact, mismatches between these channels inflict periodic additive spurious components to the output that undermine the ADC performance. To overcome this problem in the digital domain, a randomizing and rotation technique to average out the effect of the mismatches among the ADC channels was proposed. The mathematical background describing the effect of randomizing the samples among the ADC channels was analyzed and consequently a digitally oriented implementation, amenable to integration in deep submicron technology, was proposed. Analysis

and results of the new method demonstrated its effectiveness to improve significantly the TIADC performance.

- In [ELS04b], we proposed a new digital background calibration technique to compensate the capacitor mismatch in pipelined ADCs. A major limitation in the switched-capacitor pipelined ADC is the capacitor mismatch due to the finite resolution of the technology. In this work, a digital signal from the ADC output is constructed so as to transform the capacitor mismatch to gain error. A simple modification to the conventional multiplying digital-to-analog converter (MDAC) allows the ADC to toggle between different configurations to create a reference signal used to calibrate blindly the ADC in the background. The creation of this signal does not produce any limitation for the ADC in terms of speed or degradation of the input dynamic range. Also, we extended this to calibrate in the background the finite opamp gain in one-bit/stage pipelined ADCs [ELS04c].
- In [ELS06a], a method to calibrate multi-bit/stage pipelined ADC has been presented. According to one aspect of this method, a new digital background calibration technique to compensate for the nonlinearity and gain error and opamp finite dc gain in multi-bit/stage pipelined ADC was provided. By injecting subtractive voltages in a modified conventional multi-bit multiplying digital-to-analog converter (MDAC) and performing correlation based successive coefficient measurements, a background calibration was achieved. This calibration does not need accurate calibration voltages or increasing the MDAC resolution and the coefficients measurement is independent from the input signal.

Further, we presented a global gain correction for time-interleaved ADCs. Techniques to shorten the calibration duration are further provided. This method demonstrates linearity improvement by several bits in single and multi-channel multi-bit/stage pipelined ADC.

- A two-channel, 10-bit, 100-MS/s, time-interleaved pipelined ADC was designed and fabricated in 0.18μm CMOS technology. Static gain mismatch between the channels was compensated for by a background correlation scheme based on voltage injection without affecting the ADC input range as we proposed in [ELS06a]. Dynamic gain mismatch due to incomplete linear settling in the front-end S/Hs was reduced by applying skew-insensitive sampling in the first stage of every pipelined ADC channel. Power consumption and chip area were minimized by using four-input opamps sharing and comparators' preamplifiers sharing between each two consecutive stages. At sampling rate of 100 MS/s, this ADC achieved peak signal-to-noise-and-distortion ratio (SNDR) and SFDR of 57 dB and 69 dB respectively for a 3.99 MHz input signal, and it consumes 76 mW from 1.8 V power supply.

1.4 Thesis Organization

The thesis is organized into seven chapters. After the introduction, chapter 2 reviews the basic theory of pipelined and time-interleaved ADCs and their known calibration methods. In chapter 3, a new sampling method to overcome the limitation of TIADCs is presented. Blind background calibration techniques to overcome the nonlinearities

stemming from capacitor mismatch and finite opamp gain in 1.5-bit/stage pipelined ADC are presented in chapter 4. Chapter 5 covers a new digital background calibration technique to compensate for the nonlinearity in multi-bit/stage pipelined ADC. A prototype 2-channel calibrated TIADC fabricated in 0.18 μm CMOS technology is presented in chapter 6. Finally, we conclude in chapter 7 with main contribution's summary and recommendations for future research works.

Chapter 2

PIPELINED AND TIME-INTERLEAVED ADCs: ARCHITECTURES AND CALIBRATION METHODS

2.1 Introduction

Modern analog to digital converters are divided into two main categories, Nyquist-rate ADCs, and oversampled ADCs [WAL99]. Flash and pipelined ADCs are Nyquist-rate type. Sigma-delta ADCs belong to the oversampled ADC category. Although the pipeline architecture is inherently not as fast as a flash scheme, its serial nature results in a linear scaling of power and area with resolution, as opposed to the exponential scaling which occurs in a flash, resulting in the pipelined architecture being a more attractive solution around and above the 10 bit resolution level. Similarly, for very high resolution conversion, sigma delta architectures are generally used. However the oversampling nature of such schemes limits the maximum speed to a fraction of the fastest possible sampling rate. Thus, pipelined ADC is an excellent architecture to realize wide bandwidth ADC with high resolution. To increase the speed beyond the technological limits, time-interleaving several pipelined ADCs will increase the global sampling frequency, enabling the realization of high resolution and high speed ADCs suitable for direct conversion IF/RF transceivers. This chapter focuses on the architectures and nonidealities of pipelined and time-interleaved ADCs. The final section of the chapter reviews existing techniques to calibrate these ADCs.

2.2 Pipelined ADC

2.2.1 Basic Operation

Figure 2.1 shows the block diagram of a general pipelined ADC with P stages. In each stage (except the last stage which has only a flash ADC), the input signal is first quantized by a sub-ADC (SADC), then the output digital code is converted back to an analog signal by a sub-DAC (SDAC). This quantized analog signal is then subtracted from the input signal, resulting in a residue that is amplified by a gain G equals to 2^n, where n is the stage resolution. This residue is sent to the following stage and the process is repeated.

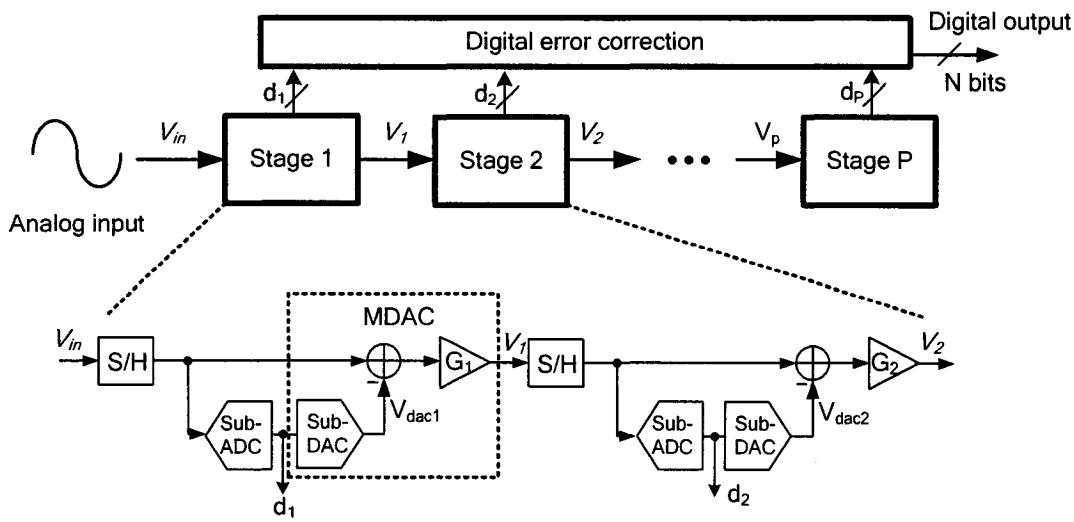

Figure 2.1: Diagram of the conventional multi-bit/stage pipelined ADC.

The output residue V_{i+1} of stage i is expressed as:

$$V_{i+1} = G_i \cdot (V_i - V_{daci}) \tag{2.1}$$

where V_{daci} and G_i are the SDAC analog output and the interstage gain of stage i respectively. The input of the entire pipelined ADC can be obtained by:

$$V_{in} = V_{dac1} + \frac{V_{dac2}}{G_1} + \frac{V_{dac3}}{G_1 G_2} + \cdots + \frac{V_{dacp}}{G_1 G_2 \cdots G_{p-1}} + \Delta \qquad (2.2)$$

where Δ stands for the quantization error of the entire ADC.

According to eq.(2.2), the input signal can be accurately generated when the effective values of V_{daci} and G_i are used. A stage with resolution n provides an $n+1$ bit digital word which is sent to the digital error correction block. The digital correction block contains shift registers and digital correction logic circuits. The one binary symbol redundancy in each stage is usually referred to as the 0.5 bit redundancy. Thus, a stage with a one-bit resolution and one-bit redundancy is named 1.5 bit/stage. This redundancy allows compensating for the comparator offset [LEW87], as explained in section 2.2.2 later.

Each stage performs conversion every two clock phases. This means that the components in each stage must settle to its final value in half of the clock period. Since alternate stages work in different clock cycles, as the sample moves from one stage to the next, the previous stage can take in a new sample as the old sample is processed by the following stage. This models a pipelined processing system. After the initial sample is clocked through all stages, the first digital output is available from the digital error correction block that creates initial latency period. After this period, one digital output is available at each successive clock cycle.

The key advantage of pipelining the conversion into many stages is the resulting high conversion rate, since there is one complete conversion per clock cycle. In addition, compared to a flash converter, the overall chip size is reduced since the resolution is linearly related to the number of pipeline stages. One disadvantage of pipelined

architecture is its inherent latency period. This precludes the use of pipelined ADC in applications where this latency represents a problem.

2.2.2 Error Sources in Pipelined ADCs

In switched-capacitor implementations of a pipelined ADC, the functions of SDAC, subtraction, and amplification are usually combined together and referred to as the multiplying digital-to-analog converter (MDAC). The SADC is composed from flash ADC and a digital encoder.

For the sake of simplicity, we study the error sources in pipelined ADC using 2.5 bit/stage architecture where $G = 2^2$, the resolution $n = 2$ with 1-bit redundancy. A one stage pipelined, based on "capacitor-flip-over" 2.5 bit/stage MDAC and SADC, and its clocks control signals relation are shown in Fig. 2.2.

During the sampling phase (ϕ_1 is high), the input voltage V_i presented to stage i is sampled on C_1, C_2, C_3 and C_f. At this time, the comparators matrix of the SADC compares V_i with the references $\frac{1}{2^3}(2i+1)V_R, i \in \{-3,-2,-1,0,1,2\}$, where V_R is the reference voltage. This comparison produces the digital output d_i where $d_i \in \{-1, 0, 1\}$ and $d = \sum_{i=1}^{3} d_i$. During the amplifying phase (ϕ_2 is high), C_f is connected to the output of the opamp, while C_1, C_2 and C_3 are connected to $-V_R$, ground or V_R, in other word $d_i V_R$, depending on the digital output code d_i.

The residue voltage for the stage i can be derived as:

$$V_{i+1} = G_A \cdot G_C \cdot \left(V_i - V_{daci} + \frac{C_T + C_p}{C_T} \cdot V_{os} \right) \tag{2.3}$$

where

$$C_T = C_f + C_1 + C_2 + C_3 \tag{2.4}$$

$$G_A = \frac{1}{1 + \frac{1}{Af}} \tag{2.5}$$

and G_A is the interstage gain due to the finite opamp gain A that is ideally equal 1.

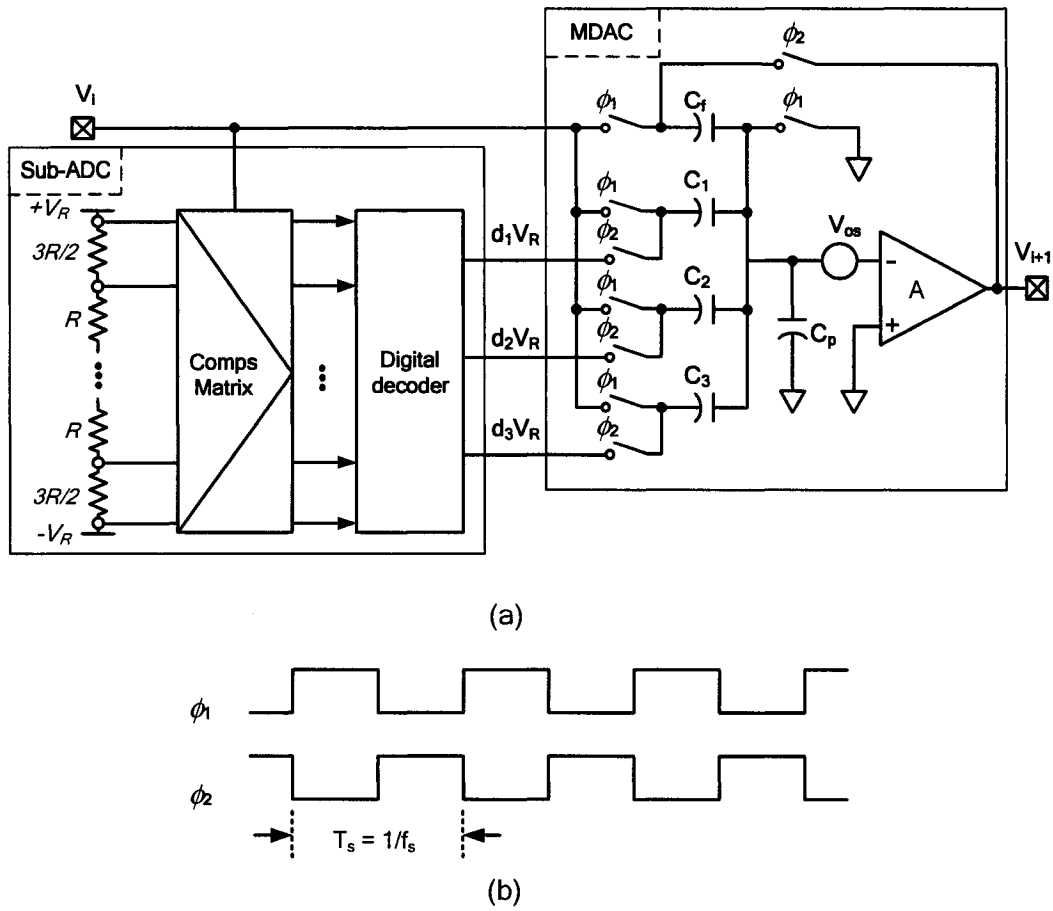

Figure 2.2: Switched capacitor implementation for 2.5 bit/stage of a pipelined ADC (a) and its clocks control signals (b).

The feedback factor f is equal:

$$f = \frac{C_f}{C_T + C_P} \tag{2.6}$$

C_P is the virtual ground parasitic capacitance.

$$G_C = \frac{C_1 + C_2 + C_3 + C_f}{C_f} \tag{2.7}$$

G_C is the interstage gain due to sub-DAC ideally equal 2^2.

$$G_i = G_A G_C \tag{2.8}$$

$$V_{daci} = \left(\frac{d_1 C_1 + d_2 C_2 + d_3 C_3}{C_T} \right) V_R \tag{2.9}$$

G_i is the interstage gain, V_{daci} is the sub-DAC output, and V_{os} is the input-referred offset voltage of the opamp.

Some of the major error sources in a pipeline ADC are: the comparator offset, the finite opamp gain, the opamp offset, and the capacitor mismatch. If these errors are neglected, the output voltage V_{i+1} of a 2.5b/stage can be written:

$$V_{i+1} = 4\left(V_i - \frac{\sum_{i=1}^{3} d_i}{4} V_R \right) \tag{2.10}$$

Figure 2.3 indicates an ideal residue plot where the output voltage is expressed in eq. (2.10). The comparator offset is mainly due to a mismatch between the two transistors in the differential pair that constitutes the input stage of the comparator. This offset can be modeled as a voltage that is added to one input of the comparator and not the other. Thus, when the two inputs of the comparator are close to each other, the comparator may make a wrong decision and the binary output d_i is wrong. That will cause the wrong reference voltage $d_i V_{ref}$ to be subtracted from the input.

To understand the importance of the redundancy, in other word using 2.5 bit/stage instead of 2 bit/stage, let us write the residue voltage of stage i with 2 bit/stage MDAC:

$$V_{i+1} = 4 \cdot \left(V_i - \frac{\sum_{i=1}^{2} d_i}{4} V_R \right) \tag{2.11}$$

where $d_i \in \{-1, 0, 1\}$ and $d = \sum_{i=1}^{2} d_i$.

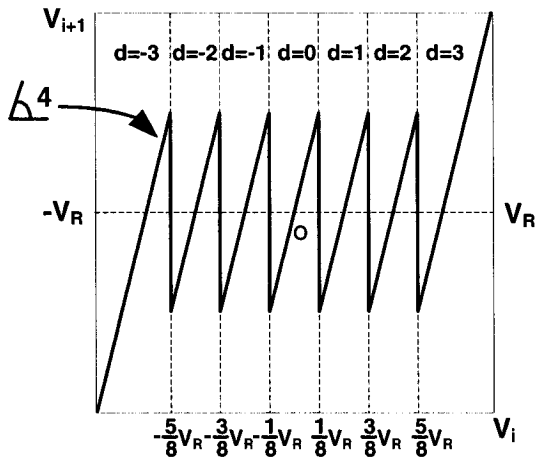

Figure 2.3: Residue plot of a 2.5 bit ideal pipeline stage.

As shown in Fig. 2.4(a), comparator offsets cause the residue to exceed V_R or $-V_R$ and therefore to be out of range of the next stage of the pipeline (stage i+1). The above operation and its effect on the input-output relationship of the overall pipelined ADC, when the stage i is considered as the first stage and the remaining stages are ideal, is illustrated in Fig. 2.4(b), where missing decision levels have been produced. Thus, redundancy has been devised to tolerate comparator offsets.

The residue plot of a 2.5 bit/stage MDAC, while the effects of comparator offsets are included, is illustrated in Fig. 2.5(a). Note that the residue output V_{i+1} remains inside the dynamic range of the following stage since it never gets close to V_R or $-V_R$ at code transition points. Thus, missing decision levels, which result when the residue output exceeds $\pm V_R$ at code transition points, are prevented. As a conclusion, the digital error correction is inherent in redundancy and any comparator error less than $\pm 1/8 V_R$ is corrected without affecting the overall characteristic of the pipelined ADC (Fig. 2.5(b)).

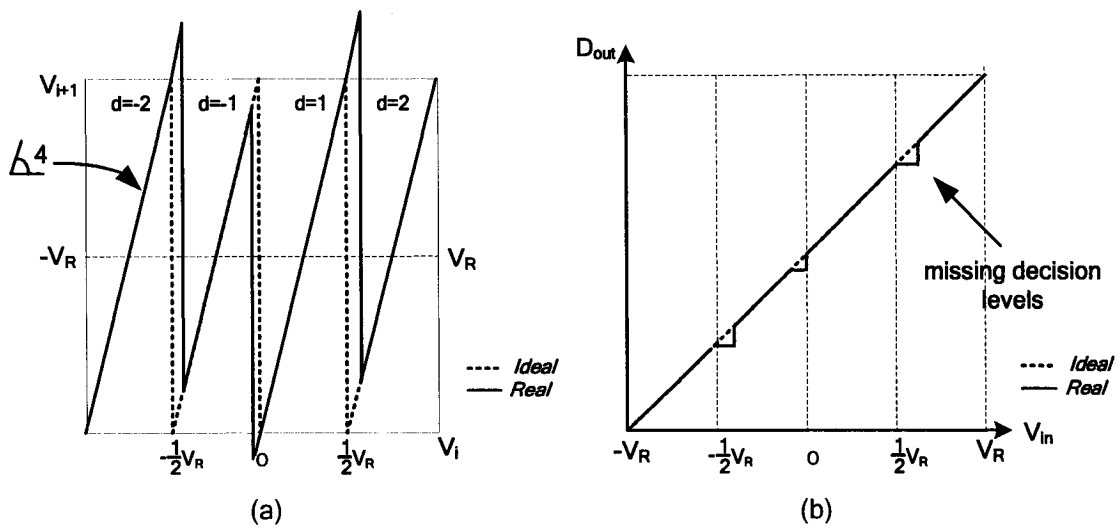

Figure 2.4: The residue plot of a 2 bit/stage with comparator offset error (a) and the input-output relationship of the overall pipelined ADC.

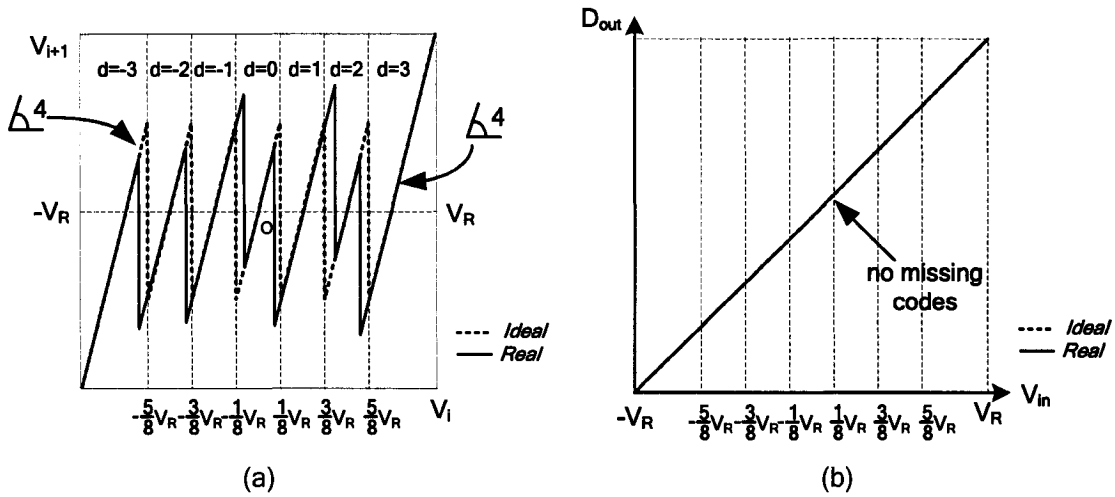

Figure 2.5: The residue plot of a 2.5 bit/stage with comparator offset error (a) and the input-output relationship of the overall pipelined ADC.

From eq. (2.3) we see that offset of opamp introduces a constant error, or a shift, at the output of pipeline stage equal to $V_{off} = G_A \cdot ((C_T + C_p)/C_f) \cdot V_{os}$ as shown in Fig. 2.6(a). To reduce the offset error, the input transistors of the opamp are often kept quite big, which usually takes a large area. Due to redundancy, as illustrated in Fig. 2.6(b), this

offset produces an overall input referred offset voltage and does not affect the ADC linearity.

While high-performance ADCs rely on high gain opamps, lowering the supply voltage in deep-submicron technology reduces the available signal swing and makes the design of high gain opamp topologies very difficult. Figure 2.7(a) shows the effect of finite opamp gain causing gain error on the residue plot of the MDAC. Because of finite opamp gain, there is an error voltage at the input of opamp equal to $-V_{i+1}/A$. From eq. (2.5), this error voltage causes the gain G_A to deviate from its ideal value equal to one. That makes the slope of the residue plot to become less than four and that introduces mismatch in the residue jumps in the different boundaries of the digital code d as shown in Fig. 2.7(a). Figure 2.7(b) shows the effect of this error on the input-output relationship of the overall pipelined ADC when the stage i is considered as the first stage and the remaining stages are assumed to be ideal.

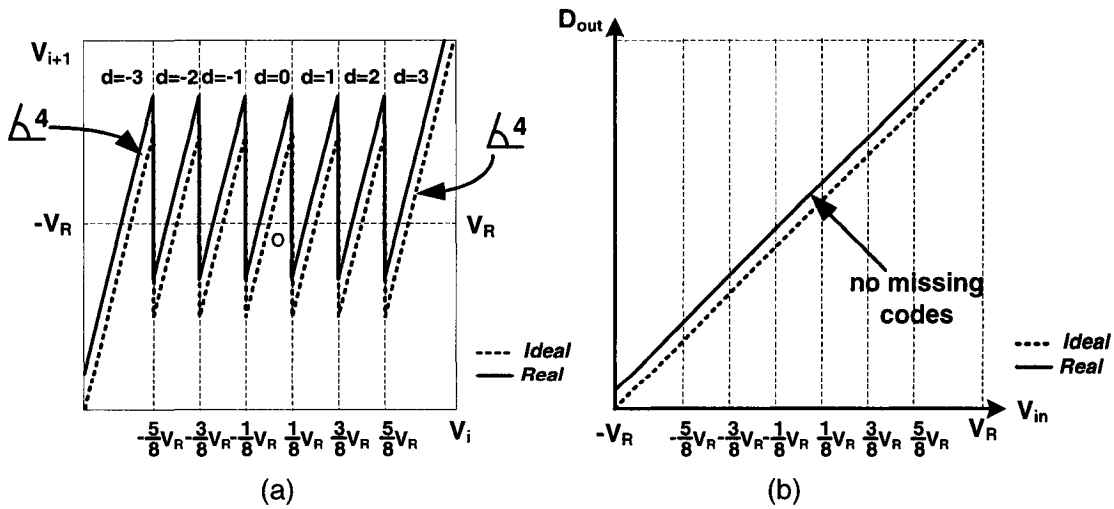

Figure 2.6: The residue plot of a 2.5 bit/stage with opamp offset error (a) and the input-output relationship of the overall pipelined ADC.

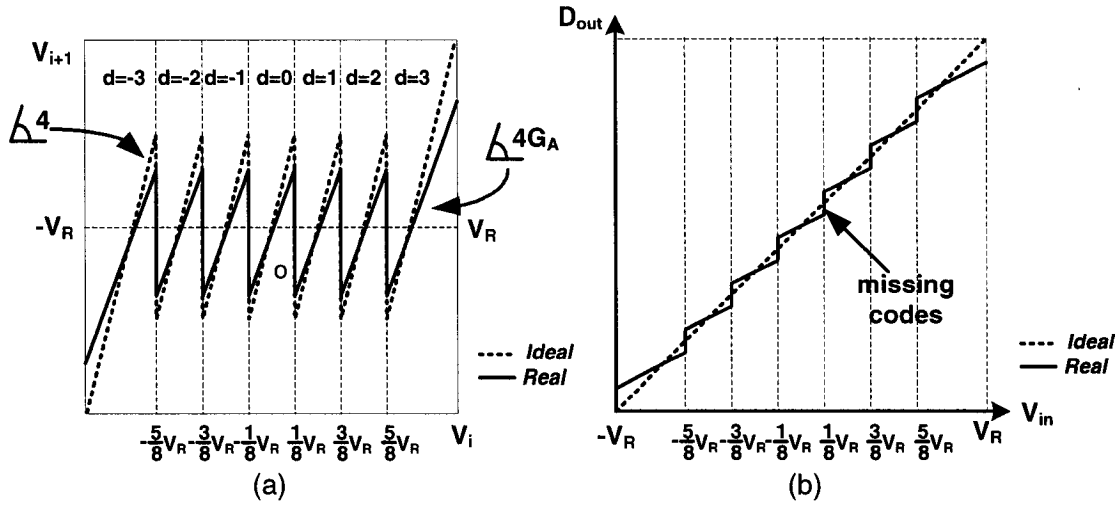

Figure 2.7: The residue plot of a 2.5 bit/stage with opamp finite gain error (a) and the input-output relationship of the overall pipelined ADC.

Figure 2.8(a) shows the effect of capacitor ratio error, due to capacitor mismatch, on the residue plot of 2.5 bit/stage MDAC. There are several mismatch error sources in on-chip capacitors. The major error source consists of gradient related system errors, which are strongly correlated for all capacitors on the same chip. These can be kept to a minimum by using unit capacitor layout techniques with common centroid geometry. Nevertheless, in the absence of component trimming or calibration, the conversion accuracy is usually limited to approximately 10-12 bits. Capacitor mismatch not only results in a slope error in the behavior of the stage due to the deviation of G_C from its ideal value (eq. (2.7)), but also, it affects the SDAC value (V_{daci}) as shown in eq. (2.9) and that introduces mismatch in the residue jumps in the different boundaries of the digital code *d*. Figure 2.8(b) shows the effect of this error on the input-output relationship of the

overall pipelined ADC when the stage *i* is considered as the first stage and the remaining stages are assumed to be ideal.

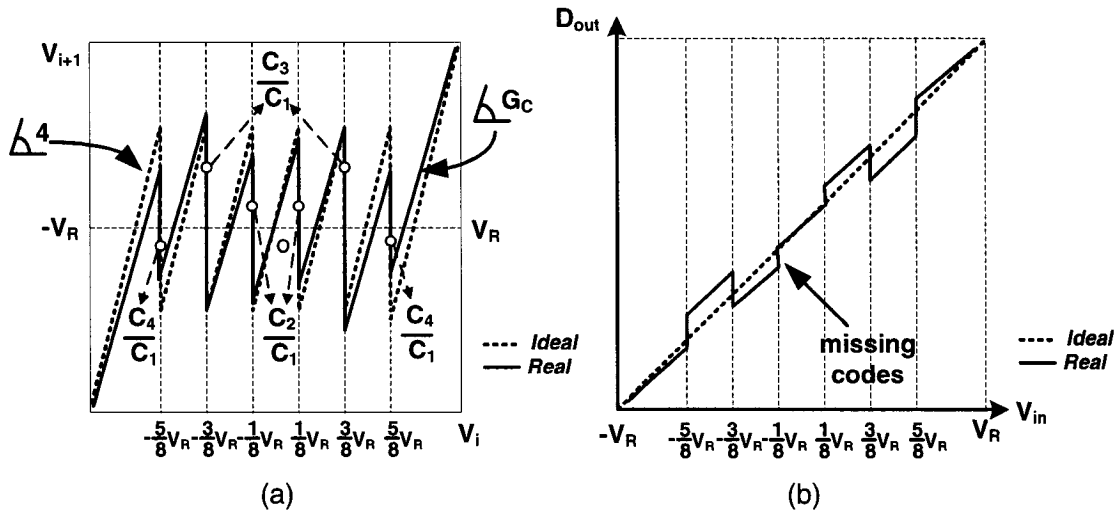

Figure 2.8: The residue plot of a 2.5 bit/stage with capacitor mismatch error (a) and the input-output relationship of the overall pipelined ADC.

The discontinuities in Figs. 2.7(b) and 2.8(b), caused by the missing codes, are generally referred to as major-carry jumps in the ADC curve. These discontinuities cause deleterious missing codes and harmonic distortion that degrade considerably the ADC performance.

2.3 Time-Interleaved ADC

2.3.1 Structure

Figure 3.1 shows a general block diagram of a time-interleaved ADC. Each ADC channel (ADC_1, ADC_2, ..., ADC_M) operates, respectively, with one of M phase clocks (CK_1, CK_2, ..., CK_M) at sampling rate f_s/M, where M is the number of parallel ADC

channels and f_s is the overall sampling frequency. This way, the sampling rate of the ADC as a whole is increased by M times compared to the channel sampling at the cost of additional hardware.

An example of the clocking scheme of a 2-channel parallel pipelined ADC system is shown in Fig. 2.9. The sampling instant of each S/H in each channel is shifted by a half of the clock period. The arrows show the clock phases used during the sampling periods. The digital multiplexer interleaves the digital output of the ADCs, thus producing the overall analog to digital conversion results

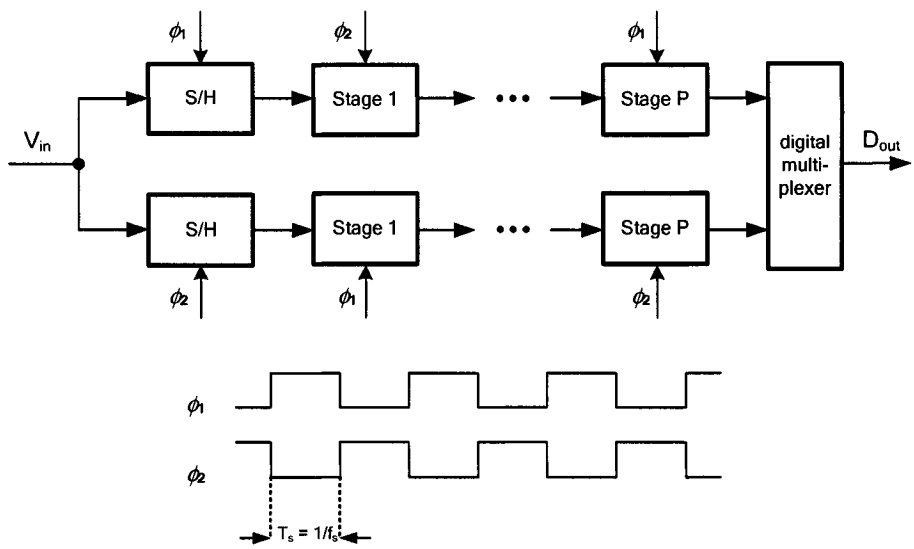

Figure 2.9: A two-channel parallel pipeline ADC clocking example

2.3.2 Error Sources in Time-Interleaved ADCs

Ideally all the time-interleaved ADC channels would have the same transfer function. Unfortunately, any mismatch between the time-interleaved ADC channels leads to degradation in the linearity performance [VOG05]. In particular, offset, gain and clock

skew mismatches among the parallel channels are unpredictable and produce spurious tones in the signal band, thus worsening the spurious-free dynamic range (SFDR), as well as the signal-to-noise distortion ratio (SNDR) performance.

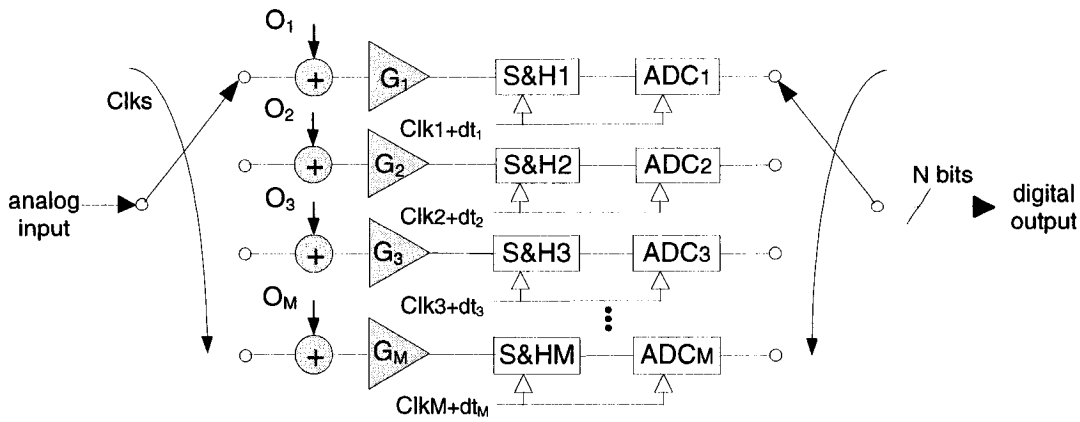

Figure 2.10: Offset, gain and time skew mismatches model.

A. Offset Mismatch Effects

The primary source of channel offset mismatch in TIADC is the mismatch in the global offset, referred to the input of every ADC channel. This offset is mainly due to opamp offset mismatch and MOS switches charge injection mismatch in the S/H of each channel. Channel offset can be modeled as extra voltage sources, (O_1, O_2,.., O_M), added to the input of every channel as shown in Fig. 2.10. The mismatch between the offset of every channel causes fixed noise pattern in the ADC system. The noise pattern is almost independent of the input signal in time and frequency domains, and it is an additive noise in time domain while in frequency domain it causes noise peaks at kf_s/M, k = 1, 2, 3, etc.

B. Gain Mismatch Effects

The major sources of gain mismatch are capacitor and opamp dc gain mismatches that create a different global gain error for every ADC channel. Gain mismatch can be modeled as gain stages, (G_1, G_2..., G_M), connected in series with input of every ADC channel as shown in Fig 2.10. This mismatch results in amplitude modulation of the input samples, causing scaled copies of the input spectrum to appear centered around integer multiples of the channel sampling rate f_s/M.

C. Clock Timing Error Effects

The sources of timing mismatch are the clock generator network, the actual turning off time of the MOS switches in the front-end S/H circuits, and the thermal noise of the electronic devices. These timing errors in an interleaved ADC system, causes clock skew (systematic error) and clock jitter (random error). Clock jitter effects are unavoidable in any ADC system but the interleaved architecture also suffers from clock skew effects. Clock skew mismatch can be modeled as the timing offset, (dt_1, dt_2,..., dt_M), added to the ideal timing instants of the M phase clocks (CK_1, CK_2, ..., CK_M) as shown in Fig. 2.10. These timing mismatches result in phase modulation of the input samples, which also causes scaled copies of the input spectrum to appear centered at the same frequencies as the spurious components stemming from gain mismatch.

To sum up, when a sine wave input signal having a frequency f_{in} is applied at the input of the TIADC, the gain and sample-time mismatches introduce undesirable spurs concentrated at $kf_s/M \pm f_{in}$, while the offset errors introduce undesirable spurs

concentrated at kf_s/M. For example, in the case of having four ADC channels, the output sequence of the TIADC is ADC_1, ADC_2 ADC_3, ADC_4, ADC_1, etc, and this periodic sequence creates spurs at the frequencies $kf_s/4 \pm f_{in}$ and $kf_s/4$, as shown in Fig. 3.2. These in-band spurious components undermine the SFDR and SNDR performances of TIADCs.

2.4 Calibration of Pipelined and Time-Interleaved ADCs

To improve the resolution of pipelined ADCs, methods to compensate the technologies limitations such as capacitor mismatch and finite opamp gain should be used. Capacitor mismatch gives rise to nonlinearity in the internal SDAC and also interstage gain error. The finite resolution of the technology limits the accuracy to about 10 bits [SUT88]. For good capacitor matching, large capacitors are needed and consequently the conversion speed goes down and the power increases. Beside capacitor mismatch, high performance pipelined ADC relies on fast and high gain opamps that are difficult to obtain in deep-submicron CMOS technologies.

With calibration, a high performance ADC could be obtained using low gain opamp and with large capacitor mismatch. Furthermore, by using a low gain opamp, the design of fast pipelined ADC becomes easier. Thus, a calibration technique enables the existence of high resolution and high speed ADCs.

Several calibration methods have been proposed to calibrate pipelined and time-interleaved ADCs. They can be divided based on the nature of the circuitry or the execution.

Based on the nature of the circuitry added to compensate ADC errors, the calibration

is named analog or digital. Analog calibration [LIN91] techniques use analog signal paths and extra analog and/or mixed signal circuitries, such as DAC, to apply corrections to the stage being calibrated. One way to implement this calibration is using trimming methods. On the other hand, digital calibration techniques [LEE92] measure the error contributions of the stage in the digital domain and then post process the raw data of the uncalibrated ADC to deliver precise data, as shown in Fig. 2.11. Digital calibration is more appealing than analog counterpart, since the added digital circuitries track gracefully the advancement of the deep submicron technologies. This is due to the fact that the cost and the power dissipation of the digital calibration circuitries are decreasing owing to scaling of CMOS technologies. With digital calibration, a high performance ADC could be obtained using low power supply and inexpensive CMOS process.

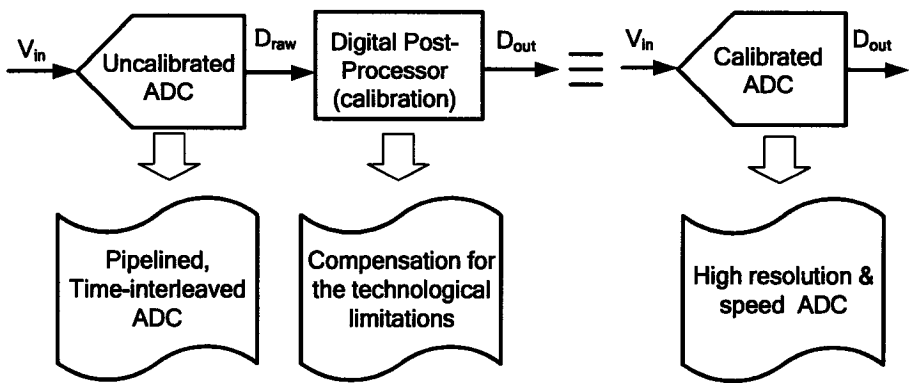

Figure 2.11: High performance ADC for SDR transceivers

Based on execution, calibration can be performed on the foreground (off-line) [SUM02a] or on the background (on-line) [LI03]. The former can be implemented at factory by trimming voltages/currents and/or capacitors/resistors as presented in [DEW93]. However, this solution is expensive and unable to track offset variations with

temperature or ageing over time.

Several foreground self-calibration techniques can be found in the literature [CHU02, SAB03, CON93, LEE94]. With self-calibration, the backend ADC is used to measure the errors related to the stage undercalibration. However, these calibration processes interrupt the input signal conversion. An interesting foreground digital self-calibration method for 1-bit per stage pipeline ADCs is presented in [KAR93]. The idea behind this calibration technique is to measure the residual error characteristics of an undercalibration pipeline stage at the comparator threshold voltage using the remaining stages. In other words, referring to the residue plot shown in Fig. 2.12, the real value of S_1 and S_2 are measured. Note that a nominal gain less than two is used up for the stages to be calibrated to eliminate missing decision levels. The calibration algorithm is given by:

$$\begin{aligned} Y &= X, if\ D = 0 \\ Y &= X + S_1 - S_2, if\ D = 1 \end{aligned} \tag{2.12}$$

where X is the digital output of the current stage plus the following stages, D is the output bit from the previous stage. Y is the calibrated output of the current stage and the following stages. Using this method for multibit/stage MDACs necessitates the existence of accurate reference voltages at the respective comparator threshold levels [SUM02b].

To prevent the interruption of the operation of the A/D converter, on-line calibration is preferred. On-line calibration techniques are more difficult to implement, since they operate in background while the ADC is working normally. Several solutions for achieving on-line calibration have been presented in literature.

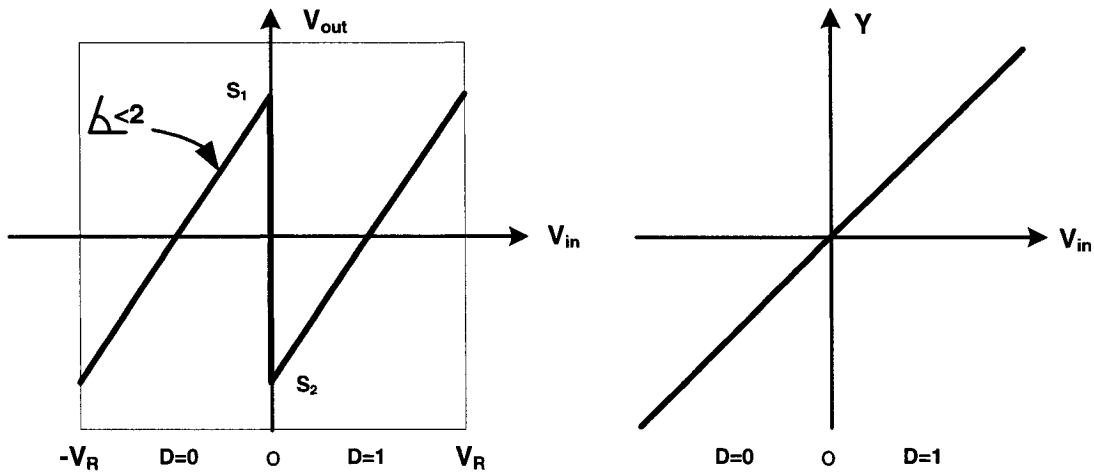

Figure 2.12: Principle of digital self-calibration: (a) error coefficient measurement, and (b) missing code elimination.

Some of these calibration techniques address the capacitor mismatch in pipelined ADCs. Among them we find the active [SON88], and passive [CHI04a] error averaging techniques. Generally, these techniques generate a residue voltage pair that contains complementary gain errors, and then average this residue voltage pair to obtain an accurate 1.5 bit/stage MDAC amplifying operation. Active averaging technique necessitates an extra set of averaging opamps and capacitors beside additional clock phases. The passive error averaging is proposed to reduce the extra circuit complexity of active averaging technique. Figure 2.13 shows an MDAC using passive averaging technique. This circuit operates as follows. In sampling phase 1, the first voltage of the complementary residue pair produced by the previous stage, V_{in1}, is sampled by capacitor C_1 (Fig. 2.13(a)). In sampling phase 2, the second residue V_{in2} voltage is sampled by capacitor C_2 (Fig. 2.13(b)). Two capacitors C_3 and C_4 from the next pipeline stage sequentially sample the residue voltage pair during two transfer phases (Figs 2.13(c) and

2.13(d)). The averaging amplifier needed in active averaging is eliminated; since averaging the error (*delta*) due to capacitor mismatch takes place when C_3 and C_4 merge charges in the subsequent phases. However, the passive averaging takes four clock phases to complete the sampling and amplifying processes.

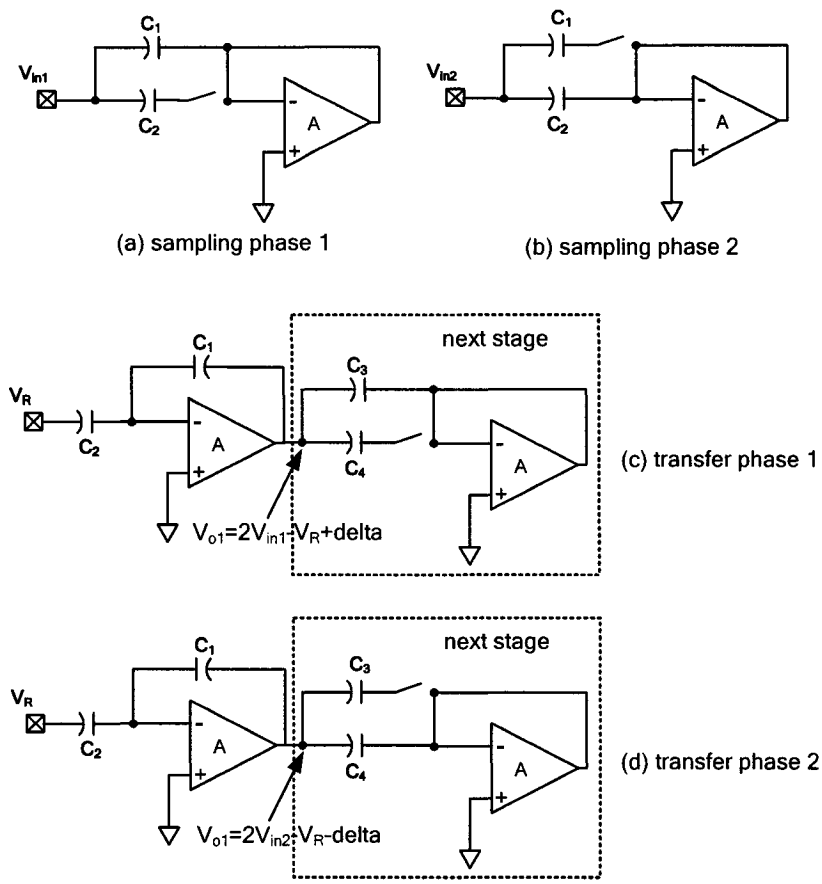

Figure 2.13: Schematic diagram of passive capacitor error-averaging technique [CHI00].

Also other techniques have been proposed to reduce the capacitor mismatch such as the commutative feedback capacitor switching [YU96, FET03] that involves re-arrangement of the feedback capacitor. Nonetheless, this technique reduces the differential nonlinearity (DNL) but not the integral nonlinearity (INL). Also the

oversampled pipelined ADC [SHA02] is proposed to reduce the effect of the capacitor mismatch. This method modulates the distortion energy out-of the desired band, and thus trades ADC bandwidth with resolution.

Moreover, there are some methods that compensate opamp finite gain such as correlated double sampling (CDS) [NAG87], time-shifted correlated double sampling (time-shifted CDS) [LI04], and "deriving an error signal from the opamp and add it to the original signal" [ALI03]. These methods present important solutions for high speed ADC built around low gain opamps. These methods have some drawbacks such as accumulation errors and/or the need for a shadow pipelined ADC.

Another efficient technique that gives the freedom to inject a known calibration voltage, usually a reference voltage, in place of the input signal to calibrate ADC during the normal operation is the skip-and-fill [MOO97]. However, this method reduces the input bandwidth to 1/3 of the Nyquist band [KWA97]. Similarly, the Queue-based calibration [BLE03, ERD99] runs the front-end S/H slower than the ADC so as to create time slots to inject calibration signals. This method increases the noise due to the added front-end S/H and it is more suitable for calibration of algorithmic ADCs [ERD99].

An analog background calibration technique using extra-stages to substitute the stage under calibration and DAC to compensate for the errors is presented in [ING98]. This technique is not easily scaled in the technology and the substitution of the stages degrades the speed and creates a fixed pattern noise. Also, an analog online calibration method for offset and gain mismatches in TIADC exploiting an additional channel is presented in [DYE98]. By adding an ADC channel, one of channels will be idle and can be calibrated,

while the remaining operates the conversion. The calibration is carried out using a least mean square (LMS)-based mixed-signal scheme. Once the calibration cycle terminates, another channel is placed in the calibration section. Therefore, when all of the channels are calibrated, the system starts a new global calibration sequence. Also in [TAM01, EKL02], additional converters and analog circuitries have been used to perform random sampling among the parallel ADCs in order to average out the TIADC mismatch errors. However, using additional ADC channels is very costly.

A background LMS-based self-calibration technique in conjunction with the addition of a calibration ADC is also presented to calibrate pipelined ADCs [SON00]. The basic idea of this digital error correction scheme is to correct for the residue errors in a non-ideal pipelined stage using a suitable set of parameters. These parameters are determined by comparing this residue with an ideal estimated one, which is generated using a slow-but-high-resolution ADC (SHADC) connected in parallel to the stage under correction. Connecting the SHADC to the input of all the stages to be calibrated requires precise switching analog circuitries and disturbs the residue signal path.

To not disturb the signal path, in [CHU04b] the analog impairments in pipelined ADC are treated in analogy to distortion in communication channels. Component errors from all stages of the pipeline are removed simultaneously using an adaptive finite-impulse response (FIR) digital filter as shown in Fig. 2.14. The output vector $\boldsymbol{D}$ of a high speed, inaccurate pipelined ADC is decimated and applied to an adaptive digital filter (ADF). A parallel, slow-but-accurate ADC is used to obtain D_{in} while the ADF tap values

are updated using an LMS algorithm driven by the error signal e. The update is performed at the speed of the slow ADC.

The analog overhead is the slow-but-accurate ADC which can be a self-calibrated cyclic ADC or a Sigma-Delta ADC that should have resolution as the desired resolution of the calibrated ADC. The slow ADC sampling must be fast enough to track the temperature variation, supply voltage drift, and component aging. The problem for the architecture is that the input signal should be somehow busy to fully calibrate the ADC and also the front-end S/H cannot be calibrated.

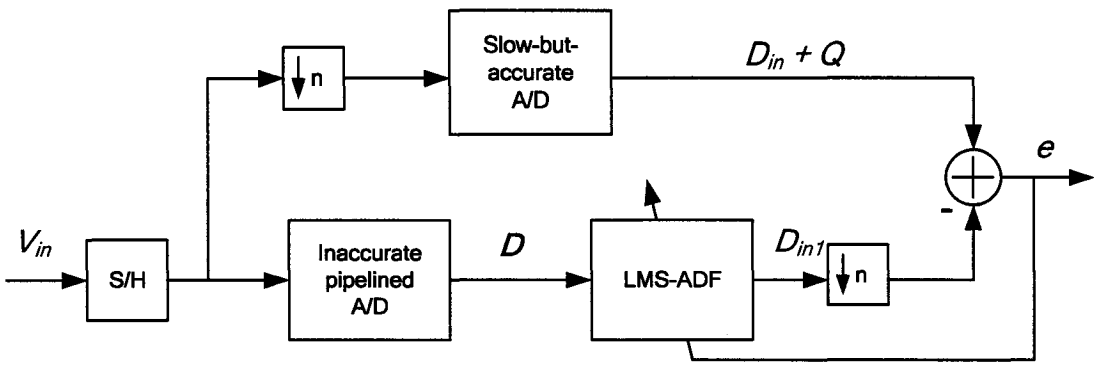

Figure 2.14: Error correction of pipelined ADC in channel equalizer like scheme [CHU04b].

On the other hand, correlation-based techniques have been proposed to calibrate pipelined ADCs in the background. A general block diagram of correlation-based technique is shown in Fig. 2.15 [JEW97]. This technique is based on modulating with a pseudorandom number (PN) calibration signal, the ADC errors and to recover them later by correlating the ADC output with the same PN signal in digital domain. This calibration signal, generally a digital signal, is converted to the analog domain by a DAC

and is added to the input of the ADC. Both the input signal and the PN signal are then converted to digital domain by the ADC. The correlation of the ADC output and the calibration signal is measured, and the results are used to compensate for the nonlinearity of the ADC. Finally, the digital version of the calibration signal is subtracted from the ADC output to remove its contribution.

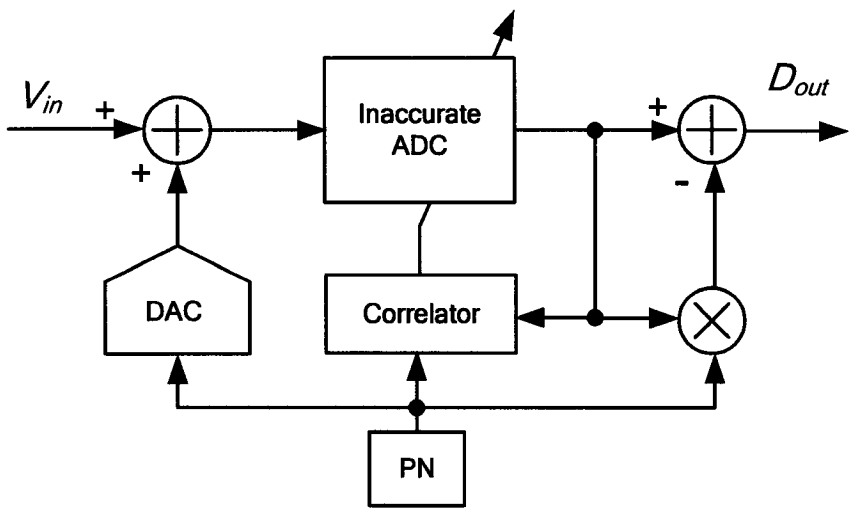

Figure 2.15: Correlation-based techniques to calibrate pipelined ADC [JEW97].

This technique has been applied to compensate the mismatches in pipelined [LI05] and TIADC [FU98]. A disadvantage of this technique is that it reduces the dynamic range because the calibration signal occupies part of the input range. Also, the DAC, used to convert the PN from digital to analog signal, must have the same resolution as the desired one for the whole ADC. Moreover, the convergence is related to the magnitude of the calibration signal. A smaller signal slows down the conversion, while a larger signal reduces further the dynamic range. One way to overcome this problem is to perform the

online calibration only when the input is in the idle state. In this case, this solution is no longer a true background calibration.

In the literature, we find a large variety of improved correlation-based calibration techniques. An interesting method proposed to compensate for the interstage gain error in pipelined ADC is the gain error correction (GEC) [SIR00]. This technique requires somehow increasing the SDAC resolution and the addition of accurate analog voltages. Another technique to compensate the interstage gain error by using slow-but-accurate sigma-delta ADC is presented in [SHU97]. The correlation based technique can be implemented by dithering the thresholds of the comparators in the SADC. The stage gain multiplied by this injected signal is extracted by correlation to correct linear [LI05] or nonlinear gain errors [MUR04] in the ADC. This technique cannot work properly under certain input conditions when the input is far from the sub-ADC comparator thresholds.

Other methods are proposed to correct for the SDAC nonlinearity. Among these methods we find the background DAC noise cancellation (DNC) [GAL00, GIO05], oversampling calibrator that monitors the ratio errors of a resistor-string digital-to-analog converter (DAC) [SHU97], and the DAC auto-calibration [KIN04]. The SDAC and feedback capacitor averaging with mismatch noise cancelling [YU01] and the recently proposed subtractive dither-continuous gain correction [NAI04] correct for the SDAC nonlinearity and for interstage gain error in the SDAC but not the gain error due to the opamp finite dc gain. Also the combination between the DNC and GEC [SIR04] methods to address nonlinearity and the interstage gain error has recently been demonstrated. This combination of DNC and GEC requires injection of accurate calibration voltage,

increasing the SDAC resolution, and also using a complex digital shuffler between the SADC and SDAC that widens the gap between the sampling and holding phases subsequently limiting the ADC speed.

In the following chapters, we present new methods and techniques to calibrate pipelined and time-interleaved ADC that overcome some limitations of the above stated methods.

Chapter 3

NEW SAMPLING METHOD FOR WIDE BANDWIDTH TIME-INTERLEAVED ADCs

3.1 Introduction

As discussed in chapter 2, to achieve higher sample rates, parallelism can be introduced to multiple ADC channels to form a one wide bandwidth TIADC. The main drawback stemming from interleaving the ADC channels to form a global TIADC is the mismatches among these sub-channels. These mismatches create in-band distortion components, which undermine the SFDR performance [KUR01]. As we mentioned earlier, in wireless receivers, channel selection and filtering after the A/D conversion increases the SNR but cannot overcome distortion in the ADC bandwidth. In this chapter a new sampling method to improve the SFDR performance in TIADCs is presented. To overcome this problem in the digital domain, a randomizing and rotation method to average out the effect of the mismatches among the ADC channels is proposed. The mathematical background describing the effect of randomizing the samples among the ADC channels is analyzed and consequently a digitally oriented implementation, amenable to deep submicron technologies, is described. This work has been published in a journal paper presented in «Journal of Circuits, Systems, and Computers, © World Scientific Publishing Company, 2004». This paper is reproduced in the following pages.

3.2 New Sampling Method to Improve the SFDR of Wide Bandwidth ADC Dedicated to Next Generation Wireless Transceiver

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Abstract

Modern wireless communication standards that support high rates of voice and video streaming need high-speed Analog-to-Digital Converters (ADCs) with wide spurious-free dynamic range (SFDR). Conventional time-interleaved ADCs suffer from spurious components that seriously affect the SFDR. In this paper we present the mathematical background describing the effect of randomizing the samples among the interleaved ADCs and we propose a digitally oriented method based on this analysis to randomize the mismatches among the ADC channels. Analysis and simulations show the effectiveness of the proposed approach in multi-channel ADCs with arbitrary bit resolution, channel's number and sampling rate. For a 10-bit 500MS/sec ADC, the SFDR achieved using the proposed randomizing method can be as wide as 75 dB, which is an enhancement of more than 26 dB comparing to the conventional time interleaved ADC.

Keywords: Analog and mixed-signal circuits design; ADC; Digital signal processing; SFDR.

1. Introduction

Advances in the ever-increasing range of wireless communication standards with higher data rates, that support voice and image streaming, call for receivers with high degree of flexibility to accommodate backwardly existent standards and to allow smooth migration to future generation standards [1]. To enable the flexibility of the next generation receivers, the channel selection in their front-ends, needed to reject interferers from other channels, should be programmable for a very wide bandwidth [2]. This high programmability favours the digital implementation of this channel selection. This claim is based on two facts: firstly the difficulty to perform this tuneable filtering in the analog domain; and secondly the fast scaling of the digital components and their high density of integrations comparing to the analog components. To enable the digital channel selection, a wide bandwidth ADC with high dynamic range is needed to adapt a large number of wireless standards. Channel selection after the ADC will increase the Signal-to-Noise Ratio (SNR) but it cannot overcome distortion in the ADC bandwidth, which makes the Spurious-Free Dynamic Range (SFDR) a very important parameter to feature the efficiency of an ADC.

Time interleaved ADC (TIADC) [3] is the most promising topology for high-speed and high-resolution ADC. The principles of such architecture as well as its drawbacks have been widely published. Due to its importance, special attention has been given to the SFDR performance of TIADCs. The SFDR is the ratio of the single-tone signal amplitude to the largest non-signal component within the spectrum of interest [4]. This parameter has been discussed and elements affecting it have been identified in TIADC [5, 6]. As

discussed in [5], the spurious components are created by cyclic mismatch factor such as timing, offset and gain. Also it has been noticed that as the number of ADCs increases (in order to increase the sampling rate), the number of spurious components increases. Recent research works have proposed solutions to improve the SFDR using random time-interleaved sampling methods. In [7] a random chopping sampling for the input signal is proposed that only removes the offset mismatches. In [8] and [9], additional converters and analog circuitries have been used to perform the random sampling among the parallel ADCs that add large overhead on the system. In [10], a randomizing method without adding ADCs is proposed. This architecture consists on delaying M samples from the input signal and randomizing their distributions between the M channels of the TIADC using an analog swapper circuit. This architecture needs M analog circuits to hold the samples at the input of the ADC channels, which add imperfection to the ADC. In this paper we present the mathematical background describing the effect of randomizing the samples among the interleaved ADCs and we propose a randomizing and rotation method, based on this analysis, to average out the effect of the mismatches among the ADC channels and improve the SFDR performance of the TIADC [11, 12]. A digitally oriented implementation of this new time-interleaved architecture is also presented. Performance analysis of the new method is given. Simulation results that demonstrate its effectiveness are shown and discussed.

This paper is divided into five additional sections. Section 2 gives a brief review of the time interleaved ADCs. Section 3 follows with the description of the new randomizing method. Section 4 presents the digitally oriented implementation of the

method. Section 5 shows the simulation results and is followed by a conclusion in Section 6.

2. Time-interleaved ADCs

Figure 3.1 shows a block diagram of time-interleaved ADC. Each ADC channel operates at the system sampling rate f_s divided by M, where M is the number of parallel ADC channels. Ideally all the channels would have the same transfer function. Unfortunately the mismatches between the ADCs weaken the performance of the TIADC. These mismatches between the ADC channels inflict a periodic additive noise pattern to the output of the ADC. As discussed in [5], when a sine wave input signal having a frequency f_{in} is applied at the input of the TIADC the gain and sampling time mismatches introduce undesirable spurs concentrated at $kf_s/M \pm f_{in}$ while the offset errors introduce undesirable spurs concentrated at kf_s/M. For example, in the case of having four ADC channels, the output sequence of the TIADC is ADC_1, ADC_2, ADC_3, ADC_4, ADC_1...etc, and this periodic sequence creates spurs at the frequencies $kf_s/4 \pm f_{in}$ and $kf_s/4$ as shown in Fig. 3.2.

In order to reduce the spurs concentration at these frequencies, a certain swap inside this periodic sequence is needed. This swapping could be done by randomizing the distributions of the samples converted by the TIADC channels. Additional converters have been used to break this sequence, which adds large overhead [8, 9]. A complete randomizing could be implemented by delaying a number of samples equal to the ADC

channels and randomize their distributions between the different ADCs [10]. For instance, in the case of M interleaved ADCs, 0 delay is added before ADC_1, ADC_2 needs one delay, ADC_3 needs 2 delays and finally ADC_M needs M-1 delays; that means the architecture requires $((M\text{-}1)M)/2$ analog delays. These added analog circuits undergo leakage of the held values as well as many other well-known problems of analog circuits, which will worsen the mismatches between the ADC channels, and consequently increase the nonlinearity of the global ADC in a real implementation. Hereafter, a new method based on randomizing the samples among the ADC channels and also performing rotation between these channels is presented. This method gives an equivalent performance to a complete randomizing without additional imperfect analog circuits.

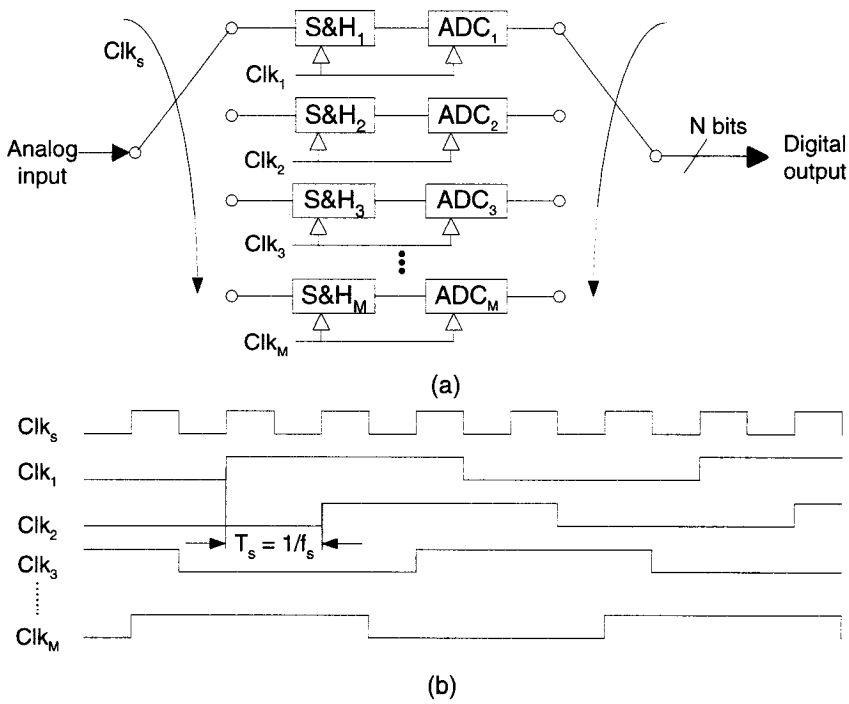


Figure 3.1: Conventional time-interleaved ADC: (a) structure and (b) clock waveforms.

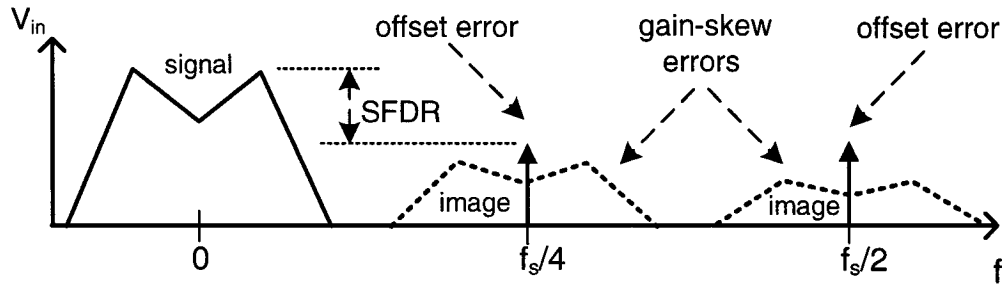


Figure 3.2: Spurs distribution for four channels conventional TIADC.

3. New random sampling TIADC method

3.1. *Analysis of randomizing the samples*

In the following discussion, M is the number of the ADC channels and $T = 1/f_s$ is the equivalent sampling period of the TIADC. When a sine wave input signal having a frequency f_{in} and amplitude A_0 is applied at the input of the TIADC and the gain and offset errors are introduced by adding a channel-dependent terms a_m and d_m respectively, the resulting signal spectrum can be written as [13]:

$$F(k) = \frac{1}{MT}\left[\left(\sum_{m=0}^{M-1} \pi\left(A_0 + a_m\right)e^{-jkm\frac{2\pi}{M}}\right)\delta\left(f + f_{in} - k\frac{f_s}{M}\right)\right.$$
$$+\left(\sum_{m=0}^{M-1} \pi\left(A_0 + a_m\right)e^{-jkm\frac{2\pi}{M}}\right)\delta\left(f - f_{in} + k\frac{f_s}{M}\right) \qquad (3.1)$$
$$\left.+\left(\sum_{m=0}^{M-1} 2\pi d_m e^{-jkm\frac{2\pi}{M}}\right)\delta\left(f - k\frac{f_s}{M}\right)\right]; \quad k \in (-\infty, +\infty)$$

We can see from Eq. (3.1) that the gain and offset errors introduce undesirable spurs concentrated at $kf_s/M \pm f_{in}$ and kf_s/M. In the following, we will study the spurs produced

by the offset error d_m, and we will consider the case of having four parallel ADC channels. We note here that the following discussion is valid for any number of channels, and that the study of spurs produced by the gain error can be carried out similarly, but the spurs will be shifted in the frequency by $\pm f_{in}$ from that of the offset error. In the case of conventional TIADC composed of four ADC channels, M is equal to 4.

Now for $k = 0$, Eq. (3.1) gives a DC component of:

$$\frac{\pi}{2T}\left(\sum_{m=0}^{3} d_m\right) \tag{3.2}$$

This component is the offset of the global ADC. This offset is not critical for several applications, such as telecommunication, and it could be subtracted easily in the digital domain in the background [14].

For $k = 1$, we have spurs with values centered at $f_s/4$:

$$\frac{2\pi}{4T}\left(\sum_{m=0}^{3} d_m e^{-jm\frac{\pi}{2}}\right) \tag{3.3}$$

These values are distributed as shown in Fig. 3.3(a) with a scale of $2\pi/T$ and where $M = 4$. If $d_0 = d_1 = d_2 = d_3$, then the spurs sum is equal to zero, and consequently no mismatches between the ADCs.

This result is difficult to achieve for analog blocks despite respecting the matching rules of integrated ADCs on the same chip. Always from Fig. 3.3(a), we can obtain the spur centered at $f_s/4$ with amplitude of:

$$\frac{1}{2}\cdot\sqrt{(d_0-d_2)^2+(d_1-d_3)^2} \tag{3.4}$$

These spurs centered on $f_s/4$ and the other frequencies degrade the SFDR to unacceptable values.

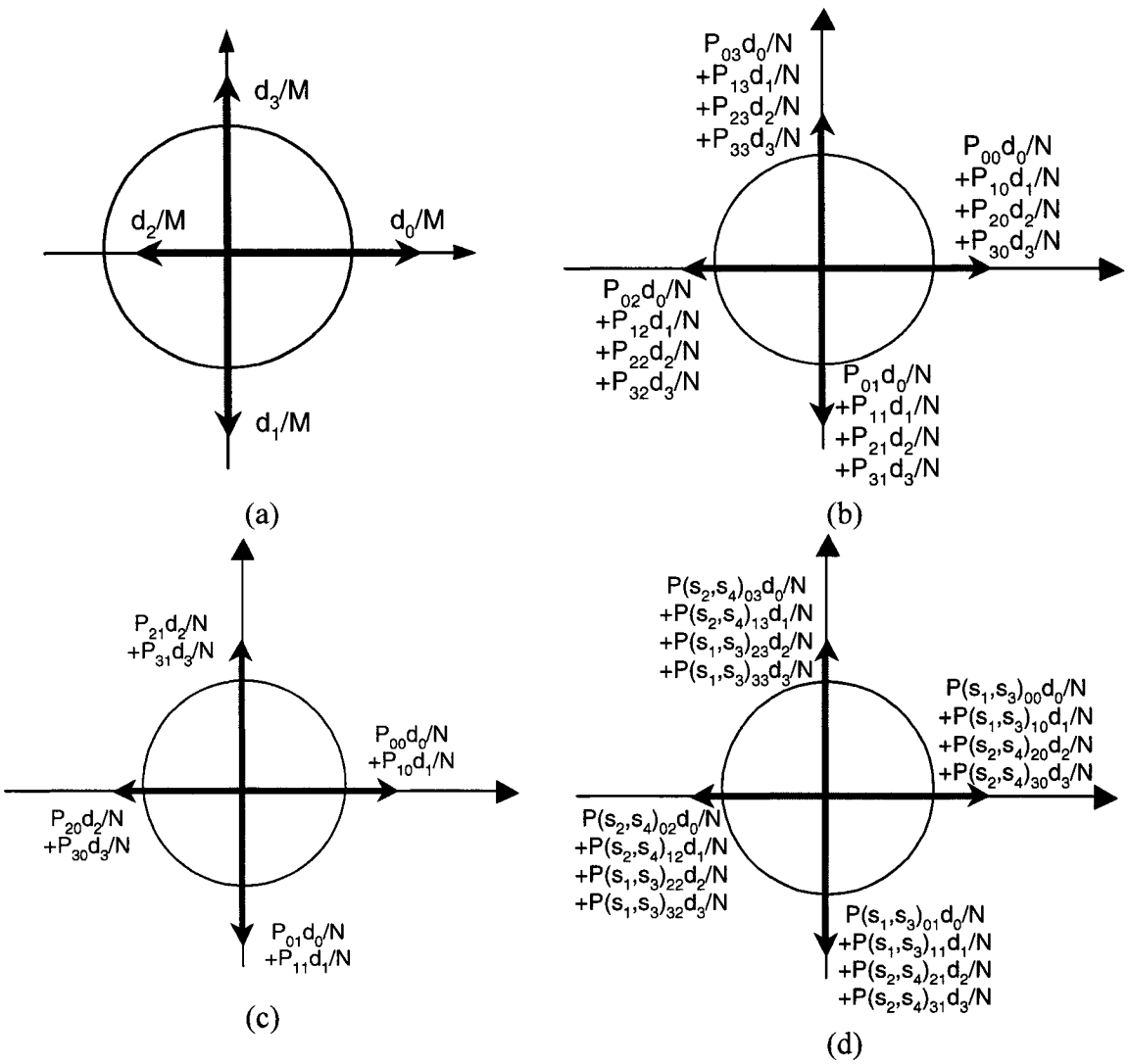


Figure 3.3: Spurs distribution for $f = f_s/4$: (a) without randomizing, (b) with total randomizing, (c) with the new randomizing, and (d) with the new randomizing and rotation.

In order to reduce the spurs concentration at these frequencies, a certain swap inside the sequence $d_0d_1d_2d_3$ is needed. For example, it can be $d_0d_2d_1d_3$ or any other swapping

scheme. Now, if we randomize the samples at the input of the TIADC, we should replace M in Eq. (3.1) by the period of the randomizing sequence. In other words, if a Pseudo-Random Bit Generator number (PRBG), with period P is used to control the randomizing, the sequences that repeat periodically every N samples equal to $4P$ is obtained and the period of the Discrete Fourier Transform (DFT) given by Eq. (3.1) will become $N = 4P$. The mismatches error is distributed in a such manner that we may find d_i/N in every direction which minimizes the total sum due to this mismatch as shown in Fig. 3.3(b) for $f_s/4$ ($k = M/2$), where:

$$\sum_{j=0}^{3} P_{ij} = P, \qquad i \in (0 \ldots 3) \tag{3.5}$$

When N is a big number, these P_{ij} are almost equal to $P/4$ for every i and the sum of the error due to every mismatch is minimized. A straightforward method to implement a complete randomizing is to delay a number of samples equal to the ADC channels and randomize their distributions between the different ADCs. As mentioned before, this method necessitates a large number of analog circuitries that create new mismatches and then reduces the strength of this randomizing method.

3.2. The new spurs reduction method

Let's suppose now that we can swap randomly between d_0 and d_1 and also between d_2 and d_3 for a long period of N values. Doing so, sequences like ($d_0d_1d_2d_3$, $d_1d_0d_2d_3$, $d_0d_1d_3d_2$,..) can be obtained.

For $f = f_s/4$, spurs are distributed as shown in Fig. 3.3(c), where:

$$\sum_{j=0}^{1} P_{ij} = P, \quad i \in (0 \ldots 3) \tag{3.6}$$

This new randomizing eliminates the spur at $f = f_s/2$ completely as shown in Fig. 3.4 because there is errors d_i in all directions. For $f_s/4$ a great reduction in the spurs is obtained in all the other cases other than $d_0.d_1 > 0$ and $d_2.d_3 > 0$, where the spurs are not reduced. This is actually the worst case as far as this randomizing is concerned.

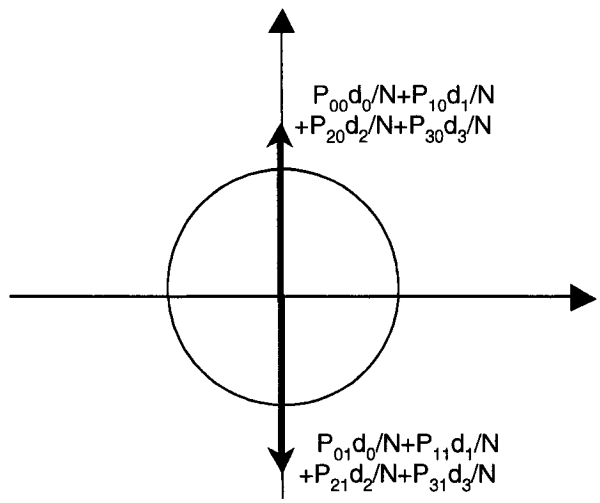


Figure 3.4: Spurs distribution for $f = f_s/2$ with the new randomizing.

By performing randomizing between two groups of two ADCs, the spurs at $f_s/4$ will not be reduced. Now, to obtain randomizing equivalent to the expensive complete randomizing, we propose to make a rotation technique of the ADCs position. For example, instead of having a sequence repeated every N samples as ($d_0d_1d_2d_3$, $d_1d_0d_2d_3$, $d_0d_1d_3d_2$, ...), we will be able to obtain different sequences. We divide the periodic N samples into four sets: the first set of elements can have the same sequence like ($d_0d_1d_2d_3$, $d_1d_0d_3d_2$); while the second set can be obtained by rotating the positions of two couples of

two ADCs, which result on new sequence like ($d_2d_3d_0d_1$, $d_3d_2d_1d_0$); and then we toggle between the two previous sequences twice during the N samples. An illustration of this scheme, for $f = f_s/4$, is shown in Fig. 3.3(d), where s_1, s_2, s_3 and s_4 are the four sequences that represent the N samples. The number of d_i elements is given by:

$$\sum_{j=0}^{1} P(s_1, s_3)_{ij} + \sum_{j=2}^{3} P(s_2, s_4)_{ij} = P, \qquad i \in (0,1) \tag{3.6}$$

and

$$\sum_{j=2}^{3} P(s_1, s_3)_{ij} + \sum_{j=0}^{1} P(s_2, s_4)_{ij} = P, \qquad i \in (2,3) \tag{3.7}$$

where $P(s_1, s_3)_{ij}$ is the number of d_i elements due to the sequences s_1, and s_3. Similarly, $P(s_2, s_4)_{ij}$ is the number of d_i elements due to the sequences s_2 and s_4.

Fig. 3.3(d) shows that the mismatch errors d_i exist in all the directions. This leads to a considerable reduction of the total error similar to the results from totally randomizing the sequences. The number of rotations performed, which is four in this example, is very small compared to the number N of samples.

As mentioned earlier, a total randomizing for any number of ADC channels can be obtained by only randomizing the sample distribution between every group of two ADCs and then performing rotation among the different groups. In the following section, we present a digitally-oriented implementation of this proposed method.

4. Digitally oriented implementation of the new randomizing and rotation method

4.1. *Implementation of the randomizing*

The proposed randomizing architecture consists of dividing the TIADCs into two sets. In the case of M interleaved ADCs, each set is composed of $M/2$ ADCs, as shown in Fig. 3.5.

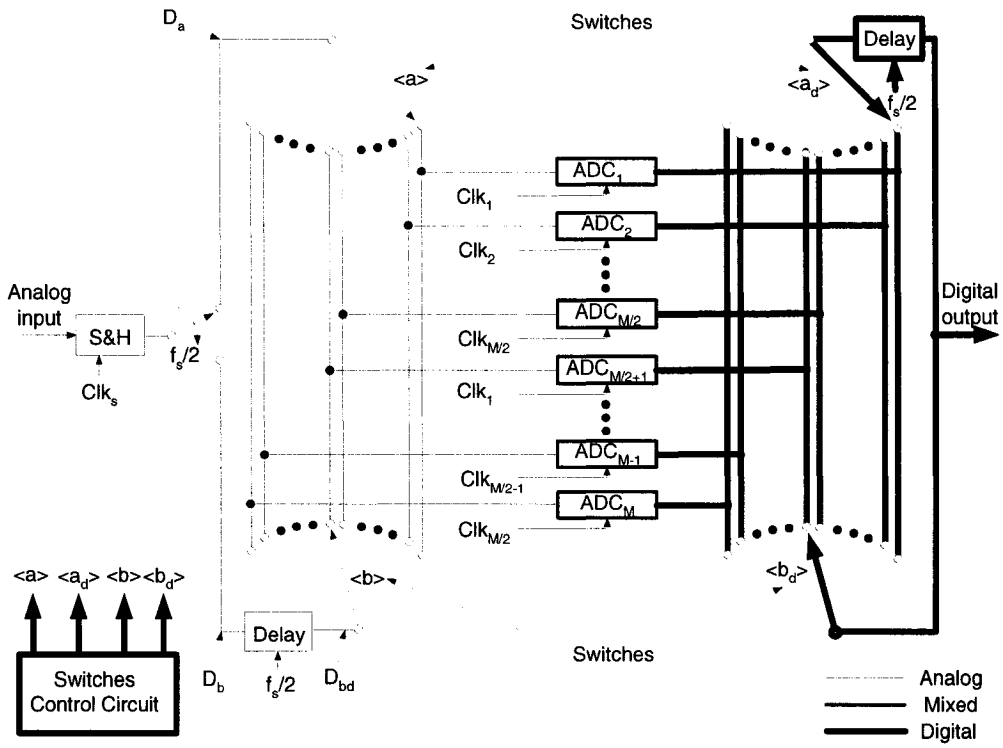


Figure 3.5: Architecture of the new random time-interleaved ADC.

The S&H circuit, at the front-end of the TIADC, operates at full speed, i.e., at the sampling frequency f_s of the TIADC. Each ADC channel of this configuration operates at f_s/M. An analog switch that distributes the samples periodically between the upper and the lower sets of ADCs follows the S&H circuit. The frequency at which the analog switch operates is $f_s/2$. The data D_a and D_b are distributed between the upper and the lower sets of ADCs as in Fig. 3.6. This figure shows the expected waveforms at the inputs of the two sets of ADCs. With an analog delay inserted in the path of D_b (Fig. 3.5),

data are clocked as D_a for the upper set and as D_{bd} for the lower set. Note that D_a and D_{bd} are aligned together. Referring to Fig. 3.5, we see that two ADCs (e.g. ADC_i and $ADC_{M/2+i}$) are simultaneously ready to receive randomly a sampled input: one from the upper set and the other from the lower set. The examples of randomized samples between the two sets of ADCs are illustrated in Fig. 3.6.

As shown in Fig. 3.5, we have two sets of switches <*a*> and <*b*> that distribute samples between two ready ADCs. <*a*> and <*b*> can have one of the M values $<e_1>$... $<e_M>$ shown in Fig. 3.7.

To make such randomizing possible, we need to have a mechanism that memorizes the previous values of vectors <*a*> and <*b*>. The ADC with rank i from the upper set have the same clock of the ADC with rank $M/2+i$ in the lower set. So, if vector <*a*> takes the value $<e_i>$, <*b*> should take the value $<e_{M/2+i}>$. To realize this randomizing scheme, we propose the circuit shown in Fig. 3.8. In this circuit, we are using two FIFOs of $(M/2)M$ bits each. $FIFO_A$ is initialized with $<e_1>...<e_{M/2}>$, and $FIFO_B$ with $<e_{M/2+1}>...<e_M>$. Values $<e_1>$ and $<e_{M/2+1}>$ are applied to the input of two muxes in a way that $<e_1>$ has rank 0 for MUX_1 and rank 1 for MUX_2. The inverse is true for vector $<e_{M/2+1}>$. Now, to control the muxes, a Pseudo-Random Bit Generator (PRBG) with period N is used. When the output of the PRBG is 1, vector <*a*> becomes $<e_{M/2+1}>$ and vector <*b*> becomes $<e_1>$, and if the output of the PRBG is 0, the inverse happens. Figure 3.9 gives examples of the FIFOs cycles during the randomizing process.

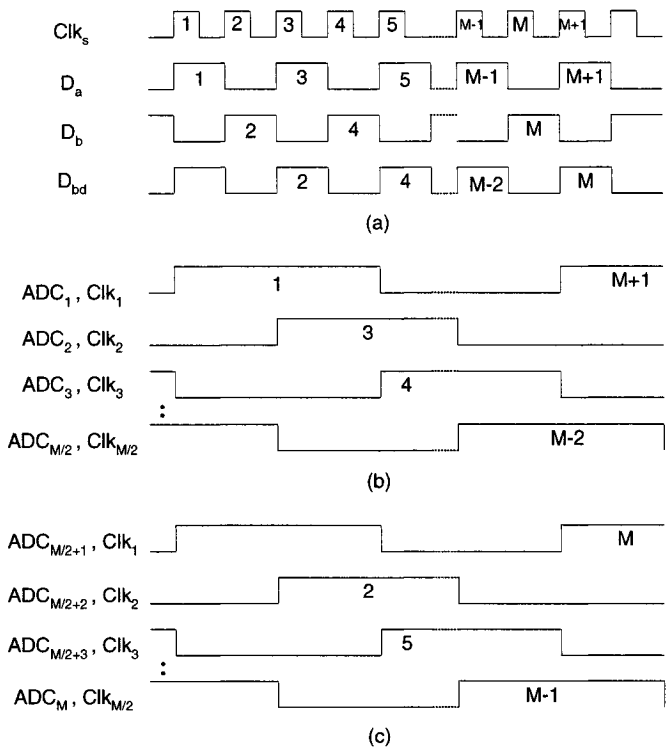


Figure 3.6: The distribution of the samples at the inputs of the two ADCs sets: (a) waveforms, (b) set 1, (c) set 2.

$$E = \begin{array}{c} \langle e_1\rangle\langle e_2\rangle\langle e_3\rangle \ \ldots \ \langle e_M\rangle \\ \begin{bmatrix} 1 & 0 & 0 & \ldots & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ \ldots & \ldots & \ldots & 1 & \ldots \\ 0 & \ldots & 0 & 0 & 1 \end{bmatrix} \end{array}$$

Figure 3.7: Possible values of vectors <a> and <b>.

The muxes drive randomly the analog switches with vectors $\langle a \rangle$ and $\langle b \rangle$, and the digital switches with vectors $\langle a_d \rangle$ and $\langle b_d \rangle$. The outputs of the muxes are stored in FIFO circuits, and the FIFOs outputs become inputs for the muxes in a cyclic way. In such control scheme, we assure that if $\langle a \rangle = \langle e_i \rangle$, then $\langle b \rangle$ should be $\langle e_{M/2+i} \rangle$ and vice versa.

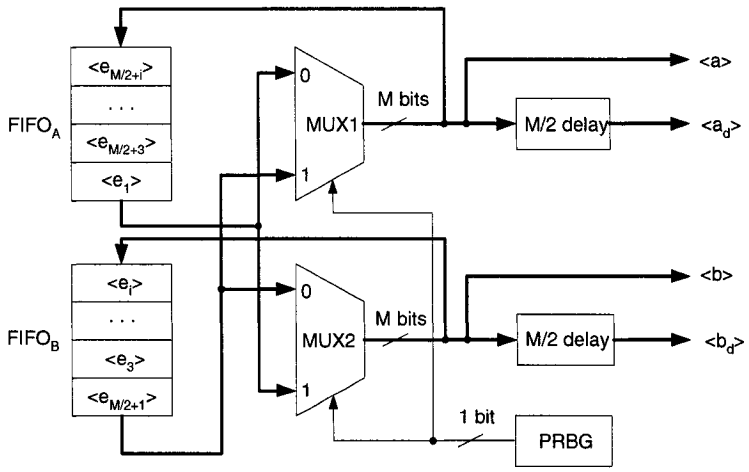


Figure 3.8: Block diagram of the new random TIADC controller.

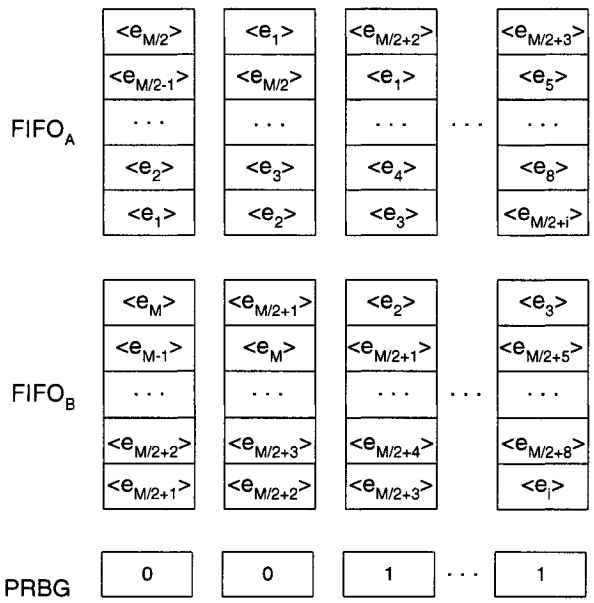


Figure 3.9: Examples of the FIFOs cycles during the randomizing.

Since we are applying the two sets of ADCs in the same time, we consequently should expect two digital outputs: the sample that was delayed at the input should be delay free at the output, and the one that was delay free at the input should be delayed at

the output. Using the proposed randomizing scheme, we can create sequences for $M = 4$ like ($ADC_1ADC_3ADC_2ADC_4$; $ADC_3ADC_1ADC_2ADC_4$; ADC_1ADC_3 ADC_4ADC_2;...; etc). These long sequences repeat every N samples, where N is the period of the PRBG.

4.2. *Implementation of the rotation*

In order to simplify the analysis, we will consider the case of having four parallel ADC channels. To get a complete randomizing between the ADCs without adding any analog circuits, we propose here a rotation technique of the ADCs position based only on digital circuit. For example, instead of having a sequence repeated every N samples, with the proposed rotation method, we divide these N samples into four sets. The first set of elements can have sequence like (ADC_1ADC_3 ADC_2ADC_4; $ADC_3ADC_1ADC_4ADC_2$); the second set can be obtained by rotating the positions of two couples of two ADCs, which results on new sequence like (ADC_2ADC_4 ADC_1ADC_3; ADC_4ADC_2 ADC_3ADC_1); and then, we toggle between the two previous sequences twice during the N samples. For a TIADC of four channels (Fig. 3.5) ADC_1 and ADC_3 have the same clock Clk_1 and the samples are distributed randomly between them, so we use $ADC_{1,3}$ to represent them. Similarly, ADC_2 and ADC_4 have Clk_2 and we use $ADC_{2,4}$ for them. When a rotation is triggered, the sequence such as ($ADC_{1,3}$, $ADC_{2,4}$) generated from the circuit of Fig. 3.5 is changed directly to a sequence of ($ADC_{2,4}$, $ADC_{1,3}$). To perform a rotation, Clk_2 of $ADC_{2,4}$ should be changed to Clk_1 because the two consecutive sequences end and start by $ADC_{2,4}$. This means $ADC_{2,4}$ must run faster, which is impossible. A method to implement the rotation is possible at the expense of skipping the conversion of two

samples. The effect of skipping the conversion of two samples every $N/4$ samples is raises the noise floor. To overcome this problem, we proposed to randomize the position of the rotation.

The importance of randomizing the rotation can be demonstrated by the following equations. We suppose that $v_i(t)$ is the sampled input signal and that the ADC is ideal. We assume also that the only error due to sampling stems from the rotation and consequently from skipping the conversions of samples in every rotation. We suppose that the rotation happens every K samples, where K is a constant value and that we substitute the skipped samples by near ones. So, at nKT instead of having $v_i(t\text{-}nKT)$ we will have $(1+\varepsilon).v_i(t\text{-}nKT)$, where ε represents the mean of the deviation of $v_i(t\text{-}nKT)$ from its ideal value. Then, the sampled signal can be written as follows:

$$v(t) = \sum_{n=-\infty}^{+\infty} v_i(t).\delta(t - nT) + \sum_{n=-\infty}^{+\infty} \varepsilon.v_i(t).\delta(t - nKT) \tag{3.8}$$

The Fourier transform for this signal is:

$$V(f) = \frac{1}{T}\sum_{n=-\infty}^{+\infty}\left[V_i(f - nf_s) + \varepsilon.V_i\left(f - n\frac{f_s}{K}\right)\right] \tag{3.9}$$

In the case of performing four rotations in the N sample, K will be equal to $N/4$. From Eq. (3.9) one can see that at constant frequencies nf_s/K, an image from the main spectre multiplied by ε is generated. These in-band distortions will degrade the SFDR as shown in Fig. 3.10, in the case of K = 6. Now if the rotation is initiated randomly inside the interval of the $N/4$ elements, K will be a random number from the interval [1:$N/4$] and the

error will be distributed on frequencies that span from 0 to $f_s/2$. This allows spreading the effect of the rotation over the entire Nyquist band.

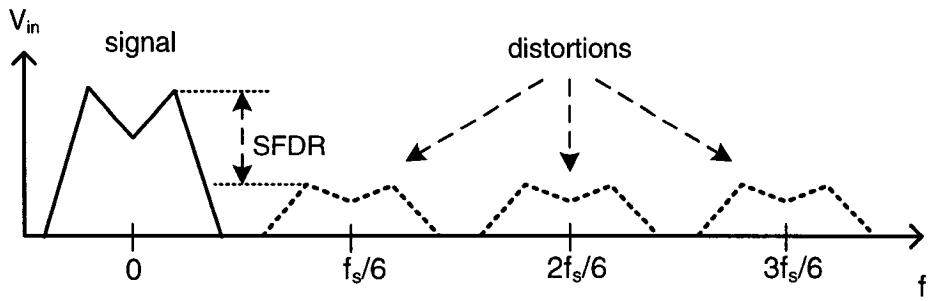


Figure 3.10: Distortion due to periodic rotation.

The circuit, shown in Fig. 3.11(a), initiates rotations at an arbitrary position inside the chosen number of samples (e.g., $N/4$), instead of generating these rotations periodically. This circuit, formed by a pseudo-random counter, works at low frequency of $(f_s/2)/(N/4)$ where $f_s/2$ is the samples distribution frequency at the input of the ADC channels as shown in Figs. 3.5 and 3.12. This counter generates randomly a number between 1 and N/4. The generated number will be compared to the output of a modulo N/4 counter. In case of matching the signal, C_m will be activated. In this way, we can generate a signal that randomizes the rotation position. The input C_m activates the circuit shown in Fig. 3.11(b) that generates control signals for the ADCs switches shown in Figs. 3.11(c) and 3.11(d). When C_m is active, this value is latched ($L_1 = 1$) and waits for Clk_1 to be active. On the rising edge of Clk_1, the previous value of signal C_1 flips from high to low, or vice versa. We see from Fig. 3.12 that when the rotation occurs, $ADC_{1,3}$ discard converting of the samples (10,11) and delivers at the output the samples (6,7). When the state $L_1=1$ and the rising edge of Clk_1 is latched ($L_2 = 1$) and when Clk_2 is at the rising edge, C_2 flips

value. At this time, $ADC_{1,3}$ receive (12,13) instead of $ADC_{2,4}$, and the latter go to the previous inputs of $ADC_{1,3}$, and the outputs of $ADC_{2,4}$ provides the samples (8,9) to the TIADC output. After certain delay, the outputs of $ADC_{1,3}$ and $ADC_{2,4}$ are switched due to C_d and C_{db} (Fig. 3.11(c)). The state C_m = 1 and the rising edges of Clk_1 and Clk_2 is latched (L_3 = 1). When ($L_1L_2L_3$ = 1), the latches are reset and ready to detect a new random rotation command.

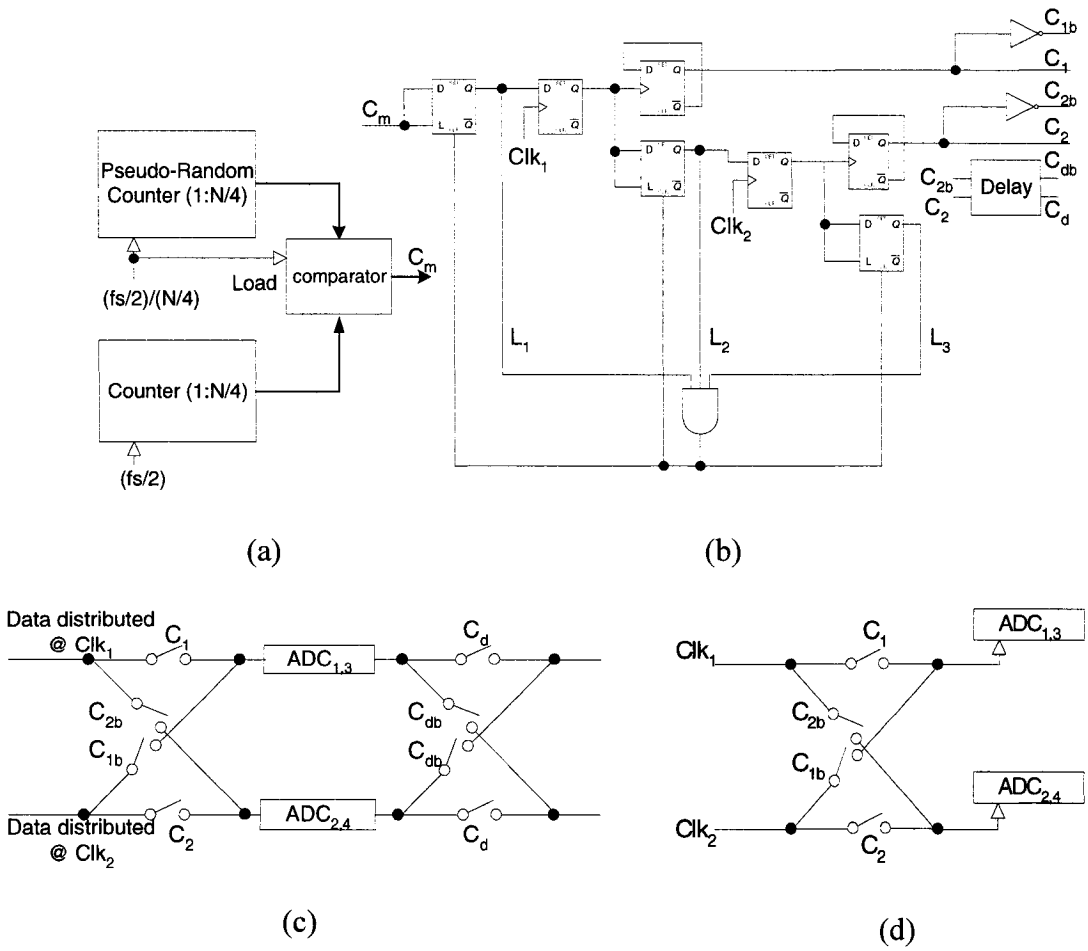


Figure 3.11: Rotation circuits implementation: (a) rotation trigger, (b) control signals generation, (c) switches to rotate the ADCs , and (d) switches to rotate the clocks.

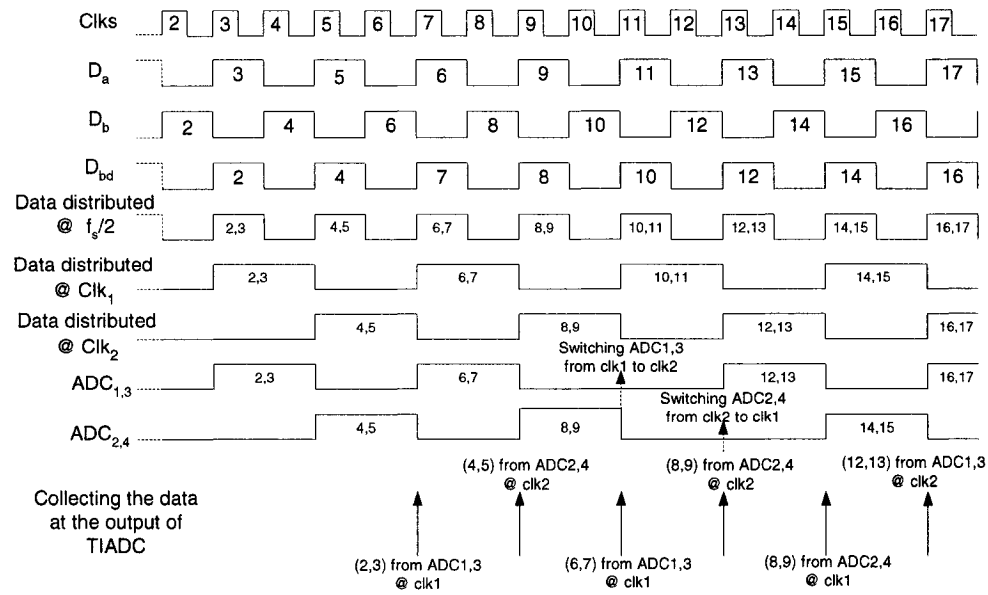


Figure 3.12: Waveforms at the inputs of the four ADCs.

The rotation is pipelined on $2T$ to allow time for the ADCs to settle in their new states. The skipped samples are substituted by the values of the 2 closest samples. Minimizing more the effect of skipping samples can be obtained by adding an extra digital circuit at the output of the TIADC. Digital delays are needed to hold the digital outputs inside the core of the global ADC, and substitute the skipped values by interpolating some previous and new values. However, the rotation happens sporadically and its induced error will be spread over the entire Nyquist band, which reduces its effect on the SNR.

5. Results

Behavioral simulations have been performed to verify the proposed randomizing scheme. A 10-bit resolution TIADC with 500 MS/s has been simulated. Different configurations have been considered: 2, 4, 6, and 8 ADC channels. A full-scale (FS) sinewave input has

been used with different frequencies. A peak-to-peak gain mismatch of 1% and an offset of 5 mVpp from 2 V power supply were introduced for each ADC. The results were carried out in terms of the SFDR improvement. For 10-bit ADC the SFDR should be more than 60 dB that corresponds to one LSB.

Without randomizing and with FS sinewave of 50 MHz frequency, the simulation results show an SFDR of 47 dB in the case of four ADCs (Fig. 3.13(a)). With the proposed method the SFDR achieved can be as wide as 79 dB as shown in Fig. 3.13(c). It is clear that the spurious components are completely converted to white noise.

For an input of 150 MHz, an improvement of 20 dB is obtained (Figs. 3.13(b) and 3.13(d)). More improvement could be obtained by increasing the rotation frequency and by increasing the period of the PRBG circuit. There is trade-off between more improvement of the SFDR and increasing the noise floor due to rotation. This could be settled using a more sophisticated interpolation [15] to substitute the skipped samples due to rotation. Another alternative is to use a queue-based S&H at the input of TIADC and running the ADC channels slightly faster than the input S&H. In this way, the rotation happens without skipping samples when the queue of the S&H is empty [16].

Figure 3.14 shows the effectiveness of this method when the number of channels increases to 6 and 8, where an enhancement of more than 20 dB is achieved. As mentioned earlier, more reduction could be easily obtained by increasing the frequency of the rotation at the expense of increasing of the noise floor. Post-channel selection filtering in the telecommunication applications will increase the SNR considerably.

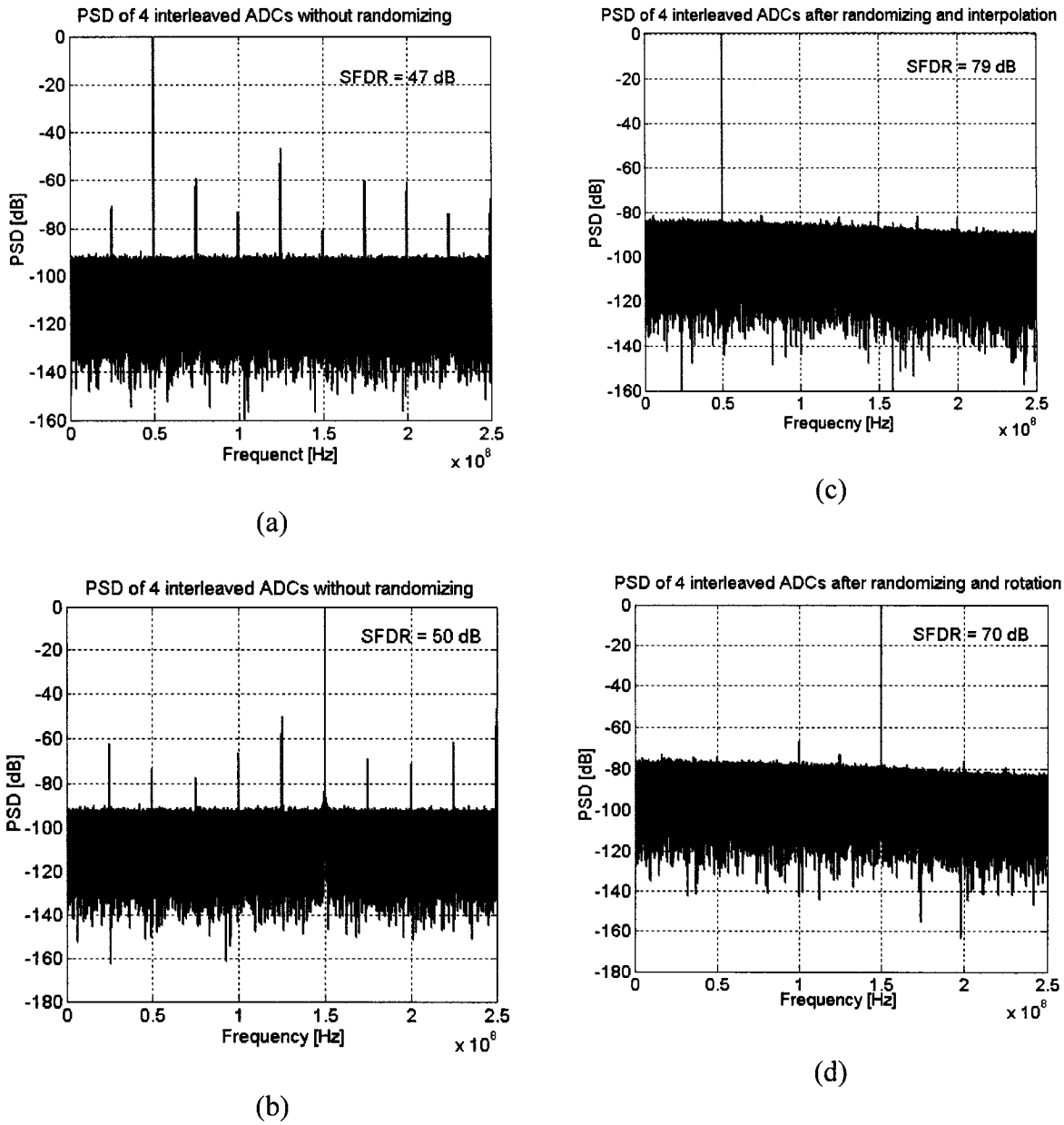


Figure 3.13: Output spectrum of four TIADC (a), (b) without, and (c), (d) with the proposed method.

Figure 3.15 shows the SFDR variations with gain error for 4, 6 and 8 ADCs, where $sigma_a/mean_a$ represents the standard deviation of the gain error over the ADCs gain

average. We see that this method can accommodate as large as 5%pp gain mismatch and it is still giving a 10-bit SFDR performance. Concerning the offset mismatches, this method can accommodate as large as ±10 mVpp offset mismatch.

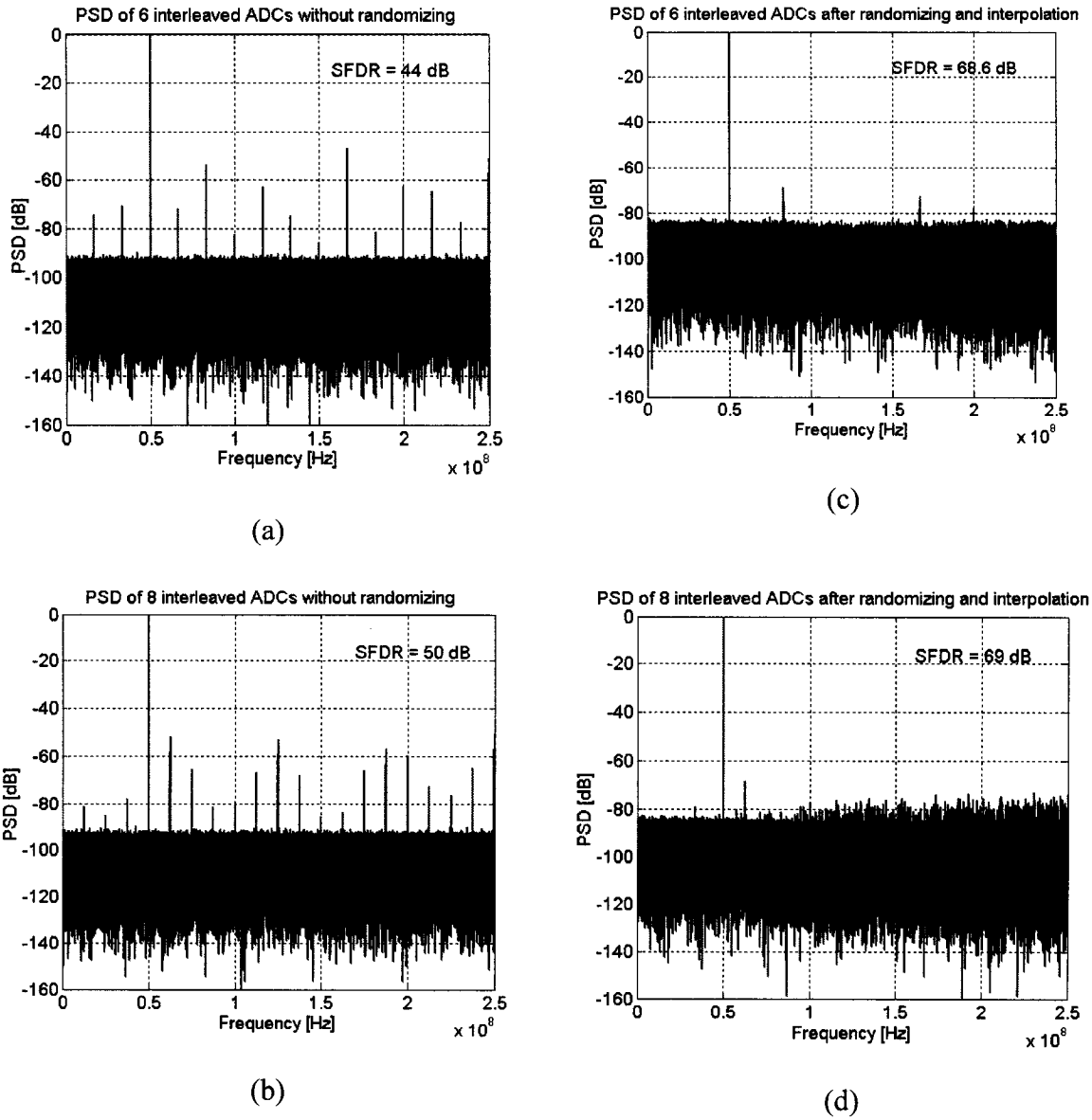
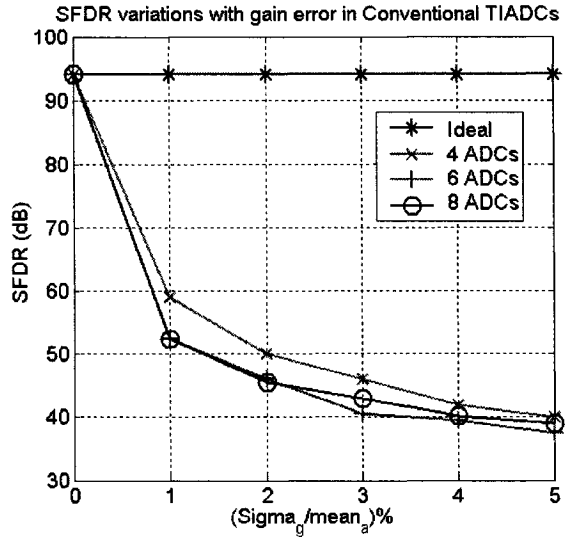
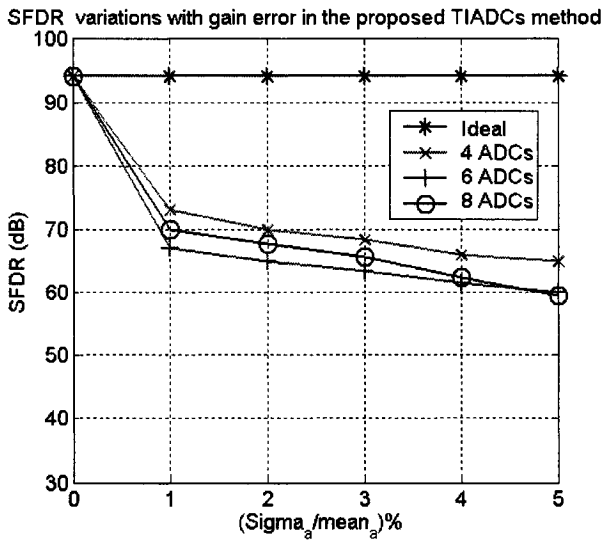


Figure 3.14: Output spectrum of 6 and 8 TIADCs (a), (b) without, and (c), (d) with the proposed method.



(a)



(b)

Figure 3.15: SFDR in terms of gain error mismatches: (a) without, and (b) with the proposed method.

To confirm the reliability of the proposed method, Monte Carlo (MC) simulations were carried out for TIADC with four channels. In these simulations, the gain and the

offset mismatches are normally distributed between ±5pp% and ±10 mVpp, respectively. MC simulations with 2250 cycles are shown in Fig. 3.16. The simulations give an average SFDR of 47.9 dB for the ADC before randomizing, while this method increases the average SFDR to 74.5 dB, which corresponds to more than 26 dB enhancements.

We can summarize from the previously presented simulations that with the proposed method, the undesirable spurs are spread over the frequencies in the Nyquist range instead of being concentrated in specific tones (i.e., kf_s/M or $kf_s/M \pm f_{in}$). This improves considerably the SFDR performance of the TIADC beyond the technology limits. Another advantage of this method is that, in addition to randomize the effect of the mismatches among the channels, this method will randomize the distortion stemmed from the characteristic of the individual ADC and that means reducing the distortion due to the TIADC nonlinearity.

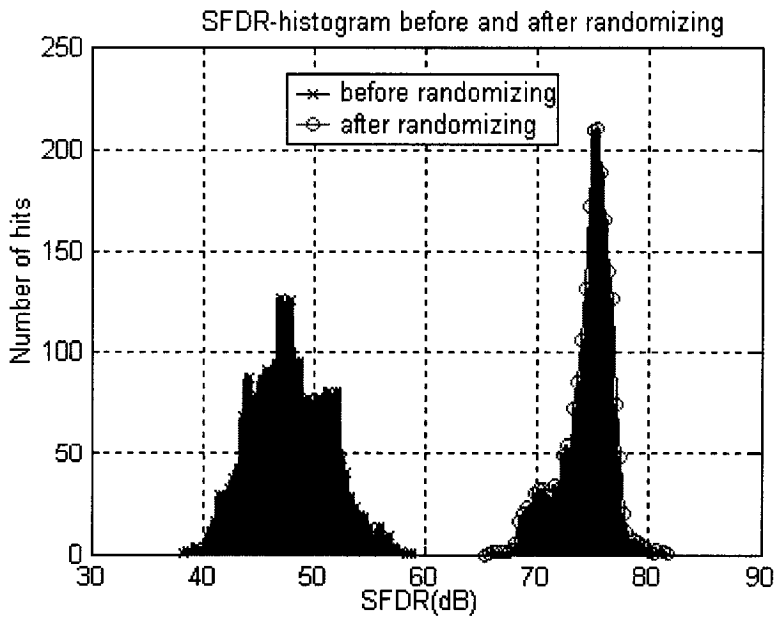


Figure 3.16: SFDR-histogram of the TIADC before and after the randomizing.

6. Conclusions

In this paper we presented the mathematical background describing the effect of randomizing the samples among the interleaved ADCs and we propose a randomizing and rotation method based on this analysis to randomize the mismatches among the ADC channels. A digitally oriented implementation of this new time-interleaved architecture is also presented. This method makes possible the realization of high-speed high-resolution TIADCs at the expense of little digital and analog circuitries overhead on the conventional TIADC. This method works continuously in the background, compensating for gain and offset variations due to temperature and power supply. Analysis and behavioral simulations show the effectiveness of the proposed approach. For a 10-bit 500 MS/s ADC, SFDR enhancement of more than 26 dB comparing to the conventional TIADC is achieved. The proposed method allows the building of high-speed and precision ADCs dedicated to modern wireless communication applications. Implementation on silicon of the proposed design is undertaken.

Acknowledgements

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References

[1] J. Mitola III, "Software Radio Architecture: Object-Oriented Approaches to Wireless Systems Engineering", *John Wiley & Sons Publishers*, 2000.

[2] X. Li, and M. Ismail, "Multi-Standard CMOS Wireless Receivers: Analysis and Design", *Kluwer Academic Publishers*, 2002.

[3] C. Conroy, D. Cline, P. Gray, An 8-b 85-MS/s parallel pipeline A/D converter in 1-μm MOS", *IEEE Journal of Solid-State Circuits*, Vol.28, pp.447 –454, Apr. 1993.

[4] R.Walden, "Analog-to-digital converter survey and analysis", *IEEE Journal on Selected Areas in Communications*, Vol.17, pp.539 –550, Apr. 1999.

[5]N. Kurosawa, H. Kobayashi, K. Maruyama, H. Sugawara, and K. Kobayashi, "Explicit analysis of channel mismatch effects in time-interleaved ADC systems", *IEEE transactions on Circuits and Systems I*, vol.48, pp.261-271, Mar. 2001.

[6] S. Sai-Weng, U. Seng-Pan,R. Martins and J. Franca, "Timing-mismatch analysis in high-speed analog front-end with nonuniformly holding output", in *Proc. IEEE Int. Symp. Circuits Systems*, pp. 129-132, 2003.

[7] J. Eklund and F. Gustafsson, "Digital offset compensation of time-interleaved ADC using random chopper sampling", in *Proc. IEEE Int. Symp. Circuits Systems*, pp. 447-450, 2000.

[8] J. Eklund, " Parallel analog-to-digital converter having random/pseudo-random conversion sequencing", *US patent* 598769, Jun. 2000.

[9] M. Tamba, A. Shimizu, H. Munakata, and T. Komuro, "A method to improve SFDR with Random Interleaved Sampling Method", in *Proc. IEEE Int. Test Conference*, pp. 512-520, 2001.

[10] G. Bernardinis, P. Malcovati, F. Maloberti, and E. Soenen, "Dynamic Stage Matching for Parallel Pipeline A/D Converters", in *Proc. IEEE Int. Symp. Circuits Systems*, pp. 905-908, 2002.

[11] K. El-Sankary, A. Assi and M. Sawan, "New sampling method to improve the SFDR of time-interleaved ADCs", in *Proc. IEEE Int. Symp. Circuits Systems*, pp Vol.1, pp. 833 -836, 2003.

[12] K. El-Sankary, A. Assi and M. Sawan, "Digitally-Oriented Channel Random Sampling Method for Parallel Time Inetrleaved ADCs", in *Proc. IEEE Northeast Workshop on Circuits and Systems*, pp.145-148, 2003.

[13] G. Leger, E. Peralias, and A.Rueda, "SNR probability in time-interleaved ADCs with random channel mismatches", in *Proc. IEEE Int. Symp. Circuits Systems*, pp. 380-383, 2002.

[14] K.Gulati and H. Lee, "A low-power reconfigurable analog-to-digital converter", *IEEE Journal of Solid-State Circuits*, Vol. 36, pp. 1900 –1911, Dec. 2001.

[15] U. Moon and B.Song, "Background digital calibration techniques for pipelined ADCs", *IEEE transactions on Circuits and Systems II*, Vol.44, pp.102 –109, Feb. 1997.

[16] E. Blecker, T. McDonald, O. Erdogan, P. Hurst and S. Lewis, "Digital background calibration of an algorithmic analog-to-digital converter using a simplified queue", *IEEE Journal of Solid-State Circuits*, Vol.38, pp.1059- 1062, Jun. 2003.

Chapter 4

DIGITAL BLIND BACKGROUND CALIBRATION FOR PIPELINED ADCs

4.1 Introduction

In recent years, pipelined switched-capacitor architecture has emerged as an especially attractive approach to implementing power-efficient Nyquist-rate ADCs with medium-to-high resolution at medium-to-high conversion rates. The effective resolution n per stage of a pipelined ADC is determined by the interstage gain G_i, as explained in Chapter 2. The 1.5b/stage architecture, where $n = 2$ with 1-b redundancy, is commonly used to maximize the conversion rate at reasonable power consumption [LEW92]. Decreasing the interstage gain means: 1) reduction in the feedback factor seen by the opamp, and 2) reduction in the opamp load capacitance by decreasing the number of comparators it must drive. This leads consequently to increasing the ADC speed. This architecture is also known to tolerate large comparator offsets ($\pm \frac{1}{4} V_R$) due to digital redundancy or digital error correction. In this chapter, a digital blind background calibration for 1.5b/stage pipelined ADC is presented. This contribution has been published in The «IEEE Transactions on Circuits and Systems-II, 2004» and it is reproduced in this chapter in section 4.2. This method has been extended in [ELS06b] to calibrate in the background the finite opamp gain in 1.5b/stage pipelined ADCs. This extension will be presented in section 4.3.

4.2 A Digital Blind Background Capacitor Mismatch Calibration Technique for Pipelined ADC

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Abstract— A new digital background calibration technique to compensate the capacitor mismatch in pipelined analog-to-digital converter (ADC) is presented. A digital signal from the ADC output is constructed so as to transform the capacitor mismatch to gain error. A simple modification to the conventional multiplying digital-to-analog converter (MDAC) allows the ADC to toggle between different configurations to create a reference signal used to calibrate blindly the ADC in the background. The creation of this signal does not produce any limitation for the ADC in terms of speed or degrading the input dynamic range. Simulation results show the effectiveness of this new method.

Index Terms—Analog-to-digital converter (ADC), pipelined ADC, background calibration, time interleaved ADC.

I. INTRODUCTION

A major limitation in the switched-capacitor pipelined analog-to-digital converter (ADC) is the capacitor mismatch due to the finite resolution of the technology that limits

the accuracy to about 10 bits. For good capacitor matching, large capacitors are needed. Consequently, the conversion speed goes down.

Numerous calibration techniques have been proposed to tackle the technology limitation and to increase the ADC linearity. The foreground method interrupts the normal operation of the ADC [1]. The oversampled pipelined ADC [2] and active [3], passive [4], and digital [5] error averaging methods trade ADC bandwidth with resolution. The commutative feedback capacitor switching [6] and random swapping [7] reduce the differential nonlinearity (DNL) but not the integral nonlinearity (INL). The addition of a calibration signal [8] causes the reduction of the useful dynamic range of the converter.

In Section II, a digital background blind calibration technique is presented. The main target of this method is to create a reference signal from every pipelined stage under calibration. These signals are used to calibrate the stages and they do not produce any limitation of the ADC in terms of speed or input dynamic range. The rest of this paper is arranged as follows. Section III presents a modified multiplying digital-to-analog converter (MDAC) proposed to generate the reference signal. Section IV provides the simulation results, and conclusions are given in Section V.

II. BLIND BACKGROUND CALIBRATION

The analog residue V_{i+1} of stage i of a 1.5-b/stage pipelined ADC using capacitor-flip-over MDAC [9] is expressed as

$$V_{i+1} = 2 \cdot V_i - D_i \cdot V_r \tag{4.1}$$

where the digital code D_i can take one of three values –1, 0 or +1, and the reference voltage is V_r.

In a practical implementation, V_{i+1} is given by:

$$V_{i+1} = \left(\left(1 + \frac{C_1}{C_2} \right) \cdot V_i - \left(\frac{C_1}{C_2} \right) \cdot D_i \cdot V_r \right) \cdot (1 - \varepsilon_i) + V_{ofi} \tag{4.2}$$

where $C_1/C_2 = 1+\alpha_i$, α_i represents the capacitor mismatch, ε_i is the error due to the finite opamp gain, and V_{ofi} represents the offset term due to the charge injection effects and residual op-amp offset. The errors ε_i and V_{ofi} can be controlled by the analog designer but the capacitor mismatches have a technological limit that usually limits the ADC accuracy to no better than about 10 bit.

Taking into consideration only the capacitor mismatch, (4.2) is written as follows:

$$V_{i+1} = \left(1 + \frac{C_1}{C_2} \right) \cdot V_i - \left(\frac{C_1}{C_2} \right) \cdot D_i \cdot V_r \tag{4.3}$$

This value is digitized by the previously calibrated backend ADC (Fig. 4.1) and the result is given by

$$D[V_{i+1}] = D\left[\left(1 + \frac{C_1}{C_2} \right) \cdot V_i - \left(\frac{C_1}{C_2} \right) \cdot D_i \cdot V_r \right] \tag{4.4}$$

where $D[V]$ denotes the digitized value of V. Subtracting from (4.4) the digitized value of V_i by the stage i, ($D[D_i V_r]$), as shown in Fig. 2.1, yields

$$V_{gd} = D\left[\left(1 + \frac{C_1}{C_2} \right) \cdot V_i - \left(\frac{C_1}{C_2} \right) \cdot D_i \cdot V_r \right] - D[D_i \cdot V_r]$$

$$= D\left[\left(1+\frac{C_1}{C_2}\right)\cdot\left(V_i - D_i \cdot V_r\right)\right] = D\left[g_1 \cdot V_g\right] \tag{4.5}$$

where g_1 and V_g are given by:

$$g_1 = \left(1+\frac{C_1}{C_2}\right) \tag{4.6}$$

$$V_g = V_i - D_i \cdot V_r \tag{4.7}$$

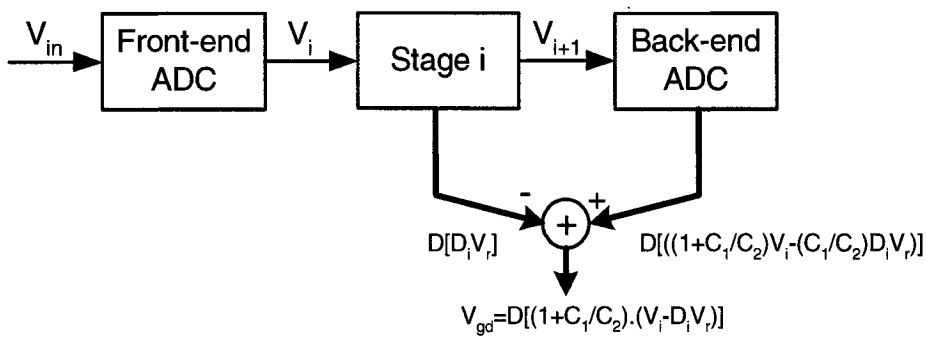


Figure 4.1: Digital transformation of the capacitor mismatch in capacitor-flip-over MDAC to gain error.

This manipulation transforms the capacitor mismatch to a gain error without the need to change the conventional capacitor-flip-over MDAC structure. This digital output V_{gd} is different from the digital representation of the analog input V_{in} digitized by the ADC and it is constructed simultaneously with the normal operation of the ADC. The capacitor mismatch could be changed to gain error also without the need of explicit construction of the signal V_{gd} by redefining the input, the output, and the equivalent radix of every stage taking into account the effects of all the mismatch errors [10]. In this case, the digital

output of the ADC can be obtained by using a radix calculation [10] based on the modified radix where it is equal 2 in our case.

Now, by interchanging the role of C_1 and C_2, (4.5) becomes

$$V_{gd} = D\left[\left(1+\frac{C_2}{C_1}\right)\cdot\left(V_i - D_i \cdot V_r\right)\right] = D\left[g_2 \cdot V_g\right] \tag{4.8}$$

where g_2 is given by:

$$g_2 = \left(1+\frac{C_2}{C_1}\right) \tag{4.9}$$

By toggling the stage i at frequency $f_s/2$ between the two configurations obtained from swapping the role of C_1 and C_2, as shown in Fig. 4.2, V_g can be considered to be sampled by two-channel time-interleaved ADC (TIADC).

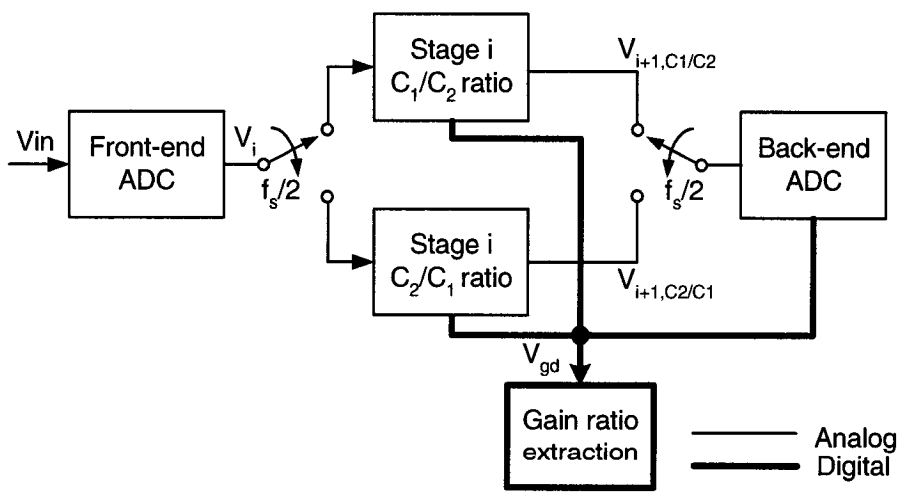


Figure 4.2: The new background calibration principle.

The first ADC channel has a gain g_1 and the second has a gain g_2, as illustrated in Fig. 4.3.

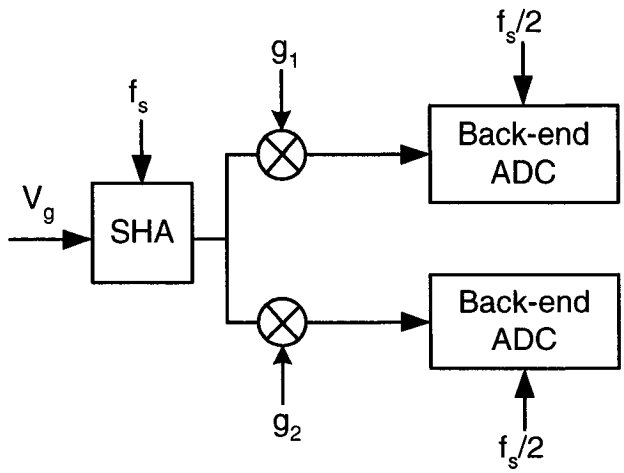


Figure 4.3: Drawing the ADC like two channels TIADC.

Based on the theory of TIADCs [11], the gain mismatch between g_1 and g_2 in the two paths will create an in-band image at $kf_s/2 \pm f_{in}$ in the spectrum of the signal V_{gd} where f_{in} is the frequency of the signal V_g given by (4.7) and f_s is the sampling frequency. The spectrum of the digitized output V_{gd} is given by (4.10) and is shown in Fig. 4.4(a) and (b).

$$V_{gd}(f) = \frac{1}{2T_s} \sum_{k=-\infty}^{+\infty} \left(V_g\left(f - \frac{kf_s}{2} \right) \times \left(g_1 + g_2 e^{-jk\pi} \right) \right) \tag{4.10}$$

From Fig. 4.4(b), we see that a sine at frequency f_o will have an image at frequency $f_{im} = f_s/2 - f_o$. This two-channel TIADC is free from offset and skew mismatch problems between the channels usually found in TIADCs. Using the same backend ADC to sample the signal V_{i+1} means that the offset is same for the two channels [including V_{ofi} in (4.2)], and the skew error is ruled out since the signal V_i is sampled by the same sample-and-hold.

In [12], a method to equalize the gain between two channels of a TIADC is proposed. In that method, the output of the ADC, in our case V_{gd}, is chopped by multiplying it by

$(-1)^n$ and the signal V_{gdc} is obtained (Fig. 4.5). This chopping will cause the image at f_{im} to shift to f_o and the input at f_o to shift to f_{im} (Fig. 4.4(c)). The multiplication of V_{gd} and V_{gdc} in the time domain will result a dc component proportional to the gain mismatch (Fig. 4.4(d))

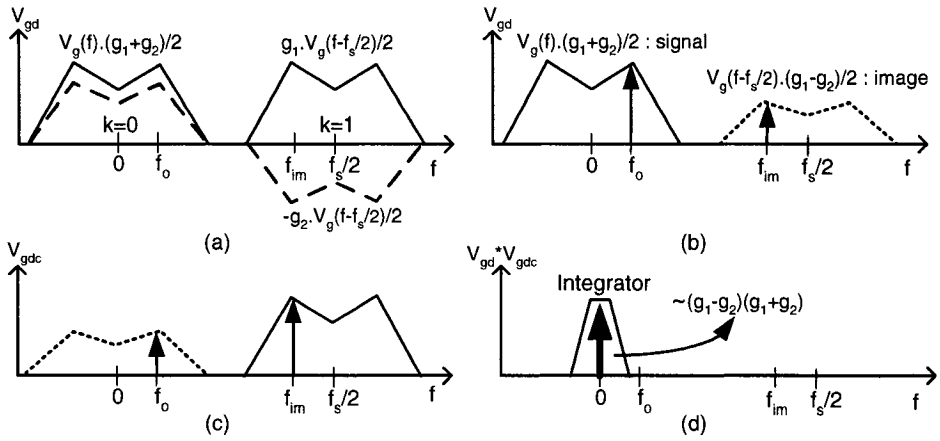


Figure 4.4: Output spectrums for $f_s/2$ swapping frequency in (a) and (b). The spectrum after (c) chopping and (d) convolution.

By scaling this spectrum by *mu* and using an integrator (Fig. 4.4(d)), the dc signal can be extracted ($R(n)$ in Fig. 4.5). $R(n)$ is used to scale the gain g_2 to force the image to be eliminated. In the steady state, the negative feedback in Fig. 4.5 will cause $R(n)$ to converge toward g_1/g_2 that is equal to the needed ratio C_1/C_2.

Aliased signals due to sampling and overlapping between the image and the input signal (when V_g is at $f_s/4$) will deteriorate the image and weaken the precision of the gain ratio measurement. To protect the image, we propose to swap the conversion between the two configurations at frequency $f_s/4$ instead of $f_s/2$. We will see also that this will accelerate the convergence of this method. Swapping at frequency $f_s/4$ means that two

samples will be converted by the ADC in the first configuration and will experience a gain g_1, and two other samples by the second configuration and will experience the gain g_2.

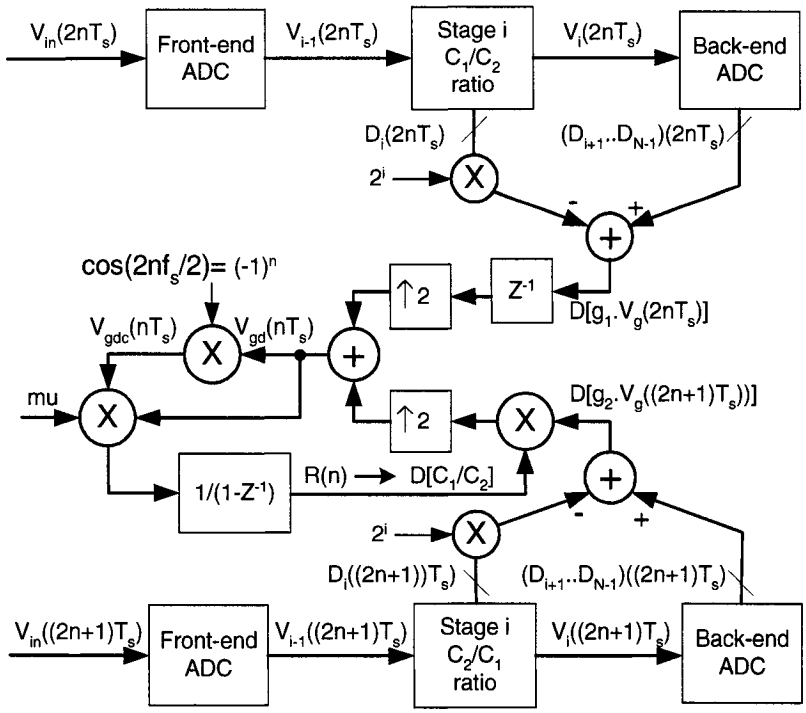


Figure 4.5: Gain ratio extraction diagram.

This swapping means it as if we have four-channel TIADC where the first two ADCs and the second two ADCs are identical, respectively. This modification is not feasible in traditional TIADCs because it is impossible to have two identical ADCs. The output V_{gd} obtained at $f_s/4$ swapping frequency is given by:

$$V_{gd}(f) = \frac{1}{4T_s} \sum_{k=-\infty}^{+\infty} \left(V_g\left(f - \frac{kf_s}{4}\right) \times \left(g_1 + g_1 e^{-jk\pi/2} + g_2 e^{-jk\pi} + g_2 e^{-jk3\pi/2}\right) \right) \tag{4.11}$$

Fig. 4.6(a) shows the spectrum output of V_{gd} due to swapping at $f_s/4$. After the addition of the entire spectrums in (11), a sine at frequency f_o will have two images, one at $f_{im1} = f_s/4 - f_o$ and the other at $f_{im2} = f_s/4 + f_o$ [Fig. 4.6(b)]. By multiplying V_{gd} by $\cos(2\pi n f_s/4)$ instead of $\cos(2\pi n f_s/2) = (-1)^n$, the spectrum of V_{gd} will be shifted by $f_s/4$ and that will result V_{gdc}, as shown in Fig. 4.6(c). The convolution between V_{gd} and V_{gdc} will result in a dc component proportional to the gain mismatch, and it will be extracted as explained earlier by an integrator.

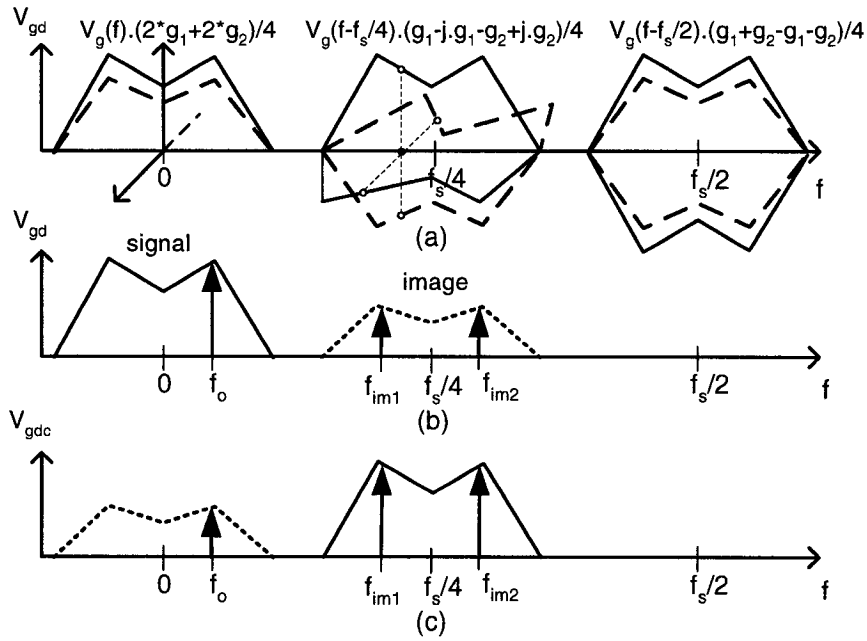


Figure 4.6: Spectrum outputs for $f_s/4$ swapping frequency in (a) and (b) and the spectrum after chopping in (c).

Creating more images especially one below $f_s/4$, will protect the image from aliased signals due to sampling and also will accelerate the conversion of the algorithm and make it more robust against transient input where the image and the signal are superimposed. Moreover, a random swap between $f_s/2$ and $f_s/4$ or any other frequency will modulate the

image in a frequency hopping scheme and protect the convergence against persisting noise such as a false image due to input signal and not to capacitor mismatch.

III. MDAC MODIFICATION

To allow the swapping of the stage under-calibration between the two gains (g_1 and g_2) and using different frequency rates ($f_s/2, f_s/4$ or any other frequency), the only needed modification on the MDAC is to add two switches as shown in Fig. 4.7(a). The MDAC operates using three clocks Ph_1, A_2 and B_2 to control the sampling and the multiplying-by-two phases. The timing relations of the clocks are illustrated in Fig. 4.7(b).

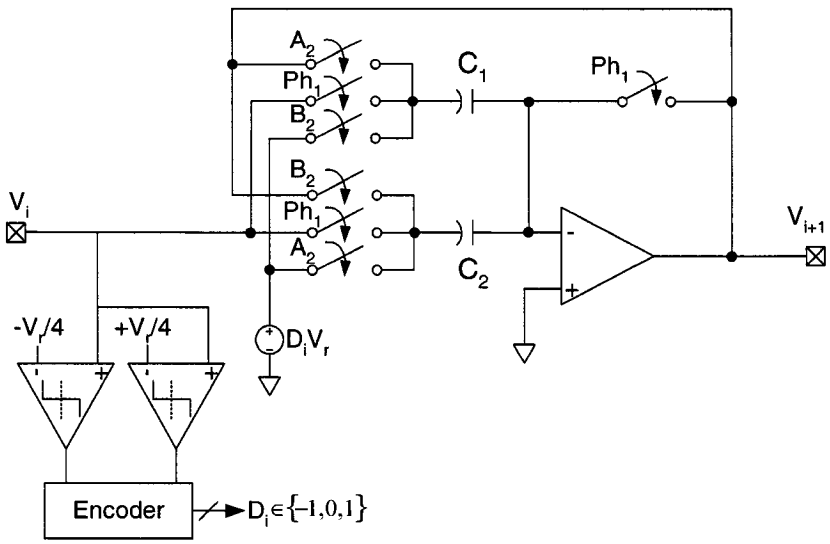
To toggle between the capacitors at $f_s/2$, two signals A and B with frequencies $f_s/2$ are needed. By multiplying A and B by Ph_2, we obtain the signals A_2 and B_2. During the sampling phase (Ph_1 is high), V_i is sampled onto the capacitors C_1 and C_2. During the multiplying-by-two phase and when A_2 is high, the voltage D_iV_r is sampled onto the capacitor C_2 and C_1 is chosen as the feedback capacitor. The inverse happens when B_2 is high.

To perform toggling at $f_s/4$, the periods of A and B are selected also equal to $f_s/4$. In this manner, two samples will be converted by the gain g_1, since A_2 is high for two successive periods, and two samples by the gain g_2 when B_2 is high (Fig. 4.7).

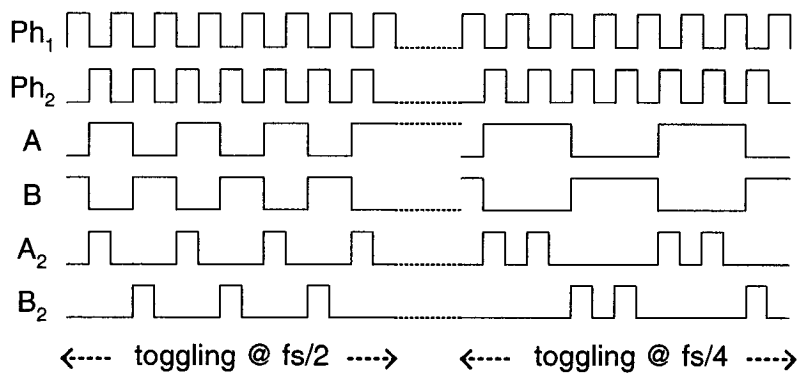
IV. SIMULATION RESULTS

Simulations have been performed to verify the effectiveness of this new blind background calibration technique. A capacitor mismatch of 3% and comparator offsets of $\pm V_r/10$ were added in all the stages of 15-b 1.5-b/stage pipelined ADC. The number of

corrected stages was taken equal 8. To reach 15-b accuracy for this ADC, the number of total samples needed to correct the eight stages was around 2^{23}. For a 100-MS/s ADC, this corresponds to 0.08 s that could be done in the warm-up period, while the ADC can still operate normally.



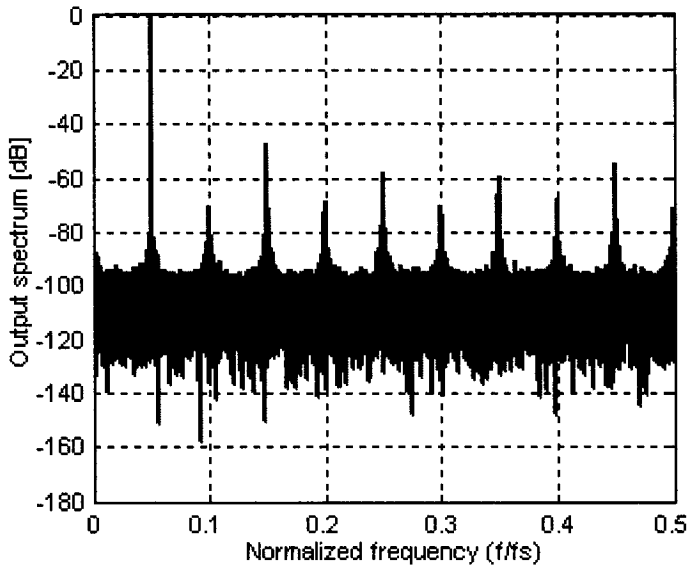
(a)



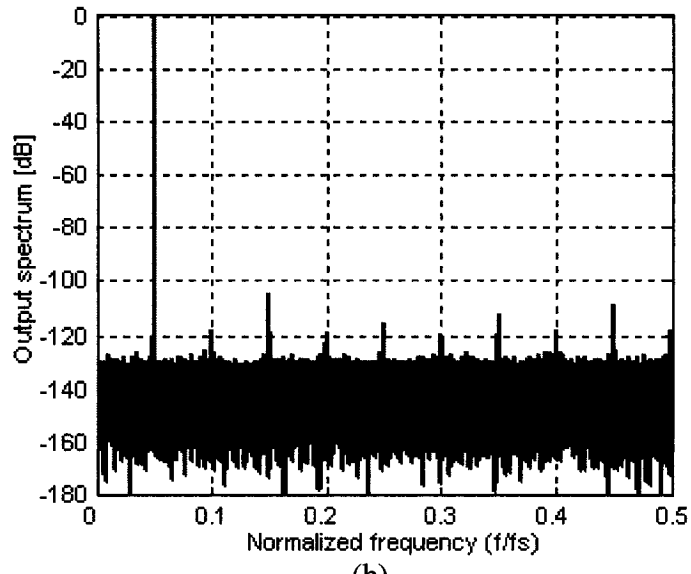
(b)

Figure 4.7: MDAC modification allowing the swapping between (a) the different capacitor ratios, the (b) MDAC control signals.

A full-scale sinewave at 1/20 the sampling frequency (f_s) was applied to the input of the 15-b ADC before and after calibration. Fig. 4.8(a) shows the power spectrum of the digital output without calibration.



(a)



(b)

Figure 4.8: Spectrum of the output of a 15-b pipelined ADC (a) without and (b) with the proposed calibration technique.

The signal-to-noise-and-distortion ratio (SNDR) is 43.9 dB, resulting in an effective number of bits (ENOB) of 7 bits, and the spurious free dynamic range (SFDR) is 47 dB. The power spectrum density of the digital output after calibration is shown in Fig. 4.8(b). The SNDR becomes 89.3 dB, resulting in an ENOB of 14.5 bits, and the SFDR is increased to 103 dB.

V. CONCLUSIONS

A new blind background calibration technique to compensate for the capacitor mismatch in pipelined ADCs is proposed. A digital signal from the ADC output is constructed so as to transform the capacitor mismatch to a gain error. A simple modification to the conventional MDAC allows the ADC to swap between different configurations to create a reference signal used to calibrate the ADC in the background. This method does not produce any limitation of the ADC in terms of speed or input dynamic range. Although a 1.5-b/stage pipelined ADC is demonstrated in this paper, the proposed method is applicable to multi-bit pipelined ADCs, and then appropriate modifications to the MDAC are needed.

ACKNOWLEDGEMENTS

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REFERENCES

[1] H. Lee, "A 12-b 600 ks/s digitally self-calibrated pipelined algorithmic ADC *IEEE J. Solid-State Circuit*s, vol.29, pp.509-515, Apr. 1994.

[2] A. Shabra and H. Lee, "Oversampled pipeline A/D converters with mismatch shaping," *IEEE J. Solid-State Circuit*s, vol.37, p.566-578, May 2002.

[3] B. Song, F. Tompsett and K. Lakshmikumar, "A 12-bit 1-Msample/s capacitor error-averaging pipelined A/D converter," *IEEE J. Solid-State Circuit*s, vol.23, pp.1324-1333, Dec.1988.

[4] Y. Chiu, "Inherently linear capacitor error-averaging techniques for pipelined A/D conversion," *IEEE Trans. Circuits Syst. II*, vol. 47, pp. 229-232, Mar. 2000.

[5] P. Rombouts and L. Weyten, "A digital error-averaging technique for pipelined A/D conversion," *IEEE Trans. Circuits Syst. II*, vol. 45, pp. 1321-1323, Sept. 1998.

[6] P. Yu and H. Lee, "A 2.5-V, 12-b, 5-MSample/s pipelined CMOS ADC," *IEEE J. Solid-State Circuit*s, vol. 31, pp. 1854 -1861, Dec. 1996.

[7] H. Fetterman, "Multistage analog-to-digital converter with amplifier component swapping for improved linearity," US patent 6 515 611, Feb.2003.

[8] H. Liu, Z. Lee and J. Wu, "A digital background calibration technique for pipelined analog-to-digital converters," in *Proc. IEEE Int. Symp. Circuits System*s, vol.1, pp.881 -884, May 2003.

[9] A. Abo and P. Gray," A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter", *IEEE Journal of Solid-State Circuits*, Vol.34, pp. 599 -606, May 1999.

[10] J. Li and U. Moon, "Background calibration techniques for multistage pipelined ADCs with digital redundancy," *IEEE Trans. Circuits Syst. II*, vol. 50, pp. 531–538, Sep. 2003.

[11] N. Kurosawa, H. Kobayashi, K. Maruyama, H. Sugawara and K. Kobayashi, "Explicit analysis of channel mismatch effects in time-interleaved ADC systems," *IEEE Trans. Circuits Syst. I*, vol. 48, pp. 261–271, Mar. 2001.

[12] S. Jamal, D. Fu, N. Chang, P. Hurst and S. Lewis, "A 10-b 120-Msample/s time-interleaved analog-to-digital converter with digital background calibration," *IEEE J. Solid-State Circuit*s, vol. 37, pp. 1618 -1627, Dec. 2002.

4.3 Background Finite Opamp Gain Compensation Technique in Medium Resolution 1.5b/stage Pipelined ADC

The proposed calibration method is extended in this section to calibrate medium-resolution, high-speed, 1.5-bit/stage pipelined stages, which are built by fast but low gain opamps to allow the implementation of high speed ADCs.

4.3.1 Gain ratio extraction

Ideally, for stage i with 1.5bit/stage, named as radix 2, G_i is equal to 2 and V_{daci} is equal to $-V_R/2$. Capacitor mismatch and the opamp finite gain deviate G_i and V_{daci} from their ideal values. According to eq. (2.2) the input signal can be accurately generated when the effective values of V_{daci} and G_i are used.

Assuming that we can change the stage under calibration between two configurations (e.g. radix 2 and radix<2) periodically at frequency $f_s/2$ (Fig. 4.9), the output V_{i+1} will be written as

$$V_{i+1,config1}(2n) = G_{1,config1} \times V_g(2n) \tag{4.12}$$

$$V_{i+1,config2}(2n+1) = G_{2,config2} \times V_g(2n+1) \tag{4.13}$$

where n is a discrete-time index and V_g is given by:

$$V_g = V_i - V_{daci} \tag{4.14}$$

Based on these equations, the design in Fig. 4.9 can be considered as two-channel TIADC with gains g_1 and g_2 for configurations 1 and 2 respectively as illustrated in Fig. 4.3. Extraction of the ratio $G_{1,config1}/G_{2,config2}$, in a similar way as presented in section 4.2,

can be used to compensate for the finite opmap gain as will be explained in the following sub-sections.

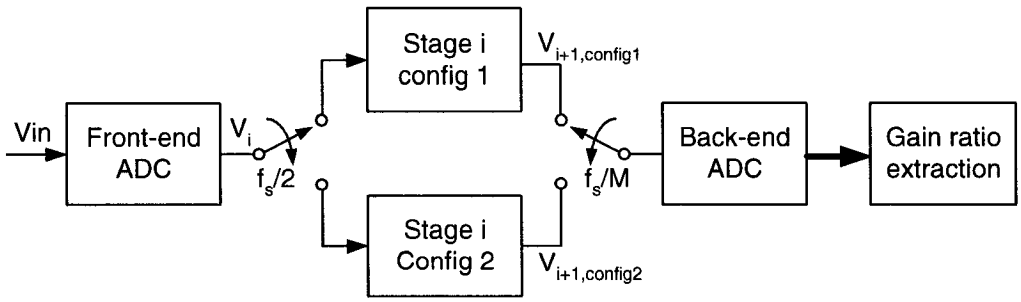


Figure 4.9: Swapping the stage *i* between two configurations.

4.3.2. Gain ratio construction

For a radix 2 MDAC, shown in Fig. 4.10(a), G_i and V_{daci} in (2.2) are given by:

$$G_i = \left(1 - \frac{1}{A.f}\right) \cdot \left(1 + \frac{C_s}{C_f}\right) \tag{4.15}$$

$$V_{daci} = \frac{C_s}{C_s + C_f} V_r D_i \tag{4.16}$$

where A is the opamp gain, C_s and C_f are the sampling and the feedback capacitors respectively. V_r is the reference voltage, D_i is the digital code and the feedback factor f is equal to:

$$f = \frac{C_f}{C_f + C_s + C_p} \tag{4.17}$$

C_p is the parasitic capacitor from the opamp input to ground.

For pipelined ADC with radix < 2, shown in Fig. 4.10(b), these values are:

$$G_i = \left(1 - \frac{1}{Af}\right) \frac{C_{s1}}{C_f} \tag{4.18}$$

$$f = \frac{C_f}{C_f + C_{s1} + C_r + C_p} \tag{4.19}$$

$$V_{daci} = \frac{C_r}{C_{s1}} V_r D_i \tag{4.20}$$

where C_{s1} and C_r are the sampling capacitors and C_f is the feedback capacitor.

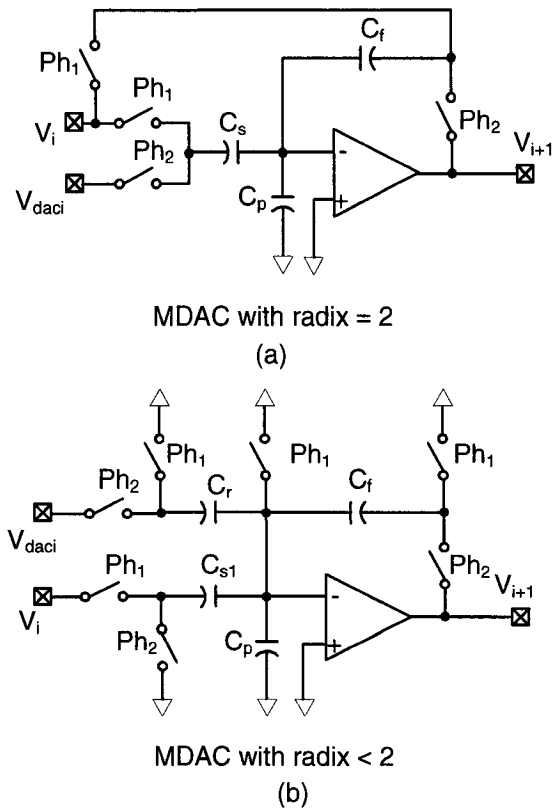


Figure 4.10: MDAC implementations for 1 bit/stage pipelined ADC: (a) radix 2 and (b) radix <2.

Actually, for current CMOS technology a capacitor matching around 10-bit accuracy can be obtained [SUT88, SHA02], thus V_{daci} can be computed to the required precision. This makes, for low voltage medium-resolution (around 10-bit) and high-speed ADC, the opamp finite gain is the dominant source of the ADC nonlinearity due to the deviation of

G_i from its real value. Notice from equations (4.17) and (4.19) that for a finite gain opamp the effect of C_p, which is almost same order with the other capacitors, is serious on reducing the feedback factor to unknown value and consequently the gain G_i. Usually C_f, C_s, C_{sl} and C_r are formed from matched unit capacitors of value C. Suppose that $C_f = C_s = C_r = nC$ and $C_{sl} = n_1 C$, where $n < n_1 < 2n$ to realize a radix less than 2 in eq. (4.18). G_i in equations (4.15) and (4.18) are written as shown in equations (4.21) and (4.22) respectively.

$$G_i = 2 \cdot \left(1 - \frac{2n + x}{An}\right) = G_{1,radix2} \tag{4.21}$$

$$G_i = \left(1 - \frac{n_1 + 2n + x}{An}\right)\frac{n_1}{n} = G_{1,radix<2} \tag{4.22}$$

where $C_p = x.C$ and x is unknown value. Now by replacing $C_f = C_s = C_r = n_2.C$ and $C_{sl} = n_3 C$, with $n_1/n = n_3/n_2$, in equations (4.15) and (4.18) we obtain:

$$G_i = 2\left(1 - \frac{2n_2 + x}{A.n_2}\right) = G_{2,radix2} \tag{4.23}$$

$$G_i = \left(1 - \frac{n_3 + 2n_2 + x}{An_2}\right)\frac{n_3}{n_2} = G_{2,radix<2} \tag{4.24}$$

If the ratios $G_{1,radix2}/G_{2,radix2}$ and $G_{1,radix<2}/G_{2,radix<2}$ are known, A and x can be found. By finding the value of A and x at the required ADC precision and computing the real value of the gain G_i, the input V_{in} can be found accurately using eq. (2.2).

By realizing an MDAC that is configured in radix 2 and radix <2 and measuring these gain ratios, using the above method, the ADC calibration can be fulfilled. Below a modified MDAC to realize the ADC configuration with little overhead is proposed.

4.3.3 MDAC configuration

To implement the different configurations with the least overhead only one capacitor C_3 is added to the radix <2 MDAC used in [BLE03] as shown in Fig. 4.11(a) (C_p is removed for clarity). In this MDAC $C_1 = C_2$ and $C_3 = C_4$. To measure the ratio $G_{1,radix<2}/ G_{2,radix<2}$ a control signal K is set to 1 and another control signal S is alternated between 1 and 0 at frequency $f_s/2$ (Fig. 4.12(b)) or $f_s/4$ ((Fig. 4.12(c)). For $K = 1$ and $S = 1$, C_3 is added in parallel to C_p (Fig. 4.11(a)). For $K = 1$ and $S = 0$, C_3 is grounded from both extremities (Fig. 4.11(b)). Connecting C_3 in parallel to C_p changes the feedback factor f without affecting the equality between n_1/n and n_3/n_2 needed in equations (4.22) and (4.24) to obtain the radix <2.

To measure the ratio $G_{1,radix2}/ G_{2,radix2}$, K is set to 0. For $K = 0$ and $S = 1$ capacitors C_1 and C_2 are used to realize the radix 2 MDAC and C_3 and C_4 are shunted to ground (Fig. 4.9(c)). For $K = 0$ and $S = 0$ capacitors C_3 and C_4 are used to realize the radix 2 MDAC and C_1 and C_2 are shunted to ground (Fig. 4.9(d)).

With these modifications to the MDAC, equations (4.21)-(4.24) are constructed and the ratios are measured as discussed above. After solving the equations $G_{1,radix2}/G_{2,radix2}$ and $G_{1,radix<2}/ G_{2,radix<2}$, the opamp gain A and the parasitic capacitor $C_p=xC$ are estimated, consequently the gains G_i, and then the input voltage is estimated accurately using equation (2.2). Fig. 4.13 shows the MDAC after the addition of the control switches and the capacitor C_3. Adding of this capacitor decreases the feedback factor and increases the opamp settling time and therefore a higher bandwidth from the opamp is needed. However, this method allows the use of a low gain opamp that eases its design for higher

bandwidth. After calibration is done only one configuration (e.g. radix=2) is maintained and the swapping between the 2 configurations of radix 2 is only needed to track the changes of the gain A with the temperature variation (x is already determined).

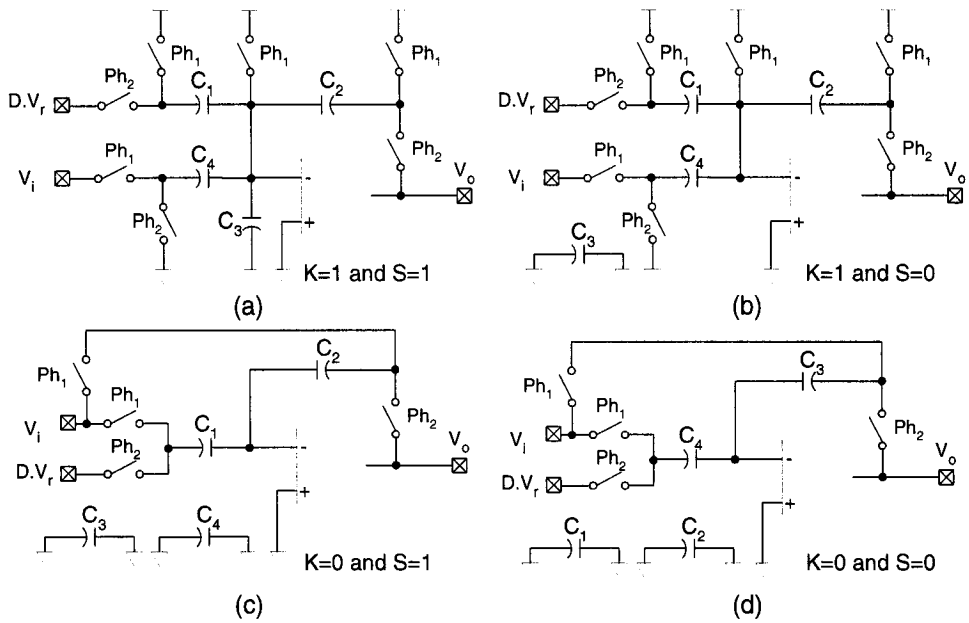


Figure 4.11. MDAC configurations: (a) *K=1* and *S=0* (radix < 2), (b) *K=1* and *S=1* (radix <2), (c) *K=0* and *S=1* (radix 2), (d) *K=0* and *S=0* (radix 2).

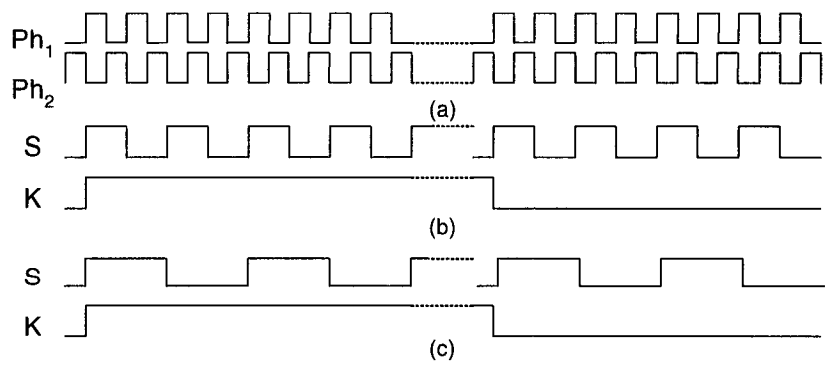


Figure 4.12. Control signals for the MDAC: (a) S/H clock phases, (b) the control signal to swap the TIADCs at $f_s/2$,(c) $f_s/4$.

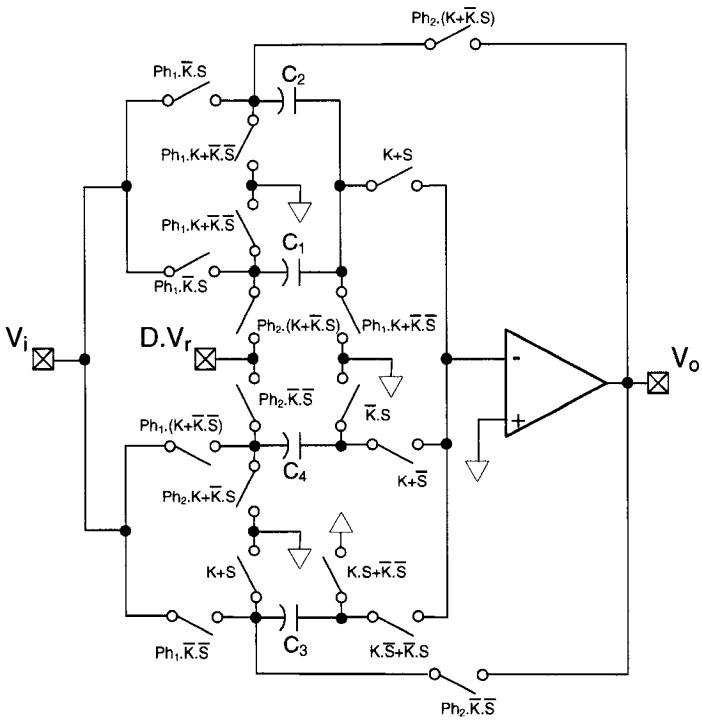
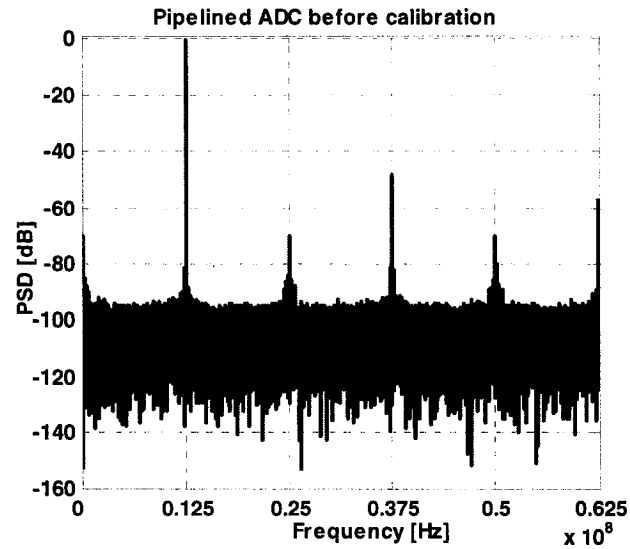


Figure 4.13. MDAC modifications with the control signals.

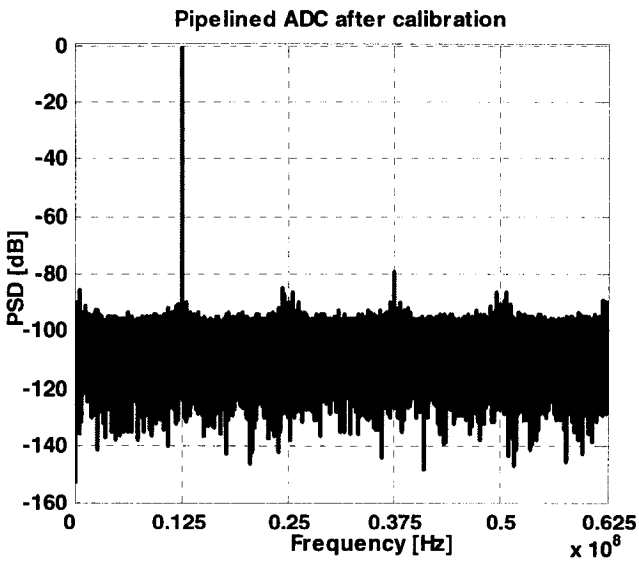
4.3.4 Results

Simulations have been done to verify the effectiveness of the proposed calibration techniques. The simulated 10-bit 125 MS/sec pipelined ADC comprises opamps with gain of 40 dB. A traditional 10-bit design would require an opamp with at least 65 dB of gain. The capacitor mismatch was assumed to be less than 0.1%, which means that the capacitors are matched for 10-bit precision. Comparator offsets of $\pm V_r/10$ were added in all the stages of the pipelined ADC. The number of corrected stages was taken equal 4. To reach 10-bit accuracy for this ADC, the number of total samples needed to correct the 4 stages was around 2^{21}. For a 125-MS/sec ADC, this corresponds to 0.016 second that could be done in the warm-up period, while the ADC can still operate normally. A full-scale sinewave at 1/10 the sampling frequency (f_s=125MHz) was applied to the input of

the ADC. Fig. 4.14(a) shows the power spectrum of the digital output without calibration.



(a)



(b)

Figure 4.14. Spectrum of the output of the 10-bit pipelined ADC: (a) without and (b) with the proposed calibration technique.

The signal-to-noise-and-distortion ratio (SNDR) is 44 dB resulting in an effective number of bits (ENOB) of 6.9 bits; the spurious free dynamic range (SFDR) is 48 dB. The power spectrum density of the digital output after calibration is shown in Fig. 4.14(b) The SNDR becomes 61 dB resulting in an ENOB of 9.9 bits, and the SFDR is increased to 79.7 dB

Chapter 5

DIGITAL BACKGROUND CALIBRATION USING IMPRECISE VOLTAGE INJECTION

5.1 Introduction

For high resolution pipelined ADCs, converting more bits per stage generally decreases power consumption. This is mainly due to the fact that resolving multi-bit per stage reduces the accuracy and settling requirement of the MDAC opamp and the total number of stages. Moreover, resolving multi-bit per stage in the front-end stages relaxes the noise and matching requirements for the following stages [CLI96]. As a result, a high performance pipelined ADC architecture has one or two front-end stages with higher resolution followed by low-resolution stages. To meet the high resolution requirement, the capacitor mismatch and the finite opamp gain have to be compensated for. Another concern in pipelined ADC is that several calibration methods and the gain error in the front-end sample and hold (S/H) cause the slope of the overall ADC transfer characteristic to be not well controlled. Figure 5.1 shows that the gain for the input-output relationship of digitally calibrated pipelined ADC is different from the ideal one and that causes a global gain mismatch.

In Figure 5.2, the transfer functions of two calibrated ADCs (ADC_1 and ADC_2) are compared with the ideal one. When these ADCs are used to form two-channel TIADC

their global gain mismatch will create in-band distortions, as explained in section 2.3.2, that degrade considerably the SFDR and the SNDR performances.

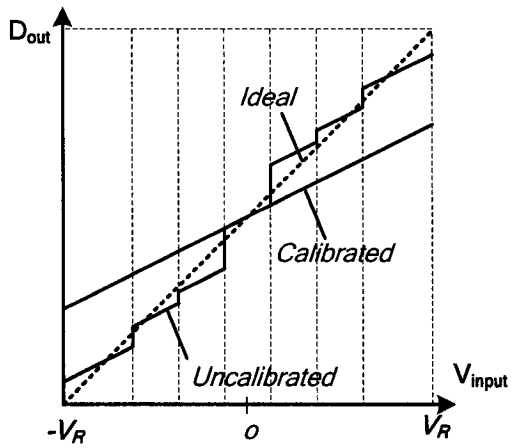


Figure 5.1: The input-output relationship of the overall pipelined ADC.

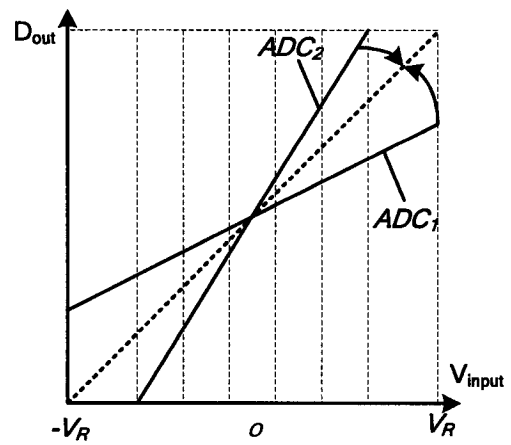


Figure 5.2: Global gain correction for 2 ADCs.

In this chapter a novel background calibration method, using imprecise voltage injection to calibrate multi-bit/stage pipelined ADC, is presented. Furthermore, a global gain correction for multi-channel pipelined ADC is also presented. This work was

accepted for publication in The «IEEE Transactions on Circuits and Systems-II, 2006». This contribution is reproduced in the following pages.

5.2 A Background Calibration Technique for Multi-bit/Stage Pipelined and Time-Interleaved ADCS

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Abstract— A digital background calibration technique to compensate for the nonlinearity and gain error in the sub-digital-to-analog converter (SDAC), and the operational amplifier finite dc gain in multi-bit/stage pipelined analog-to-digital converter (ADC) is proposed. By injecting subtractive calibration voltages in a modified conventional multi-bit multiplying digital-to-analog converter and performing correlation based successive coefficient measurements, a background calibration is performed. This calibration technique does not need an accurate reference voltage or an increasing in the SDAC resolution. A global gain correction essential for time-interleaved ADCs is presented. Simulation results show that in the presence of realistic capacitor and resistance mismatch and finite opamp gain, this technique improves the linearity by several bits in single and multi-channel pipelined ADC.

Index Terms— Pipelined analog-to-digital converter, multi-bit/stage ADC, background calibration, time-interleaved ADC.

I. INTRODUCTION

Resolving multi-bit per stage in pipelined analog-to-digital converter (ADC) decreases the power consumption by reducing the accuracy and settling requirement of the residue amplifier [1]. Regarding the resolution, the capacitor mismatch and the finite opamp gain determine the accuracy of CMOS pipelined ADC.

Several calibration methods have been proposed to calibrate multi-bit/stage pipelined ADCs. Self-calibration interrupts the operation of the ADC [2]. Background DAC noise cancellation (DNC) [3, 4], oversampling calibrator [5], and DAC auto-calibration [6] correct only for the sub-digital-to-analog converter (SDAC) nonlinearity. Other methods that address the interstage gain error in multi-bit/stage pipelined ADC, such as the gain error correction (GEC) [7], require the addition of an accurate analog voltage. The SDAC and feedback capacitor averaging (DFCA) with mismatch noise cancelling (MNC) [8] and the recently proposed subtractive dither-continuous gain correction (SD-CGC) [9] correct for the SDAC nonlinearity and for interstage gain error in the SDAC but not the gain error due to the op-amp finite dc gain. Also recently combining between the DNC and GEC [10] methods is demonstrated to address nonlinearity and the interstage gain error.

In this paper, a background calibration technique that corrects for the nonlinearity and gain error in the SDAC and the op-amp finite dc gain in multi-bit/stage pipelined ADC is presented. In section II, the background calibration technique is presented. Section III provides the simulation results, and finally conclusions are given in Section IV.

II. Background Calibration Technique

A. Multi-bit/stage Pipelined ADC Digital Calibration

For a 2.5-bit/stage multiplying digital-to-analog converter (MDAC) shown in Fig. 5.3(a), the residue voltage for the stage i can be derived as:

$$V_o = G_A \cdot G_C \cdot \left(V_i - V_{daci} + \frac{C_T + C_p}{C_T} \cdot V_{os} \right) \tag{5.1}$$

where $C_T = C_f + C_1 + C_2 + C_3$, $G_C = C_T / C_f$, and $G_A = 1/(1+1/Af)$. A is the opamp dc gain, the feedback factor $f = C_f/(C_T + C_p)$ and C_p is the virtual ground parasitic capacitance. V_{os} is the input-referred offset voltage of the op-amp. The SDAC output $V_{daci} = ((d_1.C_1 + d_2.C_2 + d_3.C_3)/C_T) \cdot V_R$, where V_R is the reference voltage, d_i are the digital output codes of the sub-analog-to-digital converter (SADC), where $d_i \in \{-1, 0, 1\}$ and $d = \sum_{i=1}^{3} d_i$.

Fig. 5.3(b) depicts the residue plot of a realistic 2.5-bit MDAC given by (5.1) compared with an ideal one. Nonlinearity of the SDAC and the interstage gain error introduce mismatch in the residue jumps in the different boundaries of the digital code d. These errors generate discontinuities in the input-output relationship of the uncalibrated ADC that cause deleterious missing codes and harmonic distortion that degrade considerably the ADC performance.

By measuring exactly the value of the jumps $G_A(C_i/C_f)V_R$ in the residue and by using the following equation the residue output becomes linear when it is referred to the

input of the stage i despite the errors generated from the SDAC and the op-amp finite gain.

$$V_o + \sum_{i=1}^{3} d_i \cdot G_A \cdot \frac{C_i}{C_f} \cdot V_R = G_A \cdot G_C \cdot V_i + V_{off} \tag{5.2}$$

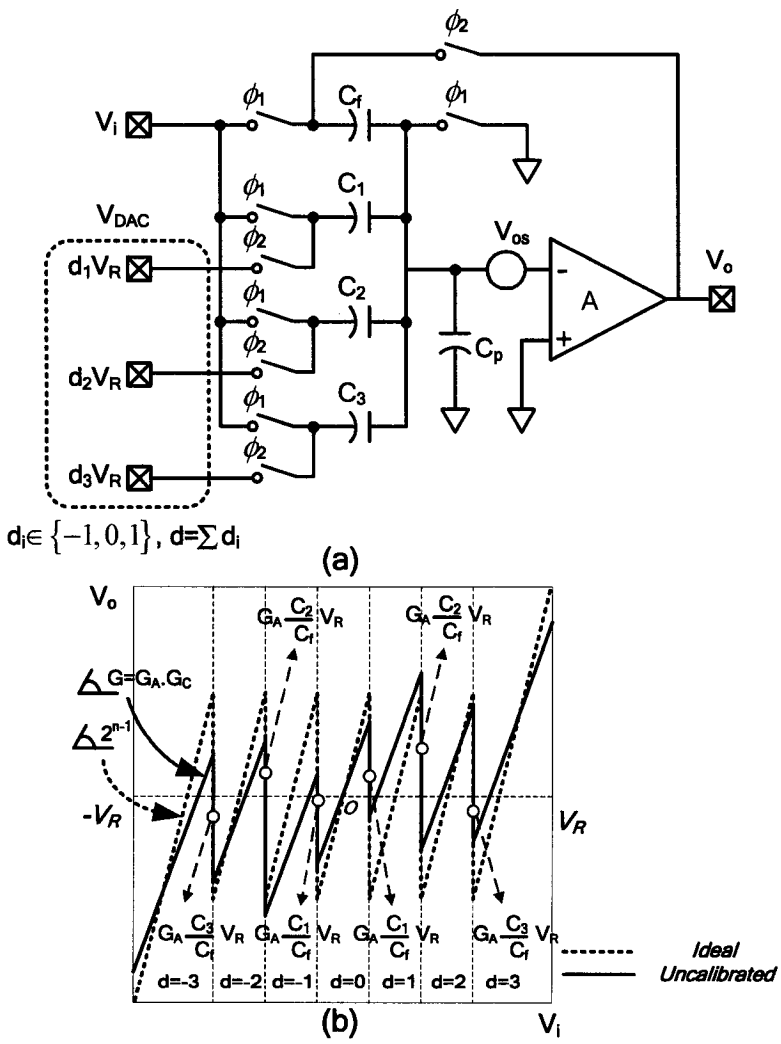


Figure 5.3: MDAC implementation for 2.5 bit/stage pipelined (a), and the residue plot of a realistic stage compared with an ideal one (b)

After the correction using (5.2) the backend, constituted now from the stage i and the following stage, is linear with a global gain $G_A \cdot G_{i-1}$. The offset $V_{off} = G_A \cdot ((C_T + C_p)/C_f) \cdot V_{os}$ is manifested, due to redundancy, as an overall input referred offset voltage and does not affect the ADC linearity. After stage i calibration, the stage $i-1$ can be calibrated using the linearized backend formed from stage i and the following stages.

B. Digital Background Calibration

In the proposed background calibration technique the term $G_A(C_i/C_f)V_R$ is measured for the different values of C_i to enable the correction using (5.2). A schematic of a 2.5-bit MDAC employing the proposed calibration is shown in Fig. 5.4.

The modification of this MDAC from the conventional one is the addition of an extra capacitor C_4 and some digital control circuits. Also the other modification is that the voltage $V_1 \cdot P_N$ is sampled onto the feedback capacitor C_f when ϕ_1 is high, where P_N is a pseudorandom signal alternating between 0 and 1. The capacitor C_4 is used instead of C_f to sample the input voltage when ϕ_1 is high.

By doing so, a voltage equal $G_A \cdot V_1$ is injected in the residue output. To not consume much from the non-overload range allocated for the SADC offset correction, V_1 should be small. For this reason, a voltage $V_2 \cdot P_N$ is sampled onto the capacitor C_4 in the next phase when ϕ_2 is high.

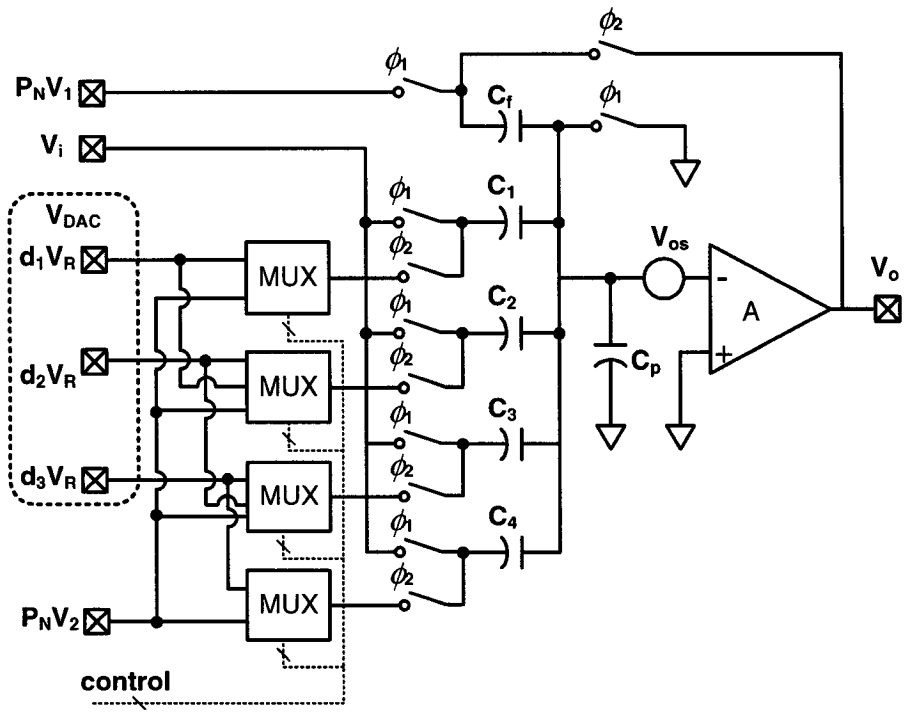


Figure 5.4: 2.5-bit MDAC employing the proposed calibration.

By injecting these voltages in this way, a subtractive calibration voltage (SCV) is injected and the output residue for the stage under-calibration is given by:

$$V_o = G_A \cdot \left(G_C \cdot V_i - \frac{d_1.C_1 + d_2.C_2 + d_3.C_3}{C_f} \cdot V_R \right.$$

$$\left. + P_N \cdot V_1 - P_N \cdot \frac{C_4}{C_f} \cdot V_2 + \frac{\sum_{i=1}^{4} C_i + C_f + C_p}{C_f} \cdot V_{os} \right)$$

$$= G_A \cdot \left(V_1 - V_2 \cdot \left(C_4 / C_f \right) \right) \cdot P_N + V_{o1} \qquad (5.3)$$

where $G_C = (C_1 + C_2 + C_3 + C_4)/C_f$ and V_{o1} is the remaining term in V_o that represents the residue without the injected voltages.

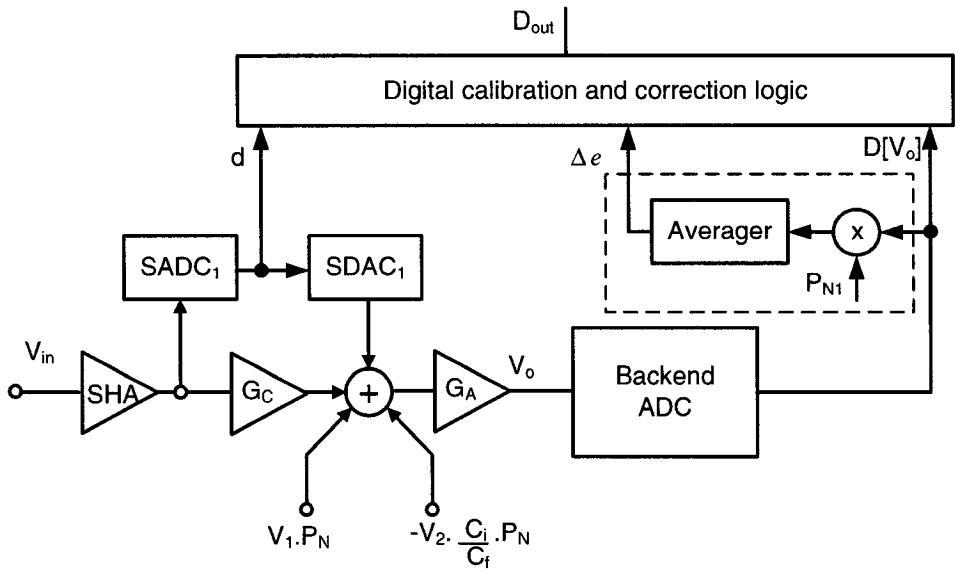


Figure 5.5: The SCV technique is applied to the first stage.

A simplified example wherein the SCV technique is applied to the first stage is shown in Fig. 5.5. By correlating the backend ADC digital output $D[V_o]$ with P_N the term $\Delta V = G_A \cdot (V_1 - (C_4/C_f)V_2)$ is extracted. P_{N1} is used for correlation instead of P_N, Where P_{N1} alternates between –1 and +1 instead of 0 and 1 in P_N. That substitution averages out the mean of the remaining term $D[V_{o1}]$ since P_{N1} has a mean value of 0. The output of the averager Δe is given by:

$$\Delta e = \frac{1}{N}\sum_{k=1}^{N}\left(D[V_o(k)]\cdot P_{N1}(k)\right)$$

$$= \frac{1}{N}\sum_{k=1}^{N}\left(D[\Delta V]\cdot P_N(k)\cdot P_{N1}(k)\right) + \frac{1}{N}\sum_{k=1}^{N}\left(D[V_{o1}(k)]\cdot P_{N1}(k)\right) \qquad (5.4)$$

The expected value of Δe is:

$$E[\Delta e]=\frac{D[\Delta V]}{N}\sum_{k=1}^{N}\left(E\left[P_N(k)\cdot P_{N1}(k)\right]\cdot\right)+\frac{1}{N}\sum_{k=1}^{N}E\left[D[V_{o1}(k)]\cdot P_{N1}(k)\right]$$

$$=\frac{1}{2}\cdot D[\Delta V] \tag{5.5}$$

since $D[V_{o1}]$ and P_{N1} are uncorrelated and $E\left[P_N(k)\cdot P_{N1}(k)\right]=\frac{1}{2}$.

The variance, $\sigma_{\Delta e}^2$, of Δe is:

$$\sigma_{\Delta e}^2=E\left[\Delta e^2\right]-E\left[\Delta e\right]^2=\frac{1}{N^2}\sum_{i=1}^{N}\left(E[D[V_{o1}(k)]^2]\cdot E[P_{N1}^2(k)]\right)$$

$$=\frac{1}{N}\cdot\sigma_{D[Vo1]}^2 \tag{5.6}$$

where $\sigma_{PN1}^2=E[P_{N1}^2(k)]=1$.

Now the term $G_A(C_4/C_f)V_R$ is found by injecting subtractive calibration voltages (SCV) and performing successive coefficient measurements (SCM) as will be explained. In the first coefficient measurement V_1 is set equal to $(K-1)V_R/K$ and V_2 equal to V_R, where K is even number. In that case a term g_1 is measured. In the second one V_1 is set to $(K-1)V_R/K$ and V_2 equal to $(K-2)V_R/K$ and that gives g_2. At the $K-1$ measurement V_1 is set to V_R/K and V_2 to $2\cdot V_R/K$ and that gives g_{K-1}. Finally V_1 is set to V_R/K and V_2 to ground and g_K is obtained. Using the following equations:

$$g_1=G_A\cdot(((K-1)\cdot V_R/K)-(C_4/C_f)\cdot V_R)$$

$$g_2=G_A\cdot(((K-1)\cdot V_R/K)-(C_4/C_f)\cdot((K-2)\cdot V_R/K)))$$

$$g_3=G_A\cdot((K-3)\cdot(V_R/K)-(C_4/C_f)\cdot((K-2)\cdot(V_R/K)))$$

....

$$g_{K-1} = G_A \cdot ((V_R / K) - (C_4 / C_f) \cdot (2 \cdot V_R / K))$$

$$g_K = G_A \cdot (V_R / K) \tag{5.7}$$

the term $G_A(C_4 / C_f)V_R$ is obtained by:

$$G_A(C_4 / C_f)V_R = -g_1 + g_2 - g_3 + g_4 - \cdots + g_{K-2} - g_{K-1} + g_K \tag{5.8}$$

The same procedure is repeated for every capacitor where the multiplexers in Fig. 5.4 select the capacitor corresponding to the term to be measured and reroute the digital control line for that capacitor to the substitute capacitor. For instance, when measuring the term $G_A(C_1 / C_f)V_R$, the capacitor C_1 is selected to sample $V_2 \cdot P_N$ and C_i ($i = 2, 3, 4$) are selected to samples $d_i \cdot V_R$ (i = 1, 2, 3) respectively during the phase ϕ_2 high. The multiplexers need only to switch between two capacitors, at any given time, independently from the number of the capacitors and consequently from the MDAC resolution. This minimizes the delay between the SADC and the SDAC compared to DNC, DFCA and SD-CGC methods where complex digital shufflers between the SADC and SDAC are needed that widen the gap between the sampling and holding phases subsequently limiting the ADC speed.

The reference voltages used in the SCM do not need to be accurate because there are eliminated from (5.8) and a simple string resistance can be used to generate the references. Fig. 5.6 suggests a circuit used to generate the voltages V_1 and V_2 using a simple switching matrix and a string resistance.

If K is chosen equal to eight, in every coefficient measurement a voltage around $V_R/8$ is injected in the second stage. Injecting such small voltage means that the non-

overload range equal $V_R/2 - V_R/8$ is left for the SADC correction. A more comparator offset relaxation can be obtained arbitrary by using more reference voltages and by performing more SCM.

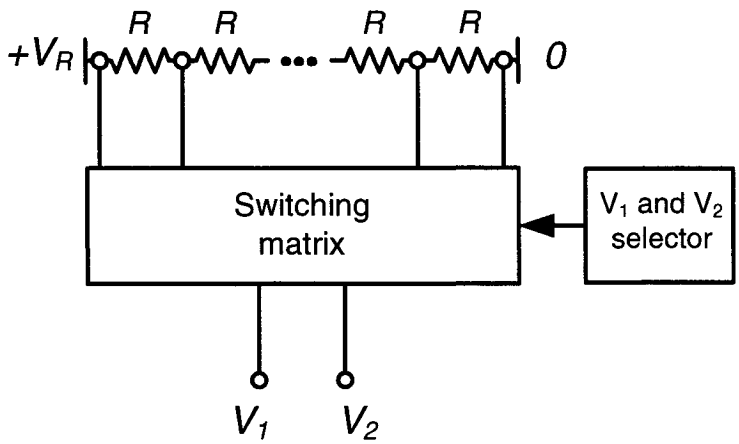


Figure 5.6: Switching matrix used to generate the voltages V_1 and V_2.

Finally, we mention that this technique does not need the injection of an accurate analog voltage or an increasing in the SDAC resolution. Also the injected voltage can be made arbitrary small that is not possible when splitting up the sampling capacitor used for the voltage injection. And finally, the added analog complexity is one capacitor independently from the MDAC resolution.

C. Global Gain Correction for Time-Interleaved ADC

Several calibration methods and the gain error in the front-end sample and hold (S/H) cause the slope of the overall ADC transfer characteristic to be not well controlled. The global gain error of the ADC does not affect its linearity but it is harmful for time interleaved ADCs (TIADC) that are inevitable when increasing the speed is desired with

high resolution ADCs to overcome the technology limits. With gain mismatch between the different channels, inband distortions are created and that degrades considerably the spurious free dynamic range (SFDR) and the signal-to-noise-and-distortion ratio (SNDR) performances of the TIADC [11]. This proposed technique could be modified to perform a global gain correction (GGC) for the ADC.

When a conventional charge redistribution S/H, shown in Fig. 5.7(a), is used in the front-end, the ADC output (V_{out}) will be given by:

$$\begin{aligned} V_{out} &= G_B \cdot V_o = G_B \cdot G_S \cdot V_i \\ &= G_B \cdot \frac{1}{1+\frac{1}{Af}} \cdot \left(\frac{C_1}{C_f}\right) \cdot V_i \end{aligned} \tag{5.9}$$

where G_B is the global gain of the calibrated ADC and G_S is the S/H gain due to capacitor mismatch and op-amp finite dc gain.

For calibration purpose the front-end S/H is changed as shown in Fig. 5.7(b) where there is no need for adding a capacitor to make the voltage subtraction. Instead the sign of the input signal V_i is monitored using a comparator and a voltage equal to V_R is injected without affecting the dynamic range of the S/H as shown in Fig. 5.8(a) Here, V_1 is chosen to be equal to ground and $V_2 = sign(V_i) \cdot V_R$ where $sign(V_i) = 1$ when V_i is positive and $sign(V_i) = -1$ when V_i is negative. In this case the ADC output will be given by:

$$V_{out} = G_B \cdot G_S \cdot \left(V_i - PN \cdot sign\left(V_i\right) \cdot V_R\right) \tag{5.10}$$

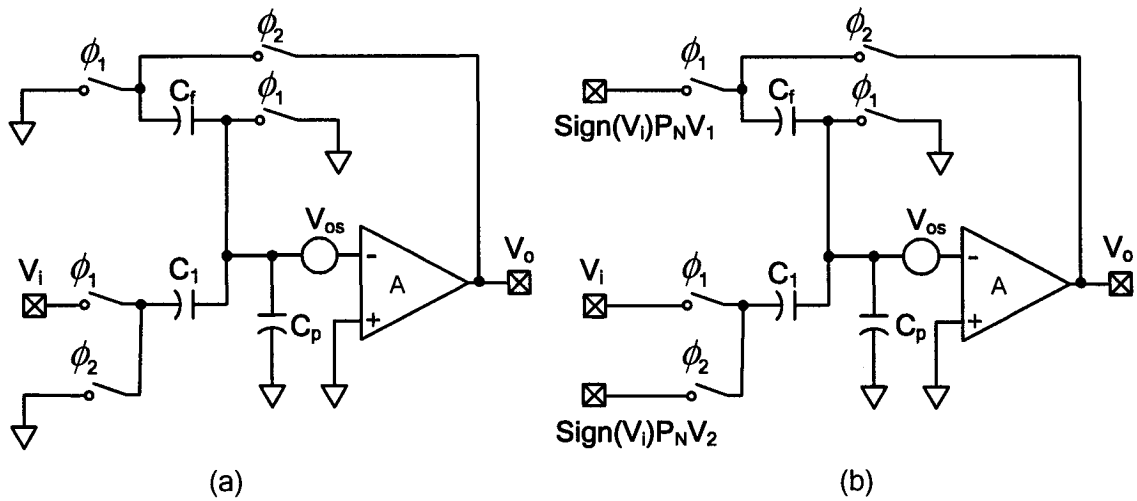


Figure 5.7: Conventional (a), and modified (b) S/H.

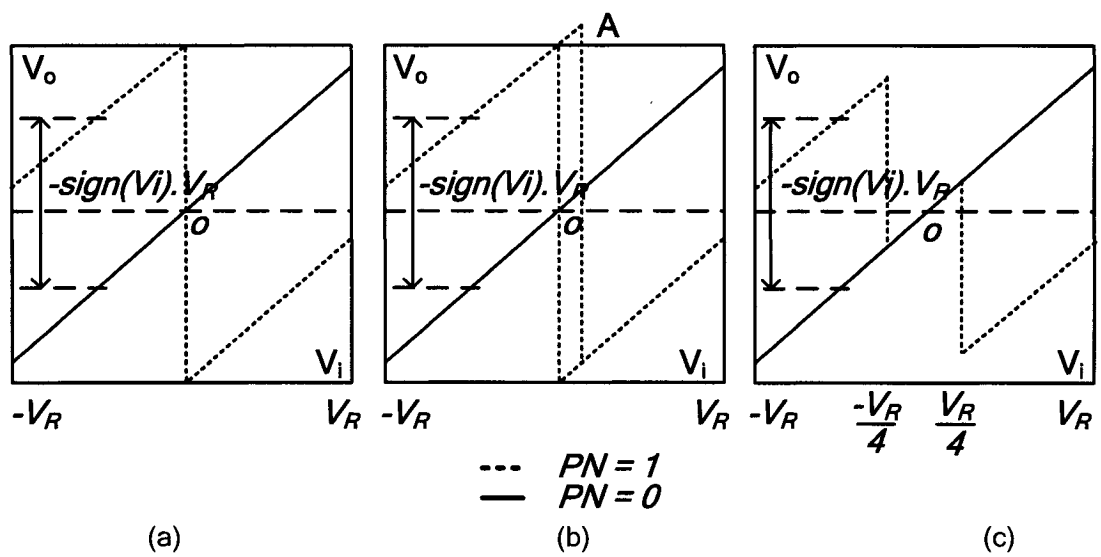


Figure 5.8: S/H transfer functions: with one comparator (a), with overload error (b) and when two comparators are used (c).

Using one comparator to compare V_i with the ground to find $sign(V_i)$ may lead to distortion in the S/H transfer function when the comparator is not accurate as the case shown in Fig. 5.8(b) at point A where the S/H output V_o exceeds the reference voltage V_R.

Therefore, instead of using an accurate comparator, two imprecise comparators are used. One comparator compares V_i with $-V_R/4$ and the other with $V_R/4$. Thus, the voltage V_2 is chosen equal to $sign(V_i)\cdot V_R$ when $V_i \geq V_R/4$ or $V_i \leq -V_R/4$. Otherwise V_2 is chosen equal 0 by forcing PN to be 0 (Fig. 5.8(c)). In this case, an offset in every comparator as large as $V_R/4$ is tolerated without overloading the S/H output.

The digitized value of V_{out} is correlated with $PN\cdot sign(V_i)$ in the background to extract the gain $G_S\cdot G_B$. A multiplication by $1/(G_S\cdot G_B)$ for the ADC output will compensate for the ADC global gain error.

D. Calibration Duration Shortening

The term $(1/2)\cdot D[\Delta V]$ extracted in (5.5) is not constant in steady state. Instead, it contains a random fluctuation stemmed from the variance of $D[V_{o1}]$ divide by N as seen in (5.6). However, (5.6) can be made arbitrarily small by increasing the number of samples N at the input of the averager in Fig. 5.5. Increasing N means increasing the required calibration time. Also we notice that (5.6) can be minimized by subtracting V_{o1} from (5.3) before the correlation. In [12] an ADC is connected in parallel with an algorithmic ADC to measure the input signal so as to be subtracted later in order to accelerate the calibration. Knowing that a multi-bit/stage pipelined ADC usually has front-end stages resolving several bits (e.g. 2.5 or 3.5b/stage) and a backend constituted from 1.5b/stages as shown in Fig. 5.9, here we propose a simple solution to accelerate the calibration by using the backend ADC and the SADC for the stages under-calibration to estimate the value of V_{o1} during the normal operation of the ADC. Knowing that the backend ADC is

configured as 1.5b/stage with relaxed accuracy, so this backend could be run at double speed without the need for large additional overhead.

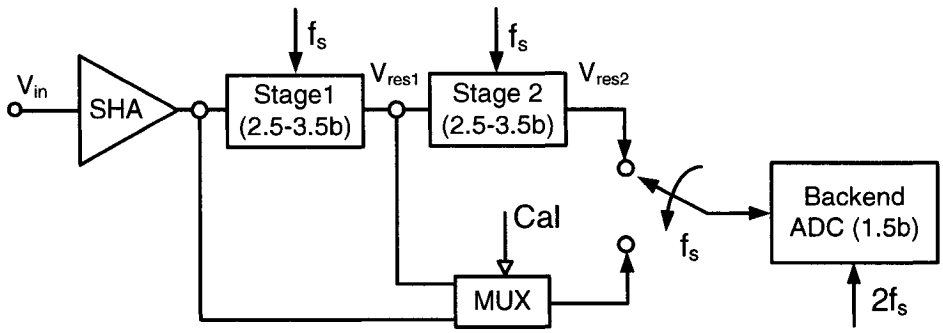


Figure 5.9: Using the 1.5b/stage backend ADC to shorten the calibration cycles.

When the stage 2 is under-calibration, in one cycle the backend ADC is connected at the input of this stage (Cal =1) to estimate the input signal V_{res1}. In the next period, this backend is performing its normal operation for the whole ADC. V_{res1} is sampled at f_s while the backend is operating at $2f_s$ that means that this voltage is constant during the 2 operations.

The value obtained by the backend ADC during the normal operation of the ADC can be simplified by:

$$V_{res2} = G_2 \cdot (V_{res1} - V_{DAC2}) + \Delta V \cdot PN \tag{5.11}$$

If we subtract from $G_2 \cdot V_{res1}$ the value estimated by the backend ($V_{res1,est}$) multiplied by 2^2 and by adding the output of the SADC ($V_{DAC2,est}$), obtained during the normal operation, multiplied by 2^2 instead of $G_2 \cdot V_{DAC2}$ (5.11) becomes:

$$V_{res2,new} = (G_2 \cdot V_{res1} - 2^2 \cdot V_{res1,est}) - (G_2 \cdot V_{DAC2} + 2^2 \cdot V_{DAC2,est}) + \Delta V \cdot PN \tag{5.12}$$

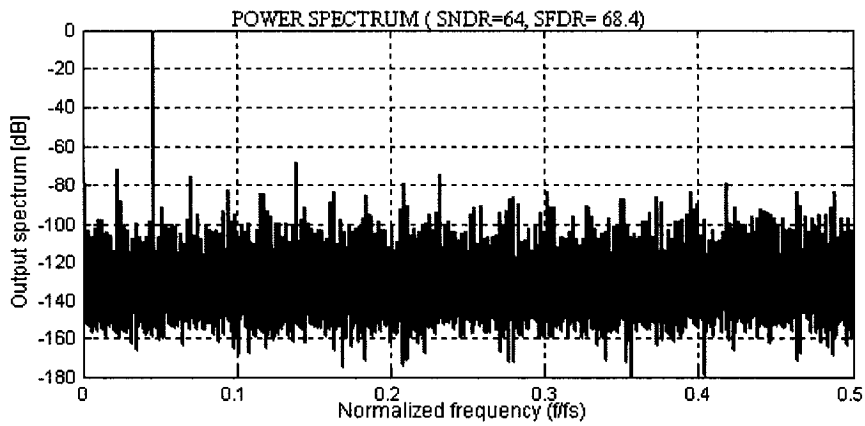
For capacitor mismatch of ±0.2% and op-amp dc gain of 60dB we find that $G_2 \cong 2^2 \cdot (1+\varepsilon \cdot 2^{-7})$, where $\varepsilon \in [-1,+1]$. A simple developing for (5.12) shows that the variance of Δe can be approximated now by: $\sigma^2_{\Delta e} \cong (2^{-10}/N) \cdot \sigma^2_{D[Vo1]}$.

Thus, the number of samples needed without these signals subtraction is divided by 2^{10}. That shortens the calibration cycle by one thousand times compared to (5.6) to obtain the same resolution. The 1.5b/stage backend ADC can also be used to accelerate the calibration of stage 1 when the control signal Cal, in Fig. 5.9, is selected equal to 0.

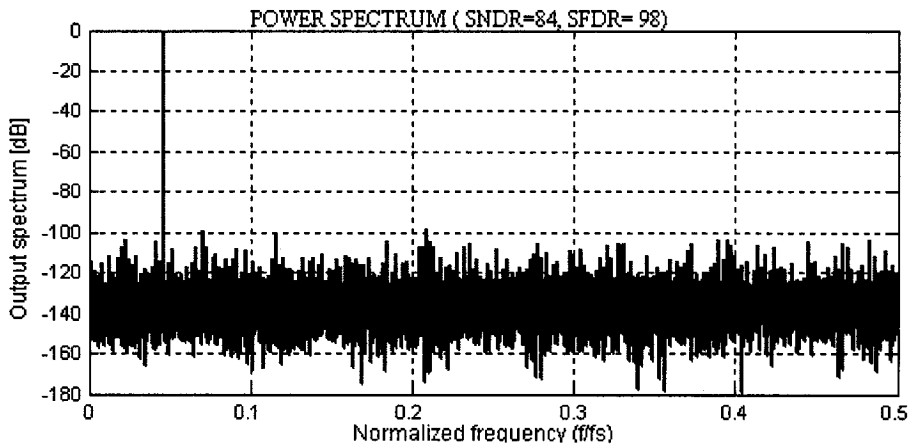
III. Simulation Results

Simulations have been performed to verify the effectiveness of the proposed calibration technique on a 14-bit pipelined ADC. This ADC has two 2.5-bit front-end stages and a backend part of nine 1.5-bit stages. Capacitor mismatch of ±0.2%, comparator offsets of ± V_R/12, and opamp dc gain of 60 dB were used in all the stages. The reference voltages for the SADCs and the calibration voltage circuits were generated by simulated string resistances wherein each resistance was chosen with a random error of ±0.2% standard deviation. Only the two front-end stages were calibrated. Without shortening the calibration cycles, a number of samples around 2^{32} were needed for K equal eight. When shortening the calibration is used, the number of the need samples is dropped to around 2^{22} as expected from the calculations in Section II-D.

A sinewave slightly lower that the full-scale signal around 1/20 the sampling frequency (f_s) was applied to the input of the 14-bit ADC before and after calibration using the proposed technique with calibration duration shortening. Fig. 5.10(a) shows the power spectrum of the digital output without calibration.



(a)



(b)

Figure 5.10: Spectrum of the output of a 14-bit pipelined ADC without (a) and with the proposed calibration technique (b).

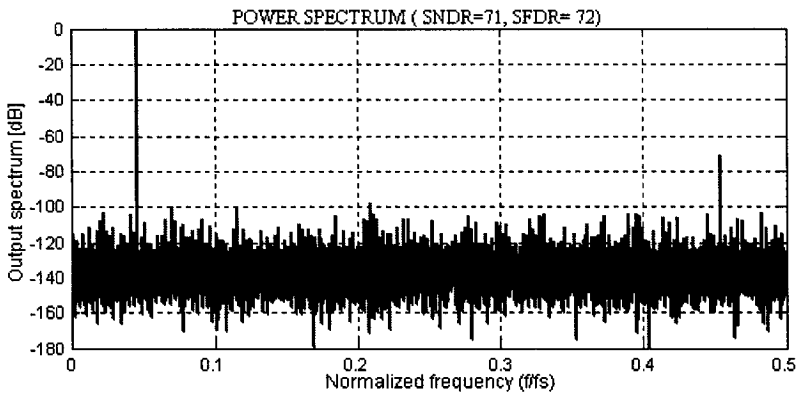
The SNDR is 64 dB resulting an effective number of bits (ENOB) of 10.3 bits, and the SFDR is 68.4 dB. The power spectrum density of the digital output after calibration is shown in Fig. 5.10(b) The SNDR becomes 84 dB resulting in an ENOB of 13.7 bits, and the SFDR is increased to 98 dB.

A two-channel TIADC is simulated before and after GGC. The two channels have the same configuration and resolution as the one used in the previous simulation and they are already calibrated by the proposed technique. The effects of the skew and offset mismatches between these channels are neglected in order to examine the improvement due to the gain mismatch correction alone. Before GGC the SNDR is 71 dB resulting in an effective number of bits ENOB of 11.5 bits, and the SFDR is 74 dB (Fig. 5.11(a)). The SNDR after GGC becomes 82 dB resulting in an ENOB of 13.3 bits, and the SFDR is increased to 91 dB as shown in Fig. 5.11(b).

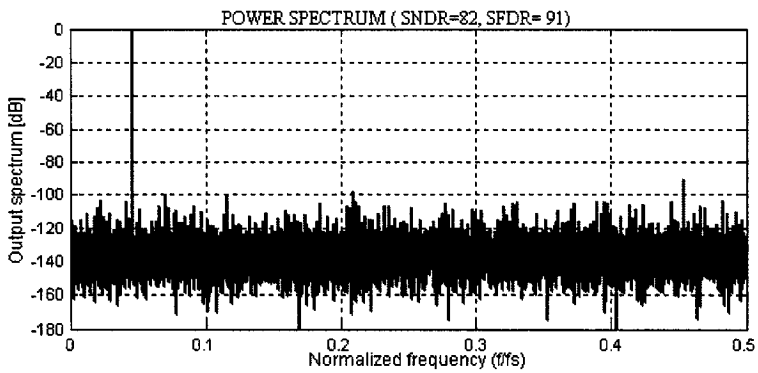
IV. Conclusion

In this paper, a digital background calibration technique to compensate for the nonlinearity and interstage gain error of the internal SDACs due to capacitor mismatch and the op-amp finite dc gain in multi- bit/stage switched-capacitor pipelined ADC is presented. Global gain correction essential for TIADC is also presented. Technique to shorten the calibration duration is proposed.

These calibration techniques have a minimal impact on analog complexity, while digital complexity is increased, but this is the preferred tradeoff in deep submicron technologies and will moderately impact the overall die area. Simulation results show the effectiveness of these techniques.



(a)



(b)

Figure 5.11: Spectrum of the output of a 14-bit pipelined ADC without (a) and with the proposed calibration technique (b).

ACKNOWLEDGEMENTS

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REFERENCES

[1] D. Cline and P. Gray, "A power optimized 13-b 5 Msamples/s pipelined analog to-digital converter in 1.2 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 31, pp. 294–303, Mar. 1996.

[2] L. Sumanen, M. Waltari, T. Karhonen and K. Halonen, " A digital self-calibration method for pipeline A/D converters," in *Proc. IEEE Int. Symp. Circuits Systems*, vol. 2, pp. 792 -795, May 2002.

[3] I. Galton, "Digital cancelation of D/A converter noise in pipelined A/D converters," *IEEE Trans. Circuits Syst. II*, vol. 47, pp. 185–196, Mar. 2000.

[4] C. Giovanni and P. Andrea "Method of correction of the error introduced by a multibit DAC incorporated in an ADC," *US patent* 6,867,718, Mar. 2005.

[5] T. Shu, B. Song, and K. Bacrania, "A 13-b, 10-Msample/s ADC digitally calibrated with oversampling delta–sigma converter," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1866–1875, Dec. 1997.

[6] M. Kinyua, F. Maloberti, and W. Gosney, "Digital background auto-calibration of DAC non-linearity in pipelined ADCs," in *Proc. IEEE Int. Symp. Circuits Systems*, vol. 1, pp. 23 -26, May 2004.

[7] E. Siragusa and I. Galton, "Gain error correction technique for pipelined analog-to-digital converters," *Electron. Lett.*, vol. 36, pp. 617–618, 2000.

[8] P. Yu et al., "A 14 b 40 MSample/s pipelined ADC with DFCA," *ISSCC Dig. Tech. Papers*, pp. 136–137, Feb. 2001.

[9] K. Nair and R. Harjani, "A 96dB SFDR 50MS/s digitally enhanced CMOS pipelined A/D converter," *ISSCC Dig. Tech. Papers*, pp. 456–457, Feb. 2004.

[10] E. Siragusa and I. Galton, "A digitally enhanced 1.8V 15b 50MS/s CMOS pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 39, pp. 2126–2138, Dec. 2004.

[11] C. Vogel, "The impact of combined channel mismatch effects in time-interleaved ADCs," *IEEE Trans. Instrumentation and Measurement*, vol. 54, pp. 415–427, Feb. 2005.

[12] J. Li, G.-C Ahn, D.-Y Chang and U.-K Moon, "A 0.9-V 12-mW 5-MSPS Algorithmic ADC With 77-dB SFDR," *IEEE J. Solid-State Circuits*, vol. 40, pp. 960–969, Apr. 2005.

Chapter 6

RESULTS AND DISCUSION

6.1 Introduction

Two-channel, 10-bit, 100-MS/s, time-interleaved pipelined ADC designed and fabricated in 0.18 μm CMOS technology is presented in this chapter. The block diagram of the proposed two-channel ADC is shown in Fig. 6.1. Every channel has a front-end wide input bandwidth sample-and-hold (S/H) and it was implemented with nine cascaded 1.5-bit/stages architecture. Each stage is composed of one 1.5b/stage MDAC and one fully-differential 1.5 bits SADC.

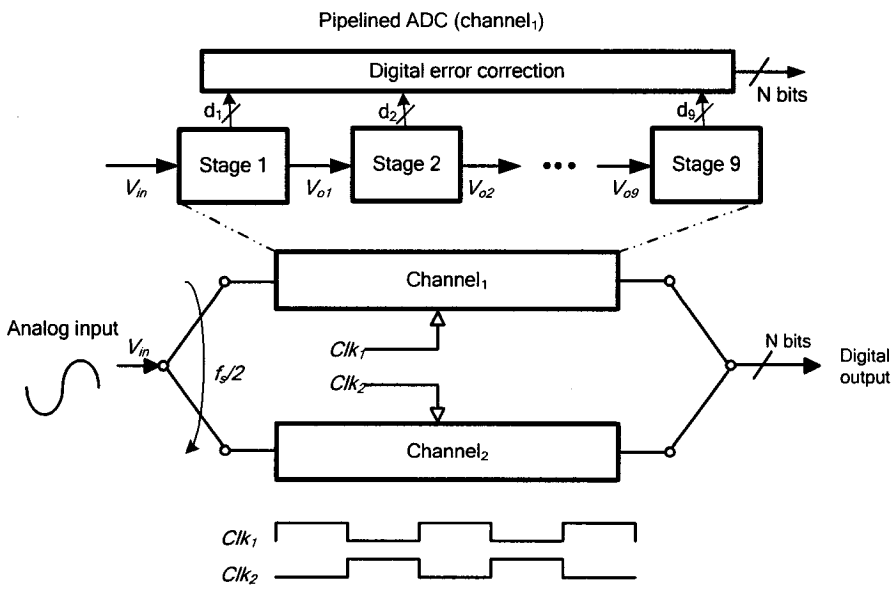


Figure 6.1: The block diagram of the proposed two-channel ADC.

6.2 Two-Channel Time Interleaved ADC

6.2.1 Front-end Sample and Holds

The implemented front-end S/H circuits based on modified charge redistribution architecture are shown in Fig. 6.2(a). The modification to these S/Hs is done through connecting the sampling capacitors C_{si} (i =1, 2, 3 or 4) to a voltage V_1 instead of ground during the hold phase (e.g. for the upper channel when Ph_{2B} is high). When conventional charge redistribution S/H is used, ADC_1 output for $channel_1$ (V_{out1}) will be given by:

$$\begin{aligned} V_{out1} &= G_{B1} \cdot V_{S1} = G_{B1} \cdot G_{S1} \cdot V_i \\ &= G_{B1} \cdot 1/\left(1+1/Af\right) \cdot \left(C_s/C_f\right) \cdot V_i \end{aligned} \tag{6.1}$$

where G_{B1} is the global gain of ADC_1 and G_{S1} is the S/H gain due to capacitor mismatch and opamp finite dc gain. For gain calibration purpose, as explained in section 5.2, the sign of the input signal V_i is monitored using two comparators and a voltage equal to V_R, the reference voltage, is injected without affecting the dynamic range of the S/H_1 as shown in Fig. 5.8(c). Thus, the voltage V_1 is chosen equal to $sign(V_i).V_R$ when $V_i \geq V_R/4$ or $V_i \leq -V_R/4$. Otherwise, V_1 is chosen equal 0 by forcing P_N to be 0 (Fig. 5.8(c)).

In this case, $channel_1$ output will be given by:

$$V_{out1} = G_{B1} \cdot G_{S1} \cdot \left(V_i - P_N \cdot sign\left(V_i\right) \cdot V_R\right) \tag{6.2}$$

The digitized value of V_{out1} is correlated with $P_N.sign(V_i)$ in the background to extract the gain $G_{B1}G_{S1}$.

Similarly the gain $G_{B2}G_{S2}$ is extracted for ADC_2 in $channel_2$. Multiplications by $1/(G_{B1}G_{S1})$ and $1/(G_{B2}G_{S2})$ for ADC_1 and ADC_2 outputs will compensate for the static

gain mismatch between the two channels. This gain mismatch calibration features fast convergence due to the injection of full scale calibration voltage, V_R, without affecting the input range of the ADC.

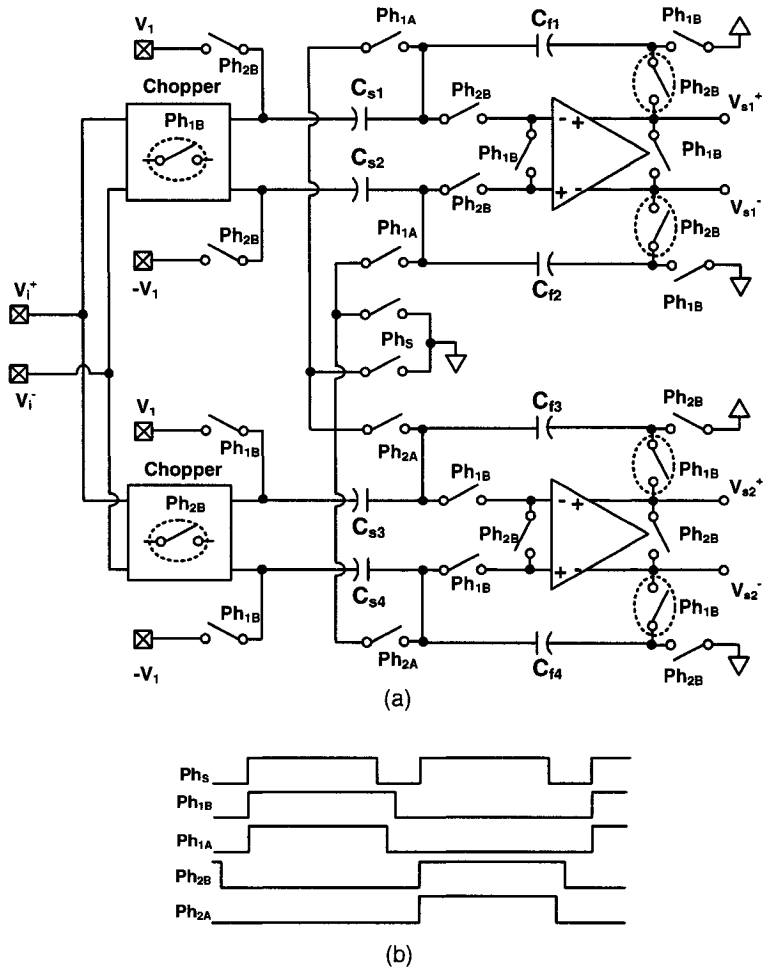


Figure 6.2: Front-end S/H Circuits' implementation: (a) and their signals timing (b).

Moreover, these S/Hs perform timing skew insensitive input sampling due to the series full speed sampling switch clocked by Ph_s as shown in Fig. 6.2. The offsets between the two ADC channels, referred to the S/Hs inputs, are calibrated for by using input choppers and correlators in the background [EKL00]. In these choppers,

bootstrapped sampling switches similar to the one proposed in [DES99] are used to allow wide bandwidth input signal. In this design, the NMOS sampling switch is implemented in deep N-well to enable the connection of its bulk to the input node during the sampling phase to reduce its on-resistance and nonlinear junction capacitances variations.

6.2.2 Pipelined ADC Stages Implementation

Fig. 6.3 shows the multiplying digital-to-analog converters (MDACs) of stages 1 and 2 for ADC_1 where opamp sharing is used to reduce power consumption. While static gain mismatch can be calibrated by the technique described in Section 6.2.1, settling mismatch between the two inputs S/Hs will create dynamic gain mismatch [LEE05]. This due to the fact that stage 1 of ADC_1 samples S/H_1 output at Ph_{2A} while stage 1 of ADC_2 samples S/H_2 output at Ph_{1A}. With this sampling scheme, any incomplete linear settling between the S/Hs circuits will introduce gain mismatch errors. This gain mismatch is dynamic and will be more pronounced for higher input and clock frequencies when the S/Hs outputs will not be considered as dc signals.

To reduce the dynamic gain mismatch in this prototype, the same sampling skew insensitive scheme used for the input S/Hs, is used to define the sampling instances for stage 1 in ADC_1 and ADC_2 by adding the series switch S_1 clocked by the full speed clock Ph_S (Fig. 6.3). By doing so, any incomplete linear settling in the S/Hs outputs will change to common gain mismatch for $channel_1$ and $channel_2$ and will be corrected using the same calibration coefficients of static gain mismatch.

The opamp sharing technique used to reduce the power consumption has some drawbacks. The additional switches to perform the sharing introduce series resistances and that mandates the use of larger switches to reduce their on-resistances.

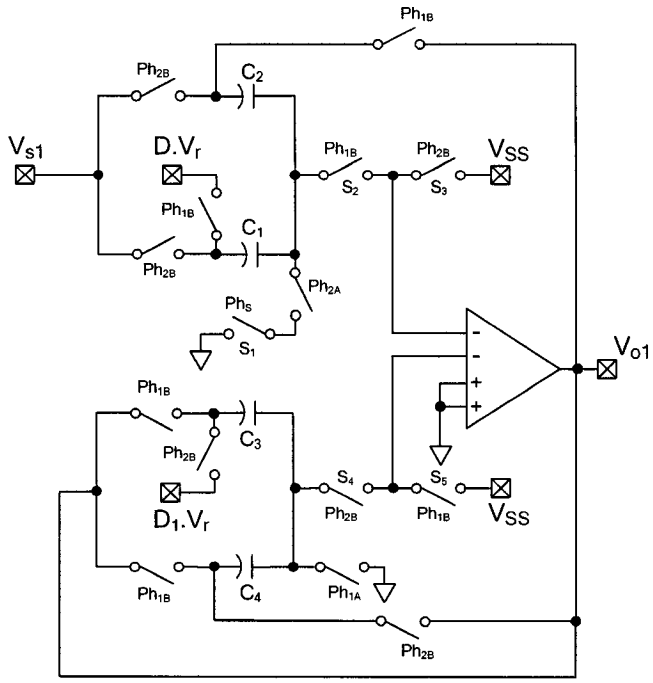


Figure 6.3: The MDACs of stages 1 and 2 of ADC_1.

Using larger switch at the opamp input creates offset voltage, caused by charge injection, that will be referred to the S/Hs inputs by redundancy and removed by offset calibration. Also, the usage of larger transistor causes additional capacitance at the input of the opamp. Without special technique this extra capacitor in addition to the opamp input capacitance will never be reset between samples and that will be a source of nonlinearity especially for the residue output of stage 1 that will be affected by the residue output of stage 2 [NAG97]. To reduce the ADC nonlinearity, we use a four inputs opamp, shown in Fig. 6.4, while every MDAC will have dedicated inputs. A similar

technique was used in [BEC03] while two inputs of the opamp are reset to the input common mode (ICM) voltage and the other two inputs are used to amplify the signal. Resetting the unused inputs to the ICM means that only half of the current flows into the input transistors that are used at a given time for amplification. As a result, the unity gain frequency of the opamp is reduced by 30% and its dc gain by 3dB for a given biasing current (g_m of the input transistor is divided by $\sqrt{2}$). To avoid this drawback in this prototype, the inputs transistors during the reset phase are turned off by applying V_{SS} to their gates. Thus, all the current will flow into the inputs transistors that amplify the signal. By referring to Fig. 6.3, Ph_{1B} is used to switch the opamp from stage 2 to stage 1. Despite turning off one set of the input transistors, there is no speed reduction due to the fact that the same clock is used to switch the two sets of input transistors between the input CM voltage and V_{SS}.

A worst case simulated current switching time between the input transistors at 50MHz was 200psec. Moreover, to avoid any potential turn-off or slow recovery for the opamp during the current switching, the clock driving the switch S_5 is locally delayed compared to the one driving S_2 to assure that the current transition between the input transistors happens while all the opamp other transistors are in the saturation region.

The performance of the implemented four-input two-stage Miller-compensated fully differential opamp is 78dB of dc gain and 400 MHz of unity gain frequency. A common mode feedback, with duplicate sampling capacitor C_C, has been used for each stage (Fig.6.4(b)). This scheme continuously refreshes C_{CM} during both clock phases to improve common-mode stability with opamp sharing technique.

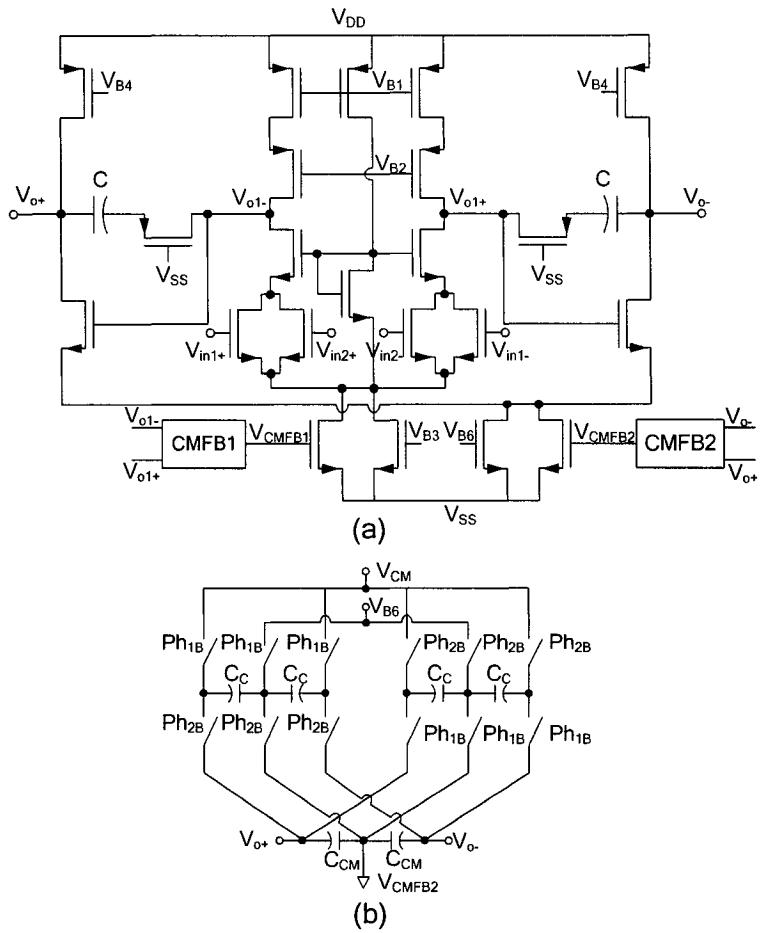


Figure 6.4: Opamp schematic (a) and the common-mode feedback circuit (b).

The schematic of the comparator, used for the gain mismatch calibration and in stages 1 to 3 in the pipelined ADC, is shown in Fig. 6.5. Preamps are used to combat the coupling of kickback noise from the latch comparators into the ADC analog input and the MDAC residue paths. These preamps are shared between stages to reduce the power consumption as shown in Fig. 6.5. The measured offset of this comparator is around 35 mV at sampling frequency of 100 MHz. Also, a 10mV offset mismatch is measured between two comparators distanced on-chip by 1.5mm.

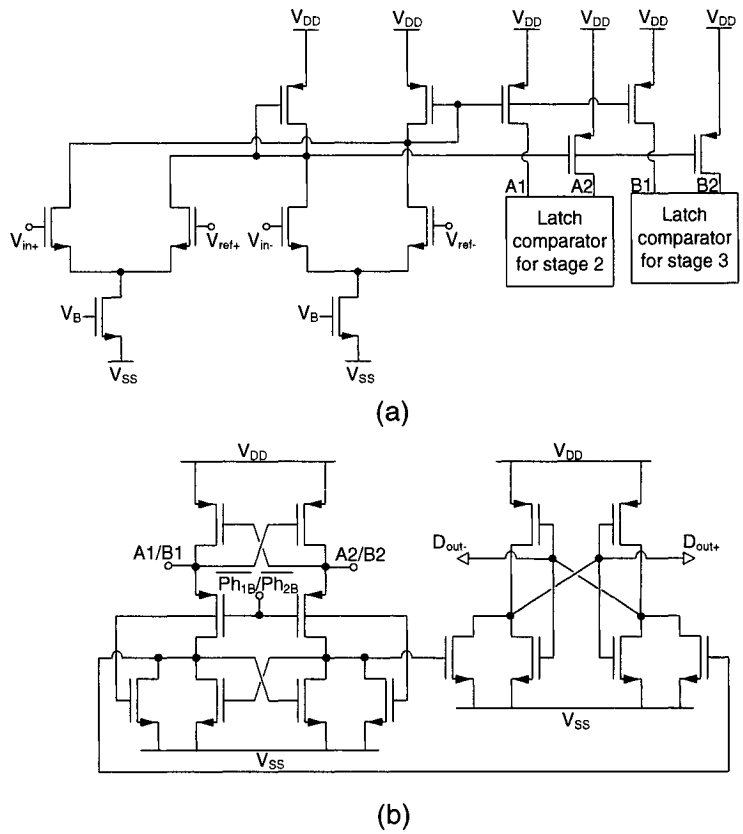


Figure 6.5: Current-mirrored fully differential preamp (a) and latch stage (b).

6.3 Experimental Results and Discussions

The converter is fabricated with TSMC 0.18μm 1P6M mixed signal CMOS process with MiM capacitors. Fig. 6.6 shows the die photomicrograph, with a total die area of 3.6 mm^2. The chip is bonded to a 120-pin CQFP package and placed on the Printed Circuit Board (PCB) using an appropriate socket. Fig. 6.7 shows the PCB from the top side. The input signal and the clock are connected to the test board through SMA (SubMiniature version A) connectors. The digital output of each channel was sampled separately by the logic analyzer and the gain and offset calibrations were performed off-chip.

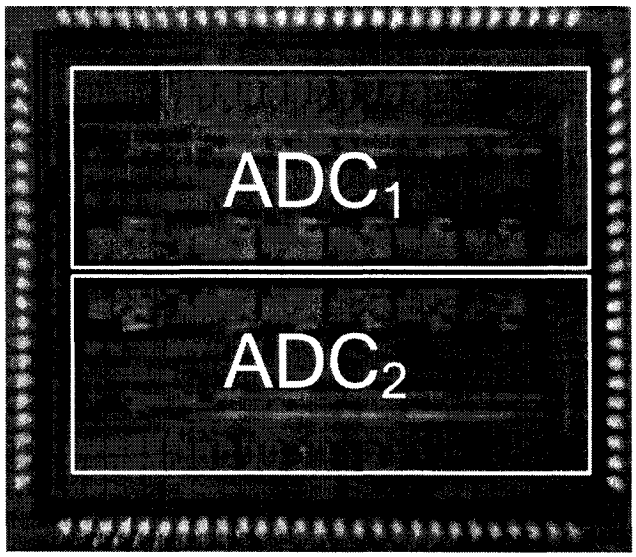


Figure 6.6: Die photograph of the prototype ADC.

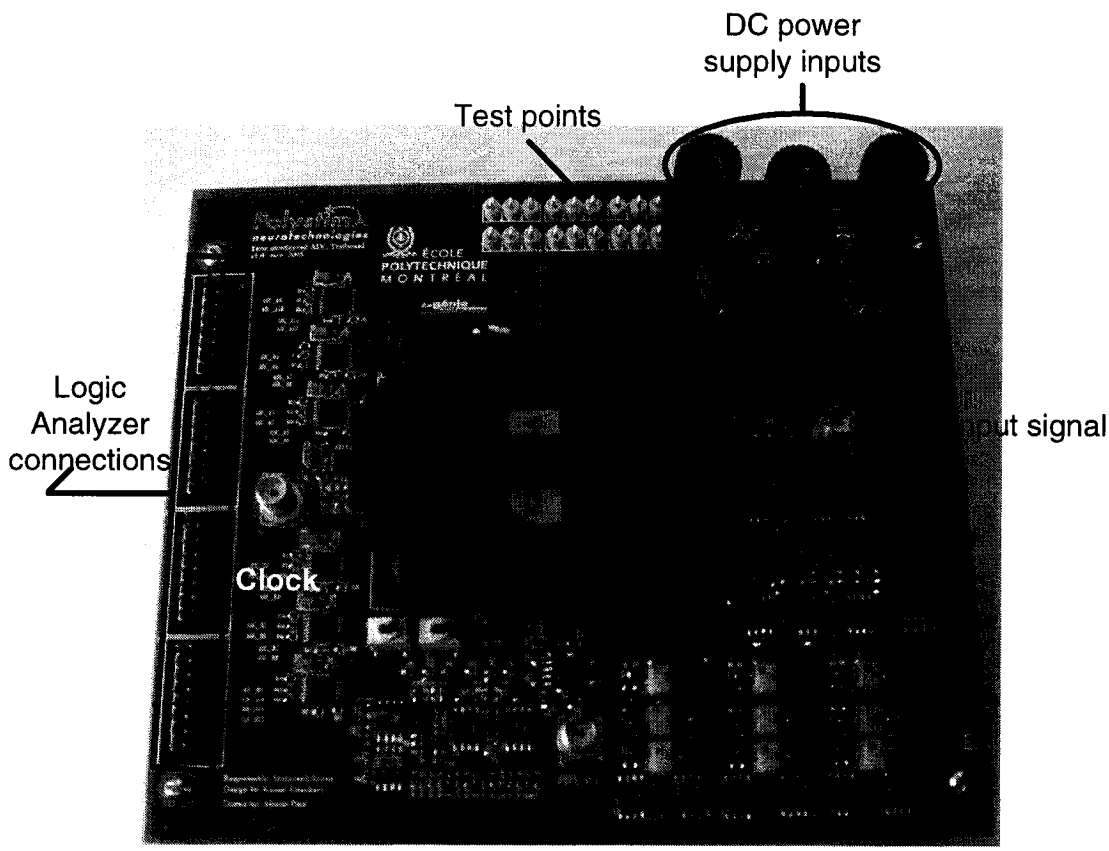


Figure 6.7: Top side photo of the PCB

Figs. 6.8 and 6.9 show the reconstructed input signals when a ramp and a square wave with 10 KHz frequencies were sampled respectively by the ADC at 100MHz. Figs. 6.10 and 6.11 shows the reconstructed digital output for a 1 MHz and 99 MHz full scale sinusoidal inputs sampled by the ADC at 100MHz respectively. We see from Fig. 6.11 that the input signal at 99 MHz is subsampled to generate a 1 MHz sine wave.

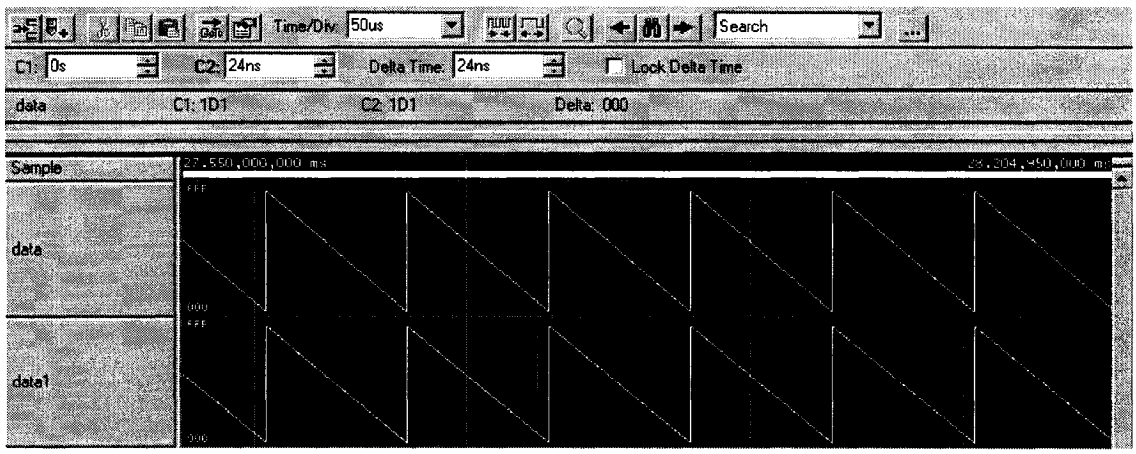


Figure 6.8: Logic analyzer output for 10 KHz ramp input.

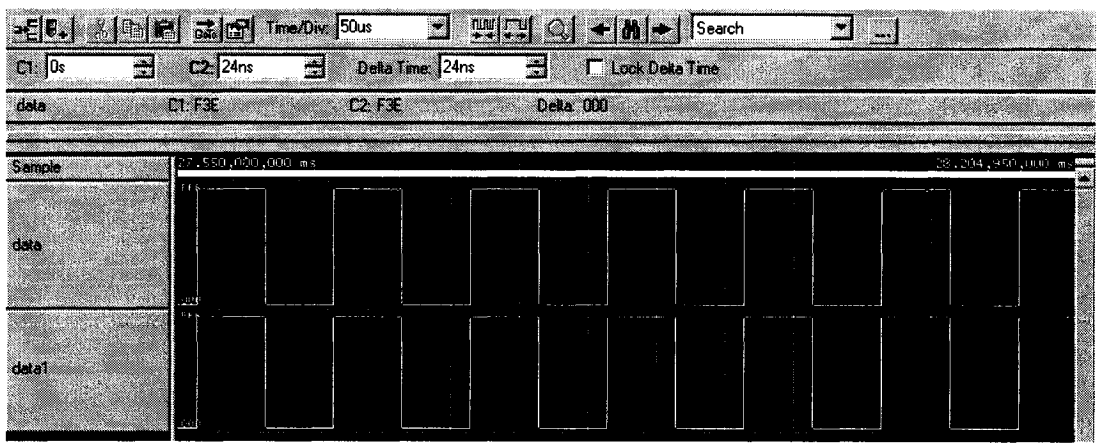


Figure 6.9: Logic analyzer output for 10 KHz square input.

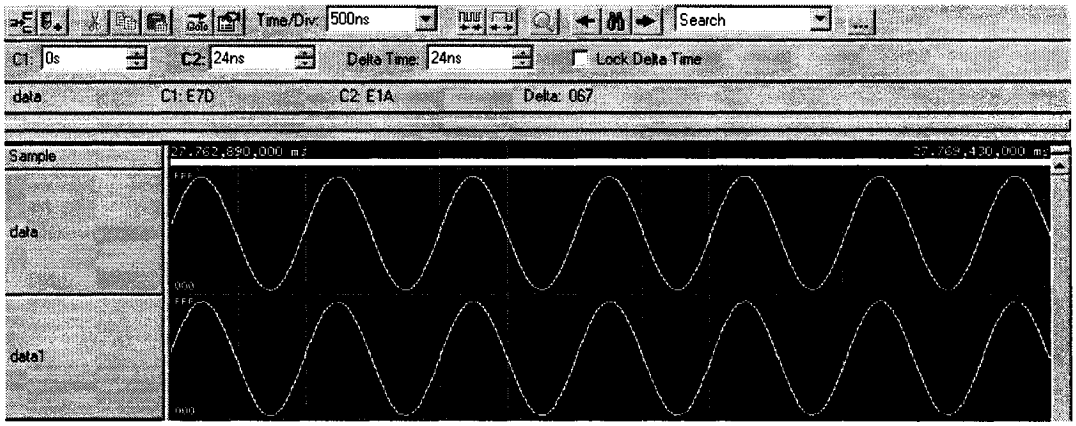


Figure 6.10: Logic analyzer output for 1 MHz sinusoidal input.

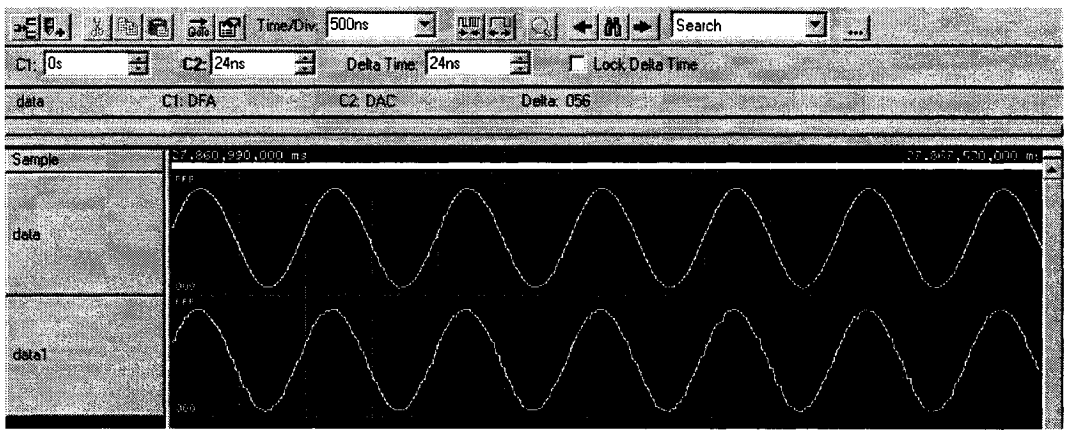
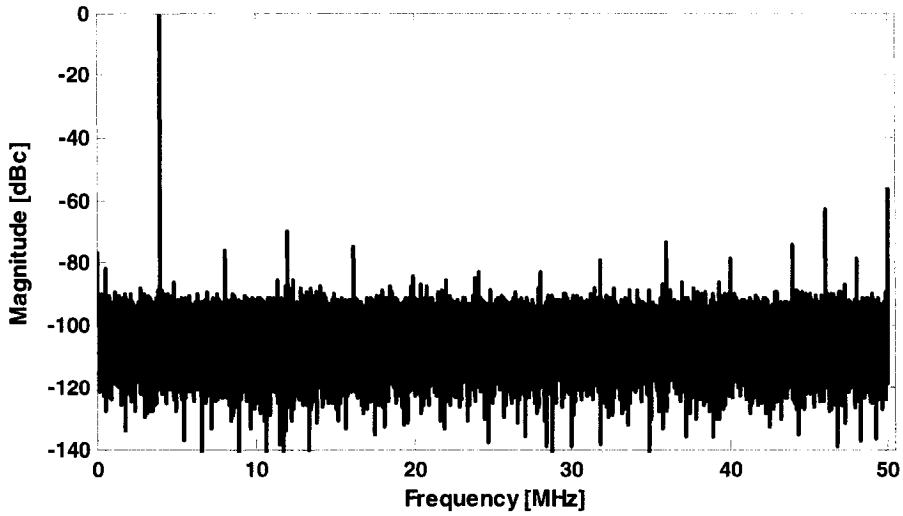


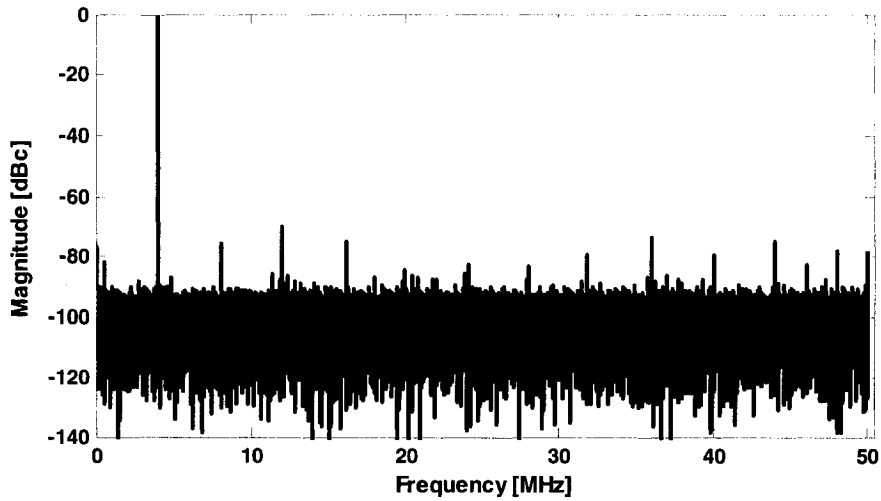
Figure 6.11: Logic analyzer output for 99 MHz sinusoidal input.

Fig. 6.12 shows the ADC output spectrum with and without calibration. The input is a fully-differential $1.6V_{pp}$ sinusoidal signal at input frequency (f_{in}) of 3.99 MHz where the sampling frequency (f_s) is 100 MS/s. Before calibration, the measured SNDR and SFDR were 48dB and 57dB respectively.

The performance is limited by offset mismatch tone of -57dBc at $f_s/2$ and gain mismatch tone of -61 dBc at $f_s/2$-f_{in}. After calibration, the SNDR and SFDR were improved to 57dB and 69dB respectively.



(a)



(b)

Figure 6.12: ADC output spectrum: (a) without calibration, and (b) with calibration.

(f_s = 100 MS/s, V_{in} = 1.6Vpp , and f_{in} = 3.99 MHz).

Fig. 6.13 plots the SNDR and SFDR for the calibrated ADC as function of the signal power, for an input sinusoidal at 3.99 MHz with sampling frequency of 100MS/s. The chip total power consumption is 76 mW at 1.8-V supply and 100 MHz sampling frequency. Table 6.1 summarizes the measured performances. The obtained performance

of the proposed ADC is comparable with state-of-the-art 10-b, 100MS/s ADCs as shown in Table 6.2.

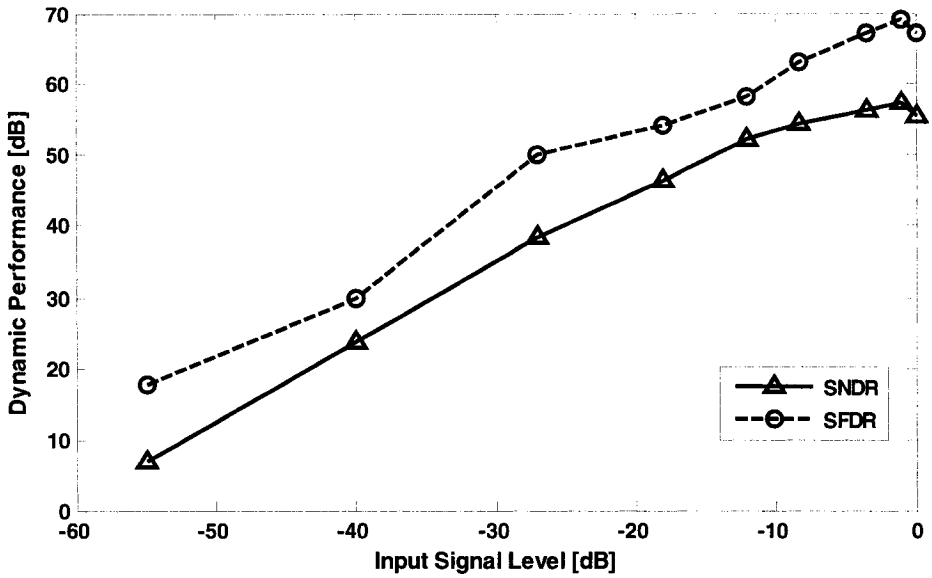


Figure 6.13: Measured dynamic performance versus input signal level.

Table 6.1: Performance summary

Resolution	10-bit
Sampling rate	100 MS/s
Technology	0.18μm CMOS
Active area	3.6 mm^2
SNDR / SFDR	57dB / 69dB
INL/DNL	1.8LSB / 0.75LSB
Input range	1.6 Vpp
Supply voltage	1.8 V
Power	76 mW

Table 6.2: Performance comparison with state-of-the-art 10-b, 100MS/s ADCs

REF	SNDR [dB]	SFDR [dB]	Process CMOS	Supply [V]	Power [mW]
This work	57	69	0.18μm	1.8	76
[AND05]	56.5	69.1	0.18μm	1.8	94
[LI04]	54	65	0.18μm	1.8	67
[JAM02]	56.8	70.2	0.35μm	3.3	234
[YOO02]	54	68	0.25μm	2.5	208
[NAI00]	58	66	0.35μm	3	105

6.4 Conclusion

Two-channel 10-bit, 100-MS/s time-interleaved pipelined ADC has been designed and fabricated with TSMC 0.18μm 1P6M mixed signal CMOS process with MiM capacitors. This ADC achieves peak SNDR and SFDR of 57 dB and 69 dB, consumes 76 mW and occupies 3.6 mm^2. The front-end S/Hs circuits of this ADC have been modified to enable the injection of calibration voltage to compensate for the static channel gain-mismatch without reducing the input range. Dynamic gain-mismatch due to the finite settling of the S/H is reduced by applying skew-insensitive sampling and using the same calibration coefficients of static gain mismatch. Power reduction is realized using four-input opamp sharing without unity gain frequency or dc gain reductions.

Chapter 7

CONCLUSION AND RECOMMENDATIONS

This chapter summarizes the contributions presented in this thesis and offers some suggestions for future research.

7.1. Contributions of this Thesis

In this dissertation, the following new research contributions associated with high-performance time-interleaved and pipelined ADCs were presented:

- Sampling method to improve spurious free dynamic range of TIADC. Firstly, the mathematical background describing the effect of randomizing the samples among the ADC channels in TIADC was analyzed and consequently a digitally oriented implementation, amenable to integration in deep submicron technology, was proposed.
- Digital blind background calibration method for 1.5b/stage pipelined ADC without affecting the speed or the input dynamic range was presented. In this method, a simple modification to the conventional MDAC allowed the ADC to toggle between different configurations to create a reference signal used to calibrate blindly the ADC in the background.
- Multi-bit-per-stage pipelined ADC calibration using imprecise voltage injection and correlation-based background calibration with duration shortening. By injecting subtractive voltages in a modified conventional multi-bit MDAC and performing correlation based successive coefficient measurements, a background

calibration was achieved. Further, a global gain correction for time-interleaved ADCs was provided. Technique to shorten the calibration duration was further provided.

- A prototype of two-channel 10-bit, 100 MS/s time-interleaved ADC was designed and fabricated in 0.18μm CMOS technology. The front-end S/Hs circuits of this ADC were modified to enable the injection of calibration voltage to compensate for the static gain-mismatch. Dynamic gain-mismatch was reduced by applying skew-insensitive sampling. Power reduction was realized by sharing between every two consecutive stages a four-input opamp free from conventional double sampling drawbacks.

7.2. Recommendations for Future Work

These contributions are behind our motivation to present the following recommendations for future research investigations into the design of high performance pipelined and time interleaved ADCs:

- Investigate the practical energy bounds of A/D conversion, and to develop architecture and circuit techniques to approach such limits. A solution to reduce the power consumption of pipelined ADC can be developed by replacing the opamp by an extremely low power imprecise analog circuit such as passive switched capacitors circuits with very poor linearity and settling precision. That substitution removes the most power hungry block in the ADC and helps to achieve ultra-low power A/D conversion with supreme power efficiency. The

proposed methods in this thesis can be modified to calibrate the ADC from the error stemming while using such imprecise circuits.

- Experimental verification of the proposed methods that have not been verified on-chip; especially the blind background calibration method owing to its very low analog overhead and its promising performance and capability. Also an extension of this method to address not only the errors due to capacitor mismatches and finite opamp gain but also the nonlinear opamp gain is envisaged for future research. A combination between this method and the methods proposed in [GRA05] and [MUR04] to compensate the nonlinearity errors of the opamp is worth of attention.
- In high density SoC, coupling from digital circuits into analog components mostly propagates through the common substrates, thereby being named as substrate coupling. Substrate coupling degrades analog signal integrity in mixed signal integrated circuits where several digital circuits may inject hundreds of millivolts of disturbance in the substrate potential especially during clock transitions. Traditionally, layout techniques have been used to minimize the effect of substrate coupling noise. Modeling the effect of this noise on the ADC performance, and use of digital calibration of this kind of noise are strongly recommended research subjects.

BIBLIOGRAPHY

[ALI03] Ali, A., and Nagaraj, K., "Background calibration of operational amplifier gain error in pipelined A/D converters", *IEEE Trans. Circuits Syst II*, vol. 50, pp. 631 -634, Sept. 2003.

[AND05] Anderson, M., Norling, K., Dreyfert, A., and Yuan, J., " A reconfigurable pipelined ADC in 0.18 μm CMOS ", *Dig. Tech. Papers, Symp. on VLSI Circuits*, pp. 138-139, Feb. 1997.

[BEC03] Beck, D., Allstot, D., and Garrity, D., "An 8-bit, 1.8 V, 20 MSample/s analog-to-digital converter using low gain opamps," in *Proc. IEEE Int. Symp. Circuits Systems*, vol. 1, pp. 25 -28, May 2003.

[BLE03] Blecker, E., McDonald, T., Erdogan, O.,Hurst, P. and Lewis, S., "Digital background calibration of an algorithmic analog-to-digital converter using a simplified queue", *IEEE Journal of Solid-State Circuits*, Vol.38, pp.1059-1062, June 2003.

[BUR00] Buracchini, E., "The software radio concept", *IEEE Communications Magazine*, Vol. 38, pp.138 –143, Sep. 2000.

[CHI00] Chiu, Y., "Inherently linear capacitor error-averaging techniques for pipelined A/D conversion," *IEEE Trans. Circuits Syst. II*, vol. 47, pp. 229-232, Mar. 2000.

[CHU02] Chuang, S., "Digitally self-calibrating circuit and method for pipeline ADC," US patent 6,369,744, Apr.2002.

[CHI04a] Chiu, Y., Gray, P., and Nikolic, B., "A 14-b 12-MS/s CMOS pipeline ADC with over 100-dB SFDR," *IEEE J. Solid-State Circuits*, vol. 39, pp. 2139 -2151, Dec 2004.

[CHU04b] Chiu, Y., Tsang, C.-W., and Nikolic, B, Gray, P., "Least mean square adaptive digital background calibration of pipelined analog-to-digital converters," *IEEE Trans. Circuits Syst. I*, vol. 51, no. 1, pp. 38–46, Jan. 2004.

[CLI96] Cline, D., and Gray, P., "A power optimized 13-b 5 Msamples/s pipelined analog to- digital converter in 1.2 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 31, pp. 294–303, Mar. 1996.

[CON93] Conroy, C., Cline, D., Gray, P., An 8-b 85-MS/s parallel pipeline A/D converter in 1-μm MOS", *IEEE Journal of Solid-State Circuits*, Vol.28, pp.447 –454, Apr. 1993.

[DES99] Dessouky, M. and Kaiser, A., "Input switch configuration suitable for rail-to-rail operation of switched op amp circuits," *Electron. Lett.*, vol. 35, pp. 8–10, Jan. 1999.

[DEW93] De Wit, M., Tan, K.-S., and Hester, R., "A low-power 12-b analog-to-digital converter with on-chip precision trimming," *IEEE J. Solid-State Circuits*, vol. 28, pp. 455–461, Apr. 1993.

[DYE98] Dyer, K., Fu, D., Hurst, P., Lewis, S., "An analog background calibration technique for time-interleaved analog-to-digital converters," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1912 -1919, Dec. 1998.

[EKL00] Eklund, J. and Gustafsson, F., "Digital offset compensation of time-interleaved ADC using random chopper sampling", in *Proc. IEEE Int. Symp. Circuits Systems*, pp. 447-450, 2000.

[EKL02] Eklund, J., "Parallel analog-to-digital converter having random/pseudo-random conversion sequencing," *US patent* 6,392,575, May 21, 2002.

[ELS03] El-Sankary, K., Assi, A., and Sawan, M., "New sampling method to improve the SFDR of time-interleaved ADCs," in *Proc. IEEE Int. Symp. Circuits Systems, ISCAS*, vol.1, pp.833-836, 2003.

[ELS04a] El-Sankary, K., Assi, A., and Sawan, M., "New Sampling Method to Improve the SFDR of Wide Bandwidth ADC Dedicated to Next Generation Wireless Transceiver," *Journal of Circuits, Systems, and Computers*, Vol. 13, No. 6, pp. 1183-1201, Dec 2004.

[ELS04b] El-Sankary, K., and Sawan, M., "A Digital Blind Background Capacitor Mismatch Calibration Technique for Pipelined ADC," *IEEE Transactions Circuits and System II*, vol. 51, pp. 507-510, Oct. 2004.

[ELS04c] El-Sankary, K., and Sawan, M., "A New Digital Background Calibration Technique for Pipelined ADC," in *Proc. IEEE Int. Symp. Cir. Syst., ISCAS,* vol.1, pp.5-8, 2004.

[ELS06a] El-Sankary, K., and Sawan, M., "Digital Background Calibration Techniques for Multibit/Stage Pipelined and Time-Interleaved ADCs," accepted for publication in *IEEE Transactions Circuits and System II,* to appear in June 2006.

[ELS06b] El-Sankary, K., and Sawan, M., "High Resolution Background Calibrated ADCs for Software Defined Radios," accepted for publication in *Microelectronics Journal, Elsevier,* 2006.

[ERD99] Erdogan, O., Hurst, P., and Lewis, S., "A 12-b digital-background calibrated algorithmic ADC with -90-dB THD," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1812–1820, Dec. 1999.

[FET03] Fetterman, H., "Multistage analog-to-digital converter with amplifier component swapping for improved linearity," US patent 6 515 611, Feb.2003.

[FU98] Fu, D., Dyer, K., Hurst, P., Lewis, S., "A digital background calibration technique for time-interleaved analog-to-digital converters," *IEEE J. Solid-State Circuit*s, vol. 33, pp. 1904 -1911, Dec. 1998.

[GAL00] Galton, I., "Digital cancelation of D/A converter noise in pipelined A/D converters," *IEEE Trans. Circuits Syst. II*, vol. 47, pp. 185–196, Mar. 2000.

[GIO05] Giovanni, C., and Andrea, P., "Method of correction of the error introduced by a multibit DAC incorporated in an ADC," *US patent* 6,867,718, Mar. 2005.

[ING98] Ingino, J., and Wooley, B., "A continuously calibrated 12-b, 10-MS/s, 3.3-V A/D converter," *IEEE J. Solid-State Circuit*s, p.1920-1931, Dec.1998.

[JAM02] Jamal, S., Fu, D., Chang, N., Hurst, P., and Lewis, S., "A 10-b 120-Msample/s time-interleaved analog-to-digital converter with digital background calibration," *IEEE J. Solid-State Circuit*s, vol. 37, pp. 1618 -1627, Dec. 2002.

[JEW97] Jewett, R., Poulton, K., Hsieh, K.-C., and Doernberg, J., "A 12 b 128 MSample/s ADC with 0.05 LSB DNL," *Proc. IEEE Int. Solid-State Circuits Conf.*, vol. 40, pp. 138-139, Feb. 1997.

[KAR93] Karanicolas, A., and Lee, H., "A 15-b 1-Msample/s digitally self-calibrated pipeline ADC," *IEEE J. Solid-State Circuit*s, vol. 28, pp. 1207–1215, Dec. 1993.

[KIN04] Kinyua, M., Maloberti, F., and Gosney, W., "Digital background auto-calibration of DAC non-linearity in pipelined ADCs," in *Proc. IEEE Int. Symp. Circuits Systems*, vol. 1, pp. 23 -26, May 2004.

[KUR01] Kurosawa, N., Kobayashi, H., Maruyama, K., Sugawara, H, and Kobayashi, K., "Explicit analysis of channel mismatch effects in time-interleaved ADC systems," *IEEE Trans. Circuits Syst. I*, vol. 48, pp. 261–271, Mar. 2001.

[KWA97] Kwak, S., Song, B., and Bacrania, K., "A 15-b, 5-Msample/s low-spurious CMOS ADC," *IEEE J. Solid-State Circuit*s, vol. 32, pp. 1866–1875, Dec. 1997.

[LEE92] Lee, S., and Song, B., "Digital-domain calibration of multistep analog-to-digital converter," *IEEE J. Solid-State Circuit*s, vol. 27, pp. 1679–1688, Dec. 1992.

[LEE94] Lee, H., "A 12-b 600 ks/s digitally self-calibrated pipelined algorithmic ADC *IEEE J. Solid-State Circuit*s, vol.29, pp.509-515, Apr. 1994.

[LEE05] Lee, S.-C, Kim, G.-H, Kwon, J.-K, Kim, J., and Lee, S.-H, "Offset and dynamic gain-mismatch reduction techniques for 10b 200ms/s parallel pipeline ADCs," in *Proc.of ESSCIRC*, pp. 531 -534, Sept. 2005.

[LEW87] Lewis, S., and Gray, P., "A pipelined 5-Msample/s 9-bit analog-to-digital converter," *IEEE J. Solid-State Circuit*s, vol. 22, pp. 954-961, Dec 1987.

[LEW92] Lewis, S., "Optimizing the stage resolution in pipelined, multistage, analog-to-digital converters for video-rate applications," *IEEE Trans. Circuits Syst. II*, vol. 39, pp. 516–523, Aug. 1992.

[LI02] Li, X., and Ismail, M., "Multi-Standard CMOS Wireless Receivers: Analysis and Design", *Kluwer Academic Publishers*, 2002.

[LI03] Li, J., and Moon, U.-K, "Background calibration techniques for multistage pipelined ADCs with digital redundancy," *IEEE Trans. Circuits Syst. II*, vol. 50, pp. 531–538, Sep. 2003.

[LI04] Li, J., and Moon, U.-K, "A 1.8-V 67-mW 10-bit 100-MS/s pipelined ADC using time-shifted CDS technique," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1468-1476, Sept. 2004.

[LI05] Li, J., Ahn, G.-C, Chang, D.-Y, and Moon, U.-K, "A 0.9-V 12-mW 5-MSPS Algorithmic ADC With 77-dB SFDR," *IEEE J. Solid-State Circuits*, vol. 40, pp. 960–969, Apr. 2005.

[LIN91] Lin, Y., Kim, B., and Gray, P., "A 13-b 2.5-MHz self-calibrated pipelined A/D converter in 3u CMOS," *IEEE J. Solid-State Circuits*, vol. SC-26, pp. 628–636, Apr. 1991.

[MIR00] Mirabbasi, S., and Martin, K., "Classical and modern receiver architectures", *IEEE Communications Magazine*, Vol. 38, pp.132 –139, Nov. 2000.

[MIT00] Mitola, J., "Software Radio Architecture: Object-Oriented Approaches to Wireless Systems Engineering", *John Wiley & Sons Publishers*, 2000.

[MOO97] Moon, U.-K, and Song, B., "Background digital calibration techniques for pipelined ADCs," *IEEE Trans. Circuits Syst. II,* vol. 44, pp. 102–109, Feb. 1997.

[NAG97] Nagaraj, K., Fetterman, S., Anidjar, J., Lewis, S., and Renninger, R., "A 250-mW, 8-b, 52-Msamples/s parallel-pipelined A/D converter with reduced number of amplifiers," *IEEE J. Solid-State Circuit*s, vol. 32, pp. 312–320, Mar. 1997.

[NAG87] Nagaraj, K., Viswanathan, T., Singhal, K., and Vlach, J., "Switched-capacitor circuits with reduced sensitivity to amplifier gain," *IEEE Trans. Circuits Syst. II*, vol. 34, pp. 571–574, Aug. 1987.

[NAI04] Nair, K., and Harjani, R., "A 96dB SFDR 50MS/s digitally enhanced CMOS pipelined A/D converter," *ISSCC Dig. Tech. Paper*s, pp. 456–457, Feb. 2004.

[NAI00] Nairn, D., "A 10-bit, 3V, 100MS/s Pipelined ADC", *IEEE Custom Integrated Circuits Conference,* pp. 257-260, 2000.

[RAZ97] Razavi, B., "RF microelectronics", *Prentice Hall*, 1997.

[SAB03] Sabouri, F., "Self-calibrating methods and structures for pipelined analog-to-digital converters," US patent 6,563,445, May 2003.

[SHA02] Shabra, A., and Lee, H., "Oversampled pipeline A/D converters with mismatch shaping," *IEEE J. Solid-State Circuit*s, vol.37, p.566-578, May 2002.

[SHU97] Shu, T., Song, B., and Bacrania K., "A 13-b, 10-Msample/s ADC digitally calibrated with oversampling delta–sigma converter," *IEEE J. Solid-State Circuit*s, vol. 32, pp. 1866–1875, Dec. 1997.

[SIR00] Siragusa, E., and Galton, I., "Gain error correction technique for pipelined analog-to-digital converters," *Electron. Lett.*, vol. 36, pp. 617–618, 2000.

[SIR04] Siragusa, E., and Galton, I., "A digitally enhanced 1.8V 15b 50MS/s CMOS pipelined ADC," *IEEE J. Solid-State Circuit*s, vol. 39, pp. 2126–2138, Dec. 2004.

[SON88] Song, B., Tompsett, F., and Lakshmikumar, K., "A 12-bit 1-Msample/s capacitor error-averaging pipelined A/D converter," *IEEE J. Solid-State Circuit*s, vol.23, pp.1324-1333, Dec.1988.

[SON00] Sonkusale, S., van der Spiegel, J., and Nagaraj, K., "True background calibration technique for pipelined ADC," *Electron. Lett.*, vol. 36, no. 9, pp. 786-788, Apr. 2000.

[SUM01] Sumanen, L., Waltari, M., and Halonen, K., "A 10-bit 200-MS/s CMOS parallel pipeline A/D converter," *IEEE J. Solid-State Circuit*s, vol. 36, pp. 1048–1055, July 2001.

[SUM02a] Sumanen L., Waltari M., Karhonen T. and Halonen K., " A digital self-calibration method for pipeline A/D converters," in *Proc. IEEE Int. Symp. Circuits System*s, vol. 2, pp. 792 -795, May 2002.

[SUM02b] Sumanen, L., "Pipeline analog-to-digital converters for wide-band wireless communications," *Ph.D. Thesis*, Helsinki University of Technology, 2002.

[SUT88] Sutarja, S., and Gray, P., "A pipelined 13-bit, 250-ks/s, 5V analog-to-digital converter," *IEEE J. Solid-State Circuit*s, vol. 23, pp. 1316 -1323, Dec. 1988.

[TAM01] Tamba, M., Shimizu, A., Munakata, H., and Komuro, T., "A method to improve SFDR with Random Interleaved Sampling Method", in *Proc. IEEE Int. Test Conference*, pp. 512-520, 2001.

[VOG05]Vogel, C., "The impact of combined channel mismatch effects in time-interleaved ADCs," *IEEE Trans. Instrumentation and Measurement*, vol. 54, pp. 415–427, Feb. 2005.

[WAL99] Walden, R., "Analog-to-digital converter survey and analysis", *IEEE Journal on Selected Areas in Communications*, Vol.17, pp.539 –550, Apr. 1999.

[YOO02] Yoo, S.-M, Oh, T.-H, Moon, J.-W, Lee, S.-H, and Moon, U.-K, " A 2.5 V 10 b 120 MSample/s CMOS pipelined ADC with high SFDR", *IEEE Custom Integrated Circuits Conference,* pp. 441-444, 2002.

[YU96] Yu, P., and Lee, H., "A 2.5-V, 12-b, 5-MSample/s pipelined CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1854 -1861, Dec. 1996.

[YU01] Yu, P., et. al., "A 14 b 40 MSample/s pipelined ADC with DFCA," *ISSCC Dig. Tech. Papers*, pp. 136–137, Feb. 2001.