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UNIVERSITÉ DE MONTRÉAL

A MICROCONTROLLER CONTROLLED FLAT GAIN PHASE SHIFTER

ZHONG ZHIYONG

DÉPARTEMENT DE GÉNIE ÉLECTRIQUE
ÉCOLE POLYTECHNIQUE DE MONTRÉAL

MÉMOIRE PRÉSENTÉ EN VUE DE L'OBTENTION
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Ce mémoire intitulé:

A MICROCONTROLLER CONTROLLED FLAT GAIN PHASE SHIFTER

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a été dûment accepté par le jury d'examen constitué de :

M. WU Ke, Ph. D., président

M. AKYEL Cevdet, Ph. D., membre et directeur de recherche

M. CHRISTOPHE Caloz, Ph. D., membre

DEDICATION

To my wife, and
Xiaoxiang, Xiaoxuan and Ziqi for their love

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ABSTRACT

The purpose of this research project is to design and develop a microcontroller controlled flat gain phase shifter that will be used in an automatic active permittivity measurements system (AAPMS), which has a lot of advantages over traditional permittivity measurements: it can measure permittivity in high power, real-time environments at low cost and avoid non-linearity problems.

The AAPMS makes use of an oscillating loop containing a test cavity; it adjusts the phase in the loop so that the oscillating frequency is made exactly equal to the resonant frequency of the test cavity. Then an appropriate algorithm is applied to get the cavity's Q factor which is used to determine the material permittivity in the cavity. The phase shifter is the key component in the AAPMS. It needs to be adjusted to more than 360° with stable gain, because if gain changes too much, the oscillating condition may be lost.

We designed a variable phase shifter that can be regulated continuously to 360° at the frequency of 5.8GHz, and it can be digitally controlled by a computer or microcontroller with the help of D/A converters. Usually, we can design a reflection type or a loaded line type variable phase shifter. The reflection type phase shifter has better matching characteristics but a narrow bandwidth. A loaded line type phase shifter has the advantage of simple fabrication and wide bandwidth, so we prefer this type of phase shifter and use varactors to regulate the phase. An optimized loaded line phase shifter design method is introduced to design a phase shifter with better S parameters, which includes design formulas, varactors selection etc.

However, an optimized insertion loss phase shifter has several dB losses when the

phase is shifted around 360°. Therefore we need a method to compensate the loss. An automatic gain control (AGC) method is introduced to be used here. Gain compression is analyzed, from which we can see if the gain of the feedback circuits and the gain slope constant of the gain controlled device (GDC) are high enough, the output voltage will remain constant when the gain of other in-loop devices are changed. A flat gain phase shifter is realized by combining a loaded line phase shifter, a power detector, a variable attenuator, two power amplifiers and some control circuits. Phase can be changed by regulating the DC bias of varactors in the phase shifter; its output power is detected and compared with a gain reference voltage and then fed back to control a variable attenuator to compensate its gain change. The gain can be regulated by adjusting the setup reference voltage (V_{ref}). Furthermore, if we add an input signal to the reference, we obtain a new AGC circuit, which we call an input tracing AGC circuit. In such circuits, the output power follows the input power and the reference voltage (V_{ref}).

A microcontroller is used to control both V_{ref} and V_{bias} to control system gain and phase. It can be connected to a computer through a RS232 interface in the future to construct a computer controlled automatic permittivity measurement system.

Résumé

Un système actif, automatisé et commandé par ordinateur pour mesurer la permittivité (computer-controlled automatic active permittivity measurement system (AAPMS)) a quelques avantages par rapport à d'autres systèmes comparatifs : le coût est diminué, la précision est plus grande et il peut être plus facilement installé dans un environnement de temps réel. L'objectif de ce projet de recherche est de construire une partie d'un tel système, incluant un déphaseur, le circuit de compensation de gain et le microcontrôleur. Nous appelons ce système un déphaseur à gain constant commandé par microcontrôleur (microcontroller controlled flat gain phase shifter).

L'AAPMS utilise une boucle d'oscillation contenant une cavité. Il règle la phase dans la boucle afin que la fréquence d'oscillation soit égale à la fréquence de résonance de la cavité. Ensuite, un algorithme approprié est appliqué pour obtenir le facteur Q de la cavité, qui est utilisé pour déterminer la permittivité du matériel à l'intérieur de la cavité. Le déphaseur est l'élément de clé dans l'AAPMS : il doit être réglable jusqu'à plus de 360° à gain stable.

D'habitude, il y a deux types de déphaseurs qui peuvent être réglés de façon continue : un déphaseur à réflexion ou un déphaseur à lignes chargées. L'adaptation du déphaseur à réflexion est meilleure, mais il montre une largeur de bande limitée. Un déphaseur à lignes chargées a l'avantage d'une fabrication plus simple et une grande largeur de bande, donc on choisit ce type de déphaseur. Des varactors sont utilisés comme des capacités variables pour régler la phase en changeant leurs polarisations. En outre, une méthode pour le design optimisé d'un déphaseur à lignes chargées avec des

meilleurs paramètres S est présentée. Cette méthode inclut les équations nécessaires, la sélection des varactors, etc.

Pourtant, même pour un déphaseur optimisé, il y aura des pertes d'insertion autour d'une phase de 360°. Donc, pour compenser ces pertes, on utilise la commande automatique de gain (automatic gain control). On analyse la compression du gain, et ainsi, on peut voir si le gain des circuits de rétroaction et la pente du dispositif à commande automatique (gain controlled device) sont assez grands pour maintenir la tension à une valeur constante alors que l'on change le gain des autres dispositifs dans la boucle. Un déphaseur à gain constant est réalisé en combinant un déphaseur à lignes chargées, un détecteur de puissance, un atténuateur variable, deux amplificateurs à puissance et quelques circuits de commande. La phase peut être changée en réglant la polarisation des varactors dans le déphaseur. Leurs puissances de sortie sont détectées et comparées avec une tension de référence de gain et ensuite utilisées pour régler un atténuateur variable pour compenser le changement de gain. Le gain peut être réglé en ajustant la tension de référence de setup (V_{ref}). En outre, si on ajoute un signal d'entrée à la référence, on obtient un nouveau circuit AGC qui s'appelle un "input tracing AGC circuit". Dans de tels circuits, la puissance de sortie suit la puissance d'entrée et la tension de référence (V_{ref}).

Un microcontrôleur est utilisé pour ajuster à la fois Vref et Vbias pour régler le gain du système et la phase. Dans le futur, il peut être connecté à un ordinateur par une interface RS232 pour établir un système actif, automatisé et commandé par ordinateur pour mesurer la permittivité.

CONDENSÉ EN FRANÇAIS

La permittivité d'un milieu est une quantité physique très importante qui décrit comme un champ électrique influent et est influencée par ce milieu. La permittivité peut être vue comme la qualité d'un matériel à conserver de la charge électrique. Une certaine quantité de matériel avec une grande permittivité peut conserver plus de charges qu'un matériel avec une permittivité plus petite. Des différents matériels peuvent être distingués en mesurant leurs permittivités complexes. Il existe différentes méthodes pour mesurer la permittivité correspondante à la fréquence et la technologie de mesure. La technique de la perturbation de cavité a une meilleure précision : habituellement, les mesures de perturbation de cavité conventionnelles utilisent une cavité de transmission, un détecteur de puissance et un oscilloscope ou un autre instrument pour enregistrer la courbe de résonance et ensuite calculer le facteur Q des valeurs obtenues. Avec ce dernier, on peut enfin obtenir la permittivité d'un échantillon placé à l'intérieur de la cavité. Pourtant, ces méthodes mesurent l'amplitude des signaux, qui peut être distordue par des non-linéarités dans des détecteurs, des amplificateurs, etc. En raison de ce problème, des méthodes actives ont été proposées dans le but d'améliorer la précision. Ils utilisent une boucle d'oscillation avec la cavité, pour que la fréquence d'oscillation soit proche à la fréquence de résonance de la cavité contenant l'échantillon à analyser. Un algorithme approprié ajuste la fréquence de résonance de la cavité afin que la fréquence d'oscillation soit égale à la fréquence de résonance de la cavité. Le facteur Q de la cavité est trouvé par une modulation d'un déphaseur dans la boucle afin de produire un

décalage de fréquence d'oscillation qui est proportionnel au facteur Q de la cavité. Pour réaliser des mesures en temps réel, un système commandé par ordinateur devient nécessaire. Un tel système actif, automatisé et commandé par ordinateur pour mesurer la permittivité (computer-controlled automatic active permittivity measurement system (AAPMS)) peut être établi par un microcontrôleur ensemble avec un compteur de fréquence et des composants actifs micro-ondes pour mesurer la permittivité avec une cavité. Un ordinateur peut être utilisé pour télécommander le système. La méthode proposée a quelques avantages auprès d'autres systèmes comparatifs : le coût est diminué, la précision est plus grande et il peut être plus facilement installé dans un environnement de temps réel. L'objectif de ce projet de recherche est de construire une partie d'un tel système, incluant un déphaseur, le circuit de compensation de gain et le microcontrôleur. Nous appelons ce système un déphaseur à gain constant commandé par microcontrôleur (microcontroller controlled flat gain phase shifter).

Dans l'AAPMS, le facteur Q_{0s} de la cavité avec l'échantillon peut être calculé de la fréquence de résonance ω_{0s}, la différence de fréquence $\Delta\omega_{0s}$ et les paramètres sans l'échantillon ω_0, $\Delta\omega_0$ et Q_0. Le déphaseur est l'élément de clé dans l'AAPMS. Il doit 1) être réglable jusqu'à plus que 360° afin de trouver le point résonant, 2) maintenir un gain stable pendant que la phase est changée, sinon la condition d'oscillation disparaît, et 3) avoir assez de largeurs de bande et une bonne perte de réflexion.

Généralement, il y a deux types de déphaseurs qui peuvent être réglés de façon continue : un déphaseur à réflexion ou un déphaseur à lignes chargées. D'habitude, un déphaseur à réflexion se compose d'un coupleur hybride et de deux charges identiques. Il

utilise un nombre minimal de composants, il est compact et montre une meilleure perte de réflexion que le deuxième type. Pourtant, la largeur de bande est limitée. Par contre, un déphaseur à lignes chargées a l'avantage d'une fabrication plus simple et une grande largeur de bande, donc on choisit ce dernier pour notre projet. Il peut être vu comme plusieurs étages de circuits LC, dont chaque partie peut être considérée comme un réseau Pi. La phase de cette structure peut être variée en changeant l'admittance Y_c. Une autre façon de décrire cette structure est d'une ligne de transmission avec une impédance caractéristique variable et une vitesse de phase variable. La perte d'insertion inclut la perte de la diode et la perte de la ligne. La perte totale dépend du facteur de charge x, et la perte d'insertion optimale est trouvée autour de $x = 1$.

La variable Y_c est normalement réalisée par une diode varactor, qui utilise les caractéristiques de la couche de déplétion d'une diode P-N. Il y a trois types de varactors: (abrupt junction varactors, frequency linear et hyperabrupt junction varactors). Ils ont, de différentes caractéristiques pour la courbe C-V. (L'abrupt junction varactors) montre un intervalle limité de capacitance, un facteur Q élevé et une faible distorsion; (l'hyperabrupt jonction varactor) permet un plus grand changement de capacitance pour le même intervalle de polarisation, et le (frequency linear varactor) a une courbe caractéristique fréquence-tension qui est presque linéaire. Pour choisir un varactor approprié, nous devons considérer quelques paramètres: 1) la fréquence de coupure, qui est reliée au facteur Q ou les pertes de la diode, 2) le rapport du réglage de capacité qui détermine l'intervalle de phase et 3) la fréquence de résonance et la fréquence Bragg qui influence la perte d'insertion.

La procédure de la conception du déphaseur suit les étapes suivantes : 1) Pour $x = 1$, il faut trouver l'impédance caractéristique Z_0. 2) De la fréquence f, il faut trouver la fréquence Bragg f_b et la fréquence de résonance f_r – toutes les deux se doivent d'être plus grandes que f – et ensuite, de ces valeurs, il est possible de déterminer la capacité maximale C_{max} ainsi que l'inductance L_p du varactor. 3) Maintenant, on peut choisir les diodes varactors. 4) Il faut déterminer la distance entre les varactors pour des différents facteurs de charge x. 5) Le déphasage maximal par étage doit être évalué et donc le nombre de varactors nécessaire pour obtenir un déphasage total de 360° pour des différentes valeurs de x peut être déterminé. 6) En effectuant une simulation ADS, on peut prédire les résultats. 7) Ensuite, on peut choisir la solution avec les meilleurs paramètres S. 8) Maintenant, il est possible d'effectuer le design RF.

Avec cette méthode nous avons terminé notre design de déphaseur en utilisant 16 varactors de type MDT21002-46, une ligne de transmission avec un substrat de $\varepsilon_r = 3.05$, une épaisseur $h = 20$ mil, une largeur de ligne $W = 21.92$ mil et une distance entre les varactors $l_{sec} = 3.3$ mm. Les résultats de la simulation dans ADS démontrent qu'une variation de polarisation du déphaseur de 2 V à 29 V permet une variation de la phase jusqu'à 360° avec un changement de gain de 2.5 dB.

Même si une méthode pour optimiser les pertes d'insertion est utilisée, le gain varie encore de quelques dB en réglant la phase. Pour réaliser un déphaseur à gain constant, il est nécessaire de trouver un moyen pour compenser cette variation. Une méthode de commande automatique de gain (automatic gain control (AGC)) est introduite. Son principe est fondé sur la théorie de contrôle de rétroaction. Le signal de sortie est détecté

et comparé avec une référence et un signal de contrôle est généré pour régler le dispositif à commande automatique (gain controlled device (GCD)) afin de maintenir le signal de sortie à un niveau constant. Le GCD peut être un amplificateur à commande de gain ou un atténuateur réglé. Dans notre projet on utilise ce dernier. Si la puissance d'entrée est dans l'intervalle $V_1<V_{in}<V_2$ ou le gain est dans $Ga_1<Ga<Ga_2$, le niveau de la sortie reste presque stable si la pente du GCD et le gain de la boucle de rétroaction sont beaucoup plus larges que 1. Cela peut être démontré avec les modèles dynamiques pour les AGC. Comme pour tout autre système de contrôle, nous avons besoin de retrouver son modèle avec la méthode de fonction de transformation, et ensuite, nous pouvons concevoir le filtre d'AGC avec ce modèle afin de permettre la stabilité et une réponse rapide du système avec peu d'erreurs statiques. Dans ce projet, la stabilité et les erreurs statiques sont considérées comme plus importantes que le temps de réponse pour faciliter le design du filtre.

Un déphaseur à gain constant est réalisé en combinant un

déphaseur à lignes chargées, un détecteur de puissance, un atténuateur variable, deux amplificateurs à puissance et quelques circuits de commande. La phase peut être changée en réglant la polarisation des varactors dans le déphaseur. Le gain peut être réglé en variant la tension de référence de setup (V_{ref}). En effectuant une simulation ADS, on peut prédire les résultats. D'abord, on construit les modèles ADS des atténuateurs variables et du déphaseur en utilisant des amplificateurs contrôlés combinés avec des déphaseurs, dont les paramètres sont déduits des spécifications ou des mesures à des différentes polarisations. Ensuite, on peut établir le modèle ADS entier avec les autres

composants comme le diviseur de puissance, l'amplificateur et le détecteur. Lors des résultats de la simulation le temps de réponse est moins que 50 ms, les erreurs statiques sont assez petites, et les conditions suivantes peuvent être satisfaites : 1) Si la tension de référence de gain est changée, la puissance de sortie suit, mais la phase n'est pas influencée. 2) Si la polarisation du déphaseur est variée, la phase de sortie suit, mais le gain reste stable. 3) Un changement à l'entrée n'influencera pas l'amplitude et la phase à la sortie. 4) La fréquence changera la sortie légèrement. En outre, si on ajoute un signal d'entrée à la référence, on obtient un nouveau circuit AGC qui s'appelle un "input tracing AGC circuit ". Dans tels circuits, la puissance de sortie suit la puissance d'entrée et la tension de référence (V_{ref}).

Le circuit RF est fabriqué sur un substrat de $\varepsilon_r = 3.05$, une épaisseur $h = 20$ mil, et il est adapté à 50 Ω. L'atténuateur variable est un Hittie HMC345MS8G GaAs MMIC, qui peut être réglé de 0 à 30 dB avec une polarisation de 0 à -2.5 V jusqu' à une fréquence de 8 GHz. Après l'atténuateur et le déphaseur, on ajoute deux amplificateurs pour s'assurer que le signal reste dans un certain intervalle dynamique. On utilise l'amplificateur Gali29, qui peut opérer de DC à 7 GHz avec une puissance de sortie de 17.6 dBm et qui est déjà adaptée à 50 Ω à l'entrée et la sortie. La puissance d'entrée/ de la sortie est autour de 5 dBm, donc on peut utiliser des diodes Schottky pour détecter le signal. Nos diodes choisies sont des Agilent SOT-363 Schottky barrier diodes HSMS-282K. Un 3-dB 90° hybride est utilisé comme diviseur de puissance. Pour un design préliminaire, on utilise d'abord un déphaseur commercial qui peut être réglé jusqu'à 360°. Pourtant, le changement de gain pour ce déphaseur est très élevé avec une valeur de 10 dB et ses

paramètres S ne sont pas bons. Par contre, après la compensation cette solution pourrait fonctionner. Si la performance de ce déphaseur n'est pas suffisante, un nouveau déphaseur, comme il a été décrit ci-dessus, doit être conçu. L'expérience démontre que la phase du déphaseur commercial n'est pas beaucoup influencée par la compensation du gain et le gain peut être stabilisé avec un circuit de compensation, donc il est possible d'utiliser celui-ci dans notre projet.

Un circuit de microcontrôleur est construit avec les éléments suivants: 1) une alimentation électrique pour générer ±5 V et ±15 V, 2) un ATMEL AT89C52 microcontrôleur à 8 bit, 3) un clavier numérique pour saisir la phase et le gain directement ou pour les augmenter / réduire, 4) un affichage à cristaux liquides (liquid crystal display (LCD)) pour montrer les valeurs, 5) des convertisseurs numériques analogiques (on utilise des MAX5541), 6) un convertisseur analogique numérique pour surveiller la puissance dans le futur et 7) des circuits de commande pour la phase et le gain. Le circuit est fabriqué sur une carte de circuits imprimés pour de basses fréquences. Le microcontrôleur accomplit les tâches suivantes : 1) il lit la valeur d'entrée pour le déphasage et le gain du système du clavier et les montre sur l'affichage. 2) Il lit et écrit l'EEPROM pour charger / conserver les dates afin de les réutiliser. 3) Il contrôle les convertisseurs numériques analogiques pour sortir la phase et le gain aux amplificateurs.

Conclusion : Un déphaseur à gain constant commandé par microcontrôleur (microcontroller controlled flat gain phase shifter) a été réalisé. La phase peut être réglée jusqu'à 360°. L'ondulation du gain est réduite de ±5 à ±0.2 dB. Le gain et la phase peuvent être réglés par le microcontrôleur étape par étape ou en saisissant les valeurs

directement avec le clavier. Le déphaseur démontré peut être utilisé indépendamment ou comme un dispositif secondaire pour régler la phase et le gain lors d'un ordinateur en ajoutant une interface appropriée.

Travail dans le futur : La performance du déphaseur commercial qui est utilisé est mauvaise concernant ses pertes d'insertion et réflexion. Il pourrait devenir nécessaire de concevoir la solution qui a été simulée. Une interface RS232 ou sans-fil et un logiciel pourraient être ajoutés afin de réaliser un système actif, automatisé et commandé par ordinateur pour mesurer la permittivité (computer-controlled automatic active permittivity measurement system).

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INTRODUCTION

Permittivity measurements using resonant cavity techniques have been studied over the past sixty years. Conventional cavity perturbation measurements usually use a transmission cavity, sweeper, power detector, and an oscilloscope or another instrument to record the resonance curve and thereby provide the necessary information on the Q-factor to calculate the permittivity of a sample material placed within the cavity. A new automatic active measurement system (AAPMS) was presented [16] which use a digitally controlled phase shifter and attenuator to form an oscillating loop containing the test cavity, so that the frequency of oscillation is equal to the resonant frequency of the cavity with its test sample, and then through some algorithm obtain the Q-factor and permittivity. In Chapter 1 of this thesis, a detailed description of such a system and the calculation of the Q-factor will be provided. Furthermore, the advantages of such system over others will be discussed.

One of the key components in the AAPMS is the phase shifter that needs to be adjusted to more than 360°. In Chapter 2 we will introduce different types of phase shifters and their advantages and disadvantages. Then, a detailed design procedure for varactor loaded line phase shifter will be introduced, include the selection of suitable varactors, the design of the transmission line, the durance of varactors, and its simulation in ADS.

In an AAPMS, the phase shifter should maintain a stable gain when phase changes. However, phase shifter usually shows a loss of several dB when adjusting the phase. Therefore a method to compensate the gain is needed. In Chapter 3, we will present the

principle on how to compensate the gain loss and the specific circuits' realization. We will build different components' models and simulate the compensation system in ADS. We will introduce a new input tracing AGC method that does not only maintain stable output power as conventional AGC do, but also maintain a stable Pout/Pin ratio when the input power changed. This new method is simulated in ADS.

A microcontroller control circuit will be presented in Chapter 4. We can use it to control phase (in degrees) and gain (in dB) entered from keypads. D/A converters are used to transfer the input values to the phase shifter's bias voltage V_{bias} and its gain setup reference voltage V_{ref}.

Finally, the whole project will be concluded and a set of future works will be proposed and discussed.

Chapter 1. PERMITTIVITY MEASUREMENT

1.1. Medium Permittivity

The permittivity of a medium is an important physical quantity that describes how an electric field affects and is affected by the medium. Permittivity can be seen as the quality of a material that allows it to store electrical charge. A given amount of material with high permittivity can store more charge than a material with lower permittivity.

Permittivity can have a real or complex value. In general, it is not constant, as it can vary with the position in the medium, the frequency of the field applied, humidity, temperature, and other parameters. The permittivity of a material is usually given relative to that of vacuum, as a relative permittivity, ε_r (also called dielectric constant in some cases). The actual permittivity is then calculated by multiplying the relative permittivity by ε_0:

$$\varepsilon = \varepsilon_r \varepsilon_0 = (1 + \chi_e)\varepsilon_0 \tag{1.1.1}$$

where χ_e is the electric susceptibility of the material.

Opposed to vacuum, the response of real materials to external fields generally depends on the frequency of the field. This frequency dependence reflects the fact that a material's polarization does not respond instantaneously to an applied field. The response must always be *causal* (arising after the applied field). For this reason permittivity is often treated as a complex function of the frequency of the applied field ω, $\varepsilon \rightarrow \hat{\varepsilon}(\omega)$. The

definition of permittivity therefore becomes

$$D_0 e^{i\omega t} = \hat{\varepsilon}(\omega) E_0 e^{i\omega t}, \tag{1.1.2}$$

where D_0 and E_0 are the amplitudes of the displacement and electrical fields, respectively, $i = \sqrt{-1}$ is the imaginary unit.

The static permittivity is a good approximation for altering fields of low frequencies, and as the frequency increases, a measurable phase difference δ emerges between ***D*** and ***E***, but ***D*** and ***E*** remain proportional, and

$$\hat{\varepsilon} = \frac{D_0}{E_0} e^{i\delta} = |\varepsilon| e^{i\delta} \tag{1.1.3}$$

Separating its real and imaginary parts, it becomes

$$\hat{\varepsilon}(\omega) = \varepsilon'(\omega) - i\varepsilon''(\omega) = \frac{D_0}{E_0}(cos\delta - i \sin \delta) \tag{1.1.4}$$

The real part of the permittivity, ε', is related to the fraction of the energy dispersed by the medium.

The complex permittivity is usually a complicated function of frequency ω, but in the narrow frequency ranges that are often studied in practice, the permittivity can be approximated as frequency-independent.

1.2. Permittivity measurement methods

The dielectric constant of a material can be found by a variety of static electrical measurements. The complex permittivity is evaluated over a wide range of frequencies by using different variants of dielectric spectroscopy, covering nearly 21 decades from 10^{-6} to 10^{15} Hz. Also, by using cryostats and ovens, the dielectric properties of a medium can be characterized over a wide range of temperatures.

Measurement methods are strongly dependent on the frequency. As shown in the table below, several techniques are therefore used, each useful only in a certain frequency range. [1]

Frequency Range (Hz)	**Measurement Method**
10^{-4} to 10^{-1}	D.C. Transient Measurements
10^{-2} to 10^{2}	Ultra Low Frequency Bridge
10 to 10^{7}	Schering Bridge and Auto Balancing Bridge
10^{5} to 10^{8}	Resonance Circuits
10^{8} to 10^{9}	Coaxial Line and Re-entrant Cavity
10^{9} to 3 x 10^{10}	H_{01n} Cavity Resonator and Waveguides

Table 1- 1 Different permittivity measurement methods according to frequency

The measurement of complex dielectric permittivity at microwave frequencies is considered important since it gives the relaxation time, dipole moment in liquids, characterization of ferrites for device applications, microwave conductivity, momentum relaxation time, effective mass in semiconductors, etc. Depending on the sample conditions, the method of measurement varies: while Surber's plunger technique [2] is widely used for liquids, von Hippel's SWR technique [3] is used for solids.

The cavity perturbation technique was proposed by Montgomery in 1947[4] and further developments in both experimental and theoretical aspects have been made shown

[5]-[7]. This technique is used for both liquids and solids. Simple measurement procedure, high sensitivity, automated experiment facility, direct evaluation of complex dielectric permittivity, as well as magnetic permeability are some salient features of the technique. It is based on the change in the resonant frequency and quality factor of the cavity due to the insertion of a sample inside the cavity at the electric field maximum position or the magnetic field maximum position, depending on the nature of the parameter to be studied. For normal case, the complex permittivity can be obtained as follows:

$$\frac{f_1 - f_0}{f_0} = -\frac{1}{2F}\left(\varepsilon' - 1\right) \tag{1.2.1}$$

$$\frac{1}{Q_1} - \frac{1}{Q_0} = \frac{\varepsilon''}{F} \tag{1.2.2}$$

where f_0 and f_1 are the resonant frequency of the empty and sample loaded cavity, respectively, Q_0 and Q_1 are the quality factors of the empty and sample loaded cavity, respectively. F is a filling factor that depends on sample geometry and field distribution in the cavity.

Conventional cavity perturbation measurements usually use a transmission cavity, sweeper, power detector, and an oscilloscope or other instrument to record the resonance curve, and thereby, provide the necessary information on the resonant frequency and the Q factor to calculate the permittivity of a sample material placed within the cavity. Although there are different methods such as ***(a)*** successive transmission tests (empty cavity, cavity with test sample) [9] or a reference cavity [10], ***(b)*** a cavity with two operating modes where both modes can be used to measure the test sample, or one mode is used to heat the

sample and the remaining mode is used to make the permittivity measurements [11], and *(c)* reflection coefficient test [12], they all use amplitude measurement methods to determine the cavity response.

1.3. Automated-active circuits method

Active permittivity measurements methods were proposed [13], [14] to improve accuracy. They make use of an oscillating loop containing the test cavity, so that the frequency of oscillation is close to the resonant frequency of the cavity with its test sample. An appropriate algorithm [15] adjusts components in the resonant loop such that the oscillating frequency is made exactly equal to the resonant frequency of the test cavity. The Q factor of the cavity is found by modulating a phase shifter, within the loop, so as to produce a frequency shift in the oscillating frequency, proportional to the cavity Q factor. The absolute value of the Q factor is then found by relating the relative Q factor measurement of the test cavity to the measurement made on a reference cavity containing a sample material of known permittivity.

The advantage of this method is that all the measurements are related to the phase response of the cavity rather than to its amplitude response which may be distorted by nonlinearities in detectors, saturated amplifiers, etc. So the peak of the cavity response is more accurately determined. Another advantage is that measurement and sample heat can be done together, thereby providing an accurate determination of material behaviour under heat stresses produced by microwave power or more simple to measure the

variation of the sample permittivity with increasing temperatures. The simple structure is shown in Figure 1-1, here the oscillating conditions are uniquely determined by the following relation [16]:

$$\prod G_i \geq 1 \tag{1.3.1}$$

$$\sum \Phi_i = 2\pi N \tag{1.3.2}$$

where G_i represents the gain of both active and passive circuit components and Φ_i the phase change for the same components.

The simplest active circuit consists of an amplifier, a 360° phase shifter, a length L of transmission line corresponding to the path lengths between the various components, and a test cavity resonant at a radian frequency ω_0. For oscillations occurring at a frequency ω near the cavity resonance ω_0, the phase modulator is needed to enable control of the generated frequency and make it exactly equal to the test cavity resonant frequency, see Figure1-1

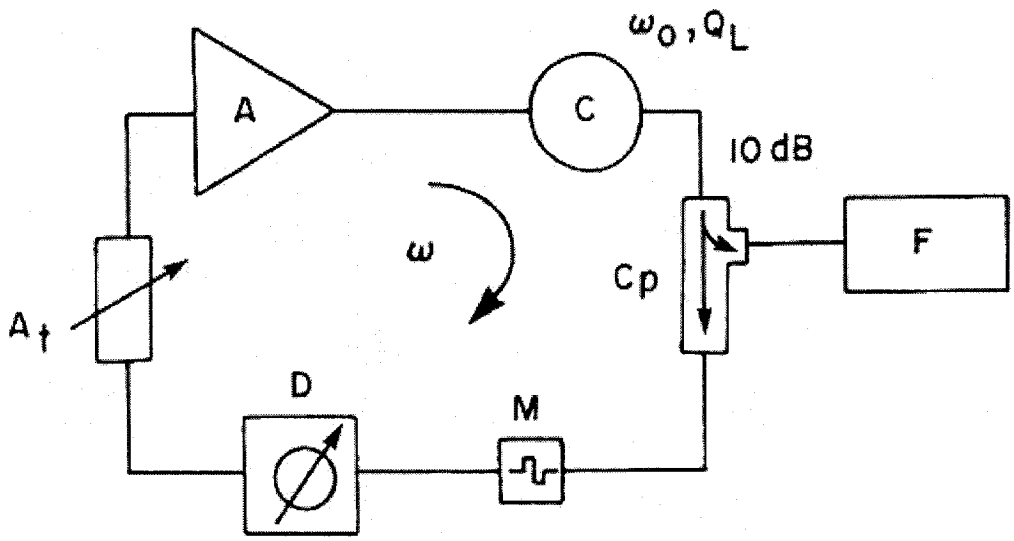


Figure 1- 1 Active cavity permittivity measurement

The phase shift ϕ_c of the cavity at the radian frequency ω is given by

$$\phi_c = -\tan^{-1}\left[Q_0\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right)\right] \tag{1.3.3}$$

Equation (1.3.2) can be now written as:

$$\phi_D + \phi_M = T\omega + \tan^{-1}\left[Q_0\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right)\right] - \phi_A + 2N\pi \tag{1.3.4}$$

where

ϕ_D Phase difference provided by the phase shifter,

ϕ_M Phase modulation provided by the phase modulator,

ϕ_A Amplifier phase difference,

T Delay introduced by the length of transmission line.

A phase modulation $\Delta\phi_M$ will produce a radian frequency shift $(\Delta\omega)$ at a given value of

the phase shifter (ϕ_D), given

$$-T\Delta\omega+\frac{\Delta\phi_c}{\Delta\omega}d\omega+\Delta\phi_M=0 \tag{1.3.5}$$

From the above it can be shown that

$$\Delta\omega=\Delta\phi_M\frac{1}{T+\dfrac{\omega_0 Q_0\left(\dfrac{1}{\omega_0^2}+\dfrac{1}{\omega^2}\right)}{1+Q_0^2\left(\dfrac{\omega}{\omega_0}-\dfrac{\omega_0}{\omega}\right)^2}} \tag{1.3.6}$$

The above equation provides a new resonance curve ($\Delta\omega$ versus ϕ_D) by simply varying the value of the phase shifter ϕ_D. For constant values of $\Delta\phi_M$ and *T*, the new resonance curve passes through a minimum when the value of ϕ_D produces a value of ω equal to ω_0 (see Figure. 1-*2*).

A. *Relative Q, value measurements*

From (1.3.4) it can be shown that

$$\Delta\phi_M=\left(T-\frac{\Delta\phi_C}{\Delta\omega}\right)\Delta\omega \tag{1.3.7}$$

when

$$\frac{\Delta\phi_D}{\Delta\omega}=\frac{\Delta\phi_A}{\Delta\omega}=0 \tag{1.3.8}$$

Using the following approximations for $\omega\approx\omega_0$

$$\omega_0\left(\frac{1}{\omega_0^2}+\frac{1}{\omega^2}\right)\approx\frac{2}{\omega} \tag{1.3.9}$$

and

$$\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\approx\frac{2(\omega-\omega_0)}{\omega_0} \tag{1.3.10}$$

It can be shown from (1.3.3) that

$$\frac{\Delta\phi_c}{\Delta\omega}=\frac{-2Q_0}{\left[1+4Q_0^2\left(\frac{\omega-\omega_0}{\omega}\right)^2\right]\omega} \tag{1.3.11}$$

If ω is very close to ω_0

$$\frac{\Delta\phi_c}{\Delta\omega}\approx-\frac{2Q_0}{\omega} \tag{1.3.12}$$

then from (1.3.10) we get

$$Q_0=\frac{\Delta\phi_{\mathrm{M}}}{2}\frac{\omega_0}{\Delta\omega_0}-\frac{T}{2}\omega_0 \tag{1.3.13}$$

In the case where a sample is present in the cavity we get

$$Q_{0s}=\frac{\Delta\phi_M}{2}\frac{\omega_{0s}}{\Delta\omega_{0s}}-\frac{T}{2}\omega_{0s} \tag{1.3.14}$$

where ω_{0s} is the new value of the radian resonant frequency and $\Delta\omega_{0s}$ is the new value of the radian frequency modulation corresponding to the same phase modulation $\Delta\phi_M$. Combining (1.3.13) and (1.3.14) we get

$$Q_{0s}=Q_0\frac{\Delta\omega_0}{\Delta\omega_{0s}}\frac{\omega_{0s}}{\omega_0}-\frac{T}{2}\omega_{0s}\left(\frac{\Delta\omega_{0s}-\Delta\omega_0}{\Delta\omega_{0s}}\right) \tag{1.3.15}$$

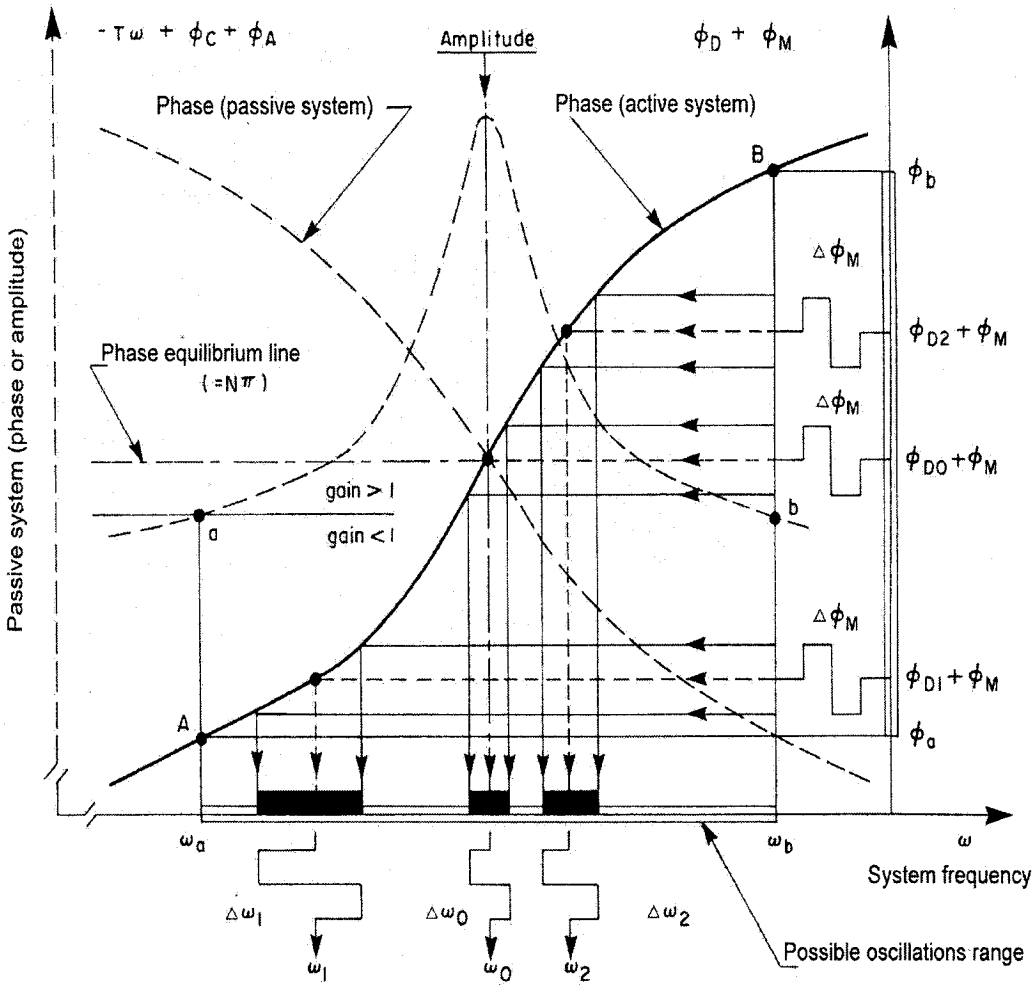


Figure 1- 2 Resonant frequency tracking algorithm with constant phase modulation to determine relative Q factor

At the frequency about 5.8GHz, T is very small, and (1.3.15) can be simplified as:

$$Q_{0s} = Q_0 \frac{\Delta\omega_0}{\Delta\omega_{0s}} \frac{\omega_{0s}}{\omega_0} \tag{1.3.16}$$

***B**. Absolute Q value measurement*

The amplitude measurement is used to determine the Q_0 of the empty cavity. Figure

1-3 shows the method of the measurement.

First attenuation is maximized so that no oscillation can occur, then it is continuously decreased and the phase is regulated to 360° at each attenuator position until oscillation is achieved, then attenuation and phase are regulated until oscillation occurs only at one single phase value. At this point the oscillation frequency is equal to the cavity resonance frequency (f_0). By decreasing the above attenuation level by 3 dB, an oscillation zone is identified between two frequencies f_2 and f_1. The Q_0 value is then given by

$$Q_0 = \frac{f_0}{f_2 - f_1} \tag{1.3.17}$$

Such an automatic active cavity permittivity measurement system can be constructed as shown in Figure 1-4. Here a variable attenuator is used to control the gain as shown in Figure 1-3. It is also used to compensate loss when adjusting phase. A phase shifter is used to regulate phase from 0 to 360° to the resonant point ω_0 as in Figure 1-2 and Figure 1-3. The RF amplifier is used to amplify the signal to some level so that it can be detected easily, it also act as preamplifier for the power amplifier, which is used to increase the cavity input power needed for measurement. A band pass filter is used to reject noise, and a phase modulator is added to act as phase modulation as shown in Figure 1-2. A microcontroller control circuit is used to get information of power and frequency as well as to control phase shifter and variable attenuator in order to regulate system's phase and gain. In addition, the microcontroller can be connected to a PC via RS-232 interface to

allow for comprehensive processing and displaying of the measured data.

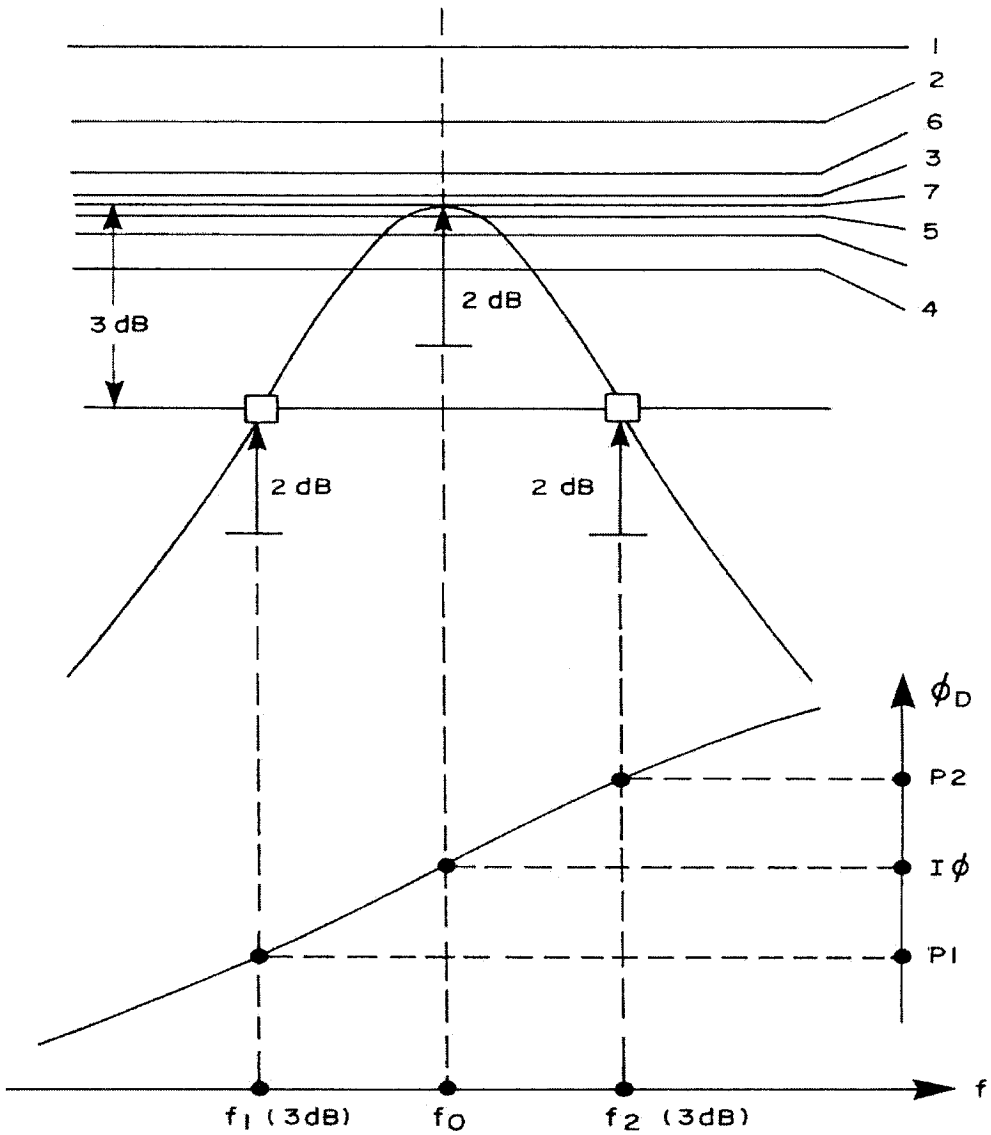


Figure 1- 3 Absolute-Q measurement algorithm using precision digitally controlled attenuator

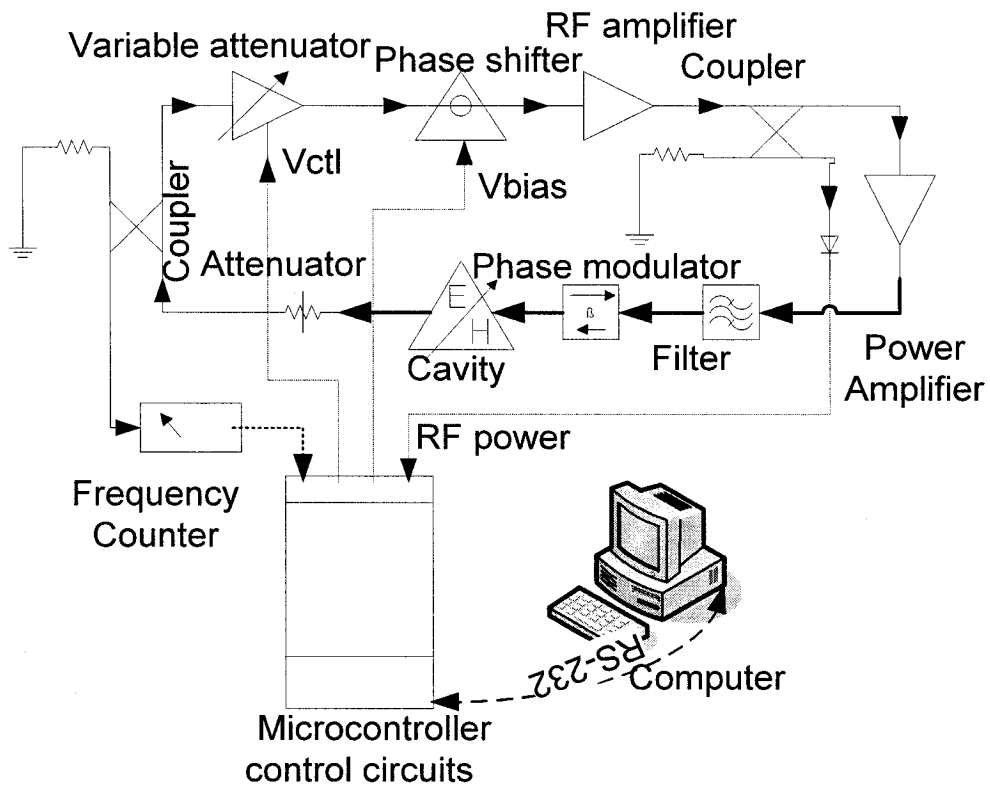


Figure 1-4 An automatic active cavity permittivity measurement system at 5.8GHz

1.4. Phase shifter requirement in automated measurement

Figure 1-2 and 1-3 shows that we need to regulate the phase in order to get the resonant frequency or obtain oscillation both in absolute Q and relative Q measurement. Thus, the phase shifter is one of the key components in the automatic measurement system. It should provide the following features:

1) The phase should be adjusted from 0 to 360°.

From Figure 1-3, to obtain oscillation, we need regulate gain step by step, and in each step, regulate the phase to 360°. Figure 1-2 shows that phase should be shifted from Φ_a to Φ_b, which is within 0 to 360°.

2) The gain of the phase shifter should remain stable.

Formulas (1.3.3) to (1.3.17) are derived from oscillation condition. If the gain changes when shifting phase, the condition may be lost because (1.3.1) may not be satisfied anymore.

3) The phase should be digitally controlled.

To realize automatic measurement, a computer or a microprocessor digital control signal needs to control a digital phase shifter, or to control the bias voltage of an analog phase shifter through a D/A converter.

The aim of this project is to realize key parts of an AAPMS as in Figure 1-4, that regulate phase and gain by a microcontroller and maintaining gain stable. We call this system "a microcontroller controlled flat gain phase shifter", shown in Figure 1-5.

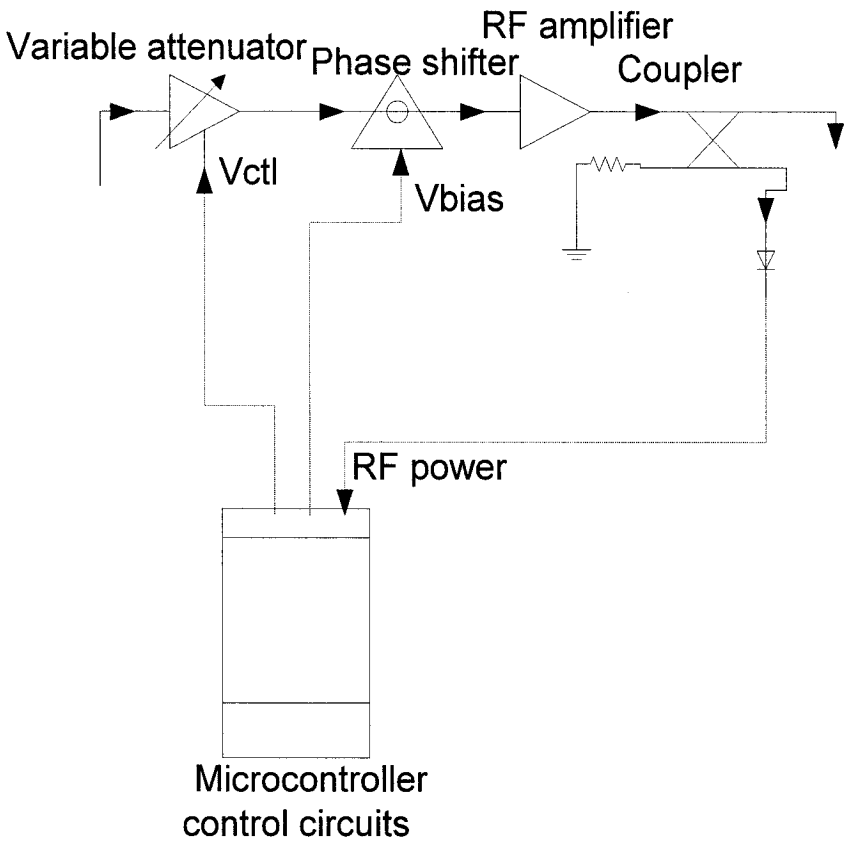


Figure 1-5 Structure of a microcontroller controlled flat gain phase shifter

Chapter 2. PHASE SHIFTER

2.1. Phase shifter types

Phase shifters are devices that are used to adjust the transmission phase in a system by changing phase parameters. As we know:

$$\phi = \beta * l \tag{2.1.1}$$

$$\beta = \frac{w}{v_p} \tag{2.1.2}$$

$$v_p = \frac{1}{\sqrt{\varepsilon_{eff}}} = \frac{1}{\sqrt{LC}} \tag{2.1.3}$$

From (2.1.1), to change the phase Φ, it is either needed to change β or change l. Changing β can be realized by modifying L,C or ε_{eff}.

There are different types of phase shifters. Three well known types are the switch line, the reflection, and the loaded line phase shifter.

Switch line phase shifter:

This type of phase shifter changes phase by adjusting l by using two SPDT switches as shown in Figure 2-1. The lower path has a transmission length l, while the upper path has a transmission length $l+\Delta l$. This difference in length Δl results in a phase difference $\Delta\Phi$ according to:

$$\Delta\phi = \frac{2\pi\Delta l}{\lambda} \tag{2.1.4}$$

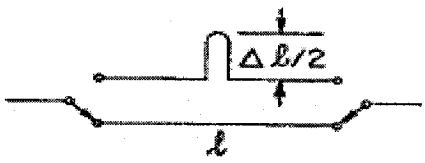


Figure 2- 1 Switch line phase shifter

The effective length is then given by the electrical length plus the equivalent length of the capacitive OFF diode switches. In general, selecting $2\pi l\lambda$ in the range of 20° to 50° will sure that phase errors are a minimized. This type of phase shifter is simple and has low loss advantage, suitable for making a phase shifter that generates fix phase.

Reflection Phase shifters:

The reflection type phase shifter can be designed as switch or analog one depends on its termination. They can be realized in many different forms, but in general they include a quadrature coupler and dual, identical reflective loads. The reflective loads are one-port circuits with variable phase reflection characteristics. The quadrature coupler's function is to isolate the input and output signals, and turning the phase shifting behaviour of the reflective load into more usable two-port device.

Figure 2-2 shows a typical reflection phase shifter. The input and output ports are assumed to be matched to 50Ω. The input power at port (1) is divided equally to the coupled port (3) and through port (2) of the hybrid and reflected from these ports. The reflected signal undergoes a phase change determined by the reflection coefficient of the terminating impedance. The power is then recombined at the isolated port of the hybrid which forms the circuit output. In the simplest case of an ideal diode termination, the

reflection coefficient is controlled by switching ON and OFF to realize a phase shift of 180°.

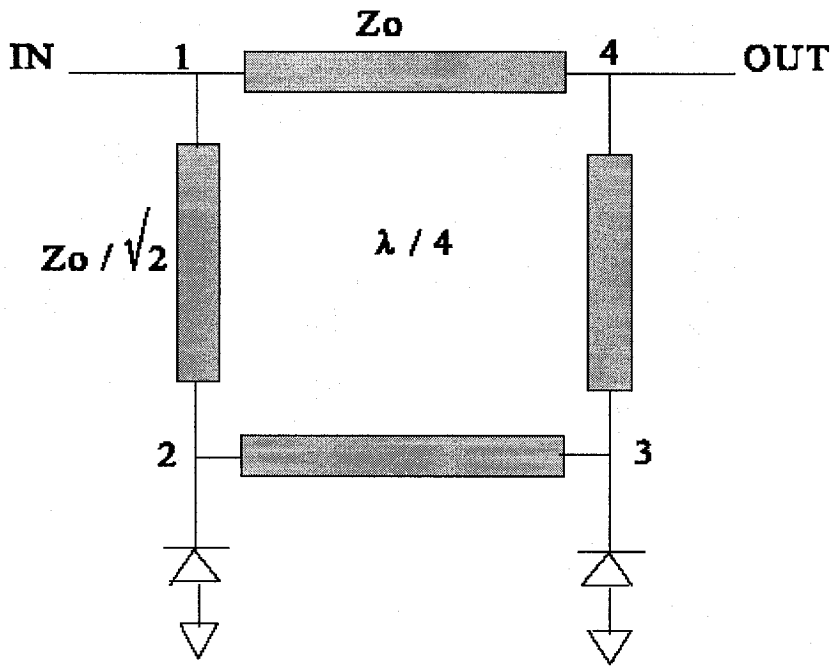


Figure 2- 2 Reflection phase shifter

We can describe the phase shifter principle as relations below:

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = -\frac{1}{\sqrt{2}} \begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} \tag{2.1.5}$$

$$a_2 = b_2 \angle \theta_2 \tag{2.1.6}$$

$$a_3 = b_3 \angle \theta_3 \tag{2.1.7}$$

If $\theta 2 = \theta 3 = \theta$ then

$$b_4 = -\frac{1}{\sqrt{2}}(a_2 + ja_3) = -\frac{1}{\sqrt{2}}(b_2 + jb_3)\angle\theta = ja_1\angle\theta = a_1 e^{j\varphi} \tag{2.1.8}$$

From (2.1.8), the output phase varies depends on terminal phase change θ.

A source of error for the reflecting phase shifters are the mismatches between the terminating impedance and the 3 - db hybrid coupler, which can contribute to large phase errors. A VSWR of 1.2 can cause a phase error of about ± 21 degrees. Therefore it is important not to have any mismatches between the 3 db hybrids and the reflecting elements. This mismatch phase error is very closely given by [26]

$$\varepsilon\varphi = 100°(VSWR - 1) \tag{2.1.9}$$

Figure 2-3 shows a reflection switch phase shifter where the bias of the diode is omitted.

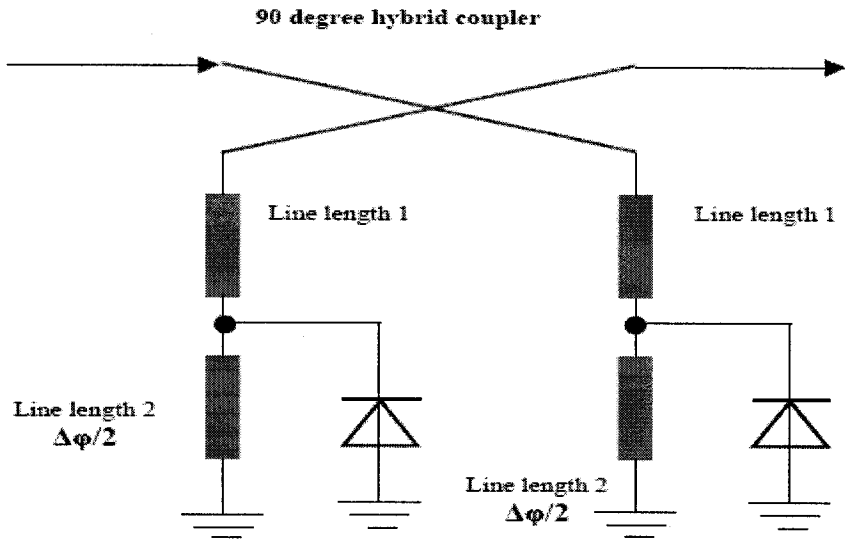


Figure 2- 3 Reflection switch phase shifter

It uses two PIN diodes to switch in or out the additional line lengths 2 to change the phase.

$$\Gamma_{on} = e^{j\varphi} \tag{2.1.10}$$

$$\Gamma_{off} = e^{j(\varphi \pm \varphi)} \tag{2.1.11}$$

For best return loss performance $\Gamma on = \Gamma off^*$ we can write:

$$\varphi = -(\varphi + \Delta\varphi) + 2k\pi \tag{2.1.12}$$

$$\varphi = k\pi - \frac{\Delta\varphi}{2} \tag{2.1.13}$$

or

$$\Delta\varphi = 2k\pi - 2\varphi \tag{2.1.14}$$

where $k = 0,1,2,3,\ldots$

Analog or variable reactance reflection phase shifter is shown in Figure 2-4

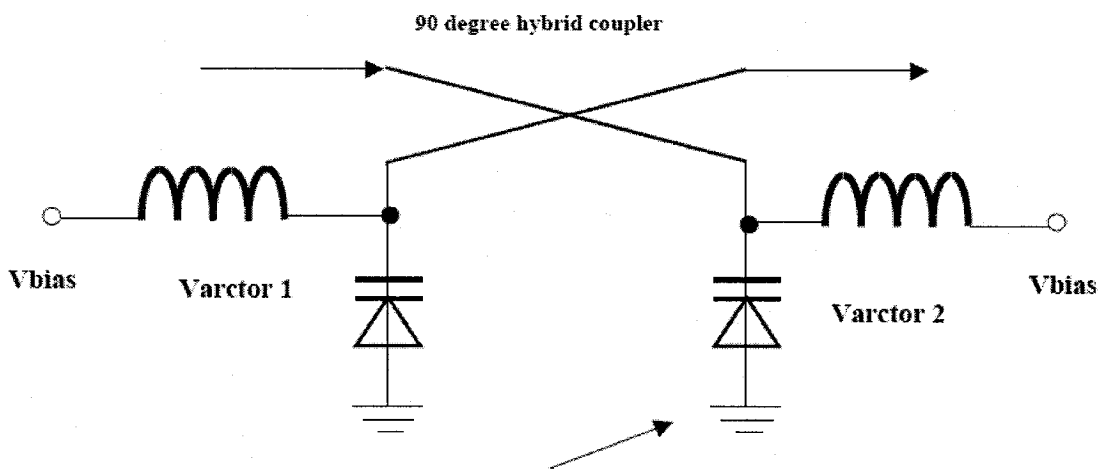


Figure 2- 4 Variable reactance reflection phase shifter using varactors as the variable reactance.

A varactor is a variable capacity. From passive microwave theory, it can be seen as a short transmission line, shown in Figure 2-5.

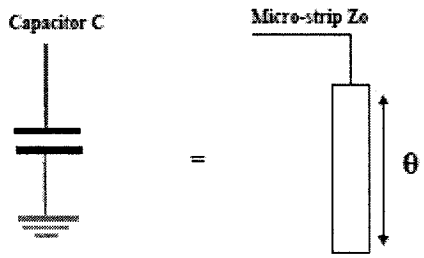


Figure 2- 5 Equivalent of electrical degree and shunt capacity

$$\omega C = \frac{\tan\theta}{Z_0} \tag{2.1.15}$$

shifted phase satisfy [18]:

$$\Delta\phi = 2\left[\arctan\left(\sqrt{r_c}\right) - \arctan\left(\frac{1}{\sqrt{r_c}}\right)\right] \tag{2.1.16}$$

where θ<90° and r_c is the tuning ratio of an ideally selected varactor

Loaded-Line Phase Shifters:

In loaded-line type phase shifter, a shunt reactance is added to the microstrip line (in the form of an inductor or capacitor) causing the incident signal to undergo a phase shift shown as Figure 2-6.

The shift phase is given by:

$$\Delta\phi = -\tan^{-1}\left(\frac{b}{2}\right) \tag{2.1.17}$$

For a single stage phase shift, the maximum $\Delta\Phi$ is 45°.

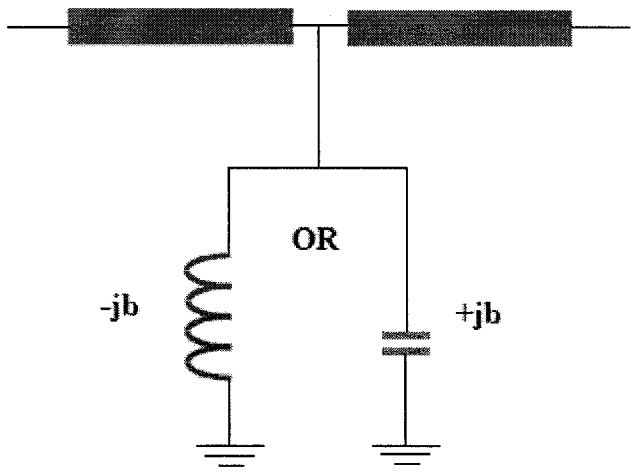


Figure 2- 6 Load line phase shifter

A continuously adjustable loaded line phase shifter is usually realized by periodically loading a high impedance transmission line with variable shunt capacitances as shown in Figure 2-7.

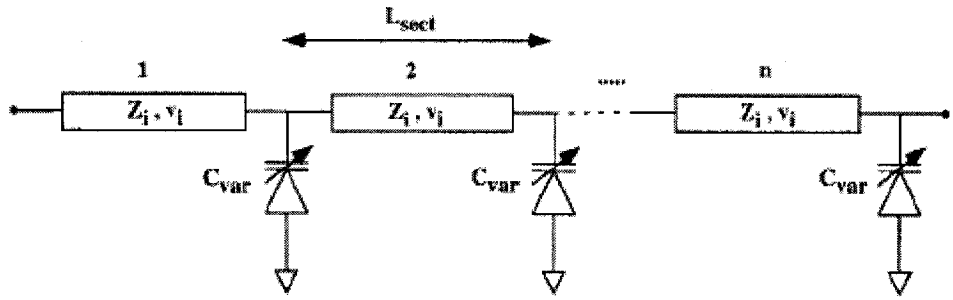


Figure 2- 7 Varactor loaded line phase shifter

Phase is changed by changing the varactors' capacities through modifying their DC bias. The circuit can be equivalently described by a Π network of low pass filters as it is shown in Figure 2-8. Each section can be seen as a Π type LC structure that can shift the phase in a small rang. The cascading of several sections allow for extending the phase

range.

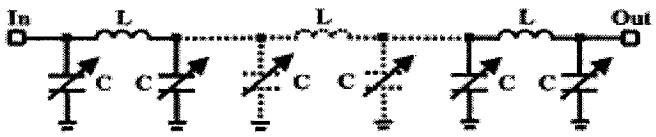


Figure 2- 8 LC equivalent circuits of distributed analog phase shifter

The matrix for the elements of the Π type low-pass structure, normalized to the characteristic wave impedance, is given by [26]

$$\begin{vmatrix} A & B \\ C & D \end{vmatrix} = \begin{vmatrix} 1 & 0 \\ jY_c & 1 \end{vmatrix} \begin{vmatrix} 1 & jX_L \\ 0 & 1 \end{vmatrix} \begin{vmatrix} 1 & 0 \\ jY_c & 1 \end{vmatrix} = \begin{vmatrix} 1-Y_cX_L & jX_L \\ jY_C(2-Y_CX_L) & 1-Y_CX_L \end{vmatrix} \tag{2.1.18}$$

where

$$X_c = \frac{1}{Y_c} = \frac{1}{wCZ_0} \tag{2.1.19}$$

and

$$X_L = \frac{1}{Y_L} = \frac{wL}{Z_0} \tag{2.1.20}$$

are the normalized impedances of the capacitance and inductance, respectively. The transmission term S21 of the scattering matrix can be calculated by

$$S_{21} = \frac{2}{2(1-Y_cX_L)+j\left(X_L+2Y_c-Y_c^2X_L\right)} \tag{2.1.21}$$

Thus, the corresponding transmission phase is

$$\varphi_{21} = \tan^{-1}\left[\frac{\left(Y_c^2X_L-X_L-2Y_c\right)}{2(1-Y_cX_L)}\right] \tag{2.1.22}$$

For a cascade of N sections, the phase is given by $N\varphi_{21}$.

In our project, we are looking for an analog phase shifter that can be continually adjusted to 360°, so possible types are given by a reflection or loaded line type phase shifter.

The reflection-type phase shifter uses a minimum number of components. From (2.1.16) we know that the phase shift range depends on the tuning ratio r_c, but in practice, most varactors can only provide limited r_c. Only varactor diodes with special doping profiles are usually able to achieve large tuning ranges. However, most of these devices have low Q. Therefore, the single varactor technique is not very useful except in limited circumstances where loss is not a huge concern or the required phase shift is small. In [19], a technique is described for adding the admittances of two diodes to double the phase shift. This was accomplished by using a $\lambda/4$ transmission line of appropriate impedance. In [20], a reflective load consisting of two separate varactor circuits resonating at different frequencies was used to extend the phase shift range of low tuning varactors. However, they have some drawback. Firstly they have narrow bandwidth; secondly, mismatches between the terminating impedance and the 3-dB coupler cause large phase errors.

The loaded line analog phase shifter is attractive because of its simple fabrication and wide bandwidth. It is created by adding tuneable capacitance to a transmission line. Adjusting the capacitance alters the phase velocity of the signal propagating along the line, varying its electrical length, and therefore the phase shift. The main draw back of this type phase shifter is its larger size compared to a reflection type one. Secondly, when the

capacitances change, the characteristic impedance of the transmission line changes, and result in impedance mismatch as the circuit is tuned.

Comparing the two types of phase shifter we prefer the loaded line one. We need to design wide bandwidth and allow for an easy implementation, whereas we don't have to respect any restrictions in terms of circuit size, and we can make use of a special design to reduce impedance mismatch to an acceptable value.

2.2. Varactor Loaded line phase shifter

As mentioned above, analog loaded-line phase shifters use tuneable reactance. In general, tuneable inductors are more difficult to implement than tuneable capacities. So, such phase shifters are mostly implemented based on variable capacity. Different methods can be used to realize it. Ferrites phase shifter is a type that changes phase by changing permeability μ. It has the advantage of being smaller, having less loss, and more power efficient. The main drawback is that in order to tune the ferrite material, strong magnetic fields must be generated and coils are required that have high bias voltages. GaAs MMIC technology offers the broadest range of options for the design of phase shifter circuits, but they are expensive. MEMS (micro-electro-mechanical systems) technology uses advanced thin-film processing techniques to realize miniaturized mechanical systems. This technology is attractive for low-loss and high-frequency applications. However its implementation needs a large number of processing steps. All these methods are not easy to implement and costly. In practice, varactor diode is the first choice.

A varactor diode is a device that is processed to capitalize on the properties of the depletion layer of a P-N diode. Under reverse bias, the carriers in each region (holes in the P type and electrons in the N type) move away from the junction, leaving an area that is depleted of carriers. Thus a region that is essentially an insulator has been created, and can be compared to the classical parallel plate capacitor model. The effective width of this depletion region increases with reverse bias, and so the capacitance decreases. Thus the depletion layer effectively creates a voltage dependent junction capacitance, which can be varied between the forward conduction region and the reverse breakdown voltage.

The property of capacitance change is utilized to achieve a change in the frequency and/or the phase of an electrical circuit.

2.2.1 Varactor model and parameters

A simple mathematical model of a packaged varactor diode is shown below.

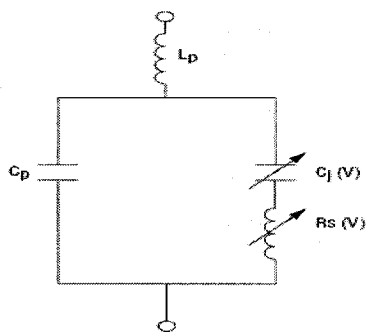


Figure 2- 9 Varactor diode model

C_j *(V)* is the variable junction capacitance of the diode and R_s *(V)* is the variable series resistance of the diode. C_p is the fixed parasitic capacitance arising from the installation of

the die in a package. Contributors to the parasitic capacitance are the package material, geometry, and the bonding wires or ribbons. These factors also contribute to the parasitic inductance L_p. The contribution to the series resistance from the packaging is very small and may be ignored. In general, there are three types of varactors: abrupt junction, frequency linear and hyperabrupt junction varactors. The C_j *(V)* characteristics of different types of varactors are shown as Figure 2-10 [18].

for abrupt junction varactor:

$$C_j = \frac{C_{j0}}{\left(1+\frac{V_R}{\Phi}\right)^{\gamma}} \tag{2.2.1}$$

for frequency Linear varactor:

$$C_j = \frac{C_{j0}}{(1+V_R)^2} \tag{2.2.2}$$

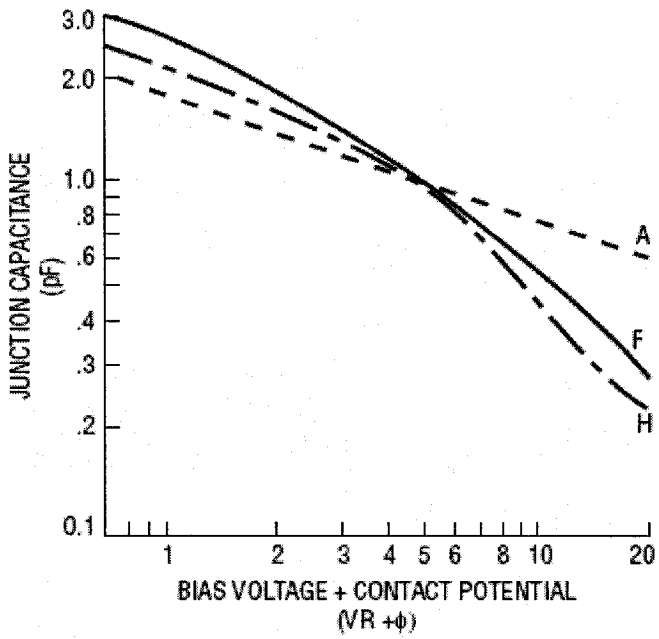


Figure 2- 10 Varactor C-V Curves

for hyperabrupt junction varactor:

$$C_j = \frac{C_{j0}}{\left(1+\frac{V_R}{\Phi}\right)^{\gamma}} \tag{2.2.3}$$

where γ is the so-called power law of the junction or slope factor and γ = 0.5 for abrupt junction, $\gamma > 0.5$ for hyperabrupt junction. Φ is the contact potential (Φ = 0.7V for Si, Φ = 1.1 V for GsAs). C_{j0} is the junction capacitance when the DC bias V_R=0.

Cutoff frequency

The series resistance exists as a consequence of the remaining undepleted semiconductor resistance, a contribution due to the die substrate, and a small lead and package component, and is foremost in determining the performance of the device under

RF conditions. As normally RC circuits, it exits a cutoff frequency.

The cutoff frequency is an important parameter of varactor diodes. The varactor diode should always work below the cutoff frequency. It is a variable parameter that changes with the bias voltage, so manufactures do not give it directly, but give a quality factor Q instead. The quality factor Q can be calculated as:

$$Q = \frac{X_c(V)}{R_s(V)} = \frac{1}{\omega C_j(V) R_s(V)} \tag{2.2.4}$$

The cutoff frequency is

$$f_c(V) = \frac{1}{2\pi R_s(V) C_j(V)} \tag{2.2.5}$$

So Q can be determined from (2.1.4) and (2.1.5) as

$$Q = \frac{f_c}{f} \tag{2.2.6}$$

In general the manufacture specifies the Q as quart volt, $f_c(4v)$ and normalize to f=50MHz, so the Q becomes

$$Q = \frac{f_c(4v)}{50MHz} \tag{2.2.7}$$

Figure.2-11 shows the characteristics Q(V) of different types of varactors [18]

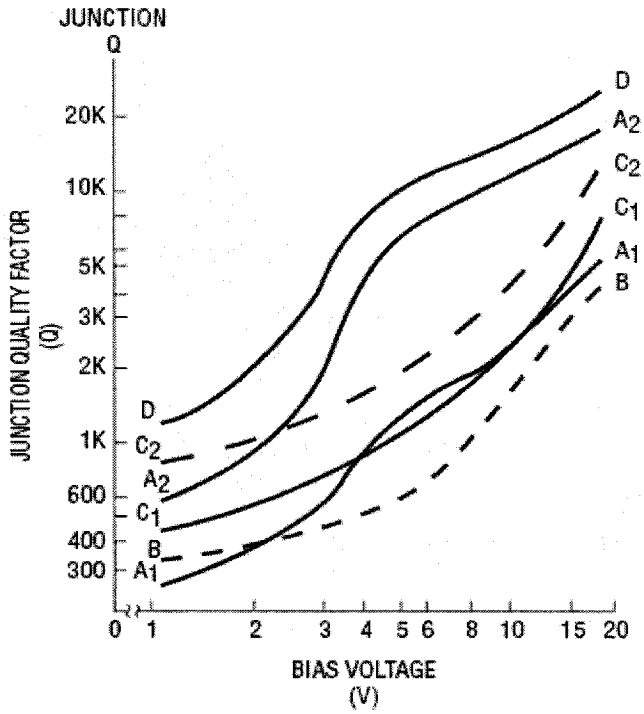


Figure 2- 11 Varactor Q-V curves.

A1 = Abrupt Junction Ratio -10

A2 = Abrupt Junction Ratio -5

B = Ion Implanted Hyperabrupt Ratio -5

C1 = Controlled Epi Linear, Ratio -20

C2 = Controlled Epi Linear, Ratio -8

D = GaAs Abrupt, Ratio -6

Capacity tuneable ratio

Capacity tuneable ratio is a very important parameter. It determines the phase shift range and affects the *Q* factor, which is related to cut off frequency and insertion loss. It is

defined as (2.2.8).

$$r_c = \frac{C_j^{\max}}{C_j^{\min}} \tag{2.2.8}$$

Resonance frequency

From Figure 2-9, we can see that L_p, C_j and C_p create a resonant circuit. The resonant frequency is given by:

$$f_r = \frac{1}{2\pi\sqrt{L_p(C_j + C_p)}} \tag{2.2.9}$$

At resonance, the varactor acts like a short circuit, so the signal cannot propagate any more. Therefore, the working frequency should less than *fr*.

Linear variation of frequency with applied control voltage.

Many applications require a linear or nearly linear variation of frequency with applied control voltage. Figure 2-12 shows the frequency versus bias voltage curves of different types of varactors.

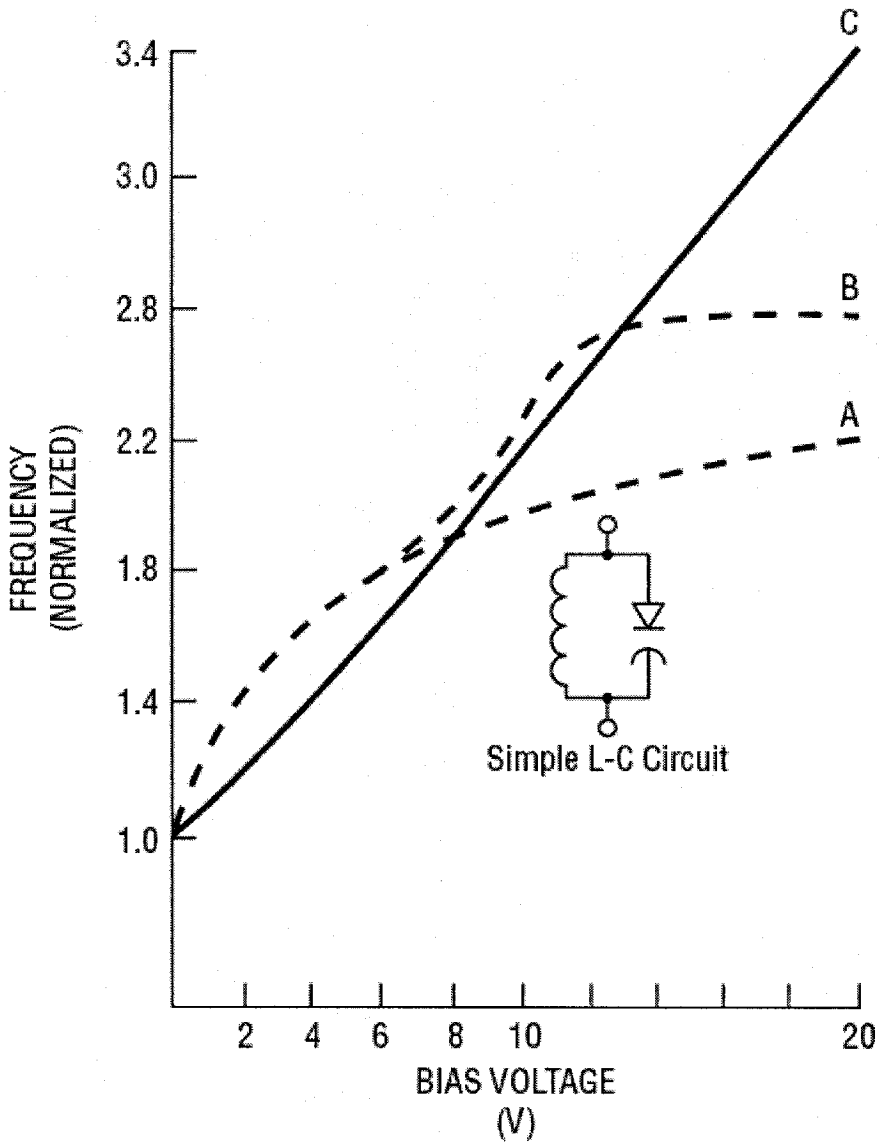


Figure 2- 12 Tuning varactor frequency-voltage curves

A = Abrupt Junction

B = Ion Implanted Hyperabrupt

C = Controlled Epi Linear

2.2.3 Design equation

The distributed phase-shifter circuit shown in Figure 2-7 consists of a high-impedance transmission line periodically loaded with spacing varactors. We can define a unit cell for this periodic structure, which includes a section of transmission line and a shunt variable capacitor to ground. The transmission-line section can be approximated as a lumped inductance and capacitance, as shown in the equivalent circuit in Figure 2-13.

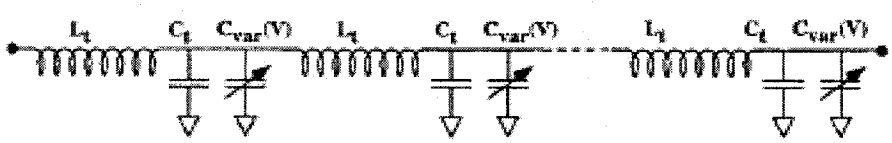


Figure 2- 13 Circuit equivalent for the varactor diodes loaded line

The discontinuities created by the additional shunt elements result in small reflections from each element as the signal propagates along the circuit. As the frequency of the signal approaches a certain value, the phases of the incident and reflected signal interfere destructively, preventing forward propagation of the wave. When the signal cannot propagate, the transmission loss increases, and the signal is reflected back towards the source. The frequency where the signal is completely prevented from forward propagation is called the Bragg frequency, after a similar phenomenon in crystalline solids. The relationship between this frequency, $f_{Bragg,}$ and the circuit model elements is defined in equation (2.2.10) [21]

$$f_b = \frac{1}{\pi\sqrt{L_t(C_t + C_{\text{var}})}} \qquad (2.2.10)$$

where

$$L_t = \frac{l_{sect}}{v_0} Z_0 \tag{2.2.11}$$

and

$$C_t = \frac{l_{sect}}{v_0 Z_0} \tag{2.2.12}$$

are the inductance and capacitance per unit cell, and Z_0 and v_0 are the impedance and phase velocity on the high-impedance line, respectively. For frequencies well below the Bragg frequency, the periodically loaded line may be treated as a synthetic transmission line as shown in Figure 2-14.

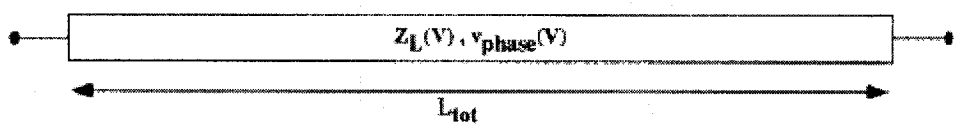


Figure 2- 14 Synthetic transmission line with voltage-dependent characteristic impedance ($Z_L(V)$) and phase velocity ($v_{phase}(V)$).

The capacitance per unit length has been increased due to the periodic loading. The inductance per unit length for this synthetic line remains unchanged from the value of the original unloaded line. Since the loading capacitors are voltage dependent, the properties of this synthetic transmission line, such as its characteristic impedance and phase velocity, are voltage dependent.

$$Z_L(\mathrm{V}) = \sqrt{\frac{L}{\left(C + C_{\mathrm{var}}(V)/l_{sec\,t}\right)}} \tag{2.2.13}$$

$$v_{phase}(V) = \frac{1}{\sqrt{L\left(C + C_{\mathrm{var}}(V)/l_{sec\,t}\right)}} \tag{2.2.14}$$

$$L = \frac{Z_0}{v_0} \tag{2.2.15}$$

$$C = \frac{1}{Z_0 v_0} \tag{2.2.16}$$

We can define:

$$x = \frac{C_{\mathrm{var}}^{\max}/l_{sec\,t}}{C} \tag{2.2.17}$$

$$r_c = \frac{C_{\mathrm{var}}^{\min}}{C_{\mathrm{var}}^{\max}} \tag{2.2.18}$$

The parameter r_c is just the ratio of the minimum-to-maximum varactor capacitance. The loading factor is the ratio of maximum varactor capacitance per unit length to the transmission line capacitance C per unit length. We assume that the varactor shows its maximum capacitance when the loaded line is matched to a 50 Ω system. From the above condition we obtain:

$$Z_0 = 50\sqrt{1+x} \tag{2.2.19}$$

For the spacing l_{sec}, when the varactor shows maximum capacitance, the Bragg frequency is at its minimum value:

$$f_b^{\min} = \frac{v_0}{\pi l_{sect}\sqrt{1+x}} \tag{2.2.20}$$

$$C_{\text{var}}^{\max} = \frac{1}{50 f_b^{\min}} \frac{x}{1+x} \tag{2.2.21}$$

At any given frequency, the maximum possible differential phase shift that can be obtained from a single section is given by

$$\Delta\Phi = 2\pi f \frac{l_{sect}}{v_0}\left(\sqrt{1+x} - \sqrt{1+xr_c}\right) \tag{2.2.22}$$

Thus,the number of sections required for a 360° phase shifter at frequency f is given by:

$$N = \frac{2\pi}{\Delta\phi} \tag{2.2.23}$$

The total circuit loss is infected by two parameters: diode loss and transmission-line loss. For a CPW line loaded with varactor diodes, the total loss IL is given by:

$$IL = N\pi \frac{f^2}{f_s} C_{\text{var}}^{\max} Z_L(v) + N l_{sect}\alpha \frac{Z_0}{Z_L(v)} \tag{2.2.24}$$

$$f_s = \frac{1}{2\pi r_s C_{\text{var}}^{\max}} \tag{2.2.25}$$

where f is the working frequency, f_s is the diode cutoff frequency, r_s is the series resistance of the diode, α is the transmission-line loss (dB/in).

The total circuit loss depends on the loading effect as shown in Figure 2-15 [21]. The optimum performance of insertion loss is achieved for a value of x around 1

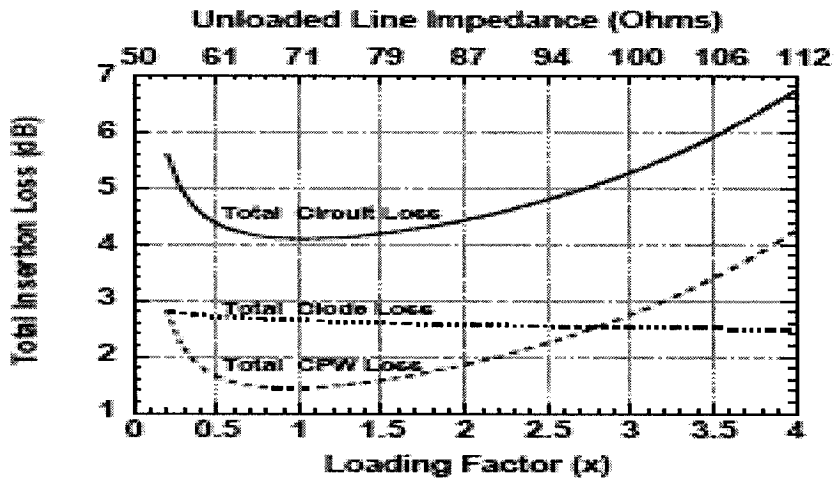


Figure 2- 15 Effect of loading factor on total circuit loss

2.3. Design of phase shifter

As shown in Figure 2-7, the loaded line phase shifter consist of a high-impedance transmission line periodically loaded with spacing varactors. So the design of such a phase shifter includes: the selection of suitable varactors, the design of the transmission line impedance parameter, and the distance of the varactors to be inserted.

The phase shifter in our project needs to work at frequency of 5.8 GHz with a bandwidth of 200 MHz. Moreover, we need to optimize insertion loss, allow for linear phase tuning and minimize return loss.

2.3.1 Varactor selection

The design frequency is 5.8GHz, so we assume the varactor diode cut-off frequency f_c is 8GHz, whereas the resonant frequency f_r and minimum Bragg frequency f_b are larger

than 12GHz. The loading factor is assumed to x=1. Thus according to (2.2.1) the varactor should satisfy:

$$C_{\text{var}}^{\max} = C_j + C_b \le \frac{1}{50*12*10^9} * \frac{1}{1+1} = 0.83*10^{-12} \quad \text{F} \qquad (2.3.1)$$

From (2.2.9) we obtain:

$$L_p \le \frac{1}{(2*\pi*f_r)^2 * C_{\text{var}}^{mar}} = 2.12*10^{-10} \quad \text{H} \qquad (2.3.2)$$

To select a suitable varactor, we should consider: the range of frequencies the circuit must operate at and hence an appropriate capacitance range; the available bias voltage; and the required frequency response.

A). *C-V* curve. The *C-V* curve summarizes the range of useful capacitance. Different junction profiles can be produced that exhibit different capacitance-voltage (*C-V*) characteristics. The abrupt junction type shows a small range of capacitance due to its diffusion profile, and as a consequence shows high Q and low distortion, while the hyperabrupt type allows a larger change in capacitance for the same range of reverse bias. So-called hyper-hyperabrupt, or octave tuning variable capacitance diodes show a large change in capacitance for a relatively small change in bias voltage. This type of varactor is useful in the case that bias voltage is limited. In our case, we prefer an abrupt junction type varactor to get high Q and low distortion.

B) The capacitance ratio. It is a useful parameter that shows how quickly the capacitance changes with applied bias voltage. The higher the ratio, the wider the range of the phase shifter, but the smaller Q as it is shown in Figure 2-11.In our case the Q is more important to get lower loss and therefore we select a varactor with lower ratio.

C) The quality factor *Q*. In general, it is preferable to select a varactor with high *Q*. However the minimum required value for *Q* at a frequency of 50 MHz can be obtained from (2.2.7) to Q=12000/50=240. Thus, we should select a varactor that shows a *Q* larger than 240 at 50MHz.

D) The reverse breakdown voltage V(BR). *V(BR)* is also a criteria for device selection, as the maximum V_R corresponds to the minimum achievable capacitance. We select V(BR)=30V.

E) Device package. At microwave frequencies, packaging is an important aspect we should consider. As (2-3-1) and (2-3-2) indicate, the capacitance Cp and the inductor Lp should be small enough to get good response at high frequency.

Package parasitic are unwanted electrical and mechanical attributes that result from the physical construction of the package. Package types have various combinations of parasitic, which limit circuit performance in different ways.

Table 2-1 shows different microwave diode packages and their maximum frequencies [22].

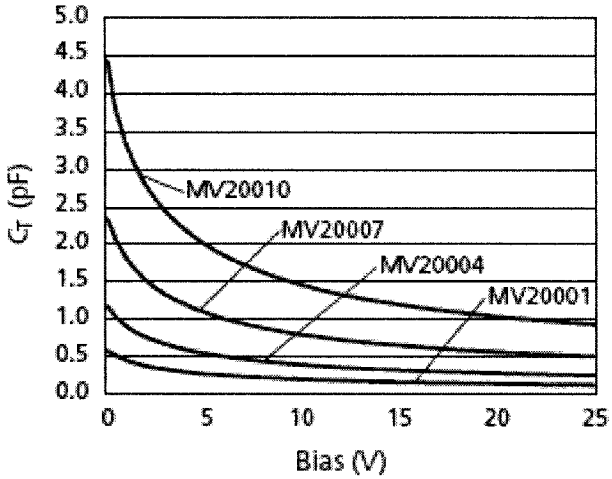
Pkg. Type	Lp	Cp	Rs	θj	Cost	Max Freq.	Hermetic	Comments
Ceramic	Excellent	Excellent	Excellent	Excellent	High	18 GHz	Yes	All products available
MELF	Good	Fair	Excellent	Very Good	Moderate	2 GHz	Yes	Only select PIN diodes available
MMSM	Very Good	Very Good	Good	Very Good	Low	8 GHz	No	Only select PINs and varactors
EPSM	Good	Good	Good	Good	Moderate	6 GHz	No	All products available
Glass Axial	Fair	Good	Good	Poor	Moderate	1.5 GHz	Yes	Many products available
Plastic	Poor	Fair	Fair	Poor	Low	2 GHz	No	Only select PINs, varactors & Schottkys
Stripline	Good	Good	Good	Fair	Moderate	8 GHz	Yes or No	All products available

Table 1 · Microwave diode package comparisons.

Table 2- 1 Different microwave diode package

Ceramic packages are the best performing and most expensive microwave packaging types available. They are hermetic and usually used in military and space applications. They combine low parasitic inductance and low parasitic capacitance and can have superior thermal resistance characteristics as well. Most products are available in ceramic packages. MMSM packages (Microwave Monolithic Surface Mount) combine the attributes of excellent microwave performance, surface mount convenience, and economy pricing, but only some products are available in this outline. Stripline packages for microwave frequency are usually also ceramic and can be completely hermetic or have epoxy encapsulation. They combine low parasitic inductance, low parasitic capacitance and are designed specifically for stripline or microstrip construction. They can, however, have high thermal resistance and are not the best choice for applications which will result in high device dissipation. Enhanced Performance Surface Mount (EPSM™) packages offer consistent performance for applications up to 6 GHz. Both parasitic inductance and parasitic capacitance are very low compared to conventional plastic injection molded surface mount packages. Thermal resistance is moderate but is also superior to plastic. Additionally there are a wide range of outlines from which to choose, and most products offered are available in EPSM. All of these four types package can be used at our design frequency of 5.8GHz.

Considering A) to E) we select the **MDT** GaAs abrupt tuning varactor.



Typical Total Capacitance vs. Bias

Figure 2- 16 MDT abrupt junction varactor C-V curve

High Q Abrupt Tuning Varactors (Specifications @ 25°C)

Gamma = 0.5

Part Number	C_T[4] ± 10% (pF)[1, 2, 4]	$\frac{C_T^0}{C_T V_{BR}}$ Typ.[3]	V_{BR} @ 10 µA	Typical Q @ -4 V[2]
MV20001	0.3	2.4	15	8000
MV20002	0.4	2.6	15	7500
MV20003	0.5	2.8	15	7000
MV20004	0.6	2.9	15	6500
MV20005	0.8	3.0	15	6000
MV20006	1.0	3.1	15	5700
MV20007	1.2	3.2	15	5000
MV20008	1.5	3.3	15	5000
MV20009	1.8	3.4	15	5000
MV20010	2.2	3.4	15	4000
MV21001	0.3	2.8	30	8000
MV21002	0.4	3.1	30	7500
MV21003	0.5	3.4	30	7000
MV21004	0.6	3.6	30	6500
MV21005	0.8	3.8	30	6000
MV21006	1.0	4.0	30	5700
MV21007	1.2	4.2	30	5000
MV21008	1.5	4.3	30	5000
MV21009	1.8	4.5	30	5000
MV21010	2.2	4.6	30	4000

[1] Capacitance is measured at 1 MHz using a shielded fixture.
[2] Measured by DeLoach Technique and referenced to 50 MHz.
[3] Tightened tolerances available upon request.
[4] Package parasitics are included in above specifications. The contributions of package capacitance add to the overall total capacitance and will vary depending upon package style selected. The values for package capacitance, C_P, can be made available upon request.
[5] The capacitance ratio is calculated using C_P = 0.15 pF. Ratios will vary depending upon case style selection.

Figure 2- 17 MDT abrupt junction varactor electrical characteristics

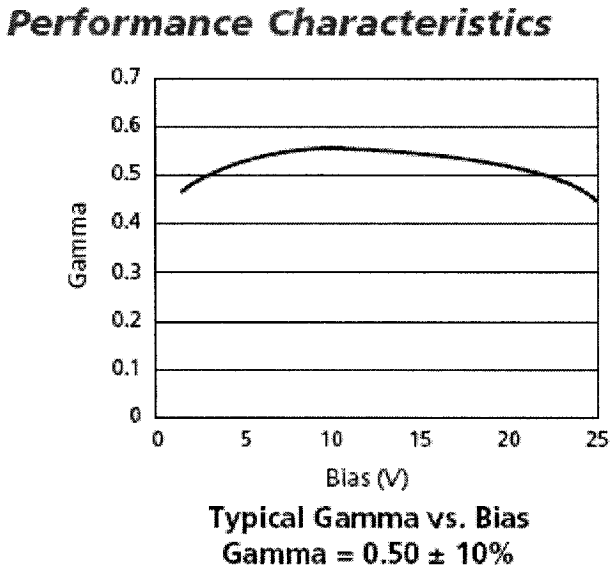


Figure 2- 18 MDT abrupt junction varactor performance characteristics

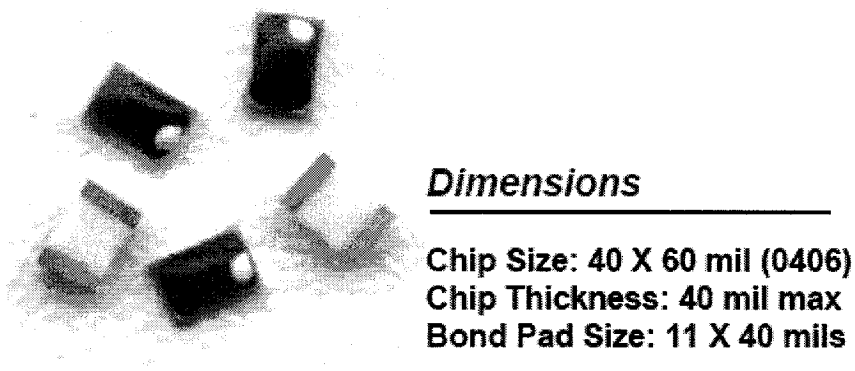


Figure 2- 19 MDT abrupt junction varactor chip-on-board package

From Figure 2-16 and Figure 2-17 we observe that a higher capacitance ratio leads to a lower Q factor and vice versa. For our purpose, we select the varactor MDT21002-46. Its COB package has a parasitic inductance of 0.4 nH and a parasitic capacitance of 0.06 pF.

With the above value of *Lp* (2.3.2) cannot be satisfied, thus the maximum desired

capacitance $C_{\text{var}}^{\max}$ has to be reduced:

$$C_{\text{var}}^{\max} \le \frac{1}{(2*\pi*f_r)^2 * L_p} = 0.44*10^{-12} \tag{2.3.3}$$

In that case, the bias can be regulated from 4V-30V, which gives a capacitance ratio of around 3.

2.3.2 Impedance of loaded line

From (2.2.19) we obtain Z_0=70.71 Ω. We select a substrate of ε_r = 3.05 and the thickness h = 20 mil. The formula according to [23] or any CAD software yield line widths of 49.5mil (ε_{eff}= 2.469) and 27.3mil (ε_{eff}= 2.362) for the impedances Z_0 = 70.71 Ω and Z_0 = 50 Ω.

For $\frac{W}{h}$ <1

$$Z_0 = \frac{60}{\sqrt{\varepsilon_{eff}}} \ln\left[\frac{8h}{W} + \frac{W}{4h}\right] \tag{2.3.4}$$

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\left(1 + 12\frac{h}{W}\right)^{-\frac{1}{2}} + 0.04\left(1 - \frac{W}{h}\right)^2\right] \tag{2.3.5}$$

For $\frac{W}{h}$>1

$$Z_0 = \frac{120\pi / \sqrt{\varepsilon_{eff}}}{\frac{W}{h} + 1.393 + 0.667\ln\left(\frac{W}{h} + 1.444\right)} \tag{2.3.6}$$

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + 12\frac{h}{W}\right)^{-\frac{1}{2}} \tag{2.3.7}$$

2.3.3 Space between varactors

From (2.2.24) we obtain

$$l_{sect} = \frac{v_0}{\pi f_b^{\min} \sqrt{1+x}} \tag{2.3.8}$$

$$v_0 = \frac{c}{\sqrt{\varepsilon_{eff}}} = 1.952 * 10^8 \left(m/s\right) \tag{2.3.9}$$

where c is the velocity of light of around $3*10^8$ (m/s)

For x=1 and f_b =12 GHz we obtain a line length of l_{sec} =3.66 mm

Thus using (2.2.22) we get a phase difference of $\Delta\Phi$=0.4 radian.

Furthermore, from (2.2.23), the number of required stage N is obtained to16.

2.3.4 ADS simulation and optimization

The above design is done assuming a value of x = 1. However to optimize the result, we need to compare with the other values of x based on the same varactor characteristics. Use the formulas above we can obtain different parameters at different x as shown in table 2-2.

x	Z0	Eeff	W	v0	*lsect*	ΔΦ	N	
0.5	61.24	2.406	35.42	1.934	4.19	0.2813		23
1.0	70.71	2.362	27.30	1.952	3.66	0.40		16
1.2	74.16	2.347	24.91	1.958	3.50	0.4311		15
1.5	79.06	2.328	21.92	1.966	3.30	0.4671		14
3.0	100.00	2.261	12.92	1.995	2.65	0.5618		12
5.0	122.47	2.210	7.41	2.018	2.19	0.6119		11

Table 2- 2 Different parameters with different loading factor x respectively

Figure 2-20 shows the varactor ADS simulation model. In all our following simulations we use this model with values of l_s=0.4, R_s=5, C_p=0.06. Figure 2-21 shows a design of 16-stages phase shifter. A simulation of the phase shifter using this model by varying x is performed. The results are shown in Figure 2-22 to 2-26.

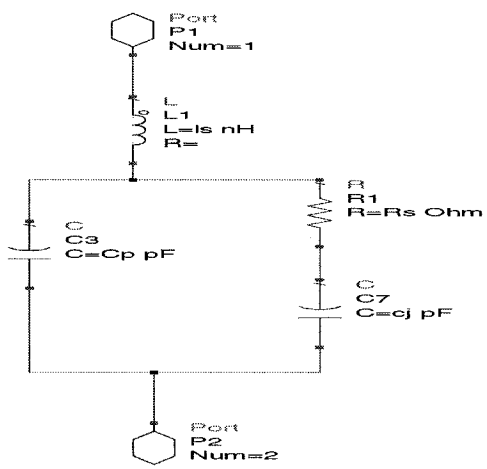


Figure 2- 20 Varactor ADS model

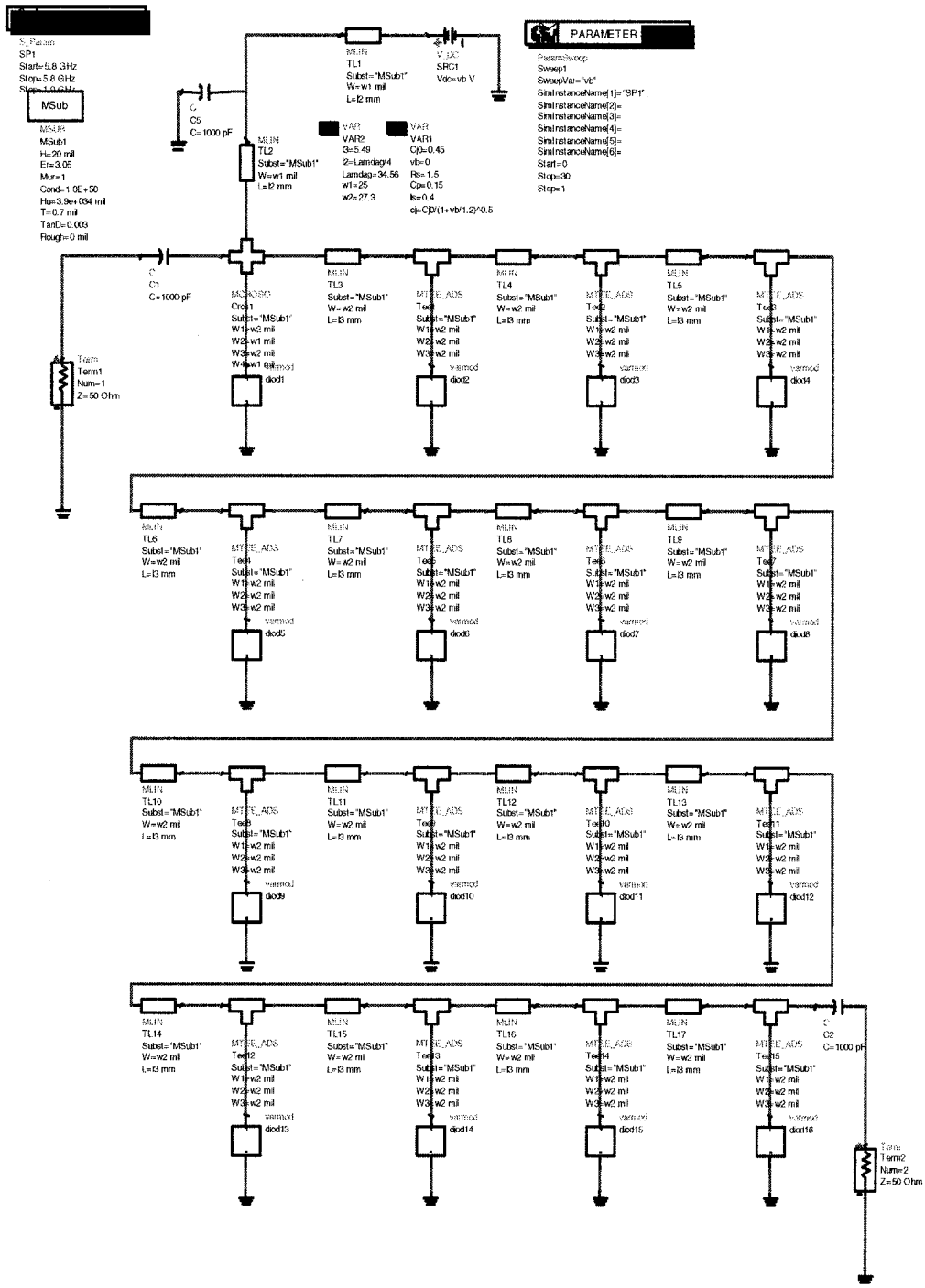


Figure 2- 21 16-stages phase shifter

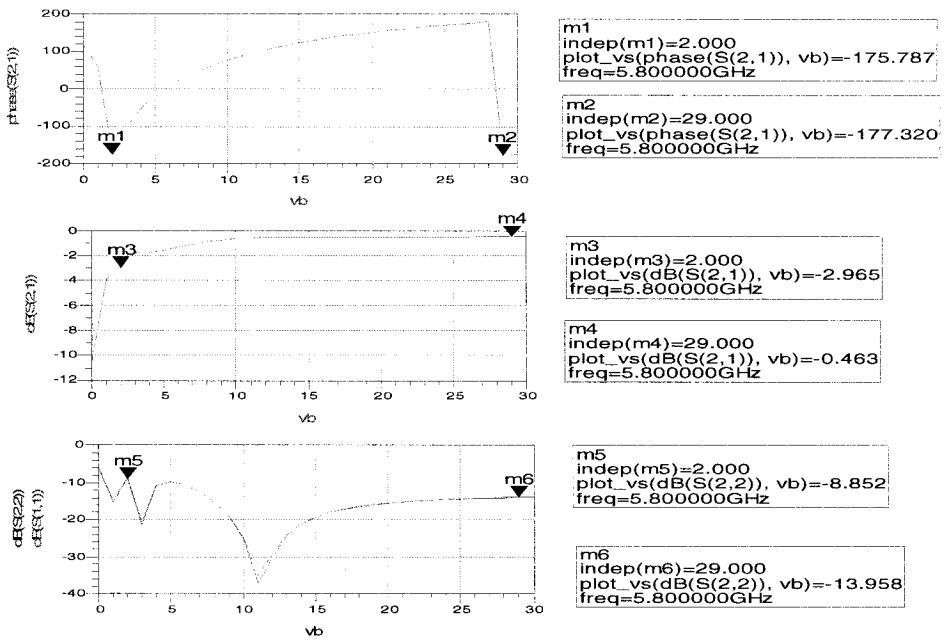


Figure 2- 22 16-stages phase shifter ADS simulation result (x=1)

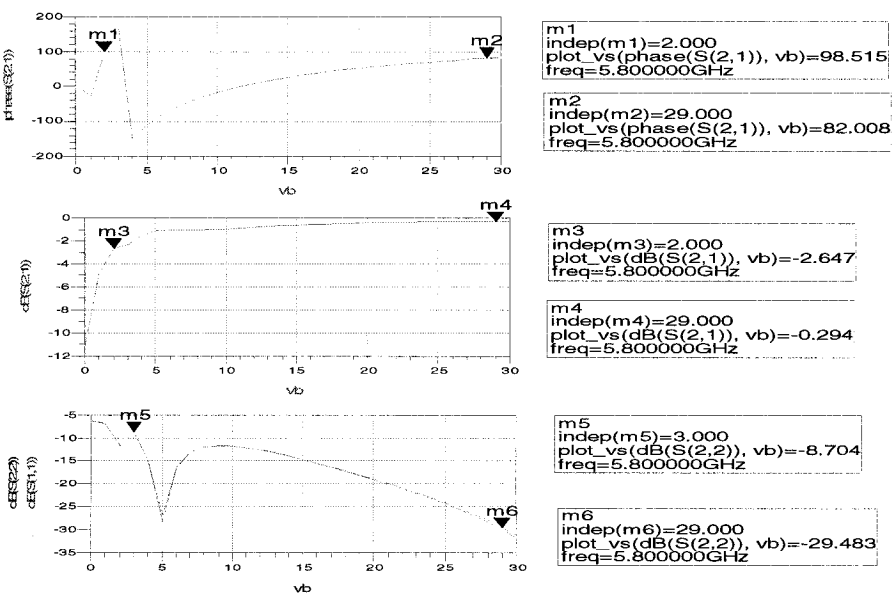


Figure 2- 23 16-stages phase shifter ADS simulation result (x=0.5)

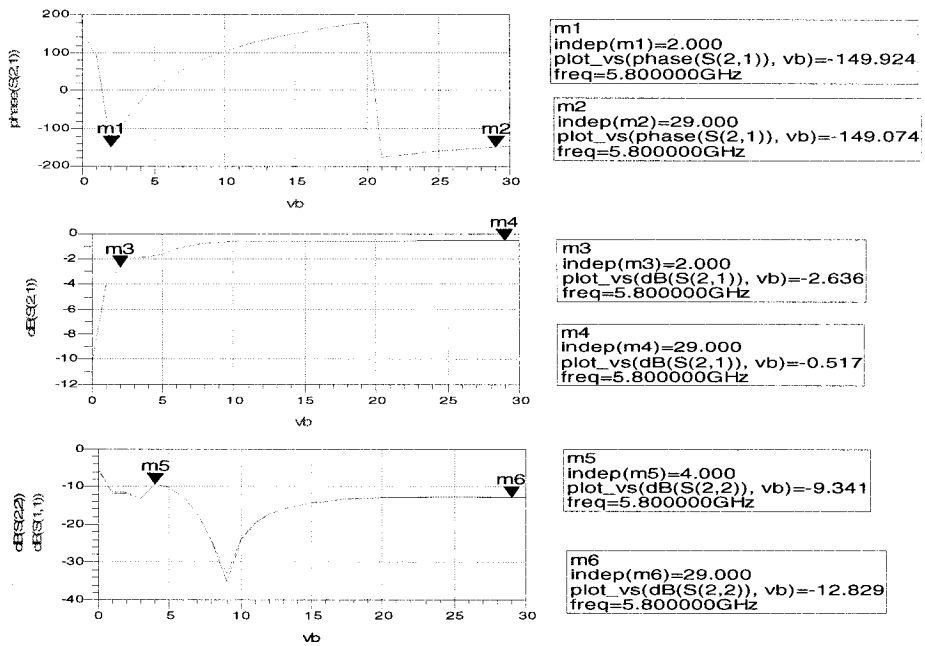


Figure 2- 24 16-stages phase shifter ADS simulation result (x =1.2)

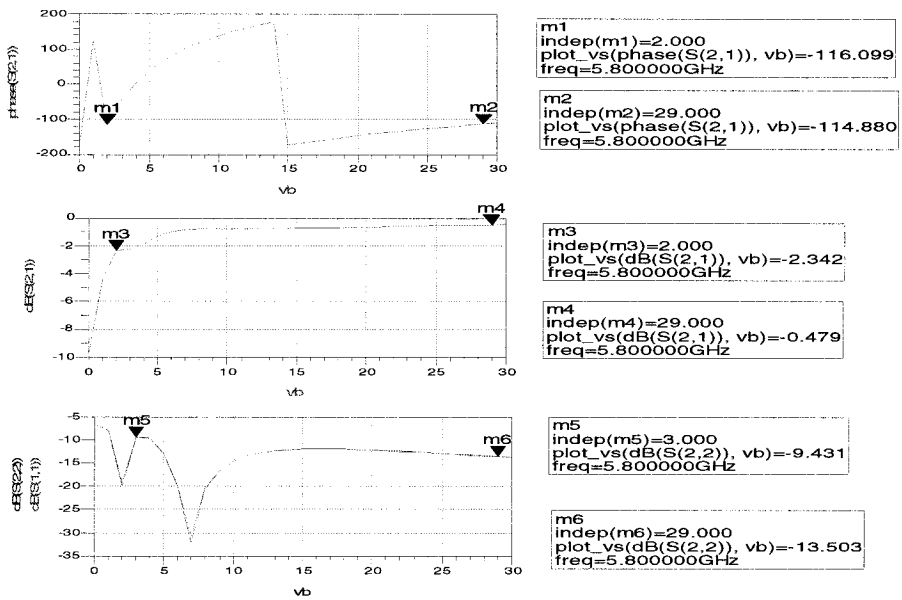


Figure 2- 25 16-stages phase shifter ADS simulation result (x =1.5)

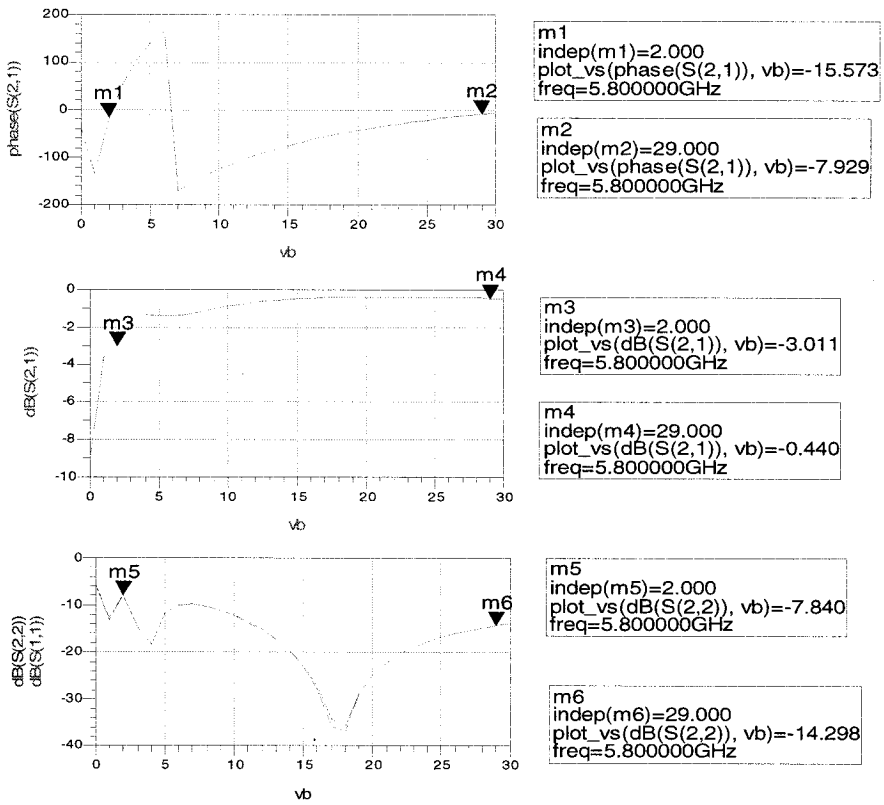


Figure 2- 26 16-stages phase shifter ADS simulation result (x = 3)

Comparing the simulation results, we observe that a loading factor of x=1.5 results in optimum S parameters. Therefore our phase shifter design will be built on this result.

Now we slightly change l_{sect} or Z_0 (the line W) to track the change in simulate results.

By decreasing l_{sect} from 3.3 to 3.0, we observe an increase of insertion loss and a decreased phase range as shown in Figure 2-27. Similarly, increasing l_{sect} to 3.6, insertion loss and return loss decrease, as it can be seen from Figure 2-28. The insertion loss and return loss increased. Changing W from W=21.92 to W=20, increase insertion loss, while

a value of W=24 cause a decreased phase range, as it is shown in Figure 2-29 and Figure 2-30. So the designed l_{sect} and Z_0 are the optimized value.

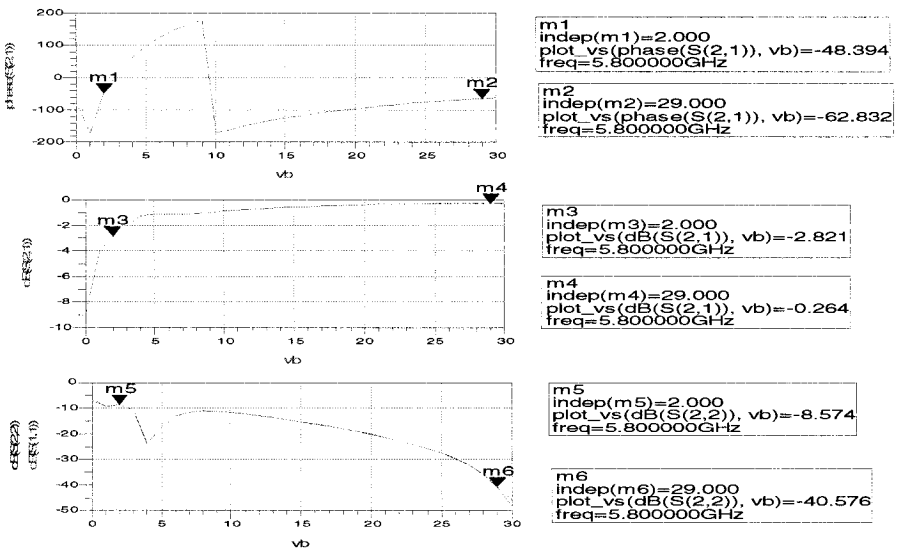


Figure 2- 27 16-stages phase shifter ADS simulation result (x =1.5), reduced l_{sect}

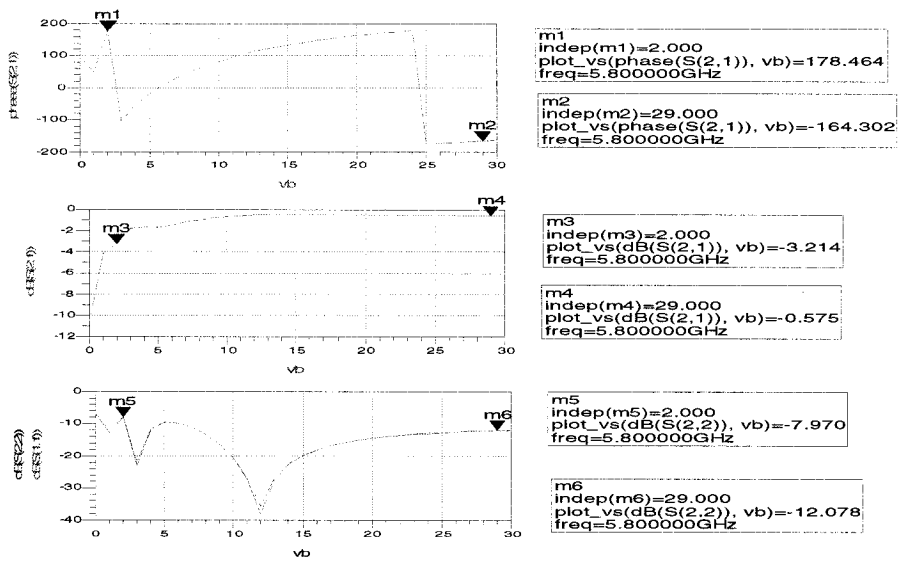


Figure 2- 28 16-stages phase shifter ADS simulation result (x =1.5), increduced l_{sect}.

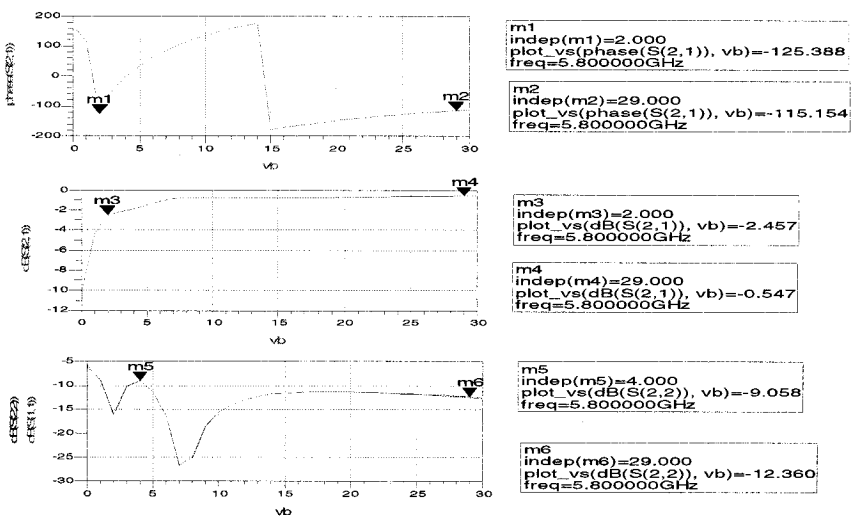


Figure 2- 29 16-stages phase shifter ADS simulation result (x =1.5), reduced W.

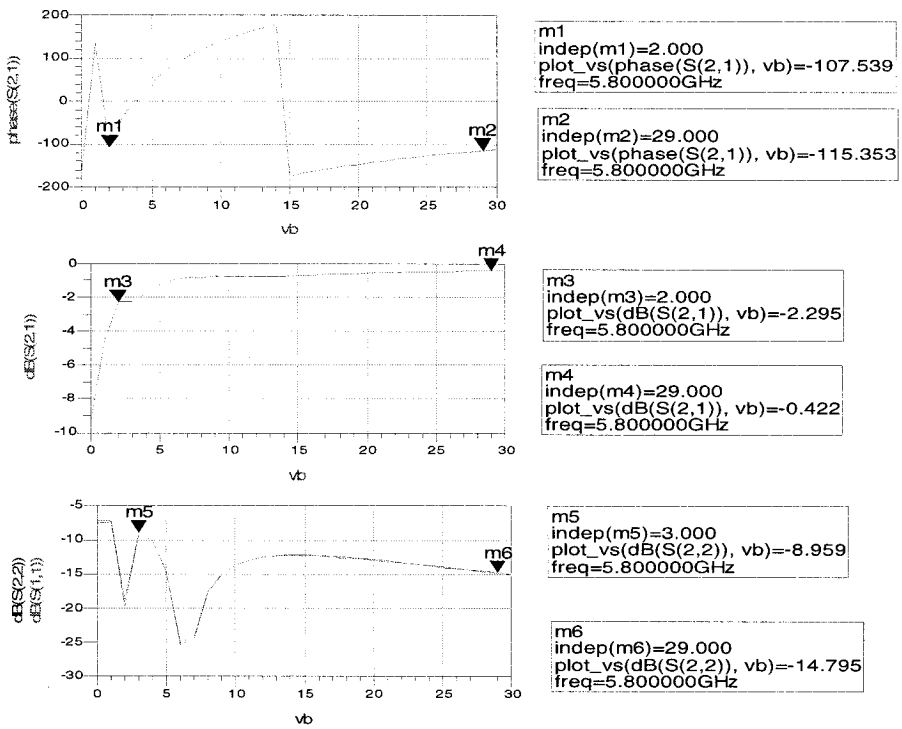


Figure 2- 30 16-stages phase shifter ADS simulation result (x =1.5), increased W.

Chapter 3. PHASE SHIFTER GAIN COMPENSATION

3.1. Automatic gain control (AGC)

Even if we make use of a design method that optimizes insertion loss, we still obtain a certain loss when the phase is shifted from 0 to 360°. Therefore, a method to compensate this loss is required in order to design a flat gain phase shifter. An appropriate way of compensation is given by automatic gain control method.

Automatic gain control (AGC) circuits are widely used in communications, where the signal amplitude needs to be kept at a fixed level. One example is a phase modulated system, where phase-locked loop circuits incorporating sinusoidal phase detectors used for demodulation are sensitive to signal amplitude. AGC can be used to compensate the effect of gain variations on the demodulated output. Its principle is based on feedback control theory. The output signal is detected and compared with a reference level, and generate a control signal to control the gain controlled device (GCD) to maintain the output single at a stable level. The GCD can be a gain controlled amplifier or a gain controlled attenuator. The diagram of an AGC is shown in Figure 3-1.

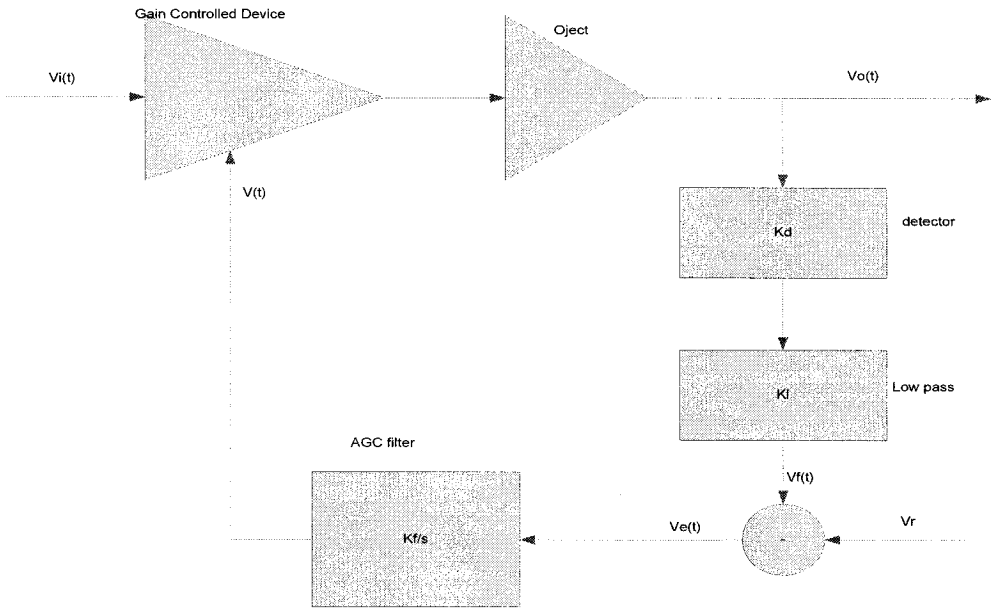


Figure 3- 1 Block diagram of a conventional AGC circuit.

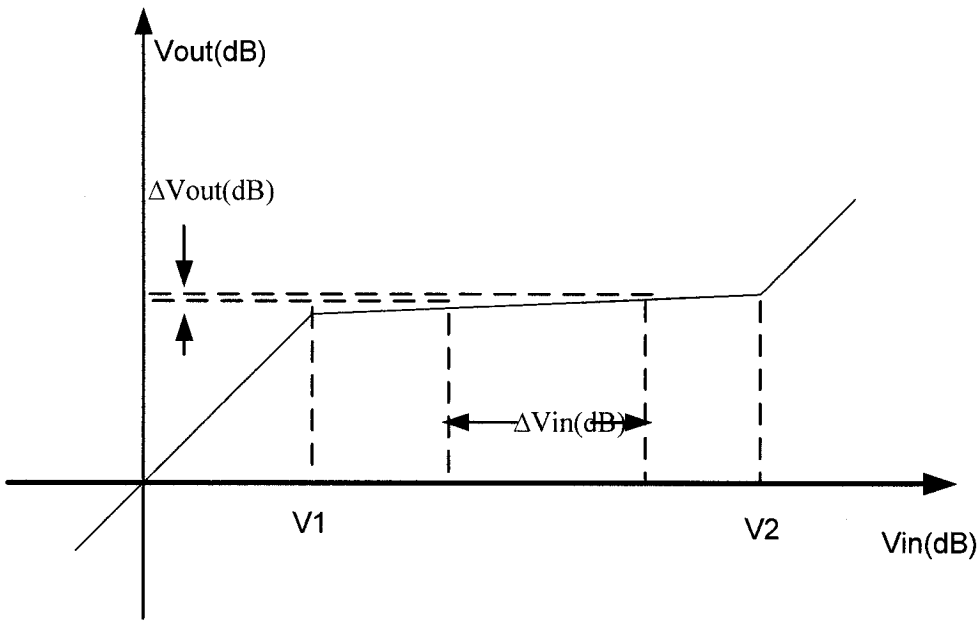


Figure 3- 2 AGC characteristics

As indicate in Figure 3-2, The AGC will be not achieved below or above a certain

input level. But in its achieved region for $V_1 < V_{in} < V_2$, the AGC system maintains V_{out} constant. This characteristic is often used to protect the output power in a high power amplifier or to maintain signal level in many communication systems.

3.2. Gain compensation principle

3.2.1 Gain compression

To analyze the gain compression characteristics we simplify Figure 3-1 to a circuit shown in Figure 3-3 by removing the filters.

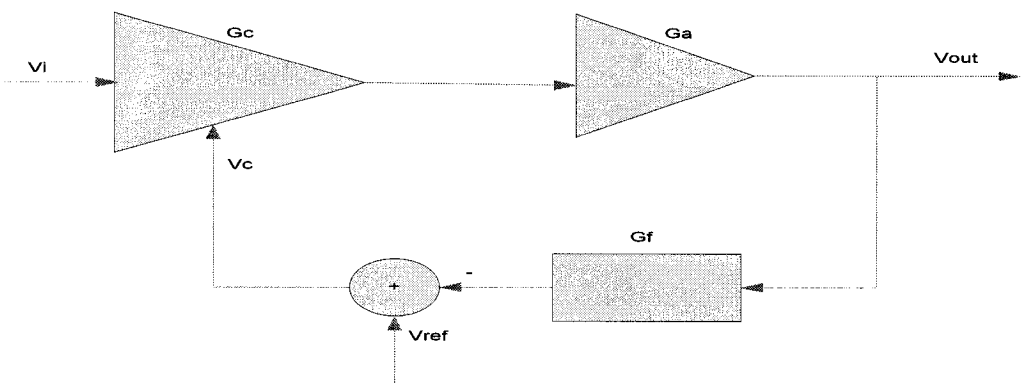


Figure 3- 3 Simplified diagram of AGC

At any given level, the input and output signals are related by:

$$V_{out} = Gc * Ga * V_{in} \tag{3.2.1}$$

From Figure 3-3, we have

$$Vc = V_{ref} - G_f * V_{out} \tag{3.2.2}$$

In an AGC we are mainly interested in its dynamic behavior. In general, G_f and V_{ref} are constant. The following calculations show a dynamic analysis for two different cases.

i) G_a is remain constant.

From (3.2.1) and (3.2.2) we get:

$$d(V_{out}) = G_a * V_{in} * d(G_c) + G_c * G_a * d(V_{in}) \tag{3.2.3}$$

$$d(V_c) = -G_f * d(V_{out}) \tag{3.2.4}$$

Dividing (3.2.3) by (3.2.4) we obtain:

$$-\frac{1}{G_f} = G_a * V_{in} * \frac{dG_c}{dV_c} - \frac{G_c * G_a}{G_f} * \frac{dV_{in}}{dV_{out}} \tag{3.2.5}$$

or

$$\frac{\Delta V_{out} / V_{out}}{\Delta V_{in} / V_{in}} = \frac{1}{1 + G_a * G_f * V_{in} * \left(dG_c / dV_c \right)} \tag{3.2.6}$$

Since can write

$$\frac{\Delta V_{out} / V_{out}}{\Delta V_{in} / V_{in}} \approx \frac{\Delta V_{out}(dB)}{\Delta V_{in}(dB)} \tag{3.2.7}$$

and

$$\frac{1}{G_c} \frac{dG_c}{dV_c} = \frac{2.303}{20} * K \tag{3.2.8}$$

we get the following relation for compression ratio:

$$M = \frac{\Delta V_{in}(dB)}{\Delta V_{out}(dB)} = 1 + L \tag{3.2.9}$$

$$L = G_a * G_f * V_{in} * dG_c / dV_c = 0.1151 * K * G_f * V_{out} \tag{3.2.10}$$

where K is the slope of the voltage controlled GCD expressed in decibels per volt. L describes the loop gain. If an AGC system is operating in a stable condition, we can write:

$$V_{out}(dBu) = \Delta V_{out}(dB) + \bar{V}_{out}(dBu) \tag{3.2.11}$$

$$V_{out}(dBu) = \frac{\Delta V_{in}}{\bar{M}} + \bar{V}_{out}(dBu) \tag{3.2.12}$$

$$\bar{M} = 1 + 0.1151 * K * G_f * \bar{V}_{out} \tag{3.2.13}$$

where $\bar{V}_{out}(dBu)$ gives the mean (i.e. the desired) value of the output signal and $\bar{M}$ the compression ratio at $\bar{V}_{out}$.

From (3.3.12) and (3.2.13) we know if K and G_f are large enough, we have $V_{out} \approx \bar{V}_{out}$ when V_{in} changes. This is the conventional AGC principle.

ii) V_i remain constant

Now we consider the case that G_a changes with V_i remaining constant.

$$d(V_{out}) = G_a * V_{in} * d(G_c) + G_c * V_{in} * d(G_a) \tag{3.2.14}$$

$$d(V_c) = -G_f * d(V_{out}) \tag{3.2.15}$$

Dividing(94) by (95) we have:

$$-\frac{1}{G_f} = G_a * V_{in} * \frac{dG_c}{dV_c} - \frac{G_c * V_{in}}{G_f} * \frac{dG_a}{dV_{out}} \tag{3.2.16}$$

$$\frac{\Delta V_{out} / V_{out}}{\Delta G_a / G_a} = \frac{1}{1 + G_a * G_f * V_{in} * \left(dG_c / dV_c \right)} \tag{3.2.17}$$

Again, we get a value of gain compression ratio:

$$\text{M'} = \frac{\Delta Ga(dB)}{\Delta V_{out}(dB)} = 1 + L = \text{M} \tag{3.2.18}$$

$$V_{out}(dBu) = \frac{\Delta G_a}{\bar{M}'} + \bar{V}_{out}(dBu) \tag{3.2.19}$$

$$\bar{M}' = \bar{M} = 1 + 0.1151 * K * G_f * \bar{V}_{out} \tag{3.2.20}$$

From (3.2.19) and (3.2.20) we know if K and G_f are large enough, we have $V_{out} \approx \bar{V}_{out}$ when G_a changes. So the gain Vout/Vin will remain at a constant value. This is the principle of our gain compensation. Figure 3-4 shows the characteristic of this gain compression principle.

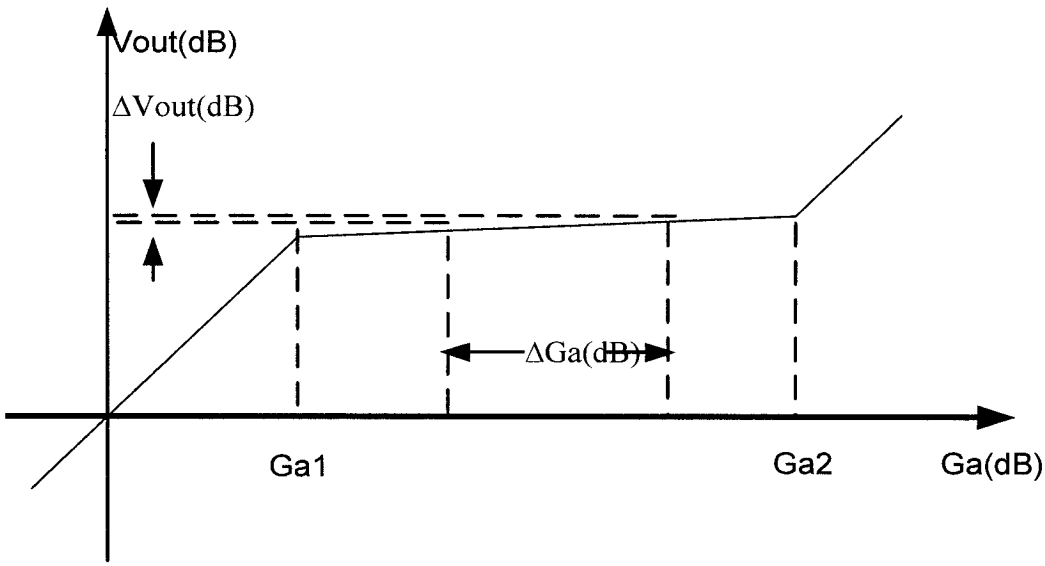


Figure 3- 4 Characteristic behavior of AGC gain compression

3.2.2 AGC Control system

Gain Controlled Device: The gain of the GCD is often modeled to depend exponentially upon the control voltage V [25].

$$g(v) = Ge^{-\alpha v} \tag{3.2.21}$$

where $G > 0$ and $\alpha > 0$ are constants.

$$g(v)dB = 20\log_{10} g(v) = G(dB) - 8.686\alpha v \tag{3.2.22}$$

Control Object: The control object varies from system to system, but it is often modeled as a first- or second-order delay element with variable gain G_a represent by the following relations: $G_a/(s+a)$ or $G_a/(s^2+as+b)$. At high frequency the group delay is often very small compare to the time constant of AGC filter or detector filter. Thus the object is often modeled as G_a.

Power detector: The power detector is usually a combination of a diode detector and a low pass filter. So it can be modelled as an element by the relation: $K_d/(1+\tau_1 S)$.

AGC filter: The AGC filter is often designed as a RC circuit together with OP amplifiers, which can be modelled as $K_g/(1+\tau_2 S)$.

Thus the AGC system can be modeled as Figure 3-5, where V_i and V_a are the disturbances from the variation of input signal and object gain. V_{out} remain a value of V_{ref}/K_d. The static relationship of V_{out} and V_{ref} is shown in Figure 3-6. In our system, the object is the phase shifter, the gain variation when changing the phase will be decompressed and V_{out} will be not affected.

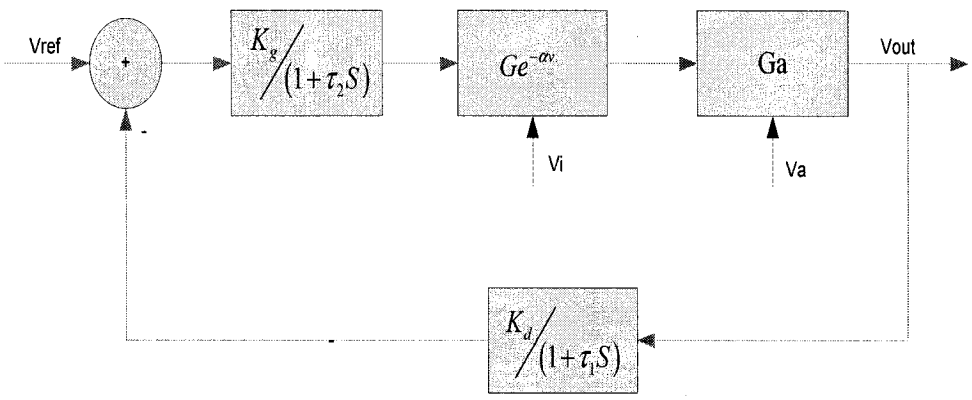


Figure 3- 5 AGC control system model

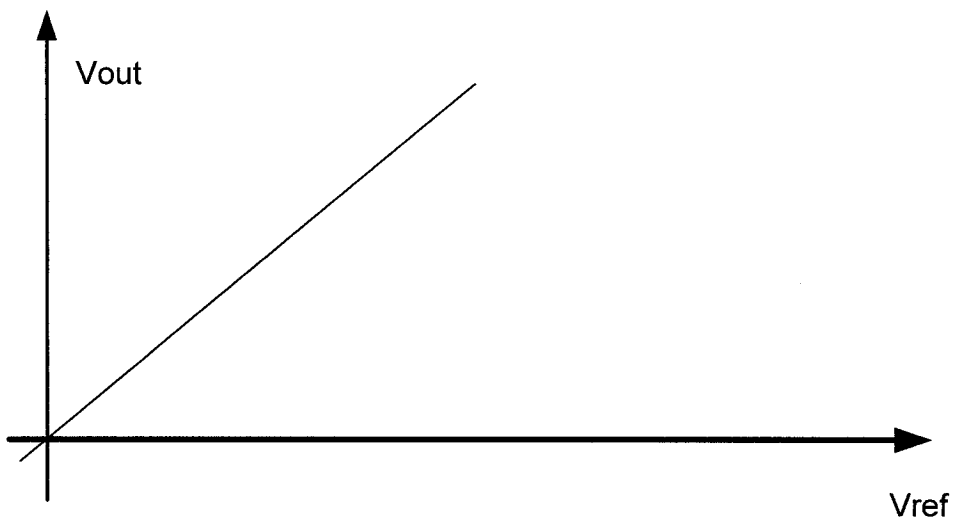


Figure 3- 6 V_{out} vs V_{ref} relationship

3.2.3 Input tracing AGC control system

Figure 3-6 shows that V_{out} is linearly follows V_{ref} changes in a linear system. If V_{ref} is equal to V_{in}, then V_{out} is given by

$$V_{out} = K*V_{in}, \qquad 3.2.23$$

where K is a constant. It meets exactly the requirement for the relation between input and output voltages of a stable gain system. If we introduce this assumption into our system model, we obtain a block diagram as it is shown in Figure 3-7.

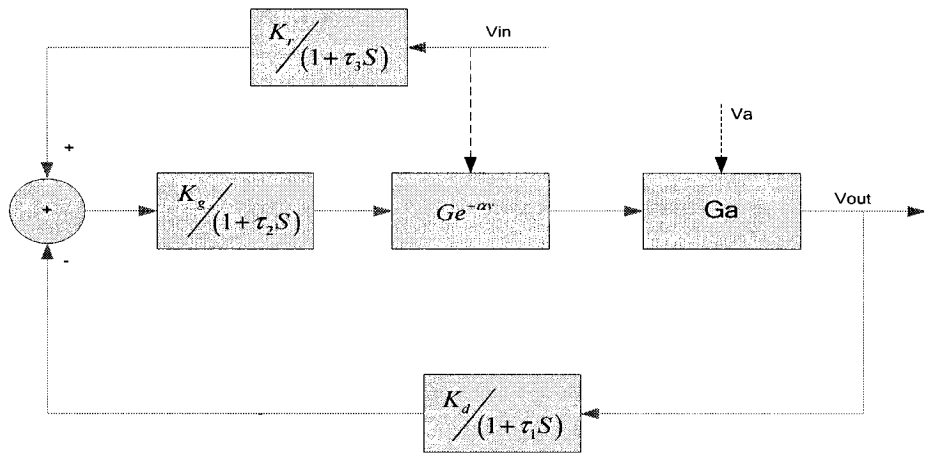


Figure 3- 7 Input tracing AGC control system model

V_{in} acts as control signal input and interference input. If the delay time constants satisfy $\tau_3 \gg \tau_2 \gg \tau_1$, then the signal input and interference input will separate and the system could be stable.

Similar to the other control system design, this system needs to be designed to have a stable, quick and precise response. Response precision can be achieved by a large loop gain, while a quick response can be realized through a lead-lag compensation filters, which can lead to response dumpling or Butterworth [25]. However in our application, we mainly require precision and stability. Therefore, we use the simple but very effective RC constant delay filter as shown in Figure 3-7. The loop is always stable regardless of loop gain, and the response will never show overshoot. Figure 3-8 shows the output response versus unit input. Curve **a** represents the RC constant delay filter, curve **b** a lead-lag filter.

Curve **b** response quicker with overshoot.

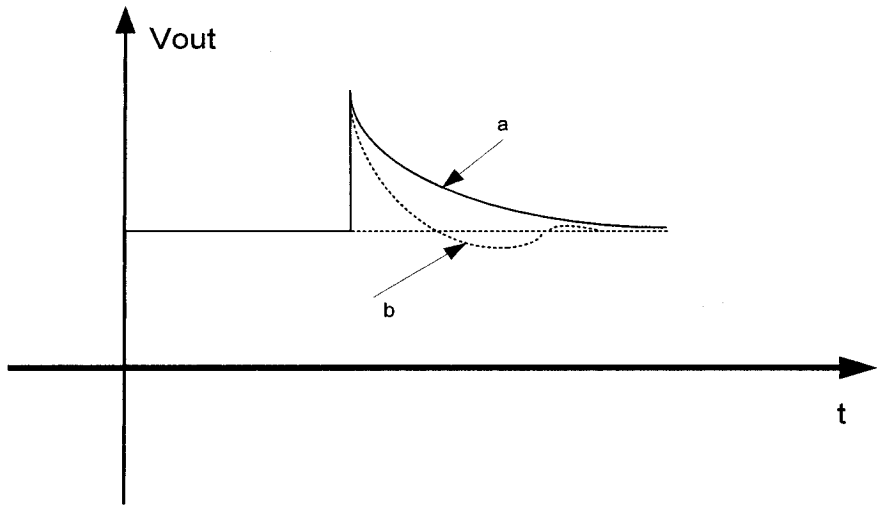


Figure 3- 8 Output response of unit input

3.3. Flat gain phase shifter circuit implementation

Figure 3-9 shows the structure of the implemented circuit. We use a 90° hybrids as RF coupler or divider to achieve enough power in order to be able to use a simple PIN diode to detect it. The selected variable attenuator is a Hittite HMC345MS8G GaAs MMIC, which can be tuned from 0 to 30dB by a negative voltage 0 to –2.5 volt under 8 GHz. After the attenuator a RF amplifier is used to compensate the loss. The feedback control filter is designed to make the closed loop control response stable and precise, and consists of an OP amplifier combined with a RC circuit. The input RF coupler and the followed power detector, together with RC delay filter are optional. They may need to be added in the future to obtain constant V_{out}/V_{in}.

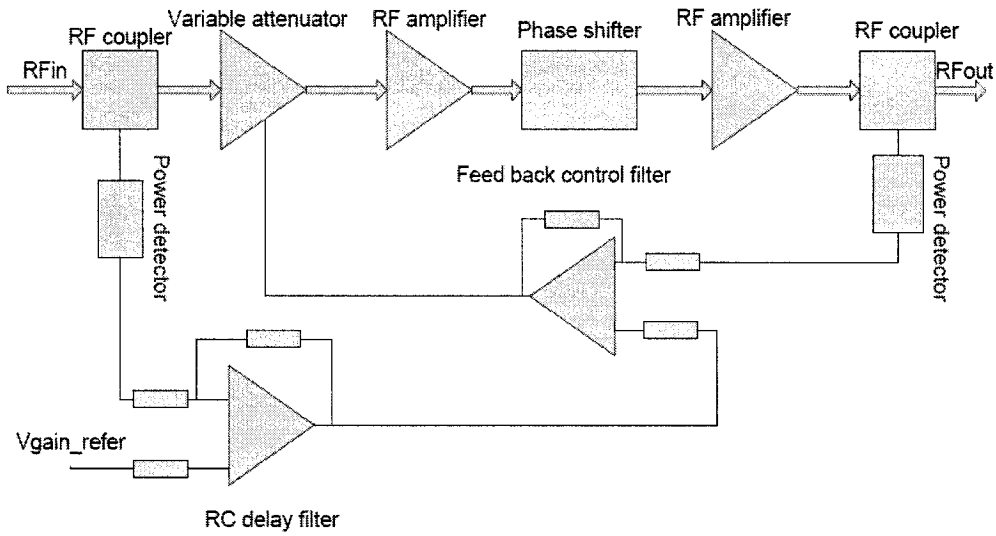


Figure 3- 9 Flat gain phase shifter implement diagram

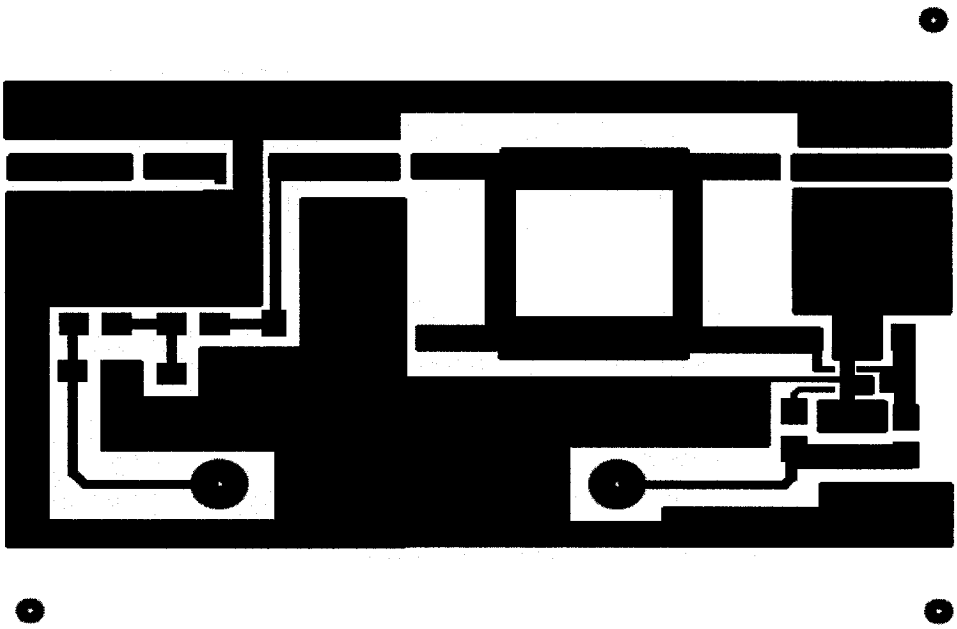


Figure 3- 10 RF power amplifier, power divider and detect layout

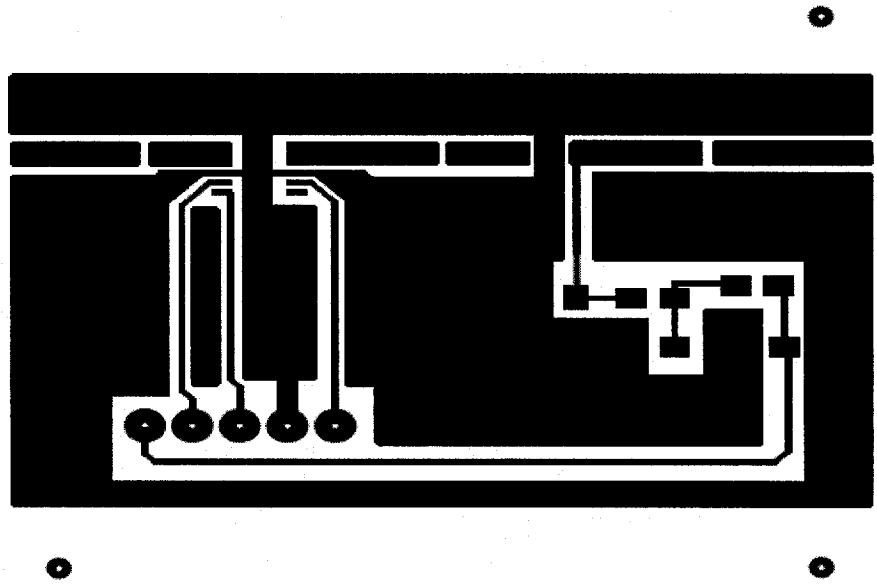
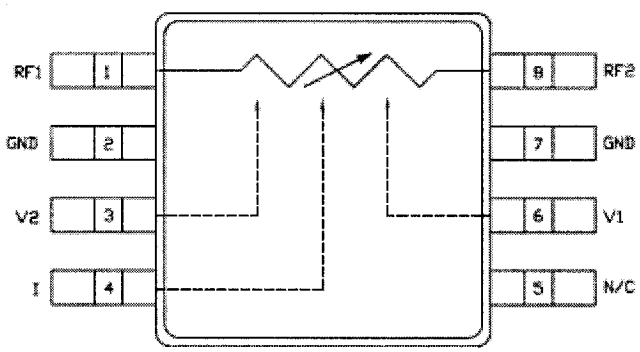


Figure 3- 11 Variable attenuator and power amplifier layout

3.3.1 Variable analog attenuator

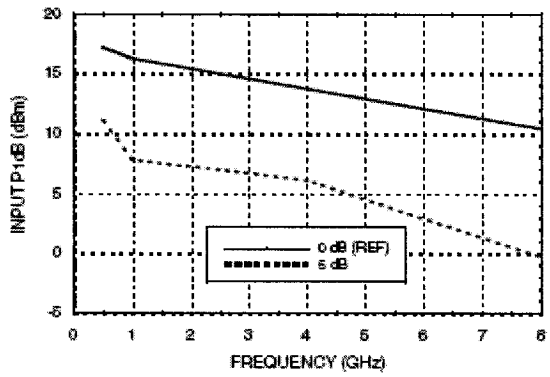


Electrical Specifications, T_A = +25° C, 50 ohm system

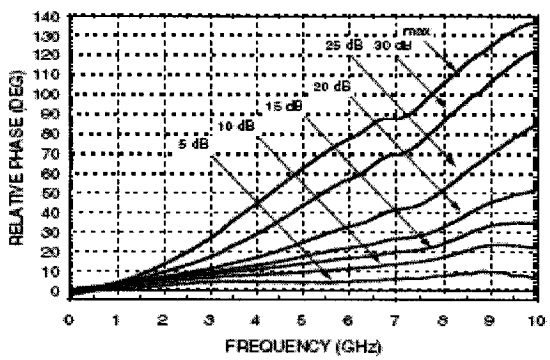
Parameter		Min	Typical	Max	Units
Insertion Loss	DC - 8 GHz		1.5	2.5	dB
Attenuation Range	DC - 8 GHz	27	32		dB
Return Loss	DC - 8 GHz	5	10		dB
Switching Characteristics	tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)		2 8		ns ns
Input Power for 0.25 dB Compression (0.5 - 8 GHz)	Min. Atten. Atten. >2 dB		+8 -2		dBm dBm
Input Third Order Intercept (0.5 - 8 GHz) (Two-tone Input Power = -8 dBm Each Tone)	Min. Atten. Atten. >2 dB		+25 +10		dBm dBm

Figure 3- 12 Hittite HMC345MS8G GaAs MMIC variable attenuator specification

1 dB Compression vs. Attenuation



Relative Phase



Relative Attenuation vs. Control Voltage @ 8 GHz

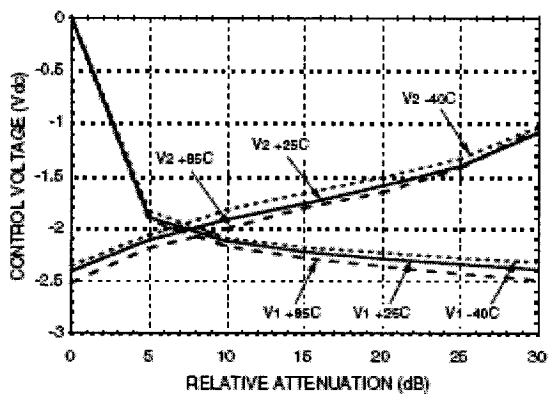


Figure 3- 13 Hittite HMC345MS8G variable attenuator characteristics.

Before fabrication, we should simulate the circuits with CAD software. Thus we need to build ADS model of each component in the circuits, such a model can be represented in different ways such as by S parameters or mathematical expressions. In our case, we use a simplified mathematical relation to model our circuit.

The HMC345MS8G variable attenuator can be represented as:

$$G_c(dB) = 2.63V_c \qquad \text{if } |V_c| \le 1.9 \qquad (3.3.1)$$

$$G_c(dB) = 74.23 + 41.7V_c \qquad \text{if} |V_c| \ge 1.9 \qquad (3.3.2)$$

From (3.2.20) we need select high K to get high gain compression ratio, so we can assume to let the variable attenuator work in the range of $|V_c| \ge 1.9$. The phase Ph(degree)~Vc(Volt) relation can be obtained using Matlab. From Figure 3-13 we can get a phase-attenuation relation at 5.8 GHz:

Gc(dB)	-5	-10	-15	-20	-25	-30
Ph(degree)	4	10	17	22	33	56
Vc(Volt)	-1.9	-2.02	-2.14	-2.26	-2.38	-2.39

Table 3- 2 HMC345MS8G variable attenuator Gc~Vc, Phase~Vc relation at 5.8Ghz.

Using Matlab, curve fitting yields the following expression:

$$Ph = -107 - 58.3 * V_c \qquad (3.2.3)$$

The ADS model of the variable attenuator can be expressed as a controlled amplifier combined with a phase shifter as shown in Figure 3-14.

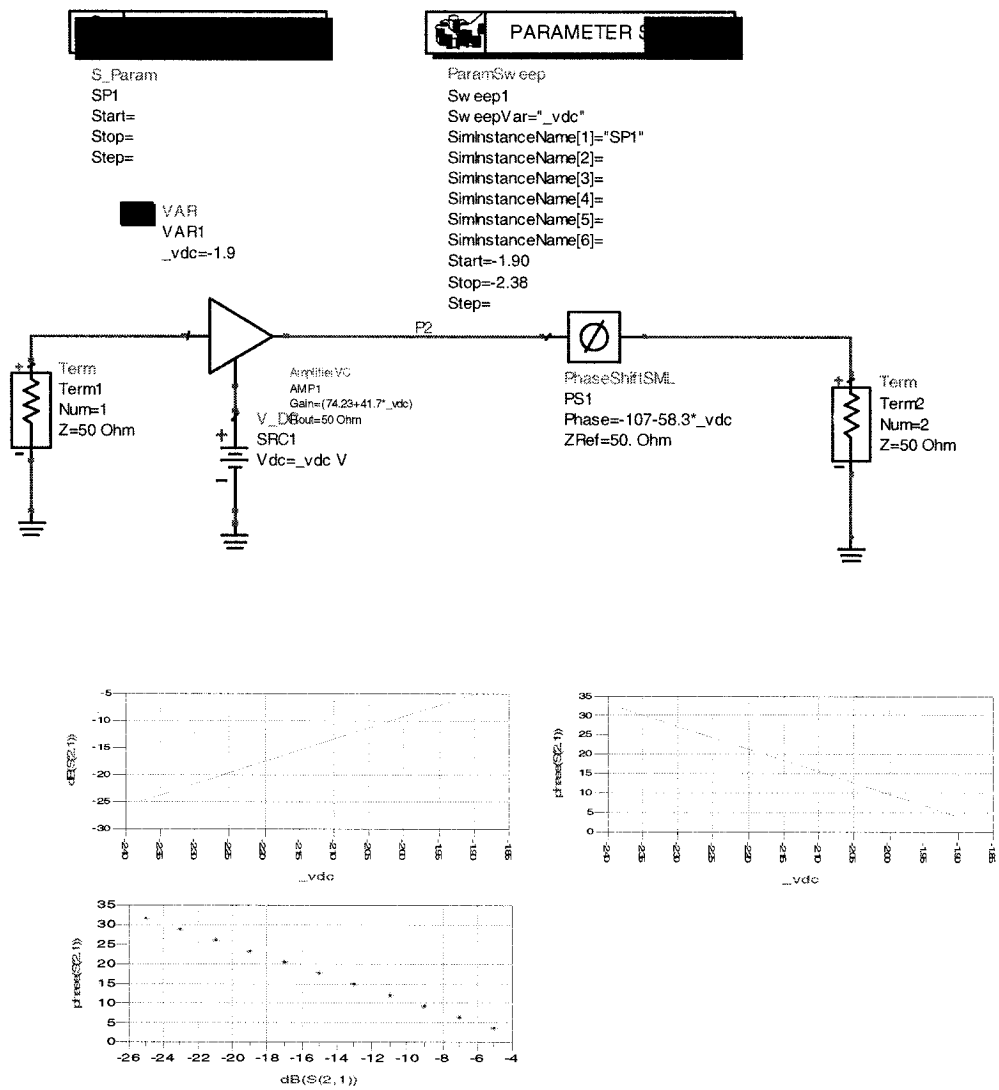


Figure 3- 14 HMC345MS8G variable attenuator ADS simulator model

To realize the gain control circuit that is always match to a 50Ω system, it is recommended to follows the circuits provided by the manufacture, which is shown in Figure 3-16.

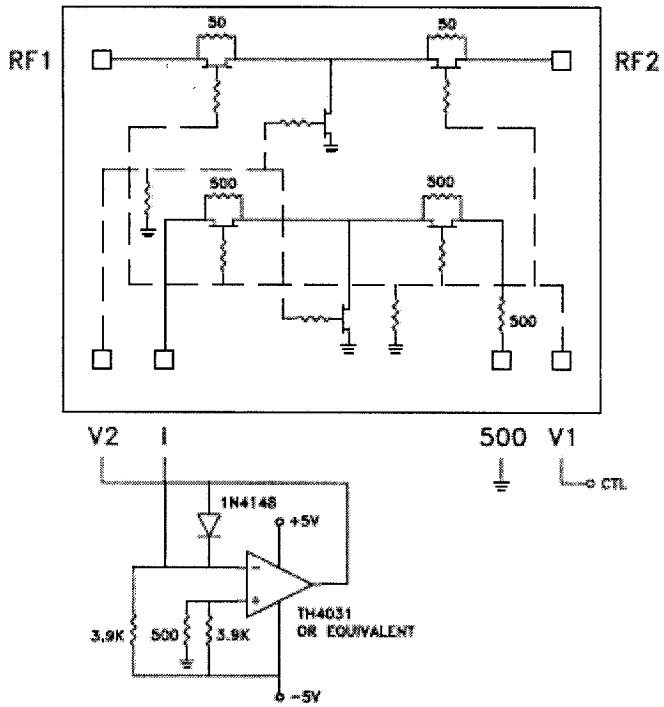
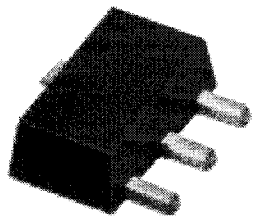


Figure 3- 15 Hittite HMC345MS8G variable attenuator control circuits.

3.3.2 Signal amplifiers

After the attenuator and the phase shifter we need add an amplifier to amplify the signal to make sure the signal level stay within a certain dynamic range. We select the Gali29 amplifier, which can work from DC to 7 GHz, with 17.6 dBm output power and 50Ω input/output impedance, so it can be used directly in a 50Ω system without any additional matching network. Figure 3-16 shows the amplifier's characteristics. Its bias circuit is shown in Figure 3-17



CASE STYLE : DF782

Electrical Specifications @ 25°C

	MODEL NO.	FREQ.▲ (GHz)	GAIN, dB Typical									MAXIMUM POWER, dBm at 7 GHz*			DYNAMIC RANGE at 2 GHz*		VSWR (:1) Typ.				MAXIMUM CURRENT RATING**	DC OPERATING POWER @ Pin 3***				THERMAL RESIS-TANCE	PRICE $
			over frequency, GHz								Min. @ 2 GHz	Output (1 dB Comp.)		Input (no dmg.)	NF	IP3	In		Out			Current	Device Volt			θjc typ.	Qty (25)
		f_L-f_U	0.1	1	2	3	4	5	7	10		Typ.	Min.		dB Typ.	dBm Typ.	DC-1 GHz	3-4 GHz	DC-3 GHz	3-4 $_{U}$ GHz	mA	(mA)	Typ	Min	Max	°C/W	
LOW POWER	Gali-19	DC-7	12.1	11.7	11.6	10.7	10.8	10.1	11.0	14.5	9.6	10.6	6.0	15	6.5	23.7	1.6	1.7	1.5	2.3	55	40	3.6	3.2	4.0	311	1.19
	Gali-29	DC-7	15.4	15.1	14.7	13.7	13.6	12.9	14.2	12.5	12.7	11.2	10.0	15	6.0	24.7	1.6	1.6	1.5	2.3	55	40	3.6	3.2	4.0	340	1.19
	Gali-39	DC-7	20.8	21.1	19.7	17.7	17.8	16.3	17.6	9.6	17.7	10.5	9.0	13	4.9	22.9	1.6	1.8	1.5	2.3	55	36	3.6	3.1	3.9	350	1.19
MEDIUM POWER	Gali-49	DC-6	14.0	13.7	13.6	13.7	13.3	13.1	10.7	—	11.5	18.4	15.0	20	5.5	33.3	1.7	1.2	1.6	1.4	85	65	5.0	4.5	5.4	171	1.79
	Gali-59	DC-5	20.6	19.7	18.3	16.7	15.4	14.0	10.2	—	16.3	17.8	10.5	13.0	4.3	33.3	1.6	1.5	1.5	1.7	85	66	4.6	4.3	5.2	209	1.79

▲ Low frequency cutoff determined by external coupling capacitors.
* For Pout @ 1dB compression, Gali-49,-59 at 2 GHz.
For IP3, Gali-49,-59 at 7 GHz.
** Permanent damage may occur if any of these limits are exceeded. These ratings are not intended for continuous normal operation.
*** Reliability predictions and normal operating conditions are applicable at current specified.

f_U is the upper frequency limit for each model as shown in the table.

Figure 3- 16 Mini-circuit Gali29 amplifier characteristics.

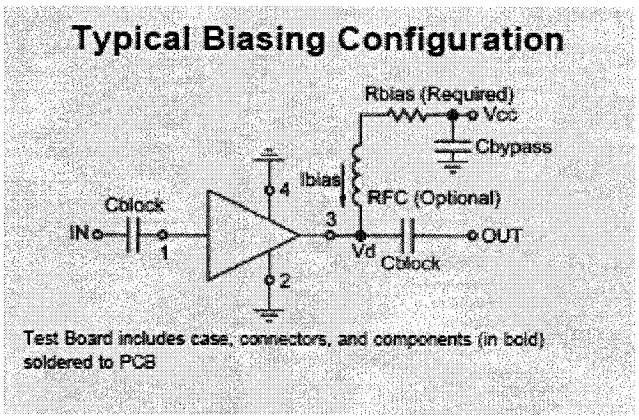


Figure 3- 17 Mini-circuit Gali29 amplifier bias circuits

The Hittite HMC345MS8G variable attenuator and the Mini-circuit Gali29 amplifier circuits are shown in Figure 3-18. The attenuator control circuits are placed on a low

frequency control board and connected to the RF board by cables. The amplifier's bias RFC is replaced by a λ/4 high impedance line at 5.8GHz.

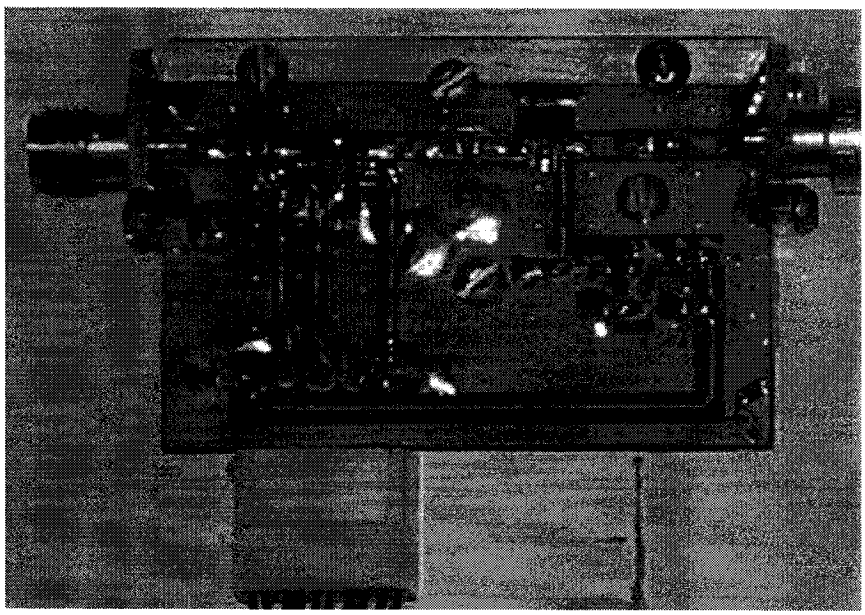
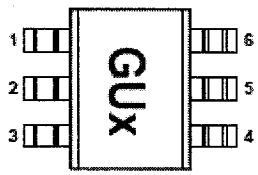


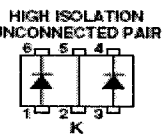
Figure 3- 18 Variable attenuator and amplifier circuits implement

3.3.3 Power detector

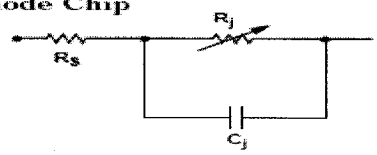
The input/output power is around 5dBm, so we can use Schottky barrier diodes to detect it. We use Agilent' SOT-363 surface mounted Schottky barrier diode HSMS-282K as our detector. Figure 3-19 shows its characteristics.

The detector circuit is shown in Figure 3-21. C_4 and R_1 are used to match the circuit to 50Ω. R_2 and C_3 build a low pass filter.





Linear Equivalent Circuit Model
Diode Chip



R_S = series resistance (see Table of SPICE parameters)
C_j = junction capacitance (see Table of SPICE parameters)
$R_j = \frac{8.33 \times 10^{-5}\ nT}{I_b + I_s}$

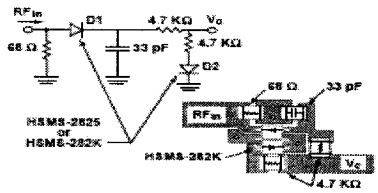


Figure 18. Temperature Compensated Detector.

SPICE Parameters

Parameter	Units	HSMS-282x
B_V	V	15
C_{J0}	pF	0.7
E_G	eV	0.69
I_{BV}	A	1E-4
I_S	A	2.2E-8
N		1.08
R_S	Ω	6.0
P_B	V	0.65
P_T		2
M		0.5

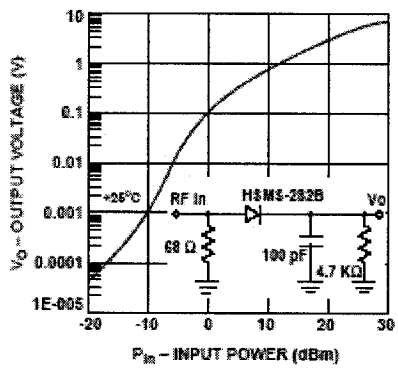


Figure 3- 19 schottky barrier diode HSMS-282K characteristics

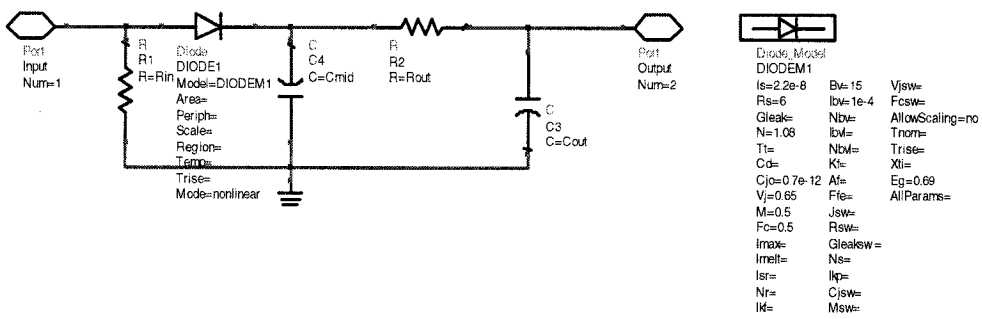


Figure 3- 20 HSMS-282K Detector circuits

To detect the power, a RF divider needs to be added. For this purpose, we use a 3dB 90°hybride as shown in Figure 3-22. Figure 3-23 shows the power detector test circuit, in which the red block is the 3dB hybrid and the two- port block is the HSMS-282K detector circuit that is shown in Figure 3-21. Its ADS simulation result is shown in Figure 3-24. In Figure 3-25 you can see the final power detecting circuit we fabricated.

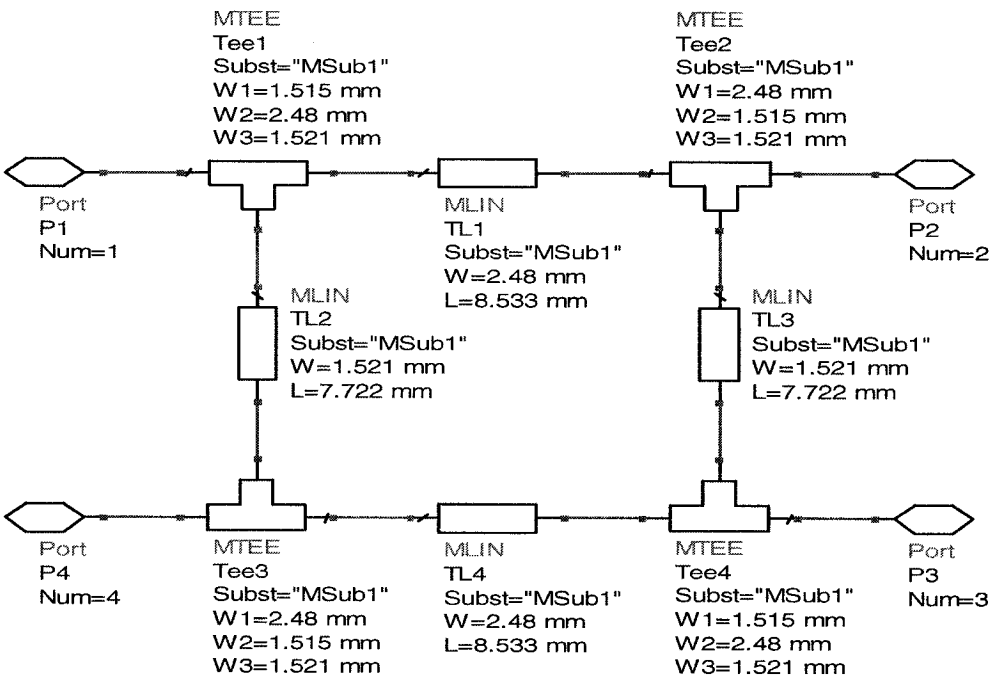


Figure 3- 21 90° 3dB hybrid coupler.

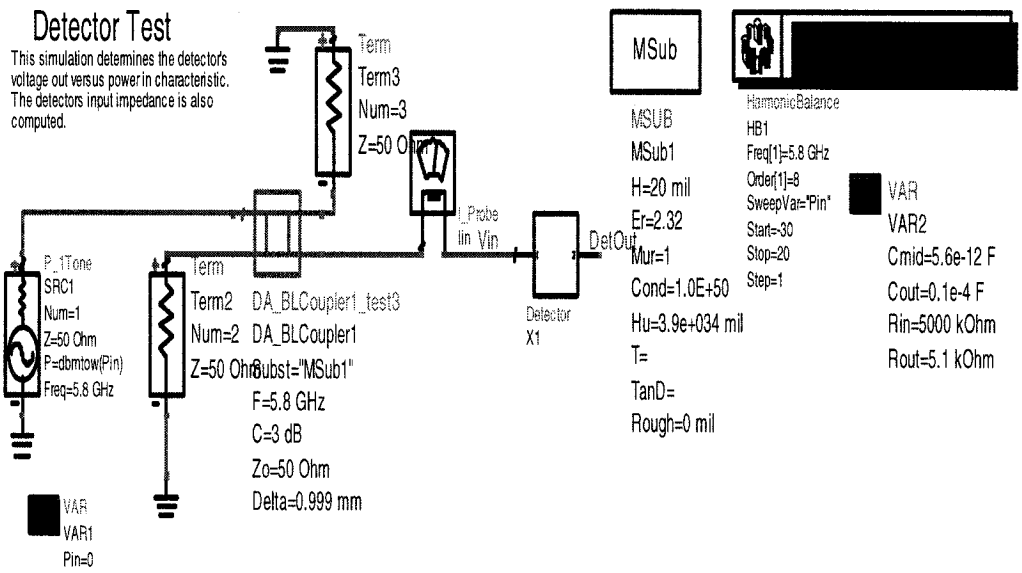
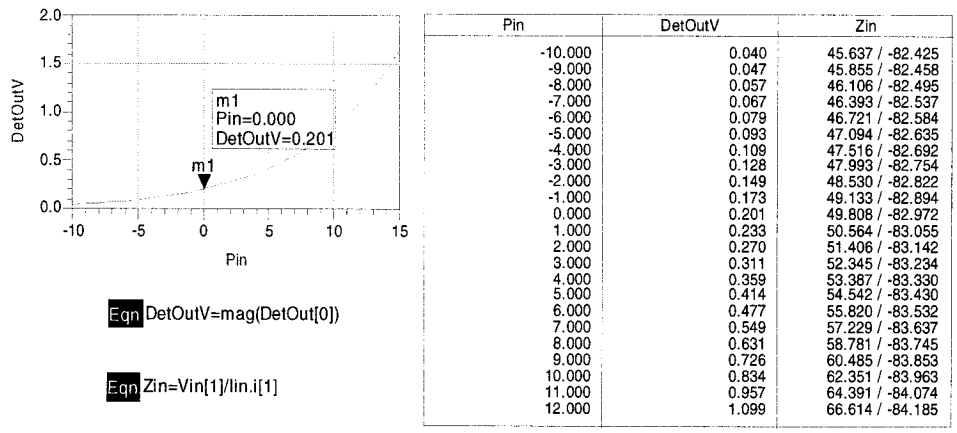


Figure 3- 22 Power detector test circuit.



Pin	DetOutV	Zin
-10.000	0.040	45.637 / -82.425
-9.000	0.047	45.855 / -82.458
-8.000	0.057	46.106 / -82.495
-7.000	0.067	46.393 / -82.537
-6.000	0.079	46.721 / -82.584
-5.000	0.093	47.094 / -82.635
-4.000	0.109	47.516 / -82.692
-3.000	0.128	47.993 / -82.754
-2.000	0.149	48.530 / -82.822
-1.000	0.173	49.133 / -82.894
0.000	0.201	49.808 / -82.972
1.000	0.233	50.564 / -83.055
2.000	0.270	51.406 / -83.142
3.000	0.311	52.345 / -83.234
4.000	0.359	53.387 / -83.330
5.000	0.414	54.542 / -83.430
6.000	0.477	55.820 / -83.532
7.000	0.549	57.229 / -83.637
8.000	0.631	58.781 / -83.745
9.000	0.726	60.485 / -83.853
10.000	0.834	62.351 / -83.963
11.000	0.957	64.391 / -84.074
12.000	1.099	66.614 / -84.185

Figure 3- 23 Power detector ADS simulation result

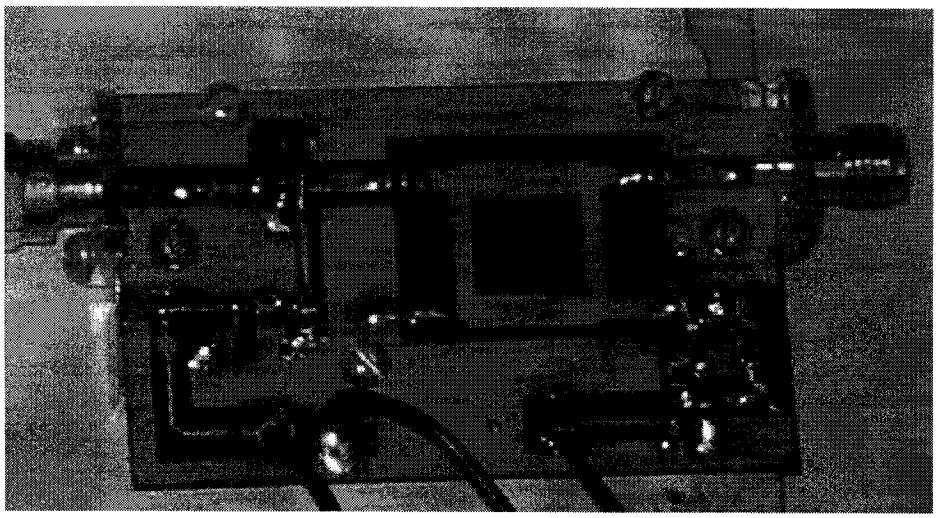


Figure 3- 24 Power amplify and detect circuits

3.3.4 Phase shifter

In chapter 2 we discussed the design of a varactor loaded line phase shifter. However, here we use an existing designed one as shown in Figure 3-26. Although its performance is worse (higher insertion loss and return loss), we can use it for the first trial. If it is not suitable in our future application, it needs to be redesigned as described in chapter 2.

To use this phase shifter in our system, we should track its S parameters as the bias changes. In Figure 3-27 to Figure 3-30 a summary of measurement results are shown.

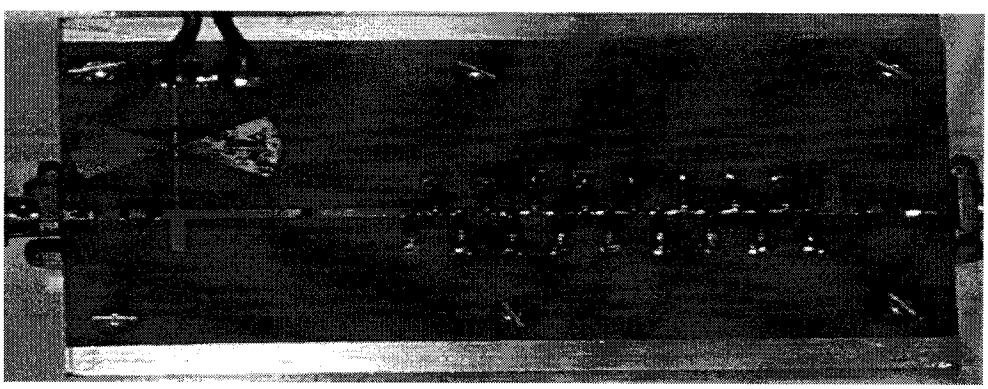


Figure 3- 25 Phase shifter

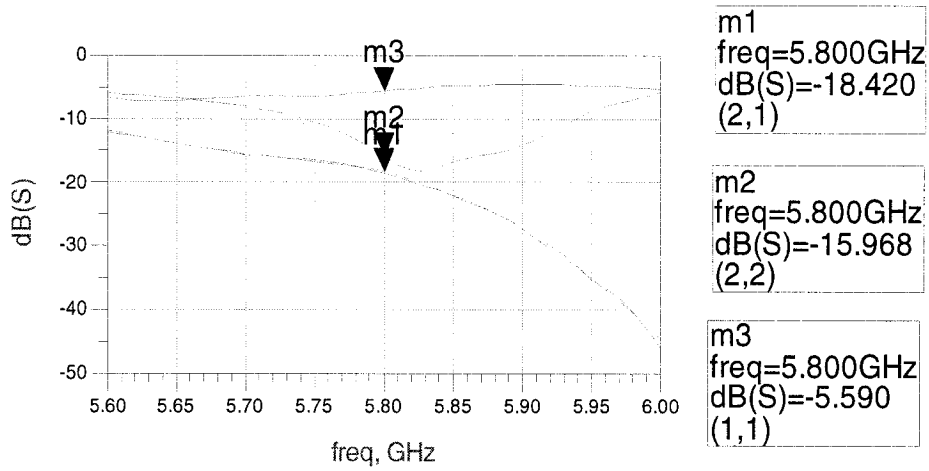


Figure 3- 26 Phase shifter S- parameters at Vdc=16V

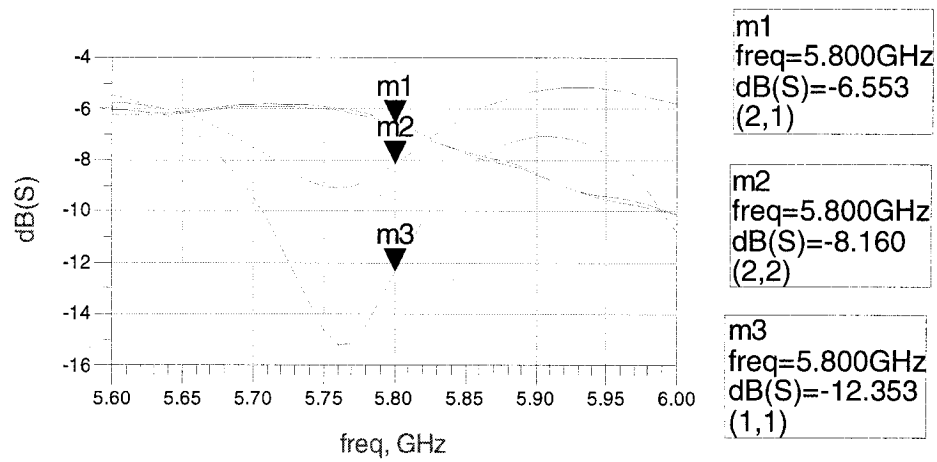


Figure 3- 27 Phase shifter S- parameters at Vdc=20V

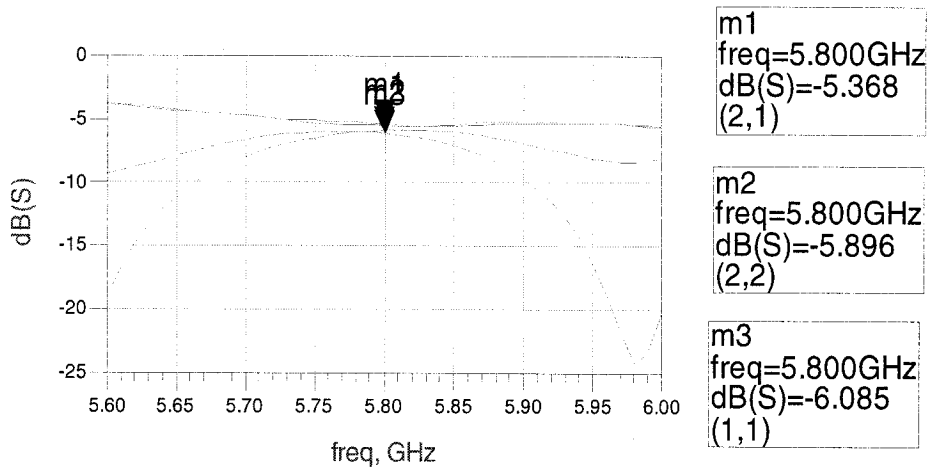


Figure 3- 28 Phase shifter S- parameters at Vdc=25V

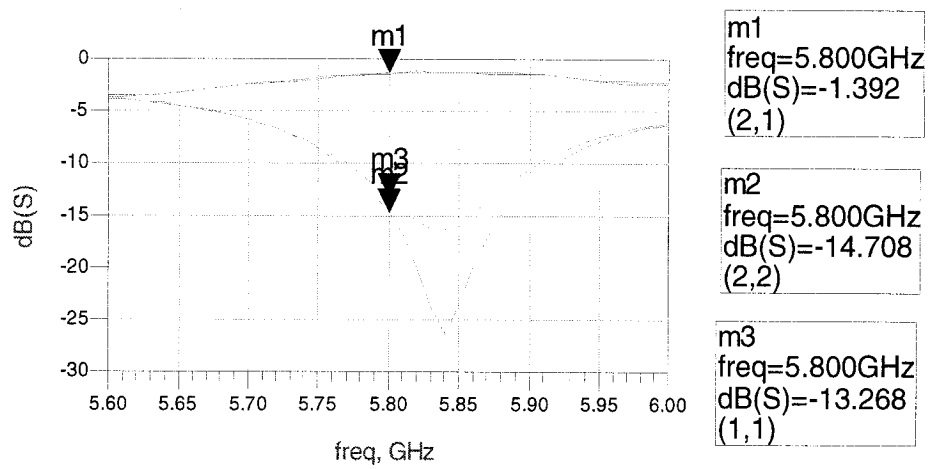


Figure 3- 29 Phase shifter S- parameters at Vdc=29V

From these parameters we extract magnitude and phase of S21 over Vbias as shown in Figure 3-31 and Figure 3-32

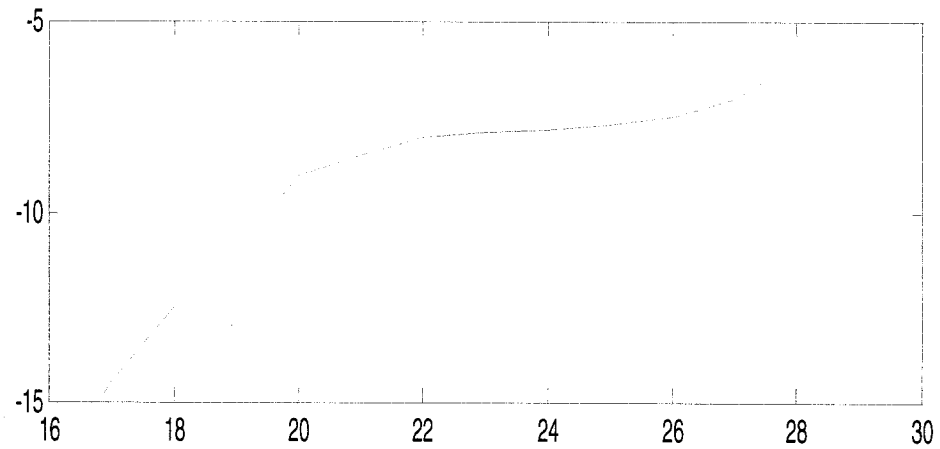


Figure 3- 30 Phase shifter |S21| vs Vbias

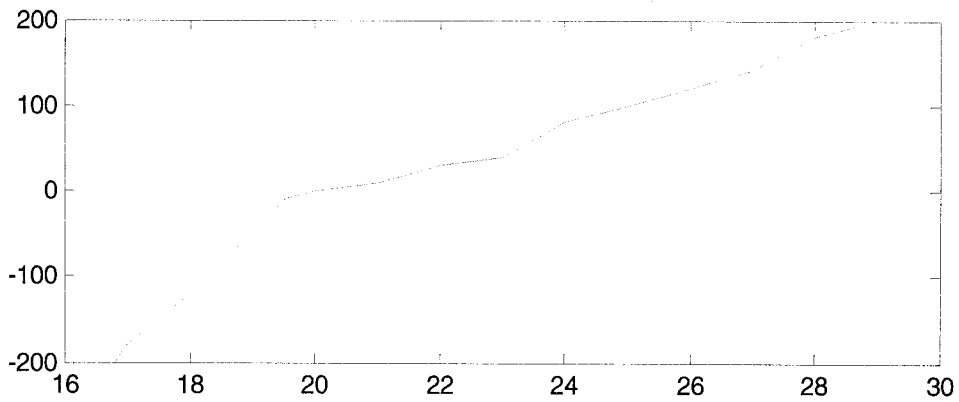


Figure 3- 31 Phase shifter phase (S21) vs Vbias

To simulate this phase shifter in ADS, we model it by a controlled amplifier in combination with a controlled phase shifter as shown in Figure 3-32.

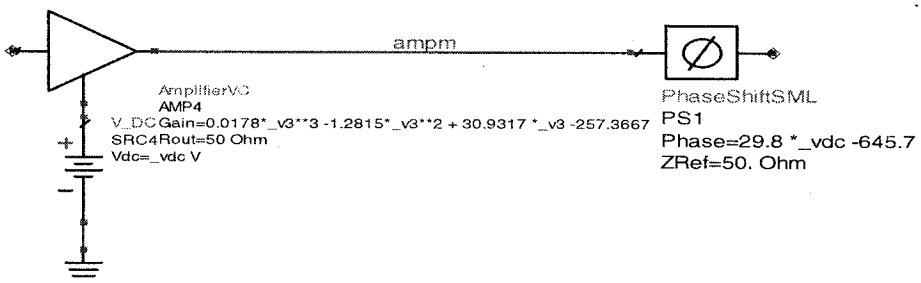


Figure 3- 32 Phase shifter ADS model

3.4. ADS Simulation and Circuits Test Results

A simulation in ADS helps us to predict the circuit's structure, functionality and its performance change for different parameters changing. This accelerates the circuit design process, even if the simulation models deviate slightly from our real circuits.

Figure 3-33 shows the AGC ADS model circuit's structure. We use the envelope simulation method to simulate its functionality. By verifying the phase shifter's bias V_{dc} and the gain reference voltage V_{ref} while tracing output voltage V_{out}, we can find the following results:

(1) A varies in the bias voltage change the phase, but does not influence the output power;

(2) When regulating V_{ref}, the phase of V_{out} remains stable but the output power is increased.

(3) When we change the input power, the output power remains constant.

(4) Gain and phase change only slightly when the working frequency varies.

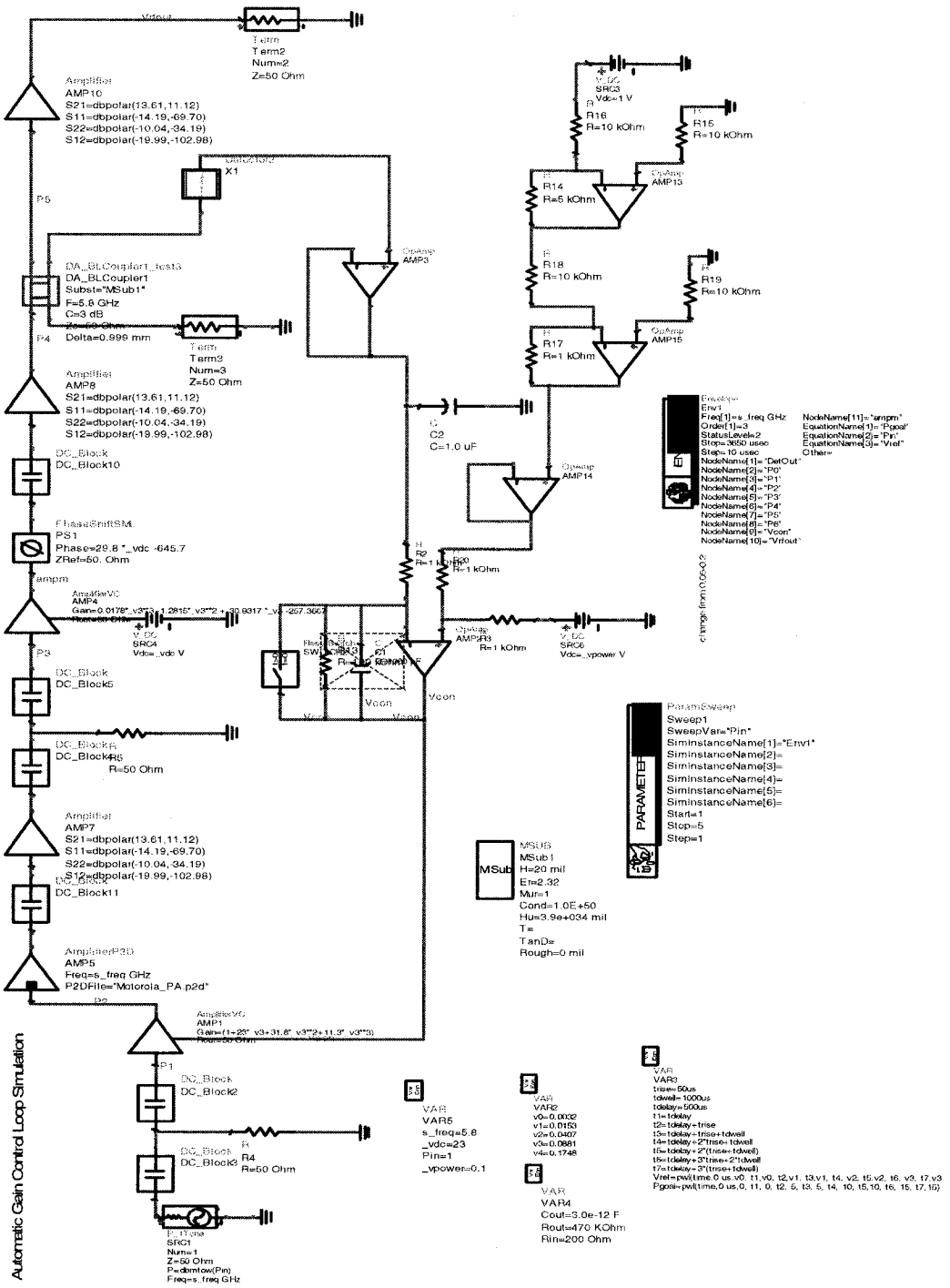


Figure 3- 33 AGC ADS simulation circuit

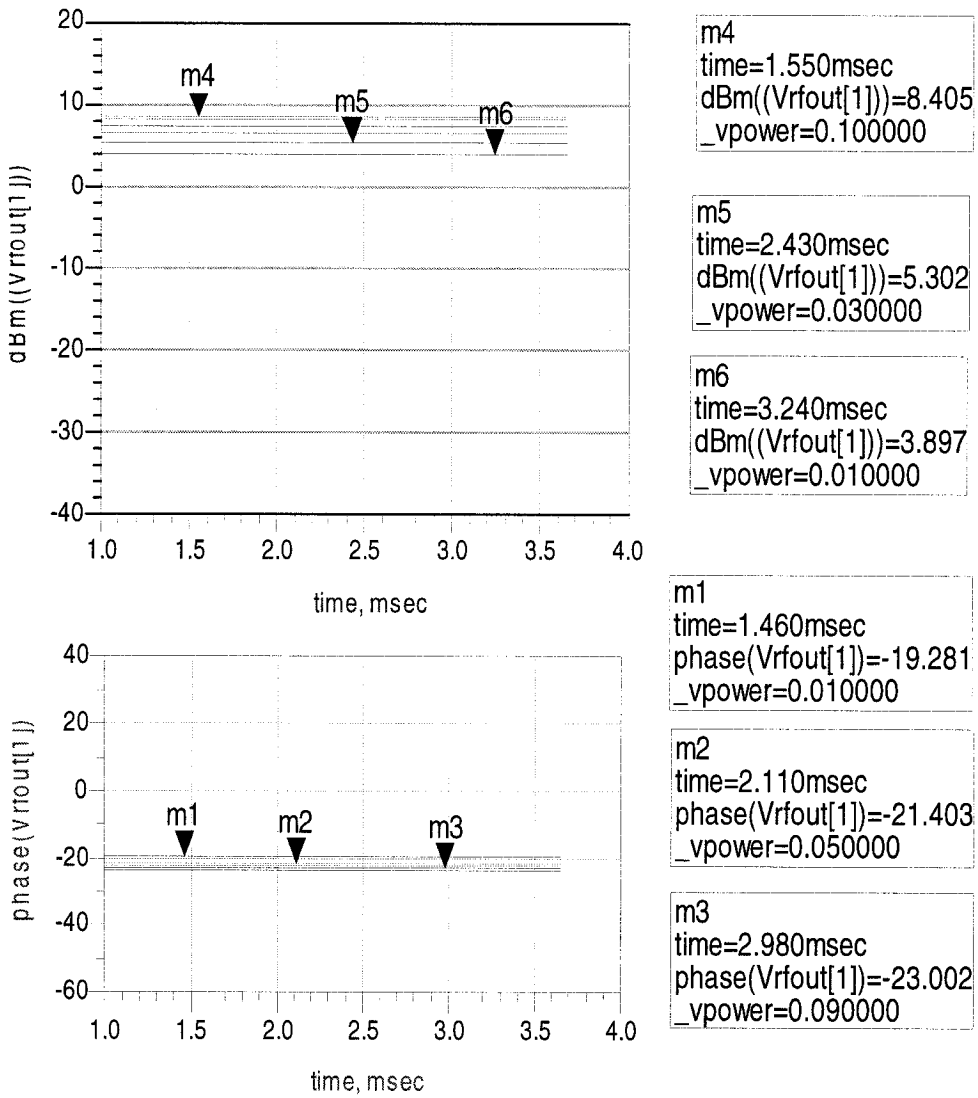


Figure 3- 34 AGC simulation result: RF output vs Vref of gain

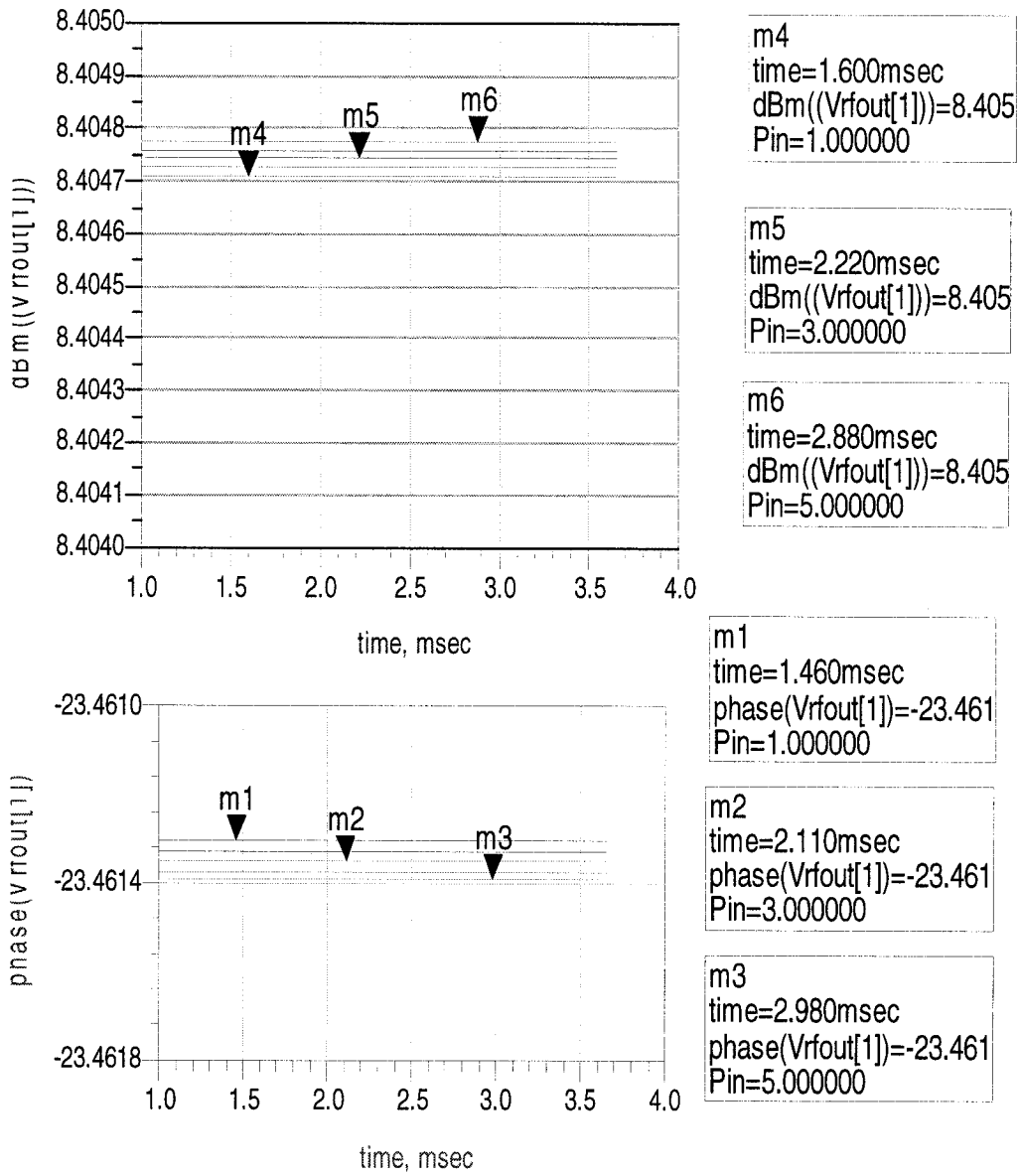


Figure 3- 35 AGC simulation result: RF output vs input

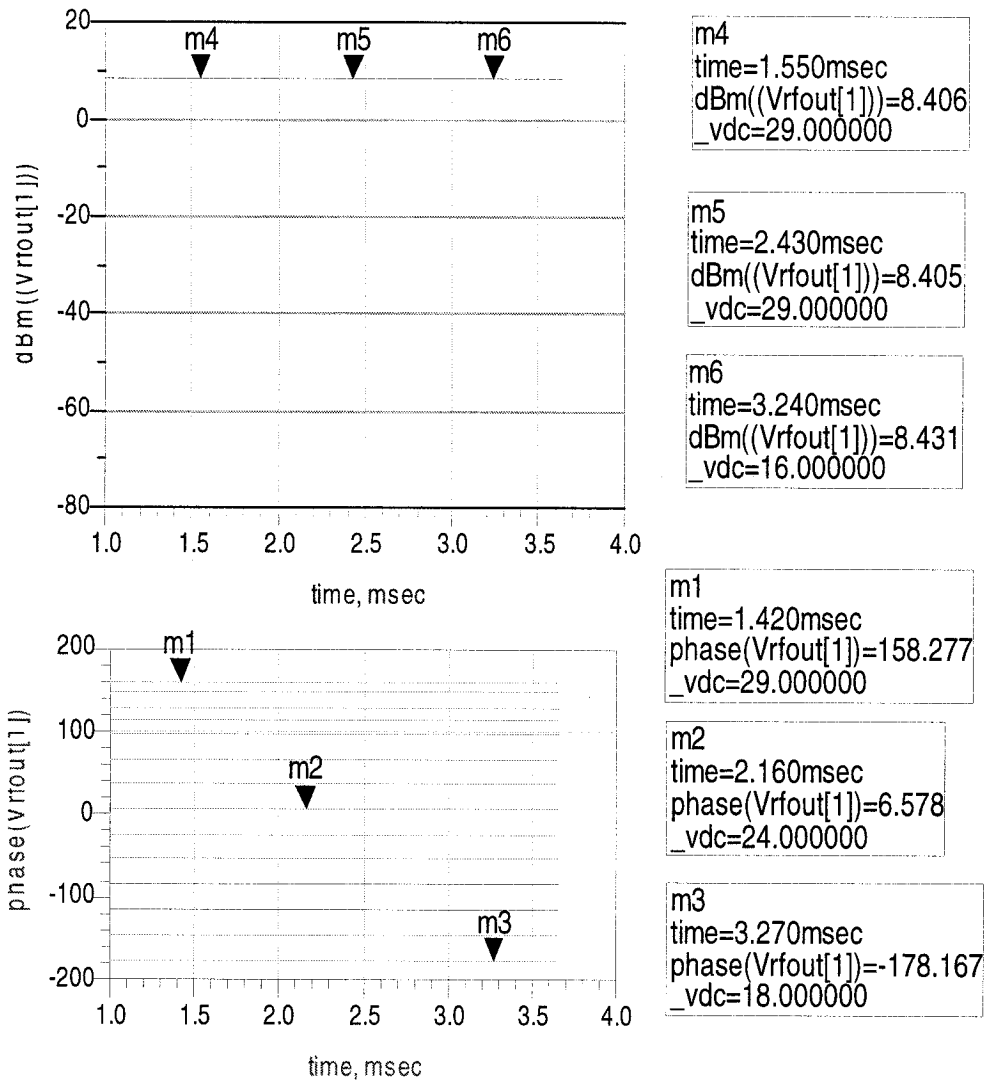


Figure 3- 36 AGC simulation result: RF output vs Vbias of phase shifter

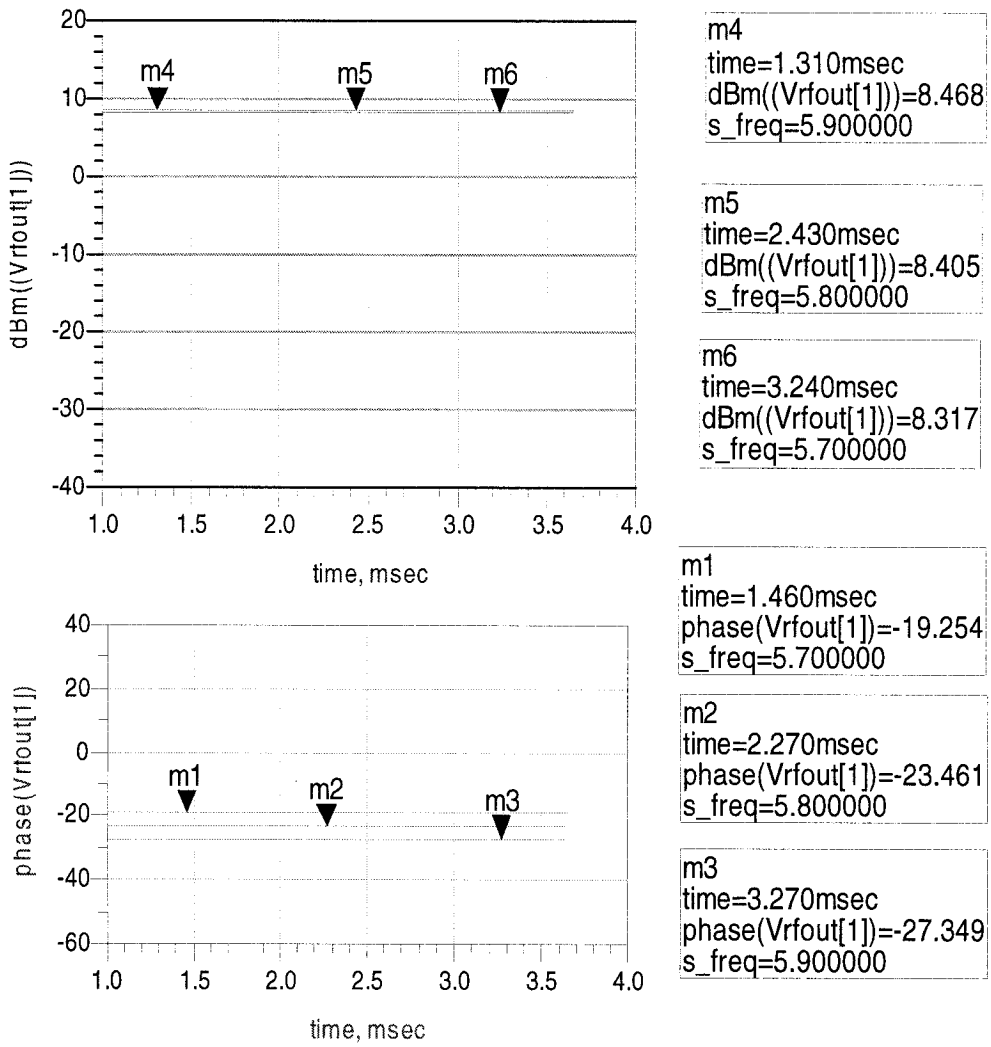


Figure 3- 37 AGC simulation result: RF output in different frequency

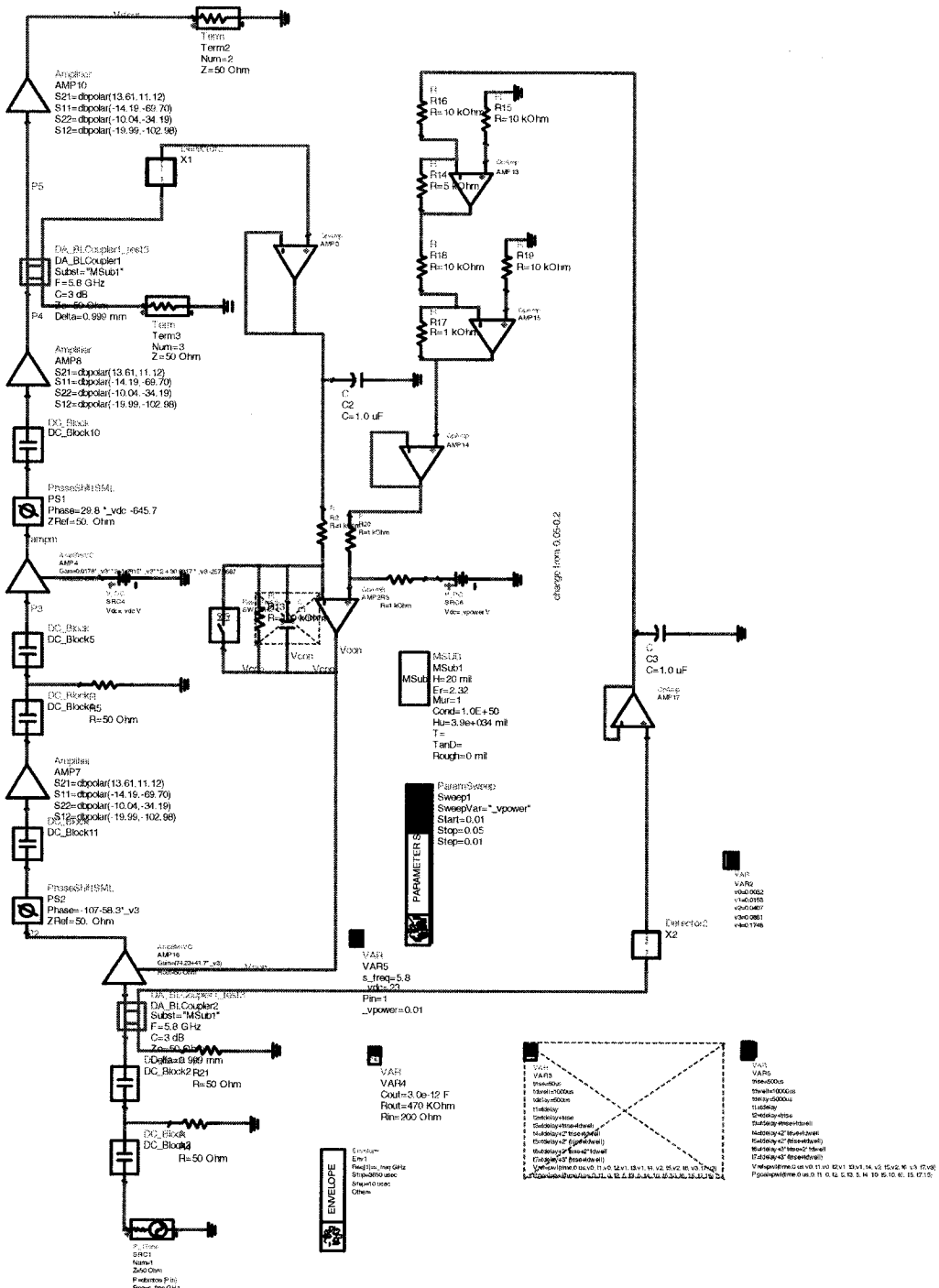


Figure 3- 38 Input tracing AGC ADS simulation circuit

Figure 3-38 shows the input tracing AGC ADS model circuit's structure. Here we also use the envelope simulation method to simulate the circuit's functionality. By varying the phase shifter's bias voltage V_{dc}, gain reference voltage V_{ref} and the input power P_{in}, we can trace the behavior of the output voltage.

From the simulation results in Figure 3-39 to Figure 3-42 we can find:

(1) When changing bias of the phase shifter, the output phase changed but power remains almost constant;

(2) A change in V_{ref}, does not influence the phase of V_{out} but increase its power.

(3) When we change input power, the output power follows the change almost linearly after the system become stable.

(4) Gain and phase change slightly when the working frequency varies.

Compare this result to Figure 3-33, we can find: In AGC circuit, a change in input power does not affect the output power, whereas in input tracing AGC system the output power follows variation of input power.

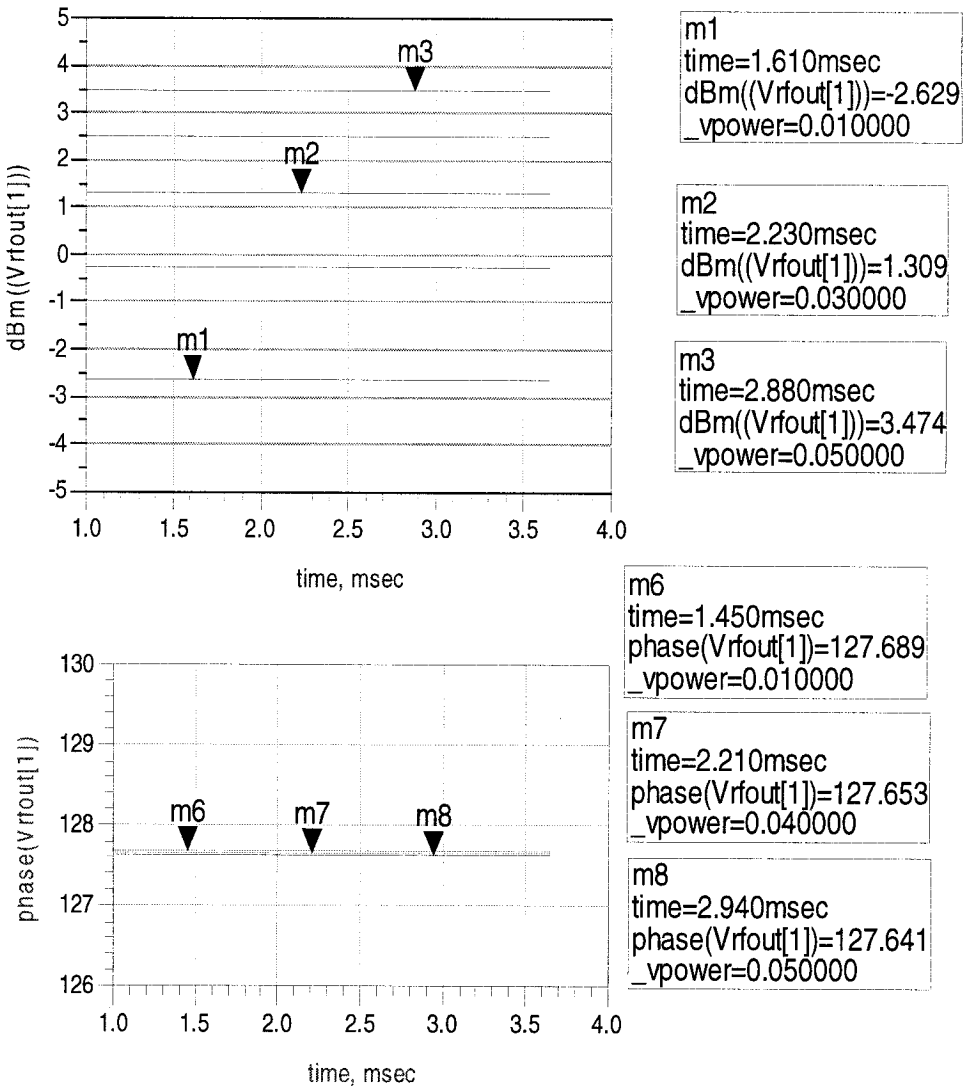


Figure 3- 39 Input tracing AGC ADS simulation result: RF output vs Vref of gain

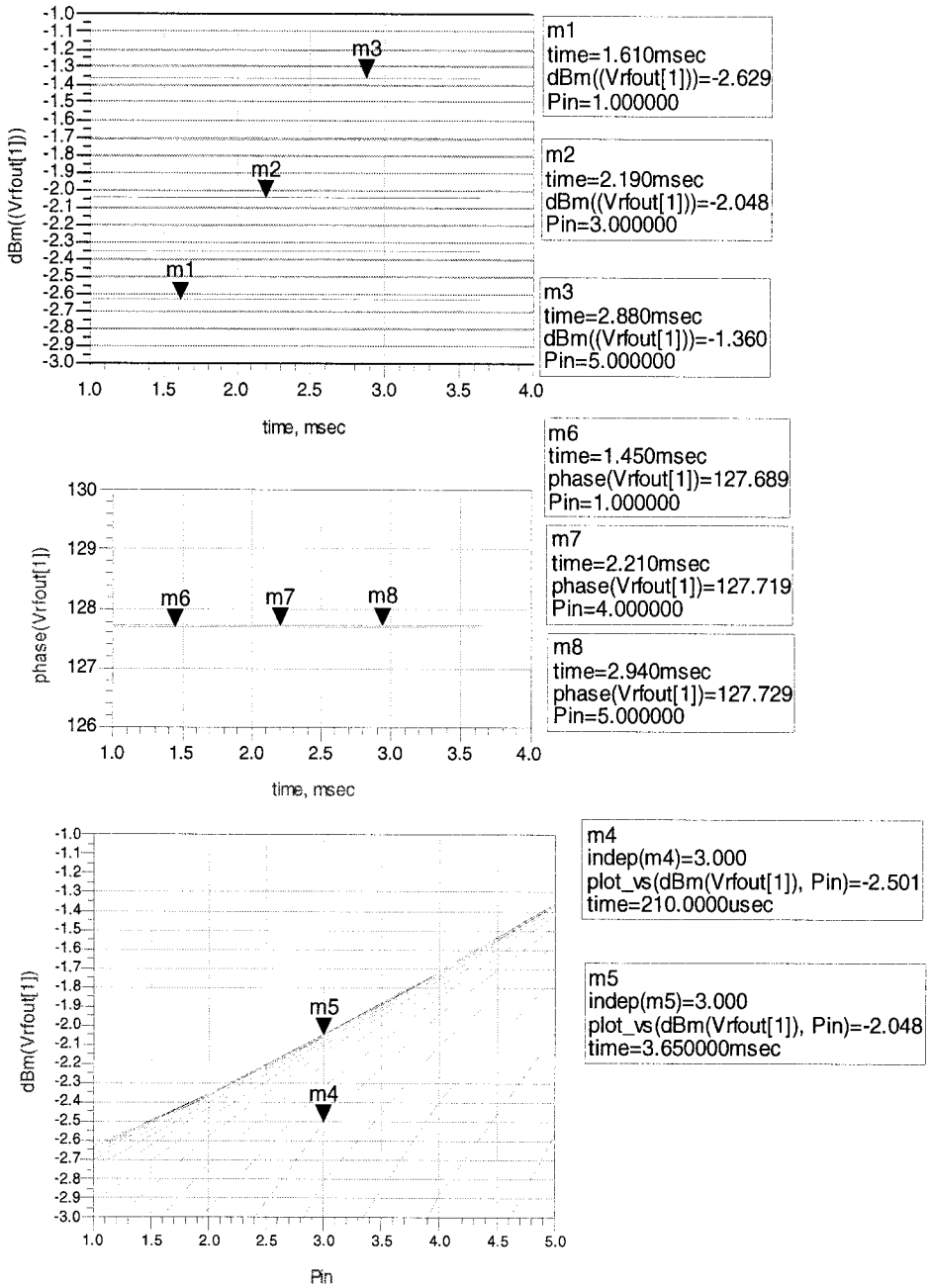


Figure 3- 40 Input tracing AGC simulation result: RF output vs input

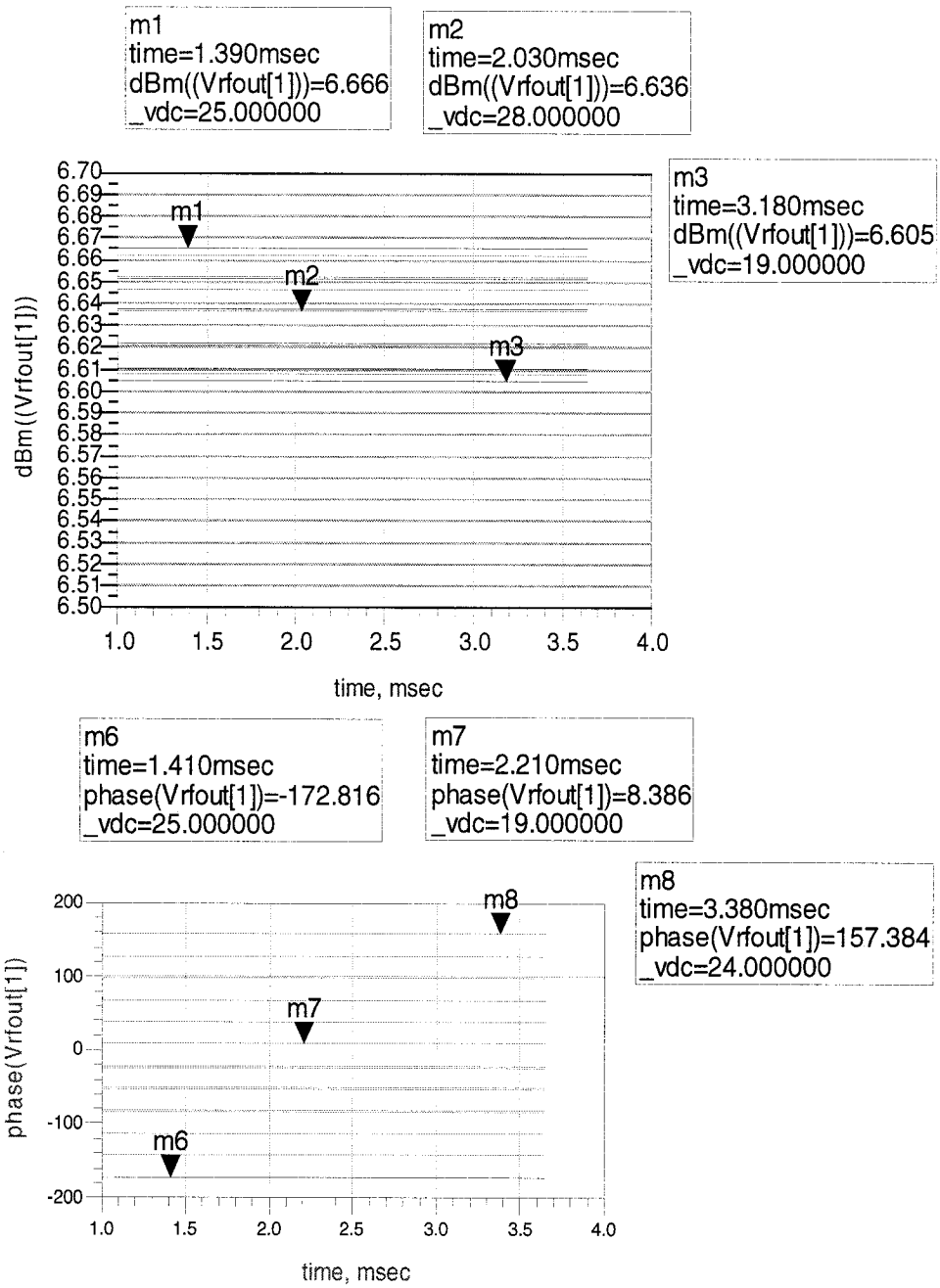


Figure 3- 41 Input tracing AGC simulation result: RF output vs Vbias of phase shifter

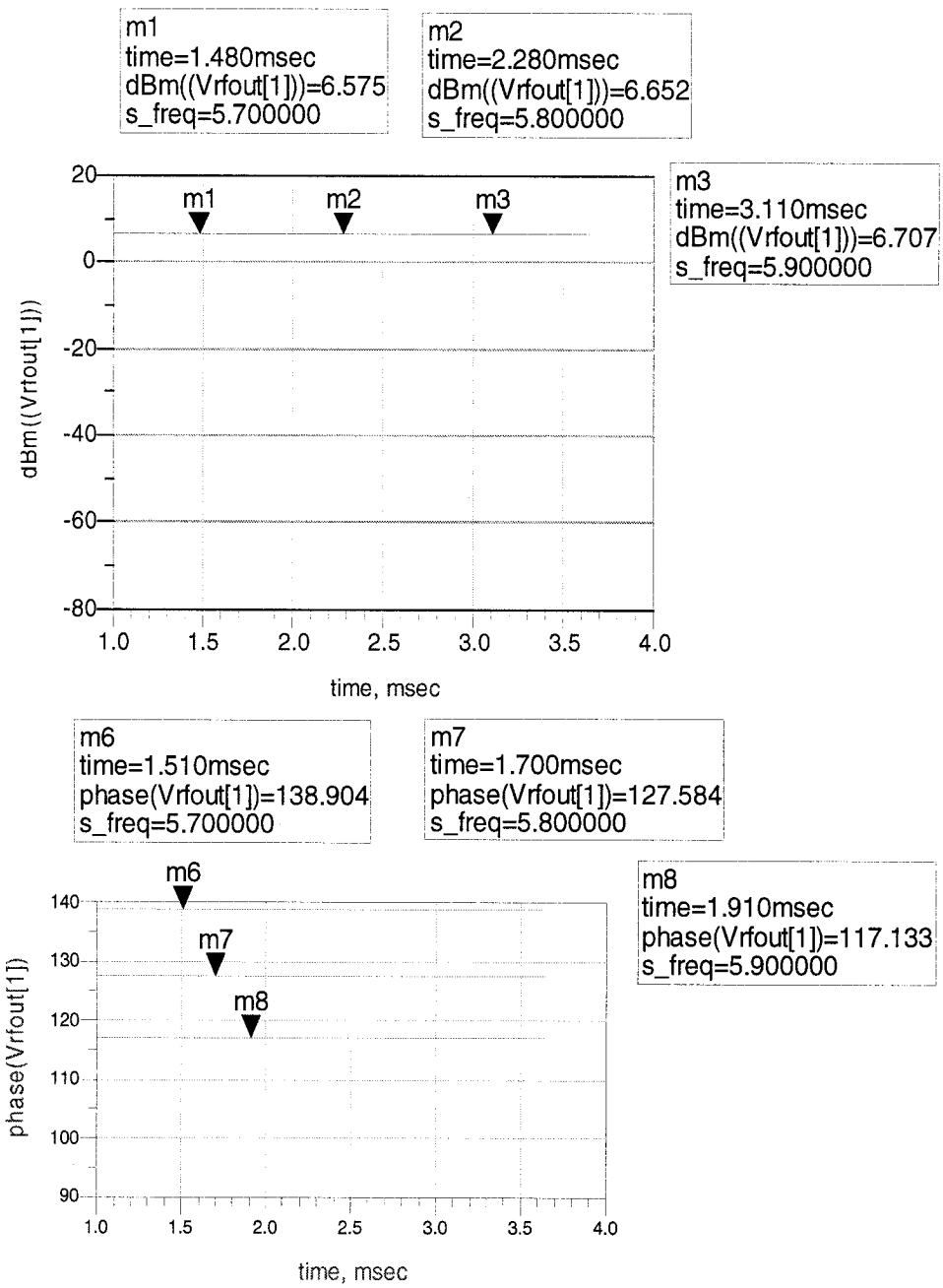


Figure 3- 42 Input tracing AGC simulation result: RF output in different frequency

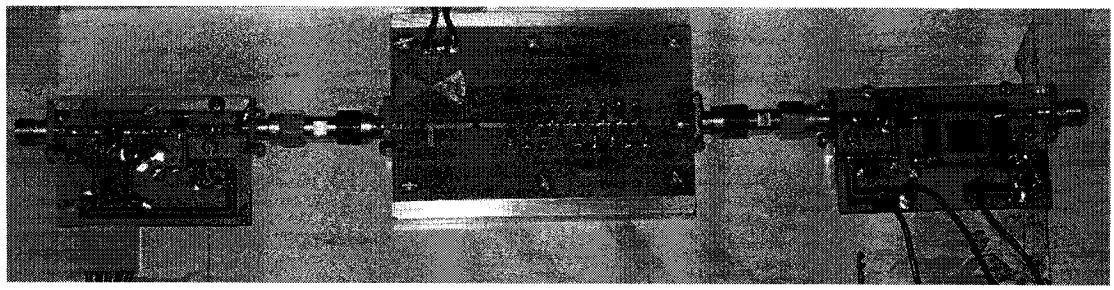


Figure 3- 43 AGC implement circuits

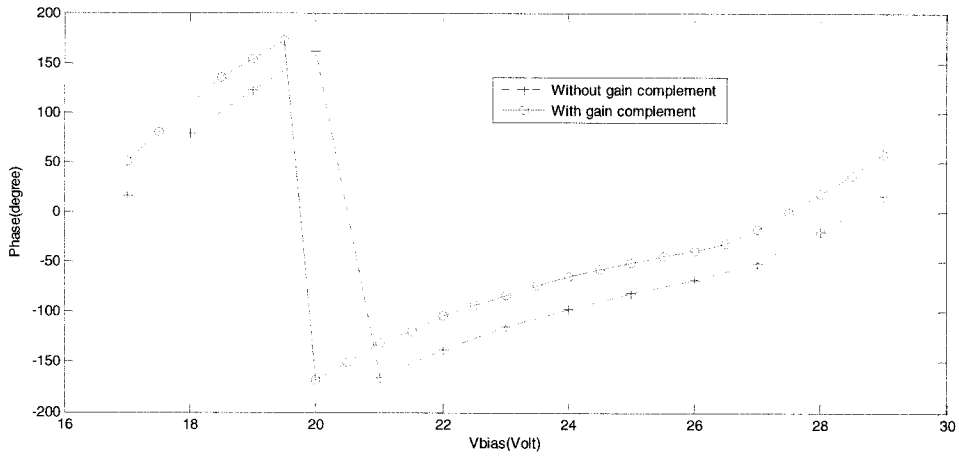


Figure 3- 44 Phase of S21 with and without gain compensation at 5.8GHz

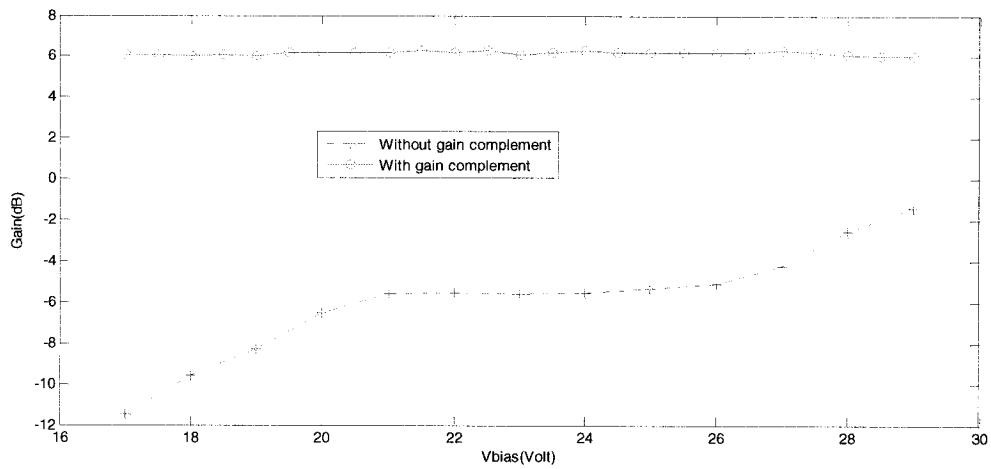


Figure 3- 45 Amplitude of S21 with and without gain compensate at 5.8GHz

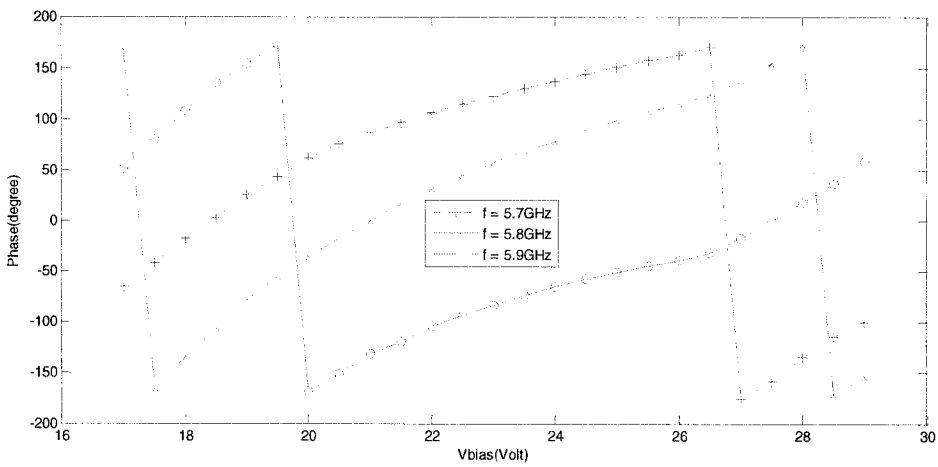


Figure 3- 46 Phase of S21 at different frequency after gain compensation

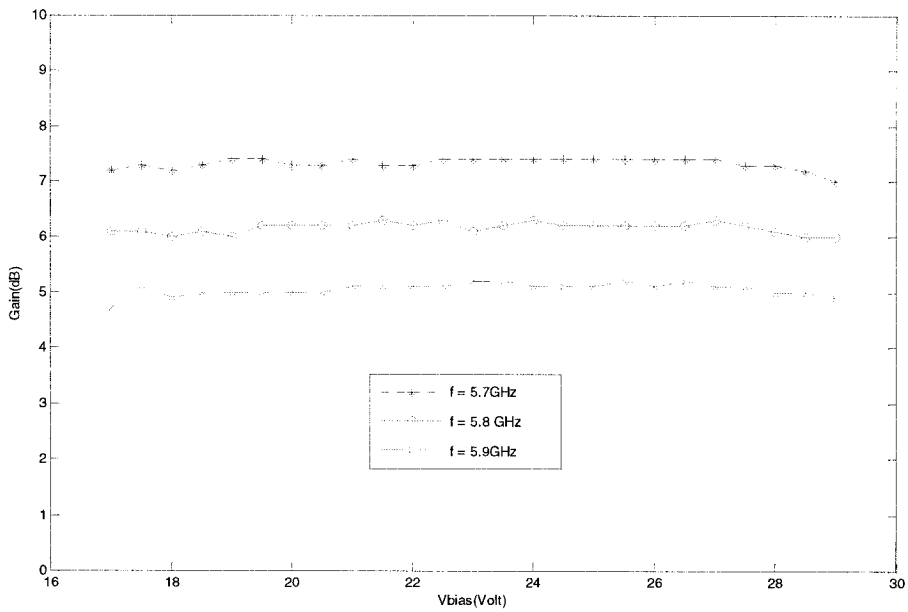


Figure 3- 47 Amplitude of S21 at different frequency after gain compensation

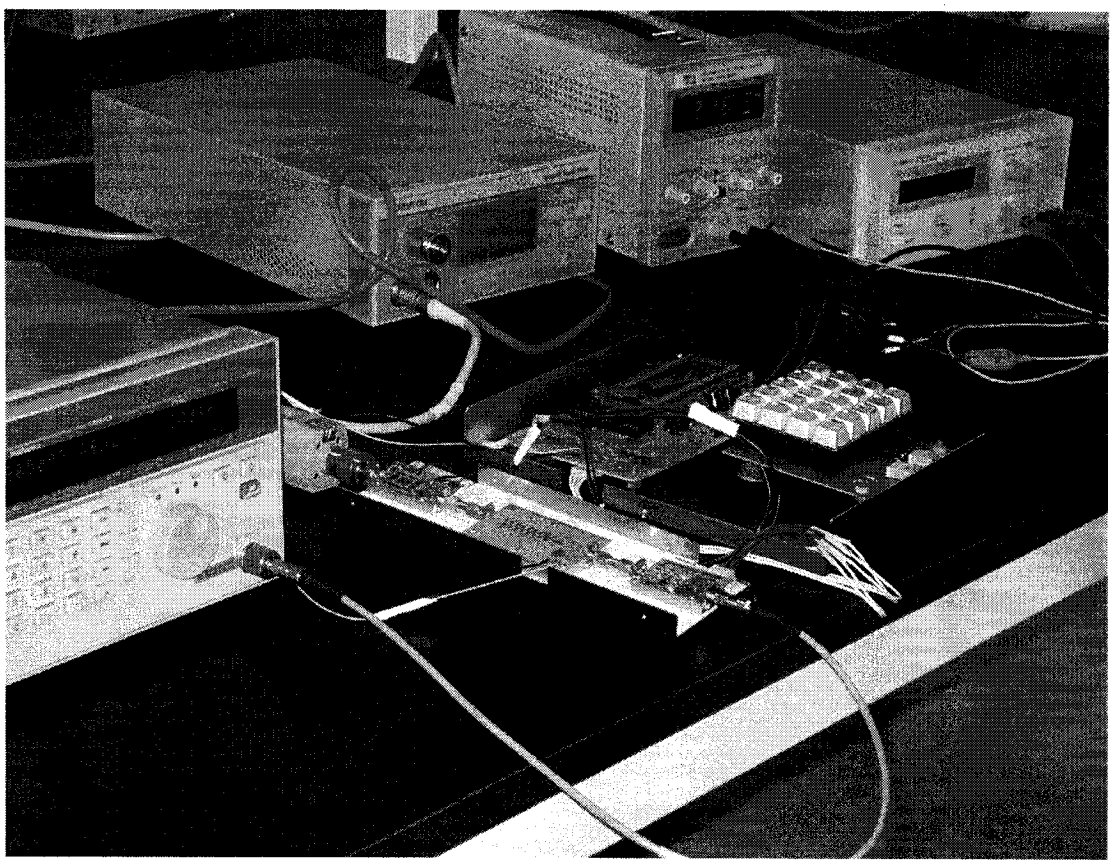


Figure 3- 48 Flat gain phase shifter test diagram

Figure 3-43 to Figure 3-48 show the implemented and tested circuits and their test results. From these results we observe:

(1). A flat gain phase shifter with the phase can be changed to 360° is realized.

(2).The gain ripple is compressed from 10dB to ±0.2dB.

(3).Phase and gain show some variation when the working frequency is changed. The measured change is larger than the value obtained from ADS simulations.

Chapter 4. DIGITAL CONTROL OF PHASE SHIFTER

4.1. Microcontroller controlled phase shifter

From Figure 1-2 we can see that the phase needs to be shifted continually. To realize a computer controlled automatic measurement, we need to digitally control the phase shifter. As shown in Figure 1-5, the most convenient method is using a microcontroller circuits to obtain signal power and frequency data and then to control system phase and gain. A computer can send commands to the microcontroller through an RS-232 interface to control the measurement system. Figure 4-1 shows the microcontroller circuits.

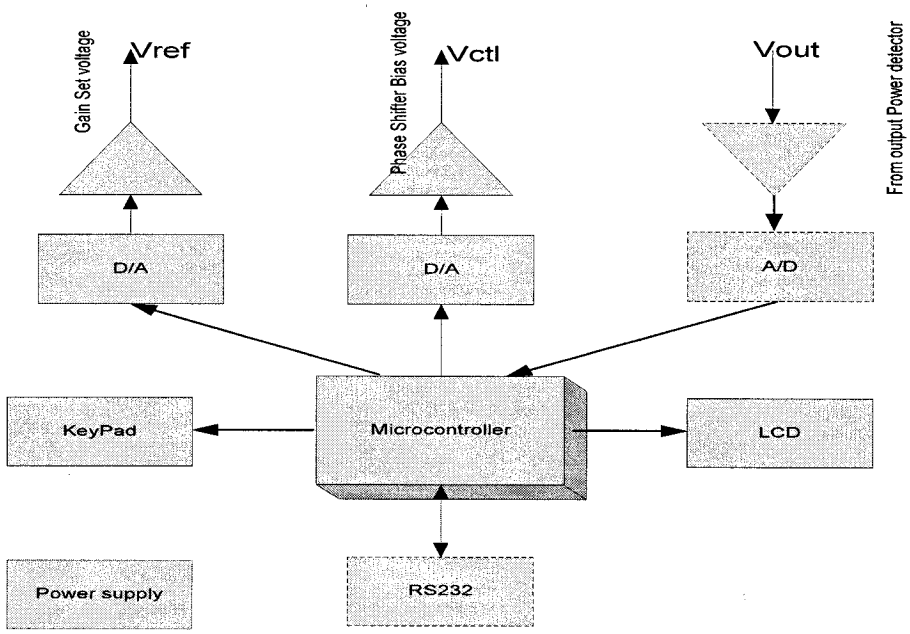


Figure 4- 1 Phase shifter microcontroller control circuit's structure.

As a special feature, in our system it is possible to enter the desired phase and gain value through a keypad. The RS-232 interface for data transfer between the PC and the

microcontroller is not implemented but ready to be added in the future. The actual circuits are shown in Figure 4-2

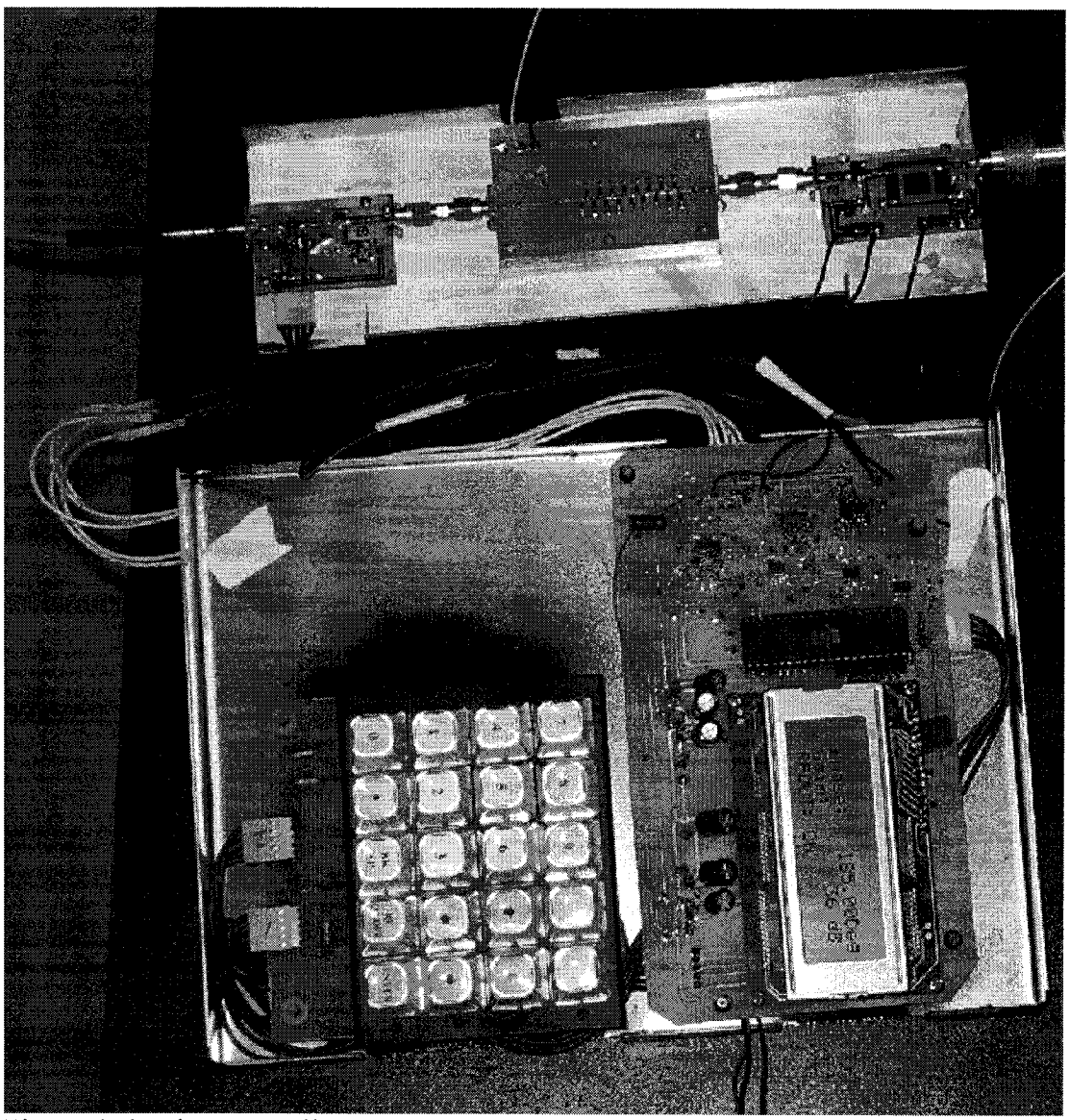


Figure 4- 2 Microcontroller controlled phase shifter.

4.2. Controller Circuits

Figure 4-3 shows the controller circuits. It includes a +/- 5V power supply, the

89C52 microcontroller and its peripherals, a Keypad, an LCD displayer, gain setup and control circuits, the phase shifter control circuit and the power detector A/D circuit.

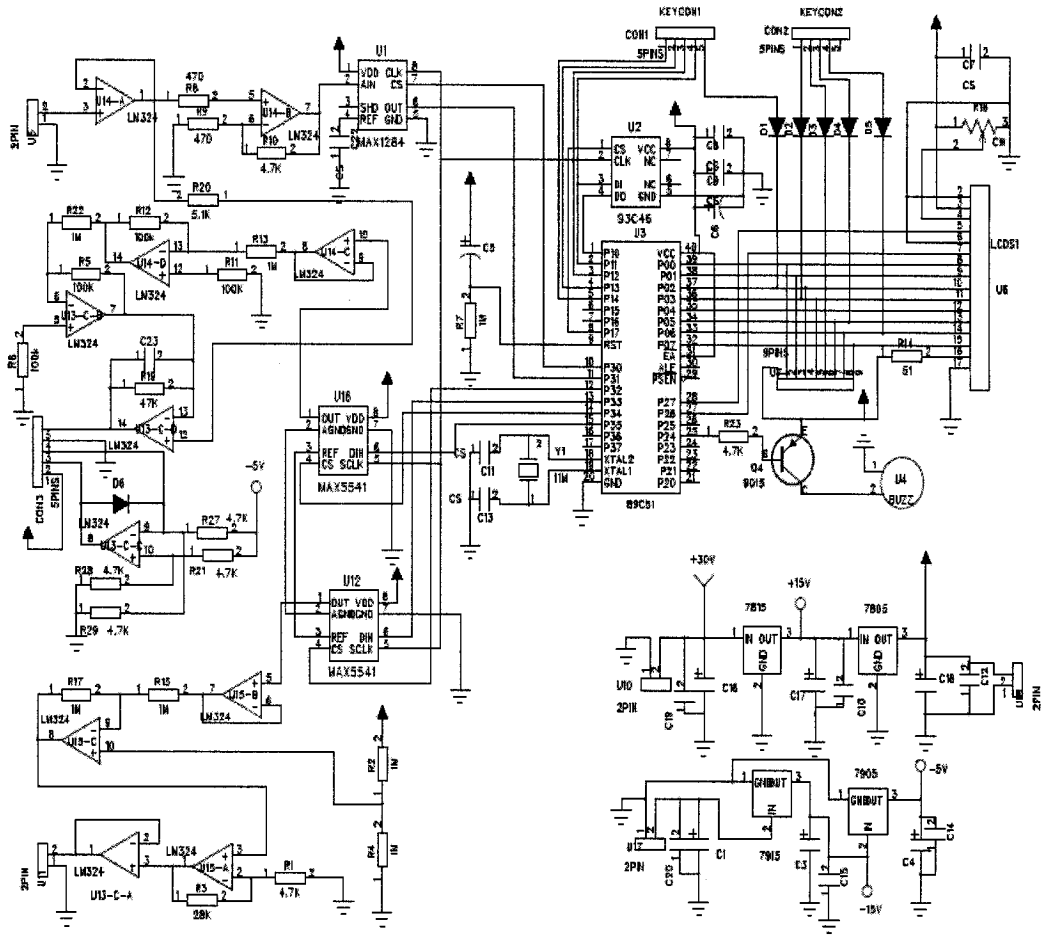


Figure 4- 3 Schematic of microcontroller control circuits.

4.2.1 Power supply circuits.

The phase shifter requires a maximum of +30V controlled DC power. If we use an OP amplifier to control it, we need a supply voltage of around +32V this OPA. The RF amplifier Gali29 needs a +15V power supply, whereas the microcontroller and A/D, D/A, EEPROM, LCD and Keypad circuits need +5V DC supply. The HMC345MS8G

variable attenuator requires a 0 to -2.5 V controlled DC supply, thus we need +/-5V DC supply for the control OP. The DC power supply circuits can be designed as shown in Figure 4-4. Voltage regulators of type 7815, 7805, and 7905 are used to supply +15V, +5V and -5V. In addition a 7915 is introduced as a protection of the 7905 IC in the case the negative voltage becomes too high.

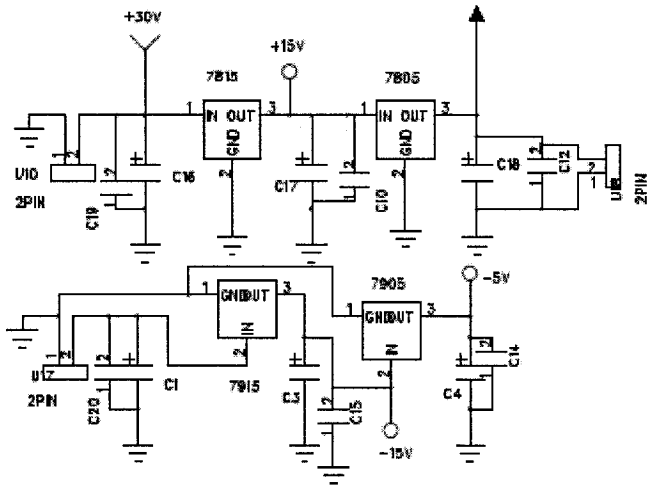


Figure 4- 4 DC power supply circuits.

4.2.2 Phase shifter control circuits.

Figure 4-5 shows the phase shifter control circuits. We use high input impedance and low output impedance differential circuits for the phase shifter control circuits. A D/A converter is used to generate a reference voltage of 0 to 2.5V (V_{ref}) voltage and the differential OP generate 15V to 30V phase shifter control voltage.

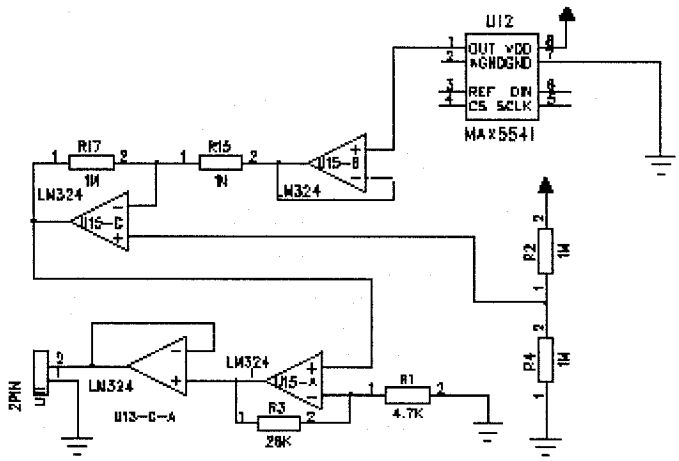


Figure 4- 5 Phase control circuits.

We use a MAX5541 IC as our digital-to-analog converter (DAC). It is a serial-input, voltage-output, 16-bit monotonic DAC that operates from a single +5V supply. The DAC output range is from 0V to Vref with 1LSB offset error.

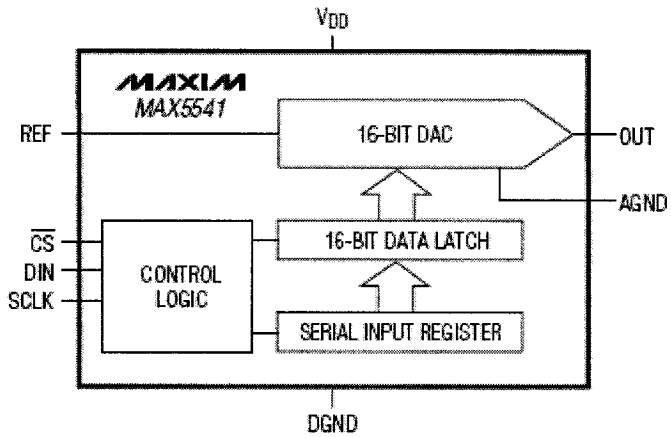


Figure 4- 6 MAX5541 functional diagram

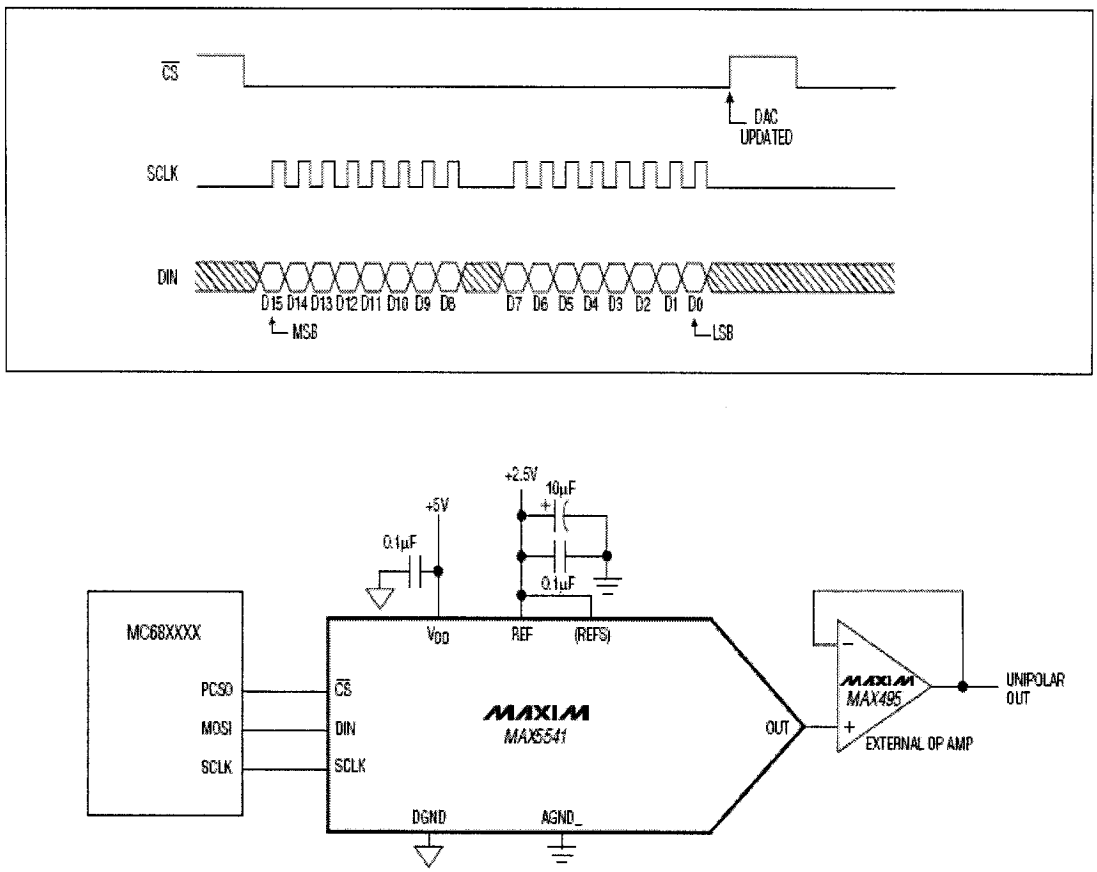


Figure 4- 7 MAX5541 Typical Operating Circuit and 3-Wire Interface Timing Diagram.

DAC LATCH CONTENTS MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111 1111	$V_{REF} \times (65{,}535 / 65{,}536)$
1000 0000 0000 0000	$V_{REF} \times (32{,}768 / 65{,}536) = {}^{1}/_{2}V_{REF}$
0000 0000 0000 0001	$V_{REF} \times (1 / 65{,}536)$
0000 0000 0000 0000	0V

Figure 4- 8 MAX5541 Unipolar Code Table.

From Figure 4-8, we can see that one bit represents 360°/65536 =0.0055°, so in theory the phase shifter can be controlled very precisely.

4.2.3 Gain control circuits.

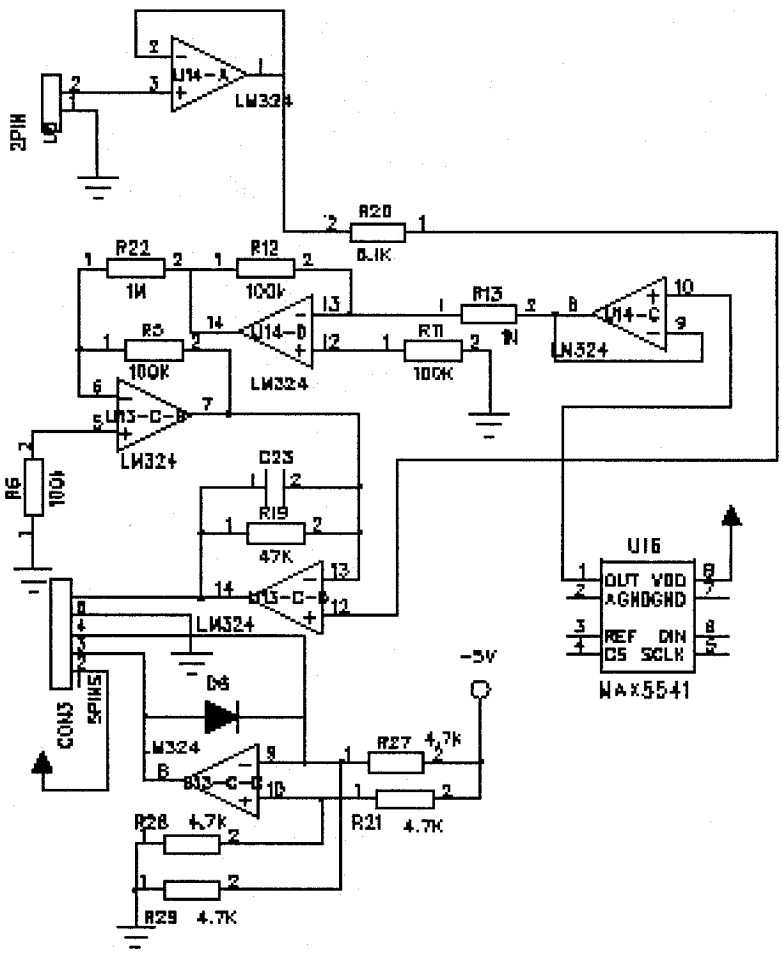


Figure 4- 9 Gain setup and feedback control circuits.

The value of the gain input coming from the microcontroller is converted by the DAC and amplified by an OPA, and then it is compared to the detected power and then amplified to control the variable attenuator. The capacity C23 is the most important parameter because it determines the response timing constant. The optimized value is around 1uF.

4.3. Microcontroller Program Flow Charts

The microcontroller fulfills the following tasks: 1) Read the input value of shift phase and the system gain from the keypad and displays them on LCD displayer. 2) Read/write the EEPROM to load or store the data for reusing them. 3) Control the DACs to output phase and gain to the OP amplifiers. The program flow chart that implements these tasks is shown in Figure 4-8.

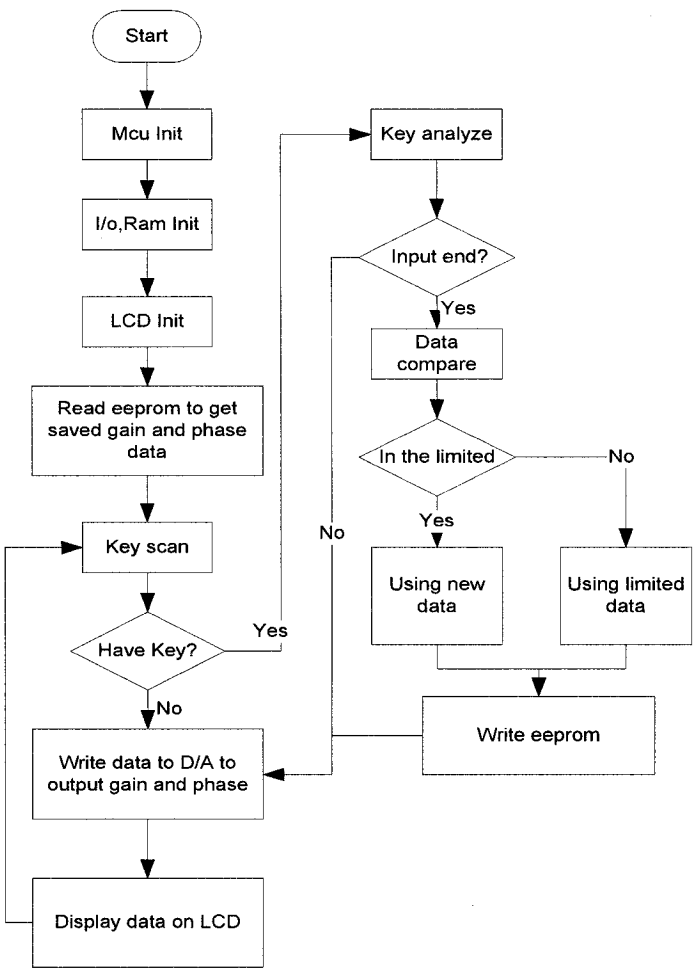


Figure 4- 10 Microcontroller program flow charts

CONCLUSIONS AND FUTURE WORK

A microcontroller controlled flat gain phase shifter has been implemented. The microcontroller is an 8 bit 89C52, the phase shifter is realized as a varactor loaded line structure. The gain loss while shifting phase is compensated by an AGC circuit. ADS simulations and measurements have shown that:

(1). the phase can be changed up to 360° controlled by a microcontroller.

(2). the gain ripple is compressed from 10dB to ±0.2dB when phase shifting from 0 to 360°.

(3). the gain can be regulated by a microcontroller step by step or enter directly.

(4). Pout/Pin remains constant while shifting phase if using an input tracing AGC.

This phase shifter can be used independently. It can also be used as a slave device to control phase and gain from a computer by adding an RS232 interface to form a computer controlled AAPMS.

To realize such a system shown in Figure 1-4, the following additional works have to be considered in the future.

1) The microcontroller circuits needs to be revised: a RS-232 interface has to be added together with its software.

2) The performance of the phase shifter currently used is poor in terms of insertion loss and return loss. Although offers compensation, the insertion loss will visibly not

affect the system. However it will reduce the possible regulation range. Figure 3-4 shows the regulating range depending on the gain change. If the phase shifter does not work well, we need to consider redesigning it according to the procedure in chapter 2.

3) The input tracing AGC is not implemented in our circuit; it may need to be added in the future.

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