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NUMERICAL CALIBRATION TECHNIQUES AND APPLICATIONS OF PLANAR INTEGRATED MICROWAVE STRUCTURES

LIN LI
DÉPARTEMENT DE GÉNIE ÉLECTRIQUE
ÉCOLE POLYTECHNIQUE DE MONTRÉAL

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Cette thèse intitulée:

NUMERICAL CALIBRATION TECHNIQUES AND APPLICATIONS OF PLANAR INTEGRATED MICROWAVE STRUCTURES

présenté par : LI Lin

en vue de l'obtention du diplôme de: Philosophiae Doctor

a été dûment accepté par le jury d'examen constitué de :

M. BOSISIO Renato G., M.Sc., président

M. WU Ke, Ph. D., membre et directeur de recherche

M. CALOZ Christophe, Ph. D., membre

M. RONI Khazaka, Ph. D., membre

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RÉSUMÉ

Dans cette thèse, des techniques de calibration numérique thru-reflect-line (TRL) et thru-resistor (TR) sont proposées pour éliminer l'effet de discontinuité du port qu'entraîne la source d'excitation discrète de l'algorithme de la Méthode des Moments (MoM) déterministe. Ainsi, le modèle équivalent au circuit planaire peut être extrait correctement. Ces techniques sont compatibles avec les logiciels de simulation électromagnétique commerciaux.

A l'aide des techniques de calibration numérique, les modèles de circuit des discontinuités de port sont extraits rigoureusement. Les erreurs causées par la discontinuité de port sont analysées en se basant sur la transformation des paramètres S en paramètres Y/Z. La technique de calibrage numérique proposée est utilisée pour extraire les modèles de circuit du circuit-ouvert microruban, de la ligne espacée microruban, du saut d'impédance de la ligne microruban, du condensateur interdigital (CID) et des lignes microruban. En se basant sur les modèles de circuit complets, un filtre passe-bas, un résonateur et un filtre passe-bande utilisant une ligne à onde lente sont conçus. Il a été démontré que les modèles complets sont critiques pour la conception de circuits intégrés sur la base de stratégies de conception bien établies pour l'analyse et l'optimisation des circuits. Un nouveau combineur de puissance planaire quasi-optique est proposé. La technique de calibrage numérique est utilisée pour extraire les paramètres de la structure de distribution/combinaison de puissance.

ABSTRACT

In this work, a set of numerical thru-reflect-line (TRL) and thru-resistor (TR) calibration techniques are proposed and combined with commercial planar electromagnetic (EM) simulation software. Such numerical calibration techniques are used to eliminate port discontinuities brought by the lumped current/voltage exciting sources in a deterministic method-of-moments (MoM) algorithm. Therefore, accurate equivalent full-wave-based circuit models of the planar discontinuities can be extracted and established for CAD and optimization purposes.

The TRL calibration makes use of three standards, namely, through, reflect and line connections. The TRL calibration standards are easy to realize in both practical circuit measurements and numerical EM simulations. The error boxes, which consist of the port discontinuity effects and guided (or feed) line sections from the exciting source planes to DUT (device-under-test), can be set up by using these standards. Then, accurate parameters that electrically characterize the DUT can be obtained. In a TRL calibration procedure, the characteristic impedance of the line standard should be known exactly a priori. To obtain this characteristic impedance for the TRL calibration, a resistor standard is introduced in this work as impedance reference for extracting a three-dimensional (3D) characteristic impedance of the line standard. Generally, the numerical TRL calibration is bandwidth-limited and it is difficult to extend to a scenario of multi-port calibration. To remedy this situation, we have proposed numerical 2-port TR and multi-parallel port TR calibration techniques. The 2-port TR calibration procedure

deploys through and resistor standards while the multi-parallel port TR calibration uses through, match and multi-resistors standards. Comparing results obtained from our proposed numerical calibration techniques with published results as well as the static modeling results has validated the proposed numerical calibration techniques.

With the help of a numerical calibration technique, field-based equivalent circuit models of the port discontinuities are rigorously extracted. Generally, the circuit model of a port discontinuity can be represented by a shunt capacitor and a series inductor. Values of those elements in the circuit model might unfortunately be different when different exciting schemes are applied. From the analysis that is based on a transformation from S parameters to Z or Y parameters, we can observe that a small port discontinuity change can generate huge errors in the extracted equivalent circuit elements of planar circuits and this verily confirms that the calibration is absolutely necessary to remove the errors.

The proposed numerical calibration techniques are implemented to extract the equivalent full-wave circuit models of various microstrip discontinuities such as open, step and gap. Also, the 3D characteristic impedance of microstrip line and microstrip couple line is calculated. Based on the extracted full-wave circuit models of those microstrip circuit elements, a microstrip low-pass-filter and a microstrip resonator are designed. Measurement results are in a very good agreement with the predicted ones. With the calibrated circuit models of planar discontinuities, the design of planar circuit becomes more accurate than a design based on static models and more efficient than a design based on EM simulations.

The proposed numerical calibration techniques are also implemented to extract the equivalent circuit model of Interdigital-Capacitor (IDC) in CPW interface. The circuit model of IDC can be represented by one series capacitor (the dominant parameter which is related to coupling), two shunt capacitors (which are much smaller than their series counterpart), and other loss-related resistors and conductors. By using the circuit model of the IDC, we can realize a slow wave line by loading IDC onto a CPW line. The slow-wave line has a much smaller phase velocity than its bold counterpart. A 2-pole band-pass-filter (BPF) is designed by using the IDC as converter and using the slow wave line as half wavelength resonator. The design and simulation of this BPF is based on lumped-element network topologies. Measured results have confirmed the extracted full-wave circuit model of the IDC as well as the model of the slow wave line loaded with IDC.

The numerical calibration technique is also used to extract the parameters of a novel planar power distributing/combining structure. An approximate circuit model of the power distributing/combining structure is proposed. The power distributing/combining structures are realized by the transition between an oversized microstrip line and parallel multi-microstrip lines. By using the planar power distributing/combining structures, a quasi-optic power combiner is designed, which operates over 25-31 GHz, using 4 amplifier ICs. Measured results show a good agreement with simulated ones, and a combining efficiency 79.5% is obtained at 25 GHz. The whole quasi-optical power combiner is in a planar form, and of course it can be fabricated with a conventional planar circuit technology. Therefore, no complicated mechanical

assembling is needed, and the circuitry is very compact. It is very convenient for the power combiner to interconnect with other planar circuits. This quasi-optical power combiner manifests how a quasi-optical combiner circuit works.

CONDENSÉ EN FRANÇAIS

Dans cette thèse, des techniques de calibration numérique sont proposées pour éliminer l'effet de discontinuité du port qu'entraîne la source d'excitation discrète de l'algorithme de la Méthode des Moments (MoM) déterminée. Ainsi, le modèle équivalent au circuit planaire peut être extrait correctement.

0.1 Technique de calibration TRL numérique

La simulation de discontinuités planaires ou de façon plus générale, le Dispositif Sous Test (DST), s'effectue en appliquant une source d'excitation reliée au DST par un guide. La discontinuité de port se trouve entre le guide et la source d'excitation. Les sources d'erreurs comprennent le guide de transmission et la discontinuité du port. La procédure de calibrage TRL utilise trois types de standards: le *passe-tout*, le *réflecteur* et la *ligne*. Ces standards de calibration sont simples et faciles à réaliser à la fois pour la mesure et la simulation MoM.

On effectue la connexion des standards *passe-tout*, *réflecteur* et l*igne* aux plans de référence du DST, R1 et R2, et on simule les paramètres S pour ces trois cas aux plans de référence de la source d'excitation, P1 et P2. On transfert ensuite les paramètres S en paramètres T. Les paramètres des boîtes d'erreur du DST peuvent être calculés par l'entremise de l'algorithme TRL. La procédure de calibrage est directe et permet d'obtenir les termes d'erreur sous forme d'expressions explicites. Le modèle de circuit complet de la discontinuité planaire peut être extrait des paramètres du DST.

Le modèle équivalent de deux circuits ouverts microruban sur des substrats différents, alumine ($\varepsilon_r = 9.9$, $W = h = 0.635mm$, 2-5 GHz) et Duroid 5880 (ε_r = 2.2, h = 0.254mm, W=0.762mm, 2GHz to 40GHz) sont extraits par la technique de calibrage TRL. Le logiciel IE3D est utilisé pour la simulation électromagnétique. Les résultats provenant du calibrage TRL ne présentent que très peu de variation en fréquence et sont fortement en accord avec ceux obtenus des formules [38] et [39] alors que les résultats sans calibrage fluctuent de bas en haut avec l'augmentation de la fréquence.

Pour déterminer l'impédance caractéristique en trois dimensions du standard *ligne*, un standard alternatif appelé "standard de résistance" est introduit dans le calibrage TRL numérique [33]. L'impédance caractéristique du standard *ligne* est définie par Z. La matrice T du standard *ligne* est :

$$N_2 = \begin{bmatrix} ch(\gamma l) - \frac{Z^2 + Z_0^2}{2ZZ_0} sh(\gamma l) & \frac{Z^2 - Z_0^2}{2ZZ_0} sh(\gamma l) \\ -\frac{Z^2 - Z_0^2}{2ZZ_0} sh(\gamma l) & ch(\gamma l) + \frac{Z^2 + Z_0^2}{2ZZ_0} sh(\gamma l) \end{bmatrix} = \begin{bmatrix} 1 & a \\ a & 1 \end{bmatrix} \begin{bmatrix} e^{-\gamma l} & 0 \\ 0 & e^{+\gamma l} \end{bmatrix} \begin{bmatrix} 1 & a \\ a & 1 \end{bmatrix}^{-1}$$

$$, \quad a = \frac{Z - Z_0}{Z + Z_0} \tag{0.1}$$

Cependant, si l'impédance caractéristique du standard *ligne* n'est pas précisément connue, la procédure de calibrage TRL ne peut être complétée. De plus, si l'impédance caractéristique du standard *ligne* est connue mais erronée, de faux paramètres seront extraits du DST. L'impédance caractéristique du standard *ligne* ne peut être obtenue que par le coefficient de réflexion Γ du standard *résistance*.

L'impédance caractéristique d'une ligne microruban sur un substrat d'alumine est calculée. Les résultats obtenus démontrent que la partie réelle de l'impédance caractéristique du standard *ligne* est équivalente à celle rapportés dans [33]. La partie imaginaire de l'impédance caractéristique est due aux pertes du standard et est de beaucoup inférieure à la partie réelle.

0.2 Technique de calibrage numérique TR

La technique de calibrage TR est proposée pour extraire le modèle de circuit de discontinuités planaires sur une large bande de fréquence. Les boîtes d'erreur sont supposées être symétriques et réciproques. La technique de calibrage TR utilise deux standards : *passe-tout* et *résistance*. Le standard *résistance* a pour valeur R. L'algorithme de calibrage TR peut être dérivé en se fondant sur les paramètres Y ou T.

Des circuit-ouverts microruban sur deux différents substrats sont étudiés en utilisant le calibrage TR à deux ports. La valeur de R est 50 ohms. Le résultat de la capacitance de bord obtenu du calibrage TR est en accord avec le résultat obtenu du calibrage TRL. La validité de la technique de calibrage TR est donc prouvée.

Le calibrage TR à ports multi-parallèles utilise trois standards: *passe-tout*, *adapté* et *multi-résistance*. En simulant le réseau connecté aux standards, il est possible de retirer les boîtes d'erreur que sont les lignes multi-guides et la discontinuité du port entre les ports d'excitation et les lignes multi-guides. Donc, les paramètres du DST peuvent être obtenus. L'algorithme du calibrage TR multi-parallèle est fondé sur les paramètres T. L'exemple de lignes couplées sur un substrat Duroid 5880 est étudié. Les lignes couplées ont deux ensemble de constantes de propagation: une pour le mode paire et

l'autre pour le mode impaire. Les résultats obtenus du calibrage numérique TR multi-parallèle sont en accord avec les résultats statiques.

0.3 Discontinuité du port et analyse d'erreur

Pour obtenir le modèle de circuit de la discontinuité de port entre le port d'excitation et le guide microruban, on utilise, au lieu du DST, la même section de ligne de transmission que le guide [20]. Puisque la ligne de transmission est physiquement identique au guide, la boîte d'erreur A peut être exprimée par

$$[T_A] = [T_P][T_l] \tag{0.2}$$

où [TP] est la matrice T de la discontinuité de port et [Tl] est la matrice T de la ligne de transmission. Par le calibrage numérique, on peut retirer la boîte d'erreur et obtenir les paramètres corrigés de la ligne de transmission, [Tl]. Ensuite, on peut calculer les paramètres de la discontinuité de port en retirant le guide de la boîte d'erreur. Tel qu'en [20], le modèle de circuit équivalent de la discontinuité de port peut être représenté par un condensateur parallèle et une inductance série (Les pertes infimes reliées à la résistance ou au conducteur sont négligées). Les modèles de circuit des discontinuités de port sur différents substrats (alumine ou Duroid 5880) sont extraits en utilisant plusieurs types de simulateurs électromagnétiques (Momentum d'Agilent ou IE3D de Zeland). On remarque que les valeurs des éléments du modèle de circuit de la discontinuité de port demeurent presque inchangées en fonction de la fréquence. Avec différents substrats ou différents logiciels de simulation électromagnétique, la valeur des éléments du modèle

diffèrent. Ceci s'explique par la différence entre les méthodes d'excitation (verticale ou horizontale, source de courant ou de tension) utilisées par les logiciels.

Les paramètres S de la discontinuité de port démontrent que la magnitude de S11 est très petite et que S21 est presque égale à 1. Cependant, si l'on désire extraire le modèle de circuit de la discontinuité planaire, la discontinuité de port peut entraîner une erreur importante. En regardant de plus près la transformation des paramètres S en Y/Z, on constate que le dénominateur des paramètres Y/Z atteint zéro sur certaines régions. Lorsque le dénominateur approche zéro, les erreurs des paramètres S calculées du circuit seront amplifiées ce qui résulte en d'importantes erreurs une fois converties en paramètres Z. Si la discontinuité de port n'est pas calibrée, la valeur des paramètres Y/Z présente une variation périodique autour de la valeur réelle. La variation périodique est imputable à la longueur de la ligne guide reliant le port d'excitation au DST. Les effets de la discontinuité de port sur un circuit ouvert et un saut d'impédance microruban sont démontrés. Les résultats indiquent que la procédure de calibrage est absolument nécessaire pour l'extraction précise du modèle de circuit.

0.4 Application aux discontinuités microruban

La technique de calibrage numérique proposée est utilisée pour extraire les modèles de circuits de lignes espacées série et à saut de largeur sur un substrat Duroid 5880. Pour cette application, la hauteur du substrat est de 0,254 mm et la plage de fréquence s'étend de 20 GHz à 40 GHz.

La largeur de la ligne microruban aux deux extrémités du saut varie de 0,254 mm à 1,524 mm. Puisque les impédances caractéristiques des deux côtés sont différentes, nous

devons utiliser deux procédures de calibrage TRL sur la base de différentes impédances de référence pour calculer les deux boîtes d'erreur, respectivement. Le modèle de circuit complet de la discontinuité de saut peut être exprimé par une admittance capacitive parallèle, deux impédances série inductives et les résistances et conductances reliées à la radiation [18]. Lorsque W2 est plus petit ou égal à 1,016 mm, les paramètres du modèle de circuit indiquent que lorsque la fréquence augmente, l'inductance Xp/ω et la capacitance Bg/ω ne varient presque pas (Xp/ω augmente légèrement mais Bg/ω décroît légèrement et ils démontrent les propriétés d'éléments discrets), et les pertes par radiation reliées à la conductance Gg augmentent. À mesure que la ligne W2 s'élargit Xp/ω, Bg/ω et Gg augmentent. Inversement, à mesure que la ligne plus mince W1 s'élargie, Xp/ω, Bg/ω et Gg diminuent. On observe également que plus le saut est important, plus grands seront Xp/ω, Bg/ω et Gg. Ceci s'explique par la transition du flux de courant de la direction longitudinale à transverse au bord de la ligne plus large près du saut, ce qui se traduit en une augmentation de la courbure de la densité de courant. Dans le cas où W2 serait égale à 1,524 mm, Xp/ω et Bg/ω varient de façon irrégulière lorsque la fréquence augmente. Ce phénomène est dû aux conditions d'application du modèle discret. En effet, le saut ne peut être considéré sous forme d'éléments discrets qu'à la condition que sa dimension soit beaucoup plus petite que la longueur d'onde.

La largeur de la ligne microruban de l'espacement est de 0,762 mm et l'espacement varie de 0,025 mm à 0,508 mm. Le modèle équivalent complet de l'espacement microruban peut être représenté par deux admittances parallèles capacitives, une admittance capacitive parallèle, une résistance et une conductance reliée aux pertes par

radiation [19]. Les résultats obtenus du calibrage numérique démontrent que lorsque la fréquence augmente, les conductances G1 et G2 reliées à la radiation augmentent, C1 demeure presque constant et C2 décroît légèrement. Lorsque la largeur de l'espacement augmente, C1 et G1 augmentent alors que C2 et G2 décroissent, indiquant une diminution de l'effet de couplage.

En se basant sur les modèles de circuit complets de l'espacement et de saut de la ligne microruban, un filtre passe-bas et un résonateur opérant en bande Ka sont conçus. Les circuits sont analysés tel un réseau formé par la cascade de lignes et de discontinuités microruban. La simulation et l'optimisation des circuits deviennent directes et très facile. La validité des modèles de circuits extraits est démontrée par des résultats de mesure. Les modèles complets de circuit extraits procure une méthode de conception efficace et précise.

0.5 Conception d'un filtre utilisant la ligne à onde lente

Le condensateur interdigital (CID) sur guide coplanaire (GCP) est étudié en utilisant les techniques de calibrage numérique et le modèle extrait est implanté pour la conception d'un filtre utilisant une ligne à onde lente. Le CID est placé sur un GCP sans plan de masse sous le substrat. Les dimensions physiques du CID et du GCP sont : N=12, w=s=10μm, S_0=100μm, W_0=230 μm et l'épaisseur de la couche métallique est de 2 μm. Le modèle de circuit complet du CID consiste en deux condensateurs parallèles C_p, un condensateur série C_s (le composant dominant représentant la capacité de couplage) et les conductances G_p et G_s reliées aux pertes par radiation et par la couche métallique. Puisque le CID est symétrique, le modèle de circuit équivalent l'est

également. La plage de fréquence pour l'extraction du modèle est de 10 GHz à 20 GHz. La longueur du CID varie de 50 μm à 1 mm alors que les autres dimensions demeurent inchangées. Le modèle extrait montre que les condensateurs équivalents C_p, C_s et les conductances G_p, G_s, augmentent presque linéairement avec un accroissement de la longueur L à la condition que L demeure inférieur à 0,3 mm. Lorsque L est supérieur à 0,4 mm, les valeurs des condensateurs et des conductances fluctuent grandement avec la fréquence et le CID ne se comporte plus tel un condensateur discret. Ceci s'explique par le fait que le condensateur n'est plus suffisamment petit par rapport à la longueur d'onde.

En chargeant la ligne GCP périodiquement par une capacitance par unité de longueur C_1, on réalise une ligne à onde lente. Les paramètres de transmission de la ligne à onde lente sont:

$$C_0' = C_0 + C_1 \tag{0.4}$$

$$Z_0' = \sqrt{\frac{L_0}{C_0'}} \tag{0.5}$$

$$v' = \frac{1}{\sqrt{L_0 C_0'}} \tag{0.6}$$

Théoriquement, la valeur de la capacitance par unité de longueur C_1 devrait être calculée depuis un CID infiniment long. Cependant, pour faciliter la modélisation, on peut calculer approximativement la valeur de C_1 depuis un CID de longueur finie. Les paramètres du substrat, de la ligne GCP et du CID sont respectivement: ε_r=9,8, h=250μm, w=s=10μm, S_0=100μm et W_0=30 μm. L'épaisseur de la couche métallique

est de 2 μm. À 17 GHz, les paramètres de propagation de la ligne GCP chargée sont : Z_0= 109 ohms, permittivité effective ε_{reff}=5,24 et facteur de perte α=42,3 dB/m. En chargeant la ligne classique par des CID aux deux extrémités, les paramètre de la ligne à onde lente sont : Z_0= 26,8 ohms, permittivité effective ε_{reff}=87,2 et facteur de perte α=167,1 dB/m. La longueur d'onde de la ligne à onde lente est plus courte que celle de la ligne GCP non chargée par un facteur de quatre. Ceci s'explique par le fait que la capacité de charge C_1 est beaucoup plus grande que C_0. Il est donc possible de réaliser un circuit plus compact en utilisant la ligne à onde lente.

Un filtre passe-bande (FPB) a été conçu en utilisant le modèle du circuit de la ligne à onde lente et le CID décrit plus haut. Le FPB est réalisé par la cascade série de résonateurs à onde lente d'une demi-longueur d'onde et de CID de couplage. Les paramètres du filtre sont :

- N=2 de type Chebyshev.
- Fréquence centrale, f0 = 17.5 GHz.
- La bande passante se situe de 16.5 GHz à 18.5 GHz.
- Ondulation de 0.5 dB.

La longueur totale du FPB est de 2,4 mm. Les résultats de simulation du FPB fondés sur le modèle de la ligne à onde lente et le CID sont très près des résultats de mesure et des simulations électromagnétiques. Cet exemple de conception d'un FPB démontre que l'extraction du modèle complet est très efficace pour la conception de circuit sous forme de schéma.

0.6 Combineur planaire quasi-optique

Une nouvelle structure de combinaison de puissance est proposée. La structure de distribution/combinaison de puissance est réalisée par la transition en une ligne microruban surdimensionnée et des lignes microruban multi parallèles. Un diviseur de puissance de 1 à 4 ports opérant à 25-31 GHz est conçu. Le substrat utilisé est le Duroid 5870 et a pour paramètres ε_r = 2.33 et h = 0,254 mm. Les quatre lignes microruban parallèles sont espacées également. La relation entre le nombre de lignes microruban multi parallèles 2N, l'impédance caractéristique de la ligne mince Z_2 et l'impédance caractéristique de la ligne surdimensionnée Z_1 est définie par :

Puisque la structure agit selon un mode électromagnétique quasi transverse et que la distribution de courant sur le métal est foncièrement plane selon la direction transverse, la puissance d'entrée est presque également divisée aux quatre sorties. Le mode TE10 de la ligne microruban surdimensionnée doit être évité puisqu'il réduit l'efficacité de combinaison de puissance. La transition de largeur de la ligne d'entrée à la ligne surdimensionnée réalise l'adaptation d'impédance et réduit les modes supérieurs pouvant se propager. Les lignes microruban multi parallèles fonctionnent principalement selon un mode paire et le couplage entre chacune d'elle est très faible. Les résultats de simulation démontrent que les magnitudes et les phases des signaux distribués aux ports 2-5 et aux ports 3-4 n'ont que très peu de différence. L'application du calibrage TR à ports multi parallèles permet d'obtenir les paramètres de la transition de la ligne microruban surdimensionnée aux lignes microruban multi parallèles. Le modèle de circuit équivalent de la transition peut être approximativement considéré tel quatre sauts

microruban connectées à une ligne microruban surdimensionnée. Deux diviseurs de puissance 1-4 connectés dos à dos ont été fabriqués et mesurés. Les résultats de mesure sont en accord avec les résultats obtenus par simulation. La magnitude du paramètre S_{21} mesurée se situe entre -0.8 dB et -1.6 dB.

Quatre amplificateurs MMIC HMC283 fabriqués sur Arsénure de Galium (GaAs) par *Hittite Microwave Corporation* sont utilisés pour construire le combineur de puissance. Le gain de cet amplificateur est de 21 dB et le point P_{1dB} se situe typiquement à 18 dBm. Les résultats de mesure sont près des résultats simulés. La mesure montre un P_{1dB} de 23 dBm signifiant une efficacité de combinaison de puissance de l'ordre de 79,5%. L'ensemble de la structure de combinaison est planaire et le combineur de puissance quasi-optique possède un concept de circuit clair.

0.7 CONCLUSION

Des techniques de calibrage numérique ont été proposées pour résoudre le problème des discontinuités de port engendré par les sources d'excitation courant/tension discrètes dans l'algorithme MoM déterminé. L'utilisation des ces techniques permet d'extraire précisément le modèle de circuit équivalent complet de structures planaires. De plus, ces techniques sont compatibles avec les logiciels de simulation électromagnétique commerciaux.

Il a été démontré que les modèles complets sont critiques pour la conception de circuits intégrés sur la base de stratégies de conception bien établies pour l'analyse et l'optimisation des circuits. L'utilisation de modèles de circuits de discontinuités planaires permet une conception plus précise que celle réalisée à partir des modèles

statiques et s'avère plus efficace qu'une conception par simulation électromagnétique. Les techniques de calibrage proposées sont puissantes et efficaces pour faire le pont entre la simulation de champs et la conception de circuits.

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2D	Two-dimensional
3D	Three-dimensional
ABCD parameter	Transmission Parameter or Chain Parameter
BPF	Band Pass Filter
CAD	Computer Aided Design
CPS	Coplanar Stripline
CPW	Coplanar Waveguide
DUT	Device Under Test
EM	Electromagnetic
FGCPW	Finite-Ground Coplanar Waveguide
IC	Integrated Circuit
IDC	Interdigital Capacitor
MMIC	Monolithic Microwave Integrated Circuit
MOM	Method of Moments
SOC	Short-open Calibration
SOLT	short-open-load-through
S parameter	Scattering Parameter
TE	Transverse Electric
TEM	Transverse Electromagnetic

TR	Thru-Resistor
TRL	Thru-Reflect-Line
T parameter	Chain Scattering Parameter or Scattering Tranfer Parameter
Y parameter	Admittance Parameter
Z parameter	Impedance Parameter

INTRODUCTION

The state-of-the-art design of planar microwave and millimeter-wave circuits and components is generally made in two different ways. One way is based on lumped-element network topologies, which are developed with static or quasi-static equivalent circuit models of electrically small-sized structures or discontinuities and connecting transmission lines such as planar microstrip or coplanar waveguide elements. This design procedure is quite similar or even identical to the schemes commonly used for low-frequency electronic circuits. A large variety of equivalent circuit models for planar discontinuities has been established and widely used in commercial software packages including Agilent Advanced Design System (ADS), Agilent EEsof EDA, Ansoft Designer and others. However, these models and their network parameters are generally formulated by static/quasi-static closed-form equations with approximations or assumptions, which do not account for high frequency effects such as frequency dispersion, high-order modes, parasitic coupling, space radiation and substrate leakage. In addition, a commercial software package may be able to handle only a limited number of all possible planar discontinuities in its design library, and the designer has to develop his/her own models for the other portion of planar discontinuities. Nevertheless, the equivalent network approach is still the most powerful and preferred technique for the designer.

The other way which is more accurate and reliable is completely based on full-wave electromagnetic modeling and simulation. The terminology "full-wave" means that the

field model is directly developed from the Maxwell's equations although certain assumptions or approximations may also be considered in the model construction such as lossless structures and vanishing conductor thickness. A handful of commercial method-of-moments (MoM) simulators including Agilent Momentum, Ansoft Ensemble, Sonnet EM Suite, Zeland IE3D and other field-based software packages present popular design tools, allowing one to implement accurate full-wave simulation and optimization of planar integrated circuits and antennas. Generally, the full-wave packages are related to simulation and modeling aspects rather than design and optimization processes even though a sophisticated field-based scheme may be possible at the expense of requiring a huge computational resource. This is in particular true when an electrically large planar structure is designed and optimized. Therefore, the global field-based optimization of such a complete structure is impractical and sometimes impossible with the commonly used computing facility. So the most efficient way is to segment the overall complex geometrical layout into a number of electrically small and geometrically simple discontinuities together with uniform transmission line sections and then carry out a direct synthesis and optimization procedure based on its equivalent circuit network topology, which is constructed by characterization and establishment of an equivalent circuit model of each individual part. In this way, element-to-element and adjacent couplings can be involved through multi-level segmentation procedure. However, the fundamental problem in this procedure is whether it is able to obtain very accurate equivalent circuit models with full-wave electromagnetic modeling and simulation techniques for such electrically small structures.

The deterministic MOM algorithms [1]–[13] have been recognized as probably the most powerful candidates for accurate and efficient modeling of planar or quasi-planar structures. However, lumped current/voltage sources such as delta-voltage are generally used to excite the structure, allowing the deterministic and efficient calculations of field parameters. Since the artificial sources can never describe the exact field profile at the ports of excitation because of multilayered geometry and non-uniform field profile, the resulting "artificial" field discontinuities or differences between the lumped sources and the "true" fields can bring errors or parasites to the calculated network parameters or equivalent circuit models. To solve this problem of port discontinuities, several techniques such as double-delay calibration, external exciting and de-embedding, were presented [13]-[17]. But no further attempts were published for systematic understanding of this critical problem until the proposal of short-open calibration (SOC) technique [18]-[30].

The SOC technique, which was inspired from the real-world measurement techniques, makes use of the even/odd excitations with one section of uniform line to formulate the open/short standards and then calculate the error boxes of the structure. Such SOC calibration techniques have successfully been used in equivalent circuit modeling and applications of various microwave planar structures including microstrip, coplanar stripline (CPS), and finite-ground coplanar waveguide (FGCPW) circuits. The original 2-port SOC calibration technique has also been extended to the multi-port SOC [30]. The use of SOC techniques requires intermediate field calculations within the MoM software, which has to be implemented by the software developer. Considering

that nearly all commercial MoM simulators can only provide the calculated network parameters at a specified external location along the feeding line, the SOC technique was found difficult in theory for its compatibility and integration with them. Therefore, it is not practical for us to consider the SOC technique in the commercial electromagnetic simulation and analysis. To remove this hurdle, we propose thru-reflect-line (TRL) and thru-resistor (TR) numerical calibration techniques that can be combined with such commercial EM software packages as Agilent Momentum and Zeland IE3D to model the port discontinuities and extract the circuit model of planar discontinuities[31]-[33] in a similar way as the SOC scheme.

It is well known that the TRL calibration technique [34]-[37] has widely been used in microwave measurements and it was also deployed in [17] to numerically extract the S-parameters of planar circuits from full-wave MoM simulations. The TRL standards are easily realized in both practical measurements and numerical simulations. Distinct technical merits of the TRL and TR calibration techniques can be summarized by two aspects, namely, easily realizable calibration standards and complete compatibility with commercial EM software. With the TRL and TR calibration techniques and commercial packages, one can easily formulate full-wave based equivalent circuit model of planar circuits. In this work, these calibration techniques will be described and discussed with respect to their applications as microstrip circuits, slow wave line filter and planar quasi-optical power combiner.

Slow wave lines are widely implemented in microwave circuits because the size of the circuit using slow-wave line can be greatly reduced. However, the accurate full-wave

models of slow-wave line are difficult to be extracted. The full-wave equivalent circuit model of interdigital capacitors (IDC) in Coplanar waveguides (CPW) configuration will be extracted by using numeric TRL calibration technique combined with commercial EM software and will be implemented in the slow-wave line filter design. In addition, a new planar quasi-optical power combiner will be proposed in this work. The power distributing/combining structures are simply realized by transition between the oversized microstrip line and the parallel multi microstrip lines. With the numerical calibration technique we proposed, we can extract the equivalent circuit model of the power distributing/combining structures. Such structure is a planar structure and has merits of both the circuit based power combiner and the traditional quasi-optics power combiner. It can be fabricated using planar circuit technology. No complicated mechanical assembling is needed, and the volume can be greatly reduced. The interconnections with other planar circuits are very easy.

To avoid any possible confusion of terminology in connection with the use of discontinuity, we should point out that the modeling of a planar discontinuity is concerned with the investigation of a "useful" circuit element and its equivalent circuit model will be developed by numerical calibration and parameter extraction while the port discontinuity is related to parasites due to the "artificial" source or excitation mechanism required in the numerical methods.

CHAPTER 1

NUMERICAL TRL CALIBRATION TECHNIQUE

1.1 Introduction

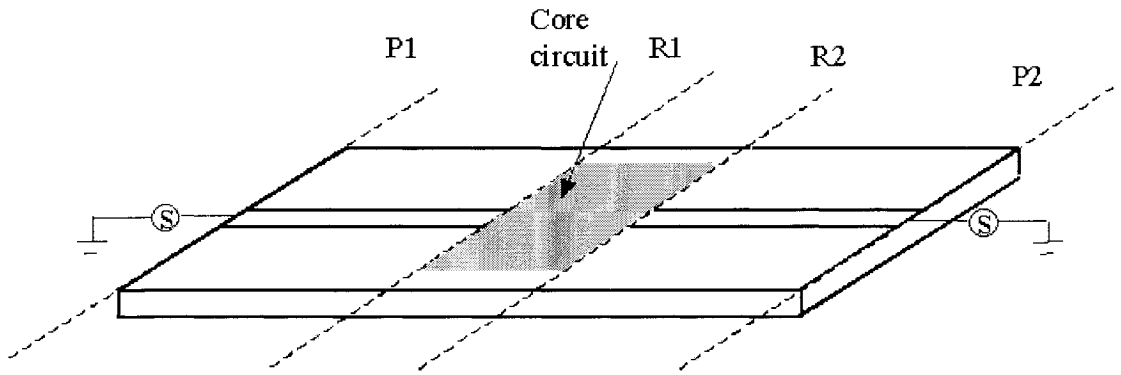
A variety of error models and calibration procedures has been proposed and developed for practical measurements. Two of the most popular schemes are the full 2-port short-open-load-through SOLT calibration and TRL calibration. All the proposed calibration procedures rely on simple and idealized standards. The difference between the calibration procedures is in number, specific nature, complexity of the used standards, and type of measurement to be performed. In a real measurement, for example, both SOLT and TRL calibrations can be used if the device-under-test (DUT) has a coaxial structure. If the DUT has a microstrip structure, however, the TRL calibration is better than the SOLT calibration because the SOLT calibration cannot remove discontinuity effects of the transition from coaxial connector to microstrip. Also, the standards in the TRL calibration are much easier to realize than those in the SOLT calibration.

Theoretically, all the calibration procedures proposed in real measurement can also be used in numerical EM simulations. The ideal open and short standards are not easy to realize in an EM simulation of planar structures when we make use of those commercial EM simulation packages based on MOM algorithm. For example, the open always has a

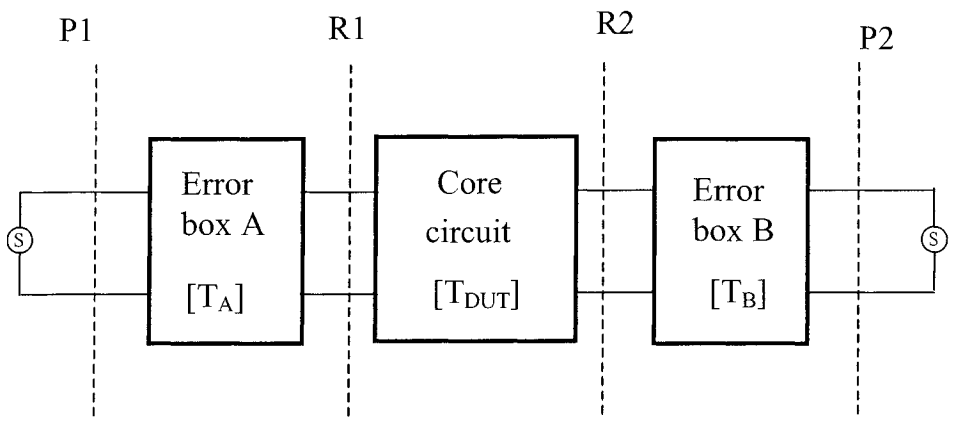
capacitance effect, and the short that is realized by the via connecting to ground always has an inductance effect. However, the TRL calibration standards are much easier to realize. The reflect standards do not need to be perfect. The line and through standards can easily be implemented. Therefore, we believe that the TRL calibration is much more proper for use in the numerical calibration combined with the commercial EM simulation packages based on MOM algorithm.

1.2 Numerical TRL calibration

Fig.1.1(a) illustrates a two-port microstrip discontinuity under modeling. The shadow region between reference planes R1 and R2 represents the discontinuity from which we want to extract the circuit model. The discontinuity is named as device under test (DUT). The port discontinuities exist between microstrip feed lines and exciting sources. The equivalent network is shown in Fig.1.1 (b). The error boxes involve the transmission feed line and port discontinuity.



(a)



(b)

Fig.1.1. Two-port microstrip discontinuity under modeling (a) and its equivalent network (b).

A calibration procedure is used to characterize the error boxes; then the actual error-corrected parameters of the DUT can be calculated. The simplest way to do calibration is to use three or more known standards, such as short, open, and match loads. The problem with this approach is that such standards are always imperfect to some degree, and consequently introduce errors into the calibrated parameters of the DUT. The TRL

calibration scheme does not rely on exactly known standards. The TRL calibration technique makes use of three standards: thru, reflect, and line, which are shown in Fig.1.2.

In Fig.1.2, the thru connection is made by directly connecting port at reference plane R1 and port at reference plane R2; the reflect connection uses a load having a high reflection coefficient, Γ_L, as this will be determined in the TRL calibration procedure while the line connection is made by connecting port at reference plane R1 to port at reference plane R2 through a section of uniform transmission line. It is not necessary to know the exact length of the line, and it is not required that the line be lossless as such parameters will be determined in the TRL procedure.

The TRL calibration standards are simple and easily realizable in both practical measurement and numerical MOM simulation. The only critical parameter is the characteristic impedance Z_0 of connecting or reference lines. The calibration procedure is straightforward and results in explicit analytical expressions for the error terms. The TRL calibration technique does have some limitations. Higher-order modes can affect the calibration accuracy and they must be eliminated. For best accuracy, the line standard should be less than 1/2 wavelength long at the highest frequency. However, the difference in length between the line standard and the through standard should be discernible (greater than $\approx 20°$) at the lowest frequency. These restrictions limit the frequency span for a given set of standards to a ratio of 8:1. Thus, for a larger desired frequency range, multiple standards and calibrations must be applied.

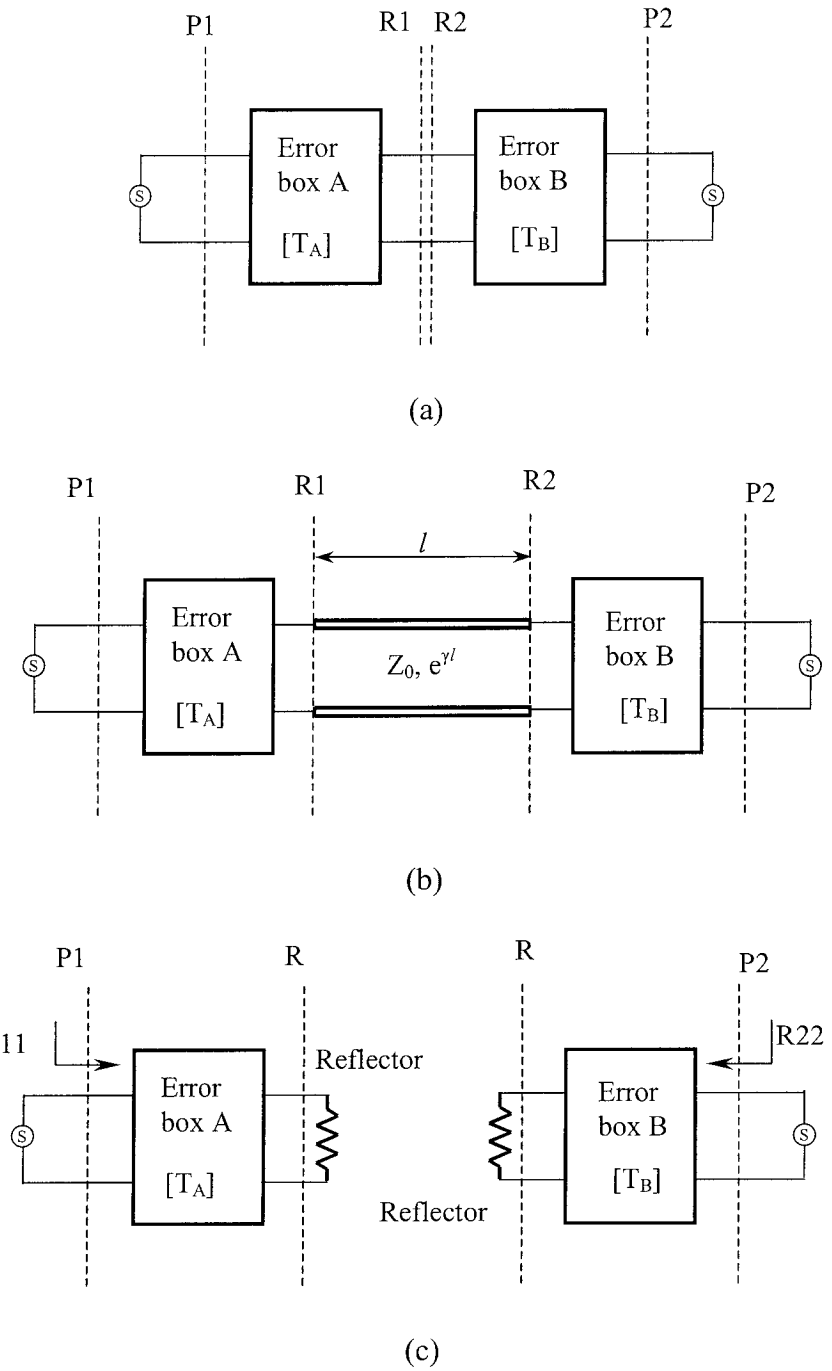


Fig.1.2. Block diagram of the numerical TRL calibration procedure. (a) Thru connection; (b) Line connection; (c) Reflect connection.

1.2.1 TRL calibration algorithm

We apply the through, reflect, and line connections over the reference planes at DUT, R1 and R2, and simulate the S-parameters for these three cases at the reference planes of an exciting source, P1 and P2. Thereafter, we can transfer these S-parameters into T parameters. The following derivation of the TRL algorithm similar to the derivation in [34][35] can be set up. Each connection of standard or DUT which has generalized transfer matrix N_x will lead to the following matrix M_x:

$$M_x = AN_xB^{-1}, \tag{1.1}$$

in which A and B^{-1} are the cascading matrices of error boxes A and B; N_x are the cascading matrices of the standards or the cascading matrices of the DUT and M_x are the cascading matrices obtained at reference planes P_1 and P_2.

From the thru connection, we have

$$M_1 = AN_1B^{-1}, \tag{1.2}$$

$$N_1 = \begin{bmatrix} I & 0 \\ 0 & I \end{bmatrix}. \tag{1.3}$$

From the line connection, we can get the following expressions

$$M_2 = AN_2B^{-1}, \tag{1.4}$$

$$N_2 = \begin{bmatrix} e^{-\gamma l} & 0 \\ 0 & e^{+\gamma l} \end{bmatrix}. \tag{1.5}$$

Because the length of the line standard is an unknown, so is N_2 in equation (1.4). Two similar matrices P and Q are defined as follows

$$Q = M_2 M_1^{-1} \text{ and } P = N_2 N_1^{-1}, \tag{1.6}$$

$$P = A^{-1} Q A . \tag{1.7}$$

From equation (1.7) we can see that such similar matrices have equal eigenvalues:

$$eig(P) = eig(Q) = \lambda_{1,2}, \quad \Lambda = \begin{bmatrix} \lambda_1 & 0 \\ 0 & \lambda_2 \end{bmatrix}, \tag{1.8}$$

where eig( ) is the eigenvalue operator. Λ denotes the matrix of eigenvalues which is related to P and Q via the following transformation

$$\Lambda = X^{-1} P X = Y^{-1} P Y , \tag{1.9}$$

where the columns of the transformation matrices X and Y are composed of the eigenvectors of P and Q, respectively. Since P is equal to N_2, N_2 and Λ have identical eigenvalues, the unknown propagation constants of the line standard can be derived by

$$N_2 = \begin{bmatrix} e^{-\gamma l} & 0 \\ 0 & e^{+\gamma l} \end{bmatrix} = \Lambda = \begin{bmatrix} \lambda_1 & 0 \\ 0 & \lambda_2 \end{bmatrix}. \tag{1.10}$$

As P and Q are known (Q is the measured data at reference planes P_1 and P_2), the eigenvectors can be evaluated except for an arbitrary factor, we can write

$$X = X_0 \beta , \qquad \beta = diag(\beta_1, \beta_2), \tag{1.11}$$

$$Y = Y_0 \delta , \qquad \delta = diag(\delta_1, \delta_2) , \tag{1.12}$$

where β_i and δ_i are arbitrary constants, X_0 and Y_0 can be computed from equation (1.9). As P is diagonal, one possible solution for X_0 is a unit matrix. From equation (1.9) we have

$$P = X Y^{-1} Q Y X^{-1} . \tag{1.13}$$

From equation (1.13) we can partly determine A as

$$A = YX^{-1} = Y_0 \delta \beta^{-1} = A_0 K , \tag{1.14}$$

where $A_0 = Y_0$, and $K = diag(\frac{\delta_1}{\beta_1}, \frac{\delta_2}{\beta_2}) = \begin{bmatrix} k_1 & 0 \\ 0 & k_2 \end{bmatrix}$, k1 and k2 are arbitrary constants.

B can be derived by

$$B = M_1^{-1} A N_1 = M_1^{-1} A = M_1^{-1} A_0 K = B_0 K , \tag{1.15}$$

where $B_0 = M_1^{-1} A_0$.

So far, there are two unknowns to be determined in A and B: k_1 and k_2. The reflect standard is used to determine these two unknowns. The reflection coefficient of the reflect standard is not known exactly, but it can be chosen to be an imperfect short or an imperfect open which has a reflect coefficient $|\Gamma| \approx 1$. So we have the reflect coefficient at the reference planes P_1 and P_2

$$\Gamma_{Xa} = (A_{11}\Gamma + A_{12})(A_{21}\Gamma + A_{22})^{-1}, \tag{1.16}$$

$$\Gamma_{Xb} = (B_{22}\Gamma + B_{21})(B_{12}\Gamma + B_{11})^{-1}. \tag{1.17}$$

From equation (1.16)(1.17), we can get

$$\Gamma = k_2^{-1} X_2 k_1 = k_1^{-1} X_1 k_2 , \tag{1.18}$$

$$X_1 = (A_{0,11} - \Gamma_{Xa} A_{0,21})^{-1} (\Gamma_{Xa} A_{0,22} - A_{0,12}) , \tag{1.19}$$

$$X_2 = (B_{0,22} - \Gamma_{Xb} B_{0,12})^{-1} (\Gamma_{Xb} B_{0,11} - B_{0,21}) . \tag{1.20}$$

Solving equation (1.18) yields

$$k_2 k_1^{-1} = \pm \sqrt{\frac{X_2}{X_1}} . \tag{1.21}$$

The sign in equation (1.21) can be determined by evaluating the sign of Γ in equation (1.18). So we have

$$k_2 = \alpha k_1, \qquad \alpha = \pm\sqrt{\frac{X_2}{X_1}}, \tag{1.22}$$

$$K = \begin{bmatrix} k_1 & 0 \\ 0 & k_2 \end{bmatrix} = k_1 \begin{bmatrix} 1 & 0 \\ 0 & \alpha \end{bmatrix}. \tag{1.23}$$

We can now complete the calibration because we can derive the T parameters of any DUT by

$$N_x = A^{-1} M_x B = K^{-1} A_0^{-1} M_x B_0 K = \begin{bmatrix} 1 & 0 \\ 0 & \alpha \end{bmatrix}^{-1} A_0^{-1} M_x B_0 \begin{bmatrix} 1 & 0 \\ 0 & \alpha \end{bmatrix}. \tag{1.24}$$

Furthermore, the value of k_1 can be determined by using the reciprocity property. We assume that the error box has a reciprocity property. Such property exists in most of passive structures in the full-wave electromagnetic simulations.

From the reciprocity property of error box A, we have

$$A_{11}A_{22} - A_{12}A_{21} = 1. \tag{1.25}$$

From equations (1.14), (1.23) and (1.25), we can calculate the value of k_1 by

$$k_1^{\,2} = \frac{1}{\alpha(A_{0,11}A_{0,22} - A_{0,12}A_{0,21})}. \tag{1.26}$$

By using three standards: thru, line and reflect connections, we can calculate the parameters of the error boxes, and the correct core parameter of the DUT can be obtained by removing the error boxes through equation (1.24). The TRL calibration

technique can be implemented in both practical measurement and full-wave MOM simulation.

1.2.2 Examples

In full-wave MOM simulations, it has been known that port discontinuities brought by the imposed lumped current/voltage exciting source will cause errors in the calculated parameters of the circuit of interest (as in the measurement, we name it as DUT). By using our numerical TRL calibration technique, the port discontinuities can be considered in the error boxes, and their effects can be removed in order to extract the correct parameters of the DUT. Therefore, we can use the numerical TRL calibration to extract parameters of planar discontinuities such as microstrip open, step, gap and so forth. In the following, an example will be studied to validate the proposed numerical TRL calibration technique.

A simple microstrip open-end circuit is studied in this work. Fig.1.3 depicts the physical layout arranged for the TRL-based de-embedding of equivalent open-end capacitance (Coc). The radiation-related conductance (Goc) is negligible at low frequency. The substrate of this open circuit is Alumina $\varepsilon_r = 9.9$, $W = h = 0.635mm$, $L = 10.4mm$. We use IE3D to carry out the EM simulation. A local port model is selected instead of other port models for the deterministic or direct MoM algorithm as detailed in [19]. Therefore, network parameters at the port can directly be derived from the calculated port quantities such as port voltages/currents or amplitudes of

incident/reflected waves, without resorting to any additional simulation of current density distributions along the feeding line in the indirect MoM algorithm as in [19].

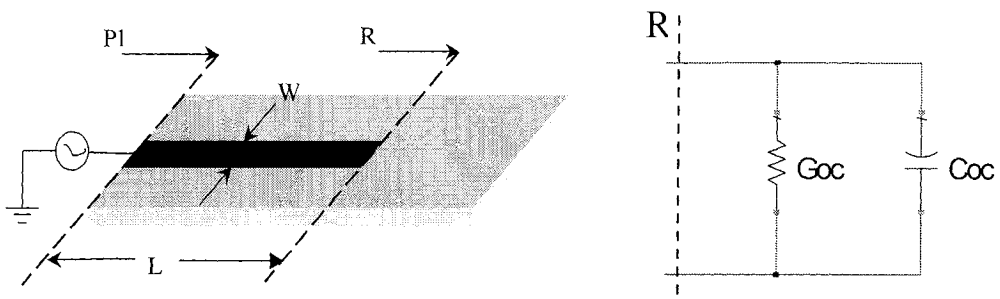
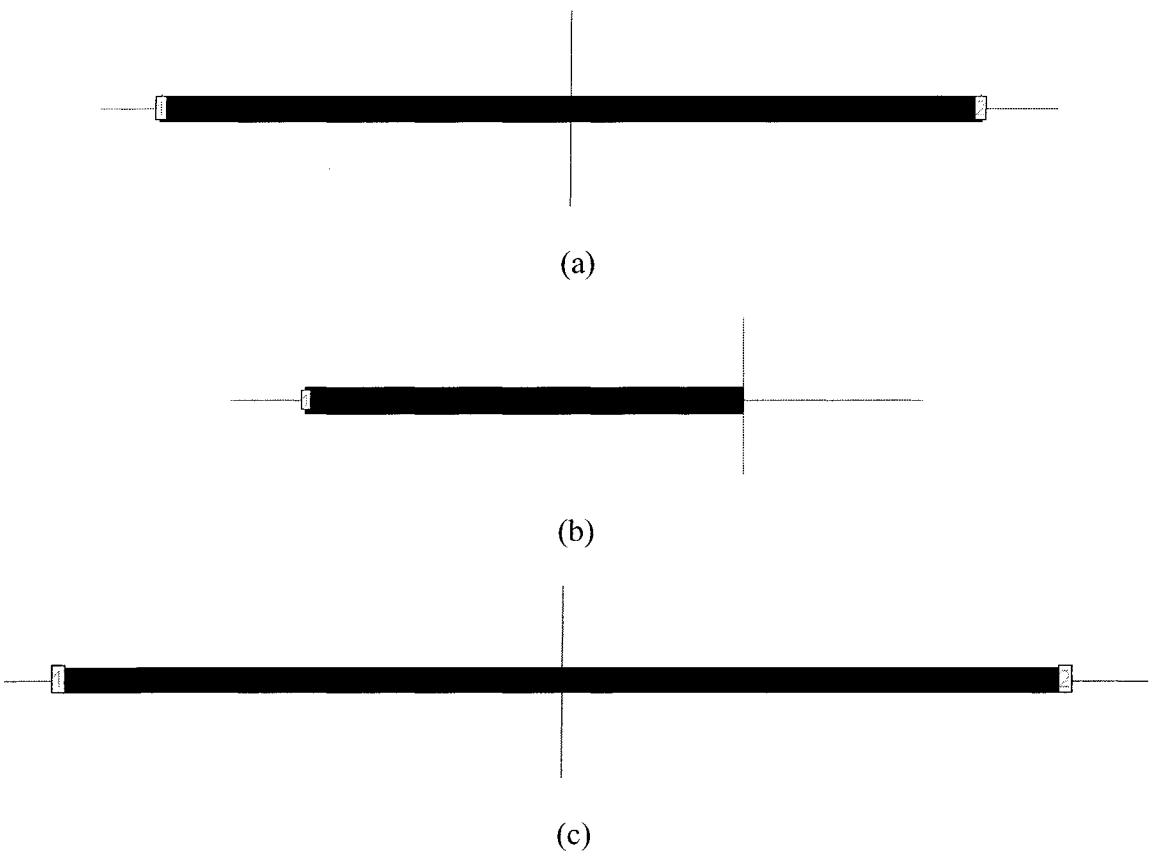


Fig.1.3. Geometry and generalized equivalent circuit model of a microstrip open-end circuit.

First, the complex reflection coefficient at the port can numerically be calculated and then converted to its corresponding input admittance with the help of characteristic impedance. Next, the three microstrip thru, line and reflect connections are realized in the EM simulation and the S parameters are generated. The length of the line standard is chosen to be 5.6mm. From the static calculation, the electrical length of the line standard is about 35° at 2GHz and 87° at 5GHz, which can satisfy the necessary condition from 20° to 160° in the frequency range from 2 to 5 GHz. We choose the open-end (the same open-end we want to study) as the reflect standard. All the S parameters corresponding to the thru and the line standard are transferred to the T parameters. Then we use the TRL calibration algorithm as described above to do the calibration and the network parameters of the error terms with regard to the feed line section (port-to-end section in Fig.1.1(a)) can be obtained. The layouts of the connection of the three standards in IE3D

are shown in Fig.1.4. As a result, the load admittance at the open-end can be derived in an analytical way by removing out the error box. Actually, because we use the reflect standard that is the same as the open-end during the TRL calibration procedure, we can calculate the reflection coefficient Γ of the open-end from equation (1.18). Then we can obtain the input admittance of the open-end by

$$Y_{in} = Y_0 \frac{1-\Gamma}{1+\Gamma}. \tag{1.27}$$



(a)

(b)

(c)

Fig.1.4. The layout of the three connections (IE3D). (a) Thru connection; (b) Reflect connection; (c) Line connection.

And the capacitance of the equivalent circuit model as shown in Fig.1.3 can be calculated by

$$C_{oc} = \frac{IM(Y_{in})}{2\pi f_0},\ G_{oc} = RE(Y_{in}). \tag{1.28}$$

For the purpose of comparison, such a capacitance is also extracted from the calculated port admittance using a simple transmission line theorem [19], as shown in Fig.1.5.

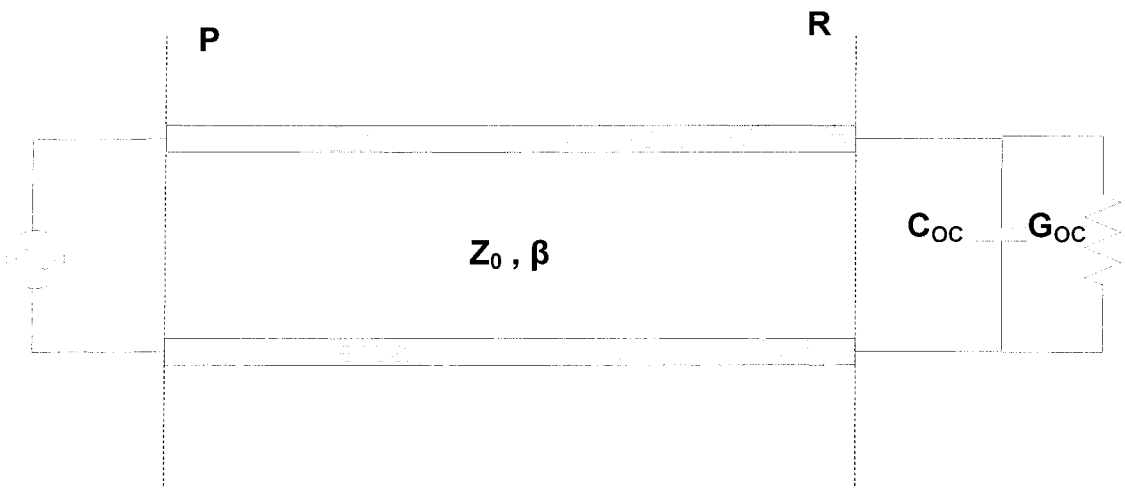


Fig.1.5. The de-embedding procedure based on a simple transmission line theory.

Fig.1.6 shows the obtained normalized capacitance (Coc) using the above two de-embedding techniques against those obtained from closed-form equations as given in [38][39]. It can be seen that the TRL results appear almost unchanged with frequency and they are in a very good agreement with those from formula [38][39] while the conventional non-TRL results irregularly go up and then fall down as frequency

increases. In this case, the unwanted parasitic effects in connection with the port discontinuity are a primordial factor as discussed in [19][20].

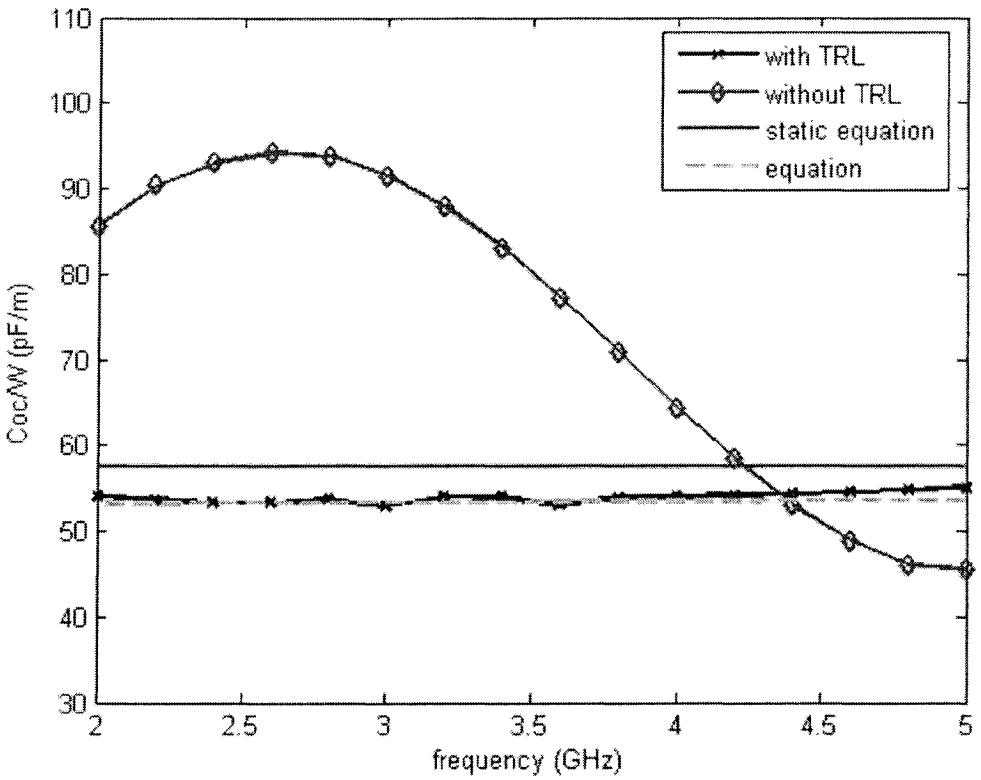
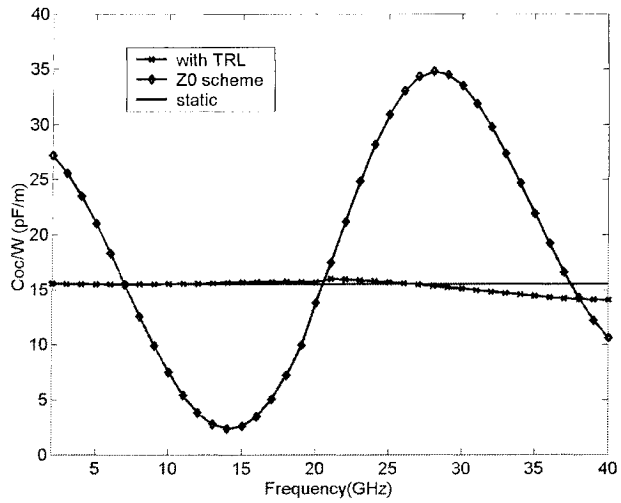


Fig.1.6. TRL-extracted open-end fringing capacitance together with those obtained from the non-TRL parameter extraction scheme and two closed-form design equations [38][39] (w = h = 0.635mm, ε_r = 9.9, L = 10.4 mm).

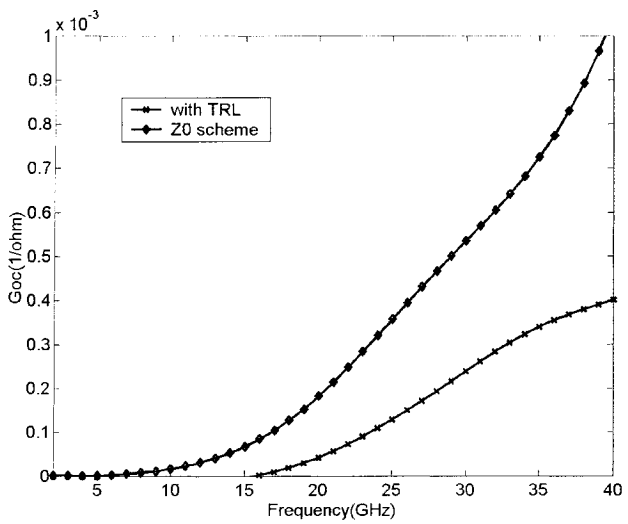
Another microstrip open-end circuit on substrate Duroid 5880 (ε_r = 2.2, h = 0.254mm, W=0.762mm) is calculated. The frequency range is selected from 2GHz to 40GHz. Because the frequency range is too large for a single TRL calibration procedure, two TRL calibration procedures are required. In this case, one is considered from 2GHz to

10GHz, and the other is from 10GHz to 40GHz. Fig.1.7 shows the obtained normalized capacitance (Coc) and the conductance using the above two de-embedding techniques against those obtained from closed-form static equations as given in [39]. It can be seen that at low frequency the TRL results appear almost unchanged and are in a very good agreement with those from static formula [39] while the conventional non-TRL results contains large uncertain errors. We also see that the radiation becomes large and not negligible at high frequency.

From this example, we can observe that the port discontinuity due to the exciting scheme effectively brings error to simulation results. Through the TRL calibration, we can set up the error boxes that include both the port discontinuity and the feed line effects. Then the correct circuit model of the planar circuit can be generated.



(a)



(b)

Fig.1.7. Extracted parameters of the circuit model of microstrip open-end obtained from TRL calibration compared with those calculated from other two methods: Z_0-scheme (without calibration), and static equation [39] ($\varepsilon_r = 2.2$, h = 0.254mm, W=0.762mm) .

1.3 Determination of the characteristic impedance of a transmission line by using a resistor standard in TRL calibration

In the previous sections, an effective numerical TRL calibration was proposed, developed and integrated with a deterministic MoM-based commercial simulator for the characteristic parameter extraction of a planar discontinuity. As such, an accurate equivalent circuit model of the planar discontinuity can be generated from this process. The proposed numerical TRL calibration can easily be implemented in existing MoM commercial packages such as Agilent Momentum, Ansoft Ensemble, Sonnet EM Suite, Jansen LINMIC+/N, Zeland IE3D and so on.

However, the calibration reference impedance, which is equal to the characteristic impedance of the line standards, should be known a priori in the TRL technique. In general, the characteristic impedance and propagation constant of the line standards are calculated from a two-dimensional (2D) modeling method, which assumes the lines to be infinitely long. Because of the inconsistency between the 2D and three-dimensional (3D) impedance definitions of transmission line, the characteristic impedance of the line standards obtained from the 2D method will yield some difficult-to-estimate error effects [23]. In the TRL calibration, the 3D definition of characteristic impedance should be used.

The short-open calibration (SOC) was proposed and it has successfully been used to determine the 3D characteristic impedance of a transmission line [23]. Nevertheless, the SOC technique is not directly compatible with the existing commercial EM software, as

it requires some intermediate results of field calculation within the software framework. In order to determine the 3D characteristic impedance of the line standards for improving accuracy in the parameter extraction of planar circuits, we introduced an alternative standard called "resistor standard" in the numerical TRL calibration [33]. The impedance of the resistor standard Z_t can be chosen to be equal to the reference impedance of the TRL calibration procedure or not. The reflection coefficient of the resistor standard is known. The reference impedance is chosen to be around the characteristic impedance of the line standard that is calculated from a 2D method. Such a resistor standard is very easy to implement in commercial full-wave EM software.

The resistor standard is similar to that used in TR calibration in next Chapter but not the same application concept. Here the resistor standard is used as a supplement of the TRL method to determine the characteristic impedance of the transmission line. In the followings, we will discuss this additional standard and its related analytical derivations.

1.3.1 THEORY

In the TRL calibration, three calibration standards are used to extract the embedded error terms. Compared to other techniques such as the short-open-load-through (SOLT) calibration, the TRL standards are more easily realizable. The only critical parameter is the characteristic impedance of line standards. For the TRL calibration, the characteristic impedance of the line standard should be known exactly in the very beginning; the TRL itself cannot determine it. To determine this important parameter, we propose a resistor

standard as shown in Fig.1.8. The configuration of the connection of this resistor standard is the same as that of the reflect standard. The impedance of the resistor standard Z_t is chosen to be match standards with $\Gamma = 0$ or other terminators with known reflection coefficient.

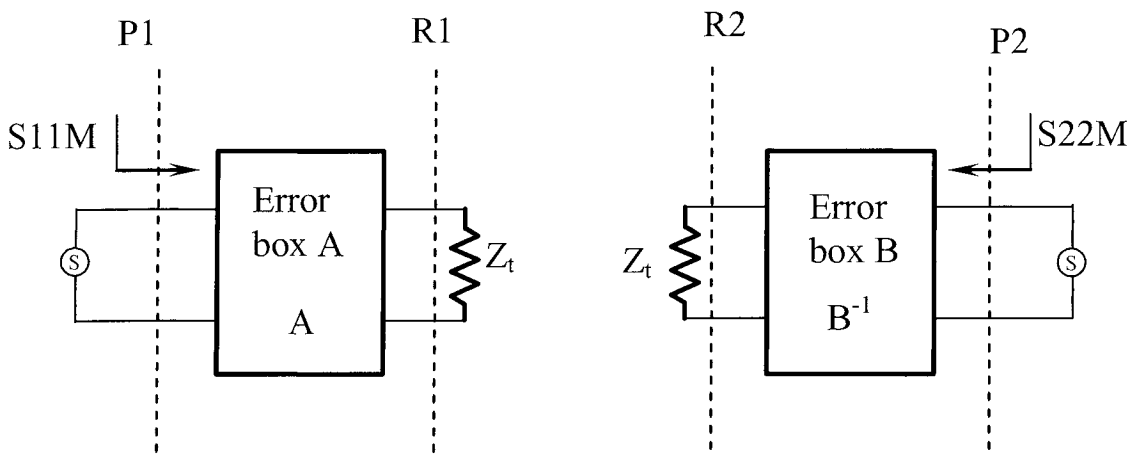


Fig.1.8. Resistor standard connection of the proposed improved numerical TRL calibration procedure.

We can easily make a resistor standard in commercial full-wave EM software. For example, in Momentum of ADS and Zeland IE3D, we can realize the resistor connection by using a thin film resistor.

The TRL calibration algorithm is derived in section 1.2. The derivation is based on such a condition that the characteristic impedance of the line standard is known and equal to the reference impedance in the calibration procedure, then equation (1.5) can be used as described in section 1.2.1. So error parameters in the error box can be

determined by measurements of the three TRL standards connections and the true or core parameters of the DUT can be extracted correctly.

If the characteristic impedance of the line standard is not known exactly, however, equation (1.5) cannot be used, and the TRL calibration procedure cannot be completed. Or if there is an error in the characteristic impedance of the line standard, it will cause an error in the extracted parameters of the DUT. Therefore, we need another standard to generate the characteristic impedance of the line standard. Equations (1.1) to (1.4) in section 1.2.1 can also be used again here. Like in section 1.2.1, we define two matrices P and Q as follows

$$Q = M_2 M_1^{-1} \text{ and } P = N_2 N_1^{-1} \text{ with } P = A^{-1} Q A . \tag{1.29}$$

Because P and Q are similar, we can define an eigenvalue matrix Λ, which gives

$$P = N_2 N_1^{-1} = N_2 = X \Lambda X^{-1}, \tag{1.30}$$

$$Q = Y \Lambda Y^{-1}, \tag{1.31}$$

$$P = X Y^{-1} Q Y X^{-1}, \tag{1.32}$$

$$A = Y X^{-1}. \tag{1.33}$$

We can write the characteristic impedance of the line standard as Z, which is an unknown. Equation (1.5) in section 1.2.1 becomes

$$N_2 = \begin{bmatrix} ch(\gamma l) - \dfrac{Z^2 + Z_0^2}{2ZZ_0} sh(\gamma l) & \dfrac{Z^2 - Z_0^2}{2ZZ_0} sh(\gamma l) \\ -\dfrac{Z^2 - Z_0^2}{2ZZ_0} sh(\gamma l) & ch(\gamma l) + \dfrac{Z^2 + Z_0^2}{2ZZ_0} sh(\gamma l) \end{bmatrix}. \tag{1.34}$$

On the basis of a matrix calculation, we can get the eigenvalue of N_2 as follows

$$\Lambda = \begin{bmatrix} e^{-\gamma l} & 0 \\ 0 & e^{+\gamma l} \end{bmatrix}. \tag{1.35}$$

So N_2 can be expressed by

$$\Lambda = X^{-1} N_2 X = X^{-1} P X . \tag{1.36}$$

where the columns of X are composed of eigenvectors of N_2. The eigenvectors can be written as

$$X = X_0 \beta , \tag{1.37}$$

$$\beta = diag(\beta_1, \beta_2) . \tag{1.38}$$

where β are arbitrary constants.

One possible X_0 is

$$X_0 = \begin{bmatrix} 1 & a \\ a & 1 \end{bmatrix}, \; a = \frac{Z - Z_0}{Z + Z_0} . \tag{1.39}$$

In the same way, we can write Y in equation (1.31) as

$$Y = Y_0 \delta , \; \delta = diag(\delta_1, \delta_2) . \tag{1.40}$$

Because Q is the measured data at reference planes P_1 and P_2, so we can calculate Y_0 except for an arbitrary constant δ. From equations (1.33), (1.37) and (1.40), we can obtain

$$\begin{aligned} A = YX^{-1} &= Y_0 \delta \beta^{-1} \begin{bmatrix} 1 & a \\ a & 1 \end{bmatrix}^{-1} = Y_0 \delta \beta^{-1} \frac{1}{1 - a^2} \begin{bmatrix} 1 & -a \\ -a & 1 \end{bmatrix} \\ &= A_0 K \begin{bmatrix} 1 & -a \\ -a & 1 \end{bmatrix} = A_0 K \begin{bmatrix} 1 & b \\ b & 1 \end{bmatrix} \end{aligned} . \tag{1.41}$$

where $A_0 = Y_0$, $b = -a$ and $K = diag(\frac{\delta_1}{\beta_1(1-a^2)}, \frac{\delta_2}{\beta_2(1-a^2)}) = \begin{bmatrix} k_1 & 0 \\ 0 & k_2 \end{bmatrix}$, k1 and k2 are arbitrary constants.

Equation (1.41) can be written as

$$A = A_0 K \begin{bmatrix} 1 & b \\ b & 1 \end{bmatrix} = \begin{bmatrix} A_{0,11}k_1 + A_{0,12}k_2 b & A_{0,11}k_1 b + A_{0,12}k_2 \\ A_{0,21}k_1 + A_{0,22}k_2 b & A_{0,21}k_1 b + A_{0,22}k_2 \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix}. \quad (1.42)$$

From equation (1.2), we have

$$B = M_1^{-1} A N_1 = M_1^{-1} A = M_1^{-1} A_0 K \begin{bmatrix} 1 & b \\ b & 1 \end{bmatrix} = B_0 K \begin{bmatrix} 1 & b \\ b & 1 \end{bmatrix} = \begin{bmatrix} B_{0,11}k_1 + B_{0,12}k_2 b & B_{0,11}k_1 b + B_{0,12}k_2 \\ B_{0,21}k_1 + B_{0,22}k_2 b & B_{0,21}k_1 b + B_{0,22}k_2 \end{bmatrix} = \begin{bmatrix} B_{11} & B_{12} \\ B_{21} & B_{22} \end{bmatrix}, \quad (1.43)$$

where $B_0 = M_1^{-1} A_0$.

So far, there are three unknowns to be determined in A and B: b ($b = -a$), k_1 and k_2. The method stated in [35] cannot be applied here because of three unknowns instead of two unknowns. That is why we have to introduce another resistor standard to complete the calibration procedure. As in [35], using a known value resistor connection yields

$$\Gamma_{Xa} = (A_{11}\Gamma + A_{12})(A_{21}\Gamma + A_{22})^{-1}, \quad (1.44)$$

$$\Gamma_{Xb} = (B_{22}\Gamma + B_{21})(B_{12}\Gamma + B_{11})^{-1}. \quad (1.45)$$

At first, we use two match standards with $\Gamma = 0$. From equation (1.44), we have

$$A_{12} = \Gamma_{Xa} A_{22}. \quad (1.46)$$

Combining equations (1.42) and (1.46) leads to

$$A_{0,11}k_1b + A_{0,12}k_2 = \Gamma_{Xa}A_{0,21}k_1b + \Gamma_{Xa}A_{0,22}k_2, \tag{1.47}$$

$$k_1b = (A_{0,11} - \Gamma_{Xa}A_{0,21})^{-1}(\Gamma_{Xa}A_{0,22} - A_{0,12})k_2. \tag{1.48}$$

We can write equation (1.48) as

$$k_1b = X_1k_2. \tag{1.49}$$

where $X_1 = (A_{0,11} - \Gamma_{Xa}A_{0,21})^{-1}(\Gamma_{Xa}A_{0,22} - A_{0,12})$.

In the same way, we can obtain from equations (1.43)(1.45)

$$B_{21} = \Gamma_{Xb}B_{11}, \tag{1.50}$$

$$B_{0,21}k_1 + B_{0,22}k_2b = \Gamma_{Xb}B_{0,11}k_1 + \Gamma_{Xb}B_{0,12}k_2b. \tag{1.51}$$

Equation (1.51) can be written as

$$k_2b = X_2k_1, \tag{1.52}$$

where $X_2 = (B_{0,22} - \Gamma_{Xb}B_{0,12})^{-1}(\Gamma_{Xb}B_{0,11} - B_{0,21})$.

Solving equation (1.49)(1.52) generates the following condition

$$b^2 = X_1X_2,\ b = \pm\sqrt{X_1X_2}. \tag{1.53}$$

So the characteristic impedance of the line standard is

$$Z = Z_0\frac{1 \mp \sqrt{X_1X_2}}{1 \pm \sqrt{X_1X_2}}. \tag{1.54}$$

The sign in b could be decided in two ways. The first way can be described as the following. If we know approximately the value of Z, so we can decide the sign of *b* by comparing the value calculated from equation (1.54) with the approximate value. So the best way is to select the reference impedance Z0 to be far from the pre-evaluated

characteristic impedance of the line standard. In case that the reference impedance Z0 is selected to be near the real Z, then b is very small, however, we cannot distinguish which sign that corresponds to the right value. Another way to estimate the sign of b is to use the reflect (with high reflecting coefficient) standard. We suppose the reflect standard is an open (not necessarily an ideal open) standard.

From equation(1.44), we have

$$\Gamma = (\Gamma_{Xa} A_{21} - A_{11})^{-1}(A_{12} - \Gamma_{Xa} A_{22}). \tag{1.55}$$

From $k_2 b = X_2 k_1$ and $k_1 b = X_1 k_2$ in equations (1.49) and(1.52), equation (1.42) can be written as

$$\begin{aligned} A &= \begin{bmatrix} A_{0,11}k_1 + A_{0,12}k_2 b & A_{0,11}k_1 b + A_{0,12}k_2 \\ A_{0,21}k_1 + A_{0,22}k_2 b & A_{0,21}k_1 b + A_{0,22}k_2 \end{bmatrix} \\ &= \begin{bmatrix} (A_{0,11} + A_{0,12}X_2)k_1 & (A_{0,11} + A_{0,12}/X_1)k_1 b \\ (A_{0,21} + A_{0,22}X_2)k_1 & (A_{0,21} + A_{0,22}/X_1)k_1 b \end{bmatrix}. \\ &= \begin{bmatrix} A_{11}'k_1 & A_{12}'k_1 b \\ A_{21}'k_1 & A_{22}'k_1 b \end{bmatrix} \end{aligned} \tag{1.56}$$

When error box A is connected with an open, we can obtain the following with reference to equations (1.55) and (1.56)

$$\Gamma = \frac{1}{k_1}(\Gamma_{Xa} A_{21}' - A_{11}')^{-1}(A_{12}' - \Gamma_{Xa} A_{22}')bk_1 = \tilde{\Gamma} b, \tag{1.57}$$

where $\tilde{\Gamma} = (\Gamma_{Xa} A_{21}' - A_{11}')^{-1}(A_{12}' - \Gamma_{Xa} A_{22}')$.

Because we know the reflection coefficient of the open standard that is almost equal to 1, from equation (1.57), we can decide the sign of b (+ or -). From equation (1.49), we have $k_2 = k_1 b / X_1$. So there is only one unknown k_1 now. It is enough to

complete de-embedding of the error box without knowing the value of k_1. If the error box has the reciprocity property, we can get the value of k_1. The reciprocity property exists when we carry out the EM simulations with a deterministic MoM commercial simulator. According to the reciprocity property we have

$$A_{11}A_{22} - A_{12}A_{21} = 1. \tag{1.58}$$

From equations (1.56)(1.58), we can obtain

$$A_{11}'k_1A_{22}'k_1b - A_{12}'k_1bA_{21}'k_1 = 1. \tag{1.59}$$

Equation (1.59) can be written as

$$k_1^2 = G \qquad \text{and} \qquad k_1 = \pm\sqrt{G}, \tag{1.60}$$

where $G = \dfrac{1}{(A_{11}'A_{22}' - A_{12}'A_{21}')b}$.

So k_1 is determined except for the sign. As stated earlier, if we directly make use of the TRL calibration with the network analyzer in a real measurement, there is no reciprocity property in the error boxes. But if we use a full two-port calibration first then use a TRL calibration, the error box has the reciprocity property.

In fact, we can use other terminators with known reflection coefficient to get the characteristic impedance of the line standard. If a reflector or a resistor standard is used with a known value Γ, from equation (1.44) we have

$$\begin{aligned}&(A_{0,11}\Gamma - \Gamma_{Xa}A_{0,21}\Gamma)k_1 + (A_{0,11} - \Gamma_{Xa}A_{0,21})k_1b + \\ &(A_{0,12} - \Gamma_{Xa}A_{0,22})k_2 + (A_{0,12}\Gamma - \Gamma_{Xa}A_{0,22}\Gamma)k_2b = 0\end{aligned}. \tag{1.61}$$

From the previous analysis in the case of a match connection, we know that there should be a linear relation between k_1 and k_2, as $k_2 = lk_1$. So we can write equation (1.61) as

$$C_1 k_1 + C_2 b k_1 + C_3 l k_1 + C_4 l b k_1 = 0, \tag{1.62}$$

where, $C_1 = A_{0,11}\Gamma - \Gamma_{Xa} A_{0,21}\Gamma$, $C_2 = A_{0,11} - \Gamma_{Xa} A_{0,21}$, $C_3 = A_{0,12} - \Gamma_{Xa} A_{0,22}$ and $C_4 = A_{0,12}\Gamma - \Gamma_{Xa} A_{0,22}\Gamma$.

Equation (1.62) can be written as

$$k_1 (C_1 + C_2 b + C_3 l + C_4 l b) = 0. \tag{1.63}$$

Because k_1 cannot be equal to zero, so we have

$$C_1 + C_2 b + C_3 l + C_4 l b = 0. \tag{1.64}$$

In the same way, from Equation (1.45) we can get

$$D_1 + D_2 b + D_3 l + D_4 l b = 0. \tag{1.65}$$

Solving equations (1.64) and (1.65) leads to two unknowns l and b. So the calibration procedure is completed.

From the above analysis, we can see that with the known Γ of the reflect standard or the resistor standard, we can derive the needed parameters of the error box and the characteristic impedance of the line standard. Sometimes the fourth standard can facilitate the decision of the sign or the calculation. As indicated in [34], we can also obtain the propagation constant of the line standard.

In various calibration procedures, the generally used standards are open, short or resistor. We choose the match standard here, because the error in the resistor brought by

the parasitic effect could be smaller than that in a short or an open. The error in the standard can be caused by series inductance or parallel capacitance. So it will give error to the reflection coefficient. The reflect coefficient of a terminator is

$$\Gamma = \frac{Z - Z_0}{Z + Z_0} = \frac{Y_0 - Y}{Y_0 + Y}. \tag{1.66}$$

From equation(1.66), we obtain

$$\frac{\partial \Gamma}{\partial Z} = \frac{2Z_0}{(Z + Z_0)^2} = \frac{-2Y_0}{(Y_0 + Y)^2}. \tag{1.67}$$

For the short connection

$$\frac{\partial \Gamma}{\partial Z} = \frac{2}{Z_0}. \tag{1.68}$$

For the open connection

$$\frac{\partial \Gamma}{\partial Y} = -\frac{2}{Y_0}. \tag{1.69}$$

For the match connection

$$\frac{\partial \Gamma}{\partial Z} = \frac{1}{2Z_0} = \frac{-1}{2Y_0}. \tag{1.70}$$

From equations (1.68)-(1.70) we can see that the parasitic inductance or capacitance will bring less error in the case of the match connection than the other connections.

1.3.2 Examples

To show the validity and effectiveness of the proposed numerical TRL method, we now examine the characteristic impedance of a microstrip line, as shown in Fig.1.9. In our example of calculation, the permittivity of substrate is 9.9, the substrate thickness H and the line width W are all equal to 0.635 mm, and the length of the microstrip line is 4.0 mm. An electromagnetic simulator is used (Agilent's Momentum in our case).

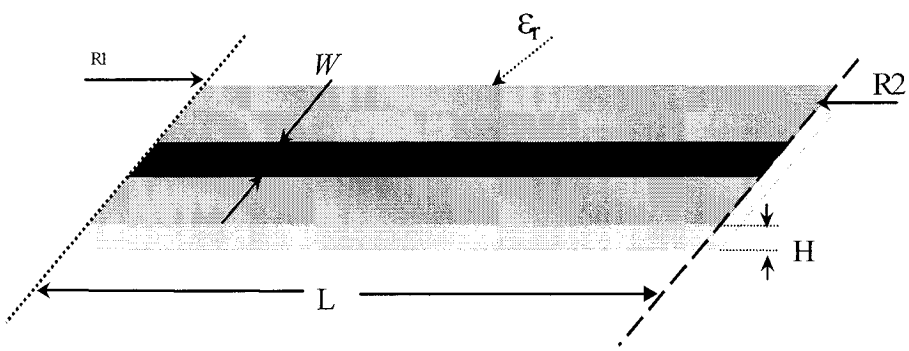


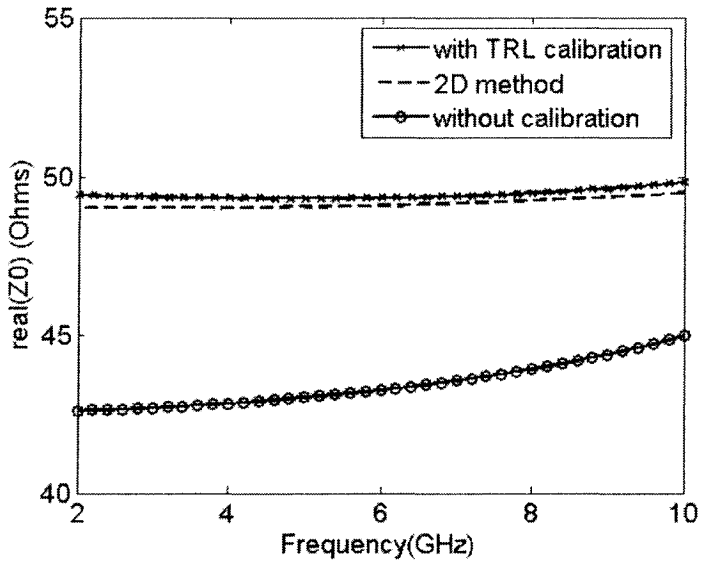
Fig.1.9. A section of microstrip line to be calculated for the characteristic impedance.

In the scheme of simulation, local ports are used instead of other extension port modes, which is important for the validity of the improved numerical TRL method. The value of the resistor standard Z_t is set to be equal to the reference impedance of 50 ohms. In the calibration procedure, an open standard is used to decide the sign of b. The calculated characteristic impedance of the microstrip line is shown in Fig.1.10. The calculated results from 2D method and the result without calibration are also shown in Fig.1.10. We can see that the real part of the characteristic impedance of the line standard agrees with that from 2D method. The imaginary part of the characteristic

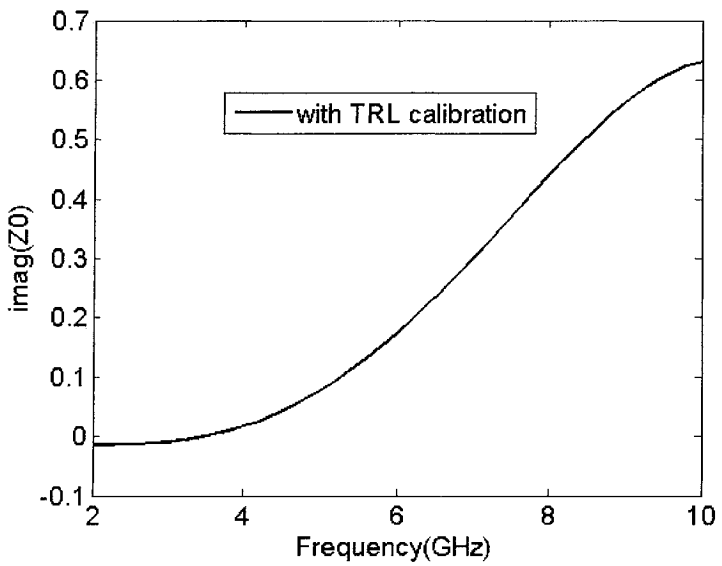
impedance is caused by the loss of the line standard and it is much smaller than the real part. We can observe that without a TRL calibration, the calculated characteristic impedance is influenced by the error terms and the results are not correct. It can be seen that the numerical calibration makes a big difference in this example.

1.4 Summary

We have extended the usually measurement-oriented TRL calibration technique to the numerical de-embedding of equivalent circuit models of planar integrated circuits and discontinuities on the basis of full-wave MoM simulations. The TRL calibration algorithm has been derived. Our comparative investigation has demonstrated that the proposed numerical TRL scheme is able to calibrate the port discontinuity involved in the deterministic MoM algorithm by formulating three calibration standards. With its easy implementation and direct compatibility in the existing MoM commercial packages, this developed TRL technique has a great potential for accurate CAD and optimization with the extracted circuit models. Additionally, to solve the ambiguity problem of characteristic impedance of the line standard in such a calibration procedure, we have introduced an additional standard called "resistor standard" into the numerical TRL calibration. From a detailed comparative investigation, we have validated the proposed scheme in the determination of the characteristic impedance of the line standard. The new additional resistor standard in the numerical TRL calibration can also be made for the practical TRL measurements.



(a)



(b)

Fig.1.10. Characteristic impedance of a microstrip line obtained from the improved numerical TRL method compared with the data obtained without calibration and the data obtained from the 2D method. (a) real part, and (b) image part. (ε_r = 9.9, w = h = 0.635mm).

CHAPTER 2

NUMERICAL TR CALIBRATION TECHNIQUE

2.1 Introduction

The numerical TRL calibration technique has been investigated and developed in Chapter 1. Our comparative investigation has demonstrated that the proposed numerical TRL scheme is able to calibrate the port discontinuity involved in a deterministic MoM algorithm by formulating three calibration standards. Those standards for the TRL calibration are simple and easily realizable in full-wave MOM simulation. But the TRL calibration technique presents some limitations. The characteristic impedance of the line standard should be known exactly. For a wide band calibration, multiple Line standards and calibrations must be applied. It is known that in the extraction of circuit model of planar discontinuities, the error boxes always possess both reciprocal and symmetrical properties. In this chapter, we suppose a simpler alternative calibration method called TR calibration technique, which is suitable for the parameter extraction of planar discontinuities in MOM algorithm. The TR calibration technique uses two standards: thru and resistor standards. The TR calibration technique looks like the improved TRL calibration technique which uses thru, line, reflect and resistor standards. But the resistor standard in the improved TRL calibration technique is a supplement that is used to determine the characteristic impedance of the line standard. Actually, every calibration technique makes use of a different combination of the standards like thru, line, resistor,

match, open, short, etc. Each calibration technique has its own characteristics as well as its own limitations, and may be more prone to different problem. The TR calibration technique is proposed in this work to extract the circuit model of planar discontinuities for a wide frequency band.

2.2 Two-port TR calibration

The proposed TR calibration assumes that the error boxes are symmetrical and reciprocal, which are often the cases for passive circuit elements. The error box model for the TR calibration is shown in Fig.2.1. The TR calibration replies on two standards, namely, thru standards and resistor standards. The Resistor standard has value of R. The connection arrangements of these two standards are shown in Fig.2.2.

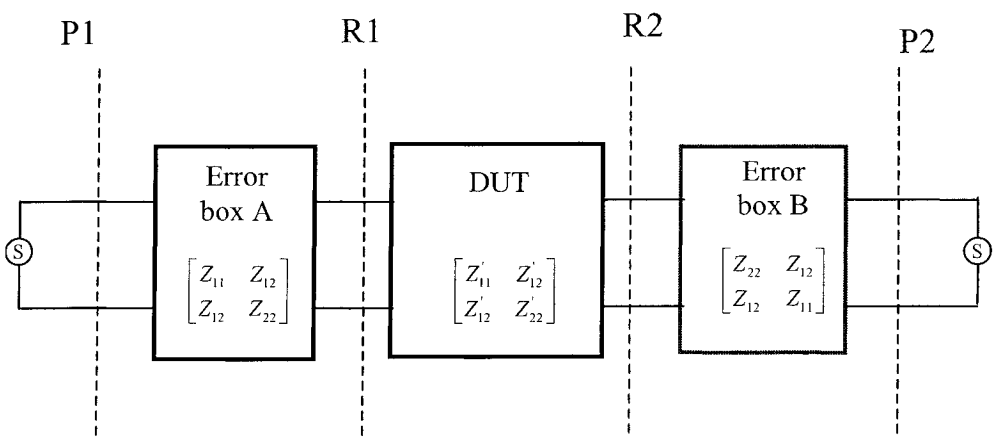
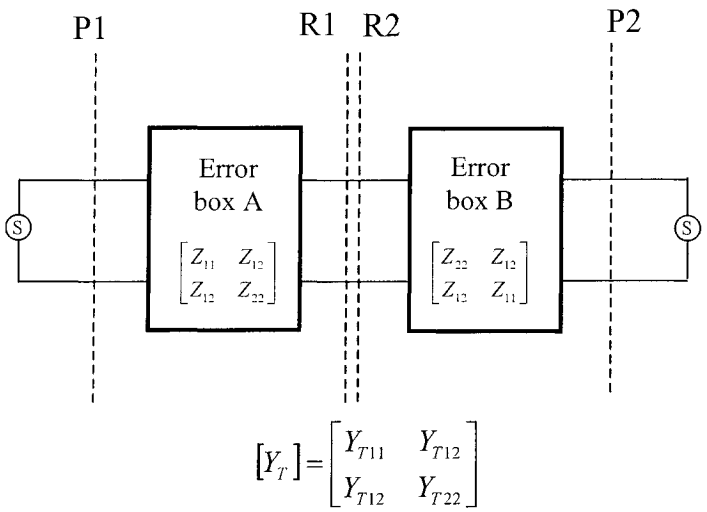
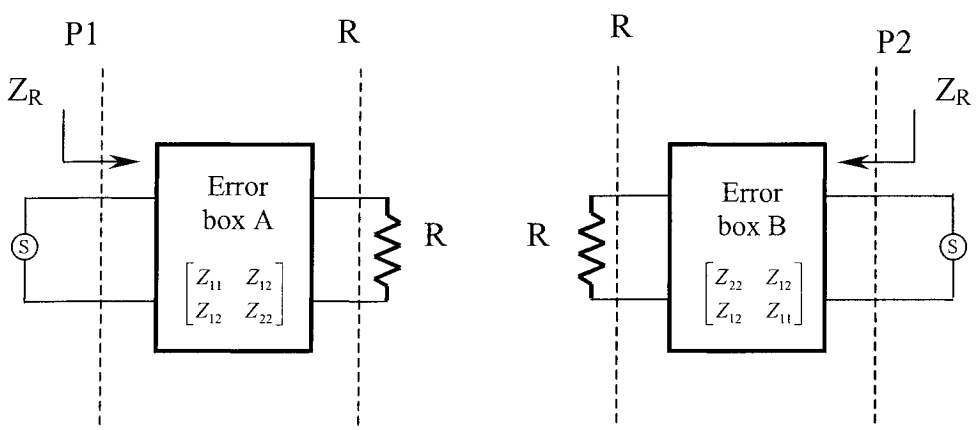


Fig.2.1. Equivalent error box model for the TR calibration.



(a)



(b)

Fig.2.2. Block diagram of the TR calibration procedure. (a) Thru connection; (b) Resistor connection.

2.2.1 Theory

The TR calibration algorithm can be derived on the basis of Y-parameters or T-parameters. The derivation based on Y-parameters is more direct while that based on T-parameters is easier to compare with the other calibration techniques discussed in this work.

A. TR calibration algorithm based on the Y parameters

From Thru connection, we can obtain 2-port parameters, namely, $[Y_T]$. From Resistor connection, we can yield input impedance Z_R. Since the error boxes are symmetrical and if we make use of odd or even voltage sources at ports P1 and P2 when Through standard is used, it behaves as if the error boxes are terminated by a short or open. The input impedance is obtained at port P1 with Z_O and Z_S corresponding to open and short connection, respectively.

$$Z_O = \frac{1}{Y_{T11} + Y_{T12}}, \tag{2.1}$$

$$Z_S = \frac{1}{Y_{T11} - Y_{T12}}. \tag{2.2}$$

From Z_R, Z_O, and Z_S, we can get the following parameters of error box,

$$Z_{11} = Z_O, \tag{2.3}$$

$$Z_{22} = R * \frac{Z_O - Z_R}{Z_R - Z_S}, \tag{2.4}$$

$$Z_{12}^2 = (Z_O - Z_S) * Z_{22}. \tag{2.5}$$

Theoretically, the value of Resistor standard R can be arbitrary. In formulating such Resistor standard in commercial MOM software, it can be expected that there is some parasitic effect. It can bring error to the TR calibration, especially at high frequencies. To eliminate such errors due to the grounding of Resistor standard, we change the connection of the Resistor standard to the connection as described in Fig.2.3. The value of Z_R is,

$$Z_R = \frac{1}{Y_{R11} - Y_{R12}}. \tag{2.6}$$

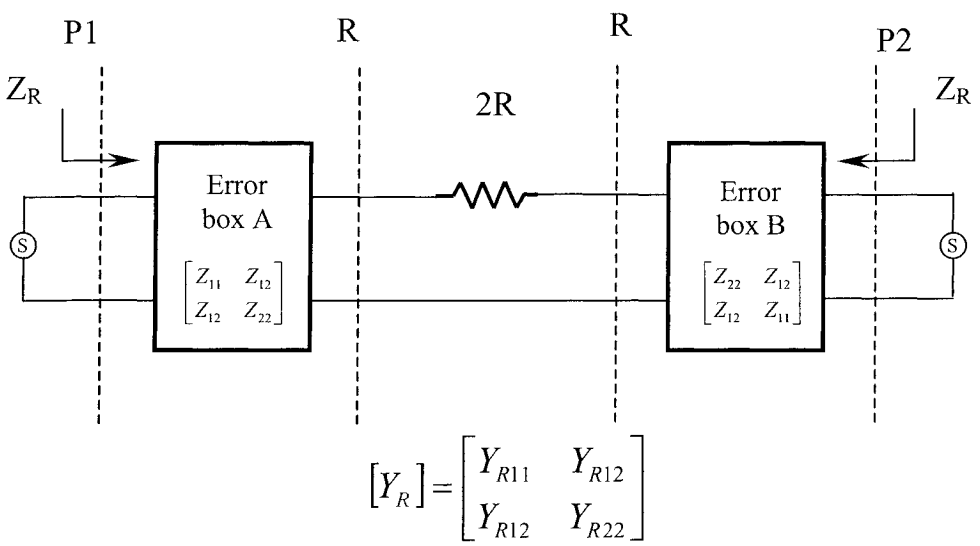


Fig.2.3. Modified connection of Resistor standard for the TR calibration.

Once the error boxes are determined, we can easily derive the ABCD matrix of device under test (DUT), $[A_{DUT}]$, with the following equation:

$$[A_{DUT}] = [A_A]^{-1}[A_{EXT}][UA_AU]^{-1}, \tag{2.7}$$

in which $U = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}$, [$A_{EXT}$] is the ABCD matrix generated by field simulations for the DUT connection including the error boxes, and [A_A] is the ABCD matrix of error box A.

B. TR calibration algorithm based on the T parameters

The reference impedance of the calibration procedure is selected to be equal to the value of the resistor standard. All T-parameters are normalized to the impedance value of the resistor standard. Similar to the procedure described in Chapter 1., the measured transfer matrix M is related to the thru standard connection by

$$M = ANB, \tag{2.8}$$

where $N = \begin{bmatrix} I & 0 \\ 0 & I \end{bmatrix}$. We can write matrix A as

$$A = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix}. \tag{2.9}$$

Because the error box B is symmetrical to the error box A, matrix T of B can be written by

$$B^{-1} = \begin{bmatrix} A_{22} & A_{21} \\ A_{12} & A_{11} \end{bmatrix}. \tag{2.10}$$

From equation (2.8), we can obtain

$$\begin{bmatrix} -E & M_{12} & 0 & M_{11} \\ M_{12} & -E & M_{11} & 0 \\ 0 & M_{22} & -E & M_{21} \\ M_{22} & 0 & M_{21} & -E \end{bmatrix} \cdot \begin{bmatrix} A_{11} \\ A_{12} \\ A_{21} \\ A_{22} \end{bmatrix} = 0. \tag{2.11}$$

Because equation (2.11) is a homogeneous equation, there is at least one unknown. So the additional standard, resistor standard, is used to calculate the error box. For the ease of analyse, we select the resistor standard as a match standard. From the match connection, we have

$$A_{12} = S_{11} A_{22} . \tag{2.12}$$

From equations (2.11) and (2.12), we can get

$$\begin{aligned} A_{12} &= aA_{22} \\ A_{11} &= bA_{22} . \\ A_{21} &= cA_{22} \end{aligned} \tag{2.13}$$

where $a = S_{11}$, $b = M_{11} + M_{12} S_{11}$ and $c = M_{21}^{-1}(1 - M_{22}(M_{11} + M_{12} S_{11}))$.

The value of A_{22} can be calculated by using the reciprocity property

$$A_{11} A_{22} - A_{12} A_{21} = 1 . \tag{2.14}$$

By using equations (2.13) and (2.14), we have

$$A_{22}^{\ 2} = \frac{1}{b - ac} . \tag{2.15}$$

The calibration procedure can now be completed, and we can obtain the correct parameters of the DUT by using the following equation.

$$N = A^{-1} M B^{-1} . \tag{2.16}$$

2.2.2 TR calibration-based parameter extraction of planar discontinuities

The same microstrip open-end as in Chapter 1 (see Fig.1.3) is studied by using the TR calibration. The value of R is set at 50 ohm. Results of the extracted open-end fringing capacitance are shown in Fig.2.4. We can see that the results of the TR calibration agree with those from the TRL calibration. The proposed TR calibration technique is thus validated.

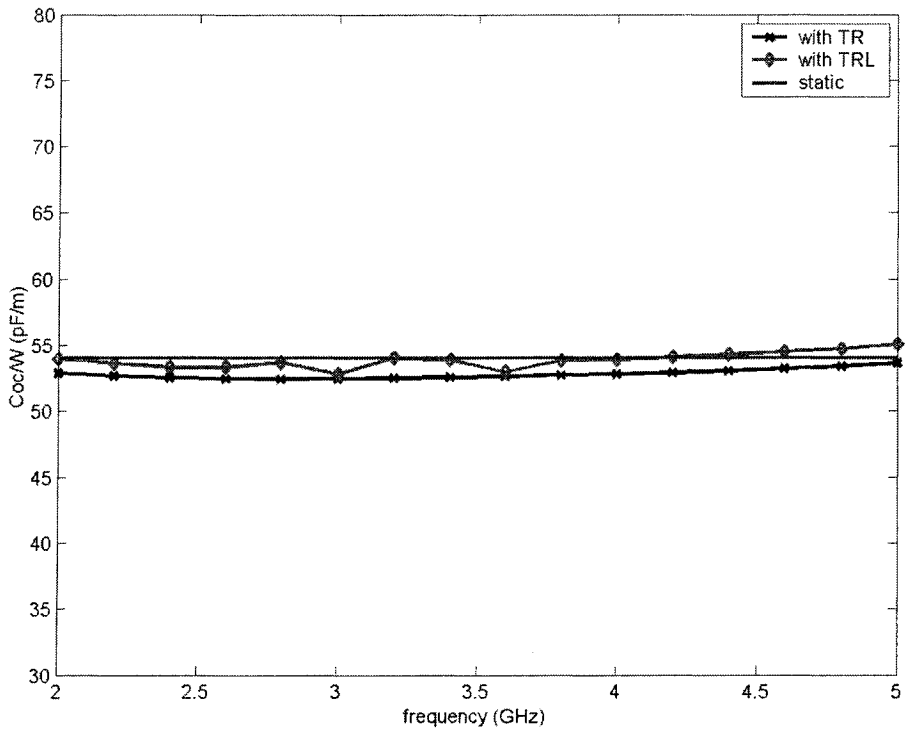


Fig.2.4. TR-extracted open-end fringing capacitance together with those obtained from the TRL parameter extraction scheme in section I and a closed-form design equation (w = h = 0.635mm, $\varepsilon_r = 9.9$).

Theoretically, resistor standard R can be of arbitrary value. In formulating this standard in a commercial MOM software, parasitic capacitance of the gap as well as that of the via from the microstrip line to the resistor that can be considered as a series inductance can bring up a little change in value of the resistor standard. The parasitic parameters of the resistor standard may bring error to the TR calibration, but it is much smaller than that in a real-world measurement. We choose the value of R to be around the characteristic impedance of the feed line. For the microstrip open-end, extracted parameters by using different R value are shown in Fig.2.5. We can see that within a wide range of the R value, the extracted capacitance changes little.

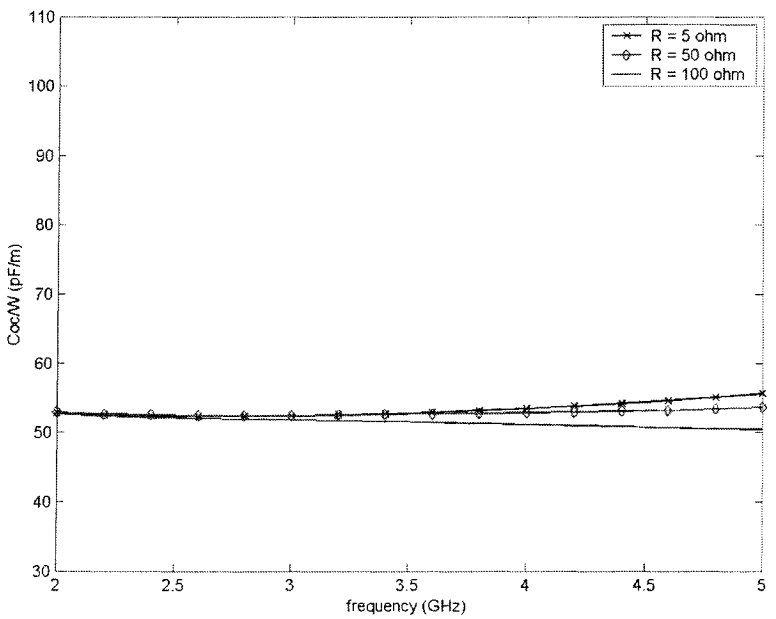
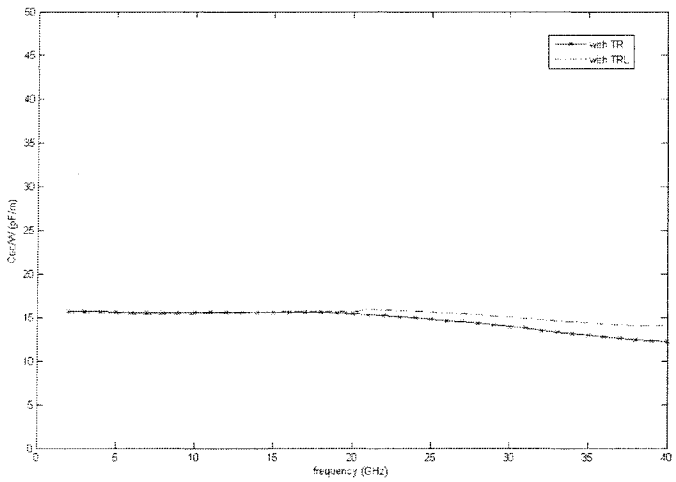
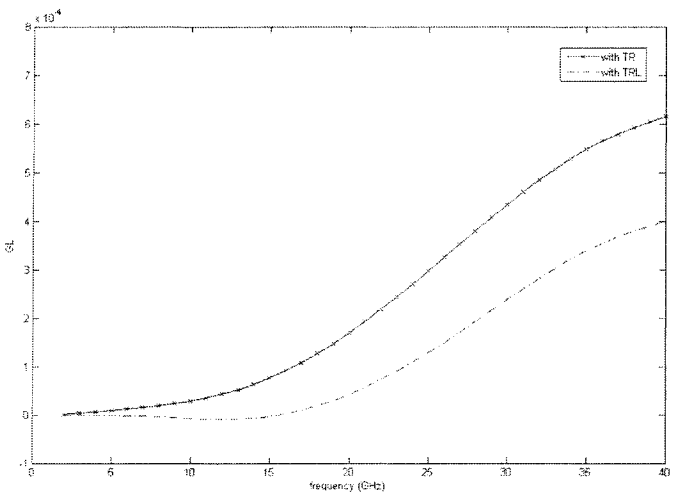


Fig.2.5. TR-extracted open-end fringing capacitance using different values of R (w = h = 0.635mm, $\varepsilon_r = 9.9$).

As shown in Fig.1.7 in Chapter 1, the open-end fringing capacitance on substrate Duroid 5880 ($\varepsilon_r = 2.2$, h = 0.254mm, W=0.762mm) has been extracted by using the TRL calibration. In the following, we use the TR calibration technique to extract the circuit model of this same open-end from 2GHz to 40GHz. The obtained results are shown in Fig.2.6(a) and (b). Results in Fig.2.6(a) agree with those in Fig.1.7. From Fig.2.6(b) we can see that as frequency increases, the radiation loss-related conductance/resistor of the open end becomes large and in fact not negligible. If we use the TRL calibration to carry out the calibration from 2GHz to 40GHz, at least two calibration procedures and two sets of calibration standards are needed.



(a)



(b)

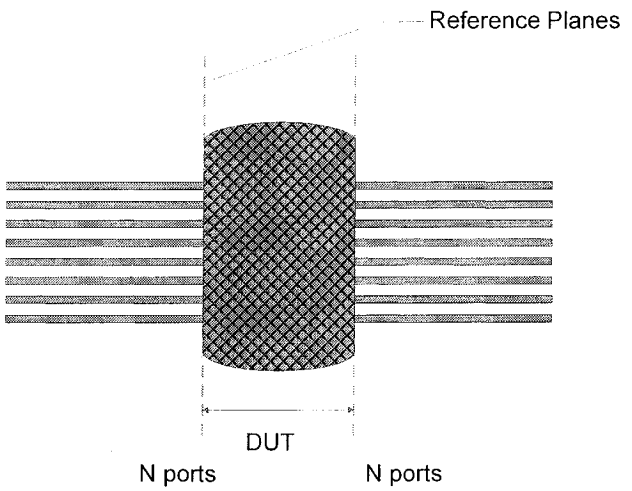
Fig.2.6. Extracted open-end fringing capacitance Coc and radiation-related conductance GL by using the TR calibration (ε_r = 2.2, h = 10mil, W=30mil).

2.3 Multi-parallel-port TR calibration

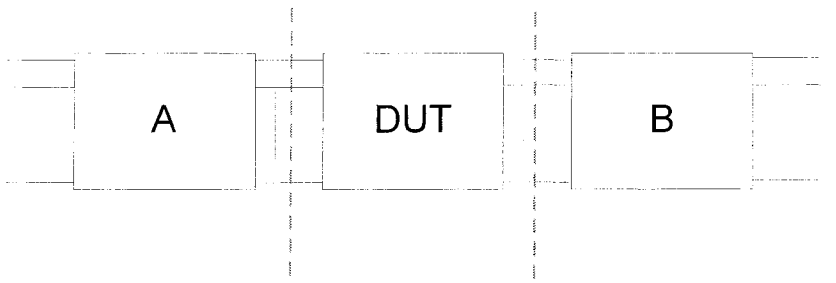
To remove the "port discontinuity" brought by the lump current/voltage excitation mechanism in a deterministic MoM algorithm, we have proposed numerical thru-resistor (TR) and thru-reflection-line (TRL) calibrations for the characteristic parameters extraction of a planar discontinuity in the previous sections. By using such numerical calibrations, correct parameters of the core planar discontinuity can be obtained, and an equivalent circuit model of the planar discontinuity can be generated. The proposed numerical calibration techniques can easily be implemented in existing MoM commercial packages such as Agilent Momentum, Zeland IE3D and so forth.

The previous numerical TR and TRL calibration techniques focus on 2 port or 1-port circuits. Multi-port calibration technique was discussed and a generalized equation was given in [40]. *Seguinotn et al.* presented a multimode TRL calibration method [35]. They considered the multi-mode circuit as a multi-port circuit but the calibration technique presented in [35] cannot be completely used in multi-port calibration. In [30] *Okhmatovski* extended the short-open calibration (SOC) to multi-port circuits. It is understood that the SOC technique needs an elaborate programming based on MOM algorithm and cannot be integrated with commercial EM simulators. In this work, we extend the numerical TR calibration technique proposed in the previous section into multi-parallel port applications.

2.3.1 Theory



(a)



(b)

Fig.2.7. Block diagrams for a multi-port circuit.

Fig.2.7(a) shows a typical multi-parallel port circuit under study. To calculate the correct parameters of the DUT, we have to remove effects of the multiple –feed lines and port discontinuities between the exciting ports and multiple feed lines. We can consider the port discontinuities and the multiple feed lines as the error boxes A and B, as shown in Fig.2.7(b). In an EM simulation of the circuit, the error boxes A and B are

usually reciprocal and symmetrical. Our derivation of the multi-port TR calibration is based on the reciprocity and symmetry properties. Such properties are not general in a real measurement. If A and B are not symmetrical, we can also use the equations below by performing two separate calibration procedures. The calibration procedure uses three standards: thru, match and multi-resistor, as shown in Fig.2.8.

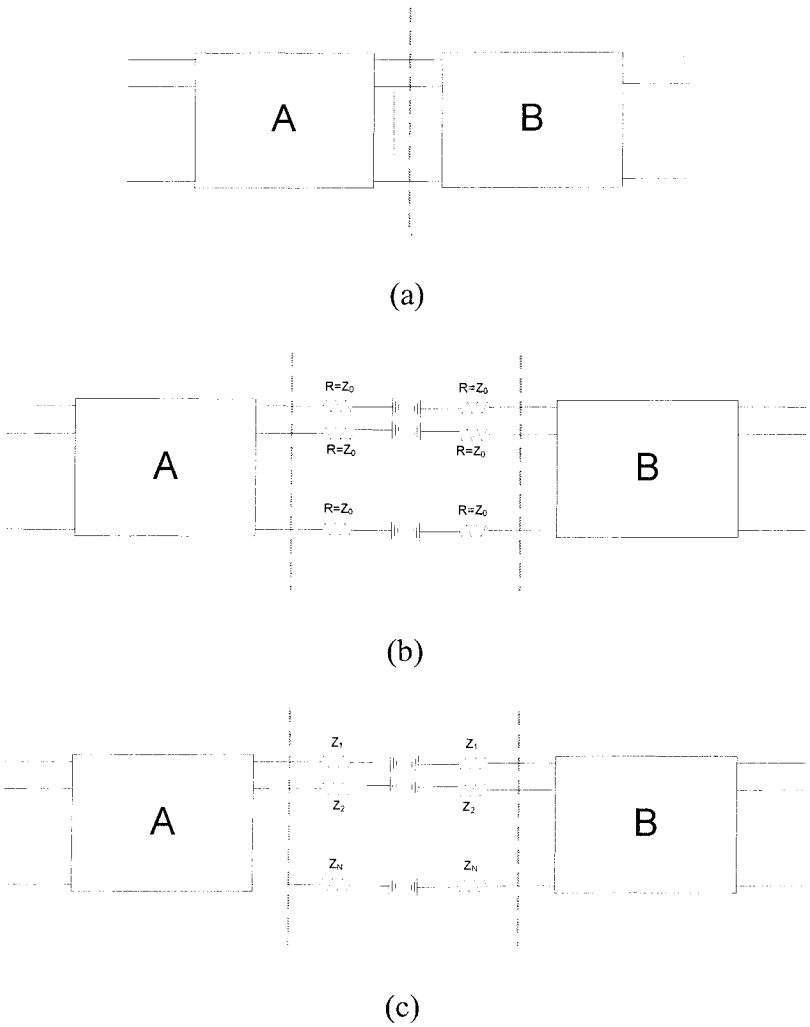


Fig.2.8. Connection scheme of standards in a multi-parallel TR calibration. (a) Thru connection; (b) Resistor connection; (c) Multi-resistor connection.

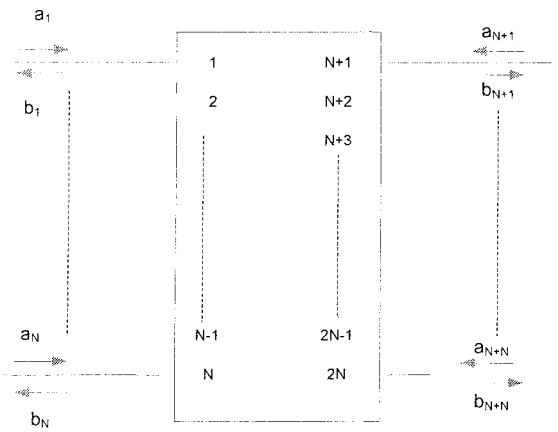


Fig.2.9. A 2N port network.

The proposed multi-port TR calibration utilizes a generalized transfer matrix or simply T matrix. For a 2N port network as shown in Fig.2.9, the relationship between incident(a_i) and reflected(b_i) waves are expressed in terms of the transfer matrix as follows

$$\begin{bmatrix} b_1 \\ b_2 \\ . \\ b_N \\ a_1 \\ a_2 \\ . \\ a_N \end{bmatrix} = [T_{2N\times 2N}] \cdot \begin{bmatrix} a_{N+1} \\ a_{N+2} \\ . \\ a_{N+N} \\ b_{N+1} \\ b_{N+2} \\ . \\ b_{N+N} \end{bmatrix}. \tag{2.17}$$

As in [35], we write the 2N port transfer matrix in the form of four sub-matrices

$$[T_{2N\times 2N}] = \begin{bmatrix} T_{11(N\times N)} & T_{12(N\times N)} \\ T_{21(N\times N)} & T_{22(N\times N)} \end{bmatrix}. \tag{2.18}$$

In general, we can calculate the S-parameters from the EM simulation. The conversion between multi-port S-parameters and T parameters follows [35]

$$\begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} = \begin{bmatrix} S_{12} - S_{11}S_{21}^{-1}S_{22} & S_{11}S_{21}^{-1} \\ -S_{21}^{-1}S_{22} & S_{21}^{-1} \end{bmatrix}, \quad \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} T_{12}T_{22}^{-1} & T_{11} - T_{12}T_{22}^{-1}T_{21} \\ T_{22}^{-1} & -T_{22}^{-1}T_{21} \end{bmatrix}. \tag{2.19}$$

The measured transfer matrix M is related to the thru standard connection by

$$M = ANB, \tag{2.20}$$

where $N = \begin{bmatrix} I & 0 \\ 0 & I \end{bmatrix}$

As in equation (2.18), we can write matrix A as

$$A = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix}. \tag{2.21}$$

Because the error box B is symmetrical to the error box A, matrix T of B can be written by

$$B^{-1} = \begin{bmatrix} A_{22} & A_{21} \\ A_{12} & A_{11} \end{bmatrix}. \tag{2.22}$$

From equation (2.20), we can formulate

$$\begin{bmatrix} -E & M_{12} & 0 & M_{11} \\ M_{12} & -E & M_{11} & 0 \\ 0 & M_{22} & -E & M_{21} \\ M_{22} & 0 & M_{21} & -E \end{bmatrix} \cdot \begin{bmatrix} A_{11} \\ A_{12} \\ A_{21} \\ A_{22} \end{bmatrix} = 0. \tag{2.23}$$

Because equation (2.23) is a homogeneous equation, there is at least one unknown. Actually, from the reciprocity and symmetry properties, we can find out that the rank of

matrix in equation (2.23) is less than or equal to 2N. So, additional standards are needed to calculate the error box. From the match connection as shown in Fig.2.8(b), we have

$$A_{12} = S_{11} A_{22} . \tag{2.24}$$

From equations (2.23) and (2.24), we can establish the following equalities

$$\begin{aligned} A_{12} &= aA_{22} \\ A_{11} &= bA_{22} \\ A_{21} &= cA_{22} \end{aligned} , \tag{2.25}$$

where $a = S_{11}$, $b = M_{11} + M_{12} S_{11}$ and $c = M_{21}^{-1}(1 - M_{22}(M_{11} + M_{12} S_{11}))$.

The value of A_{22} can be calculated by using the multi-resistor connection, as shown in Fig.2.8(c). The multi-resistor connection has the reflection coefficient $\Gamma = diag(\Gamma_i)$, $\Gamma_i = \dfrac{Z_i - Z_0}{Z_i + Z_0}$, $i = 1 \; to \; N$. We have

$$\Gamma_X = (A_{11}\Gamma + A_{12})(A_{21}\Gamma + A_{22})^{-1} . \tag{2.26}$$

From equations (2.25) and (2.26), we can set up

$$A_{22}\Gamma A_{22}^{-1} = (\Gamma_X c - b)^{-1}(a - \Gamma_X) . \tag{2.27}$$

From equation (2.27) we can see that Γ and $(\Gamma_X c - b)^{-1}(a - \Gamma_X)$ are similar matrices. So we have $A_{22} = A_{0,22}\beta$, where β are arbitrary constants: $\beta = diag(\beta_1, \beta_2 ... \beta_N)$. The error box A T matrix can be written by

$$A = \begin{bmatrix} A_{0,11} & A_{0,12} \\ A_{0,21} & A_{0,22} \end{bmatrix} \cdot \begin{bmatrix} \beta & 0 \\ 0 & \beta \end{bmatrix} . \tag{2.28}$$

Note that the N resistors cannot be totally the same. Otherwise, A_{22} can be of any value in equation (2.27). Up to now, the matrix A is known except for the constant β. According to the reciprocity property we have $S_{12} = S_{21}$ and

$$T_{22}^{-1} = T_{11} - T_{12}T_{22}^{-1}T_{21}. \tag{2.29}$$

By using equations (2.28) and (2.29), we have

$$\beta Y \beta = X, \tag{2.30}$$

where $Y = (b - ac)A_{0,22}$ and $X = A_{0,22}^{-1}$. From equation (2.30), we can calculate the value of the constant β by

$$\beta_i \beta_j Y_{i,j} = X_{i,j}. \tag{2.31}$$

From equations (2.28) and (2.31), we calculate parameters of the error boxes, and then the calibration procedure can be completed by using equation (2.16).

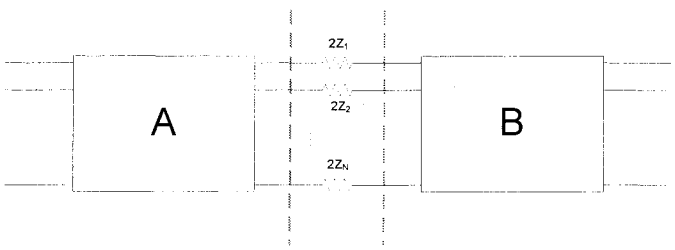


Fig.2.10. The connection of multi-parallel resistor standard.

As in Fig.2.3, we can realize the multi-resistor standard by using multi-parallel resistor standard, as shown in Fig.2.10. From the simulation of 2N ports in Fig.2.10, we can generate the S-parameters. Then, we can transfer the parameters from S to Y (2N*2N). For the 2N ports network in Fig.2.10, we have

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = Y \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}. \tag{2.32}$$

Because the network in Fig.2.10 is symmetrical, the even mode (when $V_1 = -V_2$) is the same as in Fig.2.8(c). We have

$$Y_s = Y_{11} - Y_{12}. \tag{2.33}$$

Then we can transfer Y_s to S_s, which is equal to S_{11} that we used in equation (2.24).

2.3.2 Example

Rautio [41] gave the three-dimensional (3D) characteristic impedance definition of a microstrip line. Such a 3D impedance definition was revisited in [23] by using the short-open calibration (SOC) technique. Similar to the 3D characteristic impedance definition of a microstrip line in [23], we can define 3D properties of the microstrip coupled line. When the microstrip coupled line is excited by an even or odd mode signal, the coupled line can be treated as a single transmission line [37]. ABCD parameters of the single transmission line are different for the odd mode or the even mode. So we have two sets of 3D properties for the microstrip coupled line, that is, one is for the even mode, and the other is for the odd mode.

An example of the calculation of the parameters of a microstrip-coupled line, as shown in Fig.2.11, is considered to verify the multi-port TR calibration. Results of the microstrip coupled line are shown in Fig.2.12. We can see that the results from the numerical multi-port TR calibration agree with the static results. Without the calibration

with respect to the local port, the characteristic impedance of the even/odd mode is not accurate. That is because the effects of the port discontinuities bring errors into the simulated ABCD parameters.

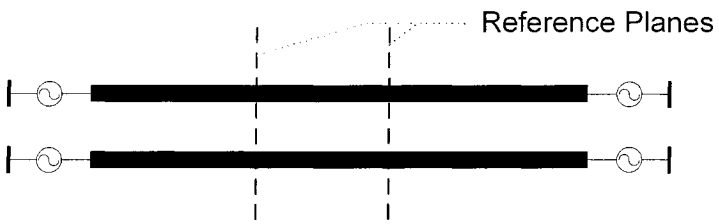


Fig.2.11. A coupled microstrip line under study.

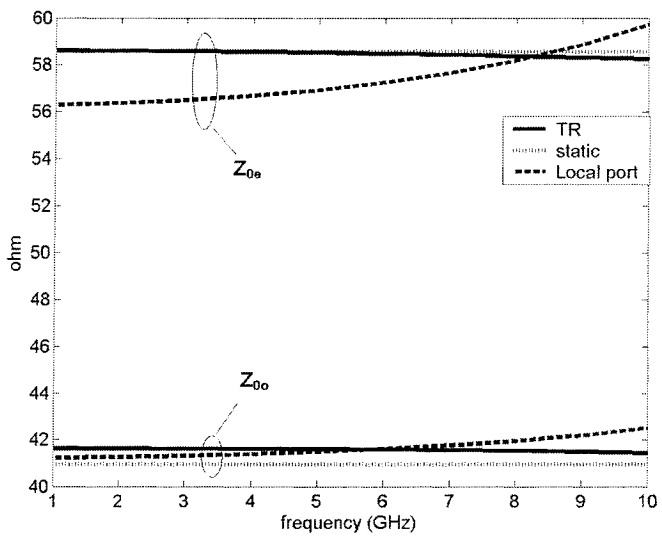


Fig.2.12. 3D properties of the characteristic impedance of a microstrip line obtained from a multi-parallel-port TR calibration together with the data obtained without the calibration (local port) and the data obtained from a 2D method [reference ???] ($\varepsilon_r = 2.2$, w = 30 mil, h = 10 mil and s = 5 mil).

2.4 Summary

We have proposed and developed two new schemes, namely, 2-port TR calibration technique and multi-parallel-port TR calibration technique, for the parameter extraction of planar discontinuities and circuits. These calibration techniques can easily be integrated with existing commercial full-wave MoM packages. They make use of MoM simulation results and removes error effects due to the port discontinuities involved in the simulation by formulating thru and resistor standards. The 2-port TR calibration technique makes use of one thru standard and one resistor standard. The multi-parallel port TR calibration utilizes one thru standard, one multi-match standard and one multi-resistor standard. The TR calibration techniques assume that the error boxes are symmetrical and reciprocal. Therefore, the numerical TR calibration techniques cannot be applied in most practical measurements.

Two microstrip open-ends and a microstrip coupled line have been studied, which has validated the proposed TR calibration technique. The proposed technique overcomes the characteristic impedance problem of the TRL calibration, which should be known a priori exactly. Because no line standard is used in the TR calibration, the TR calibration technique does not have limitation of frequency range.

CHAPTER 3

PORT DISCONTINUITY AND ERROR ANALYSIS

In the above chapters, the numerical TRL and TR calibration techniques are described. By using such numerical calibration techniques, the port discontinuity effects can be removed and correct equivalent circuit models of the core planar discontinuities can be extracted from field simulations. In this chapter, we will discuss the port discontinuities and analyze the error influences. First of all, we will extract the circuit model of a port discontinuity. Then, we will discuss how the port discontinuity brings error effects to parameters of the circuit model of the DUT.

3.1 Equivalent circuit model of the port discontinuity

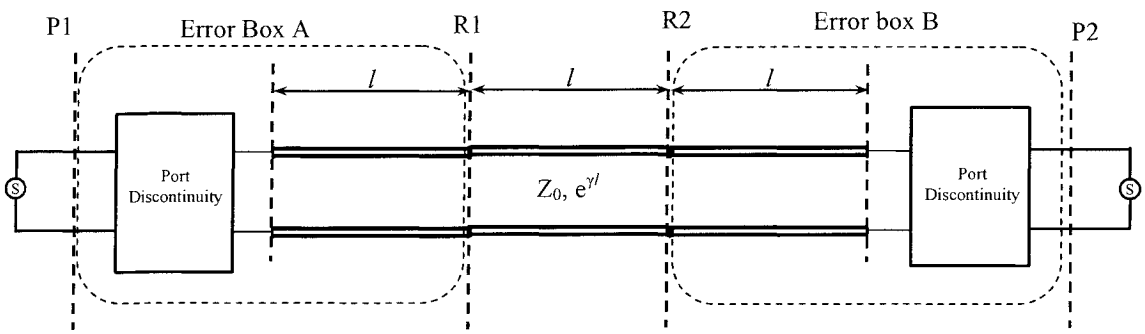


Fig.3.1. Equivalent network connection of a transmission line section.

To obtain the circuit model of a port discontinuity between the exciting port and the microstrip feed line, we can use the same section of transmission line as the feed line instead of the DUT [20], as shown in Fig.3.1. The error boxes comprise the port discontinuity and the feed line. Since the transmission line is physically identical to the feed line, the error box A can be expressed by,

$$[T_A] = [T_P][T_l], \tag{3.1}$$

here [T$_P$] is T-matrix of the port discontinuity and [T$_l$] is T-matrix of the transmission line. From the numerical calibration, we can remove out the error boxes and obtain the correct parameters of the transmission line [T$_l$]. Then we can get the T-matrix of the port discontinuity by

$$[T_P] = [T_A][T_l]^{-1}. \tag{3.2}$$

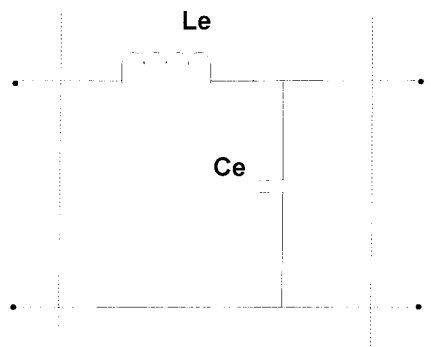
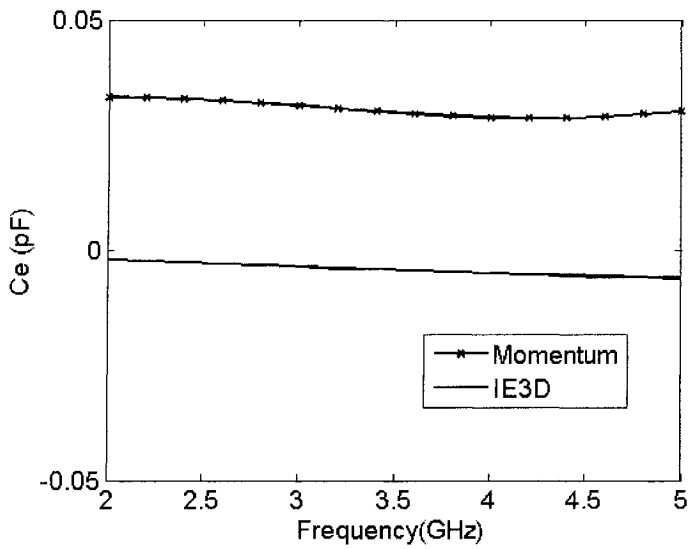


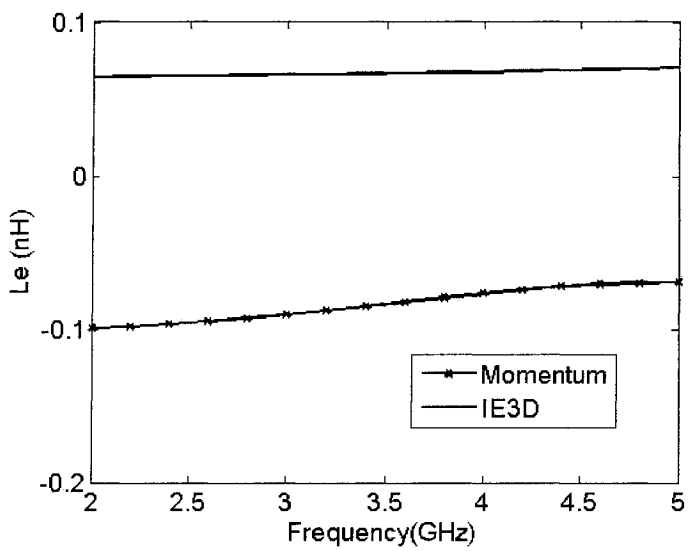
Fig.3.2. Equivalent circuit model of the port discontinuity.

By using the method that we described above, we can calculate parameters of the port discontinuities involved in the examples in Chapters 1 and 2. As in [20], the equivalent

circuit model of the port discontinuity can be represented by a shunt capacitor and a series inductor (the very small loss related resistor/conductor is neglected), as shown in Fig.3.2. In our investigation, two kinds of commercial EM software are used: one is MOMENTUM of ADS while the other is IE3D of Zeland. Results of the extracted circuit models of the port discontinuities with alumina substrate (ε_r = 9.9, w = h = 0.635mm) are shown in Fig.3.3. And also, results of the extracted circuit models of the port discontinuities with Duroid 5880 substrate (ε_r = 2.2, h = 0.254mm, W=0.762mm) are shown in Fig.3.4. We can see that the values of elements in the circuit models of the port discontinuities keep almost unchanged when frequency increases. Using a different substrate or a different type of EM software, the values of elements in the circuit models are different. The reason is that, in a different kind of EM software, a different exciting scheme is used such as vertical source or horizontal source, and current source or voltage source. With different substrate and different line width, the values of elements in the circuit models of the port discontinuities are different. It is quite similar to the circuit model of a microstrip step that will be studied in Chapter 4.

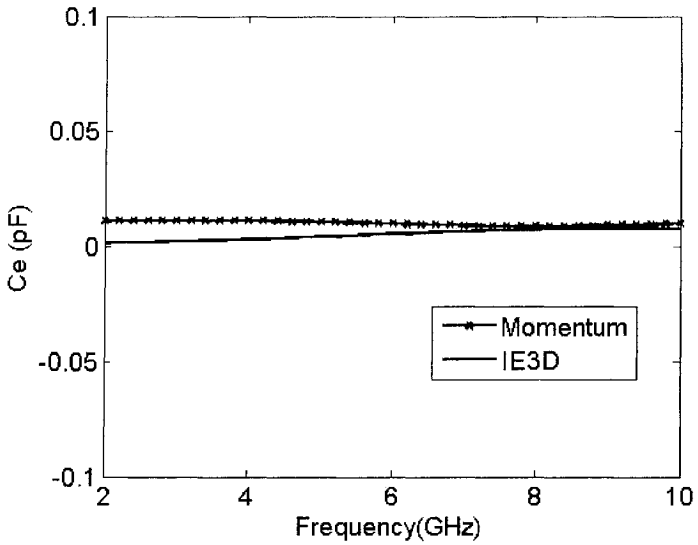


(a)

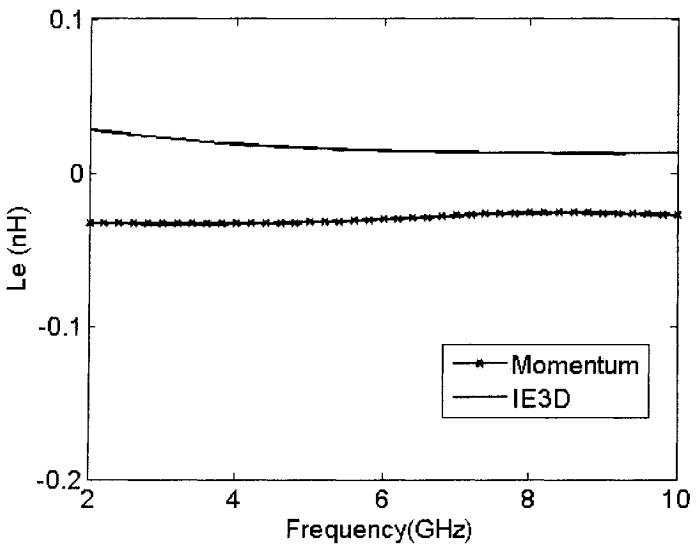


(b)

Fig.3.3. Calculated parameters of a port discontinuity with alumina substrate (w = h = 0.635mm, $\varepsilon_r = 9.9$).



(a)



(b)

Fig.3.4. Calculated parameters of a port discontinuity with Duroid 5880 substrate(ε_r = 2.2, h = 0.254mm, W=0.762mm).

3.2 Effects of the port discontinuity on the extracted one-port circuit model.

The port discontinuity is caused by the difference in distribution of electrical and magnetic fields between the port and the feed line. The port discontinuity is generally not obvious if we just pay attention to the S-parameters, which will be discussed in the followings. However, if we want to extract the circuit model of a planar discontinuity that is usually electrically small, the port discontinuity may bring out a large error. For example, the S-parameters of a port discontinuity used in the example (as shown in Fig. 1.6) are shown in Table 3.1. We can see that S11 of the port discontinuity is very small and S21 is almost equal to one. How a small parasitic effect of the port discontinuity can bring a large error in the extracted circuit model? We can do an analysis in the followings.

Table 3.1. S-parameters of a port discontinuity with alumina substrate (w = h = 0.635mm, $\varepsilon_r = 9.9$)

frequency(Hz)	magS11	angS11°	magS21	angS21°	magS12	angS12°	magS22	angS22°
2.00E+09	0.0228	-98.5080	0.9993	0.0967	0.9993	0.0967	0.0230	-79.3177
2.20E+09	0.0249	-99.8354	0.9991	0.0935	0.9991	0.0935	0.0251	-77.7410
2.40E+09	0.0268	-101.1451	0.9989	0.0870	0.9989	0.0870	0.0270	-76.1856
2.60E+09	0.0286	-102.3904	0.9987	0.0777	0.9987	0.0777	0.0288	-74.7000
2.80E+09	0.0302	-103.5161	0.9984	0.0658	0.9984	0.0658	0.0305	-73.3337
3.00E+09	0.0316	-104.4610	0.9981	0.0519	0.9981	0.0519	0.0320	-72.1349
3.20E+09	0.0328	-105.1629	0.9979	0.0363	0.9979	0.0363	0.0333	-71.1480
3.40E+09	0.0339	-105.5653	0.9976	0.0194	0.9976	0.0194	0.0345	-70.4118
3.60E+09	0.0349	-105.6279	0.9973	0.0016	0.9973	0.0016	0.0356	-69.9559
3.80E+09	0.0359	-105.3372	0.9971	-0.0170	0.9971	-0.0170	0.0366	-69.7969
4.00E+09	0.0370	-104.7166	0.9968	-0.0364	0.9968	-0.0364	0.0376	-69.9356
4.20E+09	0.0382	-103.8398	0.9966	-0.0586	0.9966	-0.0586	0.0387	-70.3478
4.40E+09	0.0396	-102.8065	0.9964	-0.0855	0.9964	-0.0855	0.0399	-70.9968
4.60E+09	0.0412	-101.7448	0.9963	-0.1151	0.9963	-0.1151	0.0414	-71.8388
4.80E+09	0.0433	-100.8693	0.9960	-0.1479	0.9960	-0.1479	0.0433	-72.6605
5.00E+09	0.0455	-100.2153	0.9957	-0.1826	0.9957	-0.1826	0.0455	-73.3126

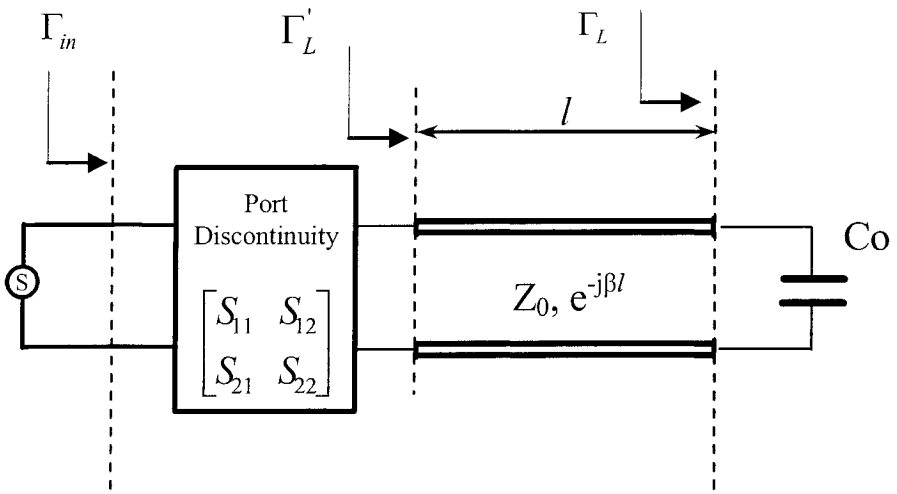


Fig.3.5. Network representation of an open-end capacitor.

In Fig.3.5, the circuit model of an one-port planar discontinuity under parameter extraction is shown. The Γ_L is a reflection coefficient of this one-port planar discontinuity. The feed line connects with the planar discontinuity and the exciting port. The port discontinuity is of course unknown in this case. We assume that the port discontinuity is nevertheless reciprocal and lossless. The S parameters of the port discontinuity can simply be expressed by three variables: a, Φ_1, and Φ_2 as follows

$$S_{11} = a \cdot e^{j\phi_1}, \tag{3.3}$$

$$S_{22} = a \cdot e^{j\phi_2}, \tag{3.4}$$

$$S_{12} = \sqrt{1 - a^2} \cdot e^{j(\phi_1 + \phi_2 \pm \pi)/2}. \tag{3.5}$$

At low frequency in the port discontinuity as shown in Table 3.1, for example, a is very small. Therefore, we can obtain

$$\Gamma_{in} = S_{11} + \frac{S_{12}^2 \Gamma_L^{'}}{1 - S_{22}\Gamma_L^{'}} \approx \Gamma_L^{'} e^{j(\phi_1+\phi_2\pm\pi)} + ae^{j\phi_2} e^{j(\phi_1+\phi_2\pm\pi)} \Gamma_L^{'2} + ae^{j\phi_1}. \quad (3.6)$$

We can see that there are three factors a, ϕ_1 and ϕ_2, which are responsible for the difference in magnitude or angle of Γ_{in} and $\Gamma_L^{'}$. If a is very small, this difference in magnitude is very small such that the error is not obvious regarding the reflection coefficient. In the following, we can see that a little error in phase or in magnitude of the reflection coefficient will bring a large error in the extracted circuit model.

From the transmission line theory, the relationship between Γ_L and $\Gamma_L^{'}$ is formulated by

$$\Gamma_L = \Gamma_L^{'} e^{j2\phi_0}. \quad (3.7)$$

The admittance of the load can be expressed as

$$Y_L = Y_0 \frac{1-\Gamma_L}{1+\Gamma_L} = Y_0 \frac{1-\Gamma_L^{'} e^{j2\phi_0}}{1+\Gamma_L^{'} e^{j2\phi_0}} = G + j\omega C_O. \quad (3.8)$$

When the denominator in this question $1+\Gamma_L^{'} e^{j2\phi_0} \approx 0$, the little error (brought by the port discontinuity) in $\Gamma_L^{'}$ will generate a large error into the extracted C_O. This region (the denominator approaches zero) is not easy to avoid because it is decided by the end load Γ_L and the length of the feed line. This can explain why the extracted C_O without any calibration exhibits a periodical variation around the true C_O value, as shown in Fig.1.7. In the example in connection with Fig.1.7 at f = 3GHz, the calculated values of the open-end from the TRL calibration are C = 53.7pF/m and Γ = 0.997∟-3.368°. Without calibration (only the conventional transmission line theory is used), the

calculated values of the open-end are C' = 93.7pF/m and Γ' = 0.9965$\angle$-5.876°. We can notice that the calculated capacitance error is almost 100% if no calibration is applied.

The scenario of this microstrip open-end example can naturally be generalized into other circuits. Although the port discontinuity may not bring a significant error in extracted circuit model parameters of planar discontinuity in some cases, it is difficult to predict what kind of planar circuit is not sensitive to the port discontinuity and how long the feed line should be. Therefore, the calibration techniques are absolutely necessary to remove the efforts of port discontinuity.

3.3 Effects of the port discontinuity on the extracted two-port circuit models.

The above error analysis is presented for one-port circuits. The following discussion is presented for two-port circuits. Once we obtain S-parameters (or T-parameters) of the core circuit by removing the error box effects, we are able to build up a circuit model of the core circuit. Since the TRL calibration procedure works with the T and S parameters, we cannot directly generate Z or Y parameters of the circuit. In this case, a circuit model should be generated on the basis of a conversion from S parameters to Z or Y parameters.

For simplicity, we consider a lossless and reciprocal 2-port network. The S parameters can simply be expressed by 3 variables: a, Φ_1, and Φ_2, as formulated in equations (3.3)-(3.5). The normalized Z parameters can then be written as in equations (3.9)-(3.11), which have a same denominator. Similarly, the normalized Y parameters

can also be formulated in Equations (3.12)-(3.14), which also have another same denominator. But the common denominator in Z parameters is different from that in Y parameters. If the denominator approaches zero, errors in the calculated S parameters of the circuit will be amplified and pronounced, resulting in much large errors in the converted Z parameters. Therefore, we should be careful when S parameters happens to be close to the region of a zero denominator.

$$\overline{Z}_{11} = \frac{1 + a \cdot (e^{j\phi_1} - e^{j\phi_2}) - e^{j(\phi_1+\phi_2)}}{1 - a \cdot (e^{j\phi_1} + e^{j\phi_2}) + e^{j(\phi_1+\phi_2)}}. \tag{3.9}$$

$$\overline{Z}_{22} = \frac{1 - a \cdot (e^{j\phi_1} - e^{j\phi_2}) - e^{j(\phi_1+\phi_2)}}{1 - a \cdot (e^{j\phi_1} + e^{j\phi_2}) + e^{j(\phi_1+\phi_2)}}. \tag{3.10}$$

$$\overline{Z}_{12} = \frac{2\sqrt{1-a^2} \cdot e^{j(\phi_1+\phi_2 \pm \pi)/2}}{1 - a \cdot (e^{j\phi_1} + e^{j\phi_2}) + e^{j(\phi_1+\phi_2)}}. \tag{3.11}$$

$$\overline{Y}_{11} = \frac{1 - a \cdot (e^{j\phi_1} - e^{j\phi_2}) - e^{j(\phi_1+\phi_2)}}{1 + a \cdot (e^{j\phi_1} + e^{j\phi_2}) + e^{j(\phi_1+\phi_2)}}. \tag{3.12}$$

$$\overline{Y}_{22} = \frac{1 + a \cdot (e^{j\phi_1} - e^{j\phi_2}) - e^{j(\phi_1+\phi_2)}}{1 + a \cdot (e^{j\phi_1} + e^{j\phi_2}) + e^{j(\phi_1+\phi_2)}}. \tag{3.13}$$

$$\overline{Y}_{12} = -\frac{2\sqrt{1-a^2} \cdot e^{j(\phi_1+\phi_2 \pm \pi)/2}}{1 + a \cdot (e^{j\phi_1} + e^{j\phi_2}) + e^{j(\phi_1+\phi_2)}}. \tag{3.14}$$

In the following, an error analysis can be made regarding this aspect. First of all, we can formulate differential forms $\overline{dZ}/da$ and $\overline{dZ}/d\phi$ as in equation (3.15)-(3.23). Some typical examples of correlation between $\overline{dZ}/da$, $\overline{dZ}/d\phi$ and a, ϕ ($Z_1 = \overline{Z}_{11} - \overline{Z}_{12}$, $Z_2 = \overline{Z}_{22} - \overline{Z}_{12}$, $Z_3 = \overline{Z}_{12}$) are shown in Fig.3.6 (a~g). In Fig.3.6

(a), $\phi_1 = 20^\circ$, $\phi_2 = 170^\circ$ and $d(1/Z_3)/da$ versus a are shown in the range of a from 0 to 1. In Fig.3.6 (b,c,d), $\phi_2 = 0^\circ$ and a = 0.1, 0.5, 0.9, respectively, $dZ/d\phi_1$ versus ϕ_1 are shown in the range of ϕ_1 from -180° to 180°. In Fig.3.6 (e,f,g), $\phi_2 = 90^\circ$ and a = 0.1, 0.5, 0.9, respectively, $dZ/d\phi_1$ versus ϕ_1 are also shown in the range of ϕ_1 from -180° to 180°. From such numerical examples in Fig.3.6 (a~g), we can see that in some regions, the errors on the calculated a, ϕ of the core circuit will cause a much larger error on Z parameters of the core circuit. These regions move around as a and ϕ change and such regions become larger when a approaches 1. Therefore, after the error due to the port discontinuities is removed by using the numerical calibration techniques, we can obtain accurate extracted circuit parameters so that we can get the correct circuit model of the core circuit. In Fig.3.6 (a) we can see that when a approaches 0, dZ_3/da becomes much more significant than $d(1/Z_3)/da$, it means that the error in a becomes less pronounced in $1/Z_3$. That is because they have different denominators, and the regions of denominator approaching zero are different. Sometimes if one of the inductances in the circuit model has a large error, we may replace it by a capacitance in order to reduce the error. So how we chose Z parameters (T type circuit) or Y parameters (II type circuit) to build the circuit model is very important for reducing the error.

$$\frac{\overline{dZ}_{12}}{da} = \frac{-2\left[e^{j\phi_1} + e^{j\phi_2} - a - a\cdot e^{j(\phi_1+\phi_2)}\right] e^{j(\phi_1+\phi_2\pm\pi)/2}}{\sqrt{1-a^2}\cdot\left[1 - a\cdot(e^{j\phi_1} + e^{j\phi_2}) + e^{j(\phi_1+\phi_2)}\right]^2}. \tag{3.15}$$

$$\frac{\overline{dZ}_{22}}{da} = \frac{2e^{j\phi_2}\left[1-e^{j2\phi_1}\right]}{\left[1-a\cdot(e^{j\phi_1}+e^{j\phi_2})+e^{j(\phi_1+\phi_2)}\right]^2}. \tag{3.16}$$

$$\frac{\overline{dZ}_{12}}{da} = \frac{-2\left[e^{j\phi_1}+e^{j\phi_2}-a-a\cdot e^{j(\phi_1+\phi_2)}\right]e^{j(\phi_1+\phi_2\pm\pi)/2}}{\sqrt{1-a^2}\cdot\left[1-a\cdot(e^{j\phi_1}+e^{j\phi_2})+e^{j(\phi_1+\phi_2)}\right]^2}. \tag{3.17}$$

$$\frac{\overline{dZ}_{11}}{d\phi_1} = \frac{j2\left[a\cdot e^{j\phi_1}-e^{j(\phi_1+\phi_2)}\right]\cdot\left[1-a\cdot e^{j\phi_2}\right]}{\left[1-a\cdot(e^{j\phi_1}+e^{j\phi_2})+e^{j(\phi_1+\phi_2)}\right]^2}. \tag{3.18}$$

$$\frac{\overline{dZ}_{22}}{d\phi_2} = \frac{j2(ae^{j\phi_2}-e^{j(\phi_1+\phi_2)})\cdot(1-ae^{j\phi_1})}{\left[1-a\cdot(e^{j\phi_1}+e^{j\phi_2})+e^{j(\phi_1+\phi_2)}\right]^2}. \tag{3.19}$$

$$\frac{\overline{dZ}_{11}}{d\phi_2} = \frac{j2(a^2-1)e^{j(\phi_1+\phi_2)}}{\left[1-a\cdot(e^{j\phi_1}+e^{j\phi_2})+e^{j(\phi_1+\phi_2)}\right]^2}. \tag{3.20}$$

$$\frac{\overline{dZ}_{22}}{d\phi_1} = \frac{j2(a^2-1)e^{j(\phi_1+\phi_2)}}{\left[1-a\cdot(e^{j\phi_1}+e^{j\phi_2})+e^{j(\phi_1+\phi_2)}\right]^2}. \tag{3.21}$$

$$\frac{\overline{dZ}_{12}}{d\phi_1} = \frac{-j\sqrt{1-a^2}\,e^{j(\phi_1+\phi_2\pm\pi)/2}\left[1+a\cdot(e^{j\phi_1}-e^{j\phi_2})-e^{j(\phi_1+\phi_2)}\right]}{\left[1-a\cdot(e^{j\phi_1}+e^{j\phi_2})+e^{j(\phi_1+\phi_2)}\right]^2}. \tag{3.22}$$

$$\frac{\overline{dZ}_{12}}{d\phi_2} = \frac{-j\sqrt{1-a^2}\,e^{j(\phi_1+\phi_2\pm\pi)/2}\left[1-a\cdot(e^{j\phi_1}-e^{j\phi_2})-e^{j(\phi_1+\phi_2)}\right]}{\left[1-a\cdot(e^{j\phi_1}+e^{j\phi_2})+e^{j(\phi_1+\phi_2)}\right]^2}. \tag{3.23}$$

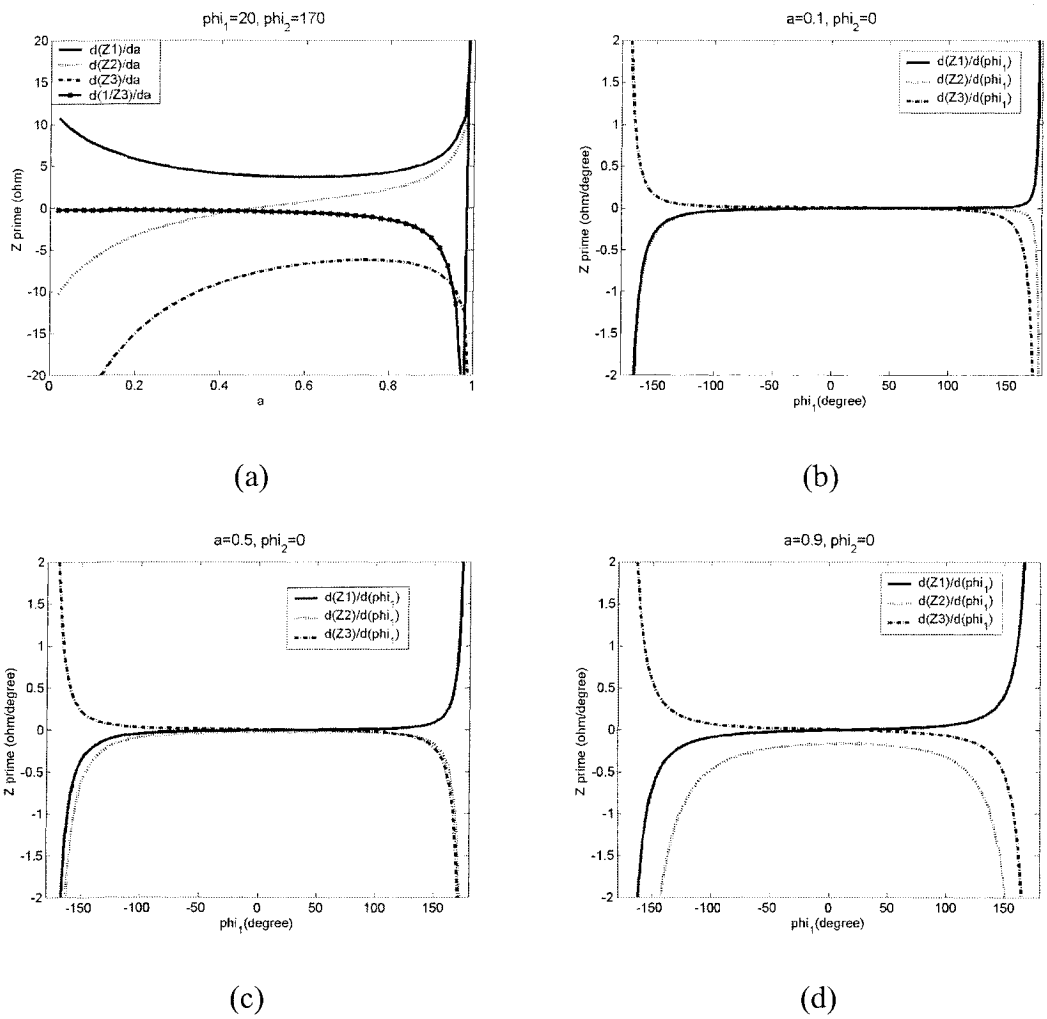
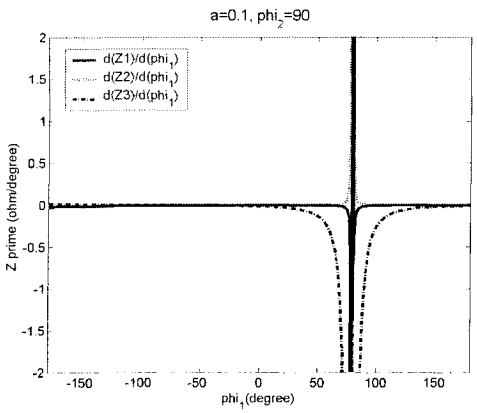
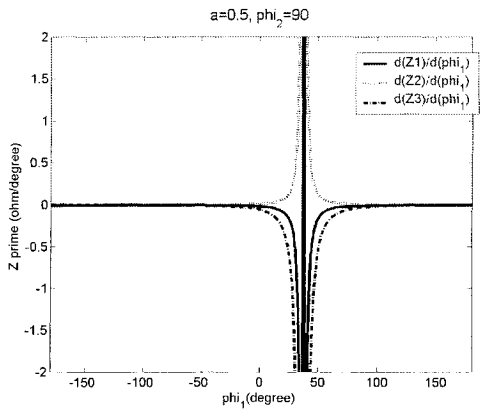
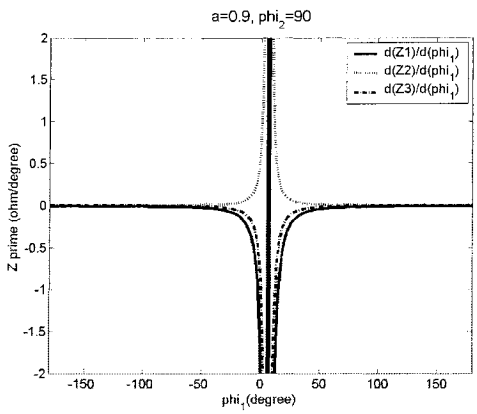


Fig.3.6. Examples of correlations between $\overline{dZ}/da$, $\overline{dZ}/d\phi$ and a, ϕ. (a) $\overline{dZ}/da$ when ϕ_1=20 and ϕ_2=170. (b), (c), (d) $\overline{dZ}/d\phi_1$ when ϕ_2=0 and a=0.1, 0.5, 0.9 respectively. (e)(f)(g) $\overline{dZ}/d\phi_1$ when ϕ_2=90 and a=0.1, 0.5, 0.9 respectively.





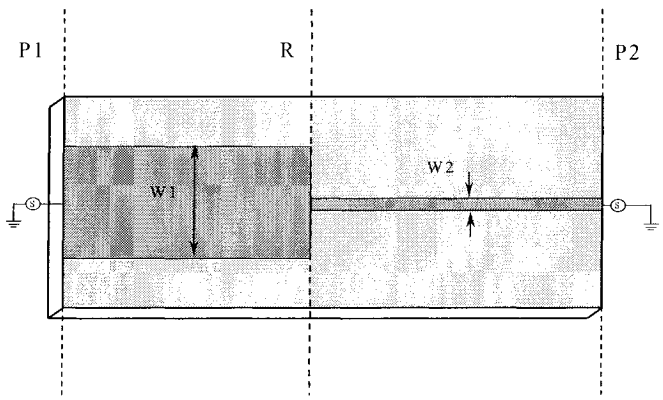
(e) (f)



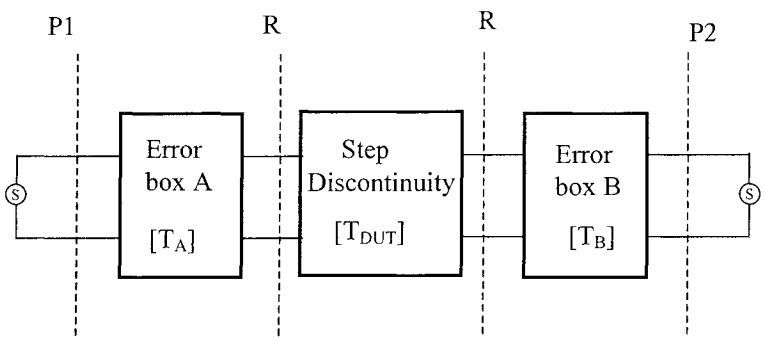
(g)

Fig.3.6. Continued

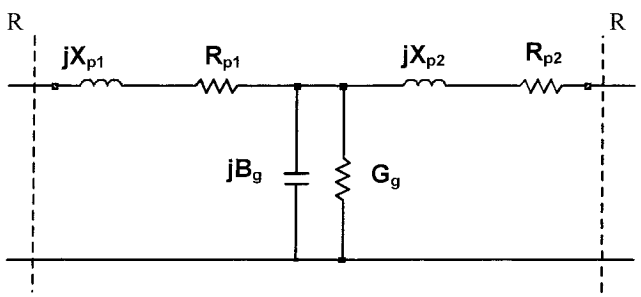
An example of a step discontinuity of microstrip line can be used to demonstrate the effect of port-discontinuities on two-port circuits. The physical layout of the step discontinuity simulated with the Momentum is shown in Fig.3.7(a). In Fig.3.7(b), the network model of this layout consists of 3 parts, namely, error box A, error box B, and step discontinuity or the core circuit for which the characteristic parameters are to be extracted. The error boxes include effects due to the port discontinuity and the connect line from the port to the step discontinuity. Using the proposed numerical TRL calibration, we can effectively remove the error boxes and obtain the parameters for the step discontinuity. As the characteristic impedance of the lines at both sides is different, we should use two TRL procedures based on different reference impedances to calculate the two error boxes, respectively.



(a)



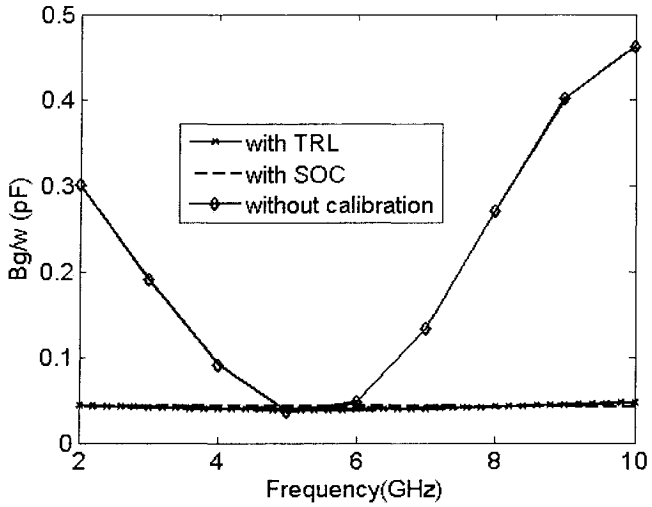
(b)



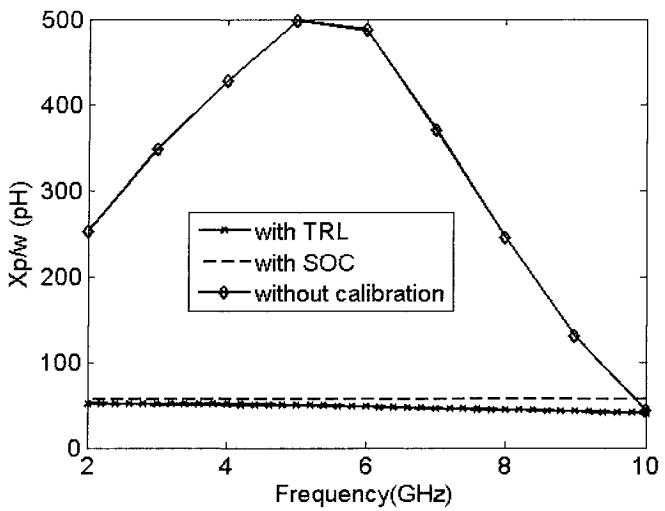
(c)

Fig.3.7. Geometry and equivalent circuit model of a step discontinuity of microstrip line. (a) Physical layout in Momentum. (b) Equivalent network. (c) Circuit model of the step discontinuity.

The equivalent full-wave circuit model of the step discontinuity can be expressed in terms of one shunt capacitive admittance and two series inductive impedances [18], as shown in shown in Fig.3.7(c). The extracted parameters of the circuit model are shown in Fig.3.8(a) and (b). Results of the resistor and conductance in the circuit model of Fig.3.7(c) are very small and are not shown here. We can see that the results obtained from the proposed TRL calibration scheme are comparable to those of the SOC calibration [18]. Without the calibration, the port discontinuity will make the accurate parameter extraction impossible. At 10GHz, the S-parameter of the step discontinuity is: a=0.051, ϕ_1=-105.5°, and ϕ_2=-86.64°. From the equations (3.9)-(3.11), the correlations between L, C and a, ϕ are shown in Fig.3.9. We can obtain $dL/da = 8.2\times10^3 (pH/unit)$, $dC/da = -100(pF/unit)$ from equations (3.15)-(3.17). From this value, we can conclude that a small port discontinuity can bring up a large error in the calculated inductance and capacitance as evidenced in Fig.3.9. This is why the calibration procedure is absolutely necessary for the accurate circuit model extraction in this case.



(a)



(b)

Fig.3.8. TRL-extracted parameters of a step discontinuity compared with those generated from other three methods: static, SOC technique [18] and Z_0-scheme (without calibration)[18] (ε_r = 10.2, h = 0.635mm, W_1=2.0mm, W_2 = 0.4mm) ($X_p = X_{p1} + X_{p2}$). (a) Bg/ ω. (b) Xp/ω.

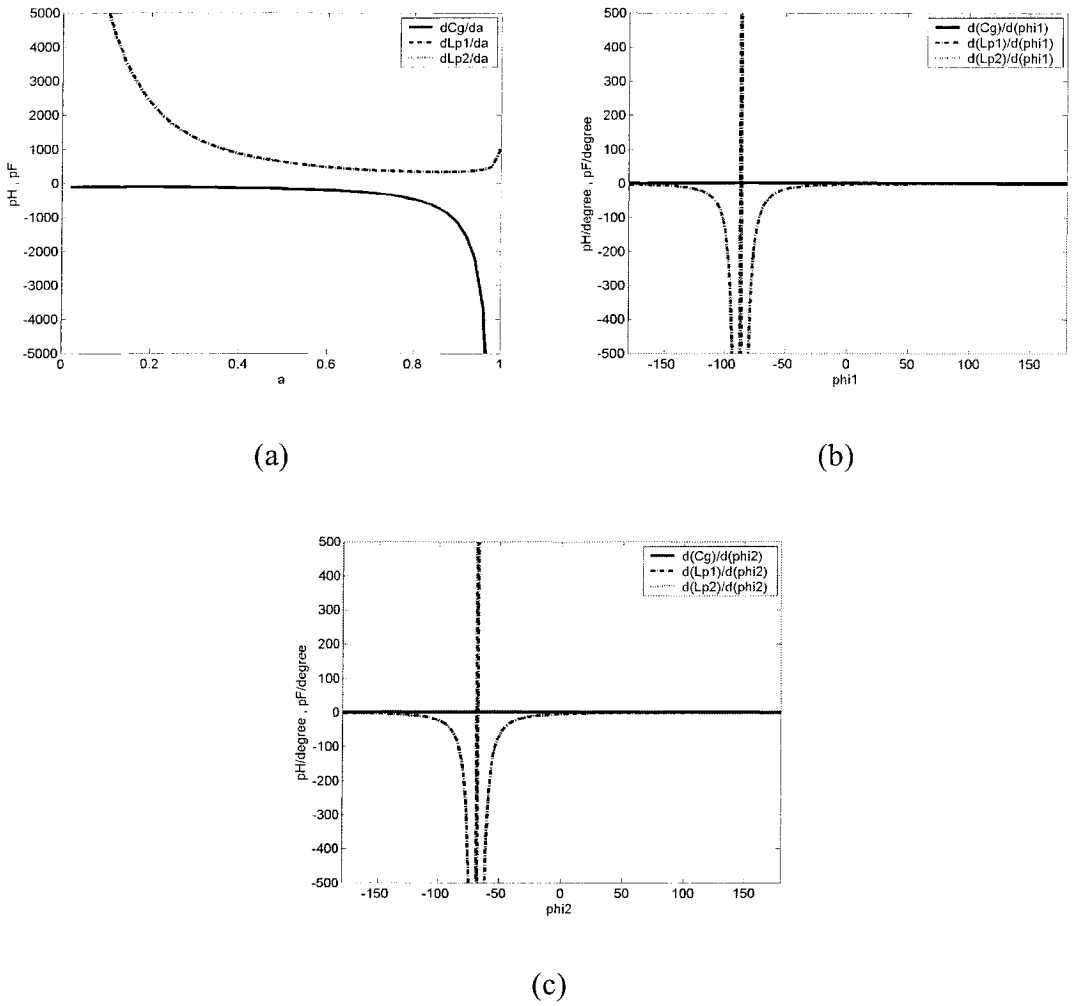


Fig.3.9. Typical numerical correlations between L, C and a, ϕ. (a) dCg/da and dLp/da. (b) $dCg/d\phi_1$ and $dLp/d\phi_1$. (c) $dCg/d\phi_2$ and $dLp/d\phi_2$.

3.4 Summary

The equivalent circuit model of port discontinuities has been extracted by using the numerical calibration techniques. It has been shown that the model can be represented in terms of a shunt capacitor and a series inductor. Different exciting scheme has a different circuit model. Through our analysis of the error models, we can observe that the port discontinuity generally brings very little change in magnitude of the S-parameters. However, once we transform the S-parameters to Z or Y counterparts for generating equivalent circuit models of the core planar discontinuities, this little error in magnitude or phase in connection with the S-parameters may cause a huge error in the extracted circuit models. Therefore, the numerical calibration techniques are absolutely necessary and they offer a special capability of removing effects of the port discontinuities and generating the correct circuit models of planar circuits under modeling

CHAPTER 4

ACCURATE MODELING OF MICROSTRIP DISCONTINUITIES

4.1 Introduction

With the calibration techniques we proposed, the errors brought by the port discontinuities can effectively be removed, and the parameters of simulated planar discontinuities can accurately be extracted. On the basis of the correct extracted parameters, the full-wave equivalent circuit model of the planar discontinuities can be established. By combining the proposed calibration techniques with commercial Method-of-Moment (MOM) packages, the procedure for extracting the full-wave equivalent circuit model becomes very simple.

As we mentioned before, the microwave circuit can be regarded as a set of cascaded discontinuities and transmission line sections. With the extracted full-wave circuit model of planar discontinuities, we can design the microwave circuit based on the network topologies. So the design procedure is very efficient and accurate because network-based synthesis and optimization are widely available. In this chapter, we will extract the full-wave circuit model of several typical microstrip discontinuities and make the design of microwave circuit based on the extracted circuit models.

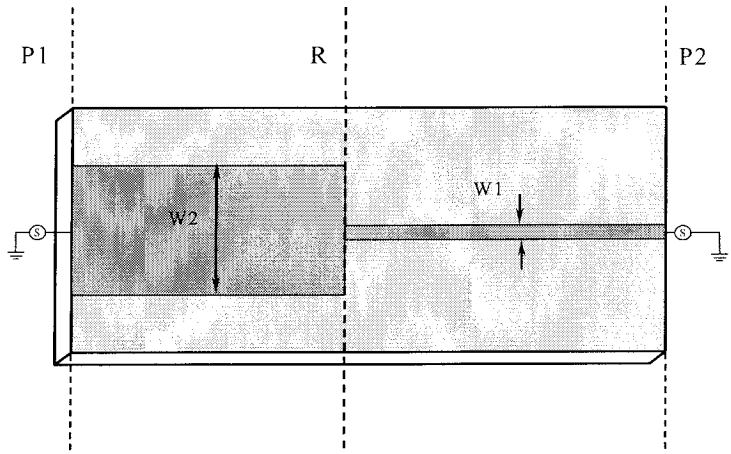
A large amount of work has been done for extracting full-wave equivalent circuit models of microstrip discontinuities based on the SOC technique. In the previous Chapters, the circuit models of microstrip open-end discontinuities are extracted by

using the proposed numerical calibration techniques, and they agree with the static models or the extracted circuit models by other techniques, which have well been validated.

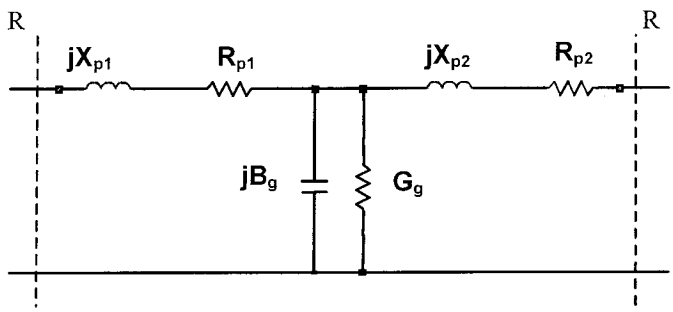
4.2 Circuit model of microstrip step and low pass filter design

4.2.1 Extraction of the circuit model of microstrip step

We will extract the circuit models of microstrip steps, which are a set of popular building blocks in microwave integrated circuits. In our work, Rogers Duroid 5880 is chosen as the substrate of these microstrip discontinuities for simulation and parameter extractions. So far, the full-wave circuit model of microstrip discontinuities based on this substrate is rarely studied. Frequency range is selected from 20GHz to 40 GHz. The IE3D package of Zeland is used in our investigation. In simulation with the IE3D, a local port model is pre-selected instead of other port models for the deterministic or direct MoM algorithm as detailed in [19].



(a)



(b)

Fig.4.1. Geometry and equivalent circuit model of a step discontinuity. (a)Physical layout in Momentum; (b)Circuit model of the step discontinuity.

The physical layout of the step discontinuity is shown in Fig.4.1(a). The height of the substrate is 0.254mm, and the width of transmission line varies between 10 mil and 60 mil. As the characteristic impedance of the lines at both sides is different, we should use two TRL procedures based on different reference impedance to calculate the two error boxes respectively. The equivalent full-wave circuit model of the step discontinuity can

be expressed by one capacitive shunt admittance, two series inductive impedances and the radiation related resistors and conductance [18], as shown in Fig.4.1 (b).

The extracted parameters of the circuit model are shown in Fig.4.2. When W2 is smaller than or equal to 40mil, we can observe that as the frequency increases the inductance Xp/ω and capacitance Bg/ω are almost unchanged (Xp/ω increases a little but Bg/ω decreases a little, so they exhibit lumped element property), and the radiation loss related shunt conductance Gg increases; as the width of the wider line W2 increases, Xp/ω, Bg/ω and Gg increase; as the width of the thinner line W1 increases, Xp/ω, Bg/ω and Gg decrease. The greater the step changes, the bigger Xp/ω, Bg/ω and Gg are. That is because when the current flows from longitudinal to transverse directions on the edge of the wider line around the step, the curvature of the current density increases. When W2 is equal to 60mil, we can see that Xp/ω and Bg/ω changes irregularly as frequency increases. That is because the microstrip step can only be considered as a lumped element on condition that the size of the step is much smaller than one wavelength. In this substrate, one wavelength at 30GHz is about 7 mm, and one quarter wavelength is about 1.8mm. When W2 is 60 mil (1.524mm), it approaches one quarter wavelength. Therefore, the values of elements in the equivalent circuit models vary irregularly when frequency increases. The small negative value of the series resistance Rp may represent the EM power exchange between the series and shunt parameters in this T-type network and can be ignored in the circuit model [18].

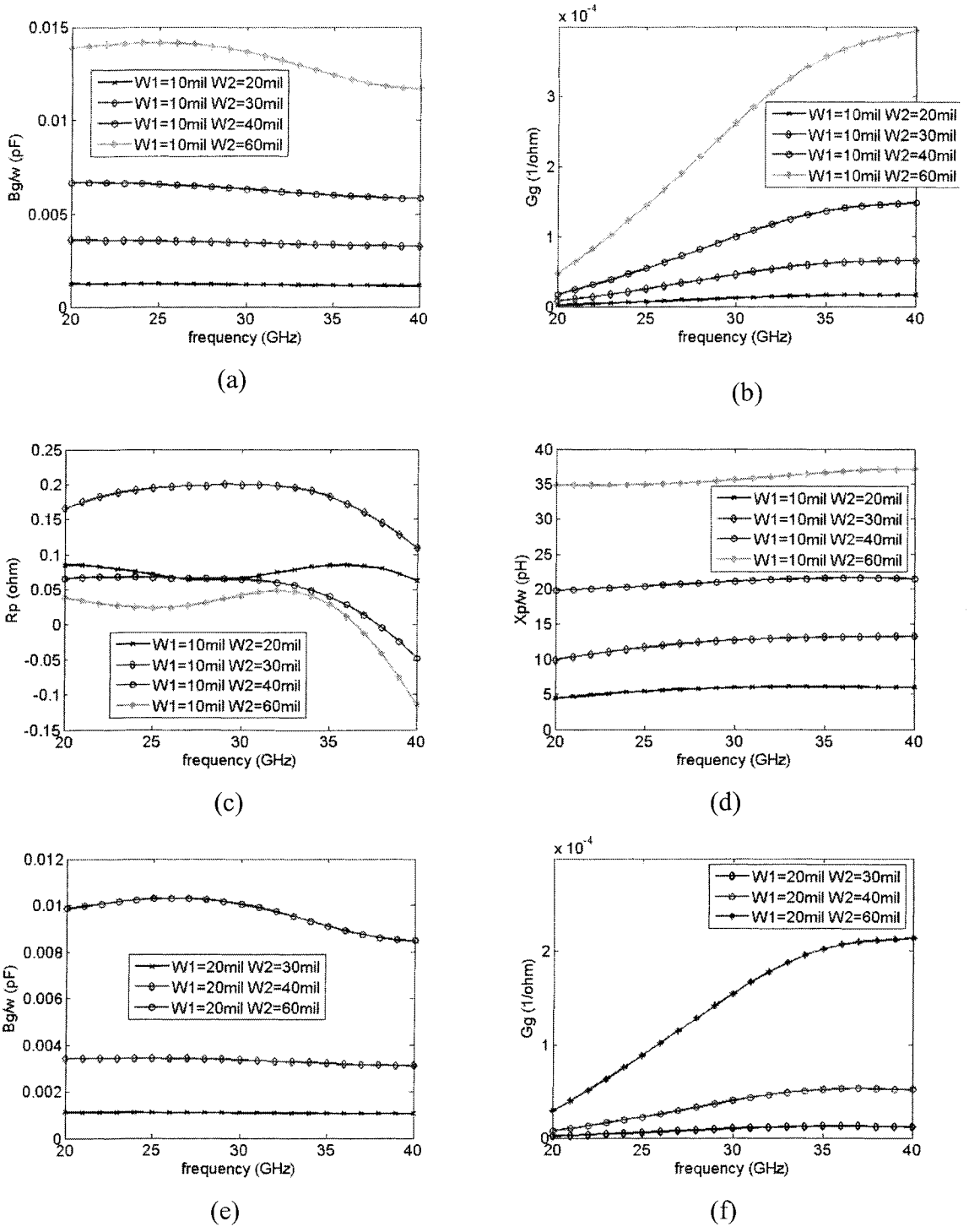
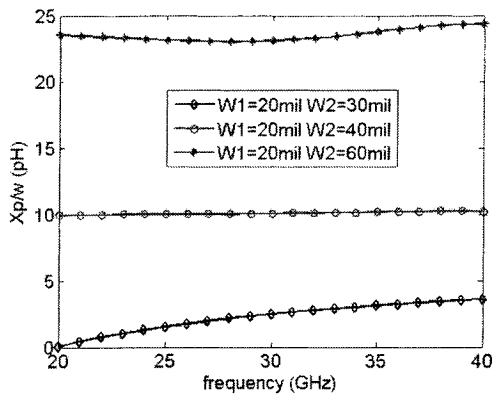
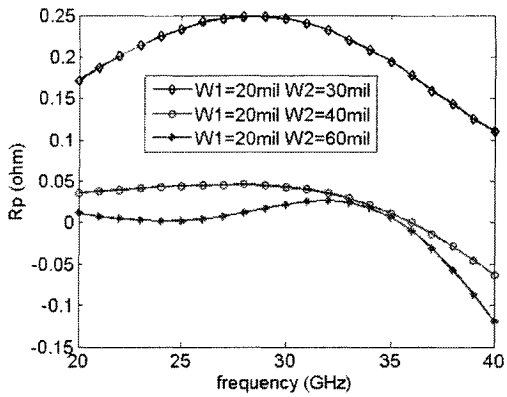


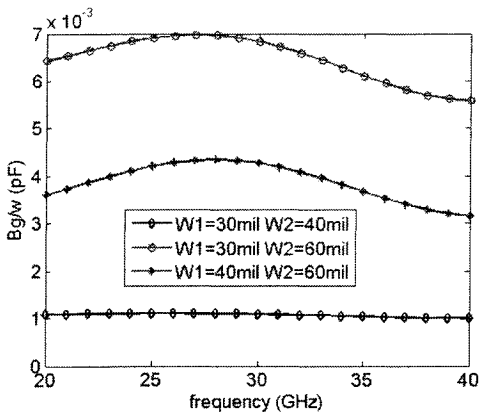
Fig.4.2. Extracted parameters of the circuit model of microstrip step (ε_r = 2.2, h = 0.254mm) ($X_p = X_{p1} + X_{p2}, R_p = R_{p1} + R_{p2}$).



(g)



(h)



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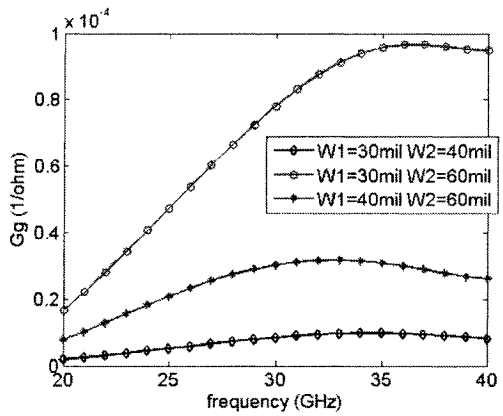

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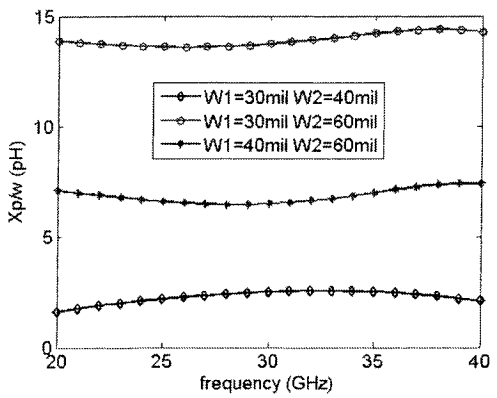

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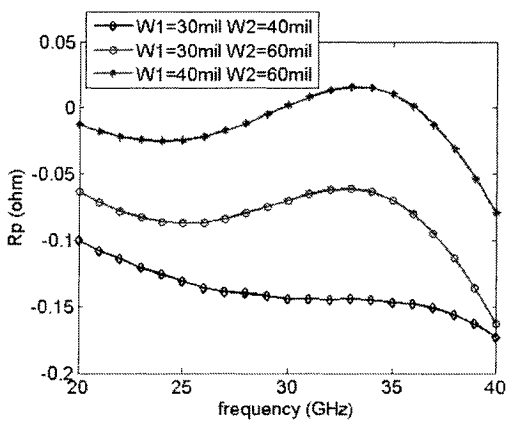


(l)

Fig.4.2. Continued

4.2.2 Low pass filter design

A low pass filter that involves microstrip steps is designed by using the extracted circuit models in 4.2.1, as shown in Fig.4.3. By using the circuit models, the circuit can be analyzed as a network that consists of cascaded microstrip lines and microstrip discontinuities. The whole layout of the low pass filter is thus decomposed into small pieces. Each piece is one discontinuity or a section of microstrip line, as shown in Fig.4.4. Simulation and optimization of the circuit becomes straightforward and very easy. The circuit is also simulated in this work by Hewlett-Packard Momentum package and fabricated. There are little differences between the simulated results based on the extracted circuit models and measured results, as shown in Fig.4.5. The little differences are mainly due to the fabrication errors. When we simulate the whole layout of the low pass filter by using the Momentum, a local port model is selected for comparison with the results based on the extracted circuit models. Because the port discontinuities exist, the S11 parameter of the simulation results of the whole layout does not agree with the measurement result.

It takes 2.6 seconds to do the simulation of the low pass filter by using the TRL extracted circuit models. With Momentum, it takes about 20 minutes to complete the simulation of the low pass filter on 21 sampling frequency points. Therefore, with the extracted circuit models, it is much easier to carry out the simulation and optimization of microstrip integrated circuits.

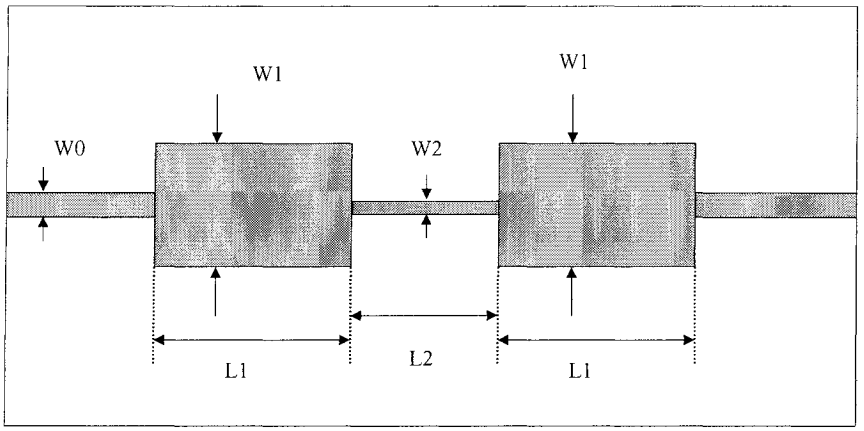


Fig.4.3. Layout of the microstrip low pass filter. ($\varepsilon_r = 2.2$, h = 0.254mm, W0=30mil, W1=60mil, W2=10mil, L1=160mil, L2=170mil)

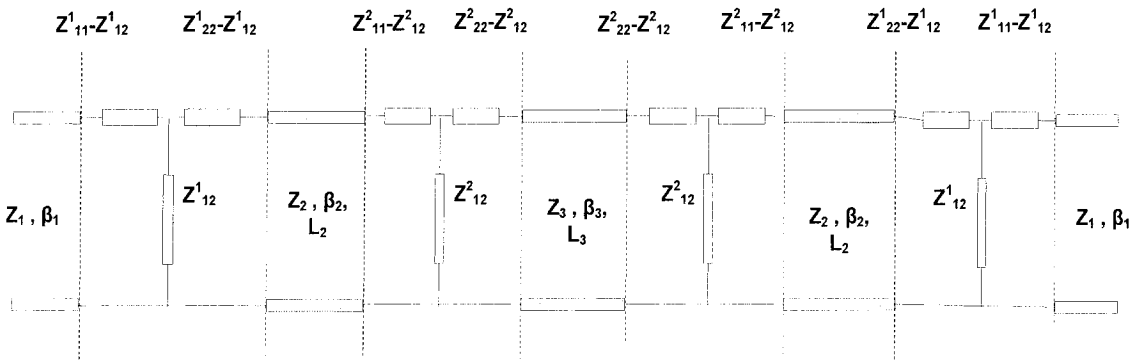
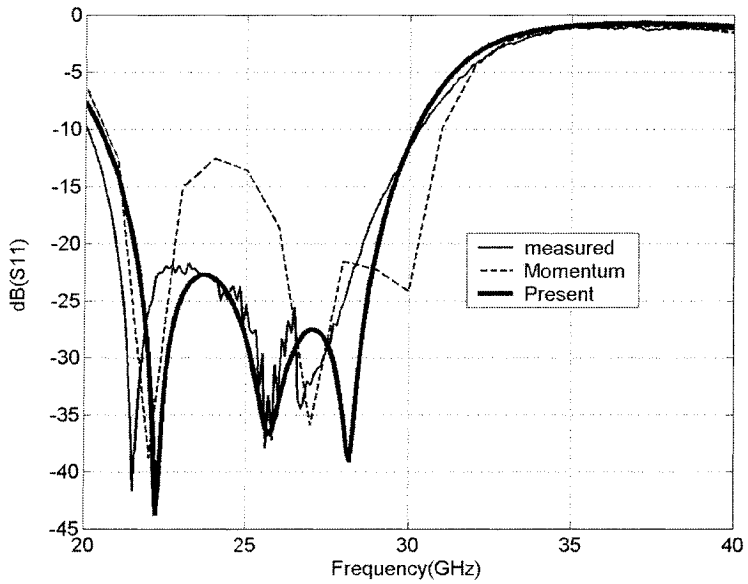
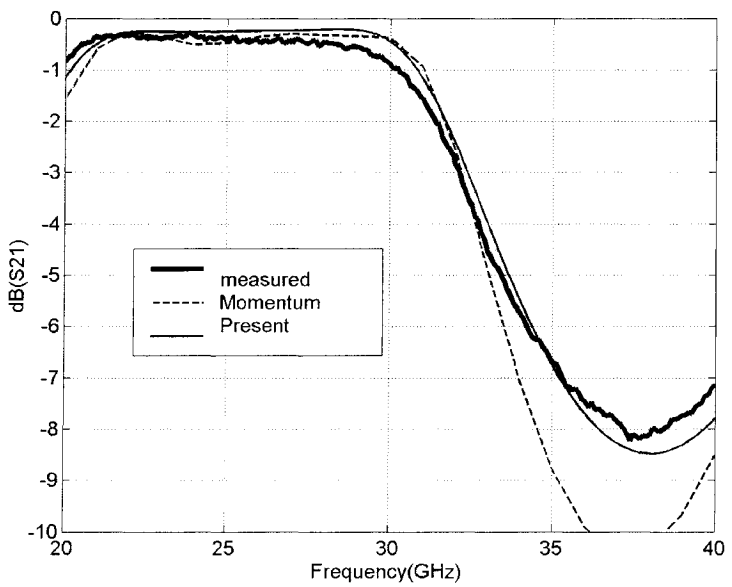


Fig.4.4. Equivalent network of the microstrip low pass filter.



(a)



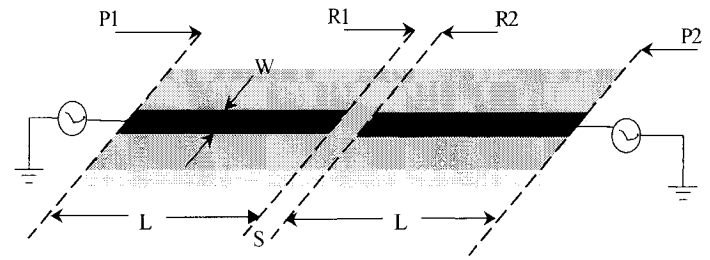
(b)

Fig.4.5. Comparison of the frequency responses of the low pass filter obtained from simulation based on the extracted circuit model, Momentum, and measurements.

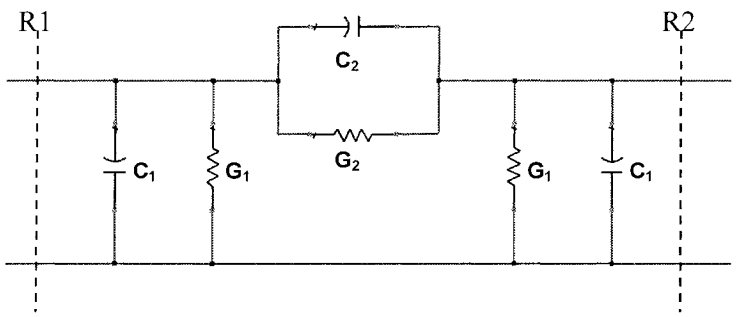
4.3 Circuit model of microstrip gap and resonator design

4.3.1 Extraction of the circuit model of microstrip gap

The circuit models of microstrip steps have been extracted and validated by the design of a simple low pass filter. In the following, we will extract the circuit models of microstrip gaps. The same substrate, software and frequency range as shown in 4.2.1 are used again here. The microstrip gap under modeling is shown in Fig.4.6(a). The width of the gap varies between 1 mil and 20 mil. The equivalent full-wave circuit model of the microstrip gap can be expressed by two capacitive shunt admittance, one capacitive shunt admittance and the radiation related resistor and conductance[19], as shown in Fig.4.6 (b). Because the gap is physically symmetrical, the circuit model of the microstrip gap is symmetrical. The extracted parameters of the circuit model for the microstrip gap by using TRL calibration are shown in Fig.4.7. We can see that as frequency increases, the radiation related G1 and G2 become large, C1 almost remains constant while C2 decreases a little bit. When the gap width increases, C1 and G1 increase while C2 and G2 decrease, which indicates the diminishing tendency of the coupling effect of the gap.



(a)



(b)

Fig.4.6. (a), (b) Geometry and equivalent circuit model of a microstrip gap.

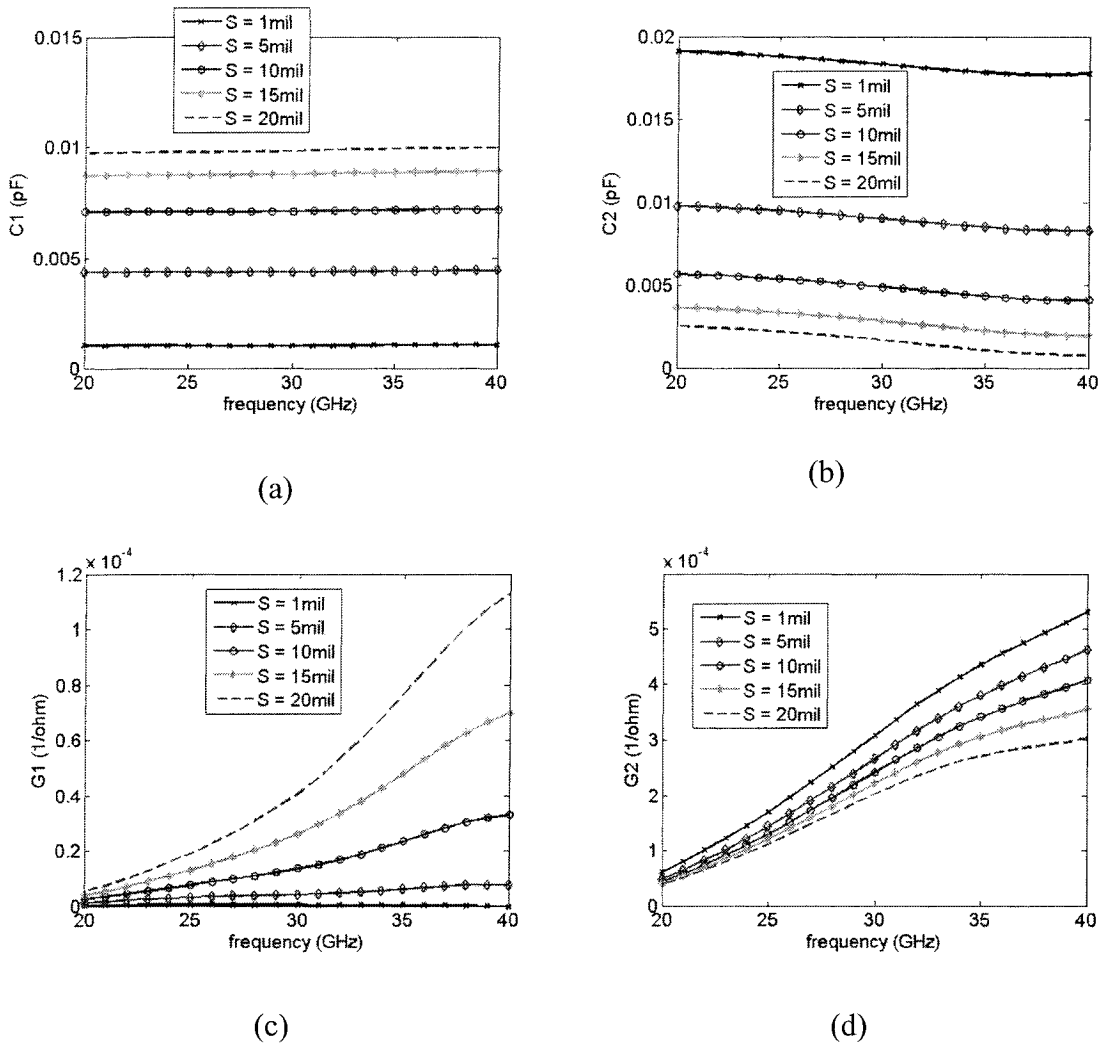


Fig.4.7. Extracted parameters of the circuit model of a microstrip gap ($\varepsilon_r = 2.2$, h = 0.254mm, W=0.762mm).

4.3.2 MICROSTRIP RESONATOR

By using the extracted equivalent circuit models of microstrip gap, a microstrip resonator using microstrip gaps is designed as shown in Fig.4.8. The equivalent network consists of cascaded microstrip lines and microstrip gaps, as shown in Fig.4.9. The simulated and measured magnitude-frequency responses of this resonator are shown in Fig.4.10. The simulated results based on the extracted circuit models agree well with those of the whole circuit simulated by Momentum. It should be noted that effects of the port discontinuities involved in Momentum simulation is not significant as in the low pass filter simulation as shown in 4.2.2. The reason is that the reflection coefficient of the resonator is not small here. Therefore, the effect of the port discontinuities is relatively weak. Measured center frequency of this resonator is lower than expected in simulation. The difference can be attributed to the fabrication errors.

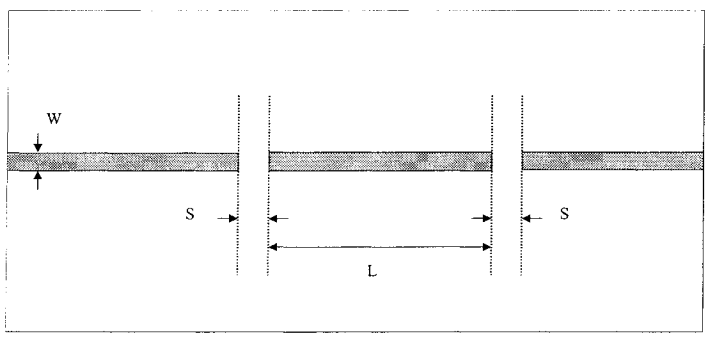


Fig.4.8. Layout of the microstrip resonator. (ε_r = 2.2, h = 0.254mm, W=30mil, S=5mil, L=160 mil)

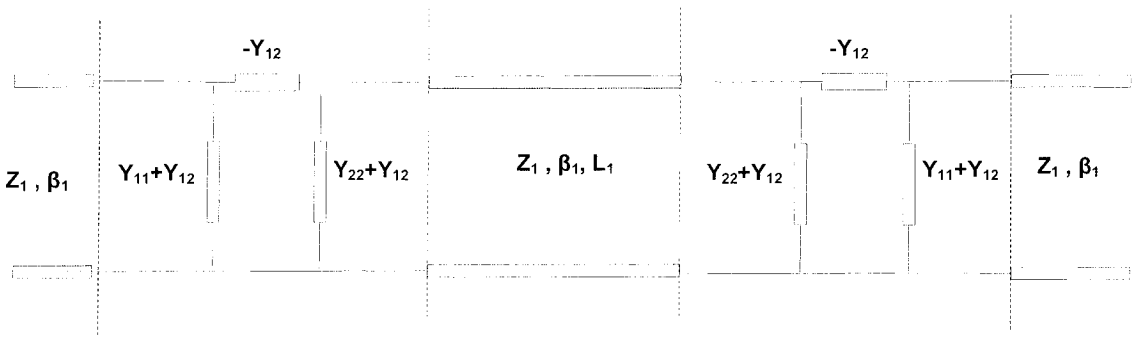


Fig.4.9. Equivalent circuit network of the microstrip resonator.

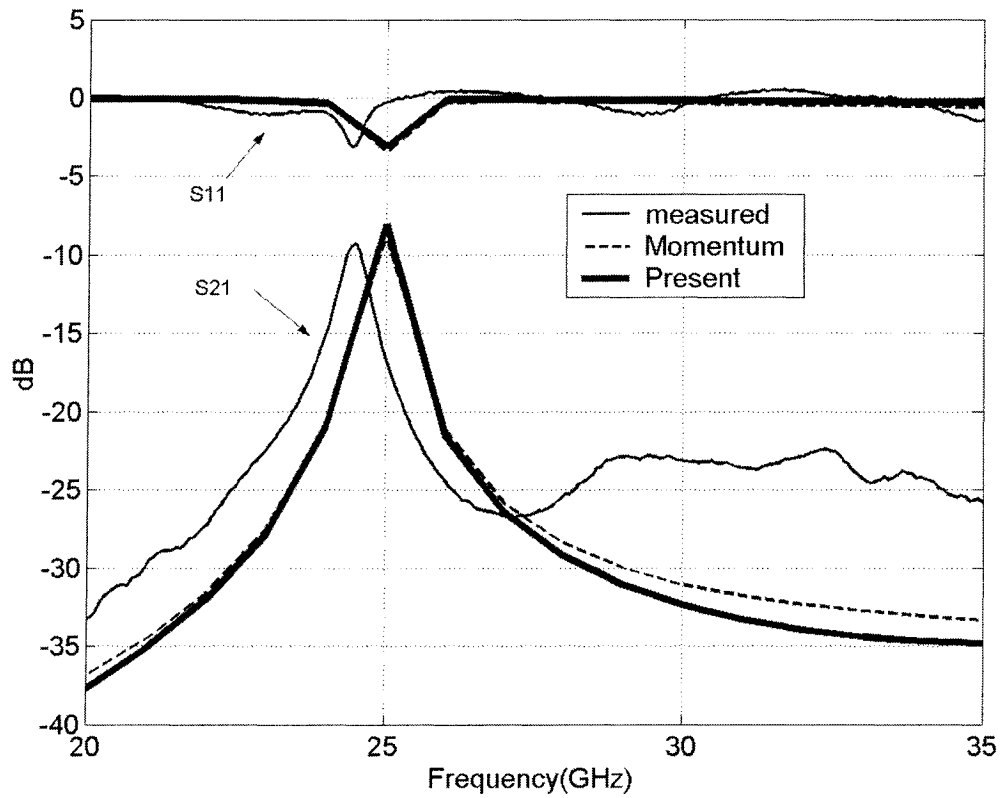


Fig.4.10. Frequency responses of the microstrip resonator obtained from simulation and measurement.

4.4 Summary

With the proposed numerical calibration techniques combined with commercial MOM packages, we have successfully extracted the full-wave circuit models of microstrip gaps and microstrip steps on the basis of substrate Duroid 5880 from 20GHz to 40 GHz. The circuit model of microstrip gap can be considered as two capacitive shunt admittances, one capacitive shunt admittance, and the radiation related resistor and conductances while the circuit model of the microstrip step can be expressed in terms of one capacitive shunt admittance, two series inductive impedances and the radiation related resistors and conductance. It has been shown that values of such circuit elements in the model of these microstrip discontinuities change as a function of the physical size of the discontinuities. Generally, the capacitance and inductance change little as frequency changes, but the radiation related resistor or conductance increases significantly with frequency.

Based on the extracted full-wave circuit models of the microstrip gap and microstrip step, a low-pass-filter and a resonator have been designed and fabricated. Measured results of the circuits have validated the extracted circuit models. Using the numerical calibration technique combined with commercial MOM packages, we can easily extract the circuit models of planar discontinuities. It is no doubt that the extracted full-wave circuit model provides an efficient and accurate way for microwave planar circuit design and optimization.

CHAPTER 5

SLOW-WAVE LINE FILTER DESIGN

5.1 Introduction

Interdigital capacitors (IDCs) have been widely used as a quasi-lumped capacitor in microwave circuits [29][42]–[45]. Various two-dimensional (2D) static equivalent circuit models were derived for its computer-aided design (CAD) model in earlier days. But such models may not be reliable since they ignore the fringing field effects of multiple finger ends [42], [43] or they roughly account for a partial amount of these effects such as the end capacitance [44]. Very recently, a lumped full-wave models [29] [45] has been proposed for the CAD purpose. The models were derived in a three-dimensional (3D) method of moments (MoM) algorithm. The models proposed in [29] [45] are accurate but it is based on microstrip circuits. Coplanar waveguide (CPW) is widely used in the design of uniplanar microwave integrated circuits because of its attractive features such as easy connection of shunt and series devices, low-frequency dispersion and less substrate dependence. As we know, IDC in CPW is rarely studied up to now. In this work, IDC in the form of CPW will be studied by using the proposed numerical calibration techniques, and the extracted circuit model of IDC in CPW will be implemented in a slow-wave line filter design.

5.2 Circuit model of Interdigital capacitor

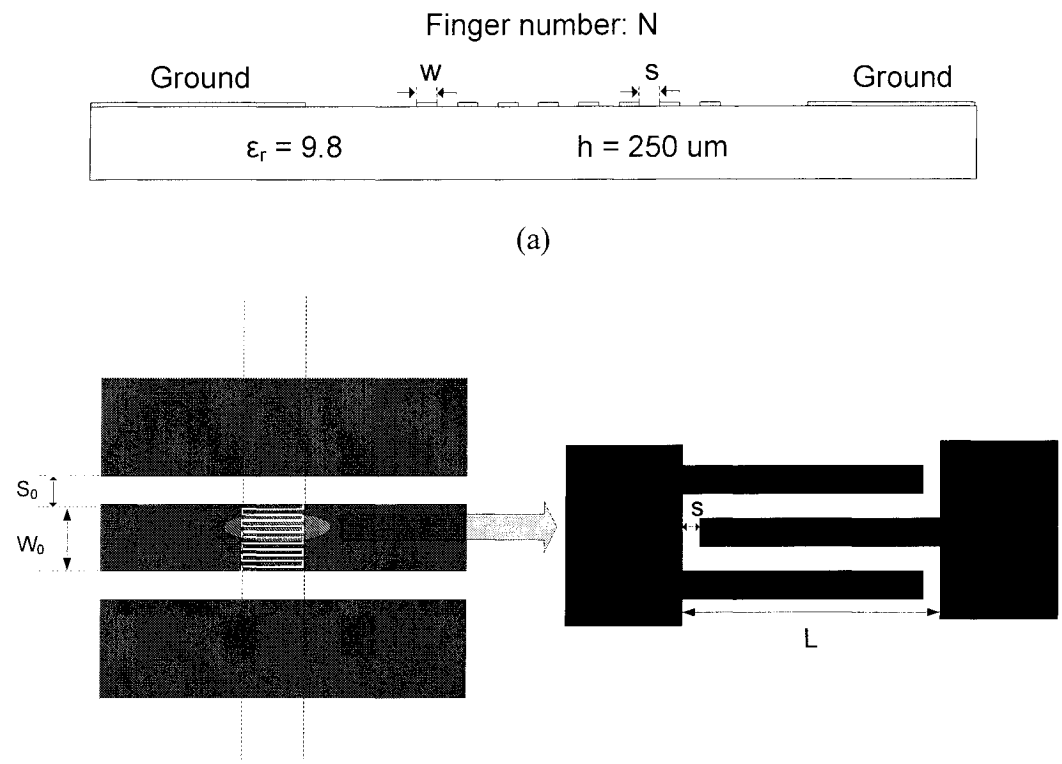


Fig.5.1. Physical layout of IDC in CPW. (a) Cross section of IDC. (b) Top view of IDC.

The physical structure of one IDC in CPW is shown in Fig.5.1. The IDC is placed in CPW without ground at the backside of the substrate. In Fig.5.1, the physical dimension is described as follows: N =12, w=s=10um, S_0=100um, W_0=230 um and the thickness of the metal is chosen to be 2um. The circuit model of IDC is presented by two shunt capacitors C_p, one series capacitor C_s and the radiation loss and ohmic loss related conductances: G_p and G_s, as shown in Fig.5.2. Because the IDC is symmetrical, the equivalent circuit model is also symmetrical. Note that this model of IDC is frequency

dependant at high frequency. The frequency independent circuit model can be realized by a more complicated circuit model including inductors.

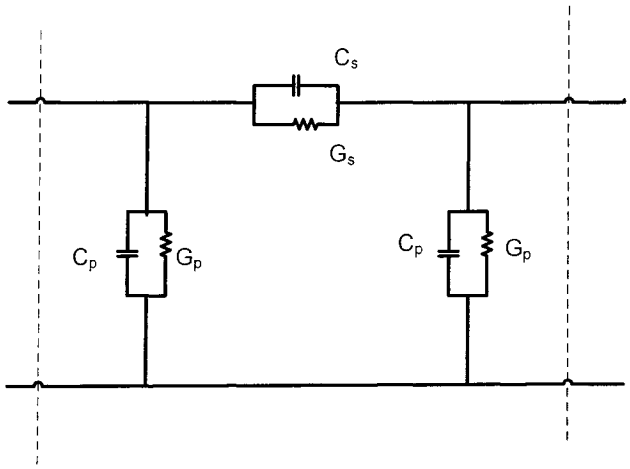
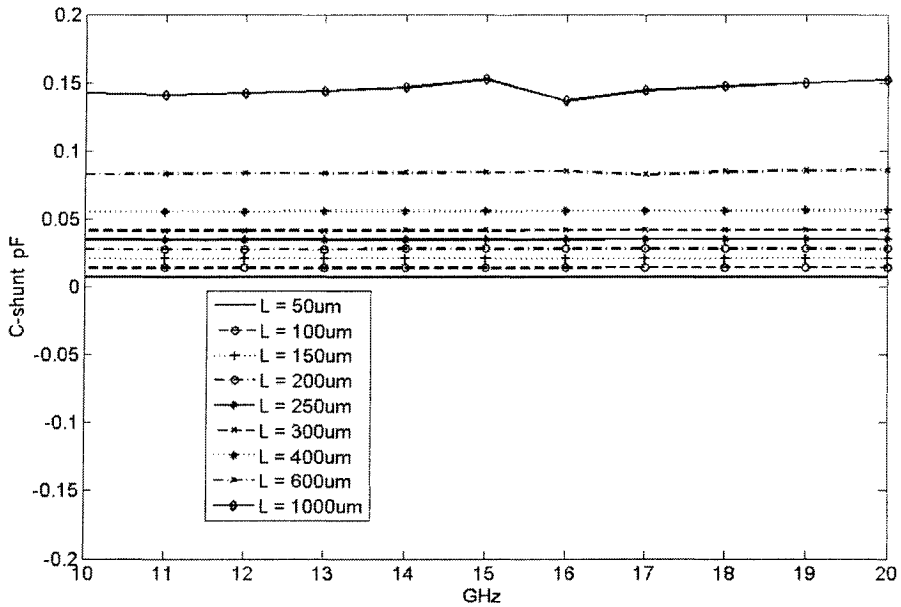
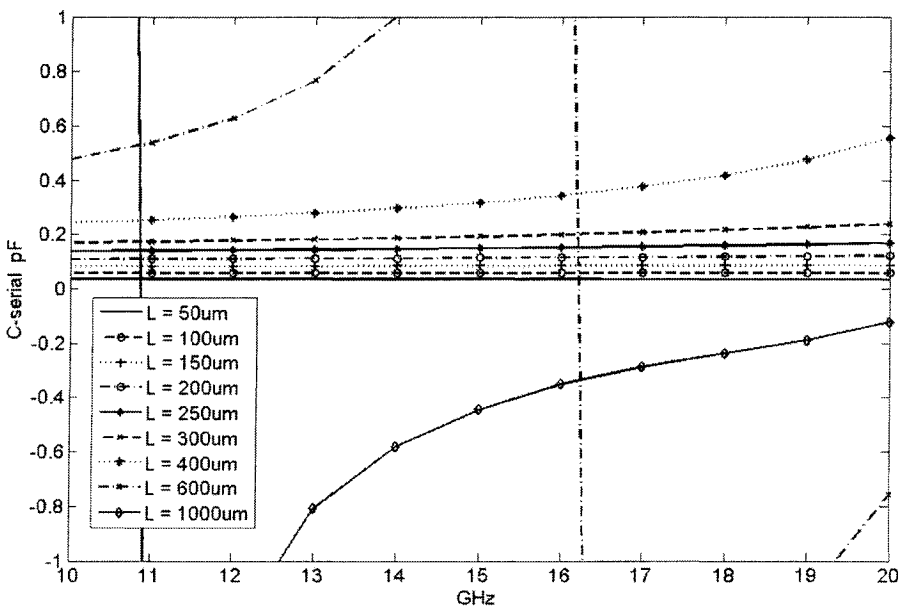


Fig.5.2. Equivalent full-wave circuit model of IDC.

By using the numerical TRL calibration technique, we can extract the full-wave equivalent circuit model of the IDC. The calibration configuration and procedure are the same as described in the previous chapters. The frequency range is chosen from 10GHz to 20GHz. The lengths of the IDC L vary from 50 um to 1000 um, and the other dimensions remain unchanged. The extracted circuit models corresponding to different L are shown in Fig.5.3. When frequency is fixed at 17GHz, the values of capacitors and conductances versus length L are shown in Fig.5.4. When L is less than 300um, the equivalent capacitors C_p, C_s and the conductances G_p, G_s increase almost linearly as the length L increases. When L is greater than 400 um, the values of capacitors and conductances change significantly as frequency changes and the IDC does not act as a lumped capacitor anymore. That is because the size of the IDC is not much smaller than one quarter wavelength; the IDC cannot be treated no longer as a lumped capacitor.

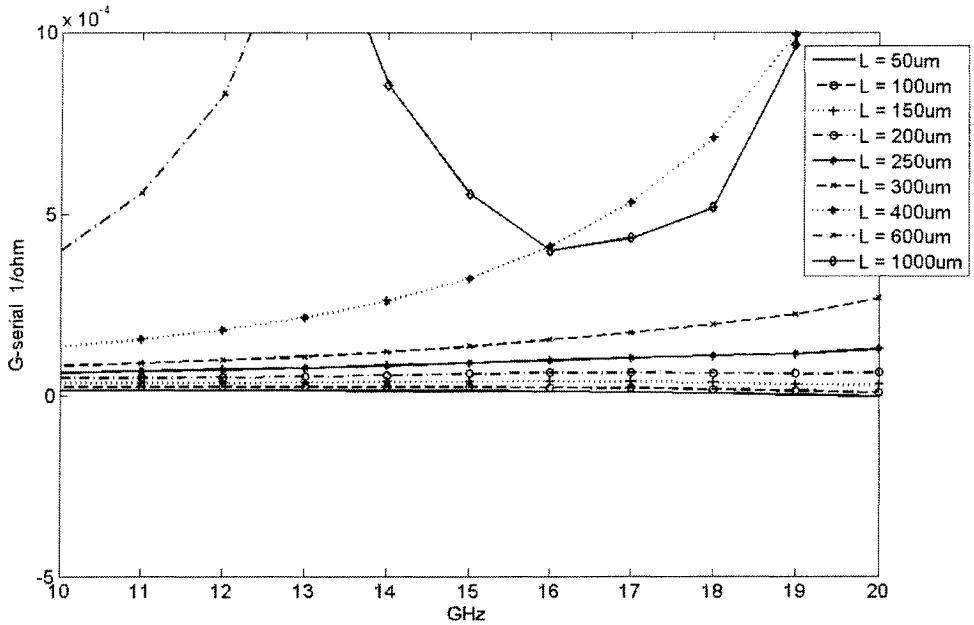


(a)



(b)

Fig.5.3. Values of the extracted circuit model versus frequency for different length L of the IDC. (a) Shunt capacitor C_p . (b) Series capacitor C_s. (c) Shunt conductance G_p. (d) Series conductance G_s,



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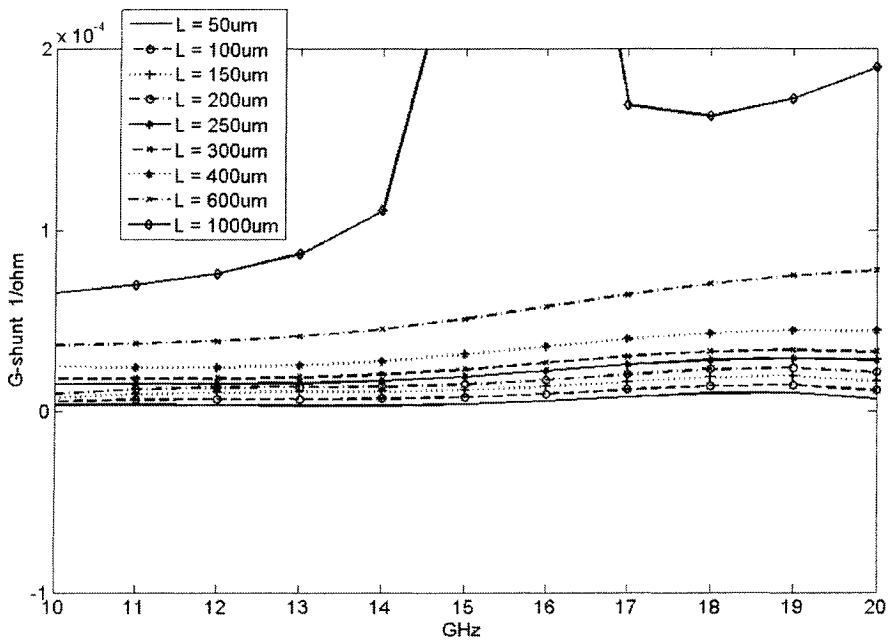
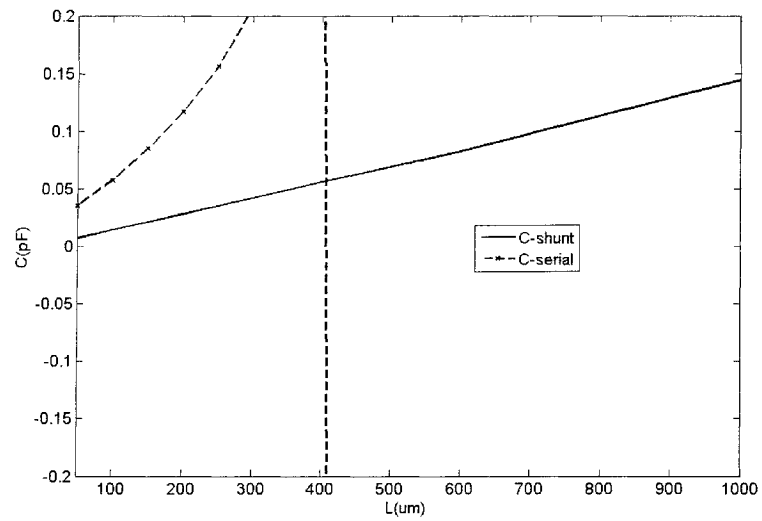
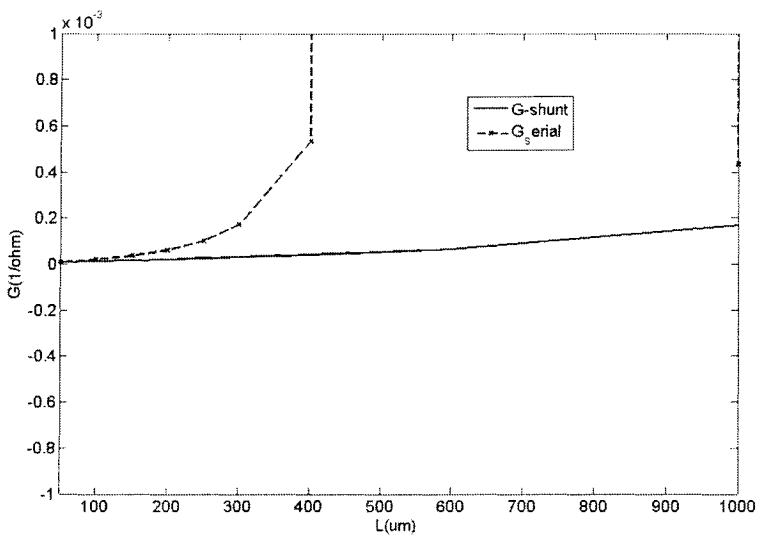


(d)

Fig.5.3. Continued



(a)



(b)

Fig.5.4. Values of the extracted circuit model versus length L of the IDC, f=17GHz. (a) Capacitors C_p and C_s. (b) Conductances G_p and G_s,

5.3 CPW slow-wave line with loaded IDCs

The full-wave circuit models of the IDCs were extracted by using the numerical calibration technique. By loading such IDCs on to the CPW transmission line, we can realize a slow-wave line [46].

In the beginning, we will describe the slow wave line theory briefly. A section of bald CPW transmission line and its equivalent lumped circuit model are shown in Fig.5.5. If we assume that the transmission line is lossless, the characteristic impedance and the phase velocity in the bald transmission line can be expressed by according to the lumped element circuit theory:

$$v = \frac{1}{\sqrt{L_0 C_0}}, \tag{5.1}$$

$$Z_0 = \sqrt{\frac{L_0}{C_0}}. \tag{5.2}$$

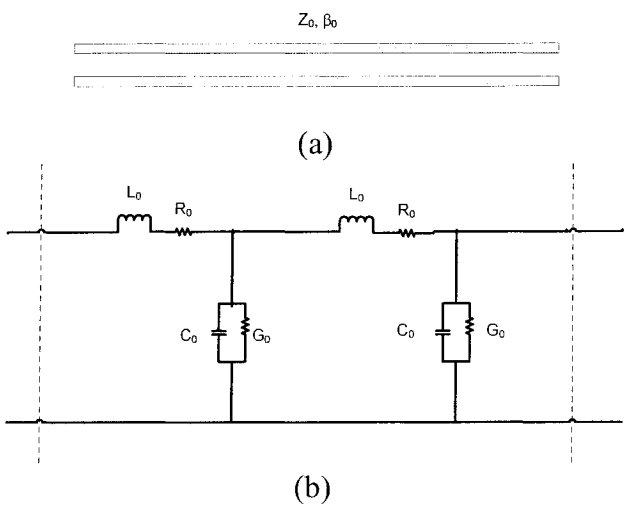


Fig.5.5. (a) Bald transmission line. (b) Equivalent circuit model of the bald transmission line.

From equation (5.1) we can see that the phase velocity v is dependent on both inductance L_0 per unit length and capacitance per unit length C_0. Changing both L_0 and C_0 can change the phase velocity. But in a conventional distributed TEM transmission line, L_0 and C_0 are related to each other. For example, for a given substrate, the change in physical dimension of a microstrip line will cause a large difference in characteristic impedance but little difference in phase velocity. That is because it is hardly to change the phase velocity by changing L_0 or C_0 without affecting each other. Therefore, it is difficult to change the phase velocity in a conventional distributed TEM transmission line. To overcome this, we can load the bald transmission line periodically with capacitor or inductance. It means that we only change the value of L_0 or C_0 without affecting the other. If we load the bald line periodically with parallel capacitance per unit length C_1, we have

$$C_0' = C_0 + C_1, \tag{5.3}$$

$$Z_0' = \sqrt{\frac{L_0}{C_0'}}, \tag{5.4}$$

$$v' = \frac{1}{\sqrt{L_0 C_0'}}. \tag{5.5}$$

The capacitance loaded transmission line behaves as another new transmission line with different characteristic impedance and phase velocity, as shown in Fig.5.6. Note that capacitance loaded transmission line behaves as an electrically smooth line only when the size of finger of the loaded capacitor is much small compared with wavelength.

The phase velocity of the loaded transmission line decreases due to the loaded capacitance C_1.

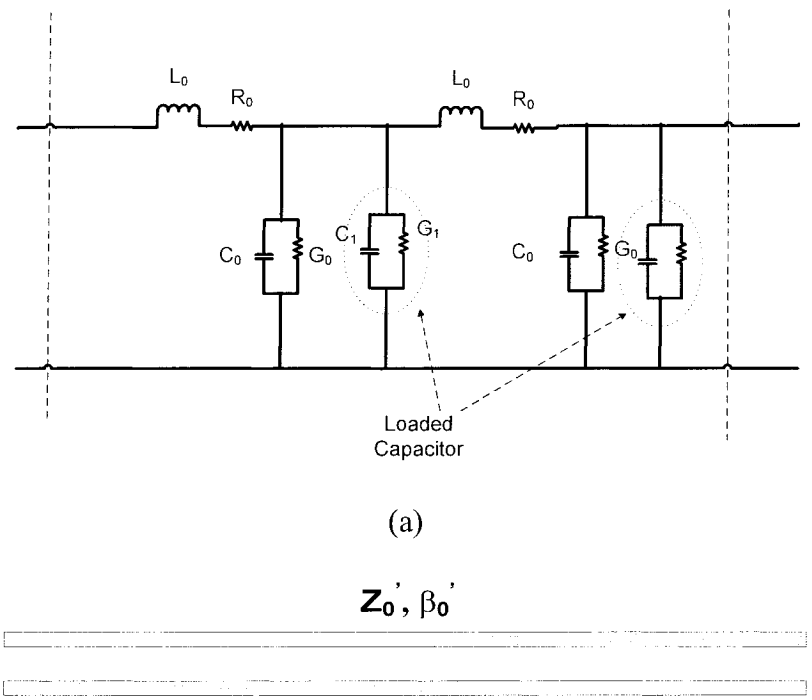


Fig.5.6. Capacitance loaded transmission line. (a) Equivalent lumped circuit model of the loaded transmission line. (b) New equivalent transmission line.

Therefore, by loading the parallel IDC to the CPW transmission line, we can develop a slow-wave line, as shown in Fig.5.7.

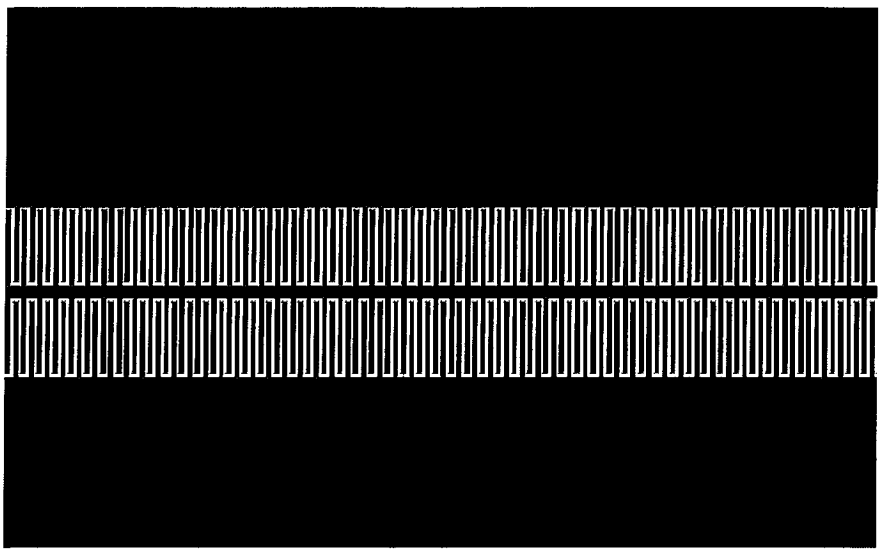


Fig.5.7. Structure of a slow-wave line realized by CPW transmission line loaded by parallel IDCs.

For the IDC shown in Fig.5.1, the value of the parallel capacitance per unit length C_1 can be obtained from the following equation (note that there are two IDCs loaded at both sides of the CPW line.):

$$C_1 = \frac{2*(C_S + C_P)}{W_1}, \tag{5.6}$$

where W_1 is the width of the IDC. For the IDC shown in Fig.5.1, N=12, W_1=12*(w+s) =240um. Actually, as shown in Fig.5.8, two parts of capacitances contribute to the total capacitances in the extracted circuit model of the IDC as shown in Fig.5.1. One part is the capacitances of gap, as we studied in Chapter 4. The other part is the capacitances of coupled fingers. The capacitances of the gap are much smaller compared with the capacitances of the coupled fingers. For accuracy, only the capacitances of the coupled

fingers are considered in the slow-wave line. Therefore, in equation(5.6), the value of capacitances C_S and C_P should ignore the effects of the gap.

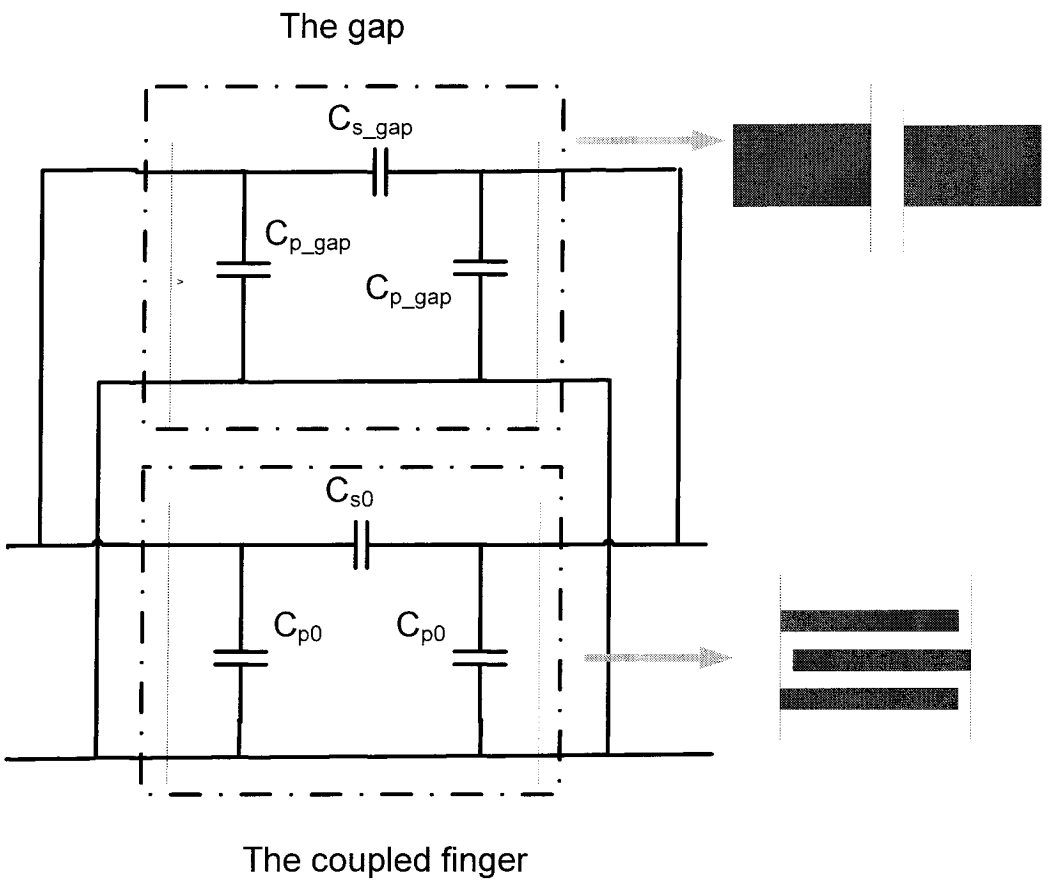


Fig.5.8. Capacitances in the extracted IDC circuit model involve two parts: the capacitances of gap and the capacitances of coupled finger.

Theoretically, the value of the parallel capacitance per unit length C_l of the loaded IDC should be calculated for an infinite long IDC. But for easier modeling, we can approximately calculate the value of C_l by an IDC with a finite length. The capacitances of the IDC with different finger number N are extracted by using the numerical TRL calibration technique, and results are shown in Fig.5.9 (f = 17GHz). From those results we can see that the capacitances per unit length C_{S0} and C_{P0} of the IDC change very little

when N is greater than 12. Therefore, the IDC with more than 12 fingers (the other physical dimensions are the same as ones in Fig.5.1.) can be approximately considered as an IDC with infinite width.

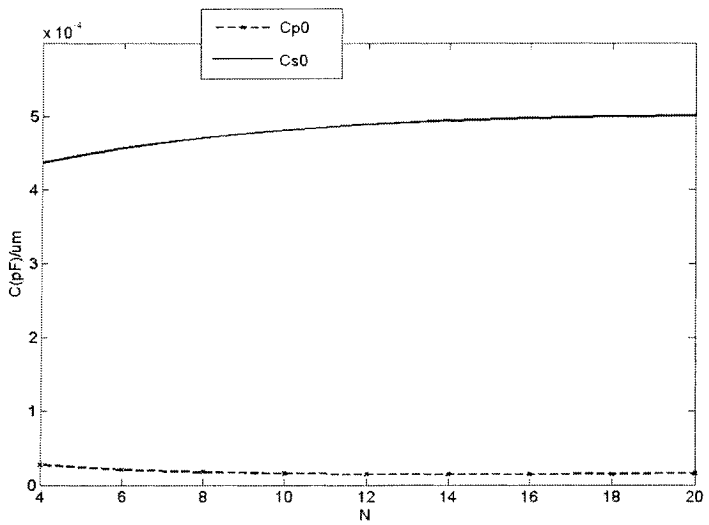


Fig.5.9. Extracted capacitances per unit length of the coupled fingers when a different number of fingers N is selected.

In the following example, we will calculate a slow-wave line as shown in Fig.5.7. The substrate, the size of the CPW line and the size of the finger of the loaded IDC are: ε_r=9.8, h=250um, w=s=10um, S_0=200um, W_0=30 um and the thickness of the metal is chosen to be 2um. In extraction of the capacitance of the IDC, we select N=12 and L=200um.

The equivalent circuit model of the CPW line as shown in Fig.5.5(b) can be extracted by applying a numerical TRL calibration to a very small section of the CPW line (the length is very small compared to the wavelength). At 17 GHz, the values of elements of the equivalent circuit model of the CPW line are expressed by C_0= 6.99e-11 (F/m), L_0=8.33e-07 (H/m), G_0= 4.14e-02 (1/ohm*m), R_0= 5.69e+02 (ohm/m). From equations

(5.1) and (5.2), we calculate the transmission parameters of the unloaded CPW line, which are Z_0= 109 (ohm), equivalent permittivity ε_{reff}=5.24 and loss factor α=42.3 (dB/m).

From Fig.5.3 and Fig.5.9, the extracted capacitance per unit length of the IDC is: C_1 =1.09e-9 (F/m), and the conductance is G_1= 6.02e-01 (1/ohm*m). Therefore, from equations (5.3)-(5.5), we can obtain the transmission parameters of the slow-wave line: Z_0= 26.8 (ohm), equivalent permittivity ε_{reff}=87.2 and loss factor α=167.1 (dB/m).

Calculated transmission parameters of the loaded CPW line compared with the unloaded CPW line are shown in Fig.5.10. In Fig.5.10, Z0, ereff0 and alpha0 are characteristic impedance (ohm), equivalent permittivity and loss factor (dB/meter) of the unloaded CPW line, respectively; Z1, ereff1 and alpha1 are characteristic impedance, equivalent permittivity and loss factor of the loaded CPW line, respectively. We can see that the characteristic impedance of the capacitance loaded CPW line is much smaller than that of the unloaded CPW line and the equivalent permittivity of the loaded CPW line is much bigger than that of the unloaded CPW line. The wavelength in this slow-wave line is shorter than the wavelength in the unloaded CPW line by 4 times. That is because that the loaded capacitance C_1 is much bigger than C_0. Therefore, by using the slow-wave line to design the circuit, the compact size can be reached. The loss factor per meter of the loaded CPW line seems very large. It is 4 times larger than that of the unloaded CPW line. Since the wavelength in the loaded CPW line is also 4 times shorter than that of the bald CPW line, the loss factor per wavelength in the loaded CPW line is in fact comparable to that of the bald line.

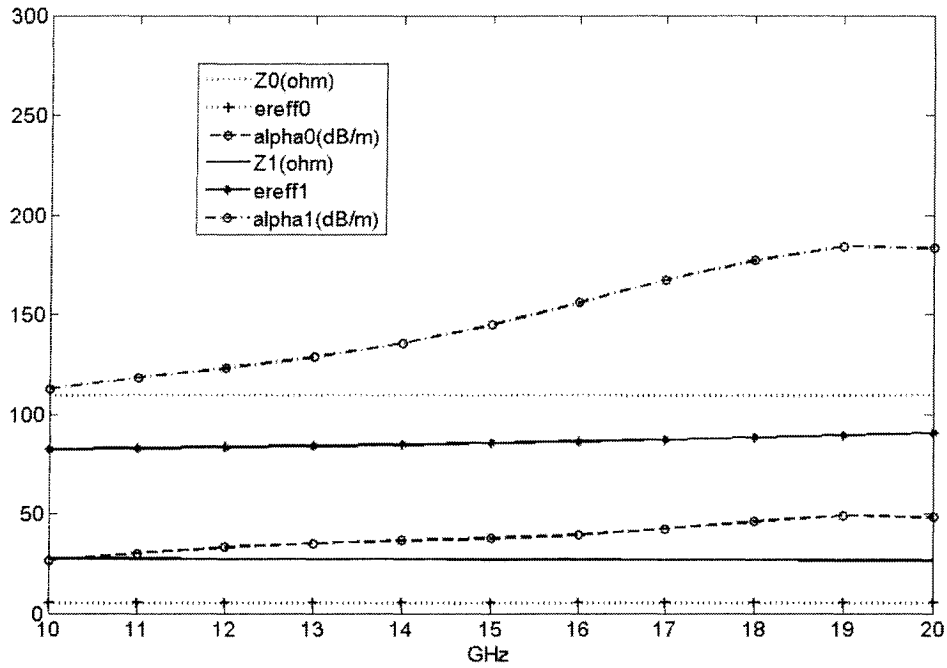


Fig.5.10. Transmission parameters calculated for both the loaded CPW line and the unloaded CPW line.

If we load the bald CPW line described above with different value of capacitances, different transmission parameters of slow-wave line can be got, as shown in Fig.5.11. The bigger the loaded capacitance per unit length, the lower characteristic impedance and the bigger equivalent permittivity can be got.

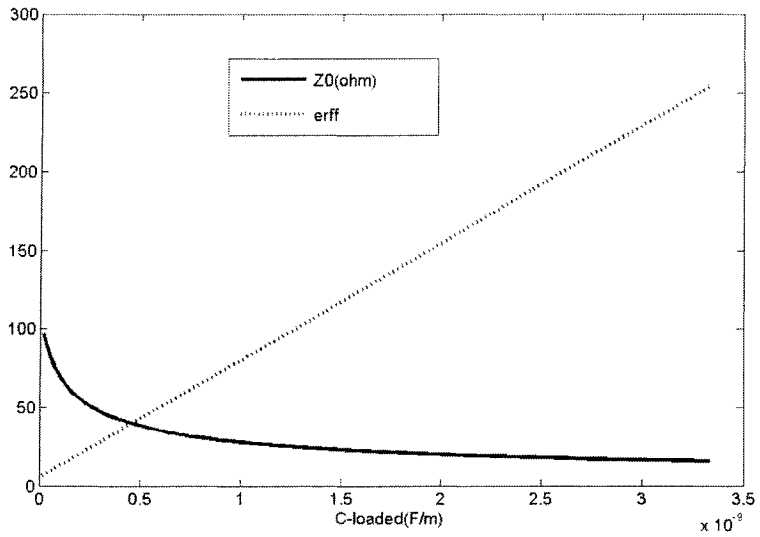


Fig.5.11. The transmission parameters of the slow-wave line loaded with different value of capacitance to the same bald CPW line.

5.4 Band pass filter using slow-wave lines

We can now design filters by using the slow-wave line and the IDCs described above. In the design process, the slow-wave line can replace the transmission line in a traditional filter. Because the wavelength in the slow-wave line is much smaller than in the bold transmission line, the filter using a slow-wave line will be more compact. In this work, we will design a band pass filter (BPF). The BPF is realized by series cascaded half wave length resonators and coupling capacitors, as shown in Fig.5.12. In our design, the resonators will use slow-wave line resonators, and the coupling capacitors will use IDCs.

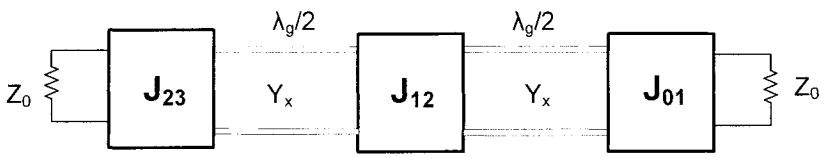


Fig.5.12. Equivalent network of the 2-pole BPF.

The performance of the filter:

N=2 Chebyshev type.

Center frequency f0 = 17.5 GHz.

The passband from 16.5 to 18.5 GHz.

Ripple 0.5 dB.

The design procedure is similar to the traditional filter design technique:

1. Calculate the low-pass prototype values: g0, g1, g2, g3.

2. The value of the converters can be obtained from:

$$J_{01} = \sqrt{\frac{G_A w B_1}{g_0 g_1}},$$

$$J_{12} = w\sqrt{\frac{B_1 B_2}{g_1 g_2}}, \qquad (5.7)$$

$$J_{23} = \sqrt{\frac{G_B w B_2}{g_2 g_3}},$$

in which w is the relative bandwidth, Ga and GB are the conductances of the loads. And

$B_i = \frac{\pi}{2} Y_x$ (Yx is the characteristic impedance of the resonator line).

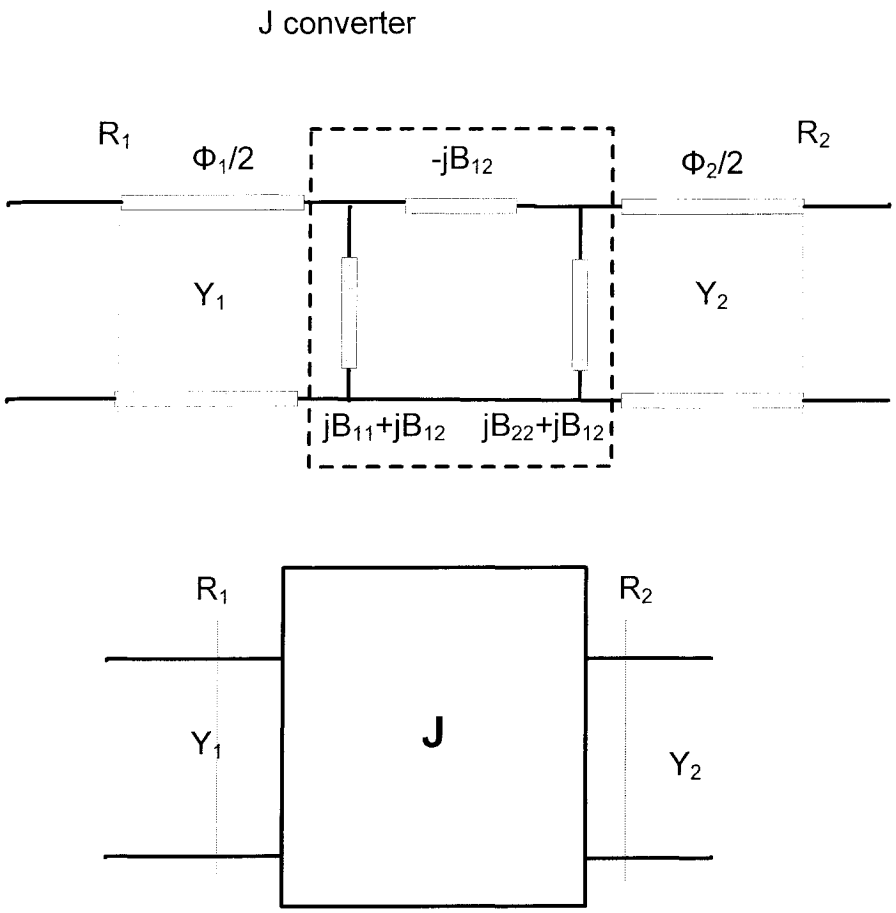


Fig.5.13. J-converter network.

The converter, as shown in Fig.5.13, is realized by the IDCs as studied in section 5.2 and can be calculated from the following equations [29]

$$\frac{J}{\sqrt{Y_1 Y_2}} = \frac{\sin(\phi_1/2) + \bar{B}_{11}\cos(\phi_1/2)}{\bar{B}_{12}\sin(\phi_2/2)}, \tag{5.8}$$

$$\phi_1 = -\tan\left[\frac{2(\bar{B}_{11} + \bar{B}_{22}|\bar{B}|)}{1+\bar{B}_{22}^2 - \bar{B}_{11}^2 - |\bar{B}|^2}\right], \tag{5.9}$$

$$\phi_2 = -\tan\left[\frac{2(\bar{B}_{22} + \bar{B}_{11}|\bar{B}|)}{1+\bar{B}_{11}^2 - \bar{B}_{22}^2 - |\bar{B}|^2}\right], \tag{5.10}$$

where $\bar{B}_{11} = B_{11}/Y_1$, $\bar{B}_{22} = B_{22}/Y_2$, $\bar{B}_{12} = B_{12}/\sqrt{Y_1 Y_2}$ and $|\bar{B}|^2 = \bar{B}_{11}\bar{B}_{22} - \bar{B}_{12}^2$.

3. Determination of physical dimension. The circuit substrate and the slow-wave line are the same as those in section 5.3. The electrical length of the slow-wave resonator is one half wavelength minus ϕ_1 and ϕ_2, and the physical length calculated by using the equivalent permittivity in section 5.3 is 770um. The first and the last coupling IDCs are the same, and the dimension is: w=s = 10 um, N=12 and L=200um. The second IDC's dimension is: w=20um, s=10um, N=14 and L =100um. The layout of the BPF is shown in Fig.5.14. The length of the whole circuit is 2400 um.

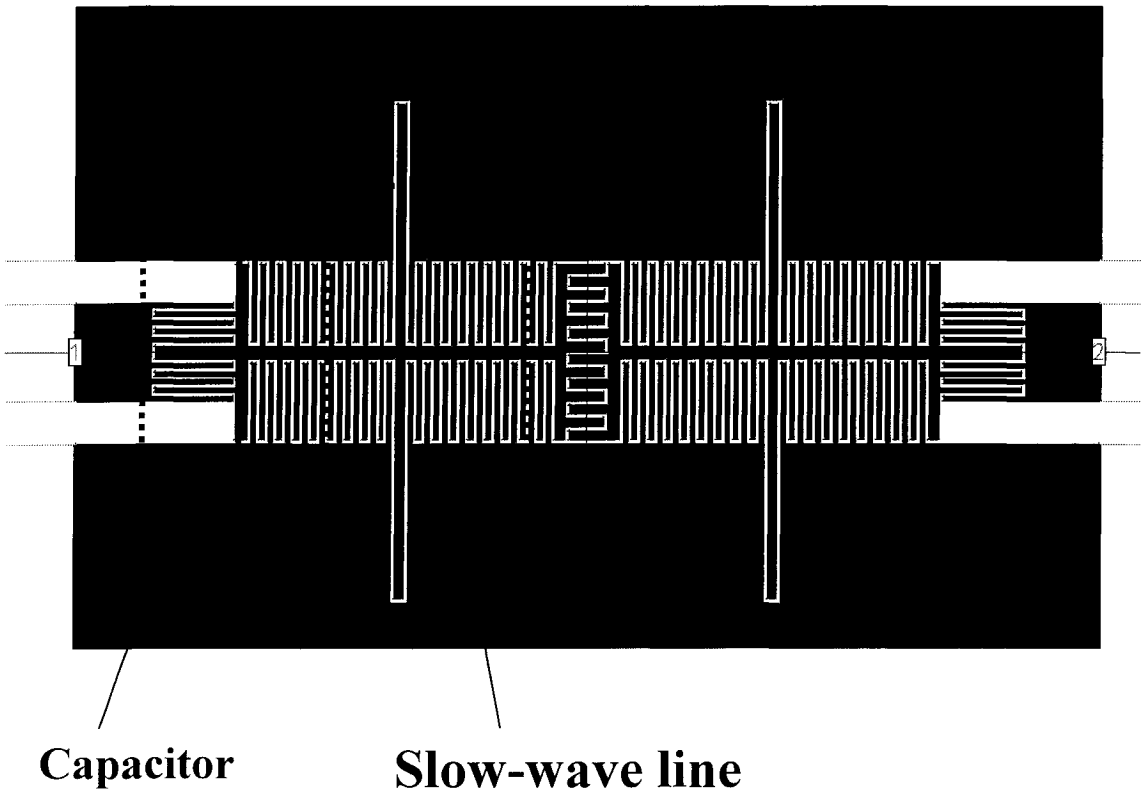


Fig.5.14. Structural layout of a 2-pole BPF using the slow-wave line resonator.

To simulate the BPF shown in Fig.5.14, two different ways are used. One is to use the full-wave EM simulation of the circuit. The other is to assemble all the extracted circuit models of elements in the BPF together, and the network built by these circuit models in ADS is shown in Fig.5.15. The filter is composed of lossy transmission lines and equivalent circuit models of the IDCs. Simulated results compared with measured results are shown in Fig.5.16. We can see that the simulated results of the slow-wave line BPF based on the circuit models are very close to the measured ones and the EM simulation results. The center frequency of the measured results agrees with that of the predicted results. The frequency bandwidth and the insertion loss from measurement are a little

smaller than the predicted one. From this BPF design, we can see that the extracted full-wave circuit models are effective for the circuit design in a schematic way. There is a little difference between the predicted results and measured ones as well as full-wave EM simulation results. That is because when we extract the equivalent circuit models, we assume that the circuit elements are isolated without mutual coupling. In real circuits, there is always coupling between neighbouring elements. Because the structure of the filter is complicated, the EM simulation consumes a lot of time and computer memory due to a large amount of meshes. Therefore, the design based on the extracted circuit models is the most efficient method in the design of this filter.

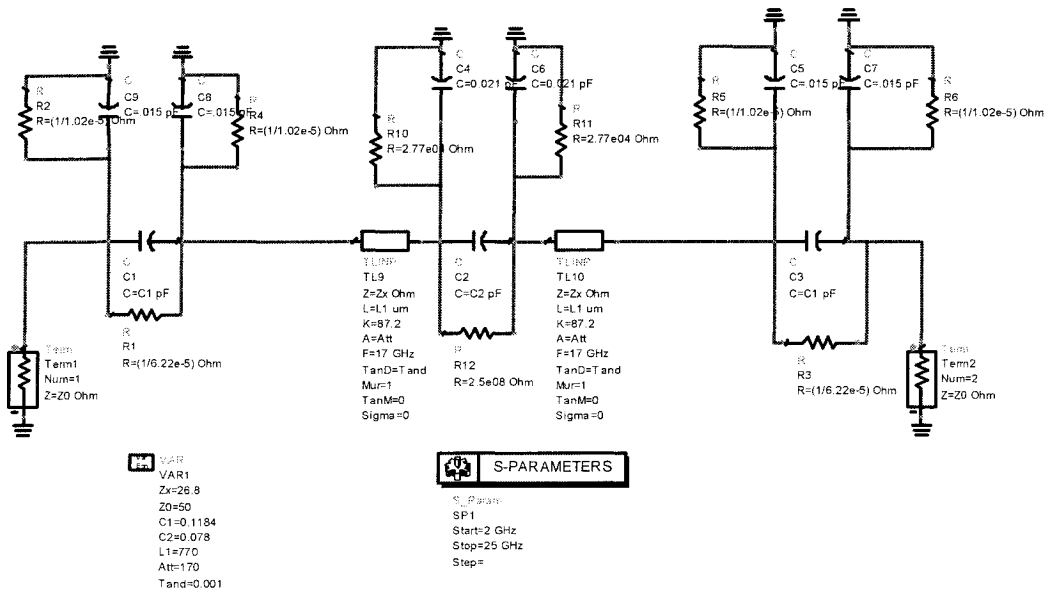


Fig.5.15. Equivalent network of the 2-pole BPF used in ADS schematic simulation.

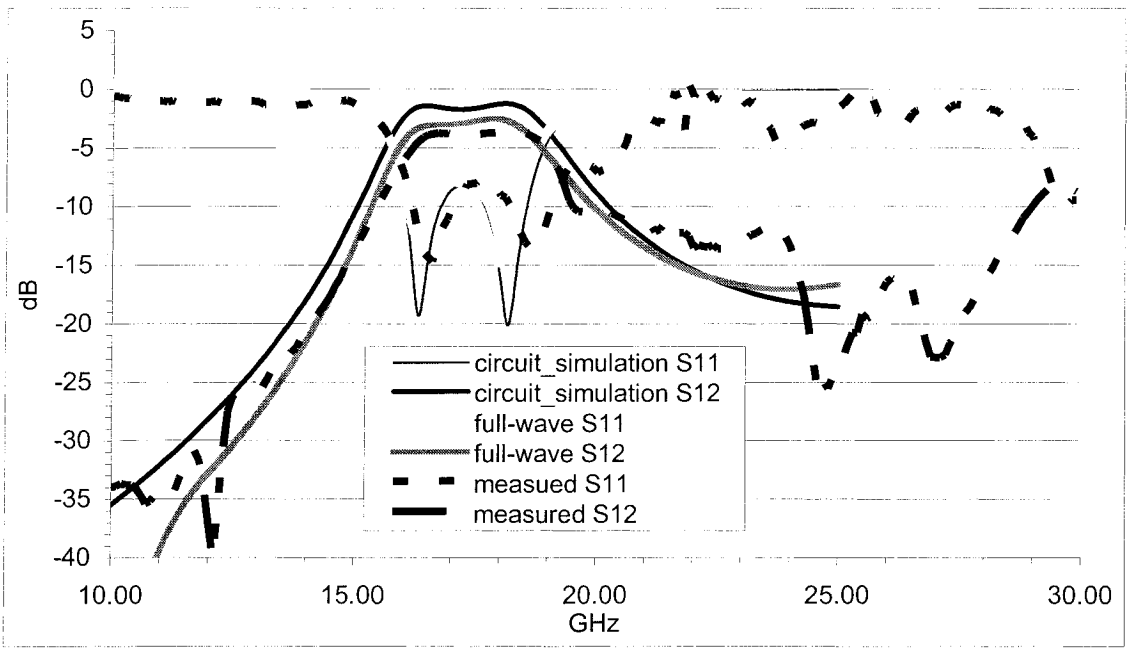


Fig.5.16. Measured results of the slow-wave line 2-pole BPF compared with the simulated results.

5.5 Summary

By using the developed numerical calibration technique, we have extracted the equivalent full-wave circuit models of the IDCs. When the size of the IDC is much smaller than one quarter wavelength, the IDC can be treated as a lumped element. The circuit model of the IDC can be represented by two shunt capacitors, one series capacitor and the radiation loss and metal loss related conductances. The series capacitor is the dominant component that represents the coupling capacitance. The coupling capacitance changes almost linearly with the length of the IDC.

By loading the IDC onto the CPW line, we can realize a slow wave line. Phase velocity of the slow wave line is greatly reduced due to the loaded capacitance, and the characteristic impedance of the slow wave line is also reduced. The circuit using the slow-wave line can be made very compact. By choosing different loaded IDCs, we can obtain different phase velocities and characteristic impedances of the slow wave line.

A 2-pole slow-wave line BPF has been designed by using the extracted equivalent circuit models of the IDCs. Measured results agree with the predicted ones. Once again, the extracted full-wave circuit models of IDCs from numerical calibration have been validated. To realize the performance optimization of the BPF, the best way is to build a library of the extracted full-wave circuit models of the IDCs, as in the commercial microwave design software.

CHAPTER 6

PLANAR QUASI-OPTICAL POWER COMBINER

6.1 Introduction

Recently, quasi-optical power combining technology has been developed rapidly [47][48][49]. Various three-dimensional quasi-optical architectures reported so far may be classified as either 'tray' or 'tile' approach[50]. The essential character of such quasi-optical power combiners is that all of the amplifier elements operate in parallel in one stage. In this case, the loss is roughly independent of the number of amplifier elements in connection with the stage. This is why the power combining efficiency of the quasi-optical architecture can be much better than the corporate binary Wilkinson power combiner if the number of amplifier elements is large. Nevertheless, quasi-optical techniques have also experienced problems including insufficient modeling results, difficult packaging issues, complicated mechanical assembling, and large physical size.

A majority of quasi-optical power combiners developed so far involve three-dimensional circuits that are not easy to handle with respect to both mechanical and electrical aspects. Different from the three-dimensional counterparts, two-dimensional planar quasi-optical power combiners have also been studied, most of which were based on lens concepts [51][52]. In particular, an interesting planar quasi-optical power combining structure was proposed and demonstrated in [53], where a multimode interference was used to realize the power combining function. However, those

structures still suffer from such problems as large physical size, narrow bandwidth and insufficient modeling.

We propose in this work a new simple scheme for designing power combining structure, which is a 'quasi-optical planar power combiner'. This structure presents merits of both binary circuit based power combiner and conventional quasi-optical power combiner. In this proposed structure, the power dividing/combining functions are simply realized by transition between an oversized microstrip line and a set of parallel multi-port microstrip lines. So the entire power combiner remains in the planar form, which can be fabricated with a simple planar circuit technology. No complicated mechanical assembling is needed, and the circuit volume can greatly be reduced. In addition, interconnects with other planar circuits are just straightforward. Another attractive property of this structure is that it can work over a wide frequency bandwidth because the non-resonant structure works with quasi-TEM mode.

6.2 Operating Principle

In the following, the presentation of the operating principle that is simple and straightforward will directly be related to our practical design without loss of generality. Fig.6.1 illustrates the geometry of a 1-to-4 novel power divider/combiner that is proposed for operation at 25-31GHz in our design. The substrate is Duroid 5870 with εr = 2.33 and thickness h = 10 mil. The input (left-hand side) is a standard 50 ohm microstrip line with its line width W0=0.74 mm. The output (right-hand side) presents four parallel standard 50 ohm microstrip lines, which are equally spaced, the space being

S=0.4 mm. The width of the oversized microstrip line is selected to be W1=4.4 mm, whose characteristic impedance is 12.5 ohm, and this value corresponds to 50 ohm divided by 4.

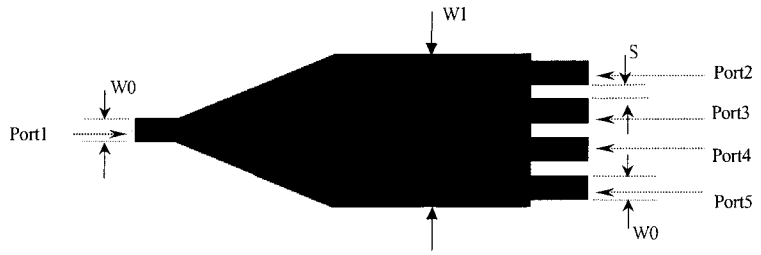


Fig.6.1. The proposed structure for realizing a 1-to-4 power divider/combiner in our case study

If we excite port 1 with an input signal, the signal will pass through the line taper to the oversized microstrip line. Then the signal is divided into four parts and get out onto four output ports 2, 3, 4 and 5. The surface current distribution at 31 GHz over the structure generated by Momentum of ADS is shown in Fig.6.2. Inversely, if the four ports 2, 3, 4, and 5 are equally (coherently) excited with four signals, they then add up at port 1 as Fig.6.3 (Fig.6.3 looks quite similar to Fig.6.2). Because the microstrip line works with quasi-TEM mode, so the current density profile over the metal surface is mainly flat in the transverse direction except for the two edges (current density at the two edges is higher than the other parts), as shown in Fig.6.4. So the power is almost equally divided into the four output ports.

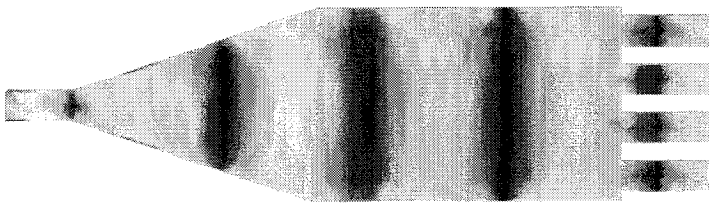


Fig.6.2. Surface current distribution at 31 GHz generated by Momentum when port 1 is excited.

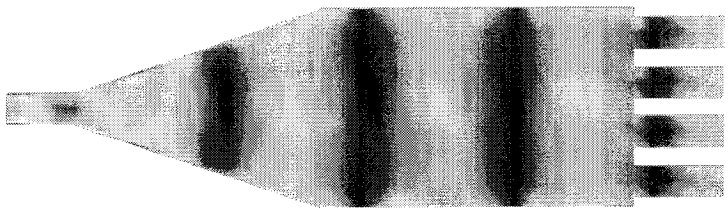


Fig.6.3. Surface current distribution at 31 GHz generated by Momentum when ports 2 to 5 are excited equally (coherently).

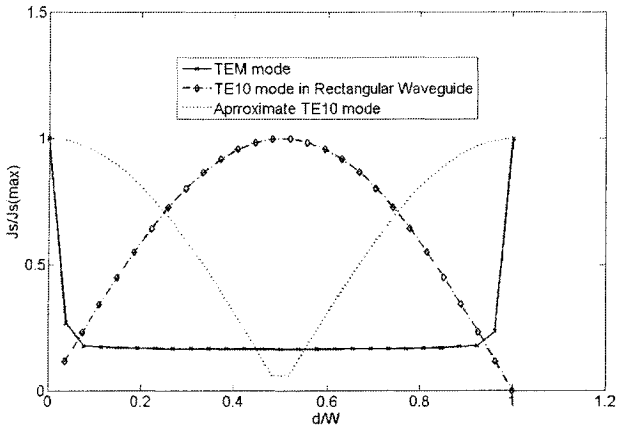


Fig.6.4. Current distribution density on surface of the oversized microstrip line.

This designed structure operates over the frequency range of 25–31 GHz. In the section of the oversized microstrip line, W1 = 4.4 mm and there are two principal modes, namely, quasi-TEM mode and a waveguide TE10 mode. The quasi-TEM mode is preferred in the design. Fig.6.5 describes electrical field distribution of the TE10 mode over the oversized microstrip line at 31 GHz, which is generated by HFSS. In addition, the approximate current distribution density of TE10 mode on surface of the oversized microstrip line is shown in Fig.6.4. It can be seen that this TE10 mode is just similar to its counterpart in rectangular waveguide. The difference lies in that the distribution profile of electrical field in the oversized microstrip line satisfies a cosine function and it reaches peak at both edges of the conductor and becomes null in the center. This TE10 mode in the oversized microstrip line should be avoided because it can cause an uneven power distribution at the four output ports, which will reduce the power combining efficiency. This suggests that we should carefully design the taper and the transition

from the oversized microstrip line to the multi parallel microstrip lines. In this case, the taper is used to realize the impedance matching and also reduce unwanted higher modes that may propagate in the oversized microstrip line. Therefore, the taper should be made as smoothly as possible. As far as the transition is concerned, the physical location of the output lines is critical in the design. First of all, the location must be made symmetrical, and it is very important to avoid exciting higher modes such as the TE10 mode. Secondly, the spacing of the multi parallel microstrip lines should be arranged as equally as possible. This is because the distribution of current in the transverse direction is approximately flat. The equally spaced multi microstrip lines will cause a minimum current distortion over the transition.

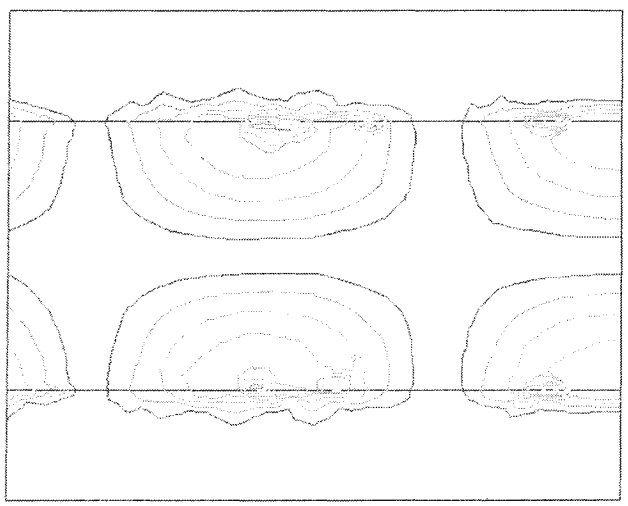


Fig.6.5. Electrical field distribution of the TE10 mode in the oversized microstrip line (generated by HFSS).

The maximum allowable number of the multi-parallel microstrip lines can be determined by the following equation.

$$Z_1 = Z_2 / 2N , \tag{6.1}$$

in which Z1 is the characteristic impedance of the oversized microstrip line; Z2 is the characteristic impedance of an output line in the multi parallel microstrip lines, and 2N denotes the number of the multi lines.

The coupling among the parallel multi-port microstrip lines is generally very weak because the quasi-TEM mode is used herewith for the output lines, we can thus neglect it. For simplicity, we just consider two coupled adjacent microstrip lines in the structure of Fig.6.1. The adjacent coupling is calculated to be –21.27 dB. In this case, the odd mode characteristic impedance is 46.38 ohm, and the even mode characteristic impedance is 55 ohm, which gives Z0= 50.5 ohm. If the power combiner is well designed on the basis of TEM mode properties, the signal at each output port has the equal magnitude and phase, and the multi-parallel microstrip lines work at even mode exciting. In this case, a single transmission line may be used to represent the whole multi-lines, which has Zeven as its characteristic impedance. Therefore, Zeven is approximately equal to Z0 and we can consider them as a single transmission line in case that the coupling is weak. If the parallel microstrip lines work at odd mode, however, performance of the power combiner will be degraded. Since the odd mode characteristic impedance of the coupled line will be different from that of the even mode, a mismatch between power amplifiers and multi-parallel lines will cause some reflection loss. In addition, the odd mode on the multi-parallel lines may yield

waveguide modes instead of quasi-TEM mode in the oversized microstrip line. Over the taper section, some part of energy of the waveguide modes will reflect back to the power amplifiers because the narrow end of the taper behaves as an impasse for the waveguide modes. The other part of energy of the waveguide will be converted to a TEM mode. Thus, the odd mode along the multi-parallel microstrip lines will reduce the power combining efficiency.

In our work, Momentum of ADS was used to simulate the structure in Fig.6.1, and the simulation results are shown in Fig.6.6. From Fig.6.6, we can see that the signals distributed into port 2 and port 3 exhibit little difference in both magnitude and phase. Since the structure is symmetrical, S14 = S13 and S15 =S12. The difference in amplitude between S14 and S15 is about 0.4dB. It means that the signal input to port 1 is almost equally divided into the four output ports and the amplitude of the signal at each output port is almost a quarter of the input signal at port 1.

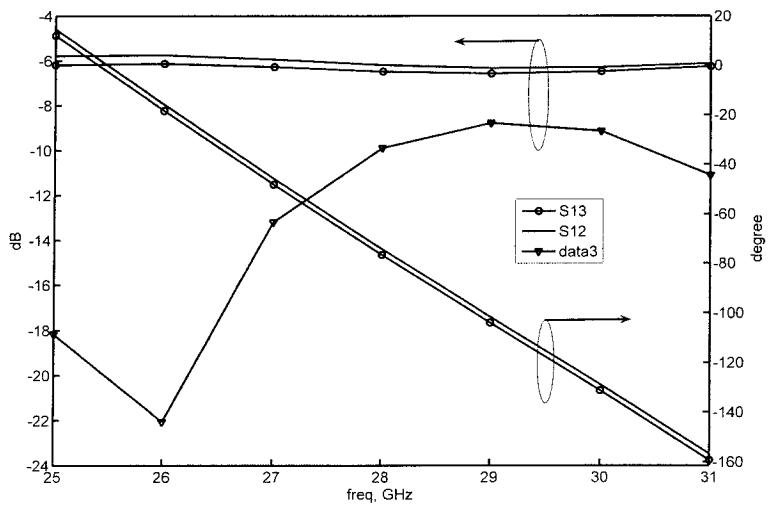
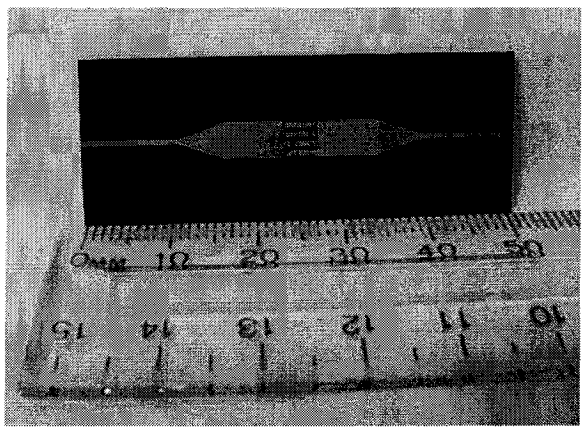
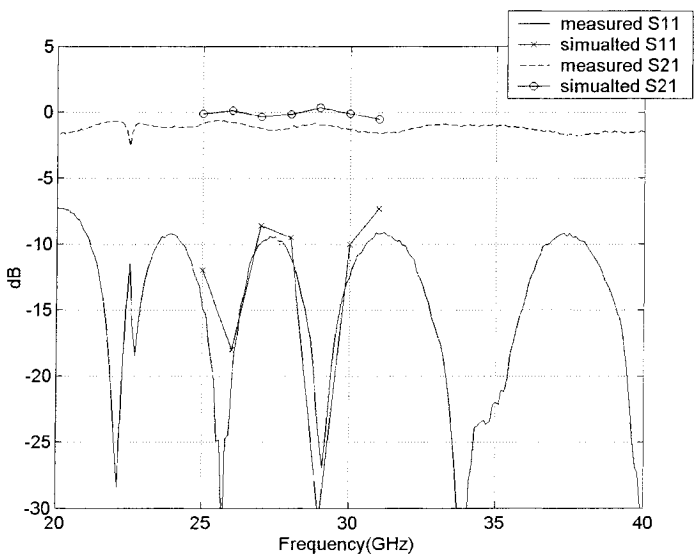


Fig.6.6. Simulated S parameters of an 1-to-4 power divider as a function of frequency.

A back-to-back connected 1-to-4 power divider/combiner shown in Fig.6.7(a) is fabricated and measured. Measured results compared with simulated results are shown in Fig.6.7 (b).



(a)



(b)

Fig.6.7. (a) The back-to-back connected 1 to 4 power divider; (b) The measured S parameters compared with simulated ones.

From Fig.6.7, we can see that the measured S11 parameters agree with the ones obtained from simulation. The measured magnitude of S21 is between –0.8 and –1.6 dB because the ideal conductor is used in simulation, S21 is about 0 dB. If we split the two dividers as shown in Fig.6.7(a) and connect 4 power amplifiers between the two dividers, we can build up a planar power combiner. The maximum potential combining efficiency can be estimated by [53]:

$$\eta_c \approx \sqrt{\frac{|S_{21}|^2}{1-|S_{11}|^2}}. \tag{6.2}$$

Calculated results from equation (6.2) for the structure in Fig.6.7 (a) are shown in Table 6.1. It is shown that combining efficiency around 90% can be achieved within a wide frequency range. The high combining efficiency is due to the low loss of the power dividing/combining structure in which the oversized microstrip line is used. The loss factors due to metallic loss with different width of microstrip lines versus the width are shown in Fig.6.9(calculated by using HFSS). It is shown that the oversized microstrip line has less conductor loss than its normal counterpart.

Table 6.1. The calculated maximum potential combining efficiency.

Frequency (GHz)	η_c	$dB(\eta_c)$
20.00	0.92	-0.70
21.00	0.93	-0.62
22.00	0.93	-0.62
23.00	0.92	-0.68
24.00	0.94	-0.51
25.00	0.92	-0.71
26.00	0.92	-0.71
27.00	0.92	-0.74
28.00	0.92	-0.71
29.00	0.90	-0.94
30.00	0.89	-1.03
31.00	0.89	-1.00
32.00	0.90	-0.90
33.00	0.90	-0.87
34.00	0.89	-1.06
35.00	0.89	-0.99
36.00	0.88	-1.06
37.00	0.89	-0.99
38.00	0.87	-1.16
39.00	0.86	-1.28
40.00	0.84	-1.53

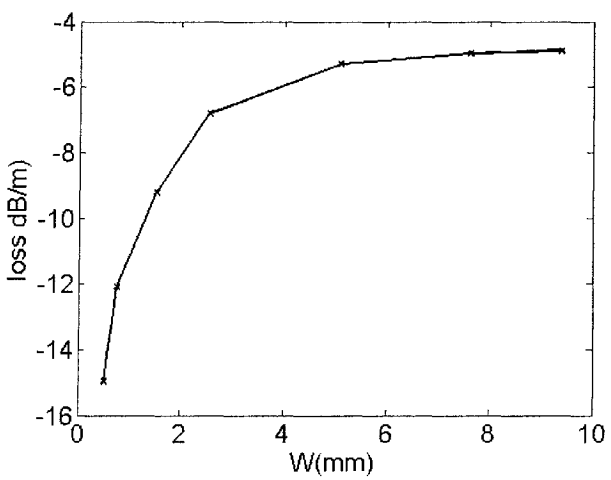


Fig.6.8. The loss factors versus width of the microstrip line.

6.3 Circuit model of the transition by using multi-parallel-port TR calibration

The transition from the oversized microstrip line to the parallel multi-port microstrip lines shown in Fig.6.1 is to accomplish the power dividing and combining functions. Multi-parallel-port TR calibration proposed in Chapter 2 can be used to extract the correct network parameters of the transition. As illustrated in Chapter 2, after we get the parameters of the error boxes, the parameter of the DUT can be calculated by using the de-embedding equation (2.16). However, equation (2.16) is only valid when the port numbers on both sides of the DUT are equal to each other. If the port numbers are different (for example, the transition from oversized microstrip line to parallel multi microstrip lines has one port at one side and multi ports at the other side), equation (2.16) should be modified. A general problem of two cascaded networks that have different port numbers is shown in Fig. 6.8,. The left network has M+N ports, but the right one has 2N ports. We define the left network as DUT, the right network as error box, and the whole cascaded network as EXT.

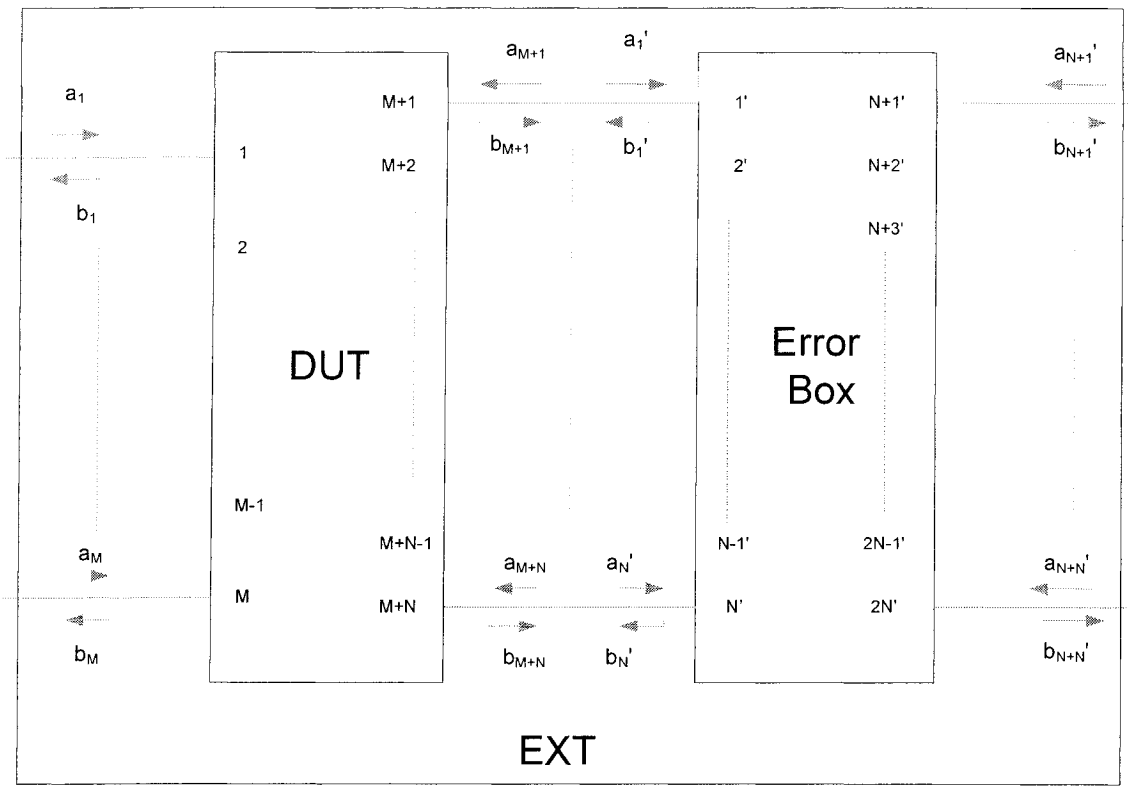


Fig.6.9. Cascade connection of two networks that have different port numbers.

For DUT and EXT, we have:

$$\begin{bmatrix} b_1 \\ b_2 \\ \cdot \\ b_M \\ b_{M+1} \\ b_{M+2} \\ \cdot \\ b_{M+N} \end{bmatrix} = [S_{DUT}]_{(M+N)\times(M+N)} \cdot \begin{bmatrix} a_1 \\ a_2 \\ \cdot \\ a_M \\ a_{M+1} \\ a_{M+2} \\ \cdot \\ a_{M+N} \end{bmatrix}, \tag{6.3}$$

$$\begin{bmatrix} b_1 \\ b_2 \\ . \\ b_M \\ b_{N+1}' \\ b_{N+2}' \\ . \\ b_{N+N}' \end{bmatrix} = [S_{EXT}]_{(M+N)\times(M+N)} \cdot \begin{bmatrix} a_1 \\ a_2 \\ . \\ a_M \\ a_{N+1}' \\ a_{N+2}' \\ . \\ a_{N+N}' \end{bmatrix}. \tag{6.4}$$

For the error box, we have:

$$\begin{bmatrix} b_1' \\ b_2' \\ . \\ b_N' \\ a_1' \\ a_2' \\ . \\ a_N' \end{bmatrix} = [T_{2N\times 2N}] \cdot \begin{bmatrix} a_{N+1}' \\ a_{N+2}' \\ . \\ a_{N+N}' \\ b_{N+1}' \\ b_{N+2}' \\ . \\ b_{N+N}' \end{bmatrix}. \tag{6.5}$$

The T matrix of the error box can be written as

$$[T_{2N\times 2N}] = \begin{bmatrix} T_{11(N\times N)} & T_{12(N\times N)} \\ T_{21(N\times N)} & T_{22(N\times N)} \end{bmatrix}. \tag{6.6}$$

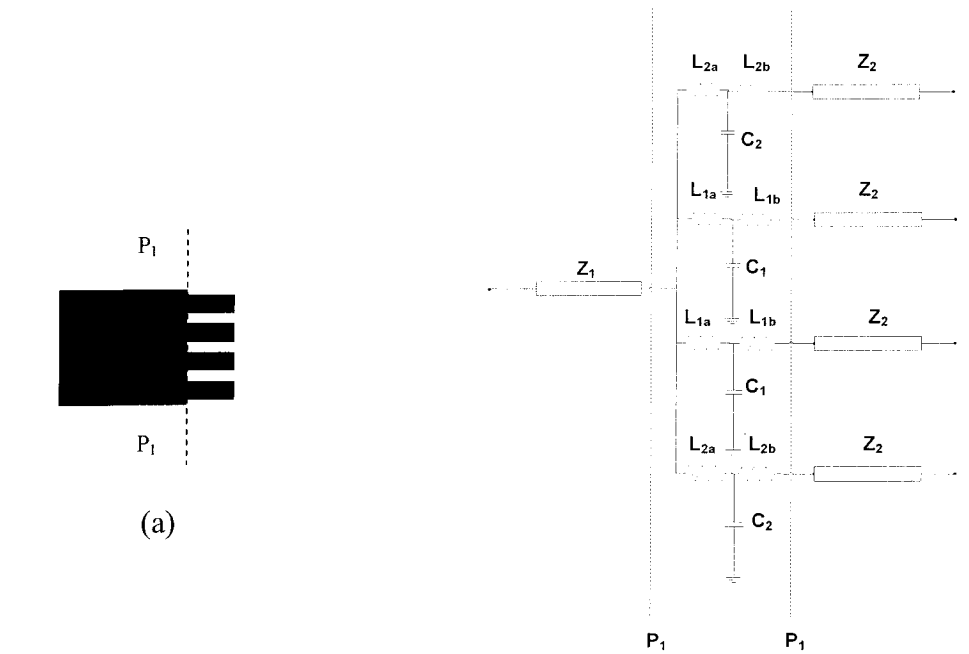
From matrix calculation, we have

$$[S_{EXT}]_{(M+N)\times(M+N)} = \left\{ \begin{bmatrix} I & 0 \\ 0 & T_{22} \end{bmatrix} - [S_{DUT}] \cdot \begin{bmatrix} 0 & 0 \\ 0 & T_{12} \end{bmatrix} \right\}^{-1} \cdot \left\{ [S_{DUT}] \cdot \begin{bmatrix} I & 0 \\ 0 & T_{11} \end{bmatrix} - \begin{bmatrix} 0 & 0 \\ 0 & T_{21} \end{bmatrix} \right\}, \tag{6.7}$$

$$[S_{DUT}]_{(M+N)\times(M+N)} = \left\{ \begin{bmatrix} I & 0 \\ 0 & T_{22} \end{bmatrix} \cdot [S_{EXT}] + \begin{bmatrix} 0 & 0 \\ 0 & T_{21} \end{bmatrix} \right\} \cdot \left\{ \begin{bmatrix} 0 & 0 \\ 0 & T_{12} \end{bmatrix} \cdot [S_{EXT}] + \begin{bmatrix} I & 0 \\ 0 & T_{11} \end{bmatrix} \right\}^{-1}. \tag{6.8}$$

The equation (6.8) can be used to de-embed the parameter of DUT in the calibration procedure.

The correct S parameters of the transition at the reference plane P1 as shown in Fig. 6.8(a) can be extracted by Using multi-parallel-port TR calibration. An equivalent circuit model of the transition of Fig. 6.8(a) can approximately be presented as a five-port network as depicted by Fig. 6.8(b). Since this structure is symmetrical, the circuit model is also symmetrical. The circuit model can effectively be considered as four microstrip steps connected to an oversized microstrip line. In Fig. 6.8(c) and (d) the S parameters of the circuit model are compared with those simulated on the basis of the EM simulation (MOMENTUM of ADS). All the S parameters are obtained with respect to reference plane P1. We can notice that in.Fig. 6.8(d) S12 and S13 are both greater than -6dB. In fact, S12 and S13 cannot be greater than -6dB at the same time. This error is caused by our calibration procedure when we make use of a shift port in the EM simulation. Note that the equivalent circuit model shown in Fig. 6.8(b) is approximate and it is used to demonstrate the concept of this kind of planar power dividing/combining structure.



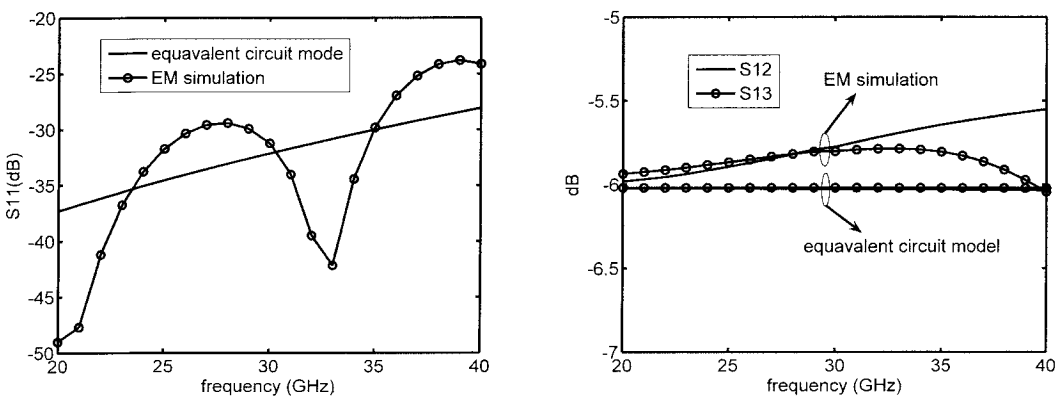


Fig.6.10. Approximate equivalent circuit model and simulated results of the transition from the oversized microstrip line to the parallel multi microstrip lines.

6.4 Experiments

The structure shown in Fig.6.7(a) can be used to realize a power combiner. However, due to the limitation of technology in our laboratories, we cannot place all the biasing capacitors and bonding wires in such a narrow spaced structure. Therefore, a larger structure, which is originally made as a 1-to-8 divider, is designed to realize a 4 unit power combiner, as shown in Fig.6.11. The port 1 is a 50 ohm microstrip line, and. the character impedance of the oversized microstrip line is 6.25 ohm (W=9.4 mm).

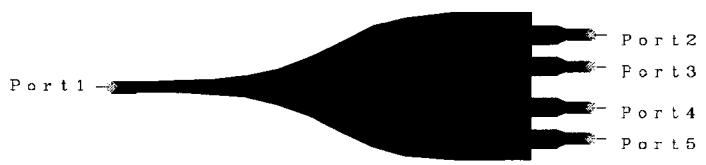


Fig.6.11. The structure of the 1-to-4 power divider/combiner to be used in the power combiner.

According to equation (6.1), the characteristic impedance of each line should be 25 ohm if we use four microstrip lines as the output ports. Therefore, a quarter wavelength impedance transformer is used between the 50 ohm line and 25 ohm line (in the structure, the section of 25 ohm lines are taken out to simplify the structure). The transformer line has impedance of 35.4 ohm and the width is 1.2 mm. The taper section

between the 50 ohm microstrip line and the 6.25 ohm microstrip line is designed on the basis of a theory of Dolph-Tchebycheff taper [54].

The surface current distribution when port 1 is excited is shown in Fig.6.12. Simulated results of the divider are shown in Fig.6.13. The phase difference between S12 and S13 is from 18 degrees to 1.4 degree. The amplitude inbalance between S12 and S13 is around 2dB from 25 to 29 GHz and become larger after 29 GHz.

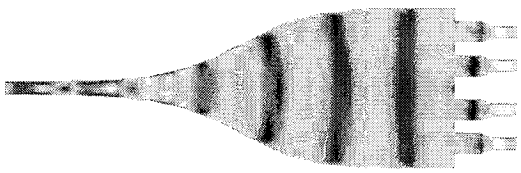


Fig.6.12. The surface current distribution at 31GHz plotted by Momentum.

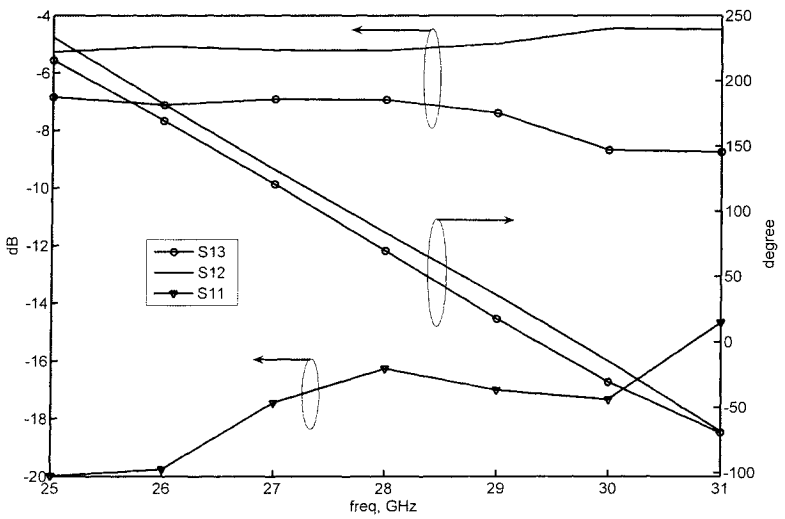


Fig.6.13. Simulated S parameters of the 1-to-4 power divider.

Four GaAs MMIC amplifiers are used to build up the power combiner. The part number of MMIC amplifiers is HMC283 of Hittite Microwave Corporation. It works from 17 to 40 GHZ with a gain of 21dB and a typical P1B of 18 dBm. The power combiner fabricated is shown in Fig.6.14. Both measured and simulated results are shown in Fig.6.15. It is observed that the measured S11 is higher than the simulated one while the measured S12 is lower than the simulated one. The main reason for such discrepancies that bonding wires connecting the IC amplifiers and the microstrip lines are not short enough (0.31 mm was suggested for HMC283, but more than 0.5 mm used in our circuit assembling). The input power versus output power at 25 GHz is shown in Fig.6.16. The P1B point of the power combiner is 23 dBm, meaning that the power combining efficiency is about 79.5%. The P1B parameters versus frequency are shown in Fig.6.17. In [47], the combining efficiency of 82.2% has been achieved at 14.75 GHz, using 12 MMICs, and also the other power combiner using 32 MMICs [48] has reached the combining efficiency of 80% at 10 GHz. There are mainly two factors that lower the power combining efficiency; one is the loss of the power dividing/combining structure and the other is the unequal distribution of power on the multi-port microstrip lines. In [47] and [48], the power combining efficiency is mainly decided by the loss in the passive parts and has little relation to the number of the MMICs. The predicted power combining efficiency of this circuit is between 82% and 87% from 25GHz to 31GHz from equation (6.2). The reduction in power combining efficiency is caused by the inequality of the power distribution on the parallel multi-port microstrip lines, which can be improved by more elaborate design.

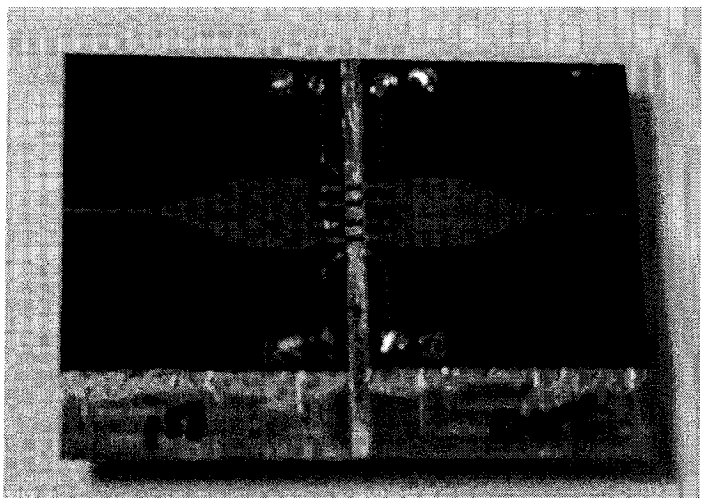


Fig.6.14. The photography of the fabricated quasi-optical planar power combiner.(the size is 69*40 mm^2)

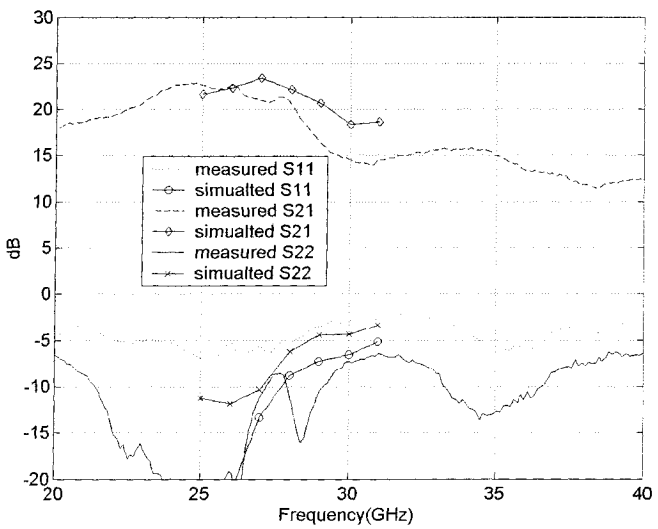


Fig.6.15. Frequency response of measured S parameters compared with simulated ones.

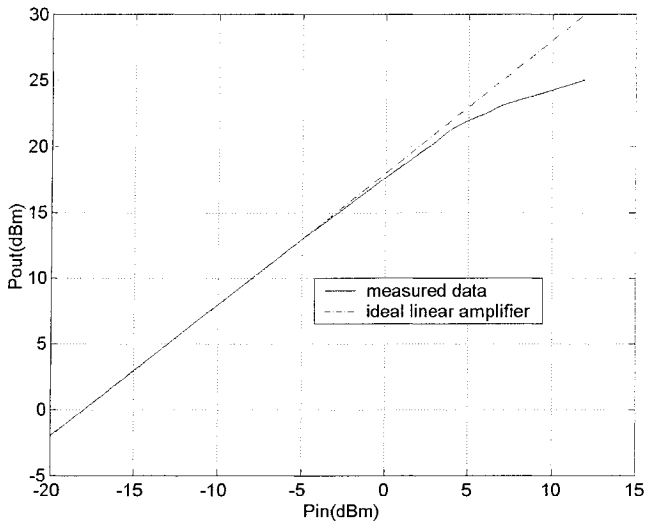


Fig.6.16. Input power versus output power performance at 25 GHz .

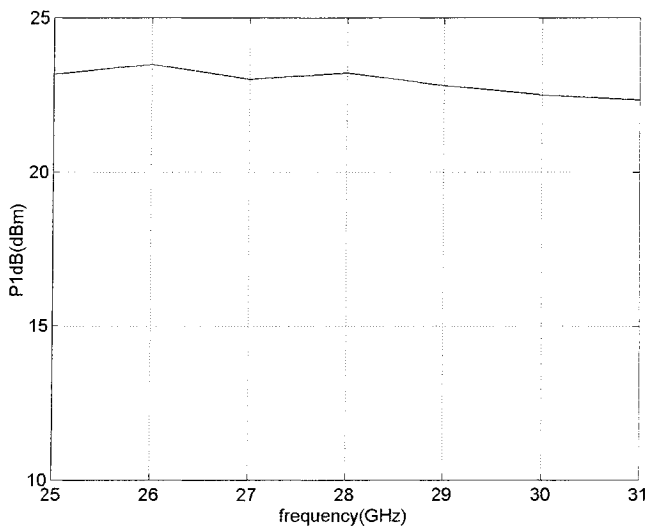


Fig.6.17. The P1B parameters of the power combiner plotted against frequency

This power combiner is similar to the tile style as described in [50]. Here we realize the power combining in only one tile. Comparing this structure with a typical tile style structure [47], we can see that the power dividing/combining structure in [47] is realized

by using parallel multi-port fin lines but in this work the structure of power dividing/combining function is realized by multi-port microstrip lines. The structure in this work is in a planar form, and it is easy to simulate by using the planar EM simulation software. The fabrication of this kind of planar power combiner is very easy by using a planar circuit technology and no complicated mechanical assembling is needed. Since there is only one single substrate required to integrate several power amplifier ICs, so the number of ICs is limited as compared with the other quasi-optical power combiners. This single substrate structure is more suitable for use in a planar system to realize power combiner with moderate number of units. A larger number of power amplifier units may be realized by a multilayered scheme.

6.5 Summary

We have proposed a new simple planar scheme to realize quasi-optical power combiner. The power combining/dividing structure is realized by transition between a simple oversized microstrip line and parallel multi-port planar microstrip lines. A working prototype of the power combiner at 25-31 GHz has been designed and fabricated with 4 amplifier ICs. Measurements show a good agreement with simulations and a combining efficiency of 79.5% with 22dB gain has been achieved at 25 GHz. This type of planar quasi-optical power combiner can be simulated by using full-wave planar EM simulation software and can easily be fabricated. Such power combiners are in a planar form so it is very convenient to integrate these structures with other planar

integrated circuits. A potential problem of this kind of power combiner is that there is only one plane to place the power amplifier units, so the number of the amplifiers involved in a single planar substrate cannot be very large. Multilayer structure should be employed to increase output power capacity of the power combiner because it can contain larger number of amplifier units. From this planar power combiner designing, we can get an extent acknowledge of the quasi-optics power combiner from a circuit viewpoint.

CONCLUSION

We have proposed the numerical TRL and TR calibration techniques to solve the problem of the port discontinuities brought by the inherent lumped current/voltage exciting sources in deterministic MOM algorithms. Therefore, we can accurately de-embed characteristic parameters and extract equivalent full-wave circuit models of the planar structures. Such numerical calibrations techniques are completely compatible with the existing commercial planar electromagnetic simulation software.

Several standards, which are similar to the standards used in real measurement as reflect, line, thru and resistor, have been formulated in the different numerical calibration procedures. Detailed analytical derivation of the calibration algorithms has been given in this work. The TRL calibration has a frequency range limitation, and the characteristic impedance of the line standard in the TRL calibration should be known a priori. In order to obtain 3D characteristic impedance of the line standard, an additional resistor standard has been introduced and demonstrated. For a wide-frequency range calibration, multiple TRL calibration procedures should be used. The proposed TR calibration has no frequency limitation, and it can be used for multi-parallel port calibration.

Equivalent circuit models of the port discontinuities have been extracted by using the numerical calibration techniques. With different exciting schemes, substrates or widths of the line at the exciting port, the values of elements in the circuit model are different.

Based on the transformation from the S parameter to Z or Y parameters, the errors brought by the port discontinuity into the extracted equivalent circuit models of the planar circuit have been analyzed in detail. We can observe that effects of the port discontinuity are irregular and the calibration techniques are absolutely necessary.

Combined with the commercial planar electromagnetic (EM) simulation software, the proposed numerical calibration techniques have been implemented to extract the full-wave circuit models of various planar discontinuities such as microstrip open, microstrip step, microstrip gap, inter-digital capacitor in CPW and the 3D characteristic impedance of microstrip line and microstrip coupled line. Based on the extracted circuit models, one microstrip resonator, one microstrip low-pass filter and one slow-wave line filter have been designed. Design and simulation of the circuits are based on a set of network-oriented topologies. It has been that measured results have confirmed the extracted circuit models. By using the circuit models of planar discontinuities, the design of planar circuit is more accurate than the design based on static model and more efficient than the design with EM simulation.

A novel planar quasi-optical power combiner has been proposed in this work. The power dividing/combining structures have been realized by transitions between the oversized microstrip line and parallel multiple microstrip lines. The numerical calibration technique has been used to extract parameters of the planar power dividing/combining structure, and an approximate circuit model of the structure has been proposed. A Ka-band power combiner using 4 amplifier ICs has been designed and implemented. Measurement has shown a good agreement with simulation, and we have

obtained a combining efficiency 79.5% at 25 GHz. The whole power combiner is a planar structure, and no complicated mechanical assembling is needed. Therefore, it can be integrated in a planar microwave circuit environment. From this planar quasi-optical power combiner design, we can have a clear circuit concept of the quasi-optical power combiner.

On the basis of the proposed numerical calibrations techniques, one can accurately generate the full-wave equivalent circuit model of various planar microwave discontinuities and circuit elements, which can also give insight into the physical behavior of the structures. It has been demonstrated that those accurate models are critical in the design of innovative integrated circuits on the basis of well-established network design strategy for analysis and optimization. The proposed numerical calibrations and de-embedding techniques have been powerful and effective in bridging the gap between the field simulation and circuit design. Such concepts are not just limited to the modeling of electromagnetic problems; they can be well extended to other computational engineering disciplines such as mechanical engineering.

Several possible studies were suggested as an area for future research:

- In this work, numerical calibration techniques have been used to extract the full wave equivalent circuit model of individual elements in circuits. The coupling effect between adjacent elements can be studied through multi-level segmentation procedure.
- The extracted full-wave circuit models of IDCs have been successfully implemented into slow-wave line filter design. Such models can also be

extended to design other circuits such as slow-wave couple line, slow-wave antenna, etc.

- Multi-layer structures for planar quasi-optical power combiner that can contain more power amplifier units.

REFERENCES

[1] R. W. Jackson and D. M. Pozar, "Full-wave analysis of microstrip openend and gap discontinuities," *IEEE Trans. Microwave Theory Tech.,* vol. MTT-33, pp. 1036–1042, Oct. 1985.

[2] L. P. B. Katehi and N. G. Alexopoulos, "Frequency-dependent characteristics of microstrip discontinuities in millimeter-wave integrated circuits," *IEEE Trans. Microwave Theory Tech.,* vol. MTT-33, pp. 1029–1035, Oct. 1985.

[3] H. Y. Yang and N. G. Alexopoulos, "Basic blocks for high frequency interconnects: Theory and experiment," *IEEE Trans. Microwave TheoryTech.,* vol. 36, pp. 1258–1264, Aug. 1988.

[4] L. P. Dunleavy and L. P. B. Katehi, "A generalized method for analyzing thin microstrip discontinuities," *IEEE Trans. Microwave Theory Tech.* vol. 36, pp. 1758–1766, Dec. 1988.

[5] R. W. Jackson, "Full-wave, finite element analysis of irregular microstrip discontinuities," *IEEE Trans. Microwave Theory Tech.,* vol. 37, pp.81–89, Jan. 1989.

[6] W. P. Harokopus and L. P. B. Katehi, "Characterization of microstrip discontinuities on multilayer dielectric substrates including radiation losses," *IEEE Trans. Microwave Theory Tech.,* vol. 37, pp. 2058–2066, 1989.

[7] S. C. Wu, H. Y. Yang, N. G. Alexopoulos, and I. Wolff, "A rigorous dispersive characterization of microstrip cross and T junction," *IEEE Trans. Microwave Theory Tech.,* vol. 38, pp. 1837–1844, Dec. 1990.

[8] T. S. Horng, N. G. Alexopoulos, S. C. Wu, and H. Y. Yang, "Fullwave spectral-domain analysis for open microstrip discontinuities of arbitrary shape including radiation and surface-wave losses," *Int. J. Microwave Millimeter-Wave Computer-Aided Eng.,* vol. 2, no. 4, pp. 224–240, 1992.

[9] J. R. Mosig, "Arbitrarily shaped microstrip structures and their analysis with a mixed potential integral equation," *IEEE Trans. Microwave Theory Tech.,* vol. 36, pp. 314–323, Feb. 1988.

[10] J. R. Mosig, "Integral equation technique," in *Numerical Techniques forMicrowave and Millimeter-Wave Passive Structures,* T. Itoh, Ed. New York: Wiley, 1989, pp. 133–214.

[11] R. H. Jansen, "The spectral-domain approach for microwave integrated circuits," *IEEE Trans. Microwave Theory Tech.,* vol. MTT-33, pp. 1043–1056, Oct. 1985.

[12] R. H. Jansen and W. Wertgen, "Modular source-type 3-D analysis of scattering parameters for general discontinuities, components and coupling effects in (M)MIC's," in *Proc. 17th European Microwave Conf.,* Rome, Italy, Sept. 1987, pp. 427–432.

[13] J. C. Rautio and R. F. Harrington, "An electromagnetic time-harmonic analysis of shielded microstrip circuits," *IEEE Trans. Microwave Theory Tech.,* vol. MTT-35, pp. 726–730, Aug. 1987.

[14] A. Skrivervik and J. R. Mosig, "Equivalent circuits of microstrip discontinuities," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1991, pp. 1147–1150.

[15] J. C. Rautio, "A deembedding algorithm for electromagnetics," *Int. J .Microwave Millimeter-Wave Computer-Aided Eng.*, vol. 1, no. 3, pp.282–287, 1991.

[16] A. Hill, J. Burke, and K. Kottapalli, "Three-dimensional electromagnetic analysis of shielded microstrip circuits," *Int. J. Microwave Millimeter- Wave Computer-Aided Eng.*, vol. 2, no. 4, pp. 286–296, 1992.

[17] B. Linot, M. F. Wong, V. F. Hanna, and O. Picon, "A numerical TRL deembedding technique for the extraction of S-parameters in a 21/2D planar electromagnetic simulator," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1995, pp. 809–812.

[18] L. Zhu, K. Wu, "Short-open calibration technique for field theory-based parameter extraction of lumped elements of planar integrated circuits" *IEEE Trans. Microwave Theory and Tech.*, vol. 50, issue 8, pp. 1861 –1869, Aug. 2002.

[19] L. Zhu and K. Wu, "Unified equivalent-circuit model of planar discontinuities suitable for field theory-based CAD and optimization of M(H)MIC's," *IEEE Trans. Microwave Theory and Tech.*, vol. 47, no. 9, pp. 1589 –1602, Sept. 1999.

[20] L. Zhu and K. Wu, "Network equivalence of port discontinuity related to source plane in a deterministic 3-D method of moments " *IEEE Microwave Guided Wave Lett.*, vol. 8 no 3, pp.130-132, Mar. 1998.

[21] L. Zhu and K. Wu, "Field-Extracted Lumped-Element Models of Coplanar Stripline Circuits and Discontinuities for Accurate Radio-Frequency Design and Optimization" *IEEE Trans. Microwave Theory and Tech.*, vol. 50, issue 4, pp. 1207 –1215, April 2002.

[22] L. Zhu and K. Wu, "Characterization of Finite-Ground CPW reactive Series-Connected Elements for Innovative Design of Uniplanar M(H)MICs" *IEEE Trans. Microwave Theory and Tech.*, vol. 50, issue 2, pp. 549 –557, Feb. 2002.

[23] L. Zhu, K. Wu, "Revisiting characteristic impedance and its definition of microstrip line with a self-calibrated 3-D MoM scheme" *IEEE Microwave and Guided Wave Letters*, vol.8, pp.87-89, Feb. 1998.

[24] J. C. Rautio, "Comments on 'Revisting characteristic impedance and its definition of microstrip line with a self-calibration 3D-MoM scheme'," *IEEE Trans. Microwave Theory Tech.*, vol. 47, pp. 115–117, Jan. 1999.

[25] L. Zhu and K. Wu, "Authors' reply," *IEEE Trans. Microwave Theory Tech.*, vol. 47, pp. 117–119, Jan. 1999.

[26] J. C. Rautio, "Comments on 'On deembedding of port discontinuities in full-wave CAD models of multiport circuits'," *IEEE Trans. Microwave Theory Tech.*, vol. 52, pp. 2448–2449, Oct. 2004.

[27] L. Zhu and K. Wu, "Comparative investigation on numerical de-embedding techniques for equivalent circuit modeling of lumped and distributed microstrip circuits" *IEEE Microwave and Guided Wave Letters*, vol.12, no.2, pp.51-53, Feb. 2002.

[28] L. Zhu, "Guided-wave characteristics of periodic coplanar waveguides with inductive loading - unit-length transmission parameters" *IEEE Trans. Microwave Theory and Tech.*, vol. 51, issue 10, pp. 2133 –2138, Oct. 2003.

[29] L. Zhu and K. Wu, "Accurate Circuit Model of Interdigital Capacitor and Its Application to Design of New Quasi-Lumped Miniaturized Filters with Suppression of Harmonic Resonance " *IEEE Trans. Microwave Theory and Tech.*, vol. 48, issue 3, pp. 347 –356, March 2000.

[30] *Okhmatovski, V.I.; Morsey, J.; Cangellaris, A.C.*, "On deembedding of port discontinuities in full-wave CAD models of multiport circuits" *IEEE Trans. Microwave Theory and Tech.*, vol. 51 , issue: 12 , pp. 2355 - 2365, Dec. 2003.

[31] L. Li, K. Wu and L. Zhu, "Numerical TRL Calibration Technique For Parameter Extraction of Planar Integrated Discontinuities In a Deterministic MoM Algorithm" *IEEE Microwave and Guided Wave Letters*, vol.12, no.12, pp.485-487, Dec. 2002.

[32] L. Li, K. Wu, "NUMERICAL THROUGH-RESISTOR (TR) CALIBRATION TECHNIQUE FOR MODELING OF MICROWAVE INTEGRATED CIRCUITS" *IEEE Microwave and Guided Wave Letters*, vol.14, no.4, pp.139-141, Apr. 2004.

[33] Lin Li, Ke Wu, Russer, P. "Improved numerical TRL calibration technique in a deterministic MoM algorithm" Microwave Conference, 2004. 34th European, vol 1, pp 447 – 450, 11-15 Oct. 2004.

[34] Eul, H.-J.; Schiek, B, "A generalized theory and new calibration procedures for network analyzer self-calibration" *IEEE Trans. Microwave Theory and Tech.*, vol. 39 , issue: 4 , pp. 724-731, April 1991.

[35] Seguinot, C.; Kennis, P.; Legier, J.-F.; Huret, F.; Paleczny, E.; Hayden, L, "Multimode TRL. A new concept in microwave measurements: theory and

experimental verification" *Trans. Microwave Theory and Tech.*, vol. 46, pp. 536-542, issue: 5 , May 1998.

[36] G. F. Engen and C. A. Hoer, " "Thru-Reflect-Line": an improved technique for calibrating the dual six-port automatic network analyzer," *IEEE Trans. Microwave Theory Tech.*, vo.MTT-27, no.12, pp.987-993, Dec. 1979.

[37] D. M. Pozar, *Microwave Engineering*, 2nd ed. New York:Wiley, pp. 217-221, 1998.

[38] N. G. Alexopoulos and S.-C. Wu, "Frequency-independent equivalent circuit model for microstrip open-end and gap discontinuities," *IEEE Trans. Microwave Theory and Tech.*, vol. 42, no. 7, pp. 1268 –1272, July 1994.

[39] K. C. Gupta, R. Garg, I. Bahl and P. Bhartia, *Microstrip Lines and Slotlines*, pp.180-182, (2nd ed.), *Artech House*, Inc., Boston, 1996.

[40] R. A. Speciale, "A generalization of the TSD network-analyzer calibration procedure, covering n-port scattering-parameter measurements, affected by leakage errors," *Trans. Microwave Theory and Tech.*, vol. 25, pp. 1100-1115, no.12, Dec. 1977.

[41] J. C. Rautio, "A new definition of characteristic impedance," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1991, pp. 761–764.

[42] G. D. Alley, "Interdigital capacitors and their application to lumpedelement microwave integrated circuits," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-18, pp. 1028–1033, Dec. 1970.

[43] E. Pettenpaul *et al.*, "CAD models of lumped elements on GaAs up to 18 GHz," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 294–304, Feb. 1988.

[44] S. S. Gevorgian *et al.*, "CAD model for multilayered substrate Interdigital capacitors," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 896–904, June 1996.

[45] G. Coen, D. D. Zutter, and N. Fache, "Automatic derivation of equivalent circuits for general microstrip interconnection discontinuities," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 1010–1016, July 1996.

[46] J. Zhou, D. Hung, M. J. Lancaster, H. T. Su, X. Xiong, "A novel superconducting CPW slow-wave bandpass filter," *Microwave and Optical Technology Letters*, vol. 34, No. 4, pp. 255–259, August 2002.

[47] Belaid, M.; Ke Wu;, "Spatial power amplifier using a passive and active TEM waveguide concept", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-51, pp. 684–689, Mar. 2003.

[48] Pengcheng Jia; Lee-Yin Chen; Alexanian, A.; York, R.A.;, "Multioctave spatial power combining in oversized coaxial waveguide", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-50, pp. 1355–1360, May 2002.

[49] Ivanov, T.; Balasubramaniyan, A.; Mortazawi, A.;, "One- and two-stage spatial amplifiers", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-43, pp. 2138–2143, Sept. 1995.

[50] DeLisio, M.P.; York, R.A.;, "Quasi-optical and spatial power combining", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-50, pp. 929–936, Mar. 2002.

[51] J. S. H. Schoenberg and Z. B. Popovic, "Planar lens amplifier," in 1994 IEEE MTT-S Int. Microwave Symp. Dig., San Diego, CA, 1994, pp. 429-432.

[52] C. W. Hicks, H. S. Hwang, M. B. Steer, J. W. Mink, and J. F. Harvey, "Spatial power combining for two-dimensional structures", IEEE Trans. Microwave Theory Tech., vol. MTT-46, pp. 784–791, June 1998.

[53] Tayag, T.J.; Steer, M.B.; Harvey, J.F.; Yakovlev, A.B.; Davis, J., "Spatial power splitting and combining based on the Talbot effect ", *IEEE Microwave and Guided Wave Letters*, vol.12, pp.9-11, Jan. 2002.

[54] R. W. Klopfenstein, "A transmission-line taper of improved design," *Proc. IRE*, vol. 442, pp. 31–35, Jan. 1956.