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METHODS FOR THE MODELING AND ANALYSIS OF MIS INTERCONNECTS IN VLSI CIRCUITS

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METHODS FOR THE MODELING AND ANALYSIS OF MIS INTERCONNECTS IN VLSI CIRCUITS

Présentée par: JIN Zhongfang

en vue de l'obtention du diplôme de Philosophiae Doctor

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To my family

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RÉSUMÉ

Les objectifs de cette thèse sont: 1. la modélisation de longues interconnexions en configuration Métal-Isolant-Semi-conducteur (MIS), 2. le développement d'une méthode visant à simplifier la modélisation de ces interconnexions et 3. une analyse de l'intégrité du signal dans des réseaux renfermant de longues interconnexions.

Dans cette thèse, une méthode innovatrice est proposée pour estimer l'erreur de simulation induite pour un modèle développé dans le domaine du temps, en utilisant les paramètres du circuit dans le domaine fréquentiel. Une telle méthode se base sur le spectre fréquentiel d'une source de tension et sur la différence des fonctions de transfert de tension entre un modèle et sa référence. Concrètement, les fonctions de transfert de tension peuvent être obtenues à partir de la matrice de répartition normalisée (paramètres *S*). Pour illustrer la méthode, un simple modèle de ligne RC avec résistance de source R_s et charge capacitive C_L est utilisé. Il est démontré que l'estimation que fournit ladite méthode pour l'erreur induite par un modèle fournit une borne supérieure de l'erreur dans le cadre d'une simulation de circuit dans le domaine du temps.

Une approche pratique est proposée pour modéliser une interconnexion MIS simple dans un circuit intégré à très grande échelle (ITGE). Trois étapes composent cette méthode. En premier lieu, mettant à profit la littérature concernant le sujet, on construit un modèle RLCG-B original avec cinq paramètres de circuit. Deux largeurs physiques équivalentes sont proposées pour la trace de métal, représentant respectivement les distributions de champ pour les couches d'isolant et de semi-conducteur. Le modèle RLCG-B original étend la validité de certaines expressions d'un espace unidimensionnel (1D) à un espace 2D en plus d'être validé par des simulations numériques pour des fréquences allant jusqu'à 10 GHz et pour des substrats avec des résistivités supérieures à 1 Ω·cm.

En second lieu, le modèle RLCG-B original est modifié dans le but d'incorporer des modèles simples de circuits équivalents dans des logiciels de simulation tel SPICE. Le nouveau modèle est appelé modèle RLCG-B modifié. Deux paramètres de circuit variant avec la fréquence et reliés aux impédances série dans le modèle RLCG-B original sont remplacés dans le modèle modifié par un sous-circuit RL renfermant quatre paramètres de circuit indépendants de la fréquence. Des expressions analytiques sont proposées pour obtenir les quatre nouveaux paramètres de circuit. Des simulations numériques démontrent que la différence entre les modèles RLCG-B original et modifié en ce qui concerne les impédances séries par unité de longueur est minime et peut être négligée pour les plages de fréquence et de résistivité d'intérêt (fréquence$\leq$10 GHz et résistivité$\geq$1 Ω·cm).

Le modèle modifié se révèle précis, cependant qu'il met à forte contribution les ressources de temps et de mémoire. Conséquemment, quelques simplifications sont finalement apportées au modèle modifié RLCG-B, de façon à obtenir un modèle efficace. Partant du modèle RLCG-B modifié comme référence, cinq modèles simplifiés sont analysés soit en négligeant l'effet pelliculaire dans la trace de métal, en négligeant les pertes diélectriques dans la couche semi-conductrice ou encore en considérant la couche semi-conductrice comme un conducteur électrique parfait. En mettant à profit la méthode présentée dans cette thèse, l'erreur de simulation induite respectivement par les cinq modèles simplifiés est estimée en considérant les conditions à la source et à la charge. En combinant le spectre fréquentiel d'une source de tension avec la différence entre les fonctions de transfert des modèles simplifiés et de la référence, la différence absolue entre les tensions de charge des modèles simplifiés versus le modèle de référence sont obtenues. Pour un cas donné, il est démontré que l'erreur induite par le modèle dans le domaine du temps est minime si l'on néglige l'effet pelliculaire dans la trace métallique, cependant que l'erreur est grande si les pertes diélectriques sont négligées. Il est intéressant de constater que l'erreur de modélisation reste raisonnable lorsqu'on considère la couche semi-conductrice comme un conducteur électrique parfait.

Dans le but d'analyser la précision de modélisation en terme d'erreur de simulation, l'intervalle de fréquence d'intérêt dicté par le spectre fréquentiel de la tension de charge est divisé en trois sous-régions fréquentielles. La largeur de bande de la tension de charge dépend de deux facteurs: la largeur de bande de la source de tension ainsi que celle de la fonction de transfert de l'interconnexion. Pour le même cas donné plus haut, les résultats numériques montrent que la précision de modélisation a beaucoup d'impact sur l'erreur de simulation pour la partie du spectre fréquentiel de tension se situant entre le courant continu et le point à –3 dB, région où se concentre la majeure partie de l'énergie. Hors de cette région fréquentielle, la contribution à l'erreur totale de simulation est faible.

Pour faciliter la modélisation d'une interconnexion simple en configuration MIS, un plan γ_n normalisé est défini dans le but de visualiser les différences existant entre les caractéristiques de propagation du modèle simplifié et d'une référence. Dans ce plan, tout le spectre de fréquences d'intérêt peut être représenté par une courbe. Ainsi, en comparant la courbe d'un modèle simplifié avec celle d'une référence dans la plan γ_n normalisé, on constante les différences d'atténuation d'amplitude et de délai de phase entre le modèle et la référence lorsque que des signaux parcourent l'interconnexion. Ceci implique que les impédances de source et de charge soient toutes deux égales à l'impédance caractéristique de la ligne.

Pour fins de comparaison, la modélisation d'une interconnexion simple sera mise en parallèle avec la modélisation d'une configuration à deux interconnexions MIS couplées et dont l'une des deux est utilisée pour le retour de courant (mode impair). Cette configuration fait également l'objet de cette thèse. Deux étapes sont nécessaires pour créer un modèle efficace pour le mode impair de deux interconnexions couplées. Basé sur le modèle RLCG-B original pour une interconnexion simple et d'autres modèles de la littérature, un modèle RLCG-B hybride est d'abord élaboré pour le mode impair de deux interconnexions couplées. Ce modèle hybride est alors modifié pour devenir un

simple modèle RLC en considérant le semi-conducteur comme un diélectrique parfait et en négligeant l'impact du plan métallique de mise à la masse sur les deux interconnexions. En comparant la constante de propagation complexe du modèle simple RLC avec les résultats fournis par des modèles basés sur la méthode des moments, nous pouvons affirmer que le modèle simple RLC reproduit fidèlement le comportement électrique du mode impair de deux interconnexions si l'espace entre les deux conducteurs s_m est comparable à la largeur du conducteur w_m. Il existe une valeur seuil de s_m/w_m . En deçà de ce seuil, un fort couplage existe entre les deux interconnexions et des prédictions fiables peuvent être obtenues avec un modèle RLC simple. Au-dessus du seuil, le couplage devient faible. Ainsi, l'impact du plan arrière en métal sur les deux interconnexions ne peut plus être négligé, et le modèle RLC simple devient non approprié pour modeler le mode impair des deux interconnexions. Dans certains cas avec la technologie à l'échelle du micron, en considérant une tranche de silicium de 300 μm d'épaisseur, la valeur seuil s_m/w_m observée est autour 8, ce qui correspond à un espacement de moins de 25 μm entre les deux interconnexions.

Cependant, dans ces conditions de couplage faible, la différence entre les caractéristiques de propagation des interconnexions couplées et d'une interconnexion simple est minime. Ainsi, deux interconnexions couplées avec un faible couplage peuvent être considérées comme deux interconnexions simples sans couplage. Ce qui revient à dire qu'un modèle tel que le RLCG-G modifié, développé pour une interconnexion MIS simple peut également prédire le comportement électrique de deux interconnexions MIS couplées. De la même façon que pour le modèle simple RLC, une valeur seuil de s_m/w_m est utilisée pour déterminer si le modèle à une ligne décrit bien le mode impair de deux interconnexions. Au-dessus de ce seuil, le couplage est faible et des prédictions de qualité peuvent être obtenues du modèle à une ligne. Basé sur des résultats numériques, la gamme valide de s_m/w_m pour le modèle à une ligne semble être

recouverte par celui pour le modèle simple RLC. Anisi, une valeur-seuil de s_m/w_m peut être placée pour les deux modèles.

Ces efforts de modélisation mènent à une analyse d'intégrité pour un signal parcourant des interconnexions MIS. Dans cette thèse, deux démarches sont investiguées. La première consiste à évaluer le délai temporel de propagation pour des lignes RC avec impédance de source R_S et charge capacitive C_L dans des circuits ITGE. On recherche les conditions de validité qui permettraient de modéliser une ligne avec des sections RC d'eléments discrets. Puisque l'évaluation de forme d'onde asymptotique est une procédure ayant fait ses preuves pour ce qui est de prédire la réponse temporelle de circuits linéaires, cette méthode est ici utilisée pour analyser le délai de propagation sur des lignes RC. Un nombre limité de pôles est utilisé dans l'analyse pour éviter l'instabilité numérique, même si cela peut introduire de l'imprécision dans le cas de circuits compliqués. La précision des modèles discrets avec un certain nombre de sections est représentée dans un plan *r-c* normalisé, lequel plan est valide pour diverses technologies. En utilisant l'information détaillée dans cette thèse, un utilisateur peut sélectionner un modèle de complexité minimale qui remplit les exigences de précision d'une approximation donnée. Dans certains cas, la structure de base d'une section (T ou π) exerce une influence significative sur la précision d'une certaine complexité de modèle. Cette thèse guide l'utilisateur vers le choix du modèle le plus efficace.

Le nombre essentiel de sections T ou π pour des modèles de lignes RC est également mis en relation avec la largeur de bande de la tension de charge. Pour une source de tension échelon, le spectre fréquentiel de la tension de charge sera déterminé uniquement par la bande passante du système, qui peut être estimée par le délai temporel de propagation. Ainsi, pour une ligne RC spécifique, la largeur de bande de la tension aux bornes d'une petite charge associée à une forte source est supérieure à la largeur de bande de la tension aux bornes d'une grosse charge associée à une faible source. Considérant ceci, la précision de modélisation d'une ligne RC distribuée a davantage

d'impact sur l'erreur de simulation induite par la modélisation dans le premier cas mentionné et donc, plus de sections T ou π sont nécessaires dans le modèle.

L'autre volet de l'analyse d'intégrité de signal étudié porte sur la divergence des temps de propagation dont l'analyse est faite. Dans cette thèse, une nouvelle méthode hybride est proposée pour réduire la divergence des temps de propagation. Cette méthode comporte trois outils. Des directions de propagation alternatives sont utilisées pour des signaux parallèles afin de réduire l'interférence électromagnétique entre lignes voisines. Un agencement de phase en zigzag est instauré pour les signaux voyageant dans la même direction afin de réduire davantage l'interférence entre les lignes. Des suiveurs et des inverseurs sont alternativement insérés en guise de répéteur dans chaque interconnexion pour compenser l'effet de l'interférence due aux cas de double polarité sur l'incertitude des délais de propagation. Pour des applications pratiques, nous recommandons premièrement l'utilisation d'inverseurs seulement afin de réduire la divergence des temps de propagation. Si celle-ci surpasse toujours les tolérances permises, l'usage alternatif de suiveurs comme répéteurs pour réduire l'effet de couplage sur la divergence des temps de propagation. Les dimensions des suiveurs et inverseurs devraient être ajustées avec soin pour éviter d'obtenir des valeurs variables de divergence de temps de propagation, ce qui peut arriver avec des répéteurs présentant des caractéristiques différentes.

ABSTRACT

The objectives of this thesis are: 1.modeling of long interconnects in the metal-insulator-semiconductor (MIS) configuration, 2.developing a method to simplify modeling of long interconnects and 3.analyzing signal integrity of networks including long interconnects.

In this thesis, a novel method is presented to estimate the time-domain model-induced simulation error using frequency domain circuit parameters. Such method is based on the spectrum of voltage source and on the difference of the voltage transfer functions between a model and a reference. Practically, the voltage transfer functions can also be obtained from the renormalized S-parameters. A simple RC transmission line net with source resistance R_S and load capacitance C_L is used to illustrate this method. It is demonstrated that the model-induced error produced by the proposed method provides an upper limit for the time-domain simulation error obtained from circuit simulator.

A practical approach is presented to model a single MIS interconnect in VLSI circuits. Three steps are taken in this approach. At first, based on the literature, an "original RLCG-B" model with five equivalent circuit parameters is constructed for a single MIS interconnect. Two equivalent widths are proposed for the physical metal strip, reflecting the field spread for the insulator and semiconductor layers, respectively. The original RLCG-B model extends the validity range of some closed-form expressions from 1D to 2D, and is validated by numerical simulations for frequencies up to 10 GHz and for substrate resistivities greater than 1 Ω·cm.

Secondly, the original RLCG-B model is revised for the purpose of embedding simple equivalent circuit models into simulation software such as SPICE. The new model is called a "modified RLCG-B" model. Two frequency-dependent circuit parameters related to the series impedance in the original RLCG-B model are replaced by a RL sub-

network of four frequency-invariant circuit parameters in the modified RLCG-B model. Analytical expressions are proposed to obtain the values of the four new circuit parameters. Numerical simulations demonstrate that the difference of series impedance per unit length between the modified and the original RLCG-B models is small and can be neglected for frequency and resistivity ranges of interest (frequency$\leq$10 GHz and rersistivity$\geq$1 Ω·cm).

The modified model is accurate, however, it is time-and-memory consuming. Thus, some simplifications are finally performed for the modified RLCG-B model in order to obtain an efficient model. Regarding the modified RLCG-B model as a reference, five simplified models are analyzed either by neglecting the skin effect in metal strip, or by neglecting the dielectric losses in the semiconductor layer, or by treating the semiconductor layer as a perfect electric conductor. Using the method proposed in this thesis, the model-induced simulation error for those five simplified models is estimated by including the conditions on the source and load. Combining the spectrum of a voltage source with the differences of voltage transfer functions between the simplified models and the reference, the absolute difference of load voltages between the simplified models and the reference is obtained. For a special case, it is demonstrated that the time-domain model-induced error is small if the skin effect in the metal strip is neglected but the error is large if the dielectric losses are neglected. It is interesting see that the model-induced error is not large if the semiconductor layer is treated as a perfect electric conductor.

In order to analyze the modeling accuracy over different frequency sub-regions on the simulation error, the whole frequency range of interest is divided into three frequency sub-regions according to the bandwidth of the load voltage. Here, the bandwidth of the load voltage depends on both the bandwidth of voltage source and the one of the interconnect. For the specific case above, numerical results show that the modeling accuracy has great impact on the simulation error inside the voltage spectra from DC to

the –3 dB point, where most of the energy is concentrated, and that the contribution to the total simulation error outside is small.

In the practical approach to model a single interconnect in the MIS configuration, a newly normalized γ_n-plane is defined in order to display the difference of propagation characteristics between simplified model and a reference, where the whole frequency range from DC to the highest frequency of interest can be mapped-out by a curve. Therefore, by comparing the curve of a simplified model with the one of a reference in the normalized γ_n-plane, we can assess the differences of magnitude attenuation and phase delay between the model and the reference as signals travel through the interconnect. Here, it is assumed that the source and load impedances are both equal to the characteristic impedance of the wire.

Besides modeling of a single MIS interconnect, for comparison, a topology of two coupled interconnects in the MIS configuration is also investigated in this thesis, where one of the two coupled interconnects is used as current returning path. There are two steps to create an efficient model for the odd mode of two coupled interconnects. Based on the original RLCG-B model for a single interconnect and other models in the literature, a "hybrid RLCG-B" model is first constructed for the odd-mode of two coupled interconnects. This hybrid RLCG-B model is then evolved into a simple RLC model by assuming the semiconductor as a perfect electric conductor and by neglecting the impact of the back metal plane on the two interconnects. By comparing the complex propagation constant of the simple RLC model with the results predicted by moment method models, we find that the simple RLC model captures the electrical behavior of the odd-mode of coupled interconnects well if the wire spacing s_m is comparable to the line width w_m. It seems that there is a threshold value of s_m/w_m . Under the threshold, a strong coupling exists between the two interconnects and a good prediction can be obtained with the simple RLC model. Above the threshold, the coupling between the two interconnects becomes weak. So, the impact of the back metal plane on the two

interconnects can no longer be neglected, and the simple RLC model becomes not suitable to model the odd-mode of two interconnects. For a group of special cases with micron technology, it is found that for a typical 300 μm thick Si wafer, the threshold value of s_m/w_m is around 8, which corresponds to the spacing between two interconnects less than 25 μm.

On the contrary, the difference of propagation characteristics between single and coupled interconnects is small under the conditions of weak coupling. Therefore, two coupled interconnects with weak coupling can be approximately treated as two single interconnects without coupling. That is to say, a one-wire model such as the modified RLCG-B model originally for a single MIS interconnect, can also approximate the electrical behavior of two coupled MIS interconnects. Similarly to the simple RLC model, a threshold value of s_m/w_m is used to determine if the one-wire model is suitable for the odd mode of two interconnects. Above the threshold, a coupling is weak and a good prediction can be obtained from the one-wire model. Based on numerical results, the valid range of s_m/w_m for the one-wire model seems to be partially overlapped by the one for the simple RLC model. Thus, a threshold value of s_m/w_m can be set for both models.

The purpose of modeling is for signal integrity analysis. In this thesis, two issues are studied. One issue is the propagation time delay for RC wires with source impedance R_S and capacitive load C_L in VLSI circuits. The validity conditions are investigated for modeling a wire with lumped RC sections. Since asymptotic waveform evaluation (AWE) is a well-known procedure to predict the time response of linear circuits, it is implemented to analyze time delay on RC wires. A limited number of AWE poles are used to avoid the numerical instability, though it may lead to inaccuracy for complicated circuits. The accuracy of lumped models with the number of sections is mapped in a normalized *r-c* plane, which is valid for different technologies. Using the information provided in this thesis, a user can select a model of minimal complexity that meets the

accuracy requirements of a given approximation. In some cases, the basic cell structure (T- or π-) has a significant impact on accuracy for a given model complexity, and this thesis allows selecting the most efficient model.

The essential number of T- or π- sections for RC wire models is also illustrated with respect to the bandwidth of the load voltage. For a step voltage source, the bandwidth of the load voltage will only be determined by the bandwidth of the system, which can be estimated by the propagation time delay. Thus, for a specific RC wire, the bandwidth of load voltage with a strong driver and a light load is wider than that of load voltage with a weak driver and a heavy load. Thus, the modeling accuracy of a distributed RC wire has more impact on the time-domain model-induced simulation error for the front case, and more T- or π- sections are needed for RC wire models.

The other issue on signal integrity analysis is the propagation time skew analysis. In this thesis, a new combined method is proposed to reduce propagation time skew. There are three features in our method. Alternative propagation directions are used for parallel signals to reduce the electromagnetic interference (EMI) intervals among neighbour wires. A zigzag phase pattern implementation for the same direction signals is implemented to further reduce the crosstalk among neighbour wires. Alternatively buffers and inverters as repeaters are inserted in each interconnect to compensate the impact of dual-polarity crosstalk on the propagation time delay uncertainty. For practical applications, we first recommend using the method of inverters only to reduce the propagation time skew. If the time skew is still larger than tolerated, then we select alternative usage of both buffers and inverters as repeaters to reduce the impact of the coupling effect on the propagation time delay uncertainty. The sizes of buffers and inverters should be carefully adjusted to minimize the variation of propagation time skew due to the different characteristics of buffers and inverters.

CONDENSÉ EN FRANÇAIS

MÉTHODES POUR LA MODÉLISATION ET L'ANALYSE DES INTERCONNEXIONS DANS DES CIRCUITS INTÉGRÉS À TRÈS GRANDE ÉCHELLE

Les objectifs de cette thèse sont: la modélisation de longues interconnexions en configuration Métal-Isolant-Semi-conducteur (MIS), le développement d'une méthode visant à simplifier la modélisation de ces interconnexions et une analyse de l'intégrité du signal dans des réseaux renfermant de longues interconnexions.

0.1 Introduction

La croissance rapide et effrénée de la technologie d'intégration à très grande échelle (ITGE) a été rendue possible par les progrès constants réalisés dans la miniaturisation des dispositifs ITGE. Une évolution aussi soutenue est lourde d'impacts sur la conception des interconnexions. Les performances électriques des interconnexions sont devenues un facteur important lorsque vient le temps d'évaluer le rendement d'un système. Puisque l'analyse du comportement électrique des interconnexions dans un circuit ITGE est un sujet très large, nous avons concentré nos efforts sur la modélisation électrique d'interconnexions et sur l'analyse d'intégrité de signal, qui sont de près reliées à deux projets industriels nous impliquant. D'autres volets tels l'optimisation de la dissipation de puissance dans les interconnexions sont mis sur la glace pour le futur.

0.2 Revue bibliographique

À cause de la contribution significative des interconnexions aux temps de propagation, une modélisation équivalente et efficace d'interconnexions sur puces utilisant la technologie ITGE est devenue extrêmement nécessaire. Il y a plusieurs arrangements dignes d'intérêt pour des interconnexions en configuration MIS tel que montré à la figure 2.1. La figure 2.1a montre une ligne microruban en configuration MIS, pour laquelle le plan de masse est utilisé en guise de retour de courant. Les premières études concernant les lignes microruban remontent aux années'60 [33,34]. Un arrangement un peu plus complexe consiste en deux interconnexions MIS couplées, pour lesquelles une des deux peut agir comme retour de courant. D'autres arrangements plus complexes encore existent, telle est la situation montrée dans la figure 2.1c, qui est en fait une vue de coupe sur le plan défini par la ligne AA' dans le circuit de la figure 2.1d , laquelle représente une longue trace porteuse de signal qui traverse une géométrie interdigitée de traces d'alimentation et de masse. De telles conceptions complexes existent pour conjuguer deux réalités particulières présentes dans les circuits ITGE modernes. Dans cette thèse, nous concentrons nos efforts sur la modélisation d'une interconnexion MIS simple, en considérant que l'étude d'un cas aussi simple peut aider à la compréhension des mécanismes fondamentaux de propagation en configuration MIS. Comparativement, nous étudions également un modèle de circuit équivalent pour le mode impair de deux interconnexions MIS couplées, pour lesquelles une des deux peut agir comme retour de courant. Malgré la disponibilité de plusieurs modèles [10-12][14,15][84,85], ceux-ci ne répondent pas aux critères de performance recherchés en simulation, puisqu'ils consomment temps et mémoire en trop grandes quantités. Conséquemment, des modèles simples deviennent nécessaires dans le but de les incorporer dans des simulateurs tels SPICE, fonctionnant dans le domaine du temps.

Dès que les paramètres du circuit distribué équivalent sont connus, il devient possible de construire des modèles de circuit en utilisant plusieurs techniques [21] telles que

l'obtention de circuits discrets itératifs (« ILC : iterated lumped circuits») et la méthode des caractéristiques (MC). À ce stade, une méthode générique est nécessaire pour estimer l'erreur de simulation commise entre un modèle approximatif et une référence. En se basant sur cette méthode, on peut déterminer si un modèle simple représente fidèlement une interconnexion simple ou deux interconnexions couplées. Plus que tout, en étudiant l'impact de la précision de la modélisation sur l'erreur de simulation dans le domaine du temps, on peut déterminer si de plus ou moins grandes variations de la constante complexe de propagation et de l'impédance caractéristique complexe peuvent être tolérées, ces quantités étant calculées dans le domaine fréquentiel.

Le but de la modélisation d'interconnexions dans le contexte de circuits intégrées à très grande échelle réside dans la nécessité de procéder à des analyses d'intégrité de signal [29], lesquelles se basent sur des paramètres tels les temps de propagation, le sous-dépassement, le sur-dépassement et d'autres encore. En guise d'exemple, une ligne RC distribuée est utilisée pour étudier le temps de propagation dans les circuits ITGE. Les lignes RC ont déjà fait l'objet d'études poussées [55,56], or les paramètres physiques de celles-ci varient selon les différentes technologies. Donc, une approche générique est nécessaire pour sélectionner les paramètres appropriées au modèle d'une ligne RC donnée. Un autre paramètre de l'analyse d'intégrité de signal est la divergence des temps de propagation qui se révèle d'une grande importance dans le cadre de l'utilisation d'une technologie ITGE sur grandes surfaces (« WSI »). Des applications haute vitesse développées avec des circuits « WSI » imposent des spécifications excessivement sévères pour les interconnexions de grande longueur. Les méthodes existantes [59-68] capables de réduire la divergence des temps de propagation relèvent du logiciel, du matériel ou d'une combinaison des deux. Des méthodes simples et pratiques sont requises pour réduire la divergence des temps de propagation dans un bus d'interconnexions parallèles.

0.3 Méthode d'estimation de l'erreur temporelle de simulation dans le domaine fréquentiel

La plupart des publications concernant la modélisation des interconnexions utilisent des validations dans le domaine fréquentiel, lesquelles sont réalisées en comparant pour le modèle et la référence des paramètres tels la constante complexe de propagation, l'impédance caractéristique complexe, les matrices d'impédance et d'admittance et d'autres types des caractéristiques. Ces comparaisons dans le domaine fréquentiel sont valables, mais davantage appropriées à une utilisation dans les applications radio fréquences (RF). En technologie ITGE, le domaine du temps offre un point de vue de prédilection pour évaluer les distorsions de signal, les délais de propagation, etc. De plus, la validation des modèles dans le domaine fréquentiel peut se révéler exigeante en ressources lorsqu'on travaille à de hautes fréquences, auxquelles une grande précision peut ne pas être nécessaire pour obtenir des prédictions satisfaisantes dans le domaine du temps.

Dans la section 3.2, nous proposons une méthode générique pour estimer l'erreur temporelle dans le pire des cas en utilisant les caractéristiques des interconnexions dans le domaine fréquentiel. Cette méthode se base sur le spectre fréquentiel d'une source de tension et sur la différence des fonctions de transfert de tension entre un modèle et sa référence. Dans la section 3.2.2, la bande fréquence d'intérêt est divisée en plusieurs régions afin d'illustrer la contribution des composantes d'un groupe de fréquences à la forme du signal temporel. Ceci est fait en se basant sur la largeur de bande d'une source transitoire de tension, avec ou sans considération pour la bande passante du système. La limite supérieure d'erreur de simulation temporelle impliquant des interconnexions ITGE est démontrée à la section 3.3 avec un exemple simple tel que montré à la figure 3.1. Puis, une relation entre la fonction de transfert de tension et les paramètres S est obtenue à la section 3.4. L'avantage d'utiliser les paramètre S fait également l'objet de discussions dans ce chapitre.

0.4 Modélisation d'une interconnexion simple en configuration MIS

Ce chapitre traite de l'obtention de modèles d'interconnexions précis. La méthode proposée dans le troisième chapitre est utilisée pour étudier l'impact de l'imprécision engendrée par la modélisation sur l'erreur de simulation temporelle. Dans la section 4.2, un modèle RLCG-B original est élaboré avec cinq paramètres de circuit équivalent. Dans ce cas, deux largeurs physiques équivalentes sont proposées pour la trace de métal, représentant respectivement les distributions de champ pour les couches d'isolant et de semi-conducteur. Le modèle RLCG-B a été validé par des simulations numériques pour des fréquences allant jusqu'à 10 GHz et pour des substrats avec des résistivités supérieures à 1 Ω·cm.

De façon à obtenir un modèle avec des paramètres insensibles à la fréquence, le modèle RLCG-B original est alors modifié avec un sous-circuit RL à la section 4.3. Les valeurs des nouveaux paramètres de circuit sont calculées de façon analytique. Des simulations numériques furent utilisées pour vérifier la précision des impédances série linéiques obtenues avec le modèle RLCG-B modifié. La différence obtenue étant minime, elle peut être négligée sans conséquences. Le modèle modifié sera donc utilisé comme référence pour la suite.

Dans la section 4.4, nous analysons l'impact de l'effet pelliculaire et des pertes diélectriques sur les modèles de circuit. Une façon de ne pas considérer l'effet pelliculaire dans la trace métallique est d'utiliser les valeurs de la résistance et de l'inductance séries dans les équations 4-10a et 4-10b. De la même façon pour les pertes diélectriques, deux moyens existent pour négliger leur impact. La première consiste à considérer le semi-conducteur comme un isolant idéal. Aucune contribution à la résistance série ne provient de la couche semi-conductrice. La seconde façon consiste à traiter le semi-conducteur comme un conducteur électrique parfait.

En combinant l'effet pelliculaire et l'impact des pertes diélectriques sur les paramètres de circuit, nous proposons cinq modèles simplifiés énoncés dans le tableau 4.1. Dans la section 4.5, les différences absolues entre les tensions de charge obtenues des modèles simplifiés et de la référence sont estimés dans le cas d'un exemple simple : une ligne avec résistance de source R_s et charge capacitive C_L. Les résultats numériques regroupés dans le tableau 4.5 montrent que les valeurs estimées fournissent une limite supérieure évidente pour la différence maximale entre les tensions de charge des modèles et de leur référence. En nous basant sur ces résultats estimés et pour une tolérance d'erreur donnée, nous pouvons juger de la pertinence des modèles simplifiés sans procéder à des simulations dans le domaine du temps.

0.5 Modélisation d'interconnexions couplées en configuration MIS

Le chapitre précédent portait sur la modélisation d'une interconnexion simple, une seule ligne MIS avec l'arrière-plan métallique utilisé comme retour de courant. Pour fins de comparaisons, ce chapitre porte sur l'étude d'une autre configuration, une interconnexion double couplée avec retour de courant sur une deux deux lignes (mode impair). Pour la simplicité, nous analysons seulement le mode impair de deux interconnexions en considérant la source et la charge balancées.

À la section 5.2, partant du modèle original RLCG-B pour une interconnexion simple proposé à la section 4.2 et d'autres modèles documentés, un modèle RLCG-B hybride est élaboré pour le mode impair de deux interconnexions couplées. Ce modèle hybride est ensuite modifié pour devenir un simple modèle RLC en considérant la couche semi-conductrice comme un conducteur électrique parfait et en négligeant l'impact de l'arrière-plan métallique sur le couplage des interconnexions. Dans la section 5.3, en comparant la constante de propagation complexe obtenue de l'équation 5.4 basée sur le modèle simple RLC avec le résultat prédit par une simulation sur ADS Momentum

(Agilent Technologies), on peut vérifier les conditions de validité du modèle RLC simple.

Pour les cas spécifiquement abordés dans ce chapitre, il est démontré que le modèle RLC simple (modèle à deux lignes simple) reproduit fidèlement le comportement électrique du monde impair de deux interconnexions couplées si l'espacement entre les deux lignes s_m est comparable à la largeur de la ligne w_m. Il semble que il y a une valeur seuil de s_m/w_m. En deçà de ce seuil, un fort couplage existe entre les deux interconnexions et des prédictions fiables peuvent être obtenues avec un modèle à deux lignes simple. Cependant, au-dessus du seuil, le couplage entre les deux interconnexions se révèle être faible et l'influence du plan de masse ne peut plus être négligée : le comportement du modèle à deux lignes simple s'éloigne alors du mode impair pour deux interconnexions. Dans certains cas avec la technologie à l'échelle du micron, en considérant une gaufre de silicium de 300 μm d'épaisseur, la valeur seuil de s_m/w_m est autour 8, ce qui correspond à un espacement de moins de 25 μm entre les deux interconnexions.

Parallèlement, nous trouvons que deux interconnexions couplées avec un faible couplage peuvent être considérées comme deux interconnexions simples sans couplage. Ce qui revient à dire qu'un modèle tel que le RLCG-G modifié, développé pour une interconnexion MIS simple peut également prédire le comportement électrique de deux interconnexions MIS couplées. De la même façon que pour le modèle à deux lignes, une valeur seuil de s_m/w_m est utilisée. Au-dessus de ce seuil, le couplage est faible et des prédictions de qualité peuvent être obtenues du modèle à une ligne. Basé sur des résultats numériques, la gamme valide de s_m/w_m pour le modèle à une ligne semble être partiellement recouverte par celui pour le modèle à deux lignes. Anisi, une valeur-seuil de s_m/w_m peut être placée pour les deux modèles. Donc, un modèle simple, soit à une

ou deux lignes, peut reproduire fidèlement les caractéristiques de propagation du mode impair de deux interconnexions couplées avec la valeur seuil de s_m/w_m .

0.6 Analyse du délai de propagation d'une ligne RC distribuée avec résistance de source R_S et charge capacitive C_L

Les derniers chapitres présentaient les considérations de modélisation des interconnexions en ITGE et analysaient la précision de ces modèles avec un regard à l'erreur temporelle de simulation. Le reste de la thèse porte sur l'analyse d'intégrité de signal. Dans ce chapitre, nous utilisons une simple ligne RC distribuée comme exemple pour étudier le délai temporel de propagation dans un circuit ITGE. Le chapitre suivant est en fait une étude de la divergence des temps de propagation pour des interconnexions couplées en configuration MIS.

La structure de notre modèle de circuit équivalent pour une ligne RC est montrée à la figure 6.1. Dans ce cas, des modèles discrets construits par itération (sections T ou π) ont été choisies pour modéliser des lignes RC. Dans la figure 6.1, la résistance de ligne R_w peut être obtenue en multipliant la résistance linéique de la ligne R_w^l (Ω/m) par la longueur de celle-ci d (m). De la même façon, la capacitance de la ligne C_w peut être obtenue en multipliant la capacité linéique C_w^l (F/m) par la longueur de la ligne d (m). Les figures 6.1a et 6.1b montrent une section T et une section π. Les figures 6.1c et 6.1d montrent des structures de n sections en T et de n section en π.

En utilisant les modèles de circuit équivalent appropriés, la réponse à une entrée échelon des lignes RC avec résistance de source R_S et charge capacitive C_L est analysée. Une évaluation asymptotique de forme d'onde à deux ou trois pôles est utilisée pour analyser le délai de propagation sur les lignes RC. Tel qu'anticipé, la précision des modèles discrets augmente avec le nombre de sections utilisées. En utilisant

l'information détaillée dans cette thèse, un utilisateur peut sélectionner un modèle de complexité minimale qui remplit les exigences de précision d'une approximation donnée. Dans certains cas, la structure de base d'une section (T ou π) exerce une influence significative sur la précision d'une certaine complexité de modèle. Cette thèse guide l'utilisateur vers le choix du modèle le plus efficace.

0.7 Analyse de la divergence de temps de propagation dans une configuration de circuit WSI

Tel que mentionné ci-haut, la divergence des temps de propagation est un autre sujet d'intérêt abordé dans cette thèse. Des applications haute vitesse développées avec des circuits utilisant la technologie ITGE à l'échelle de la gaufre («wafer scale integrated WSI ») imposent des spécifications excessivement sévères pour les interconnexions de grande longueur La divergence des temps de propagation devient très importante pour la conception de ces circuits « WSI ». Dans ce chapitre, une nouvelle méthode combinée est proposée pour réduire la divergence des temps de propagation. Elle s'énonce en trois volets :

- Des directions de propagation alternatives sont utilisées pour des signaux parallèles afin de réduire l'interférence électromagnétique entre lignes voisines.
- Un agencement de phase en zigzag est instauré pour les signaux voyageant dans la même direction afin de réduire davantage l'interférence entre les lignes.
- Des suiveurs et des inverseurs sont alternativement insérés en guise de répéteur dans chaque interconnexion pour compenser l'effet de l'interférence due aux cas de double polarité sur l'incertitude des délais de propagation

Pour des applications pratiques, nous recommandons premièrement l'utilisation d'inverseurs seulement afin de réduire la divergence des temps de propagation. Si celle-ci surpasse toujours les tolérances permises, l'usage alternatif de suiveurs comme répéteurs pour réduire l'effet de couplage sur la divergence des temps de propagation.

Les dimensions des suiveurs et inverseurs devraient être ajustées avec soin pour éviter d'obtenir des valeurs variables de divergence de temps de propagation, ce qui peut arriver avec des répéteurs présentant des caractéristiques différentes.

0.8 Conclusion

Cette thèse contribue à plusieurs aspects concernant les interconnexions. De façon à simplifier la modélisation de longues interconnexions, une nouvelle méthode est proposée pour estimer l'erreur temporelle induite par le modèle dans une simulation en utilisant les paramètres du circuit dans le domaine fréquentiel. Les résultats numériques démontrent qu'avec cette méthode, l'erreur engendrée par la modélisation est bornée supérieurement pour les simulations temporelles.

Pour la modélisation de longues interconnexions dans un circuit ITGE, une approche pratique a été proposée pour modéliser une interconnexion simple MIS. Pour une telle interconnexion avec une source et une charge typiques, nous avons démontré que l'erreur induite par la modélisation dans le domaine du temps est minime si l'effet pelliculaire dans la trace métallique est négligé, cependant que cette erreur est non-négligeable si on ne considère pas les pertes diélectriques. Il fut intéressant de constater que l'erreur de modélisation demeure petite si la couche semi-conductrice est traitée comme un conducteur électrique parfait. Ceci nous confirme que la couche semi-conductrice peut être traitée comme un plan de masse virtuel sans perte d'intégrité du signal pour les plages de fréquence et de résistivité qui nous intéressent. Dans cette thèse, les contributions de différentes sous-régions fréquentielles à l'erreur de modélisation totale dans le domaine du temps furent également étudiées. La plage de fréquence d'intérêt a été divisée en trois sous-régions en se basant sur la largeur de bande de la tension de charge.

En plus de présenter la modélisation d'une interconnexion simple et pour fins de comparaisons, l'étude d'une autre configuration, une interconnexion double couplée avec retour de courant sur une des deux lignes (mode impair) a également été réalisée. Quelques cas furent analysés et les résultats de simulation ont montré que la constante complexe de propagation varie grandement entre une ligne MIS simple et deux lignes MIS fortement couplées. Nous avons démontré qu'il était possible de construire un modèle équivalent efficace pour les deux interconnexions couplées. Ce modèle peut être à une ou deux lignes. Un seuil est utilisé pour déterminer si l'un ou l'autre des deux modèles reproduit adéquatement le comportement électrique des deux interconnexions couplées.

Dans cette thèse, deux volets traitent de l'intégrité de signal. Le premier concerne le délai de propagation dans des lignes RC avec impédance de source R_S et charge capacitive C_L dans un circuit ITGE. Nous avons étudié les conditions de validité d'une modélisation de ligne à base de sections RC discretes. Une méthode d'évaluation asymptotique de forme d'onde (« AWE ») a été élaborée pour analyser le délai de propagation sur des lignes RC. Un nombre restreint de pôles "AWE" furent utilisées pour éviter l'instabilité numérique, même si cela peut engendrer de l'imprécision dans le cas de circuits compliqués. La précision de modèles discrets avec un certain nombre de sections a été représentée dans un plan *r-c* normalisé, qui est valide pour différentes technologies. En utilisant l'information détaillée dans cette thèse, un utilisateur peut sélectionner un modèle de complexité minimale qui remplit les exigences de précision d'une approximation donnée. Dans certains cas, la structure de base d'une section (T ou π) exerce une influence significative sur la précision d'une certaine complexité de modèle. Cette thèse guide l'utilisateur vers le choix du modèle le plus efficace.

L'autre volet traitant de l'intégrité de signal porte sur la divergence des temps de propagation. Dans cette thèse, nous avons proposé une méthode combinée pour réduire ce paramètre. Des recommandations pratiques sont également mises de l'avant.

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a_1, a_2	incident waves [$V/\sqrt{\Omega}$]
a_1, a_2, a_k	coefficient functions in ABCD-matrix [no unit]
b_1, b_2	reflection waves [$V/\sqrt{\Omega}$]
b_1, b_2, b_k	coefficient functions in ABCD-matrix [no unit]
b_s	source wave [$V/\sqrt{\Omega}$]
c	velocity of light [m/s]
c	normalized capacitance [no unit]
C_i, C_s	shunt capacitance [F/m^2] (1D model)
C_L	load capacitance [F]
C_w	wire capacitance [F]
C_w^l	wire capacitance per unit length [F/m]
C, C_1	capacitance element [F]
C, C_1, C_2, C_{12}	capacitance per unit length [F/m]
C_{1a}, C_{2a}	capacitance per unit length [F/m]
C_{1b}, C_{2b}, C_{2ab}, C_{eff}	capacitance per unit length [F/m]
C_f, C_p	capacitance per unit length [F/m]
C_{g0}, C_{gab}, C_g	capacitance per unit length [F/m]
d	length of wire [m]
f_{h1}, f_{h2}	frequency [Hz]
f_s	sampling frequency [Hz]
G_s	shunt conductance [Simens] (1D model)
G, G_2	shunt conductance [Simens/m] (2D model)
G_n	normalized conductance [no unit]
H, H_{eq}	height [m]
$H(s)$, $H_{mod}(s)$, $H_{tl}(s)$	voltage transfer functions in s (=jω) domain [no unit]

$\widetilde{H}_{mod}(k)$, $\widetilde{H}_{tl}(k)$	samples of $H_{mod}(s)$, $H_{tl}(s)$ [no unit]
$[H]_{R_s}$	hybrid ABCD matrix
$[H]_t$, $[H]_{kt}$	hybrid ABCD matrix
$[H]_\pi$, $[H]_{k\pi}$	hybrid ABCD matrix
I_1, I_2	port currents [A]
L, L_w^l	inductance per unit length [H/m] (2D model)
L_w	wire inductance [H]
L_1, L_2, L_{12}	inductance per unit length [H/m] (2D model)
L_{1a}, L_{1b}, L_{1ab}, L_{eff}	inductance per unit length [H/m] (2D model)
L_i, L_m, L_s	inductance [H] (1D model)
N	total sampling points
n, n_1, n_2	index of sampling points
n	number of T- or π- sections
r	normalized resistance [no unit]
r_{eq}	equivalent radius [m]
R	resistance element [Ω]
R	resistance per unit length [Ω/m] (2D model)
R_1, R_2, R_{1a}, R_{1b}, R_{eff}	resistance per unit length [Ω/m] (2D model)
R_{2a}, R_{2b}, R_{2ab}	resistance per unit length [Ω/m] (2D model)
R_m, R_s	resistance [Ω] (1D model)
R_S	source resistance [Ω]
R_w	wire resistance [Ω]
R_w^l	wire resistance per unit length [Ω/m]
R_1	resistance [Ω]
R_n	normalized resistance [no unit]
s	complex frequency jω [rad/s]
s, s_m	spacing between two interconnects [m]

t_p , eff_t_p	thickness of metal or substrate layer [m] (p=i, m or s)
t_r	rise time [s]
t_{r10}, t_{r10_mod} , t_{r10_tl}	rise time [s]
t_{r50}, t_{r50_mod} , t_{r50_tl}	rise time [s]
t_{r90}, t_{r90_mod} , t_{r90_tl}	rise time [s]
t_s	sampling time interval [s]
T_f	propagation time [s]
$T_{0.9}$	threshold time [s]
V_{dd}	power supply voltage [V]
$v_L(t)$	load voltage [V]
$V_L(s)$	load voltage $v_L(t)$ in s (=jω) domain [V]
$v_{mod}(t)$, $v_{tl}(t)$	load voltage [V]
$\tilde{v}_{mod}(n)$, $\tilde{v}_{tl}(n)$	samples of load voltage [V]
$\tilde{V}_{mod}(k)$, $\tilde{V}_{tl}(k)$	Fourier transform of $\tilde{v}_{mod}(n)$, $\tilde{v}_{tl}(n)$ [V]
$v_s(t)$	source voltage [V]
$V_s(s)$	source voltage $v_s(t)$ in s (=jω) domain [V]
$\tilde{v}_s(n)$	sample of source voltage [V]
$\tilde{V}_s(k)$	discrete Fourier transform of $\tilde{v}_s(n)$ [V]
v_t	normalized threshold voltage [no unit]
V_t	threshold voltage [V]
V_1, V_2	port voltages [V]
w_m	width of interconnect [m]
w_p, w_{p1}, w_{p2}	width [m]
w_n, w_{n1}, w_{n2}	width [m]
eff_w_{mp}	effective width of interconnect [m] (p=i or s)
Y_L	load admittance [Simens]
Y_{shunt} , y_{shunt}	shunt admittance [Simens/m] (2D model)

Y_{shunt}^{d}	shunt admittance for a wire of length d [Simens]
$\{Y(j\omega)\}$	admittance matrix [Simens]
Y_c, Y_0	characteristic admittance [Simens]
Z_c, Z_0	characteristic impedance [Ω]
Z_{series}, z_{series}	series impedance per unit length [Ω/m] (2D model)
Z_{series}^{d}	series impedance for a wire of length d [Ω]
Z_{01}, Z_{02}	port impedances [Ω]
$\{Z(j\omega)\}$	impedance matrix [Ω]
z_{ym}, z_{ys}	complex wave impedance [Ω]
α, α_z	attenuation constant [Np/m]
β, β_z, β_0	phase constant or propagation constant [rad/m]
γ_{ym}, γ_{ys} γ_z, γ_{z0}	complex propagation constant [Np/m, rad/m]
γ_n	normalized complex propagation constant [Np, rad]
ω, ω_h	angular frequency [rad/s]
ω_h	normalized angular frequency [rad]
σ_m, σ_s	conductivity [Simens/m]
ρ_s	resistivity [Ω·m]
$\delta_v(t)$	absolute voltage difference [V]
$\tilde{\delta}_v(n)$	sample of $\delta_v(t)$ [V]
δ_{tr10}, δ_{tr10_mod}, δ_{tr10_tl}	absolute rise time difference [s]
δ_{tr50}, δ_{tr50_mod}, δ_{tr50_tl}	absolute rise time difference [s]
δ_{tr90}, δ_{tr90_mod}, δ_{tr90_tl}	absolute rise time difference [s]
Δ	upper limit of $\tilde{\delta}_v(n)$ [V]
Δ_I, Δ_{II}, Δ_{III}	contributions to Δ from sub-regions I, II and III [V]
Δt	time interval [s]
τ_{ED}	Elmore delay [s]

ε_0	permittivity of vacuum [F/m]
ε_{rp} , eff_ε_{rp}	relative dielectric constant (no unit) (p=i or s)
μ_0	permeability of vacuum [H/m]
ϕ_m, ϕ_s	electrical length [rad]
$tan\delta_l$	loss tangent [no unit]

LIST OF ABBREVIATIONS

AWE	*Asymptotic Waveform Evaluation*
CPW	*Coplanar Waveguides*
DC	*Direct Current*
DFT	*Discrete Fourier Transform*
EMC	*Electromagnetic Compatibility*
EMI	*Electromagnetic Interference*
IDFT	*Inverse Discrete Fourier Transform*
ILC	*Iterative Lumped Circuits*
LVDS	*Low Voltage Differential Signaling*
MC	*Method of Characteristics*
MIS	*Metal-Insulator-Semiconductor*
MoL	*Method of Lines*
RC	*Resistance-Capacitance*
RF	*Radio Frequency*
RL	*Resistance-Inductance*
RLC	*Resistance-Inductance-Capacitance*
RLCG	*Resistance-Inductance-Capacitance-Conductance*
TEM	*Transverse Electromagnetic*
TL	*Transmission Line*
VLSI	*Very Large Scale Integration*
WSI	*Wafer Scale Integration*
1D	*One-Dimensional*
2D	*Two-Dimensional*
ITGE	*Intégré à Très Grande Échelle*

CHAPTER 1

INTRODUCTION

1.1 Introduction

The driving force behind the rapid growth of very large scale integrated (VLSI) technology has been the constant reduction of the minimum feature size of VLSI devices [1,2]. Such continuous evolution of VLSI devices has strong impacts on the design of interconnects. Firstly, the device density on integrated circuits grows dramatically with the decrease in the minimum feature size, while the size of a chip is kept constant, or tends to increase. Thus, on-chip interconnects become more and more crowded. Secondly, since devices tend to be larger while operating at higher speeds, the electrical length of on-chip interconnects increases with the frequency. Therefore, signal integrity analysis of long interconnects has become a dominant factor in determining system performance. At last, the dissipated power per area increases with the logic density. Thus, voltage drops and current densities of interconnect go up and become dominant factors in the design of VLSI chips.

Since the analysis of the electrical behavior of interconnects [3-9] in VLSI circuits and power supply networks is a very broad topic, we have focused on the electrical modeling of long interconnects. Related topics are signal integrity analysis, power dissipation optimization, electromagnetic compatibility (EMC) and electromagnetic interference (EMI) considerations. Besides the electrical modeling of long interconnects, this thesis mainly deals with signal integrity analysis.

1.2 Objectives of this thesis

The objectives of this thesis are rooted in two industrial research projects in which we were involved. One project was a study on propagation time delay analysis of interconnects in VLSI circuits. The other project was an analysis of propagation time delay difference (skew) of high-speed interconnects in wafer scale integrated (WSI) circuits. As illustrated in Figure 1.1, the above two projects can be divided into several tasks: modeling of interconnects (Task A), signal integrity analysis (Task B), power supply network design (Task C), power distribution network design (Task D), EMC/EMI considerations (Task E) and so on. All these tasks are related to each other and are essential parts of typical industrial projects. For example, signal integrity analysis (Task B) and design of power supply and distribution (Tasks C & D) networks relies on the available interconnect models (Task A), while selection of simplified models for interconnects (Task A) is needed to evaluate signal integrity (Task B) of circuits including interconnects with proper power supply and distribution networks (Tasks C & D). Here, power supply networks refer to networks delivering power from outside of VLSI circuits to functional blocks on chips, while power distribution networks refer to on-chip power and ground buses feeding power to all the gates in VLSI circuits.

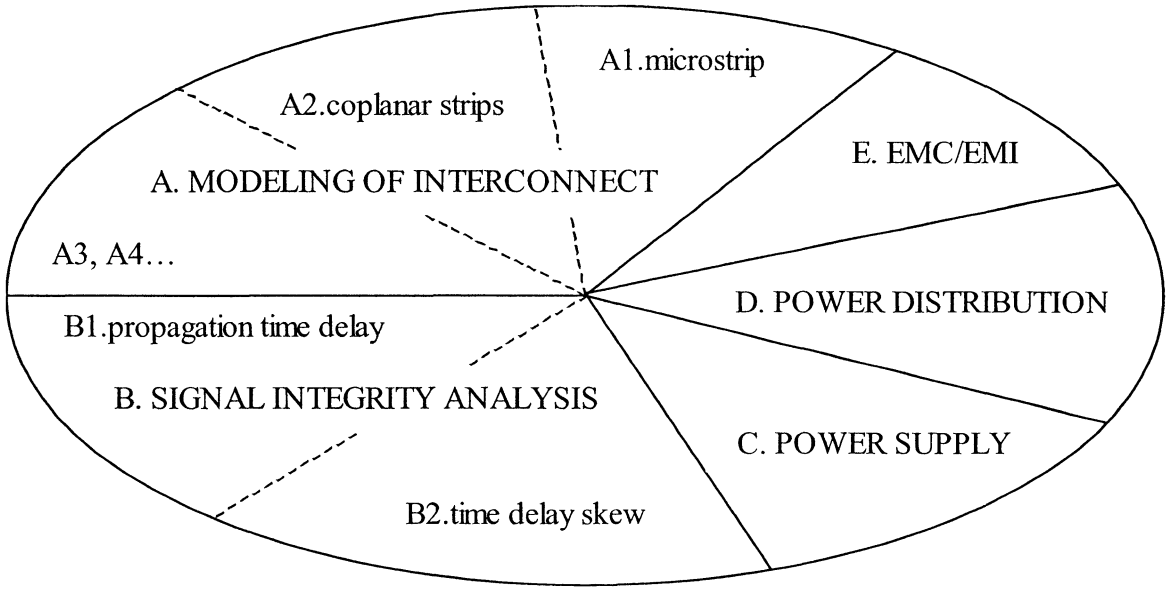


Figure 1.1: Topics related to VLSI/WSI circuit design

In this thesis, there are three objectives: modeling of long interconnects in the metal-insulator-semiconductor (MIS) configuration, developing a method to simplify modeling of long interconnects, and analyzing signal integrity of networks including long interconnects. The first and second objectives belong to Task A, while the third objective is related to Task B. Similarly to the multiple tasks above, these three objectives are also related to each other. Modeling of long interconnects can be regarded as a fundamental element for the kind of work presented in this thesis. Without proper models for interconnects, signal integrity (propagation time delay and propagation time skew) of networks including interconnects cannot be analyzed. Moreover, assessing simplified models for interconnects requires a good understanding of signal integrity of networks including interconnects.

As mentioned above, the premier objective of this thesis is modeling of long interconnects in the MIS configuration. The purpose of modeling interconnects in the MIS configuration is to obtain the distributed equivalent circuit parameters for interconnects. In this thesis, we first focus on the modeling of a single interconnect in

the MIS configuration, where the back plane is used as the current returning path. Analysis of such a simple topology can help us understand the propagation mechanism. This interconnect topology has been investigated extensively by many authors [10-16] in the past. Based on the existing literature [10][14,15][17,18], we propose a new resistance-inductance-capacitance-conductance (RLCG) model using two values of effective width for the metal strip forming interconnect. For comparison, the premier objective also includes study of another interconnect topology: coupled interconnects in the MIS configuration, where one of the coupled interconnects called local ground wire is used as the current returning path. Based on the existing literature [19,20], we use a hybrid RLCG model to illustrate the difference between these two interconnect topologies.

The second objective of this thesis is developing a method to simplify modeling of long interconnects. Based on the distributed equivalent circuit parameters, equivalent circuit models can be constructed by implementing circuit techniques such as the iterative lumped circuits (ILC) [21] and the method of characteristics (MC) [21]. The ILC technique cascades T- or π- type of lumped circuit components to model interconnects. The MC technique cascades MC cells to model interconnect, where an MC cell is composed of a lossless transmission line segment with a series resistance and a shunt conductance at each end. These equivalent circuit models can be directly used in most circuit simulation software and tools such as SPICE. However, they are often complicated and time-and-memory consuming. In order to use simple equivalent circuit models, we need to determine the conditions under which the skin effect in the metal strip or the dielectric losses need to be considered in these equivalent circuit models. In this thesis, we propose a novel method to evaluate the impact of modeling accuracy on the simulation error. Based on this method, we can estimate the simulation errors among different equivalent circuit models. Thus, for a given error tolerance, once distributed equivalent circuit parameters are obtained, circuit techniques can be implemented in circuit simulation with proper simplifications.

The third objective of this thesis is to investigate approaches to perform signal integrity analysis of networks including interconnects. A signal with a good integrity has digital levels at required voltage levels at required times. Here, we first study the propagation time delay for distributed resistance-capacitance (RC) wires with source resistance R_S and load capacitance C_L. The asymptotic waveform evaluation (AWE) [22] method is used to obtain the propagation time delay. Then, we investigate the propagation time skew with coupled interconnects in the MIS configuration. The minimal propagation time skew is obtained by the combined use of methods at hardware and software levels.

1.3 Organization of this thesis

The thesis is divided into eight chapters. The first is an introduction, and the second reviews recent work on modeling of interconnects and on signal integrity analysis. The third chapter presents a method of estimating a bound on time-domain simulation error in the frequency domain.

The fourth and fifth chapters are related to modeling of interconnects. In the fourth chapter, we analyze a single interconnect in the MIS configuration, where the back plane is used as the current returning path. We propose two values of effective width for the physical metal strip. Based on the literature [10][14,15][17,18], an original RLCG-B model with five circuit parameters is proposed and then modified into a model with seven frequency invariant circuit parameters. In this chapter, we also analyze five simplified models for practical applications, which either neglect the skin effect or the dielectric losses. Using our method described in the third chapter, we estimate the time-domain simulation error based on five simplified frequency domain models. This analysis is used to formulate recommendation on which simplified model is appropriate. For comparison, in the fifth chapter, we analyze another interconnect topology: coupled interconnects in the MIS configuration, where one of the interconnects is used as the

current returning path. Based on the literature [19,20], we use a hybrid RLCG-B model to illustrate the difference between these two MIS interconnect topologies.

Chapters six and seven are related to signal integrity analysis. In the sixth chapter, we investigate the propagation time delay for distributed RC wires with source resistance R_S and load capacitance C_L. AWE method is used to obtain the propagation time delay. In the seventh chapter, we analyze the propagation time skew with coupled interconnects in the MIS configuration. The minimal propagation time skew is obtained by the combined use of methods at both hardware and software levels.

Finally in Chapter eight, conclusions and recommendations for future research work are provided.

1.4 Main contributions of this thesis

The main contributions of this thesis are:

- the introduction and validation of a novel general method [23] to estimate the time-domain model-induced simulation error using frequency domain circuit parameters;
- the introduction and validation of new combined methods [24] to reduce propagation time skew among parallel interconnects in WSI circuits;
- the introduction of a normalized rc-plane [25] to analyze the propagation time delays with RC wires for different technologies;
- a practical approach [23] to efficiently model a single MIS interconnect in VLSI circuits;
- a comparison on propagation characteristics [26] between single and coupled MIS interconnect topologies in VLSI circuits to illustrate the possibility of constructing an efficient model for coupled MIS interconnects.

CHAPTER 2

REVIEW OF LITERATURE

Analysis of the electrical behavior of interconnects [3-9][27-32] in VLSI circuits and power supply networks is a very broad topic. This thesis focuses on the electrical modeling of long interconnects and signal integrity analysis.

2.1 Modeling of interconnects

Effective and efficient modeling of on-chip interconnections in modern VLSI circuits has become extremely important because interconnects contribute to a significant fraction of propagation delay in high-speed designs. There are several topologies of interest for interconnects in the MIS configuration as shown in Figure 2.1. Figure 2.1a shows a single interconnect in the MIS configuration. Coupled interconnects can be coplanar strips as shown in Figure 2.1b, where one of the strips is used as the current return path. A more complicated structure has latch-up prevention function with contacts between the power distribution network and the silicon substrate as displayed in Figure 2.1c. This structure can be seen as a cross section along line AA' of the structure shown in Figure 2.1d, representing a long signal trace running across inter-digitated power/ground traces. A lot of work has been done on the modeling of such interconnects in the MIS configuration.

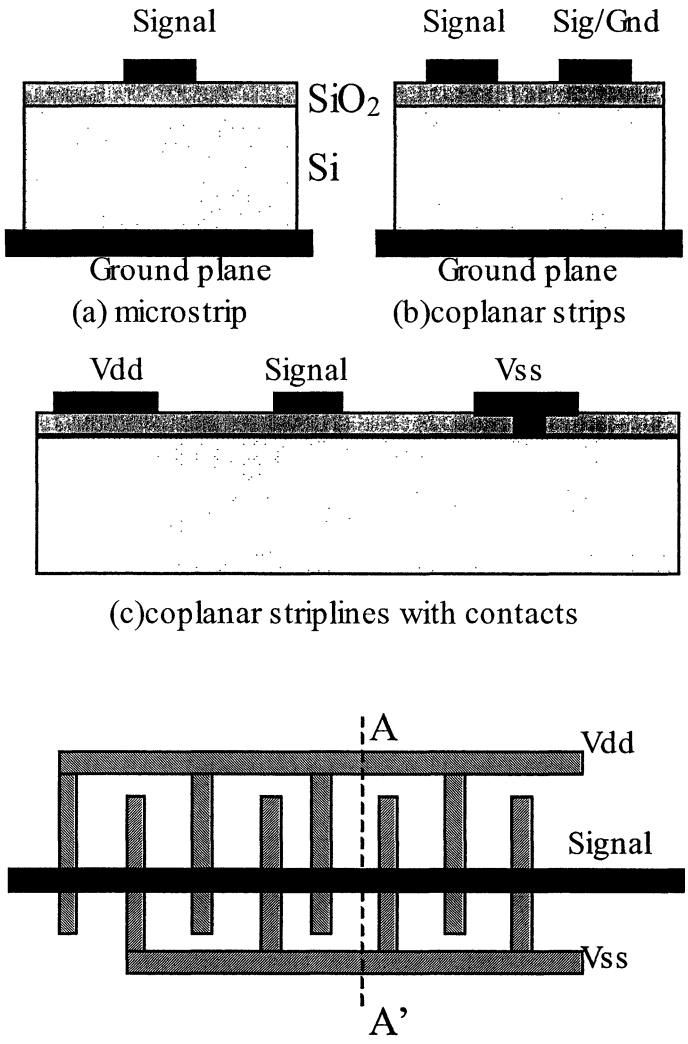


Figure 2.1: Topologies of interconnects in VLSI circuits

2.1.1 Microstrip

The simplest topology of interconnect in the MIS configuration is the microstrip shown in Figure 2.1a. Early study of microstrip in the MIS configuration can be dated back to 1960's. In 1965, Hyltin [33] investigated the possibility of utilizing microstrip transmission lines as interconnects of devices on semiconductor dielectrics. He showed that the loss of the microstrip transmission line on a common substrate of both semi-insulating gallium arsenide (GaAs) and silicon (Si), with resistivity greater than 1000Ω·cm, was sufficiently low to implement efficient interconnects among devices.

In 1967, Guckel *et al.* [34] studied the fundamental mode of a 1D parallel–plate waveguide with a two-layer loading medium, a conducting semiconductor substrate and a relatively thin dielectric. They predicted the existence of slow-wave phenomena but did not consider the fringing fields. Based on such parallel-plate model, Hasegawa *et al.* [10] extensively studied the fundamental TM_0 mode of MIS transmission lines. They predicted the existence of three types of behavior for the fundamental mode: skin effect, slow-wave and quasi-TEM, and illustrated the conditions for the appearance of each type of behavior in the resistivity-frequency plane. Moreover, they discussed the propagation mechanism, constructed 2D distributed equivalent circuit model for each case, and analyzed the fringing field effect for the slow-wave mode.

2.1.2 Coplanar strips and coplanar striplines

A slightly complicated topology consists of coplanar strips as shown in Figure 2.1b, where one of the strips is used as the current return path. A corresponding symmetric structure would be a coplanar stripline with power/ground lines on both sides of a signal line. As expected, the slow-wave phenomenon was also found in such structures.

In 1977, Hasegawa and Okizaki [35] experimentally studied the slow-wave effect of MIS and Schottky coplanar striplines on GaAs substrates by using a quasi-TEM (quasi-static) analysis. The reported measurement illustrated both the slow-wave factor and the characteristic impedance as functions of frequency. In 1981, Seki and Hasegawa [36] investigated a crosstie slow-wave CPW on semi-insulating GaAs substrates by using a quasi-TEM analysis. Their experimental results showed that the attenuation coefficient was frequency-dependent. In 1987, Kwon *et al.* [37] presented a simple quasi-TEM analysis of "slow-wave" mode propagation on micron-size coplanar MIS transmission lines on heavily doped semiconductors. Excellent agreement was found between theoretical results with measurements on four such structures at frequencies from 1.0 to 12.4 GHz. They included the conductance loss of the metal besides the dielectric losses of semiconductor substrate, and showed that metal losses of the experimental transmission lines dominate the attenuation at frequencies below 25 GHz and are still significant at frequencies between 25 and 100 GHz.

Besides quasi-TEM (quasi-static) analysis, full-wave techniques are also used to investigate slow-wave phenomenon in MIS CPW. In 1983, Fukuoka *et al.* [38] analyzed the slow-wave characteristics of an MIS CPW using two different full-wave methods: mode-matching and spectral-domain techniques. These experimental values are in good agreement with theoretical results predicted by using two full-wave methods. In 1984, Sorrentino *et al.* [39] extensively investigated the characteristics of MIS coplanar waveguides (CPW) for monolithic microwave circuits by using a full-wave method: the mode-matching technique.

2.1.3 Other interconnect topologies

Microstrip, coplanar strips and coplanar striplines can be regarded as the conventional topologies in the MIS configuration. Besides these conventional topologies in the MIS configuration, where metal strip lines are placed on two substrate layers: insulator and

semiconductor, there are more complicated cases similar to the one shown in Figures 2.1c and 2.1d. Such kinds of complicated topologies are due to two particular features present in modern VLSI circuit technologies. One feature is that there may be buried layers besides the insulator layer and the semiconductor layer. The other particular feature is that the ground lines for the coplanar lines are normally connected to semiconductor substrate through ohmic contacts with a certain pitch along the interconnects.

(1) Buried layers

A buried layer of interest in the MIS configuration is a Scottky-barrier contact. Slow-wave mode was found in a microstrip transmission line with the Scottky-barrier contact between the strip metal layer and the lossy semiconductor layer. There is an extra depletion substrate layer in such complicated MIS configuration. The depletion layer results from the Scottky-barrier contact and its thickness strongly depends on the applied voltage along the microstrip transmission line. In 1972, Jaffe [40] described a short high-frequency variable delay line and showed that it was possible to vary the phase velocity over an 8:1 ratio from approximately c/50 to c/6 by using the depletion layer, where c is the velocity of light in vacuum. In 1975, Hughes and White [41] showed that MIS and Scottky-barrier microstrip structures having substrate resistivities within a certain range propagate slow waves with phase velocities that are dependent upon the instantaneous voltage at each point along the line. Their experimental measurements for such complicated MIS microstrip structure also confirmed the frequency dependence of the attenuation constant as predicted. In 1976, Jager [42] extensively investigated a Schottky-contact microstrip line in the complicated MIS configuration, where the depletion layer depended strongly on the bias voltage. They illustrated that the nonlinear propagation behavior resulted from the voltage-dependent capacitance per unit length of such lines.

As to coplanar stripline with a Schottky-contact, its slow-wave propagation characteristics was investigated by Seguinot *et al.* [43] in 1984. They proposed an original two-dimensional (2D) analytical model. Some of the model's parameters were determined by semi-empirical considerations.

An interconnect topology in the MIS configuration including buried layers can be more complicated. For example, in 1990, Yuan *et al.* [13] analyzed a multilayer structure including buried layers, epi-layers, and p-n junction space-charge capacitance. They proposed a 2D analytical lossy and dispersive interconnect model for integrated circuit simulation. SPICE simulation of their model showed good agreement with measurements. In 1994, Wu *et al.* [44] proposed a method-of-lines (MoL) based technique to efficiently analyze the propagation characteristics of such kind of planar circuits including segmented layers and miniature topologies, Their approach was able to not only handle very narrow strips/very large slots topologies, but also simulate bilaterally unbounded structures with possible segmented multilayers.

The electrical performance of an interconnect topology including buried layers can be very different from one excluding buried layers. In 1999, Tony *et al.* [16] investigated a multilayer structure with an interface layer between the insulator layer and the semiconductor layer. The interface layer was of the semiconductor permittivity but infinite resistivity because this region was depleted of carriers. For a typical MIS geometry with the slow-wave mode of operation, they demonstrated that ignoring the depletion region leads to totally erroneous results in estimating attenuation constant α with error up to 15%, phase constant β with error up to 3% and characteristic impedance Z_C with error up to 90%. All these differences were analyzed in the frequency domain without considering source impedance Z_S and load Z_L. However, the impact of these frequency-domain errors needs to be investigated in the time domain, because the time-domain simulation errors may still be tolerated with interconnect of short length at low frequency of interest.

(2) Ohmic contacts

Another feature complicating interconnect topologies is that the ground lines for the coplanar lines are normally connected to semiconductor substrate through ohmic contacts with a certain pitch along the interconnects. Zaage and Groteluschen [45] experimentally determined the characteristic impedance Z_C and the propagation constant γ_z of such interconnect geometry. They illustrated that the transmission behavior of these interconnects with contacts on conductive substrates strongly depended on the line geometry, the resistivity of the substrate material and the frequency of the applied signals.

2.1.4 Modeling of microstrip and coplanar strips in the MIS configuration

In this thesis, we focus on a single interconnect in the MIS configuration as shown in Figure 2.1a, for such a simple case can help us understand the fundamental propagation mechanism in the MIS configuration. We also study the equivalent circuit model for coupled interconnects in the MIS configuration as shown in Figure 2.1b, where one of the coupled interconnects is used as the current return path other than the ground plane.

Though many models are available for microstrip and coplanar strips, some are theoretical, and some experimental. Practical and efficient models are needed so that these models can be directly embedded in time domain simulators such as SPICE or ADS. Regarding MIS interconnects as lossy waveguides, some authors studied more general models. In 1986, Brews [11] suggested a general 2D resistance-inductance-capacitance-conductance (RLCG) transmission line model for lossy waveguide interconnects in VLSI circuits. The distributed circuit parameters were determined by field integrations from the solution of quasi-static problems.

In 1988, Lawton *et al.* [12] also investigated the two-layer dielectric microstrip line structure and proposed a general 2D equivalent circuit model, which allows for the losses in dielectric layers and the skin effect in metallization. Unlike Brews' paper [11], experimental results were used to determine the values of equivalent circuit parameters.

In 1992, Tuncer *et al.* [14] considered the field spreading and suggested a unique 2D quasi-static analytical model of a microstrip over a semiconductor layer. By using the transverse resonant technique, this model included the contribution of semiconductor layer to the series impedance per unit length of microstrip. A distance parameter k, a measure of how much the fields spread before reaching the ground plane, was selected by matching their numerical results with those obtained from Wheeler's equations [46]. They demonstrated that the agreement of complex propagation constants between the quasi-static and full-wave calculations was excellent almost over four orders of magnitude of frequency and conductivity. Only at the very highest frequency and conductivity was there a noticeable difference ($\leq$20%) for the slow-wave factor β/β_0. Here, the structure consists of a 160-μm wide microstrip over a 1-μm thick silicon dioxide layer and on a 250-μm thick silicon layer.

In fact, at the highest frequency of interest with semiconductor of high conductivity (e.g. 10^3 S/cm), interconnects in the MIS configuration normally operate in skin-effect mode. Both the electric and magnetic fields are usually confined in a small area near the insulator/semiconductor interface, because the skin depth of semiconductor will be much less than the thickness of the semiconductor. Thus, for the shunt elements of a RLCG model, the associated lossy element of low impedance is in series with high impedance insulator layer and can be omitted. Therefore, the very lossy semiconductor can be treated as an ideal ground plane. However, this is only true for the shunt elements (capacitance and conductance). As to the series elements, there is a significant contribution from the boundary layer and the lossy semiconductor really acts as a ground plane of poor conductivity compared to good conductors such as aluminum (*Al*) and

copper (*Cu*). The series resistance of the transmission line will significantly increase due to the losses in the semiconductor. The series inductance will dramatically decrease with the decrease of the magnetic flux. By applying a complex image theory [47], Weisshaar *et al.* [48] approximately replaced the lossy substrate with an image plane located at a complex distance from the insulator/semiconductor interface. By using a closed-form expression for the external inductance per-unit-length of an ideal microstrip line given by [49], the series inductance and resistance parameters can be determined by original Eqs.3 and 4 in [48]. Proposed closed-form solutions were shown to be in good agreement with electromagnetic field solutions.

In VLSI circuits, especially for deep sub-micron technologies, the width of metal strips is normally much smaller than 160-μm. For narrow interconnects operating with low loss semiconductor of resistivity above 1 Ω·cm, and with highest frequency of interest up to 10 GHz, conductance loss is much larger than the semiconductor losses. In such situation, quasi-static models such as Williams' [15] integral model are still very useful in practical applications. Based on the Brews' method [11], Williams [15] investigated the fundamental TM_0 mode of 1D MIS transmission line. He developed closed-form expressions for 1D distributed circuit parameters, compared his results with those of full-wave calculations, and explored the limitations of his expressions. He also showed that in certain fairly common circumstances, the TM_0 mode of propagation becomes so lossy that it could no longer be considered to be a fundamental or dominant propagation mode. As mentioned by Wee *et al.* [19], Williams illustrated that the substrate effect on the resistance weakened as the center conductor width shrank, and that the fringing fields could not be ignored when the width of strip was much smaller than the thickness of the lossy substrate. Under these conditions, the 1D MIS results could not be used for practical design.

In order to construct effective and efficient interconnect models in the MIS configuration, a lot of authors investigated the frequency-dependent parameters of

models for microstrip and coplanar striplines. Based on numerical results obtained from solutions of integral equations, other numerical results and theoretical considerations, Djordjevic and Sarkar [50] presented closed-form formulas of frequency-dependent resistance and inductance per unit length for microstrip and coplanar striplines.

In 1994, Klingbeil and Heinrich [51] calculated CPW per unit length resistance and inductance by using a quasi-static mode-matching approach. Such an approach is of particular interest when considering the frequency range between the skin effect and the direct current (DC) limit, where none of these two approximations give realistic results.

In 1998, Wee *et al.* [19] proposed a new analytic model for interconnect characteristics including the substrate as a current return path, since the dielectric losses can be neglected at low frequency, while they have a prevalent effect on the characteristics of interconnects at high frequency. They also mentioned that the dielectric effect on the resistance was negligible if the width of the signal interconnect lines was scaled down below 1 μm for given frequency ranges (1 MHz ~ 10 GHz) and that the difference between the dc-based model and proposed model was negligible.

In 2000, Zheng et al. [20] presented a CAD-oriented equivalent circuit models for single and coupled interconnects on lossy silicon substrate. Their models were based on an efficient quasi-static spectral domain approach [52] and considered the frequency-dependent behavior of the interconnect structure.

Based on the literature, in this thesis, we investigate the frequency-dependent parameters of a 2D analytical circuit model for single interconnect in the MIS configuration. For comparison, a 2D analytical circuit model for the odd-mode of two coupled interconnects is also studied.

Once the frequency-dependent parameters of models are obtained for microstrip and coplanar striplines, models with frequency invariant parameters can be constructed. In 1994, Yu *et al.* [53] proposed circuit models of transmission line segments considering skin effect and frequency-dependent dielectric losses, treating the ordinary RLCG line as a special case. The skin effect was represented as the impedance of a resistance-inductance (RL) ladder, and the complex dielectric parameter as the admittance of an RC ladder. In this thesis, RL ladders have been implemented to obtain frequency invariant parameters of the 2D analytical model for a single interconnect in the MIS configuration.

2.2 Simulation error vs. modeling accuracy

Once the distributed equivalent circuit parameters are obtained, circuit models can be constructed by using several circuit techniques such as ILC and MC. These circuit models can be directly embedded into common circuit simulators and RF(radio-frequency)/microwave design tools such as Agilent Technologies ADS [54]. There may be thousands of interconnects in a circuit. Complicated models for interconnects are time-and-memory consuming to use, while simple models may lead to larger simulation errors. A general method is required to estimate the simulation error between a model and a reference. Based on this method, we can determine if simple models are sufficient to describe single and coupled interconnect topologies. Moreover, by investigating the impact of modeling accuracy on the time-domain simulation error, we can also determine if smaller or larger variations on complex propagation constant γ_z and complex characteristic impedance Z_C of microstrip and coplanar striplines can be tolerated.

In this thesis, we propose a novel method of estimating the time-domain simulation error that corresponds to modeling errors in frequency domain. For example, a single transmission line network with source resistance R_S and load capacitance C_L is used to

describe and illustrate our method. Such method is based on the spectrum of a voltage pulse source, and the difference between the voltage transfer function of a simplified model and that of a reference. As performed in Gupta *et al.*'s paper [21], we represent reference transmission lines with ILC models. The validation of this time-domain simulation error bound with VLSI interconnects is demonstrated with relevant networks. Although our method is introduced with a two-port network with a simple transmission line, it can be applied to other more complicated networks, such as a multi-port network including coupled interconnects.

2.3 Signal integrity analysis – propagation time delay

Practically in VLSI circuits, the purpose of interconnect modeling is to analyze signal integrity issues such as propagation time delays, undershoot, overshoot and so on. A single distributed RC wire is used as an example to investigate the propagation time delay in VLSI circuits. The RC model for a single line in VLSI circuits has been extensively studied, since it is the simplest model that allows characterizing delays of lossy wires with a reasonable accuracy. Antinone & Brown [55] studied long polysilicon lines as RC transmission lines. More than 10 T-structures were utilized to calculate the characteristics of transmission lines in the frequency domain. The step response at the output of an open terminal, with different numbers of T-sections, was also calculated and compared with theoretical results. Their paper clearly shows that as the number of T-sections increases, the model accuracy improves. It also demonstrates that lumped RC ladder networks containing a finite number of stages can be used to successfully model long polysilicon lines in integrated circuits.

Rao [56] analyzed time delay of a finite length distributed RC line with a capacitive load C_L. He calculated the step response of the system in the Laplace domain, and obtained some of the common threshold-crossing times at the output load C_L. Models containing 1π- and 2π- sections were used to estimate propagation times, which were

compared with those produced by distributed model. The load capacitance C_L was normalized to the wire capacitance C_w.

In VLSI circuits, signals propagate between gates and buffer stages. Each net is characterized by several parameters such as the wire length and the fanout. Long wires and large fanout require strong buffers with low output resistance R_S. In addition to load capacitance C_L and output resistance R_S, interconnect delays are also dependent on the logic voltage threshold V_t of the gates.

By using the normalization method, four variables: source resistance R_S, wire resistance R_w, load capacitance C_L and wire capacitance C_w, can be reduced to two normalized parameters r ($=R_w/R_S$) and c ($=C_w/C_L$). For generality, the logic voltage threshold V_t is also normalized by the power supply voltage V_{dd}, which varies with technology. Thus, the propagation time delays are normalized by a time constant τ_0 ($=R_S*C_L$) for a step voltage source, and are valid for different technologies [1]. We focus on the determination of the minimum number of T- or π- sections required to predict propagation time delay within a given error tolerance. Therefore, independently of the technology used, a proper structure can be selected to model wires with sufficient accuracy as illustrated in [25].

2.4 Signal integrity analysis – propagation time skew

As mentioned in [57], high-speed applications implemented with WSI circuits impose stringent requirements on very long interconnects. Signal propagation on extremely long lossy interconnects is more susceptible to problems with transmission line effects, such as loss of signal integrity, EMI, crosstalk, reflections, and ground bounce. Consequently, propagation time delay skew is an important issue in WSI circuit design. Existing methods to reduce the propagation time skew can be implemented at "software" level, "hardware" level, or both as mentioned in [58]. Here, means of reducing crosstalk called

"software" methods when we only change how the interconnects are used, as opposed to how they are physically implemented ("hardware" methods).

One method is to insert programmable delays. Such method corrects excessive delay skew. For example, Takashi Sato *et al.* [59] described a bit-to-bit skew compensation technique that eliminated the incongruent skew among bus signals. A new multi-output controlled delay circuit was proposed to control the transmission timing of every data bit. Balakrishnan *et al.* [60] explored a control logic system for reducing skew in the parallel transmission of digital data slices (a series of data). Here, skew within a particular transmission path was compensated by providing a controlled delay path for the clock signal in each device within that path. Okajima *et al.* [61] proposed a skew-reduction circuit by the method of adjusting phases of rising edges and falling edges of signals.

Another method is to insert intentional time delays. This method leads to distributing, over time, current pulses in power distribution feed lines. Thus, it reduces switching noise due to ground bounce. Intentional time skew also reduces crosstalk among neighbor wires and minimizes the unpredictable propagation time skew.

The above two methods to reduce propagation time skew are at "software" level. At "hardware" level, at first, shield lines can be disposed around active lines. Such method reduces crosstalk among neighbor wires. For example, Tan *et al.* [62] proposed an improved signal line routing scheme, which includes static and dynamic signal lines disposed in parallel to each other, wherein at least one static signal line is disposed adjacent to one dynamic signal line. Shenoy *et al.* [63] investigated a circuit arrangement for a flip chip utilizing fixed potential shield traces between various signal traces in a redistribution layer to decrease coupling impedances and crosstalk within the layer. Takahashi *et al.* [64] offered a new circuit that reduces or removes crosstalk with a method that does not exert influence on improvements in miniaturization and the degree

of integration. Their crosstalk prevention circuit includes master and slave clock lines besides signal lines.

Another method at "hardware" level is to insert repeaters for long interconnects. The size, type and position of these repeaters have impact on the propagation time skew. For example, X.-N. Zhang [65] proposed the usage of alternating inverters for capacitive coupling reduction in transmission lines. Pai *et al.* [66] investigated the routing of repeaters in very large scale integrated (VLSI) circuits.

Besides the methods mentioned above, other methods are also found in the literature. For example, Ghoshal and Shymalindu [67] proposed a crosstalk-reduction method, which changes the amplitudes of signals on neighbor wires. Schmidt Jr. *et al.* [68] disclosed a module interconnection system, which minimizes electronic signal propagation delays. The module interconnection system included two groups of connectors. These two groups were arranged at the top and bottom sides of a board, respectively, and the connectors in one group are vertical to those in the other group.

Practically, method at "hardware" level can be implemented with methods at "software" levels. Based on existing methods, in this thesis, we propose a combination of methods to reduce the propagation time skew among parallel bus interconnects. Like others, we insert repeaters to suppress crosstalk among neighbor wires and use intentional skew or forced skew to avoid simultaneously switching among neighbor wires.

2.5 Summary

This chapter has reviewed modeling of interconnects in the MIS configuration, estimation of simulation error and analysis of signal integrity. In next chapter, we

propose a general method of estimating the simulation error among different circuit models.

CHAPTER 3

METHOD OF ESTIMATING TIME-DOMAIN SIMULATION ERRORS FROM ERRORS IN THE FREQUENCY DOMAIN RESPONSE

3.1 Introduction

Effective and efficient modeling of on-chip interconnections in modern VLSI circuits has become extremely important, because interconnects contribute to a significant fraction of propagation delay in high-speed interconnect designs. Many authors [10][12][14,15] investigated the distributed equivalent circuit models for interconnects in the MIS configuration. Based on those distributed equivalent circuit parameters, proper simple circuit models can then be constructed, so that they can be directly embedded into commercial software and tools such as SPICE for circuit simulations in the time domain. A criterion is needed to determine if these simple circuit models are appropriate.

Most of the literature [10][12][14,15] on this topic uses validation in the frequency domain by performing comparison of complex propagation constant γ_z, complex characteristic impedance Z_C, impedance and admittance matrices $\{Z(j\omega)\}$ and $\{Y(j\omega)\}$ of the interconnect models. Here, ω is the angular frequency. These quantities are easily obtained from the per-unit-length (p.u.l.) parameters of equivalent interconnect models.

Although comparison in the frequency domain is relevant, it is most useful in the context of radio-frequency (RF) applications. In VLSI circuits, the interest is rather on time-domain-related issues such as propagation time delay, waveform distortion, etc. These quantities depend on the interconnect's impulse response and the applied stimulus in the time domain, however, they cannot be readily computed from the swept-frequency p.u.l. parameters. Validation of models in the frequency domain could be too demanding

at high frequency, where accuracy may not be needed to achieve the necessary accuracy in the time domain. It was conjectured that some of the quantities of interest in the time domain could be estimated by approximate processing of the p.u.l. parameters without having to run a time domain simulation of the circuit of interest. If this were possible, considerable savings in terms of simulation efforts would be made. In view of the general objective of this thesis, which focuses on validation of interconnect models, such savings could be made in various model validation/comparisons if time domain errors introduced with proposed equivalent models could be estimated with simplified computations. Thus, a method is needed to assess accuracy of models based on time-domain response.

In this chapter, we propose a general method of estimating the worst-case time-domain error by using frequency domain characteristics of interconnects. This method is based on the spectrum of a voltage pulse source, and the difference between the voltage transfer function of a proposed model and that of a reference. The time-domain simulation error upper limit with VLSI interconnects is demonstrated with a simple example, that is, a simple two-port network of distributed RC transmission line with source resistance R_S and load capacitance C_L.

3.2 Derivation of a general formula for the worst-case time-domain error

In this section, a general formula for the worst-case time-domain error is derived by using the frequency domain characteristics of interconnects. This is a general method, because it is not focused on any specific interconnect model, and because it is not only applicable to two-port networks, but also to multi-port networks.

3.2.1 Definition of time-domain error

Typically, as shown in Figure 3.1, a transmission line (TL) is driven by a source of impedance Z_S and has a load of impedance Z_L. In circuit simulations, a model is used to replace the transmission line. The absolute difference of load voltages between the circuits based on the model and the actual TL, in time domain, is defined as the model-induced simulation error. This simulation error depends not only on the parameters of the transmission line, but also on the voltage source waveform, the source impedance Z_S and load impedance Z_L.

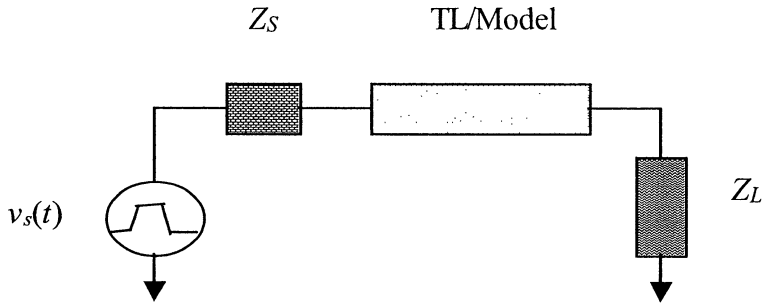


Figure 3.1: A two-port network with a voltage source $v_s(t)$, source impedance Z_S and load impedance Z_L

If we assume that $v_{tl}(t)$ and $v_{mod}(t)$ are the load voltages for circuits based on the transmission line and its proposed "equivalent" model respectively, the absolute difference of load voltages is given by

$$\delta_v(t) \equiv v_{mod}(t) - v_{tl}(t) \tag{3-1}$$

Practically, for signal integrity [69], we are more concerned about output voltage levels at required times. For a single pulse voltage source, considering its rising transition, t_{r10_tl}, t_{r50_tl} and t_{r90_tl} are the times at which the voltage waveform v_{tl} reaches 10%, 50% and 90% of the full voltage swing respectively. Similarly, t_{r10_mod}, t_{r50_mod} and t_{r90_mod} are

the corresponding quantities for voltage waveform v_{mod}. Thus, the absolute time differences between models and TL are given by

$$\delta_{tr10} \equiv t_{r10\_mod} - t_{r10\_tl} \tag{3-2a}$$

$$\delta_{tr50} \equiv t_{r50\_mod} - t_{r50\_tl} \tag{3-2b}$$

and $$\delta_{tr90} \equiv t_{r90\_mod} - t_{r90\_tl} \tag{3-2c}$$

Similarly, the times of a falling edge can also be used to estimate the simulation errors. For simplicity, we will focus on the absolute differences of times at the rising edge of voltage waveforms.

3.2.2 Division of frequency regions

In order to illustrate the contributions of a group of frequency components to the whole waveform of a signal, based on the bandwidth of the pulse voltage source, with or without consideration of the bandwidth of the system, the whole frequency range can be divided into several regions.

When dealing with digital pulses and signals in general, as mentioned by Sylvester [32], the maximum frequency of interest is related to the edge rate or rise time t_r of the pulse. Conservatively, the signal bandwidth can be defined from DC to f_{h2} (1/ t_r). An alternative definition for signal bandwidth is from DC to f_{h1} (0.35/ t_r), which corresponds to cut-off frequencies at the –3 dB points [27].

As to the bandwidth of the system, it depends on specific circuits. Thus, it cannot be expressed by a simple equation. For some circuits such as an on-chip RLC network with source resistance R_S and load capacitance C_L, it can be estimated by using Elmore delay τ_{ED} [70,71] (Appendix A).

In order not to lose generality, the division of frequency ranges can be based on the bandwidth of the pulse voltage source without consideration of the bandwidth of the system. Thus, by using the above two frequency points f_{h1} and f_{h2}, we propose to divide the whole frequency range into three frequency regions. Region I is from DC to f_{h1}, Region II from f_{h1} to f_{h2}, and Region III from f_{h2} to infinity. Since numerical time domain solutions always use a finite time step, practically the infinite upper limit can be replaced by $f_s/2$. Here, f_s is an arbitrarily high sampling frequency required by the modeling method, which can be selected to a few times f_{h2}, and above which there is no significant source signal energy transmitted to the load. Therefore, the modeling accuracy in Regions I and II should have great impact on the simulation error, while the simulation error is less sensitive to the modeling inaccuracy in Region III.

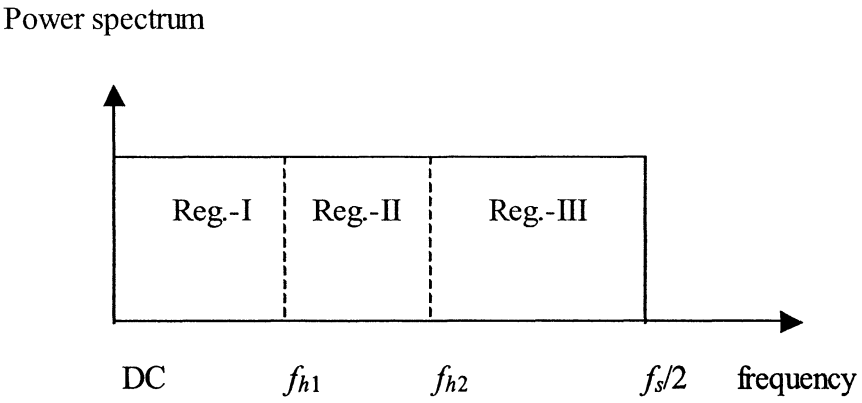


Figure 3.2: Division of frequency regions

On the condition that the bandwidth of the system can be obtained, we propose that the division of frequency ranges is revised by considering both the bandwidth of the signal and that of the system as performed in Section 4.2.2.1. However, the estimated time-domain simulation error is independent on the division of frequency ranges. It is related to the high sampling frequency f_s, which is normally selected far away from the –3 dB cut-off frequency point for a pulse voltage source.

3.2.3 Estimation of the time domain simulation errors from errors in the frequency domain response

Assuming that $\tilde{v}_{mod}(n)$ and $\tilde{v}_{tl}(n)$ are the samples of load voltages $v_{mod}(t)$ and $v_{tl}(t)$, we get

$$\tilde{v}_{mod}(n) \equiv v_{mod}(n\Delta t) \tag{3-3a}$$

and $$\tilde{v}_{tl}(n) \equiv v_{tl}(n\Delta t) \tag{3-3b}$$

where $$\Delta t = t_s \tag{3-3c}$$

and $$1 \le n \le N \tag{3-3d}$$

Here, t_s ($1/f_s$) is the sampling time interval and N is the total number of sampling points. Also assuming that $\tilde{\delta}_v(n)$ is the sample of the load voltage difference $\delta_v(t)$, we have

$$\tilde{\delta}_v(n) \equiv \delta_v(n\Delta t) \tag{3-4}$$

Here, n and Δt are expressed in Eqs.3-3c and 3-3d. Combining Eqs.3-3a, 3-3b, 3-4 with Eq.3-1, we get

$$\tilde{\delta}_v(n) = \tilde{v}_{mod}(n) - \tilde{v}_{tl}(n) \tag{3-5}$$

By using the inverse discrete Fourier transform (IDFT) [72], time-domain components $\tilde{v}_{mod}(n)$ and $\tilde{v}_{tl}(n)$ can be expressed by their respective frequency components $\tilde{V}_{mod}(k)$ and $\tilde{V}_{tl}(k)$:

$$\tilde{v}_{mod}(n) = \frac{1}{N}\sum_{k=1}^{N} \tilde{V}_{mod}(k) e^{j2\pi(k-1)(n-1)/N} \tag{3-6a}$$

and $$\tilde{v}_{tl}(n) = \frac{1}{N}\sum_{k=1}^{N} \tilde{V}_{tl}(k) e^{j2\pi(k-1)(n-1)/N} \tag{3-6b}$$

Combining Eqs.3-5, 3-6a and 3-6b, we estimate the absolute value of $\tilde{\delta}_v(n)$ in terms of frequency components $\tilde{V}_{mod}(k)$ and $\tilde{V}_{tl}(k)$:

$$\left|\tilde{\delta}_v(n)\right| = \left| \frac{1}{N}\sum_{k=1}^{N}[\tilde{V}_{mod}(k) - \tilde{V}_{tl}(k)]e^{j2\pi(k-1)(n-1)/N} \right| \quad (3-7a)$$

$$\leq \frac{1}{N}\sum_{k=1}^{N}\left|[\tilde{V}_{mod}(k) - \tilde{V}_{tl}(k)]e^{j2\pi(k-1)(n-1)/N}\right| \quad (3-7b)$$

$$= \frac{1}{N}\sum_{k=1}^{N}\left|\tilde{V}_{mod}(k) - \tilde{V}_{tl}(k)\right| \quad (3-7c)$$

Eq.3-7b is obtained from Eq.3-7a by realizing that the modules of a sum of complex numbers are no more than the sum of the modules of each complex number. Eq.3-7c arises from the unity amplitude of the exponentials in Eq.3-7b. In the following, the upper limit of $\tilde{\delta}_v(n)$ is defined as Δ, which can be expressed by:

$$\Delta \equiv \frac{1}{N}\sum_{k=1}^{N}\left|\tilde{V}_{mod}(k) - \tilde{V}_{tl}(k)\right| \quad (3\text{-}8)$$

By using the discrete Fourier transform (DFT) [72], frequency components $\tilde{V}_{mod}(k)$ and $\tilde{V}_{tl}(k)$ can be expressed from their respective time-domain components $\tilde{v}_{mod}(n)$ and $\tilde{v}_{tl}(n)$:

$$\tilde{V}_{mod}(k) = \sum_{n=1}^{N}\tilde{v}_{mod}(n)e^{-j2\pi(k-1)(n-1)/N} \quad (3\text{-}9a)$$

and $$\tilde{V}_{tl}(k) = \sum_{n=1}^{N}\tilde{v}_{tl}(n)e^{-j2\pi(k-1)(n-1)/N} \quad (3\text{-}9b)$$

where $1 \leq k \leq N$ (3-9c)

Normally, voltages $v_{mod}(t)$ and $v_{tl}(t)$ are real functions. Thus, $\tilde{v}_{mod}(n)$ and $\tilde{v}_{tl}(n)$ are real functions, too. Thus, we have

$$\tilde{v}_{mod}(n) = \tilde{v}^{*}_{mod}(n) \quad (3\text{-}10a)$$

and

$$\tilde{v}_{tl}(n) = \tilde{v}^{*}_{tl}(n) \quad (3\text{-}10b)$$

Combining Eqs.3-9a and 3-9b with Eqs.3-10a and 3-10b, a relation between frequency components $\tilde{V}_{mod}(k)$ can be given by

$$\begin{aligned}\widetilde{V}_{mod}(N+2-k) &= \sum_{n=1}^{N}\widetilde{v}_{mod}(n)e^{-j2\pi(N+2-k-1)(n-1)/N} \\ &= \sum_{n=1}^{N}\widetilde{v}_{mod}(n)e^{-j2\pi(1-k)(n-1)/N} \\ &= \left[\sum_{n=1}^{N}\widetilde{v}^{*}_{mod}(n)e^{j2\pi(1-k)(n-1)/N}\right]^{*} \\ &= \left[\sum_{n=1}^{N}\widetilde{v}_{mod}(n)e^{-j2\pi(k-1)(n-1)/N}\right]^{*} \\ &= \widetilde{V}^{*}_{mod}(k)\end{aligned} \tag{3-11a}$$

Similarly for frequency components $\widetilde{V}_{tl(k)}$, we can have

$$\widetilde{V}_{tl}(N+2-k) = \widetilde{V}^{*}_{tl}(k) \tag{3-11b}$$

where $2 \le k \le N/2$ (3-11c)

The relations between frequency components are expressed in Eqs.3-11a and 3-11b. These relations can also be illustrated by Figure 3.3, where N sampling points are equally mapped on a unit circle. It can be noted that two points k and (N+2-k) are symmetrically located at two sides of the horizontal-axis. Two axial points are of special interest. One is point 1 representing direct current (DC) frequency component, and the other is point (N/2+1) referring to frequency component sampling at $f_s/2$.

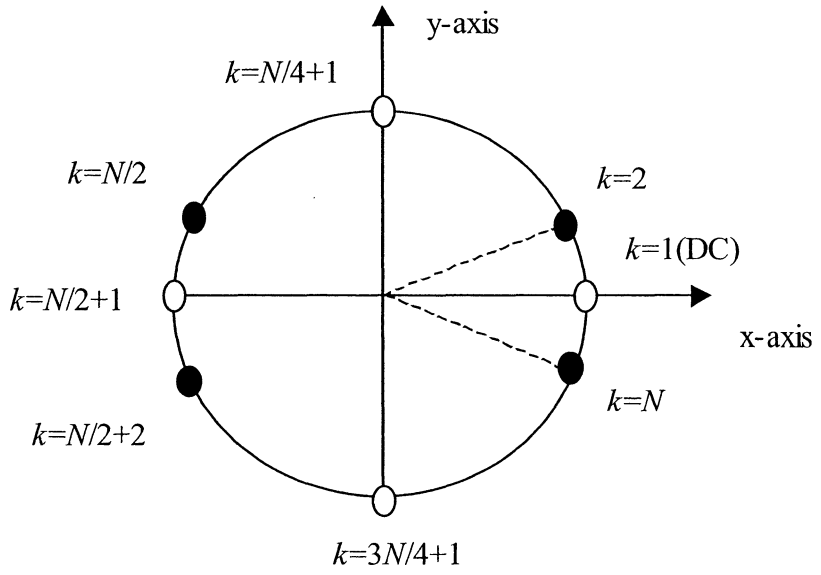


Figure 3.3: N sampling points on a unit circle

Combining Eqs.3-11a, 3-11b with 3-8, we obtain

$$\begin{aligned}\Delta &= \frac{1}{N}\sum_{k=1}^{N}\left|\tilde{V}_{mod}(k)-\tilde{V}_{tl}(k)\right| \\ &= \frac{1}{N}\left|\tilde{V}_{mod}(1)-\tilde{V}_{tl}(1)\right|+\frac{1}{N}\sum_{k=2}^{N/2}\left|\tilde{V}_{mod}(k)-\tilde{V}_{tl}(k)\right| \\ &\quad +\frac{1}{N}\left|\tilde{V}_{mod}\left(\frac{N}{2}+1\right)-\tilde{V}_{tl}\left(\frac{N}{2}+1\right)\right|+\frac{1}{N}\sum_{k=N/2+2}^{N}\left|\tilde{V}_{mod}(k)-\tilde{V}_{tl}(k)\right| \\ &= \frac{1}{N}\left|\tilde{V}_{mod}(1)-\tilde{V}_{tl}(1)\right|+\frac{2}{N}\sum_{k=2}^{N/2}\left|\tilde{V}_{mod}(k)-\tilde{V}_{tl}(k)\right|+\frac{1}{N}\left|\tilde{V}_{mod}\left(\frac{N}{2}+1\right)-\tilde{V}_{tl}\left(\frac{N}{2}+1\right)\right|\end{aligned} \tag{3-12}$$

Let us define the voltage transfer functions from the node of the source to that of the load for the model under investigation and for the reference case (TL) as $H_{mod}(s)$ and $H_{tl}(s)$, respectively. Here, s is the complex frequency $j\omega$. Assuming that $\tilde{H}_{mod}(k)$ and $\tilde{H}_{tl}(k)$ are the samples of voltage transfer functions $H_{mod}(s)$ and $H_{tl}(s)$, respectively. We have

$$\tilde{H}_{mod}(k) \equiv H_{mod}(k\Delta s) \tag{3-13a}$$

and $$\tilde{H}_{tl}(k) \equiv H_{tl}(k\Delta s) \tag{3-13b}$$

where $$\Delta s = j2\pi\Delta f = j2\pi\frac{f_s}{N} \tag{3-13c}$$

and $$1 \le k \le N \tag{3-13d}$$

Assuming that $\tilde{v}_s(n)$ is the sample of voltage source $v_s(t)$, and that $\tilde{V}_S(k)$ is the DFT of $\tilde{v}_s(n)$, the frequency components $\tilde{V}_{mod}(k)$ and $\tilde{V}_{tl}(k)$ in Eq.3-12 can then be obtained from the samples of the corresponding voltage transfer functions, $\tilde{H}_{mod}(k)$ and $\tilde{H}_{mod}(k)$, and the frequency components $\tilde{V}_S(k)$

$$\tilde{V}_{mod}(k) = \tilde{H}_{mod}(k)\tilde{V}_S(k) \tag{3-14a}$$

and $$\tilde{V}_{tl}(k) = \tilde{H}_{tl}(k)\tilde{V}_S(k) \tag{3-14b}$$

Thus, combining Eqs.3-14a, 3-14b with Eq.3-12, we obtain

$$\begin{aligned}
\Delta &= \frac{1}{N}\left|\tilde{V}_{mod}(1) - \tilde{V}_{tl}(1)\right| + \frac{2}{N}\sum_{k=2}^{N/2}\left|\tilde{V}_{mod}(k) - \tilde{V}_{tl}(k)\right| \\
&\quad + \frac{1}{N}\left|\tilde{V}_{mod}\left(\frac{N}{2}+1\right) - \tilde{V}_{tl}\left(\frac{N}{2}+1\right)\right| \\
&= \frac{1}{N}\left|\tilde{H}_{mod}(1) - \tilde{H}_{tl}(1)\right|\left|\tilde{V}_S(1)\right| + \frac{2}{N}\sum_{k=2}^{N/2}\left|\tilde{H}_{mod}(k) - \tilde{H}_{tl}(k)\right|\left|\tilde{V}_S(k)\right| \\
&\quad + \frac{1}{N}\left|\tilde{H}_{mod}\left(\frac{N}{2}+1\right) - \tilde{H}_{tl}\left(\frac{N}{2}+1\right)\right|\left|\tilde{V}_S\left(\frac{N}{2}+1\right)\right| \\
&= \Delta_I + \Delta_{II} + \Delta_{III}
\end{aligned} \tag{3-15a}$$

where

$$\Delta_I = \frac{1}{N}\left|\tilde{H}_{mod}(1) - \tilde{H}_{tl}(1)\right|\left|\tilde{V}_S(1)\right| + \frac{2}{N}\sum_{k=2}^{n_1}\left|\tilde{H}_{mod}(k) - \tilde{H}_{tl}(k)\right|\left|\tilde{V}_S(k)\right| \tag{3-15b}$$

$$\Delta_{II} = \frac{2}{N}\sum_{k=n_1+1}^{n_2}\left|\tilde{H}_{mod}(k)-\tilde{H}_{tl}(k)\right|\left|\tilde{V}_S(k)\right| \tag{3-15c}$$

and

$$\begin{aligned}\Delta_{III} = &\frac{2}{N}\sum_{k=n_2+1}^{N/2}\left|\tilde{H}_{mod}(k)-\tilde{H}_{tl}(k)\right|\left|\tilde{V}_S(k)\right| \\ &+\frac{1}{N}\left|\tilde{H}_{mod}\left(\frac{N}{2}+1\right)-\tilde{H}_{tl}\left(\frac{N}{2}+1\right)\right|\left|\tilde{V}_S\left(\frac{N}{2}+1\right)\right|\end{aligned} \tag{3-15d}$$

Here, n_1 and n_2 refer to the samples corresponding to frequency points f_{h1} and f_{h2}, and their values are given by

$$n_1 = \text{int}\left(\frac{Nf_{h1}}{f_s}\right) \tag{3-16a}$$

and

$$n_2 = \text{int}\left(\frac{Nf_{h2}}{f_s}\right) \tag{3-16b}$$

where int(·) returns the integer part of the argument.

3.3 Validation with practical interconnect models

In VLSI circuits, signals propagate between gates and buffer stages. Each net is characterized by several parameters such as the wire length and the fanout. Long wires and large fanout require strong buffers with low output resistance R_S. As shown in Figure 3.4, a typical net consists of a RC transmission line, source resistance R_S and load capacitance C_L. We will use this simple net to illustrate our method of estimating the upper limit of the time-domain model-induced error based on characteristics obtained in the frequency domain. By using circuit techniques such as ILC circuit models, the RC transmission line is replaced by an equivalent circuit model. Based on Eq.3-15a, a program was written to estimate the maximum simulation error between the circuits based on the model and the reference (TL). Numerical results are now compared with those obtained from Agilent Technologies ADS circuit simulations, making possible the validation of our method for this special case.

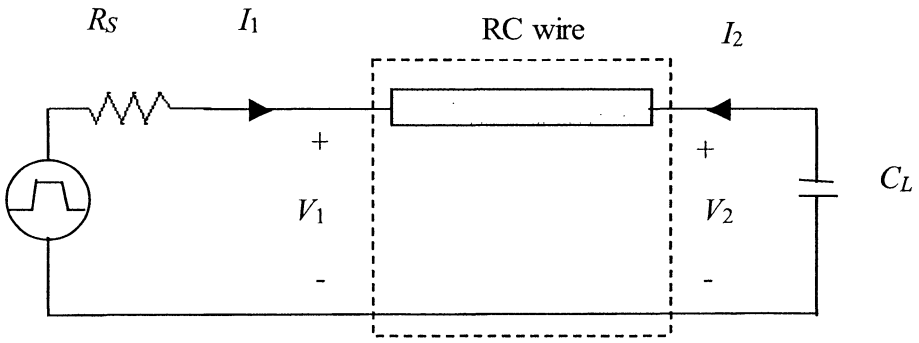
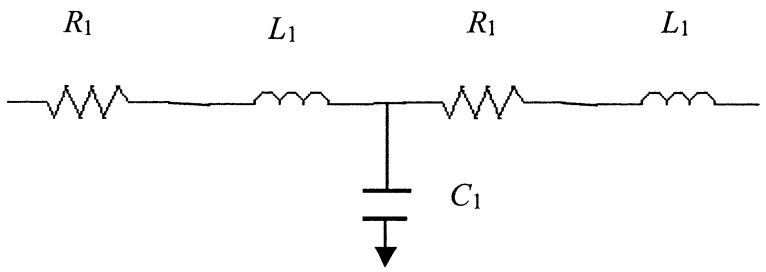


Figure 3.4 A two-port network with an RC wire, source resistance R_S and load capacitance C_L

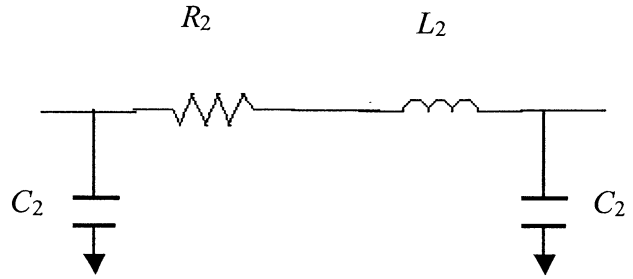
3.3.1 Description of two circuit techniques

There exist many types of interconnect models such as the lumped equivalent circuit model, the distributed equivalent circuit model, and so on. Lumped equivalent circuit models (e.g., resistance-inductance-capacitance (RLC) networks) are often used to model on-chip interconnects, while the distributed equivalent circuit models (e.g., lossy coupled multiconductor transmission lines with cross-sectional per unit length RLCG parameters) are suitable for interconnects on multichip, board or wafer. Lumped circuit models can be directly used in circuit simulations. Distributed equivalent circuit models need to be constructed into equivalent circuit models by using different circuit techniques such as ILC and MC models. These equivalent circuit models can then be embedded into circuit simulations.

In this section, we describe the two types of circuit techniques ILC and MC mentioned above. Our approach is analogue to the one used by Gupta *et al.*'s paper [21]. As shown in Figures 3.5a and 3.5b, ILC models cascade T- or π- sections. These sections are composed of lumped circuit elements. By contrast, an MC cell is composed of one lossless transmission line (TL) segment with lossy lumped elements at its two ends as shown in Figure 3.6.



(a) T-section



(b) π-section

Figure 3.5: T- and π- sections used in ILC models

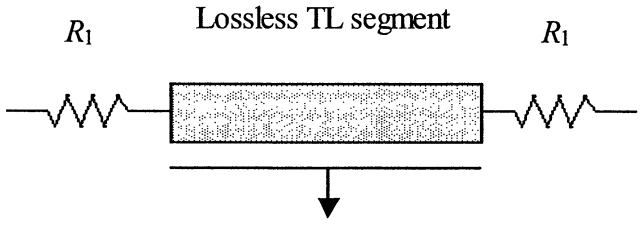


Figure 3.6: An MC cell

3.3.2 Derivation of the transfer function for an interconnect model

As discussed in Section 3.2.3, the voltage transfer function from the source node to the load is used to estimate the modeling accuracy. For the RC wire, shown in Figure 3.4,

ILC models with T-sections are used in circuit simulations. The transfer functions for both ILC model and RC transmission line are derived below.

For a two-port network (with TL or ILC) shown in Figure 3.4, by considering voltage source V_S, source resistance R_S and load capacitance C_L, the voltage transfer function from the source node to the load can be derived from ABCD parameters.

3.3.2.1 ABCD matrix of a two-port network for an RC transmission line

The ABCD matrix of the two-port network with an RC transmission line in Figure 3.4 can be obtained from the corresponded S-parameters. If the S-parameters are selected to be renormalized with respect to the complex characteristic impedance Z_C of the RC transmission line taking $Z_{C1}=Z_{C2}=Z_C$, we can have simple expressions for S-parameters as

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} = \begin{bmatrix} 0 & e^{-\gamma d} \\ e^{-\gamma d} & 0 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{3-17a}$$

where $\gamma = \sqrt{sR_w^l C_w^l}$ (3-17b)

$$Z_C = \sqrt{\frac{R_w^l}{sC_w^l}} \tag{3-17c}$$

and $s = j\omega$ (3-17d)

Here, γ is the complex propagation constant, d is the length of wire, and R_w^l and C_w^l are the wire resistance and wire capacitance per unit length of the RC transmission line, respectively.

With respect to the definitions of two-port voltages and currents in Figure 3.4, the ABCD matrix of the two-port network with an RC transmission line is derived from its renormalized S-parameters in Eq.3-17a. We have

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{3-18a}$$

where

$$Y_c = \frac{1}{Z_c} \tag{3-18b}$$

$$A = D = \cosh(\gamma_n) \tag{3-18c}$$

$$B = Z_C \sinh(\gamma_n) \tag{3-18d}$$

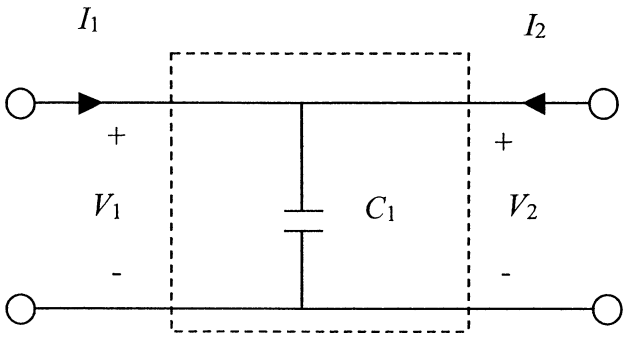
$$C = Y_C \sinh(\gamma_n) \tag{3-18e}$$

and $$\gamma_n = \gamma d \tag{3-18f}$$

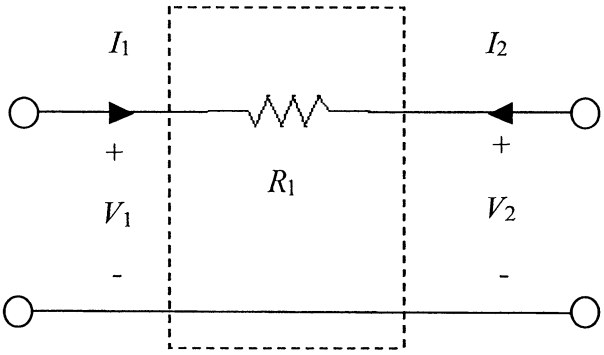
3.3.2.2 ABCD matrix of a two-port network with an ILC model of T-sections

An ILC model cascades T-sections. Thus, for a two-port network with an ILC model of T-sections, the ABCD matrix of the two-port network can be obtained from the ABCD matrix of one T-section sub-network.

Similarly, the ABCD matrix of one T-section sub-network can also be obtained from the ABCD matrices of several sub-networks. As shown in Figure 3.5a, one T-section of an RC wire consists of two series resistances R_1 and one shunt capacitance C_1. Here, L_1 is equal to 0 for RC wire. So it includes two kinds of sub-network: sub-network I with shunt element C_1 and sub-network II with series element R_1 as shown in Figures 3.7a and 3.7b, respectively.



(a) Sub-network I



(b) Sub-network II

Figure 3.7: Two sub-networks for one T-section

The ABCD matrices of sub-network I and II can be written respectively as

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ sC_1 & 1 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{3-19a}$$

and

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & R_1 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{3-19b}$$

Thus, the total ABCD matrix for one T-section can be obtained from Eqs.3-19a and 3-19b.

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & R_1 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ sC_1 & 1 \end{bmatrix} \begin{bmatrix} 1 & R_1 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$
$$= \begin{bmatrix} 1+sR_1C_1 & R_1 \\ sC_1 & 1 \end{bmatrix} \begin{bmatrix} 1 & R_1 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \quad (3\text{-}20)$$
$$= \begin{bmatrix} 1+sR_1C_1 & R_1(2+sR_1C_1) \\ sC_1 & 1+sR_1C_1 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

This is valid for one cell of the ILC model. The matrix for a full interconnect composed of n T-sections is equal to the n^{th} power of the matrix in Eq.3-20.

3.3.2.3 Voltage transfer function of a two-port network with R_S and C_L

The voltage transfer function from the source node to the load can then be derived from the ABCD parameters of a two-port network with a TL model or an ILC model. For the source resistance R_S, it can be treated as a sub-network II with series element R_S as illustrated in Figure 3.7b. The ABCD parameters of the sub-network can be expressed as

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & R_S \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \quad (3\text{-}21)$$

By combining Eq.3-21 with Eq.3-18a, the ABCD parameters of the network with RC wire (TL model) including source resistance R_S can be expressed as

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & R_S \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \cosh(\gamma_n) & Z_C \sinh(\gamma_n) \\ Y_C \sinh(\gamma_n) & \cosh(\gamma_n) \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$
$$= \begin{bmatrix} \cosh(\gamma_n)+R_S Y_C \sinh(\gamma_n) & Z_C \sinh(\gamma_n)+R_S \cosh(\gamma_n) \\ Y_C \sinh(\gamma_n) & \cosh(\gamma_n) \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \quad (3\text{-}22)$$

Similarly, by combining Eq.3-21 with Eq.3-20, the ABCD parameters of the network with an ILC model of one T-section including source resistance R_S can be expressed as

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & R_S \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1+sR_1C_1 & R_1(2+sR_1C_1) \\ sC_1 & 1+sR_1C_1 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$
$$= \begin{bmatrix} 1+sC_1(R_S+R_1) & (R_S+2R_1)+sR_1C_1(R_S+R_1) \\ sC_1 & 1+sR_1C_1 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \quad (3\text{-}23)$$

As shown in Figure 3.4, for the load we have

$$-I_2 = sC_L V_2 \quad (3\text{-}24)$$

Combining Eq.3-24 with Eq.3-22, the voltage transfer function for the RC wire (TL model) can be obtained

$$H_{tl}(s) = \frac{V_2(s)}{V_1(s)} = \frac{1}{[\cosh(\gamma_n) + R_S Y_C \sinh(\gamma_n)] + sC_L[Z_C \sinh(\gamma_n) + R_S \cosh(\gamma_n)]} \quad (3\text{-}25)$$

Similarly, by combining Eq.3-24 with Eq.3-23, the voltage transfer function for an ILC model of one T-section can be obtained as

$$H_{mod}(s) = \frac{V_2(s)}{V_1(s)} = \frac{1}{1+sC_1(R_S+R_1)+sC_L(R_S+2R_1)+s^2R_1C_1C_L(R_S+R_1)} \quad (3\text{-}26)$$

Let us now compare Eqs.3-25 and 3-26. For an ILC model of one T-section with length *d*, we have

$$R_1 = \frac{dR_w^l}{2} \quad (3\text{-}27a)$$

and $$C_1 = dC_w^l \quad (3\text{-}27b)$$

Combining Eqs.3-27a and 3-27b with Eq.3-17c, we get

and $$Z_C = \frac{1}{Y_C} = \sqrt{\frac{R_w^l}{sC_w^l}} = \sqrt{\frac{2R_1}{sC_1}} = \frac{\sqrt{2sR_1C_1}}{sC_1} \quad (3\text{-}28)$$

Combining Eqs.3-27a and 3-27b with Eqs.3-17b and 3-18f, we obtain

$$\gamma_n = \gamma d = d\sqrt{R_w^l sC_w^l} = \sqrt{2sR_1C_1} \tag{3-29}$$

Here, we define the complex variable γ_n as a normalized propagation constant.

Assuming that $|\gamma_n| << 1$, we have

$$\cosh(\gamma_n) = \frac{e^{\gamma_n} + e^{-\gamma_n}}{2} \approx 1 + \frac{\gamma_n^2}{2} = 1 + sR_1C_1 \tag{3-30a}$$

and $$\sinh(\gamma_n) = \frac{e^{\gamma_n} - e^{-\gamma_n}}{2} \approx \gamma_n = \sqrt{2sR_1C_1} \tag{3-30b}$$

Combining Eqs.3-29, 3-30a, 3-30b with Eq.3-25, we obtain

$$\begin{aligned} H_{tl}(s) &= \frac{V_2(s)}{V_1(s)} \\ &= \frac{1}{[\cosh(\gamma_n) + R_S Y_C \sinh(\gamma_n)] + sC_L[Z_C \sinh(\gamma_n) + R_S \cosh(\gamma_n)]} \\ &\approx \frac{1}{\left[(1 + \frac{\gamma_n^2}{2}) + R_S \frac{sC_1}{\gamma_n}\gamma_n\right] + sC_L\left[\frac{\gamma_n^2}{sC_1} + R_S\left(1 + \frac{\gamma_n^2}{2}\right)\right]} \qquad |\gamma_n| << 1 \\ &= \frac{1}{1 + sC_1(R_1 + R_S) + sC_L(2R_1 + R_S) + s^2 C_1 C_L R_1 R_S} \end{aligned} \tag{3-31}$$

On the condition that $|\gamma_n| << 1$, the difference between the two transfer functions in Eqs.3-26 and 3-31 is only an extra 2nd order term of $s^2 C_1 C_L R_1^2$ found in the derivation of Eq.3-26. Expanding these two transfer functions about s=0, we can rewrite both of them as Taylor series in powers of s [29]:

$$H_s(s) = m_0 + m_1 s + m_2 s^2 + m_3 s^3 + \ldots \tag{3-32a}$$

where $m_0 = 1$ (3-32b)

and $$m_1 = -[C_1(R_1 + R_S) + C_L(2R_1 + R_S)] \quad (3\text{-}32c)$$

The first moment term m_1 in Eq.3-32c is related to Elmore delay τ_{ED} [70] [Appendix A]. As proved in [71], there is only a difference of sign "-" between τ_{ED} and m_1.

$$\tau_{ED} = -m_1 = C_1(R_1 + R_S) + C_L(2R_1 + R_S) \quad (3\text{-}33)$$

It shows that the Elmore delays for the circuit with a TL model and the one with an ILC model of one T-section are identical on the condition that $|\gamma_n| << 1$.

3.3.3 Example of comparisons between estimated errors and those computed from the simulator

In this section, we analyze the pulse response of a two-port network of a typical RC wire with source resistance R_S and load capacitance C_L, as shown in Figure 3.4. For example, the source resistance R_S and load capacitance C_L are assumed to be 1 kΩ and 0.1 pF, respectively. Here, the total wire resistance and capacitance of the RC wire are assumed to be 1 kΩ and 0.1 pF, respectively. As mentioned above, the RC wire is replaced with a TL model or with an ILC model of one T-section.

In the circuit simulation, a periodic pulsed voltage source with a width of 5 ns and a period of 20 ns is used as shown in Figure 3.8. Both the rising time and the falling time of the pulse are 0.5 ns.

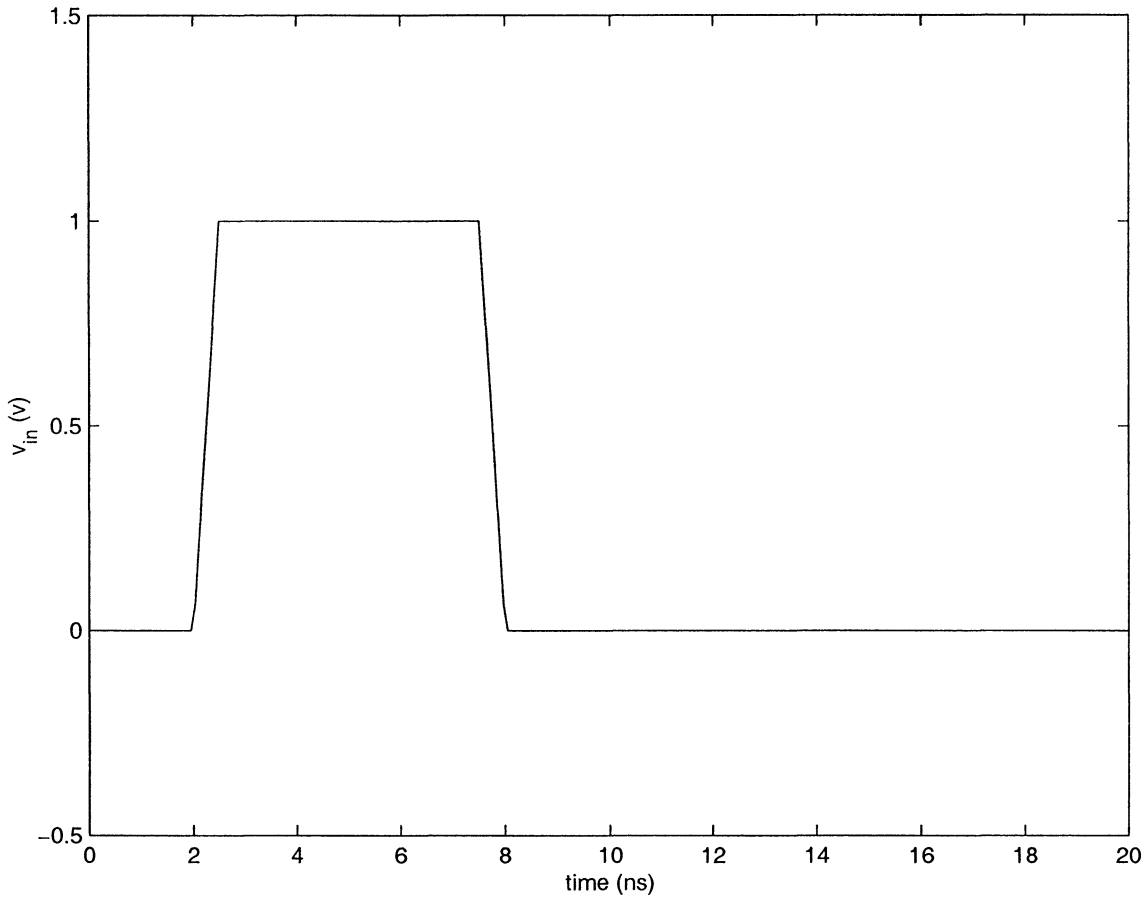


Figure 3.8: Pulse voltage source

Based on the rising time, two frequencies f_{h1} and f_{h2} are 0.7 GHz and 2 GHz, respectively. Here, 256 sampling points are used for a period of 20 ns. Thus, the sampling time interval t_s is 0.078125 ns (20/256), and the sampling frequency f_s is 12.8 GHz (1/ t_s), which is far above f_{h1}. By using Eq.3-33, the Elmore delay τ_{ED} for an ILC model with one T-section is 0.35 ns. For simplicity, below we only compare the estimated error with those from the simulator in the whole frequency range from DC to $f_s/2$ (6.4 GHz). Detailed analysis of the estimated error contributed from each frequency range will be discussed in Section 4.2.2.1. This example will confirm that the estimated time-domain error in the whole frequency range provides an upper limit for the model-induced simulation error.

By using Eqs.3-25 and 3-26, the voltage transfer functions $H(s)$ from the source node to the load are obtained for the two circuits with the TL and ILC models. Figures 3.9a and 3.9b show the magnitude and phase of $H(s)$, respectively. Here, the frequency is swept linearly from 5 MHz to 6.4 GHz ($f_s/2$). The difference of magnitude in the transfer function $H(s)$ between the TL and ILC models is almost invisible in Figure 3.9a for this special case. In Figure 3.9b, the two curves representing the phase of $H(s)$ merge together in the lower frequencies region from 5 to 100 MHz. The phase difference appears around 300 MHz, and is visible up to 6.4 GHz.

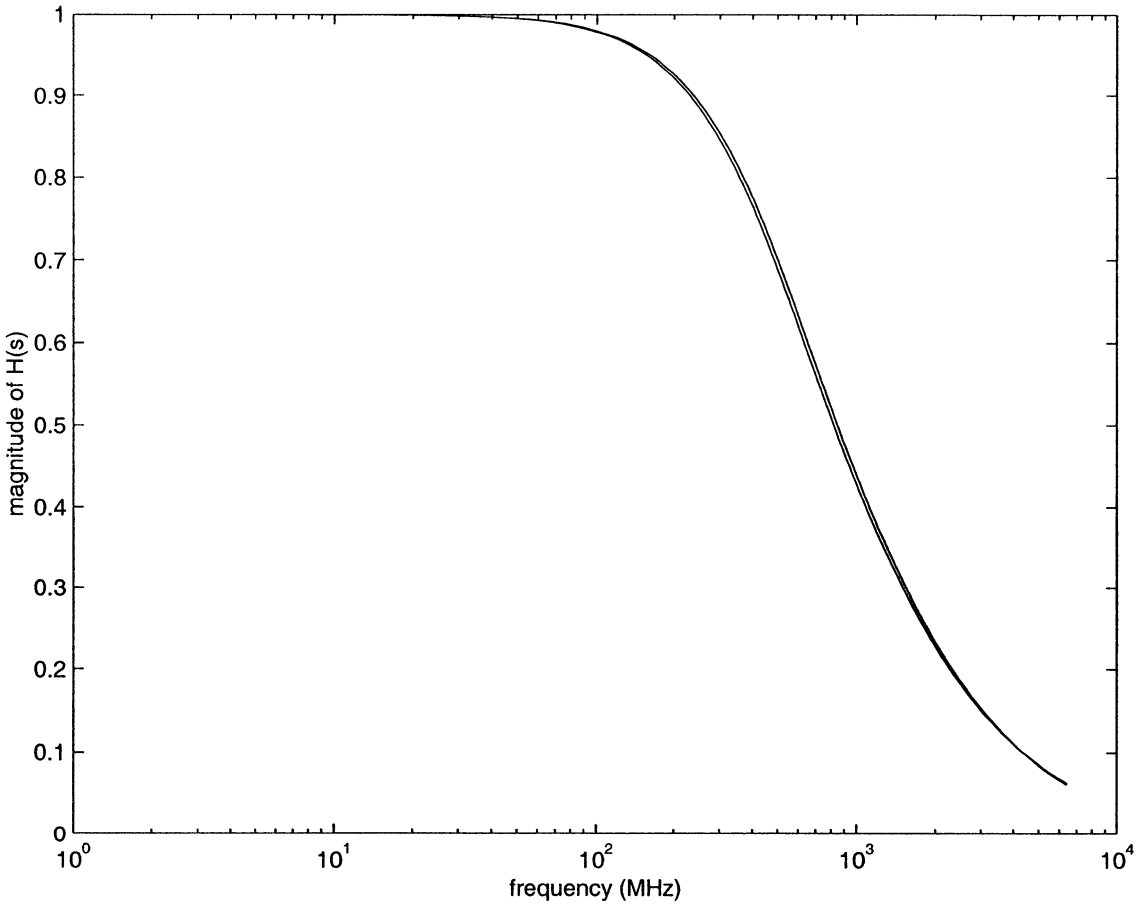


Figure 3.9a: Magnitude of voltage transfer functions
for ILC and TL models

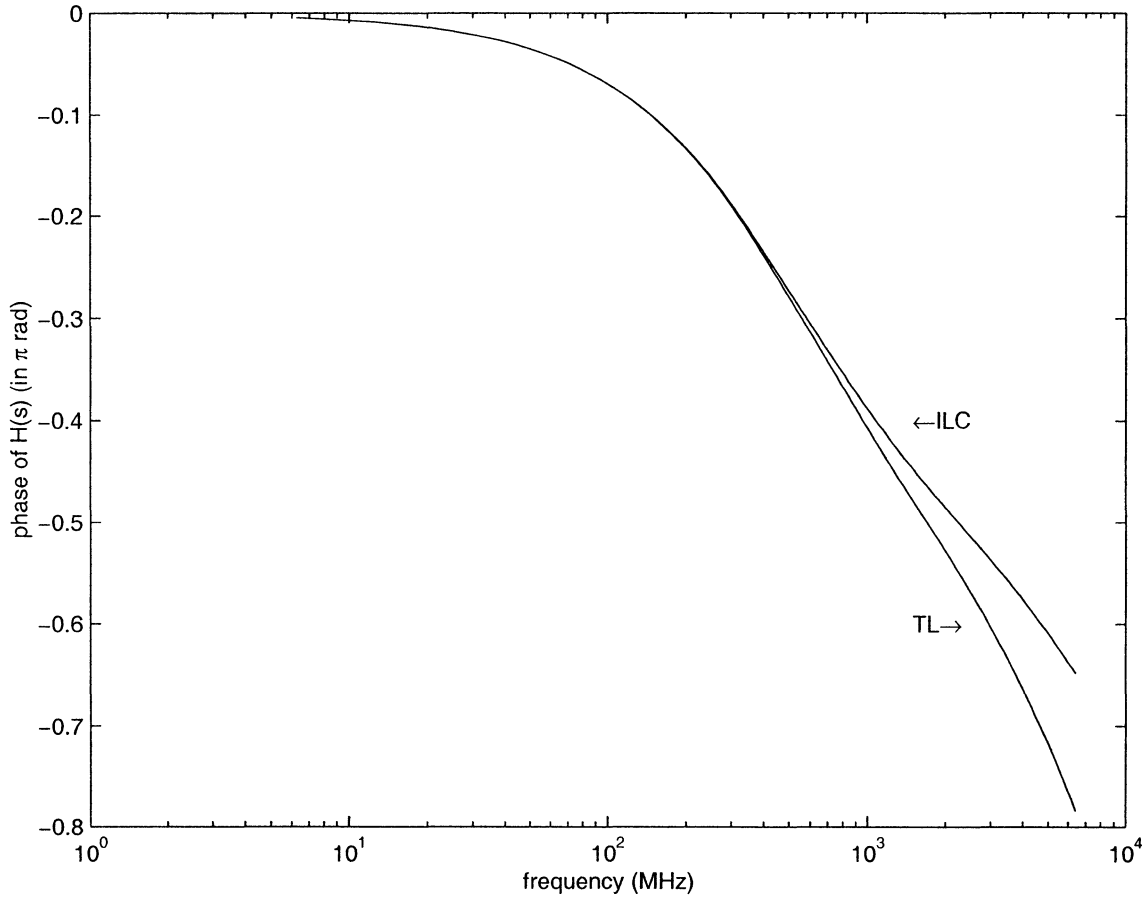


Figure 3.9b: Phase of voltage transfer functions
for ILC and TL models

By combining the pulse voltage source with the voltage transfer functions, the inverse discrete Fourier transform (IDFT) is performed and the pulse responses of load voltages are obtained for the TL and ILC models (see Figure 3.10a). Here, the two curves are almost identical. The difference of load voltage is displayed in Figure 3.10b. The maximum value of the voltage difference is about 8.4 mV. Based on Eq.3-15a, the estimated maximum voltage difference between the two models is 14 mV. For this case, our estimated error gives a conservative value of the time-domain model-induced simulation error. It confirms that our proposed method provides an upper limit for the time-domain simulation error. Though the exact time-domain simulation error cannot be obtained without performing a time-domain simulation, it will not exceed the upper

limit. Another worked example leading to the same conclusion will be illustrated in the following chapter. Certainly, in the future, more research is needed to verify whether such upper limit is really an upper bound for the time-domain simulation error and how tightness of this bound.

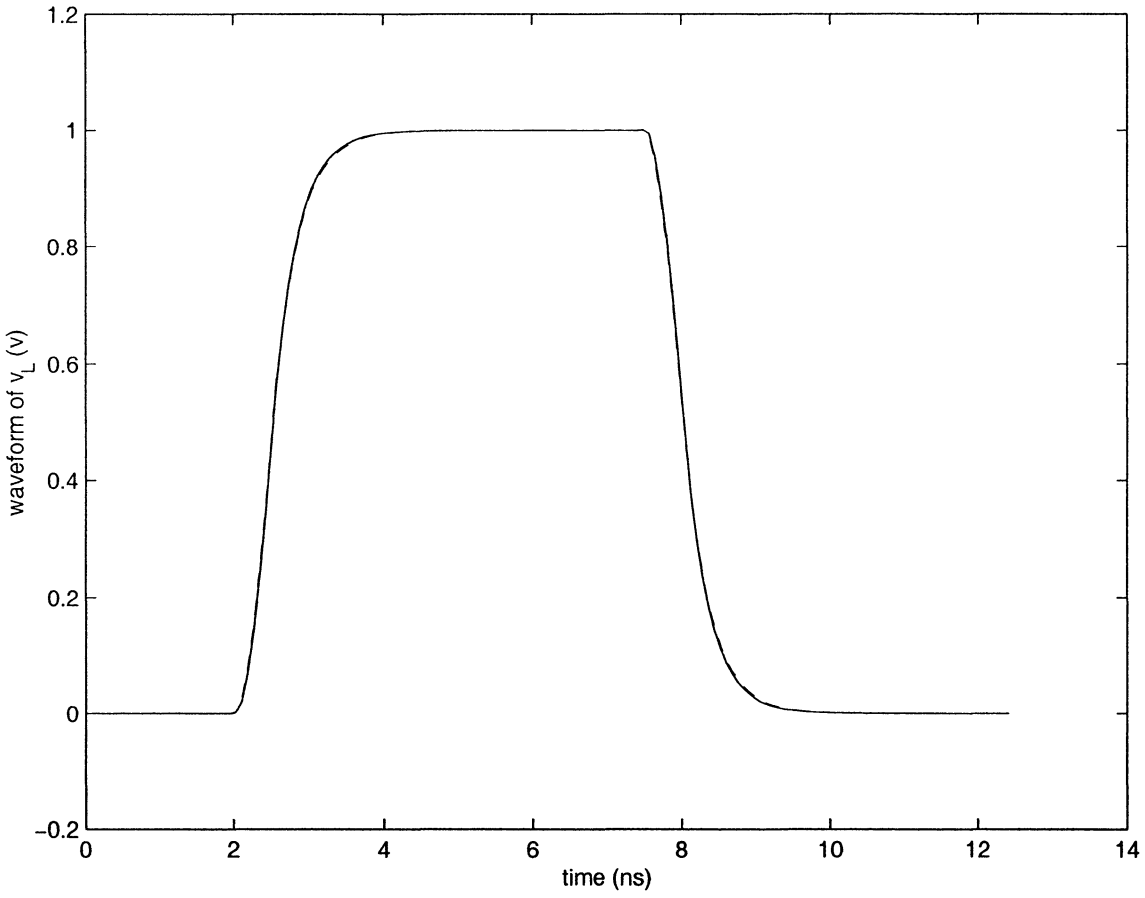


Figure 3.10a: Waveform of load voltages for ILC and TL models

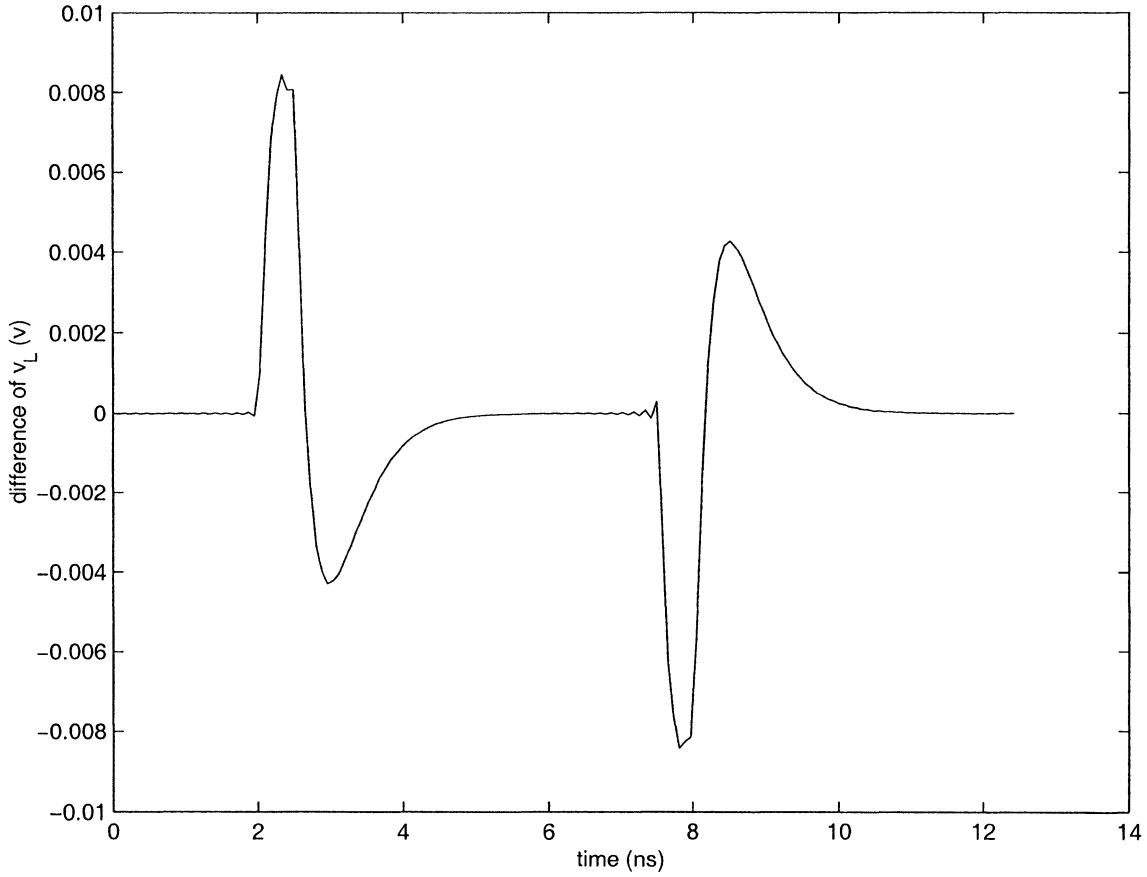


Figure 3.10b: Voltage difference between the circuits with ILC and TL models

3.4 Relation between the voltage transfer function and *S*-parameters

In Section 3.3, the voltage transfer function has been used in a selected example to estimate the impact of the modeling accuracy on the time-domain error. In Section 3.3.2, the voltage transfer function for a two-port network with an RC transmission line is derived from ABCD parameters of the two-port network. In fact, the voltage transfer function can also be derived from other types of parameters such as *S*-parameters.

There are three advantages in using the *S*-parameters. First, there is a direct relationship between the voltage transfer function and the renormalized *S*-parameters of a two-port network. It will be shown in the following that the renormalized *S*-parameters are

directly related to the voltage transfer function by multiplying a factor. Secondly, the *S*-parameters are usually obtained in swept-frequency measurements. Thus, our method cannot only be validated by other simulators, but also by experimental measurements. Finally, *S*-parameters can also easily be generalized to multi-port networks, which is not always the case with ABCD parameters. Consequently, the voltage transfer function obtained from the renormalized *S*-parameters would be easily derived for a multi-port network situation such as two coupled lines driven by two source resistances and with two load capacitances.

In the following, we derive the relationship between the voltage transfer function $H(s)$ and the renormalized *S*-parameters for a two-port net. Again, s is the complex frequency $j\omega$. As shown in Figure 3.11, a voltage source $V_S(s)$ is assumed with source impedance Z_S and load Z_L. The voltage transfer function $H(s)$ from the source node to the load node is defined as the ratio of load voltage $V_L(s)$ to source voltage $V_S(s)$.

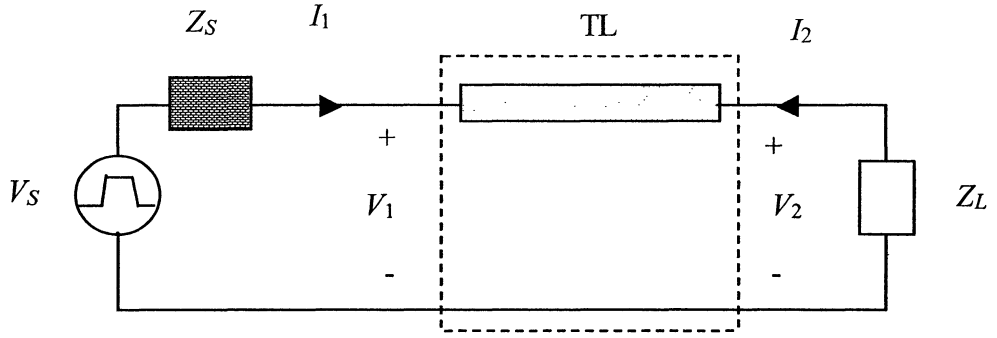


Figure 3.11: A two-port network with source impedance Z_S and load Z_L

The two steps of the method are described in the following. In the first step, we calculate the renormalized *S*-parameters of a two-port network. In the second step, we derive the transfer function $H(s)$ from the renormalized *S*-parameters.

3.4.1 Renormalized *S*-parameter S_{21}

Usually, *S*-parameters are normalized to 50 Ω. However, it is useful to use renormalized *S*-parameters when source impedance and load are different from 50 Ω. With proper renormalized characteristic impedances at all the ports in a network, all the port reflections in a network can be set to 0. Simple expressions for the renormalized *S*-parameters can be obtained and accelerates computation of the voltage transfer function.

Renormalization consists in a transformation of the *S*-matrix that enables the choice of any arbitrary impedance value to be chosen as the renormalized characteristic impedance at any port of a network. Therefore, it is most useful in cases where the connecting loads on a network have different impedances, which is often the case in a digital net. For a two-port network with source impedance Z_S and load Z_L, Z_S is selected as the renormalized characteristic impedance Z_{01} of port 1, and Z_L is selected as the renormalized characteristic impedance Z_{02} of port 2 [73].

The signal flow graph of the two-port network is shown in Figure 3.12. Node b_s stands for the wave of source flowing into the node of a_1. The other four nodes (a_1, a_2, b_1 and b_2) in this graph represent incident or reflected waves in the network. The value of wave at a node equals to the weighted sum of all the values of its neighbor nodes having signal flowing into the node with having their respective weight coefficients indicated along every path in the signal flow graph.

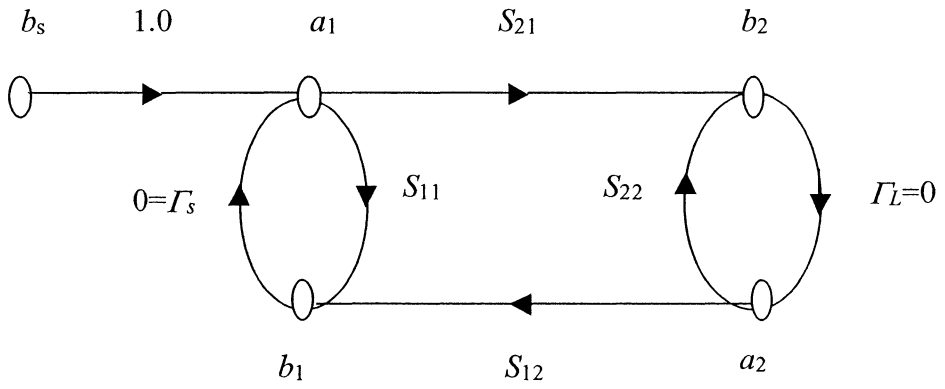


Figure 3.12: Signal flow graph of a two-port network with Z_S and Z_L ($Z_{01} = Z_S$ and $Z_{02} = Z_L$)

Since the network is terminated with the renormalized characteristic impedances, both source (Γ_S) and load (Γ_L) reflection coefficients are equal to 0. Thus, a signal b_s from the source travels to the load only through the S_{21} path shown in Figure 3.12. Therefore, only S_{21} of the four S-parameters needs to be calculated to obtain the voltage transfer function.

Expressions are given in [73] to renormalize the S-parameters. Since we are dealing with only a two-port network as shown in Figure 3.11, it is easy to derive S_{21} from the corresponded ABCD parameters of the two-port network. The relations between voltage/current and forward/reverse wave expressions of a two-port network are:

$$V_1 = (a_1 + b_1)\sqrt{Z_{01}} = (a_1 + b_1)\sqrt{Z_S} \tag{3-34a}$$

$$V_2 = (a_2 + b_2)\sqrt{Z_{02}} = (a_2 + b_2)\sqrt{Z_L} \tag{3-34b}$$

$$I_1 = \frac{a_1 - b_1}{\sqrt{Z_{01}}} = \frac{a_1 - b_1}{\sqrt{Z_S}} \tag{3-34c}$$

and

$$I_2 = \frac{a_2 - b_2}{\sqrt{Z_{02}}} = \frac{a_2 - b_2}{\sqrt{Z_L}} \tag{3-34d}$$

Since the load reflection coefficient Γ_L is equal to 0, from the signal flow graph, a_2 is equal to 0, too. Thus, Eqs.3-34b and 3-34d can be rewritten as

$$V_2 = b_2\sqrt{Z_L} \tag{3-35a}$$

and $$I_2 = -b_2 / \sqrt{Z_L} \tag{3-35b}$$

The ABCD parameters of the two-port network shown in Figure 3.11 can be expressed as:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{3-36}$$

Combining Eqs.3-34a, 3-34c, 3-35a, 3-35b and 3-36, S_{21} leads to

$$S_{21} = \frac{b_2}{a_1} = \frac{2\sqrt{Z_S Y_L}}{(A + BY_L) + Z_S(C + DY_L)} \tag{3-37a}$$

where $$Y_L = \frac{1}{Z_L} \tag{3-37b}$$

3.4.2 Voltage transfer function $H(s)$

Once S_{21} is obtained, the voltage transfer function $H(s)$ from the source node to the load node can be derived from S_{21}. $H(s)$ is given by

$$H(s) = \frac{V_L(s)}{V_S(s)} \tag{3-38}$$

At port 1, the source voltage $V_S(s)$ is normalized by the characteristic impedance Z_{01} [74], which is selected to be equal to the source impedance Z_S. We get

$$b_s = \frac{V_S}{2\sqrt{Z_{01}}} = \frac{V_S}{2\sqrt{Z_S}} \tag{3-39}$$

For the source reflection coefficient Γ_s is equal to 0. From the signal flow graph, we have

$$a_1 = b_s \tag{3-40}$$

Combining Eqs.3-39 and 3-40, $V_S(s)$ can be expressed in terms of a_1

$$V_S = 2a_1\sqrt{Z_S} \tag{3-41}$$

At port 2, the load voltage V_L is just V_2. Thus, we have

$$V_L = V_2 \tag{3-42}$$

Combining Eqs.3-35a with 3-42, V_L can be expressed in terms of b_2

$$V_L = b_2\sqrt{Z_L} \tag{3-43}$$

Thus, combining from Eqs.3-38, 3-41 with 3-43, $H(s)$ can be rewritten in terms of S_{21}

$$H(s) = \frac{b_2}{2a_1\sqrt{Z_S Y_L}} = \frac{S_{21}}{2\sqrt{Z_S Y_L}} \tag{3-44}$$

It is of interest that $H(s)$ is always related to S_{21} by a simple multiplying factor of $2\sqrt{Z_S Y_L}$. Such a factor is only related to the source and loading conditions (Z_S and Y_L) at two ports. Therefore, it demonstrates the strong relationship between the voltage transfer function and the renormalized S-parameters.

Based on multi-port renormalized S-parameters as described in [69], the voltage transfer function from one node to another of a multi-port complicated network with coupled transmission line networks can be similarly obtained. Our proposed method in this chapter to estimate the simulation error for a single transmission line network could be easily applied to the coupled transmission line networks by making use of the renormalized S-parameters to calculate the transfer function $H(s)$.

3.5 Discussion

In this chapter, a method is presented to estimate the time-domain model-induced simulation error using the frequency domain circuit parameters. Such method is based on the spectrum of voltage source and on the difference of the voltage transfer functions between models. With a simple RC transmission line net with source resistance R_S and load capacitance C_L, it is demonstrated that our estimated error is prone to be an upper limit for the model-induced simulated error in time domain from ADS simulator. In the next chapter, this method will be further validated using a simple two-port network: a single interconnect in the MIS configuration with source resistance R_S and load capacitance C_L.

Here, the voltage transfer function can be easily calculated from the renormalized *S*-parameters, because there is a strong relationship between the voltage transfer function and the renormalized *S*-parameters. Such relation is illustrated using a simple two-port network: a single interconnect in the MIS configuration with source impedance Z_S and load Z_L. By using the renormalized *S*-parameters, it accelerates computation of the voltage transfer function.

CHAPTER 4

MODELING OF A SINGLE INTERCONNECT IN THE MIS CONFIGURATION

This chapter focuses on the derivation of accurate interconnect models. The proposed method in the third chapter is used to investigate the impact of modeling limitations on the time-domain simulation error.

4.1 Introduction

Effective and efficient modeling of on-chip interconnections in modern VLSI circuits has become extremely important because interconnects contribute to a significant fraction of propagation delay in high-speed designs. The skin effect in the metal strip and the dielectric losses need to be considered in the modeling of interconnects in the MIS configuration, as the highest frequency of interest grows above 1 gigahertz, and as the length of on-chip interconnects increases up to 1 cm or more. A lot of work has been done in the modeling of interconnects in the MIS configuration.

Guckel *et al.* [34] studied the fundamental mode of a 1D parallel–plate waveguide with a two-layer loading medium, a conducting semiconductor substrate and a relatively thin dielectric. They neglected the fringing fields and predicted the existence of slow-wave phenomena.

Based on such parallel-plate model [34], Hasegawa *et al.* [10] extensively studied the fundamental TM_0 mode of MIS transmission lines. They predicted the existence of three types of behaviour for the fundamental mode: skin effect, slow-wave and quasi-TEM, and illustrated the conditions for the appearance of each type of behaviour in the

resistivity-frequency plane. Moreover, they discussed the propagation mechanism, analyzed the fringing field effect and constructed 2D distributed equivalent circuit model for each case.

Similar to the previous paper [10], Tuncer *et al.* [14] also considered the field spreading and suggested a unique 2D quasi-static model for all the three cases. This model included the impact of semiconductor on the series impedance per unit length of microstrip and the transverse resonant technique was used to revise the expression of the series impedance. A distance tuning parameter k, a measure of how much the field spreads before reaching the ground plane, was selected by matching their numerical results with those obtained from Wheeler's equations [46]. They demonstrated that the agreement of complex propagation constants between the quasi-static and full-wave calculations was excellent over almost four orders of magnitude of frequency and conductivity. Only at the very highest frequency and conductivity is there a noticeable difference for the slow-wave factor β/β_0.

Lawton *et al.* [12] also investigated the two-layer dielectric microstrip line structure and proposed a general 2D equivalent circuit model, which allows for the losses in dielectric layers and the skin effect in metallization. Unlike previous papers [10][14], experimental results were used to determine the values of equivalent circuit parameters.

More generally, Brews [11] suggested an RLCG transmission line model for lossy waveguide interconnects in VLSI circuits. The distributed circuit parameters are given in term of integrated $\overline{E}$ and $\overline{H}$ fields. The integrals need to be adapted to the geometry of the interconnect cross section. Based on the Brews' method [11], Williams [15] investigated the fundamental TM_0 mode of 1D MIS transmission line. He developed closed-form expressions for 1D distributed circuit parameters, compared his results with those of full-wave calculations, and explored the limitations of his expressions. He also

showed that in certain fairly common circumstances, the TM_0 mode of propagation becomes so lossy that it could no longer be considered as a fundamental or dominant propagation mode.

In this chapter, we focus on a single interconnect in the MIS configuration, for such a simple case can help us understand the fundamental propagation mechanism in the MIS configuration. This interconnect topology refers to a situation where the backplane is used as current returning path. In Chapter 5, we will investigate another interconnect topology: coupled interconnects in the MIS configuration, where one of the coupled interconnects, called local ground wire, may be used as the current returning path.

There are three topics of interest in this chapter. At first, due to the finite width of the metal strip and finite conductivity of the semiconductor, a rigorous analysis of wave propagation of microstrip in an MIS configuration is difficult, and is really a 2D problem. To characterize on-chip interconnect design implemented with various technologies, we must take into account the fact that the geometrical and electrical parameters may change over wide ranges. Closed-form expressions are available for various ranges of parameters such as Tuncer *et al.*'s [14] and Williams' [15] models. However, the validity range of some expressions needs to be extended from 1D to 2D, such that quick and reasonably accurate characterization can be achieved.

Secondly, the frequency dependent transmission line parameters also need to be replaced, if possible, by frequency invariant parameters, because a circuit simulation with frequency invariant parameters is usually much quicker than a circuit simulation with frequency-dependent parameters. The parameters of an equivalent circuit model may be frequency dependent because of the skin effect in the metal strip, and because of the dielectric losses.

Finally, based on the distributed equivalent circuit parameters, equivalent circuit models can be constructed so that they can be directly embedded into commercial software such as SPICE for circuit simulations in time domain. In order to use simple equivalent circuit models, we need to determine the situations where the skin effect in the metal strip or the dielectric losses has to be considered. Here, we use the method introduced in the third chapter to estimate the simulation error between simplified and modified models. Based on the estimated values, a criterion can be given out to determine if the simple model is appropriate for a given error tolerance.

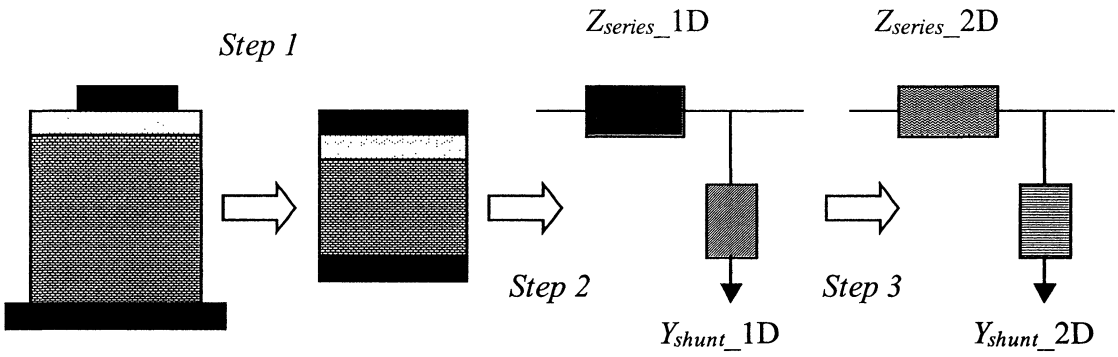
This chapter is organized as follows. In Section 4.2, based on existing literature, we extend the validity range of some closed-form expressions from 1D to 2D, and propose an RLCG-B model with five equivalent circuit parameters for an interconnect in the MIS configuration. In Section 4.3, the RLCG-B model in Section 4.2 is modified with invariant elements. In Section 4.4, a time-domain error bound is calculated using the method introduced in Chapter 3. We then use this bound to determine if the skin effect in the metal strip or the dielectric losses need to be included in circuit models for a single transmission net with source resistance R_S and load capacitance C_L. In Section 4.5, numerical simulations are performed to validate our RLCG-B model and demonstrate our criterion. The last section gives out our conclusions.

4.2 Original RLCG-B model

As mentioned above, closed-form expressions are available for various ranges of parameters such as Tuncer *et al.*'s [14] and Williams' [15] models. However, the validity range of these expressions needs to be extended from 1D to 2D, such that quick and reasonably accurate characterization can be achieved. In this chapter, based on existing literature, we propose using two equivalent widths for the physical metal strip, extend the validity range of some closed-form expressions from 1D to 2D, and propose

an original RLCG-B model with five equivalent circuit parameters for an interconnect in the MIS configuration. The contributions of semiconductor layer to series impedance and shunt admittance per unit length are estimated by the integral method [15].

There are three steps to construct the original RLCG-B model as illustrated in Figure 4.1. At first, based on simple formulas in [17] originally proposed by a number of authors [18][46][75-78], the effective parameters of an "equivalent" 1D MIS configuration are calculated from the physical parameters of the 2D MIS configuration. Secondly, based on a set of empirical formulas given in the literature [10][14,15], a group of 1D equivalent circuit parameters are obtained. By adjusting the 1D equivalent circuit parameters to account for the finite width of the strip, 2D equivalent circuit parameters are finally derived.



(a) 2D MIS ($w=w_m$) (b) Equivalent 1D MIS ($w=\infty$) (c) Equivalent 1D Model ($w=\infty$) (d) Equivalent 2D Model ($w=w_m$)

Figure 4.1: Steps for constructing the original RLCG-B model

4.2.1 Calculation of effective parameters for 1D MIS configuration

Cross sections of a 2D MIS configuration and the corresponding equivalent 1D structure are shown in Figures 4.2a and 4.2b, respectively. For equivalent 1D structure in Figure 4.2b, the left and the right boundaries of the multilayer structure are magnetic

walls. For the purpose of extracting 1D equivalent circuit parameters, the effective parameters of 1D MIS configuration need to be calculated from the physical parameters of the 2D MIS configuration. These effective parameters are geometrical and electrical parameters. The geometrical parameters are effective metal width eff_w_m, effective insulator thickness eff_t_i and semiconductor thickness eff_t_s. The electrical parameters are effective relative permittivities of insulator eff_ε_{ri} and semiconductor eff_ε_{rs}.

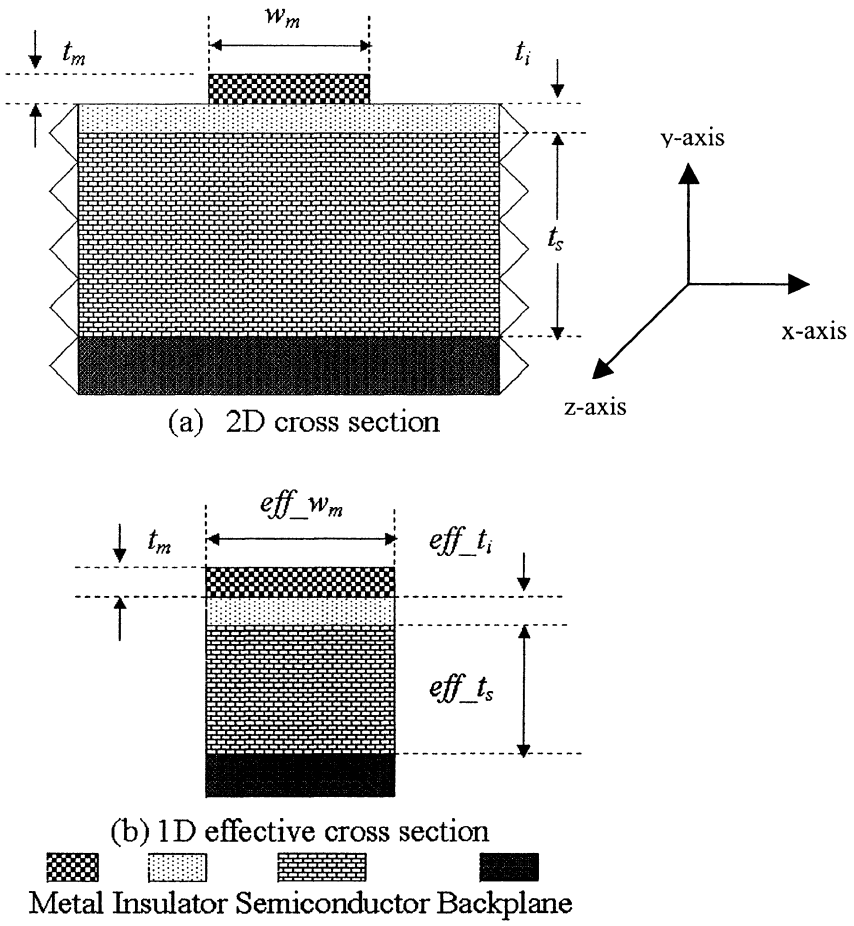


Figure 4.2: Cross section of a microstrip in the MIS configuration

For the electrical parameters, the effective permittivity eff_ε_{ri} and eff_ε_{rs} are given by Eq.4-1, which was originally proposed by Schneider [75], and later revised by Hammerstad [76]. This formula was called "S-H" formula by Collin [17].

$$eff\_\varepsilon_{rp} = \frac{\varepsilon_{rp}+1}{2} + \frac{\varepsilon_{rp}-1}{2\sqrt{1+12\frac{t_p}{w_m}}} - \frac{0.217(\varepsilon_{rp}-1)t_m}{\sqrt{w_m t_p}} \qquad \frac{w_m}{t_p} \geq 1$$

$$= \frac{\varepsilon_{rp}+1}{2} + \frac{\varepsilon_{rp}-1}{2\sqrt{1+12\frac{t_p}{w_m}}} - \frac{0.217(\varepsilon_{rp}-1)t_m}{\sqrt{w_m t_p}} + 0.02(\varepsilon_{rp}-1)\left(1-\frac{w_m}{t_p}\right)^2 \qquad \frac{w_m}{t_p} \leq 1 \tag{4-1}$$

where $p = i, s$. Here, subscript "i" stands for the insulator layer, and subscript "s" for the semiconductor layer. As mentioned in [17], by comparing the values from Eq.4-1 with the results obtained by solving integral equations, the agreement was better than 1% for $0.25 \leq \frac{w_m}{t_p} \leq 6$ and $1 \leq \varepsilon_p \leq 16$.

As to the geometrical parameters, the effective metal width eff_w_m is first calculated. The effective metal width eff_w_m is given by the expression in [17], which was originally proposed by Gunston and Weale [18]. The effect of finite thickness t_m for the microstrip on the distributed capacitance depends on the ratio of the metal width w_m to the thickness of the substrate t_p. In the MIS configuration there are two substrate layers: insulator and semiconductor. The ratio of the metal width w_m to the thickness of the substrate t_p changes dramatically as t_p varies from the thickness of insulator layer t_i to the thickness of semiconductor t_s. Thus, we propose to use two values of effective width eff_w_{mi} and eff_w_{ms} for the same physical width of metal wire, each width being relative to insulator and semiconductor layers, respectively. These two values of effective width eff_w_{mi} and eff_w_{ms} are calculated from Eq.4-2.

$$
\begin{aligned}
eff\_w_{mp} &= w_m + 0.398 t_m \left[1 + \ln\left(\frac{2t_p}{t_m}\right)\right] && \frac{w_m}{t_p} \geq \frac{1}{2\pi} \\
&= w_m + 0.398 t_m \left[1 + \ln\left(\frac{4\pi w_m}{t_m}\right)\right] && \frac{w_m}{t_p} \leq \frac{1}{2\pi}
\end{aligned}
\tag{4-2}
$$

where $p = i, s$.

Then, the effective thicknesses eff_t_i and eff_t_s are evaluated. As proposed by Hasegawa *et al.* [10], the effective thicknesses eff_t_i and eff_t_s are calculated from Eq.4-3, which was illustrated in [17] and contributed from a number of authors [46][76-78].

$$
\begin{aligned}
eff\_t_p &= \frac{eff\_w_{mp}}{r_{mp} + 1.393 + 0.667 \ln\left(r_{mp} + 1.444\right)} && r_{mp} = \frac{eff\_w_{mp}}{t_p} \geq 1 \\
&= \frac{eff\_w_{mp} \ln\left(\dfrac{8}{r_{mp}} + \dfrac{r_{mp}}{4}\right)}{2\pi} && r_{mp} = \frac{eff\_w_{mp}}{t_p} \leq 1
\end{aligned}
\tag{4-3}
$$

where $p = i, s$. Model with these effective parameters will be validated in Section 4.5.1.

4.2.2 Extraction of 1D equivalent circuit parameters ——R_m, R_s, L_m, L_i, L_s, C_i, C_s and G_s

Based on a set of empirical formulas given in the existing literature [10][14,15], the 1D equivalent circuit parameters R_m, R_s, L_m, L_i, L_s, C_i, C_s and G_s are calculated. Here R_m and L_m are the series resistance and inductance from the metal layer, L_i and C_i are the series inductance and shunt capacitance from the insulator layer. R_s, L_s, C_s, and G_s are the series resistance and inductance, and shunt capacitance and conductance from the semiconductor layer. The parameters R_m, L_m, L_i and C_i are called the elements of the conventional model, while the parameters R_s, L_s, C_s and G_s are called the elements of the integral model by Williams [15].

$$R_m + j\omega L_m \approx \frac{jz_{ym}}{\tanh(\theta_m)} \quad [\Omega] \quad (4\text{-}4a)$$

$$L_i = \mu_0 eff\_t_i \quad [H] \quad (4\text{-}4b)$$

$$C_i = \frac{\varepsilon_0 eff\_\varepsilon_{ri}}{t_i} \quad [F/m^2] \quad (4\text{-}4c)$$

and

$$R_s + j\omega L_s \approx \frac{\left[j\omega\mu_0(A_s + B_s) + j\omega eff\_\varepsilon_{rs}^* \varepsilon_0 \left|z_{ys}\right|^2 (A_s - B_s)\right]}{2\left|\cos(\phi_s)\right|^2} \quad [\Omega] \quad (4\text{-}4d)$$

$$G_s + j\omega C_s \approx \frac{j\omega eff\_\varepsilon_{rs} \varepsilon_0 \left|k_s^2\right| (A_s + B_s)}{2\left|\sin(\phi_s)\right|^2} \quad [S/m^2] \quad (4\text{-}4e)$$

where

$$A_s = \frac{\sin(2k_{s1} eff\_t_s)}{2k_{s1}} \quad [m] \quad (4\text{-}4f)$$

$$B_s = \frac{\sinh(2k_{s2} eff\_t_s)}{2k_{s2}} \quad [m] \quad (4\text{-}4g)$$

and β_0 is the propagation constant in free space

$$\beta_0^2 = \omega^2 \mu_0 \varepsilon_0 \quad [1/m^2] \quad (4\text{-}5)$$

ε_{rm}, ε_{rs} are the complex dielectric constants for metal and semiconductor layers, respectively

$$\varepsilon_{rm} = 1 - j\frac{\sigma_m}{\omega\varepsilon_0} \quad (4\text{-}6a)$$

$$\varepsilon_{rs} = 1 - j\frac{\sigma_s}{\omega\varepsilon_0} \quad (4\text{-}6b)$$

ε_{rs}^* is the conjugate of ε_{rs}

$$\varepsilon_{rs}^* = 1 + j\frac{\sigma_s}{\omega\varepsilon_0} \quad (4\text{-}6c)$$

γ_{z0} is the complex propagation constant along z-direction

$$\gamma_{z0}^2 = \left[\frac{1}{\sigma_m t_m} + j\omega\mu_0\left(eff\_t_i + eff\_t_s\right)\right]\left[\frac{j\omega\varepsilon_0}{\frac{eff\_t_i}{eff\_\varepsilon_{ri}} + \frac{eff\_t_s}{eff\_\varepsilon_{rs}}}\right] \quad [1/m^2] \quad (4\text{-}7a)$$

γ_{ym} and γ_{ys} [15] are the complex propagation constants along y-direction for metal and semiconductor layers, respectively

$$\gamma_{ym}^2 = -\varepsilon_{rm}\beta_0^2 - \gamma_{z0}^2 \quad [1/m^2] \quad (4\text{-}7b)$$

$$\gamma_{ys}^2 = -eff\_\varepsilon_{rs}\beta_0^2 - \gamma_{z0}^2 \quad [1/m^2] \quad (4\text{-}7c)$$

$$\gamma_{ys} = jk_s = j\left(k_{s1} + jk_{s2}\right) \quad [1/m] \quad (4\text{-}7d)$$

z_{ym} and z_{ys} [15] are the complex wave impedances along y-direction for metal and semiconductor layers, respectively

$$z_{ym} = \frac{\gamma_{ym}}{j\omega\varepsilon_{rm}\varepsilon_0} \quad [\Omega] \quad (4\text{-}8a)$$

$$z_{ys} = \frac{\gamma_{ys}}{j\omega\, eff\_\varepsilon_{rs}\varepsilon_0} = \frac{k_s}{\omega\, eff\_\varepsilon_{rs}\varepsilon_0} \quad [\Omega] \quad (4\text{-}8b)$$

θ_m and θ_s [15] are the complex phases for metal and semiconductor layers, respectively

$$\theta_m = \gamma_{ym} t_m = j\phi_m \quad (4\text{-}9a)$$

$$\theta_s = \gamma_{ys} eff\_t_s = j\phi_s \quad (4\text{-}9b)$$

4.2.3 Extraction of 2D equivalent circuit parameters ——*R*, *L*, C_1, C_2 and G_2

Once the effective equivalent parameters of the 1D structure are obtained, we construct a circuit model with five equivalent circuit parameters, as shown in Figure 4.3. This model is called original RLCG-B model in the following. Here, *R* and *L* are the series resistance and inductance, C_1 is the shunt capacitance contributed by the insulator layer,

and C_2 and G_2 are the shunt capacitance and conductance contributed by the semiconductor. According to 1D field analysis, the five circuit parameters can be calculated from the following equations:

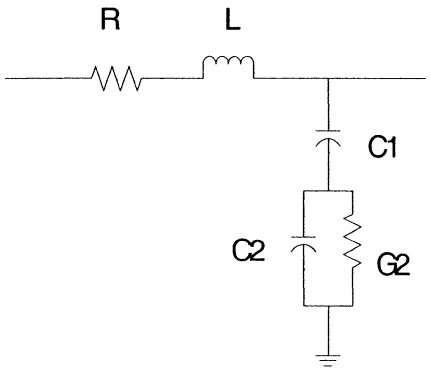


Figure 4.3: Original RLCG-B model

series elements :

$$R = \frac{R_m}{w_m} + \frac{R_s}{eff\_w_{ms}} \qquad [\Omega/\text{m}] \quad (4\text{-}10a)$$

and $$L = \frac{L_m}{w_m} + \frac{L_i}{eff\_w_{mi}} + \frac{L_s}{eff\_w_{ms}} \qquad [\text{H/m}] \quad (4\text{-}10b)$$

shunt elements:

$$C_1 = C_i eff\_w_{mi} \qquad [\text{F/m}] \quad (4\text{-}11a)$$

$$C_2 = C_s eff\_w_{ms} \qquad [\text{F/m}] \quad (4\text{-}11b)$$

and $$G_2 = G_s eff\_w_{ms} \qquad [\text{S/m}] \quad (4\text{-}11c)$$

It should be noted that different structure widths are used to compute the contributions of each substrate layer. As demonstrated later in Section 4.5.1, such process will slightly improve the accuracy of interconnect modeling.

4.3 Modified RLCG-B model

The equivalent circuit parameters R_m, L_m, R_s and L_s are generally frequency dependent. This dependence will be reflected in the circuit components of the RLCG-B model. Two main factors contribute to this frequency dependence. One is the skin effect in the metal strip [50], and the other is the dielectric losses. The shunt capacitance elements C_1 and C_2, and conductance element G_2 are almost constant in the original RLCG-B model. Thus, our attempt to obtain a frequency invariant model will focus on R and L.

The original RLCG-B model can be modified as shown in Figure 4.4 to remove the frequency dependence. Here, we select a network proposed in [53]. This topology approximates the frequency dependence of R and L with frequency independent parameters R_1, R_2, L_1 and L_2. Consequently, the total number of equivalent circuit parameters increases from 5 (original model) to 7 (modified model).

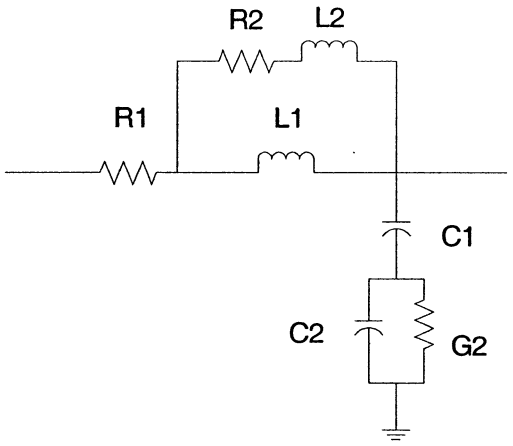


Figure 4.4: Modified RLCG-B model

For the original and modified models, the per-unit-length series impedances are expressed in Eqs.4-12a and 4-12b, respectively.

$$z_{series}(original) = R(\omega) + j\omega L(\omega) \tag{4-12a}$$

and $$z_{series}(modified) = R_1[1 + f(\omega)] + j\omega L_1[1 - g(\omega)] \tag{4-12b}$$

where $$f(\omega) = \frac{R_2}{R_1} \frac{\omega^2 L_1^2}{R_2^2 + \omega^2 (L_1 + L_2)^2} \tag{4-12c}$$

and $$g(\omega) = \frac{\omega^2 L_1 (L_1 + L_2)}{R_2^2 + \omega^2 (L_1 + L_2)^2} \tag{4-12d}$$

The values of new parameters R_1 and L_1 in the modified RLCG-B model are set to R and L of the original model at the lowest frequency (DC), where the functions $f(\omega)$ and $g(\omega)$ in Eqs.4-12c and 4-12d are much smaller than unity. The values of new parameters R_2 and L_2 in the modified model are determined by R and L of the original model at the highest frequency of interest and could also be obtained by other methods such as curve fitting or neural network [79]. Based on the values of R and L of the original model at the highest frequency point ω_h, we can obtain the values for $f(\omega_h)$ and $g(\omega_h)$.

$$f(\omega_h) \approx \frac{R(\omega_h)}{R_1} - 1 \tag{4-13a}$$

and $$g(\omega_h) \approx 1 - \frac{L(\omega_h)}{L_1} \tag{4-13b}$$

From Eqs.4-12c, 4-12d, 4-13a and 4-13b, we can derive R_2 and L_2 as

$$R_2 \approx R_1 \frac{\left(\frac{\omega_h L_1}{R_1}\right)^2}{f(\omega_h)\left\{1 + \left(\frac{\omega_h L_1}{R_1}\right)^2 \left[\frac{g(\omega_h)}{f(\omega_h)}\right]^2\right\}} \tag{4-14a}$$

$$\text{and} \quad L_2 \approx L_1 \frac{g(\omega_h)\left(\frac{\omega_h L_1}{R_1}\right)^2}{f^2(\omega_h)\left\{1+\left(\frac{\omega_h L_1}{R_1}\right)^2\left[\frac{g(\omega_h)}{f(\omega_h)}\right]^2\right\}} - L_1 \tag{4-14b}$$

As mentioned in [49], more R and L elements can be added if more accuracy is required.

The difference between the original and modified models can be easily obtained by comparing their respective series impedance per unit length in the frequency domain. The impact of such difference on the time domain waveform will be investigated in Section 4.5.1.

4.4 Impact of skin effect and dielectric losses

In order to use a simple model into circuit simulation software such as SPICE in view of time domain simulations, it is more accurate to model an on-chip interconnect by including both the skin effect in the metal strip and the dielectric losses. In the following, we first analyze the impact of not considering these physical effects on the circuit parameters. Then, by comparing such simplified models with the modified RLCG-B model including both the skin effect in the metal strip and the dielectric losses, we estimate the simulation error. Thus, for a given error tolerance, we can determine if simplified models are appropriate.

4.4.1 Impact of skin effect and dielectric losses on circuit models

One way to omit the impact of skin effect in the metal strip is to set the series resistance R_m and inductance L_m in Eqs.4-10a and 4-10b are set to their DC values, respectively.

There are two ways of neglecting the impact of dielectric losses. In one way, the series resistance R_s in Eq.4-10a and the shunt conductance G_s in Eq.4-11c need to be removed from the model, and the series inductance L_s in Eq.4-10b has to be set to its DC value. This corresponds to treating the silicon layer as a perfect insulator. In the other way, the silicon layer is treated as a perfect electric conductor. Thus, both C_2 and G_2 in Figure 4.4 are removed from equivalent circuit models.

Combining the impacts of skin effect and dielectric losses on the circuit parameters, we propose five simplified models A, B, C, D and E as listed in Table 4.1. The reference is a modified RLCG-B model with seven frequency invariant parameters as shown in Table 4.1. Model A only omits the skin effect, while model B only neglects the dielectric losses. Model C neglects both the skin effect and dielectric losses. As to models D and E, the silicon layer is assumed to be a perfect electric conductor. Model E omits the skin effect while model D doesn't.

Table 4.1: Model selection

Models	Series Elements	Shunt Elements	Features
A	R_1, L_1	C_1, C_2 and G_2	no skin effect
B	R_1, L_1, R_2 and L_2	$C=C_1C_2/(C_1+C_2)$	no dielectric losses [σ (substrate) = 0]
C	R_1, L_1	$C=C_1C_2/(C_1+C_2)$	no skin effect no dielectric losses [σ (substrate) = 0]
D	R_1, L_1, R_2 and L_2	C_1	no dielectric losses infinite σ substrate
E	R_1, L_1	C_1	no skin effect infinite σ substrate

4.4.2 Criterion for selecting simplified models

In order to determine if the simplified models are appropriate, they will be compared with the modified RLCG-B model. Here, we focus on a single transmission line net with source resistance R_S and load capacitance C_L, which approximates the case where two logic gates are connected by an interconnect as Hasegawa *et al.* [80] investigated. We use a pulsed voltage source and compare the differences of the load voltages between simplified and modified models.

At first, the complex propagation constant γ_z ($\sqrt{Z_{series}Y_{shunt}}$) and the complex characteristic impedance Z_C ($\sqrt{Z_{series}/Y_{shunt}}$) of five simplified models are compared with those of the modified model. The deviations of γ_z and Z_C for five simplified models from those of the modified model in frequency domain lead to the differences of load voltages in time domain, which can be estimated by using the technique developed in Chapter 3. Based on the obtained voltage difference, for a given error tolerance on the voltage waveform, we can finally determine if simplified models can be used.

4.4.2.1 Impacts of γ_z and Z_C on the voltage transfer function $H(s)$

We first investigate the impacts of γ_z and Z_C on the voltage transfer function $H(s)$ from the source to the load. The transfer function is expressed in terms of source impedance Z_S, load admittance Y_L ($1/Z_L$), the length of interconnect d, complex propagation constant γ_z and complex characteristic impedance Z_C ($1/Y_C$). Following the approach of Sections 3.4.1 and 3.4.2, we find:

$$H(s)=\frac{1}{\cosh(\gamma_z d)(1+Z_S Y_L)+\sinh(\gamma_z d)(Z_S Y_C+Z_C Y_L)} \tag{4-15}$$

$H(s)$ can be written in terms of $e^{\gamma_z d}$. Thus, the impact of γ_z on $H(s)$ can be illustrated by the way of comparing the magnitude and phase of $e^{\gamma_z d}$ for different models. As mentioned in Eq.3-18f, the product of γ_z and d is defined as the normalized complex propagation constant γ_n.

$$\gamma_n = \gamma_z d = (\alpha + j\beta)d = \alpha d + j\beta d \tag{4-16}$$

Here, the product of α and d is the value of attenuation in unit of "Neper" (Np) as signals travel through the interconnect, while the product of β and d is simply the value of phase delay in unit of radian as signals propagate from one end to the other end of the interconnect. At any given frequency, the performance of interconnect can be represented by a point in the αd-βd plane.

Alternatively, we propose to use the values of two products $8.686\alpha d$ and $\beta d/2\pi$ for a single frequency, in units of decibel (dB) and cycle (number of wavelength), as a newly defined normalized γ_n plane. The whole frequency range from DC to the highest frequency of interest can be mapped-out by a curve in this plane. Therefore, by comparing the curve of a simplified model with that of a reference, we can assess the differences of magnitude attenuation and phase delay between the model and the reference as signals travel through the interconnect.

The above process can be regarded as a mapping of the interconnect performance in the normalized γ_n plane. Such process is enlightened by Gupta *et al.* [21]'s work, where the parameters of interconnect were mapped in a normalized R_n-G_n-ω_n space. The three normalized parameters R_n, G_n and ω_n were defined as:

$$R_n = \frac{dR}{Z_0} \tag{4-17a}$$

$$G_n = \frac{dG}{Y_0} \tag{4-17b}$$

$$\omega_n = \omega T_f \tag{4-17c}$$

with

$$Z_0 = \frac{1}{Y_0} = \sqrt{\frac{L}{C}} \quad (4\text{-}17d)$$

$$T_f = \frac{d}{v_p} = d\sqrt{LC} \quad (4\text{-}17e)$$

Here, R, L, C and G are the per unit length parameters, and d is the length of wire. Z_0 and Y_0 are the characteristic impedance and admittance of a lossless transmission line (L and C), respectively. T_f is the propagation time for a lossless transmission line (L and C) of length d.

There are two advantages in using the normalized γ_n plane. One is that the normalized γ_n plane covers all kinds of interconnect while RC wires are not covered in the R_n-G_n-ω_n space, since L is equal to 0 in that case. The other is that, by partitioning the normalized γ_n plane properly, circuit designers are able to quantitatively define the "low-loss", "high-loss", "short" and "long" interconnects.

Let us now focus on the contribution of the complex characteristic impedance Z_C to $H(s)$. It can be noticed that in the right hand side of Eq.4-15, the complex characteristic impedance Z_C (=1/Y_C) appears in the second term of the denominator. At lower frequencies or for a short propagation distance, $\cosh(\gamma_z d)$ in the first term of the denominator is normally of order unity, while $\sinh(\gamma_z d)$ in the second term of the denominator is often much smaller than unity. In order to conveniently compare the magnitude levels of the two terms of the denominator in the right hand side of Eq.4-15, we rewrite Eq.4-15 in terms of Z^d_{series} and Y^d_{shunt} instead of Z_C and Y_C. Here, Z^d_{series} is the product of the length of wire d and the series impedance per unit length, while Y^d_{shunt} is the product of d and the shunt admittance per unit length.

$$\begin{aligned}\frac{1}{H(s)} &= \cosh(\gamma_z d)(1+Z_S Y_L)+\frac{\sinh(\gamma_z d)}{\gamma_z d}(Z_S\gamma_z dY_C+\gamma_z dZ_C Y_L)\\ &= \cosh(\gamma_z d)(1+Z_S Y_L)+\frac{\sinh(\gamma_z d)}{\gamma_z d}\left(Z_S Y^d_{shunt}+Z^d_{series}Y_L\right)\end{aligned} \tag{4-18a}$$

where

$$\begin{aligned}Z^d_{series} &= \gamma_z dZ_C\\ &= dR_1+\frac{d}{\frac{1}{sL_1}+\frac{1}{R_2+sL_2}}\end{aligned} \tag{4-18b}$$

and

$$\begin{aligned}Y^d_{shunt} &= \gamma_z dY_C\\ &= \frac{d}{\frac{1}{sC_1}+\frac{1}{G_2+sC_2}}\end{aligned} \tag{4-18c}$$

At lower frequencies or for short propagation distances, the magnitudes of $\cosh(\gamma_z d)$ and $\sinh(\gamma_z d)/(\gamma_z d)$ are both of order unity in Eq.4-18a. Thus, we just need to compare the magnitudes of the two products $Z_S Y^d_{shunt}$ and $Z^d_{series}Y_L$ with the term $(1+Z_S Y_L)$. If the products $Z_S Y^d_{shunt}$ and $Z^d_{series}Y_L$ are much smaller than this term, the voltage transfer function $H(s)$ will be dominated by the first term in Eq.4-18a. In such situation, the difference of Z_C between simplified and modified models has much less impact on the transfer function.

As to higher frequencies or long propagation distances, $\cosh(\gamma_z d)$ and $\sinh(\gamma_z d)/(\gamma_z d)$ do not remain of order unity in Eq.4-18a. Moreover, the two products $Z_S Y^d_{shunt}$ and $Z^d_{series}Y_L$ become comparable in magnitude to the factor of $(1+Z_S Y_L)$. Thus, the second term in Eq.4-18a does make contributions to the voltage transfer function $H(s)$.

In such situation, we must pay attention to the differences of Z_C between simplified and modified models.

The impact of complex characteristic impedance Z_C on $H(s)$ can be elucidated by comparing the magnitudes of the two products $Z_S Y^d_{shunt}$ and $Z^d_{series} Y_L$ with the factor of $(1+Z_S Y_L)$. The deviations of γ_z and Z_C for five simplified models from those of the modified model in frequency domain lead to the differences of load voltages in time domain, which we will now investigate by using the transfer function $H(s)$.

4.4.2.2 Estimation of simulation errors

By combining the spectrum of the voltage source with the difference of voltage transfer functions between simplified and modified models, we now apply the method developed in Chapter 3 to estimate the time-domain simulation errors. As explained before, the whole frequency range is divided into three regions, based on the bandwidth of the voltage source with or without considering the bandwidth of the system. Here, the bandwidth of the system can be approximately estimated. So the bandwidth of the voltage signal on the load will be determined by the bandwidths of both the voltage source and the system.

As mentioned in Section 3.2.2, the bandwidth of the voltage source is related to the rising and falling times of the pulse, and is labeled by two frequencies $f_{h1}(=0.35/t_r)$ and $f_{h2}(=1/t_r)$. Here, t_r is the rising time of the pulse. For simplicity, we assume that the rising and falling times of the pulse are the same.

Similarly, the bandwidth of the system is estimated by replacing the rising time t_r of pulse source with a threshold time delay $T_{0.9}$ ($90\%Vdd$) defined as the time taken to accomplish 90% of the full voltage swing. For an on-chip RC transmission line net with

source resistance R_S and load capacitance C_L, $T_{0.9}$ can be obtained from the Elmore delay τ_{ED} [70,71] as in [81].

$$T_{0.9} = 2.3\tau_{ED} \tag{4-19a}$$

where $$\tau_{ED} = R_S\left(dC_w^l + C_L\right) + dR_w^l\left(\frac{dC_w^l}{2} + C_L\right) \tag{4-19b}$$

Here d is the length of transmission line. R_w^l and C_w^l are the wire resistance and capacitance per unit length, respectively. For an on-chip RLC transmission line net with source resistance R_S and load capacitance C_L, $T_{0.9}$ can be obtained as in [82].

$$\begin{aligned} T_{0.9} &= \frac{4.72b_2}{b_1 - \sqrt{b_1^2 - 4b_2}} && \text{if } b_1^2 - 4b_2 > 0 \\ &= 1.95b_1 && \text{if } b_1^2 - 4b_2 = 0 \\ &= \frac{3.32b_2}{\sqrt{4b_2 - b_1^2}} && \text{if } b_1^2 - 4b_2 < 0 \end{aligned} \tag{4-20a}$$

where

$$b_1 = R_S\left(dC_w^l + C_L\right) + dR_w^l\left(\frac{dC_w^l}{2} + C_L\right) \tag{4-20b}$$

and

$$b_2 = d^2R_w^lC_w^l\left(\frac{R_SC_L}{2} + \frac{dR_SC_w^l}{6} + \frac{dR_w^lC_L}{6} + \frac{d^2R_w^lC_w^l}{24}\right) + dL_w^l\left(\frac{dC_w^l}{2} + C_L\right) \tag{4-20c}$$

Here d is the length of transmission line. R_w^l, L_w^l and C_w^l are the wire resistance, inductance and capacitance per unit length, respectively. It can be noticed that b_1 is simply the Elmore delay τ_{ED} [70,71]. As a first estimation, we use R_1, L_1 and C_1 to replace R_w^l, L_w^l and C_w^l in Eqs.4-20a, 4-20b and 4-20c.

Thus, the bandwidth of the voltage signal on the load is approximately determined by the bandwidth of the pulse voltage source if $T_{0.9}$ is smaller than t_r, otherwise, it is

determined by that of the system. Therefore, we use the maximum value of $T_{0.9}$ and t_r to calculate the two frequency points f_{h1} and f_{h2}.

$$f_{h1} = \frac{0.35}{\tau} \tag{4-21a}$$

and

$$f_{h2} = \frac{1}{\tau} \tag{4-21b}$$

where

$$\tau = \max(T_{0.9}, t_r) \tag{4-21c}$$

By using the above two frequencies f_{h1} and f_{h2}, the whole frequency range is divided into three regions I, II and III. As explained in Section 3.2.2, Region I is from DC to f_{h1}, Region II from f_{h1} to f_{h2}, and Region III from f_{h2} to $f_s/2$. Here, f_s is the sampling frequency related to the reciprocal of the time step used in the time domain solution. Most of the energy is concentrated in Regions I and II, where the modeling accuracy has great impact on the simulation error.

Following the procedure of Chapter 3, we can now estimate the maximum difference Δ between the output waveforms of the reference and simplified models.

4.5 Numerical simulations

In this section, we first validate our RLCG-B model. Here, we evaluate the accuracy of both the original and modified models. Then, we compare the difference between simplified and modified models in time and frequency domains.

4.5.1 Validation of the RLCG-B model

Once the 2D equivalent circuit parameters of an original RLCG-B model have been obtained, the propagation constant γ_z and the characteristic impedance Z_C can be calculated by the equations below

$$\gamma_z = \sqrt{z_{series} y_{shunt}} \tag{4-22a}$$

and $$Z_C = \sqrt{\frac{z_{series}}{y_{shunt}}} \tag{4-22b}$$

where $$z_{series} = (R + j\omega L) \tag{4-22c}$$

and $$y_{shunt} = \frac{1}{\frac{1}{j\omega C_1} + \frac{1}{G_2 + j\omega C_2}} \tag{4-22d}$$

γ_z and Z_C of the original RLCG-B model can then be compared with those predicted by numerical solutions of Maxwell equations.

Based on the original RLCG-B model, a modified RLCG-B model is constructed. Its new parameters R_1 and L_1 are set to the DC values of R and L in the original RLCG-B model, and R_2 and L_2 are derived from Eqs.4-14a and 4-14b. Thus, we check the accuracy of modified RLCG-B model by comparing its series impedance per unit length with that of the original RLCG-B model.

The physical parameter values used for the sake of validation are listed in Table 4.2. These values correspond to typical cases encountered in VLSI interconnects. Agilent Technologies ADS Momentum simulations, which can solve Maxwell's equations in lossy transmission line structures in the 2D and 3D planar MIS configuration (often referred to as 2.5D), is used to validate our model. The electromagnetic simulation results are compared with those of our original RLCG-B transmission line model. Here, frequency is scanned logarithmically from 1 MHz to 10 GHz.

Table 4.2: Main parameters in the MIS configuration

Parameters	Values	Parameters	Values (μm)
ε_{ri}	3.82	w_m	1 and 10
ε_{rs}	11.9	t_m	1
ρ_s (Ω·cm)	1 and 100	t_i	1
σ_m(S/m) (Copper)	5.7×10^7	t_s	300

A summary of the differences between simulation results and those of our model are listed in Tables 4.3a and 4.3b for the semiconductor resistivity ρ_s of 1 and 100 Ω·cm. The average relative difference of γ_z varies from 0.68% to 2.3%, and the average relative difference of Z_C ranges from 0.64% to 3.5%. It can be seen that good agreement is obtained between our model and Agilent Technologies ADS Momentum simulations.

Table 4.3a: Differences of γ_z and Z_C
between full-wave field analysis and original RLCG-B circuit model (ρ_s=100 Ω·cm)

	Relative difference of Z_C (%)		Relative difference of γ_z (%)	
w_m(μm)	Average	Standard Deviation	Average	Standard Deviation
1	1.5	0.63	3.3	1.8
2	2.0	0.68	3.3	1.1
5	1.8	0.20	2.2	0.44
10	1.3	0.21	1.1	0.11
20	0.89	0.35	0.64	0.24

Table 4.3b: Differences of γ_z and Z_C
between full-wave field analysis and original RLCG-B circuit model (ρ_s=1 Ω·m)

	Relative difference of Z_C (%)		Relative difference of γ_z (%)	
w_m (μm)	Average	Standard Deviation	Average	Standard Deviation
1	2.0	0.24	2.7	1.1
2	2.3	0.36	3.5	1.2
5	1.7	0.42	2.7	0.92
10	1.1	0.49	1.6	0.61
20	0.68	0.53	0.85	0.57

Figures 4.5 and 4.6 show the complex propagation constant γ_z and characteristic impedance Z_C as a function of frequency with ρ_s = 1 Ω·cm for a metal strip width of w_m =1 μm. Here, the simulation results are also compared with those of Tuncer *et al.*'s [14] model.

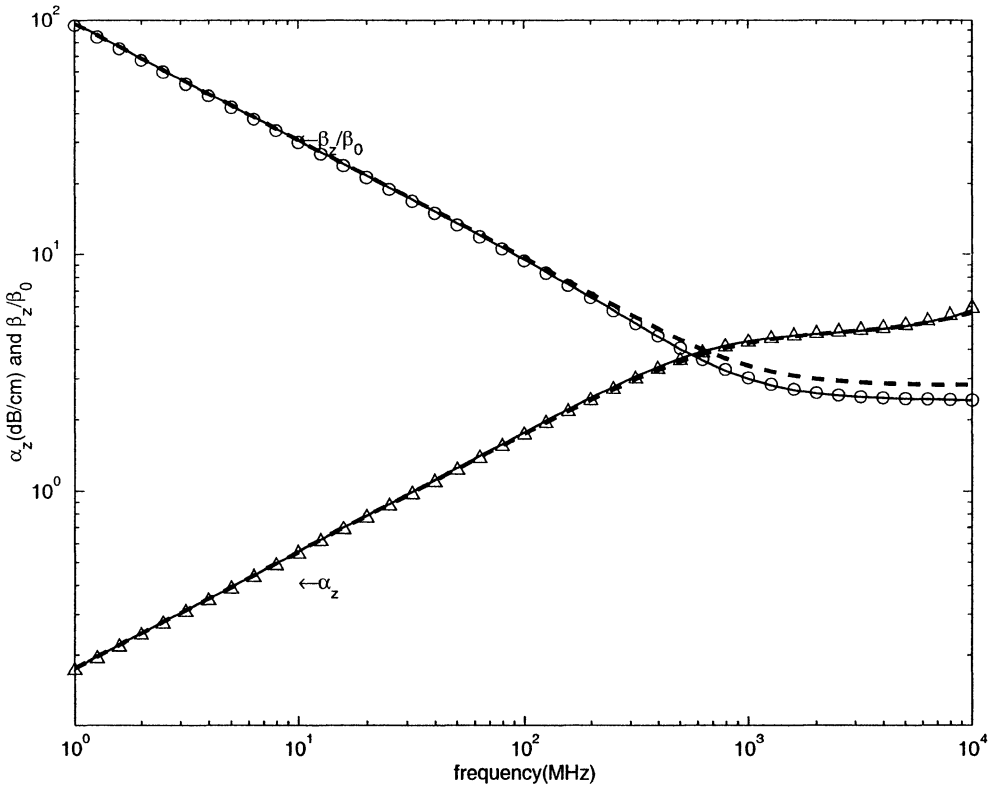


Figure 4.5: Comparison of propagation constant γ_z among Agilent-ADS, Tuncer *et al*'s model and ours, for the parameters given in Table 4.2 with w_m =1 μm and ρ_s =1 Ω·cm
("Δ" and "o" : α_z, and β_z/β_0 of ADS, and solid lines: our model, and dashed lines: Tuncer *et al*'s model.)

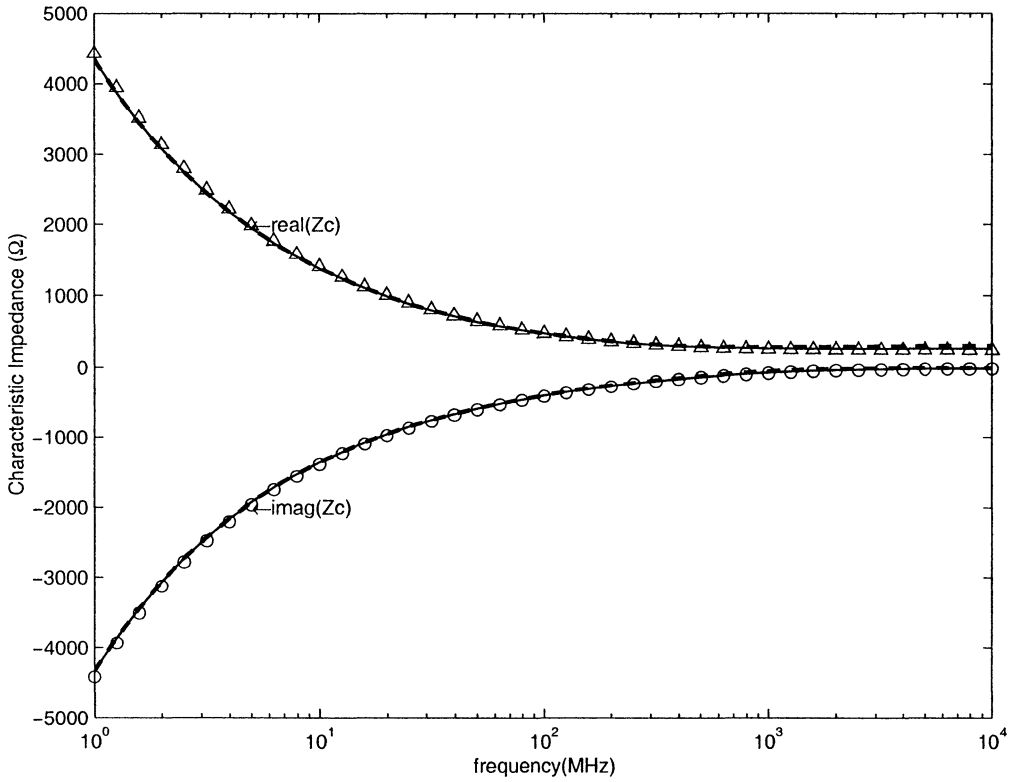


Figure 4.6: Comparison of characteristic impedance Z_C among Agilent-ADS, Tuncer *et al*'s model and ours, for the parameters given in table 4.2 with w_m =1 μm and ρ_s=1 Ω·cm
("Δ" and "o" : real and imaginary parts of Z_C from ADS, and solid lines: our model, and dashed lines: Tuncer et al's model.)

As seen in Figure 4.5, a good agreement is achieved between our model, Tuncer *et al*'s model and full-wave ADS simulation, except that there is a slight difference between Tuncer *et al*'s model and ADS simulation. Therefore, using two values of effective trace width, as proposed in the thesis has led to improved results but only at very high frequencies. From Figure 4.6, the deviation of curves for both Tuncer *et al*'s model and ours from the one with full-wave ADS simulation is barely visible. Thus, we have slightly improved the accuracy of quasi-static models for a very narrow microstrip in the most interesting frequency and resistivity regions in VLSI circuits (frequency up to 10 GHz and semiconductor resistivity more than 1 Ω·cm).

Besides validating the original RLCG-B model in Figure 4.3, the above physical parameters in Table 4.2 are also used to check the accuracy of the modified RLCG-B model implemented with a RL network of frequency invariant parameters in Figure 4.4. The difference between the original and the modified models is the series impedance Z_{series}. Thus, we only need to compare the real and imaginary parts of Z_{series} between these two models. Typical curves of resistance (Re$\{Z_{series}\}$) and reactance (Im$\{Z_{series}\}$) in both cases are displayed in Figure 4.7, and the differences are barely visible.

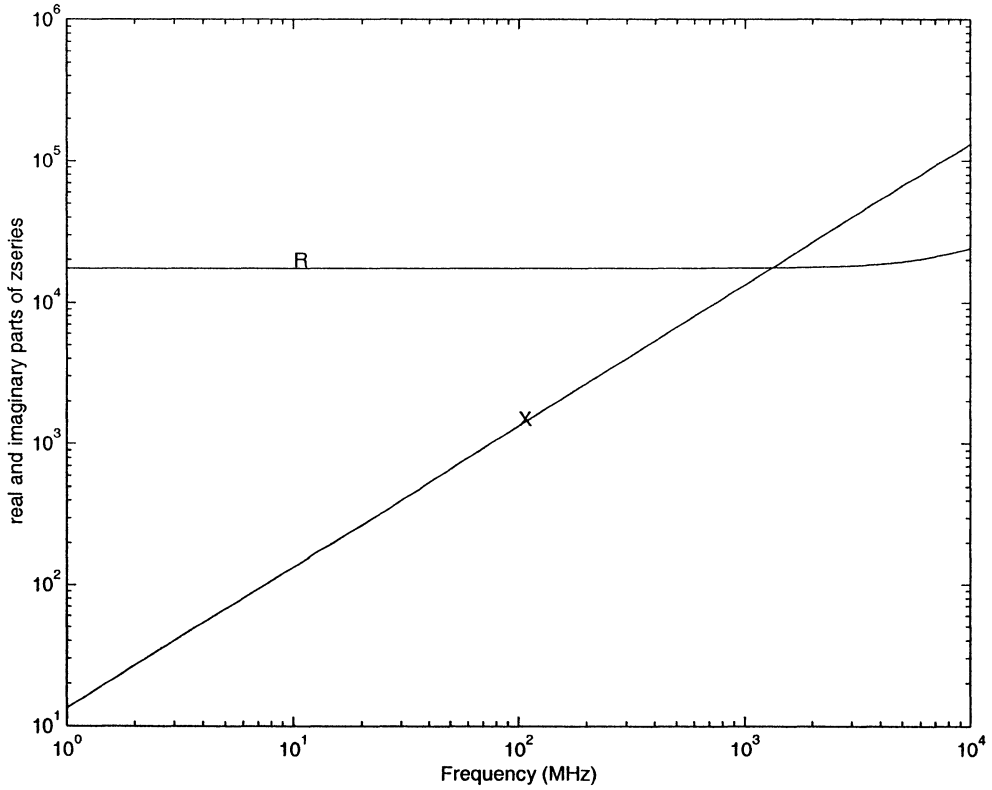


Figure 4.7: Comparison of series impedance Z_{series} between modified and original RLCG-B circuit models

Two groups with semiconductor resistivity of 1 and 100 Ω·cm were compared for the highest frequency of interest up to 10 GHz, and were listed in Table 4.4. As can be seen

in Table 4.4, the average relative difference of series impedance between two models is below 0.29% and a good agreement has been achieved.

Table 4.4: Differences of Z_{series}
between modified and original RLCG-B circuit models

w_m(μm)	Relative Difference (%) (ρ_s=100Ω·cm)		Relative Difference (%) (ρ_s=1Ω·cm)	
	Average	Standard Deviation	Average	Standard Deviation
1	0.0029	0.0055	0.29	0.55
2	0.0019	0.0034	0.19	0.34
5	0.0010	0.0018	0.096	0.17
10	0.0006	0.0010	0.042	0.071

4.5.2 Demonstration of error criterion

In this sub-section, an interconnect having the physical parameters given in Table 4.2 is used to demonstrate the validity of the error bound given in the previous section. We will attempt to predict the error resulting from the omission of the skin effect in the metal strip or the dielectric losses on the time domain response. For all the examples shown here, the width of metal strip and the conductivity of semiconductor were maintained to 1 μm and 10 Ω·cm, respectively. In order to analyze signal integrity, a transmission line net with source resistance R_S of 1 kΩ (representative of a 20 square wide driving transistor) and load capacitance C_L of 0.1 pF was utilized. The stimulus was a 1-volt voltage source with a pulse width of 5 ns, with rise and fall times of 0.5 ns. A wire length of 1cm was used. Below, five simplified models A, B, C, D and E in Table 4.1 were compared with the complete modified model, which was used as a reference in the following.

As mentioned in Section 4.4.2.2, the system bandwidth can be estimated Using Eq.4-20a for the RLC wire, the threshold time delay $T_{0.9}$ is 1.023 ns. Using Eq.4-19a for RC

wire, the Elmore delay τ_{ED} is 0.45 ns and the threshold time delay $T_{0.9}$ ($2.3\tau_{ED}$) is 1.047 ns. The small difference between these two delay values results from the overdamped response. As a first approximation, for this special case, the system bandwidth can still be estimated using the Elmore delay.

Here, the threshold time delay $T_{0.9}$ ($2.3\tau_{ED}$) is larger than the source transition times. Therefore, the bandwidth of the output voltage signal is determined by the threshold time delay $T_{0.9}$ ($2.3\tau_{ED}$). From Eqs.4-21a and 4-21b, two frequencies f_{h1}=334 MHz and f_{h2}=955 MHz are obtained. By using these two frequencies, the whole frequency range is divided into three regions I, II and III. Here, the sampling frequency f_s is set to 12.8 GHz, which is far above the –3 dB cutoff frequency f_{h1}.

Below we first consider the transmission line only, and compare the differences of the propagation constant γ_z and the characteristic impedance Z_C. Then, we analyze the transmission line net and compare the voltage transfer function $H(s)$ between the simplified models and the reference. Finally, we combine the spectrum of the pulse source with the above differences of voltage transfer functions and estimate the absolute differences of load voltages between the simplified models and the reference.

4.5.2.1 Propagation constant γ_z and characteristic impedance Z_C

The propagation constant γ_z of the simplified models and the reference 7-term model is mapped in a normalized γ_n plane in Figure 4.8, where the coordinates of a point in the normalized γ_n plane are composed of the phase and magnitude of e^{γ_n}. The magnitude stands for attenuation while the phase represents phase delay as a signal travels through such interconnect with a length of d. Here, the signal frequency is scanned from 1 MHz to 10 GHz.

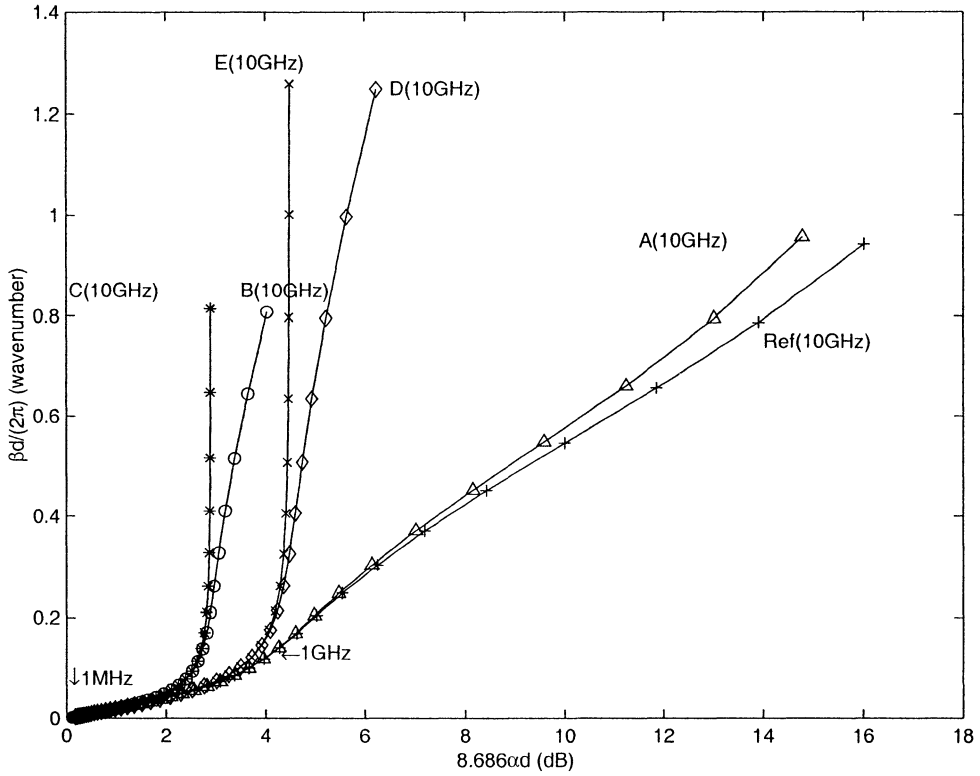


Figure 4.8: Comparison of magnitude and phase of e^{γ_n} between simplified models and reference

In Figure 4.8, "Δ", "o", "*", "×" and "◊" are used for the values of simplified model A, B, C, D and E, respectively. "+" represents those of the modified model used as a reference. As expected, the magnitude attenuation and phase delay of a signal with simplified models deviate from those of a signal with the modified model. For model A, the separation of curves begins at higher frequencies. For model B, the separation of curves occurs at middle frequencies and remains up to higher frequencies. As for model C, it combines both models A and B, and the deviation from the modified model begins at middle frequencies and increases at higher frequencies. In companying members of pairs Ref. vs. A, D vs. E and B vs. C, it appears that neglecting skin effect has a relatively small effect on e^{γ_n}. Starting with the zero resistivity substrate (D & E), the attenuation increases for the finite resistivity cases (Ref. & A) and then decreases to much lower values for the cases of infinite resistivity (B & C).

The real and imaginary parts of the complex characteristic impedance Z_C for the simplified models and the reference are shown in Figure 4.9. The differences between models A, D & E and the reference are barely visible over the complete frequency range. For models B & C, the two curves differ from the reference at low frequencies but merge to the reference case at high frequencies.

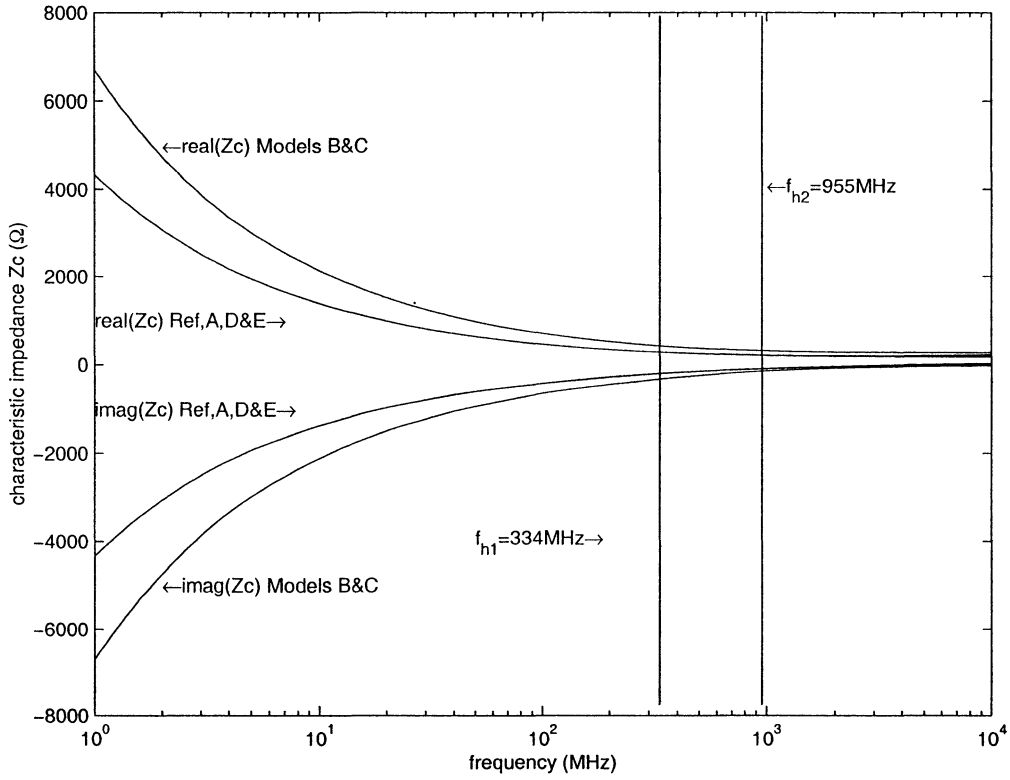


Figure 4.9: Comparison of characteristic impedance Z_C between simplified models and reference

4.5.2.2 Voltage transfer function $H(s)$

Figure 4.10a shows the magnitude of the voltage transfer function $H(s)$ for the simplified models and the reference. In Figure 4.10a, "Δ", "o", "*", "×" and "◊" stand for the values of model A, B, C, D & E, while "+" represents those of the modified model used as a reference. Here, all the distributed models are replaced by a cascade

connection of 16 lumped T-sections. We used the above transmission lines with source impedance of 1 kΩ and load capacitance of 0.1 pF, and calculated the voltage transfer function $H(s)$. As illustrated in Figure 4.10a, the differences between models A, D and E and the reference are invisible in frequency Regions I & II, and appear in Region III. The curves for models B and C separate from that of the reference in the frequency region I.

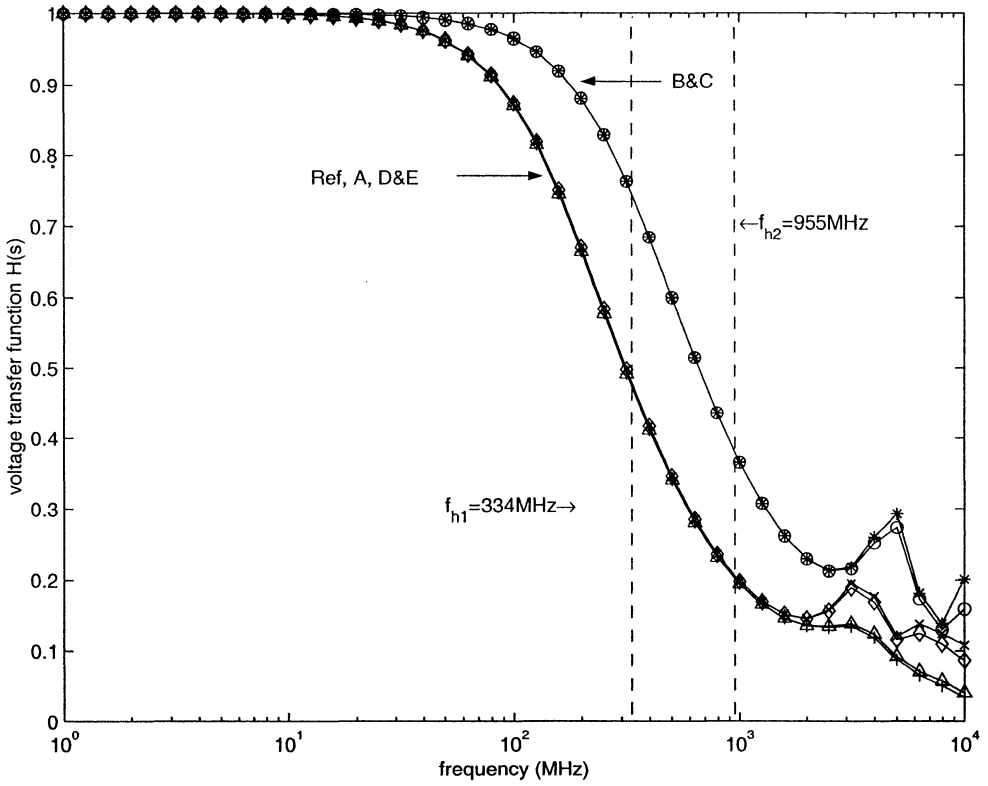


Figure 4.10a: Comparison of magnitudes of voltage transfer functions $H(s)$ between simplified models and reference

The real and imaginary parts of the voltage transfer functions $H(s)$ are shown in Figure 10b. The curves for the simplified models A, B, C, D and E are merged with that of the reference at low frequencies as expected. As frequency increases, three pairs of curves, Ref. and A, D and E, and B and C, then diverge each other. There is small difference between the curve of model A and that of the reference, while there is large difference

between the curve of model B (or C) and that of reference at high frequencies. The difference between the curve of model D (or E) and that of the reference is small, compared to the difference between the curve of model B (or C) and that of reference at high frequencies.

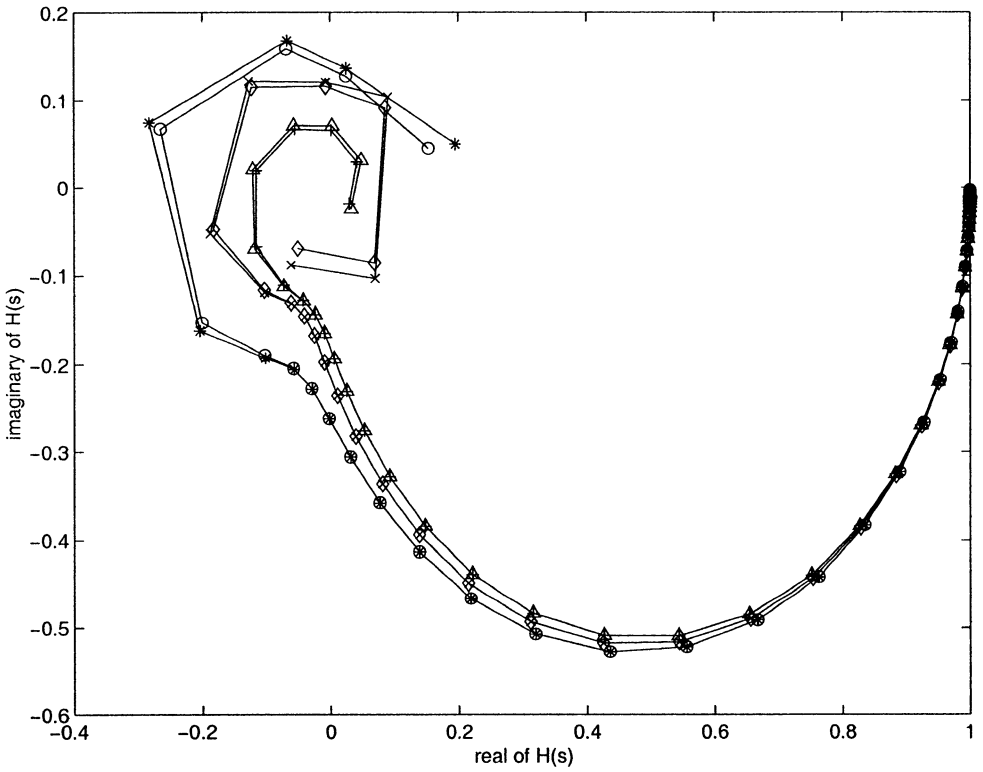


Figure 4.10b: Comparison of real and imaginary parts of voltage transfer functions $H(s)$ between simplified models and reference

We will now see how these model differences translate into error on the time domain waveform. The same transmission line as above with source impedance of 1 kΩ and load capacitance of 0.1 pF, was used to calculate the waveforms of output voltage on the load. Figure 4.11 shows the time domain waveforms of load voltages $v_L(t)$ for the simplified models and the reference. Here, all the distributed models are replaced by a cascade connection of 16 lumped T-sections.

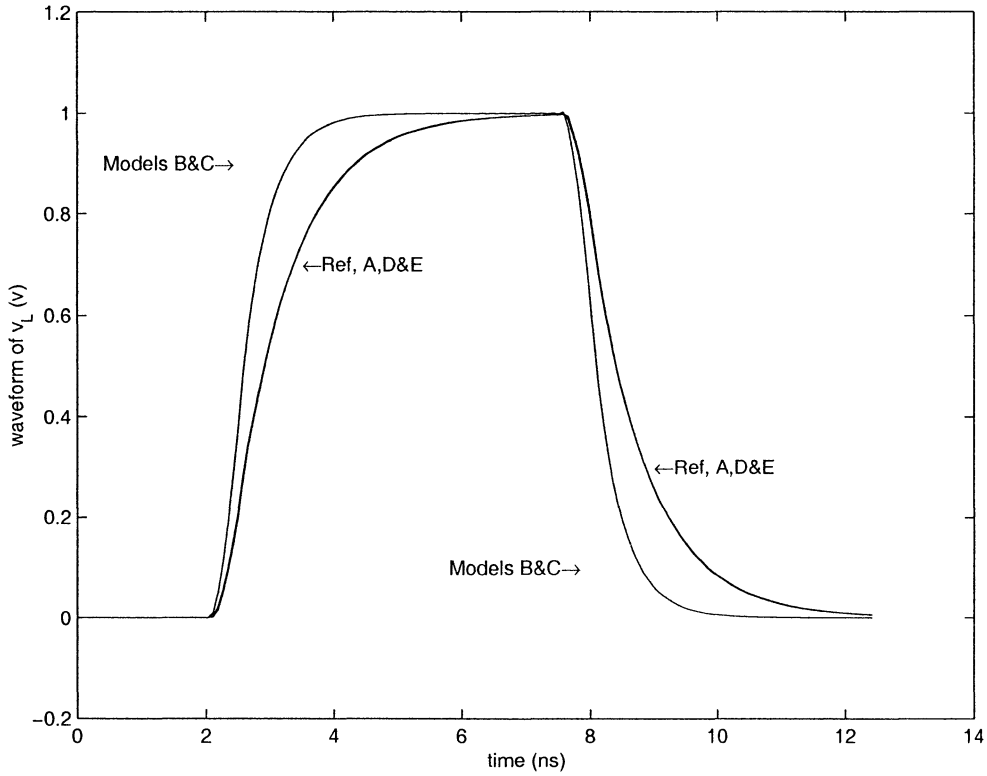


Figure 4.11: Comparison of load voltages $v_L(t)$ between simplified models and reference

As mentioned in Section 4.5.2, all the frequency range is divided into three regions I, II and III with f_{h1}=334 MHz, f_{h2}=955 MHz and f_s=12.8 GHz, which is far above the highest frequency of interest f_{h2}. Based on the absolute differences of voltage transfer functions between the simplified models and the reference, and on the pulse source's spectrum, the respective upper limits of absolute difference of time-domain load voltages are computed. These estimated results are listed in Table 4.5. The contributions from the three frequency sub-regions are shown separately in the three last columns and the sum of contributions appears in the third column. The simulated results are listed in the second column, which are obtained from Agilent Technologies ADS circuit simulations with a maximum time step of 0.078 ns (=$1.0/f_s$).

Table 4.5: Upper limits of voltage differences for a 1-volt pulse (unit: mV)

Models vs. Reference	Simulated Δ_{vL}	Estimated Δ_{vL}			
		Regs. I+II+III	Reg. I	Reg. II	Reg. III
A vs. Ref.	0.20	0.29	<0.01	0.02	0.26
B vs. Ref.	2.6×10^2	3.9×10^2	2.7×10^2	93	27
C vs. Ref.	2.6×10^2	3.9×10^2	2.7×10^2	93	27
D vs. Ref.	9	16	5	5	6
E vs. Ref.	10	16	5	5	6

For simplified model A, the estimated voltage difference and the difference obtained by simulation are quite small. Most of the contribution to the estimated difference originates from the higher frequency sub-region. Neglecting region III's contribution would result in a difference of 0.17 mV between the simulated and estimated Δv_L. However, 0.17 mV is only 0.017% of the voltage swing and is comparable to the simulation accuracy.

For simplified models B and C, the estimated Δv_L exceeds the simulated Δv_L by 50%. Here, the transfer function's difference in the first frequency sub-region is the dominant contribution and clearly, neglecting the contributions from sub-region III would have an insignificant effect.

For simplified models D and E, the estimated Δv_L exceeds the simulated Δv_L by 78% and 60% respectively. Moreover, the absolute errors between the simulated and estimated values are only 7 and 6 mV, which represents 0.7% and 0.6% of the full voltage swing.

From Table 4.5, we observe that the estimated values consistently give an upper limit for the maximum difference of load voltages between the simplified and modified

models. It is conjectured that the estimate is indeed an upper bound, but detailed analysis of this phenomenon is left for further research. Based on these estimated results, we can determine if the simplified models are appropriate for a given error tolerance. In this particular example, omitting skin effect in the metal strip (case A) mostly contributes to errors in the higher frequency range and has much less impact on the error than omitting the silicon conductivity (cases B & C). Finally, if the substrate is modeled as a perfect conductor (cases D & E), the origin of the estimated Δv_L is spread almost evenly over the whole spectrum, as indicated in Table 4.5. In fact, there are large discrepancies on the transfer functions at the higher end of the spectrum, as seen in Figure 4.10b, but they are alleviated by the lighter weight of the source's spectrum in this frequency range.

4.6 Summary

In this chapter, a practical approach to model MIS interconnects in VLSI circuit has been presented. Based on existing literature, we proposed to use two equivalent widths for the physical metal strip. This has extended the validity range of some closed-form expressions from 1D to 2D. We also proposed an original RLCG-B model with five equivalent circuit parameters for an interconnect in the MIS configuration. Numerical simulations have validated the original RLCG-B models for the highest frequency up to 10 GHz and the substrate resistivity more than 1 Ω·cm.

In order to obtain a model with frequency invariant parameters, the original RLCG-B model is then modified with seven equivalent frequency independent circuit parameters. The values of new circuit parameters are calculated by analytical equations. Numerical simulations have been used to check the accuracy of series impedance per unit length of the modified RLCG-B model. The difference between the modified and original models is small and negligible. Thus, below the modified model is used as a reference in the next chapter.

For the purpose of validating simple equivalent circuit models into simulation software such as SPICE, we propose a bound to determine the maximum error on time domain waveform. This bound can be used for example to decide whether the skin effect in the metal strip or the dielectric losses should be considered in circuit models. Here, we focused on a transmission line with source resistance R_S and load capacitance C_L. By combining the spectrum of a voltage source with the differences of voltage transfer functions between the simplified models and the reference, we estimate the absolute differences of load voltages between the simplified models and the reference. Thus, for a given error tolerance, we can decide if the simplified models are appropriate. Using this approach for validation, it was found that: 1.neglecting skin effect in the metallic strip has no visible influence on the time domain waveform; 2.treating the semiconductor layer as a perfect conductor leads to equally good results; 3.treating the semiconductor layer as an insulator leads to large discrepancies that may not be acceptable in interconnect performance analysis.

In the next chapter, we will investigate another interconnect topology composed of two coupled interconnects in the MIS configuration, where one of the two interconnects is used as a current returning path.

CHAPTER 5

MODELING OF COUPLED INTERCONNECTS IN THE MIS CONFIGURATION

5.1 Introduction

The previous chapter discusses one interconnect topology: a single wire in the MIS configuration, where the back metal plane is used as current returning path. In this chapter, we investigate another interconnect topology: two coupled wires in the MIS configuration, where one of the two wires is used as the current returning path. It will be assumed that the driver and the load at each end are balanced [83] and that the structure is *E*-symmetrical with respect to a plane passing between the two wires. Under these conditions, the two-wire interconnect can be analyzed by considering the existence of the differential mode (odd mode) and neglecting the common mode. The generalization of the modeling technique presented here to the case of the N-wire interconnect is not covered and should be the object of future work. The purpose of this chapter is to illustrate the difference between two interconnect topologies, differing by the role of the back metal plane as connected or unconnected conductor.

In this chapter, based on the original RLCG-B model for a single interconnect proposed in Section 4.2, and other models available in the literature, a hybrid RLCG-B model is first proposed for the odd-mode of two coupled wires. The hybrid RLCG-B model is then evolved into a simple RLC model by assuming that the semiconductor behaves as an ideal ground plane (Section 5.2). The simple RLC model was validated by comparing the complex propagation constant of the model with the one of the physical structure analyzed with an electromagnetic field solver, namely, ADS Momentum from Agilent Technologies (5.3).

5.2 Odd-mode model of two coupled interconnects

Closed-form expressions for the capacitances and inductances of multi-wire systems are given for various ranges of geometry parameters by many authors such as Delorme *et al.* [84] and Lewis [85]. In this section, we apply these expressions to the original RLCG-B model in Section 4.2 and propose a hybrid RLCG-B model for the odd-mode of two coupled interconnects. The hybrid RLCG-B model is then evolved into a simple RLC model for practical applications.

5.2.1 Coupled interconnects in the MIS configuration

The topology of two coupled interconnects in the MIS configuration is shown in Figure 5.1. Although this structure supports a symmetrical odd-mode or differential mode, it is common to call one of the two wires the "signal" line, while the other is called the current returning path.

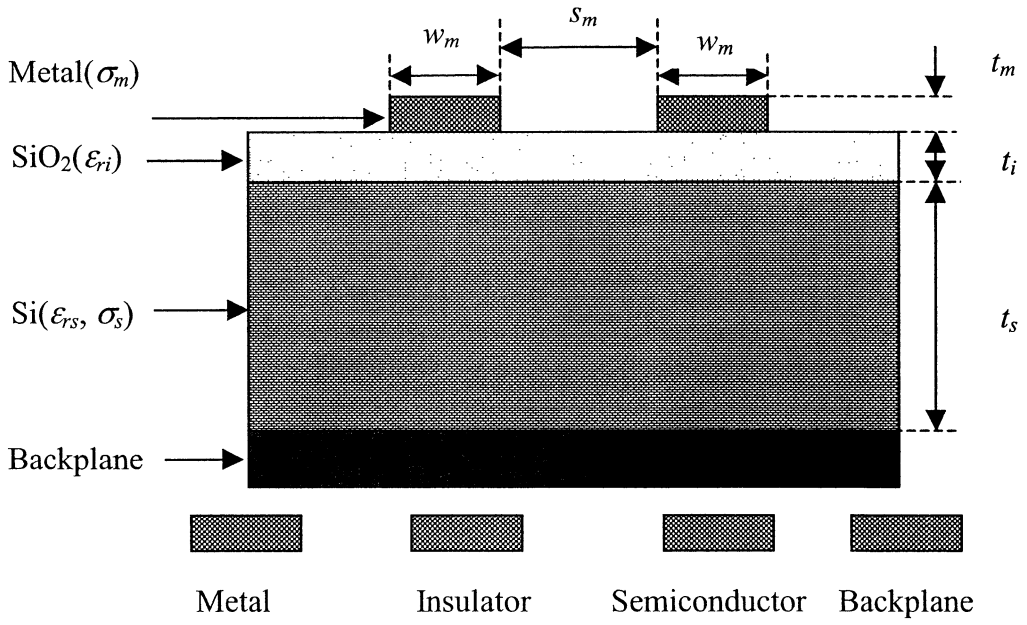


Figure 5.1: Coupled interconnects in the MIS configuration

The main electrical and geometrical parameters to be used in the illustrated examples are listed in Table 5.1. The spacing between the two coupled interconnects will take the values 8, 25 to 100 μm in the foregoing sections. These spacings are representative of practical VLSI implementations with micron technology. Here, the metal is assumed to be copper.

Table 5.1: Main parameters of coupled interconnects in the MIS configuration

Electrical		Geometrical	
Parameter	Value	Parameter	Value (μm)
ε_{ri}	3.82	t_m	1
ε_{rs}	11.9	t_i	2
ρ_s	100 Ω·cm	t_s	300
σ_m	5.7×10^7 (S/m)	w_m	3
		s_m	8/25/100

5.2.2 Hybrid RLCG-B model

Based on the original RLCG-B model for a single interconnect proposed in Section 4.2, and based on the literature [84][85], a hybrid RLCG-B model shown in Figure 5.2 is used for the odd mode of two coupled interconnects. For line A, the series elements are R_{1a} and L_{1a}, and the shunt elements C_{1a}, C_{2a} and R_{2a}. Similarly for line B, there are series elements, R_{1b} and L_{1b}, and shunt elements C_{1b}, C_{2b} and R_{2b}. Besides the elements mentioned above, there are other elements related to the two lines: mutual inductance L_{1ab} between lines A and B, coupled capacitances C_{1ab} and C_{2ab} between lines A and B for the insulator and semiconductor layers, respectively, and R_{2ab} is the shunt resistance contributed from the transverse current flowing in the semiconductor layer between lines A and B. For simplicity, the lines A and B are assumed identical. Thus for the odd mode of two coupled interconnects, there is a virtual ground plane in the middle of two lines. Here, the back metal plane is a real ground plane.

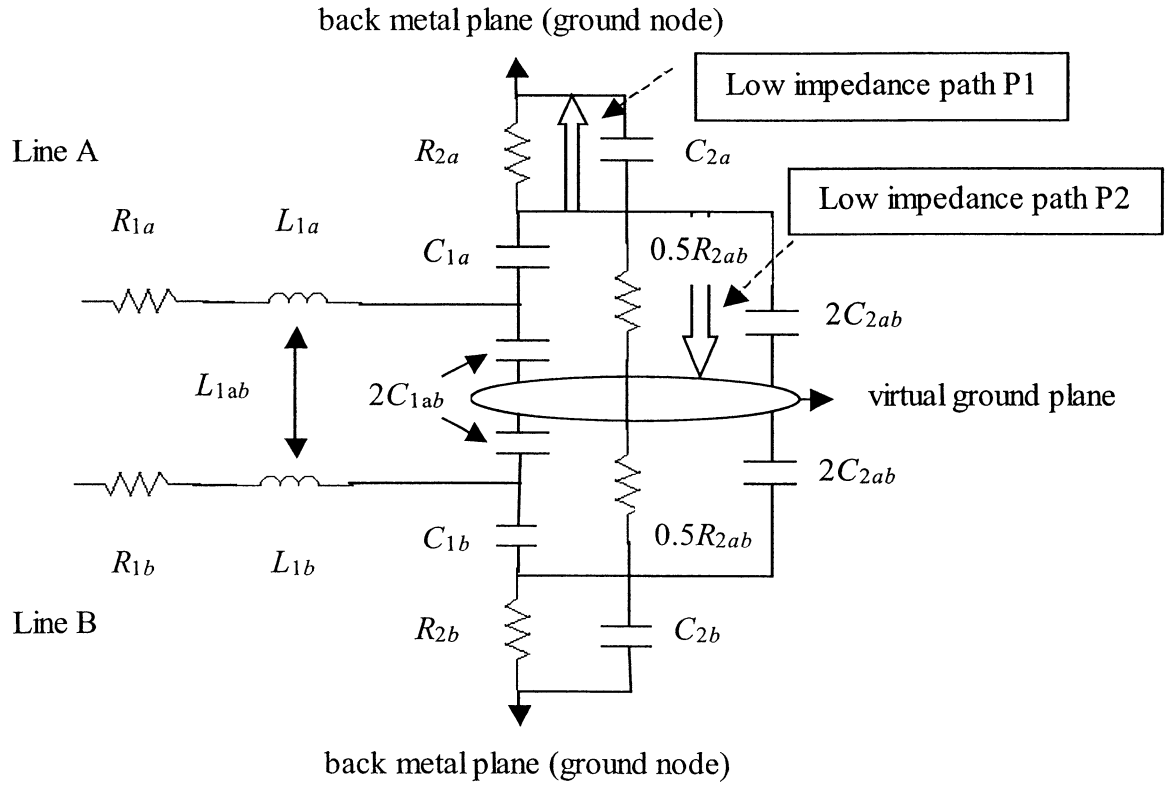


Figure 5.2: A hybrid RLCG-B model for the odd-mode of two coupled interconnects

5.2.3 Simple RLC model

For a typical semiconductor layer of 300 μm with value of resisitivity from 1 to 100 Ω·cm, one low impedance path P1 exists inside the bulk semiconductor, which is from the interface between the insulator and semiconductor layers to the back metal plane as shown in Figure 5.2. This is equivalent to assume that the shunt admittance from the insulator layer (e.g. ωC_{1a}) is much smaller than the shunt admittance from the semiconductor layer (e.g. $1/R_{2a}+\omega C_{2a}$). For the odd mode of two coupled interconnects, on the condition of small wire spacing between the two interconnects, there is another low impedance path P2 inside the bulk semiconductor, which is from the interface

between the two substrate layers to the middle virtual ground plane as shown in Figure 5.2.

As considered for one of the five simplified models in the previous chapter, the hybrid RLCG-B model can be evolved into a simple two-wire model by shortening these two low impedance paths. Thus, six shunt elements C_{2a}, C_{2b}, C_{2ab}, R_{2a}, R_{2b} and R_{2ab} in Figure 5.2 related to the semiconductor layer are removed.

In a quasi-static approach, the magnetic field still penetrates into the semiconductor layer and reaches the back metal plane. So the inductance elements L_{1a}, L_{1b} and L_{1ab} in Figure 5.2 are related to the back metal plane. Due to the identity of the two lines, the value of L_{1b} is the same as that of L_{1a}. As shown in Figure 5.3, the impact of the back metal plane on the mutual inductance L_{1ab} is determined by a respective pair of induced currents κI on the back metal plane and on each side of the virtual ground plane. Here, I is the total current flowing on line A or B, and κ has a magnitude less than 1.

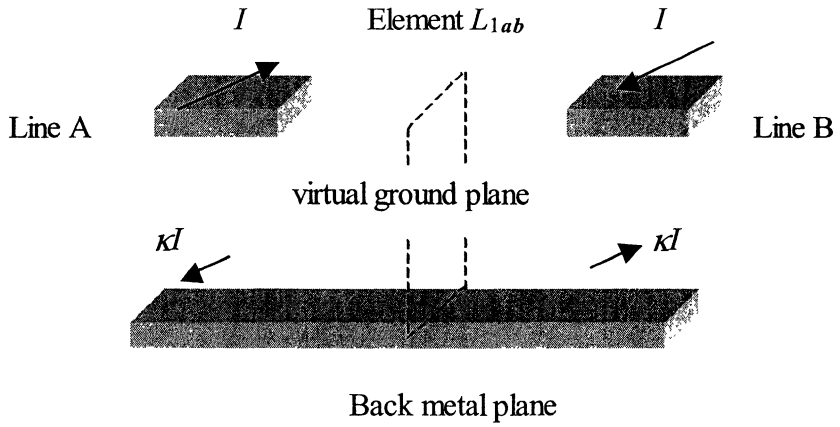


Figure 5.3: Currents flowing on three conductors forming the interconnect

Practically in VLSI circuits, the wire spacing between the two coupled interconnects will be much smaller than the thickness of the semiconductor layer. For the odd-mode of the two coupled lines, the current flowing on the back metal plane will be much smaller than the total current flowing on the two coupled interconnects. That is to say, κ will be much smaller than 1.

Due to the similarity of the two lines, three elements R_{1b}, L_{1b} and C_{1b} of line B for the hybrid RLCG-B model in Figure 5.2 are equal to their corresponding elements R_{1a}, L_{1a} and C_{1a} of line A. An RLC model with five elements R_{1a}, L_{1a}, C_{1a}, L_{1ab} and C_{1ab} is finally obtained as illustrated in Figure 5.4a.

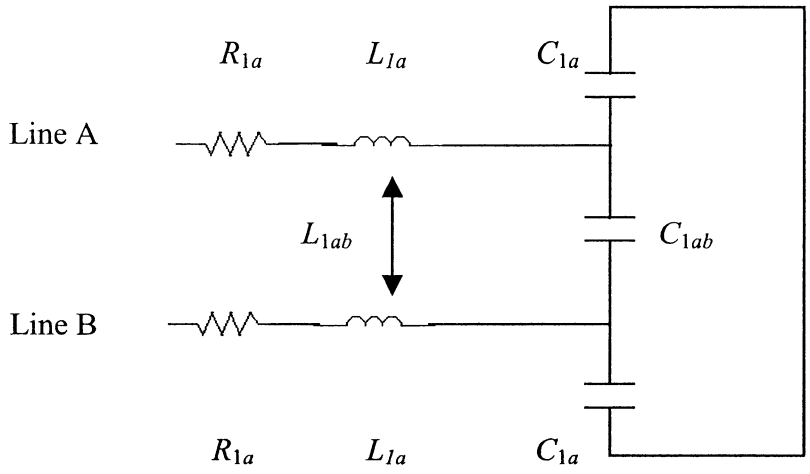


Figure 5.4a: RLC model for the odd mode of two coupled interconnects (five-element RLC model)

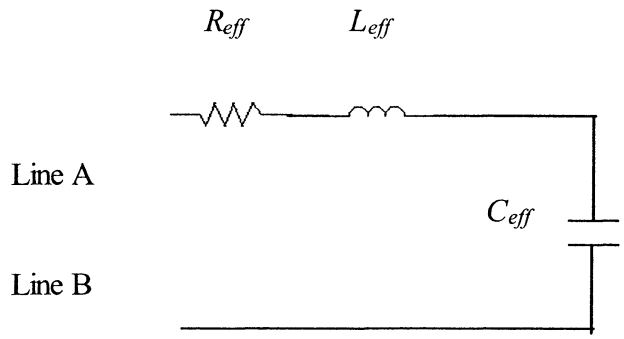


Figure 5.4b: RLC model for the odd mode of two coupled interconnects (three-element RLC model)

An alternative representation of the RLC model with five elements R_{1a}, L_{1a}, C_{1a}, L_{1ab} and C_{1ab} in Figure 5.4a is a simple RLC model with three elements R_{eff}, L_{eff} and C_{eff} as shown in figure 5.4b. Comparing Figures 5.4b with 5.4a, the relationships among the elements of the two models are written as below

$$R_{eff} = 2R_{1a} \tag{5-1}$$

$$L_{eff} = 2(L_{1a} - L_{1ab}) \tag{5-2}$$

and $$C_{eff} = C_{1ab} + \frac{C_{1a}}{2} \tag{5-3}$$

Thus, the complex odd-mode propagation constant is calculated as

$$\gamma_{odd} = \sqrt{(R_{eff} + j\omega L_{eff})j\omega C_{eff}} \tag{5-4}$$

The above complex odd-mode propagation constant will be used to compare with the result obtained from a full-wave field solver, namely, Agilent Technologies ADS Momentum. Thus, the validity conditions of the simple RLC model in Figure 5.4b will be illustrated. Below, we discuss how to obtain the three effective circuit parameters L_{eff}, C_{eff} and R_{eff}.

5.2.3.1 Effective Inductance L_{eff}

For the semiconductor layer with a resisitivity value of 100 Ω·cm, the skin depth of the semiconductor is 5 mm at a high frequency of 10 GHz as shown in Figure 5.5. The skin depth is much larger than the semiconductor thickness of 300 μm. Thus, the electromagnetic fields can still reach the back metal plane and the estimation of the mutual inductance L_{1ab} is related to the thickness of the semiconductor layer. Assuming that the spacing between the two coupled interconnects is much smaller than the thickness of the semiconductor layer, the impact of the back metal plane on the mutual inductance L_{1ab} is neglected by using a two-conductor system.

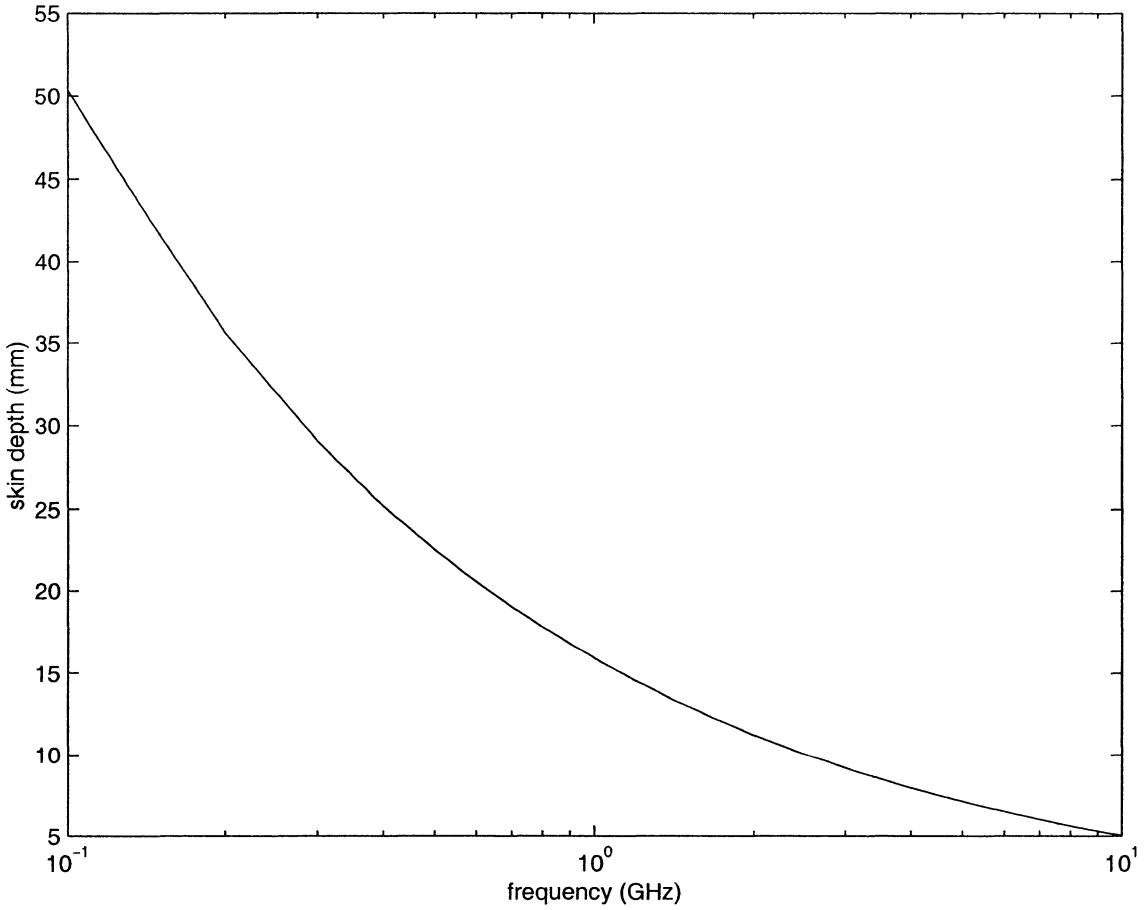


Figure 5.5: Skin depth of the semiconductor with resistivity of 100 Ω·cm

Closed-form expressions for the self and mutual inductance of two wires with rectangular cross section are not available. Approximate expressions can be used, as suggested in [84] by first applying a geometrical transformation as illustrated in Figure 5.6. Two wires of rectangular cross section are transformed into two equivalent cylindrical wires.

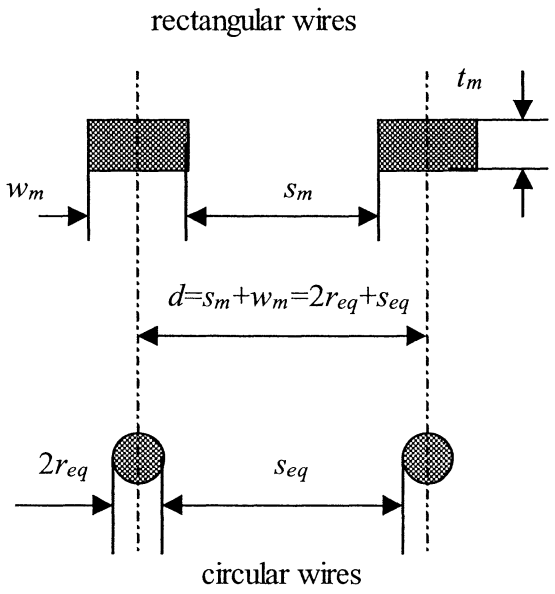


Figure 5.6 Geometrical transform

The center-to-center distance d between two rectangular wires are kept as same as the one between two equivalent cylindrical wires. Thus, we have

$$d = s_m + w_m \tag{5-5}$$

Based on previous work [84], the equivalent radius of round wire r_{eq} is derived from the width and thickness of rectangular wire.

$$r_{eq} = \frac{w_m + t_m}{4} \tag{5-6}$$

The height H from the bottom of the two rectangular wires to the back metal layer is the sum of two substrate layers.

$$H = t_s + t_i \tag{5-7}$$

The equivalent height H_{eq} from the bottom of the two round wires to the back metal plane is obtained from the height from the bottom of the two rectangular wires to the back metal plane, the width and thickness of the rectangular wire [84]:

$$H_{eq} = H + \frac{t_m - w_m}{4} \tag{5-8}$$

Then, the mutual inductance for a pair of two equivalent round wires is estimated [84]

$$L_{1ab} = \frac{\mu}{4\pi} \ln\left(\frac{\left(s_{eq} + 2r_{eq}\right)^2 + \left(r_{eq} + 2H_{eq}\right)^2}{\left(s_{eq} + 2r_{eq}\right)^2 + r_{eq}^2} \right) \tag{5-9}$$

And the self inductance is approximately given by

$$L_{1a} = \frac{L_m}{w_m} + \frac{\mu}{2\pi} \ln\left(\frac{2H_{eq}}{r_{eq}} + 1 \right) \tag{5-10}$$

The first term at the right side of Eq.5-10 is calculated by Eq.4-4a, which corresponds to the metal layer as performed in the previous chapter. The second term at the right side of Eq.5-10 is contributed from the insulator and semiconductor layers as expressed in [84]. Combining Eqs.5-9 and 5-10 with Eq.5-2, the effective inductance is finally obtained for the two coupled interconnects.

5.2.3.2 Effective capacitance C_{eff}

According to Eq.5-3, the effective capacitance for the odd-mode of two coupled interconnects is equal to the coupled capacitance C_{1ab} added by half of the self capacitance C_{1a}. As shown in Figure 5.7, five capacitances C_f, C_p, C_{g0}, C_{gab} and C_g are related to the two capacitances. Here, C_f is the fringe capacitance of a single microstrip

line, and C_p is simply the parallel plate capacitance between the strip and the reference plane (assumed to be an ideal ground plane). C_{g0}, C_{gab} and C_g are the coupled capacitances between two identical lines. C_{g0} describes the capacitance in the upper air region, and C_g describes the capacitances in the lower insulator region, while C_{gab} is simply the parallel plate capacitance between two lines.

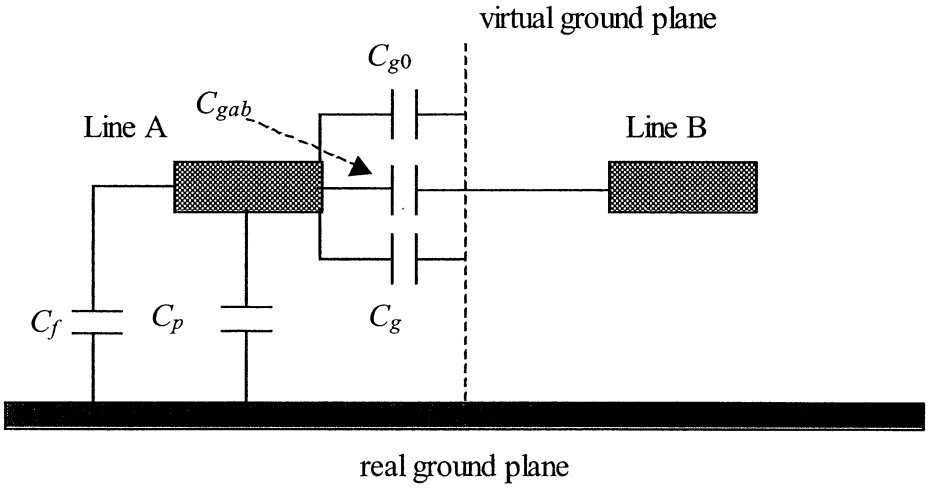


Figure 5.7 Odd-mode capacitances

Thus, the two capacitances of the simple RLC model can be expressed as

$$C_{1a} = C_f + C_p \tag{5-11}$$

and

$$C_{1ab} = \frac{C_{g0} + C_{gab} + C_g}{2} \tag{5-12}$$

Combining Eqs.5-11, 5-12 with Eq.5-3, we have

$$C_{eff} = \frac{C_f + C_p + C_{g0} + C_{gab} + C_g}{2} \tag{5-13}$$

Here, the two parallel plate capacitances C_p and C_{gab} can be simply written as

$$C_p = \varepsilon_0 \varepsilon_{ri} \frac{w_m}{t_i} \tag{5-14}$$

and $$C_{gab} = \varepsilon_0 \frac{t_m}{s_m / 2} \tag{5-15}$$

The fringe capacitance C_f can be derived from C_p and the single microstrip capacitance C_m, which has been described in the previous chapter.

$$C_f = \frac{C_m - C_p}{2} \tag{5-16}$$

The coupled capacitance C_{g0} in the upper air region is given by the simplified equations [86].

$$\begin{aligned} C_{g0} &= \frac{\varepsilon_0}{\pi} \ln\left(2\frac{1+\sqrt{k'}}{1-\sqrt{k'}}\right) && for \quad 0 \le k^2 \le 0.5 \\ &= \frac{\pi\varepsilon_0}{\ln\left(\frac{1+\sqrt{k}}{1-\sqrt{k}}\right)} && for \ 0.5 \le k^2 \le 1 \end{aligned} \tag{5-17a}$$

where $$k = \frac{s}{s + 2w_m} \tag{5-17b}$$

and $$k' = \sqrt{1-k^2} \tag{5-17c}$$

And coupled capacitance C_g in the lower insulator region is given by the simplified equations [87].

$$C_g = 0.65C_f + \frac{\varepsilon_0\varepsilon_{ri}}{\pi} \ln\coth\left(\frac{\pi s}{4t_i}\right) + \left\{0.02\varepsilon_0\sqrt{\varepsilon_{ri}}\frac{t_i}{s} + \varepsilon_0\left[1-\left(\frac{1}{\varepsilon_{ri}}\right)\right]^2\right\} \tag{5-18}$$

The above set of capacitances is used for the cases analyzed in Sections 5.3 and 5.4, where the influence of the line thickness on the capacitance is already included. Using the above equations, the effective capacitance is calculated for two coupled interconnects and the results are listed in Table 5.2. Table 5.2 shows that the effective capacitance decreases with the increase of the spacing between the two coupled interconnects. The effective capacitance varies only by 5.6% as the spacing between the two coupled interconnects changes from 8, 25 to 100 μm. Table 5.2 also shows that the fringe capacitance C_{g0} in the air region decreases a lot from 0.104 to 0.066 (36.5%), while the

fringe capacitance C_g in the insulator layer slightly reduces from 0.202 to 0.200 (1%) as the spacing between the two coupled interconnects varies from 8 to 100 μm. This is due to the fact that there is a virtual ground plane connected to the insulator layer, while it is an open boundary in the air region. Here, the semiconductor layer was assumed as a virtual ground plane in [84].

Table 5.2: Capacitance C_{eff}

Case	s_m(μm)	C_m	C_p	C_f	C_{g0}	C_{gab}	C_g	C_{eff}
A_1	8	0.975	0.507	0.234	0.104	0.022	0.202	0.535
A_2	25	0.975	0.507	0.234	0.095	0.007	0.201	0.522
A_3	100	0.975	0.507	0.234	0.066	0.002	0.200	0.505

5.2.3.3 Effective resistance R_{eff}

Based on our EM simulations for the parameters listed in Table 5.1, the effective resistance of coupled interconnects R_{eff} is roughly the sum of the two series resistances of coupled interconnects. For this special case, R_{eff} can be estimated by

$$R_{eff}(f) = 2R_1^s \tag{5-19}$$

Here, R_1^s is the series resistance of a single interconnect already mentioned in Chapter 4. Numerical simulations have validated the microstrip model for the highest frequency up to 10 GHz with a semiconductor resistivity larger than 1 Ω·cm. Exact calculation of R_{eff} depends on both the geometrical parameters and on the electrical parameters. Deploying this exact calculation is beyond the scope of this thesis. Therefore, we will use Eq.5-19 to evaluate the effective resistance R_{eff} of the simple RLC model.

Once all the effective parameters R_{eff}, L_{eff} and C_{eff} in Figure 5.4b are obtained, by using Eq.5-4, the odd-mode complex propagation constant for coupled interconnects can be calculated and compared with the values predicted by numerical field solvers, or obtained from other analytical expressions.

5.3 Validation of the simple RLC model

In order to validate the simple RLC model in Figure 5.4b, we show a comparison of the odd- mode (differential mode) complex propagation constant ($\gamma_z = \alpha_z + j\beta_z$) obtained from the simple RLC model and the one predicted by Agilent Technologies ADS momentum field solver. For convenience, the simple RLC model is called a simple two-wire model below. The main parameters in the MIS configuration for the two coupled interconnects are listed in Table 5.1. The wire spacing between the two coupled interconnects are 8, 25 and 100 μm, respectively. For the purpose of illustrating the difference of propagation characteristics between single and coupled interconnect topologies, we also compare the complex propagation constant based on a single-wire model described in Chapter 4 with the one predicted by ADS Momentum. Here, the one-wire model refers to the modified RLCG-B model in Chapter 4. Figures 5.8a and 5.8b, 5.9a and 5.9b, 5.10a and 5.10b show the cases with the line spacings of 8, 25 and 100 μm, respectively.

As shown in Figure 5.8a, there is a good agreement between the complex propagation constant based on the simple two-wire model (Eq.5-4) and the one predicted by ADS Momentum for the frequency up to 10 GHz with a wire spacing of 8 μm. However, there is a larger difference on the complex propagation constant between the one-wire model (Eq.4-22a) and ADS. For this case, the ratio of the wire spacing to the line width is 2.7. Thus, a strong coupling exists between the two interconnects. Figure 5.8a demonstrates that the simple two-wire model in Figure 5.4b captures the electrical behavior of the two coupled interconnects well if the wire spacing is comparable to the line width. As expected, the one-wire model, which excludes the whole coupling, is not suitable to model the two interconnects with strong coupling.

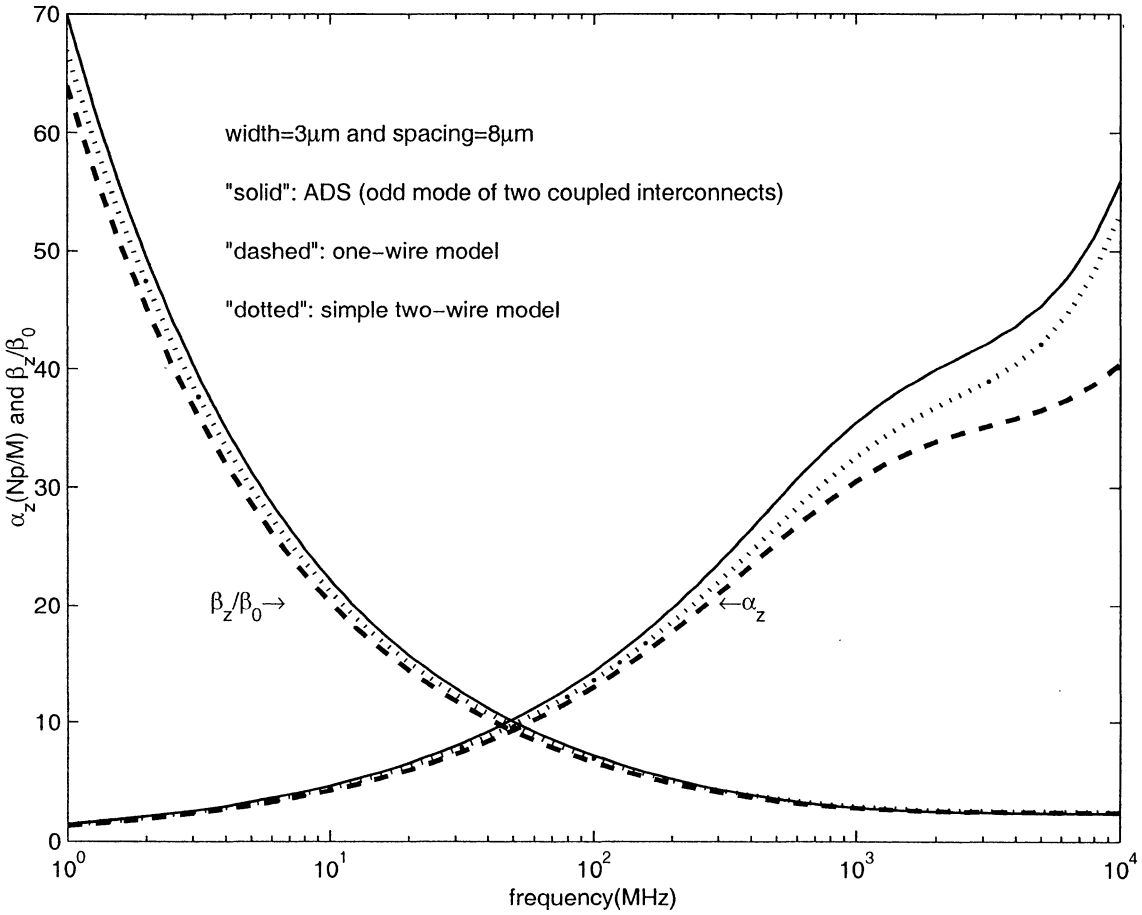


Figure 5.8a: Comparisons of complex propagation constant among one-wire model, simple two-wire model and ADS for two coupled interconnects with a wire spacing of 8 μm

Figure 5.8b shows the relative differences on the complex propagation constant between the one-wire model and ADS, and between the simple two-wire model and ADS, with a wire spacing of 8 μm. The maximum relative differences on attenuation constant α_z and propagation constant β_z between the one-wire model and ADS are around 27% at 10GHz and 9% at 1 MHz, respectively, while the maximum relative differences on α_z and β_z are about 8% at 1 GHz and 6% at 10 GHz, respectively. Figures 5.8a and 5.8b demonstrate that the simple two-wire model accurately captures the electrical behavior of the two interconnects with strong coupling. In such situation, the

coupling terms are more important than the terms neglected in the ideal ground assumption for the simple two-wire model, so the simple two-wire model is better. That is to say, the semiconductor losses can be neglected by placing an interconnect as a current return path for a signal wire with the wire spacing comparable to the line width.

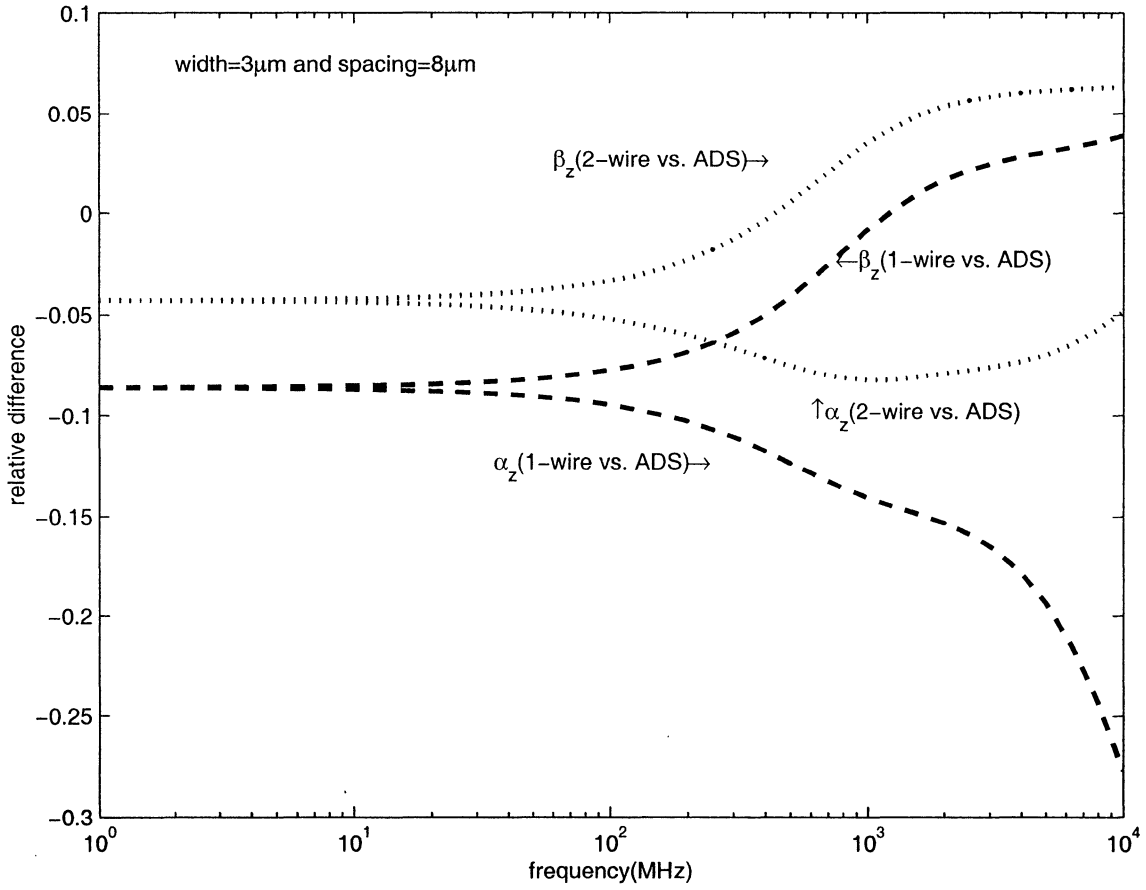


Figure 5.8b: Relative differences of complex propagation constant among one-wire model, simple two-wire model and ADS for two coupled interconnects with a wire spacing of 8 μm

Figure 5.9a shows a case with a wire spacing of 25 μm. For this case, the ratio of the wire spacing to the line width is 8.3. As shown in Figure 5.9a, there is a still smaller difference between the complex propagation constant based on the simple two-wire model and the one predicted by ADS Momentum, and there is also a smaller difference

on the complex propagation constant between the one-wire model and ADS. It seems that the ratio of the wire spacing to the line width is in a transition region, where both of the two models match well with ADS.

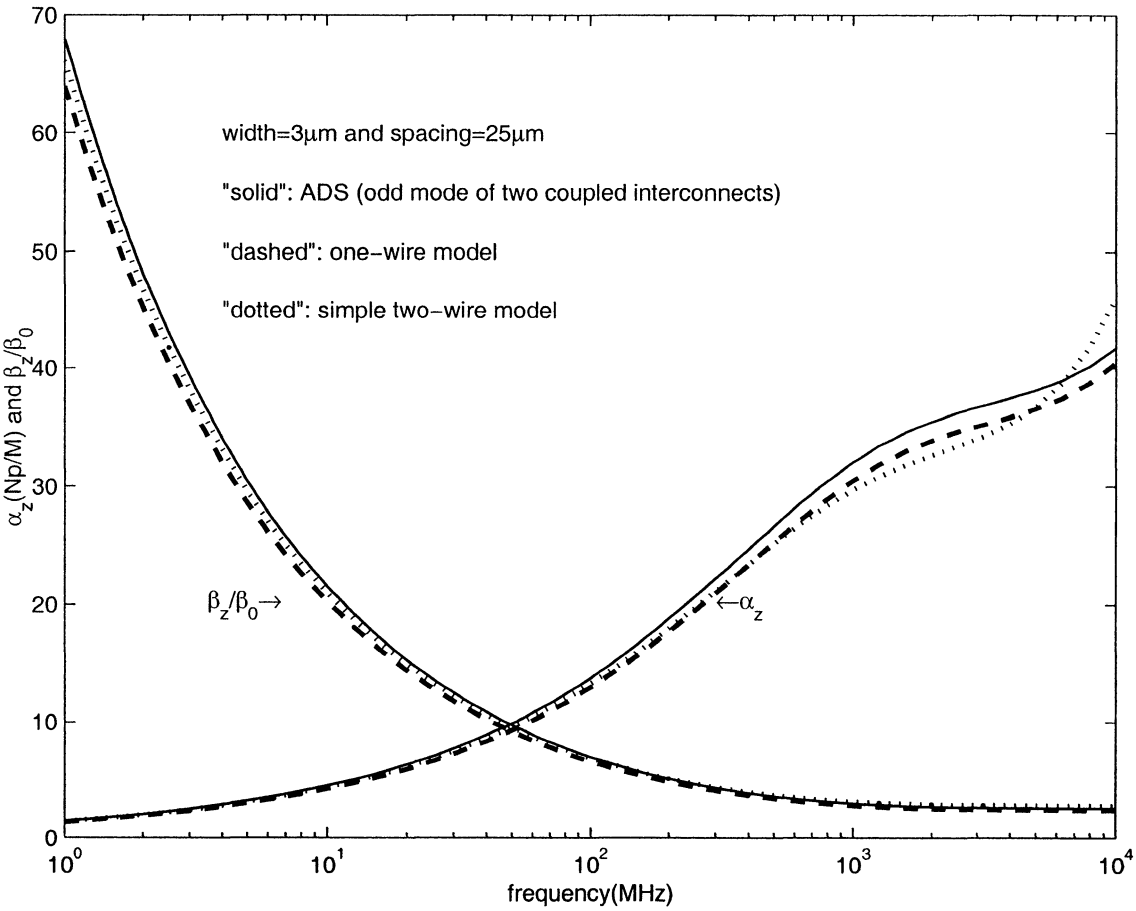


Figure 5.9a: Comparisons of complex propagation constant among one-wire model, simple two-wire model and ADS for two coupled interconnects with a wire spacing of 25 μm

Figure 5.9b shows that the relative differences on complex propagation constant between the one-wire model and ADS, and between the simple two-wire model and ADS, with a wire spacing of 25 μm. The maximum relative differences on α_z and β_z between the one-wire model and ADS are about 6% at 40 MHz and 7% at 10 GHz, respectively, while the maximum relative differences on α_z and β_z between the simple

two-wire model and ADS are around 10% at 10 GHz and 8% at 5 GHz, respectively. Figures 5.9a and 5.9b illustrate that both of the one-wire model and the simple two-wire model approximate the electrical behavior of the two coupled interconnects well as the wire spacing is 8.3 times the line width.

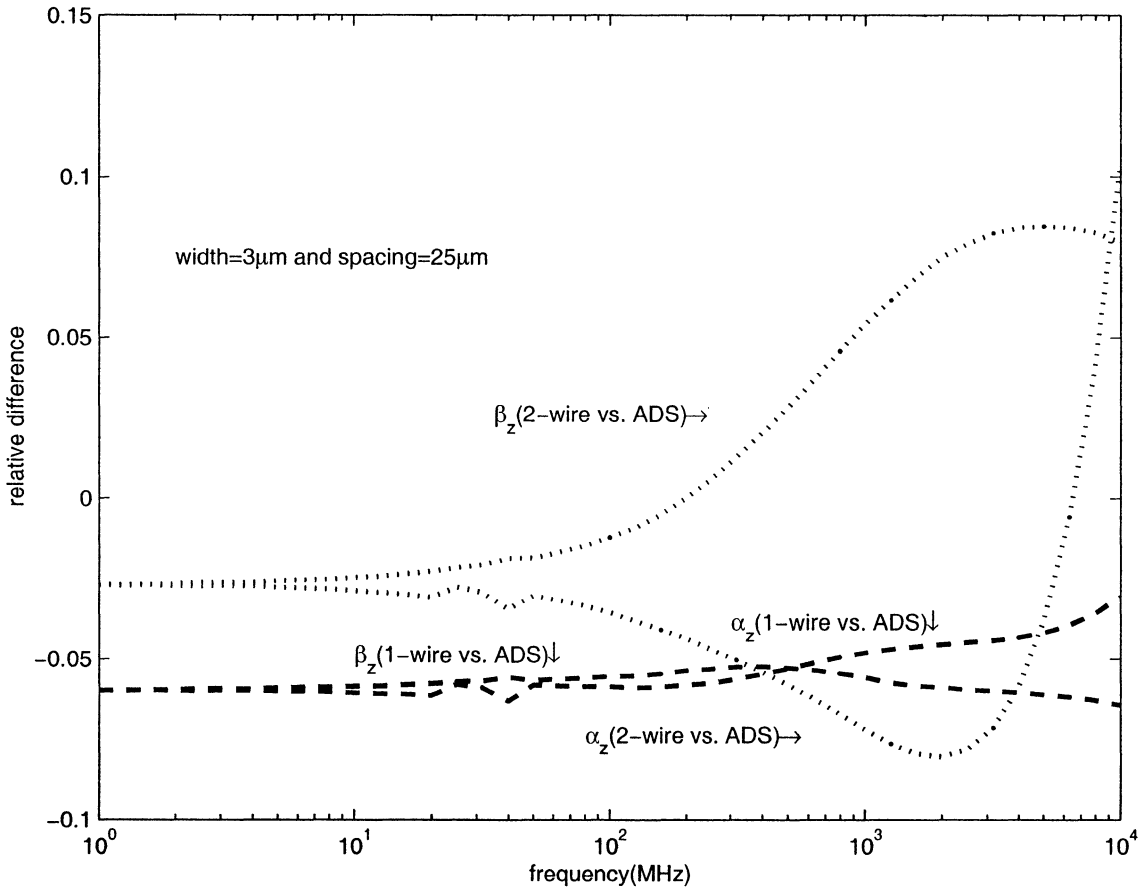


Figure 5.9b: Relative differences of complex propagation constant among one-wire model, simple two-wire model and ADS for two coupled interconnects with a wire spacing of 25 μm

As shown in Figure 5.10a, there is a larger difference between the complex propagation constant based on the simple two-wire model and the one predicted by ADS Momentum for the wire spacing of 100 μm, while there is a smaller difference on the complex propagation constant between the one-wire model and ADS. In this case, the wire

spacing is 33 times the line width, where weak coupling is expected between the two interconnects. Figure 5.10a shows that the one-wire model captures the electrical behavior of the two coupled interconnects well as the wire spacing is much larger than the line width. Thus, the two interconnects with weak coupling can be treated as two single interconnects without coupling. In this case, the simple two-wire model fails. This is due to the simplification process that the bulk semiconductor is treated as a perfect conductor when constructing the simple two-wire model.

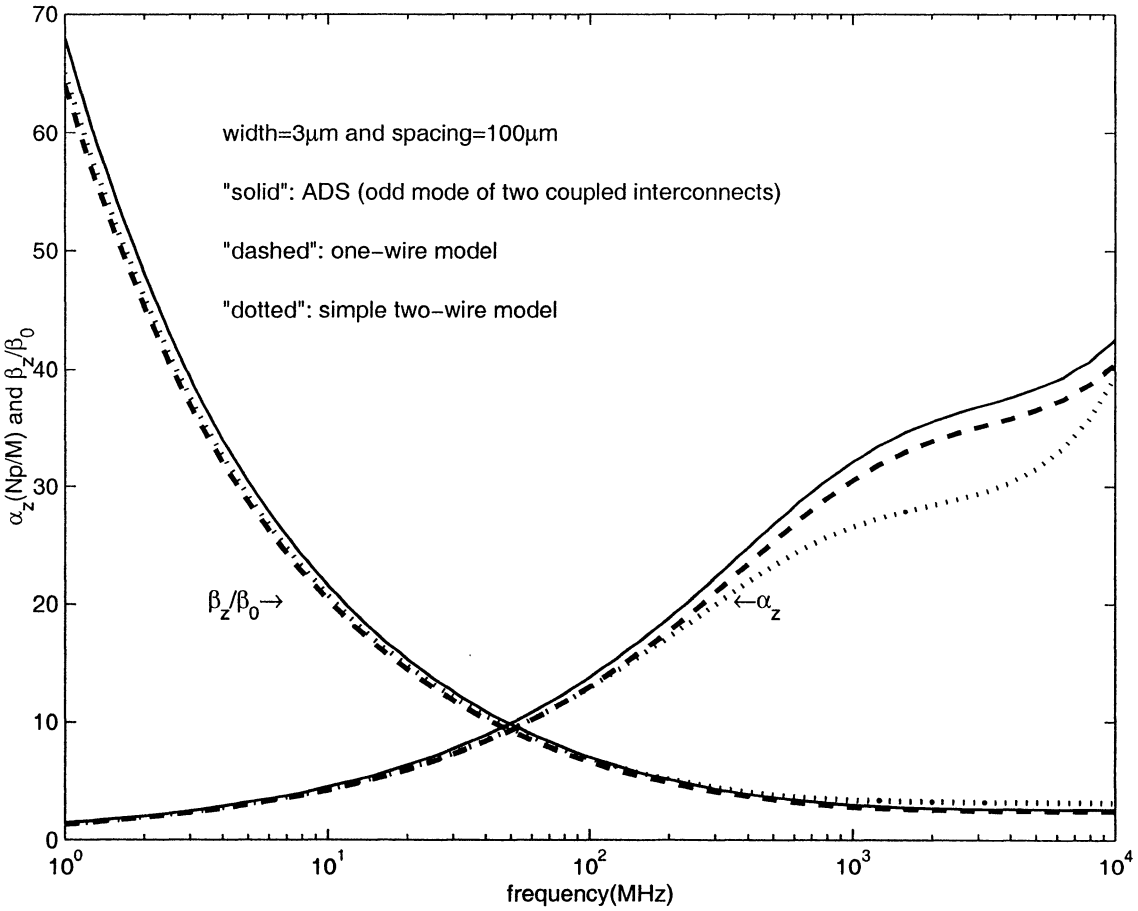


Figure 5.10a: Comparisons of complex propagation constant among one-wire model, simple two-wire model and ADS for two coupled interconnects with a wire spacing of 100 μm

Figure 5.10b shows that the relative differences on complex propagation constant between the one-wire model and ADS, and between the simple two-wire model and ADS, with a wire spacing of 100 μm. The maximum relative differences on α_z and β_z between the one-wire model and ADS are 6% at 200 MHz and 7% at 10 GHz, respectively, while the maximum relative differences on α_z and β_z are around 20% at 2.5 GHz and 22% at 7 GHz, respectively. As expected, the one-wire model is better than the simple two-wire model for the two interconnects with weak coupling. Noted that the dielectric losses are included in the one-wire model but excluded in the simple two-wire model. Figure 5.10a and 5.10b illustrate that the terms related to the dielectric losses are more important than the coupling terms neglected in the one-wire model. Thus, the one-wire model is better for the two interconnects of weak coupling.

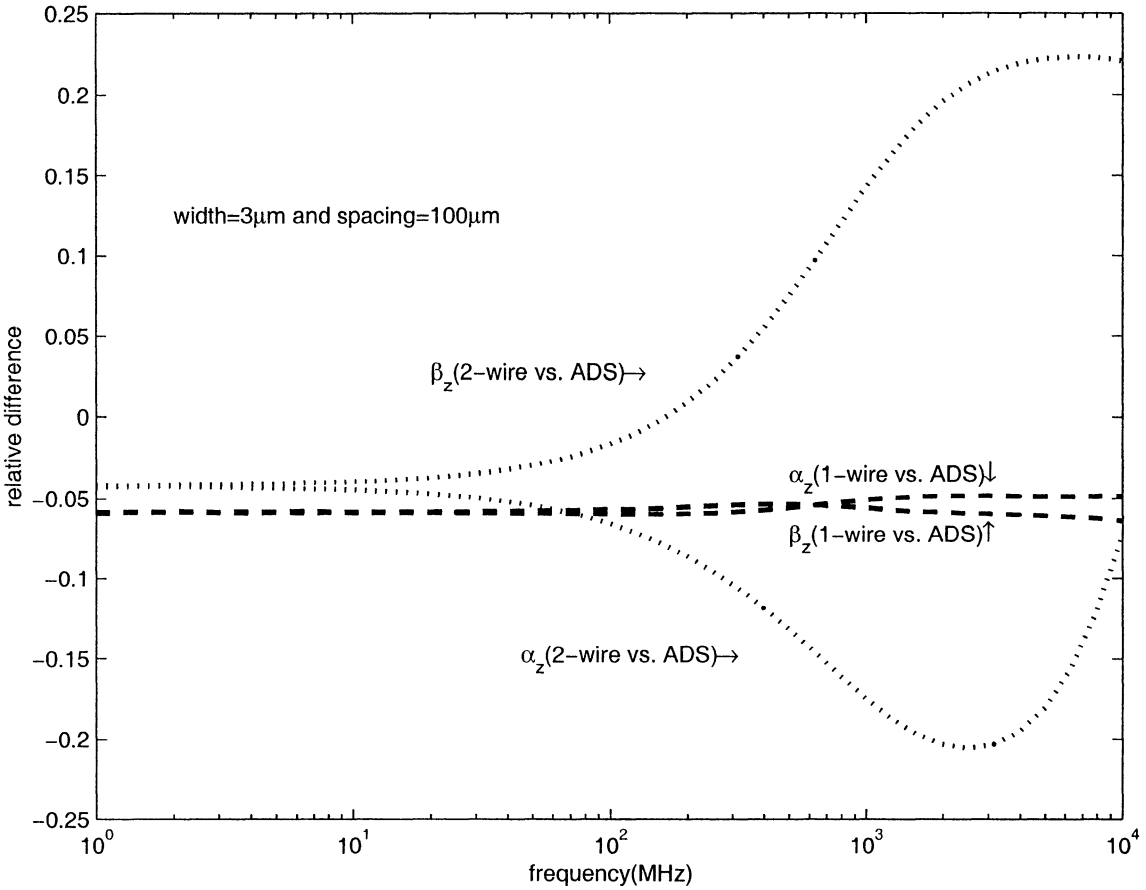


Figure 5.10b: Relative differences of complex propagation constant among one-wire model, simple two-wire model and ADS for two coupled interconnects with a wire spacing of 100 μm

5.4 Summary

In this chapter, we investigated another interconnect topology: two coupled interconnects in the MIS configuration, where one of the two coupled interconnects is used as current returning path. Based on the original RLCG-B model for a single interconnect proposed in Section 4.2 and other models in literature, a hybrid RLCG-B model is first used for the odd-mode of two coupled interconnects. This hybrid RLCG-B model is then evolved into a simple RLC model by assuming the bulk semiconductor as a perfect conductor. By comparing the complex propagation constant obtained based on

the simple RLC model with the one predicted by Agilent Technologies ADS Momentum, the valid condition of the simple RLC model is outlined. For the special cases discusses in this chapter, it is demonstrated that the simple RLC model (simple two-wire model) captures the electrical behavior of two coupled interconnects well as the wire spacing s_m is comparable to the line width w_m. It seems that there exists a threshold value of s_m/w_m. Under the threshold, a tight coupling exists between the two interconnects and the simple two-wire model works well, because the terms in modeling related to the semiconductor losses are dominated by the coupling terms for two tightly coupled interconnects. Above the threshold, a loose coupling is expected for the two interconnects and the simple two-wire model fails. This is due to the simplification process that the bulk semiconductor is treated as a perfect conductor and the semiconductor losses are neglected in the simple two-wire model. It was found that for 300 μm thick Si wafer with a line width of 3 μm, the typical threshold value of s_m/w_m is 8, which corresponds to the wire spacing between two interconnects less than 25 μm.

In this chapter, by comparing the propagation characteristics between single and coupled MIS interconnect topologies in VLSI circuits, we illustrate that a one-wire model, originally for a single MIS interconnect, captures the electrical behavior of two coupled MIS interconnects well when there is weak coupling between the two interconnects. As expected, the one-wire model excluding the whole coupling fails for the two interconnects with strong coupling. Similar to the simple two-wire model, a threshold value of s_m/w_m is used to determine if the one-wire can be properly used to model the two coupled interconnects. Based on numerical results, the valid range of the one-wire model seems to be overlapped by that of the simple two-wire model and a validity interval of s_m/w_m can be shared by models. Thus, it is possible to construct an efficient model for two coupled interconnects. This efficient model can be either a one-wire model or a simple two-wire model. A threshold value of s_m/w_m is proposed to

determine if the one-wire model or the simple two-wire is sufficient to model the two coupled interconnects.

In the future, more cases need to be analyzed. Thus, the valid ranges of one-wire model and simple two-wire model can be outlined in a s_m-w_m plane, where the threshold of s_m/w_m may be changed with variation of line width for different technologies.

CHAPTER 6

PROPAGATION TIME DELAY ANALYSIS OF A DISTRIBUTED RC WIRE WITH R_S AND C_L

6.1 Introduction

Previous chapters have presented modeling of interconnects in VLSI circuits and analyzed the modeling accuracy on the time-domain simulation error. The rest of the thesis focuses on signal integrity analysis. In this chapter, we use a single distributed RC wire as an example to investigate the propagation time delay in VLSI circuits. In the next chapter, we will study the propagation time skew of coupled interconnects in the MIS configuration.

The RC model for a single line in VLSI circuits has been extensively studied, since it is the simplest model that allows characterizing delays of lossy wires with a reasonable accuracy.

Antinone & Brown [55] studied long polysilicon lines as RC transmission lines. More than 10T- structures were utilized to calculate the characteristics of transmission lines in the frequency domain. The step response at the output of an open terminal, with different numbers of T-sections, was also calculated and compared with theoretical results. This paper clearly shows that as the number of T-sections increases, the model accuracy improves. It also demonstrates that lumped RC ladder networks containing a finite number of stages can be successfully used to model long polysilicon lines in integrated circuits.

Rao[56] analyzed time delay of a finite length distributed RC line with a capacitive load C_L. He calculated the step response of the system in the Laplace domain, and

obtained some of the common threshold-crossing times on the load C_L. Models containing 1π- and 2π- sections were used to estimate propagation times, which were compared with those produced by distributed model.

In VLSI circuits, signals propagate between gates and buffer stages. Each net is characterized by several parameters such as the wire length and the fanout. Long wires and large fanout require strong buffers with low output resistance R_S. In addition to load capacitance C_L and output resistance R_S, interconnect delays are also dependent on the logic voltage threshold V_t of the gates. In this chapter, we have considered source resistance R_S, wire resistance R_w, load capacitance C_L, and wire capacitance C_w. Our results are normalized in order to obtain general design rules valid for different technologies [1]. We focus on the determination of the minimum number of T- or π-sections required to predict delay within a given error tolerance. Therefore, independently of the technology used, proper structures can be selected to model wires with sufficient accuracy.

This chapter is organized as follows. Section 6.2 introduces the AWE [22] method to evaluate time delay in an RC wire. For this application, AWE is faster than SPICE, which the majority of engineers normally use. Solutions were obtained for millions of sets of parameters: R_S, C_L, R_w, C_w, and V_t. In our analysis, the value of every resistance element is normalized to that of source resistance R_S ($r=R_w/R_S$), and the value of every capacitance element to that of the load capacitance C_L ($c=C_w/C_L$) assumed to be at the end of the wire. V_t, the logic voltage threshold, has also been normalized with respect to the value of power supply voltage V_{dd} ($v_t=V_t/V_{dd}$). The value of v_t was varied in the interval from 0 to 1. Actual time delay can be obtained by multiplying the normalized result by a factor of R_S*C_L. Section 6.3 presents the T- and π- structures, which are used to model an RC wire. Section 6.4 presents groups of AWE simulation results, which are performed in the normalized r-c plane. These results are generated with sets of r and c values, covering the range from 0.01 to 100, and are calculated for T- and π- structures

with segmentations in 1-, 2-, 4- and 8-sections, for three voltage thresholds 0.2, 0.4 and 0.8. These results quantify the differences between models with few lumped sections and those based on distributed RC transmission lines. For a given error tolerance and a specified technology, we show how a proper structure with a sufficient number of sections can be selected from the contours of error distributions. These results can be translated into design rules to make sure that an RC wire can be modeled with a good approximation without using an excessive number of circuit elements. This is very important in order to allow analysis of circuits having a large number of nodes and gates. Section 6.5 concludes by analyzing our main results.

6.2 AWE method

Asymptotic waveform evaluation (AWE) is a well-known procedure to predict the time response of linear circuits, and it has been successfully and widely used for the analysis of interconnections [88]. Basically, the time response is expanded into a sum of exponentials, where coefficients and time constants are obtained from a moment matching procedure (Appendix B).

We have implemented an AWE routine for the interconnect problem at hand, calculated time delay, and compared them extensively with SPICE predictions for the purpose of validation. The motivation behind the use of AWE is mostly based on its CPU time performance. Here, we used two-pole AWE for 1-section model, and either two- or three- pole AWE for 2-, 4-, and 8- sections models. Choosing a smaller number of poles avoids numerical instability when the wire resistance or capacitance is too small, but it may lead to less accurate results.

6.3 Iterative lumped circuits (ILC) model

The structure of our equivalent circuit model for an RC wire is shown in Figure 6.1. As mentioned in [25], ILC models (T- or π-sections) have been selected to model RC wires. When the losses in wires are high, lumped circuit models are sufficient to model them. In Figure 6.1, the wire resistance R_w can be obtained by multiplying the resistance per unit length of wire R_w^l (Ω/m) by the wire length d (m). Similarly, the wire capacitance C_w can be obtained by multiplying the capacitance per unit length C_w^l (F/m) by the wire length d (m). Figures 6.1a and 6.1b show 1T- and 1π- network sections. Figures 6.1c and 6.1d show nT- and nπ- ladder networks. Using appropriate equivalent circuit models, the step-response of RC wires with source resistance R_S and load capacitance C_L can be analyzed.

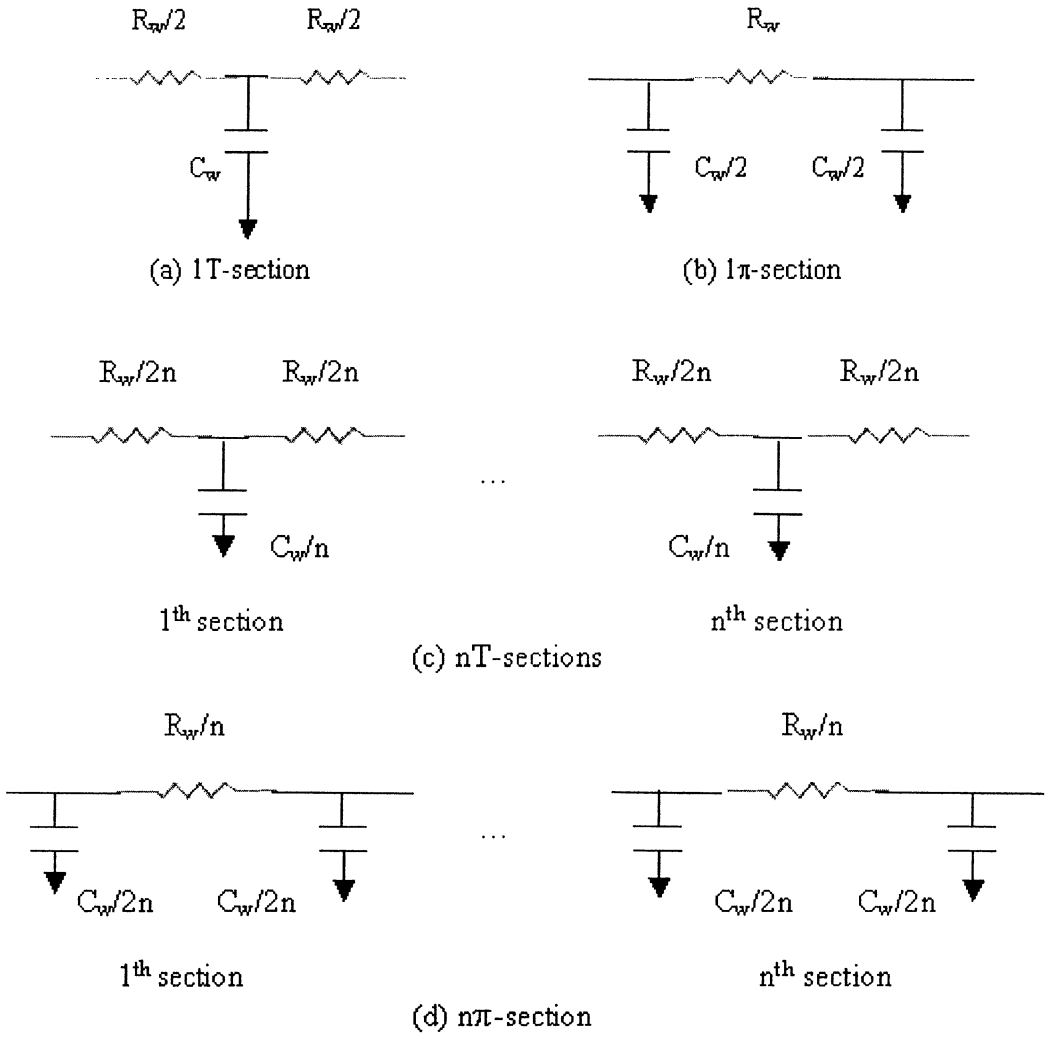


Figure 6.1: Equivalent circuits for a distributed RC wire

6.4 Estimation of voltage waveforms

RC wires are simple cases in which the voltage waveform of step response on load capacitance is monotonic [25][55,56][71]. Therefore, a limited number of poles are needed to approximate those step responses with linear transfer functions. In order to validate results produced with the models developed here, our simulation results were compared with those produced with SPICE, with the same equivalent circuit models and

under the same source and load conditions. The AWE routine we developed was validated and was observed to have a good accuracy.

6.5 Analysis of propagation time delay

For an RC wire, propagation time delay is obtained by solving for the voltage waveform on a load capacitance with a step stimulus applied at the source end. A symmetrical relationship between the behaviors of T- and π- structures has also been observed, and will be described later.

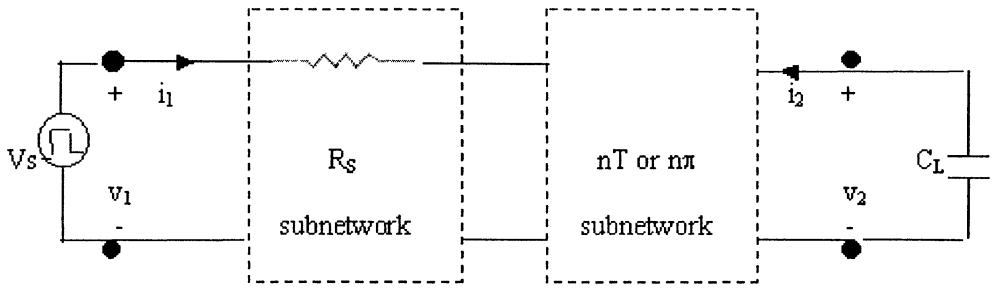


Figure 6.2 A two-port network with source resistance R_S and load capacitance C_L

Figure 6.2 represents a two-port network, which has an ideal voltage source V_S, a source resistance R_S sub-network, a nT- or $n\pi$- sub-network representing the interconnect, and a capacitive load C_L.

The hybrid matrix $[H]_{Rs}$ for the source resistance R_S sub-network can be written as:

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} v_2 \\ -i_2 \end{bmatrix} = \begin{bmatrix} 1 & Rs \\ 0 & 1 \end{bmatrix} \begin{bmatrix} v_2 \\ -i_2 \end{bmatrix} = [H]_{Rs} \begin{bmatrix} v_2 \\ -i_2 \end{bmatrix} \tag{6-1}$$

The hybrid matrix $[H]_t$ for a 1T- sub-network can be written as:

$$[H]_t = \begin{bmatrix} 1+\frac{sRC}{2} & R\left(1+\frac{sRC}{4}\right) \\ sC & 1+\frac{sRC}{2} \end{bmatrix} = \begin{bmatrix} a_1 & b_1 R\left(1+\frac{sRC}{4}\right) \\ b_1 sC & a_1 \end{bmatrix} \tag{6-2a}$$

where $a_1 = 1+\frac{sRC}{2} = a_1(sRC)$ (6-2b)

$b_1 = 1 = b_1(sRC)$ (6-2c)

and $R = R_w / n$ (6-3a)

$C = C_w / n$ (6-3b)

Assuming that the hybrid matrix $[H]_{kt}$ for a k T- sub-network can be written as:

$$[H]_{kt} == \begin{bmatrix} a_k & b_k R\left(1+\frac{sRC}{4}\right) \\ b_k sC & a_k \end{bmatrix} \tag{6-4a}$$

where $a_k = a_k(sRC)$ (6-4b)

$b_k = b_k(sRC)$ (6-4c)

Combing Eq.6-4a with Eq.6-2a, we obtain the hybrid matrix $[H]_{(k+1)t}$

$$\begin{aligned}
&[H]_{(k+1)t} \\
&= [H]_{kt}[H]_t \\
&= \begin{bmatrix} a_k & b_k R\left(1+\frac{sRC}{4}\right) \\ b_k sC & a_k \end{bmatrix}\begin{bmatrix} a_1 & b_1 R\left(1+\frac{sRC}{4}\right) \\ b_1 sC & a_1 \end{bmatrix} \\
&= \begin{bmatrix} a_k a_1 + b_k b_1 sRC\left(1+\frac{sRC}{4}\right) & (a_k b_1 + b_k a_1)R\left(1+\frac{sRC}{4}\right) \\ (b_k a_1 + a_k b_1)sC & a_k a_1 + b_k b_1 sRC\left(1+\frac{sRC}{4}\right) \end{bmatrix} \\
&= \begin{bmatrix} a(k+1) & b(k+1)R\left(1+\frac{sRC}{4}\right) \\ b(k+1)sC & a(k+1) \end{bmatrix}
\end{aligned} \tag{6-5a}$$

where $a_{(k+1)} = a_k a_1 + b_k b_1 sRC\left(1+\frac{sRC}{4}\right) = a_{(k+1)}(sRC)$ (6-5b)

$b_{(k+1)} = b_k a_1 + a_k b_1 = b_{(k+1)}(sRC)$ (6-5c)

Similarly, we can prove that the hybrid matrix $[H]_{(k+1)\pi}$ for a $(k+1)\pi$- sub-network can be written as:

$$[H]_{(k+1)\pi} = \begin{bmatrix} a_{(k+1)} & b_{(k+1)}R \\ b_{(k+1)}sC\left(1+\frac{sRC}{4}\right) & a_{(k+1)} \end{bmatrix} \tag{6-6}$$

where $a_{(k+1)}$ and $b_{(k+1)}$ are defined in Eqs.6-5b and 6-5c, and R and C are defined in Eqs.6-3a and 6-3b.

The hybrid matrix $[H]_{\pi}$ for a 1π- sub-network is written as

$$[H]_{\pi} = \begin{bmatrix} 1+\frac{sRC}{2} & R \\ sC\left(1+\frac{sRC}{4}\right) & 1+\frac{sRC}{2} \end{bmatrix} = \begin{bmatrix} a_1 & b_1R \\ b_1sC\left(1+\frac{sRC}{4}\right) & a_1 \end{bmatrix} \tag{6-7}$$

where a_1 and b_1 are defined in Eqs.6-2b and 6-2c, and R and C are defined in Eqs.6-3a and 6-3b.

Let us assume that the hybrid matrix $[H]_{k\pi}$ for a $k\pi$- sub-network can be written as

$$[H]_{k\pi} == \begin{bmatrix} a_k & b_kR \\ b_ksC\left(1+\frac{sRC}{4}\right) & a_k \end{bmatrix} \tag{6-8}$$

where a_k and b_k are defined in Eqs.6-4b and 6-4c.

Combining Eq.6-8 with Eq.6-7, we obtain the hybrid matrix $[H]_{(k+1)\pi}$

$$
\begin{aligned}
&[H]_{(k+1)\pi} \\
&= [H]_{k\pi}[H]_{\pi} \\
&= \begin{bmatrix} a_k & b_k R \\ b_k sC\left(1+\frac{sRC}{4}\right) & a_k \end{bmatrix}\begin{bmatrix} a_1 & b_1 R \\ b_1 sC\left(1+\frac{sRC}{4}\right) & a_1 \end{bmatrix} \\
&= \begin{bmatrix} a_k a_1 + b_k b_1 sRC\left(1+\frac{sRC}{4}\right) & (a_k b_1 + b_k a_1)R \\ (b_k a_1 + a_k b_1)sC\left(1+\frac{sRC}{4}\right) & a_k a_1 + b_k b_1 sRC\left(1+\frac{sRC}{4}\right) \end{bmatrix} \\
&= \begin{bmatrix} a(k+1) & b(k+1)R \\ b(k+1)sC\left(1+\frac{sRC}{4}\right) & a(k+1) \end{bmatrix}
\end{aligned}
\tag{6-9}
$$

where $a_{(k+1)}$ and $b_{(k+1)}$ are defined in Eqs.6-5b and 6-5c.

Therefore, this proves that the hybrid matrices of n T- and n π- networks have the following forms

$$
[H]_{nt} = \begin{pmatrix} a_n & b_n R\left(1+\frac{sRC}{4}\right) \\ b_n sC & a_n \end{pmatrix} \tag{6-10a}
$$

and

$$
[H]_{n\pi} = \begin{pmatrix} a_n & b_n R \\ b_n sC\left(1+\frac{sRC}{4}\right) & a_n \end{pmatrix} \tag{6-10b}
$$

where a_n and b_n are functions of the product sRC, s is the complex frequency $j\omega$.

The relation between the load voltage and the load current at port 2 in Figure 6.2 is given by

$$-i_2(s) = sC_L v_2(s) \tag{6-11}$$

The non-normalized system response $Y(s, R_w, R_S, C_w, C_L)$ at load for both T- and π-structures is defined as:

$$Y(s, R_w, R_S, C_w, C_L) = \frac{V_2(s, R_w, R_S, C_w, C_L)}{V_1(s, R_w, R_S, C_w, C_L)} \tag{6-12}$$

In the special case where R_S=1, R_w=r, C_L=1, and C_w=c, we define Y to be:

$$Y(s, R_w = r, R_S = 1, C_w = c, C_L = 1) = \frac{V_2(s, R_w = r, R_S = 1, C_w = c, C_L = 1)}{V_1(s, R_w = r, R_S = 1, C_w = c, C_L = 1)} \tag{6-13}$$

According to Eqs.6-2a, 6-2b and 6–6, the normalized system responses $Y_t(s, r, 1, c, 1)$ and $Y_\pi(s, r, 1, c, 1)$ for T- and π-structures are

$$Y_t(s,r,1,c,1) = \frac{1}{a_n\left(\frac{src}{n^2}\right)(1+s) + b_n\left(\frac{src}{n^2}\right)\left[\frac{sc}{n} + \frac{sr}{n}\left(1 + \frac{src}{4n^2}\right)\right]} \tag{6-14a}$$

and

$$Y_\pi(s,r,1,c,1) = \frac{1}{a_n\left(\frac{src}{n^2}\right)(1+s) + b_n\left(\frac{src}{n^2}\right)\left[\frac{sr}{n} + \frac{sc}{n}\left(1 + \frac{src}{4n^2}\right)\right]} \tag{6-14b}$$

From Eqs.6-14a and 6-14b, we can see that:

$$Y_t(s,r,1,c,1) = Y_\pi(s,c,1,r,1) \tag{6-15}$$

That is to say, the system response of π-structure is the same as that of T-structure, if the value of r in the π-network is changed for the value of c in the T-network, and the value of c in the π-network is changed for the value of r in the T-network.

So the propagation time delay distribution of π-structures can be obtained from that of T-structures by a simple reflection symmetry with respect to the r=c line in the r-c plane, and vice versa. We will see later that this is also true for the non-normalized case.

Let us now examine the case where $C_L \neq 1$ and $R_S \neq 1$. Without loss of generality, we can assume that r and c are normalized quantities, that is

$$r = \frac{R_w}{R_S} \tag{6-16a}$$

and

$$c = \frac{C_w}{C_L} \tag{6-16b}$$

Using Eq.6-5a for the T-network case, we find:

$$Y_t(s, R_w, R_S, C_w, C_L) = \frac{1}{a_n\left(\frac{sR_wC_w}{n^2}\right)(1+sR_SC_L) + b_n\left(\frac{sR_wC_w}{n^2}\right)\left[\frac{sR_SC_w}{n} + \frac{sR_wC_L}{n}\left(1+\frac{sR_wC_w}{4n^2}\right)\right]} \tag{6-17}$$

Let us now multiply and divide s by τ_0, where $\tau_0 = R_s * C_L$. We have:

$$Y_t(s, R_w, R_S, C_w, C_L) = \frac{1}{a_n\left(\frac{s\tau_0 rc}{n^2}\right)(1+s\tau_0) + b_n\left(\frac{s\tau_0 rc}{n^2}\right)\left[\frac{s\tau_0 c}{n} + \frac{s\tau_0 r}{n}\left(1+\frac{s\tau_0 rc}{4n^2}\right)\right]} \tag{6-18}$$

If we define s' as $s' = \tau_0 s$, it can be seen from previous equation that

$$Y_t(s, R_w, R_s, C_w, C_L) = Y_t(s', r, 1, c, 1) \tag{6-19}$$

Similarly, we have

$$Y_{\pi}(s,R_w,R_S,C_w,C_L)=Y_{\pi}(s',r,1,c,1) \tag{6-20}$$

Combining Eqs.6-19, 6-20 with Eq.6-15, we have

$$Y_t(s',r,1,c,1)=Y_{\pi}(s',c,1,r,1) \tag{6-21}$$

In the complex frequency domain ($s=j\omega$), we can see that using normalized component values merely translates into a scaling of the frequency axis by a factor of τ_0. Consequently, the transient response of the normalized circuit will be the same as the original circuit's, but with a mere scaling factor of τ_0^{-1} of the time axis. The interconnect delays calculated with normalized circuit components should therefore be de-normalized, that is multiplied by τ_0, to obtain the delays in the real circuit. Following the same steps, the same conclusion can be reached for the π-network. Accordingly, the invariance property of the delay upon a transformation from a π- to a T- structure, which was proved in the previous paragraph, also applies to the non-normalized circuits for fixed values of R_S and C_L.

It is interesting that the Elmore delay τ_{ED} [70] (Appendix A) also has a symmetrical feature in the normalized r-c plane for RC wires with source resistance R_S and load capacitance C_L. As mentioned in Section 4.4.2.2, the Elmore delay τ_{ED} for RC wires can be expresses by [71]

$$\tau_{ED}=C_w\left(\frac{R_w}{2}+R_S\right)+C_L(R_w+R_S) \tag{6-22}$$

Combining Eqs.6-16a, 6-16b with Eq.6-22, we have

$$\begin{aligned}\tau_{ED}&=C_w\left(\frac{R_w}{2}+R_S\right)+C_L(R_w+R_S)\\&=R_SC_L(1+r+c+0.5rc)\\&=\tau_0(1+r+c+0.5rc)\end{aligned} \tag{6-23}$$

Eq.6-23 demonstrates that the Elmore delay τ_{ED} remains the same as the values of r and c are exchanged.

For RC wires with source resistance R_S and load capacitance C_L, a step voltage source means that the bandwidth of the load voltage will only be determined by the bandwidth of the system, which can be approximately estimated using the Elmore delay τ_{ED} as described in Section 4.4.2.2. Thus, we can explain why more T- or π- sections are needed for RC wires with a strong driver (large r=R_w/R_S) and with a light load (large c=C_w/C_L) as demonstrated in [25].

Given an RC wire, R_w and C_w are fixed. A strong driver means a large $r(R_w/R_S)$, while a light load means a large $c(C_w/C_L)$. Eq.6-22 can be rewritten as

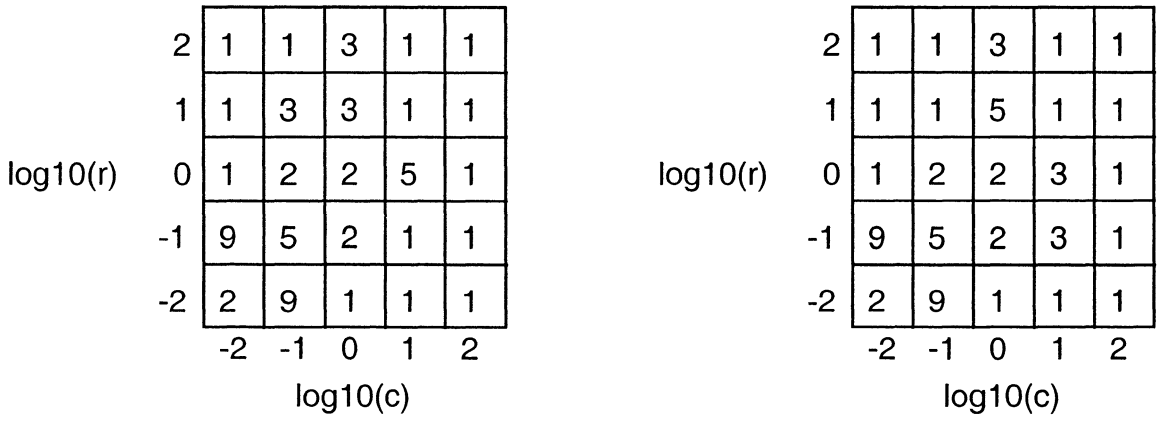
$$\begin{aligned}\tau_{ED} &= C_w\left(\frac{R_w}{2}+R_S\right)+C_L\left(R_w+R_S\right)\\ &= R_S C_L\left(1+r+c+0.5rc\right)\\ &= R_w C_w\left(\frac{1}{rc}+\frac{1}{r}+\frac{1}{c}+0.5\right)\end{aligned} \tag{6-24}$$

From Eq.6-24, it can be seen that the Elmore delay τ_{ED} will be smaller with a strong driver and a light load (case AA) than the one with a weak driver and a heavy load (case BB). Thus, the bandwidth of the load voltage with case AA is wider than the one with case BB, and the modeling accuracy of distributed RC wires with case AA has more impact on the simulation error than the one with case BB. Therefore, more T- or π- sections are needed for RC wires with case AA.

6.6 Numerical results

A software routine in C language has been implemented based on the two- and three-pole AWE method. All numerical computations were performed on a HP700 series workstation. In order to validate the accuracy of our program, a group of 25 points has

been sampled in the normalized r-c plane. The relative differences between the signal rise times, as predicted by AWE and SPICE, are shown in Figures 6.3a and 6.3b.



(a) 8T-structure (b) 8π-structure

Figure 6.3: Relative rise time difference (1/10000) between AWE and SPICE (8T- and 8π-sections, v_t=0.4)

Here, the stimulus is a unit step function for which the full swing on output is 1. The maximum relative differences among every group of 25 points taken above for T- and π-structures with 1, 2, 4 and 8 sections, for three voltage thresholds 0.2, 0.4 and 0.8, are listed in Table 6.1. These results show that the relative differences are independent on the number of sections, i.e., the complexity of circuit. There are some variations in the v_t=0.8 case, but it can be attributed to numerical errors in both SPICE and AWE. On the contrary, the relative differences depend on the voltage threshold. Note that AWE uses a small number of degrees of freedom to approximate the actual waveform, for example, a two-pole solution has only 4 degrees of freedom. Therefore, higher order approximations are needed if more accuracy is required [56].

Table 6.1: Maximum relative rise time differences between AWE and SPICE (T- and π- structures)

Section	v_t=0.2	v_t=0.4	v_t=0.8
1	0.15%	0.09%	0.04%
2	0.15%	0.09%	0.03%
4	0.15%	0.09%	0.04%
8	0.15%	0.09%	0.05%

For example, below two groups of figures are shown to illustrate the modeling accuracy increases with more T- or π- sections. Due to small variations of 4T- and 8T- structures, the values of time delays with 8T- or 8π- structures are taken as the reference. Figures 6.4a, 6.4b, 6.4c show the relative time delay difference between 1T- and 8T-, 2T- and 8T-, 4T- and 8T- structures, respectively. Figures 6.5a, 6.5b, 6.5c show the relative difference between 1π- and 8π-, 2π- and 8π-, 4π- and 8π- structures, respectively. All the time delays are for a voltage threshold of 0.4.

Figure 6.4a shows the relative difference of time delay at the voltage threshold of 0.4 between 1T- and 8 T- structures. The maximum difference reaches around 15% as the values of r and c become large at the corner.

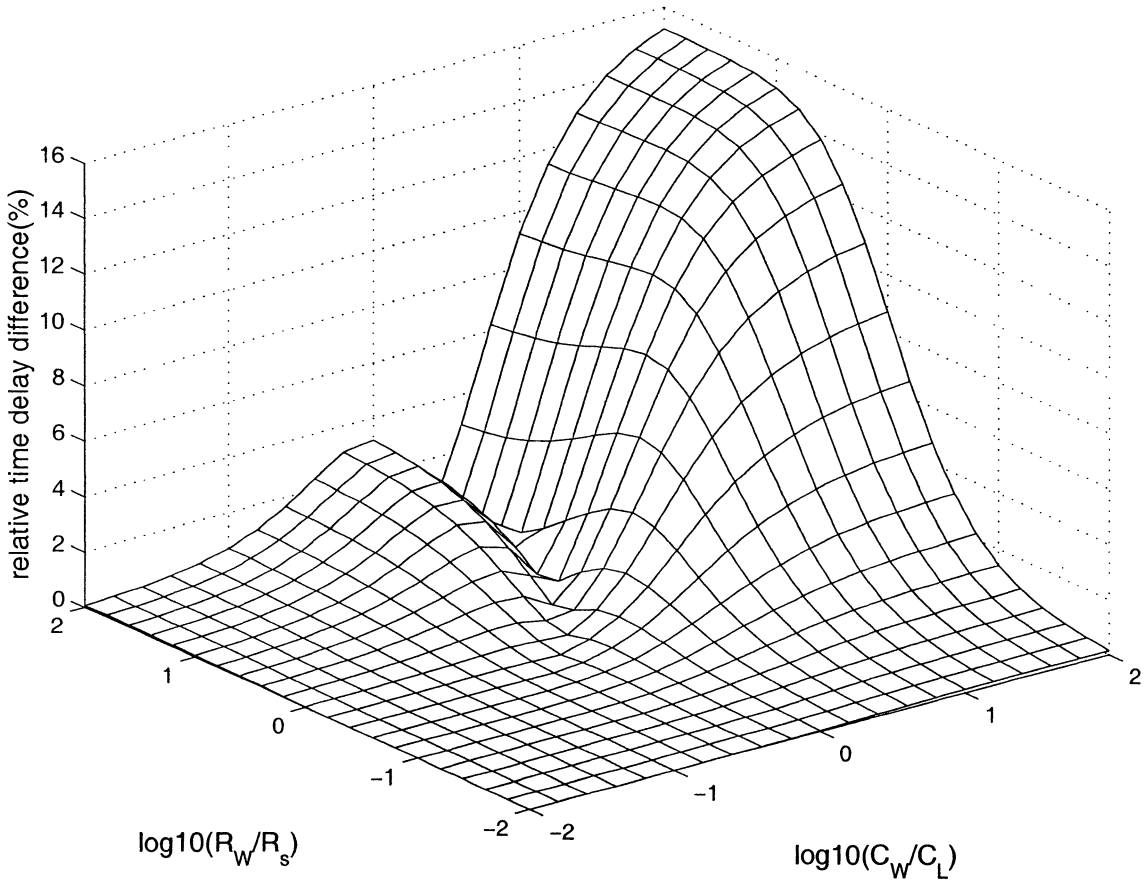


Figure 6.4a Relative difference time delay between 1T and 8T (v_t=0.4)

Figure 6.4b shows the relative difference of time delay at the voltage threshold of 0.4 between 2T- and 8 T- structures. Compared to Figure 6.4a, the peak value dramatically reduces to around 2.6%.

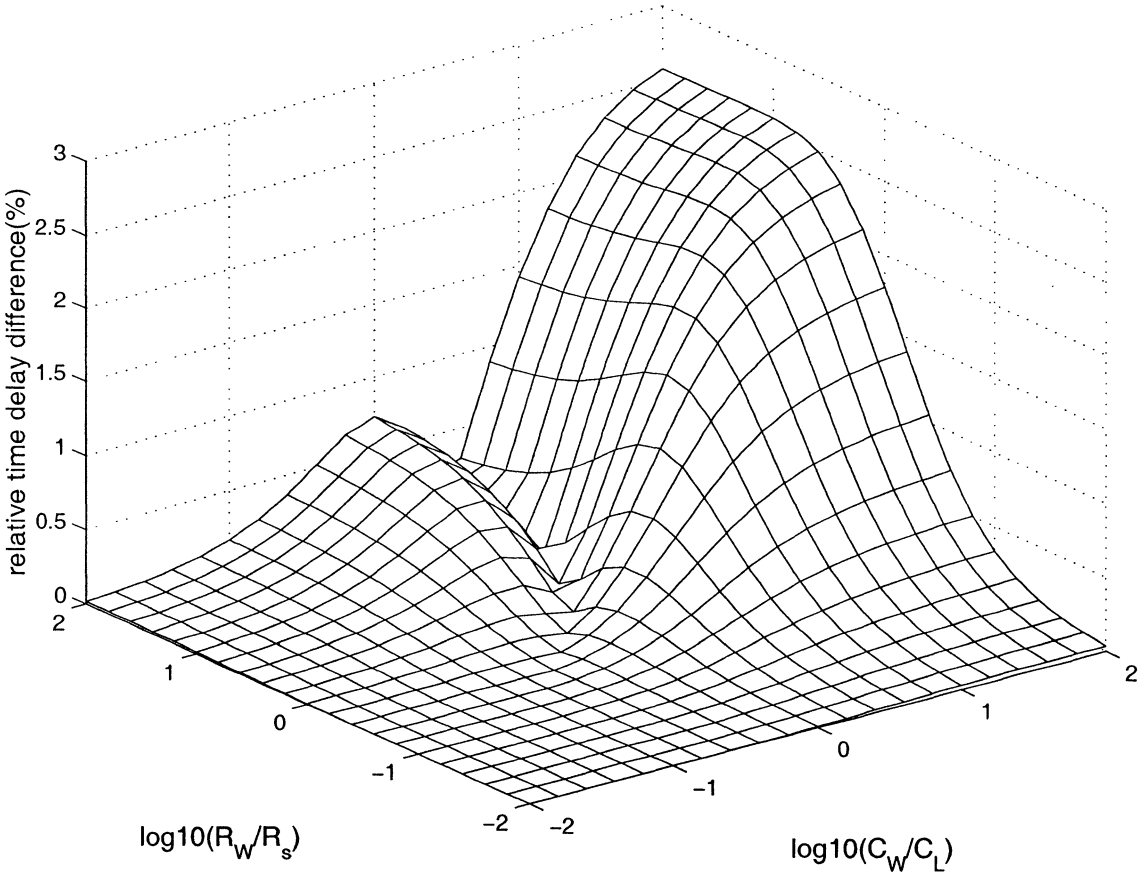


Figure 6.4b Relative time delay difference between 2T and 4T (v_t=0.4)

Figure 6.4c shows the relative difference of time delay at the voltage threshold of 0.4 between 4T- and 8 T- structures. Compared to Figures 6.4a and 6.4b, the peak value decreases to around 0.43%.

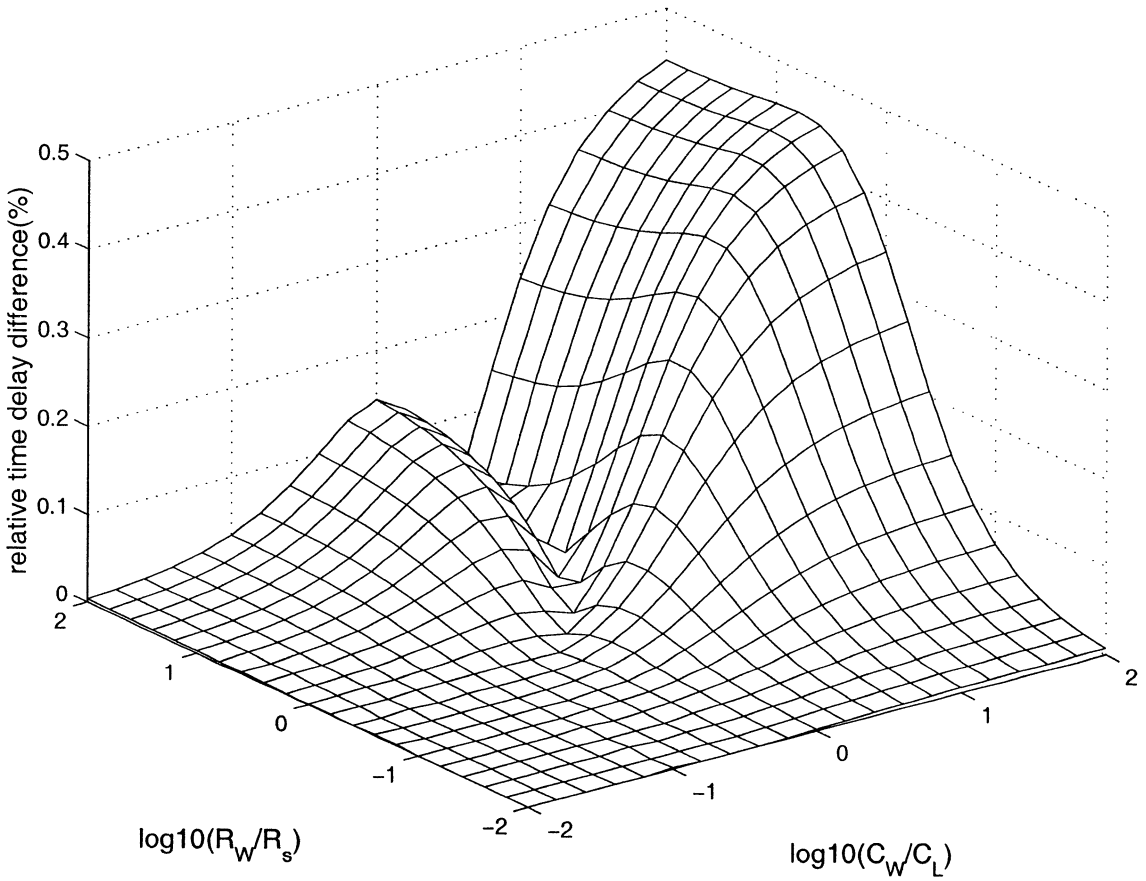


Figure 6.4c Relative time delay difference between 4T and 8T (v_t=0.4)

Figure 6.5a shows the relative difference of time delay at the voltage threshold of 0.4 between 1π- and 8 π- structures. The maximum difference reaches around 15% as the values of r and c become large at the corner. Compared to Figure 6.4a, two figures are similar due to the symmetric feature between T- and π- structures. If Figure 6.5a is mirrored with respect to a vertical plane with a (c, r, difference) = (1, -1, 0) normal, it becomes Figure 6.4a.

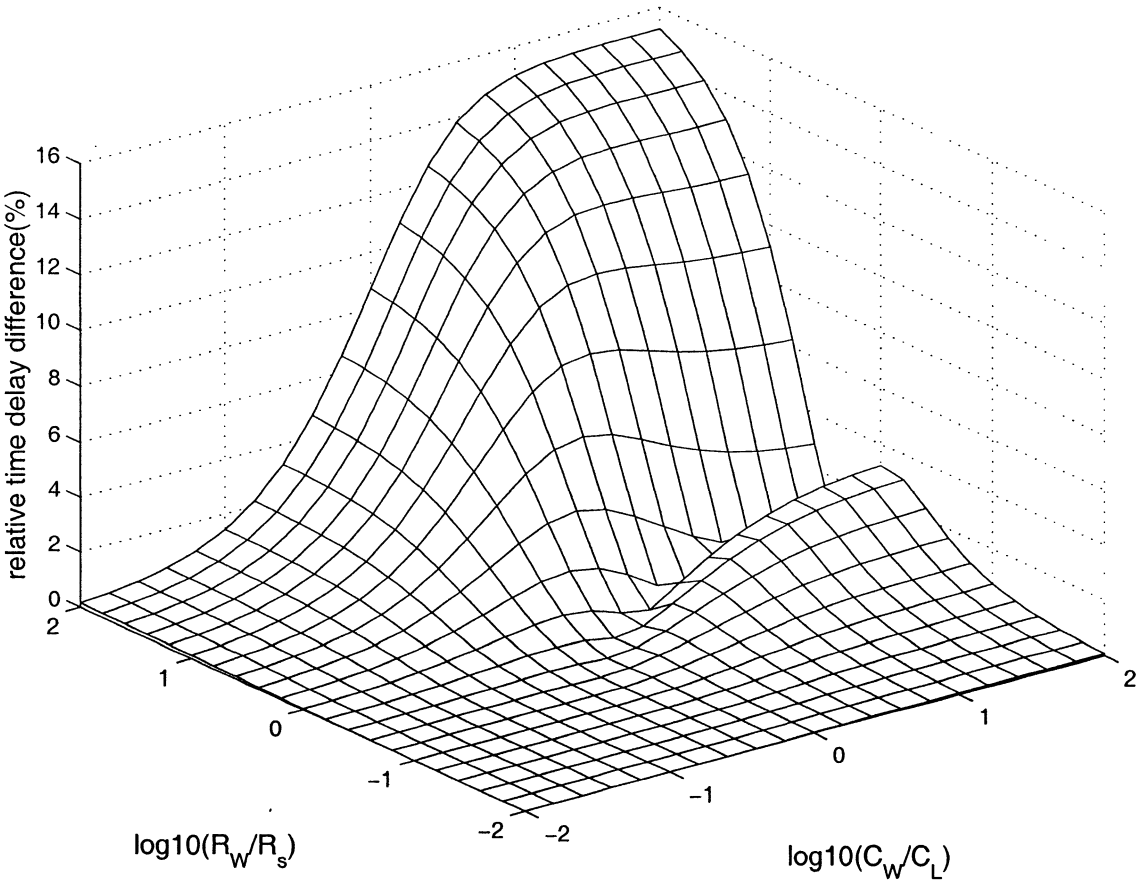


Figure 6.5a Relative time delay difference between 1π and 8π (v_t=0.4)

Figure 6.5b shows the relative difference of time delay at the voltage threshold of 0.4 between 2π- and 8 π- structures. The maximum difference reduces to around 2.6% as expected. Compared to Figure 6.5a, the two figures are similar because of the symmetric feature between T- and π- structures as mentioned above.

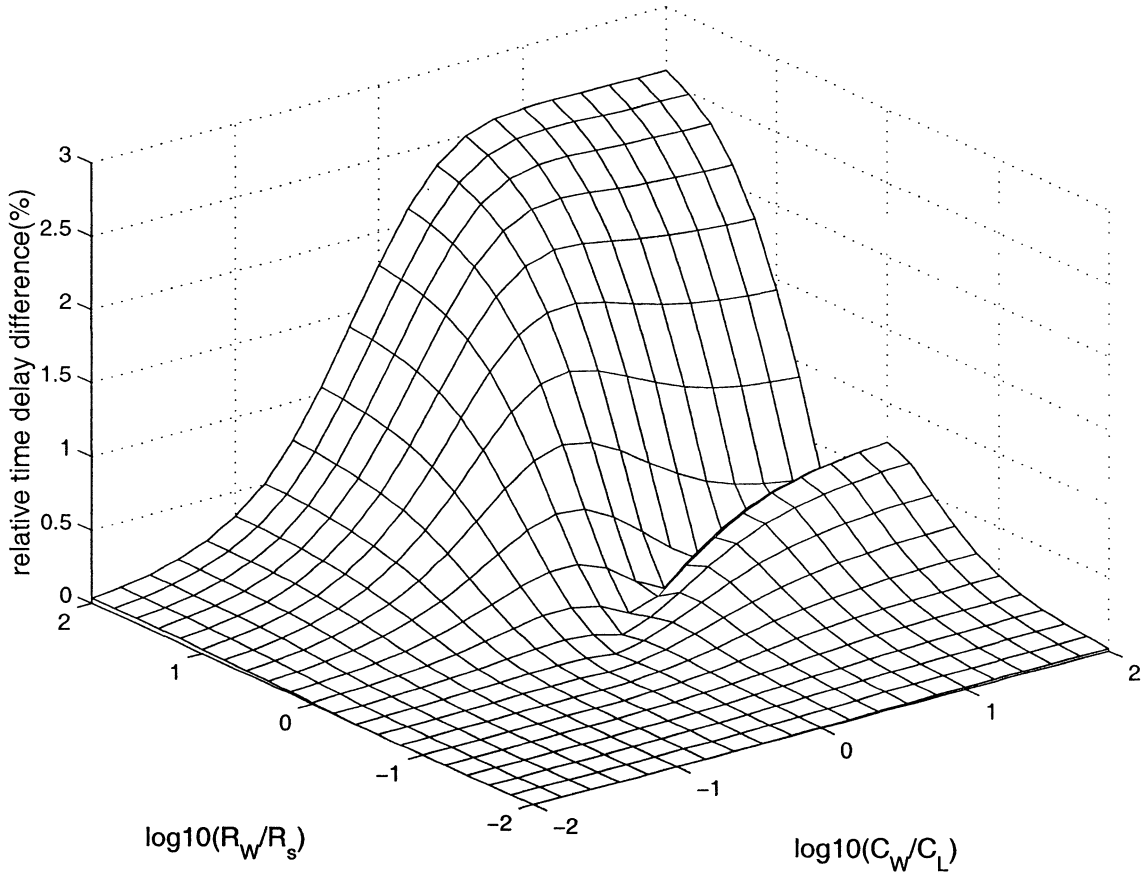


Figure 6.5b Relative time delay difference between 2π and 8π (v_t=0.4)

Figure 6.5c shows the relative difference of time delay at the voltage threshold of 0.4 between 4π- and 8 π- structures. The maximum difference decreases to around 0.43%. Compared to Figure 6.4c, the two figures are identical if Figure 6.5c is mirrored with respect to a vertical plane with a (c, r, difference) = (1, -1, 0) normal.

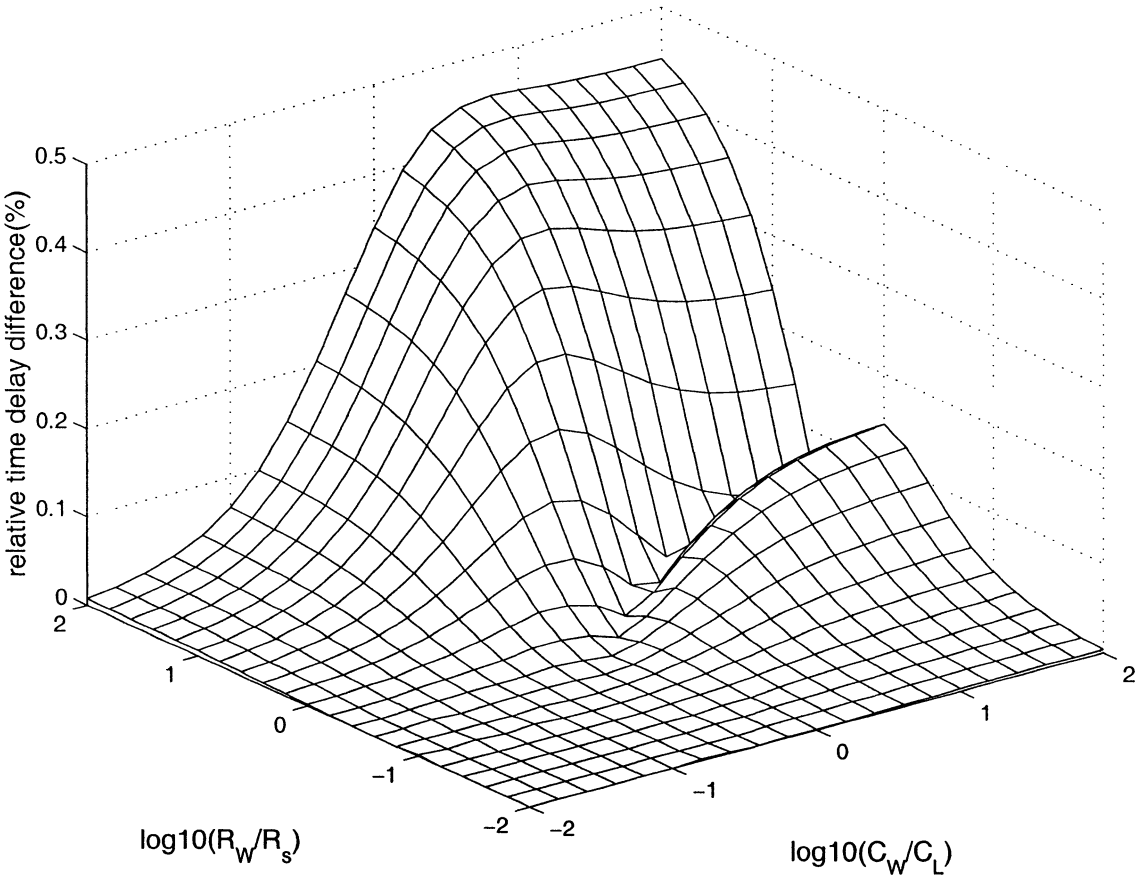


Figure 6.5c Relative time delay difference between 4π and 8π(v_t=0.4)

Similarly, we also obtain the relative time delay differences at other voltage threshold values 0.2 and 0.8. Peak values of relative time delay differences for all the situations comprised in the 4-decade by 4-decade r-c range are listed in Table-6.2. From the table, we can clearly see the rapid convergence of computed delays with the increasing number of sections. The relative differences between 4T and 8T, are as low as 1.9%, 0.43% and 0.41%. While the rate of convergence has the same order of magnitude for the three

values of voltage threshold, the relative difference remains larger for the initial portion of the waveform, as it was the case in the AWE versus SPICE comparison. Of course, the absolute time to reach lower threshold levels is smaller. Therefore, the higher relative time delay differences shown in Tables 6.1 and 6.2 may not be indicative of higher absolute time delay differences.

Table 6.2: Relative time delay differences (T-and π-structures)

Sections	v_t=0.2	v_t=0.4	v_t=0.8
1-8	37 %	15 %	6.7 %
2-8	10 %	2.6 %	2.0 %
4-8	1.9%	0.43 %	0.41%

The maximum relative time delay differences between 8π- and 8T-sections, for three voltage thresholds 0.2, 0.4 and 0.8 are respectively 0.50%, 0.17% and 0.088%, which are comparable to the differences between AWE and SPICE (0.15%, 0.09% and 0.05%). We also know that there is virtually no difference in the response of a 10-section ladder and a 100-section ladder [55]. Therefore, it is reasonable to regard the results obtained with 8-sections as a reference for distributed RC models.

Practically, the relative time delay difference at a voltage threshold of 0.5 is more useful. Below, another group of figures at the voltage threshold of 0.5 is used to illustrate how to model RC wires with source resistance R_S and load capacitance C_L.

Figures 6.6a and 6.6b show the relative time delay differences between 1- and 8-sections for T- and π-structures respectively at a voltage threshold of 0.5. The ranges of r and c are from 0.01 to 100. The peak values of relative time delay differences in Figures 6.6a and 6.6b are 8.1%.

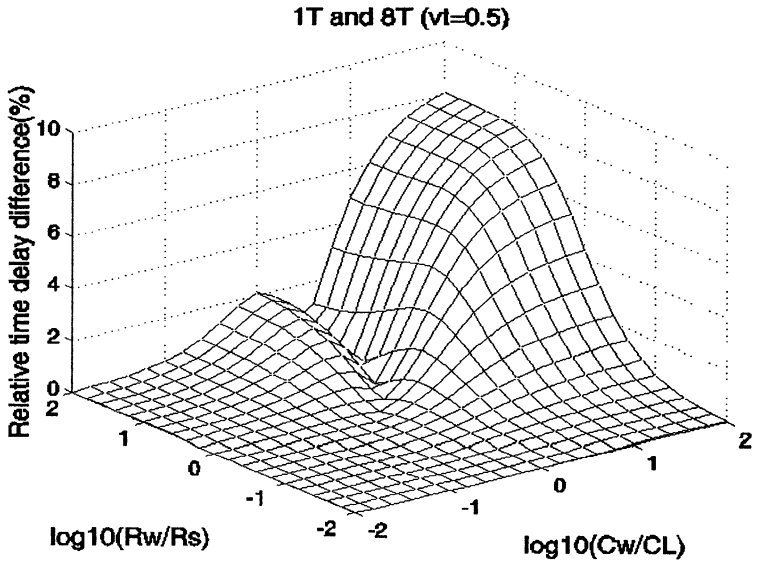


Figure 6.6a: Relative time delay difference between 1T- and 8T- sections models

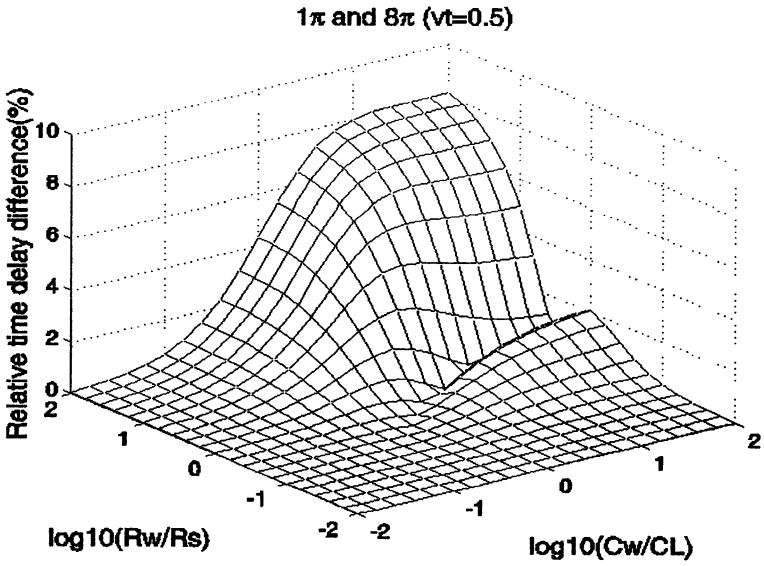


Figure 6.6b: Relative time delay difference between 1π- and 8π- sections models

Figures 6.7a and 6.7b plot the contours of absolute and relative differences between 1- and 8- sections for a voltage threshold of 0.5. For a given error tolerance, a proper structure with a sufficient number of sections can be selected from the contours of error distributions. For example, an RC wire has wire resistance 0.75 kΩ and wire capacitance 0.5 pF with source resistance 1 kΩ and load capacitance 1 pF. Therefore, the normalized r and c are 1 and 0.5, respectively. Also, the logarithmic values of r and c with base of 10 are -0.125 and -0.3, respectively. Assuming an absolute time delay tolerance of 0.1 ns, it equals to 0.1 τ_0 (R_S*C_L). In figure 6.7a, we can find two curves indicated with 0.1(t) and 0.1(π), respectively. That is to say, for a point located at the top right side of these curves, the absolute time delay difference will be above 0.1 τ_0, while it will be below 0.1 τ_0 (R_S*C_L) for a point located at the bottom left side of these curves. It is found that the point (-0.3, -0.125) is at the top right side of the curve marked with 0.1(π) and is at the bottom left side of the curve marked with 0.1(t). Thus, a model with 1T-section satisfies the accuracy requirement, while a model with 1π-section violates the error tolerance.

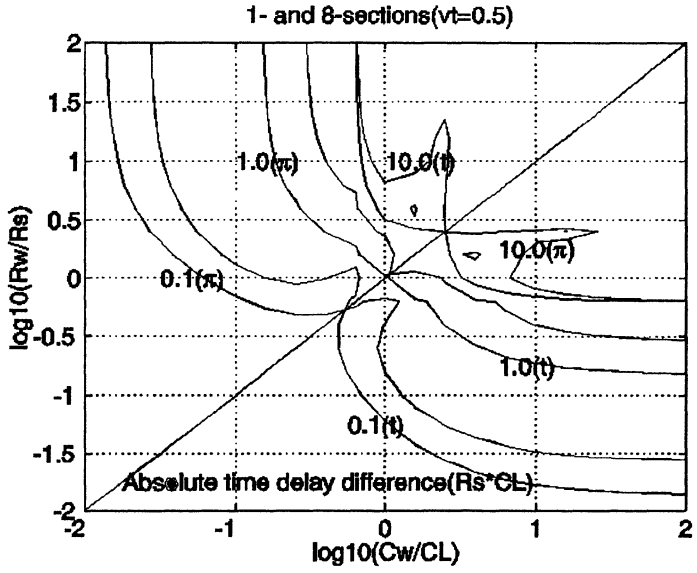


Figure 6.7a: Absolute time delay difference between 1- and 8- sections (unit in R_S*C_L)

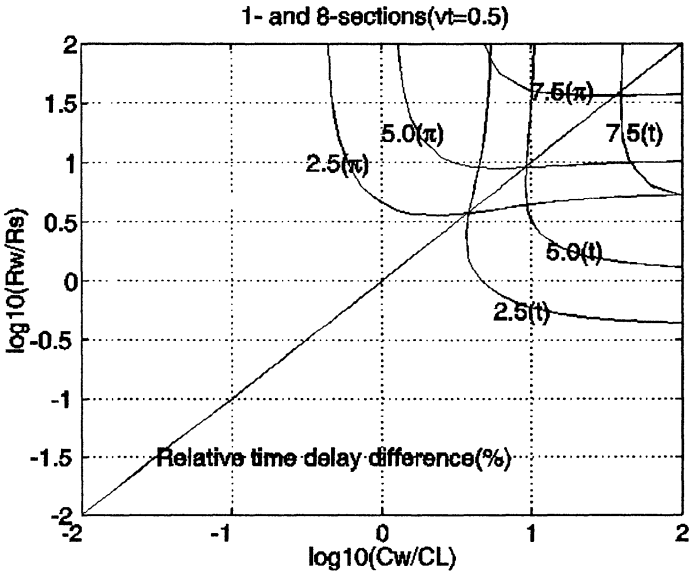


Figure 6.7b: Relative time delay difference between 1- and 8- sections (unit in %)

Similarly, given a relative time delay error tolerance of 2.5%, we can find two curves indicated with 2.5(t) and 2.5(π) in Figure 6.7b. It means that the relative time delay difference will be above 2.5% if a point is located at the top right side of these curves, while it will be below 2.5% if a point located at the bottom left side of these curves. Note that the point (-0.3, -0.125) is at the left bottom side of either of the two curves marked with 2.5(t) and 2.5(π). A model with 1T- or 1π- can satisfy the relative error tolerance of 2.5%.

Therefore, for a given number of sections, if r > c, it is better to use a T-structure. Otherwise it is better to select a π-structure. The number of sections is dependent on the error tolerance. A noteworthy feature is that absolute and relative time delay differences between sections of a π -structure behave symmetrically compared with those of a T-structure with respect to the *r=c* line. This was demonstrated earlier (see Eq.6-15).

6.7 Summary

In this chapter, we have studied the validity conditions for modeling a wire with RC sections. Two- and three-pole AWE was used to analyze time delay on RC wires. The accuracy of lumped models increases with the number of sections. The peak values of relative time delay differences between 1- and 8-sections can reach 37%, 15% and 6.7% for voltage threshold 0.2, 0.4, and 0.8 respectively. Between 2- and 8-sections, these peaks decrease to 10%, 2.6% & 2.0%. For 4- and 8-sections, these peaks reduce to 1.9%, 0.43% and 0.41%. Using the information provided in this chapter, a user can select a model of minimal complexity that meets his accuracy requirements. In some cases, the basic cell structure (T- or π-) has a significant impact on accuracy for a given model complexity, and this chapter allows selecting the most efficient model.

Because the step-response for an RC-class wire is monotonic, it is possible to analyze time delay simply without considering signal dispersion and signal symmetry [30]. Unfortunately, time delay estimation of RLC wires are more complicated since the system response can be under-damped, critically damped or over-damped. Therefore, the step response can undershoot or overshoot. As mentioned by Gupta *et al.* [30], transmission line interconnect delays cannot be accurately predicted unless a termination scheme is chosen and properly implemented.

CHAPTER 7

PROPAGATION TIME SKEW ANALYSIS IN WSI CIRCUIT DESIGN

7.1 Introduction

As mentioned in [57], high-speed applications implemented with WSI impose stringent requirements on very long interconnects. Signal propagating on extremely long lossy interconnects are more susceptible to problems with transmission line effects, such as loss of signal integrity, electromagnetic interference (EMI), crosstalk, reflections, and ground bounce. Consequently, propagation delay skew is an important issue in wafer scale integrated (WSI) circuit design. Existing methods to reduce the propagation delay skew can be implemented at the software level, hardware level, or both as mentioned in [58]. This chapter analyses and confirms the validity of some solutions emerged from a research team.

7.2 Considered structure and problem formulation

In a possible WSI system configuration, a wafer consists of hundreds of functional cells, and the edge size of each cell is 8 mm. Among hundreds of functional cells, there are more than 10^5 long interconnects transferring signals. In order to improve signal integrity, two repeaters are inserted for each signal line of 8 mm. Figure 7.1 shows a layout example of an "8+2" structure with inverters only. There are 8 signals $\{D_0D_1D_2D_3D_4D_5D_6D_7\}$ propagating in one direction and 2 power/ground wires as indicated in Figure 1. This circuit is representative of 2.5 cells.

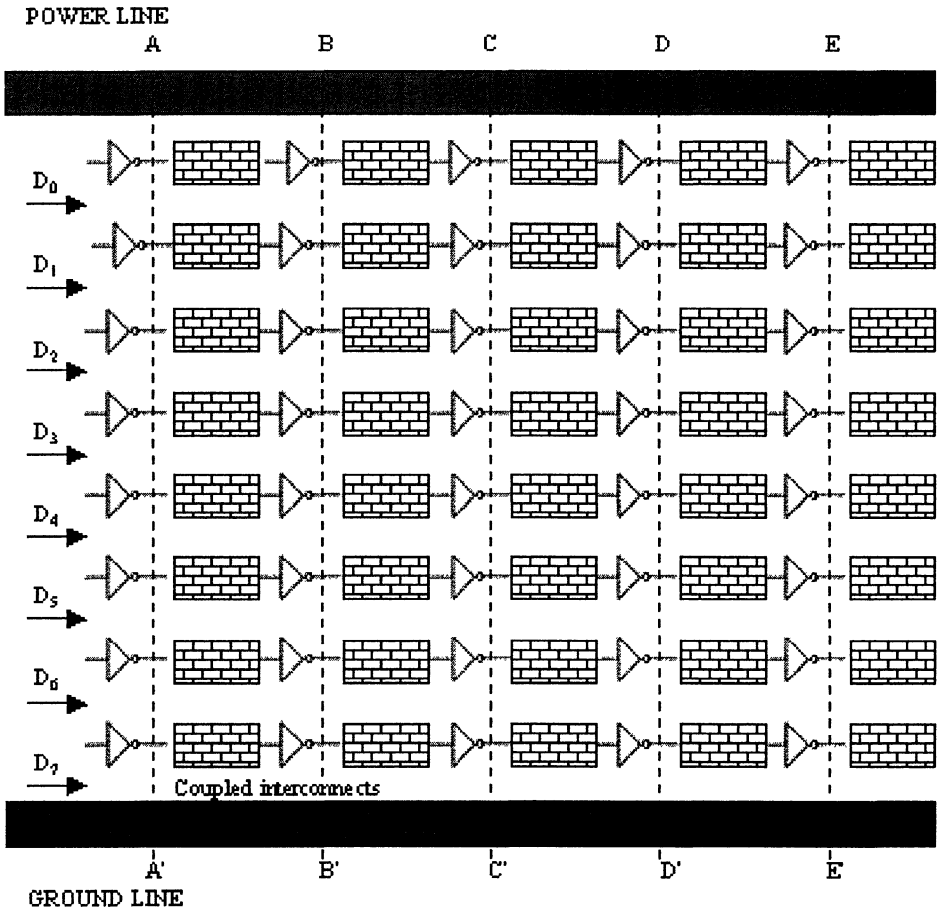


Figure 7.1 Topology of "8+2" interconnects with inverters only (signals propagate in the same directions)

7.2.1 Analysis of the"2+2" topology

In order to illustrate current flowing in the topology of Figure 7.1, we reduce the number of signal wires from 8 to 2 and analyze a simple "2+2" topology in Figure 7.2, where there are 2 signal wires with 2 power/ground lines on both sides.

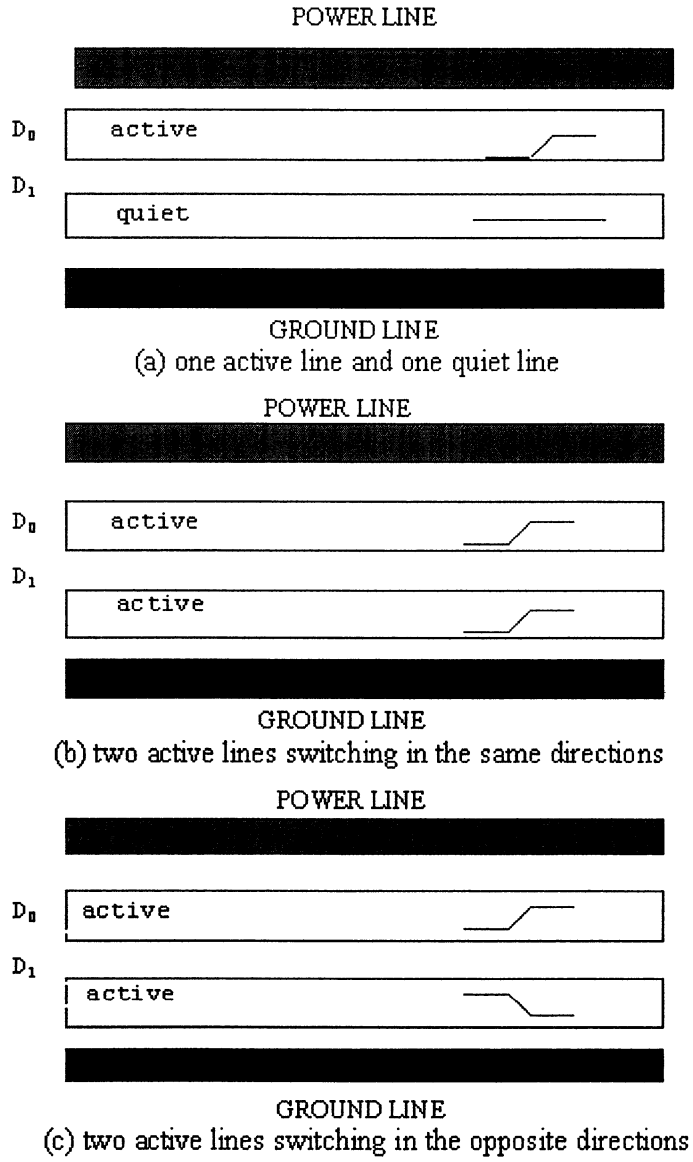


Figure 7.2 Topology of "2+2" interconnects

As shown in Figure 7.2, there are three cases for the two signal lines. In case one there is one active line (switching) and one quiet line (no switching). Case two refers to the situation where both lines are active and the two signals switch in the same directions from voltage level "0" to "1". Case three is similar to case two and the two signals switch in opposite directions.

An equivalent circuit of coupled interconnects for the "2+2" topology in Figure 7.2 is represented in Figure 7.3. Here, R_1, L_1 and C_1 are the per-unit-length wire resistance, inductance and capacitance for signal line 1. Similarly, R_2, L_2 and C_{12} are the wire parameters for signal line 2. There are coupling capacitance C_{12} and mutual inductance L_{12} between two signal lines. For simplicity, we assume that the two signal lines are identical.

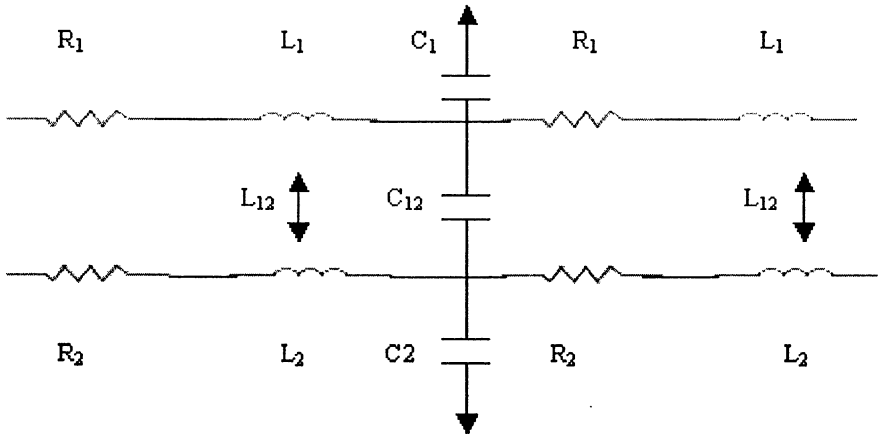


Figure 7.3 Equivalent circuit of two coupled interconnects with power and ground lines

For case one, where one signal line is active and the other is quiet, the quiet line can be treated as a shielding ground line. Thus, the wire capacitance for the active signal line is the sum of C_1 and C_{12}.

As to case two, where two signals switch simultaneously in the same direction from low levels voltage to high, the apparent wire capacitance for the active signal line is only C_1.

For case three, where two signals switch simultaneously in the opposite directions, one is from low voltage level to high, and the other is from high voltage level to low. The apparent capacitance for the active signal line is the sum of C_1 and $2C_{12}$.

Therefore, the effective wire capacitance for the same signal line 1 varies from C_1, C_1+C_{12} to C_1+2C_{12} in three cases. Under the same source and load conditions for slow switching rate, the propagation time delay is longest for case three, shortest for case two, and has an average value for case one. Therefore, the propagation time delays for two wires will vary from the maximum to the minimum values, and there will be a difference between actual and required propagation time delays. Such a time difference is called the propagation time skew. As shown in Figure 7.1, signals will propagate through many segments with inserted repeaters. A possibility consists in alternatively using cases two and three; the longest propagation time delay can thus be compensated by shortest propagation times on different segments. In that case, the total propagation time delay variations over many segments can be reduced, which reduces bus skew accordingly. This is one of the methods of reducing propagation time skews, which will be further discussed in the following.

7.2.2 Analysis of the"8+2" topology

As shown in Figure 7.1, there are 8 signal wires with 2 power/ground lines. Though the coupling among 8 signal wires is more complicated to analyze than the coupling between 2 signal wires with 2 power/ground lines, there is similarity between topologies of "8+2" and "2+2", under the condition that only two of eight wires are active at one time. At low frequency, we can still have that two signals of neighbour wires switching

in the same directions propagate more quickly than two signals in the opposite directions.

For the "8+2" topology, the coupling effect is normally dominated by adjacent neighbour wires. The interference between two neighbour wires separated by a large distance becomes weak if the two wires are shielded by one or more than one wires. Thus, if there are only two active wires at one time, the propagation time skew will be larger for two adjacent active wires than the skew for two active wires shielded by one or more than one quiet wires. Practically, there may be more than two active wires at a time.

Below, a group of simulations have been performed to analyze the propagation time delay variations among a set of wires as shown in Figure 7.1. Based on the simulation results, we propose a method to reduce the propagation time skew. Here, the 8 signal wires and 2 power/ground lines are modeled by multilayer interconnects, which are embedded in Agilent Technology ADS software package. The set of parameters for the multilayer substrate and interconnects are listed in Table 7.1. There are two substrate layers as shown in Table 7.1: SiO_2 and Si. The interconnects are assumed to be copper with conductivity 5.7×10^7 S/m. The width of power/ground lines is 3 μm and is three times the width of signal wires. These parameters are based on a 0.8 μm CMOS technology, and they are used to illustrate our method of reducing propagation time skew. However, the method introduced below can also be applied to other deep sub-micron technologies with certain adjustments.

Table 7.1: Main parameters of multilayer substrate and interconnects

Multilayer Substrate			Multilayer Interconnects (Metal)	
Substrate	Parameter	Value	Parameter	Value
Insulator SiO_2	ε_{ri}	3.82	conductivity σ_m (S/m)	5.7×10^7
			thickness t_m (μm)	1
	t_i (μm)	2	width w_m (μm)	1 (signal) 3 (power/ground)
Semiconductor Si	ε_{rs}	11.9		
	$\tan\delta_l$	1	spacing s_m (μm)	3
	t_s (μm)	300		

In Figure 7.1, inverters consist of pmos and nmos transistors from a 0.8μm CMOS technology. Sizes of inverters are listed in Table 7.2. Here, the length of interconnects between repeaters is 4mm. Sizes of buffers used in the following are also included. In order to minimize propagation skews, the sizes of buffers need to be adjusted so that buffers have almost the same rise and fall times.

Table 7.2: Sizes of inverters and buffers

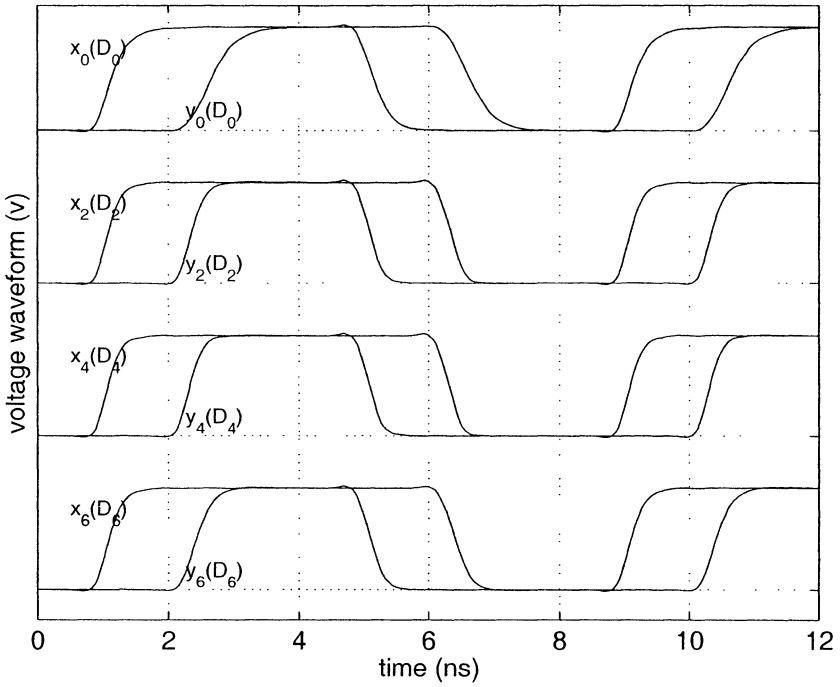
Inverter		Buffer	
Parameter	Value (μm)	Parameter	Value (μm)
w_p	88.2	w_{p1}	54
w_n	25.2	w_{n1}	18
		w_{p2}	96
		w_{n2}	38

In order to illustrate the signal integrity problem, a train of voltage pulses is used to analyze the propagation time uncertainty (skew). The rise and fall time of these pulses is 1 ns, the stable time is 3 ns, and the period is 8 ns. This is representative of a 125 MHz clock speed with 50% duty cycle.

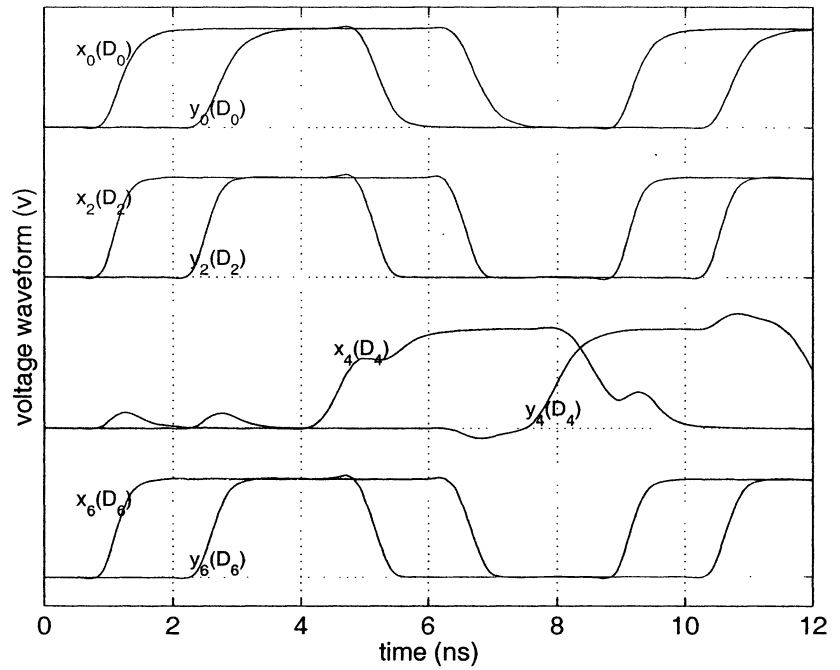
Two cases A_1 and A_2 are analyzed with the "8+2" structure shown in Figure 7.1, where signals propagate in one direction and are regenerated by inverters only. Assuming that we have an ideal zero-impedance power supply, case A_1 refers to the situation where the propagation time is shortest. Here, all 8 signals $\{D_0D_1D_2D_3D_4D_5D_6D_7\}$ switch simultaneously. That is to say, the rise and fall transitions of all 8 signals occur almost at the same time. All these signals reinforce each other through capacitance coupling. Thus, it approximates the case where signals travel at the fastest speed.

Case A_2 approximates the situation where one signal travels at the slowest speed. Here, 7 signals $\{D_0D_1D_2D_3D_5D_6D_7\}$ switch simultaneously, while signal D_4 is transmitted with an intentional delay of 3.15 ns. The value of 3.15 ns is obtained by progressively varying the initial time delay of D_4 with respect to the other 7 signals $\{D_0D_1D_2D_3D_5D_6D_7\}$, and by retaining the phase relationship that maximizes the delay. Here, delay is almost a half-period, so it is equivalent to send a negative pulse with an initial delay of –0.85 ns. The resulting worst case is obtained when D_4 is almost out of phase with the other 7 signals, where the propagation on D_4 is combated by the transitions injected on its neighbours.

Figures 7.4a and 7.4b show the voltage waveforms of 4 signals $\{D_0D_2D_4D_6\}$ for cases A_1 and A_2. In these figures, x_i and y_j (i, j=0, 2, 4 and 6) refer respectively to planes AA′ and EE′ in Figure 7.1. The rising edges of voltage waveforms at nodes before and after 4 interconnect segments are used to measure the propagation time delay uncertainty. The average propagation time delay is around 2.24 ns when only one of the 8 signals is switching. The maximum and minimum time delays for case A_1 are 1.513 ns and 1.238 ns, respectively. This is significantly less than the 2.24 ns value obtained for single signal switching. The maximum and minimum time delays for case A_2 are 3.364 ns and 1.4 ns, respectively. There is 2.126 ns (=3.364 – 1.238) time delay difference between the fastest and slowest signals. Thus, there is a large propagation time uncertainty among 8 signals. It reaches one-fourth of the clock cycle. Consequently, it is clear that



(a) Case A_1: Simultaneous switching



(b) Case A_2: t_{d4}=3.15 ns and t_{di}=0 ns (i=0,1,2,3,5,6,7)

Figure 7.4 Propagation time skew analysis for "8+2" structure with inverters only (8 signals propagating in one direction)

simultaneous switching, either in-phase or out-of-phase, is causing the variability in the propagation time delay. One of the skew reduction strategies to be presented in the foregoing section is partly based on the reduction of simultaneous switching through systematic design.

7.3 Proposed approaches for a wafer scale integrated system

Practically, methods to minimize skew can be implemented at hardware level together with methods at software level. Means of reducing crosstalk are called software methods when we only change how interconnects are used, as opposed to how they are physically implemented.

Based on existing methods, we propose a combined method to reduce the propagation time skew among parallel bus interconnects. Similarly to others, we insert repeaters to suppress crosstalk among neighbour wires and use intentional time offsets (or forced skew) to avoid simultaneous switching on neighbour wires. There are three approaches that will now be presented.

7.3.1 Approach one
—— Bus with interspersed directions of data flow

At first, we propose to have opposite propagation directions for neighbour wires on a bus. This is illustrated in Figure 7.5, where loads are not shown. In principle, adjacent signals propagating in different directions will interact only during limited times over the whole path. Such reduced interaction time window interval should lead to reduced impact of crosstalk on the propagation delay, whereas in the same direction, these signals could interact for the whole duration of propagation. This method is very effective for systems where equal or comparable number of signals must flow in two opposite directions. This feature is rather common in practice.

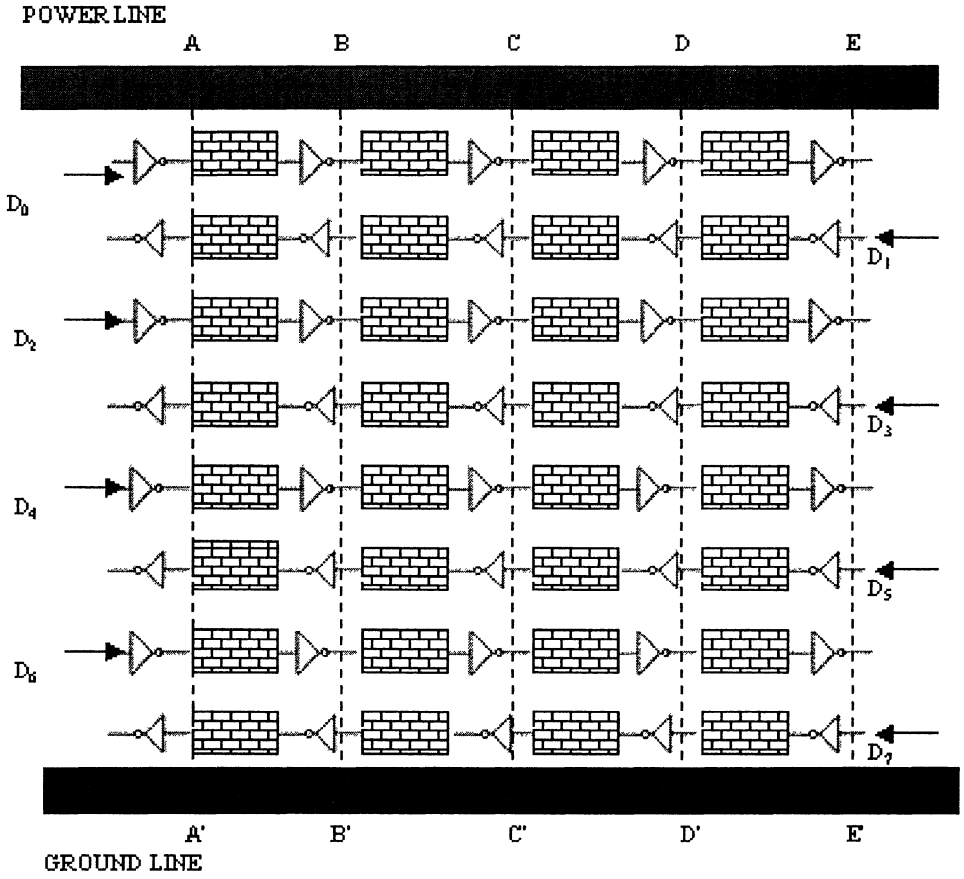
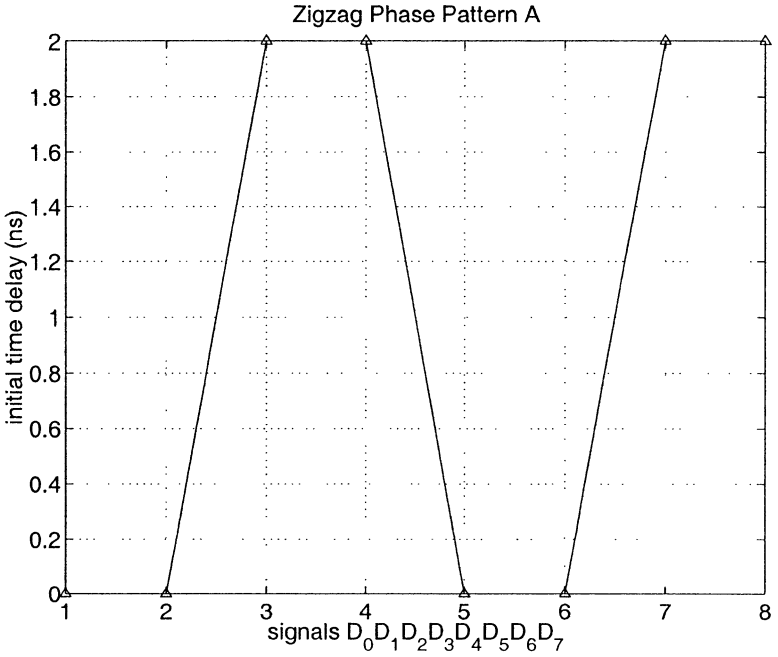


Figure 7.5 Topology of "8+2" interconnects with inverters only
(signals propagate in the opposite directions)

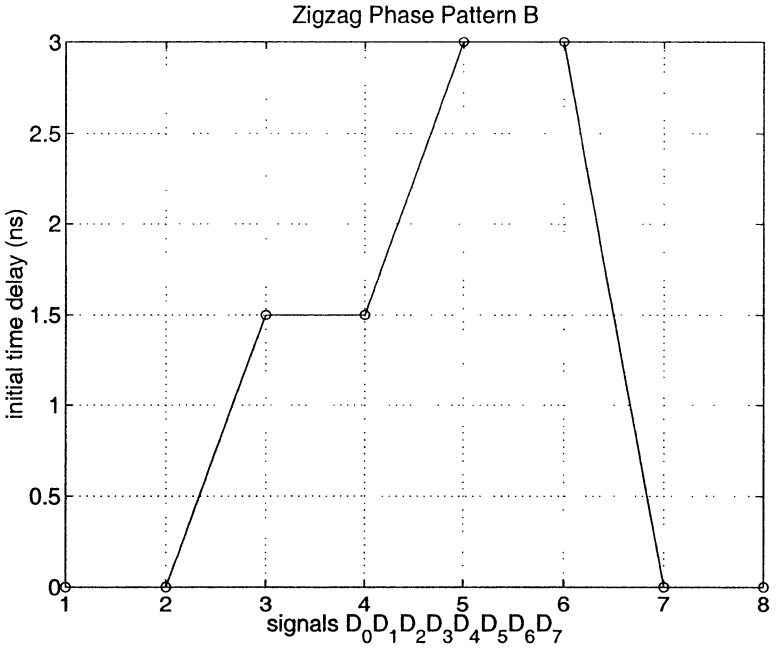
7.3.2 Approach two
——Spatially modulated signal phase pattern

As seen in Figure 7.4b, disturbance is induced on D_4 only when the other signals are switching. Such disturbances are harmless in general, unless they occur while the victim signal is also switching between states. It was conjectured that a skew minimization scheme could be implemented by inserting time offsets between the switching of source and victim signals.

One way to implement this is to use a zigzag phase pattern for parallel neighbour wires carrying signals in the same direction. As illustrated in Figures 7.6a and 7.6b, two zigzag phase patterns are used to provide enough time segmentation intervals between the switching of near neighbour wires. Pattern A separates the switching between the near neighbours in one direction. For instance, signals D_0, D_2, D_4 and D_6 have respective initial delays of 0, 2, 0 and 2 ns. These intentional delays minimize the impact of crosstalk among near-neighbour wires on the propagation time delay. Pattern B separates not only the switching between the near neighbours in one direction such as $\{D_0D_2\}$ and $\{D_2D_4\}$, but also the switching between the far neighbour wires in the same direction such as $\{D_0D_4\}$. In the foregoing section, both phase patterns A and B are investigated to illustrate the multiple choices of phase patterns. Practically, the impact of crosstalk between the near neighbours often dominates the propagation time skew. In these situations, only pattern A is needed. Otherwise, a more complex pattern such as pattern B can be used to reduce the influence of the switching between far neighbours on the total propagation time skew.



(a) Phase pattern A



(b) Phase pattern B

Figure 7.6 Zigzag phase patterns

7.3.3 Approach three
——Skew compensation by dual-polarity crosstalk

The skew compensation scheme is implemented with the alternative usage of buffers and inverters as repeaters for parallel neighbour wires in one direction. Let us consider two coupled signals, one taken as the source of crosstalk and the other as the victim. These two signals are interacting over a number of consecutive interconnect segments, as shown in Figures 7.1 and 7.5. If on one segment these two signals have opposite polarities, and if on the other consecutive segment these two signals keep the same polarity, then the crosstalk will first slow down and then speed up the victim signal (or vice versa). Thus, the overall effect after two segments should be negligible. This scheme can be implemented with more than two signals as will be shown later.

An implementation of this principle is illustrated in Figure 7.7. At hardware level, there are two features for the topology of interconnects in Figure 7.7:

- Signals alternatively propagate in opposite directions;
- Buffers and inverters are alternatively used as repeaters along each interconnect;
- If one given interconnect begins with a buffer, then the closest interconnect propagating in the same direction begins with an inverter.

The difference between this approach and that of Zhang [62] is that Zhang proposed to use inverters only but in a staggered configuration with half-segment offsets. At hardware level, the structure of Zhang is similar to the topology of interconnects in Figure 7.5. However, there is no shifting for the repeaters in Figures 7.5 and 7.7. Our purpose is to reduce skew. We achieve similar objective with a structure different from the one proposed by Zhang. The two techniques are somewhat similar since they superimpose positive and negative interferences.

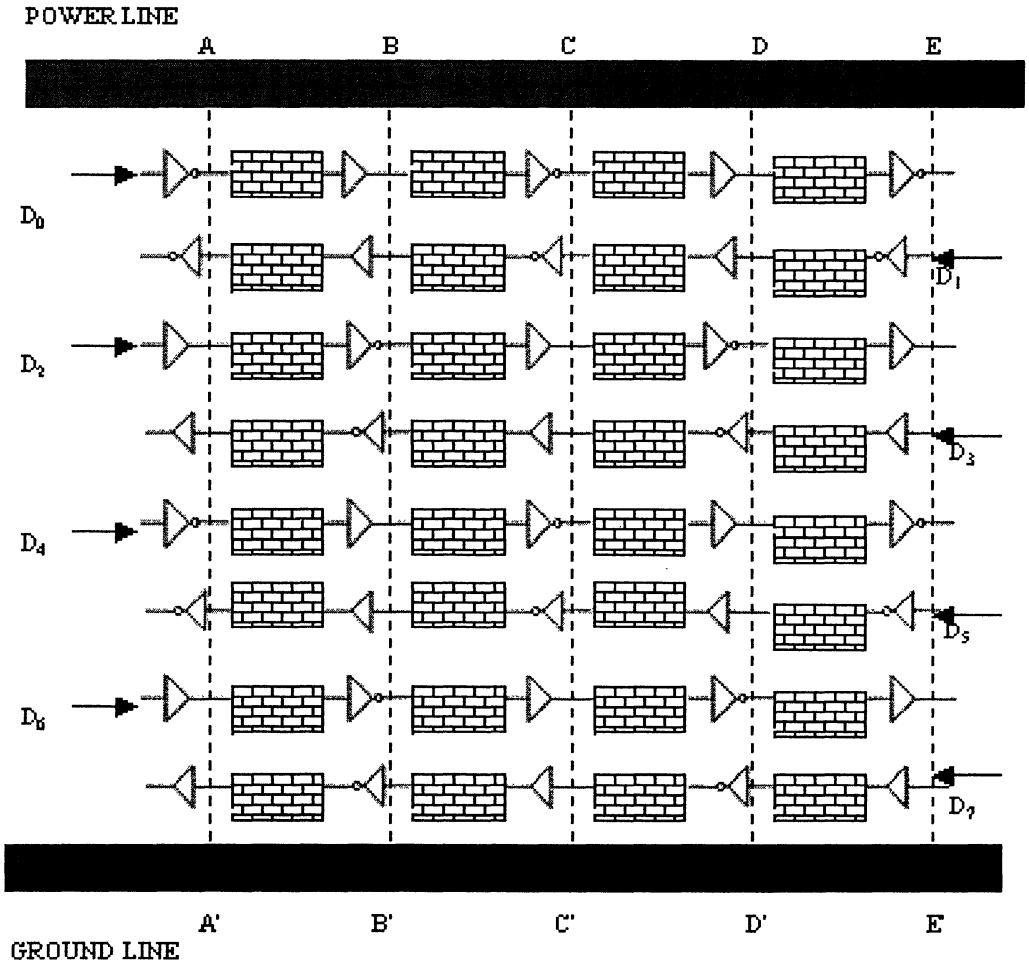


Figure 7.7: Topology of "8+2" interconnects with both buffers and inverters (signals propagate in two directions)

7.4. Simulation results

In order to demonstrate the effectiveness of the three techniques presented in the previous section, we use four cases, as shown in Table 7.3, to analyze the propagation time skew. The layout structure of cases A_1 and A_2 is shown in Figure 7.1. The layout structures of cases B_1 and B_{10}, B_2 and B_{20}, C_1 and C_{10}, C_2 and C_{20}, are shown in Figure 7.5, and the layout structures of cases D_1 and D_{10}, D_2 and D_{20} are shown in Figure 7.7. Here, index "0" means that on a bi-directional bus, only the signals on one direction are activated.

Table 7.3: Propagation time skew analysis

Cases	Methods			Layout Structure
	One/two direction	Zigzag A/B phase pattern	Inverters/Buffers	
A_1 & A_2	One-way	Without pattern	Inverters only	Fig.7-1
B_1 & B_{10}	Two-way	Without pattern	Inverters only	Fig.7-5
B_2 & B_{20}	Two-way	Without pattern	Inverters only	Fig.7-5
C_1 & C_{10}	Two-way	Pattern A	Inverters only	Fig.7-5
C_2 & C_{20}	Two-way	Pattern B	Inverters only	Fig.7-5
D_1 & D_{10}	Two-way	Pattern A	Inverters/Buffers	Fig.7-7
D_2 & D_{20}	Two-way	Pattern B	Inverters/Buffers	Fig.7-7
Note	For cases B_{10} and B_{20}, C_{10} and C_{20}, D_{10} and D_{20}, one direction is active, while the opposite direction is quiet.			

Numerical simulation with Agilent Technologies ADS has been used to demonstrate our method. It should be noted that propagation delays depend on many factors such as neighbour wires, size, type and topology of repeaters, values and topology of embedded decoupling capacitances, and so on. The reported results reflect the case where there is enough embedded decoupling capacitance near every group of repeaters. That is to say, the decoupling capacitance maintains small variation (such as 1%) of the voltage difference between power and ground lines near each group of repeaters. The design of decoupling is beyond the scope of this thesis. Thus, we can temporarily neglect the

impact of power distribution network and focus on the impact of neighbour wires and repeaters. Here, the repeaters are constructed by CMOS 0.8 μm technology available within the Agilent Technologies ADS software package. However, our method is general and can be applied to other deep sub-micron technologies such as 0.35 μm and 0.18 μm by considering scaling effects for high performance and low power [1].

In the following, we first compare signals propagating in one and two directions. Then, for the signals traveling in the two directions, we compare the propagation time skew with and without a zigzag phase pattern. Finally, we compare the difference of the propagation time skew between the layouts with inverters only and with both inverters and buffers.

7.4.1 Cases A_1 and A_2

These cases were already in Section 7.2 and the waveforms are given in Figures 7.4a and 7.4b. Cases A_1 and A_2 refer to a bundle of interconnects propagating in one direction with inverters only as shown in Figure 7.1. For cases both A_1 and A_2, all the signals $\{D_0D_1D_2D_3D_4D_5D_6D_7\}$ travel in the same direction.

Case A_1 approximates the situation of one signal with the shortest propagation time delay, where all the signals $\{D_0D_1D_2D_3D_4D_5D_6D_7\}$ switch simultaneously. Case A_2 approximates the situation of one signal with the longest propagation time delay, where all the signals $\{D_0D_1D_2D_3D_5D_6D_7\}$ except signal D_4 switch simultaneously. Signal D_4 propagates with a delay of 3.15 ns.

The results were presented before and they have been included in Table 7.4 for the sake of comparison.

Table 7.4: Propagation time delays for different cases

Types	Cases	Min (ns)	Max (ns)	Difference (ns)
A	A_1	1.238	1.513	2.216
	A_2	1.400	3.364	
B	B_1	2.308	2.446	0.295
	B_2	2.278	2.573	
	B_{10}	2.067	2.149	0.249
	B_{20}	2.164	2.316	
C	C_1	2.277	2.605	0.328
	C_2	2.405	2.529	0.124
	C_{10}	2.254	2.274	0.020
	C_{20}	2.280	2.296	0.016
D	D_1	2.502	2.605	0.103
	D_2	2.533	2.808	0.275
	D_{10}	2.414	2.432	0.018
	D_{20}	2.430	2.446	0.016

7.4.2 Cases B_1 and B_{10}, and B_2 and B_{20}

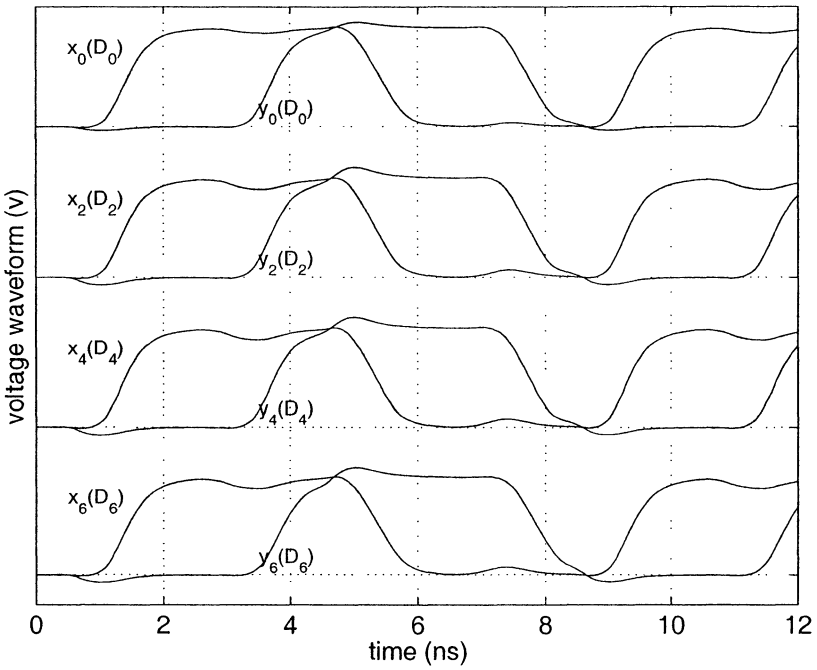
Cases B_1 and B_{10}, B_2 and B_{20} refer to a bundle of interconnects propagating signals in two directions with inverters only, as shown in Figure 7.5. Signals $\{D_0D_2D_4D_6\}$ propagate in one direction and signals $\{D_1D_3D_5D_7\}$ in the opposite direction.

Cases B_1 and B_{10} approximate the situation of one signal with the shortest propagation time delay. For case B_1, both the signals $\{D_0D_2D_4D_6\}$ and $\{D_1D_3D_5D_7\}$ switch simultaneously. For case B_{10}, all the signals $\{D_0D_2D_4D_6\}$ in one direction switch simultaneously, while all the signals $\{D_1D_3D_5D_7\}$ in the opposite direction are quiet.

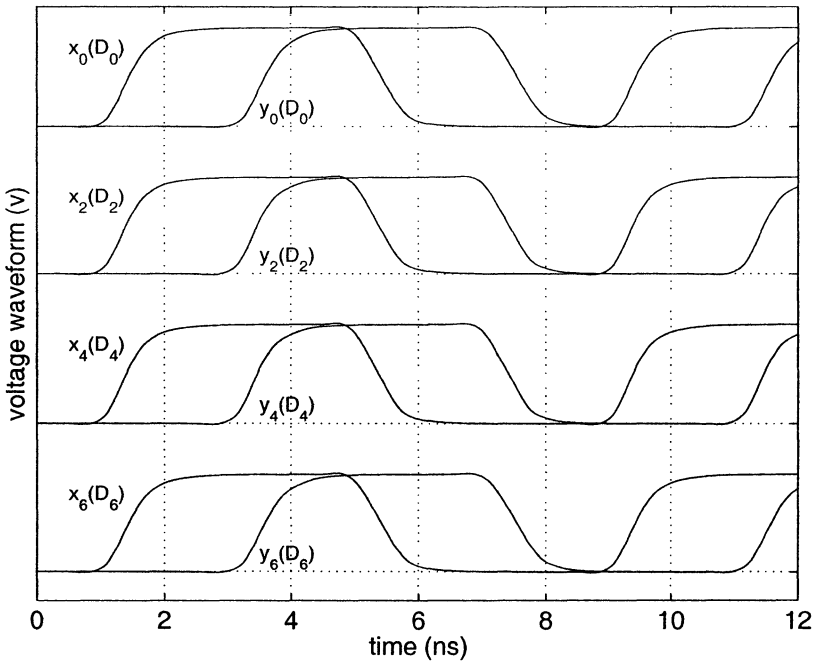
Cases B_2 and B_{20} approximate the situation of one signal with the longest propagation time delay. For case B_2, all the signals $\{D_0D_2D_6\}$ and $\{D_1D_3D_7\}$ switch simultaneously while signals $\{D_4D_5\}$ propagate with a delay of 3.15 ns. For case B_{20}, all the signals $\{D_0D_2D_6\}$ in one direction switch simultaneously, while signal D_4 is injected with a delay of 3.15 ns, and all the signals $\{D_1D_3D_5D_7\}$ in the opposite direction are quiet.

The waveforms of interest are displayed in Figures 7.8a, 7.8b, 7.9a and 7.9b. According to Figures 7.8a and 7.9a, the maximum difference of propagation time delay among 4 signals $\{D_0D_2D_4D_6\}$ is about 0.295 ns for cases B_1 and B_2. Figures 7.8b and 7.9b show that the propagation time skew reduces to 0.249 ns when the opposite signals $\{D_1D_3D_5D_7\}$ are quiet.

Compared to the simulated results for cases A_1 and A_2 as listed in Table 7.4, signals propagating in two directions dramatically reduce the propagation time skew from 2.216 ns to 0.295 ns. By keeping signals in one direction quiet, the propagation time skew in the other direction can be slightly reduced from 0.295 ns to 0.249 ns. The large difference between the skew for cases A_1 and A_2, and the one for cases B_1 and B_2 comes from the increased distance between the active wires. The small difference between the skew for B_1 and B_2 and the one for B_{10} and B_{20} confirms our hypothesis that active wires could be close neighbors if they carry signals in opposite directions. This means that such interconnect topologies could lead to savings of about 50% on the whole width of interconnect bundles, assuming that skew of 0.295 ns is acceptable.

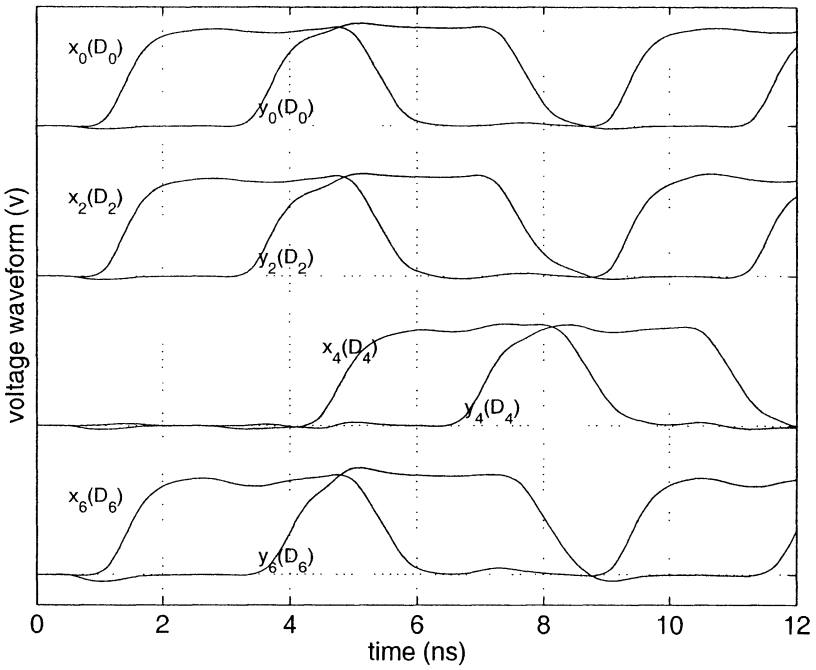


(a) Case B_1: switch simultaneously (2 directions active)

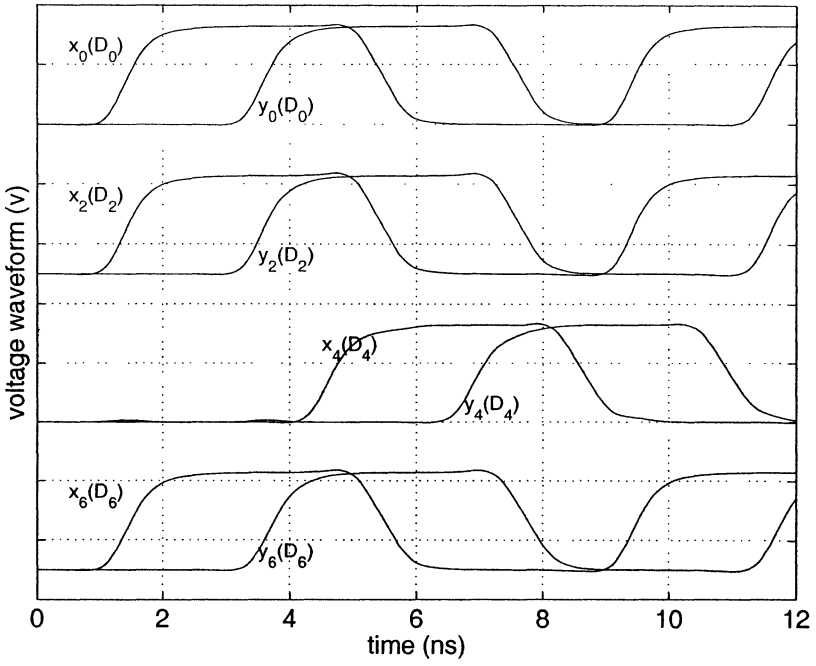


(b) Case B_{10}: Switch simultaneously (1 direction active and 1 direction quiet)

Figure 7.8 Propagation time skew analysis for "8+2" structure with inverters only (fast cases, 8 signals propagating in two directions)



(a) Case B_2: t_{d3}=t_{d4}=3.15 ns and t_{di}=0 ns (i=0,1,2,5,6,7) (2 direction actives)



(b) Case B_{20}: t_{d4}=3.15 ns and t_{di}=0 ns (i=0,2,6)
(1 direction active and 1 direction quiet)

Figure 7.9: Propagation time skew analysis for "8+2" structure with inverters only (slow cases, 8 signals propagating in two directions)

7.4.3 Cases C_1 and C_{10}, and C_2 and C_{20}

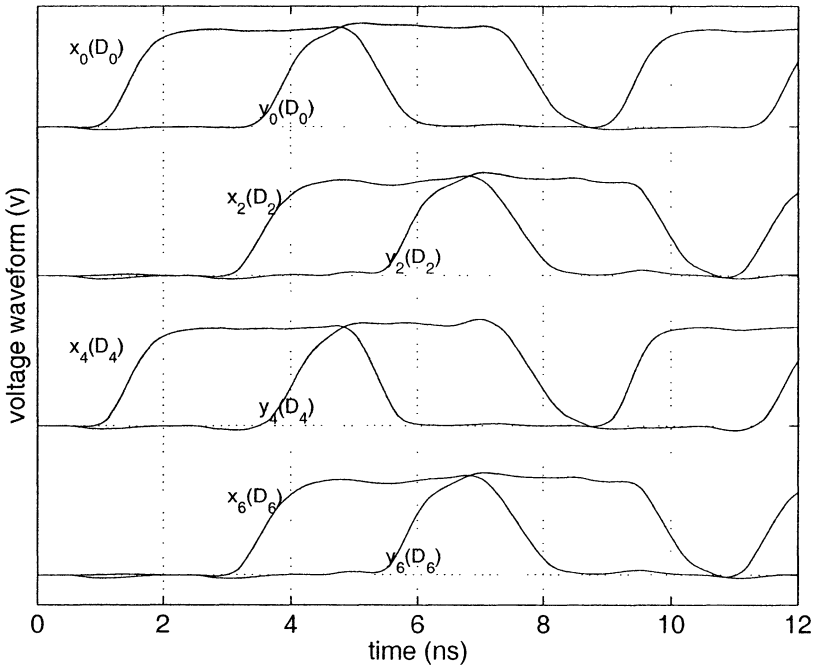
Cases C_1 and C_{10}, and C_2 and C_{20}, refer to a bundle of interconnects propagating in two directions with inverters only as shown in Figure 7.5. Signals $\{D_0D_2D_4D_6\}$ propagate in one direction, and signals $\{D_1D_3D_5D_7\}$ propagate in the opposite direction.

For case C_1, zigzag phase pattern A, as shown in Figure 7.6a, is implemented on all the signals $\{D_0D_2D_4D_6\}$ and $\{D_1D_3D_5D_7\}$. For case C_{10}, zigzag phase pattern A is implemented on signals $\{D_0D_2D_4D_6\}$ in one direction, while all the other signals $\{D_1D_3D_5D_7\}$ in the opposite direction are quiet.

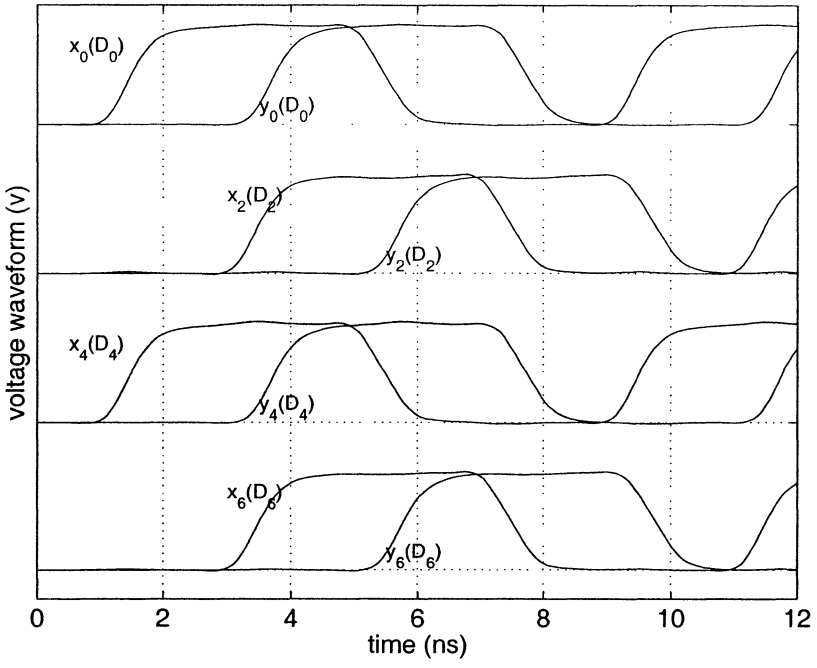
For cases C_2, zigzag phase pattern B, as shown in Figure 7.6b is implemented on all the signals $\{D_0D_2D_4D_6\}$ and $\{D_1D_3D_5D_7\}$. For case C_{20}, zigzag phase pattern B is implemented on signals $\{D_0D_2D_4D_6\}$ in one direction, while all the signals $\{D_1D_3D_5D_7\}$ in the opposite direction are quiet.

Figures 7.10a and 7.10b show the voltage waveforms of signals $\{D_0D_2D_4D_6\}$ after four segments propagation for cases C_1 and C_{10}, respectively. Figures 7.11a and 7.11b show the voltage waveforms of signals $\{D_0D_2D_4D_6\}$ after four segments propagation for cases C_2 and C_{20}, respectively. The simulation results are summarized in Table 7.4.

According to Figures 7.10a and 7.11a, the difference of propagation time delay among 4 signals $\{D_0D_2D_4D_6\}$ is about 0.328 ns and 0.124 ns, for patterns A and B, respectively. Figures 7.11b and 7.12b show that the difference of propagation time delays among 4 signals $\{D_0D_2D_4D_6\}$ reduces to 0.020 ns and 0.016 ns, for patterns A and B, respectively, as the opposite direction signals $\{D_1D_3D_5D_7\}$ are quiet.

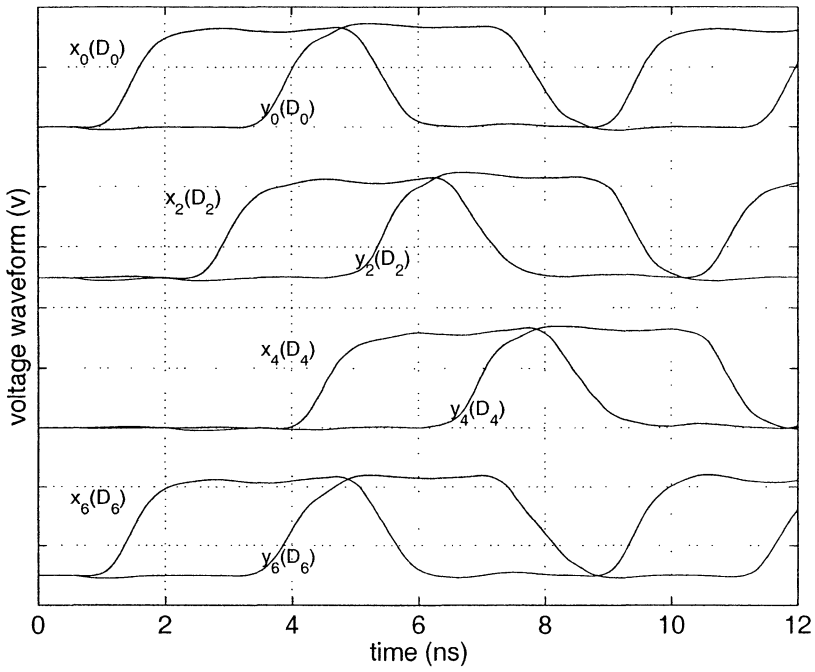


(a) Case C_1: Phase pattern A (2 directions active)

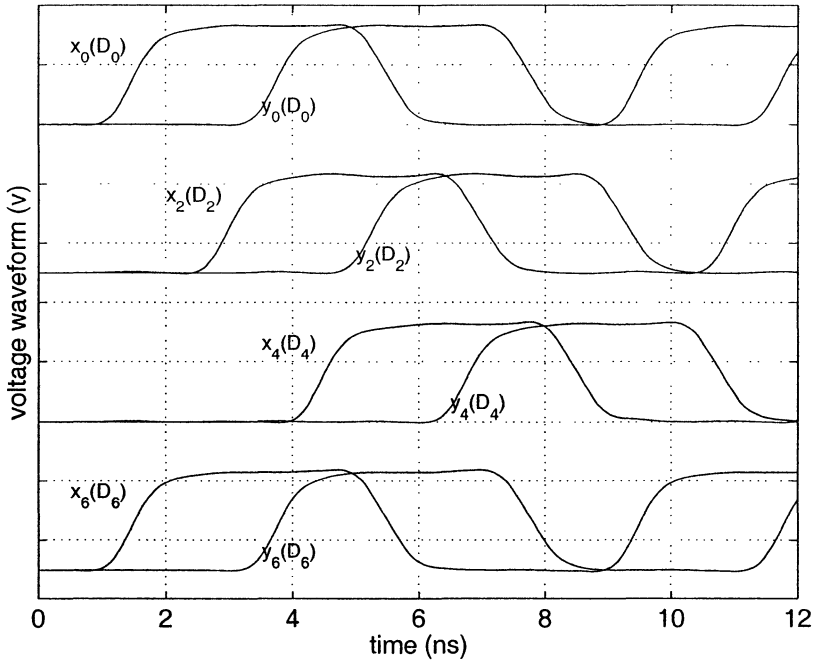


(b) Case C_{10}: Phase pattern A (1 direction active and 1direction quiet)

Figure 7.10 Propagation time skew analysis for "8+2" structure with inverters only (8 signals propagate in two directions and switch in phase pattern A)



(a) Case C_2: Phase pattern B (2 directions active)



(b) Case C_{20}: Phase pattern B (1 direction active and 1 direction quiet)

Figure 7.11 Propagation time skew analysis for "8+2" structure with inverters only (8 signals propagate in two directions and switch in phase pattern B)

Compared to the simulated results for cases B_1 and B_2, as listed in Table 7.4, the propagation time skew of 0.328 ns for pattern A is very close to the value of 0.295 ns in cases B_1 and B_2, while the propagation time skew 0.124 ns for pattern B is about half of the value of 0.295 ns in cases B_1 and B_2. As the opposite signals are quiet, the propagation time skew dramatically reduces to about 0.020ns for both patterns A and B compared to 0.249 ns for cases B10 and B20. Clearly, spatially modulated phasing is very effective, and it is only implemented for the signals traveling in one direction.

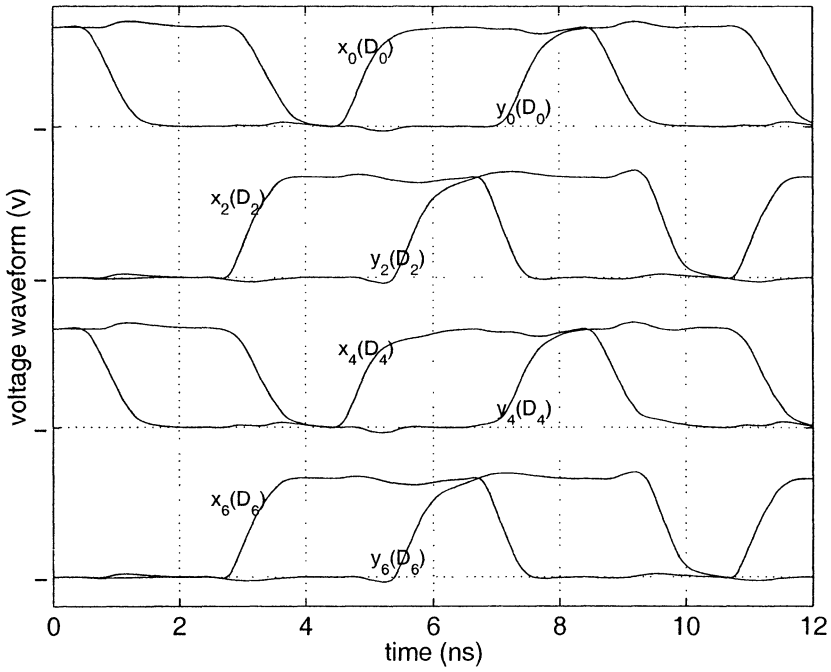
7.4.4 Cases D_1 and D_{10}, and D_2 and D_{20}

Case D refers to a bundle of interconnects propagating in two directions with both buffers and inverters, as shown in Figure 7.7. Signals $\{D_0D_2D_4D_6\}$ propagate in one direction and signals $\{D_1D_3D_5D_7\}$ in the opposite direction.

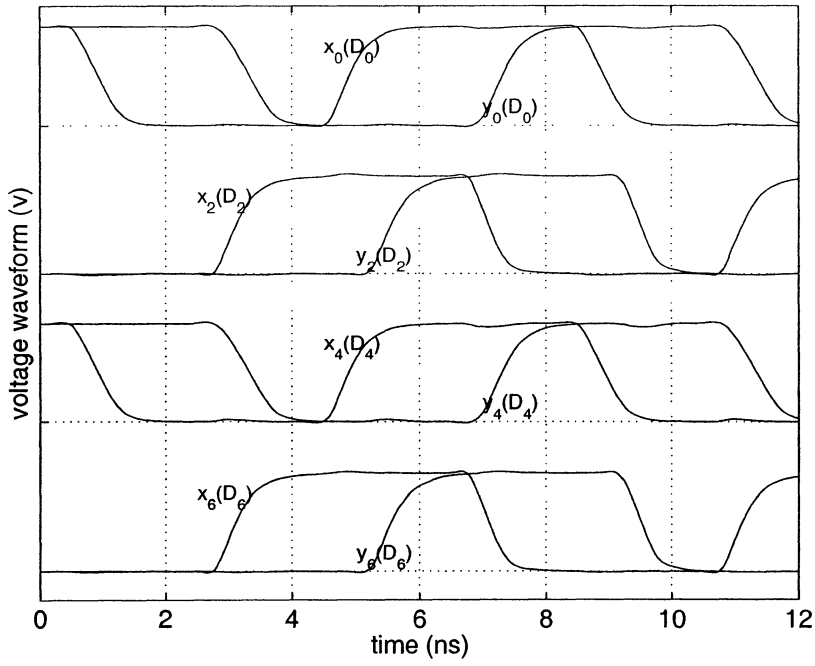
For case D_1, zigzag phase pattern A is implemented on all the signals $\{D_0D_2D_4D_6\}$ and $\{D_1D_3D_5D_7\}$. For case D_{10}, zigzag phase pattern A is implemented on signals $\{D_0D_2D_4D_6\}$ in one direction, while all the other signals $\{D_1D_3D_5D_7\}$ in the opposite direction are quiet.

For cases D_2, zigzag phase pattern B is implemented on all the signals $\{D_0D_2D_4D_6\}$ and $\{D_1D_3D_5D_7\}$. For case D_{20}, zigzag phase pattern B is implemented on the signals $\{D_0D_2D_4D_6\}$ in one direction, while all the signals $\{D_1D_3D_5D_7\}$ in the opposite direction are quiet.

Figures 7.12a and 7.12b show the voltage waveforms of signals $\{D_0D_2D_4D_6\}$ after four segments propagation for cases D_1 and D_{10}, respectively. Figures 7.13a and 7.13b show the voltage waveforms of signals $\{D_0D_2D_4D_6\}$ after four segments propagation for cases D_2 and D_{20}, respectively. The summary of the simulation results is given in Table 7.4.

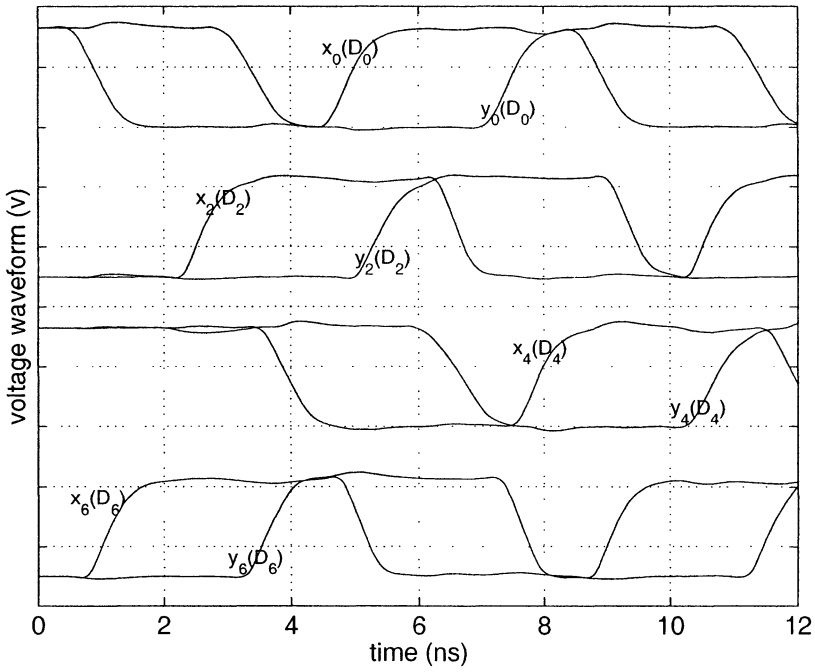


(a) Phase pattern A (2 directions active)

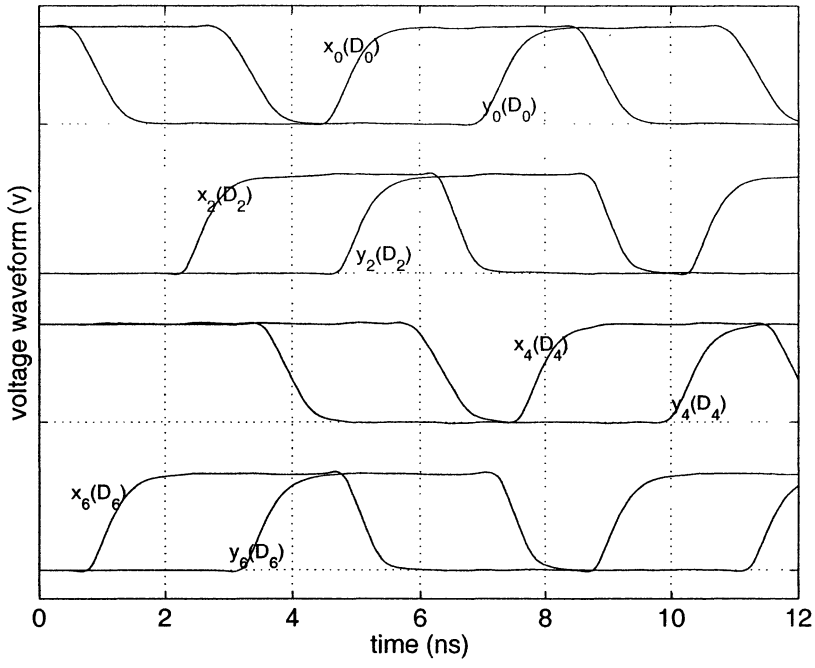


(b) Phase pattern A (1 direction active and 1 direction quiet)

Figure 7.12: Propagation time skew analysis for "8+2" structure with both inverters and buffers
(8 signals propagate in two directions and switch in phase pattern A)



(c) Phase pattern B (2 directions active)



(d) Phase pattern B (1 direction active and 1 direction quiet)

Figure 7.13: Propagation time skew analysis for "8+2" structure with both inverters and buffers
(8 signals propagate in two directions and switch in phase pattern B)

According to Figures 7.12a and 13a, the difference of propagation time delay among 4 signals $\{D_0D_2D_4D_6\}$ is about 0.103 ns and 0.275 ns for pattern A and B, respectively. Figures 7.12b and 7.13b show that the difference of propagation time delay among 4 signals $\{D_0D_2D_4D_6\}$ reduces to 0.018 ns and 0.016 ns for pattern A and B, respectively, when the opposite direction signals $\{D_1D_3D_5D_7\}$ are quiet.

Compared to the simulated results for cases B_1 and B_2, as listed in Table 7.4, the propagation time skew of 0.103 ns for pattern A is about one-third of the value of 0.295 ns in cases B_1 and B_2, while the propagation time skew 0.275 ns for pattern B is about the same as the value of 0.295 ns in cases B_1 and B_2.

Compared to the simulated results for case C_1, as listed in Table 7.4, the propagation time skew of 0.103 ns for pattern A is much smaller than the value of 0.328 ns in case C_1. However, the propagation time skew 0.275 ns for pattern B is much larger than the value of 0.124 ns in case C_2. That is to say, the propagation time skew reduces by 0.021 ns from case C_2 to D_1. Therefore, alternatively using inverters and buffers as repeaters can further minimize the propagation time skew. However, the disadvantage of such method is that it takes more area and may consume more power compared to the method using inverters only.

7.5 Conclusions

In this chapter, we proposed a new combined method to reduce propagation time skew. There are three features in our method:

- Use alternative propagation directions for parallel signals to reduce the electromagnetic interference (EMI) intervals among neighbour wires;
- A zigzag phase pattern implementation for the same direction signals to further reduce the crosstalk among neighbour wires;
- Alternatively use buffers and inverters as repeaters to compensate the impact of

dual-polarity crosstalk on the propagation time delay uncertainty.

In practice, we first recommend implementing the method of inverters only to reduce the propagation time skew. If it is still larger than tolerated, then we can implement alternative use of both buffers and inverters as repeaters to reduce the impact of the coupling effect on the propagation time delay uncertainty. As mentioned above, the sizes of buffers and inverters should be carefully adjusted to minimize the variation of propagation time skew due to the different characteristics of buffers and inverters.

CHAPTER 8

CONCLUSIONS

There are several contributions in this thesis that relate to a method of estimating time-domain model-induced simulation error, to modeling of interconnects in the MIS configuration, and to signal integrity analysis in VLSI and WSI circuits.

8.1 Method of estimating time-domain model-induced simulation error

In this thesis, a novel method was presented to estimate the time-domain model-induced simulation error using frequency domain circuit parameters. Such method was based on the spectrum of voltage source and based on the difference of the voltage transfer functions between a model and a reference. In order to illustrate this method, a simple RC transmission line net was used with source resistance R_S and load capacitance C_L. It was demonstrated that the model-induced error produced by our proposed method is prone to be an upper limit for the time-domain simulation error obtained from Agilent Technologies ADS simulator. Here, the voltage transfer functions above can be obtained from the renormalized S-parameters, because a strong relationship exists between the voltage transfer function and the renormalized S-parameters. The relationship was derived by using a simple two-port network: a single interconnect in the MIS configuration with source impedance Z_S and load Z_L. Three advantages to use the normalized/renormalized S-parameters were also described.

8.2 Practical approach of modeling a single MIS interconnect

By implementing the new method, a practical approach was presented to model a single MIS interconnect in VLSI circuits. Three steps were taken in this approach. At first, based on the literature, an original RLCG-B model with five equivalent circuit

parameters was constructed for a single MIS interconnect. Here, two equivalent widths were proposed for the physical metal strip. These widths reflect the field spread for the insulator and semiconductor layers, respectively. The original RLCG-B model extended the validity range of some closed-form expressions from 1D to 2D, and was validated by numerical simulations for the highest frequency up to 10 GHz and for substrate resistivities higher than 1 Ω·cm.

Secondly, the original RLCG-B model was revised for the purpose of embedding simple equivalent circuit models into simulation software such as SPICE. The model was called a modified RLCG-B model. Two frequency-dependent circuit parameters related to the series impedance in the original RLCG-B model were replaced by a RL sub-network specified by four frequency-invariant circuit parameters in the modified RLCG-B model. The values of the four new circuit parameters were directly derived from analytical expressions, which were proposed in this thesis. Numerical simulations demonstrated that the difference of series impedance per unit length between the modified and the original RLCG-B models is small and can be negligible for the frequency and resistivity ranges of interest mentioned above.

Finally, some simplifications were performed for the modified RLCG-B model in order to obtain an efficient model, because the modified model is accurate, however, it is time and memory consuming. Regarding the modified RLCG-B model as a reference, five simplified models were analyzed in this thesis by either neglecting the skin effect in metal strip, or the dielectric losses in the semiconductor layer, or by treating the semiconductor layer as a perfect conductor for the electric field. Using the method proposed in this thesis, the model-induced simulation error for those five simplified models was estimated by including the conditions on the source and load. Combining the spectrum of a voltage source with the differences of voltage transfer functions between the simplified models and the reference, the absolute differences of load voltages between the simplified models and the reference were obtained. Using the same

interconnect as mentioned above with typical source and load, it was demonstrated that the time-domain model-induced error was small when we neglect the skin effect in the metal strip, but the error was large when we neglect the dielectric losses. It was interesting to find that the model-induced error was at an acceptable level if the semiconductor layer was treated as a perfect conductor for the electric field. Thus, given an error tolerance, an efficient model can be determined to model a single interconnect with source resistance and load. Here, the contributions to the total model-induced time-domain error between a model and a reference from different frequency sub-regions were also studied by dividing the whole frequency range of interest into three frequency sub-regions: inside (Region I), near (Region II), and far away (Region III) from the bandwidth of the load voltage, respectively. Here, the bandwidth of the load voltage depends on both the bandwidth of the voltage source and that of the system. Different equations were used to estimate the bandwidth of the system for RC and RLC wires. For the specific example above, it was demonstrated that the modeling accuracy has great impact on the simulation error in Regions I and II, where most of the energy is concentrated, except that the contribution to the total simulation error in Regions III is large when the estimated time-domain simulation-error is near the noise level.

In our practical approach to model a single interconnect in the MIS configuration, a newly normalized γ_n-plane was defined in order to elucidate the difference of propagation characteristics between simplified model and a reference, where the whole frequency range from DC to the highest frequency of interest could be mapped-out by a curve. Therefore, by comparing the curve of a simplified model with the one of a reference in the normalized γ_n-plane, we can assess the differences of magnitude attenuation and phase delay between the model and the reference as signals travel through the interconnect. Here, we assumed that the source impedance and the load were both equal to the characteristic impedance of the wire.

8.3 Comparison between single and coupled MIS interconnects

Besides modeling of a single MIS interconnect, for comparison, a topology of two coupled interconnects in the MIS configuration was also investigated in this thesis, where one of the two coupled interconnects is used as a current returning path. Based on the original RLCG-B model for a single interconnect and other models in the literature, a hybrid RLCG-B model was first constructed for the odd-mode of two coupled interconnects. This hybrid RLCG-B model was then evolved into a simple RLC model by assuming the semiconductor as a perfect conductor. The valid condition of the simple RLC model was outlined, by comparing the complex propagation constant of the simple RLC model with the result predicted by Agilent Technologies ADS Momentum. For the special cases discusses in this chapter, it is demonstrated that the simple RLC model (simple two-wire model) captures the electrical behavior of two coupled interconnects well as the wire spacing s_m is comparable to the line width w_m. It seems that there exists a threshold value of s_m/w_m. Under the threshold, a tight coupling exists between the two interconnects and the simple two-wire model works well, because the terms in modeling related to the semiconductor losses are dominated by the coupling terms for two tightly coupled interconnects. Above the threshold, a loose coupling is expected for the two interconnects and the simple two-wire model fails. This is due to the simplification by which the bulk semiconductor is treated as a perfect conductor and its ohmic losses are neglected in the simple two-wire model. It was found that for 300 μm thick Si wafer with 0.8 μm technology and with a line width of 3 μm, the typical threshold value of s_m/w_m is 8, which corresponds to the wire spacing between two interconnects being less than 25 μm.

By comparing the propagation characteristics between single and coupled MIS interconnect topologies in VLSI circuits, we illustrate that a one-wire model, originally for a single MIS interconnect, captures the electrical behavior of two coupled MIS interconnects well when there is weak coupling between the two interconnects. As

expected, the one-wire model excluding the whole coupling fails for the two interconnects with strong coupling. Similar to the simple two-wire model, a threshold value of s_m/w_m is used to determine if the one-wire model can be properly used to model the two coupled interconnects.

Based on numerical results, the valid range of the one-wire model seems to be overlapped by that of the simple two-wire model and a validity interval of s_m/w_m can be shared by models. Thus, it is possible to construct an efficient model for two coupled interconnects. This efficient model can be either a one-wire model or a simple two-wire model. A threshold value of s_m/w_m is proposed to determine if the one-wire model or the simple two-wire is sufficient to model the two coupled interconnects.

8.4 Propagation time delay analysis

In this thesis, there are two issues on signal integrity. One issue is the propagation time delay for RC wires with source impedance R_S and load capacitance C_L in VLSI circuits. We studied the validity conditions for modeling a wire with RC sections. Because of the monotonic step-response for an RC-class wire, it is possible to analyze time delay simply without considering other signal integrity issues. Here, a limited number of AWE poles were selected for time delay analysis on RC wires to avoid numerical instability, though it may lead to inaccuracy for complicated circuits. The accuracy of lumped models with the number of sections was mapped in a normalized r-c plane, which was valid for different technologies. Using the information provided in this thesis, a user can select a model of minimal complexity that meets the accuracy requirements of a given approximation. In some cases, the basic cell structure (T- or π-) has a significant impact on accuracy for a given model complexity, and this thesis allows selecting the most efficient model.

The essential number of T- or - or π- sections for RC wires was also illustrated with the bandwidth of the load voltage. For a step voltage source, the bandwidth of the load voltage will only be determined by the bandwidth of the system, which can be estimated by the propagation time delay. Thus, given a specific RC wire, the bandwidth of load voltage with a strong driver and a light load (the front case), is wider than that of load voltage with a weak driver and a heavy load (the rear case). Thus, the modeling accuracy of a distributed RC wire has more impact on the time-domain model-induced simulation error for the front case, and more T- or π- sections are needed for RC wires for that case.

8.5 Propagation time skew analysis

The other issue on signal integrity studied in this thesis is the propagation time skew analysis. In this thesis, we proposed a new combined method to reduce propagation time skew. There were three features in our method. Alternative propagation directions were used for parallel signals to reduce the electromagnetic interference (EMI) among neighbour wires. A zigzag phase pattern implementation for the same direction signals was implemented to further reduce the crosstalk among neighbour wires. Alternatively, buffers and inverters used as repeaters were inserted in each interconnect to compensate the impact of dual-polarity crosstalk on the propagation time delay uncertainty. For practical applications, we first recommend using the method of inverters only to reduce the propagation time skew. If the time skew is still larger than tolerated, then we select alternative usage of both buffers and inverters as repeaters to reduce the impact of the coupling effect on the propagation time delay uncertainty. As mentioned above, the sizes of buffers and inverters should be carefully adjusted to minimize the variation of propagation time skew due to the different characteristics of buffers and inverters.

8.5 Suggestions for future work

Based on this thesis, several works are recommended for the future. For the method proposed in Chapter 3, we provided an upper limit for the time-domain model-induced simulation error. More research can be done to prove if this upper limit is really a bound for the time-domain simulation error and how tight this bound is.

For the modeling of interconnects, we have presented a single interconnect model applicable to low loss semiconductor layers and frequencies of interest up to 10GHz. More research can be done for other situations such as high loss semiconductors and operating frequencies higher than 10 GHz, where the TM_0 mode is no longer the fundamental mode and where the skin depth of the semiconductor layer is comparable or less than the thickness of the semiconductor layer. Thus, the semiconductor functions as a poor conductor causing dramatic increase of the series resistance and decrease of the series inductance. For coupled interconnects, more research should be done to construct a general model for a given error tolerance, though some of the circuit parameters for the odd-mode and even-mode are different. Thus, an effective and efficient model can be developed for the coupled interconnects so that complicated signal integrity issues in VLSI and WSI circuits can be analyzed.

In this thesis, we mentioned the need of decoupling capacitances on-chip and on-wafer. More work can be done to determine how much is enough and how to layout these decoupling capacitances. The same is true for the power supply network, where both lumped and distributed decoupling capacitances may be introduced.

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APPENDIX A

ELMORE DELAY MODEL

The Elmore delay model [70] is one of the most commonly used delay models on interconnect design and is originally applied to an RC tree. Rubinstein *et al.* [71] defined an RC tree as below: (i) a lumped capacitor between ground and another node is a RC tree, (ii) a lumped resistor between two nonground nodes is an RC tree, (iii) a RC line with no DC path to ground is an RC tree, and (iv) any two RC trees (with common ground) connected together to a nonground node is an RC tree. For example, Figure A-1 shows an RC tree with input node n_a, middle node n_b, and output node n_c.

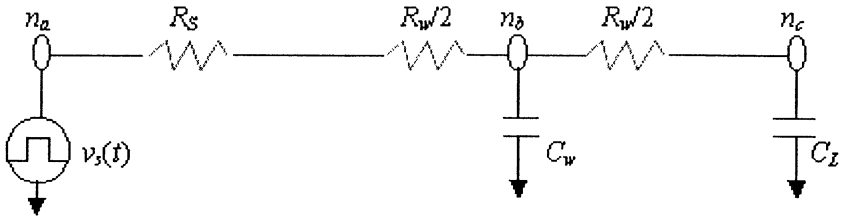

Figure A.1 An RC tree

Under the Elmore delay model, the signal delay from input node n_a to output node n_c in an RC tree is originally given by equation (4) in [71]. For the purpose of easily understanding, we rewrite that equation (4) as

$$t(n_a,n_c)=\sum_{\text{all the nodes } k}(R_{n_a,n_c}\cap R_{n_a,k})C_k \qquad \text{(A-1)}$$

Here, we define C_k as the capacitor at node k, and $R_{n_a,k}$ as the path resistance between input node n_a and node k, respectively. The common part resistance shared by two path resistances R_{n_a,n_b} and R_{n_a,n_c} is represented by $(R_{n_a,n_b}\cap R_{n_a,n_c})$ as shown on the right side of Eq.A-1.

For the RC network shown in Figure A-1, R_{n_a,n_b} is R_s+R_w/2, R_{n_a,n_c} is R_s+R_w, and $\left(R_{n_a,n_b} \cap R_{n_a,n_c}\right)$ is R_s+R_w/2. From Eq.A-1, we obtain

$$t(n_a, n_c) = (R_s + R_w/2)C_w + (R_s + R_w)C_L \tag{A-2}$$

Here, $t(n_a, n_c)$ is called "delay" by Elmore [70] and is represented by τ_{ED} in this thesis. Rubinstein *et al.* [71] has proved that Elmore delay τ_{ED} is equal to the first-order time-moment of the impulse response $h(t)$. That is, if the voltage transfer function $H(s)$ from input node to output node is

$$H(s) = \frac{1 + b_1 s + b_2 s^2 + \ldots}{1 + a_1 s + a_2 s^2 + \ldots} \tag{A-3}$$

then τ_{ED} is equal to the first-order time-moment of the impulse response $h(t)$.

$$\tau_{ED} = \int_0^\infty t\, h(t)\, dt = a_1 - b_1 \tag{A-4}$$

Moreover, if the voltage transfer function $H(s)$ is expanded using Maclaurin series in powers of s [25]

$$H(s) = \frac{1 + b_1 s + b_2 s^2 + \ldots}{1 + a_1 s + a_2 s^2 + \ldots} = m_0 + m_1 s + m_2 s^2 + \ldots \tag{A-5}$$

It is found that

$$m_0 = 1 \tag{A-6}$$

and $$m_1 = b_1 - a_1 \tag{A-7}$$

Comparing the above equation with Eq.A-4, we see that Elmore delay τ_{ED} is just the first moment term m_1 with a difference of sign "-" as illustrated in [29].

APPENDIX B

ASYMPTOTIC WAVEFORM EVALUATION (AWE) METHOD

AWE [22] is a generalized approach to approximate the waveform response of linear circuits. At first, moment terms of an impulse response from input node to output node are calculated. Then, these moment terms are used to find a reduced-order rational polynomial. Finally, the impulse response can be evaluated with the poles and residues of the reduced-order rational polynomial.

B1. Calculation of moment terms

For a simple network with only lumped models, the modified nodal admittance (MNA) [87] matrix in Laplace domain is G+sC. Here, G and C both are matrices. For an impulse input excitation, such network can be represented in the form as

$$[G+sC][X(s)]=[E] \tag{B-1}$$

where, $X(s)$ and E are impulse response vector and impulse excitation vector, respectively. Now, let us expand the impulse response vector $X(s)$ using Maclaurin series in powers of s

$$X(s)=M_0+M_1s+M_2s^2+...+M_ns^n=\sum_{i=0}^{n}M_is^n \tag{B-2}$$

where M_i are moment vectors. Combining Eqs.B-1 with B-2, we get

$$[G+sC]\left[M_0+M_1s+M_2s^2+...\right]=[E] \tag{B-3}$$

Equating powers of s on both sides of Eq.B-3, we obtain the following relationships

$$GM_0=E \tag{B-4}$$

and $$GM_i=-CM_{i-1} \qquad for\ i\geq 1 \tag{B-5}$$

From Eqs.B-4 and B-5, we then derive the moment vectors M_i

$$M_0 = G^{-1}E \tag{B-6}$$

and $$M_i = -G^{-1}CM_{i-1} \qquad for\ i \geq 1 \tag{B-7}$$

Once the moment vectors M_i are known, we can obtain the impulse response at node k, $H_k(s)$, by collecting the k^{th} terms in the M_i vectors. That is,

$$H_k(s) = m_0 + m_1 s + m_2 s^2 + \ldots + m_n s^n = \sum_{i=0}^{n} m_i s^n \tag{B-8}$$

where m_i are the k^{th} moment terms.

B2. Reduced-order rational polynomial

By using the above moment terms m_i, the impulse response H_k(s) can be approximated by a reduced-order rational polynomial $\hat{H}_k(s)$ as

$$\hat{H}_k(s) = \frac{b_0 + b_1 s + b_2 s^2 + \ldots + b_L s^L}{1 + a_1 s + a_2 s^2 + \ldots + a_M s^M} \tag{B-9}$$

In this step, we will compute the unknown coefficients a_1, a_2, …, a_M, b_0, b_1, b_2, …, b_L, which in total make L+M unknown variables.

Combining Eqs.B-8 with B-9, we have

$$\hat{H}_k(s) \approx H_k(s) \tag{B-10}$$

The Maclaurin series in Eq.B-8 is then matched to the lower-order rational polynomial given by Eq.B-9. Since there are L+M unknowns, we require that L+M moments be matched.

$$\frac{b_0 + b_1 s + b_2 s^2 + \ldots + b_L s^L}{1 + a_1 s + a_2 s^2 + \ldots + a_M s^M} = m_0 + m_1 s + m_2 s^2 + \ldots + m_{L+M} s^{L+M} \tag{B-11}$$

Cross multiplying the above equation and equating the powers of s starting from s^{L+1} to s^{L+M} on both sides, we can evaluate the denominator polynomial coefficients as shown below

$$\begin{bmatrix} m_{L-M+1} & m_{L-M+2} & \cdots & m_L \\ m_{L-M+2} & \cdots & \cdots & m_{L+1} \\ \cdots & \cdots & \cdots & \cdots \\ m_L & m_{L+1} & \cdots & m_{L+M-1} \end{bmatrix} \begin{bmatrix} a_M \\ a_{M-1} \\ \cdots \\ a_1 \end{bmatrix} = -\begin{bmatrix} m_{L+1} \\ m_{L+2} \\ \cdots \\ m_{L+M} \end{bmatrix} \tag{B-12}$$

The numerator coefficients can then be found by equating the remaining power of s, starting from s^0 to s^L as

$$\begin{bmatrix} b_0 \\ b_1 \\ b_2 \\ \cdots \\ b_L \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & \cdots & 0 \\ a_1 & 1 & 0 & \cdots & 0 \\ a_2 & a_1 & 1 & \cdots & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ \cdots & \cdots & \cdots & \cdots & 1 \end{bmatrix} \begin{bmatrix} m_0 \\ m_1 \\ m_2 \\ \cdots \\ m_L \end{bmatrix} \tag{B-13}$$

B3. Waveform evaluation

The above Eqs.B-12 and B-13 yield an approximate impulse response $\hat{H}_k(s)$ in terms of rational polynomial. In order to conveniently compute the approximate impulse response $\hat{h}_k(t), \hat{H}_k(s)$ can also be expressed in terms of poles and residues

$$\hat{H}_k(s) = \frac{k_1}{s-p_1} + \frac{k_2}{s-p_2} + \ldots + \frac{k_M}{s-p_M} \tag{B-14}$$

Here, the poles and residues are derived from the rational polynomial. Combining Eqs.B-14 with B-9, we have

$$\frac{b_0 + b_1 s + b_2 s^2 + \ldots + b_L s^L}{1 + a_1 s + a_2 s^2 + \ldots + a_M s^M} = \frac{k_1}{s-p_1} + \frac{k_2}{s-p_2} + \ldots + \frac{k_M}{s-p_M} \tag{B-15}$$

Then, the poles and residues are found by partial fraction expansion. If all the poles are non-equal, the approximate time-domain impulse response can be simply expressed as

$$\hat{h}_k(t) = k_1 e^{p_1 t} + k_2 e^{p_2 t} + \ldots + k_M e^{p_M t} \tag{B-16}$$