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UNIVERSITÉ DE MONTRÉAL

ÉCOLE POLYTECHNIQUE DE MONTRÉAL

LOW POWER AND HIGH SPEED ARITHMETIC CIRCUITS FOR SOFTWARE ASSISTED WIRELESS SYSTEMS

WEI LING

DÉPARTEMENT DE GÉNIE ÉLECTRIQUE

ÉCOLE POLYTECHNIQUE DE MONTRÉAL

MÉMOIRE PRÉSENTÉ EN VUE DE L'OBTENTION

DU DIPLÔME DE MAÎTRISE EN SCIENCES APPLIQUÉES

(GÉNIE ÉLECTRIQUE)

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Ce mémoire intitulé :

LOW POWER AND HIGH SPEED ARITHMETIC CIRCUITS FOR SOFTWARE ASSISTED WIRELESS SYSTEMS

Présenté par : Wei Ling

en vue de l'obtention du diplôme de : Maîtrise ès sciences appliquées

a été dûment accepté par le jury d'examen constitué de :

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M. SAVARIA Yvon, Ph.D., directeur de recherche

M. THIBEAULT Claude, Ph.D., membre

DEDICATE

I would like to dedicate this thesis to my wife and parents,

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First of all I would like to express my sincerest gratitude to my directeur de recherche Prof. Yvon Savaria, who guided me from the beginning with excellent supervision and invaluable suggestions. I would like also thanks Prof. Claude Thibeault and Prof. Hakim Khouas for providing detailed corrections. I would like to acknowledge the help from research group Multi-Equalizer and Software Defined Radio. Special thanks also go to my wife Minjie, for her continuous support as well as the love she has brought to me.

RÉSUMÉ

Il devient de plus en plus commun que les systèmes de communication ajustent leur performance, leur débit et leur puissance selon la tâche, la qualité du canal et les services à fournir. Une approche récente, appelé Software Assisted (Defined) Radio (SDR) attire énormément d'attention. Cette approche répond aux demandes d'adaptabilité et de faible consommation de puissance dans les prochaines générations de système de communication sans fil.

Dans ce mémoire, nous passerons d'abord en revue quelques architectures existantes de SDR, les techniques de modulation adaptative et les techniques de conception de système électronique à basse puissance. Ensuite, nous présentons un multiplieur de précision variable pour l'égaliseur de SDR. Ce multiplieur réduit la puissance dissipée en ajustant la largeur des mots traités selon le type de modulation. Il existe un bon choix de la longueur de mot pour l'égaliseur LMS associé à divers types de modulation. Il est avantageux de réaliser l'égaliseur LMS en utilisant une longueur de mot variable. L'économie de puissance en employant l'égaliseur LMS avec une longueur de mot variable peut atteindre 85% pour chaque multiplication.

Puis, nous présentons un multiplieur pipeliné conçu selon la structure logique Domino pour le processeur DSP. La question des variations paramétriques et leur impact sur la puissance dissipée au sein d'un multiplieur pipeliné profond conçu selon la structure Domino est également discutés. Nous trouvons que le circuit vague-Domino bloquant avec pied est plus approprié à des applications où les pipelines sont profonds. De plus, on

propose aussi une solution de porte dynamique inverseuse afin d'empêcher le problème classique de précharge des circuits Domino. Le multiplieur 9 bits vague-Domino a été conçu en technologie TSMC 0.18μm CMOS. Une économie de puissance de 40% est enregistrée en employant la porte dynamique inverseuse proposée. Le multiplieur 9 bits vague-Domino a été comparé avec du multiplieur réalisé par le circuit statique non-pipeliné. En effet, le circuit vague-Domino pipeliné élimine les courses internes qui peuvent produire des commutations multiples. Nos résultats montrent que sa consommation de puissance est inférieure à celle du multiplieur réalisé avec le circuit statique non-pipeliné.

ABSTRACT

It becomes more and more common that communication systems adjust their performance, throughput and power consumption according to workload, channel quality and service requirements. The emerging concept, ---- Software Assisted (Defined) Radio (SDR), is proposed to meet the requirements of adaptive and low power for next generation wireless communication systems.

In this thesis, we first give some reviews of SDR architectures and implementations, the adaptive features of next generation wireless communication standards, and existing popular VLSI low power design techniques. Then we will focus on a DSP building block ----- an array multiplier, which is heavily used in SDR systems.

We will study the word length implementation of a VLSI array multiplier under an adaptive modulation scheme. We will show that there exists a good choice of l word length implementation for a LMS equalizer for each modulation scheme. Increasing the word length beyond this good choice does little to improve performance. Based on this word length, a variable word length array multiplier is developed using dynamic voltage scaling and gating techniques. The simulation results demonstrate that a LMS equalizer based on a variable-precision multiplier can produce an 85% power reduction without performance and throughput penalties.

A long pipelined array multiplier using high-speed wave Domino circuit, which is suitable for implementing SDR cores, is also studied. Since the long pipelined circuit is more vulnerable to parametric variations, statistical timing relations are developed for

characterizing performance impacts of the parametric variations in different wave-pipelined Domino circuits and clocking styles. We demonstrate that the clock delayed, footed Domino circuit style is the most suitable for deeply pipelined array multipliers. In addition, an improved inverting dynamic gate solution is proposed to reduce the usage of dual-rail Domino logics in this array multiplier. A 40% power saving is achieved for a 15-stage wave pipelined array multiplier in using these improved inverting dynamic gates. Finally, the comparisons of two array multiplier implementations, one using static circuit and another using wave pipelined Domino circuit, are performed. The results show that the wave pipelined array multiplier consumes less power per operation compared to a static circuit implementation that is not pipelined.

CONDENSÉ EN FRANÇAIS

Il devient de plus en plus commun que les systèmes de communication ajustent leur performance, leur débit et leur puissance selon la tâche, la qualité du canal et les services à fournir. Une approche récente, appelé Software Assisted (Defined) Radio (SDR) attire énormément d'attention. Cette approche répond aux demandes d'adaptabilité et de faible consommation de puissance dans les prochaines générations de système de communication sans fil.

Dans ce mémoire, nous passerons d'abord en revue quelques architectures existantes de SDR, les techniques de modulation adaptative et les techniques de conception de système électronique à basse puissance. Ensuite, nous présentons un multiplieur de précision variable pour l'égaliseur de SDR. Ce multiplieur réduit la puissance dissipée en ajustant la largeur des mots traités selon le type de modulation. Puis, nous présentons un multiplieur pipeliné conçu selon la structure logique Domino pour le processeur DSP. La question des variations paramétriques et leur impact sur la puissance dissipée au sein d'un multiplieur pipeliné profond conçu selon la structure Domino est également discutés. Enfin, des comparaisons de la consommation de puissance entre l'implémentation d'un circuit en logique statique et en logique Domino multiphasée d'un multiplieur ont été effectuées.

Revue de littérature

Les architectures récemment proposées pour la mise en œuvre des systèmes SDR peuvent être divisées en 3 catégories : 1) Les systèmes SDR implémentés dans un ou plusieurs processeurs DSP; 2) Les systèmes SDR établis sur un ou plusieurs FPGA; 3) Les systèmes SDR basés simultanément sur la combinaison de processeurs DSP et de FPGA. Dans ce dernier cas, les opérations intensives en calcul et critiques dans le temps sont exécutées dans des FPGA, et le reste des opérations sont effectuées par les processeurs DSP. [34][45][84][87]

La modulation adaptative est actuellement supportée par les systèmes sans fil OFDM et TDMA et elle sera aussi disponible dans les futurs systèmes CDMA. Deux approches largement répandues pour la modulation adaptative sont l'adaptation basée sur la qualité de canal, et celle basée sur le service. [12]

Les techniques pour la conception de systèmes à faible puissance et à faible courant de fuite utilisées dans ce mémoire incluent l'emploi de tensions d'alimentation multiples, de seuils multiples et la technique d'activation sélective (gating).

Multiples Tensions d'Alimentation

Dans cette approche, différentes tensions d'alimentation sont choisies selon la tâche. Ces techniques sont notamment connues sous les vocables a) Cluster Voltage Scaling (CVS) et Dynamic Voltage Scaling (DVS). La technique de CVS divise le circuit en plusieurs zones, et applique les tensions d'alimentation les plus basses possibles sur chacune d'elles en évitant de violer les contraintes de temps. Le manque d'outils de conception supportant cette approche est un gros inconvénient. La technique de DVS permet d'ajuster dynamiquement la tension d'alimentation et la fréquence d'horloge d'un circuit

selon sa tâche. L'économie de puissance réalisée selon cette approche est énorme. Cependant, en raison de la surcharge en puissance causée par l'ajout du circuit de régulation de tension et de fréquence, l'utilisation de cette approche est limitée.[32][97][20][62][114][53][17][86][71][77][74]

Technique d'activation sélective (*Gating*)

La technique d'activation sélective permet d'identifier des périodes d'inactivité dans les sections d'un circuit, et de désactiver l'horloge ou les commutations dans ces sections aux moments appropriés.[9][10][65][80][105][90]

Technique des Seuils Multiples

Une approche populaire consiste à définir des sections du circuit où le seuil des transistors est bas, à l'aide de commutateurs à seuil élevé reliés en série. Ces zones peuvent être définies dynamiquement pendant des périodes inactives. Pendant les périodes actives, les commutateurs à seuil élevé sont mis en marche, et les circuits reprennent les opérations à grande vitesse et à seuil bas. Comme la tension de seuil est plus basse, la vitesse du circuit peut rester inchangée quand la tension d'alimentation est réduite. Une difficulté importante avec cette technique est de trouver un algorithme de détermination de la taille des commutateurs.[75][15][7][47][90]

Multiplieur de Basse Puissance pour l'Égaliseur

La partie d'un système de communication considérée dans cette section est un récepteur qui se compose d'un quantificateur, d'un égaliseur LMS (Least-Mean-Square) et d'un démodulateur adaptatif. Les données sont modulées soit en QPSK, soit en

16/64/256QAM et elles sont envoyées par un canal Gaussien entaché de Bruit Blanc additif (AWGN) sujet à des interférences inter-symbole (ISI de type A [78]). Le récepteur quantifie les données, passe ces données à l'égaliseur, puis envoie les résultats au démodulateur pour détecter les données originales.

Afin de trouver l'influence de la longueur de mot sur la performance, c.-à-d. la probabilité d'erreur de symbole (P_{ser}) du démodulateur, nous devons caractériser la sensibilité de la probabilité d'erreur de symbole en fonction de la variance du bruit, qui peut être définie comme suit:

$$Sensitivity = \frac{\partial \sigma_{noise}^2}{\partial P_{ser}} \Delta P_{ser} \cong \frac{\Delta \sigma_{noise}^2}{\Delta 10 \log P_{ser}} \times 1 \qquad (3.4)$$

$\Delta \sigma_{noise}^2$ est le changement du bruit reçu du démodulateur, $\Delta 10 \log P_{ser}$ est le changement de la probabilité d'erreur de symbole en échelle logarithmique, et $\Delta P_{ser}=1$ pour le cas où la probabilité d'erreur change de 1dB. Les courbes de sensibilité au bruit des différents types de modulation pour tous les points de P_{ser} sont tracées à la fig. 13. L'avantage d'utiliser la sensibilité au lieu d'une valeur absolue du bruit est que, nous pouvons évaluer l'effet de la longueur de mot fini sur la performance de la détection de symbole, sans considérer aucun détail de l'algorithme de modulation adaptative et les imperfections de l'égaliseur.

Le bruit à l'entrée du démodulateur est le bruit à la sortie de l'égaliseur LMS, qui peut être exprimé selon [21] comme suit:

$$\sigma_{total}^2 = J_{\min} + \frac{N\sigma_c^2}{2\mu} + (|w^*|^2 + 1)\sigma_d^2 \qquad (3.5)$$

Le première terme est l'erreur de la moyenne carrée de l'algorithme LMS de précision infinie. Le deuxième terme existe à cause de l'erreur dans le vecteur de poids quantifiés. N

est le nombre de poids quantifiés. Le troisième terme est produit par l'erreur de quantification des données en entrée. La variance introduite par la taille finie des poids est: $\sigma_c^2 = 2^{-2Bc}/12$. La longueur de mot des poids est B_c. La variance introduite par les données d'entrée est $\sigma_d^2 = 2^{-2Bd}/12$. La longueur de mot des données d'entrée est B_d. D'autre part, $|w^*|$ est le vecteur optimal de Weiner. Afin d'étudier les effets de la longueur du mot fini, nous nous sommes seulement intéressés au deuxième et troisième termes dans l'équation (3.5). La somme de ces deux termes est représentée à la fig. 14. Une méthode qui permet de choisir une longueur de mot d'un égaliseur est de s'assurer que le bruit produit par l'effet de la longueur de mot finie de l'égaliseur cause seulement un changement négligeable de P_{ser}. Nous définissons le changement négligeable de P_{ser} comme suit $\Delta \log P_{ser} = 1/10$, ce qui est tracé à l'échelle à la fig. 13. Combinant la fig. 13 et la fig. 14, nous obtenons des bons choix de la longueur de mot pour différents types de modulation (tableau 4).

La structure d'un égaliseur LMS légèrement modifié (forme directe retardée avec retiming) [8] est montrée sur la fig. 15. Les éléments de base de l'égaliseur sont des registres, des additionneurs et des multiplieurs. L'avantage d'employer cette architecture d'égaliseur est que le DVS peut être appliqué à l'égaliseur entier, ce qui réduit au minimum les coûts additionnels.

Ce mémoire propose un multiplieur signé en complément à 2 de précision variable. Le multiplieur est basé sur un multiplieur de 15-bit Baugh-Wooley (voir fig. 16). Quand ce multiplieur ne fonctionne pas en pleine précision, seulement la partie gauche inférieure

est utilisée. Les additionneurs du niveau supérieur sont ignorés et forcés à zéro. Le chemin critique de ce multiplieur est proportionnel à la longueur de mot. Par conséquent, la tension d'alimentation peut changer selon la longueur de mot, sans réduction de performance.

La consommation de puissance de notre multiplieur multiprécision (mis en application avec une technologie CMOS de 180nm) est simulée avec Spectre dans Cadence et est tracée à la fig. 17. La consommation de puissance d'un multiplieur 15 bits multi précision, quand ce dernier est utilisé comme multiplieur 15 bits, est presque identique à la consommation de puissance d'un multiplieur à précision fixe de 15 bits. La consommation de puissance de notre multiplieur 15-bit multi précision utilisé comme multiplieur de 9 bits est 18-28% plus élevée que celle d'un multiplieur à précision fixe de 9 bits. Ceci est le prix à payer pour un multiplieur multi précision. Cette consommation pourra être réduite dans des travaux futurs.

Les performances du récepteur utilisant la modulation adaptative sont représentées à la fig. 19 avec une longueur de mot différente. La puissance consommée moyenne d'un multiplieur multi précision est tracée à la fig. 20. À partir des fig. 19 et 20, nous constatons que, pour la modulation QPSK, à partir de 9 bits, la différence de P_{ser} entre l'implémentation avec une longueur de mot limitée et celle à virgule flottante de 32 bits est inférieure à 6%. L'implémentation à 15 bits ramène cette différence à seulement 3%. Cependant, la puissance consommée par l'implémentation de 11 bits est 3 fois supérieure à celle de l'implémentation de 9 bits. Par conséquent, 9 bits apparaît être le bon choix de la longueur de mot dans ce cas quand on cherche un compromis efficace entre la

puissance dissipée et la probabilité d'erreur. De même, pour la modulation 16-QAM, à partir de 11 bits, la différence de P_{ser} entre l'implémentation à précision limitée et celle à virgule flottante est inférieure à 5.6%. La consommation de puissance de l'implémentation à 13 bits est 1.6 fois plus grande que celle à 11 bits. Par conséquent, l'implémentation à 11 bits semble fournir le meilleur rapport performance/puissance consommée. Une analyse similaire pour le 64-QAM nous amène à conclure que 13 bits est un bon choix de la longueur de mot.

Multiplicateur de Type Vague-Domino (*Wave-Domino*) pour le Traitement DSP

Les circuits de type vague-Domino pipelinés (Wave-Domino pipelined), aussi appelés vague-Domino, ont été largement utilisés dans les microprocesseurs à grande vitesse. Différents types d'horloges, comme les horloges bloquantes et non-bloquantes, et différents types de circuits Domino, par exemple ceux qui comportent un pied (footed) et ceux sans pied (footless), sont proposés dans la littérature [94], [24] [85] [6] [113]. La logique sans pied (footless) est plus rapide, puisqu'elle élimine le transistor de pied. Le style de d'horloge bloquante doit assurer que l'horloge d'évaluation monte après que la dernière entrée soit stable. Dans le style d'horloge non-bloquante, l'horloge d'évaluation arrive avant les transitions de données sur le chemin critique. L'inconvénient d'une horloge non bloquante est que les entrées à chaque porte dynamique doivent monter de façon monotone.

En raison des contraintes serrées de synchronisation, ce genre de circuit dynamique est plus vulnérable aux variations paramétriques. Les variations paramétriques sont un souci croissant dans la conception de circuits de performance élevée. Les facteurs environnementaux, tels que les variations de la température et de la tension d'alimentation, et les facteurs physiques pendant la fabrication, telle que la tension de seuil et la variation géométrique, sont des sources de variations paramétriques. Dans cette section, nous établissons des modèles statistiques pour comparer l'impact des variations paramétriques de circuits vague-Domino.

Le circuit vague-Domino peut être modélisé comme à la fig. 22. Nous supposons que tous les étages dans le pipeline partagent un signal d'horloge de période T_c. La durée de la phase de précharge est T_{pc} La période de déphasage de l'étape i-1 à i est ζ_i. De plus, nous supposons que T_c, T_{pc} et ζ_i sont constant. Afin d'étudier l'impact des variations paramétriques, la période d'arrivée A_i des entrées, le temps D_i de départ du signal et le temps d'évaluation Δ_i de l'étape i sont considérés comme des variables aléatoires dont les espérances mathématiques sont $E(A_i)$, $E(D_i)$, $E(\Delta_i)$. Leurs déviations respectives dans le pire cas sont $\delta(A_i)$, $\delta(D_i)$ et $\delta(\Delta_i)$. Afin de propager un signal qui traverse les circuits Domino pipelinés avec une horloge à N phases, les contraintes suivantes doivent être respectées:

- Contrainte de séparation de précharge et de déphasage [59]:

$$T_{sep}^{i-1} \geq D_i + \zeta_i - D_{i-1} \qquad (4.2)$$

T_{sep}^{i-1} est le temps entre le départ du signal et le commencement de la prochain précharge (voir fig. 22).

- Contrainte de séparation de l'onde (wave)[59]: $\zeta_i \leq D_{i-1}^{min}$ (4.5)

Pour le circuit vague-Domino non-bloquant sans pied (footless), la période d'arrivée du signal de l'étage i dépend de la période de départ du signal de l'étage précédent. Nous avons $A_i=\max\{D_{i-1}-\zeta_i,\ T_{pc}\}$ et $A_i+\Delta_i= D_i$. Afin de réduire au minimum le retard, tous les signaux en entrée sont supposés arrivés en même temps, et le front montant de l'horloge locale devrait être conçu tel que $\zeta_i+ T_{pc}=E(D_{i-1})$. Selon les contraintes ci-dessus, la période d'horloge de ce circuit doit être choisie en tenant compte du pire cas comme :

$$T_c \geq T_{pc} + E(\Delta_i) + E(\Delta_{i+1}) + \sum_{j=1}^{i+1} \delta(\Delta_j) \tag{4.22}$$

Il est clair que la période d'horloge augmente avec l'augmentation de la profondeur du pipeline. Par conséquent, la fréquence de fonctionnement est dégradée. Le même résultat peut être appliqué au circuit vague-Domino non-bloquant avec pied.

Pour le circuit vague-Domino bloquant avec pied, le front montant de l'horloge locale arrive toujours plus tard que le départ du signal du pire cas de l'étape précédente. Donc, nous avons

$$\zeta_i + T_{pc} \geq D_{i-1}^{\max} \tag{4.28}$$

D'autre part, le temps de départ du signal est entièrement contrôlé par le front montant de l'horloge locale. Il devient $D_i=\Delta_i+T_{pc}$. Selon la relation précédente, en considérant le pire cas, la période d'horloge du circuit vague-Domino doit être choisie comme:

$$T_c \geq T_{pc} + E(\Delta_i) + E(\Delta_{i+1}) + \delta(\Delta_i) + \delta(\Delta_{i+1}) \tag{4.36}$$

Il est clair qu'aucune accumulation des variations paramétrique ne se produit ici. Par conséquent ce type de circuit est plus approprié à des applications où les pipelines sont profonds.

On propose aussi une ligne de distribution d'horloge (fig. 23). Cette ligne de distribution d'horloge élimine l'accumulation des variations paramétriques dans la distribution de l'horloge. En utilisant cette ligne de distribution d'horloge, la somme des intervalles des pires cas de déphasage dans chaque bloc doit être égale à une période d'horloge et dans ce cas:

$$\sum_{i=1}^{m} \zeta_i^{\max} = T_c \tag{4.37}$$

Un multiplieur de 9 bits (fig 30) pour le SDR utilisant les circuits vague-Domino bloquants avec pied est mis en application. La logique Domino à Simple-rail est employée pour économiser la puissance. On propose aussi une solution de porte dynamique inverseuse afin d'empêcher le problème classique de précharge (figue 33) des circuits Domino. Le circuit proposé est montré aux figures 34a et 35. Une économie de puissance de 39% est enregistrée en employant la porte dynamique inverseuse proposée dans le multiplicateur de rangée du vague-Domino de 9 bits (Table 7).

Conclusion

Il existe un bon choix de la longueur de mot pour l'égaliseur LMS associé à divers types de modulation. Il est avantageux de réaliser l'égaliseur LMS en utilisant une longueur de mot variable. L'économie de puissance en employant l'égaliseur LMS avec une longueur de mot variable peut atteindre 85% pour chaque multiplication.

Le multiplieur multiprécision proposé (15 bits) supporte les précisions qui changent de 9 à 15 bits. Le multiplieur multiprécision occupe 12% plus de surface et a une dissipation 2-28% plus élevée. Considérant l'économie de surface, comparé au cas ou on utiliserait des multiplieurs dédiés pour chaque longueur de mot, le multiplieur multiprécision est une solution très attrayante.

Le multiplieur 9 bits vague-Domino a été conçu en technologie TSMC 0.18μm CMOS. Nos résultats montrent que sa consommation de puissance est 40% inférieure à celle du multiplieur réalisé avec le circuit statique non-pipeliné. En effet, le circuit vague-Domino pipeliné élimine les courses internes qui peuvent produire des commutations multiples.

Il est plus avantageux, du point de vue puissance et flexibilité, de partager le multiplieur vague-Domino dans un microprocesseur, que de le mettre en application individuellement dans du matériel dédié.

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ABREVIATIONS

ADC	Analog to digital converter
AGC	Analog gain controller
ALU	Arithmetic logic unit
ASIC	Application specific integrated circuits
AWGN	Additive White Gaussian Noise
BER	Bit error rate
BPSK	Binary phase shift keying
CAD	Computer aid design
CDFG	Control data flow
CDMA	Code division multiple access
CLB	Configurable Logic Block
CQF	Channel quality feedback
CVS	Clustered voltage scaling
DAC	Digital to analog converter
DFT	Discrete Fourier transfer
DLMS	Delayed least-mean-square algorithm
DSP	Digital signal processing
DVS	Dynamic voltage scaling
EGPRS	Enhanced General Packet Radio Service

FPGA	Field programmable gate arrays
FFT	Fast Fourier Transform
GALS	Globally Asynchronous Locally Synchronous
GPRS	General Packet Radio Service
GSM	Groupe Spécial Mobile
ISI	Inter Symbol Interference
ISR	Ideal software radio
IDFT	Inverse discrete Fourier transform
LMS	Least-mean-square
MAC	Multiplier-adder unit
MMAC	Mobile Multimedia access Communication
NextG	Next-generation wireless communications
OFDM	Orthogonal frequency-division multiplexing
QAM	Quadrature amplitude modulation
QoS	Quality of Service
QPSK	Quadrature phase shift keying
PLL	Phase lock loop
PN	Pseudo-random Noise
PWM	Pulse width modulator
RF	Radio frequency
RISC	Reduced instruction set computer
RTL	Register transistor level

SDR	Software defined radio
SER	Symbol error rate
SINR	Signal to interference plus noise ratio
SNR	Signal to noise ratio
SoC	System on chips
SSRAM	Static Random Access Memory
TDMA	Time division multiple access
USR	Ultimate software radio
VLIW	Very long instruction word
VLSI	Very large scale integration
VPCS	Variable period clock synthesis
WiFi	Wireless Fidelity, commonly using the 802.11 protocol
WLAN	Wireless local area networking

CHAPTER 1

INTRODUCTION

1.1 Motivation

Next-generation wireless (NextG) communications will be a major move toward ubiquitous wireless communications systems and seamless high-quality wireless services [12]. This NextG will use concepts and technologies for innovations in adaptive and highly efficient modulation/coding, spectrum allocation/utilization, in radio communications, networks, services and applications. The NextG will also bring new challenges to VLSI system design. Dynamic and adaptive systems that provide a new paradigm for smart resource management, ultra connectivity, high data rates with effective QoS, scalable power control, and multi-standard adaptation capabilities are attracting the most attention under this aspect.

In designing for this kind of extreme levels of adaptability and re-configurability, as a greater degree of programmability is being made available recently on devices that are nearly as inexpensive as fixed function devices, more and more designers are looking at Software Defined (or Assisted) Radio (SDR) concept for solving the NextG challenges. However, SDR is still a pretty new and vague concept. The progress of digital signal processing, and general-purpose logic, field programmable gate arrays (FPGAs), application specific integrated circuits (ASICs), digital signal processors, and other programmable devices continue to provide new options in the evolution of SDR. Under this perspective, one of the objectives of this thesis work is to investigate the high

adaptive and low power implementation options for SDR using some currently available VLSI technologies. Furthermore, some improvements, in VLSI system and circuit design, are also studied in order to support the new capabilities described by the NextG.

1.2 Contributions of this thesis

In this thesis work, more specifically, both power scalable ASIC implementation and high-speed wave pipelined Domino implementation of a SDR building block, an array multiplier, are studied. System and circuit level optimizations and improvements are made. The main contributions are in the following two areas.

1.2.1 Variable-Precision Multiplier for Adaptive Modulation

The impact of word length in a Least-Mean-Square (LMS) equalized adaptive demodulator is studied. Analytic and simulation results in this thesis work show that there exists a good choice of word length implementation for LMS equalizer for each modulation scheme. Increasing the word length beyond this one does little to improve performance. In order to achieve an optima power/performance ratio, a variable word length datapath solution is needed for different modulation types. A basic building block of this kind of datapath, a variable-precision multiplier using Dynamic Voltage Scaling (DVS) and Gating techniques are proposed and implemented. Simulation results show that a LMS equalizer based on a variable-precision multiplier can produce an 85% power reduction without performance and throughput penalties.

1.2.2 Wave-Pipelined Domino Logic and Clocking Styles in Long Pipelined Applications

In recent years, wave-pipelined Domino logic has received much attention as means to implement high-speed circuits. However, they are vulnerable to parametric variations and the situation will degrade as technology scales down. In this part of the thesis, statistical timing relations are developed for characterizing performance impacts of parametric variations in different wave-pipelined Domino circuits and clocking styles. Power consumption of an array multiplier implemented with wave pipelined Domino logic is also studied. An improved inverting dynamic gate solution is proposed to reduce the usage of dual-rail Domino logics. A 40% power saving is achieved for a 15-stage wave pipelined array multiplier compared to using existing inverting dynamic gates.

CHAPTER 2

LITERATURE SURVEY

In this chapter, some recent developments of 1) SDR concepts, 2) SDR system and architecture, 3) wireless standards and adaptive modulation scheme, are discussed. They are the applications and requirements that we would like to consider. The currently available and widely used low power and low leakage VLSI design techniques, as well as the impact of parameter variations in high performance VLSI system design, are also reviewed. This thesis applies low power and high performance VLSI design techniques to SDR systems.

2.1 Software Defined Radio

Traditional communication systems have typically been implemented using custom hardware solutions. Chip rate, symbol rate, and bit rate coprocessors are often coordinated by programmable digital signal processors, but the digital signal processor does not typically participate in computationally intensive tasks. On the other hand, even with a single communication system, the hardware development cycle is onerous, often requiring multiple chip redesigns late into the certification process. When multiple communication systems requirements are considered, both silicon area and design validation are major inhibitors to commercial success. A software-based platform capable of dynamically reconfiguring communication systems enables elegant reuse of silicon area and dramatically reduces time to market through software modifications (usually taking

days) instead of time-consuming hardware redesigns (normally taking months due to manufacturing delays). Digital signal processors are now capable of executing many billions of operations per second at power efficiency levels appropriate for handset deployment. This has brought software-defined radio (SDR) to prominence.

The advantages of reconfigurable SDR solutions vs. hardware solutions are significant [38]. First, reconfigurable solutions are more flexible, allowing multiple communication protocols to dynamically execute on the same transistors, thereby reducing hardware costs. Specific functions such as filters, modulation schemes, and encoders/decoders can be reconfigured adaptively at runtime. Second, several communication protocols can be efficiently stored in memory and coexist or execute concurrently. This significantly reduces the cost of the system for both the end user and the service provider. Third, remotely reconfigurable protocols provide simple and inexpensive software version control and feature upgrades. This allows service providers to differentiate products after the product is deployed. Fourth, the development time of new and existing communication protocols is significantly reduced, providing an accelerated time to market. Development cycles are no more limited by long and laborious hardware design cycles. With SDR, new protocols are quickly added as soon as the software is available for deployment. Fifth, SDR provides an attractive method of dealing with new standard releases while ensuring backward compatibility with existing standards.

The SDR Forum [83] defines five tiers of solutions. Tier 0 is a traditional radio implementation in hardware. Tier 1, software-controlled radio, implements control features for multiple hardware elements in software. Tier 2, software-assisted-radio, implements modulation and baseband processing in software, but allows for multiple

frequency fixed function RF hardware. Tier 3, ideal software radio (ISR), extends programmability through the radio frequency (RF) with analog conversion at the antenna. Tier 4, ultimate software radio (USR), provides for fast (millisecond) transitions between communication protocols in addition to digital processing capability.

In the following sections, a typical SDR application and several recent proposed SDR systems (tier 1 and tier 2) are presented.

2.1.1 A Typical Radio Applications

Tier 1 and Tier 2 SDR are realistic approaches considering currently available VLSI technologies. In these approaches, only the baseband digital signal processing will be implemented using SDR concepts.

In this section, a baseband wireless communication system based on OFDM within a multi-path fading environment is considered. OFDM is a relatively new and complex wireless communication system. It includes not only standard radio modules, but also some new components, such as DFT/IDFT processing modules. By studying the OFDM system, we can cover most technologies used for wireless transmitters and receivers, which will helps us understand the requirements for software defined radio. Figure 1 illustrates a block diagram of a typical OFDM wireless communication system.

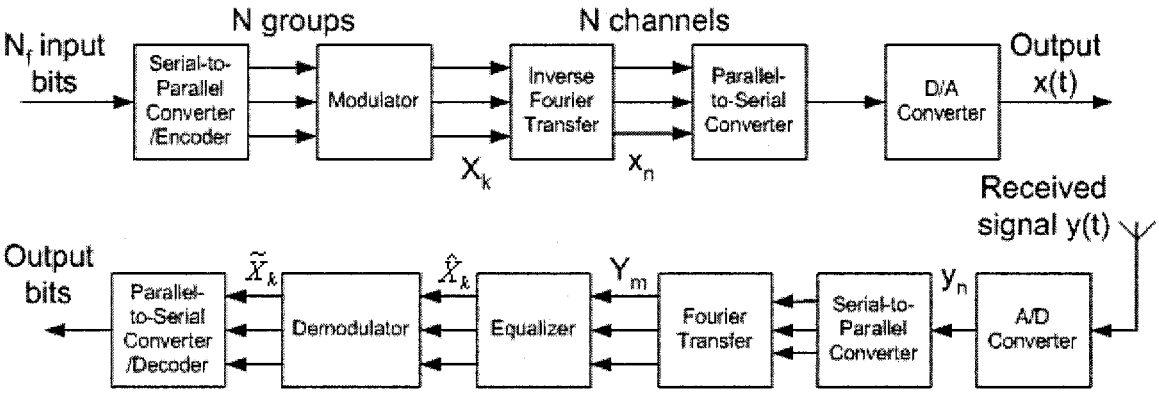


Figure 1 OFDM wireless communication system (baseband part)

The original N_f bits information sequence is segmented into N groups by a serial-to-parallel converter, where the ith group is assigned $\tilde{n}_i$ bits, and $\sum_{i=1}^{N} \tilde{n}_i = N_f$. Each group may be encoded separately, so that the number of output bits from the encoder from the ith group can be $n_i \geq \tilde{n}_i$. These groups can then be modulated and put into N independent channels using Inverse Discrete Fourier Transform (IDFT) technique. The N-point IDFT is applied to the N groups to yield a sequence in time domain [78]:

$$x_n = \frac{1}{\sqrt{N}} \sum_{k=0}^{N-1} X_k e^{j2\pi nk/N} \quad , \text{n=0,1,...N-1} \tag{2.1}$$

where x_n can be considered as a discrete time sequence sampled at $t = \frac{nT}{N}$. Each channel operates at the same symbol rate 1/T, with a distinct constellation X_k, k=0,1,...N-1. The sub-channel carrier frequency is chosen as $f_k = \frac{k}{T}$, k=1...N. After passing the D/A converter, the transmitted signal becomes [78]:

$$x(t) = \frac{1}{\sqrt{N}} \sum_{k=0}^{N-1} X_k e^{j2\pi kt/T} \tag{2.2}$$

The transmitted signals pass a multi-path fading channel. The received signal can be written as:

$$y(t) = x(t) * h(t) + u(t) . \tag{2.3}$$

where * means convolution operation, $h(t)$ is the channel impulse response and $u(t)$ is white Gaussian noise (AWGN). The received signal after the A/D converter becomes:

$$y_n = \sum_{l=0}^{L-1} h_{n,l} x_{n-l} + w_n \tag{2.4}$$

where $h_{n,l}$ and w_n represent the complex random variable for the l-th path of the channel impulse response and additive white Gaussian noise at time n. Here we assume that the multi-path fading channel consists of L discrete paths.

As defined in the standard, a cyclic extension of length T_g is used to avoid intersymbol interference (ISI) and to preserve the orthogonality of subchannels. It is also assumed that the entire channel impulse response lies inside the guard interval. The modulated signal in the frequency domain is recovered by taking the N-point Fast Fourier Transform (FFT) of y_n as:

$$Y_m = \sum_{n=0}^{N-1} y_n e^{-2\pi jmn/N} + W_m \tag{2.5}$$

Finally, we can get [46]:

$$Y_m = \sum_{k=0}^{N-1} \sum_{l=0}^{L-1} X_k [\sum_{n=0}^{N-1} h_{n,l} e^{-2\pi j(m-k)n/N}] e^{-2\pi jlk/N} + W_m \tag{2.6}$$

or

$$Y_m = \sum_{k=0}^{N-1} \sum_{l=0}^{L-1} X_k H_{m-k}^{l} e^{-2\pi jlk/N} + W_m \qquad (2.7)$$

where H_{m-k}^{l} represents the FFT of l-th path m-th channel impulse response. Equation (2.7) can also be rewritten as:

$$Y_m = \sum_{l=0,k=m}^{L-1} X_k H_0^{l} e^{-2\pi jlk/N} + \sum_{k=0,k\neq m}^{N-1} \sum_{l=0}^{L-1} X_k H_{m-k}^{l} e^{-2\pi jlk/N} + W_m \qquad (2.8)$$

The first item on the right hand side of equation (2.8) represents multi-path distortion at desired sub-channel. The second item represents Inter Channel Interference (ICI). The third item shows AWGN added during transmission.

In order to recover the original signal $\tilde{X}_k$, equalization and diversity techniques are needed to cancel channel distortion. A demodulator is also needed to detect the original constellation. The channel impulse response H is estimated based on received signals or training signals, and the received signals are passed through an adaptive filter whose taps are correlated according to the estimated H. The Fast Fourier Transfer module (IDFT and FFT) is used to increase bandwidth efficiency. It is mainly performed in a Butterfly structure that consists of 50-100 MAC (Multiplication Accumulation) units.

It is clear that the baseband wireless application, such as the system shown in figure 1, is a computationally intensive application. The basic operations are encoding/decoding, multiplications/additions, plus data flow controlling. How to partition these operations into hardware and software in an efficient way is the key to designing SDR systems. In the following 3 sections, we will go through some existing examples.

2.1.2 DSP Processor Based SDR System

[37] developed a pure software based simplified OFDM system using 16-bit C code on a DSP core. The OFDM system he considered includes 168 data channels, 22 pilot channels and 66 null channels with QPSK as modulation scheme. The channel model is an AWGN channel without any fading and multi-path. Computationally intensive signal processing operations, such as channel estimation, are not considered.

[58] [26] designed a new DSP processor with additional instructions for complex wireless communication algorithms calculation (i.e. channel estimation, FFT, Viterbi algorithm). The new instructions introduce some additional data flow to accelerate signal processing. These ASIC based DSP processors are application specific processors. Their flexibility and performance are limited by the fixed hardware implementation.

2.1.3 FPGA based SDR system

[34] revealed a FPGA based SDR architecture. The proposed system is shown in figure 2.

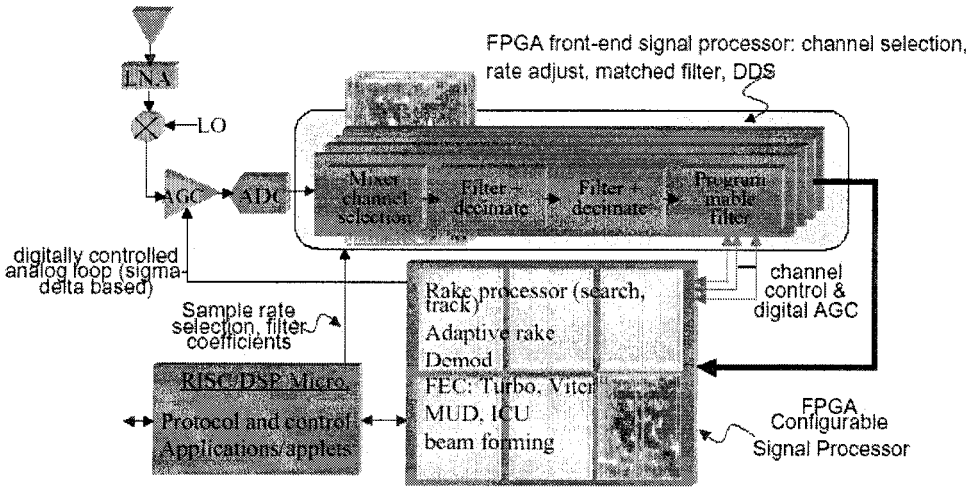


Figure 2 FPGA reconfigurable receiver [C.H.Dick, 34]

In this proposed SDR system, all digital signal processing is realized with FPGA in order to increase the throughput. The digital signal processing includes an adaptive matched filter. 20 simplified DLMS (Delayed Least-Mean-Square algorithm) engines (total of 180 multipliers) are used to adjust 40 tap coefficients of the filter. According to the author, the standard DSP processor, even with advanced architectural extensions (VLIW, very long instruction word) does not satisfy the arithmetic or I/O requirements of a modern communication signal processing engine.

[45] revealed a software radio platform called SOPRANO. This platform comprises a Six-port direct RF conversion and a software assisted PLL with multi-modulation format tracking capability. The block diagram of the platform is shown in figure 3. It can be seen that a FPGA data path controlled by a CPU processor is implemented in the system. The main digital processing task, such as demodulation, timing recovering and filtering etc., are performed through the FPGA. The software functionality is limited in controlling data flow.

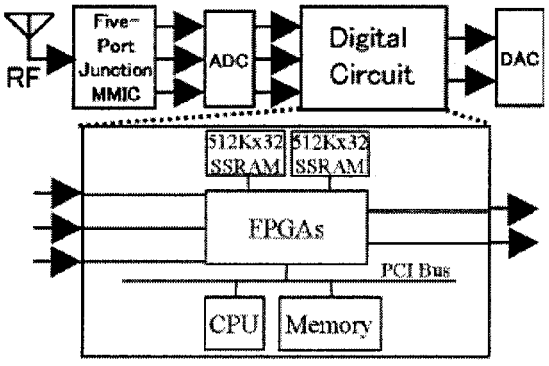


Figure 3 SOPRANO platform [S. Haruyama, 45]

2.1.4 DSP Processor and FPGA Mixed SDR system

[84] developed a reconfigurable software radio architecture for linear multiuser detection in CDMA system (Figure 4). The reconfigurable receivers (equalizer) allow for the integration of multimedia services over wireless channels with variable QoS requirements. To achieve this reconfigurability, the proposed system is partitioned functionally into two core technologies, FPGA and DSP chips. An online channel estimation (which only performs timing estimation), PN generation, and reconfigurable equalizer are implemented with FPGA. Some additional algorithmically complex operations, such as multi-user channel estimation, bit-stream processing, control and reconfiguration management, are partitioned into the DSP chips.

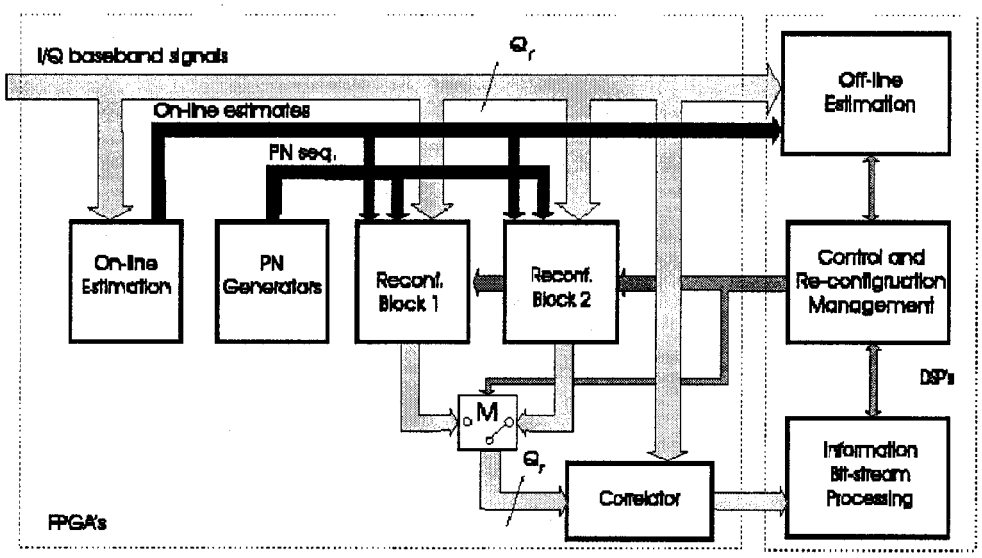


Figure 4 Block-diagram of a software radio implementation [I.P.Seskar, 84]

[87] proposed a SDR system that supports both the wide-area wireless standard (PHS) and local-area wireless standard (IEEE 802.11). The system architecture is shown in figure 5.

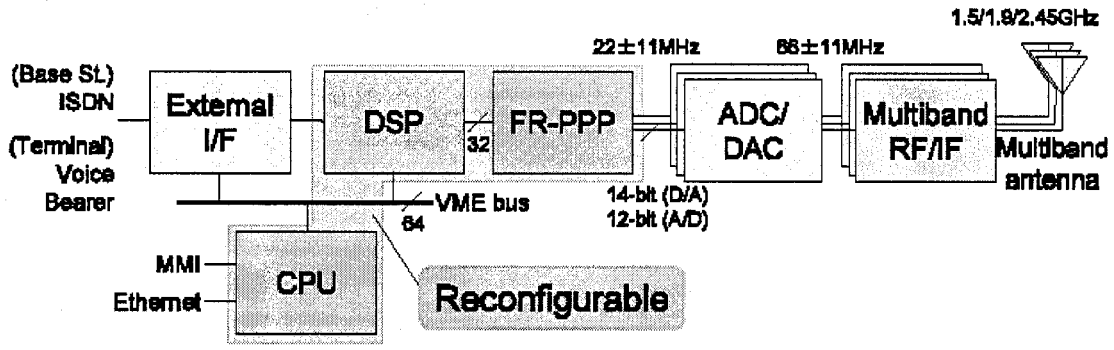


Figure 5 Block diagram of SDR prototype [H. Shiba, 87]

The DSP module in the system consists of 4 DSP chips and a shared memory. This module is used for differential modulation/demodulation. The CPU unit comprise 1 CPU and some RAM. This unit handles the access control and call control. The FR-PPP module is responsible for Direct-sequence de-spreading, timing recovery and channel filtering. This module is implemented with FPGA in order to process high-speed signals. Even though calculation intensive channel equalization is not implemented in the DSP module and the load of the DSP module is not very heavy, it was still reported that the VME bus between the CPU and the DSP causes significant processing delays.

2.1.5 Discussions

Based on the above review, we can find that:

1) DSP based SDR system may have some performance issues if the processing intensive real time operations are introduced into the system, such as channel estimation, channel selection, direct-sequence dispreading, etc.

2) The data path and the controlling path need to be separated in order to increase the system throughput.

3) The DSP and FPGA mixed system have more advantages in point view of performance, flexibility and signal processing qualities.

2.1.6 Customizable Processor

Performance of general purpose DSP processors usually limits them to baseband computations, and full FPGA implementations are costly and inefficient from the silicon area and power consumption standpoint. A good compromise is offered by some FPGA vendors, such as Altera. In their approach, a customizable processor (Nios®) is available on some FPGA devices, i.e. Stratix® and Cyclone®. Instructions of the customizable processor can be extended if DSP blocks in FPGA device are configured to connect to the processor's pins. The DSP block contains high performance full custom multipliers and adders, which can perform multiplication/addition and related operations within 1-2 clock cycle. As a typical Stratix II® FPGA device consists of up to 96 DSP block and 384 18-bit multipliers, many complex digital signal processing tasks are possible and can be configured to be executed through extended software instructions within few clock cycles, which greatly enhances the software capability. As the DSP blocks do not contain application specific operators. They are reusable and can be redeployed as needed. The

Configurable Logic Block (CLB) in the FPGA device is used to route the data flow, link DSP blocks and perform some specific operations.

This customizable processor solution is very attractive in SDR applications. Because it not only has high performance and efficiency due to the use of ASIC implementation of DSP blocks, but is also flexible as the software embedded in the FPGA device plays a major role in the whole data processing. As the DSP blocks are implemented in ASIC, it has another advantage of accessing currently available low power techniques to reduce power.

2.2 Adaptive Modulation Scheme and Algorithm

It becomes more and more common that communication systems adjust their performance and throughput according to channel quality and service requirements. An adaptive modulation scheme can be very suitable for this kind of situation. In the following sections, we are reviewing adaptive modulation schemes and algorithms used in recent and next generation wireless systems.

2.2.1 OFDM (802.11) System

Orthogonal frequency-division multiplexing (OFDM), has already been accepted for the new wireless local area network (WLAN) standards (IEEE802.11), the European Telecommunications Standards Institute's (ETSI) High Performance Local Area Network Type 2 (HIPERLAN/2) and Japan's Mobile Multimedia access Communication (MMAC) system. In the wide-area cellular network, the OFDM system is also becoming a promising technology for providing high-speed multimedia services.

The high-rate and spectrum efficient OFDM systems, employing multilevel modulation schemes with non-constant amplitude, generally require estimation and tracking of the fading channel parameters to perform coherent demodulation. In the IEEE 802.11 OFDM standard, a wireless LAN solution with data payload communication capabilities of 6, 9, 12, 18, 24, 36, 48, and 54 Mbit/s is provided. The system uses 52 sub-carriers that are modulated using binary or quadrature phase shift keying (BPSK/QPSK), 16-quadrature amplitude modulation (QAM), or 64-QAM etc. Forward error correction coding (convolutional coding) is used with coding rates of 1/2, 2/3, or 3/4. In this system, the symbol rate is kept constant.

The following tables summarizes the major parameters of the 802.11a system:

Information data rate	6, 9, 12, 18, 24, 36, 48 and 54 Mbit/s (6, 12 and 24 Mbit/s are mandatory)
Modulation	BPSK OFDM QPSK OFDM 16-QAM OFDM 64-QAM OFDM
Error correcting code	K = 7 (64 states) convolutional code
Coding rate	1/2, 2/3, 3/4
Number of subcarriers	52
OFDM symbol duration	4.0 μs (i.e. max. 0.25Msymbol/sec)
Guard interval	0.8 μs
Occupied bandwidth	16.6 MHz

Table 1 Major parameters of the OFDM Physical Layer

Modulation	Data I+jQ
BPSK	1 bit+0 bit
QPSK	1 bit+1 bit
16-QAM	2 bit+2 bit

64-QAM	3 bit+3 bit
128-QAM	4 bit+4 bit
256-QAM	5 bit+5 bit

Table 2 Modulation type and data bits

The 802.11 standard specifies the multiple data transfer rate capabilities that allow implementations to perform dynamic rate switching (adaptive modulation) with the objective of improving performance. The standard does not define the algorithm for adaptive modulation. However, in most applications, the optimum modulation scheme is assigned for each sub-channel according to its instantaneous distortion and fading characteristics. In other words, the system employs higher order modulation schemes for the sub-carriers with good channel conditions so as to carry more bits, and it employs lower order modulation schemes for those sub-carriers affected by deep fading.

2.2.2 TDMA System

In TDMA systems, slot-by-slot data rate adaptation is achieved through adaptive coding and modulation, while the symbol rate and block size are left unchanged. Time slot aggregation is also carried out in General Packet Radio Service (GPRS)-136 (1-3 time slots/20ms) and GPRS/Enhanced GPRS (EGPRS) (1-8 time slots/GSM frame) to achieve higher data rates. Channel quality is estimated at the receiver and the information is provided to the transmitter through appropriately defined messages. Metrics that have been proposed for estimating channel quality are as follows:

- Frame error rate.
- Mean and standard deviation of symbol error rate (SER) or bit error rate (BER).

- Average SINR (signal to interference plus noise ratio), which may be computed using the minimum Euclidean distance metric derived from a Viterbi decoder or alternatively computed using subspace projection techniques.

In both GPRS and EGPRS systems, measurement reports are included in supervisory ARQ status messages. The GPRS measurement reports consist of an estimated BER and a variance of the BER estimated over a short moving window. In GPRS-136, the receiver provides channel quality feedback as an indication of the modulation schemes that are permitted based on the estimated SINR.

Table 3 summarizes the adaptive modulation techniques in the second and third generation packet data standards for TDMA [12].

System or Standard	Method of rate adaptation	Channel quality feedback	Peak data rate
GPRS (General Packet Radio Service)	Time slot aggregation Adaptive coding	Measurement report in ARQ status message: Signal and interference Bit error rate Signal variance	160 kb/s
TDMA 136	Time slot aggregation Adaptive modulation Incremental redundancy	Channel quality feedback (CQF): In uplink ARQ status message In downlink packet channel feedback	44.4 kb/s
EGPRS (Enhanced General Packet Radio Service	Time slot aggregation Adaptive coding Adaptive modulation Incremental redundancy	Measurement reports in ARQ status message: Signal and interference Bit error rate	473.6 kb/s

Table 3 A summary of adaptive modulation for packet data services in TDMA

Some other adaptive modulation algorithm, such as QoS driven adaptive modulation algorithm (Variable Target SER) is also proposed [4], In this algorithm, low SER is used for voice or video communication, and high order modulation scheme and high SER is used for data communication.

2.2.3 CDMA System

In second and third generation CDMA system, rate adaptation is achieved through a combination of variable spread coding and code aggregation. The adaptive modulation scheme is not standardized, but is under intensive research [12].

2.3 Low Power Techniques

The latest market growth of battery-powered wireless devices has set new goals in the design of systems-on-a-chip (SoCs). These goals include the need for energy-efficient, and power scalable SoC designs that would provide high-performance electronic devices with prolonged battery life. In the following sections, we will go through some widely used circuit level and system level low power techniques, which are suitable for SDR applications.

2.3.1 Overview

According to [10] and [61], available system and circuit level low power techniques can be summarized as follow:

- Multiple Supply-Voltage strategy, which includes: Dynamic voltage scaling (DVS) and Clustered voltage scaling (CVS).

- Clock Gating and Operand Gating.
- Approximate signal processing. This approach allows some inaccuracies in the computation in order to reduce power dissipation.
- Control-data-flow (CDFG) transformations. This technique is to transform CDFG to reduce switching activities.
- Dynamic power management, in this approach, sleep state and idle state of each component are introduced and managed dynamically.
- Interface power minimization, this approach is to reduce power in on-chip or off-chip busses through signal encoding or physical/logical memory mapping optimization.
- Memory optimization techniques, which include: a) Caching/memory access partitioning; b) Control data transfer and placement.
- Hardware software partitioning optimization for low power.
- Instruction level power optimization.

Besides, some other techniques are also reported, they are:

- Globally Asynchronous Locally Synchronous (GALS) design style. This technique aims at reducing power consumption in clock distribution networks.
- Power awareness design style [104].

2.3.2 Power Dissipation Model

The power dissipation of a VLSI system is mainly due to 1) circuit switching power, 2) short circuit power and 3) current leakage power. It can be modeled as:

$$P = P_{switching} + I_{short\text{-}circuit} V_{dd} + I_{leakage} V_{dd} \quad (2.9)$$

where V_{dd} is the operating supply voltage. $I_{short\text{-}circuit}$ and $I_{leakage}$ are short circuit current and leakage current respectively. The switching (or dynamic) power is:

$$P_{switching} = (\sum N_i C_i V_{dd}^2) f_{clock} \quad (2.10)$$

here C_i is the average capacitance switched per operation of type i (corresponding to addition, multiplication, etc.), N_i is the number of operations of type i performed per clock cycle (switching activity). N_i is proportional to bit width of data. f_{clock} are the clock frequency of the system.

2.3.3 Multiple Supply Voltage Approach

As we can see from equations (2.9) and (2.10), the power savings obtained by reducing the supply voltage is significant due to the quadratic relationship between voltage and power. However a lowered supply voltage reduces circuit speed in most VLSI circuit. Thus, supply voltage is constrained by the worst-case critical path delay. In order to optimize the selection of supply voltage, a multiple supply voltage approach can be used on chip either dynamically (i.e. Dynamic voltage scaling (DVS)) or statically (i.e. Clustered voltage scaling (CVS)) according to workload.

2.3.3.1 Clustered Voltage Scaling (CVS)

The basic idea of Clustered Voltage Scaling is to partition the circuit into several clusters and apply the lowest possible supply voltages on different clusters without violating the time constrains. It is reported that 2 or 3 different fixed supply voltages are usually sufficient to get most of the benefits of that approach [32]. A typical compact layout is shown in figure 6.

One overhead of this approach is the need of voltage level converters while signal passes from low V_{dd} clusters to high V_{dd} clusters. However, if a latch is used between clusters, the overhead can be minimized. In fact, with some slight modifications, a latch can have the level converter functionality [97].

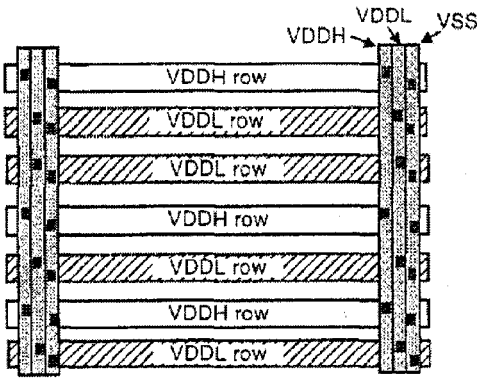


Figure 6 Typical Dual-Supply-Voltage Layout [S. Dhar, 32]

Lack of design tools for doing CVS floorplanning and layout is a major disadvantage of this technique. CAD tools for selecting supply voltages, routing the supply voltage line and identifying clusters are active research directions. [20] presented a dynamic programming approach for assigning voltage levels to the modules in non-pipelining and functionally pipelined data-paths. [114] developed a tool to automatically identify the critical path and select the optimal supply voltage for a cluster. [62] developed an algorithm based on efficient distribution of different supply voltage among the nodes in the data-flow graph. The Lagrange multiplier method is used in an iterative fashion in his algorithm.

2.3.3.2 Voltage Island

Due to the difficulty of floorplanning of small size clusters, the voltage island concept was introduced recently. The basic idea of the voltage island is almost the same as CVS, however, by separating large functional block into different voltage island, modular design is achieved and the system becomes more manageable especially in large SOC design.

[22] developed a 3.2-Gbps multi-protocol serial-link receiver logic core using the voltage island concept. According to them, the power consumption is significantly reduced by powering a large portion of the digital logic at a low supply voltage, while the analog portion runs at a higher supply level. The main advantages of voltage island concept are:

- Standard ASIC methodology and CAD tools can be used during each island design.
- The inter-connections between different voltage islands are limited.
- The power supply of different voltage islands can be different and can be switched off individually. [53]
- The transistor threshold voltage can be different in different voltage island in order to reduce the stand by power consumption [53]

A disadvantage of the voltage island technique is that its power saving is smaller than that of CVS.

2.3.3.3 Dynamic Voltage Scaling (DVS)

The basic idea of this technique is to dynamically adjust the supply voltage and clock frequency of a circuit according to its workload. Due to the area and power overhead of

voltage/frequency regulator and complexity of control algorithm (performed by software), this technique is mostly used for a microprocessor.

[51] published the first experimental results on a general-purpose processor. The architecture of a R3900 RISC core was enhanced with a critical path replica to measure the minimal required supply voltage. The RISC core operates on 1.9 V at 40 MHz and on 1.3 V at 10 MHz. All intermediate frequencies are also supported. This first general purpose implementation did not have a full chip-set and lacked an operating system. [40] presented experimental results on a complete general-purpose platform, called Itsy, running the Linux operating system. Itsy uses a standard commercial StrongARM SA1100 processor that supports voltage scaling. The savings by the Itsy are very modest because only two voltage levels have been implemented, 1.5 V (≥162 MHz) and 1.23 V (<162 MHz). The resulting difference in processor power consumption between the two levels is only 15%. Better results are obtained with the SmartBadge platform [86], which is similar to the Itsy. Extensive power measurements on real-time MP3 audio decoding and MPEG video decoding show that an energy reduction of 40% is possible. [17] designed and implemented a voltage-scaling capable processor based on an ARM8 core. Their processor is fabricated in 600–nm technology and uses aggressive power saving features. In high-performance mode, it runs at a speed of 80 MHz and consumes 476 mW at 3.8 V. When running at 5 MHz and 1.2 V, the processor only consumes 3.24 mW. Thus, power consumption is reduced with a factor of 147, while performance drops by a factor 16. [71] designed a 32-bit PowerPC Soc platform with DVS and Frequency Scaling. The PowerPC system-on-a-chip processor makes use of dynamic voltage scaling and on-the-fly frequency scaling. It adapts to dynamically changing performance demands and power

consumption constraints. It achieves frequencies as high as 380 MHz at a supply of 1.8 V, but the power consumption reduces to 53 mW at a supply of 1.0 V. The voltage and frequency scaling is under software control. [77] developed an energy priority scheduling algorithm that uses workload descriptions to compute energy-efficient schedules, to support power-aware applications on an Intel StrongARM microprocessor. The scheduling algorithm is part of their Linux OS. Their platform supports 128-different supply-voltage levels. A supply voltage of 0.79 V is used when running the processor at 59 MHz. A frequency of 251 MHz requires 1.65 V.

There are very little applications that use DVS technique to reduce power dissipation for a datapath or clusters. [74] developed on-chip controller which dynamically assigns the lowest possible supply voltage to a datapath. The controller selects the suitable supply voltage based on a built-in scan self-test.

2.3.4 Voltage Regulator and Scheduler

Supply voltage reduction can save a great deal of power. However, the voltage and frequency regulator circuit is complex and also consumes power. Understanding the overhead of the regulator circuit is essential while implementing the DVS techniques. In this section, an overview of existing voltage and frequency regulator circuits is presented.

2.3.4.1 Voltage regulator

A typical charge pump based voltage regulator is shown in figure 7 [33]. In steady state, the taps $N - 3$ through N are at logic 1 (i.e. V_{AV} s is sufficient for the test clock to propagate through), while the taps $N + 1$ through $N + 4$ are at logic 0. As a result, all pump

devices are off. If the supply voltage is higher than necessary, one or more NMOS pump devices are turned on, thus discharging the C_{pump} capacitor.

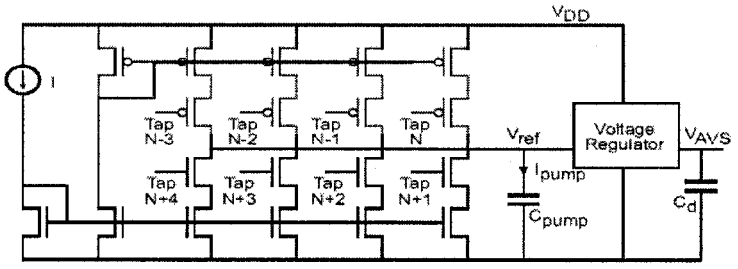


Figure 7 Charge Pump for 8 delay-line taps [Dhar, 33]

Another type of voltage regulator is the Buck Converter (Figure 8) [107]. The inductor and capacitor act as a low-pass filter, and as long as its cutoff frequency is at least an order of magnitude less than the input pulse-width modulated (PWM) rectangular-wave's switching frequency, the output is an average value where its magnitude is set by the duty-cycle of the input rectangular-wave. This PWM based voltage regulator has the advantage of offering a short response time while supporting a wide frequency range. Since the low-pass filtering is not perfect, a 1-MHz switching frequency with 9.2 μH and 10 μF inductor and capacitor sizes, results in a small ripple at the output with a peak-to-peak magnitude less than 5% of the regulated voltage. Besides the inductor and capacitor are normally placed off-chip.

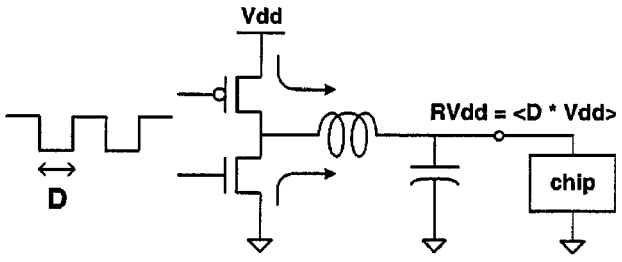


Figure 8 Buck converter [Wei, 107]

2.3.4.2 Frequency regulator

The Dynamic Voltage Scaling (DVS) technique requires an adjustable clock that covers a wide frequency range and an associated pulse width modulator (PWM) to scale the supply or threshold voltage dynamically. [73] developed a quick wake up digital clock-generator based on tunable ring oscillator. The turning range is 44MHz-124MHz. A counter based clock divider was used by [33] to deliver a frequency lower than a reference frequency. His clock generators have high accuracy, however the operating frequency range is limited. The VPCS (Variable Period Clock Synthesis) clock generator proposed by [16] can perform frequency modification within 1 clock cycle and has both clock divider and multiplier. Therefore its operating frequency range is wider, which is advantageous compared with previously developed clock circuits for DVS application.

2.3.4.3 Voltage scheduler

In a DVS system, in order to minimize energy consumption, the system frequency and supply voltage are usually adjusted in such a way that the system operates at the minimum throughput level required by the currently executing tasks. In this situation, a more sophisticated voltage/frequency regulator, with critical path replica, closed regulation loop and control logics, is required. This kind of the voltage regulator is called voltage scheduler.

[17] developed a voltage scheduler for an ARM8 microprocessor (figure 9):

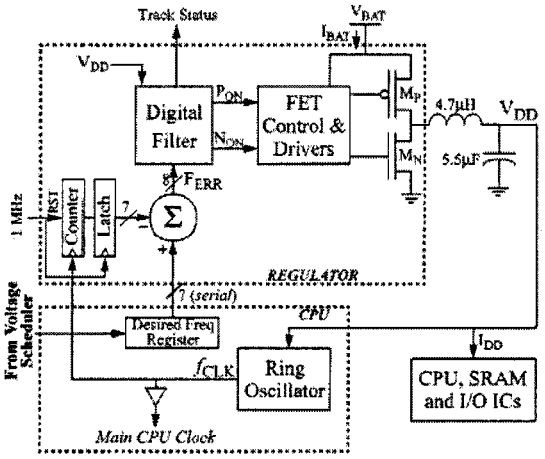


Figure 9 Frequency and Voltage feedback loop [T.D. Burd, 17]

In their system, the ring oscillator on the CPU chip outputs a clock signal whose frequency is a function of the supply voltage V_{dd} . The clock signal is sent to the regulator chip and drives a counter to quantize the frequency into a 7-bit word. This value is subtracted from the desired frequency (in MHz) as set by the operating system, to create an 8-bit frequency error F_{ERR}. The loop filter circuit implements a hybrid pulse-width/pulse-frequency modulation (PWM/PFM) algorithm which generates signals to enable the power FETs via P_{ON} and N_{ON} . The buck circuit consists of M_p and M_n , and the LC tank which down-converts V_{bat} (3.3–6.0 V) to the regulated voltage V_{dd}. This is then fed back to the CPU chip, thus closing the loop. The ring oscillator is placed on the CPU chip, and is designed to track the critical paths of the microprocessor over voltage. A beneficial side effect is that the ring oscillator will also track the critical paths over process and temperature variations. This signal demonstrates that the maximum transition time is 70 μs for V_{dd} signal transitions from 1.2 to 3.8 V and frequency changes from 5 to 80MHz under full system load. The transition energy is a maximum of 4μJ.

[51] realized a closed loop voltage scheduler which used a critical path replica to measure the minimal required supply voltage based on given frequency. His voltage scheduler is implemented in 0.4μm technology (Figure 10). It can vary voltage from 0.8V to 2.9V (with 5% accuracy). The scheduler operates between 40MHz (at 1.9V) and 10MHz (at 1.3V). The power consumption is 140mW at 40MHz.

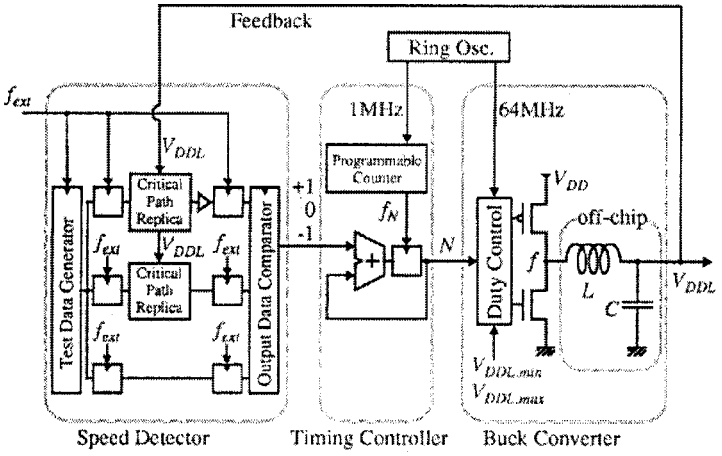


Figure 10 Variable supply-voltage scheduler [T.Kuroda, 51]

2.3.5 Gating Techniques

The idea of gating techniques is to identify periods of inactivity in parts of a circuit and disable the clock or switch on and off activities to those parts of the circuit at appropriate times. The clock gating is a proven low power technique. Automatic synthesis to insert clock gating is still an active research areas. [9] have proposed a scheme for automatic synthesis of gated clocks for finite state machines. Similar works have been done by [10] [80] [65] [105]. [90] introduced its low power solution implemented in the Prime Power® and Power Compiler®. The solution supports automated clock gating insertion as a complement to manual clock gating that designer can perform at the block level. It also

has operand isolation optimization capability within Power Compiler® to shut down whole sections of the data path.

Gated clock can produce glitches if the output of the gating element (e.g. flip-flop) is connected to its input. [81] addressed clock glitching issues on the gated clock. [109] addressed various issues in deriving a gated clock from a master clock.

Besides clock gating, [93] have proposed a technique called operand gating that places transparent latches at the inputs of a combinational logic block. These latches prevent transitions from propagating through the combinational logic when the outputs of the block are not used. [49] developed control-signal gating technique on buses to reduce the bus switching activities.

2.3.6 Power Awareness Design Style

An increasingly important figure-of-merit of a VLSI system is "power awareness" [13], which means the ability to scale power consumption in response to changing operating conditions. These changes might be brought about by the time-varying nature of inputs, desired output quality, or just environmental conditions.

[13] introduced a cost function called power awareness, which quantify the ability of system reactions to constantly changing operational demands. The *power awareness* metric is used to optimize power consumption at system architecture level. Some examples of power awareness design style are:

Increasing the system power awareness by optimizing the parallelization/pipelining partitioning through behavioral transformations.

Increasing the system power awareness by selecting best trade off between system performance and precision: [104] implemented a FFT with 2 different precision multipliers. [69] implemented a LMS equalizer using 3 different FIR length blocks with adjustable tap precision.

2.3.7 GALS Design Style

It is possible to have multi-million transistor systems running at multi-gigahertz speeds. However, such a tremendous computational capability comes at a high price in terms of power consumption and design effort in distributing a global clock signal across the chip. One of the most promising strategies that addresses these issues is the Globally Asynchronous Locally Synchronous (GALS) design style where multiple domains are governed by different, locally generated clocks.

This design style demands low power clock generator or clock multiplier to be integrated into locally synchronous modules. In addition, due to asynchronous interfaces between different modules, the local clock are often stretchable to prevent metastable problems. Clock generator based on a digitally controlled ring oscillator and cycle counters was widely used in this area. Detailed studies can be found in [70][74a, 74b]. The problem of this kind of clock generator is that the output frequency range is not large enough to fit some low power requirements. [115] [64] developed a stretchable clock generator using a ring oscillator and delay line. Their clock can be paused temporarily as a result of arbitration between rising edge of local clock and incoming request and be re-activated through a delay line. A more deterministic C-element based stretchable clock was developed by [116]. The VPCS clock generator proposed by [16] can shift within same

clock period to a delayed clock (same clock in different phases), which can be used as a deterministic stretchable clock. In addition, the proposed clock supports a wider frequency range based on frequency multiplication and division.

2.3.8 Parametric Variance in Low Power Applications

Environmental factors, such as temperature and supply voltage variations, and physical factors during manufacture, such as threshold voltage and geometric variation, are sources of parametric variations [24]. With the reduction of supply and threshold voltage and with the CMOS technology scaling down, parametric variations become a growing concern in recent and future circuit design.

[88] studied Supply-voltage scaling, circuit speed and threshold voltage variations. His study shows that: channel-length variation is a major factor contributing to circuit delay variation at higher supply voltages. On the other hand, the impact of threshold voltage variation on circuit speed scattering becomes crucial at lower supply voltages.

[41] [67] established leakage current analytic model taking the parametric variation and threshold voltage mismatch into consideration. Their work gave some quantitative guidelines in selecting supply voltage and estimating leakage current in low power design.

2.4 Leakage Reduction

There are three main sources of power consumption in digital CMOS circuits: switching power, short circuit power and leakage power. In conventional process technology, the switching component dominates, and the most efficient approach to lower energy consumption is to operate at the lowest possible power supply voltage. The individual

circuit elements, however, run slower at lower supply voltages and circuit performance degrades. One approach to maintain throughput at reduced voltages is to use parallel architectures to compensate for increased gate delays [23]. Another approach is threshold voltage scaling: by reducing the threshold voltage of the devices, the supply voltage can be scaled down without loss in performance. However, at some point, the threshold voltage and supply voltage reduction is offset by an increase in the leakage current. The leakage is typically negligible when circuits are active. However, it can become significant during an idle mode. While the circuit is in its shutdown state, the system should ideally consume nearly zero power, which is only possible if the leakage current is low, i.e. the devices have a high threshold voltage. This contradicts high-performance requirements, for which low threshold is preferred. Several approaches are proposed to dynamically control leakage currents [24]. The multi-threshold, threshold voltage biasing and input vector control are reviewed in the following.

2.4.1 Multi-threshold approaches

The idea with a first approach is to gate logic circuits that have low threshold devices with series connected high threshold switches. During active periods, the high threshold switches are turned on and circuits resume normal low threshold high-speed operations (Figure 11). A key challenge in designing this kind of circuit is to determine the transistor size of high V_{th} devices, which is strongly dependent on data dependent current profiles. [75] and [15] developed algorithms and CAD tools based on linear programming to select the gate sizes and threshold voltages.

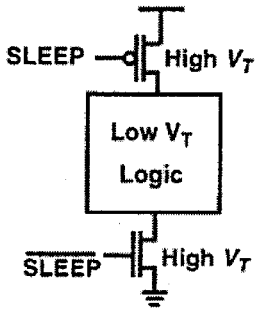


Figure 11 Leakage gating [A. Chandrakasan, 75]

Another multi-threshold approach is to place low V_{th} device in critical paths and high V_{th} in non-critical paths. Some CAD optimization mapping algorithms were studied by [7][47]. [90] Synopsys' Power Compiler© provides a leakage power optimization methodology at RTL level based on the availability of dual V_{th} libraries. The recommended flow consists of a first-pass synthesis using High-V_{th} libraries to meet the design constraints, followed by incremental second-pass replacement of high-V_{th} cells by low-V_{th} cells. The flow enables the designers to achieve their timing goals while maintaining low leakage power.

2.4.2 Threshold voltage biasing

Another proposal for idle mode leakage control involves changing the threshold voltage dynamically by changing the substrate bias [29] [47]. One potential problem with this approach is that the threshold voltage changes as the square root of the bulk voltage and therefore a large voltage swing may be required to change V_{th}. Some auto leakage biased circuits are also proposed by [43]. In his approach, the leakage biased Domino circuit can

be rapidly placed into a low leakage inactive state by using leakage currents themselves to bias internal nodes.

2.4.3 Input Vector Approach

The leakage current of a logic gate depends on its inputs. For different vectors, the leakage is different. Therefore, the input vector that gives the smallest leakage current can be applied to a logic gate or circuit during idle mode to reduce leakage [24].

2.5 Summary

In this chapter, we discussed Software Defined Radio concepts and some recent developments in this area. We found that successful Software Defined Radio implementation, from a VLSI system design standpoint, is related to the ability to partition its functionality onto various modules. These modules can become ASIC blocks, or FPGA blocks or programmable DSP cores.

We have also reviewed some widely used cutting edge low power and low leakage design techniques. These techniques will be used in the following chapters to design high performance arithmetic circuits for SDR.

CHAPTER 3

LOW POWER MULTIPLIER FOR EQUALIZER

3.1 Introduction

It becomes more and more common that communication systems adjust their performance and throughput according to channel quality and service requirements. An adaptive modulation scheme can be very suitable for this kind of situation. An existing example is the 802.11 WiFi system.

As the performance and throughput of communication systems can be adjusted dynamically, their power consumption should also be scalable. In fact, power consumption is an increasingly influential factor in VLSI system design. A component that often dominates power consumption of a VLSI system is its dynamic power (equation 2.10).

The datapath width contributes to power dissipation. Normally, the data path width is fixed and is designed to ensure the performance based on a worst-case scenario. Some variable datapath width systems have been reported [39][68][69]. In [39][68], the bit precision of an equalizer is reduced due to improved SNR (Signal to Noise Ratio) of received signals. In [69], the different intrinsic characters of LMS equalizers of 11-bit and 16-bit widths were studied. In this chapter, we focus on a variable datapath width solution for adaptive modulation. Unlike [39][68], because we are using adaptive

modulation, the improved portion of SNR of received signals will be used to increase the order of modulation. We will prove that even with an adaptive modulation scheme, the variable word length can still be applied with little performance impact. Both analytic and simulation results will be presented.

Dynamic Voltage Scaling (DVS) is a proven technique to reduce power requirements by adjusting the supply voltage according to workload. A drawback of this technique is that: lowered supply voltage increases circuit delay, as the supply voltage is usually constrained by the critical path delay of a circuit in most VLSI system design, the lowered supply voltage will reduce the system throughput. Another power saving technique is the gating technique which is introduced in Chapter 2. In this chapter, the gating and DVS techniques are both applied to the variable width datapath of the LMS equalizer to characterize how much power saving can be achieved in different modulation schemes.

The rest of the chapter is organized as follows: section 3.2 analyzes the good choice of word length of LMS equalizer and its influence on the performance of demodulator under different modulation schemes. Section 3.3 presents the detailed structure and datapath of the LMS equalizer. Section 3.4 presents our variable precision multiplier and the power saving of the LMS equalizer based on this variable precision multiplier.

3.2 Adaptive Demodulation and System Word Length

The part of a communication system that we consider in this chapter is a receiver that consists of a quantizer, a Least-Mean-Square (LMS) equalizer and an adaptive demodulator (Figure 12). The data are modulated in either QPSK or 16/64/256QAM and sent through an Additive White Gaussian Noise (AWGN) channel with Inter-Symbol

Interference (ISI type A [78]). The receiver quantizes the data, passes this data to the equalizer to cancel channel distortion, and then sends the results to the demodulator to detect the original data.

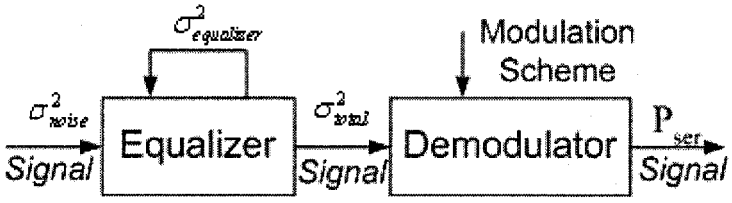


Figure 12 Wireless receiver

Given a Symbol Error Rate (SER) target, the successful symbol detection in the demodulator is limited by the noise level (σ^2_{noise}) at the input of the demodulator. This noise threshold varies for different modulation schemes. The probability of a symbol error for the M-PSK is [78]:

$$P_{ser} = 2Q\left(\sqrt{2SNR}\sin\frac{\pi}{M}\right) \tag{3.1}$$

where SNR is the average Signal to Noise Ratio per Symbol. M=2,4 for BPSK and QPSK respectively. Q(x) is the Q-function defined as:

$$Q(x) = \frac{1}{\sqrt{2\pi}}\int_x^\infty e^{-t^2/2}dt \qquad (x \geq 0) \tag{3.2}$$

The probability of a symbol error for the M-ary QAM is [78]:

$$P_{ser} = 1 - \left[1 - 2\left(1 - \frac{1}{\sqrt{M}}\right)Q\left(\sqrt{\frac{3SNR}{(M-1)}}\right)\right]^2 \tag{3.3}$$

where SNR is the average Signal to Noise Ratio per Symbol.

In order to find the influence of word length on performance, i.e. Symbol Error Probability (P_{ser}) of the demodulator, we wish to characterize the sensitivity of the symbol error probability to noise variance, which can be defined as:

$$Sensitivity = \frac{\Delta\sigma^2_{noise}}{\Delta 10\log P_{ser}} \times 1 \tag{3.4}$$

where $\Delta\sigma^2_{noise}$ is the change of received noise of the demodulator and $\Delta 10\log P_{ser}$ is the change of symbol error probability in logarithm scale. This sensitivity comes from a classic definition of sensitivity defined as: $Sensitivity' = \frac{\partial\sigma^2_{noise}}{\partial P_{ser}}\Delta P_{ser}$. Here the sensitivity can be seen as the noise variance value that triggers a 1dB Symbol error probability increase. Based on definition the sensitivity uses the same unit as noise. Using the noise performance relationship defined in equation (3.1), (3.3) and assuming the average symbol power is 1, the noise sensitivity of different modulation for all P_{ser} points are plotted in Figure 13. The advantage of using the sensitivity instead of an absolute noise value is that we can evaluate the finite word length effect on performance of symbol detection without considering any detail of adaptive modulation algorithm and equalizer imperfection. From Figure 13, we can see that, given a target P_{ser}, different modulation schemes have different sensitivities to input noise variance and the sensitivity monotonically increases with P_{ser}.

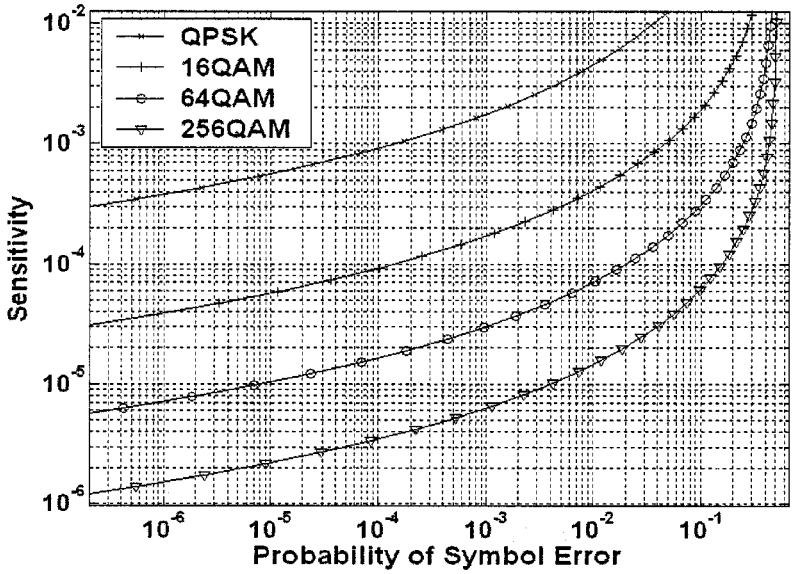


Figure 13 Sensitivity of demodulation performance as a function of symbol error probability of different modulation scheme. (Sensitivity is defined as the excess noise that leads an increase of error symbol probability by 1 dB)

The noise at input of demodulator is caused by 1) channel distortion, 2) imperfection of the equalizer 3) data quantization error and 4) finite word length effect of equalizer tap weight. The input noise at the demodulator is the total noise from output of the LMS equalizer, which can be expressed, according to [21], as:

$$\sigma_{total}^2 = J_{\min} + \frac{N\sigma_c^2}{2\mu} + (|w^*|^2 + 1)\sigma_d^2 \qquad (3.5)$$

The first term is the mean-square error of the infinite-precision LMS algorithm, which includes channel effects, misadjustment and other imperfections of the equalizer. The second term arises because of the error in the quantized tap-weight vector. In that term, N is the number of taps of the equalizer. The third term is produced by the quantization error of input data. The round off is performed after the final summation of the LMS

equalizer. The variance introduced by the finite word length of each tap-weight is: $\sigma_c^2 = 2^{-2Bc}/12$. The word length of tap-weight is B_c plus sign bits. The variance due to the finite word length of input data is $\sigma_d^2 = 2^{-2Bd}/12$. The word length of the input data is B_d plus sign bits. The sign bit is added on top of the selected word length and cannot be dismissed in our case. $|w^*|$ is the optimal Weiner vector [21]. The expected value of tap-weight vector converges exponentially to the optimal Weiner vector.

In order to study the effects of finite word length, we are only interested in the second and third terms in equation (3.5). To calculate the numeric value of these two terms, the input sequence character needs to be known. Here, we consider as an example an LMS equalizer with adaptive step size μ=0.01, and tap length N=32. This makes the second term in equation (3.5) dominates. The value of $|w^*|^2$ is around 1 and does not have much impact on the total noise. The input data word length is 2 bits smaller than that of tap weights. The value of μ should respect lower bound and upper bound conditions defined in [42] as:

$$0 < \mu < \frac{2}{\sum_{k}^{M-1} E[|u(n-k)|^2]} \qquad (3.6)$$

where $\sum_{k}^{M-1} E[|u(n-k)|^2]$ is input signal power. It is the sum of the mean-square values of inputs u(n), u(n-1),..., u(n-M-1). M is number of taps-weight. In our analysis, the above condition is met, so that the stalling/stability problems and settling time prolongation can be excluded from our analysis. The noise generated by finite word

length can be calculated by adding the second and third terms in equation (3.5). The numerical results are plotted in Figure 14, where we can see clearly that the excess noise produced by a finite word length effect of the LMS equalizer decreases exponentially as the word length increases.

From Figure 13, we know how much changes to noise can cause a performance (P_{ser}) modification in the demodulator. Noise caused by channel distortion and LMS imperfections are dominant in most cases. At run time, adaptive modulation schemes will select a modulation in such a way that the noise level is just below the noise threshold of the target P_{ser} for the selected modulation. One way of selecting an equalizer word length is to ensure that the excess noise generated by the finite word length effect of the equalizer causes only a negligible P_{ser} change. As an example, we define negligible P_{ser} change as $\Delta \log P_{ser} = 1/10$, which is the scale in Figure 13. (Some other value can be chosen, if the designer would like the system to have different P_{ser}) By combining Figures 13 and 14, we can find the word length that meets the above selection rule. As an example, if the best performance we could achieve is P_{ser}=1e-5, we should read the sensitivity values at P_{ser}=1e-5 from Figure 13, because this point is the most sensitive point within the scope. Noise that is equal or smaller than this sensitivity value will trigger, at most, a performance (P_{ser}) shift of the defined negligible value. We then look at Figure 14 to find a word length that corresponds to excess noise contributed by the finite word length smaller than this sensitivity value. The final selection results are in Table 4.

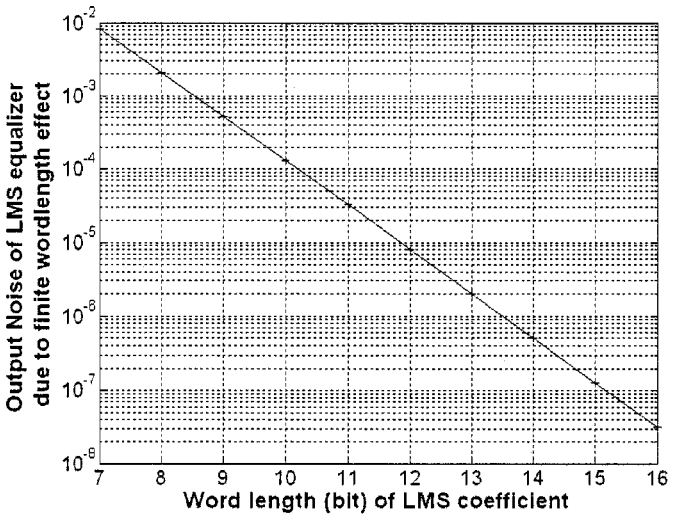


Figure 14 Finite Word Length effects on LMS Equalizer output noise

Modulation type (bits/symbol)	Sensitivity at P_{scr}=1e-5	Output Noise due to the finite word length effect of LMS equalizer	A good choice of processing word length
QPSK (1+1bit)	6e-4	5e-4	9bit+sign
16QAM (2+2bit)	5.8e-5	3.1e-5	11bit+sign
64QAM (3+3bit)	1.1e-5	8e-6	12bit+sign
256QAM (4+4bit)	2e-6	5e-7	14bit+sign

Table 4 Modulation Type and Choice of Processing Word Length

From Table 4, we see that different modulation schemes need different word lengths for the LMS equalizer implementations. As explained earlier, beyond the word lengths listed in Table 4, this parameter has little impact on the performance of the demodulator, regardless of the adaptive modulation algorithm, which is why, by using this selection rule, there is no need to further increase the word length of the datapath in the LMS

equalizer for the given condition. Matlab simulation results presented in the following section confirm this conclusion.

Another way of choosing the word length is to compare the absolute value of demodulator input noise threshold for a given P_{ser} target with the total output noise of the equalizer (Eq. 3.5). With this approach, the constraint of the word length can be further loosened if the channel and equalizer's intrinsic noises are small. In other words, the performance can be traded for shorter word length. This additional saving, if needed, can become a complementary method for choosing word length at run time.

3.3 LMS Equalizer Architecture

The structure of a slightly modified LMS equalizer (delayed direct form with retiming) [8] is shown in Figure 15. A Delayed LMS algorithm is:

$$y(n) = W^H(n)x(n) \tag{3.7}$$

$$W_k(n+1) = W_k(n) + \mu e(n-D)x_k(n-D) \tag{3.8}$$

Where W is the tap weight, e is the estimated LMS error, μ is step size, x is the input data and D is the delay. y(n) is the output signal. In our case, the delay equals the number of taps (tap-weight). The error is calculated as the difference between actual filter output and expected output d(n). During the training period, the expected output is the pilot signal. During operation period, the expected output is the detected signal at the end of demodulator.

$$e(n) = d(n) - y(n) \tag{3.9}$$

From Figure 15, we see that the basic elements of the equalizer are registers, adders and multipliers. The advantage of this delayed LMS equalizer is that its critical paths, both for tap updating and data filtering circuits, are the same, which, in our case, comprises one variable precision Baugh-Wooley multiplier [63] and one 3-input 15-bit carry save adder (complex LMS equalizer). The multiplier dominates the critical path. In fact, the critical path can be reduced if word length of data x(n) and tap weight W(n) are reduced. In the next section, we present our variable precision multiplier. The critical path of our multiplier is proportional to the word length, which will be shown to result in almost 40% reduction of equalizer's critical path. With the shortened critical path, the supply voltage can be reduced to slow down the circuit without any clock frequency reduction. From equation (2.10), we know that the power saving obtained by reducing the supply voltage is significant. In addition, due to the equivalent critical paths in each of the architecture (adder connected to multiplier), DVS can be applied to the entire equalizer, which minimizes overhead.

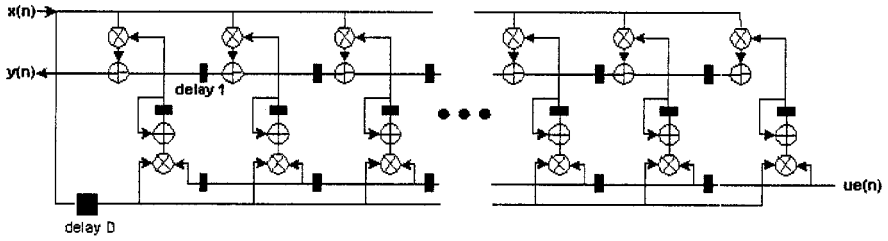


Figure 15 LMS Equalizer (Delayed direct Form with retiming)

3.4 Variable-Precision Multiplier

3.4.1 Variable precision multiplier architecture

The multipliers in equalizers based on the above architecture are reported to take most of the area and to consume 70% of total power [104]. In the remaining of the chapter, we will concentrate on the design and analysis of power scalable multipliers.

A variable precision multiplier was reported in [39], where the precision is adjusted by forcing the least significant bits of the input signal and tap weight to zero. This structure is simple. However, in Baugh-Wooley multipliers, some of "unused" adders will be used as pass through adders. These pass through adders not only consume power themselves, but also cause spurious switching in connected adders. In addition, this approach does not reduce the critical path as much as our gated multiplier, which also influence total power reduction. [85] proposed Wallace-tree multiplier using carry save adders and Booth encoding, with adaptive bit precision obtained by reducing signal and tap weight magnitude. This approach needs a programmable gain controller at the FIR filter output and has the same problems as [39]. Besides, due to excess wiring, Wallace tree multipliers consume more power than the Baugh-Wooley multipliers for word sizes below 16-bit [63].

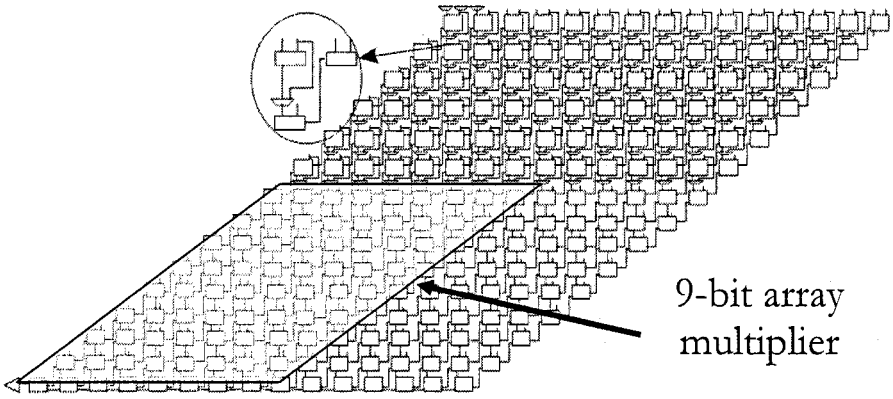


Figure 16 15-bit Signed variable precision array multiplier

In this work, a signed 2's complement variable precision multiplier is proposed. The multiplier is based on a 15-bit Baugh-Wooley multiplier (Figure 16). (The square in the Figure 16 represents full adder cell.) When this multiplier is not working in full precision, only the lower left part is used. The adders of upper level are bypassed and gated to zero. Due to the complexity of sign bit, some additional selections are added in the gating part to link partial products accordingly. The lower right part is not gated in this version because of excess overhead in using static logic gates. The multiplier can be changed to any word length between 9-bit and 15-bit.

Due to gating, the critical path of the reduced precision multiplier is similar to that of fixed precision multiplier of the same size. The overhead of the gating element increases the multiplier area by about 12% (Synopsis Design Compiler estimation). The critical path of the variable precision multiplier and the corresponding fixed precision multipliers are listed in Table 5.

Multiplier Precision	Fixed Multiplier Critical Path (ns)	Multi-precision Multiplier Critical Path	Supply voltage needed (V)

		(ns) at 1,8 V	
9X9	8.75	9.07	1.35
11X11	10.97	11.95	1.5
13X13	12.75	14.39	1.65
15X15	14.75	17.09	1.8

Table 5 Critical Path and Supply Voltage of the Variable Precision Multiplier

The minimum supply voltages in Table 5 are those, based on [23] and critical path circuit simulations of the LMS equalizer, which ensure the same system throughput as a 15-bit multiplier operating with 1.8V supply voltage.

3.4.2 Power Consumption of variable precision multiplier

The power consumption of our multi-precision multiplier (implemented with 0.18μm technology) is simulated using Spectre in Cadence and is plotted in Figure 17. The test vectors are based on the Matlab simulation data at different equalizer taps. The channel and equalizer parameters are the same as that in section 3.2. Three groups of test vectors were used. The first and second groups of vectors were collected during the LMS converging and training period. The third group of vectors was collected after the training period.

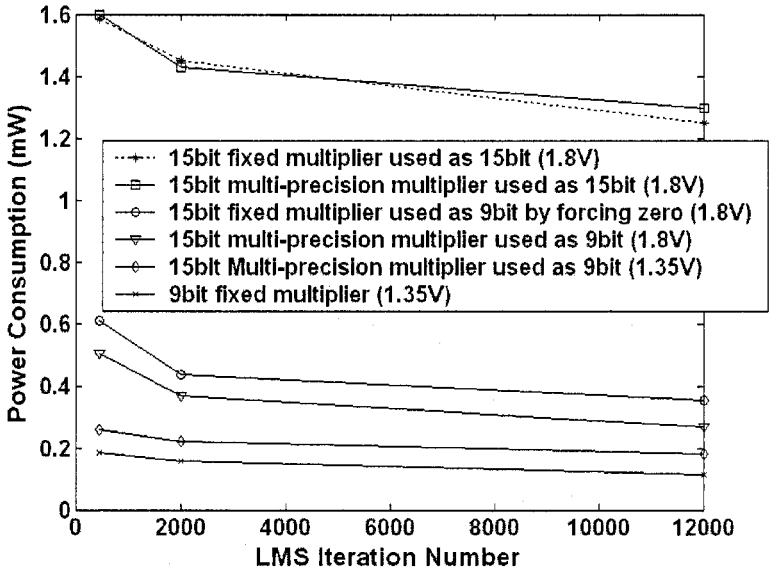


Figure 17 Multiplier comparison (33MHz)

From Figure 17, we see that the power consumption of a 15-bit multi-precision multiplier, when used as 15-bit multiplier, is almost the same as the power consumption of a fixed precision 15-bit multiplier. The power consumption of our 15-bit multi-precision multiplier used as a 9-bit multiplier is 28% higher than the one consumed by a 9-bit fixed precision multiplier. This is due to the incompletely gated adders in the lower right part and to the gating element overhead. If more gating circuits are added to gate the lower right part of the multiplier (fully gated variable precision multiplier), an additional 10% power reduction can be achieved compared to 15-bit variable precision multiplier of Figure 16 while they are used as 9-bit. However, these additional gating circuits may cause additional propagation delay and trigger more spurious switching of the following adders, which can cause 15% more power dissipation while they are used as 15-bit configuration. Detailed simulation results are presented in Figure 18. The optimization of using gating elements could be explored in future research. Considering

massive area savings, compared to having dedicated multipliers for each required width (which requires 7 different fixed-size-multipliers of 9-bit to 15-bit per MAC unit in our case), the overhead of the variable precision multiplier is acceptable.

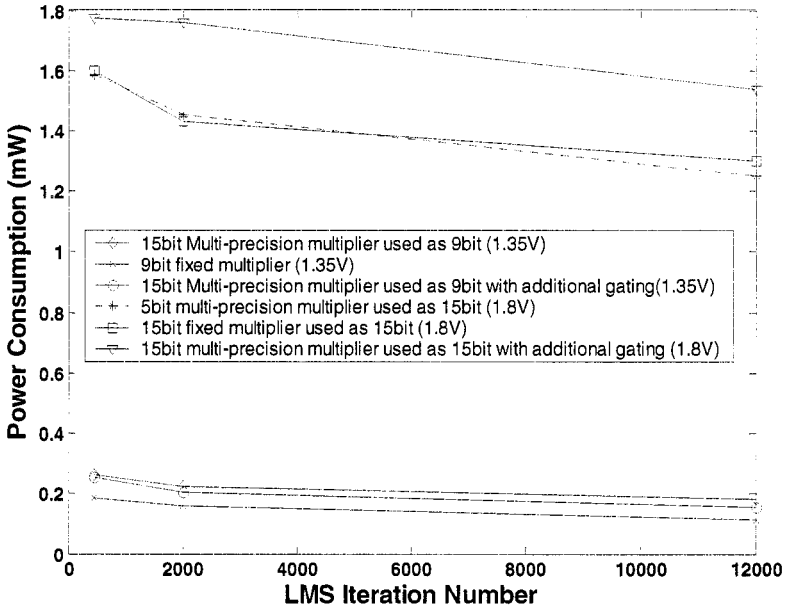


Figure 18 Power consumption comparison between the fully gated variable precision multiplier and the variable precision multiplier of Figure 16)

The power consumption of a zero-forcing 15-bit multiplier [39] used as 9-bit multiplier is compared with our variable precision multiplier used as 9-bit. A 23.5% power saving is recorded with our multiplier before any DVS reduction. The simulation results are in Figure 17. The reason is explained in the beginning of section 3.4.1. Since our multiplier has shorter critical path, additional savings can be achieved.

3.4.3 Advantage of a variable precision multiplier in LMS equalizers

In section 3.2, the performance of adaptive modulation receiver and the good choice of word length were analyzed through analytic modeling. In this section, the performance and finite word length effect of the receiver are evaluated using Matlab models. The simulation results are inline with the upper bound results obtained in section 3.2.

In the simulations reported here, the channel and LMS equalizer parameters are the same as that in section 3.2. Different word length combinations are tested together with different modulation schemes. The performance results are plotted in Figure 19. The average power consumption of a single variable precision multiplier using the test vectors described in section 3.4.2 is plotted in Figure 20. The supply voltages for different word lengths are listed in Table 5.

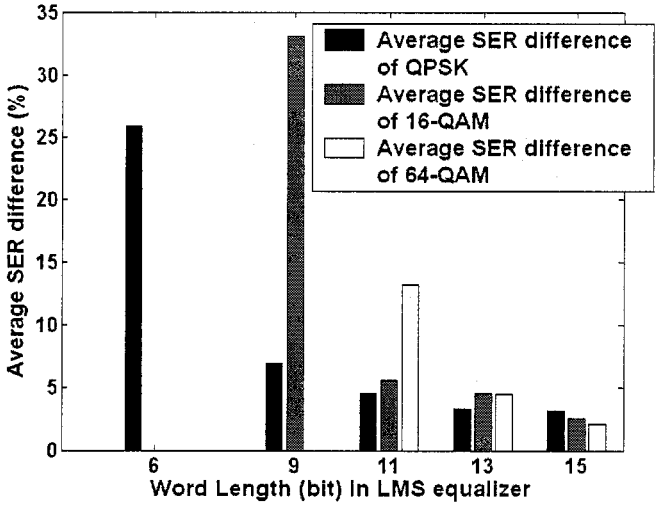


Figure 19 SER difference between finite and infinite word length implementations

From Figure 19 and 20, we find that, for QPSK modulation, starting from 9-bit, the SER difference between the finite word length implementation and floating point (32-bit)

implementation is less than 6%. The 15-bit implementation only reduces the difference to 3%, which is a very minor improvement of overall performance. However, the 6-bit implementation has 26% SER difference, compared to floating point implementation. The power consumption of the 11-bit and the 15-bit implementations is 3 and 7 times more than that of the 9-bit implementation. It is clear that when looking for a good balance between power dissipation and performance, for QPSK, the best tradeoff among the reported solutions is a word length of 9 bits. An 85% power saving is achieved in this case.

Similarly, for 16-QAM modulation, starting from 11-bit, the SER difference between finite precision and floating point precision is less than 5.6%. The 15-bit implementation only decreases the difference to 2.6%. If the word length is reduced to 9-bit, the SER difference jumps to 33%, which is unacceptable. Note that the performance remains almost the same for the 11-bit, 13-bit and 15-bit implementations, while the power consumption of the 13-bit and the 15-bit implementation is 1.6 and 3.2 times larger than with the 11-bit implementation. Therefore, the 11-bit implementation appears to provide better performance/power ratio.

For 64-QAM, the 11-bit implementation has a SER difference of 13.2%, compared to floating point models. The difference reduces to 4.5% and 2.2% for the 13-bit and 15-bit implementations respectively. The power consumption of a single 13-bit and 15-bit multiplier in the receiver is 0.96mW and 1.45mW respectively. It is clear that the 13-bit is a better tradeoff for data path width with 64-QAM modulation. Finally the full word length multiplier and datapath (15-bit) is kept, as it is necessary for 256-QAM demodulation.

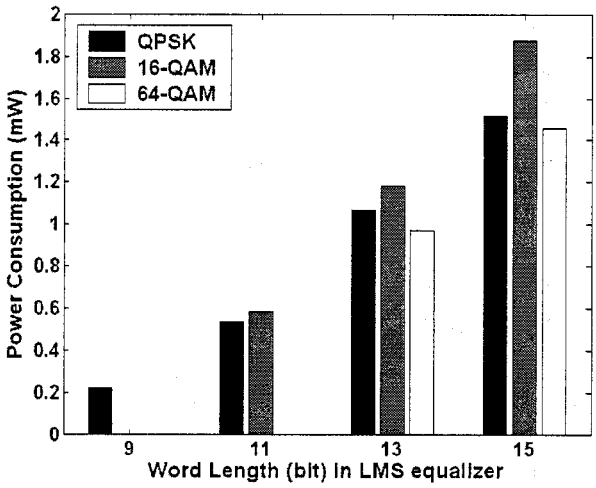


Figure 20 Power Consumption comparisons of different word length implementations (33MHz)

3.4.4 Discussion

The variable precision multiplier designed in this chapter has 12% (estimation) overhead in area and 2%, 28% overhead in power dissipation when used as 15-bit or 9-bit respectively, comparing to fixed precision multipliers of the same size. Current implementation supports 7 different precisions (from 9 bit to 15 bit) in one multiplier. If the configurability of the variable precision multiplier is reduced, for example, if it only supports 4 precisions, 9 bits, 11 bits, 13 bits, and 15 bits, the overhead can be further reduced.

The main power dissipation of the array multiplier built on non-pipelined static circuit in this chapter is due to spurious switching. In order to reduce this portion of the power consumption, a pipelined array multiplier is preferred. However, the registers, such as the flip-flops used in a standard pipelined circuit, consume too much power. One solution is

to use register free wave (pipelined) Domino circuit. In the next chapter, we will focus on building an array multiplier using long pipelined wave Domino logics.

CHAPTER 4

WAVE DOMINO MULTIPLIER FOR DSP CORE SUBJECT TO PARAMETRIC VARIATIONS

4.1 Introduction

Wave-pipelined Domino circuits, also called wave-Domino, have been widely used in high performance microprocessor. Different circuit types, e.g. footed and footless, and different clocking styles, e.g. blocking and non-blocking are proposed in the literature [94] [85] [6] [113]. Due to tight timing constraints, this kind of dynamic circuit is more vulnerable to parametric variations. However, the sensitivity of wave-Domino timing parameters to parametric variations is not well studied. In this chapter, we establish statistical models to compare the impact of parametric variations in different Domino logics and clocking styles.

Parametric variations are a growing concern in recent and future high performance circuit design. Environmental factors, such as temperature and supply voltage variations, and physical factors during manufacture, such as threshold voltage and geometric variation, are sources of parametric variations [24]. A simple way of dealing with this random deviation problem is to add some security margin in the design parameters [94]. However, as we will show, errors caused by some deviations may accumulate along a circuit and as a result, its performance and reliability can be greatly impacted. Therefore, a simple security

margin approach is not always safe or effective, and a statistical or worst-case analysis is needed during design.

Current wave-Domino pipelines used in high performance microprocessors are mostly limited to 4-6 stages [71]. However, long pipelined wave-Domino is needed in some applications, such as Software Defined Radio (SDR). The concept of SDR is to move signal processing operations, e.g. signal filtering and equalization, from dedicated hardware to a microprocessor or configurable hardware in order to enhance flexibility and reduce power. In this kind of application, 9–16 bit pipelined multiplier-adder unit (MAC) is of extreme interest. We will see later in the chapter that this MAC unit is effectively implemented as a 9 to 20 stage long pipeline, in order to reduce design complexity. It is also reported that a longer pipeline implementation saves power compared to the same functionality implemented using a shorter one with complex Domino cells [14]. However, with the increase of pipeline depth, parametric variations become more damaging. Therefore we need to identify a wave-Domino circuit and clocking style more suitable for long pipeline applications.

The rest of the chapter is organized as follows: section 4.2 analyzes the different Domino logic, clocking styles and clock delay line and their sensitivity to parametric variations. Section 4.3 presents a power saving inverting dynamic gate solution and its implementation in a 15-stage pipelined 9-bit array multiplier.

4.2 Domino Logic and Clocking Style Analysis

4.2.1 Dynamic Logic

As described in [24], in static logic, the output node of a gate is always actively driven either to the supply voltage or to ground. By contrast, in dynamic logic, the output node can either be driven or left floating. When the output node is left floating, the value is stored on the parasitic capacitance of the output node. One of the most commonly used dynamic structures is the Domino logic. Each Domnio gate is composed of a dynamic gate with an NMOS pull-down (Figure 21) or PMOS pull-up network followed by an inverter. Domnio gates are cascaded such that the inputs to each stage are driven directly by the outputs of other Domino stages. The addition of the inverter guarantees that the inputs to each stage are all deasserted by the start of the evaluation phase.

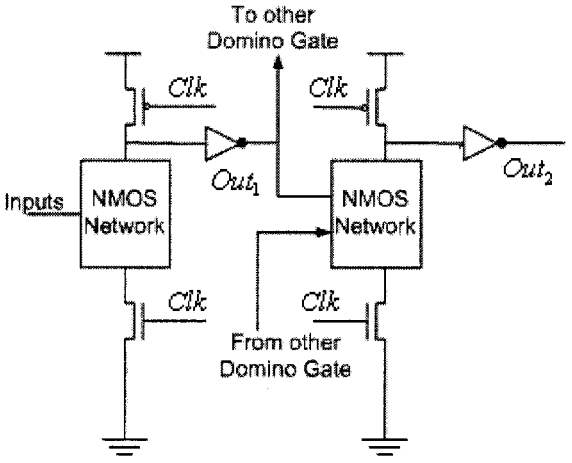


Figure 21 Domino logic (NMOS structure) [24]

4.2.2 Domino logics and clocking styles

N-phase (wave) Domino has been used widely in GigaHertz microprocessor ALU circuits [59] [85] [24]. This approach produces several clock waves in a pipeline and achieves very high operating frequency. The traditional wave dynamic circuit is considered non-blocking. This means that the evaluation clock arrives before critical path data transitions. This clocking style is more tolerant to clock skew. However, in order to use non-blocking clocks, inputs to each dynamic gate must be monotonically rising. Blocking dynamic circuit (or Clock delayed Domino circuit) was proposed recently [85] [113]. Using this clocking method, the evaluation clock of a dynamic gate rises after the latest input has settled. This guarantees that there is no change of inputs to a dynamic gate during evaluation. With blocking Domino, the monotonically rising condition can be waved.

Two types of Domino logics, footed and footless [85] [6] are used. The advantage of footless Domino is the elimination of a clocked foot transistor. The speed of the circuit can be further improved compared to the footed version. However, footless Domino also brings additional constraints, such as strict timing and monotonically rising input signals, into the design.

4.2.3 Clock model

The wave-Domino clock model and its optimization problem were analyzed in [59]. Upper and lower bounds of the wave clock period were developed in their work. However, the performance impacts of parametric variation in different clocking style and different Domino logic were not treated. In this section, we use a modified clocking

model [59] to analyze this problem, and to identify the best clocking and Domino type for long-pipeline applications. We start with reviewing the general constraints that apply to all wave Domino design styles considered.

4.2.3.1 General constraints

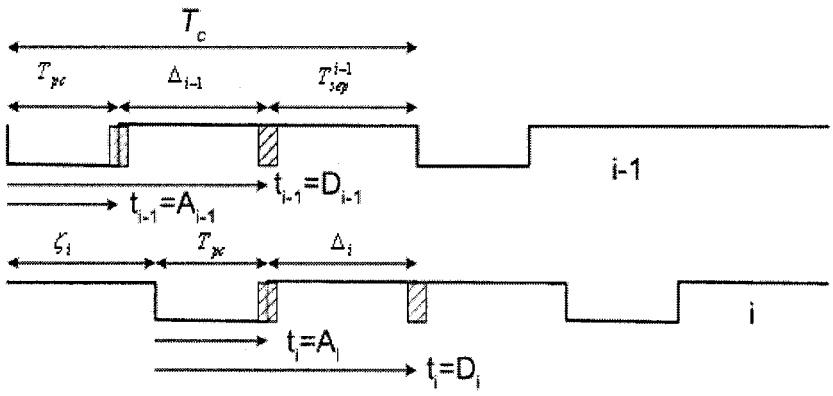


Figure 22 Wave Domino Clocking

Figure 22 shows clocks applied to 2 stages, *i-1* and *i* of a wave Domino pipeline. All stages in the pipeline share one clock signal with period T_c. The duration of the precharge period is T_{pc}. The phase shift period from stage *i-1* to *i* is ζ_i. We suppose that T_c, ζ_i and T_{pc} are constants. Because these parameters are controlled by local clock and are accurate. The input signal arrival time of the Domino pipeline stage *i* is A_i. The signal evaluation period of Domino at stage *i* is Δ_i. And the signal departure time of Domino at stage *i* is D_i. We have $D_i=T_{pc}+\Delta_i$ and $A_i+\Delta_i=D_i$. Here, A_i, D_i and Δ_i are considered as random variables with an expected value of $E(A_i)$, $E(D_i)$ and $E(\Delta_i)$. Their worst-case deviations are: $\delta(A_i)$, $\delta(D_i)$ and $\delta(\Delta_i)$ respectively. Δ_i ($i=1..n$) is considered as an independent random variable. Time variables A_i and D_i are measured with respect to the local wave time zone.

The value of tolerated worst-case deviation should be determined by the designer. It can be several times the standard deviation σ of a parameter, i.e. $k\sigma$. Basically, the designer needs to balance between chip performance and yield in order to make decision. We use the notation: $D_i^{\max} = E(D_i) + \delta(D_i)$ and $D_i^{\min} = E(D_i) - \delta(D_i)$. In order to propagate a signal through a N-phase clock pipeline, the following constraints have to be satisfied:

Precharge separation and phase shift constraint [59]: If we define T_{sep}^i as the time between signal departure and signal end (e.g. start of next precharge), we should have

$$T_c \geq D_i + T_{sep}^i \tag{4.1}$$

In order not to corrupt the wave, a certain time must separate the production of valid evaluated outputs from later precharge of the same outputs of stage *i*. This is necessary to allow enough time for the former to be properly transmitted through gates of stage *i+1*. This time can be determined based on D_i and D_{i-1} as:

$$T_{sep}^{i-1} \geq D_i + \zeta_i - D_{i-1} \tag{4.2}$$

We can define:

$$T_{sep,\min}^{i-1} \equiv D_i + \zeta_i - D_{i-1} \tag{4.3}$$

This $T_{sep,\min}^i$ value is the 'minimum' value that must separate two waves if D_i and D_{i-1} are known. It may be different from stage to stage.

Replacing T_{sep}^i by its 'minimum' value in (4.1), we get

$$T_c \geq T_{sep,\min}^i + D_i \tag{4.4}$$

Wave separation constraint [59]: This constraint is to prevent early departure signals of current wave in stage *i-1* to race through short paths and collide with previous wave in stage *i*. We have:

$$\zeta_i \le D_{i-1}^{\min} \tag{4.5}$$

As by definition, we have $D_i=T_{pc}+\Delta_i$, by taking the expected value, we have:

$$E(D_i) = E(T_{pc} + \Delta_i) \tag{4.6}$$

As T_{pc} is a constant value and is independent of Δ_i, we have:

$$E(D_i) = T_{pc} + E(\Delta_i) \tag{4.7}$$

4.2.3.2 Footless non-blocking wave Domino

For footless non-clock-blocking wave Domino logic, the signal arrival time of stage *i* is considered as:

$$A_i=\max\{D_{i-1}-\zeta_i,\ T_{pc}\} \tag{4.8}$$

and as we mentioned before, we have:

$$A_i+\Delta_i=D_i. \tag{4.9}$$

To minimize contentions and delay, all inputs are designed to arrive at the same time. This is achieved, for example, by adjusting device size. Therefore the rising edge of the local clock should be designed such that:

$$\zeta_i + T_{pc} = E(D_{i-1}) \tag{4.10}$$

If, due to timing variations, data from stage *i-1* arrives before the evaluation phase of stage *i* begins, as defined by the rising edge of the clock on stage *i*, significant short circuit currents will be produced, but according to (4.8), we consider that input data signals become effective coincides with the beginning of evaluation.

The timing analysis is developed through two worst cases that will both affect the maximum operating frequency ($1/T_c$). The first worst case is when the signal departure time of the previous stage is always maximum and takes place after the beginning of the evaluation time of the current stage, i.e. $\delta(\Delta_i)$ is always positive . In this case, (4.8) becomes $A_i + \zeta_i = D_{i-1}$. Combining it with (4.9) gives:

$$\zeta_i + D_i - \Delta_i = D_{i-1} \tag{4.11}$$

With suitable change of index variable i, (4.11) can be recursively injected in (4.11). We have:

$$D_i = D_1 + \sum_{j=2}^{i} \Delta_j - \sum_{j=2}^{i} \zeta_j \tag{4.11a}$$

In the worst-case, $D_1 = E(D_1) + \delta(\Delta_1)$ and $\Delta_j = E(\Delta_j) + \delta(\Delta_j)$ it leads to:

$$D_i^{\max} = E(D_1) + \sum_{j=2}^{i} E(\Delta_j) - \sum_{j=2}^{i} \zeta_j + \sum_{j=1}^{i} \delta(\Delta_j) \tag{4.12}$$

Taking expectation on both side of equation (4.11a), we have:

$$E(D_i) = E(D_1 + \sum_{j=2}^{i} \Delta_j - \sum_{j=2}^{i} \zeta_j) \tag{4.13}$$

As D_1, Δ_j $(j=2,3,\ldots i)$ are independent and ζ_j is constant, we can have:

$$E(D_i) = E(D_1) + \sum_{j=2}^{i} E(\Delta_j) - \sum_{j=2}^{i} \zeta_j \tag{4.14}$$

Using (4.12) and (4.14) we have:

$$D_i^{\max} = E(D_i) + \sum_{j=1}^{i} \delta(\Delta_j) \tag{4.15}$$

combining (4.3) and (4.11) gives:

$$T_{sep,\min}^{i-1} = \Delta_i \tag{4.16}$$

Combining (4.16) and (4.4), we have

$$T_c \geq \Delta_{i+1} + D_i \tag{4.17}$$

If we consider the worst case, (4.17) becomes:

$$T_c \geq \Delta_{i+1}^{\max} + D_i^{\max} \tag{4.18}$$

Combining (4.15) and (4.18), we get:

$$T_c \geq \Delta_{i+1}^{\max} + E(D_i) + \sum_{j=1}^{i} \delta(\Delta_j) \tag{4.19}$$

Combining again (4.19) and (4.7), it becomes:

$$T_c \geq \Delta_{i+1}^{\max} + T_{pc} + E(\Delta_i) + \sum_{j=1}^{i} \delta(\Delta_j) \tag{4.20}$$

In order to cover the worst-case, the wave clock period has to be chosen as:

$$T_c \geq E(\Delta_{i+1}) + \delta(\Delta_{i+1}) + T_{pc} + E(\Delta_i) + \sum_{j=1}^{i} \delta(\Delta_j) \tag{4.21}$$

Finally, it becomes:

$$T_c \geq T_{pc} + E(\Delta_i) + E(\Delta_{i+1}) + \sum_{j=1}^{i+1} \delta(\Delta_j) \tag{4.22}$$

Relation (4.22) shows the independent parameters that affect the global wave clock period of footless non-blocking wave Domino. The first parameter T_{pc} on the right side is the longest required precharge time in the circuit plus a margin, and this value is fixed for all the waves. The second and third parameters are expected evaluation periods Δ of two neighbor stages. The last parameter is the sum of the worst-case evaluation period deviation from the first stage to the last stage. This last term increases with pipeline depth

and parametric variation. As a consequence, a longer wave clock period has to be selected to compensate this accumulated worst-case deviation. In other words, the operating frequency degrades as pipeline depth and parametric variation increases.

In the second worst case, the signal departure time of the previous stage is always minimum ($D_i = D_i^{\min}$) and happens before the beginning of evaluation time of the current stage. As mentioned earlier this will cause serious short circuit currents in footless Domino. However, from the timing standpoint, (4.8) becomes $A_i=T_{pc}$ and (4.9) becomes

$$T_{pc} + \Delta_i = D_i \tag{4.23}$$

as we consider the worst case:

$$D_i^{\min} = E(D_i) - \delta(\Delta_i) \tag{4.24}$$

Combining (4.3) and (4.4), we get:

$$T_c \geq D_{i+1} + \zeta_{i+1} \tag{4.25}$$

as we are in the second worst case condition, (4.25) becomes:

$$T_c \geq D_{i+1}^{\min} + \zeta_{i+1} \tag{4.25a}$$

using (4.25a), (4.24) and (4.10), it becomes:

$$T_c \geq E(D_{i+1}) - \delta(\Delta_{i+1}) + E(D_i) - T_{pc} \tag{4.26}$$

Using (4.7), (4.26) becomes

$$T_c \geq E(\Delta_{i+1}) - \delta(\Delta_{i+1}) + T_{pc} + E(\Delta_i) \tag{4.27}$$

from (4.27) we can see that, in this extreme case, the maximum operating frequency ($1/T_c$) depends on value of precharge time T_{pc}, evaluation time deviation $\delta(\Delta_{i+1})$, and

expected evaluation time of current stage *i* and previous stage *i-1*. Negative evaluation speed deviation $\delta(\Delta_{i+1})$ would not reduce the maximum operating frequency. It is clear that parametric timing variation accumulation along the pipeline does not occur. The only concern in this case is the short circuit current.

4.2.3.3 Footed non-blocking wave Domino

For footed non-blocking wave Domino, the signal arrival time is also considered as $A_i=\max\{D_{i-1}-\zeta_i,\ T_{pc}\}$. To minimize delay, the rising edge of local clock should also be designed as $\zeta_i + T_{pc} = E(D_{i-1})$, which is the same as (4.10). All these setting should lead to the same results as that of footless non-blocking wave Domino from the maximum operating frequency standpoint, e.g. (4.22) and (4.27). The only difference is that, as footed Domino logic is chosen, there is no short circuit even if the signal departure time of previous stage is earlier than the evaluation beginning time.

4.2.3.4 Footed blocking wave Domino

For footed clock blocking wave Domino, by design, the local clock rising edge always arrives later than the worst-case signal departure time of the previous stage. Thus, we have:

$$\zeta_i + T_{pc} \geq D_{i-1}^{\max} \tag{4.28}$$

The signal departure time is fully controlled by the local clock rising edge. It becomes:

$$D_i=\Delta_i+T_{pc} \tag{4.29}$$

In worst case, we have:

$$D_i^{\max} = \Delta_i^{\max} + T_{pc} \tag{4.30}$$

Combining (4.29) and (4.28):

$$D_i \geq D_{i-1}^{max} + \Delta_i - \zeta_i \quad (4.31)$$

Using (4.3) and (4.4) we have:

$$T_c \geq D_{i+1} + \zeta_{i+1} \quad (4.32)$$

(4.32)+(4.31), we have:

$$T_c \geq D_i^{max} + \Delta_{i+1} \quad (4.33)$$

in order to cover the worst case, we have

$$T_c \geq D_i^{max} + \Delta^{max}{}_{i+1} \quad (4.34)$$

Combining (4.34) and (4.30), in worst case, the wave clock period must be chosen such that:

$$T_c \geq T_{pc} + \Delta_i^{max} + \Delta_{i+1}^{max} \quad (4.35)$$

Finally, (4.35) can be rewritten as:

$$T_c \geq T_{pc} + E(\Delta_i) + E(\Delta_{i+1}) + \delta(\Delta_i) + \delta(\Delta_{i+1}) \quad (4.36)$$

This relation shows that the minimum clock signal period (maximum operating frequency) of footed blocking wave Domino only depends on pairs of related stages. No variation accumulation occurs. Thus, a slightly longer precharge time prevent delay variation accumulation. Therefore, this clocking style is more suitable for deep pipeline applications and circuit with large parametric variations.

4.2.4 Clock delay line

In order to implement a wave Domino pipeline, a clock delay line is needed to provide dedicated clocks (e.g. phase shift ζ_i) to each logic stage. However, with parametric variations, the delay through delay elements is not accurate, and delay variations

accumulate along the clock delay line. In the worst case, when the number of phases grows, the *mth* shifted phase that arrives at $\sum_{i}^{m} \zeta_i$ can fall outside the desired clock period as a function of parametric variations, such as a change of operating temperature. In this case, the final result becomes undetermined. Therefore, the number of phases has to be limited. Figure 23 shows a clock delay line implementation for a 3-phase wave Domino pipeline with 9 stages. In this kind of circuit, there are still 9 clock waves in the pipeline, but the number of phases is limited and the delay variation is controlled within each global clock period (e.g. wave clock period). The variation of ζ_i can then be neglected.

The proposed structure pipelines a calculation over several consecutive clock cycles. It is remarkable however that the resulting multi-cycle pipelining is obtained without inserting memory element between the pipelined blocks. Such registers, avoided here, normally contribute delay and thus increase the minimum clock period duration.

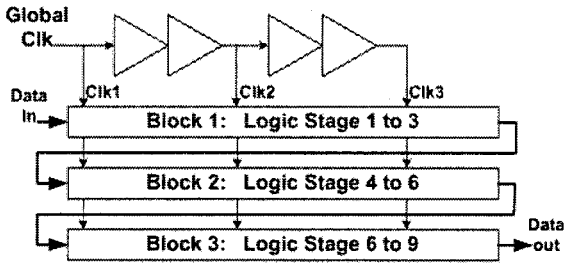


Figure 23 9- Stage pipeline sharing clock delay elements

When using a shared clock delay line as in Figure 23, the sum of the phase shift intervals in each block is equal to one wave clock period, which is:

$$\sum_{i=1}^{m} \zeta_i = T_c \qquad (4.37)$$

where m is the number of phases per wave clock period and ζ_i is the delay of phase i. Note that if the delays produced by the chain of delay elements are shorter, the m^{th} , $2m^{th}$ ... skewed clock get resynchronized with an integer number of clock period according to equation (4.37). Note also that the constraints expressed in the previous section must always be respected by this design.

4.2.5 Threshold voltage mismatch and circuit delay

According to [88], channel-length variation is a major factor contributing to circuit delay variation at higher supply voltages (above 2V). On the other hand, the impact of ΔV_{th} (threshold voltage mismatch) on circuit speed scattering becomes crucial at lower supply voltage. In this section we will try to quantify the impact of threshold voltage mismatch on circuit delay using alpha power law.

As Domino circuit speed is proportional to the saturation current of CMOS [89], We have:

$$E(\Delta) \propto 1/I_{sat} \tag{4.31}$$

where I_{sat} is the saturation current and $E(\Delta)$ is expected signal evaluation time. Using the Alpha-power law, the saturation current can be modeled as [82]:

$$I_{sat} = (V_{dd} - V_{th})^{\alpha} \frac{I_{d0,ref}}{(V_{dd,ref} - V_{th,ref})^{\alpha}} \tag{4.32}$$

where V_{dd} and V_{th} are supply and threshold voltage respectively. $V_{dd,ref}$, $V_{th,ref}$ and $I_{d0,ref}$ are supply voltage, threshold voltage and drain source current at reference point respectively. The factor α varies between 1 and 2. As an average, an α value of 1.5 is adopted in this

study. By differentiating equation (4.31) with respect to the MOSFET V_{th}, the relationship between the signal evaluation time deviation $\delta(\Delta)$ and the MOSFET V_{th} becomes:

$$\delta(\Delta) \propto \frac{\Delta V_{th}}{(V_{dd} - V_{th})^{\alpha+1}} \tag{4.33}$$

Or it can be re-written as:

$$\frac{\delta(\Delta)}{E(\Delta)} = \frac{\alpha \Delta V_{th}}{(V_{dd} - V_{th})} \tag{4.34}$$

This equation shows how the change of supply voltage and threshold voltage impacts the circuit speed deviation. Experimental results have shown that there can be random V_{th} differences between two closely placed 'identical' transistors of the order of about 0.1mV to 100mV (V_{th} mismatch, ΔV_{th}) [76]. This is a local effect that becomes extremely important in deep-submicron transistors as the mismatch magnitude is generally observed to be inversely proportional to the square root of the transistor's area [76]. This local effect is random and is among other things due to a statistical fluctuation of dopant atoms per unit volume. A simple rule of thumb to estimate threshold voltage mismatch is to assume a variation of 1mV of square root of active area per nanometer of gate-oxide thickness. For 180nm technology with 4nm of oxide thickness and minimum channel length and width of 180nm, this corresponds to a threshold voltage standard deviation σ of approximately 22mV [76]. A 3σ ΔV_{th} leads to about 0.07V. Domino circuit speed deviation (eq 4.34) under that 3σ ΔV_{th} deviation is plotted in figure 24.

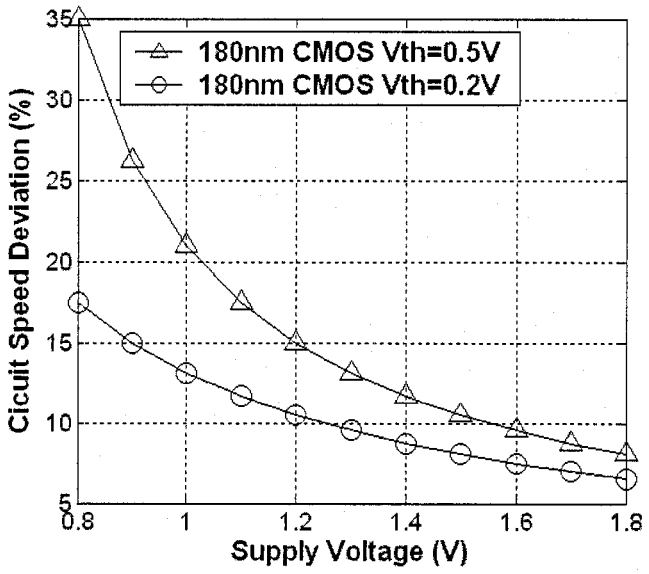


Figure 24 Delay deviation as a function of supply voltage ($3\sigma\ \Delta V_{th}$ = 0.07V)

From figure 24, we can find that circuit speed deviation due to threshold voltage mismatch can reach 22% of expected speed at supply voltage of 1.0V with threshold voltage of 0.5V. The percentage of circuit speed deviation increases quickly while decreasing supply voltage. This may become a serious issue in low power applications when supply voltage is reduced and timing constraints are tight. Also from Figure 24, we can see that reducing the threshold voltage V_{th} from 0.5V to 0.2V can reduce the speed deviation from 22% to 13% at V_{dd}=1.0V.

Although reducing threshold voltage can reduce circuit speed deviation, lower threshold voltage may lead to high leakage current and leakage power dissipation. In the following, we will see if the leakage power dissipation is a factor that influences the wave Domino circuit design. Assuming that for a gate switches, the energy consumption per cycle of a wave Domino circuit can be modeled as:

$$Energy_{total} = I_{leakage} V_{dd} T_c + C_{dyn} V_{dd}^2 + 0.5 I_{sc} V_{dd} \delta(\Delta) \qquad (4.35)$$

where the first term in the above equation represents the energy consumption due to leakage. The second term shows circuit switching energy consumption. The third term is the energy consumed by short circuit current I_{sc}. As the leakage current is mainly contributed by subthreshold leakage current in 0.18μm and 0.13μm technology, the leakage current can be modeled as [76]:

$$I_{leakage} = \frac{W}{L} e^{1.8} \mu_n C_{ox} (U)^2 \exp\left(\frac{V_{gs} - V_{th} + \eta V_{ds} - \gamma V_{bs}}{nU} \right) \left(1 - \exp(-\frac{V_{ds}}{U} \right) \qquad (4.36)$$

where W/L is the transistor dimension. μ_n is the electron mobility and C_{ox} the gate-oxide capacitance per unit area. η is the drain-induced barrier lowering coefficient. γ is the linearized body effect factor, U is kT/q, n is the so-called subthreshold slope ideality factor. These parameters for 0.18μm technology are listed in table 6 [76]. V_{gs}, V_{ds} and V_{bs} are gate to source, drain to source, bulk to source voltage respectively.

η	γ	U	V_{th}	n	C_{ox}
0.034	0.33	26mV	0.51V	1.37	8.22mF

Table 6 Parameters for 0.18μm CMOS process

Using equation (4.35) and (4.36), together with the parameters in table 6, the energy consumption due to dynamic switching and current leakage can be calculated. The analytic results show that for wave Domino circuit, the dynamic power consumption when circuit is active (during the precharge and evaluation period) is dominant, as the dynamic power consumption is 10^6 times larger than the leakage power consumption.

The leakage power consumption only becomes a concern when the circuit is in standby or idle modes.

If for some applications, only the active mode should be considered during VLSI system design, a low threshold approach or Multi-threshold approach (section 2.4.1) can be selected. The advantage of using low threshold CMOS is that it reduces circuit speed deviation as shown in figure 24. If the leakage power consumption in standby or idle modes should also be considered, then the multi-threshold approach should be used (section 2.4.1).

4.2.6 Simulation result and comparison

A 6-stage wave-Domino pipeline is used here to validate and elaborate on the analytic results of section 4.2.2. Simulation results of long pipelined (15-stage) 9-bit array multiplier will be presented in the next section.

Each stage in this 6-stage pipeline consists of a Sum Domino cell (Figure 26). This pipeline is one of the critical paths of a 7-bit array multiplier (Figure 25). This kind of wave Domino pipeline is also widely used in other applications, such as Wallace tree multipliers combined with Kogge-Stone or CLA adders. The performance of this wave pipeline using a non-blocking footless Domino cell and a footed blocking Domino cell were simulated with Spectre from Cadence using the IBM 0.13μm CMOS technology file.

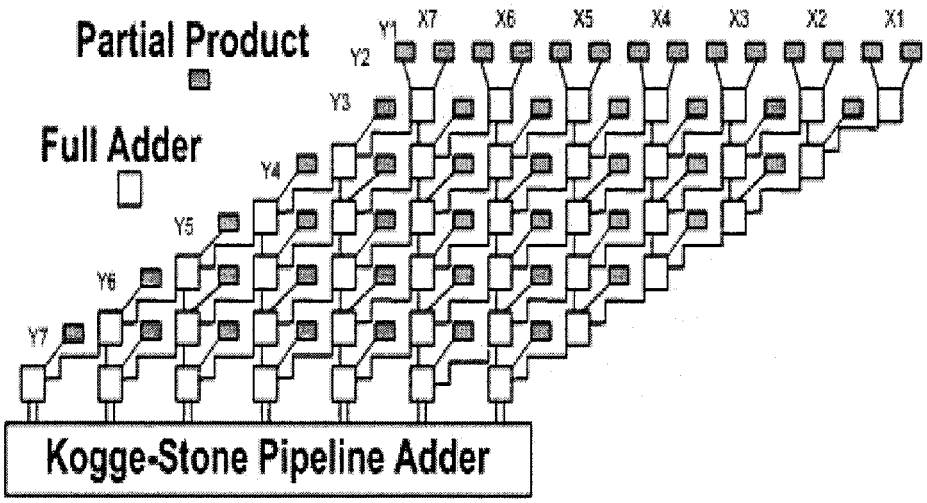


Figure 25 7-bit array multiplier

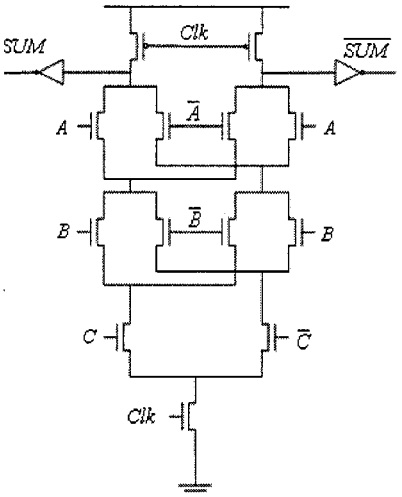


Figure 26 Dual rail Domino Sum Cell

In 0.18μm technology [30], Domino circuit speed (e.g. pre-charge and evaluation time) deviations due to parametric variations are the order of 10%. In 0.13μm technology [30], different parametric variation values can be specified in the technology model file as a function of a σ (sigma) value (for all transistors) for Spectre simulation. A negative σ value reduces circuit speed. For instance, in a negative σ parameter set, transistors'

threshold voltages are above normal value. In figure 27, speed deviations (%) of footed and footless Domino Sum cell (figure 26) under -3σ, -2σ, $-\sigma$, σ, 2σ, 3σ parametric variations are plotted (compared to circuit speed relative to the 0σ condition). We can see from figure 27 that the speed deviation of Domino Sum cell increases rapidly as the parametric variation increases. Under -3σ parametric variations, the cell delay can be as much as 2-3 times larger than with nominal (0σ) condition, which is pretty significant. The speed deviations of a low supply voltage (1.0V instead of 1.2V) Domino Sum cell are also shown in Figure 27. It is clear that a supply voltage reduction compounds the effect of parametric variations.

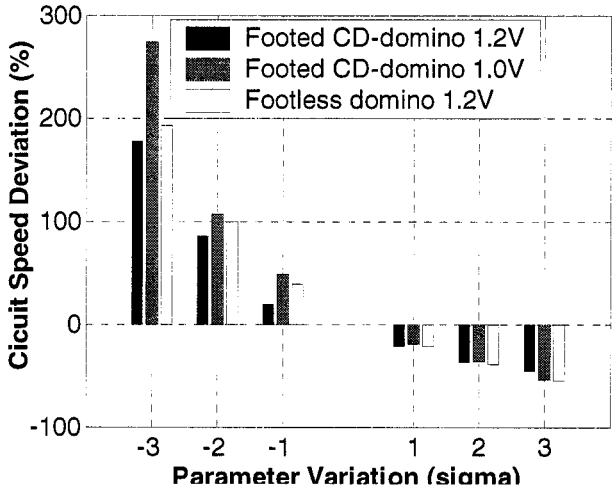


Figure 27 Circuit speed deviation (0.13μm) as a function of parameter variation

The maximum operating frequency of the 6-stage wave pipeline using footed and footless Domino SUM cell and different clocking style is calculated using wave Domino constraints developed in section 4.2.2. A linear problem can be easily formulated to find the optimal design parameters and the maximum operating frequency of a wave Domino under parametric variations. The optimal design parameters include number of phases m

and minimum wave clock period $T_{c_{\min}}$, which depend on circuit parameters, such as precharge path delay T_{pc}, evaluation path delay Δ and circuit speed deviations $\delta(\Delta)$. Note that the maximum operating frequency under $\pm k\sigma$ parametric variation is always obtained by covering the worst-case speed deviation under this parametric variation. The results are presented in Figure 28. From the figure, we see that the footless non-blocking wave Domino has the highest operating frequency if no parametric variation is present. Its performance is 20% higher than the footed blocking Domino wave pipeline of the same size. This is because circuit speed of footless Domino cell is higher than footed Domino due to the elimination of foot devices. Besides, the non-blocking clock style is less constrained and can increase performance in an ideal situation. However, the performance reduces significantly when the parametric variations become important. The maximum operating frequency of the footless non-blocking wave Domino pipeline is about 16% 30% and 36% smaller than that of footed blocking wave Domino pipeline under $\pm 1\sigma$, $\pm 2\sigma$, $\pm 3\sigma$ parameter variation condition.

Increasing the pipeline depth will even enlarge the difference of maximum operating speed. According to Figure 29, the maximum operating frequency of footless non-blocking wave Domino is reduced to 50% of the maximum operating frequency of the footed blocking wave Domino if pipeline depth increases to 12 from 6 under $\pm 1\sigma$ parameter variation condition.

The operating frequency degradation of the footless wave Domino pipeline is mainly caused by the accumulation of circuit speed deviation in each stage. It is clear that the non-blocking footless wave Domino style is more sensitive to parametric variations compared to the footed blocking wave Domino.

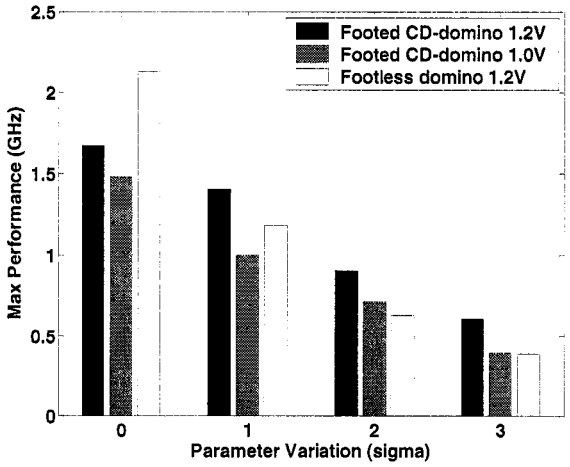


Figure 28 Max performance of wave Domino pipeline

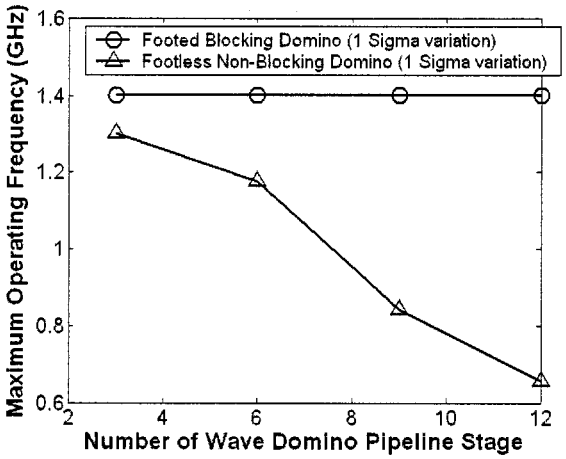


Figure 29 Operating frequency and pipeline depth

4.3 Array Multiplier

4.3.1 Multiplier structure

As an example, we developed a 9-bit array multiplier (Figure 30) for SDR using footed blocking wave-Domino. The multiplier is separated in two parts. The upper part

accumulates partial products of multiplicand and multiplicator (XY). The lower part performs the final addition with a Kogge-stone pipelined adder [24].

Four cell types are used in the upper part (Sum (XOR), Carry (Figure 31), AND, and Repeater). The Sum cell in each stage requires both complement and non-complement signals as inputs. In order to provide the complement signals (inverting signals) in a Domino circuit, a first solution is to implement all supporting cells as dual-rail Domino logic [24]. The dual-rail Domino implementation of Carry, AND and Repeater cells doubles their size and power consumption compared to their single-rail implementations. In fact, both complement and non-complement signals are available in single-rail Domino cell (Figure 31b). However, there is a precharge race problem when using complement signal directly from a single-rail Domino in wave pipeline (see section 4.3.2). a second solution is to add inverting dynamic gates (see section 4.3.2) in the single-rail Domino logic to convert the raw complement signal into a precharge low signal to prevent the problem. As single-rail Domino consumes less power and area, the second solution is selected. The upper part is implemented as a 9-stage pipelined single-rail Domino circuit with inverting dynamic gates. Dual-rail Domino is used for Sum cells, since there is only one more inverter per cell compared to a single-rail implementation.

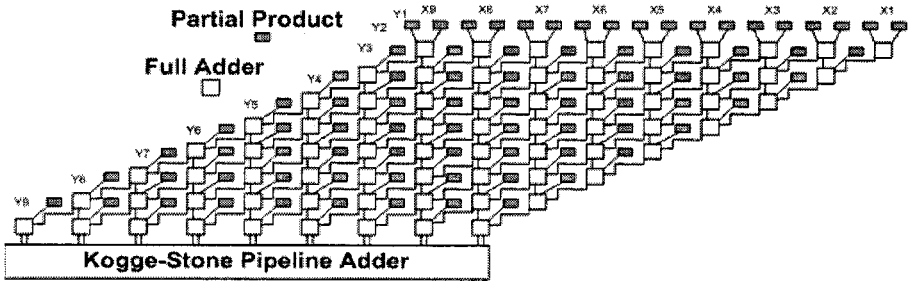


Figure 30 A 9-bit array multiplier

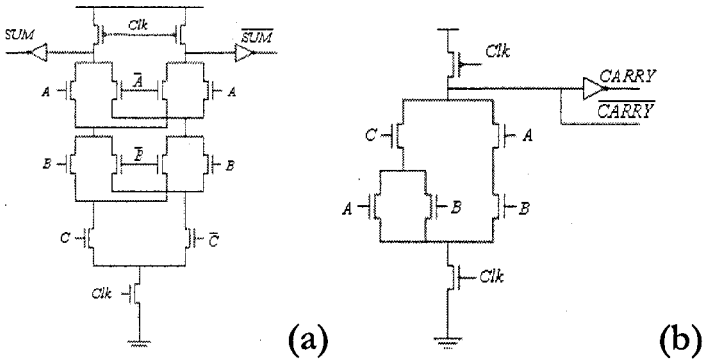


Figure 31 Sum and Carry Cells

Similarly, for the Kogge-stone adder (Figure 32), 4 types of cells are used (Sum (XOR), Carry, PG Generation, and repeater). Single-rail Domino cells can be used throughout the adder. Inverting dynamic gates only need to be added at the end of the carry propagation tree for final Sum cells. A total of 6 stages are used for the adder.

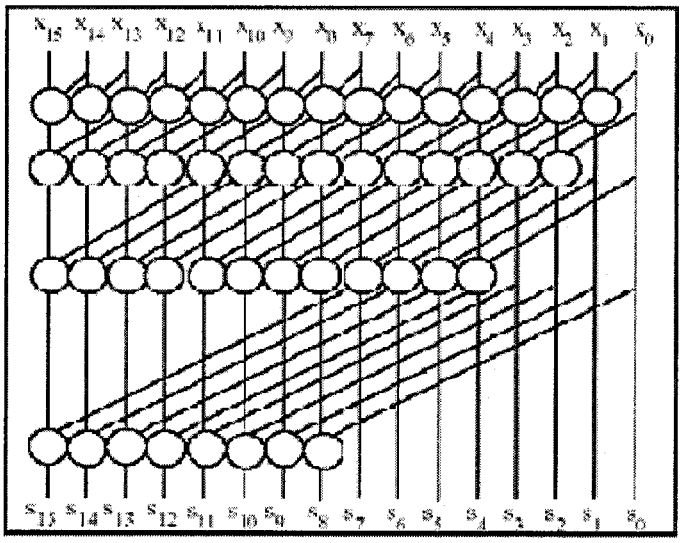


Figure 32 16-bit Kogge-Stone adder [E.Abramson, 2]

4.3.2 Precharge race prevention

The classical precharge race problem occurs when inverting signals are used in n wave Domino circuits and the inverting signal is precharged high. As shown in Figure 33, $\overline{Out1}$ is used as the inverting signal and it is precharged high. This precharge high appears before the end of previous wave (Clk2) of the following stage and disrupts $\overline{Out2}$ of the following stage.

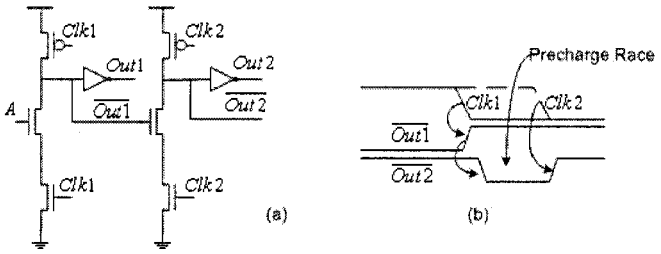


Figure 33 Precharge Race Problem

To prevent this problem, an inverting dynamic gate solution was proposed by [113] (Figure 34b) and widely used [100] [14]. Yee proposed to add an additional Domino repeater gate to produce a precharged low inverting signal. If the pull-down network is simple, this solution does not offer much advantage compared to dual rail Domino logic. Here, we propose a power saving inverting dynamic gate solution using a pass-transistor AND gate (Figure 34a). Only 2 low-V_{th} NMOS are used for the AND gate. The use of low V_{th} NMOS transistors here is to increase circuit speed. As these 2 NMOS devices are not directly connected to ground, leakage is not a concern here. If needed, additional low-V_{th} PMOS can be added to the NMOS switches to improve noise margin. The wave diagram of this power saving inverting dynamic gate is shown in Figure 35. Clearly, the precharge high is eliminated for the inverting signal. There are two glitches during the

transition of Out. They are due to the delay of the Out signal compared to $\overline{Out1}$ (in Figure 34a). The first glitch disappears just before Out settles (from low to high) and is totally controlled by the Out. Since blocking clock style is used here, the clock is blocked until the signal Out has settled, this glitch does not have any impact on signal integrity. The second glitch occurs when the stage is precharging. Since footed Domino is used, this glitch is also negligible. This pass transistor AND gate consumes 4 times less power compared to the Domino repeater gate used in Figure 34b (both with minimum size NMOS as fan out). As inverting signals are required in most cells in a multiplier, the power saving is pretty significant. The circuit speed of proposed inverting dynamic gate solution is about 5-10% slower than Domino repeater based solution (figure 34b). In this application, the proposed solution is not used in the critical path. Therefore there is no any impact on entire circuit performance.

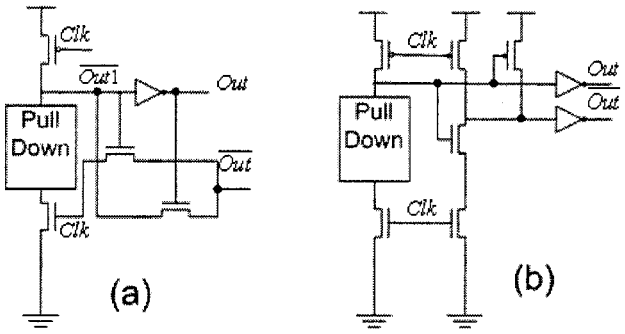


Figure 34 Inverting dynamic gate solutions

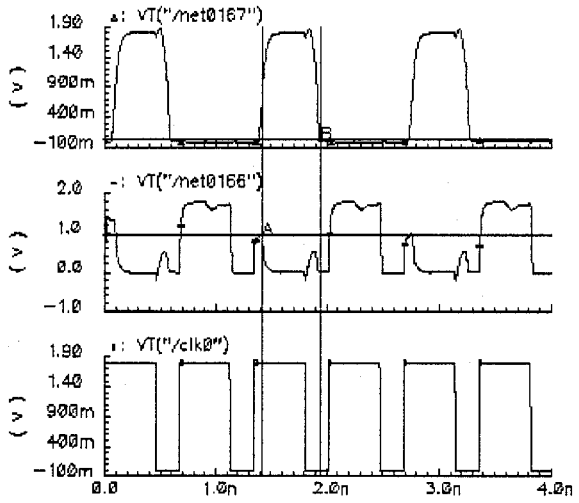


Figure 35 Pass transistor inverting dynamic gate simulated signals (top plot, signal *Out*; middle plot, signal $\overline{Out}$; bottom, local clock.)

4.3.3 Design process of wave-Domino multiplier

Domino circuit cannot be simulated with standard digital RTL simulators, such as design compiler© of Synopsis and ModelSim© of Mentor Graphics. The wave Domino clock style, multi-threshold circuit and low power techniques can only be simulated as analog circuits using Spectre in Cadence. Considering the size of multiplier circuits, e.g. thousands of transistors, it is very difficult to realize the circuit directly through graphic interfaces provided by Cadence. A more sophisticated design process is developed here to facilitate the implementation (Figure 36).

The design process starts with writing VHDL code. The multiplier should be coded as a combination of Full Adder cells and And cells in HDL at the RTL level. This is because, the static circuit implementation of Full adder cells and And cells in HDL will be replaced with Domino circuits later. The debugging and simulation of the multiplier code (VHDL) is performed in ModelSim©. The correctness of circuit connections can then be verified.

The timing is not verified at this step. The RTL level multiplier code is then synthesized using Synopsis Design Compiler© and a Verilog based Netlist is exported. The Full adder cells and AND cells in the Netlist should treated as standard cell. Any description (in Verilog) of these two cells should be removed from the Netlist.

A Domino library is established in Cadence prior to Netlist importing. The Domino Full Adder cells and Domino And cells is created in this library. The pin name and cell name should be the same as defined in VHDL code. During the importing of Verilog Netlist to Cadence, the Domino cell library is configured as reference library. The Cadence Netlist importing tool will automatically map the Full Adder and AND cell in the Netlist with the cells in Domino library. Once the Netlist importing finishes, a Domino multiplier circuit is ready to be simulated with *Spectre* in Cadence.

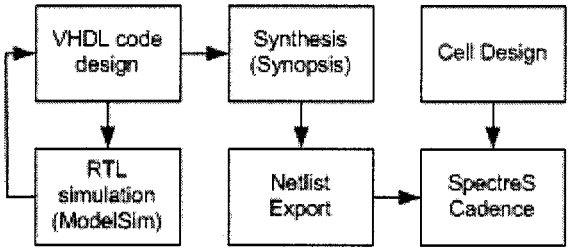


Figure 36 Design process

This design process greatly reduces the circuit implementation time. As the circuit connections are mostly implemented and verified with high level CAD tools, human errors are also reduced.

4.3.4 Simulation result and discussion

The 15-stage wave-pipelined 9-bit multiplier was implemented in TSMC 0.18μm CMOS technology provided through CMC and simulated in Cadence with Spectre. Results are shown in table 7. Minimum size is selected for most transistors in Domino cells. No intensive circuit optimization was performed.

Array Multiplier Implementation	Normalized Power (μW/MHz)	Operating Frequency (GHz)	Latency (ns)
Static non-pipelined [chapter 3]	7.42	0.115 (max.)	0
Single-Rail Wave Domino using (Fig.34a)	4.46	1.48	3.38
Single-Rail Wave Domino using (Fig.34b)	7.30	1.48	3.38

Table 7 Simulation results

Table 7 shows that single-rail Domino using our improved inverting dynamic gate can save 39% power compared to using inverting dynamic gate of Figure 34b [113]. The test vectors are the same as described in section 3.4.2.

The latency introduced by the wave pipelined multiplier is not an issue for baseband radio applications. Since typical symbol duration in radio application is between 40ns and 4μs, a 3.38nSec latency per multiplication (Table 7) will not affect most DSP computations in SDR systems.

The wave Domino implementation of the array multiplier also shows advantages compared to the non-pipelined static implementation. We can read from Table 7 that the normalized power consumption of the wave Domino implementation is 40% lower than the non-pipelined static cell implementation. This is because wave pipeline eliminates

spurious switching, which is the main source of power dissipation in array multipliers built with non-pipelined static circuit. On the other hand, the operating frequency of wave Domino array multiplier is about 10-20 times higher compared to the non-pipelined static implementation. As a typical 16-tap adaptive filter in SDR application requires 128 9-bit multipliers, it is possible and can be more advantageous, from the power and flexibility stand point, to share a high speed wave Domino multiplier implemented as a custom designed circuit instead of implementing several multipliers individually with other implementation styles. It is also advantageous to have an array of high throughput multipliers embedded in the datapath of a high performance programmable/configurable device accessible through suitable machine instructions or configurable modes.

CHAPTER 5

CONCLUSIONS

In this chapter, we will go through some conclusions that are derived from above developments.

5.1 Variable Precision Multiplier

We find that the variable data path width solution for LMS equalizers in adaptive modulation schemes can provide improved power efficiency with little performance penalties. Analytic results and Matlab model simulations support the proof of the existence of a good choice of word length implementations for different modulation types. The power savings of using acceptable performance and reduced word width LMS equalizer can reach 85% for each multiplication.

The presented 15-bit variable precision signed multiplier for the LMS equalizer supports precisions that change from 9-bit to 15-bit. It reduces critical path length in proportion to precision. A variable precision multiplier that we designed has 12% (estimation) overhead in area and 2-28% (when used as 15-bit or 9-bit) overhead in power dissipation compared to fixed precision multipliers of the same size. Considering the massive area savings, compared to using dedicated multipliers for each required width, the variable precision multiplier is very attractive. However some further improvements to this multiplier can still be made in this part.

5.2 Pipelined Wave-Domino Multiplier

The performance of some Domino logics, such as footless non-blocking Domino and traditional non-blocking Domino, degrades with an increase of pipeline depth. However, the footed clock blocking Domino logic is less sensitive to these variations. This type of circuit maintains a constant operating frequency regardless of pipeline depth and is very suitable to implement deep-pipelined Domino circuits.

Single-rail Domino logics reduce power consumption over dual-rail Domino logics. However, when complement signals are needed, an inverting dynamic gate needs to be added to single-rail Domino to prevent precharge race problem. The proposed inverting dynamic gate solution is compatible with footed clock blocking Domino circuits. It provides significant power savings compared to existing solutions. A 15-stage pipelined 9-bit array multiplier achieves 39% power reduction when using the proposed gate.

The wave Domino implementation of the array multiplier also shows advantages compared to the non-pipelined static implementation. The normalized power consumption of the wave Domino implementation is 40% lower than the non-pipelined static cell implementation because the wave pipeline eliminates spurious switching, which is a major source of power dissipation in non-pipelined static circuit. The operating frequency of wave Domino array multiplier is about 10-20 times higher compared to the non-pipelined static implementation. It is more advantageous, from the power and flexibility stand point, to share the high speed wave Domino multiplier in a custom designed microprocessor.

5.3 Software Defined Radio Platform

The main burden of migration from hardware based wireless system to SDR is the processing speed and power consumption of computationally intensive operations required by wireless applications. These operations are different for different applications. However, basic building blocks are very often composed of multipliers and adders. Typically, only the data flow, which links these building blocks together, is different from one application to another. In addition, performance and power consumption of the system highly depends on the quality of arithmetic circuit, especially multipliers. Therefore, embedding multiple arithmetic circuits in a SDR hardware platform, and moving the non-time-critical data flow controlling tasks to software is a preferred solution. It not only increases the flexibility and performance, but also reduces cost and power of SDR systems.

It is clear that from performance and power consumption standpoint, the different implementation of arithmetic circuit can make huge differences. Arithmetic circuits are one of the most intensive research areas for so many years. With recent developments of low power techniques and aggressive clocking styles, this type of circuit can be further improved. An ASIC implementation of arithmetic circuit has the advantage of having the capability of accessing all these cutting edge VLSI design techniques and can achieve great performance and low power. Because advanced VLSI circuit style are largely incompatible with conventional Configurable Logic Block (CLB) in FPGA. It is not recommended to implement arithmetic circuit in CLB, to accelerate any signal processing. As a compromise, the recent approach of customizable DSP processor brings much

attention. In this approach, built-in ASIC based arithmetic circuits are used together with FPGA CLB circuits and microprocessor. It not only has the high performance provided by ASIC circuit, but also has excellent flexibility as a result of using reconfigurable CLB circuit and programmable microprocessor to link these embedded arithmetic blocks. It seems that this is one of the promising directions to lead the future development of SDR systems.

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