POLYPUBLIE

Characterization of integrated MOS circuits under voltage stress and application to power conversion chains of electronic implants

Seyed Saeid Hashemi Aghcheh Body

Document en libre accès dans PolyPublie
Open Access document in PolyPublie

Date	2004
Type	Mémoire ou thèse / Dissertation or Thesis Mémoire de maîtrise/Master's thesis
URL de PolyPublie PolyPublie URL	https://publications.polymtl.ca/7315/
Conditions d'utilisation Terms of use	© Tous droits réservés / All rights reserved
Référence Citation	Hashemi Aghcheh Body, S. S. (2004). Characterization of integrated MOS circuits under voltage stress and application to power conversion chains of electronic implants [Mémoire de maîtrise, École Polytechnique de Montréal]. PolyPublie. https://publications.polymtl.ca/7315/

Détails de la thèse
Thesis details

Directeurs de recherche Advisors	Mohamad Sawan, & Yvon Savaria
Programme Program	Non spécifié

Ce fichier a été téléchargé à partir de PolyPublie, le dépôt institutionnel de Polytechnique Montréal
This file has been downloaded from PolyPublie, the institutional repository of Polytechnique Montréal
https://publications.polymtl.ca

UNIVERSITÉ DE MONTRÉAL

CHARACTERIZATION OF INTEGRATED MOS CIRCUITS UNDER VOLTAGE STRESS AND APPLICATION TO POWER CONVERSION CHAINS OF ELECTRONIC IMPLANTS

Seyed Saeid HASHEMI AGHCHEH BODY

DÉPARTEMENT DE GÉNIE ÉLECTRIQUE

ÉCOLE POLYTECHNIQUE DE MONTRÉAL

MÉMOIRE PRÉSENTÉ EN VUE DE L'OBTENTION DU

DIPLÔME DE MAÎTRISE ÈS SCIENCES APPLIQUÉES (M.Sc.A)

(GÉNIE ÉLECTRIQUE)

Janvier 2004

© Seyed Saeid HASHEMI AGHCHEH BODY, 2004.

National Library
of Canada

Acquisitions and
Bibliographic Services

395 Wellington Street
Ottawa ON K1A 0N4
Canada

Bibliothèque nationale
du Canada

Acquisisitons et
services bibliographiques

395, rue Wellington
Ottawa ON K1A 0N4
Canada

Your file Votre référence
ISBN: 0-612-90870-4
Our file Notre référence
ISBN: 0-612-90870-4

The author has granted a non-exclusive licence allowing the National Library of Canada to reproduce, loan, distribute or sell copies of this thesis in microform, paper or electronic formats.

The author retains ownership of the copyright in this thesis. Neither the thesis nor substantial extracts from it may be printed or otherwise reproduced without the author's permission.

L'auteur a accordé une licence non exclusive permettant à la Bibliothèque nationale du Canada de reproduire, prêter, distribuer ou vendre des copies de cette thèse sous la forme de microfiche/film, de reproduction sur papier ou sur format électronique.

L'auteur conserve la propriété du droit d'auteur qui protège cette thèse. Ni la thèse ni des extraits substantiels de celle-ci ne doivent être imprimés ou aturement reproduits sans son autorisation.

In compliance with the Canadian Privacy Act some supporting forms may have been removed from this dissertation.

While these forms may be included in the document page count, their removal does not represent any loss of content from the dissertation.

Conformément à la loi canadienne sur la protection de la vie privée, quelques formulaires secondaires ont été enlevés de ce manuscrit.

Bien que ces formulaires aient inclus dans la pagination, il n'y aura aucun contenu manquant.

Canada

UNIVERSITÉ DE MONTRÉAL

ÉCOLE POLYTECHNIQUE DE MONTRÉAL

Ce mémoire intitulé:

CHARACTERIZATION OF INTEGRATED MOS CIRCUITS UNDER VOLTAGE STRESS AND APPLICATION TO POWER CONVERSION CHAINS OF ELECTRONIC IMPLANTS

présenté par: HASHEMI AGHCHEH BODY Seyed Saeid

en vue de l'obtention du diplôme de Maîtrise ès sciences appliquées

a été dûment accepté par le jury d'examen constitué de:

M. MARTEL Sylvain	Ph.D., président
M. SAWAN Mohamad	Ph.D., directeur de recherche
M. SAVARIA Yvon	Ph.D., co-directeur de recherche
M. DESJARDINS Patrick	Ph.D., membre

To whom we are waiting for,

To my father and mother,

To my wife and children,

Acknowledgements

It has been my great pleasure to study in the Electrical Engineering Department at Ecole Polytechnique de Montreal working in GRM and PolyStim labs. This experience gave me a great chance for having wide and deep expertise in Microelectronic Engineering. My strong faith in God and in myself have remained constantly high enough to carry this work to the end.

First and foremost, I would like to express my gratitude to my supervisor, Professor Mohammad SAWAN, not only for his guidance, patience and for the freedoms he has granted me throughout my years of study.

I would also like to thank my co-supervisor, Professor Yvon SAVARIA. His many years of experience has allowed me to focus on the critical and interesting issues of all the problems encountered. The results of this research would not have been of the same quality without him pushing the design goals and test strategies always higher and higher.

I would like to thank the members of my thesis committee for their valuable feedback and contribution. I would like to acknowledge my family for their solid support of all my endeavors and their contribution in removing most of stresses from my student life.

I also wish to thank all fellow students, technicians and staff of PolyStim and GRM, in

particular Christian FAYOMI, Jonathan COULOMB, Yamu HU, Jean-Francois GERVAIS, Kamal EL-SANKARY, Jean-Luc TREPANIER, Moncef DJEBBI, Claudine OULETTE, Ghislaine ETHIER CARRIER, Rejan LEPAGE, Alex VESSY, Martin PARE for their help, support, encouragement and friendly discussions. I am very honored to be part of their family. Thanks to Robert CHEBLI, Abdallah KASSEM, Virginie SIMARD and specially, Annie TREPANIER for the French translation of the abstract and condensé en français.

Lastly, but not the least, I would like to thank the Canadian Microelectronic Corporation (CMC) for fabricating the test chip and NSERC for their financial support.

To all of you, thank you so much for all the support you have given to me during this research. Find through the above lines the expression of my heart and gratitude for all you have done for me.

Résumé

Les nouvelles technologies submicroniques améliorent la performance et l'efficacité des circuits intégrés. Cependant, ces technologies peuvent apporter quelques limitations pour certaines applications. Par exemple, ces technologies ont une tension nominale inférieure à la tension d'alimentation. D'autre part, les applications biomédicales spécifiques exigent des tensions plus élevée que celle de la nouvelle technologie submicronique. Utiliser les technologies pures CMOS qui supportent des tensions élevées ou employer des approches hybrides, où des technologies à haute et basse tension sont combinées, sont les solutions possibles. Le développement d'une chaîne de conversion de puissance ainsi qu'un circuit amplificateur de tension ont été étudiés dans ce mémoire. La fiabilité du dispositif dans des conditions de stress a été également couverte, constituant un élément important.

Il a été démontré que l'architecture d'un PCC est sujette à quelques contraintes et limitations qui influencent fortement son efficacité globale. Aussi, il est clair que l'intégration complète de l'implant pourrait améliorer sa performance d'une manière significative, mais elle impose également des issues de fiabilité. L'architecture de PCC conventionnelle a été caractérisée en termes d'efficacité de puissance. Deux nouvelles architectures ont été proposes, remplaçant les redresseurs de diode par des redresseurs synchrones intelligents, ce qui a presque doublé l'efficacité de la puissance relative et a aussi facilité l'intégration de EI.

De plus, les blocs fonctionnels de base et les caractéristiques d'un doubleur de tension ont été présentés. Il a été souligné que celui-ci souffre de la chute de tension d'une diode ou de la tension de seuil d'un commutateur MOS. Aussi, la structure d'une étape de multiplicateur de tension à rendement élevé a été introduit. Par après, la structure classique d'un multiplicateur à plusieurs étages de tension utilisant simplement des étages cascadés a été présentée. Il produit un facteur de multiplication proportionnel au nombre d'étage. En conclusion, une nouvelle structure améliorant le facteur de multiplication de façon exponentielle a été rapportée. Les résultats de simulation pour un multiplicateur simple et un multiplicateur de tension de plusieurs étages à rendement élevé ont été présentés et le résultat des paramètres de conception ont été caractérisés. Il a été prouvé que les soucis de fiabilité exigent l'utilisation de techniques de multiplication de tension d'efficacité inférieure.

Les résultats expérimentaux de la puce fabriquée ont été développés afin de caractériser les mécanismes de panne CMOS. Les résultats prouvent que le transistor MOS sera sujet à des problèmes de fiabilité lorsque des conditions de stress sont appliquées à ses bornes. Il est possible que les processus MOS ne puissent pas soutenir des tensions beaucoup plus hautes que la tension d'alimentation nominale. Lorsqu'on a besoin de telles tensions, des processus développés afin de les supporter devraient être utilisées.

Abstract

New sub-micron technologies improve the performance and efficiency of the integrated circuits. Taking advantages may bring some limitations in certain applications. For instance, these technologies have lower nominal power supply voltage. On the other hand, specific biomedical applications require voltages higher than the nominal power supply voltage of new sub-micron technologies. Using either pure CMOS technologies that support high voltages or using hybrid approaches, where low and high voltage technologies are combined are possible solutions. The development of power conversion chain and voltage boosting circuit were studied in this thesis. The device reliability under stress condition was also covered as a major concern.

It was shown that the architecture of a PCC is subject to a few constraints and limitations that heavily impact its overall efficiency. It was also clarified that integrating the whole implant could improve its performance significantly, but it also imposes reliability issues. The conventional PCCs architecture was characterized in terms of power efficiency. Two new architectures were proposed that replace diode rectifiers with Smart Synchronous Rectifiers, and almost double the relative overall power efficiency and facilitate EI integration.

Moreover, the basic building blocks and characteristics of a voltage doubler were introduced. It was outlined that it suffers from forward voltage drop of a diode or

threshold voltage of a MOS switch. Then, the structure of a high efficiency voltage multiplier stage was introduced. Later, the classical structure of a multi-stage voltage multiplier using simply cascaded stages was presented. It provides a linear multiplication factor with the number of stages. Finally, a new structure that improves the multiplication factor exponentially was introduced. The result of simulation for a single and multiple stage high efficiency voltage multiplier were presented and the result of design parameter were characterized. It is shown that reliability concerns could result in using the voltage multiplication techniques of lower efficiency.

Experimental results from fabricated chips developed to characterized CMOS breakdown mechanisms. The results prove that the MOS transistor will be subjected to reliability problem when the stress conditions are applied to their terminals. MOS processes may not be able to support voltages much higher than the nominal supply voltage. When such voltages are needed, processes developed to support them should be used.

Condensé en français

I. Introduction

Obtenir l'énergie nécessaire afin d'alimenter un implant électronique (EI) est un défi de mise en oeuvre significatif. Les systèmes de stimulation employant l'alimentation percutanée ou des batteries incorporées ne sont pas idéaux pour un fonctionnement sécuritaire à long terme. Pour les applications à long terme, les tendances récentes favorisent des liaisons RF inductives [10,64,159]. Cependant, des considérations biologiques imposent des limites sur la puissance maximale transférée à travers la peau [11].

II. Chaîne de conversion de puissance pour implants électroniques

La configuration d'une Chaîne de Conversion de puissance efficace (PCC) pour alimenter le EI est fortement désirable. De plus, les nouvelles technologies submicroniques sont très avantageuses pour l'intégration des implants électroniques.

II.1 Contraintes et limitations des Simulateurs Electriques Fonctionnels (FES) à canaux multiples

Il y a plusieurs contraintes et limitations derrière les paramètres impliqués dans une application requérant un stimulateur à canaux multiples FES. Cette section énonce les

principales contraintes identifiées.

II.1.a Variation dans le courant de charge

La puissance consommée par un EI se répartit entre celle consommée par le coeur du EI et celle requise par le générateur de stimulus. Avec l'évolution de la technologie, la puissance requise pour faire fonctionner le coeur est faible et décroissante, tandis que la puissance nécessaire pour stimuler un secteur sensible est fixe, alors que le nombre de sites de stimulation a tendance à augmenter avec les besoins de l'application. La deuxième composante a donc tendance à dominer les exigences en puissance. De plus, la stimulation efficace exige une quantité de charge minimale pour être injectée dans le tissu. Cette quantité diffère pour les divers tissus et elle varie aussi d'un site de stimulation à un autre.

II.1.b Variation dans la tension de charge

L'aire de Contact d'Electrode-Tissu efficace (ETC) pour passer le courant de stimulation varie d'un site à un autre. Par conséquent l'impédance des canaux varie. Dans un tel cas, la production de courant de stimulation exige des tensions plus hautes que la tension d'alimentation nominale des nouvelles technologies.

II.1.c Variation de la tension d'entrée

Pour un EI donné (alimenté de façon transdermique), la valeur de la puissance reçue est affectée par la distance et l'orientation relative de l'émetteur et de l'EI. Ainsi, on s'attend à des variations considérables sur le signal d'entrée pour une certaine période de temps. Pour préserver une efficacité acceptable, il est essentiel d'ajuster la puissance transmise. Ceci impose l'emploi d'une rétroaction ou d'un redresseur intelligent pour réguler la puissance transmise.

II.1.d Défi associées à la conception du circuit

Comme les tensions d'alimentation sont réduites, l'efficacité des multiplieurs de tension se dégrade significativement. Donc, des techniques de conception de circuits complexes sont exigées pour surmonter ces problèmes [36,61,115,152,158,195,213]. L'intégration complète du EI pourrait améliorer considérablement ses performances, mais cela impose aussi quelques problèmes de fiabilité à long terme [99].

II.2 Architecture de PCC conventionnelle

Une architecture conventionnelle de PCC se compose d'un redresseur à diode (DR) et d'un régulateur de tension (VR), en série avec la charge qui inclut un MCS aussi bien que le coeur de l'implant, comme illustré à la Figure 2.1. Un MSVM est inséré pour générer les hauts voltages demandés pour la stimulation. L'atténuation de tension inhérente à la polarisation directe de la diode ($V\gamma$) résulte en une perte de puissance significative à

travers le (DR). Ceci affecte l'efficacité de la PCC et diminue la tension livrée aux modules suivants. Cet impact négatif devient de plus en plus significatif dans la conception des alimentations à basse tension. C'est notamment le cas pour les nouvelles technologies submicroniques. En plus, le DR est généralement mis en oeuvre en employant des diodes discrètes, ce qui va à l'encontre de l'objectif d'intégrer complètement l'EI.

II.3 Redresseur Intelligent Synchrone (SSR)

Dans la structure des redresseurs classiques, on ne peut rien faire pour éviter la chute de tension des diodes. Les diodes Schottky, qui ont des chutes plus faibles, ne sont pas disponibles sous la forme de composants discrets à basse tension. L'utilisation de SSR [135,144] ouvre de nouvelles possibilités, en ce qui concerne l'architecture des PCCs. Cela est possible parce que la perte de la puissance dans de tels composants est reliée à la chute ohmique dans les transistors MOS. Si les paramètres de conception sont attribués de telle sorte que l'atténuation à travers le SSR soit beaucoup plus basse que celle d'une diode, alors il en résulterait une amélioration significative de l'efficacité. Un autre avantage du SSR est d'éliminer des diodes externes, ce qui est un pas vers un EI entièrement intégré. Un diagramme bloc simplifié d'un tel dispositif est illustré à la Figure 2.3. Notons que la réalisation du comparateur approprié avec un taux adéquat de sur-échantillonnage peut être un défi.

II.4 Nouvelle Architecture PCC basée sur SSR

Une nouvelle architecture PCC est obtenue en insérant un SSR à l'étage d'entrée du MSVM, comme illustré à la Figure 2.4. Avec cette architecture, l'efficacité en puissance est améliorée et la prise de l'entrée du SSR directement au lieu de l'entrée du DR fournit une haute tension au MSVM. Ceci permet de réduire le nombre d'étages dans le convertisseur de tension et donc d'obtenir des modules de multiplication de tension plus efficaces.

La seconde architecture proposée combine les deux chemins de distribution de la puissance et les alimente avec un seul SSR, comme illustré à la Figure 2.5. L'avantage de cette architecture n'est pas tant l'amélioration de l'efficacité de la PCC, mais bien l'élimination du DR, qui est généralement réalisée par des diodes hors puce.

Les résultats de l'analyse mathématique sont récapitulés aux Tableaux 5.3 et 5.4. L'analyse de l'efficacité est effectuée en utilisant les suppositions et les paramètres de circuit fournis au Tableau 5.1, ainsi que le courant et les équations de puissance du Tableau 5.2. Donc, l'utilisation des architectures proposées réduit la puissance requise pour des implants électroniques et augmente significativement leur efficacité globale.

III. Multiplieur de tension à haute efficacité

Les tensions d'alimentation requises pour des circuits analogiques sont souvent dictées

par des sources de signal externes. De plus, la charge nécessite parfois des tensions plus grandes que la tension d'alimentation. Une alimentation à basse tension impose des contraintes sévères dans la conception de circuits. Compte tenu de la réduction des tensions nominales d'alimentation des technologies submicroniques, les facteurs de multiplication requis pour produire une tension donnée sont croissants.

Il existe deux circuits conventionnels, le régulateur à commutation et le convertisseur basé sur la pompe de charge. Ces circuits peuvent produire des tensions plus hautes que la tension d'alimentation. Les circuits à pompe de charge utilisent des capacités comme dispositifs d'emmagasinage d'énergie, tandis que les régulateurs à commutation utilisent des inductances ou des transformateurs comme dispositifs d'emmagasinage d'énergie.

III.1 Pompe de charge

Les pompes de charge sont des circuits pouvant pomper la charge vers le haut pour produire des tensions supérieures à la tension d'alimentation régulière. Ils comportent des condensateurs, commutateurs et au moins une horloge à deux phases. Comme les pompes de charge n'utilisent aucun composant magnétique, il est plus facile de les implémenter dans une seule puce. Un circuit de pompe de charge typique est illustré à la Figure 3.1. Le circuit est organisé de façon à ce que dans une première phase, la capacité soit chargée à l'alimentation. Quand l'horloge est basculée, la capacité maintient la charge de la phase précédente et donc, la somme de l'alimentation et de l'amplitude d'horloge est induite sur

son autre borne. Une pompe de charge réalisée en technologie CMOS est présentée à la Figure 3.6.

Une structure de pompe de charge a été proposée par Dickson (Figure 3.3) [48]. Ce circuit comporte deux transistors NMOS croisés, couplés avec des capacités de pompe de charge et deux horloges d'entrée ayant des phases inversées. Afin d'avoir un meilleur transfert de charge, un chemin unidirectionnel est établi au travers de commutateurs PMOS séries qui ne sont pas contraints par la tension de seuil. La conception a été améliorée récemment en utilisant des commutateurs de transfert de charge statiques et dynamiques (Figures 3.4 et 3.5) [213] et des techniques de commutation du puit (Figure 3.7) [138]. Une vue d'ensemble d'un étage de multiplication de tension est présentée à la Figure 3.8a.

III.2 Caractéristiques du Multiplicateur de tension

Les caractéristiques d'un multiplicateur de tension, incluant l'efficacité de la puissance, le courant de sortie, les ondulations de sortie et le gain de tension ont été étudiées. Dans cette étude, la résistance des commutateurs est ignorée. Le courant de sortie peut être exprimé par l'équation (3.3). En pratique, les tailles des condensateurs de la pompe de charge sont considérées comme étant les paramètres de conception dominants.

La pompe de charge produit de grandes oscillations en sortie. Dans la structure d'un étage d'une pompe de charge, la tension d'oscillation peut être exprimée par l'équation

(3.4). D'après (3.4), la tension d'oscillation peut être considérablement réduite en augmentant la fréquence des horloges, en changeant les paramètres des transistors ou en utilisant une grande capacité de sortie. Dans l'état stable, on s'attend à ce que la tension d'entrée soit augmentée par l'amplitude du signal d'horloge provenant des étages subséquents, comme exprimé dans l'équation (3.5). Cependant, considérant l'effet des capacités parasites dans le circuit, le gain de tension pourrait être exprimé par l'équation (3.8).

III.3 Amélioration de l'efficacité de puissance

Les capacités parasites, les horloges sans recouvrement, un court temps de charge et décharge, la résistance entre les bornes des capacités, les pertes statiques et dynamiques dans les commutateurs, l'injection de charge et les courants de fuite peuvent tous affecter l'efficacité de puissance des multiplicateurs de tension.

Pour obtenir une meilleure efficacité de puissance, il existe une valeur optimale pour la largeur des commutateurs MOS utilisés dans la pompe de charge. Cependant, en raison de l'impossibilité d'effectuer des changements dynamiques sur la largeur des transistors sur puce, un transistor assez large ayant une fréquence de commutation élevée doit être choisi afin de garantir les niveaux de tension de sortie pour une charge maximale.

Une pompe de charge efficace nécessite de grandes capacités. La valeur des capacités est cependant limitée par les contraintes d'intégration. Ainsi il est critique de minimiser le

nombre et la valeur des condensateurs. De plus, le chevauchement des périodes des signaux d'horloge appliqués aux commutateurs de transfert de charge doit être évité. Ceci nécessite d'utiliser une horloge sans recouvrement (Figure 3.8b).

Une grande amélioration de la conductance des commutateurs de transfert de charge est obtenue si nous utilisons un décalage de niveau pour augmenter l'amplitude des signaux de grille, comme illustré dans la Figure 3.9. Cette solution pourrait aussi augmenter la dissipation de puissance. Pour les basses tensions d'entrée, une basse tension V_{eff} peut dégrader l'efficacité en puissance et la fonctionnalité complète du VM. L'efficacité peut cependant être améliorée en utilisant une pompe de charge auxiliaire qui consiste en une pompe de charge supplémentaire tel qu'illustrée à la Figure 3.10 [61].

III.4 Multiplicateur de tension à plusieurs étages

Le multiplicateur de tension classique à plusieurs étages utilise des étages de multiplication en cascade, comme illustré à la Figure 3.11. Un signal d'horloge commun alimente tous les modules de la chaîne. Ici, la tension de sortie est linéairement proportionnelle au signal d'horloge.

Une nouvelle architecture MSVM a l'avantage d'utiliser la sortie de chaque étage comme tension d'alimentation par l'étage suivant, comme illustré à la Figure 3.12. Pour un multiplicateur de tension de N étages, la tension de sortie peut alors augmenter exponentiellement comme le montre l'équation (3.14). Ce qui est remarquable avec cette

structure originale c'est que la croissance exponentielle est obtenue sans que le nombre de phases requises n'augmente avec le nombre d'étages.

IV Limites de tension des technologies submicroniques

Comme les dimensions des dispositifs sont réduites, l'influence des régions périphériques du canal, c'est-à-dire la source, le drain et les structures d'isolation deviennent significatives. Les caractéristiques des dispositifs de petites dimensions ne sont donc qu'approximativement égales a celles des dispositifs de grandes dimension.

IV.1 Effet de canal court

L'annexe A présente une étude détaillée des effets de canal court et des manières de les gérer. Les effets d'une telle diminution de dimensions sont des changements de la tension de seuil, un manque de fiabilité des oxydes, des couches supplémentaires pour former les drain/source et puit, l'augmentation de résistance de sortie, la modulation de la longueur de canal, la dégradation de la mobilité des porteurs, la saturation de la vitesse des porteurs, la distribution aléatoire des dopants, ainsi que des délais d'intercommunication. De plus, la réduction de la longueur de canal mène à une augmentation indésirable de la résistance de la ligne de la grille.

IV.2 Canal à effet étroit

La largeur du canal a aussi un impact significatif sur les caractéristiques des MOS à faible dimension. Pour des canaux étroits, la charge latérale devient comparable avec la charge directement au-dessous de la grille.

IV.3 Effets des porteurs

Lorsque les dimensions du dispositif et la tension d'alimentation ne sont pas ajustées proportionnellement, le résultat est un champ électrique latéral croissant près du drain. Ce grand champ électrique latéral pousse les porteurs à emmagasiner suffisamment d'énergie pour surmonter la barrière d'interface SiO_2-Si, ce qui par la suite produit des pièges et peut injecter des électrons et des trous dans l'oxyde. Ceci endommage graduellement l'oxyde. Ces dommages peuvent aboutir à un changement des caractéristiques courant tension des MOS (Annexe B).

IV.4 Phénomène de Punch-through

Le punch-through est un mécanisme non destructif qui peut arriver quand l'épaisseur des couches de déplétion pour les jonctions de la source et du drain sont comparables avec la longueur du canal. Ainsi, quand la tension de drain augmente, les régions de déplétion des jonctions P-N de la source et du drain peuvent se toucher. En conséquence, un courant de fuite significatif peut circuler du drain vers la source à travers le substrat. Ce courant est alors mal contrôlé par la grille, parce qu'il n'est plus contraint au canal en

surface. La tension de punch-through inclut aussi la tension nécessaire pour surmonter la barrière Source-Substrat.

La polarisation du substrat a aussi tendance à supprimer le punch-through en augmentant la hauteur de la barrière initiale autour de la jonction de la source. La tension de punch-through pour une jonction brusque peut être exprimée selon l'équation (4.13). Notez que pour un procédé à puit n, le punch-through peut arriver pour des dispositifs parasites latéraux et verticaux.

IV.5 Tensions de claquage

Les dispositifs MOS soumis à un stress de tension sont sujets à différents mécanismes de claquage. Ces mécanismes peuvent impliquer le canal, la jonction et le claquage de l'oxyde. Ces phénomènes peuvent être destructifs ou non destructifs. Le claquage du canal par avalanche arrive quand le dispositif est actif et qu'un champ électrique excessif existe dans le canal. Cela produit des électrons non thermalités qui provoquent un processus d'ionisation menant à la multiplication par avalanche. Ainsi, une augmentation rapide du courant de drain, qui devient indépendant de la tension de la grille, sera observée.

Lorsqu'une jonction est polarisée en inverse, le potentiel à travers les semi-conducteurs augmente tout comme la largeur de la couche de déplétion. La tension maximale de polarisation inverse est limitée par la tension de claquage qui est caractérisée par

l'augmentation rapide du courant en polarisation inverse. Deux mécanismes peuvent causer le claquage, notamment la multiplication par avalanche et l'effet tunnel.

Le claquage de l'oxyde est une dégradation progressive et continue du volume et de l'interface de l'oxyde, suivie par la destruction finale du diélectrique. En conséquence, le claquage est un phénomène local avec un caractère statistique qui dépend de la densité des défauts déjà présents ou pouvant être produits lors du stress de l'oxyde. Sous un grand champ électrique, les dégâts s'introduisent à l'anode et la cathode et s'étendent finalement partout dans le corps du film d'oxyde selon un modèle non uniforme. Quand un nombre critique de défauts est atteint, un chemin conducteur est formé à travers l'oxyde et le claquage de l'oxyde est déclenché [175]. L'annexe C explique le mécanisme de claquage de l'oxyde et de la grille, ainsi que les modèles associés.

V Résultats expérimentaux

Une puce prototype a été conçue et fabriquée en utilisant la technologie CMOS 0.18 µm à puit n de la TSMC. Cette puce contient des transistors PMOS et NMOS de différentes tailles fabriqués en utilisant les diverses règles disponibles. Tous les transistors, même ceux de très grandes tailles, ont été faits comme des dispositifs monolithiques. Un zone de garde dans le puit n a été utilisé pour chaque transistor, servant comme anneau de garde. Un double anneau de plots a été utilisé afin d'économiser la superficie du dé, tout en ayant un accès individuel à autant de terminaux que possible. Le dessin des masques a

été fait manuellement sous l'outil Virtuoso de Cadence. Afin d'obtenir des résultats fiables en mesurant un nombre limité d'échantillons, un protocole systématique a été appliqué.

Nos mesures confirment que la distribution de porteurs dans le canal, dépendant des paramètres du procède et de la différence de potentiel entre la grille et le substrat, a un impact significatif sur les caractéristiques du dispositif. Nous avons découvert que la structure d'essai a un impact remarquable sur l'exactitude et la validité des résultats de mesure.

Pour quelques mesures, nous avons examiné quelques configurations possibles. Il a été trouvé que le claquage de l'oxyde de grille est indépendant de la géométrie du dispositif, tandis que le claquage entre les gilles est fortement dépendant de la surface du canal. Il a aussi été trouvé que le claquage de l'oxyde sur les côtés du drain et de la source survient à des tensions inférieures à celles mesurées à la surface du canal.

En raison des contraintes des puces multi projet, le nombre de dispositifs disponibles n'était pas suffisant pour conduire des essais de fiabilité. L'impact de facteurs comme le temps et la température sur la durée de vie des dispositifs, ainsi que l'usure, n'ont pas été examinés. Finalement, nos résultats montrent que par des techniques de conception circuit appropriées, des dispositifs MOS pourraient fonctionner à des niveaux de tension jusqu'à deux fois plus grands que la tension d'alimentation nominale du procédé.

List of Contents

Dedication ..... **iv**

Acknowledgements ..... **v**

Résumé ..... **vii**

Abstract ..... **ix**

Condensé en français ..... **xi**

List of Figures ..... **xxix**

List of Tables ..... **xxxii**

List of Abbreviations ..... **xxxiii**

List of Symbols ..... **xxxv**

List of Appendixes ..... **xxxv**

List of Contents ..... **xxv**

Chapter 1 Introduction **1**

1.1 Motivation 1

1.2 Research goals 3

1.3 Thesis outline 4

Chapter 2 Power conversion chain for electronic implant **6**

2.1 Implant power-up techniques 6

2.2 Constraints and limitations 8

2.2.1 Variation in load current 9

2.2.2 Variation in load voltage 10

2.2.3 Variation in input voltage 11

2.2.4 Circuit design concerns 12

2.3 Conventional PCC's architecture 13

2.4 Smart Synchronous Rectifier 15

2.4.1 Synchronous rectifiers 15

2.4.2 Smart synchronous rectifiers 17

2.4.3 MOS implementation for SSR 17

2.4.4 New implementation for SSR 19

2.5 Smart synchronous rectifier versus classical diode rectifier 19
2.6 New PCC architectures based on SSR 20
2.6.1 Distributed topology 21
2.6.2 Monolithic topology 23
2.7 Summary 23
Chapter 3 High-efficiency voltage multiplier 25
3.1 Introduction 25
3.2 Charge pump 26
3.2.1 Concept and characteristics 27
3.2.2 Charge pump types 29
3.3 Single-stage voltage multiplier 34
3.3.1 MOS-based charge pump 34
3.3.2 Charge transfer module 35
3.3.3 Complete scheme 36
3.4 Voltage multiplier characteristics 37
3.4.1 Output current 38
3.4.2 Output ripples 39
3.4.3 Voltage gain 39
3.5 Power efficiency improvement 40
3.5.1 Switching frequency 41
3.5.2 Integrated capacitor 41
3.5.3 Non-overlapping clock 42
3.6 Low-voltage application 45
3.7 Multi-stage voltage multiplier 46
3.7.1 New architecture 48
3.8 Summary 49
Chapter 4 Reliability challenges of CMOS under sub-micron regime 51
4.1 Short channel effects 51
4.2 Narrow-channel effects 52

4.3 Subthreshold and leakage currents 54
4.3.1 Subthreshold current 54
4.3.2 Junction leakages 55
4.3.3 Gate leakage current 56
4.3.4 Latch-up 57
4.4 Hot carriers effects 59
4.5 Punch-through 60
4.5.1 Punch-through voltage and current 63
4.5.2 Punch-through improvement techniques 65
4.6 Breakdown voltages 65
4.6.1 Channel avalanche breakdown 65
4.6.2 Junction breakdown 66
4.6.3 Dielectric breakdown 67
4.7 Stress-induced measurement techniques 73
4.8 Summary 74
Chapter 5 Quantitative, simulation and measurement results 76
5.1 Quantitative results for power conversion chains 76
5.2 Simulation results for multi-stage voltage multiplier 80
5.2.1 Impact of charge pump capacitors 81
5.2.2 Impact of clock frequency 82
5.2.3 Impact of transistors dimensions 84
5.2.4 Impact of clock overlapping 84
5.2.5 Multi-stage voltage multiplier 85
5.3 Voltage limits; Experimental results 86
5.3.1 Test protocol 87
5.3.2 Test structures 90
5.3.3 Prototype chip 108
5.4 Summary 111

Chapter 6 Conclusions 113
6.1 Summary and discussion 113
6.2 Directions for future work 116
References 119

List of Figures

Figure 2.1: Block diagram of a conventional PCC 14
Figure 2.2: Smart Synchronous Rectifier (Half-Wave) 17
Figure 2.3: A simple block diagram for a SSR 19
Figure 2.4: The scheme of a distributed PCC 21
Figure 2.5: Block diagram of a monolithic PCC 23
Figure 3.1: Charge Pump General Overview 27
Figure 3.2: Cockcroft and Watson Charge Pump 29
Figure 3.3 : Dickson Charge Pump 30
Figure 3.4 : Charge pump using Static CTSs 32
Figure 3.5 : Charge pump using Dynamic CTSs 33
Figure 3.6 : MOS Implemented Charge Pump 34
Figure 3.7: Dynamic Gate Biasing 36
Figure 3.8: Classical Single Stage Charge Pump 37
Figure 3.9: Schematic of a level shifter 44
Figure 3.10 : High Efficiency Voltage Multiplier for Low Voltage Applications 45
Figure 3.11 : Classical topology for a Multi-Stage Voltage Multiplier 46
Figure 3.12: The scheme of an improved MSVM 48
Figure 4.1: Narrow channel effect 52
Figure 4.2 : Threshold voltage variation versus channel width 53
Figure 4.3 : CMOS device cross-section and parasitics responsible for latch-up 58
Figure 4.4: Lateral electric field in saturation region 59
Figure 4.5: PMOS transistor cross-section and parasitics 60
Figure 4.6: Logarithmic plot of V_{Dmax} versus L_{eff} 61
Figure 4.7 : Illustration of Punch-through 62
Figure 4.8 : Visualization of oxide breakdown failure 69
Figure 4.9 : Typical Weibull plot of the time to breakdown for MOS capacitors 70

Figure 5.1: Power efficiency vs input voltage for the 2-stage conventional architecture. 79
Figure 5.2: The schematic of a single stage voltage doubler 81
Figure 5.3: Output voltage vs charge pump capacitor size 82
Figure 5.4: Characteristics of the single stage charge pump vs clock frequency 83
Figure 5.5: Power efficiency versus the charge pump switch width 84
Figure 5.6: 5-Stage Conventional Voltage Multiplier 85
Figure 5.7: The output voltage of 5-stage voltage multiplier 86
Figure 5.8: Measurement procedure flow chart 89
Figure 5.9: Cross-section of PMOS transistor and relative parasitics 90
Figure 5.10: The cross-section and schematic of ESDR protection 91
Figure 5.11: Different setups for P_{sub}-N_{diff} junction reverse breakdown 92
Figure 5.12: Test setup for P_{sub}-N_{well} junction reverse breakdown voltage 94
Figure 5.13: Test setup for N_{well}-P_{diff} junction reverse breakdown voltage 95
Figure 5.14: Test setup for lateral punch-through voltage in NMOS 97
Figure 5.15: Test setup for lateral punch-through voltage in PMOS 99
Figure 5.16: Test setup for vertical punch-through voltage in PMOS 100
Figure 5.17: Test setup for gate oxide breakdown (edge) in NMOS 102
Figure 5.18: Test setup for gate oxide breakdown (surface) in NMOS 104
Figure 5.19: Test setup for gate oxide breakdown (surface) in PMOS 106
Figure 5.20: The view of the prototype chip 109
Figure 5.21: The specimen schematic of the zap zones 110
Figure A- 1: Plot of V_{DD}, V_T and t_{OX} trends versus L for MOS technologies 149
Figure A-2: Charge-sharing effect for short-channel devices 151
Figure A-3: Depletion layer with a large drain bias 152
Figure A-4: Drain currents for short- and long-channel devices 153
Figure A-5: Surface mobility degradation versus electric field 155
Figure A-6: Drift Velocity versus Electric Field 156
Figure A-7: Threshold voltage versus substrate doping density 158
Figure A-8: Threshold voltage-related short-channel effect 159

Figure A-9: Threshold dependence on the channel length 161
Figure A-10: Well Engineering representation 162
Figure A-11: Threshold dependence on drain voltage 164
Figure A-12: Cross-section of Lightly Doped Drain profile 165
Figure B-1: The electric field in vicinity of Drain 170
Figure B-2: The energy Diagram showing barrier heights 170
Figure B-3: Visualization of carrier multiplication in NMOS 172
Figure B-4: Quantitative comparison between HCI mechanisms in NMOS 173
Figure B-5: I-V characteristics for fresh and degraded MOS 175
Figure B-6: The LDD structure cross section 179
Figure B-7: Electric field distribution in conventional and LDD structures 180
Figure C-1: Plot of I-V characteristics for soft and hard breakdowns 184

List of Tables

Table 4.1: The specifications of electrical stress methods 74
Table 5.1: The assumption and circuit parameters for analytical study 77
Table 5.2: Input current and power equations for various PCC architectures 77
Table 5.3: Required voltage and current for PCC architectures 78
Table 5.4: Power and efficiency of various PCC architectures 79
Table 5.5: ESDR Reverse Breakdown Voltage 91
Table 5.6: The P_{sub}-N_{diff} reverse breakdown vs channel length for different setups 93
Table 5.7: The P_{sub}-N_{well} reverse breakdown voltage vs channel length 95
Table 5.8: The N_{well}-P_{diff} reverse breakdown voltage vs channel length 96
Table 5.9: Measured voltages in lateral punch-through setup for PMOS 100
Table 5.10: Oxide breakdown voltage for NMOS vs channel length 102
Table 5.11: The test structures of oxide breakdown for PMOS 103
Table 5.12: The gate oxide breakdown (surface) vs channel length for NMOS 105
Table 5.13: Oxide breakdown voltage (surface) for PMOSs 107

List of Abbreviations

AM	Amplitude Modulation
ASK	Amplitude Shift Keying
BD	Breakdown
BJT	Bipolar Junction Transistor
CDF	Cumulative Distribution Function
CHE	Channel Hot-Electron
CTS	Charge Transfer Switch
DAHC	Drain Avalanche Hot-Carrier
DC	Direct Current
DIBL	Drain-Induced Barrier Lowering
DR	Diode Rectifier
EDT	Edge Direct Tunneling
EI	Electronic Implant
ESD	Electro-Static Discharge
ESDR	Electro-Static Discharge with Resistor
ETC	Electrode-Tissue Contact
FES	Functional Electrical Stimulation
HBD	Hard Breakdown
HCI	Hot-Carrier Induced
IC	Integrated Circuit

LDD	Lightly Doped Drain
MCS	Multi-Channel Stimulator
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSVM	Multi-Stage Voltage Multiplier
NTS	Neutral Trapping Site
NMOS	N-channel Metal Oxide Semiconductor
PCC	Power Conversion Chain
PPMOS	P-channel Metal Oxide Semiconductor
RF	Radio Frequency
SBD	Soft Breakdown
SCR	Silicon-Controlled Rectifier
SDE	Source-Drain Extension
SGHE	Secondary Generated Hot-Electron
SHE	Substrate Hot-Electron
SOI	Silicon On Insulator
SR	Synchronous Rectifier
SSR	Smart Synchronous Rectifier
TDDB	Time Dependent Dielectric Breakdown
VLSI	Very Large Scale Integration
VM	Voltage Multiplier
VR	Voltage Regulator

List of Symbols

α	Charge pump capacitance to stray capacitance ratio
β	Shape parameter in Weibull distribution function
γ	Body-effect constant of MOSFET
μ_{eff}	Effective carrier mobility
μn	Electron mobility
μs	Carrier mobility at surface
μ_0	Low-field carrier mobility
λ	Channel length modulation parameter
η	Scale parameter in Weibull distribution function
η_{MSVM}	Power efficiency of MSVM
$\eta_{Overall}$	Overall power efficiency of PCC
η_{VR}	Power efficiency of VR
ε_S	Semiconductor permittivity
ϕ_F	Built-in Fermi potential
a	impurity gradient
A_j	Junction area
C	Charge pump capacitance
C'	Auxiliary charge pump capacitance
C_g	Gate capacitance

C_{OUT}	Output capacitance
C_{OX}	Gate oxide capacitance per unit area
C_S	Stray capacitance
E_{bd}	Electric field to breakdown
E_C	Critical electrical field
E_g	Difference in energy between conduction and valance bands
E_L	Energy consumed by load
E_m	Peak lateral electric field
E_{OX}	Electrical field across gate oxide
E_S	Energy delivered by source
f	Switching frequency
F(x)	Cumulative failure rate function
F_S	Charge sharing factor
g_{ds}	Source-drain small-signal Conductance of MOSFET
I_{FN}	Fowler-Nordheim tunneling current
I_{lk}	Leakage current
I_{OUT}	Output current
k	Boltzmann's Constant
l	Effective lateral electric field length
L	Channel length of MOSFET
L_{eff}	Effective channel length of MOSFET
n	Junction shape factor

n_i	Intrinsic concentration of carriers in undoped silicon
N	Number of cascaded stages of MSVM
N_A	Doping concentration in Channel
N_B	Background doping of lightly doped side of P-N junction
N_C	Density of states in conduction band
N_{diff}	N-type diffusion region
N_{OX}	Effective ion density of charge trapped in thin oxide
N_V	Density of sates in valance band
N_{well}	N-type well region
N_{Sub}	Substrate doping concentration of MOSFET
P_{Core}	Required power for Core
P_{diff}	P-type diffusion region
P_{DRO}	Power loss of diode rectifier
P_I	Input power to PCC
P_{MCS}	Required power for MCS
P_{sub}	P-type substrate region
q	Electron charge
Q_{bd}	Charge to breakdown
Q_{Ch}	Transferred charges by charge pump
r_{ds}	Output resistance of MOSFET
R_L	Load resistance
R_{ON}	Dynamic resistance of MOSFET

R_S	Source resistance
S	Subthreshold slope
t_{bd}	Time to breakdown
t_{OX}	Gate oxide thickness
T	Absolute temperature
v_{max}	Maximum drift velocity
V_γ	Diode forward-bias voltage drop
V_{bi}	Built-in voltage across junction
V_{eff}	Effective gate-to-source voltage of MOSFET
V_{BD}	Breakdown voltage
V_{Dmax}	Maximum drain voltage
V_{DD}	Positive power supply voltage
V_{DRO}	Output voltage of diode rectifier
V_{DS}	Drain-to-source voltage of MOSFET
V_{GS}	Gate-to-source voltage of MOSFET
V_{MSVMI}	Input voltage to MSVM
V_{MSVMO}	Output voltage of MSVM
V_{OX}	Voltage across the gate oxide
V_{PT}	Punch-through voltage of MOSFET
V_R	Ripple voltage
V_{SB}	Source-to-bulk voltage of MOSFET
V_{SS}	Negative power supply voltage

V_{SSRO}	Output voltage of SSR
V_T	Threshold voltage of MOSFET
V_{TO}	Threshold voltage shift
W	Channel width of MOSFET
W_m	Depletion layer depth
X_d	Thickness of the depletion region
X_{dm}	Depletion depth in channel of MOSFET
X_j	Junction depth

List of Appendixes

Appendix A.....149

Appendix B.....169

Appendix C.....182

Chapter 1

Introduction

1.1 Motivation

Since the first implantable pacemaker, exciting progress has been made in the development of a variety of implantable devices that address many different illnesses. For example, cardiac pacemakers, cochlear implants, bladder controllers, bone growth systems and nerve stimulators of various kinds have been demonstrated and have steadily improved over time. An entire industry has been created, providing meaningful employment to thousands of scientists, engineers, businessmen, and workers. Hundreds of thousands of lives have been saved by these devices, and the quality and duration of life has improved for many patients [69]. For instance, the first practical external pacemaker was invented in 1952 [218]. Such a device was approximately the size of a table radio of the time and was powered by electrical connection to 110 VAC line voltage. The treatment was painful and damaged the skin. Later, a hand-held external device was developed [106]. It was battery operated and used myocardial leads, eliminating the pain and burning associated to the ancient device.

With the advent of the transistor, the possibility of building a totally implantable device came true and the first experimental implantable pacemaker was placed in an animal [68]. This led to the first successful human implant [27]. The early units used discrete

components. They were powered by a battery and encapsulated in an epoxy compound. Many problems needed to be addressed in those early years. One area that required much research concerned the electrode materials and attaching them to the organ or nerve. The most serious remaining drawbacks and limitations to implant longevity and reliability was the power source. The first batteries were suffering from hydrogen gas generation, relatively quick self-discharge, low energy density and, failure due to the penetration of the separator by dendrites [69]. A rechargeable pacemaker was next developed using a transcutaneous recharging technology and two-way telemetry [62].

The past two decades saw further significant improvements in implant technology. The development of the printed circuit board, hybrid circuitry, and electronic microchips made possible the design of very small implants with an amazing array of features. Programmability, the ability to record various clinical parameters from inside human body and the use of telemetry to access the state of stimulation sites and broadcasting them back to the clinicians as well as multi-channel stimulation are some very common features of today implants. The future appears even more exciting, with the prospect of implantable devices and prostheses aiding in the recovery of body functions and the improvement in quality of life , as well as the saving of lives [69]. Although new sub-micron CMOS technologies provide higher performance in terms of higher speed, lower power consumption and reduced area, they also suffer from lower nominal supply voltage. For some applications, such as biomedical, the need for a given high supply voltage calls for techniques to boost supply voltage. This requirement sometimes crosses

the process reliability limits.

Hence, the solution might be using either hybrid processes, where combinations of different technologies are possible or, develop design methods such that the circuit functions within the limits of conventional CMOS technologies. The former calls for costly processes, while the latter necessitates circuit elements such as voltage boosters. The second option that produce circuits operating at voltage higher than nominal value raise questions with respect to reliability. The use of new technologies could also be beneficial if it allows producing fully integrated implants while having higher degree of power efficiency. It is worthy to notice that the increase in power efficiency is not only an issue at device level, but also an issue for further study at system and architecture level.

1.2 Research goals

The multiple goals of this work are related to the development of high efficiency multi-stage voltage multiplier capable of boosting an input voltage (from 1 V to 10 V) and of delivering it at the output terminal in an efficient manner. The design targets full integration and must provide a basis for reliable long term and safe application to implantable biostimulators.

1.3 Thesis outline

The development of high efficiency power conversion chains for an electronic biomedical implant shall be the subject of this work. The said chain is using multi-stage voltage multiplier modules realized in CMOS technology. The presentation in this research will be organized according to three distinct levels of hierarchy. The first of the three shall be an investigation at the system level of power conversion chain architecture where a conventional structure is examined and new architectures will be proposed. The second shall be an investigation at a circuit level, where the design of a high efficiency multi-stage voltage multiplier and associated circuitries will be developed. The third shall be an investigation at a device level, where MOS transistors are characterized under stress condition.

Following this outline, Chapter 2 will describe the architecture of the power conversion chain for biomedical implants. The impact of architecture on the overall power efficiency will be examined and the theoretical background describing the efficiency for a conventional structure will be provided. New architectures based on synchronous rectifiers will also be developed. They can result in efficiency improvements and facilitate integration.

Chapter 3 will describe the structure and implementation of a single-stage voltage doubler realized in CMOS 0.35 μm process. The impact of circuit parameters on the overall efficiency will be represented. The structure of a multi-stage voltage multiplier

will then be investigated and a new architecture will be introduced. It leads to a significant improvement in the overall voltage boosting factor.

Chapter 4 addresses the major mechanisms involved that influence MOS transistors characteristics under voltage stress. The fundamental electronic physics issues will be presented and the effect of hot carrier, short channel effects and breakdown phenomenon will be explained.

Chapter 5 presents the quantitative results of our study over different power conversion chain architectures, and simulations of multi-stage voltage multipliers. Finally, the strategies and the test structures used in order to characterize the MOS transistors from different type, size and terminal arrangements under voltage stress will be addressed, and some of the capabilities and limitations of these setups will be demonstrated. Device operation will be described, and a discussion of measured values and possible hypothesis with respect to breakdown nodes will be formulated and analyzed. The specifications of an implemented prototype chip will also be provided at the end of this chapter.

As a result of this work, the impact of architecture, circuit elements and design parameters will have been thoroughly investigated, and the characteristics of MOS technologies under voltage stress condition for new sub-micron processes will have been addressed. The final chapter shall provide conclusions that can be drawn from this work. We will also discuss some future directions for circuit design in CMOS technology.

Chapter 2

Power conversion chain for electronic implant

During the past two decades, sensors and stimulators operating inside the body have generated a lot of interest to monitor human organs behavior and/or to recuperate their functional activities. Advances in microelectronics have led to the development of powerful miniaturized devices, among them we find various implantable artificial organs, sensors, and Functional Electrical Stimulators (FES). These devices have recently been intensively used in many disease circumstances such as cardiac pacemakers, cochlear implants and bladder controllers. Despite the success in designing such devices, feeding them with a reliable and efficient power source remains one of the main issues that slows down progress towards building suitable miniaturized systems.

2.1 Implant power-up techniques

Procuring required energy to power up an Electronic Implant (EI) in an efficient way is a significant implementation challenge. Numerous alternatives are available for supplying power to EIs. In early implementations, power was delivered to the implants by wires passing through skin [106,218]. Hard-wired (percutaneous) stimulation systems are now considered obsolete, because they often cause infection at the points where wires break the skin, risking the safety of the patient. They also impose limitations to free movements, which increase the chance of lead wire failure [58,103,156]. In fact, these

factors remain the major drawbacks of this method, even after developing better understanding of basic electrochemistry of electrode/body interactions, further advances in electrode technology and development of alternate encapsulant materials, and refinements in electrode terminations in order to achieve better attachment of the electrode to the tissue [69].

A second approach to feed power to an EI is to include embedded batteries that are not ideal power sources for long-term use [27,62,91]. Indeed, their limited lifetime and stored energy requires frequent replacement or recharging, and their considerable size in comparison with active devices are main concerns limiting their use. Their chemical stability and probable current leakage also pose hazards for safety of live tissues and reliability of electronics. The remaining alternatives are based on wireless techniques that have none of the above listed limitations. They allow patient mobility and reduce risk of infection. Nowadays, most implant designs favor Radio-Frequency (RF) inductive links where an electromagnetic RF signal is used to transmit data and power to the implant [10,64,159]. The required energy is provided by an external and high efficiency source. The majority of available prosthetic power supplies are based on Amplitude Modulation (AM) transmission. The collected high-frequency signal (carrier) is rectified to power up the EI.

Using RF inductive link techniques, the EI lifetime is no longer limited by the stored energy, but rather by the implant electronics and body reaction. It also keeps the risk of

skin damage at a very low level and makes it possible to have bi-directional communication and energy transfer simultaneously. However, this technique lacks some characteristics such as high-energy-transfer efficiency and wide bandwidth. It also suffers from transversal, orthogonal, and other inductance alignments [57]. In fact, even though these modern power transmission techniques could provide fairly large power, biological considerations for long-term human safety impose a limit of 10 mW/cm^2 for the maximum power of transmitted RF signal through the skin [11].

In order to remove some of these restrictions, other transcutaneous power transmission techniques have been proposed. For instance, a transcutaneous optical power converter has been recently introduced. It consists of solar cells receiving light from an external light source [181]. The light source could be either a halogen-lamp- or a laser-diode-illustrating skin surface. This technique does not give the expected performances but is still employed in very restricted cases.

Therefore, configuring a high efficiency Power Conversion Chain (PCC) to feed EIs remains an area of interest. Also the need for integrating both power and stimulation circuitries on a single chip is increasingly desirable.

2.2 Constraints and limitations

Ideally, a PCC captures all the power received at its input terminals and delivers it to the load located at its output terminals. Its power efficiency is defined as the ratio of the

output to the input powers. Indeed, a part of the input power is dissipated in the circuit, because no existing circuit has ideal characteristics. This part deals with characterizing and optimizing that efficiency and therefore, accounts for the parameters which may affect it. There are several constraints and limitations behind the parameters involved in a multi-channel FES application that are described in the following sections.

2.2.1 Variation in load current

The power consumed by an implant splits in two parts, the core and the load. The implant core includes all devices needed for biasing, control, generation of complex stimuli, and testing issues. A major load of an implant is its stimuli generator. With technology evolution, the power required to operate the core is small and decreasing, while the power to stimulate a sensitive area is fixed and the number of stimulation sites tends to grow with the sophistication of the implant. The second component tends to dominate power requirements.

FESs are generally Multi-Channel Stimulators (MCSs). For instance, a recently proposed cortical stimulator comprises a matrix of 4 modules stimulating 8 channels each, to stimulate 1024 possible sites [191]. That many channels are required for effective cortical stimulation. The maximum load current grows in proportion with the number of channels, and the average current grows with the number of stimulated sites.

Effective stimulation requires some minimal charge transfer (threshold charge per phase) to be injected in the tissue, which differs for various tissues and changes from a stimulation site to another. For instance, in the case of cortical stimulation, this threshold is reported to be 15 nC at a frequency of 250 Hz [86,148]. This charge is injected by the current flowing through the contacts during the stimulation phase and is proportional to the said current and the stimulation period. To perform a multi-channel stimulation at a sufficiently fast rate (>50 Hz), the commonly used stimulation current is as low as 10 μA per channel [185].

In the case of cortical stimulation, the stimulation sites may present different interfacing conditions. Contacts are also known to age non-homogenously, as they gradually get surrounded by encapsulating tissues. Thus, in order to obtain the required stimulation efficiency, an increase of stimulation currents to values as high as 100 μA may be required [185]. Therefore, the need for a wide range of stimulation currents is predictable. For instance, assuming a 25-channel stimulator, the current may vary from 0.25 mA to 2.5 mA.

2.2.2 Variation in load voltage

The effective Electrode-Tissue Contact (ETC) area for passing the stimulation current varies from one site to another, which results in different effective impedances of the stimulation channels [86]. Contact aging makes this even worse. To our knowledge, the equivalent retina tissue impedance was found to be on the order of 10 kΩ [86], while this

value is 100 kΩ for cortex stimulations [148]. Therefore, to produce the specified range of stimulation currents, in the worst case, the required voltage is as high as 6 V for retina stimulation, and about 10 V for cortical stimulation. Always supplying stimulation current from a power supply set to the highest required voltage in worst case conditions can become very inefficient, since the voltage not needed by the load is simply dissipated in the transistor driving it. This leads to considering innovative solutions such as dynamic power supply adjustment and voltage multiplication discussed in chapter 3.

2.2.3 Variation in input voltage

For a given power transmitted through skin, the value of the received power is affected by the distance and relative orientation of the remote transmitter and the implant. Moreover, taking advantage of modulation techniques such as ASK to transmit data and power simultaneously may cause significant variations in the magnitude of transmitted RF signals. Therefore, we can expect to have considerable input signal variations over time. Since the load part is independent from the feed part, the PCC must be configured to receive adequate power during its operation. To keep the overall PCC efficiency in a high enough range, it is essential to adjust the transmitted power, which imposes employing a feedback path. Therefore, in absence of highly effective feedback adjusting transmitted power, the power conversion chain can become fairly inefficient. Indeed, excess power will simply be dissipated in the implant. An analysis of this phenomenon is presented in the following.

2.2.4 Circuit design concerns

As supply voltages are scaled down, the efficiency of charge pumps – used in voltage multiplier modules - are severely degraded due to threshold voltage drop of pass transistors, and the voltage gain of pumping stages closer to the output is further degraded by the body-effect of MOS transistors. Therefore, complex circuit design techniques are required to overcome these problems. Several authors have investigated the design of body-effect-free, high performance, and low voltage charge pump based circuits [36,61,115,152,158,195,213].

Moreover, the required range of stimulation currents and observed load impedance per channel dictate adopting a highly flexible power conversion chain architecture. The stated requirements can be met by employing an adaptive Multi-Stage Voltage Multiplier (MSVM) module, composed of a few upward DC-DC voltage converters as its basic building block. The number of stages could be fixed, based on the specific input voltage, while the maximum output voltage is determined by the required maximum voltage across the various ETCs.

Finally, integrating the whole implant could improve its performance a great deal and may facilitate its connection to the tissue, but it also imposes some limitations and challenges. Among them, using voltages higher than the nominal values supported by the technology may greatly accelerate aging phenomena such as Hot Carrier Induced (HCI), which affect MOS characteristics and cause degradations in transconductance, a shift in

the threshold voltage, and a decrease in the drain current carrying capability and undesirable junction and oxide breakdowns. This leads to long term device reliability problems [99]. The significant challenges posed by higher than nominal supply voltages will be treated later on.

2.3 Conventional PCC's architecture

The architecture of the power conversion chain in an electronic implant has a strong impact on its performance, efficiency and reliability when designed to meet the safety limitations for human body. The proper architecture for an electronic implant must also be flexible enough to meet the design main goals. In order of importance, the main goals are: (1) To drive the high impedance of tissue stimulation and/or monitoring sites, (2) To provide biologically safe power transmission, (3) To handle simultaneous multi-channel stimulation, (4) To facilitate the stimulator integration on a single die and, (5) To provide high power efficiency. In the framework of deep sub-micron technologies, the nominal supply voltage is reducing to even less than 1 V, while FES applications still require higher voltages. Therefore, there is a demand for a voltage boosting module that can deliver high voltage to the MCS. Such a module should also be capable of adaptive output selection in order to provide adequate voltage in proportion with stimuli generator voltage requirements.

The conventional architecture of a PCC is shown in Figure 2.1. It consists of a diode rectifier (DR) and a voltage regulator (VR), in series with the load, which includes a

MCS as well as the core of the implant. Here, a Multi-Stage Voltage Multiplier (MSVM) module is inserted. The number of stages in a MSVM is adjusted so that it could generate the highest voltage required for stimulation [5, 84,168].

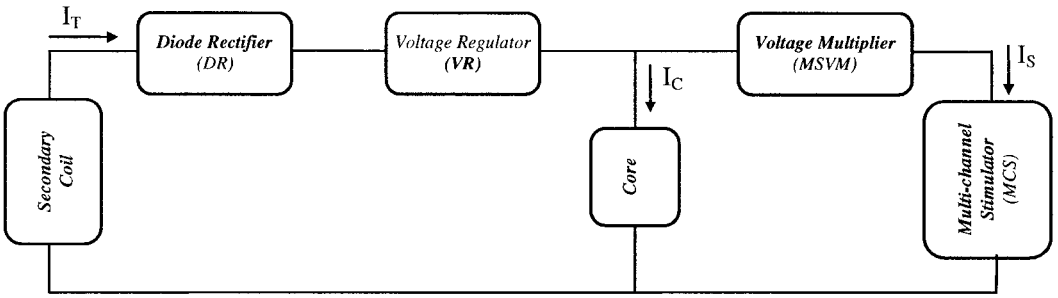


Figure 2.1: Block diagram of a conventional PCC

Considering the limited efficiency of the MSVM, VR and DR, a lot of power will be dissipated in the PCC. Recall that power consumption within the DR is proportional to the product of its inherent forward-bias voltage drop ($V\gamma$) and the forward current. The typical value for $V\gamma$ of a silicon diode is about 700 mV. Assuming V_I and I_T as input voltage and current to the secondary coil, power loss (P_{DRO}) and output voltage (V_{DRO}) of the DR is calculated with equation (2.1).

$$P_{DRO} = V_{DRO} \times I_T \tag{2.1}$$

Where $$V_{DRO} = V_I - 0.7$$

According to this equation, constant voltage drop across the DR results in a significant power loss. It affects the overall power efficiency of PCC and decreases the delivered voltage to the following modules. This equation also implicitly assumes the efficiency is controlled by the peak voltages seen before the rectifier.

In this topology, the current and required input power are determined by the following equations:

$$I_T = \left(\frac{I_S}{\eta_{MSVM}} \times \frac{V_{MSVMO}}{V_{MSVMI}} \right) + I_C \tag{2.2}$$

$$P_I = \left(\frac{P_{MCS}}{\eta_{MSVM} \times \eta_{VR}} + \frac{P_{Core}}{\eta_{VR}} \right) + V_\gamma \times I_T \tag{2.3}$$

Where η_{MSVM}, η_{VR}, P_{MCS},V_{MSVMO}, V_{MSVMI} and P_{Core}, are the power efficiency of MSVM and VR, required power for MCS, output and input voltage of MSVM and required power for core, respectively.

New sub-micron integrated circuit technologies require low supply voltages, which are not much larger than the drop of a DR. Therefore, the voltage drop and power consumption related to a DR is a first order consideration. Besides, DR is commonly implemented by using discrete off-chip diodes, which goes against the objective of a fully integrated implant. Moreover, the significant constant voltage drop across DR requires multiple voltage multiplier stages in MSVM, which also results in lower overall power efficiency.

2.4 Smart Synchronous Rectifier

2.4.1 Synchronous rectifiers

In low DC output voltage PCCs, it is quite difficult to achieve high power efficiencies

due to the power loss in the diode rectifiers. Thus, substituting those devices with other rectifiers that have lower voltage drop would be significant. Schottky diodes that exhibit lower drops are not available at low power as discrete components [18]. Currently, the most effective way to solve this problem is to use Synchronous Rectifiers (SR). Recent studies have confirmed that using SR is quite advantageous in comparison with Schottky diodes [19].

The concept of SR was introduced for amplitude detection applications [144], and was improved for high speed and high precision applications [135,164]. A synchronous rectifier is an active device that is driven ON when the applied voltage would normally cause diode conduction, and turned OFF when a reverse voltage is applied. However, SRs are not constrained by the diode constant voltage drop. Their use opens up new possibilities with respect to the architecture of PCCs. Power loss in SRs is composed of the switching and conduction losses of the active device. In case of MOSFET transistors, switching losses are proportional to gate parasitic capacitances, the square of gate voltage and switching frequency, while conduction loss is the product of the square of the instantaneous current by the R_{ON}. Considering the application related low switching frequency, and parasitic capacitances for new sub-micron integrated circuit technologies, one can ignore switching loss in comparison with conduction loss. Technically, SRs were grouped into three categories, namely the self-driven SRs, the externally driven SRs and the smart SRs. Among them, the last one has the best performance on timing precision and system simplicity. In externally-driven versions, the gate-drive signals for SRs are

synchronized with the signals of the primary side. Self-driven SRs, unlike the latter, are driven by the voltage derived directly from the secondary winding. A smart SR is self-driven and behaves like a diode according to its external bias conditions [105,136].

2.4.2 Smart synchronous rectifiers

A Smart Synchronous Rectifier combines the behavior of a SR with the possibility of controlling the conduction angle of the said device. Recall that MOSFET transistors perform as voltage-controlled current sources. Thus, they can be used as rectifiers if suitable control voltage pulses are applied to their gate terminal.

2.4.3 MOS implementation for SSR

A MOS-based implementation for the SSR is presented in Figure 2.2, where all MOS transistors are N-channels [105,136].

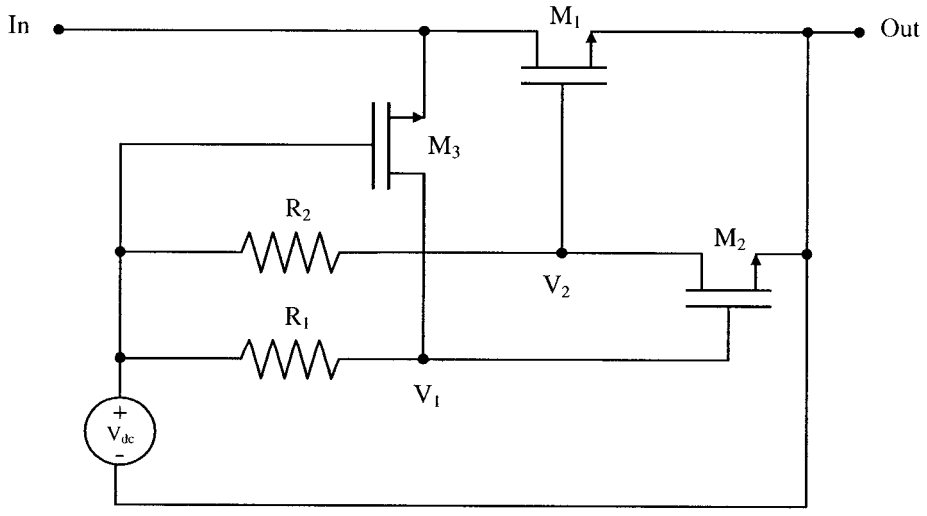


Figure 2.2: Smart Synchronous Rectifier (Half-Wave)

The transistor M_1 is the main transistor for current conduction towards the load, while M_2 and M_3 are parts of its control circuitry. The circuit functions as a half-wave rectifier and therefore has two modes of operation: blocking and conducting.

- **Blocking mode ($V_{DS1} > 0$) :**

One can easily obtain equation (2.4) as the essential condition for M_3 to conduct.

$$V_{GS3} = V_{dc} - V_{DS1} > V_{T3} \tag{2.4}$$

Therefore, if V_{dc} is set equal to V_{T3}, implies that any positive V_{DS1} will make M_3 turned off. Node V_1 will have a voltage close to V_{dc} ($V_{dc} \geq V_{T2}$) and M_2 is turned on. When this happens, M_1 gate voltage will be pulled down to a very low level and, M_1 is not turned on. In this case, the circuit is blocking the current path from input to output terminal.

- **Conducting mode ($V_{DS1} < 0$) :**

When V_{DS1} is negative, as per equation (2.4), M_3 is turned on, which creates a conduction path from node V_1 to the external terminal (In). Then, the voltage of node V_1 drops. When $V_1 < V_{T2}$, transistor M_2 turns off and the voltage at node V_2 rises accordingly. This forces M_1 to conduct.

Therefore, one can tune the conduction and blocking intervals using variable V_{dc}. However, because of multi feedback paths involved in the circuit, the amount of such tuning is extremely limited. This could be a severe problem for transcutaneously powered PCCs where the magnitude of the input RF signal is varying over time significantly.

2.4.4 New implementation for SSR

A smart enough SR should have the capability to adjust the conduction period based on the period of the input signal, and the requirement of the next module in the PCC. The proper command for such action could be obtained by comparing samples of those signals. A feedback from output terminal to the SSR can make this circuit more stable and help to manage the power delivered to the output. A secondary feedback from the SSR to the external power amplifier of the inductive link in the primary circuitry may be employed to control the power transmitted by the remote transmitter. A simple block diagram of such a device is illustrated in Figure 2.3. The bias and control module generates the proper signal to control the conduction angle of the main switch.

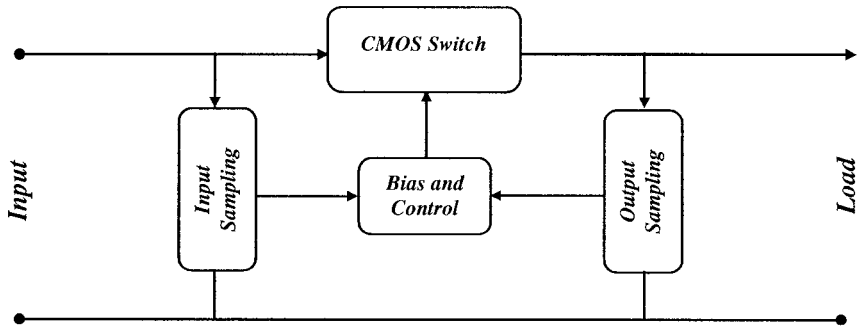


Figure 2.3: A simple block diagram for a SSR

2.5 Smart synchronous rectifier versus classical diode rectifier

In a SSR, ignoring switching losses of MOSFETs, which is reasonable for biomedical low-frequency applications, the power loss across the rectifier is proportional to the square of the instantaneous current ($I_T(t)$) as well as to the R_{ON} of the MOSFET

transistor. The value of R_{ON} can be reduced as desired by increasing the width of the rectifying transistor. These relationships are shown in equations (2.5).

$$P_{SSR} = R_{ON} \cdot \int I_T^2(t) \cdot dt \qquad (2.5)$$

where $$R_{ON} = \frac{1}{\mu C_{OX}(W/L)V_{eff}}$$

Assuming the R_{ON} of the active device within SSR is set to a reasonably low value that is feasible using sub-micron integrated technologies, the drop through the SSR is significantly lower than that of a diode. This would result in a significant improvement to power efficiency. The improvements would be even more significant in low power, low frequency and low voltage applications. With a SSR, the output voltage (V_{SSRO}) can be written as follows :

$$V_{SSRO} = V_I - (R_{ON} \times I_T) \qquad (2.6)$$

Where V_I and I_T are the input voltage and current to the SSR and R_{ON} is its dynamic resistance. Another advantage of the SSR is to eliminate external diodes, which is a useful step toward a fully integrated implant. In next section, we introduce new PCC architectures which benefit from using the SSR. Those structures are capable of delivering the required power to the implant with lower power loss.

2.6 New PCC architectures based on SSR

In order to improve the efficiency of a PCC, the drop in the diode rectifier must be reduced. Within the framework of classic rectifiers, and assuming we use silicon based

technology, not much can be done to reduce the drop below one silicon based diode drop which becomes comparable to nominal supply voltages in deep sub-micron technologies. Fully integrated PCC architectures could be obtained by replacing DR with SSR, which helps to achieve high power efficiency.

2.6.1 Distributed topology

The power dissipated in the DR degrades the overall PCC power efficiency and imposes more complexity in circuit implementation. Indeed, for boosting the voltage to a given high value, the DR-based PCC architecture tends to require more MSVM stages, compared with the DR-free PCC. This imposes the use of less efficient voltage multiplication techniques.

A new PCC architecture is proposed here by inserting an SSR at the front end of the MSVM. Also, the PCC is then split in two parallel paths. The first is composed of a DR followed by a VR and supplies the core, and the second path consists of a SSR and a MSVM to supply the MCS. This architecture is illustrated in Figure 2.4.

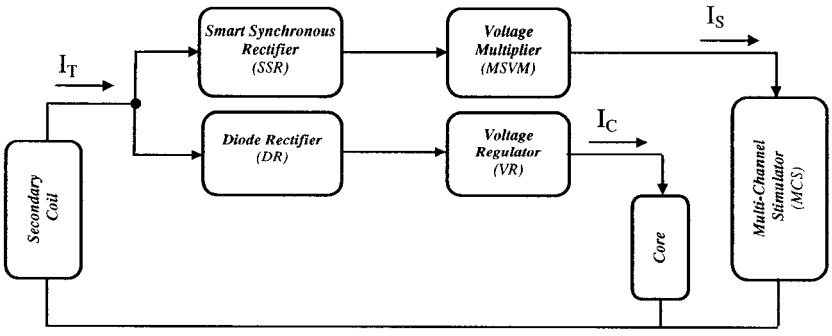


Figure 2.4: The scheme of a distributed PCC

With this architecture, power efficiency will be improved, due to the reduced losses in the DR. Besides, taking the input of the SSR directly from the input of DR can provide a higher voltage to the MSVM module, which allows reducing the number of voltage converter stages and using more efficient voltage multiplication techniques.

The power budget of this architecture is described by the following equation where P_{SSR} was obtained from equation (2.5):

$$P_I = \left(\frac{P_{MCS}}{\eta_{MSVM}} + P_{SSR} \right) + \left(\frac{P_{Core}}{\eta_{VR}} + V_\gamma \times I_C \right) \qquad (2\text{-}7)$$

Where P_{MCS}, P_{SSR} and P_{Core} are the required power for MCS, SSR and Core, respectively, and η_{MSVM} is the power efficiency for the MSVM module.

As previously noted, even though the I_T in this topology resembles to the input current in the conventional architecture, a deeper look at η_{MSVM} clarifies a significant difference. In the previous topology, the MSVM was located after the DR and VR modules, but here, it is located after the SSR. Therefore, the voltage level feeding the MSVM is higher than with the previous topology, which allows using fewer stages in the MSVM. This improves the global power efficiency of the MSVM, and it also reduces the ratio of its output to input voltages. In fact, the new I_T is quite smaller than with the conventional architecture. This combines an increase in η_{MSVM} to a decrease of power losses in the DR, to further reduce the total required input power in a significant way.

2.6.2 Monolithic topology

Here, another improved architecture is proposed. It combines both power distribution paths and feed them with a single SSR module as depicted in Figure 2.5.

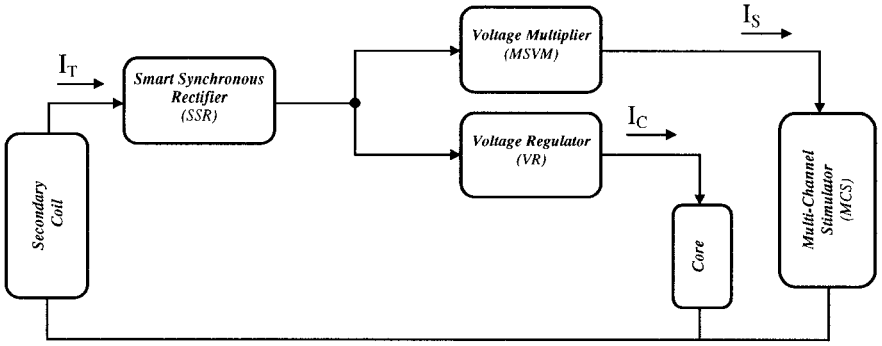


Figure 2.5: Block diagram of a monolithic PCC

In this topology, even though the core current (I_C) passes through the SSR, since this current is small compared with the upper current path, it does not change much the power loss in the SSR. The following equation describes the monolithic topology:

$$P_I = \frac{P_{MCS}}{\eta_{MSVM}} + \frac{P_{Core}}{\eta_{VR}} + R_{ON} \times I_T^{\,2} \qquad (2\text{-}8)$$

The main advantage of this architecture is not so much the improvement of the PCC efficiency, but the drop off the DR which is generally realized by off-chip diodes. A comparative study between these architectures will be given in chapter 5.

2.7 Summary

The architecture of a power conversion chain heavily impacts its overall efficiency. We

examined in this chapter the power efficiency of a conventional power conversion chain in an electronic implant to provide ground for further comparisons. The concept of Smart Synchronous Rectifiers was explained together with some suggestions to implement them. Two new power conversion chain architectures based on synchronous rectifiers were proposed. They improve the relative overall power efficiency. The second approach also removes the need for conventional diodes that are generally implemented as off-chip components. Moreover, the gate-controlled switches can also be used to stabilize the chain power efficiency while input voltage varies.

In order to boost the power supply voltage of sub-micron CMOS technologies to the level that is required for specific applications, voltage multiplier modules could be used. The next chapter is dedicated to voltage multipliers. It first review existing voltage multiplier structures and their characteristics. Then, it introduces the structure of a high efficiency multi-stage voltage multiplier with enhanced voltage multiplication factor.

Chapter 3

High-efficiency voltage multiplier

3.1 Introduction

With the rapid development of advanced electronic systems, low-power low-voltage techniques have become very important. Low supply voltages force severe constraints on circuit design. Power supply requirements for analog circuitries are often dictated by external signal sources and load which sometimes impose voltages few times higher than the supply voltage. For example, in some biomedical application, a voltage as high as 10 V may be required. Such voltage is not supported by most up-to-date semiconductor technologies.

Digital cores can benefit of techniques such as parallelism and pipelining to make trade-offs between speed and power supply voltage. However, this does not make them compatible with the analog interfaces needed for many applications. Multiple supply voltages can partially solve the conflict between requirements of digital and analog circuits, but the system cost is increased. Therefore, there is a great need for a module that could meet these requirements.

The demand for such a module is increased when one considers the fact that in the framework of deep sub-micron technologies, the supply voltage may be reduced to even

less than 1 V, while some analog applications require significantly higher than nominal supply voltage of new technologies [156].

Two classes of conventional circuits, the switching regulators and the charge pump-based converters, can provide voltages higher than the supply voltage. Both circuits use a high frequency switching action to achieve voltage conversion. The major difference between these two types of circuits is the elements used to store energy during the switching action. Charge pump circuits use capacitors as energy storage devices, while switching regulators use inductors or transformers.

Although the switching regulators employing off-chip inductors and capacitors have higher power efficiency than switched-capacitor type converters, bulky inductors are not suitable for integration and to provide low output current. Unlike the switching regulators, the output voltage of the charge pump circuits are usually not regulated.

3.2 Charge pump

The charge pump is a switched-capacitor based circuit that can provide an output voltage higher than the power supply. It can also provide a voltage of a reverse polarity. Compared to power converters with inductive energy storage components, charge pumps use no magnetic components. Hence, they are easier to integrate. The voltage gains are obtained in a charge pump as a result of transferring charges to a capacitive load not

involving amplifiers or transformers; thus the applications of charge pumps are limited mainly to a low power level [194]. Charge pumps can be used in various applications, such as analog switches [208,209], op-amp power supplies [166], flash EEPROMs [43,65,67,152,195,203], and continuous time filters [118]. Charge pump circuits are suffering from poor power efficiency, and may need large external capacitors to reduce the output voltage ripple depending on the output current.

High power efficiency, high voltage gain, low area, low output ripples, high output current and, low power consumption both at active and standby operation, are major concerns for low voltage multiplication applications. The issues such as frequency range as well as the number of clock pairs could somehow be reflected within those concerns.

3.2.1 Concept and characteristics

Charge pumps consist of capacitors, switches and at least, a two-phase clock as illustrated in Figure 3.1.

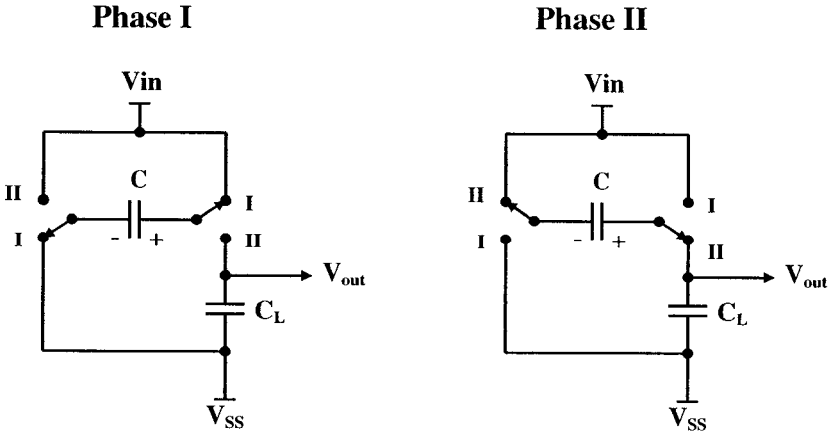


Figure 3.1: Charge Pump General Overview

The circuit is arranged in a way that in a first phase, the right plate of the capacitor is connected to the power supply, while its other plate in grounded. Therefore, it is charged to the supply voltage. When the clock toggles, in the second phase, the left plate is switched to the supply voltage. Since the capacitor maintains the charge from the previous phase, then a potential as high as twice the supply voltage is induced on its other plate. So, increased voltage levels are obtained in a charge pump as a result of transferring charges.

There exists various charge pumps structures. Dickson [48] and Makowski [112,113] charge pumps are the two most efficient and widely used designs. A Dickson charge pump uses a diode chain coupled to the inputs via capacitors, and a two-phase clock, to control charge transferring between capacitors. The Makowski charge pump is also based on a two-phase clocked voltage multiplier circuit with another circuit arrangement and a theoretical voltage gain related to Fibonacci numbers (2, 5, 13, 34, ...). These charge pumps have the highest voltage gains that need the least number of capacitors among two-phase charge pumps.

A newly proposed multi-phase charge pump [160] requires clock with more phases. To achieve the same voltage gain, the new design uses fewer capacitors, but requires multiple clock pairs that makes its control circuit much more complex. Multi-phase clocked charge pumps have the highest voltage gain if the same number of capacitors is used. Hence, a desired voltage gain can be implemented with the least design area.

3.2.2 Charge pump types

The principle of voltage multiplication based on charge pumping has been known for a long time and was developed significantly during past decades.

3.2.2.1 Cockcroft-Watson charge pump

The idea of pumping charges was originally introduced by Cockcroft and Watson to generate steady high potentials [41], as depicted in Figure 3.2. The structure of the charge pump can be extended by adding more capacitors. The output voltage it produces grows with the number of stages. This approach requires sufficiently large coupling capacitors for efficient multiplication and adequate drive capability. Therefore, it does not easily lend itself to integration in monolithic form as on-chip capacitors are limited to a few picofarads with relatively high values of stray capacitance to substrate.

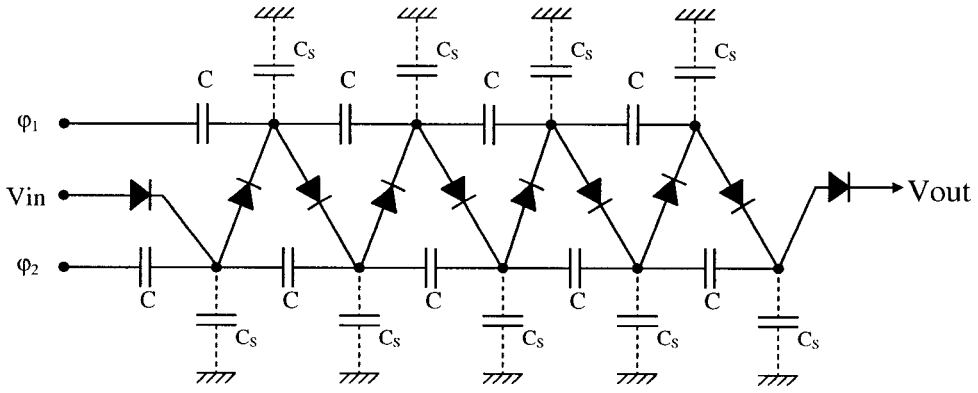


Figure 3.2: Cockcroft and Watson Charge Pump [48]

In practice, it is difficult to generate voltages significantly larger than twice the supply voltage, irrespective of the number of multiplying stages [143]. Some studies have shown

that if the number of stages is increased beyond a critical number (typically, 3 or 4), determined by the ratio of coupling and stray capacitors, the output voltage can actually decrease due to voltage drops in the diode chain [48].

3.2.2.2 Dickson charge pump

In order to overcome the limitations of Cockcroft and Watson charge pump, an improved structure was devised [48], as shown in Figure 3.3. It is suitable for integration in a monolithic form. Here, the multiplier chain is implemented using diode-connected MOS transistors in series and therefore, each stage has a voltage drop determined by the threshold voltage modified by the body effect.

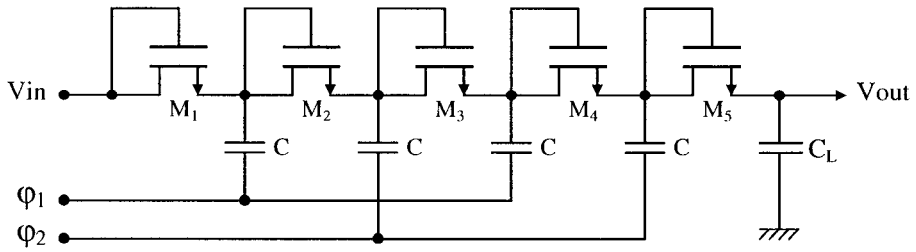


Figure 3.3 : Dickson Charge Pump [48]

The multiplier operates by pumping charges along the PMOS transistor chain as the capacitors are successfully charged and discharged during each clock cycle φ_1 and φ_2 which are of opposite polarity. When clock phase φ_1 goes low, transistor M_1 conducts until the voltage at node 1 becomes V_{in}-V_T. When φ_1 switches to high (φ_2 goes to low), the voltage at the said node becomes $V_{in}+(V_{Clk} - V_T)$. This causes transistor M_2 to

conduct until the voltage at node 2 becomes equal to $V_{in}+(V_{Clk}-V_T) -V_T$. When φ_1 gets low again, the voltage at node 2 becomes $V_{in} + 2(V_{Clk} - V_T)$. After N stages, it is easy to see that the output voltage is determined by equation (3.1).

$$V_{OUT} = V_{IN} + N \cdot (V_{Clk} - V_T) - V_T . \tag{3.1}$$

It is worthy to note that specially at the high-voltage nodes near the output, the increase in the threshold voltage can reduce the voltage pumping gain significantly. The necessary condition for the charge pump to function is that voltage fluctuations at each pumping node must be larger than the said threshold. The new configuration achieves more efficient multiplication even in the presence of stray capacitance and its drive capability is less dependent than Cockcroft configuration on the number of multiplier stages. Poor accuracy, considerable power consumption and dependency of the output voltage to the process parameters, are the other major drawbacks of this structure.

As supply voltage decreases, both clock voltage and voltage fluctuation in charging nodes are decreased accordingly, and the voltage pumping gain per stage is also reduced. Therefore, this charge pump is not suitable for low-voltage operation. It is possible to use floating-well devices to eliminate the body effect [36]. However, the resulting charge pumps may generate substrate currents and the voltage pumping gain per stage is further reduced by the threshold voltage. If the threshold voltage term could somewhat be eliminated from the circuit, the Dickson charge pump would be usable at low voltages, offer a better voltage pumping gain and a higher output voltage.

3.2.2.3 Static Charge Transfer Switch (CTS)

Several modifications from the simple charge pump have been introduced to increase the maximum output voltage by eliminating the body effect at the cost of complicated control circuits, such as multi-phase pulse generator or a boosting circuit. Static-Charge-Transfer-Switch-based charge pumps are improved charge pumps employing MOS switches to increase the voltage pumping gain [213]. The basic idea behind this technique is to use MOS switches with precise on/off characteristics to direct charge flow during pumping rather than using diodes, or diode-connected transistors, which inevitably introduce a forward voltage drop at each node. Figure 3.4 shows a charge pump using MOS CTS's with static backward control. Using this structure improves voltage pumping gain.

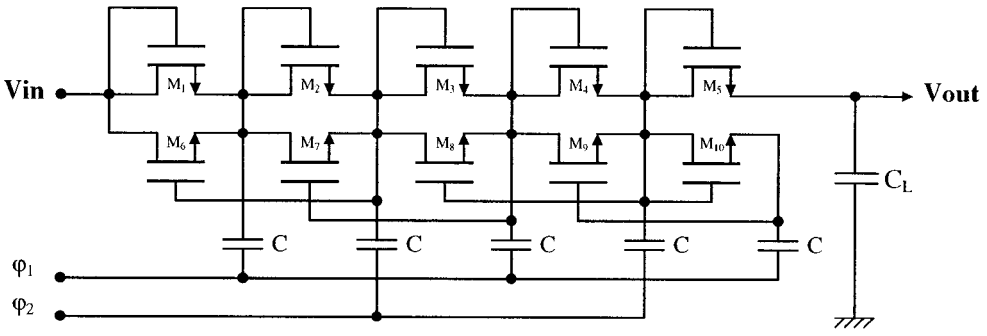


Figure 3.4 : Charge pump using Static CTSs [213]

Switches M_1-M_4 are diode-connected transistors which are involved in the pumping operation and setting up the initial voltage at each pumping node. M_6-M_{10} are the CTSs. Here, the already established high voltage is used to control the CTS of the previous stage. Unfortunately, there is one minor problem with this circuit configuration, namely,

charge leakage in the reverse direction from the CTSs, which results in reduction of the overall voltage pumping gain.

3.2.2.4 Dynamic charge transfer switch

In order to obtain better pumping performance, each CTS is accompanied by an auxiliary pair of pass transistors [213] so that the CTSs can be turned off completely while they can also be turned on easily by the backward control signal. Figure 3.5 illustrates such circuit.

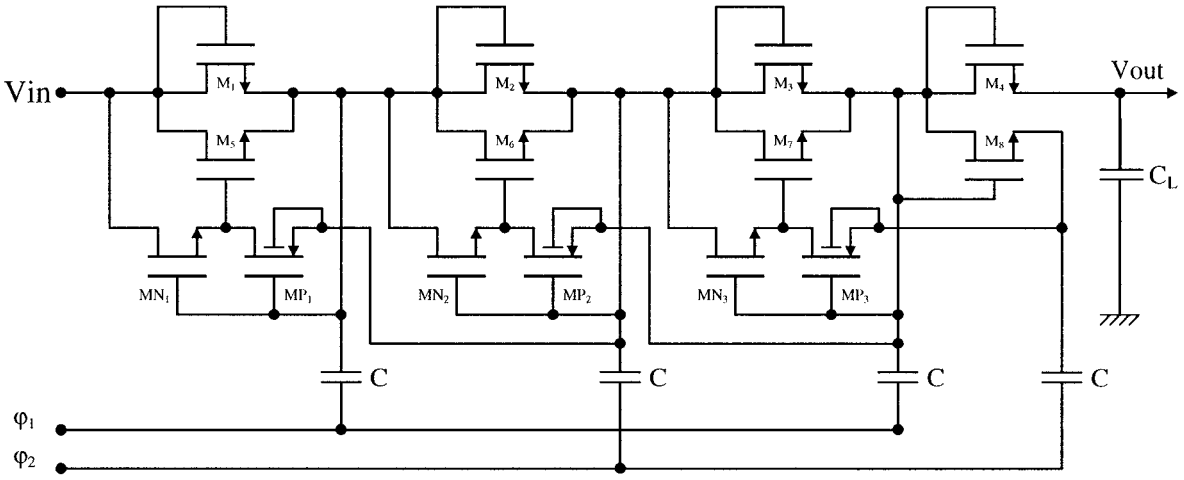


Figure 3.5 : Charge pump using Dynamic CTSs [213]

3.2.2.5 Advanced charge pump approach

Another class of charge pump designs suitable for high performance, low-voltage operation are based on switched-capacitor [158], and dynamic gate biasing [138]. The latter exhibits a quick transient to its steady state due to the reduced switch resistance.

3.3 Single-stage voltage multiplier

A single-stage voltage multiplier consists of a charge pump, a clock generator, and the charge transfer module. The stored charges in the charge pump module are pumped toward the output via a one-direction path provided by the charge transfer module if suitable timing is respected.

3.3.1 MOS-based charge pump

A DC voltage booster, viable in a CMOS technology, has been proposed [23,124]. It has the particularity of cross-connecting a NMOS transistor pair as illustrated in Figure 3.6. This circuit has two free running clock inputs, Clk and NClk, where the second is an inverted phase with respect to the first one. By clock toggling, the sum of clock and supply voltages is induced in the capacitor plate connected to the output node.

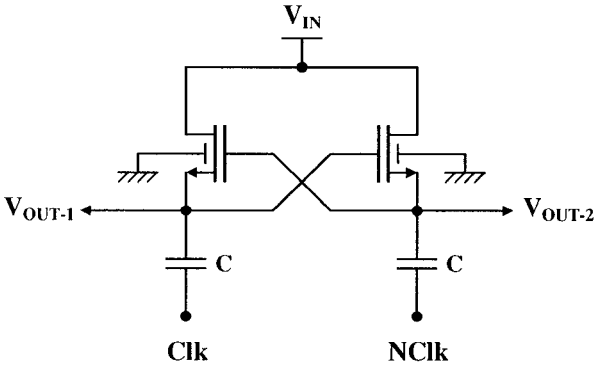


Figure 3.6 : MOS Implemented Charge Pump

This is a typical positive feedback process with two stable states. When the loop gain exceeds one, the voltages on charge pumping (output) nodes will quickly change and

enter in a stable state. The time it takes for the loop gain to exceed one (response time) depends on the transistor size, capacitance at pumping nodes (including charge pump and stray capacitances), and the voltage difference between power supply and pumping node voltages. Hence, the size of transistors must be selected such that the response time would be shorter than clock pulses. This use of NMOS transistors is efficient, not only because of higher carrier speed, but specially since it provides automatic reverse bias of the drain-bulk and source-bulk junctions.

3.3.2 Charge transfer module

In order to have successful charge transfer, it is essential to provide a uni-directional path along with the charge pump. A module that observes this requirement is a charge transfer module consisting of diodes. Using CMOS technologies, diode-connected MOS transistors could replace diodes successfully. However, they are constrained by their threshold voltage. Therefore, employing gate controlled transistors as switches is advantageous, because they present precise on/off characteristics and do not introduce significant forward voltage drop.

Although NMOS transistors benefit from faster carriers (electrons versus holes), greater conductance and less gate capacitor (C_g), their threshold voltage makes them inadequate for low voltage application. Indeed, PMOS series switches fabricated in N-well processes are often preferred because they present lower threshold voltage. However, the challenges due to their body effect and large parasitic capacitance remain. Using PMOS

switches as charge transfer devices has also its own problem. The designer must ensure proper biasing of their Drain-Bulk and Source-Bulk P-N junctions. A solution for proper bulk biasing was proposed in [34]. It uses two charge pump blocks, one for the supply and the other to boost the bulk voltage. This approach not only suffers from more complexity, but also implies a quasi-permanent charge loss, because of floating bulk of serial switch used in secondary charge pump. Figure 3.7 shows another technique to eliminate the charge leakage via the bulk of PMOS transistors. It is known as a bulk switching technique [60]. Here, M_1 is the charge transfer switch and M_2 and M_3 serve as bulk biasing devices to tie the Well to the higher voltage between source and drain terminals.

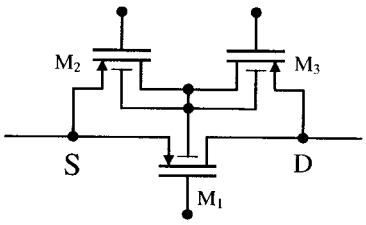


Figure 3.7: Dynamic Gate Biasing

Here, M_1 is the charge transfer switch and M_2 and M_3 serve as bulk biasing devices to tie the Well to the higher voltage between source and drain terminals.

3.3.3 Complete scheme

The overview of a single stage voltage multiplier (VM) then looks like Figure 3.8. In this configuration, M_1, M_2 and C constitute the charge pump module. Transistors M_3-M_4 and

M_5-M_6 form the charge transfer module. The former pair serves as series switches, while the latter is used for proper bulk biasing. The small capacitor, C_B, is necessary to preserve the bulk potential when switching.

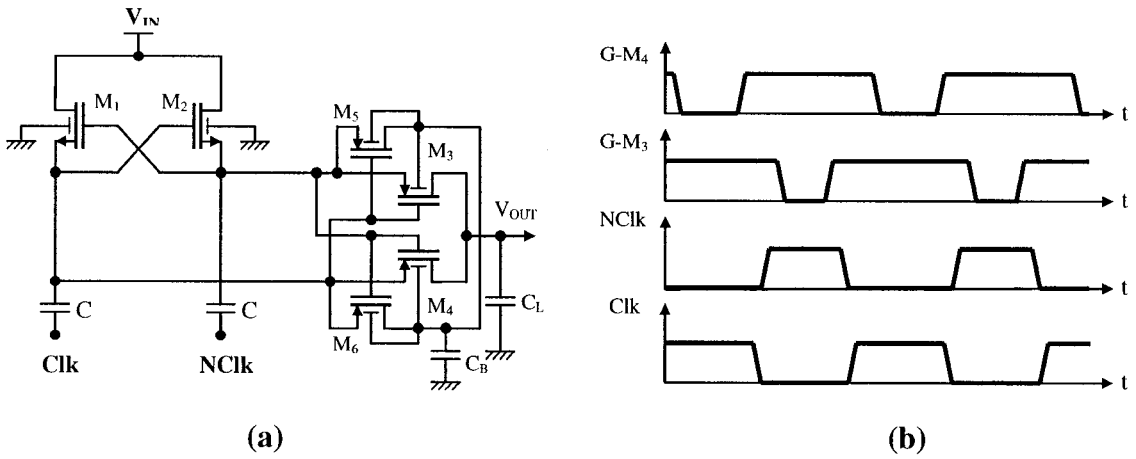


Figure 3.8: Classical Single Stage Charge Pump:
(a) Schematic, (b) Non-overlapping clocks

We may also use start-up circuit to provide initial voltages for clock generator in order to ensure proper pumping action and avoid latch-up during power-up [200].

3.4 Voltage multiplier characteristics

Power efficiency is defined as the ratio of the output power to the input power. The input power includes the power consumed through the supply as well as the one drawn from the clock generator. Internal power loss, ignoring dynamic ohmic loss in switches, consists of losses in stray capacitors. A single stage voltage multiplier was already modeled and its power efficiency was examined [61]. As a result, it was found that for a

non-ideal voltage doubler, with a source resistance of R_S, charge pump capacitors of C, stray capacitors of C_S, load of R_L and switching frequency of f, the power efficiency could be expressed as equation (3.2). In this study, the resistance of the switches is ignored.

$$\eta = \frac{E_L}{E_L + E_S} = \frac{1}{1 + C_S \cdot f \cdot \frac{(R_L + R_S)^2}{2.R_L} + 2 \cdot C \cdot f \cdot \frac{R_S^2}{R_L}} \tag{3.2}$$

Where E_L and E_S are the energy consumed by the load and the energy delivered by the source respectively. The power efficiency is also a function of the output current of the charge pumps. Therefore, the challenge to improve efficiency calls for a wide range of circuit parameter adjustments.

3.4.1 Output current

The amount of output current is a matter of concern for any power supply. This is also true for voltage multipliers. As a matter of fact, a charge pump transfers charge packets toward the output stage. So, one can express the output current with equation (3.3):

$$I_{OUT} = \frac{Q_{Ch}}{t_{Clk}} = \frac{C \cdot V_{Ch}}{t_{Clk}} = C \cdot V_{Ch} \cdot f \tag{3.3}$$

Thus, in order to provide more current at the output stage, either larger capacitors or a higher clock frequency should be employed. The former results in higher stray capacitances, which is against our objective. In the framework of application-oriented frequency allocations, there is not much room for selecting proper switching frequency

[88]. This implies the size of charge pump capacitors is a dominant design parameter in order to meet output current requirements.

3.4.2 Output ripples

The charge pump is also suffering from high amplitude output ripple. In a conventional switched–capacitor type DC-DC converter, which consists of a single charge pump, there exists a ripple voltage V_R at the output due to a load resistance R_L discharging an output capacitance C_{Out} periodically. The ripple voltage could be expressed by equation (3.4):

$$V_R = \frac{Q_{Ch}}{C_{Out}} = \frac{I_{Out} \cdot t}{C_{Out}} = \frac{I_{Out}}{C_{Out} \cdot f} = \frac{V_{Out}}{R_L \cdot f \cdot C_{Out}} \tag{3.4}$$

Ripple voltage can be substantially reduced by increasing the frequency of the clocks, by changing transistor parameters or by using large output capacitance. In the latter case, it would take the charge pump significantly longer to reach its steady state.

3.4.3 Voltage gain

In steady state and neglecting boundary conditions, the input voltage is expected to increase in proportion with the amplitude of the incoming clock signal and with the number of stages. This is expressed in equation (3.5).

$$V_{OUT} = V_{IN} + N \cdot V_{Clk} \tag{3.5}$$

Where N is the number of cascaded stages. However, because of the effect of existing parasitic capacitances in the circuit, the voltage increment (fluctuation) at each stage, ΔV,

is revised as per equation (3.6). Here, it is assumed that clock amplitude is the same as the input power supply voltage.

$$\Delta V = V_{DD} \cdot \frac{C}{C + C_S} - \frac{I_{OUT}}{f \cdot (C + C_S)} \tag{3.6}$$

The first term addresses the charge sharing in the charge pump and its stray capacitors, while the second is due to loading effect. Therefore, instead of our expectation expressed by equation (3.5), a lower voltage gain is obtained. The output voltage can be formulated as equation (3.7):

$$V_{OUT} = V_{DD} + N \cdot \Delta V \tag{3.7}$$

Substitution of equations (3.6) and (3.7) provides a clear indication on the effect of circuit parameters on the overall voltage gain:

$$V_{Out} = V_{DD} + N \cdot \left(\frac{V_{DD} \cdot C}{C + C_S} - \frac{I_{OUT}}{f \cdot (C + C_S)} \right) \tag{3.8}$$

More precise calculations considering the non-idealities in switches introduce additional drawbacks decreasing the output voltage.

3.5 Power efficiency improvement

Many issues could affect the overall power efficiency of voltage multipliers, among them, the effect of stray capacitors, overlapping clocks, shorts during charge and discharge times, capacitor plates resistance, static and dynamic losses in switches, charge injection and leakage are of major importance.

3.5.1 Switching frequency

Conventional voltage multipliers circuits are designed to operate at a fixed switching frequency, with a rated output load current and voltage. Indeed, to obtain the best power efficiency for such a CMOS-based circuit, there exists an optimal value for the width of the MOS transistor switches used in the charge pump. For instance, this optimal width is shown to be proportional to the square root of the load current for a multi-phase voltage multiplier [200].

Unfortunately, for most applications, the output load current is usually varying, depending on the mode of operation. When the load current is changing, either transistor width or switching frequency should be modified to maintain the power efficiency. Since the switches are not ideal and present an on-resistance, they require some transition times between their states. This time has an important effect on the efficiency when one considers the non-overlapping switching requirements of the circuit. Normally, it is not possible to dynamically change the on-chip transistor widths, a large enough transistor and high enough switching frequency should be chosen to guarantee the output voltage levels at the maximum loading.

3.5.2 Integrated capacitor

Charge pumps usually operate at high frequency in order to increase their delivered power within a reasonable size of total capacitance used for charge transfer. The latter helps for integrating an entire charge pump. In order to implement such charge pump in a

real circuit, a large size capacitor is required. So, it is critical to use as few capacitors as possible in a charge pump circuit design.

Furthermore, the most important components of the VM, from an efficiency point of view, are the capacitors. Efficiency of capacitive components is strongly dependent on the ratio between the switched capacitor value and its parasitics, as well as the discharge ratio of the capacitors. This is because the stored charges in the stray capacitances reduce the amount of pumped charges [49]. When these capacitors are integrated, they always present significant stray capacitances to the ground. When running at voltages below the nominal process voltage, the best choice is either using thin oxide or double poly capacitors because they offer less stray capacitances [61].

3.5.3 Non-overlapping clock

In order to hold the maximum efficiency, any overlap in the clock signals controlling charge transfer switches must be avoided. This is to guarantee that the switches are operated in a break-before-make fashion to eliminate short-circuit currents. Such currents impose lost charges and consequent dynamic switching loss during transitions. Recall that at high frequencies (above 1 MHz), the dynamic losses become significant.

Considering Figure 3.8a, there are three possible paths that can cause a short circuit current or a dynamic loss. One path is going through the cross-coupled transistors M_1 and M_2, and charge pump capacitors (C), when both input pulses are high. The other two are

going through the transistors pairs formed by M_3 and M_4, and by M_5 and M_6. When the input pulses are low and overlapping, both PMOS pairs can cause a discharge of the output node and C_B capacitor, respectively. We may need an additional large capacitor for stabilizing the well bias if there is a dynamic charge loss through the transistors M_5 and M_6. This necessitates to use a non-overlapping clock, controlling the switches as shown in Figure 3.8b [95]. It should also be noticed that due to the large gate capacitance of the transistor switches, large rise/fall time may cause the two-phase clocks to overlap.

3.5.4 Charge transfer switch conductance

The power loss in MOS switches, which results in power efficiency reduction, splits in static loss because of their resistance and, dynamic loss due to their switching. The former, which is dominant, depends on the on-resistance of the switching transistors and the load currents, while the latter depends on the switching frequency, gate size, and the output voltage.

The conductance of the PMOS transistor in triode region is expressed by equation (3.9):

$$g_{ds} = \mu_p \cdot C_{OX} \cdot \left(\frac{W}{L}\right)_p \left(V_{SG} - \left|V_{TP}\right|\right) \tag{3.9}$$

Therefore, the conductance of two cascaded PMOS switches, M_3 and M_4, as well as auxiliary dynamic gate biasing transistors M_5 and M_6 of Figure 3.8, can be improved by either employing larger switching transistors and/or increasing the gate voltage. However, realizing large transistors causes larger stray capacitances as well as further risk of clocks overlapping, which degrades the performance of the circuit. With the

architecture illustrated in Figure 3.8a, the gate signals of the cascaded PMOS switches were fluctuating between V_{IN} and $2V_{IN}$. A significant improvement in conductance of the series switches is obtained if these signals can range between 0 and $2V_{IN}$. This can be realized with a simple and well-known level shifter such as the one shown in Figure 3.9.

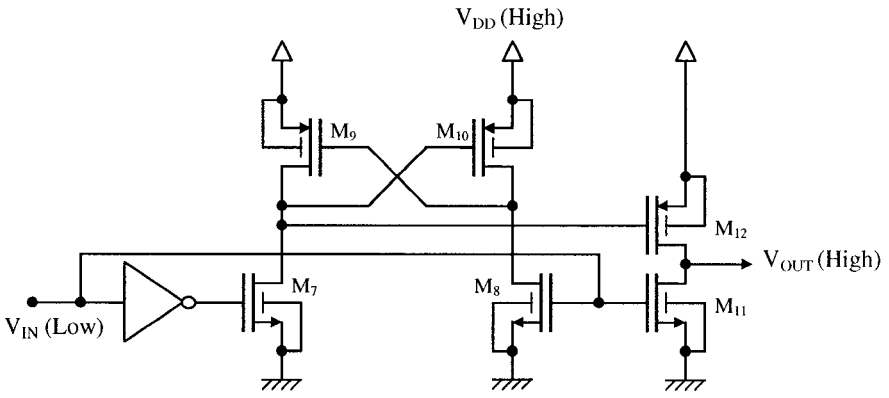


Figure 3.9: Schematic of a level shifter

The circuit consists of two stages. The first stage includes an input inverter, a NMOS transistor pair composed of M_7 and M_8, and the PMOS transistor pair composed of cross-coupled M_9 and M_{10}. The latter pair forms a voltage mirror that regenerates any voltage that appears on their drains. The second stage is an inverting pair composed of M_{11} and M_{12} that reacts to the signal produced by the first stage and to the input signal. The proposed circuit performs level shifting and produces sharp transitions. This circuit is supplied by the output voltage of the same voltage multiplier stage which is larger than its input.

Although using level shifters increases the conductance of PMOS cascaded switches, it may also increase the switching power dissipation. In fact, the level shifter consumes

additional power and its voltage swing ranges from 0 to V_{Out} level. It is worthy to notice that the period of input clock must be adjusted to the response time of the circuit. Otherwise, the level shifter will not switch state.

3.6 Low-voltage application

For low input voltages, below V_T+500 mV, the charge pump capacitors of C have voltage ranging from V_{IN} to $2V_{IN}$. So, the pair of M_1 and M_2 have a low V_{eff} voltage which may degrade the power efficiency and the overall functionality of the VM. To overcome this problem, one can make a circuit arrangement such that those gates would be driven between V_{IN} and $3V_{IN}$. This could be realized using an auxiliary charge pump that consists of two pairs of transistors (M_{1a}-M_{1b} and M_{2a}-M_{2b}) and two capacitors (C'), connected to the gates of M_1 and M_2 as shown in Figure 3.10 [61].

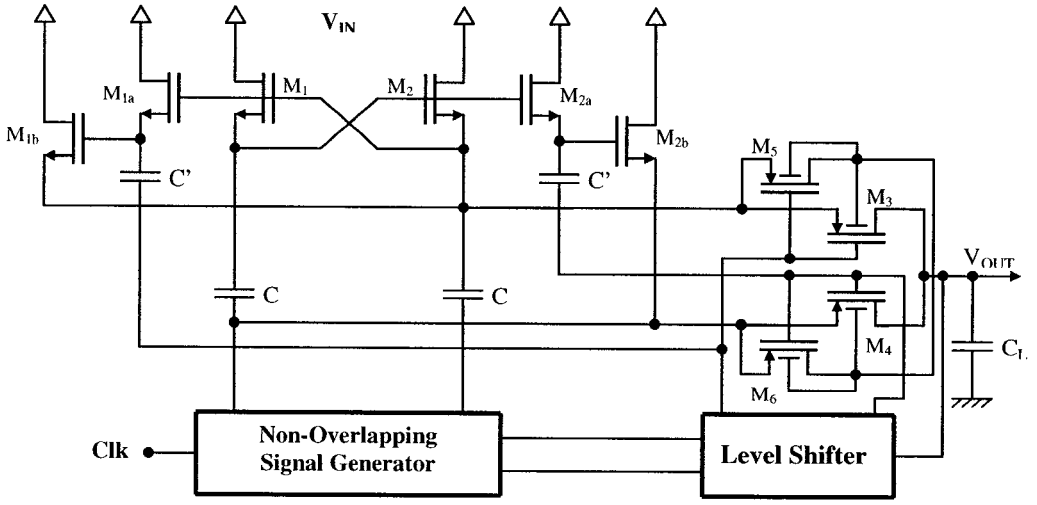


Figure 3.10 : High Efficiency Voltage Multiplier for Low Voltage Applications

The incoming clock signal to this extra charge pump is taken from the point with variation from 0 to $2V_{IN}$ which could be the outputs of the level shifter. This scheme improves the efficiency and guarantees the start-up of the charge pump.

3.7 Multi-stage voltage multiplier

Our application requires voltages a few times higher than the nominal power supply voltage of sub-micron technologies. Realizing a single stage voltage multiplier for such applications implies circuit elements of impractically large size. The classical solution calls for cascading voltage multiplier stages in a series chain. That is, the output voltage of the previous stage would be the power supply of the next one Figure 3.11. The scheme consists of a chain of three cascading voltage doublers. A common clock signal feeds all the chain modules.

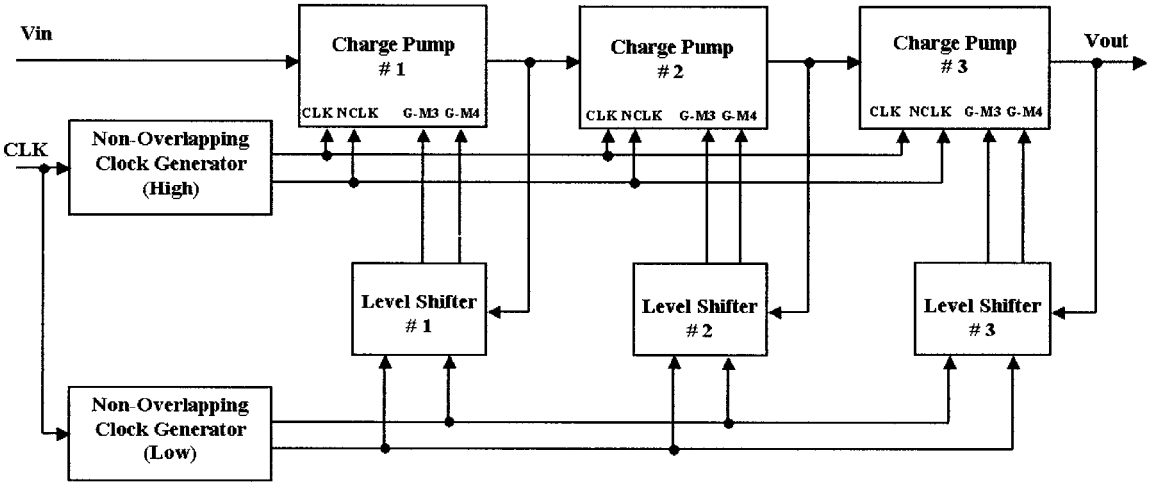


Figure 3.11 : Classical topology for a Multi-Stage Voltage Multiplier

Using Multi-Stage Voltage Multiplier (MSVM) facilitates the demand for having selective voltage multiplication, which is essential for having an efficient power conversion chain. This is because in an electronic implant, the stimulation voltage across the electrode-tissue contacts depends on their interfacing condition and could vary with time.

Using equation (3.7), the total required capacitance for a N-stage MSVM, C_{Total}, in the chain, is:

$$C_{Total} = N \cdot C = \frac{(C + C_S)(V_{OUT} - V_{DD})}{(C \cdot V_{DD}) - \frac{I_{OUT}}{f}} \cdot C \qquad (3.10)$$

As a result, the minimum capacitance, C_{Min}, of each stage to reduce the total capacitance in a charge pump is obtained by differentiation of equation (3.10) [102].

$$C_{Min} = \frac{I_{OUT}}{V_{DD} \cdot f} + \sqrt{\left(\frac{I_{OUT}}{V_{DD} \cdot f}\right)^2 + \frac{C_S \cdot I_{OUT}}{V_{DD} \cdot f}} \qquad (3.11)$$

By substituting equation (3.11) in equation (3.10), the optimum number of stages can be obtained. Here, we neglected R_{ON} of the series switches and assumed that clock and power supply are of the same voltage level. Once the required output voltage and current levels are decided, the minimum charge pump capacitor per stage, the number of stages, and the total power consumption will be obtained.

3.7.1 New architecture

Few efforts have been dedicated to introduce new architectures in order to improve the voltage multiplication factor within a MSVM [17]. They were initiated taking equation (3.5) in consideration. This equation clarifies that the voltage boosting in each stage depends on the amplitude of the clock signal. It also shows that the output voltage of each stage is larger than its inputs. Therefore, one can use the output of each stage as the high supply voltage to the following level shifters as illustrated in Figure 3.12. In this new structure, the non-overlapping clocks at high level are lifted up to be used in the following stage, while non-overlapping clocks at low levels are shifted to be used in the same stage.

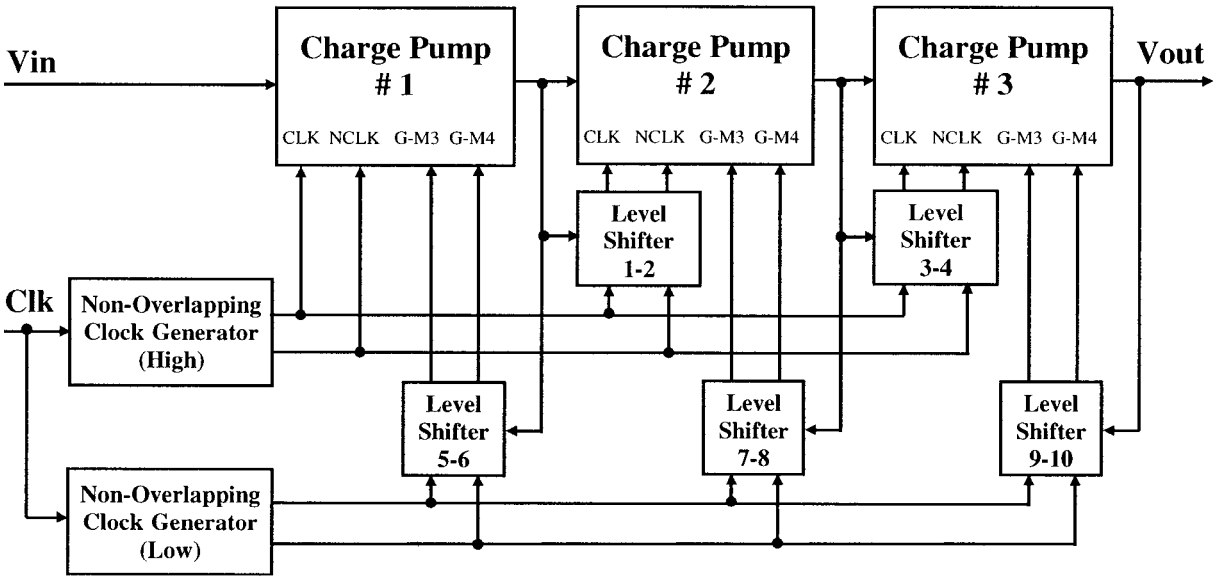


Figure 3.12: The scheme of an improved MSVM

In each stage, the input clocks to charge pump capacitors should not be overlapping when both pulses are high, and similarly, the clocks applied to charge transfer switches should

be non-overlapping when both are low. Moreover, the PMOS charge transfer transistors must start conducting after charge pump clocks get high and must be turned off before those clocks get low.

The output voltage of each stage can then be expressed by equation (3.12):

$$V_{OUT(N)} = V_{IN(N)} + V_{CLK(N)} \tag{3.12}$$

Where the clock amplitude of the N-th stage is determined by equation (3.13).

$$V_{CLK(N)} = V_{IN(N-1)} + V_{CLK(N-1)} \tag{3-13}$$

Hence, for a N-stage voltage multiplier, ignoring all non-idealities in the circuit elements, the output voltage will be boosted exponentially.

$$V_{out} = 2^{(N-1)}\left(V_{IN} + V_{Clk}\right) \tag{3-14}$$

Comparing equations (3.5) and (3.14), the output voltage is no longer in linear proportion to the number of stages but grows exponentially with that number. Therefore, using a given number of stages, the new architecture represents significant increase in the voltage multiplication factor. It further results in fewer stages, and increase in power efficiency.

3.8 Summary

In the framework of new sub-micron technologies and certain applications, there is a great demand for voltages higher than technology nominal voltage which could be provided by voltage multipliers. The poor efficiency in most switched-capacitor-based architectures justifies research on the subject. In this chapter, a brief explanation was

presented on the charge pump concept, types and relative design challenges. A high-efficiency fully integrated CMOS voltage multiplier is proposed. It can benefit of bulk switching and level shifting techniques to reduce the dynamic losses in serial switches. An extra charge pump attached to the basic circuit enhances the functionality and performance of the module for low-voltage applications. Finally, multi-stage voltage multiplier architectures were also examined. The latest structure nominally provides an exponential increase of the voltage with the number of stages.

The ability to produce voltages much larger than the nominal supply voltage of the technology provides an excellent motivation to explore the reliability and longevity of MOS device under voltage stress. Indeed all discussions on voltage multipliers assumed that the devices comprising these circuits can withstand their operating voltages.

Chapter 4

Reliability challenges of CMOS under sub-micron regime

Scaling down MOSFET dimensions has been a continuous trend since the early seventies. Smaller device size enables higher integration density. In addition, a smaller channel length improves transistor transconductance and thus, integrated circuit performances. As device dimensions are reduced, influences from the side regions of the channel, that is, source, drain and isolation edges, become increasingly significant. Device characteristics, therefore, deviate from those derived from long-channel approximations.

4.1 Short channel effects

A reduction of the channel length tends to reduce the input capacitance of CMOS transistors due to reduced gate area. It also increases charging and discharging currents, if the gate is controlled by the same V_{GS}, which improves switching speed. Additionally, size reduction leads to a smaller cell area, thus the possibility of integrating more logic cells to create more powerful ICs. These are extremely motivating, and economically rewarding benefits. However, a successful reduction of the channel length requires that some other device parameters be adjusted. Appendix A addresses a detailed study on short-channel effects and relative improvements. Such down scaling impacts threshold voltage, oxide reliability, drain/source process requirement, resistances, channel length

modulation, carrier mobility, carrier velocity saturation, random dopant distribution, and interconnection delays. Channel length reduction also leads to an undesirable increase in gate series resistance. To minimize these effects, the MOS structure is further modified by creating a silicide layer on top of the gate, which makes the processes more costly.

4.2 Narrow-channel effects

Channel width has also a significant impact on the MOS transistor characteristics when it is down sized. As a part of semiconductor manufacturing process, a metal layer is deposited on proper locations in order to make contacts to the MOS terminals and, to provide interconnections. This metal generally covers gate terminal as well as field oxides located on its sidewalls. Diffusion regions do not extend on the sides of the channel. Hence, a small depletion region extends sideways in areas lying outside the gate controlled region. Figure 4.1 illustrates the edge effect at the channel ends that determines the channel width.

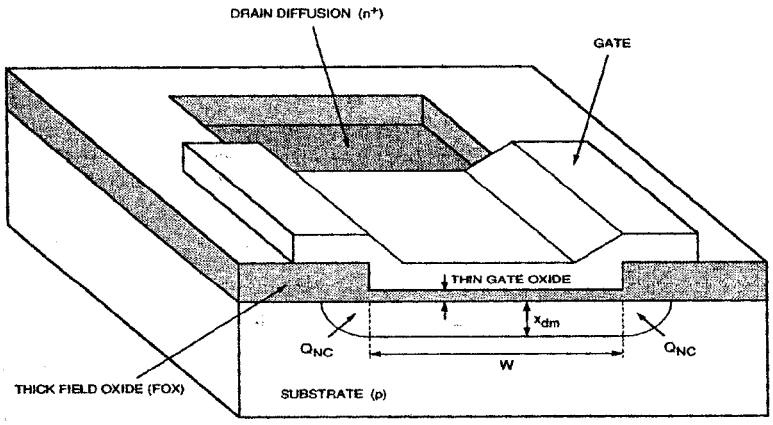


Figure 4.1: Narrow channel effect [12]

The classical threshold voltage equation is generally derived under the assumption that the gate voltage creates depletion-layer in the rectangular area under the channel. In reality, the gate voltage depletes a wider region, due to the fringing field effect which implies a waste for the gate voltage [12,56]. These are reflected in equations (4.1) and (4.2):

$$V_{TO}(Narrow-Channel) = V_{TO} + \Delta V_{TO} \tag{4.1}$$

$$\Delta V_{TO} = \frac{1}{C_{OX}} \cdot \sqrt{2 \cdot q \cdot \varepsilon_{Si} \cdot N_A \cdot |2\phi_F|} \cdot \frac{k \cdot X_{dm}}{W} \tag{4.2}$$

Here, k is an empirical parameter that depends on the shape of the fringe depletion region. For wide channels (W large), the electric-field waste approaches zero, eliminating this effect from the threshold voltage equation, but for narrow channels, the lateral charge becomes comparable to the charge directly beneath the W-width of the gate, that is, there is an increase in the effective charges/cm^2 being balanced by the gate charge. Thus, added gate charge is required to reach the start of inversion, and V_T becomes dependant on the channel width and thus, increases [139]. The change in V_{T0} is proportional to (X_{dm}/W). As a result, the threshold voltage of a narrow-channel device is larger than that of a conventional device as shown in Figure 4.2.

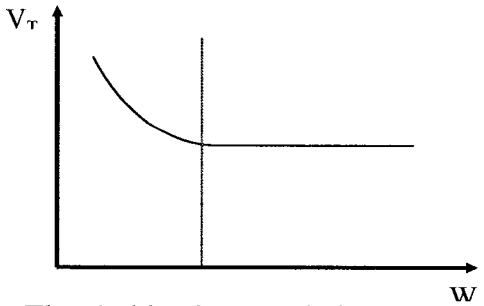


Figure 4.2 : Threshold voltage variation versus channel width

It is worthy to note that the edge effect here is opposite to that observed when reducing channel length.

4.3 Subthreshold and leakage currents

High performance circuits are mainly targeted toward maximum logic speed while preserving power. Therefore, the trade-off between these design parameters has received a great deal of attention. An undesirable part of the power consumption, the static power, is usually caused by off-state leakage currents discussed in this section [216].

4.3.1 Subthreshold current

According to theory, when $V_{GS} < V_T$, the transistor is in weak inversion, channel starts to form and a low level of current flows between source and drain. This current is called the subthreshold current. It increases the amount of off-state power consumption as well as occurrence of instabilities in the circuit functionality. It is generally accepted that current flowing in the subthreshold region is due to diffusion compared to drift in strong inversion. Therefore, the MOS in this region should behave as a BJT in normal active mode. In this region, if V_{DS} exceeds a few kT, the drain current is approximately an exponential function of gate voltage (equation 4.3) [92].

$$I_{DS} = I_{DO} \cdot \left(\frac{W}{L}\right) \cdot e^{\left(\frac{q \cdot V_{GS}}{n \cdot k \cdot T}\right)} \tag{4.3}$$

The subthreshold slope, S, is a measure of subthreshold region. It is defined as expressed

in equation 4.3:

$$S = \frac{dV_{GS}}{d(\log I_D)} \tag{4.4}$$

It could be used as a measure that shows how the device turns off in digital applications. The smaller the threshold slope, the better the transistor acts as a switch. In order to get a lower value of S, one may either reduce the oxide thickness, t_{OX}, or the channel doping N_{sub}. It is experimentally observed that unlike equation 4.3, increasing V_{DS} shifts I_{DS}. Such dependence between the subthreshold transfer characteristics (I_D versus V_{GS}) for different V_{DS} indicates an effect due to deep penetration of the drain-to-substrate depletion layer under the gate [56]. Using substrate graded doping profile, that is, low doping at the surface and higher doping below the surface, or use of silicon-on-insulator (SOI) structures, may reduce this phenomenon.

4.3.2 Junction leakages

The leakage current (I_{lk}) of the junctions is another important limitation. This current of a reversed-biased junction (drain or source-to-substrate junctions), is approximately given by equation (4.5) [92]:

$$I_{lk} = \frac{q \cdot A_j \cdot n_i}{2\tau_0} \cdot X_d \tag{4.5}$$

where A_j is the junction area, n_i is the intrinsic concentration of carriers in undoped silicon, τ_0 is the effective minority carrier lifetime, and X_d is the thickness of the depletion region which is given by equation (4.6):

$$X_d = \sqrt{\frac{2K_S\varepsilon_0}{qN_A}\cdot\left(\phi_0 + V_r\right)} \tag{4.6}$$

and n_i is given by equation (4.7):

$$n_i \cong \sqrt{N_C \cdot N_V}\cdot e^{\frac{-E_g}{kT}} \tag{4.7}$$

where N_C and N_V are the densities of states in the conduction and valance bands and E_g is the difference in energy between the two bands. As n_i approximately doubles for every temperature increase of 11 °C, down scaled circuits are subject to higher leakages that increase power dissipation. At high temperatures, leakage currents can become a real concern.

4.3.3 Gate leakage current

Assuming integrity of the gate oxide, this leakage current is due to electrons tunneling, resulting in a current from gate to drain or source. Direct tunneling is responsible for leakage when low bias voltage and electric field are applied. By contrast, when large bias or high electric fields are present, which is the case for very thin gate oxide technologies, the width of the barrier becomes not only dependent on the device structure, but also on the applied bias voltage [35]. So called Fowler-Nordheim tunneling is expected to take place. This leakage implies power consumption even when the device is inactive, and it can cause local heating that accelerates device aging. It may also introduce functional errors in memories and dynamic logic. A recent study has shown that direct tunneling current can appear between the Source-Drain Extension (SDE) and the gate overlap. The

phenomenon was called Edge Direct Tunneling (EDT). It can dominate off-state leakage current, especially in very short channel devices [214-215]. This results from the fact that the ratio of the gate overlap to the total channel length becomes large in the short channel devices compared to that of long channel devices. Thus, the gate current effect is expected to become appreciable in ultra-thin oxide, sub-100 nm MOS circuits. This tunneling current is described by equation (4.8), where C_1 and E_0 are constants and E_{OX} is the electrical field across the gate oxide layer [21]:

$$I_{FN} = C_1 \cdot W \cdot L \cdot E_{OX}^2 \cdot e^{\frac{-E_0}{E_{OX}}} \tag{4.8}$$

From the above equation, the gate leakage current is proportional to the gate area, which limits further scaling of the gate.

Using long-channel devices, small drain voltage and large threshold voltage may be considered as possible solutions for gate current leakage, but they are inconsistent with the requirements for high-speed and high-performance circuits. Such circuits need small V_T and L. Historically, every new semiconductor process tends to introduce lower V_T devices, which result in remarkable increase in leakage current. An immediate solution is to use dual V_T processes. With such processes, low-V_T transistors are used in critical paths to reduce delay, high-V_T transistors are used elsewhere to reduce power.

4.3.4 Latch-up

One of the effects that CMOS designers must be aware of, especially as dimensions

shrink, is latch-up. CMOS processes contain parasitic lateral and vertical bipolar transistors. The cross section and equivalent circuit of a typical CMOS device is shown in Figure 4.3. It consists of two cross-coupled common-emitter transistors connected in a positive feedback loop.

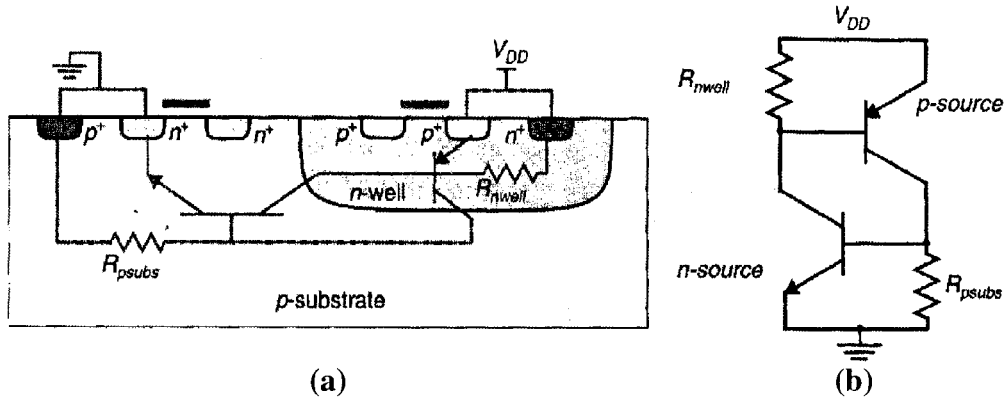


Figure 4.3 : CMOS device cross-section and parasitics responsible for latch-up [12]
(a) Cross-section of transistors, (b) Circuit schematic for parasitics

A latched-up microcircuit is equivalent to a turned-on Silicon-Controlled Rectifier (SCR) between the power supply and ground. Normally, the parasitic transistors are off, however under certain conditions, when there are sufficiently large substrate or well currents or, equivalently, large substrate or well voltage drops, they turn on. As a result, that parasitic device short circuits the power supply. If the power supply does not have a current limit, then excessive current will flow and some portion of the chip may be destroyed. Latch-up was a major problem in early CMOS processes, but now, it is mainly an issue for I/O circuits, with high current demands and possibly noisy voltages.

Avoiding latch-up requires certain layout design rules, and careful process control. Having low-impedance paths between the substrate and well to the power supplies is a

popular approach to avoid latch-up. It can be achieved by having many contacts to the substrate. In addition, any transistor that conducts large currents is usually surrounded completely by guard rings. These guard rings connect the appropriate supply voltage to the substrate for NMOS or n-well for PMOS transistors [92].

4.4 Hot carriers effects

As MOS miniaturization enters the deep sub-micron regime, there is a growing interest in hot-carrier injection mechanisms, along with their associated impact on long-term device reliability [39,83,133,179]. When the device dimensions and power supply voltage are not scaled proportionally, the result is an increasingly high lateral electric field near the drain region. Figure 4.4 illustrates lateral electric field at the channel surface of a NMOS transistor in the saturation region.

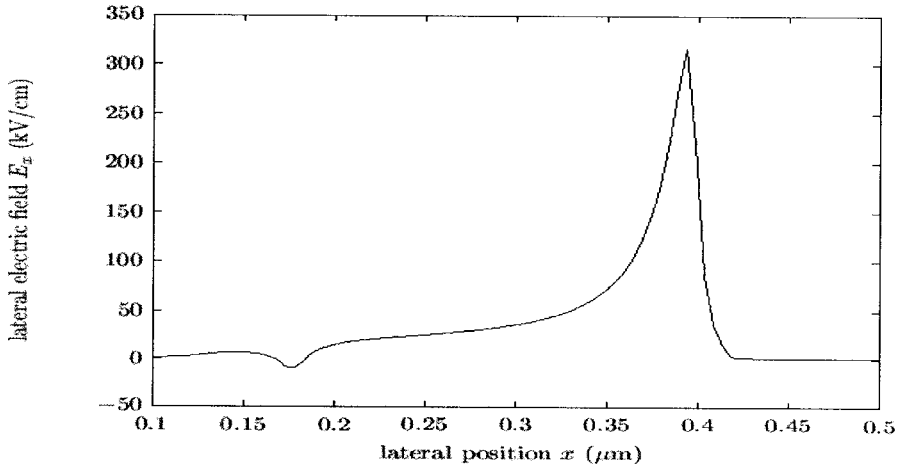


Figure 4.4: Lateral electric field in saturation region [165]

This high lateral electric field at the pinch-off region causes carriers (holes and electrons) to gain enough energy such that they become considerably "hotter" (or more energetic) than the surrounding silicon lattice. If these "hot" carriers possess sufficient energy to surmount or tunnel through the SiO_2-Si interface barrier, they can be injected into the gate and subsequently generate traps, both at the interface and in the oxide. Electron and hole trapping in the oxide cause oxide and interface damage. This damage can result in shifts in the MOS current-voltage characteristics, which may affect circuit performance depending on the particular circuit topology and operating conditions. The mechanisms involved in hot-carrier injection, the relative models, and the impacts of such phenomena on the device and circuit performance (degradations) are deeply studied in appendix B.

4.5 Punch-through

The cross-section of a PMOS in a p-substrate and associated parasitic bipolars are shown in Figure 4.5 with its equivalent schematic.

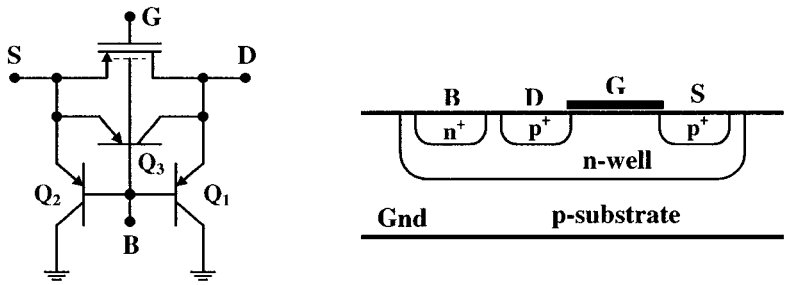


Figure 4.5: PMOS transistor cross-section and parasitics: (a) Schematic of parasitic bipolars, (b) Transistor cross-section [61]

Here, we represent three parasitic elements which are two vertical and a lateral bipolars. The vertical bipolars are always a parasitic leakage, while the lateral bipolar, when the PMOS is ON, can improve its conductance. Of course, when the PMOS is OFF, it is also a parasitic device. The existence of bipolars imply a degradation phenomena called punch-through. This parameter could be defined for all said parasitic transistors. In fact, by scaling down the dimensions, these parasitics tend to become more significant.

Punch-through is a non-destructive mechanism. However, it can cause significant currents passing from drain to source or to the substrate. Such currents imply an increased power consumption and may cause failures. Figure 4.6 shows the maximum drain voltage versus effective channel length for an ion implanted channel device with zero V_{GS} and V_{SB}. Note that rapid decrease in V_{Dmax} for $L_{eff} \leq 1.5$ μm. This is due to punch-through between drain and source [15].

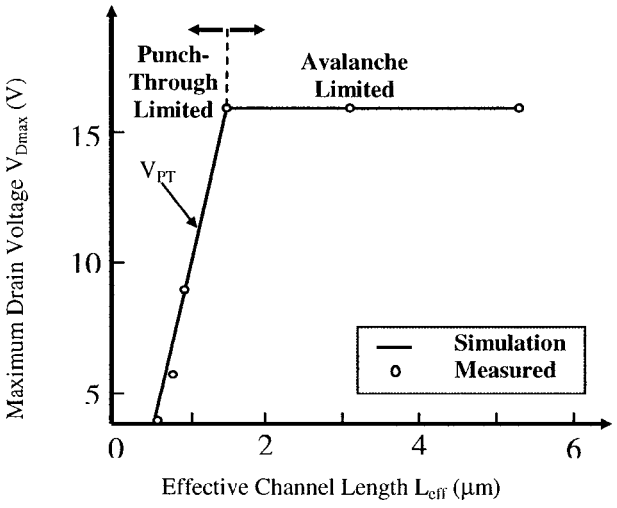


Figure 4.6: Logarithmic plot of V_{Dmax} versus L_{eff} [15]

Containing an oppositely doped region between the source and the drain, the MOS bears a striking physical resemblance to a lateral bipolar junction transistor. Thus, with the distance between the source and drain in a modern MOS reduced to a value comparable to the base width in a bipolar transistor, it is not surprising that phenomena normally associated with the operation of BJTs have been observed. One such phenomenon is the source to drain punch-through. When the source and drain are separated by a few microns, the sum of depletion-layer width for source and drain junctions is comparable to the channel length and thereby, while drain voltage increases, it becomes possible for the p-n junction depletion regions around the source and drain to touch gradually and merge together, as shown in Figure 4.7.

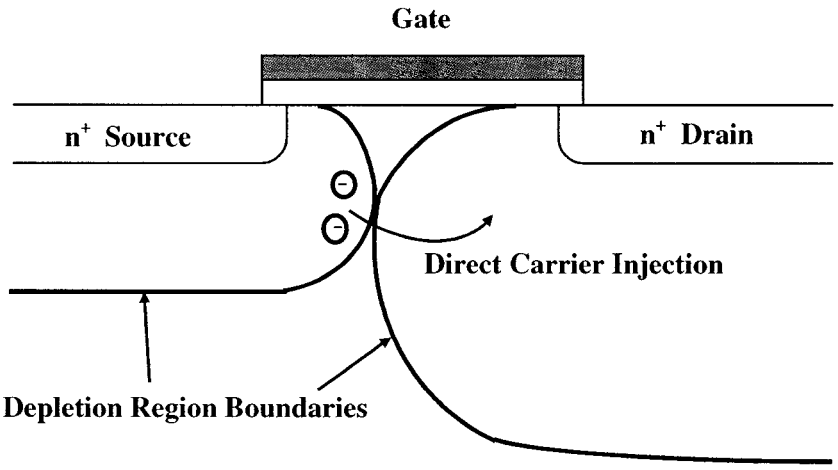


Figure 4.7 : Illustration of Punch-through [139]

As a result, a significant leakage current may flow from the drain to the source through the bulk. Notably, the gate loses control of the subgate region, except for a small portion of the region immediately adjacent to the Si-SiO_2 interface. The source-to-drain current is

then poorly controlled by the gate contact, because it is no longer constrained to the surface channel. The current tends to flow deeper in the bulk and farther away from the gate, through the touching depletion regions. Indeed, the surface potential is strongly coupled to the gate potential, and the highest concentration of the channel doping exists at the surface. Therefore, drain-field penetration is weaker at the surface than in the bulk, and punch-through occurs in the bulk accordingly. The punch-through current adds to the subthreshold leakage current, which leads to an increased power consumption. In reality, for short-channel devices, the maximum allowed drain voltage is determined by the punch-through phenomenon.

4.5.1 Punch-through voltage and current

In order to estimate the punch-through voltage, one should account for the extension of drain- and source-induced depletion regions into the channel. As per MOS fundamentals, depletion width could be expressed as equation (4.9) [176]:

$$W = \left[\frac{2\varepsilon_S\left(V_{bi} - V\right)}{qN_A}\right]^{\frac{1}{n}} \tag{4.9}$$

where N_A is the doping concentration in the channel region, V_{bi} is the built-in voltage across the junction, and n is determined by the shape of p-n junction. The parameter "n" is equal to 2 for one-sided abrupt junctions and is 3 for the linear by graded junctions. Increasing the drain voltage modulates the channel length by modulating the drain- and source-induced depletion layers. The spreading of these depletion layers is described in equation (4.10), assuming that V_D is applied to the drain and that the source is grounded.

$$W_d = W_d(V_D) + W_d(0) = \left[\frac{2\varepsilon_S(V_{bi} - V_D)}{qN_A}\right]^{\frac{1}{n}} + \left[\frac{2\varepsilon_S V_{bi}}{qN_A}\right]^{\frac{1}{n}} \quad (4.10)$$

When the drain voltage reaches a certain value, the punch-through voltage (V_{PT}), these depletion regions touch each other resulting in $L_{eff} = W_d$.

$$L_{eff} = \left[\frac{2\varepsilon_S(V_{bi} - V_{PT})}{qN_A}\right]^{\frac{1}{n}} + \left[\frac{2\varepsilon_S V_{bi}}{qN_A}\right]^{\frac{1}{n}} \quad (4.11)$$

The punch-through voltage for a NMOS with abrupt junction profile, is given by equation (4.12):

$$V_{PT} = \frac{qN_A}{2\varepsilon_S}\left(L_{eff} - \sqrt{\frac{2\varepsilon_S V_{bi}}{qN_A}}\right)^2 - V_{bi} \quad (4.12)$$

Note that the drain voltage must be somewhat larger than the minimum required for the depletion layer to reach the source. It should also be sufficiently large to overcome the source-substrate potential barrier. The substrate bias tends to suppress punch-through by increasing the initial barrier height around the source junction. Therefore, a much more accurate calculation is required. Considering substrate bias, the punch-through voltage for an abrupt junction can be obtained as equation (4.13) [15,184].

$$V_{PT} = \frac{qN_A}{2\varepsilon_S}\left(L_{eff} - \sqrt{\frac{2\varepsilon_S}{qN_A}}(V_{SB} - V_{bi})\right)^2 - (V_{bi} - V_{SB}) \quad (4.13)$$

In addition, the gate voltage can cause perturbations of the electric-field lines near to source, and thereby a fringing-field factor should be inserted [190]. The actual amount of punch-through current depends mainly on the potential distribution under the channel. If the depletion area around the drain well extends too far to the source side, the potential

barrier between source and drain will be lowered and carriers will start to move from source to drain. Analogous to the punch-through current in BJTs, this substrate "space-charge" current varies as the square of the voltage applied between the source and drain ($I_D \propto V_D^2$).

4.5.2 Punch-through improvement techniques

Several approaches can be used to prevent punch-through. As a practical matter, punch-through in small-dimension MOS is routinely suppressed by increasing the doping of the subgate region, thereby decreasing the source-drain depletion widths. However, increasing the substrate doping has the adverse effect of increasing parasitic capacitances. The new approaches make use of deep spatially restricted dopant implantations, such as Delta doping, Halo or Pocket implants [204].

4.6 Breakdown voltages

4.6.1 Channel avalanche breakdown

As the electric field in the channel is increased, due to channel hot electrons, impact ionization occurs. As a result, an exceeding number of holes is generated, which move from source to drain underneath the inversion layer. This hole current forward biases the source-bulk p-n junction. Thus, electrons are also injected as minority carriers into the p-type substrate. These electrons arrive at the drain and again create more electron-hole

pairs through avalanche multiplication. This process, called channel avalanche breakdown, leads to a rapid rise in the drain current independent of gate voltage. It is worthy to notice that channel avalanche breakdown is pronounced when the device is in on-state. Moreover, for short-channel devices, channel-length modulation effect becomes significant and enhances the channel current. This leads the channel breakdown to occur at lower voltages.

4.6.2 Junction breakdown

A reverse-biased junction corresponds to a junction where a negative voltage is applied to the p-doped region. As a junction is reverse-biased, the potential across the semiconductor increases and so does the depletion layer width. The maximum reverse bias voltage that can be applied to a p-n junction is limited by its breakdown voltage, which is characterized by the rapid increase of the current under reverse bias. Two mechanisms can cause breakdown, namely avalanche multiplication and tunneling of carriers through the bandgap. Neither of the two breakdown mechanisms is destructive. However, heating caused by the large breakdown current and high breakdown voltage may destroy the junction unless sufficient heat sinking is provided. Breakdown voltage for one-sided abrupt and linearly graded junctions are determined from the solution of Possion's equation as follows. These breakdowns are respectively given by [176]:

$$V_B = \frac{\varepsilon_C \cdot W}{2} = \frac{\varepsilon_S \cdot \varepsilon_C^2}{2q} \cdot \left(N_B\right)^{-1} \tag{4.14}$$

$$V_B = \frac{2\varepsilon_C \cdot W}{3} = \frac{4\varepsilon_C^{3/2}}{3} \cdot \left(\frac{2\varepsilon_S}{q}\right)^{1/2} \cdot (a)^{-1/2} \qquad (4.15)$$

where N_B is the background doping of the lightly doped side, ε_S is the semiconductor permittivity, ε_C is the critical field and, a is the impurity gradient. Thus, as a first order approximation, the breakdown voltage varies as N_B^{-1} for abrupt junctions and as $a^{-1/2}$ for linearly graded junctions. Furthermore, one has to take into account the radius of curvature of the metallurgical junction at the edges (edge effect). Most doping processes including diffusion and ion implantation yield a radius of curvature on the order of the junction depth. Recall that for highly doped p-n junctions, the dominant mechanism in reverse bias is tunneling. Typically, a CMOS technology is designed such that the reverse breakdown of a stand alone n-p junction is approximately $3V_{DD}$.

For a NMOS transistor, there are two p-n junctions between drain- and source-substrate junctions. P-N junctions for a PMOS transistor are drain- and source-substrate as well as bulk-substrate junctions.

4.6.3 Dielectric breakdown

As the gate-oxide is scaled down, breakdown of the oxide and oxide reliability becomes more of a concern. Higher fields in the oxide increase the tunneling of carriers from the channel into the oxide. These carriers slowly degrade the quality of the oxide and lead over time to failure of the oxide. A simple reduction of the power supply voltage has been used to eliminate this effect. However as gate oxides approach a thickness of 1.5-3

nm, carrier tunneling becomes less dependent on the applied electric field and this problem will require more attention. From the physical point of view, phenomena are the same for both NMOS and PMOS devices, but they may be quantitatively different.

The oxide reliability that is, the ability of a thin film of oxide to retain its insulating properties while subjected to high electric fields for many years, is threatened by breakdown. Breakdown is defined experimentally as a sudden increase in conductance which is often accompanied by current noise. Usually, products last so long that this cannot be verified by direct measurements, and accelerated tests as well as extrapolation procedures are mandatory to determine lifetime.

4.6.3.1 Extrinsic versus intrinsic breakdown

For many years, thermally grown silicon dioxide has been the primary gate dielectric and has demonstrated robustness and effectiveness. For ultra-thin (< 3.0 nm) gate dielectrics, oxynitrides (N incorporated in SiO_2), are used because of their greater immunity to electrical stress and suppression of boron penetration [37,97,111]. Breakdown characterizes the ability of a dielectric to sustain an electrical constraint. The oxide breakdown phenomenon consists of a progressive degradation of the oxide followed by the final dielectric destruction [205]. The expression Time Dependent Dielectric Breakdown (TDDB) is sometimes used to address such an effect.

Damage initiates throughout the interface of the oxide film, but breakdown of the oxide

does not occur uniformly at the entire interface. It usually starts at the location of a defect present in the oxide to form a damage cluster. The damage initiates at anode and cathode and eventually spreads throughout the body of the dielectric. When a critical number of defects is reached, a conductive path is formed through the oxide and oxide breakdown is triggered [175]. Figure 4.8 illustrates the failure process.

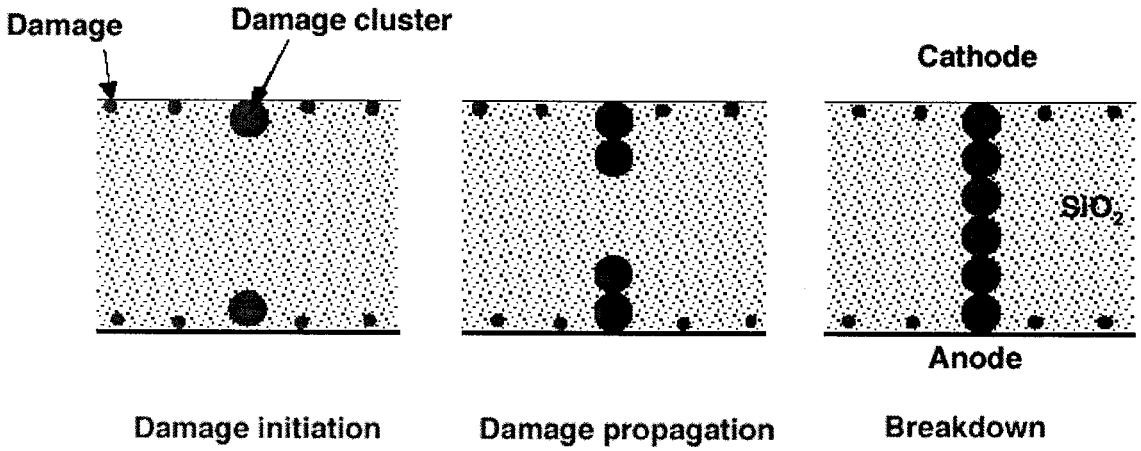


Figure 4.8 : Visualization of oxide breakdown failure [142]

Breakdown by itself is not due to thermal effects but heating can lead to the complete destruction of a local part of the oxide by Joule heating, arising from high current density in a weak spot [205]. In fact, breakdown is the result of a continuous degradation of the volume/interface of the dielectric [52], and is therefore intimately related to preexisting or stress induced defects during constraints. As a result, breakdown is a local phenomenon with a statistical (not deterministic) character that depends on the density of defects already present or to be generated in the oxide. The most commonly used approach for describing the statistics of the breakdown parameters is the Weibull probability density (equation 4.16) [72].

$$f(x) = \frac{\beta}{\eta}\left(\frac{x}{\eta}\right)^{\beta-1} \cdot e^{\left(-\frac{x}{\eta}\right)^{\beta}} \tag{4.16}$$

Where β and η are the shape and scale parameters, respectively. The Cumulative Distribution Function (CDF) of a Weibull distribution is then expressed by equation (4.17):

$$F(x) = 1 - e^{-\left(\frac{x}{\eta}\right)^{\beta}} \tag{4.17}$$

Figure 4.9 shows a typical Weibull plot of CDF, that is ln[-ln(1-CDF)], of the dielectric time-to-breakdown (t_{bd}) obtained on a large number of capacitors.

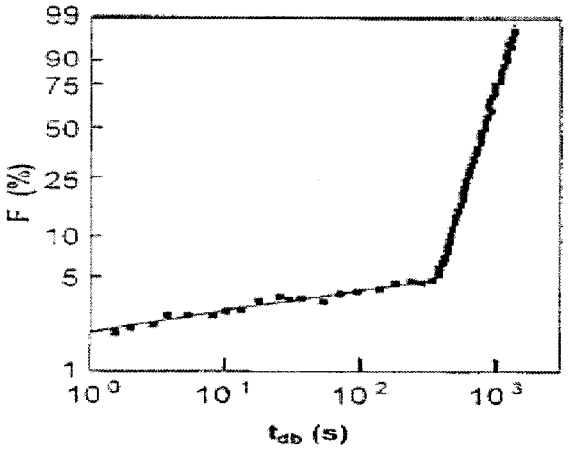


Figure 4.9 : Typical Weibull plot of time to breakdown for MOS capacitors [198-199]

Here, F stands for the cumulative failure rate. In this plot, one can distinguish two types of statistical populations as suggested by the presence of two linear regions. The family of samples with low time to breakdown is associated with "extrinsic" defects characteristics of the oxide, while the family with high time to breakdown is

representative of the "intrinsic" quality of the dielectric. The latter one is therefore related to the microscopic properties of the medium (e.g., bonding energy, lattice strength,...), while the former is associated with point defects induced by the technological processes (impurities, extrinsic defects,...).

Extrinsic failures occur with a decreasing rate over time and are caused by process defects such as contaminants on the crystalline silicon surface, and by surface roughness [46,87,131]. Failure rates generated extrinsically can be reduced by applying a burn-in or voltage screening process to the devices. The failures are accelerated at elevated voltages and temperatures. A clean and contamination free process will generally give only intrinsic breakdown.

Intrinsic failures occur with an increasing failure rate over time and are usually caused by an inherent imperfection in the dielectric material during stress. It is essential that these fails do not occur during the intended useful lifetime of the device when it is operating under specified conditions. The process of intrinsic degradation in gate dielectric begins with trap creation and formation of interface states as the device gate dielectric is stressed at elevated voltages and temperatures. The creation of these defects continues with the injected current (and therefore time) until the defect density reaches a critical value, after which dielectric breakdown occurs.

Parameters that affect when and how the dielectric breakdown occurs include the applied

stress voltage, temperature, dielectric thickness, device dielectric area, and intrinsic dielectric lifetime. Achieving highly reliable functional integrated circuits must include taking appropriate measures against both extrinsic and intrinsic failures mechanisms in random or systematic measurements [4].

4.6.3.2 Breakdown improvement

The end of the road for SiO_2 films used as gate oxides in MOSFET is already being anticipated for the next decade. The electronic structure at the atomic scale seems to limit practical oxide thickness to 0.7–1.2 nm [120]. This is a fundamental limit that cannot be overcome by technological improvements, and it will determine the end of SiO_2 gate oxide's downscaling, unless other limitations impede the use of these atomic scale films. Using oxides other than silicon dioxide, the so called high-k dielectrics, presenting better k/V_{BD} ratios than SiO_2, is a possible solution, but they mostly suffer from more complex process integration and usually have smaller bandgap, resulting in increased low-field leakage.

The use of lightly-doped drain region can be extended to increase the drain breakdown voltage. Combining this approach with the use of circular drains layout can typically increase the breakdown voltage by 2-4 V [38]. However, these solutions imply new challenges with respect to layout drawing and other circuit characteristics, which makes the case open for further challenges.

4.7 Stress-induced measurement techniques

The degradation and breakdown traditional characterization techniques consists in applying static dc voltage/current stresses [123]. However, there are valid reasons to employ dynamic stresses for reliability assessments. First, they are much faster and decrease the assessment costs accordingly. Moreover, it better corresponds to the real environment. Indeed, MOS devices experience time-varying bias in normal operation. As a consequence, it is worth studying their degradation and breakdown using dynamic stress experiments [74-75,104].

It is found that oxide degradation mechanisms under constant voltage/current stress is different from that under ramped voltage [109]. Under constant stress, first, positive charges are generated and accumulated in the oxide. These positive charges enlarge the field at the cathode, then more electrons are injected into the oxide. As time goes on, the probability of electrons being trapped increases, negative charges center appear and grow, leading to oxide breakdown. But under ramp stress, the mechanism that affects and controls the lifetime of oxide is different. Hence, the generation and accumulation of positive charges in oxide is the main reason, which forms positive feedback and causes the oxide breakdown in a very short time.

Several kinds of testing methods have been introduced to characterize breakdown in thin oxides. They can be classified according to the constraint type applied to the structure. Table 4.1 summarizes characteristics and features of each electrical stress.

Table 4.1: The specifications of electrical stress methods [66]

Electrical Stress	Constant Current (CCS)	Constant Voltage (CVS)	Linear Ramp Voltage (LRVS)	Exponential Ramp Current (ERCS)
Stress type	I	V	V	I
Monitored Parameter	V(t)	I(t)	I(t)	V(t)
Breakdown criterion	-20% on V or slope change	I > threshold or slope change	I > threshold or slope change	-20% on V
Output	t_{bd}, Q_{bd}	t_{bd}, Q_{bd}	E_{bd}	Q_{bd}
Q_{bd} density	t_{bd} . I/S	$\int I(t) \cdot d(t) / S$	---	$\int I(t) \cdot d(t) / S$
Advantages	Fast method, sensitive to extrinsic and intrinsic breakdown, good sensitivity to extrinsic defects	Very sensitive close to normal operation	Fast method	Very fast method, sensitive to extrinsic and intrinsic breakdown
Limitations	Series resistance dependent	Slow method, Series resistance dependent	Weak sensitivity to intrinsic properties, Series resistance dependent	Series resistance dependent

4.8 Summary

In this chapter, the main characteristics of MOS scaling in deep sub-micron regime were presented, and the impact of such scaling on the device and circuit characteristics were revealed. Phenomenon such as short-channel and narrow-channel were explained briefly, while a detailed study on short-channel effects was provided in appendix A. Another reliability issue, named hot-carrier injection, was also reviewed and relative mechanisms, models and associated degradations reviewed in Appendix B. The effect of breakdown,

including channel avalanche, junction and oxide breakdown voltages, was also covered in this chapter. The overview of breakdown mechanisms and models for oxide breakdown is covered in detail in appendix C. Furthermore, the different accelerated test structures for reliability purpose of MOS devices were addressed in the last sections.

Throughout this chapter, it was clarified that the down scaling of MOS devices has a significant impact on device and circuit characteristics, and the performance of the semiconductor is remarkably dependent on those issues. Therefore, measurement of parameters such as oxide and junction breakdown voltages could help to characterize the new sub-micron MOS technologies. This could lead to improved design methods for reliable devices and circuits.

Chapter 5

Quantitative, simulation and measurement results

We report in this chapter the main results from: 1) The analytical comparison between different power conversion chain architectures with respect to the required power and overall power efficiency, 2) The simulation of the high efficiency Multi-Stage Voltage Multiplier (MSVM), 3) The measurement of MOS devices characteristics under voltage stress.

5.1 Quantitative results for power conversion chains

The different architectures for a PCC, as discussed in chapter 2, were analyzed to calculate the amount of required power at the input stage of various power chains and their overall power efficiency. These architectures were designed to produce the maximum needed voltage, that is 10 V, as required by a multi-channel cortical stimulator such as the stimulator developed by PolyStim.

Table 5.1 shows all the assumptions for circuit parameters of such PCC. The term "worst case" means that the assumptions are valid for the case where all the stimulation channels present simultaneously the highest reported electrode-tissue contact impedance of almost 100 kΩ, while requiring a certain amount of current per channel, that is 100 μA.

Table 5.1: The assumption and circuit parameters for analytical study

Component	Assumptions
Cortical stimulator (25-channel)	I_S = 2.5 mA (worst-case) I_C = 0.5 mA
Voltage Multiplier stage (voltage doubler)	power efficiency = 75% voltage conversion = 90%
Voltage Regulator (VR)	power efficiency = 85%
Diode Rectifier (DR)	V_γ = 700 mV
SSR Switching Frequency	f_s = 15 MHz
PMOS Dynamic Resistance	R_{ON} = 10 Ω
Input Voltage to the Chain	V_I = 2.72 V

This analysis takes into account that voltage multiplication ratio in voltage doubler stages are reduced from an ideal factor of 2 to a real value of 1.8. This is due to non-idealities in the said stages, such as charge sharing between the stray and charge pump capacitors. Table 5.2 summarizes the applied mathematical equations used in order to calculate the required input current and power for each PCC architecture. These have been derived from the schematics shown in Figures 2.1, 2.4 and 2.5.

Table 5.2: Input current and power equations for various PCC architectures

PCC Architecture	Input Current	Input Power
Conventional	$I_T = \left(\frac{I_S}{\eta_{MSVM}} \times \frac{V_{MSVMO}}{V_{MSVMI}}\right) + I_C$	$P_I = \frac{1}{\eta_{VR}} \cdot \left(\frac{P_{MCS}}{\eta_{MSVM}} + P_{Core}\right) + V_\gamma \times I_T$
Distributed	$I_T = \left(\frac{I_S}{\eta_{MSVM}} \times \frac{V_{MSVMO}}{V_{MSVMI}}\right) + I_C$	$P_I = \left(\frac{P_{MCS}}{\eta_{MSVM}} + R_{ON} \times I_S^2\right) + \left(\frac{P_{Core}}{\eta_{VR}} + V_\gamma \times I_C\right)$
Monolithic	$I_T = \left(\frac{I_S}{\eta_{MSVM}} \times \frac{V_{MSVMO}}{V_{MSVMI}}\right) + I_C$	$P_I = \frac{P_{MCS}}{\eta_{MSVM}} + \frac{P_{Core}}{\eta_{VR}} + R_{ON} \times I_T^2$

Using the assumptions and equations stated in Tables 5.1 and 5.2, the results of Table 5.3 are obtained. It is worthy to note that taking practical values for circuit parameters, the switching losses are negligible compared with the conduction losses of the SSR and hence, are not included in the tables.

Table 5.3: Required voltage and current for PCC architectures

PCC Architecture	$V_{Input\text{-}Min}$ (V)	No. of stages (MSVM)	V_{Core} (V)	I_{Input} (mA)
Conventional (Figure 2.1)	2.72	3	1.72	35.31
Distributed (Figure 2.4)	3.23	2	2.15	14.99
Monolithic (Figure 2.5)	3.23	2	2.62	14.99

Considering the voltage drop in circuit elements of the conventional architecture, boosting the same 2.72 V peak input voltage to the desired 10 VDC output voltage requires a 3-stage MSVM, while the other proposed topologies require only two stages. This improvement increases the overall power efficiency of the MSVM module, while significantly reducing the voltage drop across these stages. It is remarkable that to produce the same V_{MSVMO}=10 V, even by reducing the number of stages in the MSVM, the minimum required input voltage is still low. This is partly due to voltage drops across the DR. Options in the PCC architecture significantly affect the performance of an electronic implant from power and efficiency points of view, as shown in Table 5.4. These results show that the two proposed architectures reduce the power requirements for

electronic implants, and significantly increase their overall power efficiency. The monolithic approach also removes the need for off-chip diodes, which is a significant improvement in facilitating electronic implant integration.

Table 5.4: Power and efficiency of various PCC architectures

PCC Architecture	P_I (mW)	Rectifier	P_{Core} (mW)	$\eta_{Overall}$ (%)
Conventional	95.76	Off-chip	0.86	27.01
Distributed	48.36	Combined	1.08	53.93
Monolithic	48.43	On-chip	1.31	54.33

As mentioned earlier in chapter 2, the input voltage to the power chain is subject to remarkable changes which could range between 0-10 V. This is due to modulation techniques (such as ASK) or changes in the distance and orientation between the electronic implant and the remote controller. Of course, below some voltages, the EI may not work properly. Variations of input voltage could degrade the overall PCC power efficiency significantly. Figure 5.1 shows this for the 2-stage conventional architecture.

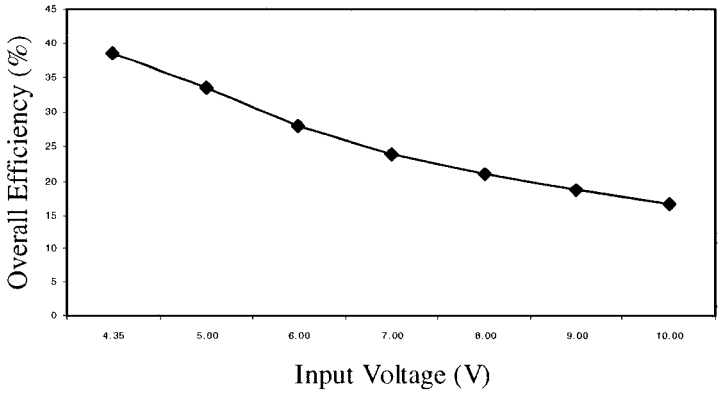


Figure 5.1: Power efficiency vs input voltage for the 2-stage conventional architecture

The proposed architectures which benefit from SSR modules are expected to be more tolerant against input variation by controlling the conduction angle of the rectifier as a function of the load power requirements. For all PCC structures, voltage ripples in the input of the voltage multiplier module are expected. Consequently, voltage fluctuations at stimulation sites – at least for some transient periods - is predictable. Flattening voltage ripples could be a challenge while designing a SSR. Recall that delivering large load currents (few mA) requires very large capacitors and/or high clock frequencies. External capacitors can give a very low ratio between the stray capacitor and the charge pump capacitor ($\alpha = C_S/C$) [61]. They also imply lower frequencies and thus, a lower dynamic loss in the switches which leads to an increase in power efficiency.

5.2 Simulation results for multi-stage voltage multiplier

A high efficiency single stage voltage doubler (multiplier) was designed based on chapter 3. The schematic of the circuit is shown in Figure 5.2. The non-overlapping clock generator of Figure 3.8b and the level shifter of Figure 3.9 were also used. As was discussed in chapter 3, several parameters can affect the characteristics of the voltage doubler. The impact of each factor was studied by conducting SpectreS simulation with the technology file of the TSMC 0.35 μm CMOS fabrication process. The simulation was run using $V_{IN} = V_{CLK} = 1.5$ V, $L_{MIN} = 1.4$ μm and $(W/L) = 10$.

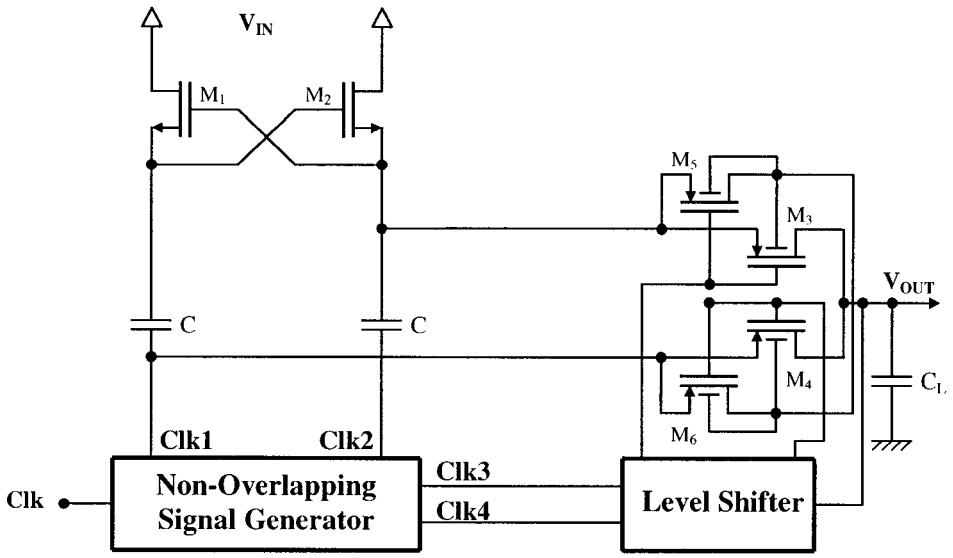


Figure 5.2: The schematic of a single stage voltage doubler

5.2.1 Impact of charge pump capacitors

The amount of stored and pumped charges is a key issue in the design of a charge pump stage. As the amount of the stored charges is proportional to the capacitor size, a strong relationship is expected between the output voltage and the capacitor size. Figure 5.3 shows the output voltage for different values of charge pump capacitors. In those simulations, the clock frequency was 10 MHz. Recall that internal capacitances larger than 20 pF are excessively large for deep sub-micron CMOS technologies. As we see, the output voltage is not linearly proportional to the charge pump capacitance. In fact, large capacitances result in more stored charges that increase the load current handling capability. However, such an increase requires large integrated circuits area, which increases the associated stray capacitance and corresponding increase of the charge sharing phenomenon. The latter degrades power efficiency. This reduces the voltage and

power efficiency of the charge pump stage. Furthermore, there is a secondary impact of large capacitor on the settling time of the stage. The larger the charge pump capacitor, the slower the tracking of input voltage by the output.

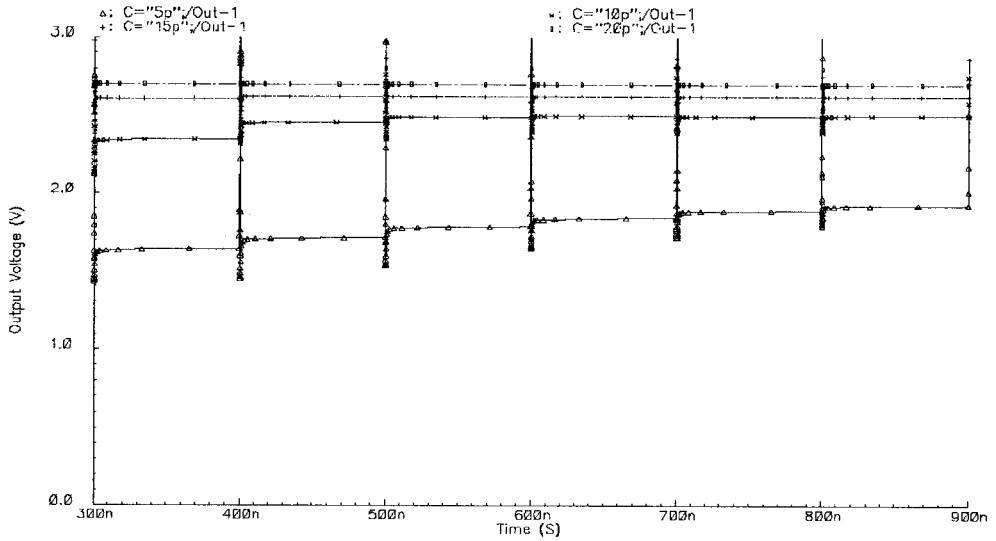
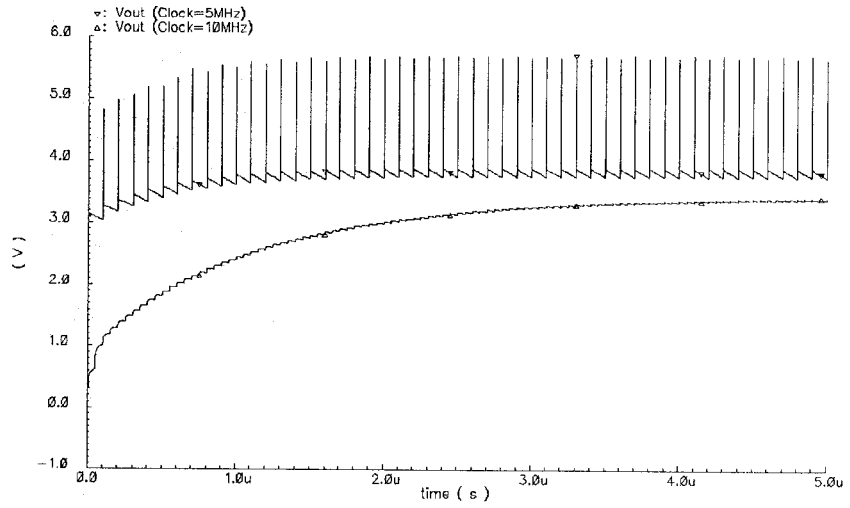


Figure 5.3: Output voltage vs charge pump capacitor size

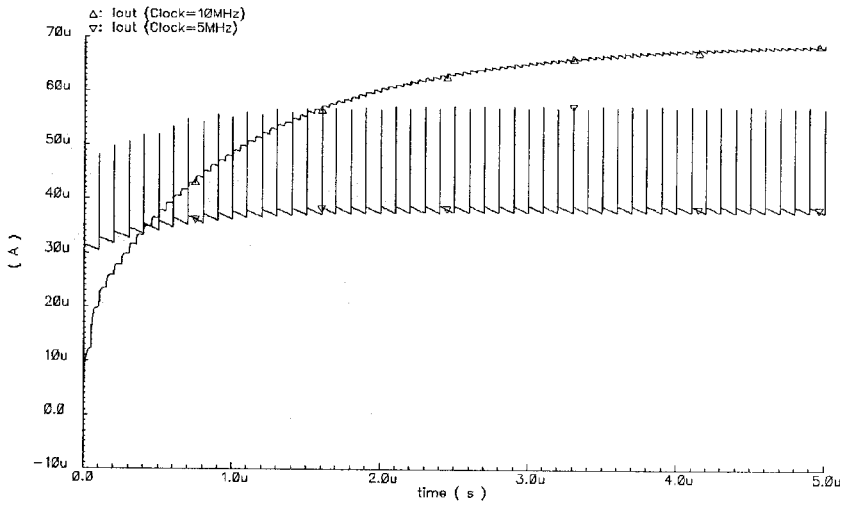
5.2.2 Impact of clock frequency

The amount of stored charge in each stage, which are eventually pumped to the following stage, is also proportional to the switching clock frequency. Therefore, increasing the clock frequency is expected to improve the load handling capability. Figure 5.4a and b illustrate the output voltage and current respectively of a single-stage charge pump for different clock frequencies, while charge capacitors, C, of 20 pF are employed. Here, an output capacitor C_{OUT}=100 pF was used to smooth the output ripples. Note that for output stages where a large voltage is applied to the capacitors, high frequency clocking prevents complete charge and discharge of the charge pump capacitors, which decreases

the power efficiency. As per prior prediction, by increasing the clock frequency, the load current handling is improved. However, higher clock frequency calls for higher dynamic (switching) losses in the switches, which degrades the efficiency accordingly.



(a)



(b)

Figure 5.4: Characteristics of the single stage charge pump vs clock frequency
a) Output voltages, b) Output currents

5.2.3 Impact of transistors dimensions

As per MOS fundamental equations, the larger the transistor, the lower its resistance in the triode region. Therefore, a doubler is expected to have higher power efficiency when wider switches are used. However, very large transistors are associated with parasitic capacitances that can degrade the performance and efficiency of the circuit at high clock frequencies. Figure 5.5 shows the impact of charge pump transistor width on the power efficiency. Here, we have used a clock frequency of f =10 MHz and C_{OUT}=100 pF.

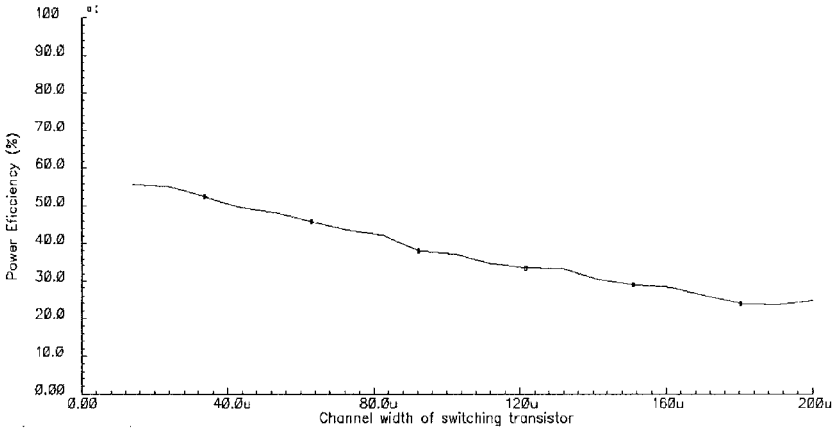


Figure 5.5: Power efficiency versus the charge pump switch width

In the cases simulated here, increasing the width of the transistors operating as charge pump switches significantly reduces power efficiency.

5.2.4 Impact of clock overlapping

Proper clocking is an important factor to maintain the charge in the charge capacitors and deliver it to the following stages. As a matter of fact, the clock levels applied to the gates

of the series PMOS switches of Figure 5.2 should be non-overlapping during the low period of clock, forcing them to be active one at a time, while the clocks applied to the plates of the charge capacitors should be non-overlapping during their high period, thus preventing the charge stored to be stolen by the active NMOS transistor to which it is connected.

5.2.5 Multi-stage voltage multiplier

An overview of a conventional multi-stage voltage multiplier is shown in Figure 5.6. Here, the structure consists of a chain of five cascaded voltage doublers. Each doubler includes a charge pump, a non-overlapping clock generator and a level shifter. A common clock signal, also feeds all the chain elements.

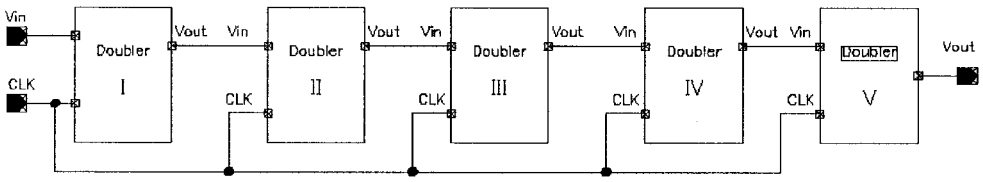


Figure 5.6: 5-Stage Conventional Voltage Multiplier

Using such a topology, one may expect to have the output of each stage lifted by the amplitude of the incoming clock signal to the same stage. Figure 5.7 shows the output of a five-stage voltage multiplier using a clock amplitude of 1.5 V applied to all stages.

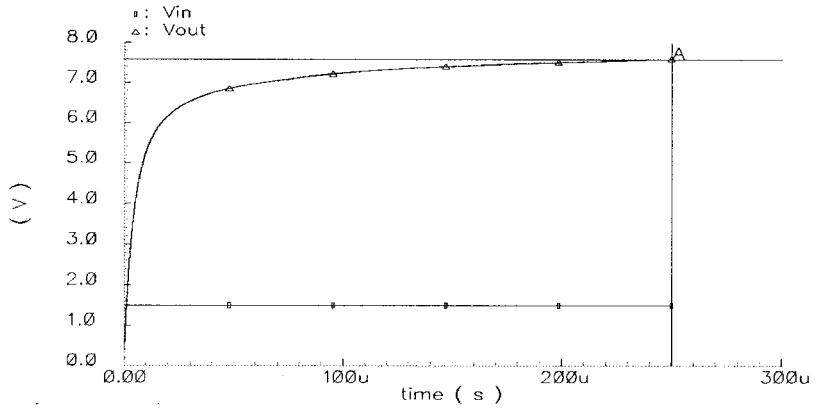


Figure 5.7: The output voltage of 5-stage voltage multiplier

It should be noted that using the TSMC CMOS 0.35 μm process, the maximum voltage applicable between gate and source/drain terminals is limited to 7.7 V and the SpectreS simulator warns for gate oxide breakdown beyond the said limit. The comparable limit is approximately 4.6 V for TSMC 0.18 μm process. Therefore, it seems essential to experimentally characterize realistic oxide and junction breakdowns, as well as punch-through events for the new sub-micron technology.

5.3 Voltage limits; Experimental results

In order to confirm the feasibility of delivering much higher DC voltages than the nominal process supply, a study was conducted to characterize MOS devices under voltage stress conditions. Special attention was paid to measuring the p-n junction reverse breakdown voltage, gate oxide breakdown voltage and punch-through voltage for the TSMC 0.18 μm CMOS process.

5.3.1 Test protocol

In order to extract reliable results from limited number of samples, a systematic measurements protocol is required. The following issues were outlined for the characterization of the MOS under voltage stress conditions.

a) The stress parameter is the voltage, and a compliance parameter, that is current is used as an imposed limit, sensed in order to prevent rapid destruction. Therefore, a great deal of attention was paid to avoid stimulating undesired phenomena. This was performed by measuring all relevant currents when the device may be subject to more than one breakdown phenomena in some tests.

b) The tests are categorized to be destructive or non-destructive. As the device characteristics are degraded significantly after destructive tests, they are ordered such that the non-destructive tests take earlier place. Therefore, the punch-through and p-n junction reverse breakdown tests are accomplished earlier than the gate oxide breakdown. Using this methodology, the same samples could be used for both tests, which alleviate requirements for large number of samples.

c) The tests are effected at the ambient temperature (25 °C), and accelerated tests to characterize reliability based on Arrhenius equation are not effected. This is due to constraints of multi-project shuttle manufacturing; the number of devices was not sufficient to conduct reliability tests.

d) The tests must start with the nominal process supported voltages and be followed in an increasing order as long as compliance is met, or some forbidden phenomena occurs. A programmable power supply generates the DC sweep voltage with the step size of 0.1 V. This provides adequate precision in the measurements, while tests take a reasonable period of time.

e) The compliances are set at values where some phenomenon has clearly happened. For example, 1 mA for destructive tests, while 1 μA is used for non-destructive tests. The former is such that heating caused by flowing currents do not damage the junction, while the latter ensures oxide degradation have led to hard breakdown. The latter also is within the current range required for our application.

f) All chips were numbered individually, testing started with a certain size of transistors, and repeated for at least 4 samples of the same size. This is to ensure acceptable accuracy with the limited number of samples considering the random nature of some breakdown mechanisms.

g) The test order and procedure was the same for all tests and samples in order to prevent the measured values from being affected in an uncontrolled way by history-dependent breakdown mechanisms.

h) The drain-bulk and source-bulk junctions are assumed to have exactly the same

characteristics. This is valid if one considers their layout symmetry.

Figure 5.8 depicts the measurement procedure flow chart for a MOS device under voltage stress conditions. The measurement is initiated by setting up the circuit such that only the desired phenomena happens. The initial voltage is the process nominal supply voltage. It is applied to respective device terminals and the current flow is measured at certain terminals. The measured current is then compared to the compliance. In case the current is less than the said limit, the procedure continues by increasing the applied voltage according to a predefined step size. Otherwise, the measurement is stopped and the latest applied voltage is registered.

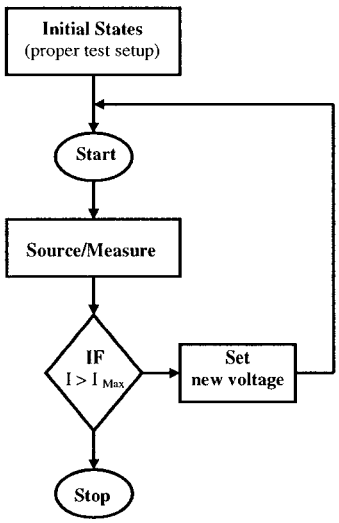


Figure 5.8: Measurement procedure flow chart

A Keithley 236 Source Measurement Unit was used to implement the above procedure, and several Keithley 2002 Digital Multimeters were used for current measurements.

5.3.2 Test structures

The MOS device is subject to different breakdown phenomenon. Figure 5.9 illustrates the cross-section of a PMOS transistor implemented in a n-well process. The probable undesired phenomenon are also shown in the figure that includes P-N junction reversed-bias breakdown, gate-oxide breakdown and punch-through (lateral and vertical) events. Here, ESD protective diodes are not shown.

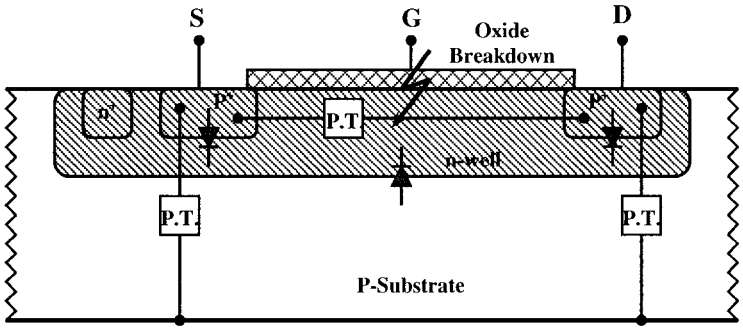


Figure 5.9: Cross-section of PMOS transistor and relative parasitics

As was clarified earlier, using proper test structures has a significant impact on the accuracy and the validity of the measurements. For some cases, more than one structure can be used for the desired measurement. In such case, we have considered possible differences. Both type of transistors (PMOS and NMOS) were fabricated using 3.3 V and 1.8 V versions of the TSMC 0.18 μm process, respectively. However, as the focus of the measurement is on PMOS transistors, due to their application as series switches with no threshold constraint, they were implemented in a wider range of lengths and widths than NMOS devices. The length of PMOS transistors were 0.30, 0.45, 0.90, 1.35 and 1.80 μm, and the experimented width are 3, 30 and 750 μm, while NMOS transistors were made

with lengths of 0.45, 0.90 and 1.80 μm and a width of 30 μm. It is worthy to notice that all device terminals are accessible from chip pins through an Electro-Static Discharge protection circuit with a series resistance limiting the flowing current (ESDR), except for global substrate, which is connected directly to V_{SS}. Figure 5.10a and b show the cross-section of the protective diodes to V_{DD} and V_{SS} respectively, and (c) is for the overall schematic. Note that a 187 Ω resistance implemented using the poly layer in series with the signal is not shown for simplicity.

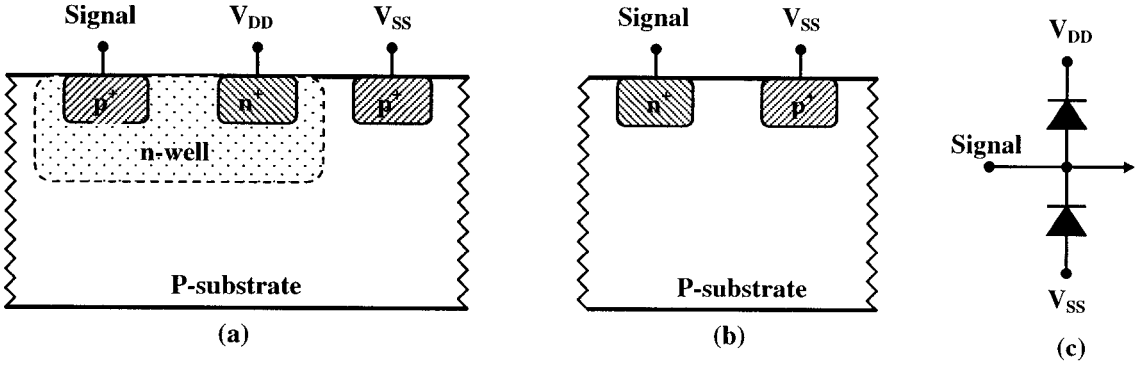


Figure 5.10: The cross-section and schematic of ESDR protection [3]: (a) to V_{DD}, (b) to V_{SS}, (c) both

A few pins were connected exclusively to the ESDR rings and not routed to the internal devices, the protection diodes were characterized in terms of reverse voltage breakdown, as shown in Table 5.5.

Table 5.5: ESDR Reverse Breakdown Voltage

ESDR Protective Diode	Reverse Breakdown
Signal to V_{DD}	10.4 V
Signal to V_{SS}	10.6 V

5.3.2.1 P-N junction reverse breakdown voltage

a) P_{sub}-N_{diff} junction

The p-n junction of a diffusion region and substrate was examined in a NMOS transistor. In order to measure the reverse breakdown voltage of the said junction, two different setups were used, as shown in Figure 5.11. Here, the main difference is that for setup (a), different voltages at gate and bulk implies that a channel is formed, while for setup (b), the channel is not formed yet.

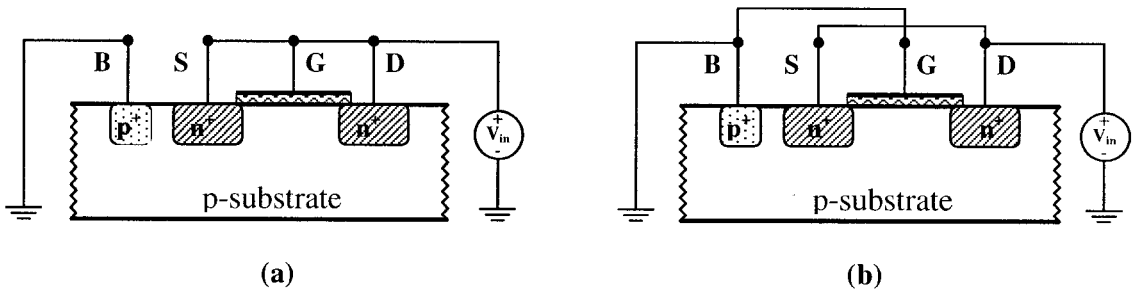


Figure 5.11: Different setups for P_{sub}-N_{diff} junction reverse breakdown: a) with formed channel, b)without channel

Using the above settings, the symmetric drain-substrate and source-substrate junctions are in reverse bias while the device is in its cut-off region ($V_{GS} \leq 0$). Furthermore, having drain and source at the same potential prohibits punch-through. A DC voltage sweep was applied to the common terminals and the current flowing out of Bulk was measured. For the first setup, a drawback is the possibility of further gate oxide breakdown occurrence. Therefore, an extra multimeter was installed to observe the current flowing through the gate. However, no gate current was measured before junction breaks. Table 5.6

summarizes the measured reverse breakdown voltage using different setups for a variety of NMOS devices designed using the of 1.8 V layout rules.

Table 5.6: The P_{sub}-N_{diff} reverse breakdown vs channel length for different setups

Transistor Length (μm)	Breakdown Voltage Setup (a) (V)	Breakdown Voltage Setup (b) (V)
0.45	8.8	3.4
0.90	8.6	3.4
1.80	8.4	3.4

Note that the measured reverse breakdown is independent on the transistor geometry. The difference between the results of setups (a) and (b) can be justified by the fact that the channel formed in the first setup could change the carrier distribution in the channel and affect the junction reverse breakdown. Another test setup may not have the problem of the above structures. It consists of leaving the gate terminal open. This was not used because of instability of the said terminal and the possible charge accumulation on the gate, which may cause an instantaneous conduction.

It is worthy to notice the difference between the measured values for the P_{sub}-N_{diff} junction breakdown, compared to values already measured for the ESDR protection diodes. At first glance, it appears to be the same layer structure. However, the doping concentration in the channel underneath the gate is remarkably larger than the doping density out of the channel [186]. As the junction reverse breakdown is inversely

proportional to the doping concentration at the lighter doping region, the reverse breakdown for diffusion-substrate junction is lower than that of the same junction for ESDR diodes.

b) P_{sub}-N_{well} junction

The P-N junction of substrate-well was also examined in a N-well PMOS transistor. Figure 5.12 illustrates the test setup used to measure the reverse breakdown of the said junction.

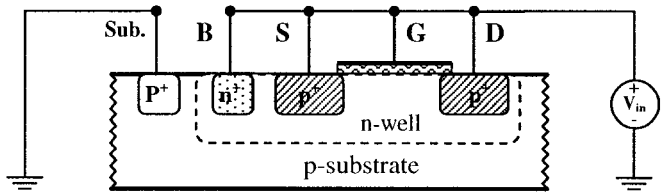


Figure 5.12: Test setup for P_{sub}-N_{well} junction reverse breakdown voltage

Using the above setting, drain, source, gate and bulk are at the same potential to prevent drain to source conduction, drain to source punch-through, forming the channel and diffusion-well junction reverse breakdown, as well as oxide breakdown. In fact, only the N_{well}-P_{sub} junction is subject to reverse breakdown. For this test, a DC sweep voltage was applied to the common terminals and the current flowing out of substrate was measured. Table 5.7 illustrates the measured breakdown voltage for different sizes of PMOS devices when compliance of 1 μA was met.

Table 5.7: The P_{sub}-N_{well} reverse breakdown voltage vs channel length (3.3 V layout rules devices)

Transistor Length (μm)	Transistor Width (μm)	Breakdown Voltage (V)
0.30 – 1.80	3.0	10.0
0.30 – 1.80	30	10.0
0.30 – 1.80	750	10.0 – 10.1

The results comply with prior expectation and prove that the reverse breakdown of the said junction is independent on the dimensions of the device. Recall that there are ESDR protection diodes located between each terminal including bulk and the V_{SS}. As the results are comparable with the reverse breakdown of the said diodes, it is not clear whether this is P_{sub}-N_{well} reverse breakdown voltage or breakdown of the ESD diode.

c) N_{well}-P_{diff} junction

The P-N junction of a diffusion-well was examined in a PMOS transistor by using two different setups. Figure 5.13 illustrates the relative setups used to measure the reverse breakdown of the said junction.

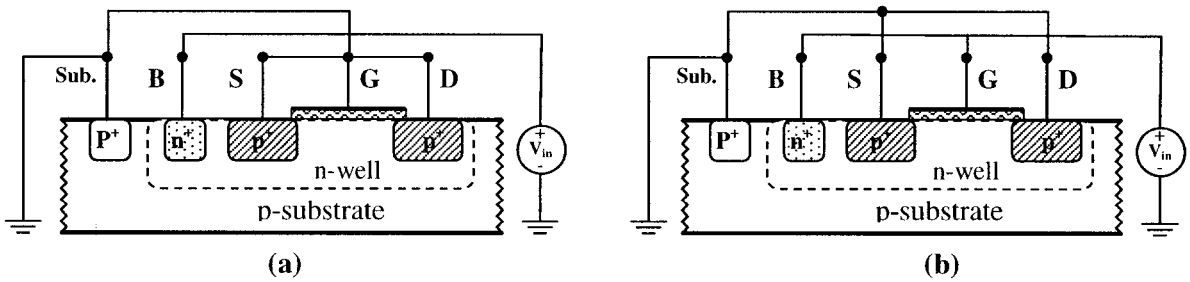


Figure 5.13: Test setup for N_{well}-P_{diff} junction reverse breakdown voltage (a) with formed channel, (b) without channel

Here, the main difference is that for setup (a), different voltages at gate and bulk imply the formation of a channel, while for setup (b), no channel is formed. Using these setups, where drain, source and substrate are connected together, prevents lateral and vertical punch-through to occur while the device is in cut-off region ($V_{GS} \geq 0$). Both setups are subject to well-substrate junction reverse breakdown.

The DC sweep voltage was applied to the bulk terminal of both structures, and the current flowing out of common terminals was measured. The first setup is also subject to gate oxide breakdown (surface) while the second structure is constrained by gate oxide breakdown at edges. So, we have installed extra multimeters to measure the current flowing through gate and substrate. The results of this current monitoring proved that the drain/source to bulk junction breaks earlier than the others, and no gate current was measured before the said junctions conduct. Table 5.8 summarizes the results of our measurement.

Table 5.8: The N_{well}-P_{diff} reverse breakdown voltage vs channel length (3.3 V)

Transistor Length (μm)	Transistor Width (μm)	Breakdown Voltage Setup (a) (V)	Breakdown Voltage Setup (b) (V)
0.30 – 1.80	3.0	7.1-7.3	8.0
0.30 – 1.80	30	6.7-6.9	8.2
0.30 – 1.80	750	5.8-6.1	8.0

The difference between the results of setups (a) and (b) is believed to be due to carrier distribution in the channel and diffusion regions. The dependence to geometry of junction

breakdown in the second setup confirms the influence of carrier distribution. Comparing this result with what is presented in subsection (a) for P_{sub}-N_{diff} of NMOS transistors, we see that the junction breakdown occurs at lower voltages, since the doping concentration in the channel for 3.3 V devices is considerably higher than that of 1.8 V devices. Recall that NMOS transistors are implemented using 1.8 V design rules while PMOS transistors layout was drawn using 3.3 V design rules.

5.3.2.2 Punch-through voltage

a) Lateral (drain to source) punch-through voltage

The lateral punch-through occurs in NMOS and PMOS devices by the same mechanism already explained in the previous chapter. Here, we measure the punch-through voltages for different types of transistors using separate setups.

a.1) NMOS transistor

The lateral punch-through voltage of NMOS transistors was measured using the test structure shown in Figure 5.14. Recall that the layout of these transistors were drawn using 1.8 V design rules.

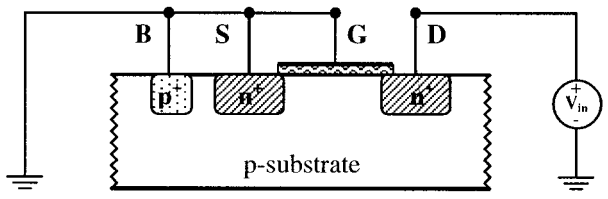


Figure 5.14: Test setup for lateral punch-through voltage in NMOS

Using this setup, having source and gate at the same potential forces the transistor deep into cut-off region. It prevents the source to substrate junction to be in reverse breakdown condition. While the transistor is off, different voltages are applied to the drain terminal in order to provide the essential condition for stimulation of punch-through events. However, voltage differences between drain and gate terminals prepare the condition for an undesired phenomena, the oxide breakdown at gate edges. Furthermore, the above setup presents the drain to substrate junction in reverse breakdown condition. Therefore, extra multimeters were installed on the gate and bulk to monitor the flowing current into the gate and out of the substrate. Moreover, connection of gate and bulk to the same voltage prevent channel formation and therefore, the carrier distribution in the channel remains unchanged.

During measurement, there was no current flowing through gate or out of source and, the current was only measured at the bulk. This means that using this test structure, drain to bulk junction reverse breakdown occurs earlier than punch-through and oxide breakdown. This junction breakdown was found to be 3.5 V for all lengths of NMOS transistors.

The reason why punch-through voltage could not be measured by this setup can be justified by recalling the fact that punch-through voltage is described to be in reverse square power to channel length. So, in this case, where device channel lengths are several times larger than technology feature size, punch-through should occur at voltages several

times higher than nominal operating voltages, that are beyond the oxide and junction breakdown voltages.

a.2) PMOS transistor

The lateral punch-through of PMOS transistors was also measured using the test setup illustrated in Figure 5.15. In the case, the layout of transistors were again drawn using 3.3 V design rules.

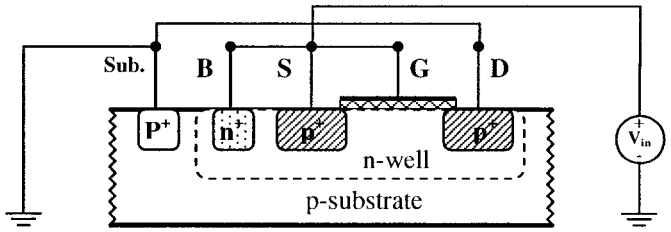


Figure 5.15: Test setup for lateral punch-through voltage in PMOS

Here, the device is subject to probable gate oxide breakdown at drain edge, as well as drain to bulk and n-well to global substrate reverse breakdowns. The advantage of such structure is that the channel is not formed and therefore, the carrier distribution in the channel, which has a significant impact on punch-through, remains unchanged. The vertical punch-through between source and global substrate is also a possibility. Therefore, extra multimeters were installed on the gate, bulk and substrate to monitor the currents passing through the said terminals. Table 5.9 depicts the measured breakdown voltages for different PMOSs. There was neither current flowing out of substrate, nor through gate, nor from drain to source. Therefore, none of n-well to substrate junction

reverse breakdown, lateral or vertical punch-through have occurred. The current was exclusively flowing out of the well, which proves that drain-well junction reverse breakdown occurs earlier than the others.

Table 5.9: Measured voltages in lateral punch-through setup for PMOS (3.3 V)

Transistor Length (μm)	Transistor Width (μm)	Measured breakdown Voltage (V)
0.30 – 1.80	3.0	7.0 – 7.2
0.30 – 1.80	30	6.7 – 7.0
0.30 – 1.80	750	6.0

Again, the lengths of the transistors is several times the minimum feature size, which makes punch-through happen at high voltages, greater than junction reverse breakdown and oxide breakdown.

b) Vertical (drain/source to substrate) punch-through

The PMOS transistors are subject to vertical punch-through phenomenon between drain/source and global substrate. Figure 5.16 shows the setup to measure such voltage.

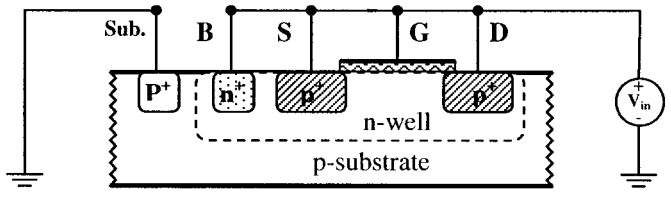


Figure 5.16: Test setup for vertical punch-through voltage in PMOS

Using this structure, drain, source, gate and bulk are at the same potential and therefore, the transistor is off and the channel is not formed yet. Furthermore, the lateral punch-through and drain/source to bulk junction reverse breakdowns do not occur. Gate oxide layer is also not subject to either edge or surface breakdown. However, the bulk-substrate junction reverse breakdown may occur if the vertical punch-through voltage exceeds the said limit. The measured breakdown voltage was found to be similar to the reverse breakdown voltage of the ESDR protective diode to V_{SS} (> 8 V). This implies that the said breakdown occurs earlier or at the same time as the vertical punch-through.

5.3.2.3 Gate oxide breakdown voltage

The gate oxide breakdown phenomena occurs in NMOS and PMOS devices by the mechanism explained in section 6 of the previous chapter. This is a destructive mechanism, and the device characteristics will be degraded significantly after stress. The gate oxide breakdown could occur between gate and drain/source edges or, between gate and channel. The former is due to significantly higher electric fields existing at the edges of the oxide layer and then, is expected to occur at voltages lower than the latter one.

a) Edge gate oxide breakdown voltage

The gate oxide breakdown at drain and source edges could be triggered using different potentials at gate with respect to either drain or source or even both of them simultaneously.

a.1) NMOS transistor

Figure 5.17 illustrates the test structure used to measure the oxide breakdown voltage for a NMOS transistor.

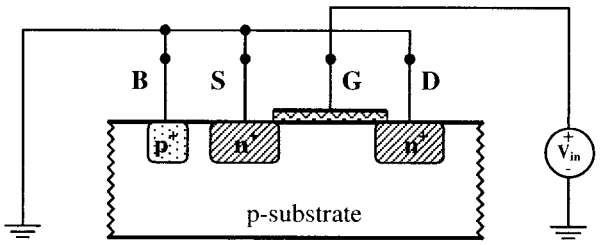


Figure 5.17: Test setup for gate oxide breakdown (edge) in NMOS

Using this setup, having drain, source and bulk with the same voltage forces the transistor deep into its cut-off region and prevents the diffusion-bulk junctions to be in reverse biasing. Furthermore, the condition for drain to source punch-through phenomena is not prepared. However, different voltages at gate and bulk terminals causes the channel to be formed and therefore, the carrier distribution in the channel is changed. Here, having different voltages at gate with respect to the drain, source and bulk may cause gate oxide breakdown. Therefore, extra multimeters were installed on bulk and drain/source to investigate edge and surface oxide breakdowns. Table 5.10 shows measurement results.

Table 5.10: Oxide breakdown voltage for NMOS vs channel length (1.8 V)

Transistor Length (μm)	Gate-Oxide Breakdown voltage (V)
0.45	4.8
0.90	4.8
1.80	4.7

The measured current at device terminals proves that gate oxide breakdown occurs at the drain/source edges earlier that in the channel. This is due to higher electric field at the edges of gate oxide layer. The results also prove that the gate oxide (edge) is independent on the transistor length. Moreover, we examined the device after breakdown and found out that its I-V characteristics were significantly changed. This confirms that the oxide breakdown is destructive.

a.2) PMOS transistor

Different test structures were examined to force the edge oxide breakdown to happen in a PMOS transistor. Table 5.11 summarizes the test setups.

Table 5.11: The test structures of oxide breakdown for PMOS

No.	Device Terminal Connections				
	D	**S**	**G**	**Bulk**	**Sub.**
1	V_{in}^-	V_{in}^-	V_{in}^+	V_{in}^-	V_{in}^-
2	V_{in}^-	V_{in}^-	V_{in}^+	V_{in}^+	V_{in}^-
3	V_{in}^+	V_{in}^+	V_{in}^-	V_{in}^+	V_{in}^+

Although, all of these structures prepare the condition for gate oxide breakdown at drain and source edges, none of them leaded to the said phenomena. The first setup resulted in oxide breakdown between gate and channel (surface), the second initialized the N_{well}-P_{diff} junction reverse breakdown and the last one launched the P_{sub}-N_{diff} junction reverse breakdown. These results came from analysis of the current passing through drain, source and bulk terminals which were measured using additional multimeters.

b) Surface breakdown voltage

The gate oxide breakdown to the channel could be obtained using different potentials at gate with respect to the channel.

b.1) NMOS transistor

Figure 5.18 illustrates the test structure used to measure the oxide breakdown voltage for a NMOS transistor at its channel surface.

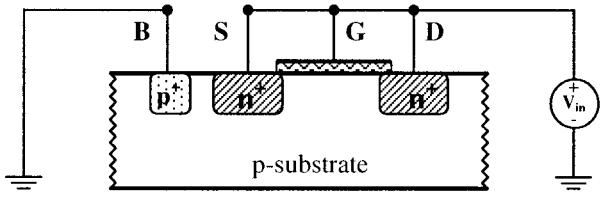


Figure 5.18: Test setup for gate oxide breakdown (surface) in NMOS

Using the above setting, the symmetric drain-substrate and source-substrate junctions are in reverse bias, while the gate is fixed to the same voltage as the drain/source, and then the device is in the cut-off region. Furthermore, with drain and source at the same potential, punch-through does not occur. Since the device is subject to probable diffusion-bulk junctions reverse breakdown, extra multimeters were used on drain and source to monitor the currents flowing through them. Although the condition of V_{GS}=0 maintains the device in deep cut-off region, different potential at gate and bulk causes a channel to be formed. For this experiment, we found that the diffusion-bulk junctions break earlier than the gate oxide layer. This shows that the oxide breakdown at the channel surface occurs at higher voltages than those of said junctions. We have also used the setup

illustrated in Figure 5.11a and continued monitoring gate current after substrate-diffusion junction reverse breakdown occurred. The results of gate oxide breakdown voltage at channel surface is shown in Table 5.12.

Table 5.12: The gate oxide breakdown (surface) vs channel length for NMOS (1.8 V)

Transistor Length (μm)	Gate Oxide (Surface) Breakdown Voltage (V)
0.45	9.0
0.90	8.8
1.80	8.6

The results prove that the said breakdown is inversely proportional to the channel area. One can justify this result with the statistical nature of gate oxide breakdown. Therefore, as gate area is increased, the probability of occurrence of such breakdown is also increased and the breakdown happens at lower voltage.

b.2) PMOS transistor

In order to force the oxide breakdown to occur between the gate and the channel of a PMOS transistor, different test structures were used which are shown in Figure 5.19. The main difference between these setups is the polarity of the gate biasing. Using these test structures, the transistor is forced to remain in cut-off region, which prevents vertical and lateral punch-through as well. Both setups provide conditions for channel to be formed, which leads to new carrier distribution in the channel beneath the gate oxide. Furthermore, the first setup is constrained to diffusion-bulk junctions and bulk-substrate

junctions reverse breakdowns, while the second structure could lead to oxide breakdown at drain/source edges. So, additional multimeters were installed on the drain, source and bulk terminals to monitor the relative currents.

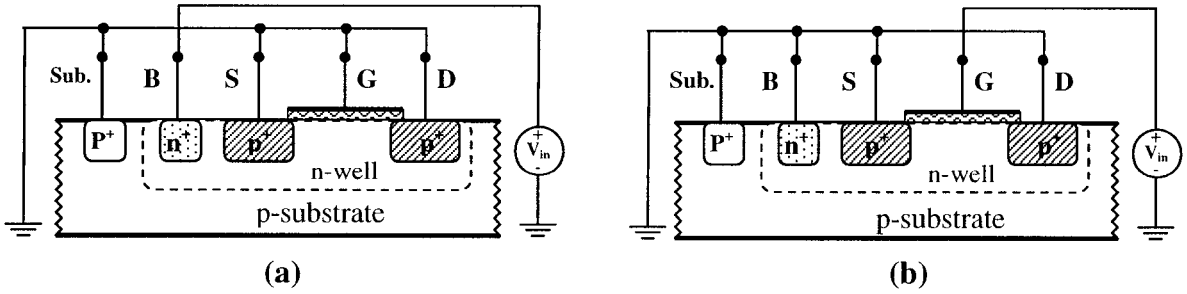


Figure 5.19: Test setup for gate oxide breakdown (surface) in PMOS:
a) with direct biasing, b) with indirect biasing

Based on the measured currents at the said terminals, we found that for the first setup, the diffusion-bulk junctions reverse breakdown begins earlier than the oxide breakdown and oxide breakdown between gate and bulk (channel surface) occurs for the second structure. Table 5.13 shows the measured oxide breakdown voltages for different lengths and widths of transistors.

As a summary, the carrier distribution in channel, which depends on the process parameters and gate to bulk potential difference, was proved to have a significant impact on device characteristics. Furthermore, downscaling MOS devices degrades reliability through issues such as hot carrier injection, gate oxide and junction reverse breakdowns, lateral and vertical punch-through phenomenon, and other parasitic effects. This brings some second and higher order effects in the foreground from circuit design standpoint.

Table 5.13: Oxide breakdown voltage (surface) for PMOSs (setup b, 3.3 V)

Transistor Length (μm)	Transistor Width (μm)	Measured Breakdown Voltage (V)
0.30	3.0	9.0 – 9.2
0.45	3.0	9.2
0.90	3.0	9.2
1.35	3.0	9.2
1.80	3.0	9.2 – 9.3
0.30	30	8.2 – 8.3
0.45	30	8.1 – 8.2
0.90	30	7.8 – 8.0
1.35	30	7.7
1.80	30	7.4
0.30	750	7.8 – 7.9
0.45	750	7.8
0.90	750	7.6
1.35	750	7.4
1.80	750	7.4

We also found out that the test structure has a remarkable impact on the accuracy and validity of the measurement results. For some measurements, we have examined few possible setups. It was found that gate oxide breakdown is independent on device geometry, while breakdown between gate and channel is strongly dependent on the channel area.

It was also found that oxide breakdown at drain and source edges occur at lower voltages, and therefore are of greater concern from a device reliability point of view. Due to constraints of multi-project shuttle manufacturing, the number of devices was not

sufficient to conduct reliability tests. The impact of factors such as time and temperature on device lifetime and wear-out were not examined. Finally, our results show that, through suitable circuit design techniques, MOS devices could operate at voltage levels up to twice the nominal process power supply.

5.3.3 Prototype chip

The respective results were measured on a prototype chip fabricated using the TSMC 0.18 μm n-well CMOS technology. The layout was done manually under Cadence Virtuoso. To reduce unexpected effects caused by the circuit layout, a systematic protocol was used for the experimental prototype chip. In order to measure the real physical values of the currents and voltages, All the transistors, even those of very large sizes, were made as monolithic devices and were not fingered.

A surrounding n-well was used around all transistors, which serves as guard ring. This helps for isolation of each transistor from deep substrate currents, which may disturb the performance and characteristics of adjacent transistors. In order to reduce the number of required pads, three different techniques were applied. First, the layout of few transistors were drawn by having shared Source, Bulk and Gate terminals, while still a few were left completely separated. Secondly, as a new method, a single die capable of dual packaging possibility was made. Using this method, dual layouts were fabricated at the same time on a single die. They were then packaged using two different pin-outs.

The pads were organized in two different rings, the inner and outer rings. This makes it possible to have dual layouts sharing the same die area. Figure 5.20 illustrates the view of the prototype chip.

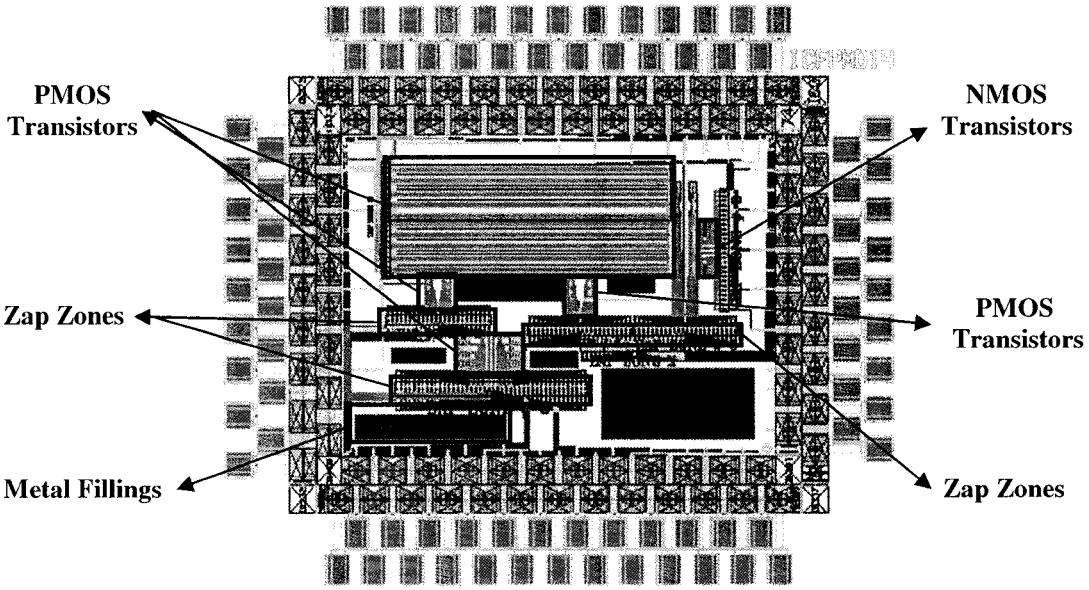


Figure 5.20: The view of the prototype chip

Layout placement was accomplished using different devices sharing the same path to access given pads. The individual paths were zapped by Nd-Yag laser surgery in zap zones, which are located right before the joint nodes. Figure 5.21 shows the specimen schematic of these zap zones. The paths must be available at metal 6 layer, where there is no further oxide layer coverage. The zap zones are arranged such that the signal path holds straight direction for at least 10 μm length and were located at a distance of 10 μm from the adjacent paths. These values are very dependent on the laser beam characteristics. Using this method, which could be managed hierarchically, it is possible to save on the number of required pads.

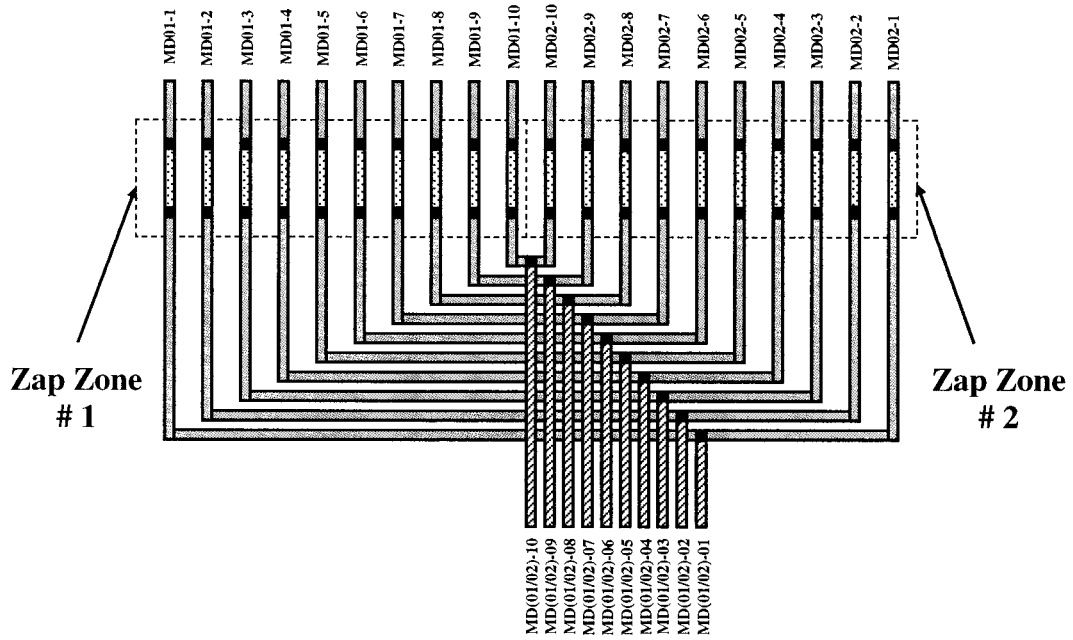


Figure 5.21: The specimen schematic of the zap zones

In order to prevent the impact of process tolerances on the measurements, the same transistors were implemented in different locations of the chip. They were also fabricated in different lengths and widths with the objective of testing many different dimensions for the PMOS transistors. This is due to our prior intention of using such devices as main switch of SSR in a high efficiency fully-integrated PCC architecture.

The ESDR protective rings were connected to four individual pads (two pads for each inner and outer rings) in order to let optional stress voltages be applied at the device terminals before being clamped by either nominal process-assigned V_{DD} or V_{SS}. This makes it possible to apply adequate voltages at the said pads by selection. Large signal paths were also employed on metal layers to reduce parasitic series resistance. The die area is 1855×1425 μm^2.

5.4 Summary

The architecture of a power conversion chain heavily impacts its overall efficiency. This chapter presents quantitative results on the study of different PCC architectures for an electronic implant in terms of power efficiency and integration. First, a conventional architecture was modeled by mathematical equations to provide ground for further comparisons. Later, two new architectures based on synchronous rectifiers were proposed. They double the relative overall power efficiency. The second approach also removes the need for diodes that are generally implemented as off-chip components. Moreover, the proposed architectures benefit from gate-controlled switches which can also be used to stabilize the chain power efficiency while input voltage varies.

Furthermore, a multi-stage high-efficiency voltage multiplier feasible for CMOS integrated circuit was examined. This module uses non-overlapping clocks. Moreover, applying bulk switching and level shifting techniques reduce the dynamic losses in serial switches. Simulation results confirm the predicted theoretical characteristics of the circuit. This could be used for boosting input voltages as low as 1.5 V. The number of stages was limited to gate oxide and junction breakdown voltages of CMOS processes.

Finally, a prototype chip was fabricated using TSMC 0.18 μm process and the relative oxide and junction breakdown and punch-through voltages were measured. As a result of the measurements, it was found that the MOS device under stress condition are subject to several breakdown mechanisms. The carrier distribution in channel, which depends on

process parameters and gate to bulk potential difference, was proved to have a significant impact on these devices characteristics.

Furthermore, the outcome leads to the conclusion that downscaling MOS devices causes reliability issues such as hot carrier injection, gate oxide and junction reverse breakdown, lateral and vertical punch-through phenomenon and parasitic effects. These phenomena have significant impacts on the performance and characteristics of devices and circuits. This brings some second and higher order issues to the forefront from circuit design point of view. We also found out that the test structure has a remarkable impact on the measurements accuracy.

Chapter 6

Conclusions

6.1 Summary and discussion

New sub-micron technologies improve the performance and efficiency of integrated circuits. Taking advantage of these technologies may bring some limitations in certain applications. For instance, these technologies have lower nominal power supply voltage. On the other hand, biomedical applications such as cortical stimulations, for example, require voltages higher than the nominal power supply voltage of new sub-micron technologies. Using either pure CMOS technologies that support high voltages or using hybrid approaches, where low and high voltage technologies are combined are possible solutions. The development of power conversion chains and voltage boosting circuits were studied in this thesis. The device reliability under stress condition was also studied as a major concern.

In Chapter 2, after an introductory discussion on techniques to feed power to electronic implant, major limitations and constraints on design of a multi-channel FES system were addressed. Among them, variations in load current and voltage as well as variations of input voltage are of greater importance. Some circuit design concerns that affect the design of such circuits were also outlined. It was clarified that integrating the whole implant could improve its performance significantly, but it also imposes reliability issues.

Furthermore, a conventional architecture for the power conversion chain of an electronic biomedical implant was presented, and the basic building blocks of such structure were introduced. It was noticed that they suffer from low overall power efficiency due to diode inherent voltage drop. Later, the concept of Smart Synchronous Rectifier was introduced and different categories of such rectifier, so called self-driven, externally-driven and smart SRs were described briefly. A possible CMOS implementation for SSR, along with a detailed description on its operation modes, was also presented. Then, a study on the features of SSR versus classical diode rectifiers from power efficiency point of view was formulated. It was shown that using SSR in place of DR could replace diode constant voltage drop with a relatively low drop depending on the load current.

Then, a distributed structure and a monolithic structure were presented. Their respective power efficiency were modeled. It was shown that the architecture of a power conversion chain heavily impacts its overall efficiency. The new proposed structures almost double the overall power efficiency. The second approach also removes the need for diodes that are generally implemented off-chip. Moreover, it was stated that structures that benefit gate-controlled CMOS switches can also be used to stabilize the chain power efficiency when the input voltage varies.

In Chapter 3, the basic building blocks of a voltage doubler stage were introduced. The concept and characteristics of various charge pumps as well as their operation were described. It was observed that they suffer from the forward voltage drop of a diode or

threshold voltage of a MOS switch. Using new circuit techniques such as static and dynamic charge transfer switches was covered as possible solutions.

Then, the characteristics of a single stage voltage multiplier such as power efficiency, output ripples and voltage gain were discussed and models were formulated. It was shown that the switch-capacitor-based structures are suffering from poor power efficiency and are subject to remarkable output ripples. The impact of changes in circuit parameters such as switching frequency, integrator capacitor, non-overlapping clocks and switch conductance were discussed. The structure of a high efficiency voltage multiplier stage was introduced. The classical structure of a multi-stage voltage multiplier using simply cascaded stages was presented. It provides a linear multiplication factor with the number of stages. Finally, a new structure that improves the multiplication factor exponentially was introduced.

In chapter 4 and related appendixes (A, B and C), the semiconductor reliability issues were addressed. The concept and impact of punch-through was reviewed. Punch-through models were presented. Breakdown voltages for channel, junctions and gate oxide were also reviewed. Popular accelerated test structures for reliability purposes of MOS devices were presented. Throughout this chapter, it was clarified that the down scaling of the MOS device has a significant impact on device and circuit characteristics and the performance of the semiconductor can be remarkably degraded by these issues.

Chapter 5 summarizes the theoretical, simulation and experimental results of this work. Measurement of parameters such as oxide and junction breakdown and punch-through voltages could help to characterize the new sub-micron MOS technologies and take advantage of the outcomes to design reliable device and circuits. First, several electronic implant power conversion chain architectures were characterized in terms of power efficiency. An architecture for a SSR was also proposed. Then, the result of simulations for single and multiple stage high efficiency voltage multiplier were presented, and the result of design parameter such as charge pump capacitors, clock frequency, transistor dimensions, and clock overlapping were characterized.

Finally, chapter 5 presented experimental results measured on fabricated chips developed to characterize CMOS breakdown mechanisms. The results prove that the MOS transistor will be subject to reliability problems when voltage stress conditions are applied to their terminals. MOS processes may not be able to support voltages much higher than the nominal supply voltage. When such voltages are needed, processes developed to support them should be used.

6.2 Directions for future work

In the framework of new sub-micron CMOS processes, the technology trend is to lower the nominal power supply voltages. The results reported in this work may not represent the limit of device parameters which can be achieved with this technology, and further

investigations of these limits would be of great interest. More detailed work covering larger number of samples with a wider range of types and dimensions under reliability test is necessary to evaluate the robustness of the results and the attached hypothesis. In general terms, several potential directions of future research can be considered:

1) Within the framework of standard processes, there are limits to the extent to which we can boost the voltage higher than the nominal power supply voltage. They imply paying so much care to ensure the reliability of MOS devices. Such concerns could also result in using the voltage multiplication techniques of lower efficiency [80]. The use of hybrid or high voltage process for higher voltage and higher efficiency applications is recommended.

2) Due to process limitations in supporting high voltage applications, it seems quite essential to dedicate more efforts to investigate power efficiency of the power conversion chain architecture in order to design more efficient structures. A close look at the power chain topology and its components from power efficiency point of view could be a proper point to start from. As a straightforward extension, the proposed circuit for Smart Synchronous Rectifiers in CMOS technology could be implemented.

3) Normal operation of a SSR takes place in two different phases, the so called

sampling and controlling phases. There is a gap between two phases needed to make proper decision out of samples data. The duration of this gap is affected by the speed of circuit elements which impose complicated and high speed components. In order to simplify the control circuitries, one can accomplish these two phases in two consequent signal periods, that is using the first period for sampling and making decision and applying such decision in second period to adjust the conduction angle of the main switch. This would be effective if and only if the input signal has a constant frequency and magnitude. The first is an inherent part of RF inductive link transmission property, and the second could be obtained by using proper modulation techniques. For instance, ASK modulation methods appear incompatible with such objectives.

4) Device testing under accelerated conditions is strongly recommended in order to confirm the device long term reliability and longevity under stress conditions. This could be done based on Arrhenius equation by applying temperatures higher than ambient values.

In conclusion, this thesis has established that new power conversion chain architectures using Smart Synchronous Rectifiers can replace conventional structures successfully. It also presented a high efficiency CMOS voltage multiplier circuit capable of boosting input voltage to higher values subject to process limits and device reliability issues.

References

[1] --- , "*Performance trends in high-end processors*," Proc. IEEE, vol. 83, pp. 20–36, 1995.

[2] ---, "*Hot-electron emission from silicon into silicon dioxide*," Solid State Electron., vol. 21, pp. 273–282, 1978.

[3] ---, "TSMC 0.18 μm Technology," www.tsmc.com.

[4] ABADEER, W.W., BAGRAMIAN, A., CONKLE, D.W., GRIFFIN, C.W., LANGLOIS, E., LLOYD, B.F., MALLETTE, R.P., MASSUCCO, J.E., MCKENNA, J.M., MITTL, S.W., NOEL, P.H., "*Key measurements of ultrathin gate dielectric reliability and in-line monitoring*," IBM J. Res. Develop., vol. 43, no.3, pp. 407-416, May 1999.

[5] AKIN, T., NAJAFI, KH., BRADLEY, R.M., "*A Wireless Implantable Multichannel Digital Neural Recording System for a Micromachined Sieve Electrode*," IEEE J. Solid-State Circuits, vol. 33, no. 1, pp. 109-118, Jan. 1998.

[6] ALAM, M.A. ET AL., "*Field acceleration for oxide - Can an accurate anodehole injection model resolve the E vs. 1/E controversy?*," Proc. IEEE IRPS, pp. 21, 2000.

[7] ALAM, M.A. ET AL., "*Physics and prospects of sub-2-nm oxides*," Proc. 4th Int. Symp. Physics and Chemistry of SiO_2 and the Si–SiO_2 Interface, pp. 365, 2000.

[8] ALAM, M.A., WEIR, B., BUDE, J., SILVERMAN, P., MONROE, D., "*Explanation of soft and hard breakdown and its consequences for area scaling*," IEEE IEDM Tech. Dig., pp. 449–452, 1999.

[9] ALAM, M.A., WEIR, B.E., SIVERMAN, P.J., MA, Y., HWANG, D., "*The statistical distribution of percolation resistance as a probe into the mechanics of ultra-thin oxide breakdown*", IEEE IEDM Tech. Dig., pp. 529–533, 2000.

[10] ALLEN, H.V., KNUTTI, J.W., MEINDL, J.D., "*Integrated power Controllers and RF Data Transmitters for Totally Implantable Telemetry*," Biotelemetry Patient Monit., vol. 6, pp. 147-159, 1979.

[11] AMERICAN NATIONAL STANDARDS INSTITUTE, "*Safety level of Electromagnetic Radiation with Respect to Personnel*," ANSI C95.1-1974, IEEE, New York, NY, 1974.

[12] ANDERS, M. TSCHANZ, J., "*Digital Design 1 – ECE574*,", OGI School of Science and Engineering, Oregon, USA, Winter 2003.

[13] ARNOLD, D., CARTIER, E., DIMARIA, D.J., "*Theory of high-field transport and impact ionization in silicon dioxide*," Phys. Rev. B, vol. 49, pp. 10278, 1994.

[14] BAKOGLU, H.B., "*Circuits, Interconnections, and Packaging for VLSI*," Addison-Wesley, 1990.

[15] BARNES, J.J., SHIMOHIGASHI, K., DUTTON, R.W., "*Short-Channel MOSFET's in the Punchthrough Current Mode*," IEEE J. Solid-State Circuits, vol. SC-14, no.2, pp. 368-375, Apr. 1979.

[16] BELLENS, R., VAN DEN BOSCH, G., HABAS, P., MIEVILLE, J.P., BADENES, G., CLERIX, A., GROESENEKEN, G., DEFERM, L., MAES, H., "*Performance and reliability aspects of FOND: A new deep submicron CMOS device concept*", IEEE Trans. Electron Devices, vol. 43, pp. 1407, 1996.

[17] BIN, L., YIN, G., LIJIU, J., "*A New Cascading CMOS Voltage-Doubler Charge Pump*," Inst. Microelectronic, Peking Univ., Beijing, P. R. China, 100871.

[18] BLAKE, C., GUERRA, A., "*Schottky diodes vs. FET synchronous rectifiers*," Electronic Engineer, May 2000.

[19] BLAKE, C., KINZER, D., WOOD, P., "*Synchronous Rectifiers versus Schottky diodes: A comparison of the losses of a synchronous rectifier versus the losses of a Schottky diode rectifier*," Proc. 9th Applied Power Electronics Conference and Exposition, vol. 1, pp. 17-23, Feb. 1994.

[20] BOHR, M., AHMED, S.S., AHMED, S.U., BOST, M., GHANI, T., GREASON, J., HAINSEY, R., JAN, C., PACKAN, P., SIVAKUMAR, S., THOMPSON, S., TSAI, J., YANG, S., "*A high performance 0.25 μm logic technology optimized for 1.8 V operation*," International Electron Devices Meeting (IEDM), pp. 847-850, Dec. 1996.

[21] BOHR, M., AHMED, S.U., BRIGHAM, L., CHAU, R., GASSER, R., GREEN, R., HARGROVE, W., LEE, E., NATTER, R., THOMPSON, S., WELDON, K., YANG, S., "*A high performance 0.35 μm logic technology for 3.3 V and 2.5 V operation*," International Electron Devices Meeting (IEDM), Technical Digest.,

pp. 273-276, Dec. 1994.

[22] BRUYERE, S., VINCENT, E., GHIBAUDO, G., "*Quasi-breakdown in ultra-thin SiO_2 films: Occurance characterization and reliability assessment methodology*," IEEE IRPS, pp. 48, 2000.

[23] BUCHANAN, J., "*MOS DC voltage booster circuit*," US Patent 3,942,047, 1976.

[24] CAO, M., GRIFFIN, P., VANDE VOORDE, P., DIAZ, C., GREENE, W., "*Transient-enhanced Diffusion Of Iridium And Its Effects On Electrical Characteristics Of Deep Sub-micron nMOSFETs*," Symp. VLSI Technology, Dig. Tech. Papers, pp. 85-86, Jun. 1997.

[25] CARTIER, E., BUCHANAN, D.A., DUNN, G.J., "*Atomic hydrogen-induced interface degradation of reoxidized-nitrided silicon dioxide on silicon*", Appl. Phys. Lett., vol. 64, pp. 901, 1994.

[26] CARTIER, E., STATHIS, J.H., BUCHANAN, D.A., "*Passivation and depassivation of silicon dangling bonds at the Si/SiO_2 interface by atomic hydrogen*", Appl. Phys. Lett., vol. 63, pp. 1510, 1993.

[27] CHADRACK, W., GAGE, A., GREATBATCH, W., "*A transistorized, self-contained, implantable pacemaker for the long-term correction of complete heart block*," Surgery, vol. 48, pp. 543, 1964.

[28] CHAN, V., KIM, J.S., CHUNG, J.E., "*Parameter extraction guidelines for hot-electron reliability simulation*", Proc. International Reliability Physics Symposium, pp. 32-37, 1993.

[29] CHEN, I.C., HOLLAND, S., YOUNG, K.K., CHANG, C., HU, C., "*Substrate hole current and oxide breakdown*", Appl. Phys. Lett., vol. 49, pp. 669, 1986.

[30] CHEN, I.C., HOLLAND, S.E., HU, C., "*Electrical breakdown in thin gate and tunneling oxides*," IEEE Trans. Electron Devices, vol. ED-32, pp. 413, Feb. 1985.

[31] CHEN, K.L., "*The effects of interconnect process and snapback voltage on the ESD failure threshold of nMOS transistors,*" Trans. Electron Devices, vol. 35, pp. 2140, 1988.

[32] CHENG, Y.C., SULLIVAN, E.A., "*On the role of scattering by surface roughness in silicon inversion layers*," *Surface Sci.*, vol. 34, pp. 717, 1973.

[33] CHEUNG, K.P., "*Thin gate-oxide reliability-the current status*," Keynote paper, Symp. Nano Device Technology 2001, Taiwan, Apr. 2001.

[34] CHO, T.B., GRAY, P.R., "*A 10-bit, 20 MS/s, 35 mW pipeline A/D converter*," IEEE Custom Integrated Circuits Conf., pp. 499-502, 1994.

[35] CHOI, C.C., YU, Z., DUTTON, R.W., "*Impact of Gate Tunneling Current in Scaled MOS on Circuit Performance: A Simulation Study*," IEEE Trans. Electron Devices, vol. 48, no.12, pp. 2823-2829, Dec. 2001.

[36] CHOI, K.H., PARK, J.M., JUNG, T.S., SUH, K.D., "*Floating well charge pump circuits for sub-2.0 V single power supply Flash memories*," Symp. VLSI Circuits Dig. Tech. Papers, pp.61-62, Jun. 1997.

[37] CHOU, A.I., LIN, C., KUMAR, K., CHOWDHURY, P., GARDNE, M., GILMER, M., FULFORD, J., LEE, J.C., "*The Effects of Nitrogen Implant into Gate Electrode on the Characterization of Dual-gate MOSFETs with Ultrathin Oxide and Oxynitrides*," Proc. International Reliability Physics Symposium, pp.174, 1997.

[38] CHRZANOWSKA-JESKE, M., "*Device Reliability: Reliability Enhancement through Layout changes*," Handout, Portland State Univ., USA, Spring 2003.

[39] CHUNG, J.E., "*Key issues in evaluating hot-carrier reliability*," Proc. SPIE International Society for Optical Engineering, vol. 2875, pp. 64-74, 1996.

[40] CHUNG, J.E., QUADER, KH.N., SODINI, C.G., KO, P. HU, C., "*The Effects of Hot-Electron Degradation on Analog MOSFET Performance*," IEEE IEDM, PP.553-556, 1990.

[41] COCKCROFT, J.D., WALTON, E.T., "*Production of high velocity positive ions*," Proc. Roy. Soc., A, vol. 136, pp.619-630, 1932.

[42] CROWELL C., SZE S.M., "*Temperature dependence of avalanche multiplication in semiconductors*," Applied Physics Lett., vol. 9, pp. 242, 1966.

[43] D'ARRIGO, S., IMONDI, G., SANTIN, G., "*A 5V-Only 256 Kbit CMOS Flash EPROM*," ISSCC Dig. Tech. papers, pp. 132-133, Feb. 1989.

[44] DEGRAEVE, R., et al., "*A consistent model for the thickness dependence of intrinsic breakdwon in ultra-thin oxides*,"IEDM, pp. 863, 1995.

[45] DEGRAEVE, R., KACZER, B., KEERSGIETER, A.D., GROESENEKEN, G., "*Relation Between Breakdown Mode and Location in Short-Channel nMOSFETs and Its Impact on Reliability Specifications*," IEEE Trans Device and Materials Reliability, vol. 1, no. 3, pp. 163-169, Sep. 2001.

[46] DEGRAEVE, R., OGIER, J.L., BELLENS, R., ROUSSEL, PH., GROESENEKEN, G., MAES, H.E., "*On the Field Dependence of Intrinsic and Extrinsic Time-Dependent Dielectric Breakdown*," Proc. International Reliability Physics Symposium, pp. 44, 1994.

[47] DENNARD, R.H., GAENSSLEN, F.H., YU, H.N., RIDEOUT, V.L., BASSOUS, E., LEBLANC, A.R., "*Design of ion-implanted MOSFET's with very small physical dimensions*," IEEE J. Solid-State Circuits, vol. SC-9, pp. 256, 1974.

[48] DICKSON, J.F., "*On-Chip High-Voltage Generation in MNOS Integrated Circuits Using an Improved Voltage Multiplier Technique*," IEEE J. Solid-State Circuits, pp. 374-378, Jun. 1976.

[49] DIJKMANS, E.C., SLUIJS, F.J., "*DC/DC Conversion, the key to low power consumption*," Philips Research Labs, Eindhoven, The Netherlands.

[50] DIMARIA, D.J., "*Hole trapping, Substrate Currents, and Breakdown in Thin Silicon Dioxide Films*," IEEE Electron Devices, vol. 16, no. 5, pp. 184, May 1995.

[51] DIMARIA, D.J., "*The Physics of SiO2 and Its Interfaces*," New York: Pergamon, vol. 160, 1978.

[52] DIMARIA, D.J., ARNOLD, D., CARTIER, E., "*Degradation and breakdown of silicon dioxide films on silicon*," Applied Physics Letters, vol. 61, pp. 2329-2331, 1992.

[53] DIMARIA, D.J., CARTIER, E., ARNOLD, D., "*Impact ionization, trap creation, and breakdown in silicon dioxide films on silicon*," J. Appl. Phys., vol. 73, pp. 3367, 1993.

[54] DIMARIA, D.J., STASIAK, J.W., "*Trap creation in silicon dioxide produced by hot electrons*," *J. Appl. Phys.*, vol. 65, pp. 2342, 1989.

[55] DIMARIA, D.J., STATHIS, J.H., "*Non-Arrhenius temperature dependence of reliability in ultrathin silicon dioxide*," Appl. Phys. Lett., vol. 74, pp. 1752, 1999.

[56] DIMITRIJEV, S., "*Understanding Semiconductor Devices*," Oxford University Press, Inc., TK7871.85 .D547 1999, USA, 2000.

[57] DJEMOUAI, A., SAWAN, M., "*Prosthetic Power Supplies*," Wiley Encyclopedia of Electrical and Electronics Engineering, John Wiley & Sons, Inc., 1999.

[58] DORMAN, M.G., PRISHE, M.A., MEINDL, J.D., "*A monolithic signal processor for a neurophysiological telemetry system,*" IEEE J. Solid-State Circuits, vol. 20, pp. 1185-1193, Dec. 1985.

[59] DUVVURY, C., ROUNTREE, R., STIEGLER, H.J., POLGREEN, T., CORUM, D., "*ESD phenomena in graded junction devices*," Proc. IRPS, pp. 71, 1989.

[60] FAVRAT, P., DEVAL, PH., DECLERCQ, M.J., "*An Improved Voltage Doubler in a Standard CMOS Technology*," IEEE Int. Symp. Circuits and Systems, pp. 249-252, Hong Kong, 1997.

[61] FAVRAT, P., DEVAL, PH., DECLERQ, M. J., "*A High-Efficiency CMOS Voltage Doubler*," IEEE J. Solid-State Circuits, vol. 33, no. 3, pp. 410-416, Mar. 1998.

[62] FISCHELL, R.E., SCHULMAN, J.H., "*A rechargeable power system for cardiac pacemakers*," Proc. 11th Intersoc. Energy Conv. Eng. Conf., vol. 1, pp. 163, 1976.

[63] FRANK, D.J., DENNARD, R.H., NOWAK, E., SOLOMOM, P.M., TAUR, Y., WONG, H.P., "*Device Scaling Limits of Si MOSFETs and Their Application Dependencies*," Proc. IEEE, Vol 89, no. 3, pp. 259-288, Mar. 2001.

[64] GALBRAITH, D.C., "*An Implantable Multi-channel Neural Stimulator*," Ph.D. dissertation, Stanford Univ., Stanford, CA, Dec. 1984.

[65] GERBER, B., MARTIN, J., FELLRATH, J., "*A 1.5V Single-Supply One-Transistor CMOS EEPROM*," IEEE J. Solid-State Circuits, vol. 23, SC-16, no. 3, pp. 195- 199, Jun. 1981.

[66] GHIBAUDO, G., PANANAKAKIS, G., KIES, R., VINCENT, E., PAPADAS, C., "*Accelerated dielectric breakdown and wear out standard testing methods and structures for reliability evaluation of thin oxides*," Microelectronics Reliability, vol. 39, pp. 597-613, 1999

[67] GIEBEL, B., "*An 8K EEPROM using the SIMOS Storage Cell*," IEEE J. Solid-State Circuits, vol. SC-15, pp. 311-317, Jun. 1980.

[68] GREATBATCH, W., CHARDACK, W., "*A transistorized implantable pacemaker for the long-term correction of complete atrioventricular block*," Proc. New Eng. Research and Engineering Meeting (NEREM), vol. 1, pp. 8, 1959.

[69] GREATBATCH, W., HOLMES, C.F., "*History of implantable devices*," IEEE Eng. Med. Biol. Mag., vol. 10, no. 3, pp. 38-41, 1991.

[70] GROESENEKEN, G., BELLENS, R., VAN DEN BOSCH, G., MAES, H.E., "*Hot carrier degradation in submicrometre MOSFET's: From uniform injection towards the real operating conditions*," Semicond. Sci. Technol., vol. 10, pp. 1208-1220, 1995.

[71] GROESENEKEN, G.V., "*Hot Carrier Degradation and ESD in Submicrometer CMOS Technologies: How Do They Interact?*," IEEE Trans. Device and Materials Reliability, vol. 1, no. 1, pp. 23-32, Mar. 2001.

[72] GUMBEL, E.J., "*Statistics of extremes*," Columbia University Press, New York, 1958.

[73] GUPTA, A., SUGIHARTO, D.S., YANG, C.Y., MATSUZAKI, N., MINAMI, M., YAMANAKS, T., NAGANO, T., "*Hole trapping as the rate-limiting factor in LDD n-MOSFET degradation*," International Integrated Reliability Workshop, pp. 119-124, 1996.

[74] HADDAD, S., CAGNINA, S., "*Dynamic behavior of negative charge trapping in thin silicon oxide*," Appl. Phys. Lett., vol. 55, pp. 1747, 1989.

[75] HADDAD, S., LIANG, M.S., "*The nature of charge trapping responsible for thin-oxide breakdown under a dynamic field stress*," IEEE Electron Device Lett., vol. EDL-8, pp. 524, 1987.

[76] HARRIS, J.S., "*Principals and Models of Semiconductor Devices*," EE-216, Autumn 2002.

[77] HEREMANS, P., BELLENS, R., GROESENEKEN, G., MAES, H.E., "*Consistent model for the hot carrier degradation in n-channel and p-channel MOSFET's*," IEEE Trans. Electron Devices, vol. 35, pp. 2194, 1988.

[78] HEREMANS, P., BELLENS, R., GROESENEKEN, G., SCHWERIN, A.V., WEBER, W., BROX, M., MAES, H.E., "*The mechanisms of hot carrier degradation*," in Hot Carrier Design Considerations for MOS Devices and Circuits, ch. 1, Wang C.T., Ed. New York: Van Nostrand-Reinhold, 1992.

[79] HOENEISEN, B., MEAD, C.A., "*Fundamental limitations in microelectronics—I. MOS technology*," Solid-State Electron., vol. 15, pp. 819, 1972.

[80] HONG, D.S., EL-GAMAL M.N. "*Low Operating Voltage and Short Settling Time CMOS Charge Pump for MEMS Applications*," Proc. International Symp. Circuits and Systems, ISCAS'03, Vol. 5 , pp. 281-284, May 2003.

[81] HORI, T., "*A 0.1 μm CMOS technology with tilt-implanted punchthrough stopper (TIPS)*," International Electron Devices Meeting (IEDM), Technical Digest., PP. 75-78, Dec. 1994.

[82] HORI, T., HIRASE, J., ODAKE, Y., YASUI, T., "*Deep-submicrometer large-angle-tilt implanted drain (LATID) technology,*" IEEE Trans. Electron Devices, vol. 39, pp. 2312, 1992.

[83] HU, C., TAM, S.C., HSU, F., KO, P.K., CHAN, T., TERRILL, K.W., " *Hot-electron-induced MOSFET degradation-model monitor, and improvement,*" IEEE Trans. Electron Devices, vol. 32, pp. 375-383, 1985.

[84] HUANG, Q., OBERLE, M., "*A 0.5-mW Passive Telemetry IC for Biomedical Applications,*" IEEE J. Solid-State Circuits, vol. 33, no. 7, pp. 937-946, July 1998.

[85] HUANG, T., YAO, W.W., MARTIN, R.A., LEWIS, A.G., KOYANAGI, M., CHEN, J.Y., "*A novel submicron LDD transistor with inverse-T gate structure,*" IEDM Tech. Dig., pp. 742, 1986.

[86] HUMAYUN, M., DE JUAN, JR.E., WEILAND, J., DAGNELIE, G., KATONA, S., GREENBERG, R., SUZUKI S., "*Pattern Electrical Stimulation of the Human Retina,*" Vision Res., vol. 39, pp. 2569-2576, 1999.

[87] HUNTER, W.R., "*A Failure Rate Based Methodology for Determining the Maximum Operating Gate Electric Field, Comprehending Defect Density and Burn-In,*" Proc. International Reliability Physics Symposium, pp. 37, 1996.

[88] INDUSTRY CANADA, "*Canadian Table of frequency Allocations, 9 KHz to 275 GHz,*" Telecommunication policy branch, Ottawa, Dec. 2000.

[89] IZAWA, R., KURE, T., TAKEDA, E., "*Impact of the gate–drain overlapped device (GOLD) for deep submicrometer VLSI*," IEEE Trans. Electron Devices, vol. 35, PP. 2088, 1988.

[90] JACOBS, J.B., ANTONIADIS, D., "*Channel profile engineering for MOSFET's with 100 nm channel lengths*," IEEE Trans. Electron Devices, vol. 42, no. 5, pp. 870-875, May 1995.

[91] JEUTTER D.C., "*A transcutaneous implanted battery recharging and biotelemeter power switching system*," IEEE Trans. Biomed. Eng., vol. 29, pp. 314-321, 1982.

[92] JOHNS, D.A, MRTIN, K., "*Analog Integrated Circuit Design*," John Willey & Sons, Inc., TK7874.J65 1996, ISBN 0-471-14448-7, USA, 1997.

[93] KACZER, B., DEGRAEVE, R., GROESENEKEN, G., RASRAS, M., KUBICEK, S., VANDAMME, E., BADENES, G., "*Impact of MOSFET oxide breakdown on digital circuit operation and reliability*," IEEE IEDM Tech. Dig., pp. 553–556, 2000.

[94] KEYES, R.W., "*Fundamental Limits of Silicon Technology*," Proc. IEEE, vol. 89, no. 3, pp. 227-239, Mar. 2001.

[95] KIM, S.H., TSOUHLARAKIS, J., HOUDT, J.V., "*A CMOS DC Voltage Doubler with Non-overlapping Switching Control*," IEICE Trans. Electron., vol. E84-C, no. 2, pp. 274-277, Feb. 2001.

[96] KUO, M.M., SEKI, K., LEE, P.M., CHOI, J.Y., KO, P.K., HU, C., "*Simulation of MOSFET Lifetime under AC Hot-Electron Stress*", IEEE Trans. Electron Devices, vol. 35, no. 7, pp. 1004-1011, Jul. 1988.

[97] KUROI, T., SHIMIZU, S., OGINO, S., TERAMOTO, A., SHIRAHATA, M., OKUMURA, Y., INUISHI M., "*Sub-Quarter-Micron Dual Gate CMOSFETs with Ultrathin Gate Oxide of 2nm*," Digest of Technical Papers, Symposium on VLSI Technology, pp. 210, 1996.

[98] LABER, C., RAHIM, C.F., DREYER, S.F., UEHARA, G.T., KWOK, P.T., GRAY, P.R., "*Design considerations for a high-performance 3-/spl mu/m CMOS analog standard-cell library*", IEEE J. Solid-State Circuits, vol. 22, no. 2, pp. 181-189, Apr. 1987.

[99] LEBLEBICI, Y., KANG, S.M., "*Hot-Carrier Reliability of MOS VLSI Circuits*," Kluwer Academic Publishers, Norwell, Massachusetts 02061 USA, 1993.

[100] LEE, C.A., LOGAN, R.A., BATDORF, R.L., KLEINMACK, J.J., WIEGMANN, W., "*Ionization Rates of Holes and Electrons in Silicon*," Phys. Rev., vol. 134, pp. A761-A773, May 1964.

[101] LEE, J.C., CHEN, I.C., HU, C., "*Statistical modeling of silicon dioxide reliability*," Proc. Rel. Phys. Symp., vol. 26, pp. 131, 1988.

[102] LEE, S.C., PARK, D.S., SONG, J.H., CHOI, M.W., LEE S.H., "*A Low-Ripple Switched-Capacitor DC-DC Converter for Low-Voltage Applications*," AP-ASIC 2000, Cheju Island, Korea, Aug 2000.

[103] LEUNG, A.M., KO, W.H., SPEAR, T.M., BETTICE, J.A., "*Intracranial pressure telemetry System using semicustom integrated circuits*," IEEE Trans. Biomed. Eng., vol. 33, pp. 386-395, Apr. 1986.

[104] LIANG, M.S., HADDAD, S., COX, W., CAGNINA, S., "*Degradation of very thin gate oxide MOS devices under dynamic high field/current stress*," IEDM Tech. Dig., pp. 394, 1986.

[105] LIANG, Y.C., TAI, L.L., TIEN D., "*Design of MOS-Controlled Smart Power Synchronous Rectifier*," IEEE TENCON 2000, Kuala Lumpur, Sep. 2000.

[106] LILLEHEI, C., GOTT, V., HODGES, P., LONG, D., BAKKEN, E., "*Transistorized pacemaker for treatment of complete heart block*," JAMA, vol. 172, pp. 2006, 1960.

[107] LOMBARDO, S., CRUPI, F., STATHIS, H.H., "*Softening of breakdown in ultra-thin gate oxide nMOSFETs at low inversion layer density*,", IEEE Proc. IRPS'2001, pp. 163-167, 2001.

[108] LUNDSTROM, I., CHRISTENSSON, S., SVENSSON, C., "*Carrier trapping hysteresis in MOS transistors*," Phys. Stat. Sol. A, vol. 1, pp. 395, 1970.

[109] LUO, H., EN, Y., KONG, X., ZHANG, X., "*The Different Gate Oxide Degradation Mechanism under Constant Volatge/Current Stress and Ramp Voltage Stress*," IEEE IRW 2000 Final Report, Poster Presentation,, PP. 141-143, 2000.

[110] LYU, J., PARK, B.-G., CHUN, K., LEE, J.D., "*Reduction of Hot-Carrier Generation in 0.1-μm Recessed Channel nMOSFET with Laterally Graded Channel Doping Profile*," IEEE Electron Device Lett., vol. 18, no. 11, pp. 535-537, 1997.

[111] MAITI, B., "*Nitrided Oxides in CMOS Technology*," International Reliability Physics Symposium (IRPS) Tutorial Proceedings, Section 3, pp. 3.1, 1998.

[112] MAKOWSKI, M.S., "*Realizability Conditions and Bounds on Synthesis of Switched-Capacitor DC-DC Voltage Multiplier Circuits*," IEEE Trans. on Circuits and Systems -1: Fundamental Theory and Applications, vol. 44, no. 8, pp. 684-691, Aug. 1997.

[113] MAKOWSKI, M.S., MAKSIMOVIC, D., "*Performance limits of switched-capacitor DC-DC converters*," IEEE PESC'95 Conf. Rec., pp. 1215-1221, Jun. 1995.

[114] MII, Y., RISHTON, S., TAUR, Y., KERN, D., LII, T., LEE, K., JENKINS, K., QUINLAN, D., BROWN, T.JR., DANNER, D., SEWELL, F., POLCARI, M., "*Experimental high performance sub-0.1 μm channel nMOSFET's*," IEEE Electron Device Lett., vol. 15, pp. 28, 1994.

[115] MIN, K.W., KIM, S.H., "*A High Voltage Generator Using Charge Pump Circuit for Low Voltage Flash Memories*," IEICE Trans. Electron., vol. E82-C, no. 3, pp. 781-784, May 1999.

[116] MIRANDA, E. et al., "*Detection and fitting of the soft breakdown failure mode*," Solid-State Electron., vol. 43, pp. 1801, 1999.

[117] MOAZZAMI, R., HU, C., "*Projecting gate oxide reliability and optimizing reliability screens*," IEEE Trans. Electron Devices, vol. 37, no. 7, pp. 1643-1650, Jul. 1990,

[118] MONNA, G.L., "*Charge pump for Optimal, Dynamic Range Filter*," Proc. ISCAS95, pp. 747-750, Apr. 1995.

[119] MONSIEUR, F., VINCENT, E., PANANAKAKIS, G., GHIBAUDO, G., "*Wear-out, breakdown occurrence and failure detection in 18-25 A^o ultrathin oxides*," Micro. & Reliab., vol. 41, pp. 1035-1039, 2001.

[120] MULLER, D.A. et al., "*The electronic structure at the atomic scale of ultrathin gate oxides*," Nature, vol. 399, pp. 758, Jun. 1999.

[121] NAFRIA, M., SUNE, J., AYMERICH, X., "*Exploratory observations of post-breakdown conduction in polycrystalline-silicon and metal-gated thin-oxide metal-oxide-semiconductor capacitors*," J. Appl. Phys., vol. 73, pp. 205, 1993.

[122] NAFRIA, M., SUNE, J., YELAMOS, D., AYMERICH, X., "*Degradation and Breakdown of Thin Silicon Dioxide Films Under Dynamic Electrical Stress*," IEEE Trans. Electron Devices, vol. 43, no. 12, pp. 2215-2226, Dec. 1996.

[123] NAFRIA, M., SUNE, J., YELAMOS, D., AYMERICH, X., "*Degradation and Breakdown of Thin Silicon Dioxide Films Under Dynamic Electrical Stress*," IEEE Trans. Electron Devices, vol. 43, no. 12, pp. 2215-2226, Dec. 1996.

[124] NAKAGOME, Y. et al., "*An experimental 1.5V 64Mb DRAM*," IEEE J. Solid-State Circuits, vol. 26, no. 4, pp. 465-472, Apr. 1991.

[125] NAKAGOME, Y., TAKEDA E., KUME H., ASAI S., "*New observation of hot-carrier injection phenomena*", Japanese J. Applied Physics, vol. 22, pp. 99-102, 1983.

[126] NG K.K., "*Complete Guide to Semiconductor Devices*," 2nd edition, John Willey & Sons, Inc., TK7871.85N4 2002, ISBN 0-471-20240-1, USA, 2002.

[127] NING T.H., OSBURN C.M., YU, H.N., "*Effect of Electron Trapping on IGFET Characteristics*", J. Electronic Materials, vol. 6, pp. 65-76, 1977.

[128] NING, T.H., OSBURN, C.M., YU, H.N., "*Emission probability of hot electrons from silocon into silocon dioxide*," J. Applied Physics, vol. 48, pp. 286-293, 1977.

[129] NING, T.H., YU, H.N., "*Optically-induced injection of hot electrons into SiO_2*," J. Applied Physics, vol. 45, pp. 5373–5378, 1974.

[130] NISHIOKA, Y., OHJI, Y., MA, T., "*Gate-Oxide Breakdown Accelerated by Large Drain Current in n-Channel MOSFET's*," IEEE Electron Device Letters, vol. 12, no. 3, pp. 134-136, Mar. 1991.

[131] OGIER, J.L., DEGRAEVE, R., ROUSSEL, P., GROESENEKEN, G., MAES, H.E., "*Analysis of the Early Failure Rate Prediction of Time-Dependent Dielectric Breakdown in Thin Oxides*," Proc. European Solid State Device Research Conference (ESSDERC), pp. 299, 1995.

[132] OGURA, S., TSANG, P.J., WALKER, W.W., CRITCHLOW, D.L., SHEPARD, J.F., "*Design and Characteristics of the Lightly Doped Drain-Source (LDD) Insulated Gate Field-Effect Transistor*," IEEE Trans.Electron Devices, vol. ED-27, no. 8, pp. 1359-1367, 1980.

[133] ONG, T.C., KO, P.K., HU, C., "*Hot-carrier current modeling and device degradation in surface-channel p-MOSFETs*," IEEE Trans. Electron Devices, vol. 37, pp. 1658-1666, 1990.

[134] ONG, T.C., SEKI, K., KO, P.K., HU, C., "*Hot-carrier-induced degradation in p-MOSFET under AC Stress*," IEEE Elecron Device Letters, vol. 9, pp. 211-213, 1988.

[135] OPRIS, I.E., "*Analog Rank Extractors and Sorting Networks*," Ph.D. dissertation, Stanford Univ., Stanford, CA, Feb. 1996.

[136] PAN, H., LIANG, Y.C., ORUGANTI, R., "*Design of Smart Power Synchronous Rectifier*," IEEE Trans. Power Elec., vol. 14, no. 2, pp.308-315, Mar. 1999.

[137] PANTISANO, L., CHEUNG, K.P., "*Stress-Induced Leakage Current (SILC) and Oxide Breakdown: Are They From the Same Oxide Traps?*," IEEE Trans. Device and Materials Reliability, vol. 1, no. 2, Jun. 2001.

[138] PHANG, K., JOHNS, D., "*A 1V 1mW CMOS Front-End with on-chip Dynamic Gate Biasing for a 75Mb/s Optical Receiver*," IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, pp. 218-219, Feb. 2001.

[139] PIERRET, R.F., "*Semiconductor Device Fundamentals*," Addison-Wesley Publishing Company, TK7871.85.P484 1996, ISBN 0-201-54393-1, USA, 1996.

[140] POLISHCHUK, I., YEO, Y., LU, Q., KING, T., HU, C., "*Hot-Carrier Reliability Comparison for pMOSFETs With Ultrathin Silicon-Nitride and Silicon-Oxide Gate Dielectrics*," IEEE Trans. Device and Materials Reliability, vol. 1, no. 3, Sep. 2001.

[141] POMPL, T., WURZER, H., KERBER, M., EISELE, I., "*Investigation of ultra-thin gate oxide reliability behavior by separate characterization of soft breakdown and hard breakdown*," IEEE IRPS, pp. 40, 2000.

[142] PUSHKAR, P., SARASWAT, K.C., "*Correlation of trap Generation to Charge-to-Breakdown (Qbd): A Physical-Damage Model of Dielectric Breakdown*," IEEE Trans. Electron Devices, vol. 41, no. 9, pp. 1595-1602, Sep. 1994.

[143] QIU, F., "*Analog Very Large Scale Integrated Circuits Design of Two-Phase and Multi-Phase Voltage Doublers*," for the Degree of Master of Science, Ohio Univ., Nov. 1999.

[144] RAMIREZ-ANGULO, J., "*High Frequency Low Voltage CMOS Diode*," Electronics Letters, vol. 28, no. 3, pp. 298-299, 1992.

[145] RASRAS, M., DE WOLF, I., GROESENEKEN, G., DEGRAEVE, R., MAES, E., "*Substrate Hole Current after Oxide Breakdown*," IEDM'00, pp. 537-540, 2000.

[146] RICCO, B., YA AZBEL, M., BRODSKY, M.H., "*A novel mechanism for tunneling and breakdown in thin SiO2 films*," Phys. Rev. Lett., vol. 51, pp. 1795, 1983.

[147] RODDER, M., AUR, S., CHEN, I.-C., "*A scaled 1.8 V, 0.18 μm gate length CMOS technology: device design and reliability considerations*," International Electron Devices Meeting, pp. 415-418, Dec. 1995.

[148] ROUSCHE, P.J., NORMANN, R.A., "*Chronic Intracortical Microstimulation (ICMS) OF Cat Sensory Cortex Using the Utah Intracortical Electrode Array*," IEEE Trans. Rehab. Eng., vol. 7, no. 1, pp. 56-68, Mar. 1999.

[149] SABNIS, A.G., CLEMENS, J.T., "*Characterization of the electron mobility in the inverted <100> Si surface*,", *IEDM Tech. Dig.*, pp. 18–21, 1979.

[150] SAI-HALASZ, G.A., "*Directions in future high-end processors*," Proc. IEEE ICCD, pp.230, 1992.

[151] SAKURAI, T., NOGAMI, K., KAKUMU, M., IIZUKA, T., "*Hot-carrier generation in submicrometer VLSI environment*", IEEE J. Solid-State Circuits, vol. 21, no. 1, pp. 187-192, Feb. 1986.

[152] SAWADA, K., SUGAWARA, Y., MASUI, S., "*An On-Chip High-Voltage Generator Circuit for EEPROMs with a Power Supply Voltage below 2V*," Symp. On VLSI Circuits, Dig. Of Technical Papers, pp. 75-76, 1995.

[153] SCHUEGRAF, K.F., HU, C., "*Hole injection SiO2 breakdown model for very low voltage lifetime extrapolation*," *IEEE Trans.Electron Devices*, vol. 41, pp. 761, 1994.

[154] SCHUEGRAF, K.F., HU, C., "*Hole injection SiO_2 breakdown model for very low voltage lifetime extrapolation*," IEEE Trans. Electron Devices., vol. 41, no. 5, pp. 761, 1994.

[155] SEMICONDUCTOR INDUSTRY ASSOCIATION (SIA), "*International Technology Roadmap for Semiconductors Accelerates Pace to Smaller Chip Dimensions*," Press presentation, pp. 16, San Jose, California, U.S.A., Nov. 2001.

[156] SHAH, M.R., PHILLIPS, R.P., NORMANN, R.A., "*A study of printed Spiral Coils for Neuroprosthetic Transcranial Telemetry Applications*," IEEE Trans. Biomed. Eng., vol. 45, no. 7, pp. 867-875, Jul. 1998.

[157] SHIGA, K., KOMORT, J., KATSUMATA, M., TERAMOTO, A., MASHIKO, Y., "*Characterization of Extrinsic Oxide Breakdown on Thin Dielectric Oxide*," IEICE Trans. Electron., vol. E82-C, no. 4, pp. 589-592, Apr. 1999.

[158] SILVA-MARTINEZ, J., "*A Switched Capacitor Double Voltage Generator*," IEEE Proc. Mid-West Symp. Circuits and Systems, vol. 1, pp. 177-180, 1994.

[159] SMITH, B., PECKHAM, P.H., KEITH, M.W., ROSCOE, D.D., "*An externally powered, multi-channel, implantable stimulator for versatile control of paralyzed muscle*," IEEE Trans. Biomed. Eng., vol. 34, pp. 499-508, Jul. 1987.

[160] STARZYK, J.A., JAN, Y.W., "*A DC-DC Charge Pump Based on Voltage Doublers*," submitted to IEEE Trans. Circuits and Systems. Part I.

[161] STATHIS, J.H., "*Percolation theory*," J. Appl. Phys., vol. 86, pp. 5757, 1999.

[162] STATHIS, J.H., DIMARIA, D.J., "*Reliability projections for ultra-thin oxides at low voltage*," IEDM Tech. Dig., pp. 167, 1998.

[163] STATHIS, J.H., VAYSHENKER, A., VAREKEMP, P.R., WU, E.Y., MONSTROSE, C., MCKENNA, J., DIMARIA, D.J., HAN, L.K., CARTIER, E., WACHNIK, R.A., LINDER, B.P., "*Breakdown measurements of ultrathin SiO_2 at low voltage*," VLSI Symp., pp. 94, 2000.

[164] STEYAERT, M.S.J., DEHAENE, W., CRANINCKX, J., WALSH, M., REAL, P., "*A CMOS Rectifier-Integrator for Amplitude Detection in Hard Disk Servo Loops*," IEEE J. Solid-State Circuits, vol. 30, no. 7, pp. 743-751, Jul. 1995.

[165] STOCKINGER, M., "*Optimization of Ultra-Low-Power CMOS Transistors*," Dissertation of Thesis for PhD. On Electronics, Wien, Jan. 2000.

[166] STORTI, S., CONSIGLIERI, F., PAPARO, M., "*A 30-A 30V DMOS Motor Controller and Driver*," IEEE J. Solid-State Circuits, vol. 23, no. 3, pp. 1394-1402, Dec. 1988.

[167] SU, L. et al., "*A High performance 0.08 μm CMOS*," VLSI Technology Symp., Tech. Dig., pp. 12, 1996.

[168] SUANING, G.J., LOVELL, N.H., "*CMOS Neurostimulation ASIC with 100 Channels, Scaleable Output, and Bidirectional Radio-Frequency Telemetry*," IEEE Trans. Biomed. Eng., vol. 48, no. 2, pp. 248-260, Feb. 2001.

[169] SUEHLE, J., VOGEL, E.M., WANG, B., BERNSTEIN, J.B., "*Temperature dependence of soft breakdown and wear-out in sub-3 nm SiO2 films*," IEEE Proc. IRPS'2000, pp.33-39, 2000.

[170] SUEHLE, J.S., CHAPARALA, P., "*Low Electric Field Breakdown of Thin SiO_2 Films Under Static and Dynamic Stress*," IEEE Trans Electron Devices, vol. 44, no. 5, pp. 801-808, May 1997.

[171] SUGIHARTO, D.S., YANG, C.Y., HUY LE, H., CHUNG, J.E., "*Beating Heat: Improving MOS Hot-Carrier Reliability through Analysis, Modeling, and Simulation,*" IEEE Circuits and Devices, pp. 43-51, 1998.

[172] SUMANEN, L., WALTARI, M., HALONEN K., "*A Mismatch insensitive CMOS Dynamic Comparator for Pipeline A/D Converters*," IEEE Int. Conf. Electronics, Circuits and Systems (ICECS), Volume 1, pp. 32-35, Dec. 2000.

[173] SUNE, J., MURA, G., MIRANDA, E., "*Are Soft Breakdown and Hard Breakdown of Ultrathin Gate Oxides Actually Different Failure Mechanisms?*," IEEE Electron Device Letters, vol. 21, no. 4, pp. 167-169, Apr. 2000.

[174] SUNE, J., MIRANDA, E., NAFRIA, M., AYMERICH, X., "*Modeling the breakdown spots in silicon dioxide films as point contacts*," Appl. Phys. Lett., vol. 75, pp. 959, 1999.

[175] SUNE, J., PLACENCIA, I., BARNIOL, N., FARRE,S E., MARTIN, F., AYMERICH, X., "*On the breakdown statistics of very thin SiO films*," Thin Solid Films, vol. 185, pp. 34, 1990.

[176] SZE, S.M., "*Physics of Semiconductor Devices*," ISBN 0471842907, Wiley, New York, 2002.

[177] SZE, S.M., "*Semiconductor Devices: Physics and Technology*," 2nd edition, John Willey & Sons, Inc., TK7871.85 .S9883 2001, ISBN 0-471-33372-7, USA, 2002.

[178] TAKEDA, E., KUME, H., TOYABE, T., ASAI, S., "*Submicron MOSFET structure for minimizing hot-carrier generation*," IEEE Trans. Electron Devices, vol. 29, pp. 611-618, 1982

[179] TAKEDA, T., YANG, C.Y., MIURA-HAMADA, A., "*Hot-carrier effects in MOS devices*," Academic Press, 1995.

[180] TAM, S., KO, P.K., HU, C., "*Lucky-Electron Model of Channel Hot-Electron Injection in MOSFET's*," IEEE Trans. Electron Devices, vol. 31, pp. 1116-1125, 1984.

[181] TAMURA, T. et al., "*Transcutaneous optical power converter for implantable devices*," Proc. SPIE, vol. 2084, pp. 99-104, 1996.

[182] TANG, J.Y., HESS, K., "*Theory of hot electron emission from silicon into silicon dioxide*," J. Applied Physics, vol. 54, pp. 5145–5151, 1983.

[183] TAUR, Y., BUCHANAN, D.A., CHEN, W., FRANK, D.J., ISMAIL, K.E., LO, S.H., SAIHALASZ, G.A., VISWANATHAN, R.G., WANN, H.C., WIND, S.J., WONG, H.S., "*CMOC Scaling into the Nanometer Regime*," Proc. IEEE, vol. 85, no. 4, Apr. 1997.

[184] TAUR, Y., NOWAK, E.J., "*CMOS devices below 0.1 μm: how high will performance go?*," International Electron Devices Meeting, Technical Digest., pp. 215-218, Dec. 1997.

[185] TAYLOR, G.W., "*Subthreshold Conduction in MOSFET's*," IEEE Trans. Electron Devices, vol. ED-25, no. 3, pp. 337-350, Mar. 1978.

[186] TEHOVNIK, E.J., "*Electrical Stimulation of Neural Tissue to Evoke Behavioral Responses*," J. Neuroscience Methods, vol. 65, pp. 1-17, 1996.

[187] THOMPSON, S., PACKAN, P., BOHR, M., "*MOS Scalling: Transistor Challenges for the 21st Century*," Intel Technology Jurnal, 3rd Quarter, 1998.

[188] THOMPSON, S.E., PACKAN, P.A., BOHR, M.T., "*Linear versus saturated drive current: tradeoffs in super steep retrograde well engineering*," Symposium on VLSI Technology, Dig. Tech. Papers, pp. 154-155, Jun. 1996.

[189] TORIUMI, A., YOSHIMI, M., TANIGUCHI, K., "*Study of gate current and reliability in ultra-thin gate oxide MOSFETs*", Tech. Dig. VLSI, Technology Symposium, pp. 110-11,1985.

[190] TROUTMAN, R.R., "*VLSI limitations from drain-induced barrier-lowering*," IEEE Trans. Electron Devices, vol. ED-25, pp. 1344, Nov. 1978.

[191] TROYK, PH.R., "*Multi-channel Transcutaneous Cortical Stimulation System-Progress Reports*," Illinois Institute of Technology, 2001.

[192] TSAI, M.Y., LIN, H.C., LEE, D.Y., HUANG, T.Y., "*Post-Soft-Breakdown Characteristics of Deep Submicron NMOSFETs with Ultrathin Gate Oxide*," IEEE Elecron Device Letters, vol. 22, no. 7, pp. 348-350, Jul. 2001.

[193] TSUCHIYA, T., OKAZAKI, Y., MIYAKE, M., KOBAYASHI, T., "*New hot-carrier degradation mode and lifetime prediction method in quarter-micrometer PMOSFET*," IEEE Trans. Electron Devices, vol. 39, pp. 404-408, Feb. 1992.

[194] UENO, S.F., INOUE, T., HARADA, I., "*Emergency Power Supply for Small Computer systems*," IEEE ISCAS, pp. 1065-1068, Jun. 1991.

[195] UMEZAWA, A. et al., "*A 5-V-Only Operation 0.6-μm Flash EEPROM with Row Detector Scheme in Triple-Well Structure*," IEEE J. Solid-State Circuits, vol. 27, no. 11, pp. 1540-1545, Nov. 1992.

[196] VAN ZEGHBROECK, B., "*Principals of semiconductor devices*," handout, 2002.

[197] VENKATESAN, S., LUTZE, J.W., LAGE, C., TAYLOR, W.J., "*Device drive current degradation observed with retrograde channel profiles*," International Electron Devices Meeting, pp. 419-422, Dec. 1995.

[198] VINCENT, E, "*Dissertation of Thesis for PhD*," INPG Grenoble, 1996.

[199] VINCENT, E., PAPADAS, C., RIVA, C., GHIBAUDO, G., "*On The Charge Build-Up Mechanisms in Very Thin Insulator Layers*," Proc. ESSDERC'96, pp. 495-498, Bologna (Italy), Sep. 1996

[200] WANG, C.C., WU, J.C., "*Efficiency Improvement in Charge Pump Circuits*," IEEE J. Solid-State Circuits, vol. 32, no. 6, pp. 852-860, Jun. 1997.

[201] WEIR, B. ET AL., "*Gate oxide reliability projection to the sub-2-nm regime*," Semicond. Sci. Technol., vol. 15, pp. 455, 2000.

[202] WEIR, B., SILVERMAN, P.J., MONROE, D., KRISCH, K.S., ALAM, M.A., ALERS, G.B., SORSCH, T.W., TIMP, G.L., BAUMANN, F., LIU, C.T., MA, Y., HUANG, D., "*Ultra-thin gate dielectrics: They breakdown, but do they fail?*," IEDM Tech. Dig., pp. 73–76, 1997.

[203] WITTERS, J.S., GROESENEKEN, G., MAES, H.E., "*Analysis and Modeling of On-Chip High-Voltage Generator Circuits for Use in EEPROM Circuits*," IEEE J. Solid-State Circuits, vol. 24, no. 5, pp. 1372-1380, Oct. 1988.

[204] WOLF, S., "*The Submicron MOSFET*," Silicon Processing for the VLSI Era, Lattice Press, vol. 3, Sunset Beach, CA, 1995.

[205] WOLTERS, D.R., VAN DER SCHOOT, J.J., "*Kinetics of charge trapping in dielectrics,*" J. Applied Physics, vol. 58, no. 2, pp. 831-837, Jul. 1985.

[206] WOLTJER, R., HAMADA, A., TAKEDA, E., "*Time dependence of p-MOSFET hot-carrier degradation measured and interpreted consistently over ten orders of magnitude*," IEEE Trans. Electron Devices, vol. 40, pp. 392, 1993.

[207] WONG, H.S., TAUR, Y, "*Three-dimensional atomistic simulation of discrete random dopant distribution effects in sub-0.1μm MOSFET's*," IEDM Tech. Dig., pp. 705, 1993.

[208] WONG, S.L., VENKITASUBRAMANIAN, S., KIM, M.J., YOUNG, J.C., "*Design of a 60 V 10A Intelligent Power Switch Using Standard Cells*," IEEE J. Solid-State Circuits, vol. 27, no. 3, pp. 429-434, Mar. 1992.

[209] WRATHALL, R.S., "*The Design of A High Power Solid State Automative Switch in CMOS-VDMOS Technology*," IEEE Power Electron. Specialist Conf. Rec., pp. 229-233, 1985.

[210] WU, E., NOWAK, E., VAYSHENKER, A., MCKENNA, J., HARMON, D., VOLLERTSEN, R.P., "*New Global Insight in Ultrathin Oxide Reliability Using Accurate Experimental Methodology and Comprehensive Database*," IEEE Trans. Device and Materials Reliability, vol. 1, no. 1, pp. 69-80, Mar. 2001.

[211] WU, E.Y., AITKEN, J., NOWAK, E., VAYSHENKER, A., VAREKEMP, P., HUCKEL, G., MCKENNA, J., HARMON, D., HAN, L.K., MONSTROSE, C., DUFRESNE, R., "*Voltage-dependent voltage acceleration of oxide breakdown for ultra-thin oxides*," IEDM, pp. 54, 2000.

[212] WU, E.Y., NOWAK, E., ABADEER, J., HAN, L.K., LO, S., "*Structural dependence of dielectric breakdown in ultra-thin gate oxides and its relationship to soft-breakdown modes and device failures*," IEDM Tech.Dig., pp. 187–190, 1998.

[213] WU, J., CHANG, K., "*MOS Charge Pumps for Low-Voltage Operation*," IEEE J. Solid-State Circuits, vol. 33, no. 4, pp. 592-597, April 1998.

[214] YANG, K.N., HUANG, H.T., CHEN, M.J., LIN, Y.M., YU, M.C., JANG, S.M., YU, C.H., LIANG, M.S., "*Edge Hole Direct Tunneling in Off-State Ultra-thin Gate Oxide p-Channel MOSFETs*," IEDM Tech. Dig., pp. 679–682, 2000.

[215] YANG, N., HENSON, W.K., WORTMAN, J., "*A Comparative Study of Gate Direct Tunneling and Drain Leakage Currents in N-MOSFET's with Sub-2 nm Gate Oxides*," IEEE Trans. Electron Devices, vol. 47, no. 8, Aug. 2000.

[216] YEAP, G.C., "*Leakage Current in Low Standby Power and High Performance Devices: Trends and Challenges*," Proc. International Symposium on Physical Design, California, USA, Apr. 2002.

[217] YEOH, T.S., KAMAL, N.R., HU, S.J., "*Gate oxide breakdown model in MOS transistors*," Proc. Int. Rel. Phys. Symp., pp.149-155, 2000.

[218] ZOLL, P., "*Resuscitation of the heart in ventricular standstill by external stimulation*," New Eng. J. Med., vol. 274, pp. 768, 1952.

Appendix A

Device Scaling and Short-Channel Effects

After more than two decades of relentless scaling to ever smaller dimensions for higher packing density, faster circuit speed, and lower power dissipation, CMOS technology has become the prevailing technology for very large scale integration (VLSI) applications today [20-21]. Figure A-1 shows the trends of power supply voltage (V_{DD}), threshold voltage (V_T), and gate oxide thickness (T_{Ox}) versus channel length (L) for CMOS logic technologies [183].

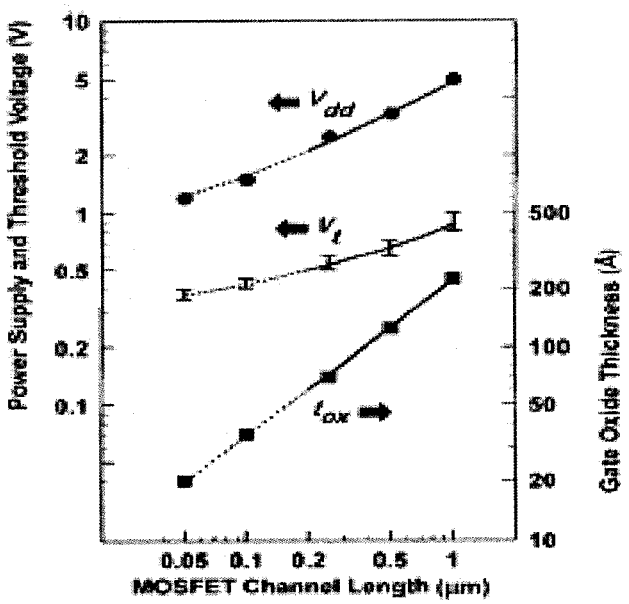


Figure A- 1: Plot of V_{DD}, V_T and t_{OX} trends versus L for MOS technologies

Starting at a minimum feature length of 10 μm in 1970 the gate length was gradually reduced to 0.15 μm minimum feature size in 2000, resulting in a 13% reduction per year.

In order to maintain this rapid rate of improvement, not only oxide scaling, but also other dimensions such as the gate/source and gate/drain alignment, and the depletion layer widths should be down sized and aggressive engineering of the source/drain and well regions would be required. Creating shallow Source/Drain Extension (SDE) profiles for improved short channel effects, the use of retrograde and halo well profiles to improve leakage characteristics, and the relatively scaling of the gate oxide thickness to maintain the control over the channel are of the major solutions [188]. Here, we address a few major challenges and possible improvements [21,63,94,183].

Basic equations of the MOS are applicable only to a long-channel device where the channel length is large compared to the source and drain depletion width. It implicitly assumes that the gate is completely responsible for depleting the semiconductor and the charges contained in the surface depletion region of the substrate are induced solely from the field created by the gate voltage.

As channel length is reduces to shorter than ≈1 μm, e.g. short-channel, however, the fields originating from the source/drain regions may influence the charge distribution and, thus, part of the depletion is accomplished by the drain and source bias. One common approach to explain some of the short-channel effects is charge sharing due to geometrical effect. Figure A-2 shows that charge induced by the gate in the depletion layer has a trapezoidal shape instead of previously assumed rectangular.

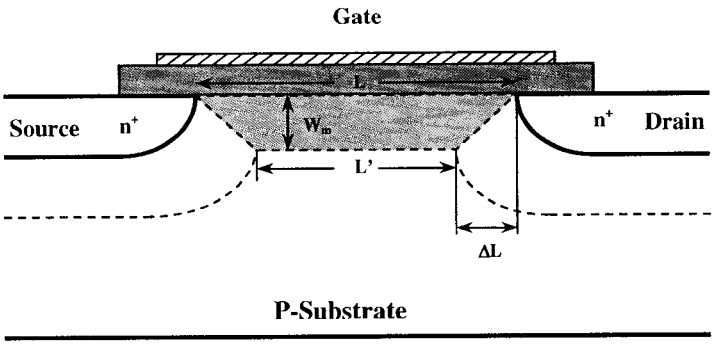


Figure A-2: Charge-sharing effect for short-channel devices

As the MOS devices are scaled down, the power supply voltage has not been scaled in proportion to the channel length. Therefore, the electric field strength has been exceeding the limits for oxide and silicon layers reliability. At such high fields, several undesirable effects as like as increase in threshold voltage and junction leakage currents as well as electron and hole mobility degradation [32,149] may occur which degrades the performance of the device.

The short-channel affects the characteristics of the device such as effective channel length, threshold voltage, carrier velocity saturation, mobility, output impedance, and some equations have to be modified to account for the effect so called, short-channel effect. It can be realized that the short-channel effects are reduced if the junction depth is reduced as the trapezoid approaches a rectangle [126,177].

A.1 Channel length Modulation

Channel length modulation in a MOSFET is caused by the increase of the depletion layer width at the drain. In the saturation region, as drain voltage increases, the depletion region

near drain expands and the pinch-off point of the channel moves back towards source, as illustrated in Figure A-3. This leads to a shorter channel length.

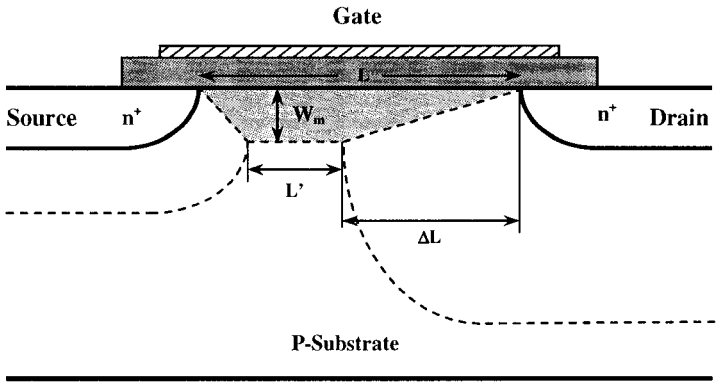


Figure A-3: Depletion layer with a large drain bias

Hence, it is required to introduce a more accurate description of the channel length that is the spacing between the depletion edges of the source and drain rather than the distance between metallurgical junctions [126]. Provided the device has a channel length fairly greater than depletion width, the change in channel length is approximated by difference in the depletion width of a step junction as follow [76]:

$$\Delta L \approx -\sqrt{\frac{2\varepsilon_S}{qN_A}} \cdot \left(\sqrt{V_D} - \sqrt{V_{DSAT}}\right) \tag{A-1}$$

where ε_S is silicon permittivity and N_A is substrate doping concentration. The drain current bearing channel length modulation parameter, λ, then could be expressed as equation (A-2) [92]:

$$I_{DSAT} = \frac{W}{2L}\mu_n C_{OX}\left(V_G - V_{DS}\right)^2 \cdot \left(1 + \lambda V_{DS}\right) \tag{A-2}$$

As drain current is in reverse proportion with effective channel length, $\lambda \propto 1/L$ shorter

channel results in an increased drain current as shown in Figure A-4. An extreme case of channel length modulation is punch-through where the channel length reduces to zero.

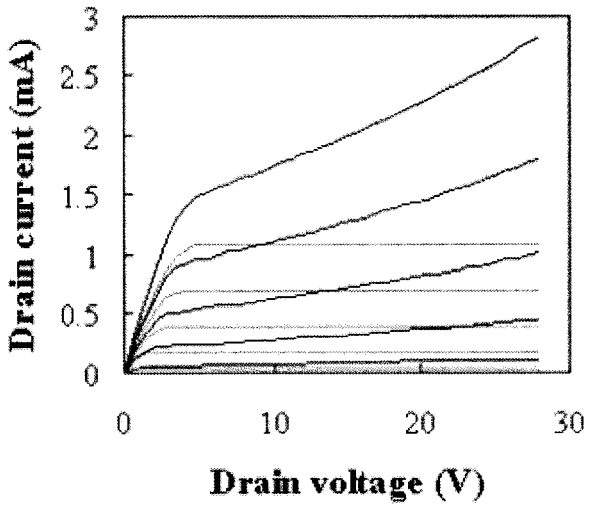


Figure A-4: Drain currents for short- and long-channel devices [196]

The channel length modulation effect typically increases in small devices with low-doped substrates. From (A-1) we note that proper scaling can reduce channel length modulation, namely by increasing the substrate doping density as the gate length is reduced.

A.2 Mobility Degradation

This effect is related to the gate voltage and appears even at the smallest drain-to-source voltages. The simple model predicts a linear region for the transfer characteristic (I_{DS} versus V_{DS}) of a MOS for small V_{DS}. However, experimental data frequently show a deviation from the expected linear dependence. This smaller than expected drain current is due to reduction of channel-carrier mobility. The principal model assumes constant

mobility μ_0 of the carriers in the channel. The mobility is the inversion layer is distinctly lower than in bulk material. This is due to the fact the electron wave-function extends into the oxide and the carrier mobility is lowered due to the lower mobility in the oxide. Higher electric fields at the surface, as typically obtained in scaled down devices, rather squeezes the inversion layer and push the electron wave-function even more into the oxide yielding a field dependent mobility. The mobility at the surface, then varies in proportion with reverse cubic root of the electric field [196]:

$$\mu_S \propto \varepsilon^{-1/3} \tag{A-3}$$

By other words, in reality, the gate voltage-induced vertical field influence the carrier-scattering mechanisms in the channel. Due to vertical electric field, surface roughness and Coulombic interactions with surface charges, the carrier scattering mechanisms in the very thin inversion layer are multiple and rather complex. However, a number of those scattering mechanisms depend on the inversion-layer thickness, and consequently on the applied gate voltage. As the physically based equations of the mobility dependence on the gate voltage are complex, the following widely accepted semiempirical equation is presented [56]:

$$\mu_S = \frac{\mu_0}{1+\eta(V_{GS}-V_T)} \tag{A-4}$$

Where the so-called surface-mobility, μ_S, is now used instead of the low-field mobility, μ_0. The parameter η is empirical constant. In near-threshold region (small V_{GS}-V_T), the added item in denominator, does little effect, however, at moderate and high gate voltages, the effect becomes pronounced. Figure A-5 illustrates the variation of surface

mobility versus vertical electric field [177]. Hence, as the gate voltage increases, the surface mobility decreases which lasts in the actual drain current falling increasingly.

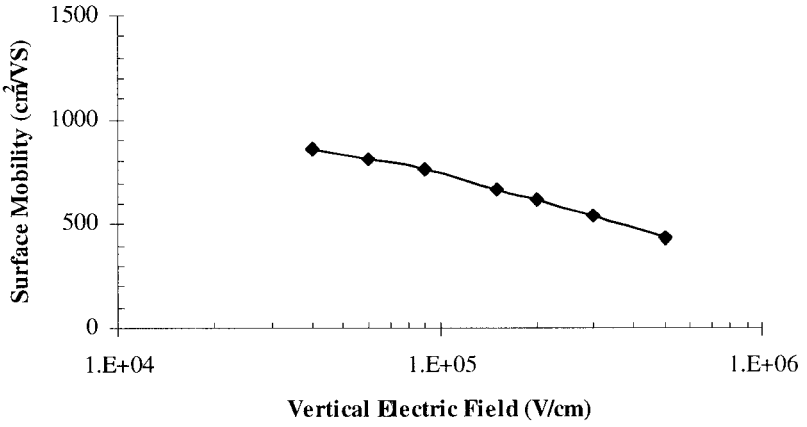


Figure A-5: Surface mobility degradation versus electric field

A.3 Carrier Velocity Saturation

Channel carrier mobility can also be reduced by a high lateral field in the channel, instead of vertical field in last case. The mobility relates drift velocity to the electric field. At small electric field, the drift velocity increases linearly with the electric field, which leads to the appearance of lateral field independent carrier mobility us. Long-channel MOS operate in the low-field region. At higher electric fields, the drift velocity deviates from the linear dependence and even saturates, which is illustrated in Figure A-6.

This happens because of increased scattering rate of highly energetic electrons, primarily due to optical phonon emission. Hence, the transit time of carriers through the channel increases [196]. To account for velocity saturation, the mobility has to be reduced.

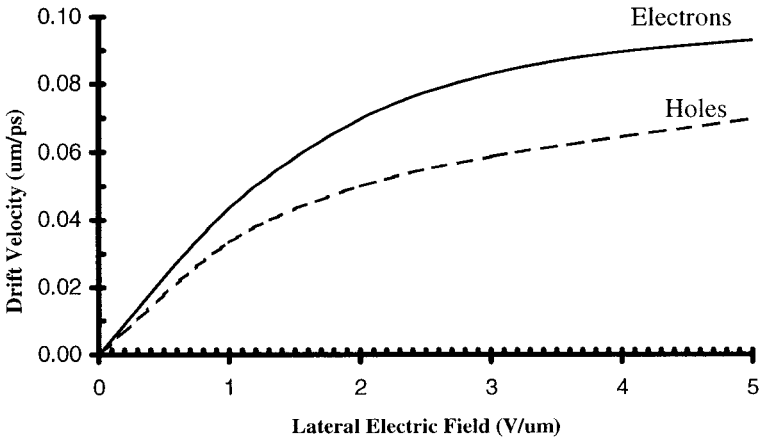


Figure A-6: Drift Velocity versus Electric Field [56]

As the lateral electric field is proportional to V_{DS}/L_{eff}, the effective mobility can be expressed in terms of the drain voltage and the effective channel length as follow [56]:

$$\mu_{eff} = \frac{\mu_S}{1 + \frac{\mu_S}{v_{max}} \cdot \frac{V_{DS}}{L_{eff}}} \tag{A-5}$$

where v_{max} is maximum drift velocity which has a typical value of $1-2\times10^5$ m/s in silicon. As the channel length, L, is reduced while the supply voltage is not, the tangential electric field increases along the channel, and the carrier velocity saturates at a critical electric field. This critical value is $\approx 1-2\times10^4$ V/cm for electrons. Hence, for n-channel MOS with L < 1 μm, velocity saturation causes the channel current to reach saturation before saturation region. Critical electric field is approximately $\approx 5\times10^4$ V/cm for holes. Therefore, this effect does not occurs for p-channel MOS until L < 0.25 μm. When electric field exceeds the critical value, the drain current is reduced which results in

extension of the saturation region. The drain current, I_D, in saturation region, would be linearly proportional to V_{GS} [126].

$$I_{Dsat} = WC_{OX}\left(V_{GS} - V_T\right)\cdot v_{\max} \tag{A-6}$$

Notice that the current is now independent of the channel length and is a linear function of V_{GS} rather than the square function, which was the case for long-channel devices.

A.4 Threshold Voltage Variation

One of the most important parameters of the MOS is the threshold voltage, that is the minimum required gate voltage to form the channel. Typically, the threshold voltage is adjusted through ion implantation into the channel region. The threshold voltage, V_T, of the MOS, as given by the following principal equations, is considered independent on the channel length and width and could changed only by substrate bias, V_{SB} [56]. Substrate bias can influence V_T because it makes the depletion region to be widened and therefore, a higher threshold voltage is required to achieve inversion in channel. Threshold voltage could also be controlled by varying the oxide thickness resulting in change of field strength.

$$V_T \approx V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F + V_{SB}} \tag{A-7}$$

$$V_{FB} = \phi_{ms} - \frac{qN_{OX}}{C_{OX}} \tag{A-8}$$

$$\phi_F = \frac{2kT}{q}\ln\frac{N_A}{n_i} \tag{A-9}$$

$$\gamma = \frac{\sqrt{2\varepsilon_S q N_A}}{C_{ox}} \tag{A-10}$$

Here, it is assumed that channel depletion region is exclusively created by gate voltage and the effect of depletion regions around source and drain were neglected. Such an assumption is valid if channel length is much longer than depletion region depths. Practically, in short-channel devices, depletion regions from drain and source extend into channel. and cause threshold voltage variations. The threshold voltage dependence on the doping density for both n- and p-type MOSs with an aluminum gate metal is depicted in Figure A-7.

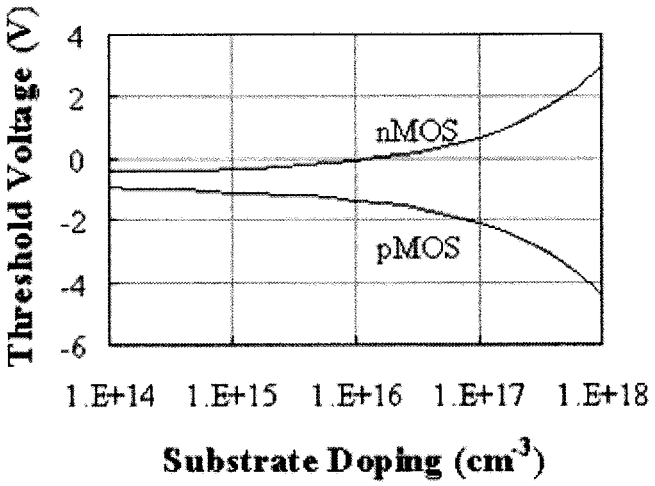


Figure A-7: Threshold voltage versus substrate doping density [196]

The threshold of both types of devices is slightly negative at low doping densities. The threshold of NMOS increases with doping while the threshold of PMOS decreases with doping in the same way. It is shown in Figure A-1 that as the MOSFET channel length is scaled down, power supply voltage is reduced as well to keep active power and electric

field (reliability) within reasonable limits [47]. Besides power management systems with architectural innovation, the most effective way to curb the growth of active power is to reduce the power supply voltage. Figure A-1 also illustrates that in contrast to the power supply voltage, the threshold voltage has not been scaled nearly as much. This is because a minimum threshold voltage of 0.3 – 0.4 V is required, below which the standby power due to off-state leakage current becomes prohibitively high. Using multiple threshold voltage devices [21] or Dynamic threshold devices are new approaches.

A.4.1 Threshold Roll-off

In reality, when the channel length and width are much larger than the channel region affected by fringing field at the channel edges (edge effect), the threshold voltage would be independent on the channel length and width. However, when the channel length or width is reduced to dimensions that are comparable to the edge–affected region, the threshold voltage experiences dependencies on the channel length or width. Figure A-8 illustrates the edge effect by the electric field (arrows) appearing in the depletion layer.

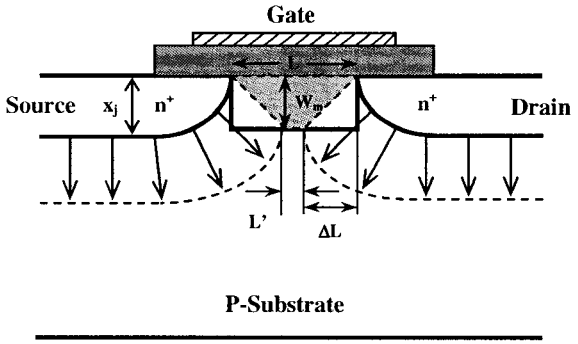


Figure A-8: Threshold voltage-related short-channel effect

The electric-field lines originate at the positive charge centers in the gate or n+ regions of drain/source, and terminate at negative charge centers in the substrate depletion region. Here, we have ignored the depletion depth inside diffusion zones. It can be seen that the electric field lines at the ends of the channel originate from the source/drain regions and not the gate.

Consequently, some charge at the edges of the depletion layer is linked to source and drain charge, and not to the gate charge. The presence of the source/drain-related edge effect means that less gate charge, and consequently less gate voltage, is needed to create the depletion layer under the channel. The principal MOS equations, estimates the gate voltage needed to create the rectangular depletion layer under the channel which overestimates the required voltage related to the charge inside the trapezoidal area. The threshold voltage shift, V_{TO}, could be simply obtained from the ratio of rectangle area ($L \times W_m$) to the trapezoidal area $(L+L')W_m/2$.

In long-channel MOS, the edge charge created by the source and drain is much smaller compared to the total charge. This can be seen by comparing the rectangular and the trapezoidal areas. Consequently, the basic equations correctly expresses the voltage needed to create the depletion layer under the channel. Therefore, the threshold voltage does not show dependence on the gate length. In the case of short-channel MOS, the charge enclosed in the trapezoidal area is significantly smaller than the charge inside the rectangular area. This is because the edge effect is now pronounced, and the source and

drain-related field are creating an observable portion of the depletion layer under the channel. To model this effect, a charge sharing factor, F_S, is introduced which is calculated as the ratio between the trapezoidal and the rectangular areas. Therefore, the equation for the threshold voltage would be modified as follow:

$$V_T \approx V_{FB} + 2\phi_F + F_S \cdot \gamma\sqrt{2\phi_F + V_{SB}} \tag{A-11}$$

A number of different equations for the charge-sharing factor, F_S, have been developed [56]. Using F_S, the shift in threshold voltage could be expressed as below [177].

$$\Delta V_{TO} = \frac{-1}{C_{OX}} \cdot \frac{qN_A W_m x_j}{L} \cdot \left(\sqrt{1 + \frac{2W_m}{x_j}} - 1 \right) \tag{A-12}$$

Where N_A is the substrate doping concentration, W_m the depletion width, x_j the junction depth, L the channel length, and C_{ox} the gate oxide capacitor per unit. It can be seen that the change in threshold voltage is proportional to the ratio of xj/L. Figure A-9 shows the dependence of the threshold voltage to the channel length.

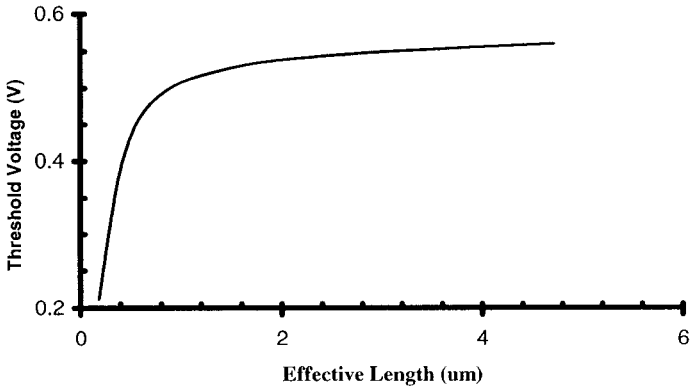


Figure A-9: Threshold dependence on the channel length

Therefore, as channel length decrease, which is the case for new process, the threshold

voltage decreases as well. Note that threshold roll-off describes the threshold reduction in linear region where V_{DS} is still small.

A.4.2 Channel engineering

To scale down MOSFET channel length without excessive short-channel effect, both the oxide thickness and the gate-controlled depletion width in silicon must be reduced in proportion to L. The latter requires increased channel-doping concentration which, for a uniformly doped channel, leads to higher depletion charge and electric field at the silicon surface. These in turn cause the potential across the oxide and therefore the threshold voltage to go up. By changing the doping profile in the channel region, the distribution of the electric field and potential contours can be changed. Retrograde Wells and halo implants have been used to optimize the channel profile and increase the transistor linear and saturated drive current without causing an increase in the off-state leakage current [24,90,147,187,197]. Retrograde and halo profiles represent non-uniform channel doping in vertical and lateral directions, respectively as illustrated in Figure A-10.

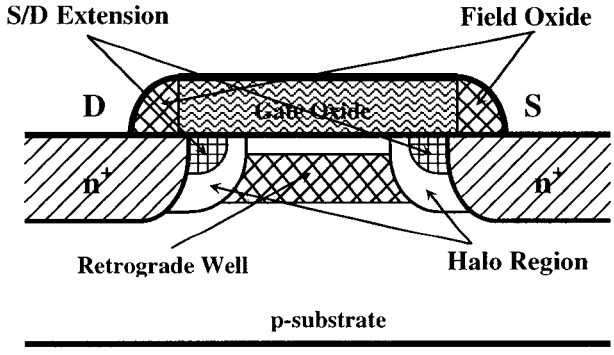


Figure A-10: Well Engineering representation

The former changes the 1D characteristics of the well profile by creating a retrograde profile toward the Si/SiO_2 surface. It has been established that it can improve short channel effects, increase surface mobility, and lead to either an increase or a decrease in saturated drive current depending on a variety of technology issues [147,187,197]. Unlikely, it compromises substrate sensitivity (body-effect) and subthreshold leakage. Halo implants places pockets of high-doping regions at two lower corners of the gate-controlled depletion region where the potential difference between the source/drain and the substrate is the highest while, in the middle of the channel and under the gate, the doping concentration remains low in order to keep the gate depletion charge to a minimum. It has been shown that halo profile improves short channel effects [81,114,167,184] and provides increased source-to-drain barrier for current flow.

A.4.3 Drain-Induced Barrier Lowering (DIBL)

When the drain voltage of a short-channel MOS increases from the linear region toward the saturation region, its threshold roll-off becomes larger. In a MOS, when the gate voltage is below V_T, the substrate forms a potential barrier between source and drain and limits the electron flow from one to another. For a device operated in the saturation region, the depletion-layer width of the drain junction is significantly wider than that of the source junction.

In long-channel devices, increase in drain voltage results in wider depletion-layer region around the drain junction which extends further into channel, however, it will not affect

the potential barrier height. Nevertheless, when the channel length is short enough, the increase in drain voltage decreases the potential barrier height. This is ascribes to the field penetration at the source region from the drain to the source when they are too close. Such a barrier-lowering effect leads to a substantial increase in electron injection from the source to the drain. As a result, when V_{DS} increases, subthreshold current increases. The threshold voltage, thus, decreases further with increasing drain bias in short-channel devices. Figure A-11 illustrates the dependence of the threshold voltage on the drain voltage for short-channel devices.

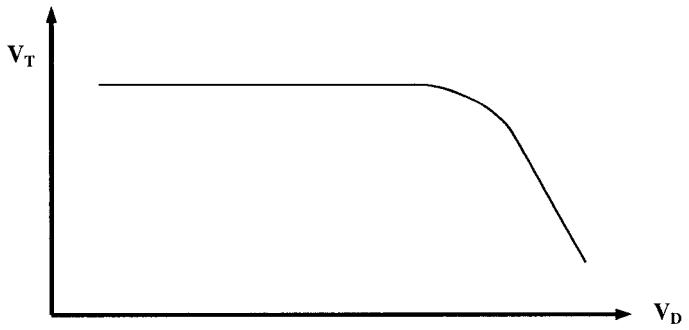


Figure A-11: Threshold dependence on drain voltage

Furthermore, DIBL causes the formation of a leakage path at the SiO2-Si interface [177]. In order to reduce the DIBL effect, we may either reduce source/drain junction depth which results in shallow junctions, or reduce gate oxide thickness to increase gate control over the depletion-layer charge or, increase the channel doping because the depletion-layer depth (W_m) is in reverse proportion to the substrate doping concentration, N_A. Moreover, new sub-micron technologies recently benefit an approach so-called as using Lightly Doped Drain (LDD), that is, low-doped regions are diffused in the neighborhood

of the diffusion regions of drain and source which causes the electric field to be spread and reduced at the drain pinch-off region and thus, reduced DIBL effect. Figure A-12 shows an schematic of LDD approach in short-channel devices. Reducing LDD junction depths will improve device short channel characteristics by reducing the amount of channel charge controlled by the drain. However, shallow junctions lead to a high external resistance [183].

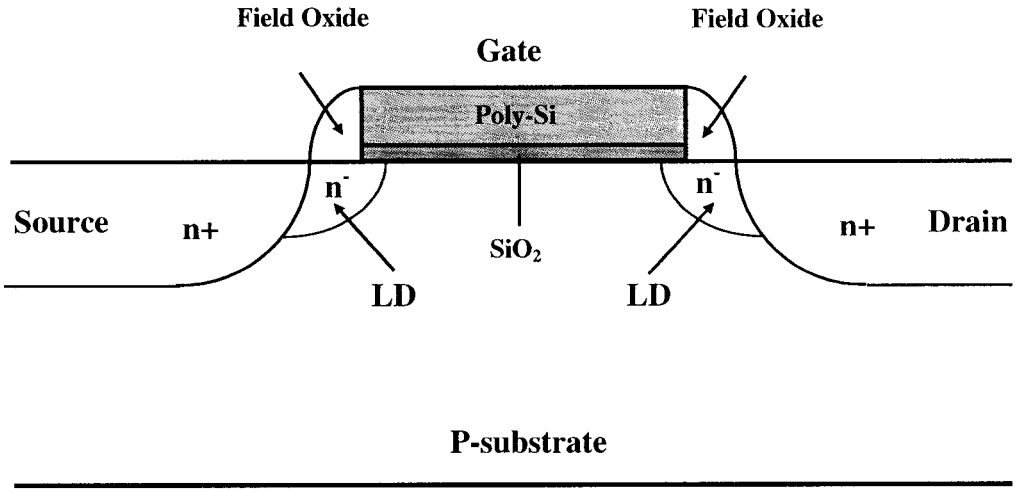


Figure A-12: Cross-section of Lightly Doped Drain profile

A.5 Output Impedance

As per definition, the output impedance (r_{ds}) for a MOS device is defined as per following:

$$r_{ds} = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}=const} \tag{A-13}$$

In saturation region, where $V_{DS} > V_{DSsat}$, the output impedance could be approximated by the slope of the MOS transfer function, that is I_{DS} versus V_{DS}.

$$r_{ds} \approx \frac{1}{\lambda I_D} \tag{A-14}$$

The ideal MOS assumes perfectly saturated current, that is horizontal I_DS versus V_{DS} which means Infinitely large output resistance. However, real MOS exhibits finite output resistance. For short-channel devices, there are at lease two effects that cause an increase of the drain current in the saturation region: (1) channel length modulation and (2) drain-induced-barrier lowering. In the saturation, the voltage drop across the channel remains approximately constant (V_{DSsat}), Therefore, increase in drain current represents lower output resistance.

A.6 Gate Oxide Dielectric

In order to keep short-channel effect under control and to maintain a good subthreshold turn-off, gate oxide thickness is reduced nearly in proportion to channel length. As the thickness of the dielectric material decreases, direct tunneling of carriers through the potential barrier can occur which leads to a gate leakage current that increases exponentially as the oxide thickness is scaled down. The gate leakage current has an effect on the chip standby power. Another issue with the thin gate oxide is the loss of inversion charge, and therefore transconductance, due to inversion layer quantization and polysilicon-gate depletion effects [21].

The exponential increasing behavior of gate leakage current may be concerned with

reliability issues due to greatly increased electron fluence passing through gate oxide over the lifetime of the device. However, as the power supply voltage is reduced to about 1 V, the electrons traversing the gate dielectric may no longer be considered "hot" and the rate at which these "cooler" electrons cause damage in these devices is greatly reduced [54]. There have been many publications that have demonstrated, both from a theoretical perspective as well as from measured results, that as the dielectric is thinned for a given applied bias, the charge required for dielectric breakdown increases rapidly [154].

Alternative high dielectric constant materials, rather than SiO_2 and nitrided SiO_2, will be the key to continued MOSFET scaling past 0.1μm gate dimensions. With the materials such as Si_3N_4, nitride, Ta_2O_5, TiO_2, BST, thicker dielectric layers can be used yet the same inversion layer characteristics can be maintained. These thicker layers result in less carrier tunneling, and they permit further scaling of the effective oxide thickness [183].

A.7 Random Dopant Distribution

One of the potentially significant sources of variation in MOSFETs at the limits of scaling is randomness in the exact location of dopant atoms. Although the average concentration of doping is quite well controlled by ion implantation and annealing processes, the doping distribution in channel remains random [63]. Such fluctuations cause have non-negligible effects on device threshold voltages [79] and also affects the terminal currents of the device [207]. Using new doping profile such as extreme retrograde profile, eliminates this effect.

A.8 Interconnection delays

If the performance of circuits is to keep pace with the speed improvement of devices, special attention has to be paid to interconnections. This is because the delay stemming from wire resistance and capacitances, has to be included with other delay components. High-performance circuits generally require two kinds of "short" and "long" wires. The former is to serve vast majority of interconnects with up to 1–2 mm in length, responsible for making the chip capable of wiring. The later, run between distant parts of the chip, and their characteristic length is that of a chip-edge. A good scaling gauge for such "long" wires is that the time of signal propagation on them should be only a small fraction of the cycle-time. From such considerations, it immediately follows that the cross section of these wires and insulators cannot have minimum lithography features. Therefore, there will be an extra need for a new type of wires , so called, fat wires [1,149].

Appendix B

Hot-Carriers: Mechanisms, Models and Degradations

Scaling down of MOS increases the lateral field in the channel, which has proved a greater reliability problem than the normal field increase. The increased lateral electric field is responsible for injection of so-called hot carriers into the oxide. The hot carriers are electrons and holes in the channel accelerated by the lateral field to the extent of that they have kinetic energies much larger than the thermal kinetic energy.

The accelerated tests for detection of hot-carrier-induced degradation are generally based on increased bias voltage, which consequently increases the lateral field in the MOS channel and the substrate current [56]. Here we address major mechanism responsible for hot-carrier injection and represent relative models. The appendix ends up with explanation of device and circuit degradation due this phenomena.

B.1 Hot-Carrier Injection Mechanisms

Due to the pinch-off condition, the electric field peaks in the vicinity of the substrate-drain junction at the Si–SiO_2 interface. Figure B-1 shows the formation of depletion regions near the drain edge for $V_G = 0$ and $V_D > 0$. If, depending mostly on drain bias, the lateral electric field is sufficiently high, strong carrier heating occurs and the average electron energy rises considerably above the thermal energy of the lattice.

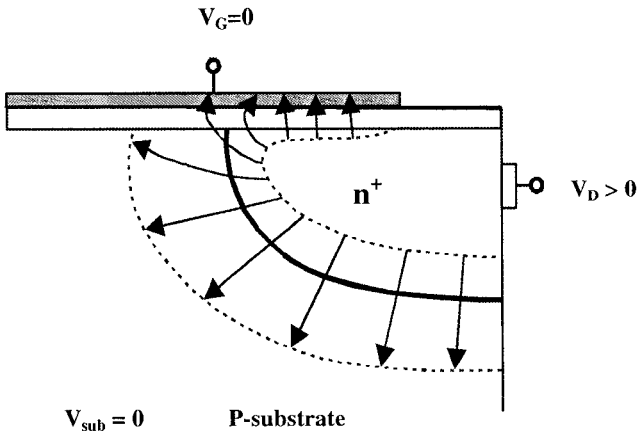


Figure B-1: The electric field in vicinity of Drain

Figure B-2 shows the barrier heights for injection of electrons and holes from Si to SiO_2.

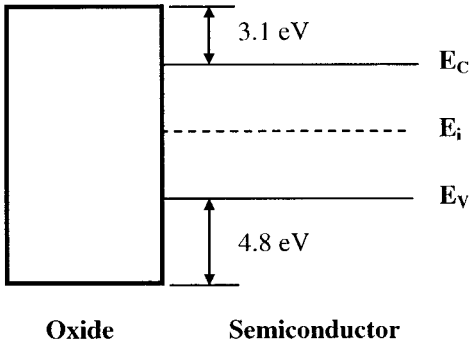


Figure B-2: The energy Diagram showing barrier heights

Electrons with a sufficient energy, exceeding a threshold of about 1.6 eV (1.5 times the Si bandgap), can create an electron–hole pair in the silicon by primary impact ionization leading to an avalanche effect [42,100]. This resulting mechanism is known as drain avalanche hot carrier (DAHC) injection [125,178]. The exact barrier is strongly dependent on the vertical electric field and therefore determined by the gate bias. The electrons (channel minority carriers) with a still higher energy can be injected from

channel into the gate oxide (process 1). This mechanism is known as channel hot-electron (CHE) injection [127]. The threshold energy of this process is, to a first order, the Si–SiO_2 conduction band offset of 3.1 eV [51,176]. They can cause gate current to flow or even worse, trapping of some of this charge can change V_T permanently. The electrons with less energy could be collected by the drain. Furthermore, the holes (channel majority carriers) generated by initial impact ionization process join the substrate and constitute a measurable substrate current (process 3). This current is thus a consequence of the primary impact ionization mechanism. The gate current is the only experimentally accessible quantity that represents a direct measure for the injection of carriers into the oxide. However, it consists of those carriers that traverse the oxide, i.e., only a fraction of all injected carriers excluding the ones whom were trapped out there.

Moreover, under a strong electric field, the majority channel carriers (holes) can ionize again the atoms of the substrate and generate new electron-hole pairs (process 4). This ionization is called as secondarily generated hot-electron (SGHE) injection [51,125,127,189] due to generating minority carriers (electrons). Furthermore, substrate hot-electron (SHE) [128] injection due to thermally and/or radiatively generated electrons in the substrate high-field region is pronounced.

The electrons, are then accelerated towards the gate by the vertical field of the gate-induced-depletion zone and may acquire enough energy to be injected into the gate (process 5). This injection gives rise to a gate current. The holes produced by avalanching

drift into the substrate and are collected by the substrate contact causes extra substrate current. This accumulative substrate current can produce a voltage drop across non-ideal substrate resistance (process 6) which can forward bias the substrate-source junction, causing electrons to be injected from source into substrate (process 7). Some of the injected electrons are collected by the reversed biased drain and cause a parasitic lateral bipolar action (process 8) which is entirely controlled by the drain voltage and not the gate voltage [2,14,129,182]. The avalanche behavior of impact ionizations (primary and secondary) would last in device failure. Figure B-3 introduces a visual scheme of hot carrier mechanism in NMOS.

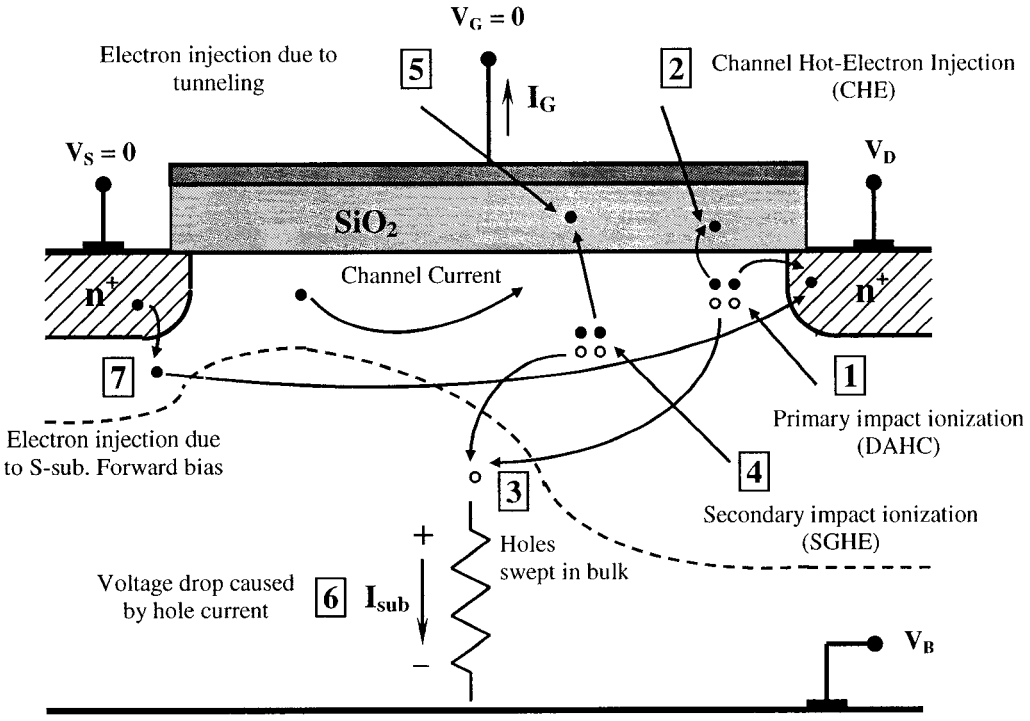


Figure B-3: Visualization of carrier multiplication in NMOS [139]

Figure B-4 shows the qualitative nature of electron and hole injection current as well as gate current for a NMOS.

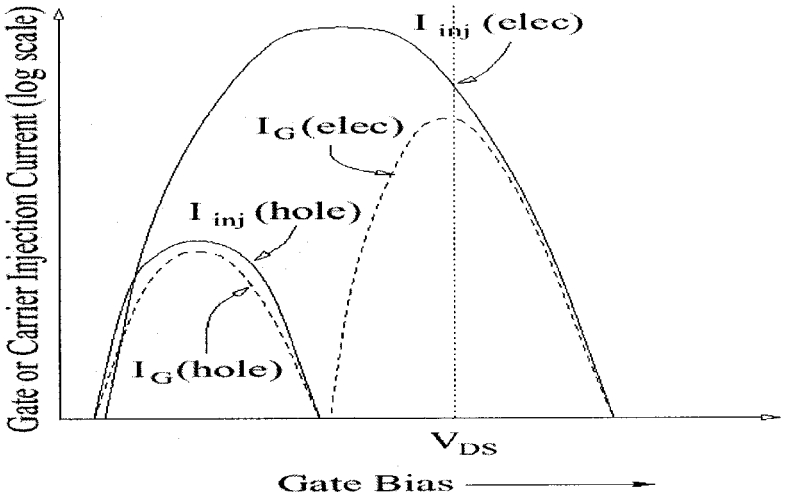


Figure B-4: Quantitative comparison between HCI mechanisms in NMOS

In complete analogy to electron injection, holes can be injected when, to a first order, the energy of the holes exceeds 4.8 eV, which is the Si–SiO_2 valence band offset. In the Si-MOS system, therefore, the barrier height for the injection of holes is much larger than that for the injection of electrons. It is thus anticipated that hole injection will, in general, be less efficient than electron injection.

Hot-carrier reliability and failure criteria have customarily been defined at the transistor level, as a 10% change in linear drain current, saturation drain current, or transconductance. However, a 10% degradation in one of above circuit parameters, so-called lifetime, does not necessarily correspond to the same degradation in circuit

performance because either degradation in an individual device may not affect circuit performance if the device does not lie in a critical path or, could be compensated by complementary characteristics of the different device types.

B.2 MOS Degradation Models

In MOS, the high lateral electric field is the main driving force underlying all hot-carrier injection mechanisms. The peak lateral electric field is a function of the applied gate and drain voltages as well as MOS parameters such as oxide thickness (t_{ox}), junction depth (x_j), and effective channel length (L_{eff}). The peak lateral electric field (E_m) can be expressed as below [83].

$$E_m = \frac{V_D - V_{Dsat}}{l} \tag{B-1}$$

where l is the effective lateral electric field length and must be empirically determined due to its dependence on t_{OX}, x_j and L_{eff}. Since it is difficult to determine electric field and electron temperature directly, substrate and gate currents are typically monitored. Substrate and gate currents both depend on E_m according to the "lucky electron" Model [180].

$$I_{sub} = I_D \exp\left(-\frac{\phi_I}{\lambda E_m}\right) \tag{B-2}$$

$$I_G = I_D \exp\left(-\frac{\phi_B}{\lambda E_m}\right) \tag{B-3}$$

where the exponential term describes the probability with which a carrier, while traversing a mean free path, λ, in an electric field E_m, gains a critical energy of $q\Phi_B$ to

overcome the SiO_2-Si barrier. Figure B-5 illustrates the fresh and degraded I-V characteristics for different MOS types.

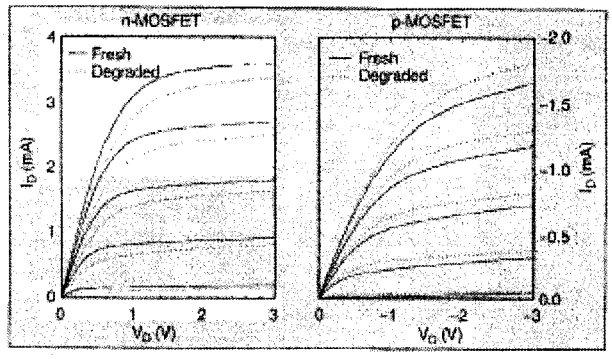


Figure B-5: I-V characteristics for fresh and degraded MOS

B.3 Hot Carrier Degradation

The hot carrier degradation mechanisms under static conditions have been extensively studied and there exists more or less a consensus on a consistent picture of the degradation mechanisms for both n-type and p-type MOS [77,78,206]. Indeed, under stressing conditions, the peak field and injection current are localized at pinch-off region near to the drain side of the channel, and so the degradation is asymmetric. The injected hot holes and electrons can cause oxide and interface damage by: (1) creating traps in the oxide, (2) being trapped in the oxide, (3) creating interface states at the interface and, (4) being trapped by interface states.

The injection of hot carriers into the oxide leads to a gradual degradation of the transistor characteristics. At the transistor level, manifestation of oxide and/or interface damage can often be observed as a shift in threshold voltage, transconductance, threshold slope and,

drive currents of the MOS depending on the exact stressing conditions [70]. Excess substrate current can overload on-chip substrate bias generators and establish a drastically increased bulk potential across its parasitic series resistance, resulting in forward bias of certain p-n junctions [96]. This can lead to threshold voltage reduction or even more serious effect like latch-up. It is recently reported that hot carrier degradation may cause serious problem in ESD protection point of view [71]. The hot carrier degradation in NMOS and PMOS are of different mechanisms. The hot-carrier degradation mechanisms for NMOS and PMOS are somehow different which will be addressed separately.

B.3.1 NMOS Degradation Model

In a NMOS, depending on stress voltages, different hot-carrier-induced (HCI) degradation mechanisms can occur. At low V_G stress, the direction of the electric field is from drain to gate, favoring the injection of the holes into the oxide near the drain. The resulting current is increasing due to the efficient hole trapping in the oxide and at the SiO_2-Si interface leading to a channel-shortening effect [73]. For this conditions, interface traps and neutral electron traps are created as well, but their influence on the current is masked by the trapped holes. Their influence might become visible, however, after neutralization of these holes, and filling of the neutral traps. For high V_G stress, the reverse is true, that is, the direction of the electric field is from gate to drain, favoring the injection of electrons, resulting in electron trapping and mobility degradation.

For NMOSs, interface state generation has been found to dominate under most biasing conditions and has the most influence on I-V degradation. Moreover, threshold voltage typically increases due to predominant electron trapping, and this increase coupled with mobility decrease results in a smaller drain current. Increase in interface trap density and change in carrier mobility and transconductance were also established [28,83,179] and correlates well with I_{sub}.

B.3.2 PMOS Degradation Model

It had long been believed that hot-carrier reliability of PMOS is not as serious an issue as hot-carrier reliability of NMOS. This was justified by the fact that the mean free path of holes in silicon is about one half that of the electrons, therefore, holes scatter more frequently and fewer of them reach high enough energies (about 4 eV) to reach interface states. However, as the transistor channel length has been scaled down into the deep sub-micron regime, hot carrier induced degradation of PMOS has been approaching that of NMOS [140,193].

Similar to NMOS, all three degradation mechanisms including hole trapping, electron trapping, and interface state generation, are possible in PMOS. For low $|V_G|$ stress, the direction of the electric field is from gate to drain, favoring the injection of electrons into the oxide. For high $|V_G|$ stress, the direction of the electric field is from drain to gate, favoring the injection of holes. However, the SiO_2-Si barrier for hole injection is 4.7 eV,

compared with 3.1 eV for the electron [127]. Thus for the same electric field magnitude, the number of holes injected is much less than electrons. For this reason, for all $|V_G|$, hot-electron degradation in PMOS correlates better with electron gate current rather than I_{sub} [83,134].

It has been established that for PMOS, I-V degradation is mainly due to electron trapping. The resulting negative charge trapped in the oxide near the drain affects the device through decrease in both $|V_T|$ and effective channel length. The presence of negative charge in the oxide enhances the electric field, thus reduces the gate voltage necessary to invert the channel. This shift in V_T turns the channel on at a lower $|V_G|$, causing the drain current to increase despite decrease in mobility. Lower V_T also cause extending the drain into the channel, causing a reduction in the effective channel length [171].This leads to an increase in the off-state leakage current, which is the main degradation problem for PMOS.

The change of the drain current in PMOS is analogous to the hole trapping case in NMOS. Electron injection and trapping increases the (absolute value of the) drain current by channel shortening and masks any effect of the generated interface traps. However, this electron trapping occurs for almost all stress gate voltages, because the electrons are becoming hotter than holes in the same electrical field and because the energy barrier for injection of electrons is smaller than for holes, which leads to efficient electron injection

over the complete gate voltage range.

B.4 Improving Hot Carrier Effects

From MOS principal equations, it is cleared that the depth of depletion region in a junction is in reverse proportion to the doping concentration of the regions. Using doping engineering-based approaches such as Lightly Doped Drain (LDD) [132] and Graded Channel (GC) [110] has resulted in significant improvements The cross section of a NMOS device using LDD approach, also called as shallow junctions, is illustrated in Figure B-6 where a lowly doped region of the drain is fully overlapped by the gate. A detailed 2D analysis shows that the optimal structure has the LDD entirely under the gate.

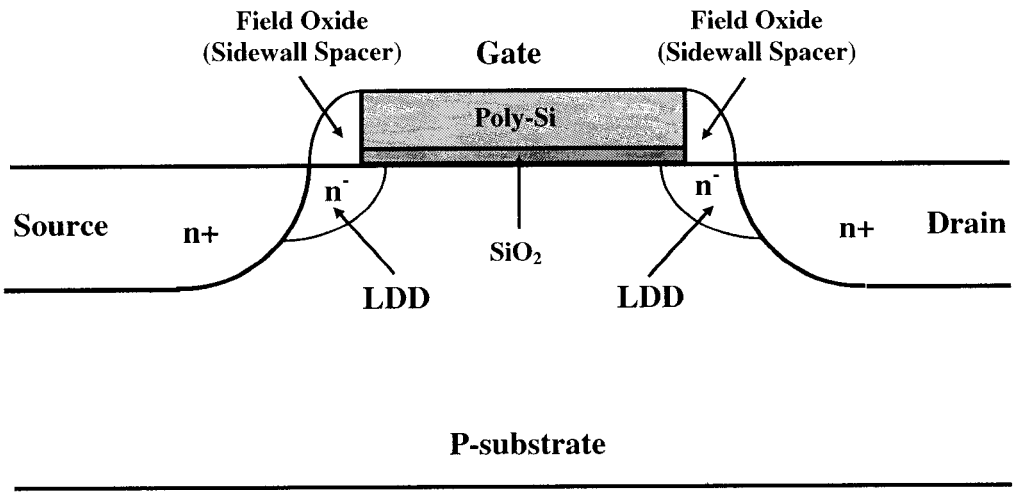


Figure B-6: The LDD structure cross section

It is shown that the incorporation of either LDD or graded junctions in a process, effectively reduces the electric field peak at the drain while maintaining a high supply

voltage [6,82,85,89]. Figure B-7 shows the scheme of electric field distribution for a conventional and drain-engineered (LDD) structures.

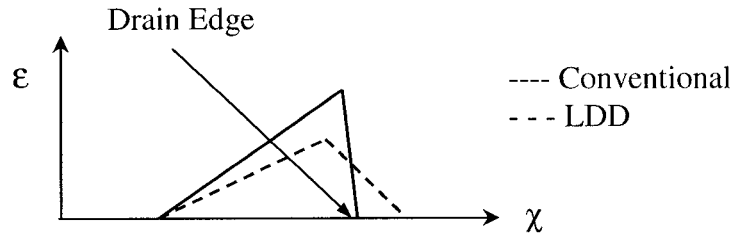


Figure B-7: Electric field distribution in conventional and LDD structures

Here, for the same V_{DD} , the area under the electric field curves is the same. However, the LDD structure spreads the high field over a larger region (into the drain). Reducing the peak field leads to a reduction of both avalanche multiplication and tunneling into the oxide, which reduces the number of generated hot carriers. But using N^- regions, represents higher resistance resulting higher static power consumption and lower drain current [31,59].

B.5 Hot-Carrier impact on circuit

Unlike other failure mechanisms such as electrostatic discharge, and gate oxide hard breakdown, failure due to hot-carrier degradation can be appropriately described as gradual rather than catastrophic. The gradual nature of hot-carrier degradation makes it difficult to detect and analyze the failure in an integrated circuit environment. To quantify hot-carrier degradation in a circuit environment, a simple approach would be to set a

threshold limit for all device parameters variations, and to declare failure if the variation of any of device parameter exceeds the set threshold limit.

The effect of hot-electron degradation on MOS operating in digital circuits and memory cell applications has been extensively examined [150]. Generally, digital circuits take benefit of complementary direction of degradation in NMOS and PMOS devices and are more robust to hot-carrier degradation than analog circuits. Analog circuits, which are sensitive to device parameter variation, are expected to be strongly affected by hot-carrier degradation. However, MOS-based circuits performing analog functions has been subject of limited study mostly focused on design methods to bypass the problem at the expense of additional circuit area and complexity [98]. Recently, the effect of hot carriers on some characteristics of analog circuitries has been reported which shows changes in output resistance, device mismatching and flicker noise [40].

Appendix C

Oxide Breakdown: Mechanisms and models

The exact mechanism of Time-Dependent Dielectric Breakdown (TDDB) is still not fully understood and is a subject of controversy. Most of the breakdown models are based on charge trapping/generation mechanisms that occur at high-stress electric fields where Fowler–Nordheim injection is the dominate mechanism of electron injection into the oxide [170]. They do not address breakdown that would occur during normal use electric fields where there would be little or no charge trapping in the oxide. Although a reasonable consensus has been reached on the breakdown mechanism, accurate time-to-breakdown extrapolations in a wide voltage range remain a subject of discussion. By scaling the oxide thickness to only a few nanometers (<5 nm), further complications have come about as different breakdown modes, "soft" and "hard" breakdown, are observed.

The dielectric breakdown of thin SiO_2 films is now believed to take place in two sequential phases [66,123]. During the first one, the oxide is slowly degraded due to the continuous charge build up resulting from the charge injection (electrons and/or holes) as the dielectric is subjected to an electric field. Since the dielectric is not ideal, the charge transport across the insulator is possible by ohmic conduction, hopping or Poole-Frenkel processes or by field emission (e.g., direct tunneling, Fowler-Nordheim or thermionic emission,...) [66]. This initial degradation stage, so called as Soft Breakdown (SBD) or "Quasi-Breakdown", can last long time and its duration strongly depends on the

magnitude of the applied electric field. The second one is a very fast current runaway locally triggered by the defects generated during the degradation phase. The nature of this second process, named as Hard Breakdown (HBD), is not well known yet, but several trap-related mechanisms such as trap-assisted tunneling [108], or resonant tunneling [146] have already been suggested [121,153].

Both mechanisms correspond to an extremely local failure which is detected as a significant sudden increase of the leakage current through the oxide [173]. The current after SBD (≈1 μA)is orders of magnitude smaller than that measured after HDB (≈ 1 mA). Moreover, the shape of the post-breakdown current-voltage (*I*–V) characteristic are also different: exponential ($I=Aexp(BV)$ or potential ($I=AV^B$) after SBD [116], and roughly linear (I=GV) after HBD [174], where A, B and G are the constants. However, in spite of these remarkable differences, SBD and HBD events are usually treated on equal grounds for reliability projections [162], i.e., these events are considered as corresponding to the same type of failure in the sense of having a common origin.

In other words, both breakdown modes are related to the generation of the same kind of defects during stress and they are locally triggered by the same effect which is the opening of a defect-related conduction path between the electrodes [173]. The differences between the post-breakdown conduction properties are due to the details of the microscopic configuration of the breakdown path which in turn depend on the final breakdown current runaway. Once the percolation path is completed, the power

dissipation through it controls the second stage of the breakdown transient (characterized by sub-microsecond time-constants, segment I-II or segment I-III, see Figure C-1) which determines the post-breakdown conduction property of the oxide.

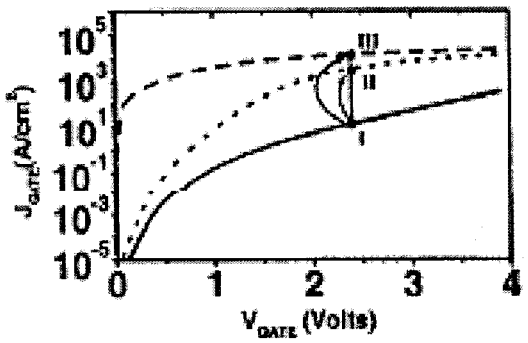


Figure C-1: Plot of I-V characteristics for soft and hard breakdowns (short dashed line for soft and long dashed line for hard breakdowns)

One interesting feature associated with this SBD mode is that the device switching behavior may be retained even after its occurrence, in strong contrast to the case of conventional hard breakdown (HBD) [202]. In addition, impacts of SBD on device characteristics also depend on the BD location. It is found that BD location plays an important role in affecting the switching function of the device.

Most of BD events would be induced in the source/drain overlapped region for deep sub-micron devices [212], where the resistance of the electrodes is low, the power dissipation at the moment of breakdown is high, and sufficient wear out of the breakdown path occurs, resulting in hard breakdown exclusively [8]. In the channel part, the resistance of the discharge path is higher and more soft breakdown is triggered. Here, the subthreshold and on-state characteristics of the drain current are not significantly affected. In contrast,

however, BD at the drain implies significant leakage form the gate which would destroy the normal operation of the device by increasing dramatically the off-state (leakage) drain current [212]. Depending on the stress conditions, oxide thickness and structure area, several SBD events may appear prior to the final HBD [192].

Although it has already been demonstrated that HBD causes the device failure, it is not clear yet whether the current leakage after SBD has to be considered as a transistor failure or not [173]. Even if SBD and HBD share the same physical origin, if devices were able to tolerate the leakage current after SBD, this would mean that HBD is a failure and SBD is not. It was a common belief that breakdown coincides with circuit failure [212], but recent studies illustrate that even after several hard breakdowns, certain digital circuits can remain functional [45,93] and therefore, even hard breakdown does not necessarily correspond to circuit failure. Furthermore, it is now commonly reported in the literature that for oxide thickness below 25 A° the BD failure event is no longer hard [107,119,169].

Recently, it has been demonstrated that the differences in alignment of the oxide traps that make up the percolation path generate a broad distribution of path conductivity [9,45]. Possibly, low conductivity paths are difficult to transform into hard breakdown, while high conductivity paths become hard breakdowns. This might explain why at places where the electrical environment is identical, we can still find both hard and soft breakdown modes. A typical oxide reliability specification requires that less than a small

fraction of failures (e.g., 0.01%) must be guaranteed on the total gate-oxide area on chip (e.g., 0.1 cm) for a predetermined period (e.g., ten years) [45].

C.1 Main Breakdown parameters

The main parameters which define the quality of a dielectric for the viewpoint of breakdown are the time-to-breakdown, the injected charge-to-breakdown, the current or voltage to breakdown, the breakdown electric field , as well as the oxide charge-to-breakdown or the hole fluence to breakdown [66]. The time to breakdown is defined as the time necessary to reach breakdown when a constraint is applied to the structure. The injected charge to breakdown corresponds to the cumulative fluence sustained by the oxide up to breakdown.

The current or voltage to breakdown are defined by the current or voltage measured just at the breakdown point (or more rigorously at the step just before breakdown), while a voltage or current stress is applied as a function of time. The breakdown electric field is thus defined as the effective electric field deduced from dividing the voltage to breakdown by oxide thickness. It should be noted that such a definition of the breakdown electric field is not very accurate, since it is subjected to the wear out kinetics which governs the oxide degradation prior to breakdown. It can be regarded as a gross parameter which gives an estimation of the maximum electric field that can sustain the dielectric, regardless of the constraint duration.

C.2 Breakdown Models

In the wear out model, defects in the oxide network are created during electrical stress of the oxide film [9]. These defects may or may not carry charge, and are called neutral traps. The term neutral trap does not mean that the traps have to be neutral. It is used to signify that the traps that lead to breakdown are not necessarily associated with positive or negative charge. The neutral traps can capture a hole to become positively charged or capture an electron to become negatively charged. When the density of these neutral traps reaches a critical value, a conduction path that links the cathode and anode may form which triggers a breakdown. Despite the huge amount of work done by many groups, both theoretical and experimental, the structure of the neutral trap that leads to oxide breakdown is still under debate. Consequently, the link between trap buildup and breakdown is based on empirical results. Not all the empirical results are consistent with each other. Here we address the major models for oxide breakdown. Several models have been advanced as breakdown mechanisms [210]. In the framework of these models, the release of species, either holes or hydrogen, has been related to defect generation which eventually leads to the breakdown.

C.2.1 Anode-Hole-Injection Model

In this model, which is the popular model for oxide breakdown, electrons are injected, by tunneling regime, from the cathode into the oxide where they gain energy from the applied field before entering the anode [29,153]. A fraction of the tunneling electrons reaching the anode are able to transfer their energy to an electron deep in the valence

band. This electron in promoted to the lowest available electron energy state, that is, the conduction band edge of the anode , thereby creating a hot hole. These hot holes are then assumed to tunnel back into oxide and be transported to the cathode where some of them are trapped in energetically deep oxide sited with the remainder, flowing out through the silicon substrate. The trapped holes charge increase with time until a critical hole fluence is reached, marking the breakdown event [50].

Recently, the important refinements for anode hole injection such as minority impact ionization have been advanced [7,201]. The improved anode hole injection model has been proposed to explain the high voltage effect and is able to explain the stress results observed either at high voltages (> 4V) or for thick oxides. This model predicts a 1/E dependence at much higher voltages and an approximate model or an exponential law for voltage dependence at low voltages (< 4V) [210].

C.2.2 Hydrogen Release Model

This model attributes the dominant role to hydrogen-related species [13,25,26,53]. It considers that the energy which is released by the electrons near the anode is used to free up processing-induced hydrogen. The liberated hydrogen is subsequently redistributed toward the oxide bulk and drifts toward the cathode where it generates several types of defects (positive charges, NTS, interface states) by chemical reaction with some unspecified precursor sites [13].

C.2.3 Electrochemical Model

This model, also called as "E" model, assumes oxide aging and breakdown is a thermodynamic process, possibly caused by molecular dipole interaction with the applied electrical and thermal stress [30,101]. It predicts that the logarithm of the median-time-to-fail, is linearly dependent on electric field.

C.2.4 Impact Ionization Model

It is shown that the gate field after breakdown can penetrate into the substrate [217]. This electric field can heat electrons in the space charge region which gives ride to an impact ionization process in the substrate. Generated holes during this process can also contribute to the total substrate hole current. After oxide breakdown, the substrate current can be due to the impact ionization in the substrate, tunneling through the leakage path or the sum of both components. However, the measurement proves that the hole current after breakdown is due to electron impact ionization in the substrate [145].

C.2.5 Percolation Model

The basic idea is that traps are created at random locations in the oxide during electrical stress. Each trap has an effective sphere of influence. When two spheres touch or overlap, they are considered linked together and conduction between the two traps is possible. When there is a continuous chain of linked sphere connecting one of the electrode to another, a breakdown path is formed. Naturally, the probability of forming such a path increases with trap density [33,44]. Recently, the percolation approach was also reported

with various schemes to investigate the thickness dependence of critical defect density and of Weibull slopes and suggests that, when oxide thickness approaches the size of the defects, one defect is sufficient to create breakdown [210,161].

C.3 Breakdown voltage Calculation

Based on constant voltage tests on small-area oxides (area < 400μm^2), the time-to-breakdown has been shown to follow the reciprocal field dependence [117]:

$$t_{bd}(T) = \tau_0(T) \cdot \exp\left(G(T) \cdot \frac{t_{ox}}{V_{ox}} \right) \qquad \text{(C-1)}$$

where t_{ox} is the gate-oxide thickness, V_{ox} is the voltage across the oxide, G(T) and τ_0(T) are temperature dependent parameters which are respectively 10^{-11} s and 350 MV/cm for T=300 °K.

C.4 Effects of temperature, drain current and area on TDDB

It is shown that a large source-drain current caused by punch-through greatly accelerates the gate-oxide breakdown [130]. At a drain voltage above punch-through voltage, a drain current of a few tens of milliamperes flows through he channel due to punch-through event, and a large number of holes is generated due to impact ionization. The generation of a large number of holes has been confirmed by the substrate current measurement. Some of these holes are injected into the gate oxide during stressing. When a sufficient number of holes is trapped in the oxide, the gate current increases due to the attractive field, and eventually breakdown occurs.

Temperature dependence of TDDB is one of the important parameters in predicting oxide reliability. A very strong temperature dependence for time-to-breakdown and charge-to-breakdown has been found for thin oxides as compared to thick oxides [22,141,169]. This is because for both extrinsic and intrinsic breakdowns, at temperatures from 25 °C to 125 °C the activation energy is lower than that at temperatures from 125 °C to 250 °C and the difference of activation energy in the extrinsic for the said interval is larger than that in the intrinsic. This observation indicated that the mechanism of oxide breakdown changes at temperatures around 125 °C [157]. In addition, a non-Arrhenius temperature dependence of oxide breakdown is applicable for ultra-thin oxides [55,169].

As the time-to-breakdown is a statistically distributed parameter, it has large area dependence both in the intrinsic as well as extrinsic breakdown mode. Area dependence of the extrinsic breakdown mode is larger than that of the intrinsic breakdown mode [157].

One of the long-standing debates in the area of oxide reliability is the controversy involved in voltage (field) dependence of time-to-breakdown. Several reports on direct experimental results have been published showing that both charge-to-breakdown and time-to-breakdown data at low voltages deviate from the prediction of an exponential law at high voltages [163,211]. In particular, data generated at low voltages using long-term module stress deviate from the prediction of an exponential law from high voltage data. A refined simulation based on the originally proposed anode hole injection model

suggests the behavior at high voltages, but an approximately exponential law reemerges below 4V [6,201].