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POLYTECHNIQUE MONTRÉAL
affiliée à l'Université de Montréal

Systems and Topologies for Large-Scale Transmitter and Receiver Arrays for Integrated Wireless Communication and Sensing Applications

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Thèse présentée en vue de l'obtention du diplôme de *Philosophiæ Doctor*
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Cette thèse intitulée :

Systems and Topologies for Large-Scale Transmitter and Receiver Arrays for Integrated Wireless Communication and Sensing Applications

présentée par **Yasser BIGDELI**
en vue de l'obtention du diplôme de *Philosophiæ Doctor*
a été dûment acceptée par le jury d'examen constitué de :

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DEDICATION

To the weary who still climb Mount Doom.

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I would like to express my deepest gratitude to my supervisor, Professor Ke Wu, for his guidance, insightful advice, and unwavering support throughout the course of this research. His expertise and encouragement have been invaluable in shaping both this work and my growth as a researcher. I am also grateful to Dr. Pascal Burasa, for his assistance, thoughtful suggestions, and constant availability, which greatly contributed to the progress of this study. Sincere thanks to the PolyGrames research center technicians for their valuable role in the fabrication and assembly of the prototypes, and for their support during measurements. Finally, I wish to thank my family, and especially my wife, for their patience, encouragement, and unwavering support. Their love and understanding have been a constant source of motivation and strength.

RÉSUMÉ

Cette thèse de doctorat, *"Systèmes et topologies pour des réseaux émetteurs et récepteurs à grande échelle pour les applications intégrées de communication et de détection sans fil"*, traite des principaux défis des technologies sans fil modernes. Alors que les systèmes 5G et émergents 6G s'appuient sur de grands réseaux pour offrir des débits élevés, une couverture étendue et une intégration multifonctionnelle, leur mise en œuvre pratique est limitée par l'inefficacité, la consommation énergétique élevée et la complexité des circuits, en particulier aux fréquences millimétriques et sub-THz. Cette recherche propose des solutions au niveau des composants et des topologies, conciliant compacité, efficacité énergétique et polyvalence, et aboutit à des conceptions adaptées aux infrastructures sans fil du futur.

Pour les grands réseaux récepteurs, deux solutions complémentaires ont été développées. Premièrement, les réseaux de mélangeurs auto-oscillants (SOM) avec topologies en quadrature permettent une réception en conversion directe complète tout en conservant faible consommation et compacité. L'extension à des réseaux d'oscillateurs couplés (COA) permet un fonctionnement indépendant des éléments, une activation reconfigurable et une rotation de phase contrôlable, offrant une flexibilité et une évolutivité inédites. Deuxièmement, les récepteurs interférométriques (IFRX) ont été améliorés pour réduire l'empreinte et augmenter la plage dynamique, permettant jusqu'à $1\,000\times$ de réduction de consommation énergétique tout en atteignant des performances comparables aux systèmes hétérodynes modernes. Ces deux approches constituent des réalisations inédites pour les grands réseaux.

Une technique innovante de formation de faisceau sans déphaseur a également été développée pour les grands réseaux à hautes fréquences millimétriques. En utilisant uniquement la rotation de polarité et des commutations à faible puissance, une formation de faisceau efficace est obtenue avec une consommation minimale, compatible avec les architectures SOM.

Côté émetteur, une conception de réseau distribué réduit la consommation énergétique en simplifiant la chaîne RF et en optimisant le fonctionnement de l'amplificateur, tout en assurant une sécurité intrinsèque au niveau physique. Cette approche, démontrée sur des prototypes basse fréquence, prépare le terrain pour des implémentations à l'échelle millimétrique.

Dans l'ensemble, cette thèse propose de nouveaux paradigmes pour des réseaux émetteurs et récepteurs à grande échelle, efficaces, compacts et multifonctionnels, avec des contributions reconnues par des publications scientifiques, des conférences et des brevets.

ABSTRACT

This doctoral thesis, titled *"Systems and Topologies for Large-Scale Transmitter and Receiver Arrays for Integrated Wireless Communication and Sensing Applications,"* investigates the key limitations that hinder the realization of large-scale arrays essential for future 5G/6G and future systems. While such arrays are set to promise high data rates, extended coverage, and integrated communication–sensing functionality, their implementation is challenged by excessive power consumption, circuit complexity, and limited scalability at millimeter-wave and sub-terahertz frequencies. The work addresses these challenges by introducing new system and topology solutions that enhance efficiency, compactness, and multifunctionality.

For receiver arrays, the thesis proposes two novel approaches. The first is based on quadrature self-oscillating mixer (SOM) arrays that merge mixing and oscillation in a single compact structure. New quadrature topologies enable direct-conversion reception with phase detection, while coupled-oscillator array (COA) configurations provide independent operation, reconfigurability, and controllable phase rotation, combining low power with high scalability. The second approach enhances interferometric receivers (IFRX) by employing nonlinear predistortion to reduce system footprint and boost dynamic range. This enables performance on par with contemporary heterodyne architectures, while consuming orders of magnitude less power.

A phase shifter-less beamforming technique is also introduced, eliminating one of the main sources of power loss in high-frequency arrays. Using low-power polarity rotation and switching at intermediate frequencies, efficient beamforming is achieved with minimal energy use and hardware overhead.

A distributed transmitter array architecture is proposed to significantly reduce power consumption and circuit complexity in large-scale wireless transmitters. By simplifying the RF chain and employing direct-RF QPSK modulation, the design eliminates the need for digital-to-analog conversion and complex baseband processing stages. This configuration enables power amplifiers to operate efficiently near their optimal power levels, while spatial signal combination preserves overall linearity and inherently enhances physical-layer security. The resulting architecture delivers a scalable, energy-efficient, and secure solution for next-generation millimeter-wave transmitter arrays.

Overall, the thesis delivers a unified framework for energy-efficient, compact, and scalable large-array transceiver architectures, paving the way for next-generation integrated wireless communication and sensing systems.

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LIST OF SYMBOLS AND ABBREVIATIONS

THz	Teraherz
mmWave	Millimeter Wave
TX	Transmitter
RX	Receiver
TRX	Transceiver
IFRX	Interferometric Receiver
SOM	Self-Oscillating Mixer
QHSOM	Quadrature Harmonic Self-Oscillating Mixer
COA	Coupled-Oscillator Array
TDD	Time Division Multiplexing
AoA	Angle of Arrival
ISAC	Integrated Sensing and Communication
Gbps	Giga Bit per Second
SoA	State of the Art
EIRP	Equivalent Isotropic Radiated Power
BIST	Built-In Self-Test
DAC	Digital-to-Analog Converter
IF	Intermediate Frequency
LO	Local Oscillator
PA	Power Amplifier
RF	Radio Frequency
QPSK	Quadrature Phase-Shift Keying
dB	Decibel
MIMO	Multiple-Input Multiple-Output
6G	Sixth-Generation Wireless Network
5G	Fifth-Generation Wireless Network
SNR	Signal-to-Noise Ratio
RFIC	Radio Frequency Integrated Circuit
PCB	Printed Circuit Board
EM	Electromagnetic
IM	Intermodulation

CHAPTER 1 INTRODUCTION

The evolution of wireless communication systems toward 5G, emerging 6G networks, and beyond is driving an increasing demand for high-performance, multifunctional, and energy-efficient radio architectures. At the core of this evolution are large-scale transmitter and receiver arrays, which enable high data rates, enhanced coverage, spatial multiplexing, and the convergence of communication and sensing functionalities. However, the practical deployment of such arrays remains challenging, particularly at millimeter-wave and sub-terahertz frequencies, where circuit complexity, high power consumption, and hardware inefficiencies can severely constrain system performance.

The motivation for this research stems from the growing gap between the theoretical potential of large-scale arrays and their practical realization. Although large arrays offer unprecedented gains in spectral efficiency and spatial processing, conventional implementations rely on bulky and power-hungry components, such as phase shifters, high-power local oscillators, and complex RF chains. These architectural constraints hinder compact integration, limit scalability, and degrade energy efficiency, underscoring the need for alternative array architectures that achieve a balanced trade-off between performance, efficiency, and multifunctionality.

This thesis addresses these challenges through a component- and topology-level investigation of large-scale array architectures, with contributions on both the receiver and transmitter sides.

On the receiver side, a revised coupled oscillator array (COA) architecture based on a quadrature harmonic self-oscillating mixer (QHSOM) is proposed. This approach introduces operational reconfigurability into COA systems through selective activation/deactivation and oscillation polarity rotation. By enabling phase information extraction within a direct-conversion receiver topology, the proposed QHSOM extends conventional self-oscillating mixers to support coherent communication applications. In parallel, interferometric receivers (IFRXs) are optimized for ultra-low-power operation and reduced physical footprint, addressing traditional limitations in dynamic range and scalability.

On the transmitter side, distributed array topologies are introduced to reduce energy consumption, simplify RF chains, and exploit spatial power combination. These architectures inherently support physical-layer security and offer a scalable solution for high-frequency transmitters suitable for future wireless systems.

In addition, a phase shifter-less analog beamforming technique is presented, enabling efficient

large array beamforming without the power and area overhead associated with conventional phase shifters. This technique relies on simple intermediate-frequency (IF) band switching functions, providing inherent frequency scalability. Importantly, its principle of operation is fully compatible with the proposed distributed transmitter architecture as well as the QHSOM-based COA receiver array.

By jointly addressing transmitter and receiver challenges, this thesis develops practical, energy-efficient, and compact solutions for multifunctional large-scale arrays. The proposed architectures bridge the gap between theoretical array performance and practical implementation, and establish a foundation for next-generation integrated wireless communication and sensing systems.

CHAPTER 2 LITERATURE REVIEW: ADVANCES IN LARGE-ARRAY FRONT-ENDS FOR MILLIMETER-WAVE AND TERAHERTZ COMMUNICATION AND SENSING SYSTEMS

abstract:

Large-scale antenna arrays have become central to modern wireless communication and sensing systems, especially as technologies advance into the millimeter-wave (mmWave) and terahertz (THz) frequency regimes. Comprising hundreds or even thousands of radiating elements, these arrays enable high beamforming gain, spatial multiplexing, and improved signal-to-noise ratio—capabilities essential for emerging applications such as 5G/6G communications, automotive radar, satellite communications (SATCOM), and high-resolution imaging. Despite their immense potential, the realization of large arrays poses critical challenges in hardware design, including integration complexity, calibration precision, power efficiency, and system scalability. Addressing these challenges calls for innovations in RF front-end architectures, packaging and interconnect technologies, and intelligent control algorithms. This paper presents a comprehensive review of large-array hardware, organized around integration levels, RF front-end design approaches, and application domains. We examine state-of-the-art architectures with a focus on RF efficiency, beamforming accuracy, and calibration techniques. Key enabling technologies—such as antenna-in-package (AiP) solutions, photonic integration, and metasurface-based implementations—are discussed in depth. In addition, we highlight software-driven aspects, including adaptive beamforming and resource management strategies. The paper also surveys recent demonstrators and practical systems from both academia and industry. Finally, we identify open challenges and outline promising research directions toward the realization of cognitive integrated sensing and communication (ISAC) hardware platforms.

2.1 Introduction

The increasing demand for high data rates, enhanced spatial resolution, and ubiquitous connectivity has catalyzed the exploration of millimeter-wave (mmWave, 30–300 GHz) and terahertz (THz, 0.1–10 THz) frequency bands for next-generation communication and sensing applications. As wireless communication systems continue to evolve—driven by the proliferation of cellular networks, Wi-Fi technologies, and non-terrestrial networks (NTN)—the currently allocated electromagnetic spectrum is becoming increasingly congested. To mitigate this limitation, the wireless industry has transitioned toward 5G and beyond, operating

across an expanded range of carrier frequencies from sub-6 GHz up to 86 GHz [17].

The 3rd Generation Partnership Project (3GPP) defines the 5G New Radio (5G NR) bands within the mmWave frequency range (FR2), spanning 24.25–52.6 GHz, as an extension of the sub-6 GHz frequency range (FR1) [18]. For instance, NR band n260, operating in time-division duplex (TDD) mode at 39 GHz, provides 3 GHz of spectrum (37–40 GHz) with a maximum channel bandwidth of 400 MHz, enabling multi-gigabit-per-second (Gb/s) data rates for user equipment. Looking beyond 5G, research efforts for 6G systems are directed toward exploiting carrier frequencies between 100 GHz and 300 GHz, in addition to maintaining lower frequency bands to ensure broader coverage and higher mobility support [18–20].

Non-Terrestrial Networks (NTN), encompassing satellite communications (SATCOM), are becoming a key component of the 6G ecosystem, supporting ubiquitous connectivity and service continuity across terrestrial and space segments. The recent allocation of K- and Ku-band spectrum enables higher-capacity satellite links and improved service scalability for broadband and mobility applications [4, 5, 8]. In parallel, future NTN architectures are expected to leverage mmWave and THz bands for inter-satellite system links (ISLs), supplemented by optical inter-satellite communication technologies. These developments aim to provide ultra-high throughput, reduced latency, and resilient space-based networking capabilities, forming a critical enabler of global 6G coverage [8].

These higher frequencies offer vast, underutilized spectrum resources and enable the integration of compact antenna arrays with many elements. This, in turn, supports massive spatial multiplexing, or massive MIMO, which has been considered as a viable feature of the upcoming 6G systems, allowing for numerous simultaneous and independent signal streams and beams, thereby significantly enhancing system capacity.

Fully digital beamforming architectures offer exceptional flexibility but are often constrained by their high power consumption. This limitation calls for energy-efficient design strategies that maintain performance under demanding operational conditions. In contrast, phased-array architectures are generally viewed as the most practical solution from both power consumption and implementation complexity perspectives. They provide an efficient approach for realizing large antenna arrays, particularly in the mmWave and THz frequency bands.

Phased-array beamforming is a key feature of 5G New Radio (NR) systems. By coherently combining signals from multiple antenna elements, these arrays generate narrow, steerable beams that not only mitigate propagation losses but also enable spatial multiplexing. This capability is fundamental for advanced applications such as 5G/6G communications, automotive radar, and satellite systems, where high gain and spatial resolution are critical (as illustrated in Figure 2.1). Moreover, in THz imaging, large phased arrays enhance the signal-

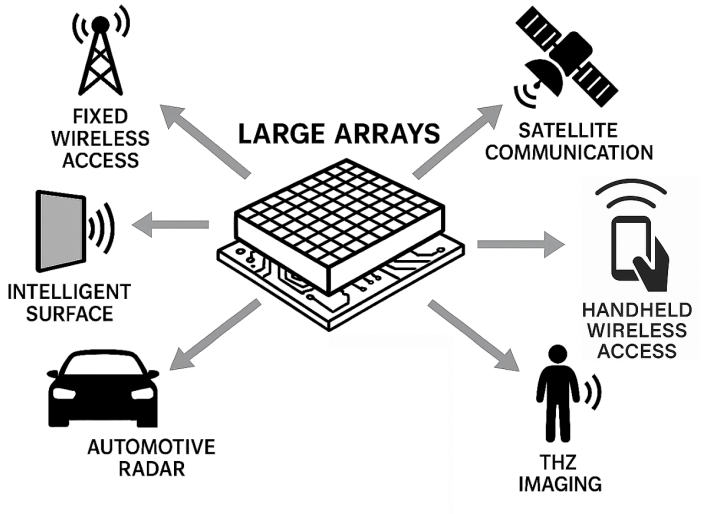


Figure 2.1 Applications of large arrays in integrated communication and sensing (ISAC) systems.

to-noise ratio, enabling higher-resolution and faster imaging. Similarly, ISAC systems, the deployment of numerous transceiver units facilitates multifunctional integration and intelligent resource allocation.

Interest in large-array systems is rapidly increasing, as evidenced by the growing number of publications over time, as shown in Figure 2.2. In the literature, arrays of around 64 elements are considered the onset of large–scale operation, where beamforming becomes effective for real-world communication and sensing. Beyond this threshold, conventional passive topologies are no longer sufficient, necessitating a transition to active array architectures that support scalability, functional integration, flexibility, and controlled power consumption. The academic and industrial interest in large-array hardware has significantly increased in recent years. Companies such as Qualcomm, Nokia, and others are investing heavily in developing phased-array transceivers for 5G base stations, while automotive manufacturers are integrating large arrays into advanced driver-assistance systems (ADAS). However, despite their promise, large-array systems present several formidable challenges that hinder practical deployment.

Maintaining signal coherency across a large number of antenna elements requires precise phase and amplitude control, which in turn demands complex calibration strategies. The sheer number of RF channels required further complicates packaging and integration matters; technologies such as antenna-on-chip (AoC), antenna-in-package (AiP), and tiled architectures each introduce trade-offs in terms of performance, cost, thermal management, and scalability.

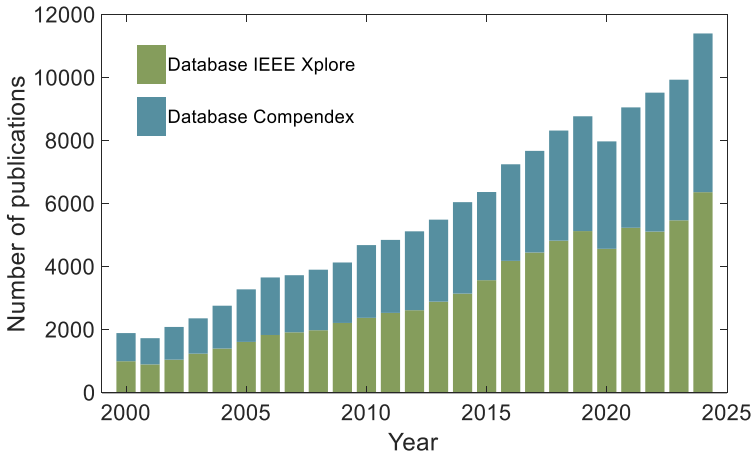


Figure 2.2 Number of publications on large arrays in the Compendex and IEEE Xplore databases steadily increased over the past decade.

This paper provides a structured and practical review of large-array hardware, emphasizing real-world constraints that affect system performance and deployment. The remainder of the paper is organized as follows. Section II introduces the key design and development principles for large-array systems. Section III reviews beamforming techniques, while Section IV discusses integration levels. Section V addresses physical implementation aspects, including packaging and signal distribution. Section VI examines active circuit topologies, followed by Section VII, which focuses on calibration methods. Section VIII explores local oscillator (LO) distribution and coherency. Section IX presents modern array architectures, and finally, Section X highlights the main challenges and outlines potential directions for future research.

2.2 Critical Thinking in Large Array Development

The design philosophy behind the development of large phased arrays in mmWave and THz systems is fundamentally application-driven. Rather than aiming for scale as an end in itself, designers pursue large array architectures as a solution to specific physical and system-level limitations imposed by high-frequency operation. Across the reviewed literature, this philosophy is shaped by the interplay between performance constraints, environmental demands, and system integration goals, with each application space—whether ground-based communication, sensing, or aerospace—driving its own reasoning for array enlargement and guiding the choice of architectural paths such as topology, modularity, or control scheme.

2.2.1 Application-Based Development

For 5G base station deployment, the emphasis is on achieving high EIRP, scalable integration, and manufacturability. Systems like those in [4, 5, 8] leverage stacked-patch antennas and tightly matched layouts to eliminate the need for calibration. In [4], for example, a 64-element array achieves up to 65.5 dBm EIRP through symmetric routing and flip-chip packaging, supported by a Wilkinson 1:64 feed network. In [5], layout symmetry and proportional to temperature (PTAT) biasing allow for calibration-free beamforming, enabling simplified production and field deployment. These systems typically adopt a tiled approach using 2×2 or 4×4 beamformer ICs to scale element counts, while maintaining compact RF and power routing.

In contrast, arrays targeting point-to-point backhaul or repeater links focus on link stability, fast beam switching, and over-the-air (OTA) performance. References [3, 21, 22] implement features like on-chip beam memory, digitally synthesized phase slopes, and dual-polarized beams to enable robust link coverage with minimal control latency. For instance, [21] introduces an architecture with over 30,000 pre-stored beams and sub-200 ns switching using digital beam calculators. Such designs trade off analog simplicity for digital flexibility, essential for urban 5G deployments with dynamic beam steering requirements.

Designs intended for SATCOM and aerospace applications emphasize long-term reliability, radiation hardness, geometrical compactness, and robust packaging. In [22], a 256-element Ka-band receiver integrates on-chip radiation sensors that monitor total ionizing dose (TID) exposure, feeding gain correction routines to mitigate performance degradation in orbital environments. In [23], a 256-element Ka-band receiver integrates on-chip radiation sensors that monitor TID exposure and feed gain correction routines, addressing performance degradation in orbital environments.

Reference [24] extends this robustness via distributed LO generation with synchronized on-chip PLLs and thermal-compensated DACs, ensuring phase coherence across 1024 elements without centralized distribution. These arrays typically adopt heterogeneous integration (e.g., AiP and interposers) and rely on embedded diagnostics to avoid frequent recalibration.

The developed experimental and testbed platforms like [14, 25] favor hardware flexibility and software-defined beamforming over static performance. For example, in [25] a chip-to-chip routing of LO and IF signals enable seamless vertical and horizontal expansion without centralized controllers. These systems are set to prioritize reconfigurability and prototyping agility, accepting higher insertion loss or reduced thermal efficiency in exchange for modularity.

Finally, radar, sensing, and passive front-end arrays like those in [9, 26, 27] are designed to focus on radiation performance, phase uniformity, and simulation fidelity. In [27], a multilayer Isola Tachyon 100G PCB is used to realize a 60–70 GHz stacked-patch array with stripline-microstrip transitions and bonded superstrates, achieving broad bandwidth and uniform gain. [28] takes a novel approach by implementing randomized array thinning, activating only a fraction of the array to lower cost and power while maintaining low sidelobe levels through OTA calibration. These systems reflect a philosophy of predictable EM behavior, often validated through full-wave simulation and anechoic chamber testing rather than digital correction.

2.2.2 Commercialization and Challenges

Commercialization brings additional constraints. For large arrays to be viable in cost-sensitive markets such as telecom and automotive, systems must be robust to fabrication imperfections and operate reliably across temperature and aging cycles. Architectures that rely heavily on calibration or hand-trimmed matching are difficult to scale and expensive to produce [9]. To address those issues, some systems adopt symmetric layouts with matched routing to reduce the need for calibration [5], while others incorporate embedded calibration logic or beam memory to enable automatic phase correction during operation [29, 30].

Beyond hardware, the computational burden in these arrays is substantial. Massive arrays operating at mmWave frequencies require real-time beam steering, channel estimation, and MIMO processing—all at very high data rates. This creates processing bottlenecks at the interface between the RF front end and digital baseband, particularly in mobile and space-constrained applications. Techniques such as hybrid beamforming, beam codebook storage, and tile-level digital preprocessing help reduce this burden and make real-time operation more tractable [21, 25, 31].

Finally, power consumption remains a defining constraint, particularly for mobile or battery-operated systems. Reducing power per channel through circuit-level optimizations (e.g., low-V_{dd} PAs, adaptive biasing), power gating of unused paths, and efficient LO generation is critical for enabling deployment in consumer and vehicular platforms [21, 23].

In totality, the design and fabrication of large mmWave and THz transceiver arrays is an intricate exercise in co-optimization—balancing RF performance, digital control, mechanical structure, thermal behavior, and cost. The state of the art (SoA) collectively reveals a clear trend toward modular, self-aligning architectures, built from scalable tiles that integrate RF, beamforming, and calibration logic in compact, testable units. This system-level thinking is crucial not only to achieve technical performance, but also to meet the manufacturing,

integration, and operational realities of commercial deployment at scale.

2.3 Beamforming Techniques in Large Transceiver Arrays

Beamforming lies at the heart of phased-array transceiver design, dictating not only performance but also system complexity, calibration effort, and application suitability. A wide spectrum of beamforming approaches have been reported in the literature, from traditional analog phase shifting to digital-assisted schemes and unconventional architectures. Below, we dissect the beamforming strategies adopted in each system and assess their intended benefits.

2.3.1 Analog Beamforming

Analog RF beamforming using phase shifters (PS) and variable gain control remains the most widely adopted technique. Analog beamforming normally accompanies single-input and single-output phased arrays (Figure 2.3(a)), and only one simultaneous RF-chain support is possible. Almost all mmWave arrays with more than 64 elements utilize analog RF beamforming. The systems reported in [5, 8, 9, 11, 18, 24, 28, 30, 32] utilize 4- to 6-bit phase resolution along with VGA control on each antenna path. RF-path phase shifting is selected over its LO-path and IF-path phase shifting counterparts as it not only facilitates signal distribution and array scaling but also requires only one mixer and LO buffer for the entire phased-array chip, resulting in considerable power and area savings [33], [34].

The analog beamforming architecture offers compact integration, low power, and high EIRP scaling as key advantages. For example, the system in [4] uses IQ vector modulators with baseband calibration to reduce DC offset and IQ imbalance, targeting scalable and low-loss beamforming at 76 GHz. Similarly, [8] adopt vector modulators with 5–6-bit resolution to ensure fine phase control and dual-beam support, while minimizing area per element. As reported in [9], compact 2×2 TRX chips are combined to form large arrays of 256 and 64 elements, respectively, emphasizing array-level scalability and low-latency performance. The design in [5] stands out by achieving high-EIRP 5G operation with no calibration, emphasizing symmetric layout and analog uniformity to avoid beam distortion, a notable cost-saving strategy in production-grade arrays.

While analog beamforming is energy-efficient, RF phase shifting usually suffers from gain variation versus phase-shifting issue, which deteriorates the beamforming quality. It lacks the spatial multiplexing capabilities of hybrid or fully digital arrays and often suffers from limited reconfigurability and temperature-dependent phase errors. To address these issues, a set of more advanced arrays implement digital-assisted RF beamforming [21], [29], [24].

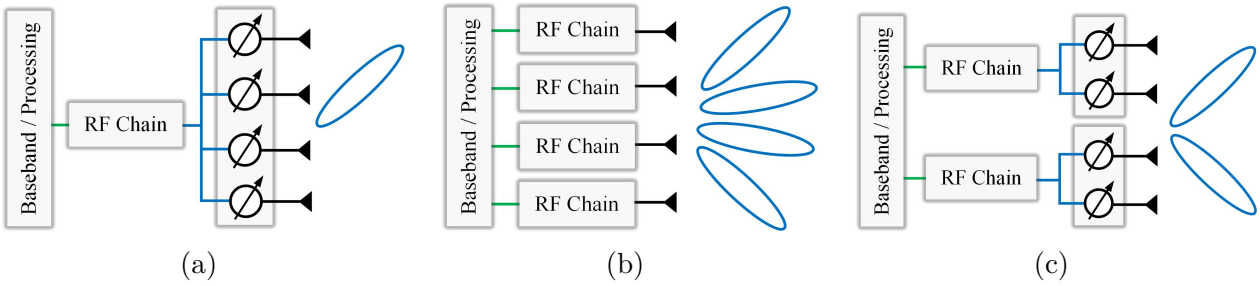


Figure 2.3 Beamforming techniques. a) Analog. b) Digital. c) Partially connected hybrid.

These systems embed beamforming logic such as on-chip beam calculators, beam memory, or slope-controlled phase registers. The systems in [21] and [29] target fast beam switching and wide beam synthesis libraries (e.g., >30,000 beams in [21]) and achieve temperature-robust phase control without calibration. [24], aimed at large-scale 1024-element base stations, employs beamforming with digital gain/phase sensors and thermal monitoring, trading off IC complexity for automation, repeatability, and high production readiness.

Another strategy evident in [9] and [14] is digital compensation and error-canceling analog beamforming. In [9], the authors combine standard RF beamforming with cross-polarization leakage cancellation and inter-element mismatch correction, boosting Dual-Polarized (DP)-MIMO performance without digital predistortion. In [14], the authors implement randomized array thinning with complementary TX and RX fills, reducing the number of active elements by up to 75% while preserving the beam shape. This approach minimizes power consumption and hardware cost while maintaining low sidelobe levels.

Passive beamforming, though limited in control, is presented in [26] and [27]. Despite lacking electronic beam control, these passive arrays emphasize broad bandwidth, low loss, and radiation uniformity, particularly for integration with external TRX modules. Their value lies in manufacturability, array-level EM performance, and thermal management, rather than beam agility.

2.3.2 Hybrid and Digital Beamforming

The fully digital architecture is highly desirable for its maximum flexibility, allowing individual control of each antenna element (Figure 2.3(b) and (c)) [35]. However, the power consumption and hardware complexity of maintaining a dedicated RF chain for each element make this approach impractical for arrays with hundreds or thousands of elements. Such systems are popular in MIMO base stations where performance is prioritized over hardware complexity and processing overhead [36–38].

To address these challenges, hybrid beamforming architectures (Figure 2.3(c)) have gained prominence, particularly in applications where both beam agility and energy efficiency are required [39]. These systems integrate analog phase shifters with digital baseband processing, significantly reducing the number of RF chains while maintaining reasonable beamforming flexibility [40]. It is beneficial in real-world scenarios where a limited number of users exist, and power consumption and complexity are important. Hybrid beamforming can be divided into fully-connected and partially-connected networks. In fully-connected networks, an RF front-end is connected to all antennas in the array, whereas partial connection limits access to antennas. Full-connection networks are feasible in small array sizes. Scaling for large arrays, the connection network becomes prohibitively complex, especially at mmWave frequencies where it adds power loss and distortion.

2.3.3 Phase Shifters

The PS is a crucial and challenging building block in the phased-array system due to the numerous metrics that should be taken into consideration including insertion loss, phase and gain error, response time, phase resolution, and linearity. For high data-rate communication applications, another parameter, so-called Bandwidth with Phase Steps (BWPS), is also of great importance since the TRX requires linear phase response to support broadband modulated signals. BWPS denotes the frequency range where the phase error remains smaller than a half of the minimum phase-shift step. For a 5-bit PS, the RMS phase error should be smaller than $360^\circ/2^5$ within its BWPS. Thus, it is much more difficult to achieve large BWPS for high-resolution PSs. Active PSs based on vector-modulation architecture can achieve extremely low RMS phase error at a specific frequency point through calibration, whereas it is difficult to maintain such a low value (smaller than half the phase-shift step) over a wide frequency range [41], [42], leading to a small BWPS.

The LO phase-shifting-based transceiver can achieve very fine beam steering resolution and gain-invariant phase tuning [43]. For example, the 7-bit PS in [44] yields a relatively large RMS phase error (larger than 1.4°) when the frequency deviates from the calibrated frequency point. This architecture is attractive because the insertion loss and non-linearity of a phase shifter will not be directly applied to the transceiver front-end performance.

IF beamforming is gaining interest in mmWave and THz applications, owing to its low noise, reduced power consumption, and improved phase error performance [45]. Despite its advantages, IF beamforming requires a super-heterodyne architecture and relatively higher IF frequencies to support practical bandwidths. Additionally, its larger footprint poses challenges for integration into 2D arrays.

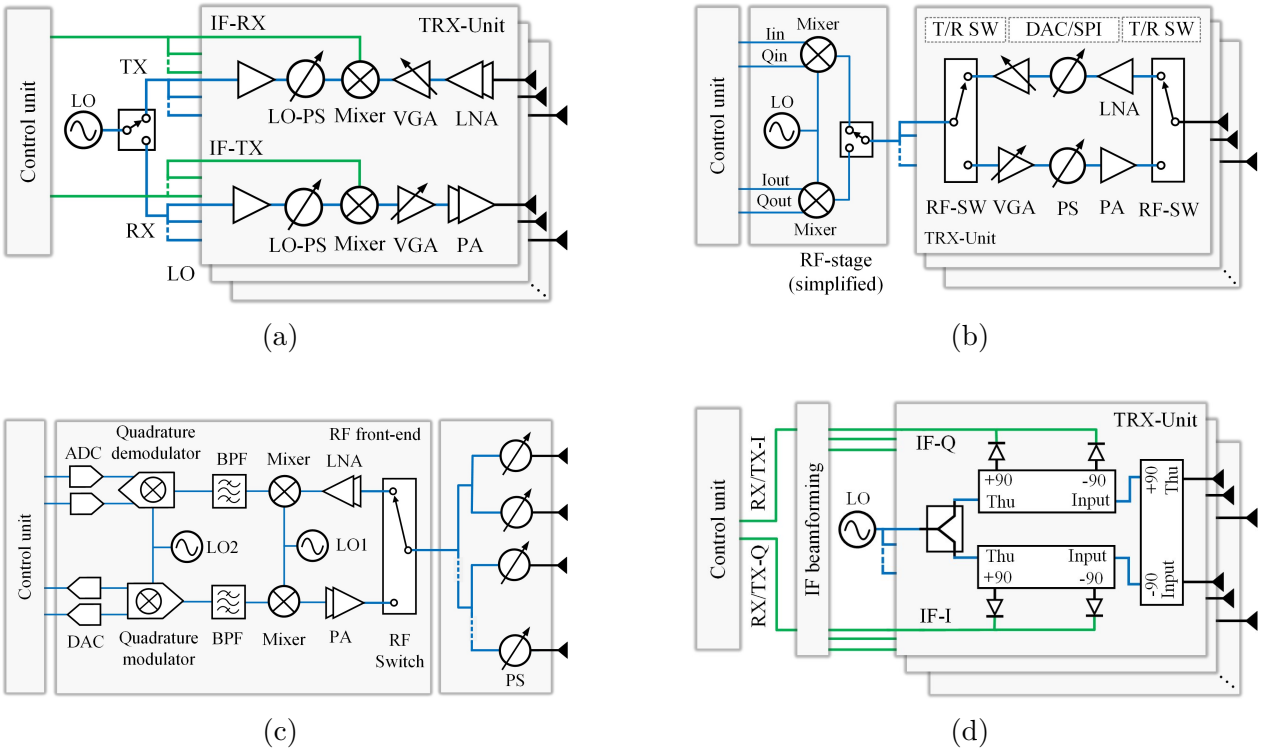


Figure 2.4 RF front-end distribution in phased arrays: (a) Local up/down conversion and amplification to antenna in a full distributed architecture. (b) Local amplification and RF phase shifting for beamforming. (c) Fully concentrated central RF front end. (d) distributed topology based on interferometric unit cell.

The choice of beamforming technique is ultimately application-driven: base stations favor digital resilience, handset modules prefer integration efficiency, and satellite or radar systems demand spatial coherence and thermal scalability. Together, these references paint a rich picture of how beamforming continues to evolve as a multi-dimensional design choice in advanced mmWave arrays.

2.4 Large Arrays and Integration Level

Transmitters and receiver RF front-end architectures in large arrays can be categorized in three groups based on level of integration. These categories are graphically shown in Figure 2.4.

The integration of functionality within IC modules in large-scale mmWave and THz phased-array systems is a decisive factor in how these arrays are architected and deployed. A spectrum of integration philosophies is reported in the literature, each aligning closely with

the system's intended application, performance targets, and packaging strategy. At the heart of this design choice is the level of functionality embedded within each beamforming unit—ranging from full transceivers with mixers, to simpler analog beamformers, to purely passive front ends.

At the highest level of integration are systems where each IC functions as a complete transceiver (Figure 2.4(a)), embedding not just PS and variable gain amplifiers (VGAs), but also frequency converters (mixers) and often on-chip LO distribution or division. It allows LO phase shifting over RF, which reduces constraints from PS, especially at mmWave and sub-THz where PSs becomes power-hungry and large. Distributing the mixers are also beneficial in extending the top-end dynamic range of receivers as mixing takes place before integration, hence improves the DR by $10\log(N)$ where N is number of antennas. These systems, such as in references [14,22,28,46,47], are set to offer direct or low-IF frequency translation alongside per-element analog beamforming. For instance, in [46], the 22 nm FinFET CMOS IC integrates direct-conversion mixers, PS, VGA, and PA/LNA blocks, enabling true tile-based transmit and receive operation across a 64-element array. Similarly, [22] adopts a digital-assisted analog beamforming architecture where each 8-channel IC integrates PS/VGA stages, I/Q mixers, LO drivers, and digital memory to store beam coefficients. These systems are designed to support fully distributed beamforming and frequency conversion, making them modular and scalable while easing routing complexity—particularly useful for high-frequency infrastructure or satellite platforms.

The second category consists of ICs dedicated to beamforming (Figure 2.4(b)), which utilize PS and VGA for analog phase and amplitude control, but depend on external mixers and LO infrastructure. This category, represented by references [3, 11, 24, 26], simplifies the per-tile IC design by omitting mixers, often operating purely at RF. These systems typically centralize the up/down conversion stages, allowing each tile to operate as an analog front-end. In [26], for example, the beamformer IC includes 6-bit phase shifters and programmable gain amplifiers, but the frequency conversion occurs off-chip. This design approach reduces IC complexity and power, making it attractive for 5G base stations and high-performance mobile terminals where calibration, layout symmetry, and manufacturability are tightly constrained.

Figure 2.4(c) illustrates systems operating at higher frequencies that use RF-only phase shifter modules, without signal amplification or frequency conversion. These modules, such as those described in [3, 4], rely on external gain blocks and centralized TRX units, using analog phase control through either switched lines or tunable elements. These designs are often found in multiband or experimental systems where designers want to decouple beam steering from gain and frequency management. For example, in [4], the 256-element array,

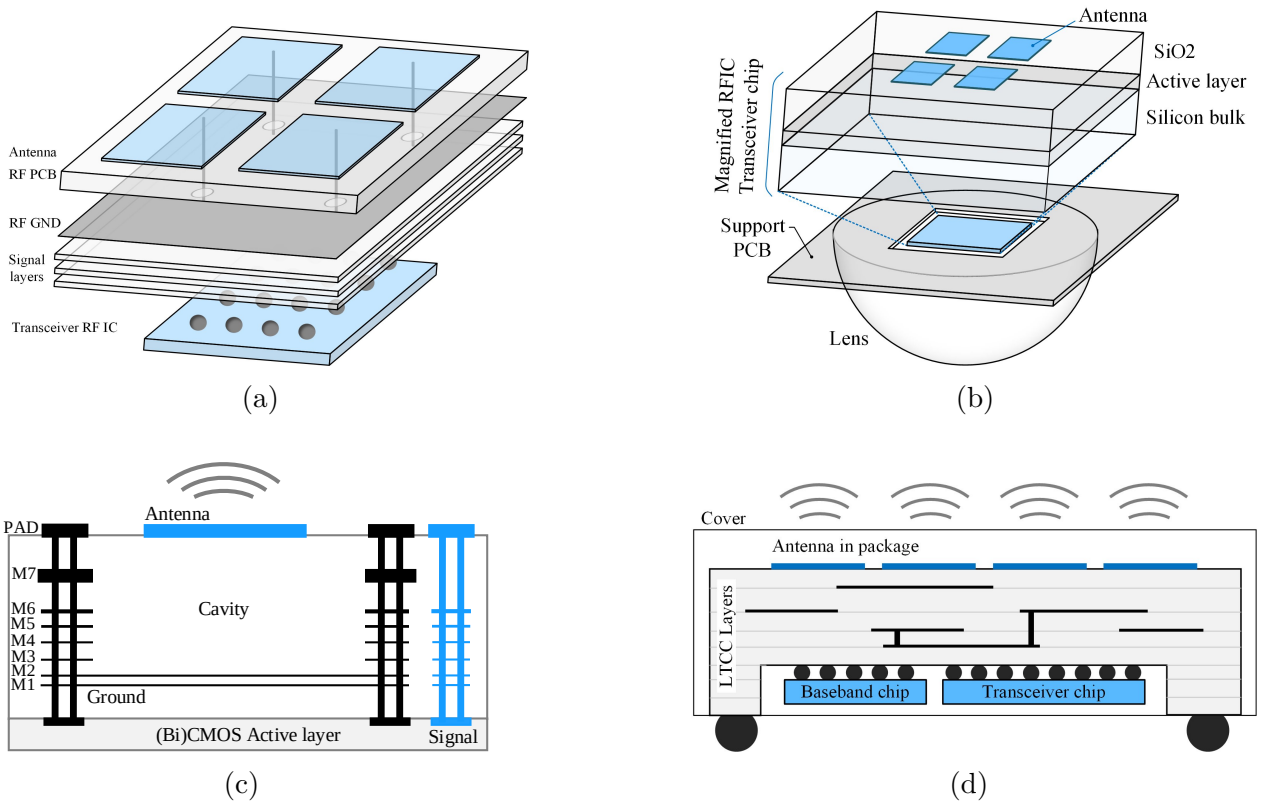


Figure 2.5 Large array implementation technologies. a) Tiled and Panel-Level Integration. b) Antenna on chip: back side radiation. c) ntenna on chip: front side radiation. d) Antenna-in-Package (AiP).

operating at 60,GHz, employs beamforming via wafer-scale phase shifters, while mixers and baseband circuitry are implemented separately.

Finally, there are hybrid or configurable platforms, like those in [10, 21, 32], where integration levels vary by design. These systems use analog beamforming tiles with some form of distributed control but may rely on external mixing or synchronization. Often, they are designed for experimentation, and their integration choices reflect the need for reconfigurability and flexibility over optimization.

As illustrated in Figure 2.4(d), interferometric transceiver units arranged in a distributed topology represent an emerging approach, designed primarily to enhance performance while minimizing power consumption. Extremely low LO power requirement ($\sim 20\,\mathrm{dB}$ lower), in addition to passive detection, makes meaningful difference in the overall power consumption in large arrays. For example, [48, 49] report 24,GHz transmitter and receiver arrays designed for multi-functional, multi-band operation. In addition, recent advancements in size miniaturization [50] and dynamic range extension [51] have addressed two major challenges in

realizing IC-compatible large arrays, particularly for communication applications. In [50], a Lange-coupler-based six-port configuration achieved a compact $\lambda/2 \times \lambda/6$ footprint, with the detectors and matching circuits fully integrated. Meanwhile, the dynamic range extension technique reported in [51] employs a pre-distortion stage ahead of the detector to effectively flatten the square-law region, incurring negligible penalties in power consumption and noise figure.

2.5 Physical Implementation of Large Arrays: Packaging, Signal Distribution, Technology

Realizing large-scale mmWave and THz transceiver arrays for applications such as 5G/6G wireless infrastructure, backhaul links, radar sensing, and satellite communications presents a complex and multidimensional engineering challenges. The promise of these arrays lies in their ability to provide high-gain beamforming, wide bandwidths, and spatial multiplexing. However, turning this potential into practical systems requires navigating a web of constraints tied to fabrication, integration, coherence, thermal behavior, signal routing, and computational complexity.

Large-scale array implementation involves various scaling challenges, including synchronization, heat dissipation, antenna integration, routing, and mutual coupling. Each can become the limiting factor depending on the frequency band, technology, and application requirements. Here we cover solutions reported for SoA large array realizations across the frequency spectrum and analyze the solutions incorporated in.

Apart from the key system-level design choice of the level of on-chip integration [52] (Section IV) for phased arrays, antenna integration is another central difficulty. On-chip antennas offer compactness and compatibility with monolithic integration but suffer from poor radiation efficiency due to silicon substrate losses [53], [54]. In addition, aperture efficiency is rather limited because of the physical size and radiation mode. In contrast, in-package antennas (AiP) can improve performance while reducing interconnect parasitics, though they increase packaging complexity and may restrict aperture scaling [30], [28]. On-board antennas, integrated directly on the system PCB, offer higher efficiency and flexibility, especially in large arrays, but require meticulous alignment with beamforming ICs and introduce challenges in board warpage and parasitic tuning [4], [8], [9]. In this case, the choice of antenna elements may be limited because of the pre-designed physical size matching and interconnects. Path loss in the antenna directly contributes to the system noise figure, because it precedes the low-noise amplifier (LNA) in the receive chain. Furthermore, application-specific requirements—such as polarization diversity, wide-angle beam scanning, or multiband operation—further com-

plicate antenna selection and feed network design.

2.5.1 Antenna on Board

At a larger scale, Antenna-on-Board (AoB) configurations distribute RFICs and antennas across a PCB, which is advantageous for low-cost manufacturing and ease of assembly. As shown in Figure 2.5(a), these designs typically employ planar antennas and surface-mount RF components

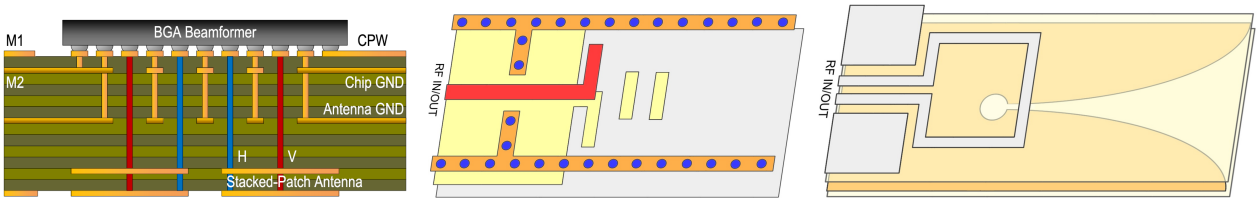
The RFICs, either as bare dies or prepackaged in a chip-scale module, are bonded to the board on the side opposite the radiation direction. As shown in Figure 2.6(a), planar 2D AoB implementations employ single- and double-stacked patch antennas to achieve higher bandwidth [1]. Edge-radiating or end-fire antennas such as LPDAs and Vivaldi antennas are also used in large arrays for ultra-wideband (UWB) applications. In this technique, a stack of 1D array PCBs is combined to effectively realize 2D array operation.

However, AoB systems are prone to higher feed losses and temperature drift, especially when the board is subjected to environmental variations. PCB manufacturing processes and tolerances pose significant challenges in achieving adequate antenna gain and efficiency, controlling antenna variations, and routing electrical signals and power supplies. These difficulties are especially pronounced under the constraints of relatively coarse design rules, including transmission line width and spacing, via drill size, and registration accuracy.

These complexities make this approach more suitable for the lower mmWave frequency bands. For example, to completely suppress grating lobes in the array, the element pitch must be approximately $\lambda/2 = 1.07$ mm at 140 GHz. At these scales, the antenna element pitch becomes comparable to the RFIC dimensions, which poses significant challenges for routing and fan-out. The antennas themselves also scale down in dimensions, putting increased demand on the PCB tolerances. Combined with the need for impedance-controlled transmission lines and sensitive transitions from chip to PCB, the cost and complexity of D-band phased array PCBs are high [55], [56], [57], [58], [59], [60], [61], [62]. Increasing levels of on-chip integration significantly relax the PCB requirements.

2.5.2 Antenna in Package

The second option, as illustrated in Figure 2.5(d), includes implementing antennas on the first-level package. Together with flip-chip–bonded ICs, the package forms a unit tile module. The module can be attached to a second-level PCB through ball-grid arrays (BGAs) to form a larger array (Figure 2.7(b)). Depending on the application, there are many substrate tech-



(a) (b) (c)

Figure 2.6 Antenna on Borad. a) 2D planar double stacked patch antenna [1]. b) Edge radiation: LPDA Yagi [2]. c) Edge radiation: Vivaldi [3].

nologies that have the appropriate properties for implementing the package with embedded antennas, including, but not limited to, low-temperature cofired ceramic (LTCC), glass, high-density interconnect (HDI), organic build-up substrate, and embedded wafer-level BGA. The AiP approach offers low loss and thermal dissipation, and a modular design and test flexibility at the cost of complexity (for example, system assembly) [63], [64], [29], [46], [65], [66], [67], and is by far the most popular scaling approach that has been used across multiple frequencies, including 28 GHz, 60 GHz, 73 GHz, and 94 GHz.

Owing to the availability of multiple layers in the package, various types of antennas can be designed and optimized for the target application. Examples include magneto-dipole antennas [4] (Figure 2.7(a)), dual-polarized antennas, and others. Moreover, as shown in Figure 2.7(c), integration of the antenna-in-package (AiP) with a heat sink is inherently feasible, since they can be placed on opposite sides of the chip, enabling straightforward fabrication.

Off-chip antennas fabricated on a high-performance substrate will typically achieve the highest efficiency, with radiation efficiencies of 85% demonstrated in the literature [68], [69]. The transition loss from the chip to the antenna, however, must be included in the overall efficiency when compared with on-chip designs. Recent work has shown transition losses of 0.9 dB [70] with low temperature co-fired ceramic (LTCC) and 1 dB with a glass substrate [71]. When combined with radiation efficiencies of 85%, however, the overall efficiency can drop to 67.5%–70%. This loss is significant despite using high-performance and high-tolerance packaging techniques that greatly increase fabrication and assembly costs. Aperture coupling, long used for microwave PCB antennas [72], balances the trade-offs between on-chip and off-chip antennas. The aperture-coupled integrated radiator utilizes a slot to excite the radiative mode of a patch antenna off-chip (Figure 2.8(a)). The slot is directly driven by on-chip transistors and, when integrated with frequency generation, confines the high-frequency routing to the chip. No physical routing to the antenna is required due to

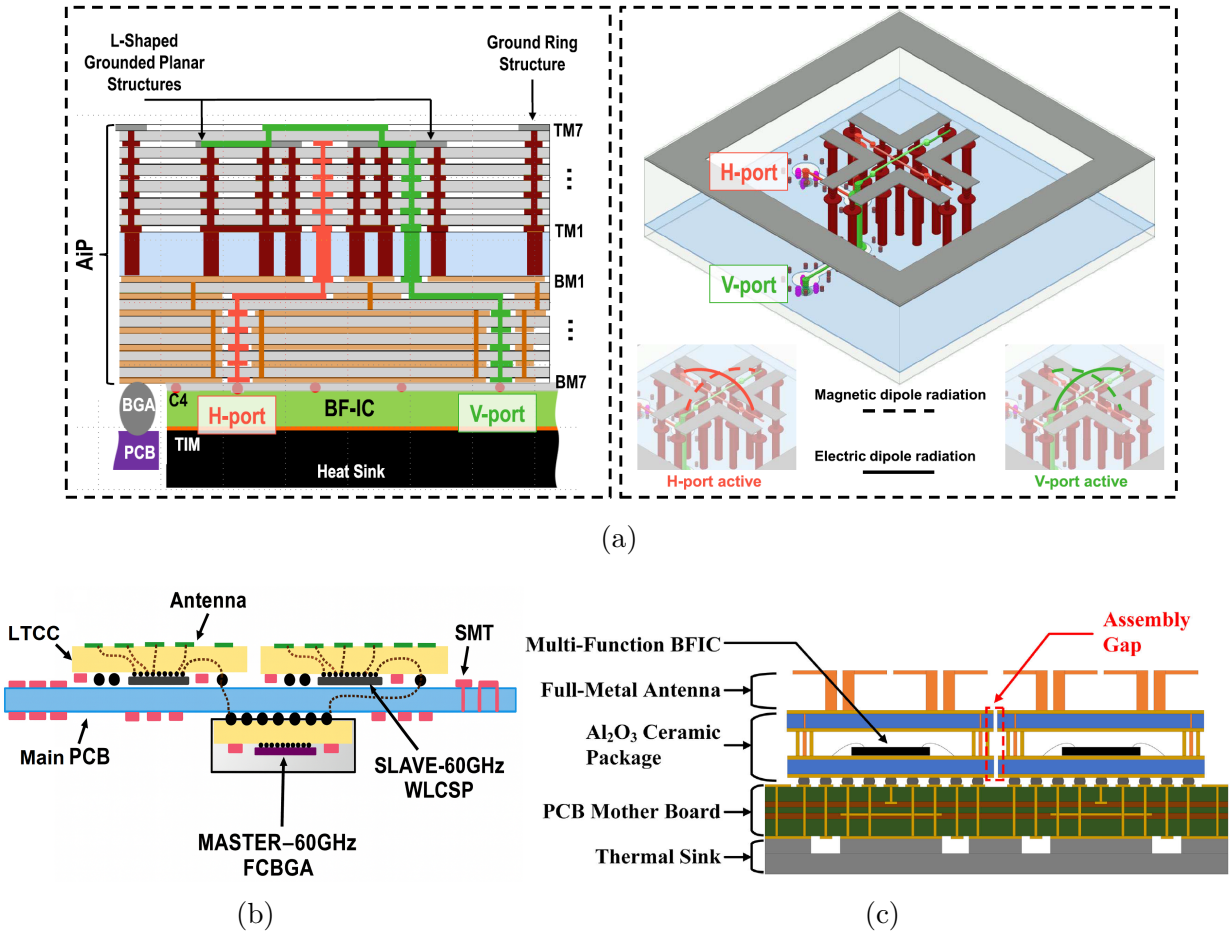
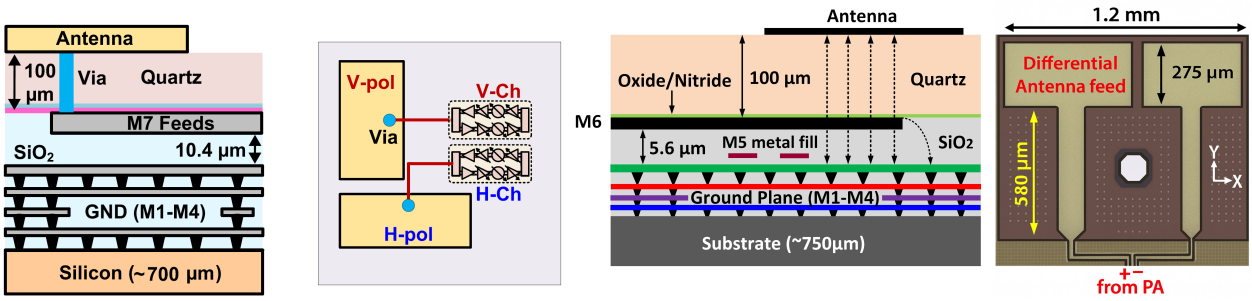


Figure 2.7 Antenna in package. a) Magneto-electric dipole [4]. b) Multi-IC configuration [5]. c) Heat sink placement [6].

the electromagnetic field coupling, eliminating the need for costly chip-to-PCB transitions and transmission lines. The patch antenna is fabricated in a low-loss substrate and achieves good efficiency, broad bandwidth, and wide steering range.

More advanced AiP techniques have been reported in the literature with improved efficiency and bandwidth. In LTCC technology, the SIW-fed Vivaldi [73] achieves wideband D-band end-fire operation with flip-chip RFIC integration, enabling scalable array solutions. Glass-based Empty-SIW (eSIW) beamformers [74] employ air-filled waveguides to reduce dielectric loss while integrating Butler matrices and slot arrays for efficient 200 GHz beamforming. Stacked end-fire AiPs [75] enhance thermal dissipation and maintain short interconnects, supporting efficient operation and two-dimensional beam scanning. Together, these techniques demonstrate notable advances in bandwidth, loss reduction, array integration, and thermal management for next-generation AiPs. However, despite these performance gains,



(a) (b)

Figure 2.8 Antenna on chip. a) Via connection from chip to superstrate antenna [4]. b) Electromagnetic coupling from on chip feed to superstrate antennas [7].

they remain costly, alignment-sensitive, and fabrication-intensive, which limits their applicability in large-array implementations.

2.5.3 Antenna on Chip

The most compact form is the Antenna-on-Chip (AoC) approach, where antennas are fabricated directly on the same die as the transceiver circuits. This integration minimizes feed loss and supports high-frequency operation. This approach is appealing as it can eliminate interconnection losses. However, there are still obstacles to address, including tackling thermal reliability concerns and establishing connections with the main PCB. Various types of on-chip antennas—including patches, slots, loops, dielectric resonator antennas, dipole, cavity, and leaky-wave—have been successfully implemented on-chip [76], [77], [78], [79], [80], [81], [82], [83], [84], [7], [85].

As graphically shown in Figure 2.5(b) and (c), these antennas can be designed to radiate from the top or back sides of the IC, leading to different design strategies. Antennas that radiate from the top typically exhibit lower efficiencies due to the significant mismatch in intrinsic impedances between the antenna medium (silicon dioxide) and air [86]. An effective strategy to enhance radiation efficiency involves the addition of a quartz superstrate atop the antenna, a technique that has demonstrated improved radiation efficiency [87] (Figure 2.8). While this method does necessitate some post-fabrication processing, the associated costs are relatively low.

The 60-GHz wafer-scale transmit phased arrays with 64 and 256 elements spaced $\lambda/2$ m apart have been demonstrated by stacking a glass (quartz) substrate containing metal patch antennas atop the RFIC. Specifically, the 256-element array was built using a sub-reticle

stitching technique to produce a chip that is larger than the standard reticle size. The challenges associated with that approach lie with improving the yield (for example, the wafer stitching and stacking processes), overcoming thermomechanical reliability issues (for example, a significant mismatch in the coefficient of thermal expansion between the wafer and package), and enabling and optimizing the interconnects at the wafer level. To improve efficiency, recently bump (microbump) antennas have been introduced, operating by bonding a metallic bump on top of a conventional on-chip patch, turning the flat 2D radiator into a hybrid 3D structure [88, 89]. The bump redirects more energy into free space and reduces loss in the silicon substrate, leading to higher radiation efficiency, gain, and bandwidth. Importantly, it relies only on standard flip-chip bumping technology, avoiding costly post-fabrication steps.

Radiation from the back side generally achieves higher efficiency compared to top-side radiation. This improvement is attributable to the high dielectric constant of the silicon substrate beneath the silicon dioxide layer, which lowers intrinsic impedance. However, back-radiation faces challenges, as unwanted surface waves can get generated within the silicon substrate, limiting its application to imaging and fixed broadside radiation [90], [91]. To address this, a hyper-hemispherical silicon lens can be added, which can significantly boost efficiency and directivity [86], [92], [93]. Yet, adopting silicon lenses has drawbacks: they are costly and require precise alignment. When utilized with an array, lenses typically suffer from poor performance due to off-axis effects, where the phase center of individual antenna elements does not align with the lens's phase center [94].

Dielectric lenses limit the field of view of the antenna, reducing an array's scan range without the use of mechanical steering or mechanical adjustment of the lens [95]. The bulky lens also results in large element spacing. Mode-suppression techniques require multiple antennas on-chip with fixed phase relationships to limit the excitation of dominant surface-wave modes. Once the array is steered, these surface modes are no longer suppressed due to the excitation phase gradient, resulting in lower efficiency. Wire bond packaging also increases the inter-chip element pitch. Techniques involving advanced post-processing steps, such as localized back etching (LBE), selectively remove silicon around the antenna, improving efficiency [96], [97], [98]. This requires complicated, non-standard processing steps that increase cost and complexity, reducing their attractiveness.

A full survey of on-chip radiators at D-band is documented in [99]. Simple post-processing techniques to boost the efficiency of on-chip radiators have been demonstrated, the most common being dielectric lenses [90], [34], [100] and reflector-based antennas with mode suppression and substrate thinning. The latter in particular has a radiation efficiency of 52% without

requiring complex post-processing or using non-standard high-resistivity silicon. These techniques, however, do not scale when used in an array that requires dense element spacing.

2.5.4 Scalability and Synchronization Considerations

A fundamental challenge begins with the design and integration of high-frequency active circuit components such as power amplifiers (PAs), low-noise amplifiers (LNAs), phase shifters, mixers, and beamforming cores. While advanced CMOS processes are often chosen for their integration density and cost efficiency [4], [21], [24], their performance at mmWave and THz frequencies is often limited by low gain, reduced output power, and higher noise. To overcome this, many systems adopt heterogeneous integration, combining CMOS logic and digital control with RF front-ends fabricated in more suitable technologies like SiGe or even III-V compounds [54], [30], [23]. The functions can be partitioned in different ICs to utilize the most appropriate process technology for each. Multiple numbers of them interface with another IC that performs additional beamforming and frequency conversion. While that approach employs the minimum circuitry, it necessitates mm-wave connections to/from the RF beamforming ICs to the frequency-conversion IC. Those high-frequency connections make it necessary to use higher-performance (read: expensive) packaging substrates, which increases the cost of the solution. Alternatively, each beamforming IC also converts mm-waves to the IF. The much lower-frequency IF signals (typically 10 GHz and below) are then routed to an IF beamforming IC or onboard IF combiners. While the latter approach facilitates the use of inexpensive substrates for beamformer routing and has been utilized by IBM [101], [102], [103], [104], [105], Qualcomm, Nokia Bell Labs [47], and Intel [46], it comes at the cost of additional on-chip circuitry and the requirement for LO distribution/synchronization.

Supporting these ICs requires equally advanced multilayer PCBs, often featuring ten or more metal layers to accommodate RF, LO, IF, power, and digital routing [4], [8], [29]. Materials such as Megtron 6 and Isola Tachyon 100G are favored for their low dielectric loss, but designers must contend with strict layout rules to maintain impedance matching and minimize coupling and skew. The coexistence of analog and digital signals across a dense array exacerbates the risk of crosstalk and parasitic effects, especially at frequencies exceeding 60 GHz.

As arrays grow in size, maintaining phase coherence becomes increasingly difficult. Traditional LO distribution schemes use a centralized oscillator and symmetric tree routing to deliver signals across the array [4], [11], [8]. While feasible in compact arrays, this approach becomes untenable in larger systems due to mismatches in trace lengths, reflections, and

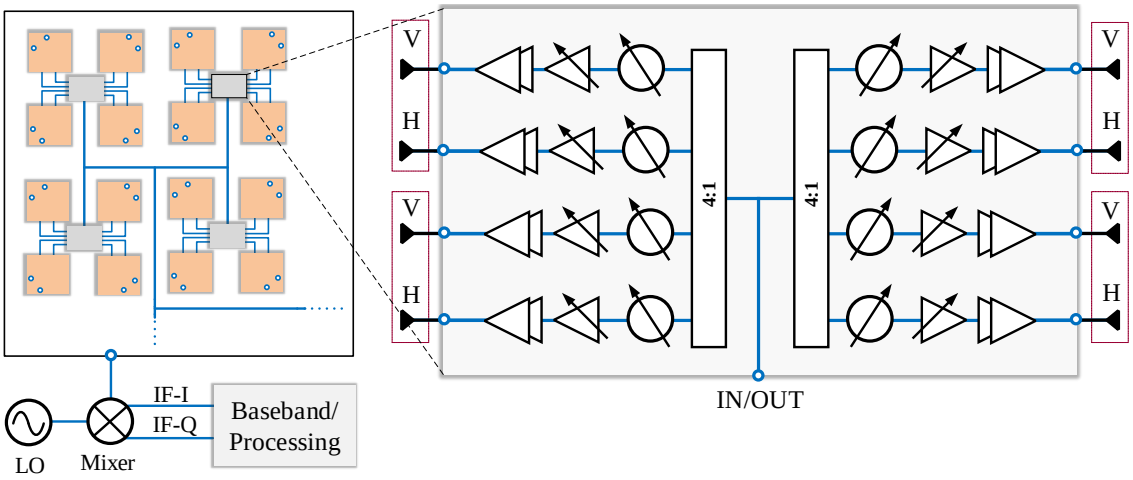


Figure 2.9 A beamformer IC has been developed for a 1024-element dual-polarized transmitter array designed for SATCOM applications [1].

thermal-induced skew. Many modern systems respond by integrating on-chip PLLs per tile, allowing each module to locally synthesize and phase-align its LO [21], [29], [30], [24]. While this enables modularity and reusability, it increases complexity, power consumption, and demands precise digital synchronization techniques.

These densely packed arrays also pose significant thermal management challenges. With each channel consuming tens of milliwatts, total array power can easily exceed 10–20 W in systems with hundreds of elements [4], [8], [29]. Heat dissipation over a confined area requires thermal-aware PCB design, use of heat spreaders, and in some cases active cooling. Uneven temperature gradients across tiles can lead to gain and phase drift, degrading beam coherence unless actively compensated [23], [24].

2.6 Active Circuit Integration

This section reviews representative works that illustrate how circuit integration has been leveraged to realize large-scale mmWave phased arrays. The emphasis is on the principles of operation from a circuit perspective, showing how different design choices enable the target applications by balancing efficiency, scalability, linearity, and polarization performance. Each case highlights the underlying chain of integration, the advantages that motivated the chosen topology, and the frequency range and application domain it addresses.

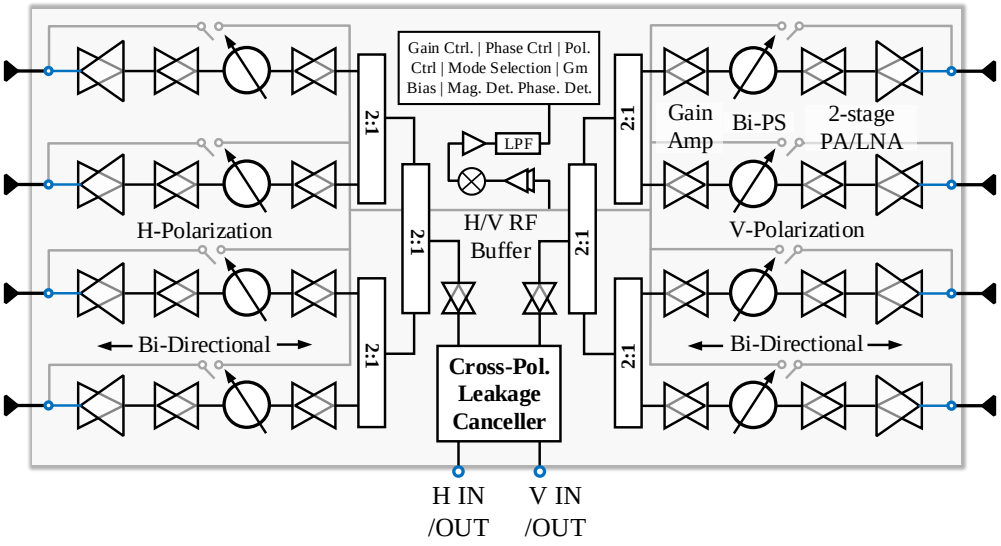


Figure 2.10 Beamformer transceiver IC with bi-directional stages [8].

2.6.1 Beamforming Transmitter IC

The 27–31 GHz Ka-band SATCOM phased-array transmitter, in Figure 2.9, achieves its operation through the tight circuit-level integration of 1024 dual-polarized stacked-patch antennas with silicon beamformer chips and embedded RF drivers on a single multilayer PCB. A 1:256 Wilkinson divider distributes the RF input to 256 eight-channel beamformers, each exciting a 2×2 antenna cell, while quadrant-level RF drivers compensate for ohmic and division losses, reduce the input drive requirement, and enable efficient subarray calibration. The stacked-patch topology provides the necessary 14% bandwidth to cover the Ka-band SATCOM uplink, and independent amplitude/phase control per channel allows agile polarization reconfiguration—linear, rotated linear, or circular—while sequentially rotated feeds suppress cross-polarization over wide scans. This architecture offers several advantages: it scales compactly to thousands of elements, ensures high efficiency by operating close to the compression point, maintains low sidelobe levels with grating-lobe-free $\pm 70^\circ$ scanning, and benefits from PCB-based manufacturing for cost-effective deployment. With a demonstrated peak EIRP of 49.5 dBW, $< 2.3\%$ EVM for QPSK/8-PSK, and suitability for compact, high-throughput, electronically steerable user terminals and SATCOM-on-the-move systems.

2.6.2 Bidirectional Transceiver Beamformer IC

The mmWave phased-array transceiver, shown in Figure 2.10, adopt a bi-directional beamformer architecture to minimize circuit area and simplify feed distribution, reusing the same gain stages, phase shifters, and PA–LNA chains for both transmit and receive. At 28 GHz (5G NR n257 band), a neutralized realization is combined with an active cross-polarization

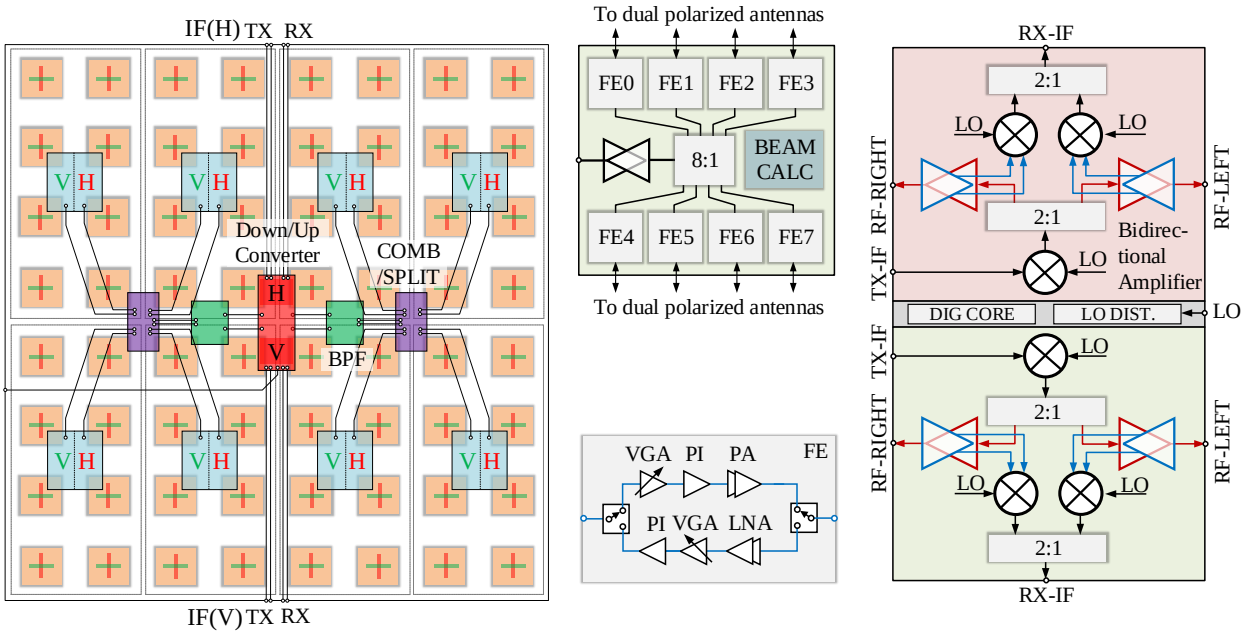


Figure 2.11 Polarized transceiver array using 2×8-element beamformer ICs [9].

leakage canceller, which maintains dual-polarized MIMO integrity under coupling and rotation, enabling $< 4\%$ EVM in 64/256-QAM signaling. This choice directly addresses the application requirement of compact, polarization-robust phased arrays for 5G terminals and access points. The second realization at 39 GHz (5G NR n259/n260 bands), where high-PAPR OFDMA signals reduce efficiency, integrates a bi-directional Doherty beamformer to enhance back-off power efficiency.

To preserve linearity across a large array, shared-LUT digital predistortion with inter-element mismatch compensation corrects AM–AM and AM–PM variations between elements. This topology achieves > 55 dBm saturated EIRP and > 20 Gb/s throughput in a 64-element array, meeting the efficiency and linearity requirements of 5G base-station class systems. In both frequency ranges, the integration of compact bi-directional architectures, polarization management, and mismatch-aware linearization enables scalable, power-efficient phased arrays tailored to the FR2 spectrum for 5G and beyond.

2.6.3 Mutli-IC TRX Chain Distribution

The 24–30 GHz phased-array transceiver is realized through a tiled architecture, where each 64-element dual-polarized module combines eight beamformer ICs, one frequency-conversion IC, and liquid-crystal-polymer (LCP) combiners and bandpass filters within a compact antenna-in-package (See Figure 2.11). Each beamformer IC integrates 16 front ends (eight per

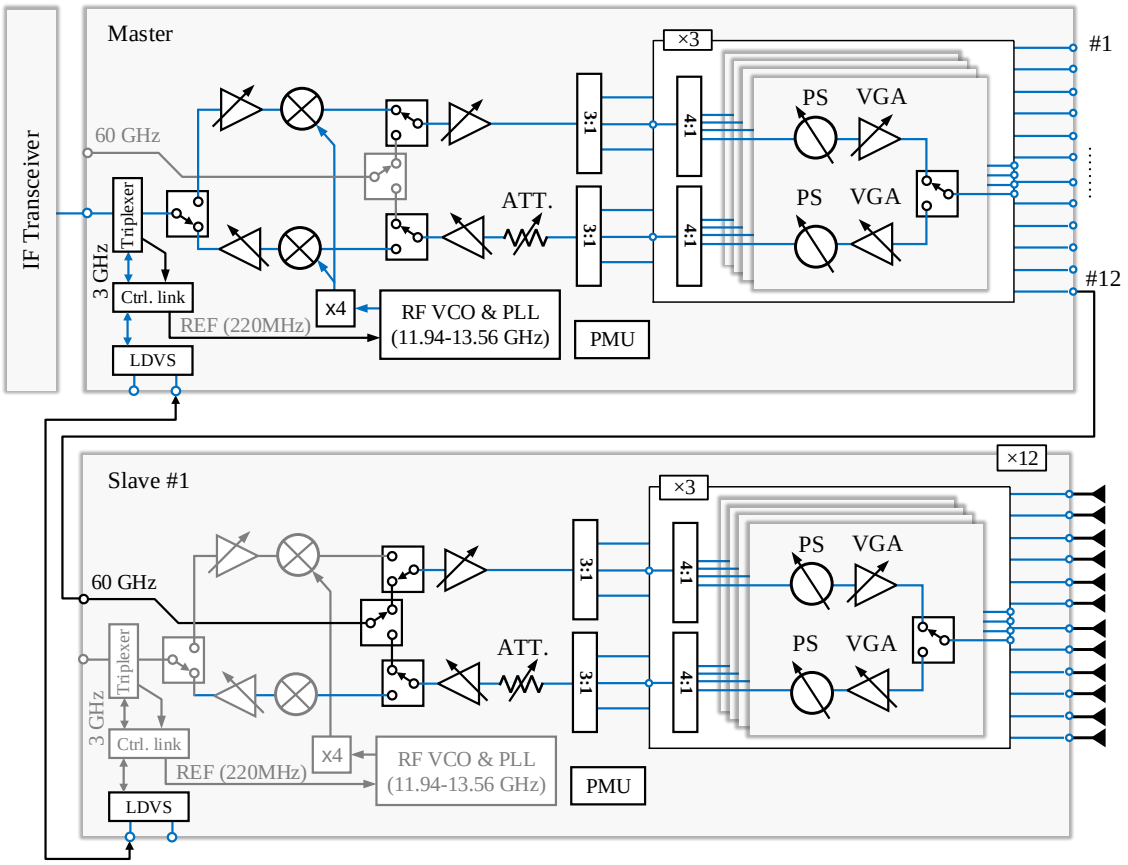


Figure 2.12 Large array configuration based on Master - Follower configuration using identical transceiver ICs with integrated synthesizer [5].

polarization), employing transformer-coupled amplifiers, phase-invariant VGAs, transmission-line phase shifters, differential phase inverters, and capacitively neutralized class-AB PAs, while bidirectional amplifiers compensate for passive losses in the package network. A co-designed transmit/receive switch embedded with the PA and LNA minimizes insertion loss, enabling $> 20\%$ peak PAE and $< 3.9\,\text{dB}$ NF at the module level. To address the growing need for agile beam management, an on-chip digital beam calculator replaces large SRAM beam tables, allowing computation of phase/gain settings per element with $< 200\,\text{ns}$ setup and 8 ns over-the-air switching for more than 30 000 beams. The in-package magnetoelectric dipole antennas provide symmetrical E/H-plane patterns, wide $\pm 70°$ dual-polarized steering, and $> 20\,\text{dB}$ cross-polarization isolation without calibration.

This integration strategy yields a saturated EIRP of 68.5 dBm in transmit mode, efficient calibration-free operation across –20°C to 85°C, and robust 5G-NR modulation performance with $< 2.5\%$ EVM. By combining scalable IC tiling, wideband dual-polarized antennas, and fast digital beam control, the architecture directly addresses the requirements of FR2 5G-

NR bands, where high EIRP, wide-angle scanning, and low deployment cost are critical for base-station class systems.

2.6.4 Master-Follower Configuration with Integrated Synthesizer

The 60 GHz phased-array transceiver, shown in Figure 2.12, employs a master–slave tiled architecture to scale a 12-element transceiver IC into a 144-element array, enabling the high EIRP and sensitivity required for backhaul applications in the unlicensed 57–66 GHz band. A 28-nm CMOS SoC provides MAC/PHY and baseband-to-IF conversion at 10.56 GHz, which feeds a configurable 60 GHz master chip. The master handles IF-to-RF up/down-conversion, LO generation, and distribution of phase-controlled RF signals to twelve slave chips, each adding 12 TX/RX chains with integrated LNAs, PAs, phase shifters, and T/R switches. This RF fan-out approach avoids the complexity of distributing multiple synchronized LOs or IF paths across the array and ensures efficient power distribution at mmWave frequencies. Each RF slice ultimately drives two LTCC patch antennas, creating a compact 288-element antenna module organized as six 48-element tiles. To maintain performance across process and routing variations, the design incorporates firmware-based self-calibration and RF built-in self-test, aligning the phase and gain of all elements without costly external equipment.

This integration strategy offers several advantages: efficient silicon utilization by reusing a single reconfigurable IC design for both master and slave roles, reduced routing loss through RF fan-out, and scalability to large arrays without prohibitive cost. By combining CMOS transceivers with LTCC antenna tiles, the system achieves a maximum EIRP of 51 dBm, receiver sensitivity of –80 dBm, and stable $\pm 60^\circ$ azimuth and $\pm 10^\circ$ elevation scanning, thereby meeting the stringent link budget (≈ 120 dB) and packet error rate requirements ($\leq 10^{-5}$) of fixed point-to-point wireless backhaul over 100–200 m LOS links.

2.6.5 TRX with Integrated Multiplier and Frequency Conversion

The 39 GHz phased-array transceiver IC, shown in Figure 2.13, is implemented in 28-nm bulk CMOS and integrates 16 TX/RX channels with PAs, LNAs, phase shifters, and RF switches on a single die to support large-scale base-station arrays. The transmit chain employs stacked differential CMOS PAs with cross-coupled capacitor neutralization, transformer-based power combining, and shunt feedback for stability, achieving > 16.5 dBm P_{sat} and $> 33\%$ PAE while ensuring reliability under high-voltage swings. Linearity is further enhanced through harmonic termination and body-floating switch techniques, improving OIP3 and extending dynamic range in T/R paths. The receive chain uses inductor-degenerated CS LNAs with cascode gain stages, achieving < 4.3 dB NF at 39 GHz. Integrated 4-bit LC-based phase

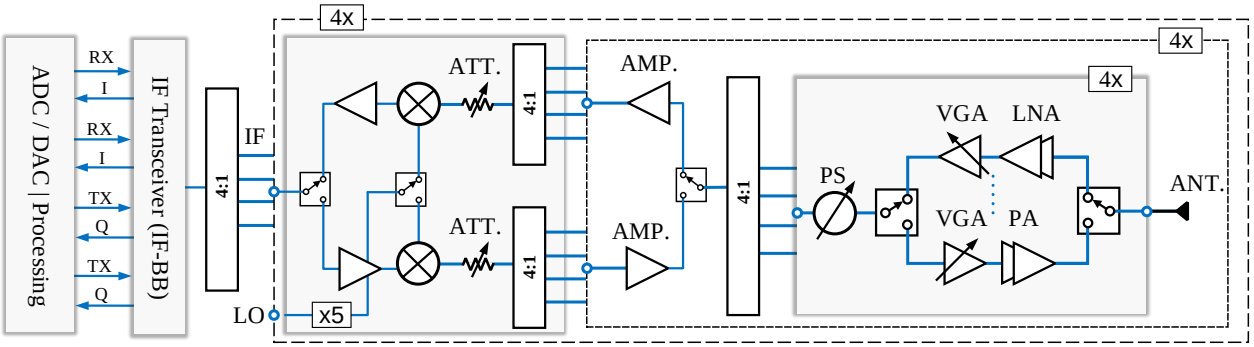


Figure 2.13 Large array formation based on multiple transceiver IC with integrated LO multiplier and down conversion stages [10].

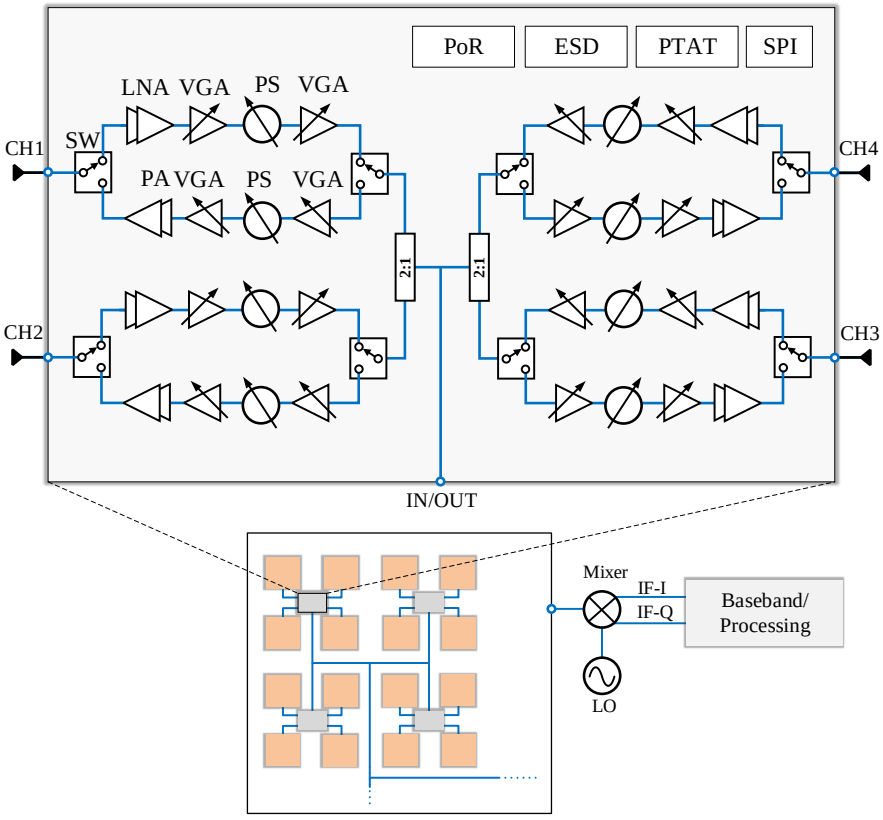


Figure 2.14 Transceiver IC with integrated frequency synthesizer and frequency conversion stage [11].

shifters provide $< 3.3°$ phase error and $< 0.33\,\mathrm{dB}$ amplitude imbalance, while mixers and LO generation with $\times 5$ multiplication deliver high gain and low spurious leakage. A DC–DC converter and thermal/power sensors are embedded for bias control and temperature compensation, enabling stable large-array operation.

At the system level, 16 such ICs tile into a 256-element phased array, scalable to 1024 el-

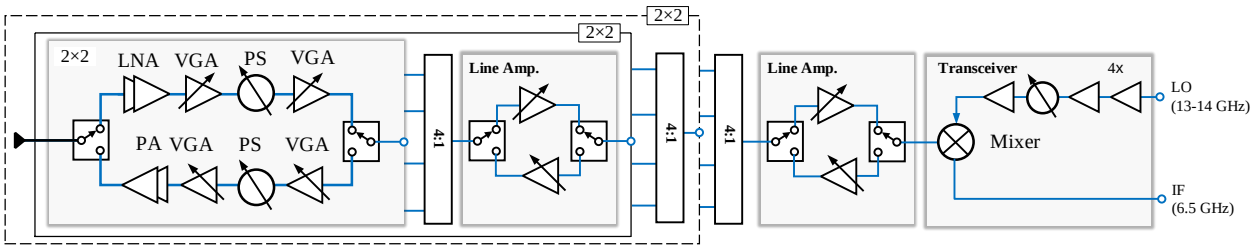


Figure 2.15 Large Array based on large transceiver chip, utilizing line amplifiers for feed network loss compensation [4].

ements for 4T/4R MIMO base-station units. This architecture delivers $> 55\,\text{dBm}$ EIRP, $< -113\,\text{dBm}$ sensitivity (100 MHz BW), and $\pm 60°$ beam scanning, meeting the stringent link budget of 5G FR2 base stations. The chosen CMOS topology offers cost and integration benefits compared to III–V approaches, while design techniques for gain, stability, and linearity overcome inherent CMOS device limitations, making it suitable for mass-deployable high-capacity mmWave 5G infrastructure.

2.6.6 Half-Duplex Switch-Based Calibration Free TRX IC

The 64-element 28 GHz phased-array transceiver is built from 2×2 TRX beamformer unit cells, each integrating LNAs, PAs, VGAs, 6-bit phase shifters, and fast T/R switches in a compact SiGe BiCMOS die. Sixteen of these chips are flip-mounted on a 12-layer PCB with symmetrical Wilkinson divider/combiner networks, while wideband stacked-patch antennas are implemented on the reverse side of the board. This symmetrical integration of chips, distribution network, and antennas minimizes phase and gain mismatch across elements, allowing the array to operate without explicit calibration while still maintaining rms errors of $\sim 1\,\text{dB}$ in amplitude and $< 10°$ in phase. The stacked-patch antennas further contribute image and LO rejection, relaxing filtering requirements at the IF interface. The distributed design enables efficient coherent power combining, yielding a saturated EIRP of 51–52 dBm with 4 GHz 3-dB bandwidth and full $\pm 50°$ azimuth, $\pm 25°$ elevation scanning.

This integration approach offers key advantages for 5G FR2 (n257, 27–30 GHz) base-station and backhaul links: (i) a scalable architecture using identical 2×2 unit cells, (ii) reduced cost and complexity by eliminating per-element calibration, and (iii) robustness against chip-to-chip and routing variations due to averaging in large phased arrays. The demonstrated link performance of 8–12 Gb/s over 300 m using 16-/64-QAM validates the suitability of the topology for high-throughput 5G wireless access and fixed backhaul systems.

2.6.7 Monolithic Large Arrays with Line Amplifier Stages

The 60 GHz wafer-scale phased-array transceivers integrate all-RF beamforming channels with 5-bit phase and 9-bit gain control, nested 1:64 Wilkinson divider/combiner networks, bidirectional line amplifiers, and dual up/downconverters with an LO quadrupler, all fabricated in SiGe BiCMOS (Figure 2.15).

Four identical reticles can then be bondwire-stitched in the IF/LO domain to form a 2×256-element super-reticle ($42 \times 42\,\mathrm{mm}^2$), enabling scalability without additional lithography steps. This reticle-to-reticle approach lowers fabrication cost, maintains yield, and allows phased arrays of 64, 128, 256, or larger sizes to be constructed from the same wafer. The dual-polarized dual-beam architecture enables simultaneous MIMO operation, effectively doubling spectral efficiency, while high-isolation Wilkinson networks and transformer-based SPDT switches preserve polarization purity. The integration of bidirectional line amplifiers distributes gain across the nested network, compensating for routing loss and maintaining uniform beamforming gain. On-chip LO generation at 52 GHz (from 13 GHz input) and coherent IF distribution at 8 GHz simplify PCB assembly and allow seamless reticle stitching.

The 64-element array achieves 37–38 dBm saturated EIRP and supports 12–16 Gb/s QPSK–64QAM links per polarization, while the 256-element stitched array reaches 42–44 dBm EIRP with $\pm 50^\circ$ scanning in both azimuth and elevation. This architecture directly addresses the requirements of 60 GHz wireless backhaul and short-range multi-Gb/s links, offering compact scalability, dual-polarization, and wafer-level integration as its primary advantages.

2.7 Calibration Techniques in Large Arrays

Accurate calibration of large-scale phased arrays is essential to sustain beamforming performance in radar, communication, and sensing systems. Amplitude and phase errors caused by manufacturing tolerances, temperature drift, frequency-dependent variation, mutual coupling, differences in RF path lengths, component tolerances, and PCB routing variations introduce non-uniform phase delays and gain discrepancies between channels [4], [11]. Even minor inconsistencies in PSs or amplifiers can severely disrupt the constructive interference required for sharp beamforming [32], [8], [9]. These variations are especially problematic in systems with a large number of elements, as their effects accumulate and cause beam squint, null filling, or power leakage.

In this regard, calibration targets specific system parameters. Most notably, phase and amplitude of the RF signal paths are calibrated to restore uniformity across the array [21], [5], [29]. Calibration techniques differ in their operating principle, applicability to receiver

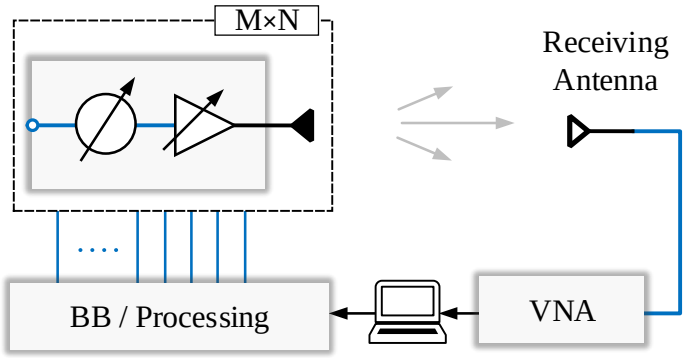


Figure 2.16 Calibration technique based on near-farfield based measurement.

(Rx), transmitter (Tx), or transceiver arrays, and requirements for external RF equipment or operational downtime. In this section, established methods are grouped into categories and compared in terms of principles, advantages, and limitations.

2.7.1 Probe-Based Calibration Techniques

Probe-based methods use external RF measurement systems to directly capture the radiated or received field of the array and compare it with the ideal pattern to extract per-element amplitude and phase errors (Figure 2.16). The two-probe method [106] positions two probes at known offsets in the measurement zone; by sequentially exciting each element or subarray, a set of equations relating probe signals to element excitations is solved to recover complex errors. The mid-field phase-rotation technique [107] uses a single fixed probe and sequentially applies known phase shifts to array elements, inferring individual channel gains from the variation in the received probe signal. Sector near-field calibration [108] partitions large apertures into smaller measurement regions, each captured in an anechoic chamber or near-field scanner, and combines them coherently.

These approaches work for both Tx and Rx arrays and directly measure the true radiated fields, giving high accuracy without requiring strong modeling assumptions. However, they require external RF hardware—such as probes, vector network analyzers, positioners, and large chambers—and are inherently offline, interrupting normal operation. For very large apertures, the required range size and measurement time can be prohibitive [109].

2.7.2 Mutual Coupling–Based Calibration

Mutual coupling–based techniques exploit the inherent electromagnetic coupling between array elements as an internal reference network. In the classical method [110, 111], a single element transmits while an adjacent element receives with all others terminated. The

measured mutual coupling coefficient is compared against a nominal value, and by scanning through transmit–receive combinations, the complex gain of all channels is reconstructed. Frugal coupling calibration [112] reduces measurement effort by selecting a sparse set of coupling measurements and solving for the remaining responses via estimation algorithms.

Such methods are most suited to transceiver arrays with bidirectional T/R modules but can be adapted to Tx-only or Rx-only arrays with switching hardware. They require no external measurement equipment and can be conducted in the field. Their low cost and operational convenience make them attractive, but they depend on the assumption of stable and uniform coupling. Coupling coefficients can vary with scan angle, environment, and element spacing, and arrays with low inherent coupling may suffer from poor SNR in coupling measurements [110].

2.7.3 Amplitude-Only Calibration

Amplitude-only calibration avoids coherent vector receivers by deducing phase from total power measurements under controlled excitation changes. The rotating element electric field vector (REV) method [113] sequentially varies the phase of one element while recording far-field power; the sinusoidal variation in power is used to extract the element's phase error. In very large arrays, the small contribution of a single element to total power flattens the sinusoid, increasing noise sensitivity. The multi-round grouped REV [114] addresses this by grouping elements whose phases are rotated together, producing larger power variations; an initial coarse calibration is refined in a second round after pre-compensation. The cyclic subarray approach [115] excites subsets of elements in sequence and uses redundant measurements to solve for individual phases.

These methods can be used on Tx or Rx arrays and require minimal equipment—often only a power detector or far-field monitor antenna (Figure 2.16). They simplify hardware but require many excitation patterns, leading to longer calibration time. Performance degrades in low SNR conditions or in environments with significant multipath [114].

2.7.4 Built-In Self-Calibration

Built-in self-test (BIST) enables on-chip testing capabilities, significantly reducing test time by allowing parallel or real-time measurements without the need for extensive external hardware. It incorporates dedicated calibration hardware into the array to generate and measure known reference signals. In the multi-beam phased array self-calibration method [116], embedded calibration antennas inject signals into the aperture and each channel's response

is normalized against a reference. The portable low-overhead system [117] uses a compact calibration module temporarily connected to illuminate the array with a coherent signal. Algorithmic approaches, such as time-domain simultaneous perturbation stochastic approximation (SPSA) [118], perturb multiple channels with pseudo-random signals and estimate correction coefficients from measured outputs.

Primarily applied to Rx arrays, these methods require no external RF probes and support true in-field operation, enabling quick recalibration during brief operational pauses. They capture both electronics and antenna path effects, but added hardware increases cost and can introduce coupling between calibration and operational paths, accuracy depends on the stability and SNR of the injected signal.

Approaches used for BIST include direct and indirect test methods [119]. Direct methods directly interface with the high-frequency signals of the circuit-under-test (CUT) and allow for high-accuracy extraction of key performance metrics, such as gain and phase. However, designing the necessary signal generation and injection circuitry is challenging, as they must process mmWave signals without affecting the CUT's sensitivity by altering impedance matching, introducing additional signal loss or noise [120,121]. Furthermore, since these BIST components function at mmWave frequencies, they tend to consume significant chip area and power [122]. Indirect approaches use low-frequency circuits to extract high-frequency parameters such as voltage, impedance, or temperature sensors. The collected sensor data is then correlated to high-frequency information through simulations or measurements and can be used for future calibration [123].

Embedded intelligence for self-calibration has become increasingly prevalent in large arrays, where continuous calibration is required to maintain performance in dynamic conditions. These systems employ on-chip AI modules to monitor temperature variations, mechanical stress, and signal drift, automatically adjusting the beamforming coefficients. A prominent example is the W-band phased array with integrated AI calibration, which maintains beam alignment with less than 1 dB deviation under temperature fluctuations from -40°C to +85°C [47].

2.7.5 Remote Source–Based Calibration

Remote source–based methods illuminate the array with a controlled wavefront without a permanent large test range. The Mobile Fourier Gauge (MFG) [109] moves a short RF line source along the aperture, measuring coupling at multiple positions; phase-corrected summation of these measurements synthesizes a virtual long line source with a known cylindrical wavefront. The satellite-based calibration (SatCal) [109] uses reflected signals from tracked

Table 2.1 Comparison of calibration methods for array systems.

Category	Example Methods	Rx/Tx Applicability	Ext. RF Equipment	Online/ In-field	Advantages	Limitations
Probe-Based External Measurement	[106–108]	Rx/Tx	Yes: probes, VNA, chamber	No	High accuracy; direct measurement	Costly, time-intensive; facility-bound
Mutual Coupling–Based	[110–112]	Tx/Rx/ Transceiver	No	Yes	Low cost; uses internal paths	Sensitive to coupling variation; SNR issues in weak coupling
Amplitude-Only	[113–115]	Rx/Tx	Minimal	Partial	No coherent receiver required	Many measurements; noise-sensitive
Built-In Self-Calibration	[116–118]	Mostly Rx	No	Yes	Fast; minimal downtime	Extra hardware; possible coupling issues
Remote Source–Based	[109]	MFG: Rx/Tx; SatCal: Rx	Yes: mobile source or satellite	Yes	Scalable; high accuracy	MFG needs precision mechanics; SatCal limited by pass schedule

satellites to measure each element's receive response, compensating for motion-induced phase changes. MFG supports both Tx and Rx calibration; SatCal is limited to Rx arrays. Both can be performed in the field and scale to very large apertures. MFG achieves high accuracy (~ 0.7 dB, 5° rms) but requires precise motion control and position tracking; SatCal depends on satellite availability and link budget.

Table 2.1 summarizes the calibration techniques discussed. No single calibration technique satisfies all accuracy, cost, and operational constraints for large phased arrays. Probe-based methods [106–108] offer unmatched precision and model independence, making them indispensable for initial acceptance tests but unsuitable for frequent recalibration due to downtime and facility requirements. Mutual coupling–based [110–112] and built-in self-calibration [116–118] approaches provide cost-effective, rapid in-field recalibration but depend on stable coupling or embedded hardware. Amplitude-only methods [113–115] are valuable for systems lacking coherent receivers, while remote source–based techniques [109] combine field deployability with high accuracy for large stationary arrays. Future research will likely focus on hybrid calibration architectures that pair high-accuracy offline measurements with autonomous, adaptive in-field updates, supported by real-time system monitoring to maintain performance in dynamic environments.

2.8 Local Oscillator Distribution and Coherency

Several distinct LO distribution techniques emerge, each tailored to the specific goals, scale, and constraints of the phased-array system under development. The most traditional ap-

Table 2.2 Comparison of LO distribution strategies for large-scale array systems.

LO Strategy	**References**	**Strengths**	**Limitations**
Centralized + Symmetric Routing	[4, 5, 8, 9, 11, 124]	Simple, low jitter, layout-driven	Sensitive to routing errors, poor for large-scale arrays
On-Chip PLL (Tile Autonomous)	[21, 23, 24, 29, 30]	Scalable, flexible, reconfigurable	Requires calibration, higher complexity and power
Daisy-Chained Chip-to-Chip	[25]	Modular, scalable, simplifies global LO tree	Needs jitter control and phase buffering across hops
Master-Slave Digital Alignment	[29, 30]	Beam memory integration, repeatable calibration	Needs SRAM, controller logic
Passive Matched Routing	[3, 9, 22, 28, 32, 54]	Fabrication-simplified, tolerates basic mismatch	Limited tuning capability, less robust to temperature/aging

proach—used in references like [4, 5, 8, 9, 11]—relies on a centralized LO source distributed via symmetrically routed PCB traces. This method ensures reasonable phase alignment in small-to-medium arrays and benefits from layout simplicity and low power overhead. However, as array sizes increase beyond 64 or 128 elements, these centralized architectures become increasingly difficult to scale due to trace mismatches, routing congestion, and thermal drift.

To address this, LO synchronization is achieved using a relatively low-frequency reference signal that is easily distributed to all of the ICs. The reference frequency is then scaled up using phase-locked loops (PLLs) and/or multipliers. However, each connection and block in the LO distribution chain is vulnerable to phase drift with temperature and time. The reference signals distributed to each IC can drift with respect to each other. The PLL phase can drift before it is corrected at every reference edge. The PLL output distribution to different on-chip blocks can drift as well. Phase matching in scaled phased arrays usually needs calibration. IC-to-IC and tile-to-tile calibration requires inter-IC and inter-tile phase communication. Over-the-air loopback is often used for phase calibration, for example, in [30].

Modern arrays such as those in [21, 24, 29, 30] implement on-chip LO generation, using local PLLs in each tile or TRX IC. These autonomous tiles either operate independently (as in [21]) or synchronize to a master reference using digital phase comparators and correction memory (as in [29, 47]). This approach allows for modularity, scalability, and robust reusability across power cycles. In [24], synchronization is maintained using a shared reference clock

and temperature-compensated tuning, making it ideal for large-scale and radiation-prone environments like space.

Compared with multipliers, PLLs offer larger multiplication ratios and a feedback loop that provides phase correction during every reference cycle. However, PLLs contain independent voltage-controlled oscillators (VCOs) that add uncorrelated phase noise (outside the PLL loop bandwidth) to each set of elements that the PLL serves. While uncorrelated phase noise leads to phase noise averaging that results in less corruption of the received signal, the averaged corruption is more difficult to track in the Rx [125], [126] compared to that caused by correlated phase noise. Moreover, integrated Si-based VCOs are much noisier than their typical off-chip counterparts, which can result in higher corruption levels. As a result, when smaller multiplication ratios can be tolerated, multipliers have been preferred to PLLs in scaled phased arrays.

Another scalable technique is found in [25], where LO signals are daisy-chained from chip to chip across a 2D array. Each chip regenerates and buffers the LO locally, which enables horizontal and vertical expansion without a global LO tree. Though efficient for modular systems, this method requires precise jitter management and buffer design to maintain coherence across hops. Table 2.2 summarizes and compares the LO distribution techniques discussed.

2.9 Developments in Large-Array Topologies

This section surveys modern topologies for large-scale transmitter and receiver arrays, focusing on how reinterpreted versions of classical architectures have led to new integration strategies. Rather than incremental improvements, these approaches introduce notable shifts in scalability, efficiency, and functionality, addressing long-standing challenges in power consumption, synchronization, and secure transmission. By examining these emerging circuit techniques, the discussion highlights how established design principles, when revisited with modern technologies, enable performance gains critical for mmWave, THz, and beyond.

2.9.1 Metasurfaces and Active–Passive Co-Integration

Large intelligent or impedance surfaces (LIS/RIS) (Figure 2.17(a)) have emerged as a key technique to reshape wireless environments by making walls, ceilings, or facades electromagnetically active. They address core challenges of modern systems: unfavorable propagation due to blockage and multipath, high interference in dense deployments, and escalating hardware and channel state information (CSI) overhead. By distributing a very large

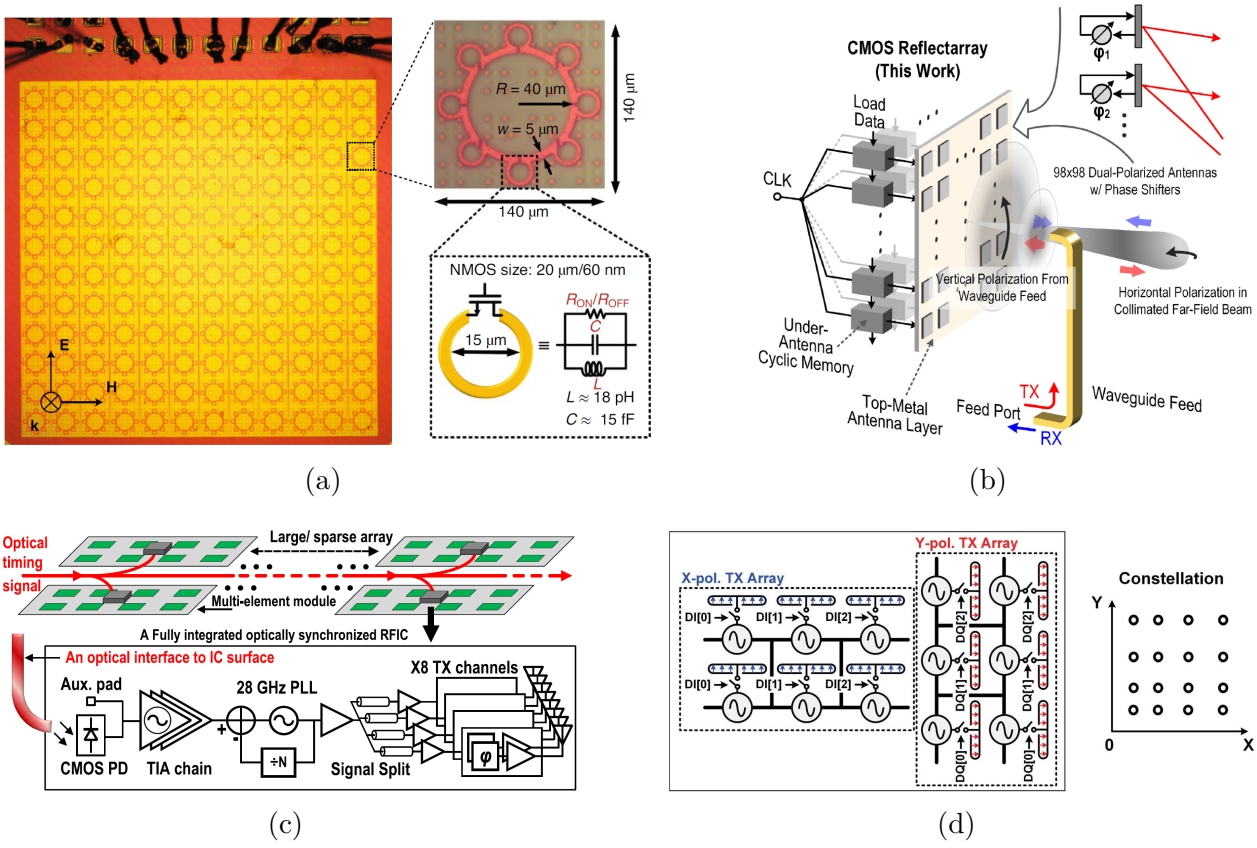


Figure 2.17 Modern topologies for large arrays. a) Large impedance surface [12]. b) Active reflect array [13]. c) Optical synchronization [14]. d) Distributed TX topology.

aperture close to users, these surfaces enable energy-efficient links, suppress interference, and exploit channel hardening, where the channel behaves deterministically as the aperture grows [127, 128].

Compared with conventional arrays and active relays, LIS/RIS offer several distinctive advantages. Their distributed aperture provides stronger coupling to nearby users, yielding power savings and reliability gains beyond co-sited massive MIMO [127]. Their ability to operate in the near field introduces a range degree of freedom, enabling volumetric focusing and spatial "hot spots" that improve coverage in indoor and dense scenarios [129]. Unlike active relays, their passive or semi-passive hardware avoids RF chains, lowering cost and power while maintaining programmability [130–132]. Furthermore, fast subspace and inverse-source methods now allow large panels to be programmed for advanced power pattern shaping, broadening application scenarios [12, 133].

The literature traces this progression from early capacity analyses, which showed asymptotic rates and channel hardening despite impairments and spatial correlation [127, 134–138],

to programmable metasurface experiments demonstrating anomalous reflection and reconfigurable scattering [139, 140]. More recent surveys formalized the concept of smart radio environments and their enabling role in wireless design [130–132]. Near-field studies then highlighted that practical apertures at mmWave operate naturally in the Fresnel region, making near-field gain and benefit distance key performance metrics. Prototypes have validated these effects with PCB unit-cell designs [129]. In parallel, optimization frameworks exploiting both radiating and non-radiating sources were introduced for rapid power-pattern synthesis at scale [133].

From a hardware standpoint, the technique benefits from simple, low-power unit cells implemented on PCB or dielectric substrates, often achieving significant focusing gains even with coarse quantization [129]. Larger apertures increase peak near-field gain but reduce the benefit distance, providing design flexibility. While dense tiling introduces mutual coupling, calibration approaches and impairment-aware analyses confirm that very large apertures mitigate much of the residual error [127, 135, 136]. In summary, LIS/RIS combine scalable hardware, near-field-aware operation, and efficient synthesis methods to transform the wireless environment itself into a controllable entity, offering cost-effective and energy-efficient alternatives to traditional antenna arrays and relays.

2.9.2 Optical Synchronization

Optical synchronization has emerged as a promising technique for overcoming the scalability challenges of phased-array synchronization in communication, radar, and sensing systems. As arrays grow larger and operate at higher frequencies, distributing a common reference clock becomes increasingly difficult. Traditional methods such as low-frequency timing synchronization (LFTS) and radio-frequency timing synchronization (RFTS) face inherent limitations: LFTS is confined to sub-GHz operation and requires buffering that adds jitter and skew [14], while RFTS supports higher frequencies but suffers from attenuation, splitter losses, and the heavy cost of RF materials [141]. Both approaches are vulnerable to electromagnetic interference (EMI) and environmental drift, limiting their suitability for lightweight and widely distributed arrays [142].

Optical timing synchronization (OTS) addresses these shortcomings by modulating timing information onto an optical carrier, distributed through low-loss fiber or free space. At each module, a photodiode converts the optical signal into an electrical reference for local RF generation (Figure 2.17(c)). OTS provides several advantages: optical fibers exhibit far lower loss and mass than coaxial cables [143]; arbitrary reference frequencies can be distributed without high multiplication-ratio synthesizers [144]; and optical links support clock and data

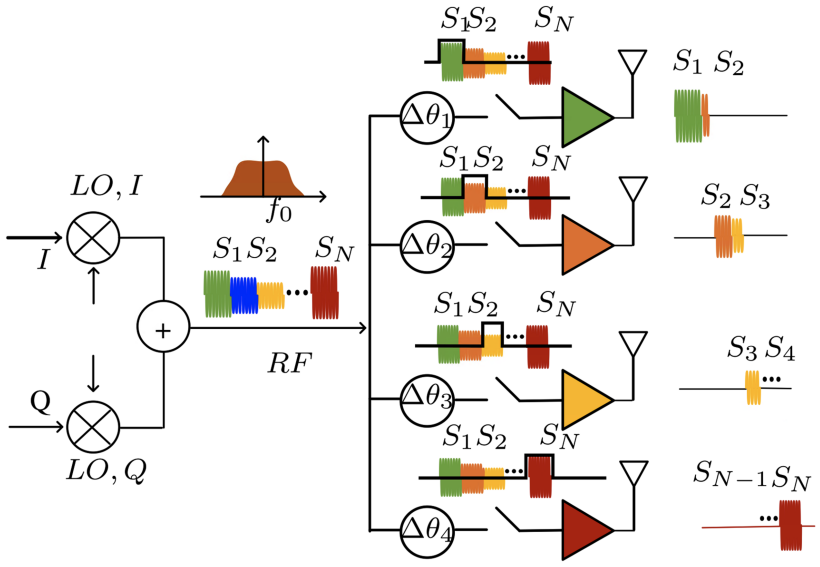


Figure 2.18 Physical layer security [15].

on the same medium [142]. Importantly, power dissipation scales linearly with array size, unlike the exponential growth in RFTS caused by splitter losses [14].

Recent work has demonstrated the feasibility of OTS in CMOS. Gal-Katziri et al. integrated a photodiode, injection-locked amplifier, and low-jitter PLL into a CMOS phased-array transmitter, realizing an eight-element 28-GHz array synchronized over $25m$ of fiber. The system achieved beam steering, high-order QAM transmission, and coherent multi-module operation [14]. Such integration highlights the potential of OTS to enable compact, low-cost, and scalable phased arrays. Applications range from indoor mm-wave imaging and wireless power transfer [145] to massive arrays for radio astronomy [146] and radar coherence processing [147], where low mass, high precision, and EMI immunity are essential. With advances in CMOS-compatible optoelectronics, OTS is poised to become a key enabler for next-generation phased arrays.

2.9.3 Integrated Physical Layer Security

Physical layer security (PLS) has been developed as a complement to cryptography by embedding secrecy into the wireless channel. Its principle is to maximize the quality of the legitimate receiver's channel while degrading that of eavesdroppers, achieving protection independent of computational assumptions [148].

The foundation of PLS was established through the wiretap channel model [149], later enhanced by artificial noise (AN) to impair unauthorized receivers [150]. Multi-antenna sys-

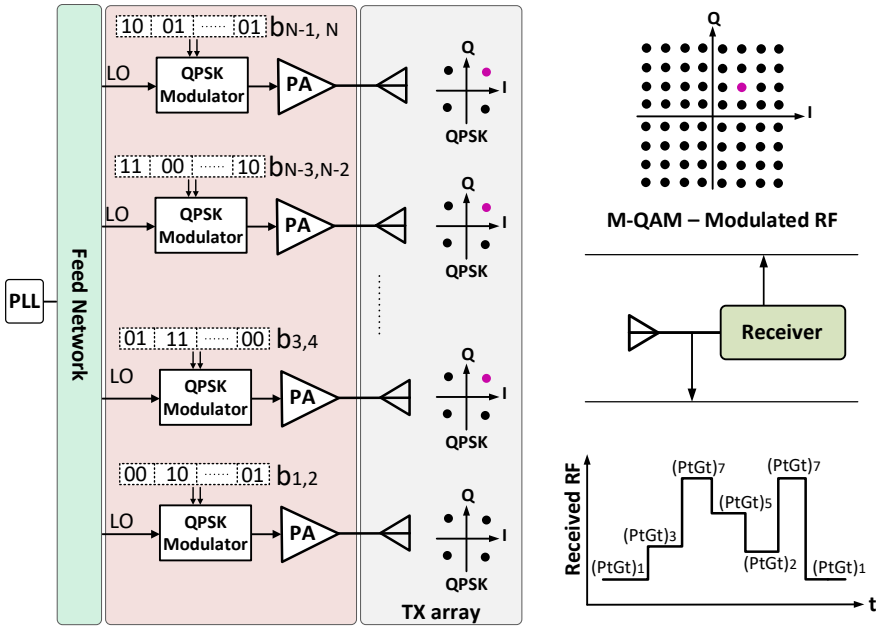


Figure 2.19 Direct-RF large transmitter array, based on QSPK TX units [16].

tems enabled secure beamforming [151], while massive MIMO extended these benefits by exploiting large spatial degrees of freedom, though challenges such as pilot contamination remained [152]. The adoption of millimeter-wave (mmWave) communication introduced highly directive beams and dense arrays, reducing the exposure region of transmissions [15].

Conventional phased arrays, however, still radiate correct constellations in sidelobes, creating security risks. To address this, directional modulation (DM) was proposed, where only the intended direction receives correct symbols, while other directions observe scrambled constellations [153] (Figure 2.18). This idea was advanced through spatio-temporal modulated arrays (STMAs), which apply controlled time variations across antenna elements. STMAs generate secure cones of transmission, producing aliasing and non-bijective mappings that remain unintelligible to even colluding eavesdroppers [153].

In parallel, direct-RF large-array transmitters were introduced (Figure 2.17(d)). In addition to offering power-efficiency benefits, these architectures spatially combine many low-order transmitter units to synthesize higher-order constellations only within the main beam. This principle is demonstrated in Figure 2.19 [16], where integrating QPSK transmitter units into a large array enables flexible higher-order QAM modulation with embedded physical-layer security. Off-axis receivers observe distorted, angle-dependent symbol mappings, thereby providing hardware-level PLS while simultaneously reducing RF complexity and enhancing energy efficiency [16].

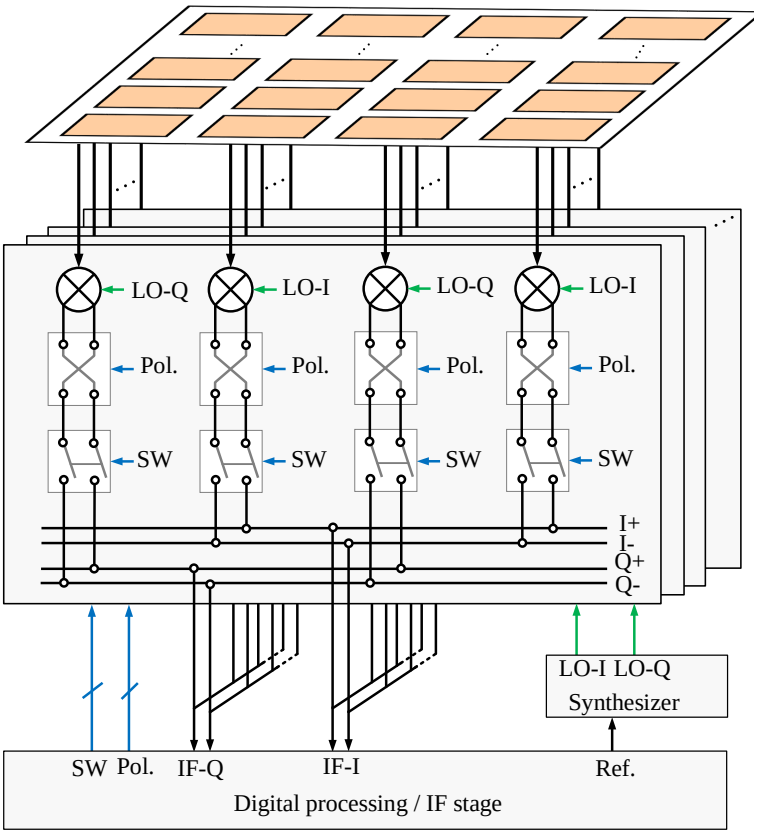


Figure 2.20 Phase shifter-less beamforming for large receiver active arrays.

The trajectory of PLS therefore spans from coding-based secrecy to waveform-embedded and hardware-level implementations such as STMA-based DM and direct-RF large arrays. These advances align with the requirements of 5G and beyond for scalable, efficient, and robust secure communication.

2.9.4 Phase shifter-less analog beamforming

Conventional phased arrays at mmWave and THz frequencies face serious scalability challenges, as RF and LO phase shifters consume large amounts of power, occupy significant chip area, and require increasingly fine resolution as the array size grows. These limitations make traditional digital, analog, and hybrid beamforming architectures difficult to extend to very large arrays, where power efficiency and integration density are critical.

To overcome these bottlenecks, a phase-shifterless analog beamforming technique has been proposed [154]. As shown in Figure 2.20, instead of employing complex phase-shifting circuits, each antenna element incorporates a local down-conversion stage, and in-phase (I) and quadrature (Q) LO signals are distributed in an interleaved pattern across the array. Beam

steering is then carried out at the intermediate-frequency (IF) stage by applying simple polarity rotation (180° switching) and selectively activating or deactivating receiver units. The outputs are combined into direct I and Q channels, enabling quadrature demodulation with inherent image rejection and wideband capability.

By relocating beamforming to the IF domain, the technique eliminates power-hungry phase shifters and precise multi-phase LO generation, reducing power consumption to the μW range while maintaining robust performance. Moreover, the approach becomes more effective as the array size increases, since phase randomness enhances orthogonality and beamforming accuracy. This makes the topology a scalable, low-power, and integration-friendly solution for next-generation 6G/THz systems.

2.10 Challenges and Future Research Directions

A summary of key performance metrics for major large-array implementations is presented in Table 2.3. Realizing large-scale mmWave and sub-THz arrays continues to face several persistent hardware bottlenecks. The inherently high propagation loss, susceptibility to blockage, and limited penetration of mmWave signals make maintaining reliable coverage difficult, especially in dense urban environments. On the hardware side, integrating large numbers of power-hungry RF front-end components—such as amplifiers, mixers, and phase shifters—into compact arrays leads to significant power consumption, thermal management challenges, and increased cost. As arrays scale, precise beamforming becomes increasingly difficult to maintain, due to phase mismatches, hardware impairments, and the need for ongoing calibration. Furthermore, mmWave channels exhibit strong multipath and frequency-selective fading, complicating channel modeling and real-time adaptation.

Addressing these limitations requires a holistic co-design approach encompassing device-level innovation, architectural adaptation, and intelligent system control. At the forefront is the need to improve power efficiency, particularly in large transmitter arrays. Power amplifiers dominate the energy budget in these systems, and as the number of elements increases, total DC power consumption can easily reach impractical levels. Future developments will focus on high-efficiency PA architectures—such as Doherty, Class-J, and envelope-tracking designs—combined with adaptive biasing and element-level power gating to reduce both static and dynamic consumption. On the receiver side, the use of ultra-low-power LNA topologies, such as current-sharing or noise-canceling stages, will be essential in reducing channel-level power to sub-5 mW levels, enabling integration into both infrastructure and user equipment platforms.

In parallel, calibration and alignment mechanisms must evolve to manage the variation and drift introduced by process nonuniformity, temperature gradients, and electromagnetic coupling. Emerging transceiver architectures increasingly incorporate on-chip calibration engines, capable of performing real-time phase and amplitude tuning using embedded look-up tables, thermal sensors, and digitally controlled trim elements. Feedback-based approaches—whether through internal test tones, loopback paths, or over-the-air pilot signals—are essential for maintaining beam coherence without costly factory calibration processes. These mechanisms enable plug-and-play array modularity, which is critical for scalable deployment and field maintenance.

Another crucial enabler for scalable systems is the adoption of hybrid beamforming architectures, which balance the performance of digital MIMO processing with the hardware simplicity and efficiency of analog control. Fully digital beamforming, while ideal from a signal processing standpoint, remains limited at mmWave frequencies due to power, area, and interconnect overheads. Hybrid solutions, on the other hand, employ coarse digital precoding combined with fine-grained analog phase and amplitude adjustments—often implemented using vector modulators or switched delay lines. This layered control structure allows systems to support multi-user and multi-beam operation across wide bandwidths, with acceptable complexity and power draw. Looking forward, hybrid architectures will increasingly incorporate software-defined routing fabrics and machine-learning-assisted beam adaptation to enable dynamic beam allocation, codebook compression, and real-time interference avoidance.

Prospectively, the boundary between electrical, photonic, and electromagnetic interconnects will continue to blur. Future packaging platforms are expected to integrate multi-modal interconnect fabrics that combine electrical redistribution layers, optical waveguides for high-speed data links, and air-filled or dielectric waveguides for RF signal distribution. Such architectures promise compact, low-loss, and thermally efficient modules capable of supporting multi-band communication, radar, and sensing functions well into the D- and J-bands (110–325 GHz). Realizing this vision will require standardized design methodologies, materials with stable permittivity and low loss tangents at sub-THz frequencies, and precise assembly processes that maintain alignment and surface integrity at micrometer scales. Together, these advances define the next generation of heterogeneous integration, where packaging becomes a primary enabler of performance rather than a limiting factor.

Meanwhile, advancements in materials, packaging, and integration—including antenna-in-package (AiP) technologies, wafer-scale stitching, and organic or LIGA-based substrates—are enabling more compact, thermally stable, and cost-effective implementations. These solutions also support higher interconnect density and reduce parasitics, which is critical as arrays scale

Table 2.3 Comparison of Large-Array Transceiver Architectures

Paper	Freq. (GHz)	Array Size	Function	Phase Shifting	TX EIRP	RX NF	Calibration	Modulati	Integration	Data Rate	TX Pwr /Ch	Total Power	Process
ISSCC 2019 [46]	71–76	64 (4×16, 2×2 ICs)	TRX	Analog BB IQ vector mod.	44.4 dBm	5 dB	Phase/delay + DC offset	SC 16-QAM @ 4–6 Gb/s	Antenna-on-package, Die-on-PCB	6 Gb/s	+10.9 dBm Psat, 16% eff.	9.47 W	22 nm FinFET CMOS
TMTT 2021 [2]	37–39.5	TX: 32, RX: 16	Separate TX & RX	4-bit STPS + tunable RTPS	47.5 dBm	6.8 dB	Phase + gain (VGA/RTPS)	SC QPSK–512-QAM	Die-on-PCB, GaAs+CMOS, Ant-on-PCB	3.6 Gb/s, 0.9 Gb/s	22.1 dBm OP1dB, 15–21% PAE	TX: 34.1 W (HPM), 16.4 W (LPM); RX: 6.03 W	65 nm CMOS + 0.15 μm GaAs
TMTT 2020 [4]	60–64	2×64, 2×256 (dual-pol)	TRX (dual-pol, dual-beam)	RF 5-bit vector mod.	37–38 dBm (64), 42–44 dBm (256)	10.6 dB	digital phase/gain + stitching	SC QPSK, 16-QAM, 64-QAM	Wafer-scale, Ant-on-chip (quartz)	32 Gb/s (dual-pol)	∼5 dBm Psat	TX: 9.4 W (64), 18.4 W (256); RX: 7.9–15.6 W	0.13 μm SiGe BiCMOS
TMTT 2016 [7]	57–66	64 & 256	TX	RF 5-bit vector mod.	∼38 dBm (64), ∼44 dBm (256)	N/A	Per-element + stitching	SC QPSK, 16-QAM	Wafer-scale, Ant-on-chip	16 Gb/s	5 dBm Psat	9.4 W (64), 18.4 W (256)	0.13 μm SiGe BiCMOS
TMTT 2023 [3]	16–52	64 (16×4)	TRX	RF 5-bit phase shifter	45.9–51.7 dBm	5.3–6.9 dB	Amplitude + phase per element	SC QPSK–256-QAM + 5G NR	Flip-chip BF + Vivaldi ant. on PCB	3.2 Gb/s	12.9–14.8 dBm OP1dB	TX: 17.6 W, RX: 13.26 W	SiGe BiCMOS (5th gen)
ISSCC 2022 [22]	24–30	256 el. (dual-pol; 4×64 tiles)	TRX (shared PS per FE)	RF PS, 180–260°, 4–5.6° res.	>40 dBm est. (>11 dBm/FE)	<4 dB	Calibration-free	5G NR	AiP, 64-el tiles on PCB	NA	16 dBm OP1dB, 23% PAE	NA	130nm SiGe BiCMOS
TMTT 2021 [11]	27.5–28.5	64 el. (16 ICs × 4ch)	TX	Dual-vector RF PS	42.5 dBm (module)	N/A	Gain/phase cal. (dual-vector)	NA	Die-on-PCB, AiP patch	NA	∼10.7 dBm Psat, 23% PAE	13.6 W (TX module)	130nm SiGe BiCMOS
JSSC 2021 [5]	57.2–65.2	144 el. (8×18 tiles)	TRX (TDD)	IF PS	47.5 dBm (144-el)	6.3 dB	Per-channel cal.	QPSK & 16-QAM	3D-EMB, AoPCB, 65nm RFIC	6.7 Gb/s	∼10.7 dBm OP1dB	13.5 W (TX), 7.7 W (RX)	65nm CMOS
JSSC 2023 [23]	24–30	256 el. (dual pol.)	TRX (TDD)	RF PS	>42 dBm	<4 dB	Calibration-free	5G NR	AiP with ME-dipole antenna	NA	16 dBm OP1dB	Est. 17–20 W/module	130nm SiGe BiCMOS
JSSC 2019 [30]	90.7	384 el. (256 TX / 128 RX)	TRX (TDD)	RF PS, 5-bit	60 dBm (full array)	∼7–8 dB est.	Self-alignment + health monitoring	16-QAM, 32-QAM	AiP, flip-chip tiles on PCB	10+ Gb/s	∼275 mW per TX el.	∼89 W	0.18 μm SiGe BiCMOS
TMTT 2023 [155]	17.7–20.2	1024 el. (dual-circ pol)	RX	Analog passive vector-mod 6-bit	N/A	1.9–2.1 dB	Temp-compensated bias	16-QAM, OFDM 50 MHz	Hybrid-pack: 65nm CMOS BF + 0.1 μm GaAs LNA, ant. on PCB	NA	N/A	∼30.9 W RX	65nm CMOS + 0.1 μm GaAs
TMTT 2025 [31]	27.5–32	64 el. (8×8)	RX, 4 beams	Analog RF 6-bit	N/A	3.7–4.5 dB	Per-element cal. (VGA + phase)	16-QAM, OFDM	Flip-chip BFIC on 12-layer PCB, AoPCB	50 MHz per beam	N/A	∼8.9 W	65nm CMOS
TMTT 2025 [25]	24.25–29.5	32 channels (2×16)	TRX (TDD)	Analog 6-bit LC RF PS	∼46–48 dBm (>11 dBm/ch)	3.2–3.7 dB	NA	64-QAM OFDM	Flip-chip IC, BF-on-PCB	>5 Gb/s (implied)	>11 dBm	TX 4.96 W, RX 1.56 W	45nm RFSOI CMOS
JSSC 2023 [23]	27.5–30	256 el. (16×16, dual-pol H+V)	RX	Analog passive RTPS	N/A	3.6–4.1 dB	On-chip distributed sensors	256-APSK, 1.5 Gbaud, dual-pol	die-on-PCB, AoPCB	24 Gb/s	2.95 mW/element	∼0.75 W	65nm CMOS
IEDM 2022 [1]	39	1024 el. (64 ICs)	TRX	Analog 4-bit LC RF PS	>55 dBm	4.3 dB	Amplitude & phase trimming	64-QAM OFDM	Flip-chip BGA, BF + up/down conv	Multi-Gbps implied	6 dBm/ch	∼108 W	28nm CMOS
PIMRC 2022 [102]	28 & 39	64 el. dual-pol (128 total)	TRX	Analog bi-directional RF PS	Up to 55.2 dBm (39 GHz)	∼4–5 dB est.	Cross-pol + inter-element cal.	SC/OFDM QPSK–256QAM	A: Flip-chip BGA, dual-pol aperture-coupled	15 Gb/s; 21 Gb/s	11.3 dBm/path	TX array ∼25.7 W	65nm CMOS
TMTT 2021 [46]	71–76	16 el./tile, scalable to 64+	TRX	Analog baseband 5-bit RFIC	30–40 dBm est. per tile	4–5 dB est.	No	OFDM/QAM	AiP, 4-die flip-chip, baseband on-package	4 Gbps/tile	6–8 dBm/el	<4 W per 16-el tile	22nm FinFET CMOS
JSYST 2022 [32]	27–29	Reconfigurable 2×2, 2×16, 4×8	TRX bidirec-tional	Analog RF, 5.6° res	Est. via P1dB	N/A	No	QAM-16/64/256	Antenna-on-PCB, standalone tile + BF IC	4.8 Gbps	Limited by PA & backoff	NA	NXP ABF IC

into hundreds or thousands of elements. At the system level, machine learning is emerging as a powerful tool for adaptive calibration, channel estimation, and beam management, providing real-time responsiveness in highly dynamic wireless environments. Software-defined mmWave testbeds are also accelerating the prototyping cycle, enabling rapid evaluation of array architectures, beamforming algorithms, and control protocols.

Looking further ahead, future systems are expected to evolve toward massive intelligent MIMO arrays, and extremely large aperture arrays ((ELAAs) that extend beyond traditional communications to support simultaneous multifunctionalities such as sensing, positioning, and environmental interaction. These platforms will not only deliver higher throughput and reliability but also enable new operational modalities including wireless power transfer functions for self-organized and potentially self-healing autonomous systems, imaging, and ISAC applications.

CHAPTER 3 ARTICLE 1: QUADRATURE HARMONIC SELF-OSCILLATING MIXER: TOWARDS LARGE ARRAY MULTIFUNCTION RECEIVER SYSTEMS

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Abstract: In this paper, a quadrature harmonic self-oscillating mixer (QHSOM) is proposed, studied, and demonstrated for future large array multifunction receivers. Its implementation is based on single-stage direct-conversion harmonic receiver topology. The proposed receiver unit is composed of a pair of harmonic self-oscillating mixers (HSOM), which are injection-locked through their second oscillation harmonic to generate quadrature phase oscillation and isolate oscillation tanks and suppress crosstalk between quadrature channels. To our best knowledge, the proposed receiver configuration is the most compact standalone quadrature receiver topology realization ever reported so far. Its structural simplicity, in addition to enhanced receiving performance makes it scalable to millimeter-wave (mmW) large array receiver realizations. Besides, substantiated capabilities of communication and radar/sensing, accompanied by operation status flexibility within an array make it an appealing candidate for integrated multifunction systems. Transmission and demodulation of digital modulated signals (M-QAM) at $\mathbf{3^{rd}}$ harmonic mixing is successfully demonstrated for the proof-of-concept (PoC). Simulation and measurement results are set to confirm the feasibility and viability of the proposed quadrature receiver.

3.1 Introduction

Many emerging and highly anticipated applications such as autonomous mobility, smart cities, virtual reality, and cellular networks, particularly those associated with the much-discussed 5G/6G technology portfolios, have sparked considerable interest within the R&D community, which are inclined towards developing multifunction wireless systems. In such multifunction scenarios, RF front-end topologies are set to integrate wireless data communication, location service, radar motion sensing, and energy harvesting functions adeptly into a single transceiver [156], [157], [158], [159], [160], [161]. This integration also aims to enhance the power–performance trade-off since the requirements for different operations are also different.

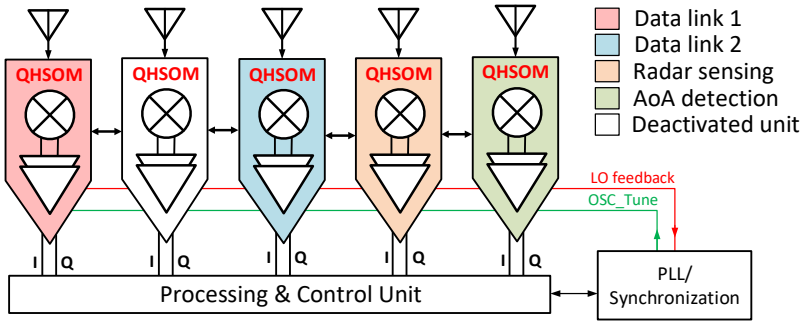

Figure 3.1 Multifunction receiver array representation.

Various forms of active array topologies have been utilized for realizing large arrays, wherein parts or the entire receiver chain are integrated into antennas to enhance topology flexibility, while simultaneously reducing RF distortion, feeding network complexity, and associated losses [162], [163]. This integration, particularly in large array sizes, facilitates the realization of reconfigurable and intelligent multifunction systems for power and performance optimization. In a two-dimensional distributed active array, each receiver unit, including the antenna, RF frontend, and interconnecting circuits, must fit within a $0.25\lambda_{RF}^2$ cell size. The area restriction further escalates in harmonic receiving. Despite the small footprint of compact receivers at microwave frequencies compared to antennas (over 100 times smaller), the distributed nature of circuits at mmW and sub-THz bands dramatically lowers this ratio. For instance, HSOMs in [164], [165], and [166] occupy comparable sizes to the antenna. On the other hand, power consumption creates a significant trade-off between power and performance, thereby restricting the feasibility of large array sizes. In this paper, as conceptually represented in Figure 3.1, we present a compact receiver topology in a coupled oscillator array (COA) configuration with deactivation and polarization rotation capabilities for multifunction receiver arrays.

Single-stage receivers are either designed for a specific application [167], [168], [169], [170], [171], [172], or they are too complex and power-hungry to be integrated into an active array topology and scaled up to mmW band realizations [173, 174]. Cascoding low noise amplifier (LNA), local oscillator (LO), and mixer as the main RF stages of a receiver is commonly used at microwave frequencies to enhance the performance of compact receivers. However, this method results in reduced voltage headroom, which increases the transistor's parasitic effects and significantly lowers its cut-off frequency. Consequently, cascoding is not scalable to millimeter-wave (mmW) and terahertz (THz) bands.

Self-oscillating mixers (SOMs) were employed primarily to enhance the receiver's compactness and power efficiency. SOMs allows integrating both frequency generation (LO) and

conversion (mixing) functionalities by exploiting the nonlinear properties of only one active element. Initially, SOM developments were limited to specific low-power applications. For instance, self-heterodyne [169] and zero-IF [167], [168] receiver configurations incorporated SOMs that were locked to the transmitted LO and RF carriers, respectively, realizing a very low-power receiver and eliminating the need for PLL and clock recovery circuits. The LNA, mixer, and VCO (LMV-Cell) cascoding topology is a direct conversion extension of SOM for GPS applications [174]. Despite the unprecedented quadrature receiving extension, the incorporated cascoded topology significantly distorts the performance of the receiver at mmW frequencies.

Some recent developments include high-mmW (>100 GHz) harmonic SOM (HSOM)-based receivers designed for the low-power RF stage of a super-heterodyne chain, targeted for imaging and low data rate applications [163], [164], [165]. Nonetheless, existing SOM architectures have not yet been adapted to accommodate single-stage amplitude and phase information extraction capability (quadrature receiving). Therefore, innovative solutions are needed to redefine the operations of compact receivers for future large-scale arrays, incorporating novel integration techniques and topologies.

The paper describes a quadrature harmonic self-oscillating mixer proposed and designed for multifunction receiver arrays, featuring the following properties:

- Realization of a direct-conversion receiver topology to facilitate data communication and improve radar/sensing capabilities.
- Capability to receive at both fundamental and harmonic frequencies, extending operation beyond cut-off frequency.
- Low complexity, low-power consumption, and high efficiency.
- Selective deactivation capability within a multifunctional topology, without phase distribution disruption across the array in a coupled oscillator array configuration.

Expanding the concept described in [166], section II studies the principle of operation of QHSOM. In section III, analytical modeling of QHSOM is provided. Section IV presents the circuit design process and related investigations. Section V presents and discusses the proof-of-concept experimental results, and the conclusion is provided in Section VI.

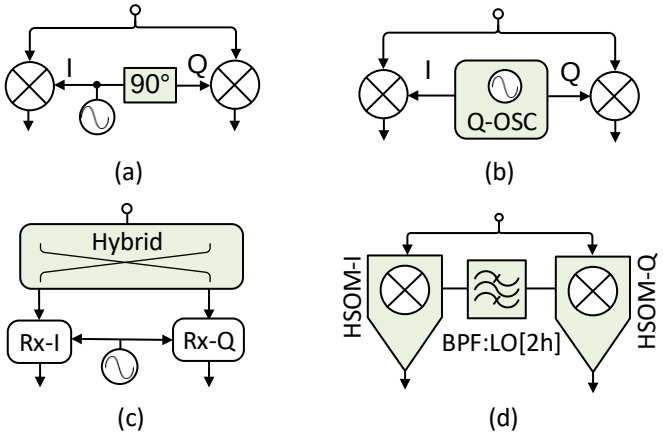

Figure 3.2 Types of compact quadrature receivers. Based on: (a) 90° delay line, (b) quadrature oscillator, (c) hybrid coupler, and (d) quadrature HSOMs.

3.2 Operation Principles of the Proposed QHSOM

Single-stage quadrature receivers can be categorized based on methods used to generate the in-phase and quadrature-phase for demodulating the I and Q channels. The most common and traditional approach, depicted in Figure 3.2(a), relies on a passive 90-degree phase shifter along the LO path and an in-phase RF signal fed to mixers. In integrated circuits (ICs) development, utilizing a quadrature oscillator, as illustrated in Figure 3.2(b), tends to enhance symmetry and augment area efficiency compared to a passive phase shifter in Figure 3.2(a), albeit at the expense of additional power consumption. Alternatively, in the topology shown in Figure 3.2(c), a hybrid coupler in the RF and LO paths generates the required quadrature phase difference. This method has been utilized in six-port receivers, typically for low-power and high frequency applications [175]. However, multi-wavelength size primarily disqualifies it for dense array realizations [156]. Figure 3.2(d) illustrates the concept of the proposed QHSOM, where mixing and oscillation functions are integrated into a single unit. The proposed QHSOM implements a direct-conversion harmonic receiver topology. The RF received signal is fed in-phase into both SOMs at the first or third harmonics, while quadrature phase oscillation is established through the second oscillation harmonic injection locking, forming the QHSOM receiver.

3.2.1 Quadrature Phase Oscillation

The circuit diagram of the proposed QHSOM implementation is depicted in Figure 3.3. HSOM-I and HSOM-Q are constructed using push-pull oscillators. With reference to the

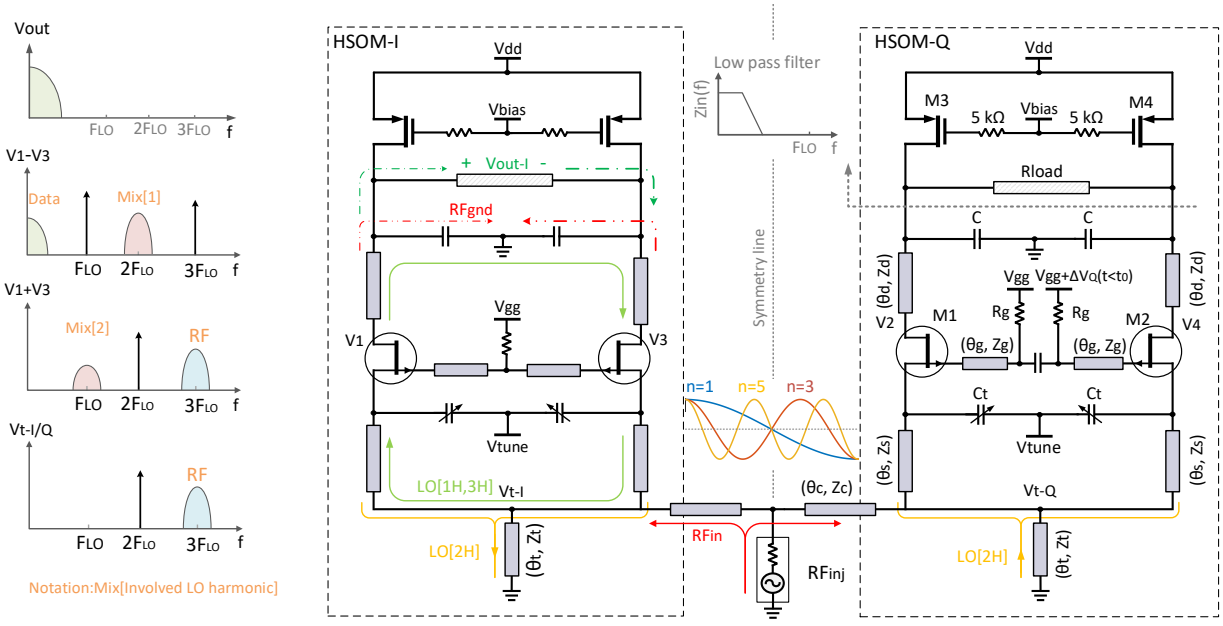

Figure 3.3 The presented QHSOM and respective signal flow graph. All transmission line lengths are in degree at oscillation frequency.

HSOM-Q, M1 and M2 represent RF FET transistors, while M3 and M4 are low-frequency PMOS transistors, both serving as active loads at IF and as biasing circuits. The capacitors (C) are selected to be large enough to short-circuit LO and RF signal paths from the subsequent stages, yet small enough to remain open circuit for data reading at the IF/baseband range. In fact, the active load acts as a low pass filter and design parameters (R_{load}, C) must be selected based on anticipated bandwidth and conversion gain.

The oscillator is configured to operate in differential mode, as detailed in Section II.B, providing anticipated operational advantages for the receiver. In this mode, the connection point $V_{t-I/Q}$ in Figure 3.3 functions as a virtual ground for all odd harmonics (1^{st}, 3^{rd} ...) while sustaining the second harmonic component. In the absence of the fundamental harmonic at $V_{t-I/Q}$ nodes, the injection locking of the two oscillators in the second harmonic forces them into either in-phase or differential phase oscillation modes at the locking frequency ($\angle V_{t-I} - \angle V_{t-Q} = 0°/180°$) [176]. The differential mode, in turn, generates a quadrature (90°) phase difference in the two oscillators at the fundamental, and all odd harmonics. The connecting transmission line (TL) with a length of $\theta_c \approx 90°(2k-1)$, where $k \in \mathbb{N}$, enforces the desired differential mode operation [177]. It is worth noting that a TL length exactly at 90° represents the ideal voltage transfer phase for the strongest locking. Nevertheless, a phase deviation up to $\Delta\theta < 45°$ at the oscillation frequency can preserve the mode state [176]

and oscillation phase values. As explained in Section III, such error resilience in a COA is one of the bases for the deactivation capability of the proposed topology. This aspect is crucial for flexibility within a multifunctional array topology. It permits deactivation of a QHSOM unit without disrupting the phase value and distribution across the entire array.

3.2.2 RF feed and frequency down-conversion

As conceptually depicted in Figure 3.2(d) and illustrated in Figure 3.3, the RF signal is injected from the virtual symmetry line to preserve an in-phase RF feed between the two HSOMs. At this juncture, the injection locking second harmonic standing wave forms a virtual ground. Thus, the RF feed port does not impose any loading, which could distort the injection locking mechanism and cause unintended radiation. From a signal-flow standpoint, in Figure 3.3, the common-mode RF signal injection to the differential pair of each HSOM resembles the single-balanced Gilbert-cell mixer. Apart from the well-known mixing advantages of this configuration, such as common-mode noise cancellation, wideband operation, and high isolation, the common-mode RF injection immunizes the oscillator from the pulling effect. This, in turn, improves the higher end of the dynamic range of the receiver compared to single-ended counterparts [170], [171].

The principle of operation applies both the fundamental harmonic (1^{st} harmonic) and any higher odd harmonic mixing (3^{rd}, 5^{th} ...). Mixing components around the second harmonic are generated through RF mixing with odd harmonics. Hence, the mixing products reside in the differential mode and get canceled out at the connection points $V_{t-I/Q}$, thereby providing isolation between the I and Q channels. In the same process, the down-converted data resides in the differential mode, allowing for a differential IF output.

3.3 Analytical Representation of QHSOM Operation

In this section, an analytical representation of the QHSOM's output for fundamental and harmonic mixing is derived and presented. We can show that the phase sequence for I and Q oscillators varies for fundamental and 3^{rd} oscillation harmonics. Thus, a comprehensive understanding of phase sequence and control methods is required.

3.3.1 Oscillation Phase Control

Taking V1 and V2 as positive nodes in I and Q oscillators, and assuming the following phase sequence at oscillation frequency for oscillator nodes in Figure 3.3, we have:

$$V_{m+1} = \sum_{i=1}^{3} A_i \cos\left[i(\omega_{LO}t - \frac{m\pi}{2})\right], m = 0, 1, 2, 3 \tag{3.1}$$

where A_i is harmonic amplitude and ω_{LO} denotes the oscillation angular frequency. Considering the phase sequence choices, we have $V_{LO-Q} = V_2 - V_4 = \sin(\omega_{LO}t)$ in HSOM-Q, thus indicating that channel-Q lags 90° behind channel-I. However, with the same phase sequence, the 90° phase lag at oscillation harmonic increases to 270° at the 3^{rd} harmonic, and hence $V_{3LO-Q} = sin(\omega_{LO}t)$, leading to a 90° phase lead for the channel-Q. This concept holds importance in communication links as the phases of transmitters and receivers in quadrature channels must be complementary. Conversely, a lead (+90°) phase sequence in the oscillation frequency results in a phase lag (−90°) sequence in the 3^{rd} harmonic LO.

A well-known aspect regarding second harmonic quadrature oscillators is the issue of phase lead/lag uncertainty [178]. Taking HSOM-I as the reference, in a completely symmetric circuit, the injection locking of the second harmonic generates a 180° second harmonic injection phase at HSOM-Q. This can result in oscillation polarity of +90° (phase lead) or −90° (phase lag) at the fundamental frequency in HSOM-Q.

Solutions based on complementary circuits, like the one described in [178], are commonly employed to complement oscillators and establish the phase interval. In this report, to include phase interval reconfigurability, a technique based on initial bias control is proposed and demonstrated. It can be shown that in a differential oscillator, as shown in Figure 3.3, the transistor with a higher initial gain will deterministically lead in oscillation and, consequently, lead in phase as well. Such asymmetry can be created by introducing imbalance in the start-up biasing of the differential pair. Thus, by setting ΔV_Q in Figure 3.3 to a positive or negative value, one can determine the receiver's lead or lag phase sequence.

3.3.2 QHSOM Array for Multifunction Applications

The concept of second harmonic injection locking and the polarity control technique is exploited in our QHSOM array for multifunction systems. In this connection, three HSOMs cut out of a larger COA array configuration is depicted in Figure 3.5 and examined for functionalities of interest. The dynamics of COAs are complex and follow Adler's equation expansion [177]. However, for intended special cases with equally spaced identical oscillators,

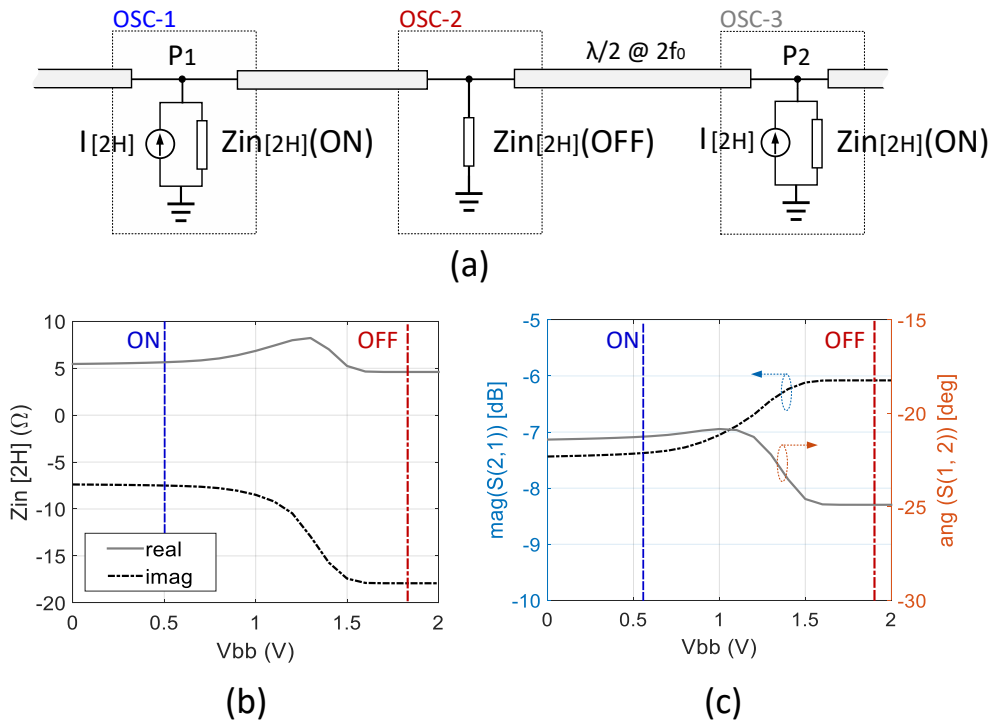

Figure 3.4 Equivalent circuit model of the oscillator array at second oscillation harmonic: (a) source input impedance On/Off variation, (b) S-parameter amplitude and phase On/Off variation.

a stable mode with the desired phase distribution can be enforced [163], [179]. We note that due to the separation between the locking frequency (at the second harmonic) and the oscillation frequency (fundamental harmonic), the oscillator is effectively shielded from the loading effects of injection locking. Consequently, regardless of the array size, the LO parameters such as phase noise and resonance frequency remain consistent..

Figure 3.5(a) and (b) studies the polarity control using bias voltage asymmetry. Following the notation in Figure 3.3, the OSC-2 with a positive bias voltage asymmetry ($\Delta V_2 < 0$) in steady state takes a 90° phase lag from the reference OSC-1. Also, OSC-3 with $\Delta V_3 < 0$, despite in-phase injection signal with OSC-1, oscillates with an opposite phase. In the same configuration, as depicted in Figure 3.5(b), by reversing the OSC-3 bias asymmetry ($\Delta V_3 > 0$), its oscillation phase switches to be in-phase with the reference OSC-1. In Figure 3.5(c) and (d), the intermediate OSC-2, in between OSC-1 and OSC-3 is deactivated to showcase the flexibility of the oscillator array for the selective deactivation within the VRM topology. As shown, despite deactivation, OSC-1 and OSC-3 continue operating similar to Figure 3.5(a) and (b) with an active OSC-2. Figure 3.4(a) presents the connection point equivalent circuit model of the oscillators at the second harmonic. To maintain the oscillation mode between

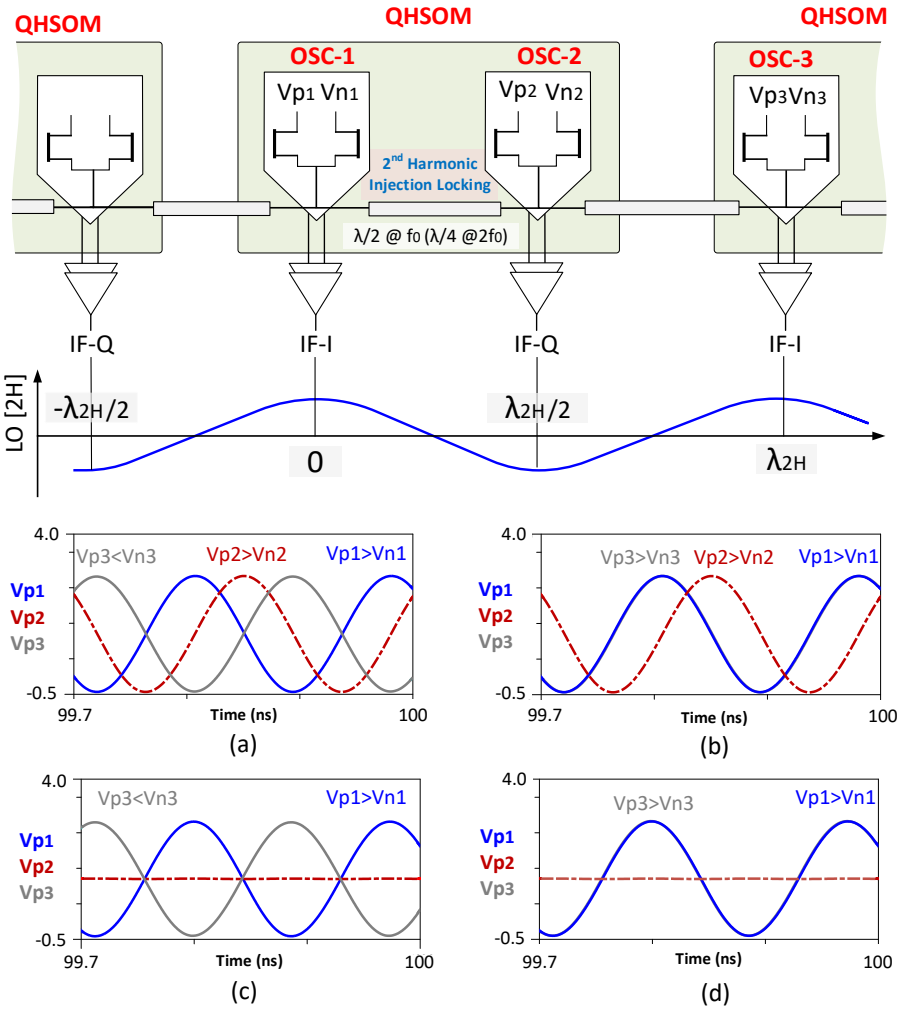

Figure 3.5 Studying the phase sequence control in array of QHSOM in Figure 3.3, with $\Delta V = V_{gg-p} - V_{gg-n}$: (a) $\Delta V_2 > 0, \Delta V_3 < 0$, (b) $\Delta V_2 > 0, \Delta V_3 > 0$, (c) OSC-2: OFF, $\Delta V_3 < 0$, (d) OSC-2: OFF, $\Delta V_3 > 0$.

OSC-1 and OSC-3, after the deactivation of OSC-2, its input impedance variation should not substantially disturb the connection line condition. In Figure 3.4(b), the imaginary part of the input impedance changes by 10Ω, while the real part remains almost unchanged. As shown in Figure 3.4(c), this variation only changes the transfer phase by about 5°, which is far from the ±45° error tolerable margin. Hence, the nominal operation mode is resilient to small variation caused by deactivation of intermediate oscillators and is extendable over multiple sequential deactivated units between active receiver units.

3.3.3 Mixing and Isolation Analysis

High isolation between channels is crucial in a quadrature receiver. Due to the high integration level in a QHSOM, this becomes more challenging. Considering the voltage values in (3.1), odd harmonics (1^{st}, $3^{rd}\dots$) and even harmonics (2^{nd}, $4^{th}\dots$) reside in differential and common mode, respectively. Hence, by injecting the input RF signal in common mode, the output mixing components of each even and odd LO mode retain the LO's original mode. To study the isolation between the I and Q channels, we investigate RF mixing with common mode LO component, particularly the second harmonic as the dominant term. Based on the notation in (3.1) for LO node voltages, and considering the general form of the modulated input RF $V_{RF} = A_{RF}(t)\cos(\omega_{RF}t + \phi(t))$, the non-zero mixing component with the second harmonic at a common node (connection node) is formulated as follows:

$$V_t = A_2 A_{RF} \alpha_2 \cos[(2\omega_{LO} \pm \omega_{RF})t] \tag{3.2}$$

where α_2 is 2^{nd} harmonic mixing coefficient. For the connection node in HSOM-Q, we have $V_{t-Q} = -V_{t-I}$. Since the RF signal is mixed with an identical LO signal but with opposite sign, the mixing product does not create any coupling for either the fundamental or harmonic mixing. The differential output at the load can be expressed as:

$$\begin{aligned} V_{out-I} &= \alpha_i A_i I(t), \\ I(t) &= A_{RF}\cos(\phi(t))\cos[(\omega_{LO} - \omega_{RF})t] \end{aligned} \tag{3.3}$$

$$\begin{aligned} V_{out-Q} &= (-1)^{i-1}\alpha_i A_i Q(t), \\ Q(t) &= A_{RF}\sin(\phi(t))\sin[(\omega_{LO} - \omega_{RF})t] \end{aligned} \tag{3.4}$$

where α_i is the mixing coefficient, and $i = 1$ and 3, for fundamental and 3^{rd} harmonic mixing, respectively. The IF data output resides in differential mode and its polarity can be simply controlled by initial imposed biasing asymmetry in the QHSOMs. There is no information passing through the connection nodes, especially in proximity of the coupling harmonic signal, thereby inherently guaranteeing channel isolation.

3.4 Circuit Design and Operation Optimization

Based on application requirements, technology and operation frequency band, a QHSOM receiver topology can be implemented using various realizations of HSOMs and second harmonic injection locking circuitries. The proposed structure in Figure 3.3 utilizes a differential

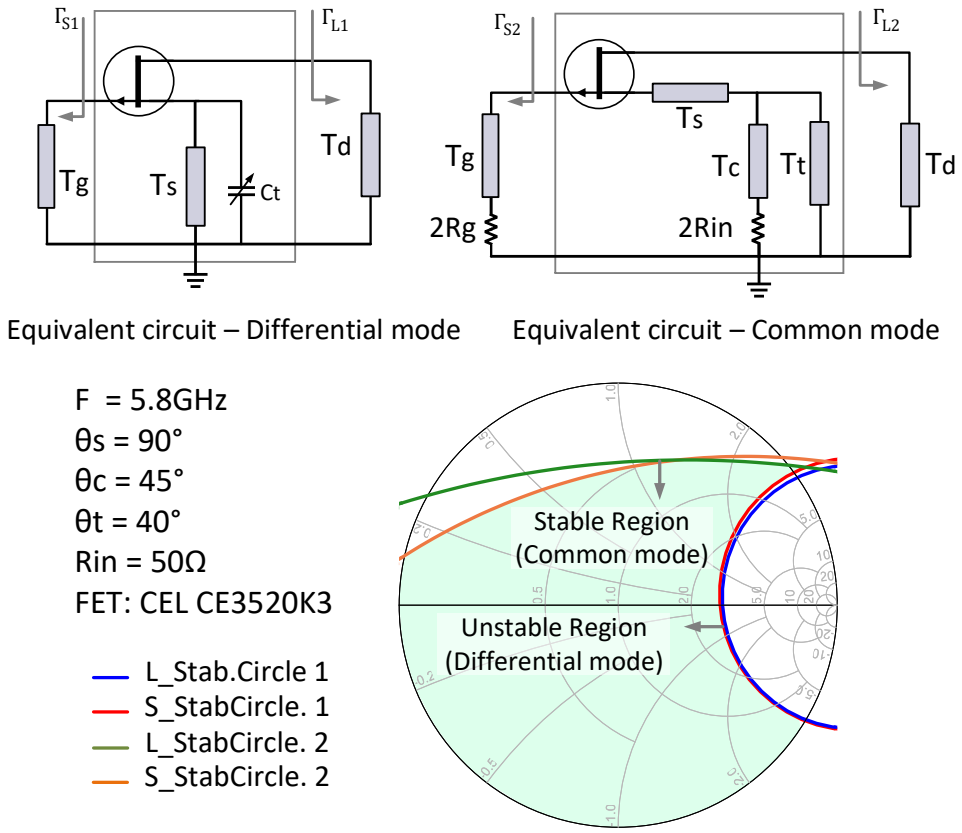

Figure 3.6 Equivalent circuit models for differential mode and common mode oscillation.

microwave oscillator for HSOM, and a TL-based coupling for second harmonic injection locking. Regardless of specific circuitries, two major groups of parameters should be considered for proper operation. The first group addresses oscillation characteristics. Parameters such as strong injection locking, phase noise, frequency tuning, and so on. The second category pertains to the mixing performance of the HSOM as a receiver, including bandwidth, noise figure, conversion gain, and so on.

Oscillator equivalent circuit models for differential and common modes are described in Figure 3.6. The symmetry enforces a virtual short and open circuit in the middle for the differential and common modes, respectively. Stability circuits for these two modes show a large stable area for Γ_s and Γ_L in the common mode, allowing for a flexible selection, while being unstable in the differential mode. Extending the source TL length from 90° to approximately 150° at oscillation frequency (f_{osc}), in addition to the effect of series resistor in the gate and RF port loading, play an important role in stabilizing the common mode. Due to the large unstable area, various combinations of values can lead to oscillation at a particular frequency. As shown in Figure 3.7, a wide range of drain and gate TL lengths can be found for a given

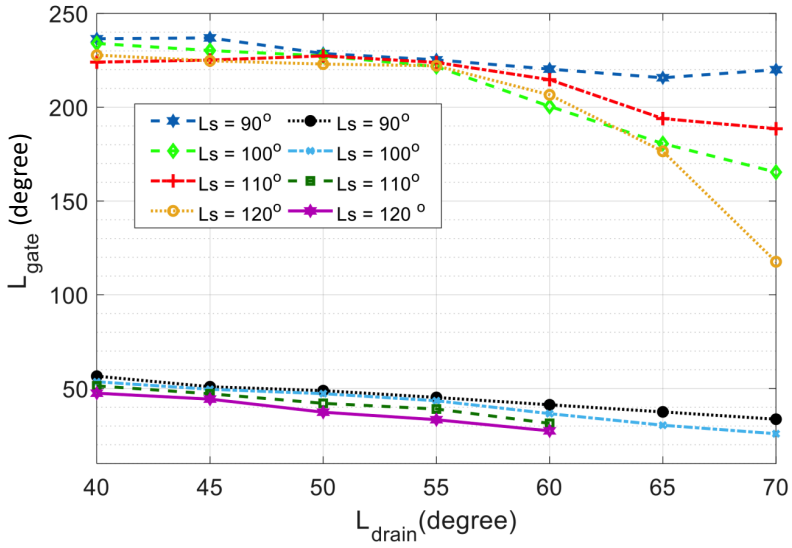

Figure 3.7 Alternative transmission line length choices (T_g, T_s, T_d) for differential mode oscillation at desired oscillation frequency (5.8 GHz).

source TL length within the instability region, all yielding the same oscillation frequency at 5.8 GHz. However, each valid length choice affects other aspects such as oscillation amplitude, harmonic power, mixing performances, coupling strength, and so on. It is worthwhile noting that, due to the periodic nature of input impedance in TLs, two gate TL values are found in Figure 3.7, with a similar function for oscillation. Time domain drain node voltages and their respective spectrum results in Figure 3.8(a) and (b) demonstrate the expected quadrature phase sequence at the oscillation frequency, and the presence of higher order harmonics. The connection node voltages ($V_{t-I/Q}$) in Figure 3.8(d) effectively contain only the second harmonic component, resulting in a 180° phase difference in the steady state, as shown in Figure 3.8(c). In the subsequent subsections, design methodologies for achieving strong harmonic coupling and enhancing mixing performance is discussed.

3.4.1 Second Harmonic Injection Locking

Ensuring an accurate 90° phase shift for the quadrature channel is crucial for optimal receiver performance. The proposed solution addresses this requirement by enhancing the second harmonic injection locking mechanism. To achieve this, the design must: a) generate a strong second harmonic, and b) ensure its availability at the connection points ($V_{t-I/Q}$) for strong locking. The saturation effect is the dominant harmonic generation mechanism in oscillators. Hence, a strong oscillation amplitude directly correlates with higher harmonic amplitudes. With reference to Figure 3.9(a), extracting the Norton equivalent circuit from

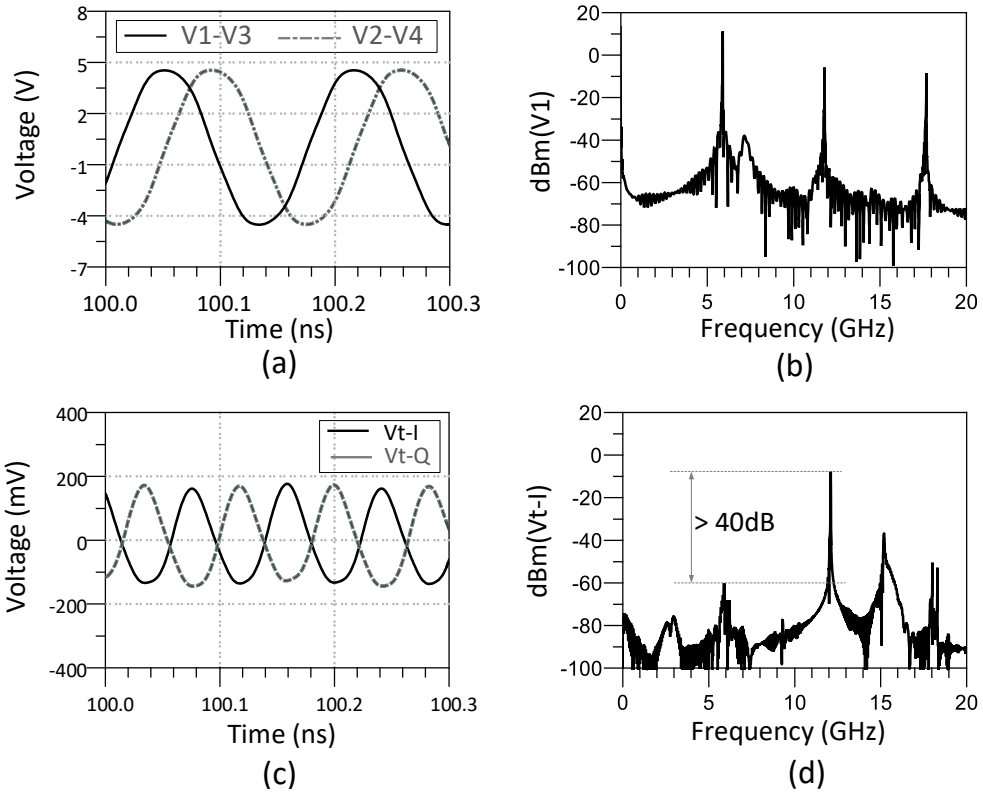

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Figure 3.8 Time domain simulation results for transmission line lengths in Figure 3.6. (a) differential drain node voltages, (b) a drain node spectrum, (c) the connection nodes, and (d) the connection node spectrum.

the transistor's source shows that the equivalent current source is directly related to the harmonic current generated within the transistor, and to optimize the output current, it is essential to short-circuit the drain node at the 2^{nd} harmonic. In an extreme scenario where the drain TL input impedance is infinite ($\theta_d = 45°$ at f_{osc}), satisfying Kirchhoff's Current Law (KCL) at the drain node forces drawing all the current from the transistor, implying that I_{2h} must circulate inside the transistor. This behavior is evident in simulation results as depicted in Figure 3.10. The extracted harmonic current decreases as the drain TL length approaches 45°. The gate TL has a negligible effect on the current, while the source TL length affects the output current by altering the input impedance from the transistor source. Lowering the drain TL lengths ($\theta_d < 25°$) dies the oscillation out. Thus, in the simulation results in Figure 3.10, the drain TL values between 25° to 40° is a viable range. The optimum value from this range is to be determined after including other performance aspects.

Figure 3.11 presents the Norton equivalent impedance for various drain and source TL lengths at the second harmonic. The real and imaginary parts for all sweep values fall within accept-

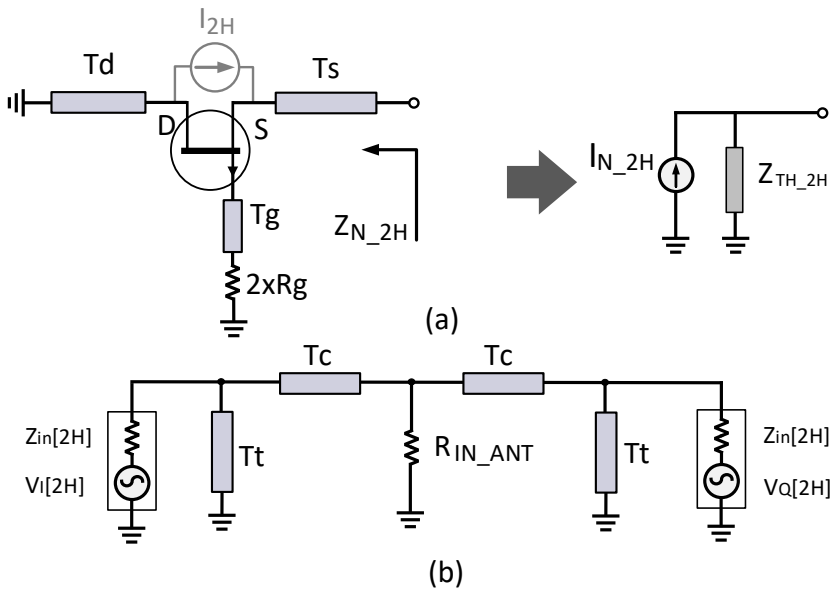

Figure 3.9 (a) Norton equivalent circuit model at 2^{nd} harmonic frequency from transistors' source, (b) connection circuit between I and Q HSOMs.

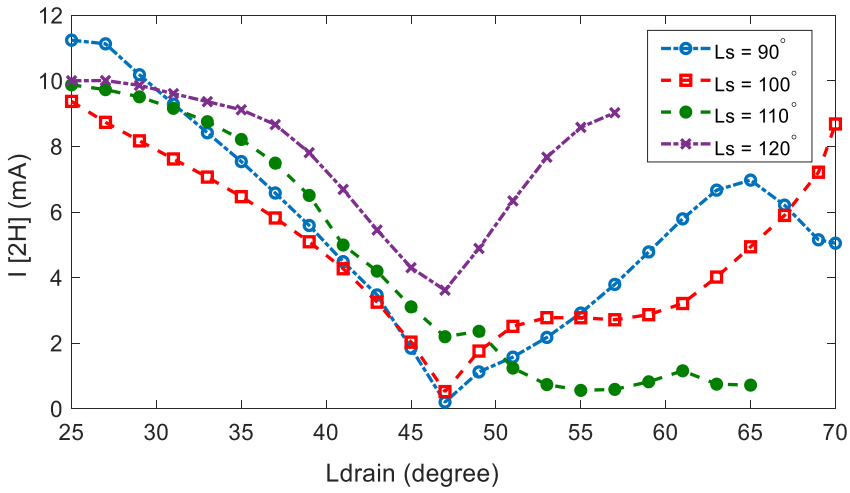

Figure 3.10 Short-circuit (equivalent Norton current source) output second harmonic (2H) current in terms of drain and source transmission line values.

able ranges for matching and compensation purposes. We note that, all simulation results are within the steady state oscillation condition, and simulations are performed using the "Auxiliary source" method outlined in [180]. At steady state, a standing wave gets formed at the connection TL between nodes (V_{t-I}, V_{t-Q}) (Figure 3.5). The equivalent model of the connection circuitry is shown in Figure 3.9(b). The primary requirement involves achieving a close to 180° transfer phase with minimal insertion loss at the second harmonic between the

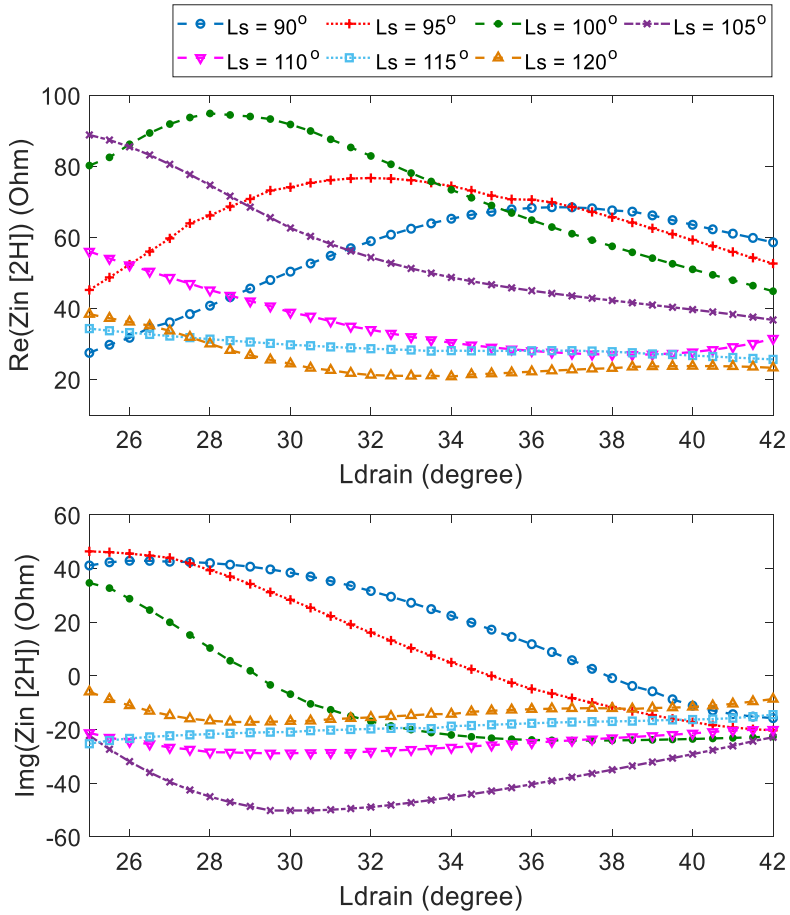

Figure 3.11 Input impedance for Norton's equivalent circuit of HSOM at second oscillation harmonic.

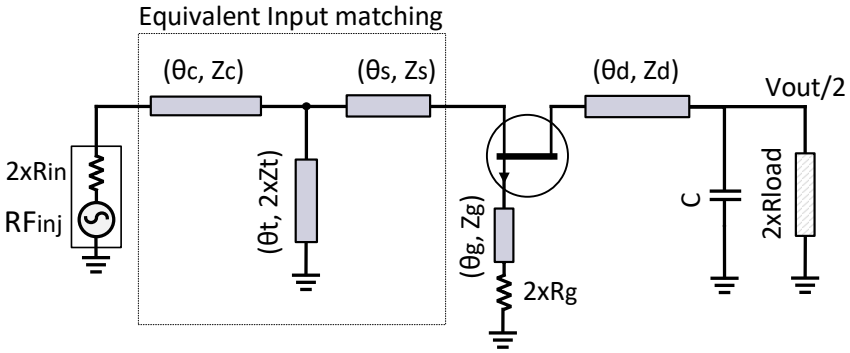

Figure 3.12 Single-ended equivalent circuit model of HSOM as a mixer. Preset values: θ_d=35°, θ_s=115°, θ_g=50°, θ_c=45°, θ_t=45°, R_g=50Ω, C=5pF, R_{load}=200Ω, $Z_{d,g,d,t,s}$=50Ω.

two designated points. Other requirements include maximizing the second harmonic voltage at the nodes by preferably ensuring the input impedance to have a reactance opposite to the

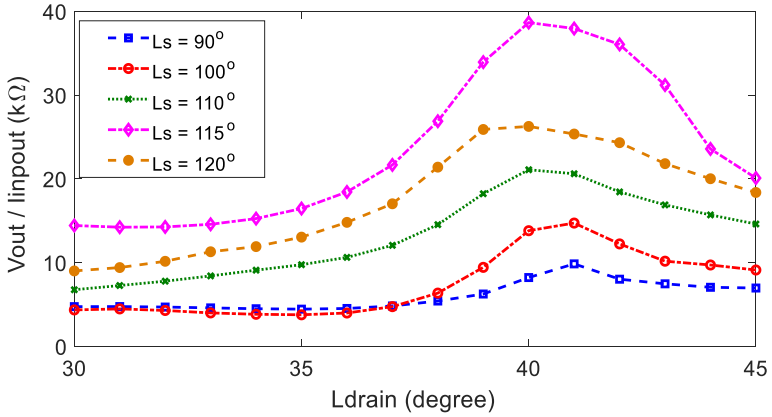

Figure 3.13 3^{rd} harmonic frequency conversion gain in terms of oscillator parameters values. Angle values at LO frequency.

HSOM input reactance as shown in Figure 3.9 ($X_{conn} \approx -X_{in-2H}$). Note that, as shown in Figure 3.12, the connection parts are also part of the input matching network, which directly affects the figure (NF) and input impedance matching requirements. Hence, these two aspects are entangled and should be co-optimized.

3.4.2 Harmonic Mixing and Conversion Gain

To investigate the mixing properties of the presented HSOM in consideration of the RF signal being injected in common mode, the single-ended equivalent model of the mixer resembles a common gate amplifier as depicted in Figure 3.12. As shown, the connection circuit components and the source TL form the input matching network and directly affect the noise figure of the receiver. Figure 3.13 depicts the output IF voltage to input RF current ratio for 3^{rd} harmonic mixing. Using the RF current input removes the effect of the input matching from the study. Increasing the drain TL length strengthens the oscillation and enhances the harmonic power, thereby increasing the conversion efficiency. However, as discussed in the previous section, it is advisable to avoid a drain TL length of 45°. Hence, based on the Figure 3.13 setting $\theta_s = 115°$ and $\theta_d = 30° - 35°$ provides a high mixing performance. We note that the gate TL length varies around 50° and serves as the dependent parameter in the harmonic balance simulation to maintain oscillation frequency at 5.8 GHz.

3.5 Proof of Concept Realization and Discussion

Depending on the technology and application, different differential oscillator cores can be considered for QHSOM realization. A parallel feedback oscillator with an integrated bandpass

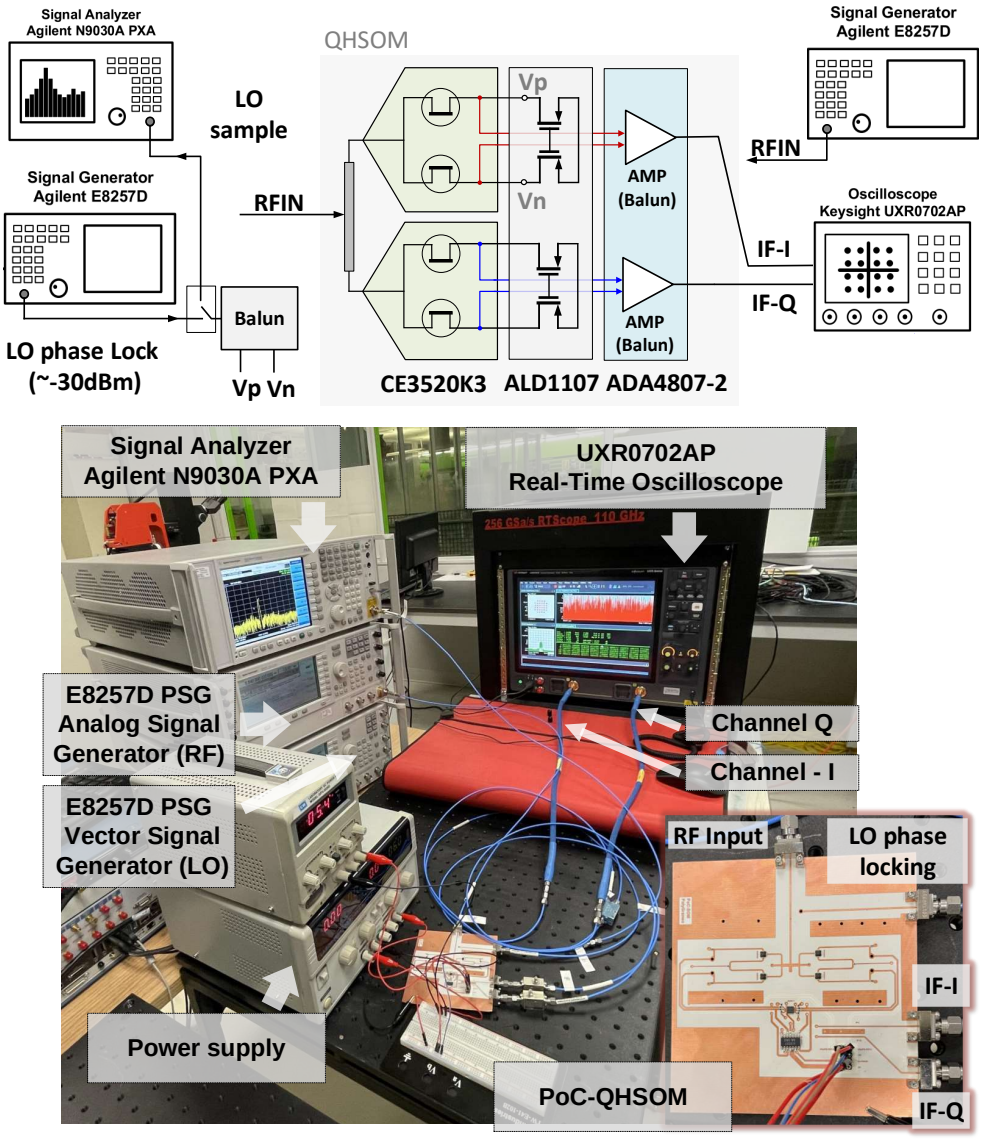

Figure 3.14 Measurement setup and connection block diagram representation.

filter has been incorporated in a previous report [166]. Based on the circuit design considerations presented in Section IV, the following design choices are made. Considering Figure 3.10 and Figure 3.13, the drain TL length $\theta_d = 35°$, and the source TL length $\theta_s = 115°$ are chosen to balance strong injection locking and conversion gain. These values prioritize higher quadrature phase accuracy from strong injection locking over conversion gain. The gate TL length of $\theta_g = 52°$ sets the resonance frequency at 5.8 GHz. All TL lengths are at the oscillation frequency. The bypass capacitor $C = 10pF$ with a differential IF load $R_{\text{load}} = 100\Omega$ provides a 160 MHz IF bandwidth. As shown in Figure 3.14, the IF loads (I and Q) are implemented using a pair of operational amplifiers, both for balance-to-unbalance conversion

Table 3.1 Performance Comparison of the SOA SOM-Based Receivers.

Ref.	**Freq. (GHz)**	**Harm.**	**DC (mW)**	**CG (dB)**	**NF (dB)**	**P1dB (dBm)**	**Technology / Feature**
[171]	5.8	3	32	11.1	6.9	-28	Hybrid / HSOM
[172]	5.79	3	9	11.5	N.A.	-22	Hybrid / HSOM
[174]	1.57	1	5.4	35*	4.8	-31	CMOS / QSOM
[173]	8.3	1	12	11.6	4.4	-13	CMOS / SOM
This Work	17.4	3	16	-8.3	11	-14	Hybrid / QHSOM

*Including IF stage gain.

and amplification. The connection TL and tail TL have two functions: injection locking and input matching for RF signal. Following the analysis of Section II.A, the former imposes the initial values of $\theta_c = 45°$ and $\theta_t = 45°$ TL lengths. To address the noise figure (NF) of the receiver, the parameters in the input matching network, shown in Figure 3.12, have been subjected to optimization. To preserve the already addressed aspects of the design, the following restricted variation around the initial values is considered: $\Delta\theta_s = \pm 5°$, $\Delta\theta_c = \pm 10°$, and $\Delta\theta_t = \pm 15°$. The optimization was conducted based on the method in [180], and the optimized values are as follows: $\theta_s = 115°$, $\theta_c = 41°$, and $\theta_t = 36°$.

The measurement setup and the connection block diagram are shown in Figure 3.14. For receiver performance measurement, to establish a synchronous communication, a weak LO signal of -30 dBm in the monitor read is injected into SOM to set the phase. Its low power, besides its injection in parallel to the LO/RF bypass capacitor in Figure 3.3, ensures its negligible effect on performance. The QHSOM is designed to oscillate at 5.8 GHz and receive at the third harmonic at 17.4 GHz. The modulated RF signal is generated via an E8257DPSG signal generator, and the IF output is measured using an UXR0702AP real-time oscilloscope. The oscilloscope takes separate I and Q channels data and retrieves the respective constellation diagram. In Figure 3.15, the measured constellation diagrams for QAM-16/32/64/128 modulations with 10 MSps data rate are provided. The 70 Mbps data rate in QAM-128 modulation is in accordance with the measured bandwidth in Figure 3.16(a). We note that lower constellation orders have a lower mandate on EVM, hence, as shown in Figure 3.15, a higher data rate in these modulation orders can be achieved at the expense of higher EVM. As shown in Figure 3.16(b), an input power compression point (P1dB) of -14 dBm and conversion gain of -8.3 dB is measured. The free-running phase noise is measured via N9030A PXA signal analyzer. The result is plotted in Figure 3.16(c), showing -71 dBc/Hz phase noise at 1 MHz frequency deviation point. A minimum 11 dB and effective in-band 13 dB noise

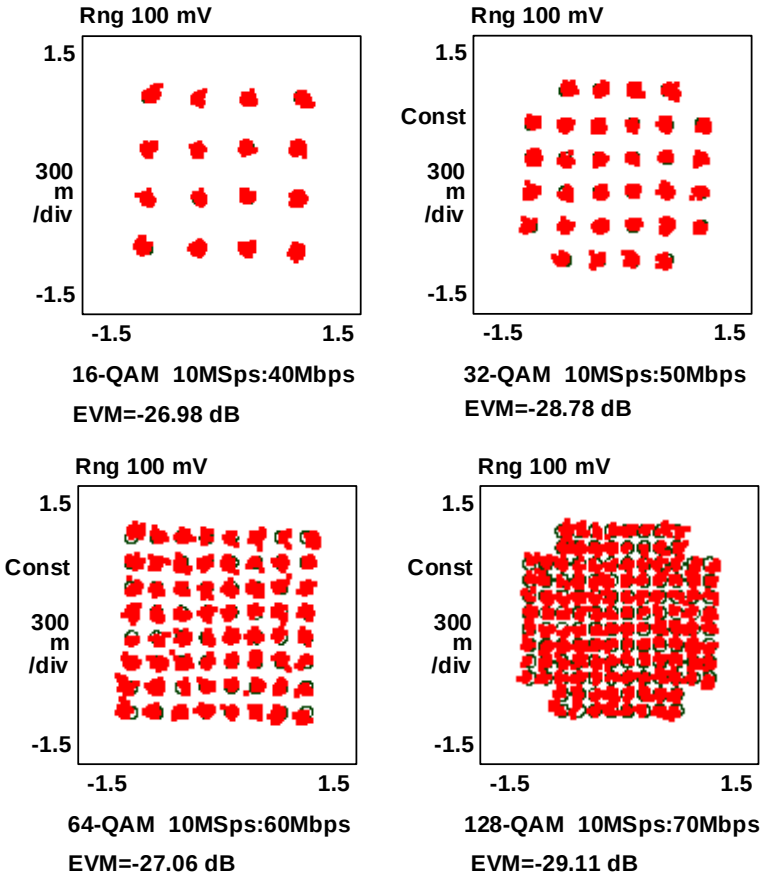

Figure 3.15 Summary of retrieved constellation diagrams with different orders of modulations (M-QAM).

figure (NF) is measured and included in Figure 3.17. Finally, input impedance matching is depicted in Figure 3.16(d).

Table 3.1 compares the presented QHSOM performance with the reported comparable band harmonic self-oscillating mixers in the literature. In comparison, the presented topology surpasses with a high 1dB compression point, mmW realization scalability, and adds quadrature receiving capability to harmonic self-oscillating mixers.

The measurement results within the utilized components and the fabrication technique are found to support the design topology and objectives. Parts like the varactor frequency tuning and complete synthesizer loop are excluded from the PoC to simplify the realization.

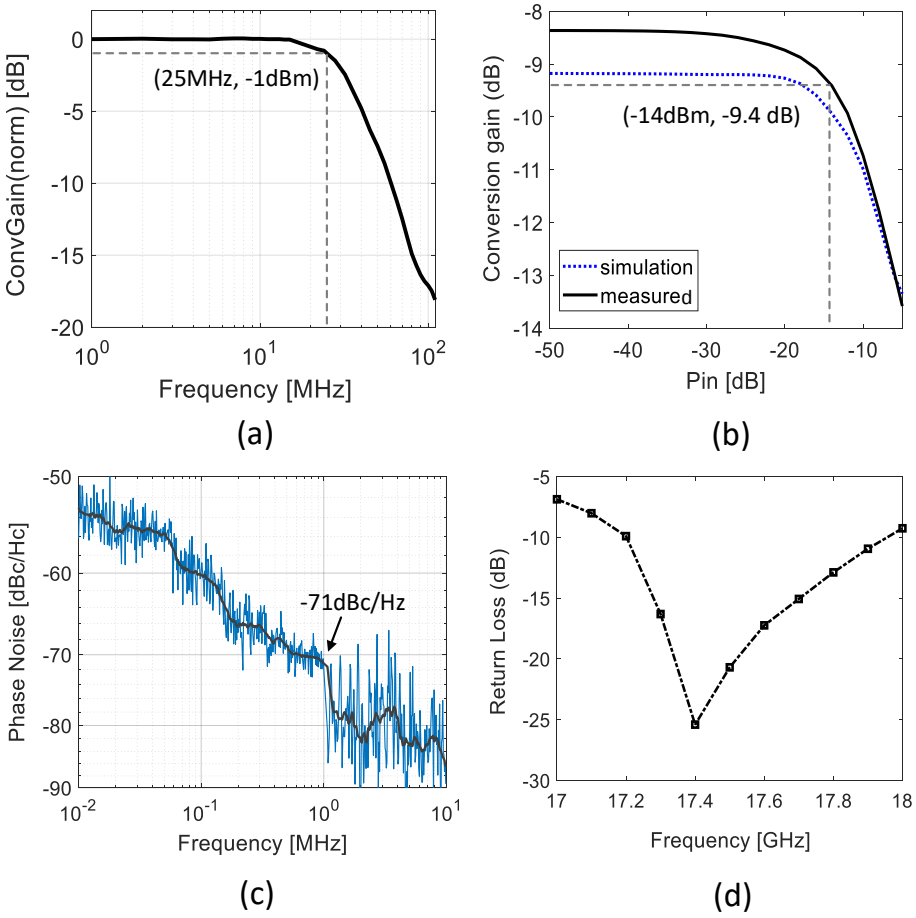

Figure 3.16 Measurement results: (a) bandwidth, (b) 1dB compression point, (c) phase noise, and (d) input impedance matching.

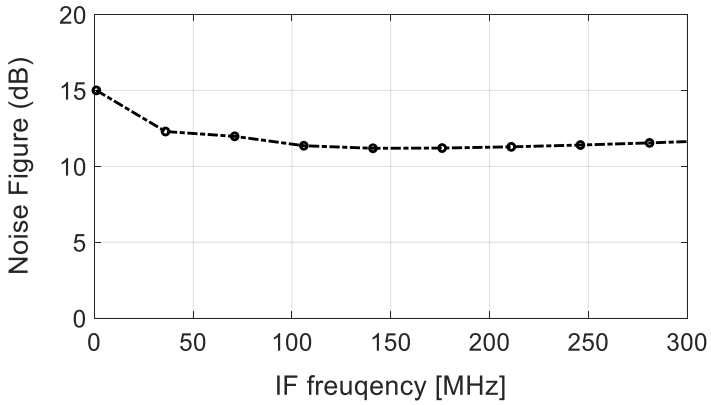

Figure 3.17 Noise figure measurement results.

3.6 Conclusion

In this paper, the concept of a harmonic quadrature receiver based on self-oscillating mixer with direct-conversion topology has been presented and demonstrated for the first time. As the most compact quadrature receiver reported so far to our best knowledge, it provides high performances per consumed power. The nature of super-harmonic coupling allows advantageous features and flexibilities for active array realization in multifunction receivers. Fundamental aspects of its operation such as harmonic coupling and mixing operation have been studied. The experimental prototype implementation for 3^{rd} harmonic reception at 17.4 GHz exhibited compatibility with the presented topology. The scheme is independent of the exact implementation circuitry and other types of HSOMs can be utilized for applications over different frequency bands with performance requirements and available technologies.

CHAPTER 4 DYNAMIC RANGE AND SIZE IMPROVEMENTS OF INTERFEROMETRIC RECEIVERS FOR LARGE ARRAYS

4.1 PART 1: ARTICLE 2: EXTENDING THE DYNAMIC RANGE OF SQUARE-LAW POWER DETECTORS FOR LARGE-SCALE RECEIVER ARRAYS

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Abstract: This paper proposes and investigates a solution to extend the compression point (P1dB) and dynamic range of square-law power detectors. A nonlinear driver stage is incorporated before the detector to compensate for the detector's I-V curve non-ideality, enabling distortion-free mixing over a wider range of input RF signal. The modified MOSFET-based detector demonstration achieves a 14 dB increase in P1dB, raising the baseline from -10 dBm to over 4 dBm while maintaining a bias current consumption of 5 µA. An off-the-shelf BJT proof-of-concept verification shows an 11 dB P1dB extension, reaching 0 dBm. The enhanced performance, combined with its compatibility with integrated circuits (ICs) implementation and low-power local oscillator (LO) requirements, makes it a promising alternative to heterodyne mixers in the development of large-scale receiver arrays for integrated millimeter-wave and terahertz applications.

4.1.1 Introduction

Millimeter wave and terahertz (THz) wireless systems enable high data rate communication and precise sensing. To counter propagation losses and reduced efficiency, large receiver arrays are used, making the performance-to-power consumption ratio of individual receivers crucial for overall array efficiency and feasibility [181], [182]. Mixers operating with switching functions require high local oscillator (LO) power. In large-array systems, the use of multiple mixers and LOs along the RF chain significantly increases both LO power consumption and system complexity. In contrast, employing square-law power detectors—as in interferometric receivers—can lower LO power requirements by approximately 20 dB, offering a more power-efficient solution for large-scale systems [183], [184], [185].

Square-law detectors, however, are constrained by a limited top-end dynamic range (DR), which has traditionally restricted their use in modern commercial applications. Therefore, any improvement in DR is highly desirable, enhancing their suitability for modern

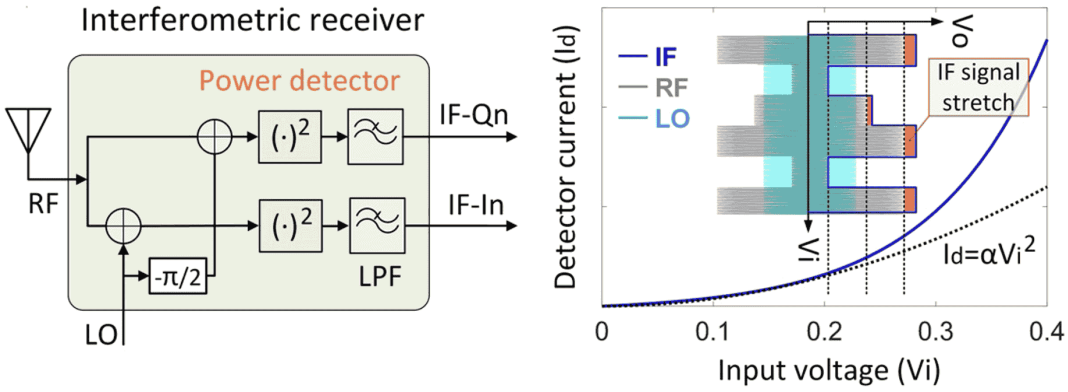

Figure 4.1 Conceptual block diagram of an interferometric receiver and dispersion mechanism representation in the I-V diagram of a square-law power detector.

mainstream systems such as high-data-rate communication and high-resolution sensing systems [186].

Both diode and transistor-based implementations of square-law detectors rely on operation within a well-defined nonlinear region of the device, where the current is proportional to the square of the input voltage [184]. This behavior occurs within a limited region of the I-V curve, and extending beyond it leads to intermodulation distortion (IMD) and harmonic generation, which cause irreversible signal distortion and information loss [184, 187]. In an interferometric receiver, as illustrated in Figure 4.1, the RF and LO signals are combined and fed into the detector. The low LO power results in a limited swing within the square-law region. At higher input RF power levels, the modulated RF swing may exceed the linear region, resulting in distortion. As shown in Figure 4.1, this distortion can be characterized by an expansion at the upper end of the swing. In a communication link, it manifests as a displacement of high-power edge symbols in the retrieved constellation, while center symbols remain unchanged, leading to error vector magnitude (EVM) distortion.

Dynamic range extension techniques can be broadly categorized into advancements in diode technology, and circuit design [188–190]. AlGaN/GaN and tunneling-based diodes have been developed for mmWave and THz applications in [188, 189]. However, implementation cost, and integration issues especially in a large array is prohibitive. Logarithmic amplifiers are integrated with detectors to effectively extend the square-law region [190]. However, the complexity and power consumption of these techniques pose challenges for frequency and array integration. In this work, we propose a compact technique to compensate for top-end distortion and effectively extend the square-law region, thereby enhancing the detector's dynamic range without compromising its compactness or frequency.

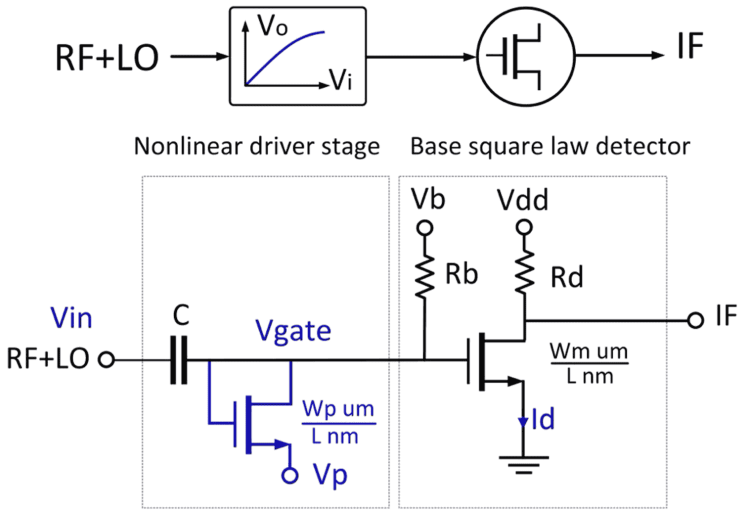

Figure 4.2 Block diagram and circuit representation of the proposed detector with a nonlinear driver stage, Rb = 5K, Rd = 10K, Wp = 1um. Wm = 17um.

4.1.2 Principle of Operation

To mitigate the distortion caused by exceeding the square-law region, as depicted in Figure 4.2, we propose a nonlinear driver stage, with a transfer function exhibiting compression as the input voltage increases. The compression point aligns with the voltage in the detector's I-V diagram where the deviation from square-law behavior occurs. As a result, the compression in the driver stage effectively counteracts the additional amplification observed in the square-law detector.

In the presented solution and demonstration, the driver stage is implemented using a forward-biased parallel diode configuration within its nonlinear region. The voltage Vb is set to bias the detector transistor around its threshold voltage for optimal performance [191], while Vp adjusts the forward voltage value of the parallel diode. The capacitor C acts as an input voltage level shifter, and DC decoupling. For high RF power levels, the high-end voltage swing puts higher forward voltage on the diode, resulting in additional bias current flow through the resistor Rb, which causes a voltage drop at the gate of the detector transistor. Figure 4.3(a) illustrates this effect on the RF voltage. For a small voltage swing of about $0.02V$ (-24dBm) to a higher swing of about $0.5V$ (4dBm), the top-end voltage experiences a compression of $0.3V$. Figure 4.3(b) depicts the I-V characteristics of the resulting detector for various Vp values. At higher forward biasing values, the driver stage induces greater compression on the input signal, resulting in a flatter I-V curve. Conversely, lowering Vp turns off the diode, resembling the detector response without the driver stage.

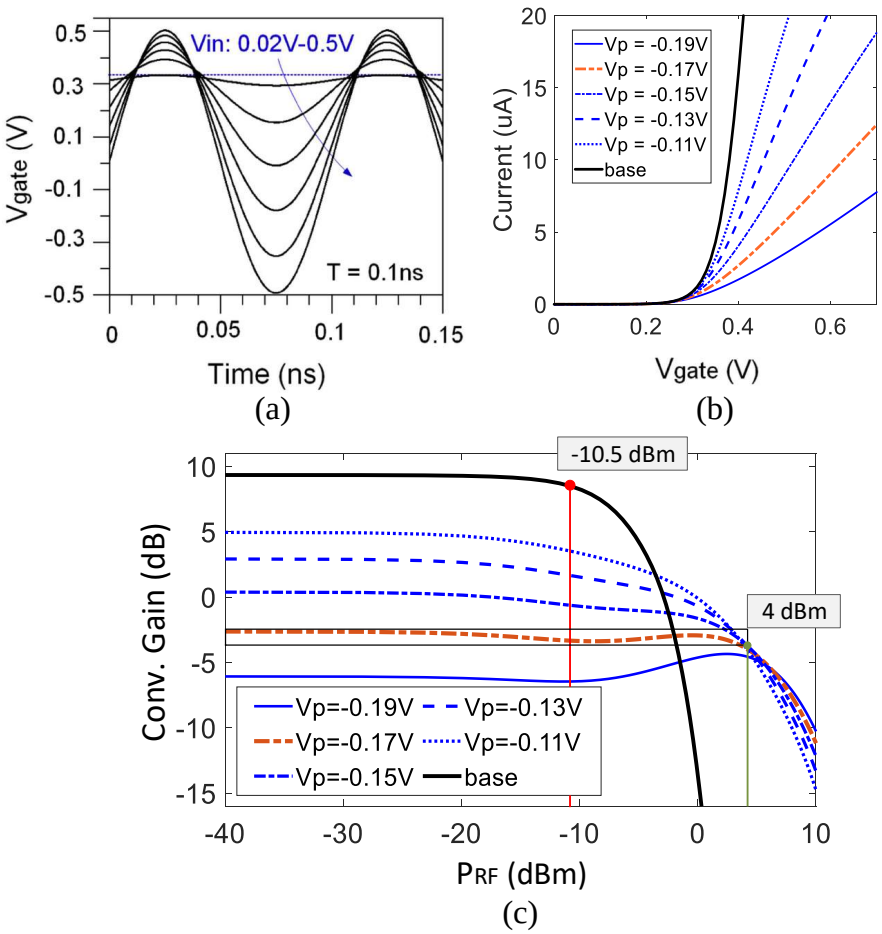

Figure 4.3 (a) Effect of the driver stage to compress the higher end on the input RF signal as a function of amplitude, (b) respective effect on the overall I-V curve of the detector, (c) conversion gain of the proposed detector in Figure 4.2.

The flatness of the I-V curve directly affects the conversion gain(CG) and LO power requirements. Figure 4.3(c) illustrates the resulting CG values corresponding to the I-V curves in Figure 4.3(b). RF and LO signals are operating at 5 and 5.01 GHz, generating IF at 10 MHz. The LO power is held constant at -15 dBm (56mV peak voltage) in the harmonic balance simulation. With increased I-V curve flatness, the square-law region, hence, compression point extends to a higher value. For instance, $Vp = -0.17V$ biasing results in the desired 4 dBm P1dB and -3 dB CG with less than 1dB gain fluctuation criteria. The curve associated with $Vp = -0.19V$ exhibits an overshoot near the compression point, adversely impacting CG flatness. This effect can be mitigated by increasing the LO power, which simultaneously raises the CG value.

Notably, increased flatness in the I-V curve comes with the trade-off of reducing the detector's current, which in turn lowers the CG and practically limits the P_{1dB} extension top-end.

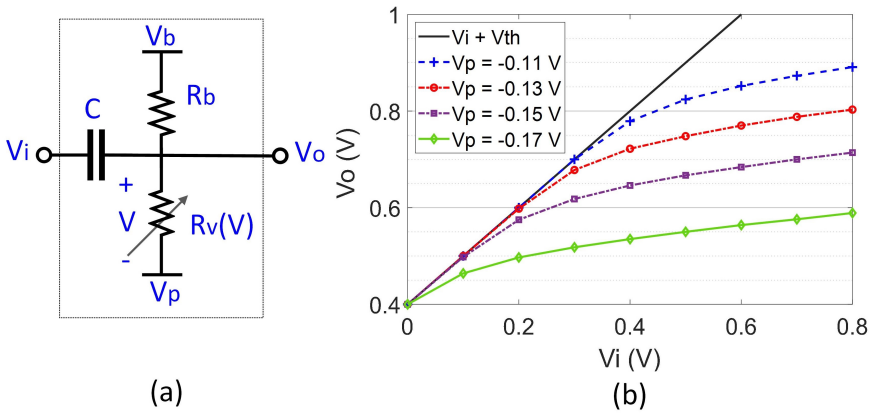

Figure 4.4 The nonlinear driver stage: (a) the equivalent circuit model, (b) the peak RF signal value variation for different bias voltage values.

Excessively low and high CG are undesirable, as they negatively impact sensitivity (due to an increased noise figure) and lead to saturation issues, respectively. Therefore, depending on the available LO input power, CG and bias current requirements, the compression point can be extended. In this work, an LO power of -15 dBm and a bias current of 5 µA resulted in a CG of -3 dB with over 14 dB improvement in the compression point. A high equivalent resistance (R_v) results in only a low 1.5 dB NF degradation from the base detector's 8 dB. Due to the temperature dependence of the threshold voltage ($\Delta V_{th} \approx -2, \text{mV}/^{\circ}\text{C}$), higher temperatures increase nonlinearity and lead to reduced CG.

The equivalent circuit model of the driver stage is shown in Figure 4.4(a). The diode connection is modeled as a variable resistor $R_v(V) = 1/K(V - V_{th})$, where $K = \mu_n C_{ox}(W_p/L)/2$ and V_{th} is the threshold voltage [187]. Solving Kirchhoff's Current Law (KCL) at node V_o, we end up with a second-order ordinary differential equation. Given $V_i = A_i \cos(\omega t)$, and $V_o = A_o \cos(\omega t + \phi) + A_{dc}(A_i)$, and assuming $\omega C >> 1$ we get $V_o = V_i$, allowing us to analytically solve for DC component at the output node. For transistor parameters in Figure 4.2, the result is shown in Figure 4.4(b), where the curves represent the output signal peak value for different biasing condition. The peak voltage level rises nonlinearly with the input signal and can be effectively controlled via biasing. Therefore, based on the circuit model of the nonlinear driver stage and power detector, the explicit relation for the CG can be derived and adjusted for an optimal design.

4.1.3 Experimental Verification

For experimental validation and demonstration, Infineon BFP840F and CEL NE696 RF BJT transistors are used as the driver stage and detector, respectively. The BFP840F transistor

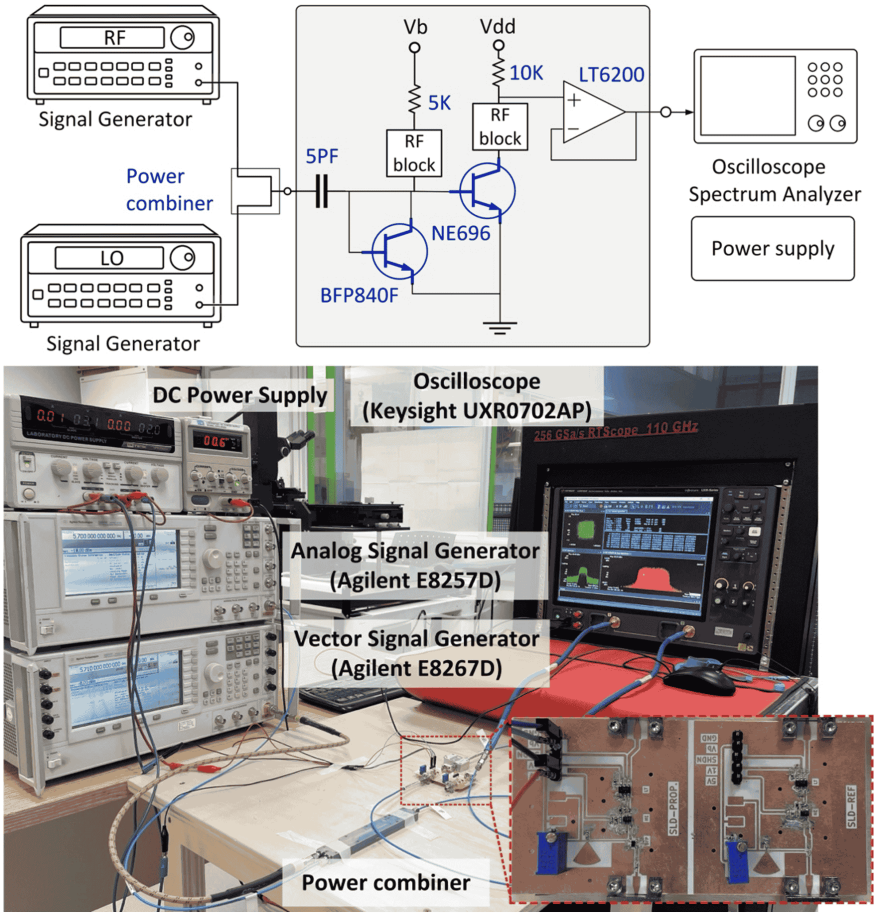

Figure 4.5 The measurement setup.

demonstrates the desired I-V curve behavior, with a lower threshold voltage compared to the NE696 transistor. The variation in current gain (β) in discrete BJTs can lead to implementation inconsistencies. However, the resistance in diode connection is insensitive for available large β values [187]. A buffer circuit, implemented using an LT6200 operational amplifier, is employed to eliminate loading effects from the detectors. For the selected transistor, a bias voltage of $Vb = 0.68V$ and $Vp = 0V$ ensures the desired CG response. Additionally, a reference detector, without the nonlinear driver stage, is designed for comparison and to evaluate improvements in the compression point. To calibrate and account for the impact of non-ideal input matching on the measured P1dB, the measured P1dB is subtracted from the input return loss to determine the actual power injected into the detector.

The measurement setup and block diagram are shown in Figure 4.5. The input LO and RF signals are combined using a Wilkinson power combiner at 5 GHz and 5.01 GHz, respectively, to emulate an interferometric receiver. With a constant LO power, the RF power is swept from -30 dBm to 5 dBm. Then the resulting 10 MHz IF signal is fed to the oscilloscope

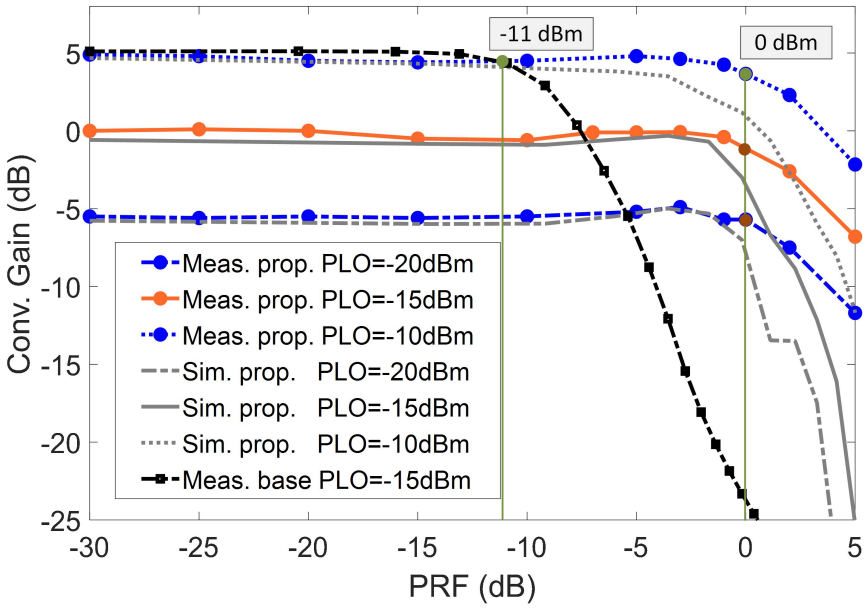

Figure 4.6 Conversion gain versus input RF power for base and proposed power detector configurations.

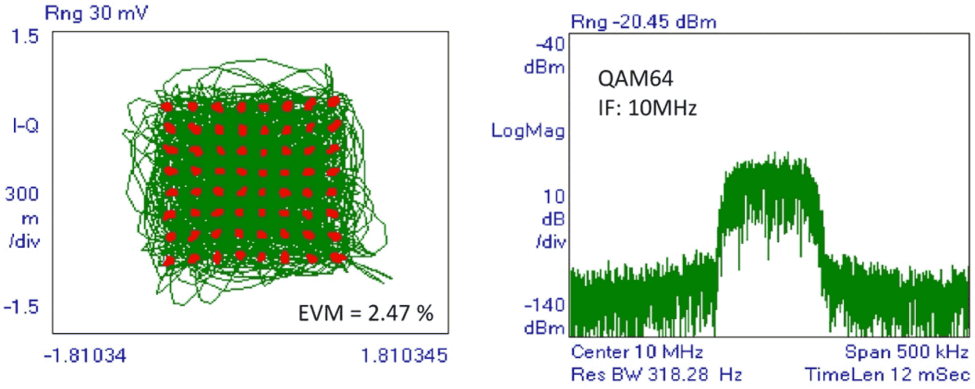

Figure 4.7 Constellation diagram and received IF signal spectrum of an input RF signal with 64-QAM modulation at the compression point of 0 dBm.

to extract the compression point and evaluate the EVM for the target digital modulations. Figure 4.6 shows the conversion gain measurement results compared to the simulation results. Both predict similar compression points at around 0 dBm. The measurement results have a softer landing which we believe is a result of the lower Q factor of the discrete components used and the input matching calibration. The base reference detector circuit shows a 5 dB higher CG with a similar LO power, which is consistent with the simulation results using the MOSFET implementation in Figure 4.2. The proposed technique achieves an 11 dB

improvement.

Figure 4.7 studies the performance of the detector with a modulated RF input signal. A -15dBm LO power, with RF power at P1dB (0 dBm) and 64-QAM modulation, is applied to the receiver. The IF signal spectrum does not expand the signal bandwidth, which confirms the lack of distortion. The constellation is accurately retrieved with a 2.47% EVM. Hence, the modulated input signal supports the lack of compression predicted by the measured CG diagram in Figure 4.6. Table 4.1 provides a comparison with techniques based on specialized detectors and the logarithmic linearization method.

Table 4.1 Comparison with state-of-the-art power detectors.

References	Methodology	P_{1dB} (dBm)	Power Consumption	Frequency (GHz)
[188]	AlGaN/GaN[a]	2	0	2, 5
[189]	InP TB-RTD*	-9	0	340
[190]	Log amp.	-20	0.9 mW	5
This Work	MOSFET/BJT	4	5 μW	5

* Indium phosphide (InP) triple-barrier resonant tunneling diode.
[a] Based on high-electron mobility transistors (HEMTs)

4.1.4 Conclusion

The proposed and demonstrated technique based on nonlinear driver stage has been shown to improve the top-end dynamic range shortcoming of square-law power detectors. A 14 dB and 11 dB improvement in dynamic range has been achieved, reaching 1dB compression points of 4 dBm and 0 dBm for the MOSFET and BJT case studies, respectively. The measurement results confirm the presented theoretical framework. Significant improvement in the compression point, while preserving its nature of low-power detection, IC implementation compatibility, makes the presented detector an ideal candidate to integrate in communication and sensing large-array receivers.

4.2 PART 2: ARTICLE 3: A MINIATURIZED INTERFEROMETRIC RECEIVER FOR DENSELY INTEGRATED LARGE ARRAYS

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Abstract: This paper proposes and demonstrates a small-footprint interferometric six-port receiver unit developed for large-scale active receiver arrays. The proposed architecture integrates three Lange couplers with a miniaturized Wilkinson power divider and power detectors' matching networks, achieving an exceptionally compact footprint of $0.22\lambda \times 0.45\lambda$. The proof-of-concept prototype operating at 5.6 GHz demonstrates a 3 GHz six-port junction bandwidth and supports a data rate of 200 Mbps, validating the anticipated performance. The introduced compactness, along with the inherent low local oscillator (LO) power requirement, and integrated circuit (IC) compatibility, makes the proposed receiver an excellent candidate for high frequency and power-efficient large-scale receiver arrays.

4.2.1 Introduction

Large-scale arrays in multi-input multi-output (MIMO) or phased array configurations offer distinct advantages, including beamforming, enhanced channel security and capacity, and multi-functionality, making them essential for next-generation RF/millimeter-wave (mmWave) 5G and 6G wireless communication, and terahertz (THz) sensing applications [192]. The array size at these frequencies is practically constrained by power consumption, which introduces challenges such as heat dissipation and increased system complexity. Thus, low-power transceiver units integrated within active array architectures have garnered significant interest [193], [194].

In large-scale active receiver arrays, the LO signal becomes a major contributor to overall power consumption. For instance, the widely adopted mixer-first receiver (RX) topology at mmWave and THz frequencies typically requires 8 dBm of LO power per mixer [195]. In a 32×32 array, this requirement translates to a total LO power of 6.45 watts (W). Considering a state-of-the-art power added efficiency (PAE) of 15% at 140 GHz [196], the corresponding DC power ramps up to 43 W. Alternatively, interferometric receivers (IFRX), as illustrated in Figure 4.8, utilize square-law power detectors that operate with substantially lower LO power of -20 dBm to -10 dBm. Implementing the same 32×32 array using IFRX units with -15 dBm LO power reduces the total LO power to merely 32 mW, and DC power to only 215 mW, demonstrating a $\times200$ reduction in power consumption. These advantages have renewed

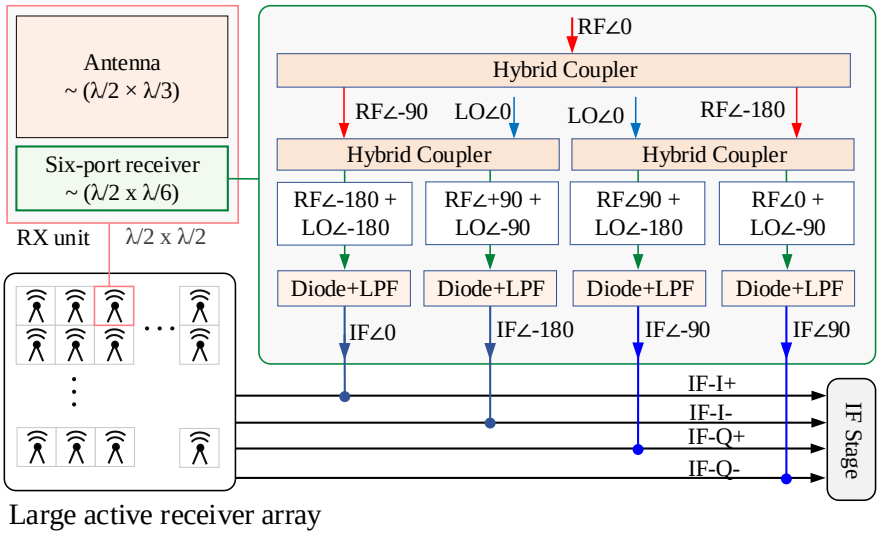

Figure 4.8 Illustration of large receiver array using interferometric unit cells.

interest in IFRX development for large arrays, particularly to address dynamic range [197] and multifunctionality [193] limitations.

Despite advantages, IFRX typically occupy a multi-wavelength (λ) footprint, making them unsuitable for integration into large-scale arrays. Compact lumped-element-based solutions have been reported [198,199]; however, their operation is limited to low frequencies. Existing transmission line based compact IFRX realizations often overlook the integration of power detectors and matching networks and generally occupy a major portion of the array unit cell [200, 201]. In this work, we propose and demonstrate an IFRX solution based on Lange coupler, featuring an area-efficient layout that occupies less than 30% of a standard $0.25\lambda^2$ unit cell. The proposed solution is compatible with standard PCB fabrication processes and is directly scalable for integrated circuits (IC) implementation in mmWave and THz band applications using commercial processes such as CMOS.

4.2.2 Interferometric Receiver Design

Amongst various six-port and multiport receiver topologies, the configuration shown in Figure 4.8 is adopted to maintain symmetry and exploit the compactness of the Lange coupler. The IFRX consists of three Lange couplers, a Wilkinson power divider (WPD), and diode matching networks. The following subsections outline the design process for each part.

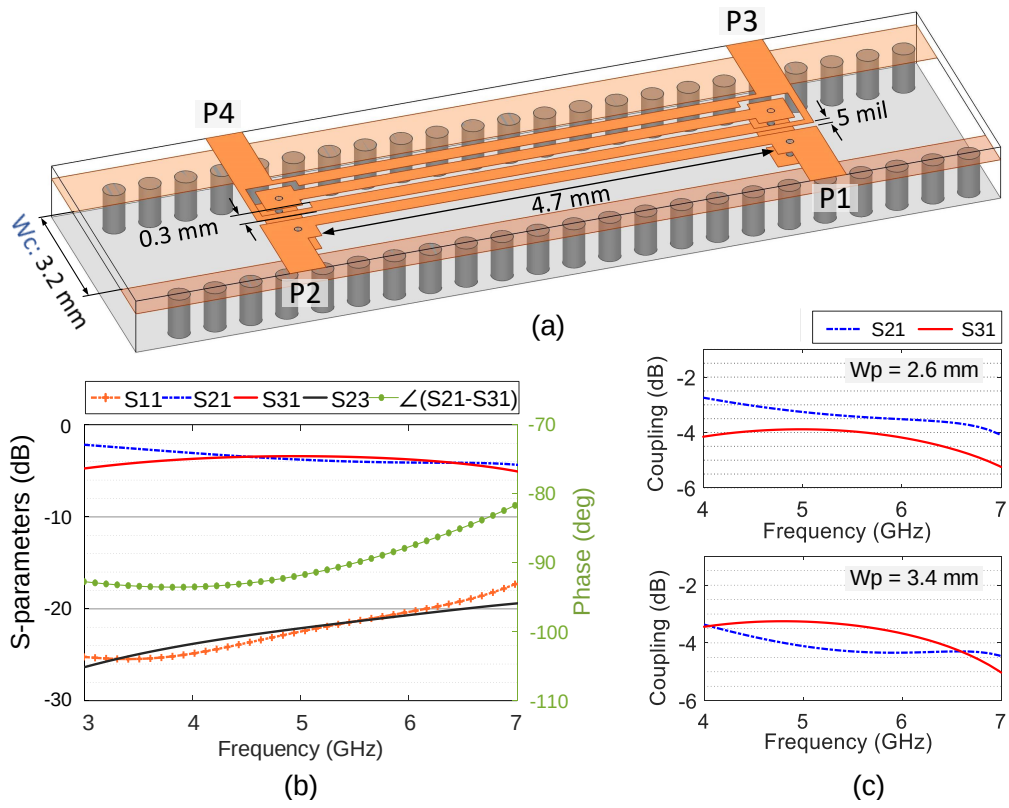

Figure 4.9 The proposed Lange coupler: (a) Layout, (b) S-parameter results, (c) Effect of transverse cavity width (W_c) on coupling strength.

4.2.3 The Proposed Lange Coupler

The unfolded Lange coupler, shown in Figure 4.9(a), is selected for its structural simplicity and compact form factor. Originally introduced for integrated circuit (IC) integration due to its compact design [202], the Lange coupler features narrow trace widths and spacings that are well-suited for MHMIC and IC fabrication technologies. However, to achieve the required coupling while adhering to PCB fabrication rules—including a 10 mil via pad and 5 mil minimum line width and spacing—a stack of two Rogers RO3003 substrates (ε_r= 3), with thicknesses of 10 mil and 30 mil is used. The jumpers in the Lange couplers are implemented using metallized vias that connect Layer 1 to Layer 2, ensuring a minimal connection length.

The coupler dimensions and corresponding full-wave simulation results are shown in Figure 4.9(a) and (b). The design achieves a bandwidth exceeding 3 GHz, centered at 5.6 GHz, with a maximum phase deviation of 5° between the output ports. Additionally, it maintains input matching and channel isolation better than −20 dB at the RF and LO ports. The

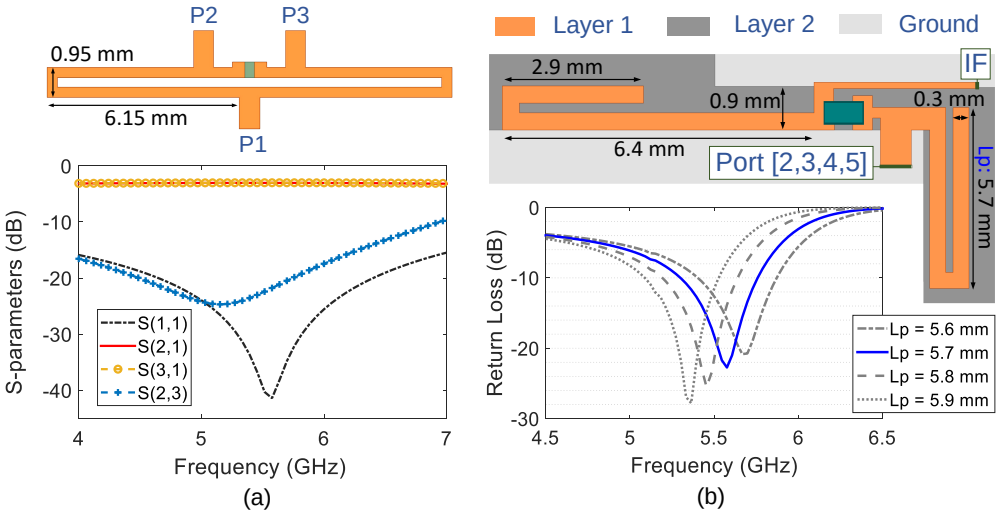

Figure 4.10 (a) Layout and S-parameters of the Wilkinson power divider, (b) Compact single-stub matching network (port names corresponding to Figure 4.11).

via rows in the bottom substrate form a cavity in the transverse direction and are essential in providing isolation between the Lange couplers in the compact layout. As illustrated in Figure 4.9(c), the spacing between the via rows (W_c) directly affects the coupling behavior of the Lange coupler. This structure can be modeled using the well-studied coupled lines in a grounded coplanar waveguide (GCPW) configuration, where a narrower spacing reduces coupling strength, while the effect diminishes as the spacing increases [203]. In the proposed design, a spacing of $W_c = 3.2$ mm achieves a practical coupling balance.

4.2.4 Interferometric Receiver Layout

The layout of the proposed IFRX is shown in Figure 4.11. Three Lange couplers are employed to generate the required RF and LO phase distributions (Figure 4.8). A single-stage compact Wilkinson Power Divider (WPD), shown in Figure 4.10(a), is used to distribute the LO signal, providing the required wide bandwidth while ensuring isolation between the two couplers.

A key and distinguishing feature of the proposed compact design is the integration of matching networks required for the power detectors. Asymmetry and impedance mismatch at the detectors lead to reflections of the RF and LO signals within the six-port network, resulting in phase and amplitude imbalances in the output intermediate frequency (IF) signals.

A power detector diode can be modeled with an RLC equivalent circuit. The zero-biased configuration exhibits a low input resistance ($R < 10\,\Omega$), while the input reactance varies with frequency, transitioning from capacitive to inductive behavior. The low resistance leads to

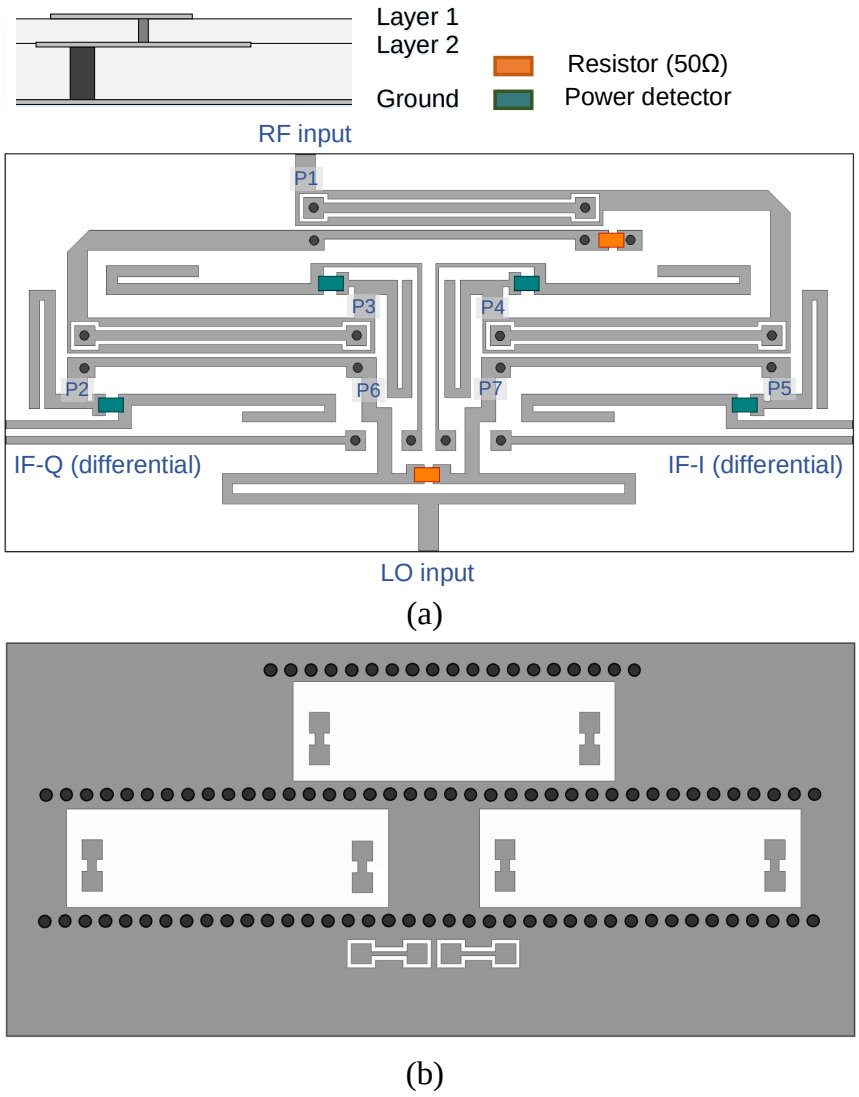

Figure 4.11 Layout of the proposed compact interferometric receiver; (a) layer 1 (top), (b) layer 2 (middle).

a narrowband matching, posing challenges for broadband integration. This issue can largely be mitigated by transistor-based square-law detectors [197, 204]. In this work, SMS7630 Schottky diodes are utilized, showing $R_{\text{in}} = 6\ \Omega$ and $C_{\text{in}} = 4.5$ pF at 5.6 GHz, resulting in $Z_{\text{in}}(\Omega) = 6 - j70$. As shown in Figure 4.10(b), a single-stub matching network is considered and placed on the two sides of the Lange couplers (Figure 4.11(a)). To ensure symmetry in the matching network layout between ports 2 and 3 (and similarly between 4 and 5), the matching open-stub and 90° RF-blocking transmission lines are placed at the edge of the layer 2 metal, serving as their partial ground planes (Figure 4.10(b)). Owing to thin 10 mil top substrate, a ground plane extension of just 0.6 mm from the track edge is sufficient to

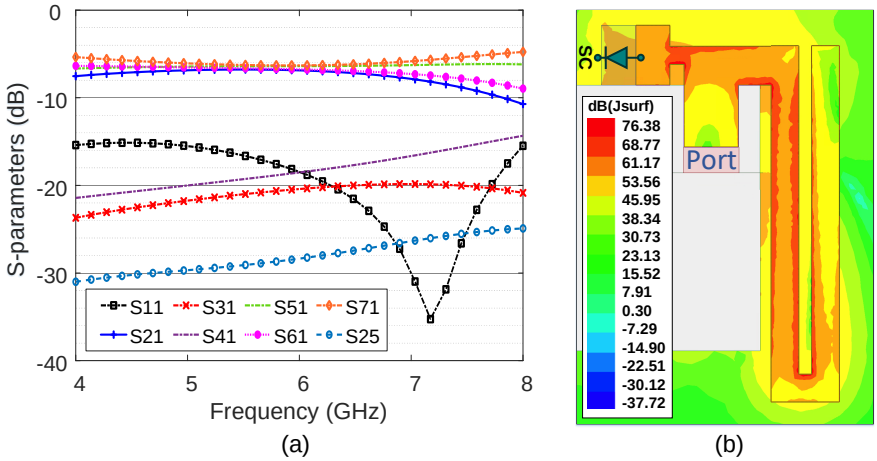

Figure 4.12 (a) S-parameters of the six-port junction of Figure 4.11, (b) heat map of the matching stub surface current, illustrating current confinement.

behave as a continuous plane.

The S-parameters of the resulting six-port junction, obtained from full wave simulations in Ansys-HFSS, are presented in Figure 4.12(a). The results indicate input matching better than -15 dB, port isolation between the I and Q channels exceeding -25 dB, and efficient RF power division across the 4 GHz to 7 GHz frequency range.

The surface current distribution on the matching stub is shown in Figure 5(b), illustrating that the majority of the current is concentrated along the internal leg, with minimal propagation on the ground plane (Layer 2). This ensures high isolation between adjacent lines. This stems from the use of a thin top substrate, which minimizes the impact of meandering on impedance reduction and effective electrical length, and reducing coupling between the WPD lines, enabling a narrower gap and improved compactness.

4.2.5 Experiment Results and Discussion

For experimental validation and demonstration of the proof-of-concept prototype, SMS7630 Schottky diodes are used for power detection. The measurement setup is illustrated in Figure 4.13. RF and LO signals with carrier frequencies of 5.6 GHz and 5.4 GHz respectively, are generated using an Agilent E8257D analog signal generator and an E8267D vector signal generator. The single-ended in-phase and quadrature IF outputs are fed to Keysight UXR0702AP oscilloscope for constellation formation and error vector magnitude (EVM) calculation.

For input RF signals modulated with 16-QAM and 256-QAM schemes, symbol rates of 50

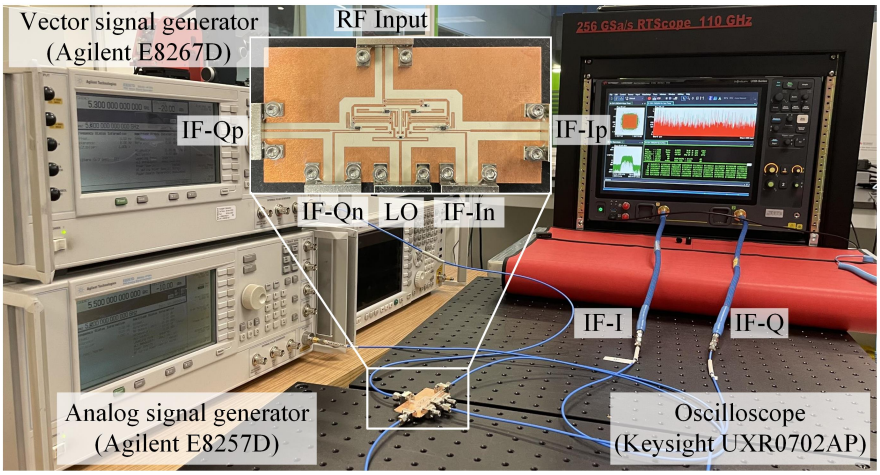

Figure 4.13 Measurement setup.

Table 4.2 Receiver's measured performance parameters.

Sensitivity (BW: 10 MHz)	-57 dBm
1dB compression point (P1dB)	-15 dBm
Weakest detected signal	16-QAM: 50 MSps, EVM: 7.9% 256-QAM: 5 MSps, EVM: 1.6%

Table 4.3 Comparison with the SoA compact interferometric receivers.

Ref.	BW/f_0 (GHz)	Data rate	W/λ × L/λ	Core Component
[201]	3 / 7.5	500 Mbps	1.22×1.36*	Branch-line coupler
[198]	0.6 / 2.4	40 Kbps	0.44×0.32*	Lumped element
[200]	2 / 25.5	850 Mbps	1.61×1.45	Wilkinson pwr. comb.
[205]	1 / 2.5	15 Mbps	0.83×1.25	Branch-line coupler
[206]	4 / 28	1.6 Gbps	3.73×3.31	Metal WG + SIW
[207]	8 / 24	30 Mbps	6.09×2.63	SIW pwr. comb.
This Work	**3 / 5.5**	**200 Mbps**	**0.22×0.45**	**Lange coupler**

* Without power detector and matching circuit integration.

MSps and 5 MSps were successfully retrieved, achieving EVM values of 7.9% and 1.6%, respectively. These results are comparable to those reported in [208], where the interferometric receiver features the same power detectors and prototyping technology, but utilizes an ideal receiver layout. The corresponding constellations, shown in Figure 4.14, are obtained without any post-processing. The ideal balance between I and Q channels demonstrates accurate

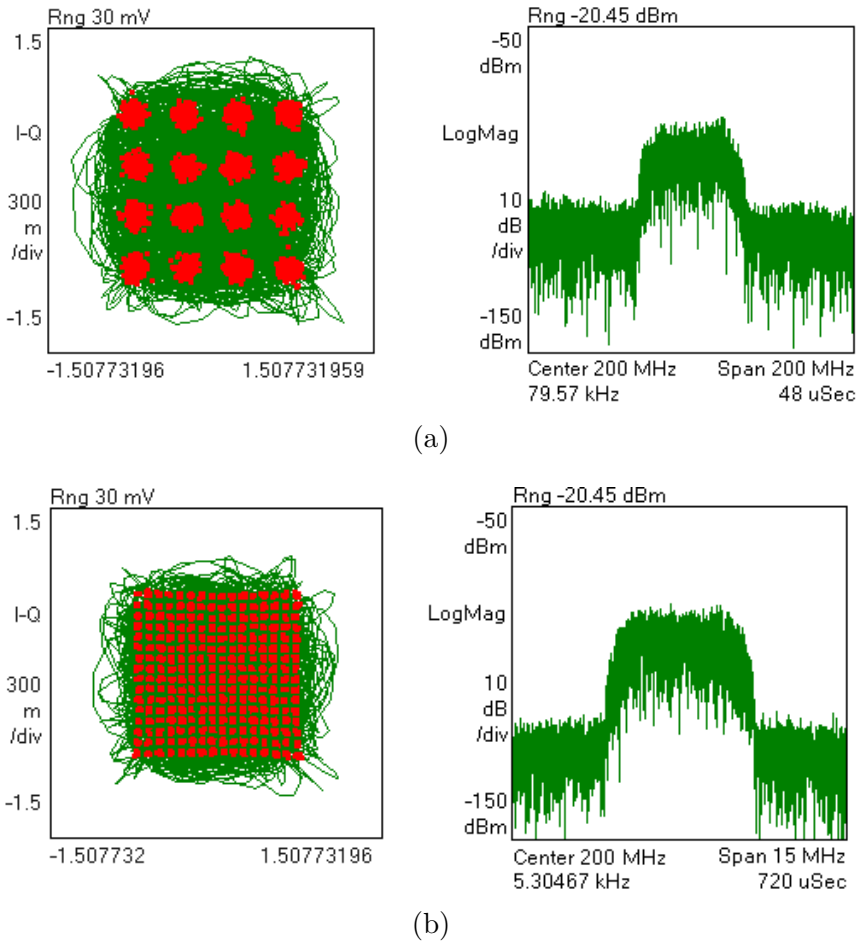

Figure 4.14 Measured constellation and related spectrum diagram of modulations: (a) 16-QAM, (b) 256-QAM.

quadrature phase alignment and equal amplitude division, confirming the performance of the proposed interferometric receiver. Additionally, the clean spectra corresponding to both constellations confirm the absence of distortion in the detector outputs in retrieving the transmitted data rates. The measured performance parameters are summarized in Table 4.2, reporting nominal operation parameters for the power detector [208].

A comparison with compact interferometric receivers reported in the literature is presented in Table 4.3. The footprint of the proposed solution is comparable to that of the lumped-element-based technique in [198]. Notably, the reported sizes for the transmission line-based techniques exclude the power detector and its matching network integration within the receiver, whereas included in the proposed design.

4.2.6 Conclusion

The proposed interferometric receiver unit, demonstrated using standard lithography design rules, achieves a 55% six-port junction bandwidth ranging from 4 GHz to 7 GHz, delivering performance comparable to that of optimal-layout, large-footprint counterparts. Th receiver occupies a compact footprint of 12mm×25mm, corresponding to $0.22\lambda \times 0.45\lambda$ at 5.6 GHz. Its high integration and compact form, along with compatibility for IC implementation, makes it a strong candidate for large array and low power applications.

CHAPTER 5 ARTICLE 4: A SCALABLE LARGE ARRAY M-QAM DIRECT-RF TRANSMITTER TOPOLOGY WITH INTEGRATED PHYSICAL LAYER SECURITY—A PROOF OF CONCEPT

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Abstract: This article introduces a transmitter array topology that employs QPSK direct-RF transmitter (TX) units for realizing scalable large-array wireless communication and multifunction systems. By leveraging spatial power combination, the TX units are set to synthesize an extended M-QAM constellation, enabling flexible and high-order modulation. The QPSK modulation, when transmitted in an array, bolsters physical layer security by confining the constellation retrieval to the intended radiation angle exhibiting high selectivity. Additionally, its low dynamic range waveform supports high-power output and improves the efficiency of power amplifiers compared to higher-order constellations, thus significantly enhancing the array's overall power-performance ratio. A comprehensive analysis is conducted on key performance factors, including location-dependent antenna gain variations, beamforming effectiveness, and phase front flatness. To validate the proposed technique, a 2×4 array proof-of-concept (PoC) implementation is presented. Measurement results demonstrate robust performance across modulation orders ranging from 16-QAM to 256-QAM, aligning with theoretical predictions. This topology effectively integrates spatial constellation formation with the requirements of large-array systems, offering superior power efficiency. Its scalable building blocks, reconfigurability, and inherent secure communication capabilities make it a strong candidate for next-generation high-data-rate large-array transmitter systems.

5.1 Introduction

Over the past few decades, wireless technology has undergone significant advancements, driven by the increasing demands of our information society for higher data rates, lower latency, greater capacity, and intelligent connectivity. The evolution of fifth-generation (5G) and beyond 5G (B5G) wireless communication technologies are geared to establish a framework for high-speed, low-latency, and secure communication [209–214]. In this context, large-scale transmitter arrays are expected to be pivotal in future millimeter-wave (mmWave) and terahertz (THz) wireless networks. However, conventional transmitter architectures struggle

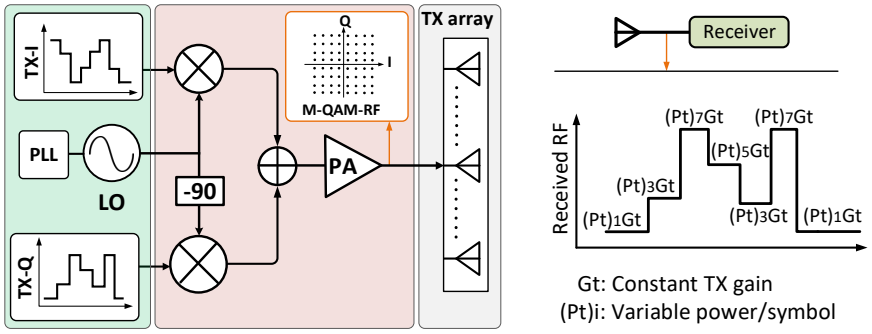


Figure 5.1 Illustration of a conventional transmitter array.

to meet these stringent demands due to inherent limitations in power and computational resources. Consequently, innovative solutions are required to redefine mmWave and THz transmitter designs through integrating specialized architectures for multi-functionalities, such as data communication, parametric sensing, and imaging.

A conventional modern transmitter array topology is illustrated in Figure 5.1. Digital-to-analog converters (DACs) and power amplifiers (PAs) are two essential components and major sources of power consumption. High-speed DACs can consume up to one watt of power, and the cumulative consumption of PAs in millimeter-wave (mmWave) and terahertz (THz) arrays can reach impractical levels, increasingly causing heat dissipation complexities [215–222]. In particular, to ensure distortion-free operation, a power amplifier (PA) must operate with a back-off from its peak efficiency and maximum output power, by an amount proportional to the dynamic range (DR) of the transmitted signal. Although DAC and PA designs have significantly been matured over the years, addressing the power consumption challenge in large arrays requires alternative solutions at the architectural level to achieve practical efficiency without sacrificing performance.

The direct-RF technique is employed in mmWave high-data-rate communication to eliminate the DAC from the transmitter chain, where a modulator directly controls the phase, amplitude, or frequency of the carrier signal (LO) through switching action [223–234]. Low-order modulations such as ASK, BPSK, and QPSK have been commonly implemented [223, 224]. However, scaling up the modulation order to improve spectral efficiency without substantially increasing system complexity remains a challenge. Two QPSK signals with different power levels (1, 1/4) are used to generate a 16-QAM constellation. However, extending this technique to a 4^N-QAM scheme requires combining N transmitters operating at progressively scaled power levels (1, 1/4, 1/16, ...), which introduces significant calibration challenges in accurately realizing the required voltage levels—particularly at mmWave frequencies. An array of TX units harnesses a fundamental switching function and polarization orthogonality

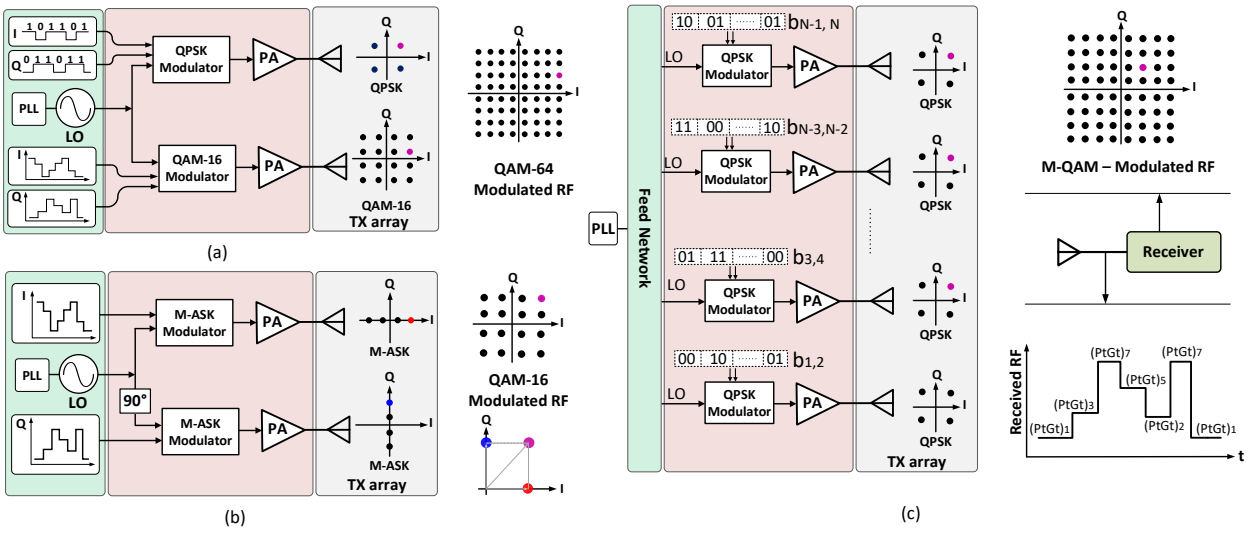


Figure 5.2 Transmitter topologies based on spatial power combination. (a) Combination of QPSK and 16-QAM TX units. (b) Combination of two M-ASK TX units. (c) The proposed distributed topology based on an array of identical QPSK TX units.

to generate higher-order Spatially Orthogonal ASK (SO-ASK) modulation [229]. The simplicity of the transmitter units enables scalability in both frequency and array size. However, this approach necessitates a custom receiver and, despite leveraging dual polarization, results in a higher error vector magnitude (EVM) requirement for a constant data rate compared to conventional QAM or similar modulation schemes.

The proposed technique, as conceptually shown in Figure 5.2(c), employs the collaborative operation of identical TX units using direct-RF QPSK modulation within an array to synthesize higher-order M-QAM modulation over the air. QPSK, being the simplest form of quadrature modulation, requires relatively simple modulator circuitry and offers a low peak-to-average power ratio (PAPR). Figure 5.3 presents a time domain illustration of compression effect at higher-order constellation symbols. Typically, a PA has to be designed to remain linear up to the maximum symbol power, which increases with the constellation order. In the proposed topology, however, when transmitting QPSK signals, each PA operates near its compression region, effectively enhancing the achievable output power and efficiency. To study the effect of PAPR on PA's power consumption, Table 5.1 presents two PAs operating at 140 GHz and delivering similar output powers—one transmitting QPSK and the other 1024-QAM modulation. The latter requires approximately 10 dB extra output back-off compared to QPSK, necessitating a design with a 10 dB higher output 1dB compression point (OP1dB) [235, 236]. This leads to a 5 times increase in power consumption. In a 10×10

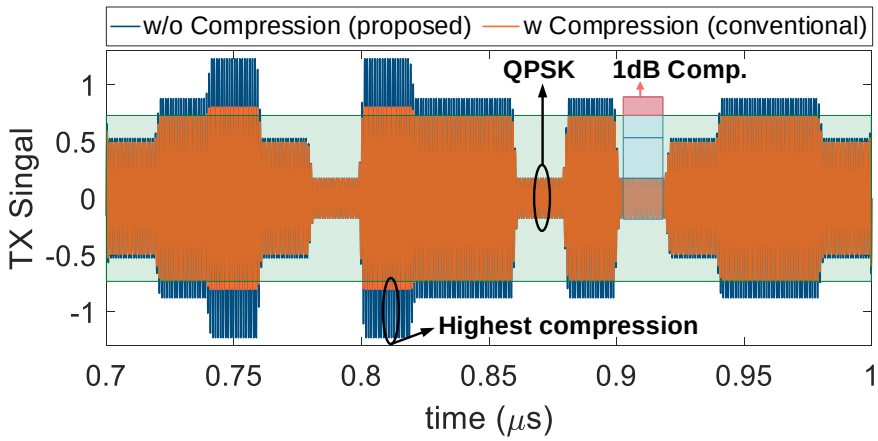


Figure 5.3 Signal compression effect in power amplifier for higher order symbols.

large array, such disparity scales considerably, resulting in a meaningful impact on overall system efficiency.

Large transmitter arrays utilize beamforming to extend communication range in mmWave and THz bands, compensating for additional propagation losses and low power generation efficiency [238, 239]. The resulting directional radiation toward the target receiver enables spatial multiplexing and enhances channel security. However, eavesdroppers still receive an exact copy of the transmitted data, only with a reduced power [240–242]. To enhance communication security, Encryption methods have been introduced for single-antenna transmitters; however, they impose significant processing overhead, especially for high-data-rate applications [243, 244]. Alternatively, hardware-enabled security techniques have been introduced in the literature, wherein the signal constellation is accurately formed at the broadside (or steered) angle but becomes increasingly distorted as the observation angle deviates. This angle-dependent behavior introduces an inherent physical layer security feature into the communication link [240–242]. Several time-modulation-based TX architectures have been proposed to enhance physical layer security [245–250]. However, these techniques require an extra RF stage and rely on high-speed switching of RF signals, which becomes inefficient and power-consuming in high-data-rate mmWave and THz applications. Additionally, they are generally constrained to small array sizes, reduce the equivalent isotropic radiated power (EIRP), and introduce higher system and processing complexity, making scalability to large mmWave array systems challenging. Methods based on spatial interference, integrate physical layer security without requiring additional hardware modifications. A spatial combination of 16-QAM and QPSK transmitters, as conceptually illustrated in Figure 5.2(a), is used to generate a target 64-QAM constellation [251]. Alternatively, as shown in Figure 5.2(b), the combination of two orthogonal M-ASK modulations can also produce M-QAM constella-

Table 5.1 Comparison between two amplifiers at 140 GHz with different saturation points and identical output power ratings.

REF	QAM Order	OP1dB (dBm)	Back-Off* (dB)	Pout (dBm)	Gain (dB)	Pin (dBm)	Pdc (mW)	Pdc-10×10 Array (W)
[237]	4	1.5	1	0.5	25.4	-24.9	30	1.35
[217]	1024	11.2	11	0.2	19.2	-19	150	15

* Back-Off = OP1dB - PAPR - Margin.

tion [225]. However, contribution of only two transmitters in constellation formation, and high base constellation orders results in slow and predictable deformation pattern.

In this work, a distributed approach leveraging the collaborative operation of simplified TX blocks within an array is proposed to optimize efficiency in the key power-limiting components. Simultaneously, physical layer security is explored for the large array of QPSK transmitters. We demonstrated that the combination of low-order modulation and a high number of TX units enables reliable reception for the intended user while causing strong distortion for eavesdroppers—all without additional hardware or processing overhead. This topology offers several key advantages over existing approaches: a) The symmetrical structure of the TX units allows for scalability in large arrays without calibration requirement, b) QPSK-based TX units are compact, power-efficient, and well-suited for distributed array topologies in mmWave and THz applications, c) The use of QPSK TX units strengthens physical layer security.

The rest of the paper is organized as follows: In section II, the principle of operation of the proposed topology is explained. Section III analyses performance aspects and effect of possible error sources on it. The proof-of-concept realization and measurement results are provided in section IV, and conclusion is drawn and presented in section V.

5.2 Principle of Operation

The signal received at the receiver is a vector summation of the radiated fields from all transmitting (TX) units [238]. The amplitude, phase, and arrangement of contributing TX units in the array determine the characteristics of the resulting beamforming. For communication efficiency and to achieve maximum directivity in conventional transmitter arrays, as illustrated in Figure 5.1, all antennas are driven by identical excitation signals. The resulting beamforming in these arrays affects only the power distribution of the received signal across different directions.

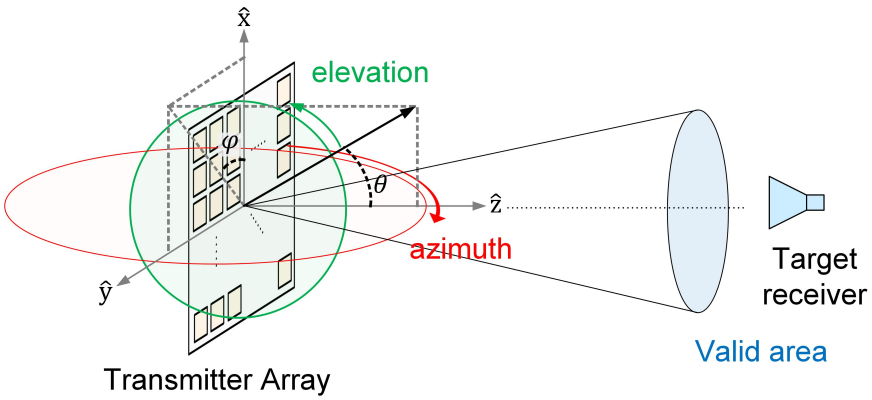


Figure 5.4 Coordinate system, and representation of transmitter array positioning and valid area.

In contrast, the spatial combination technique, as illustrated in Figure 5.2, makes use of TX units with distinct excitation signals. In this approach, the integration of radiated fields occurs naturally in free space through spatial interference. For the intended application of higher-order QAM constellation formation, TX units generates a simpler, lower-order QPSK constellation, which then combines in free space to form the desired higher-order QAM constellation. The electric field representation of the co-polarized radiated wave in the far field is given by [238]:

$$E(\theta,\phi) = \sum_{i=1}^{N} A_i E_i(\theta,\phi) e^{-jk\hat{r}\cdot\bar{r}'} \tag{5.1}$$

where $E_i(\theta,\phi)$ is electric filed radiation of each antenna in the array (element factor), A_i is the complex-valued excitation signal, k is the wave number of the transmission frequency in free space, $\hat{r}$ represents the observation angle (receiver direction). The coordinate system representation is provided in Figure 5.4. Assuming the array in x-y plane, and antennas with identical radiation pattern, the total electric field in the broadside ($\hat{r} = \hat{z}$) received electric field (E_n) simplifies to expression in given (5.2).

$$E_n = E(\theta,\phi) \sum_{i=1}^{N} A_i \tag{5.2}$$

According to (5.2), in the broadside direction, the amplitude and phase of the received signal are determined by the vector summation of all excitation signals. For example, as illustrated in Figure 5.2(b), combining the outputs of two antennas with a 90° phase difference and identical power results in a signal with a 45° phase. Such a one-to-one relation enables

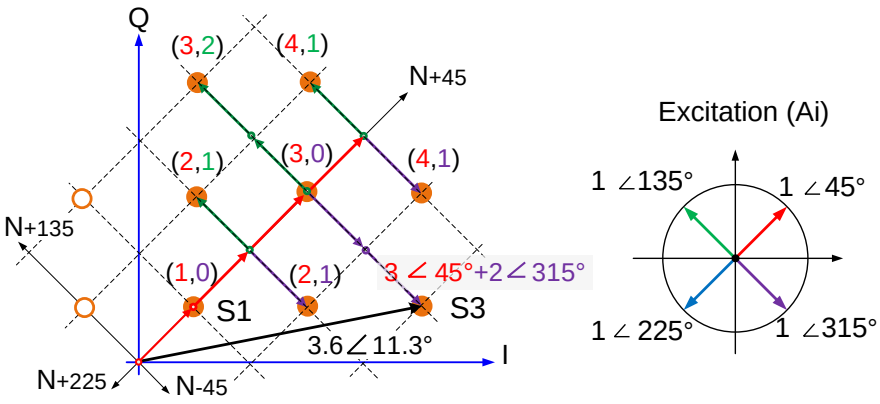


Figure 5.5 Sample QAM constellation positioning and QPSK vector illustration.

a straightforward mapping between constellation symbol positions in the complex-plane to number of TX units and their associated phases.

In the proposed topology shown in Figure 5.2(c), the TX units with QPSK modulation, generate signals with identical power and four discrete phase values: 45°, 135°, 225°, and 315°. Accordingly, by selective activation of TX units with the appropriate phase values, the desired symbol in the target QAM constellation can be generated. Figure 5.5 illustrates the QPSK TX unit excitation allocation used to generate the first quadrant of a 32-QAM target constellation. For example, to generate symbol S3, one TX unit with a phase of 45° and two TX units with aphase of 315° are activated. Unlike conventional arrays, this approach uses a variable number of transmitter units to generate different constellation symbols, offering reconfigurability and improved power efficiency, particularly in large arrays.

The minimum number of transmit (TX) units (N_{TX}) required for 16 to 1024-QAM modulations are listed in Table 5.2. As illustrated in Figure 5.5, the minimum number of required TX units is determined by the number of unit vectors pointing to the farthest constellation symbol in the outermost column. For a given M-QAM modulation, it is calculated using the empirical formula $2\left\lceil \sqrt{M}/2 \right\rceil - 1$. In large array implementations, the number of participating TX units increases multiplicatively. According to Equation (5.2), the formation of the symbol is independent of the specific locations of the activated TX units within the array. However, as demonstrated in Section III, the positions of the antennas influence the angular range within which the constellation remains valid and retrievable (Figure 5.4).

To demonstrate the impact of positioning of contributing TX units in the array on beamforming, the symbol formation process for S3 is shown in Figure 5.6. Depending on the symbol, one or two (of the four possible phases in QPSK) are chosen at any given time. Figure 5.6(a) demonstrates the impact of various antenna arrangements on the formation of

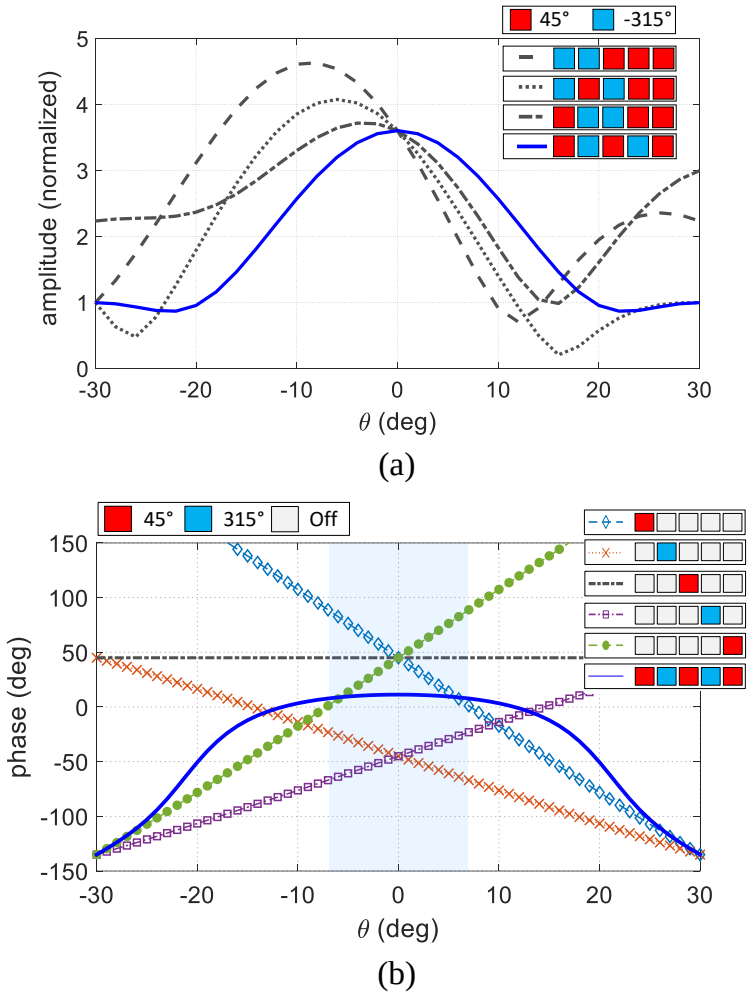


Figure 5.6 Formation of the constellation element S3 in Figure 5.5 using QPSK phase values. (a) Amplitude. (b) Phase variations for various antenna positions.

symbol S3. All arrangements provide identical amplitude values in the broadside direction, as predicted by Equation (5.2). However, they differ in their radiation patterns, which affect amplitude and phase consistency near the broadside. This effect applies to all constellation symbols where TX units with two-phase components are present. These deviations cause the constellation symbols to shift within the complex plane at the receiver, ultimately leading to signal loss. This phenomenon underpins the concept of physical layer security demonstrated in Section III.C. Figure 5.6(b) illustrates the phase variation of each TX unit around the broadside for the specified arrangement, where their integration effectively produces the desired phase value. For small angular deviations, the phase variation is minimal, ensuring reliability. However, as the angular deviation increases, the phase variation accelerates, leading to constellation deformation for eavesdroppers.

Integration of these deviations for all symbols is characterized by an angular validity range

(Figure 5.4), within which the target constellation can be retrieved with acceptable accuracy. In large arrays, this range, along with other performance parameters, can be optimized by carefully positioning the TX units. This operating principle also applies to TX arrays equipped with phase shifters for beam steering, similar to conventional phased arrays. Section III provides a quantitative analysis of the effects of various potential error sources.

5.3 System Analysis

5.3.1 Modulation and Power Efficiency

In the proposed technique, as illustrated in Figure 5.5, only the necessary number of transmitter units with identical power and appropriate phase values are activated for different constellation symbols. In contrast, state-of-the-art techniques involve continuous transmission from all transmitter units.

The deactivation of TX units in the array and the transmission of signals with two orthogonal phase values are two fundamental operation principles of the proposed topology. These mechanisms simultaneously cause a reduction in the equivalent isotropic radiated power (EIRP) of the transmitter array. The associated losses (L_t) with the two factors are modeled by power loss (L_{PWR}) and modulation loss (L_{MOD}), corresponding to each factor, respectively.
By dividing the symbol power by the radiated power, we quantify the power lost through spatial interference, averaged over constellation symbols. The expression is as follows:

$$
\begin{aligned}
L_t = (\sum_{i=1}^{M} L_i)/M, L_i = \frac{S_i}{P_{ar}} = \frac{S_i}{P_i} \times \frac{P_i}{P_{ar}}. \\
L_{MOD} = -10 \log \left[(\sum_{i=1}^{M} S_i/P_i)/M \right], \\
L_{PWR} = -10 \log \left[(\sum_{i=1}^{M} P_i/P_{ar})/M \right].
\end{aligned} \tag{5.3}
$$

here, S_i is the symbol radiated power, P_i is the total radiated power from the activated TX units for the *i-th* symbol, P_{ar} is the available power in the array when all TX units transmit synchronously, and M is the QAM constellation order. Assuming equal probabilities for all symbols, the power efficiency of each symbol formations is averaged to compute the overall constellation efficiency.

Power loss (L_{PWR}) accounts for the loss due to deactivation of antennas , relative to a fully active phased array of the same size. For instance, in 16-QAM, the average number of active antennas is $4 \times (1 + 3 + 3 + 3)/16 = 2.5$ out of a possible 3, resulting in a power loss of

Table 5.2 Performance parameters comparison for various QAM modulation formation in the proposed topology.

QAM	16	32	64	128	256	512	1024
N_{TX}	3	5	7	11	15	23	31
L_{PWR} (dB)	0.79	1.25	1.25	1.60	1.50	1.77	1.63
L_{MOD} (dB)	1.09	1.62	1.54	1.83	1.63	1.91	1.74
Goal EVM (%) [252]	<12.5	<11	<8	<6	<3.5	<2.5	<1.6
PA Back-Off (L_p)	7	8	9	9.2	9.5	10	11
EIRP Gain (wo. PA)	-1.88	-2.87	-2.79	-3.43	-3.19	-3.68	-3.37
EIRP Gain (w. PA)	4.12	4.13	5.21	4.77	5.31	5.32	6.63

EIRP Gain (wo. PA) $= -(L_{PWR} + L_{MOD})$.
EIRP Gain (w. PA) $= -(L_{PWR} + L_{MOD}) - (L_P[\text{QAM}] - L_p[\text{QPSK}])$.

approximately 0.79 dB. L_{MOD} models the loss associated with the simultaneous presence of two phase values within the topology.

The loss values for various QAM modulation orders is listed in Table 5.2. Power amplifier back-off (L_p) at mmWave frequencies normally has to increase due to the infeasibility of digital pre-distortion in high data rate links. The reported accumulated loss is in comparison to equivalent sized phased arrays. These values do not account for power amplifier (PA) considerations required for high dynamic range signal transmission, as discussed in Section II and summarized in Table 5.1. When PA back-off requirements are factored in, the EIRP improves accordingly. Thus, the overall EIRP is given by Equation (5.4).

$$\begin{aligned} EIRP =& IP_{1dB} + G_{PA} + 10\log(N_{TX}) \\ &+ G_{ANT} - L_{MOD} - L_{PWR} - L_p. \end{aligned} \tag{5.4}$$

Peak EIRP value is crucial for regulatory compliance, link budget, and safety. In the proposed topology, the activation of participating TX units effectively generates the power associated with each constellation symbol. Consequently, the peak EIRP follows the constellation's peak-to-average-power-ratio (PAPR) and is equal to $EIRP_{peak} = EIRP_{avg} + PAPR$. In this equation, $EIRP_{avg}$ is equal to the value in (4), and $PAPR$ represents the constellation's PAPR. For rectangular M-QAM modulations, the peak EIRP is equal to $3(\sqrt{M}-1)^2/(M-1)$ [235].

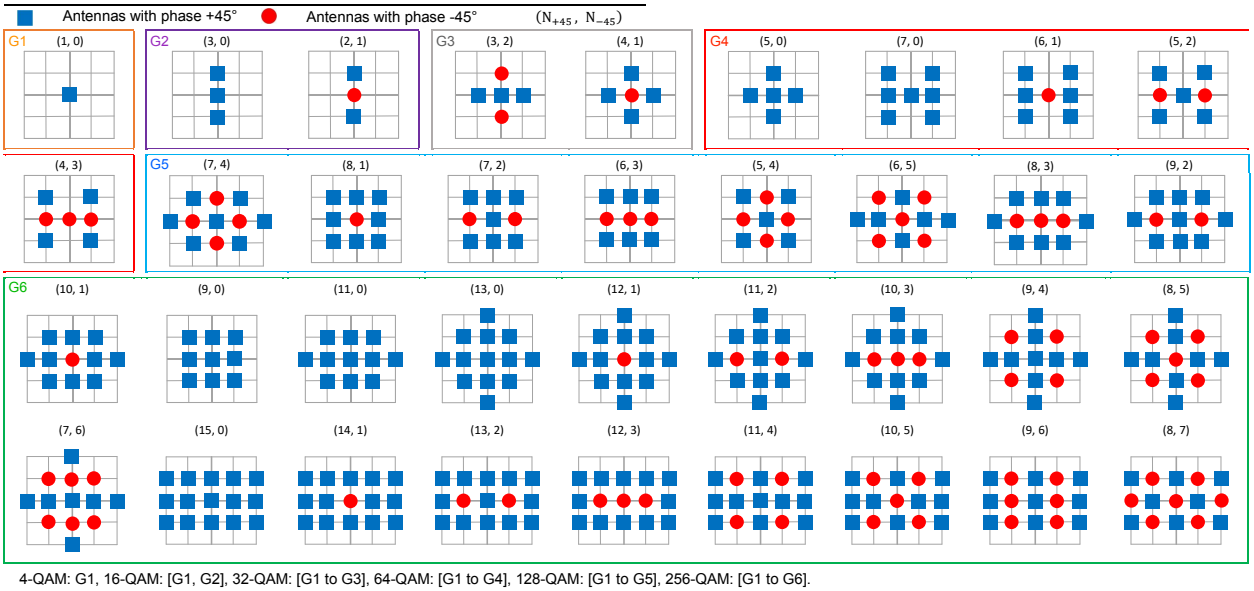


Figure 5.7 The suggested antenna arrangement in the array to extend the validity range (amplitude and phase consistency) for minimal size array implementation. Each color group represents the added TX units to implement the QAM order.

5.3.2 Beamforming

Unlike conventional phased arrays, which generally make use of identical excitation across all antennas, spatial modulation techniques transmit distinct signals from each antenna. The majority of existing techniques involve a small number of antennas with wide radiation angles. However, for the large array transmitter envisioned in this concept, the beamforming parameters must be re-evaluated. Specifically, to fully leverage the benefits of beamforming in improving the link budget and enhancing channel security, it is essential to achieve directional radiation, a smooth radiation pattern around the main lobe, a high side-lobe-level (SLL), and the absence of grating lobes.

In the proposed topology, as shown in Figure 5.5, diagonal constellation symbols are associated with transmitter units operating at a single phase value, while non-diagonal symbols incorporate two phases, selecting two of the four possible QPSK modulation phases with a 90° relative phase difference. The former case is similar to conventional arrays with a constant phase front, where traditional beamforming techniques are applicable.

For the latter group, as shown in Figure 5.6(a), the phase positioning within the array has a significant impact on beamforming. Similar to Figure 5.6, an intertwined symmetric arrangement with maximum homogeneity yields the most favorable beamforming characteristics. Figure 5.7 illustrates all unique antenna positioning configurations for the minimum

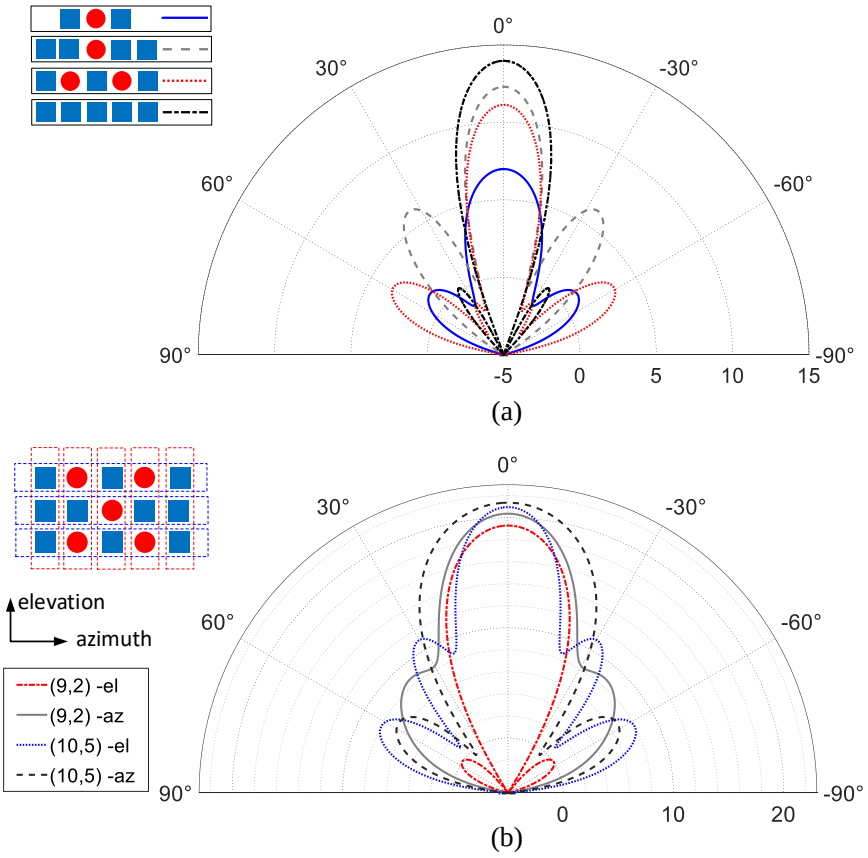


Figure 5.8 Radiation patterns (dB). (a) For the specified homogeneous two-phase antenna positioning. (b) For the symbols (9,2) and (10,5) in Figure 5.7.

array implementation required to form lower-half and first-quarter constellation symbols for modulation schemes up to 256-QAM. Due to symmetry, the positioning for other constellation regions can be derived by substituting the corresponding phase values. For instance, the lower half of the second quarter can be generated by replacing the 45° and 315° phases in the transmitter units with 135° and 225° phases, respectively.

To analyze the radiation pattern of each symbol in the azimuth direction, the antennas are grouped into parallel strips aligned along the elevation direction, with the reverse configuration used for the elevation pattern. As a result, the antenna positioning along the x and y axes in Figure 5.7 can be categorized into four distinct configurations. Figure 5.8(a) shows the corresponding radiation patterns for these groups. The homogeneous antenna positioning results in the highest SLL for the required excitation phases. Similar to a conventional phased array, this configuration produces a directional broadside radiation pattern without grating lobes. The directivity varies in proportion to the relative power of the intended constellation symbol. The azimuth and elevation radiation patterns for two symbols, (10, 5) and (9, 2), which exhibit high positioning complexity, are shown in Figure 5.8(b). It is important to note

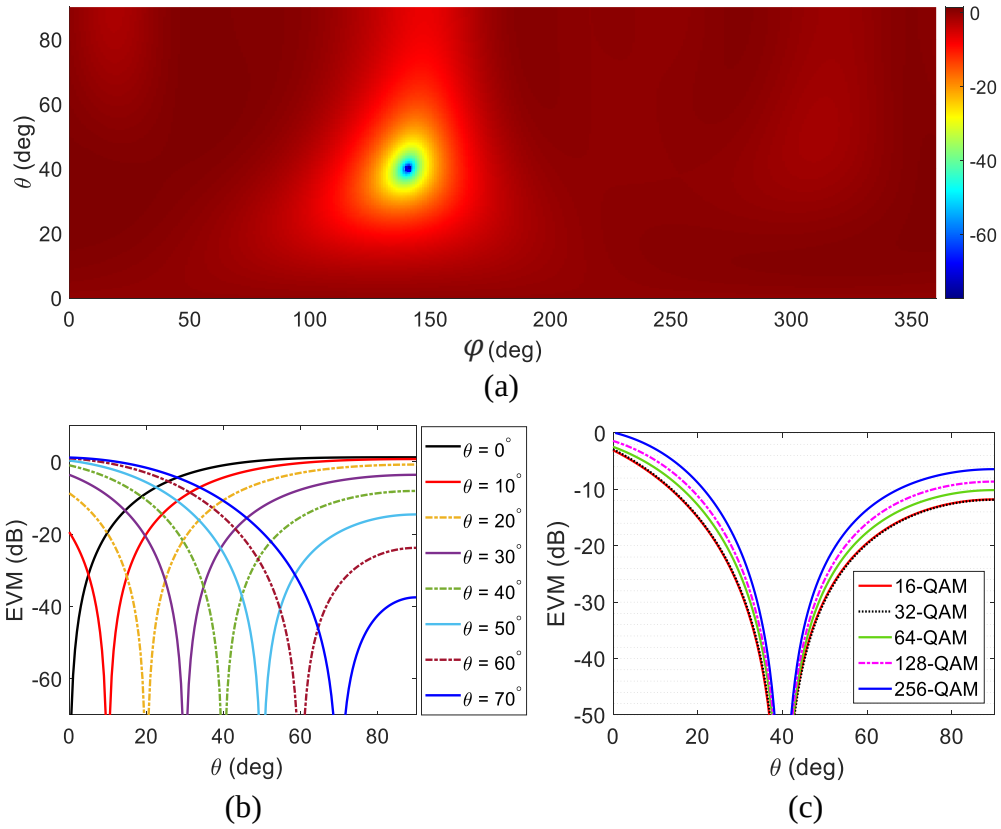


Figure 5.9 EVM variation for the array positioning in Figure5.7. (a) Beam steering at elevation and azimuth angles of 40° and 140°. (b) Elevation angle deviation from broadside across different QAM modulation orders. (c) Various constellation orders.

that a similar fundamental radiation behavior is observed for any phase combination across all QAM orders. For large array implementations, the same symmetry and homogeneity can be easily scaled to accommodate a larger number of antennas. Furthermore, varying the number of contributing antennas in a large array allows for position optimization in a sparse array, enhancing performance factors such as extended validity range, reduced side-lobe levels (SLL), and more.

$$EVM_{\mathrm{dB}} = 20\log\left[\frac{\sqrt{\frac{1}{N}\sum_{n=0}^{N-1}\left|S_{\mathrm{ref}}[n]-S_{\mathrm{maes}}[n]\right|^2}}{\sqrt{\frac{1}{N}\sum_{n=0}^{N-1}\left|S_{\mathrm{ref}}[n]\right|^2}}\right] \tag{5.5}$$

5.3.3 Physical Layer Security and Validity Angle Range

The integrated physical layer security allows for accurate signal retrieval only within the target beamforming angle (Figure 5.4). As opposed to conventional transmitter arrays, the spatial power combination within the proposed topology distorts the phase of the individual

TX units, and prevents eavesdroppers from reconstructing the transmitted constellation, even with a high signal-to-noise ratio (SNR).

To evaluate the array performance and the accuracy of constellation formation at the receiver, we analyze the error vector magnitude (EVM) of the received constellation. EVM quantifies the deviation of the received symbols from their expected positions, serving as a measure of the error introduced at a particular stage of the communication link. The EVM is calculated as:

where, N represents the number of received constellation symbols, while S_{ref} and S_{meas} denote the expected and measured symbol values, respectively. Based on the proposed positioning of the transmitter units in Figure 5.7, the EVM of the formed signal is calculated in terms of the elevation angle deviation from target beamforming angle for various constellation orders. As shown in the Figure 5.9(a) surface plot, at the beamforming angle, an ideal phase and amplitude combination occurs, resulting in zero degradation. As the angle deviates, both the amplitude and phase values change, introducing significant distortion to the constellation symbols and causing EVM increase to around 0 dB, which represents the total unrecoverable state. The EVM variation for different beamforming angles is shown in Figure 5.9(b), demonstrating consistent behavior at practical beamforming angles. The effect of different QAM orders is shown in Figure 5.9(c). Higher-order constellations exhibit faster degradation, as they involve a larger number of TX units, which increases the potential sources of error. For an acceptable EVM of less than -30 dB, which is required for valid constellation retrieval in commercial communication systems, the maximum validity angle of 20° is achieved. This aligns with the half-power beamwidth (HPBW) of a 3×5 conventional patch antenna array with half-wavelength separation, used for 256-QAM. The normalized broadside array gain and phase variation plots for four antenna positioning configurations provided in Figure 5.10(a) and 5.10(b) are compatible with the obtained validity angle range. Within $\theta < 10°$ (inside the HPBW) the corresponding curve remains mostly flat, resulting in minimal EVM disruption.

Thus, the constellation remains valid within the HPBW, where most of the transmitted power is concentrated. However, beyond this range, the EVM continues to degrade, significantly distorting the signal and making it impractical for unintended listeners to retrieve. Due to the symmetry of the array positioning, a similar EVM variation occurs for azimuth angle deviations. It is worth noting that in a large array with a narrower beamwidth, the validity range will proportionally decrease. Optimization techniques can be applied in large arrays to either extend or reduce the validity range, or alternatively, to enhance beamforming performance for a specific application.

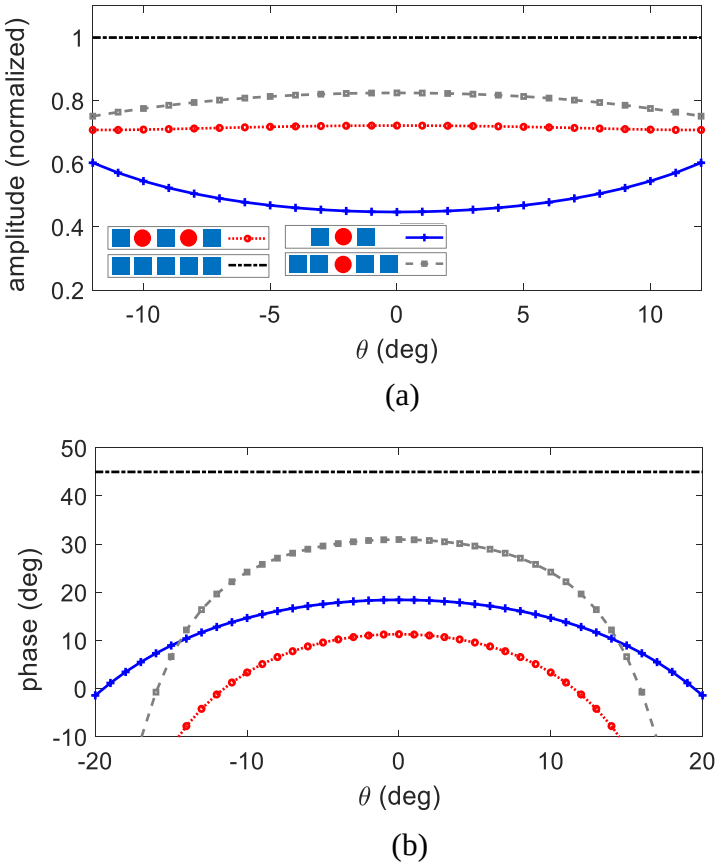


Figure 5.10 Close-up view of: (a) Normalized amplitude. (b) Phase variations for the specified antenna positions around the broadside.

The discrete nature of phase shifters for beam steering does not affect the EVM behaviour (Figure 5.9(b)), as it is consistent for all TX units in the array. Furthermore, performance variation among phase shifters in amplitude and phase deviation effects is examined in Section III.E).

5.3.4 Radiation Pattern Variation Effect

In the constellation formation described in Section II and illustration in Figure 5.9, it is assumed that all active transmitter (TX) units operate identically, providing uniform amplitude and phase contributions for constellation formation. However, RF design asymmetries or power distribution variations may lead to performance discrepancies among the TX units. In the proposed topology, the TX units are identical, thereby minimizing fabrication-related errors and ensuring consistent performance. However, the large number of radiative elements involved in constellation formation requires similar radiation properties across all elements

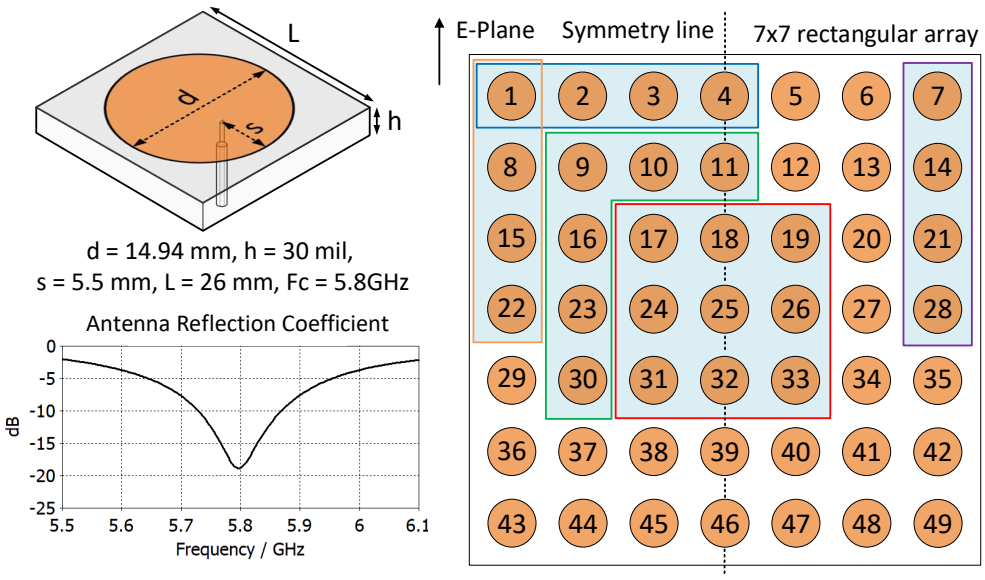


Figure 5.11 Array of 7×7 circular patch antennas with a half-wavelength separation on a RO4003 substrate with 30 mils thickness.

to maintain the desired amplitude and phase values at the target receiving point.

The radiation pattern of each antenna in an array is influenced by its shape and boundary conditions. In an array with identical antennas, these boundary conditions vary depending on the antenna's location within the array. To examine the effect of the radiation pattern on constellation formation, the 7×7 array shown in Figure 5.11 is considered. This array consists of circular patch antennas with half-wavelength separation and a 1/4-wavelength ground plane extension surrounding the array. Adjacent antennas exhibit -16 dB and -18 dB coupling in the E and H planes, respectively. Figs. 5.12(a) to (e) show the co-polar electric field patterns of the antennas, extracted through full-wave simulations in CST Studio Suite, and categorized into five distinct groups (shown in Figure 5.11). The nine central antennas in Figure 5.12(a) exhibit the most consistent radiation patterns, with no noticeable tilt or gain variation. As we move toward the outer antenna layers, shown in Figs. 5.12(b) and (c), the patterns gradually exhibit greater fluctuations. The radiation patterns of the antennas on the left and right sides, shown in Figs. 5.12(d) and (e), exhibit considerable tilting toward the center due to boundary condition asymmetry in the H-plane. The radiation pattern variation with reference to the center antenna (number 25) is shown around the broadside in Figure 5.12(f). As each layer progresses outward—represented by the red, green, and blue curves—the variation percentage increases, exceeding 5% in the outermost layer. Therefore, the gain differences and fluctuations in the electric field of the boundary elements, particularly the four corner antennas, can be significant, rendering them

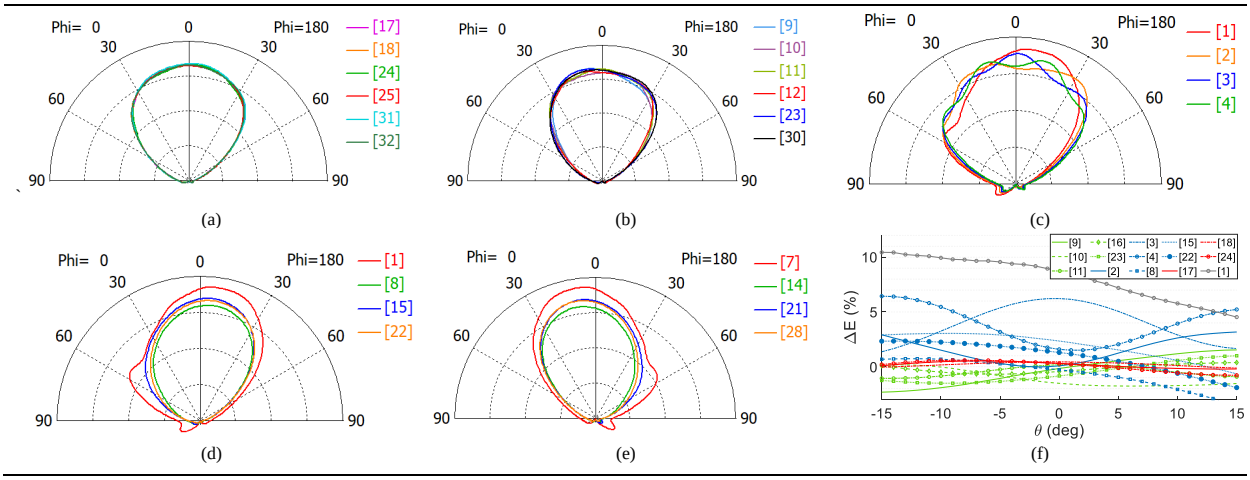


Figure 5.12 Radiation pattern variation of patch antennas shown in Figure 5.11 based on their location in the array: (a) Red square at the center. (b) Green circle in the second layer. (c) Blue square at the horizontal edge. (d) Orange square in the left column. (e) Purple square in the right column. (f) Graphical representation of pattern variations based on array location.

unsuitable for constellation formation applications. In contrast, the inner antennas (in the 5x5 array) exhibit high consistency.

To numerically assess the impact of pattern imperfections, the EVM for 16-QAM to 256-QAM constellations is calculated using the inner (5×5) array antennas from Figure 5.11, with the results presented in Figure 5.13. To account for the effect of individual antennas, the far-field complex radiated electric field of each antenna within the array structure is extracted through full-wave simulation and incorporated into equation (5.1) to form the total radiated electric field. As shown in Figure 5.13, the variation in the radiation pattern leads to EVM degradation around the broadside, reaching approximately -45 dB. However, for larger deviation angles, the EVM curves converge with those of the ideal array, as shown in Figure 5.9. Beyond this point, the accurate amplitude and phase contributions of the TX units for large angle deviations become the dominant factor in spatial power combination. As a result, the EVM degradation due to antenna radiation imperfections remains well within acceptable limits, typically ranging from -25 to -40 dB, for most applications.

Using the border antennas as supporting elements for the active array offers the simplest solution to improve pattern consistency. However, in area-limited scenarios, with low coupling levels or low constellation orders, the guard antennas can be reduced to corner antennas. Alternatively, antenna decoupling techniques [253,254] and the use of high-isolation antennas [255] can be explored to achieve enhanced performance.

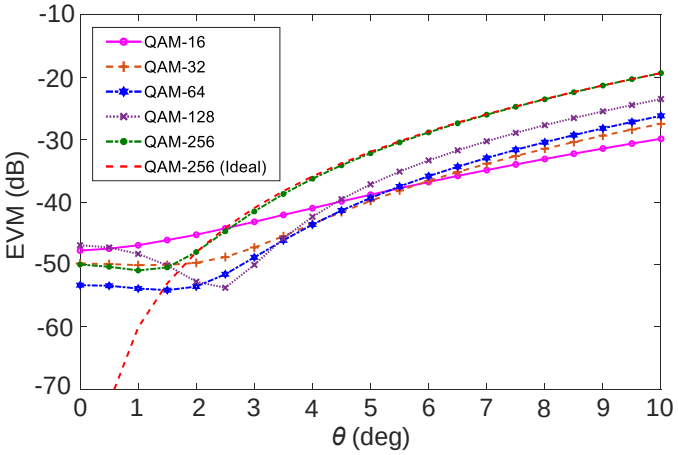


Figure 5.13 Retrieved signal EVM variation for 16-QAM to 256-QAM, considering the effect of antenna pattern variations.

5.3.5 LO Amplitude and Phase Error

The amplitude and phase of the LO input can be influenced by implementation imperfections, layout constraints, coupling, and asymmetries. This issue becomes particularly critical in large arrays, where even small deviations can accumulate, resulting in significant variations at the TX unit feed points. Therefore, it is crucial to study the acceptable error limits to ensure system performance.

In this context, a 60-element array (four times larger than the minimum size required for 256-QAM) is considered. For broadside radiation, the TX locations do not contribute to errors in this study. Given the large number of scenarios involving relative phase and amplitude deviations across the antennas, a statistical approach is employed. For the amplitude error study, assuming a variation in the input LO amplitude from zero to $\Delta\%$ for all TX units, the EVM for the constructed constellations is calculated. For each maximum allowed deviation ($\Delta\%$), the average and maximum EVM distortion are calculated over 200,000 random combinations, with the results shown in Figure 5.14(a). A similar analysis is conducted for LO phase deviations ($d\theta$), and the result is presented in Figure 5.14(b). Counterintuitively, Figure 5.14 reveals that higher-order QAM modulations exhibit lower EVM distortion for a given amplitude or phase error.

This resilience stems from the fact that higher-order constellations involve a larger number of TX units contributing to the overall signal. Given a constant error percentage (Δ and $d\theta$) per transmitter, we can divide the signal to deterministic and statistical parts. Assuming an arbitrary symbol signal as $S_i = NA + N\sum_{m=0}^{N-1}\Delta_i$, and a Normal distribution for error (Δ_i)

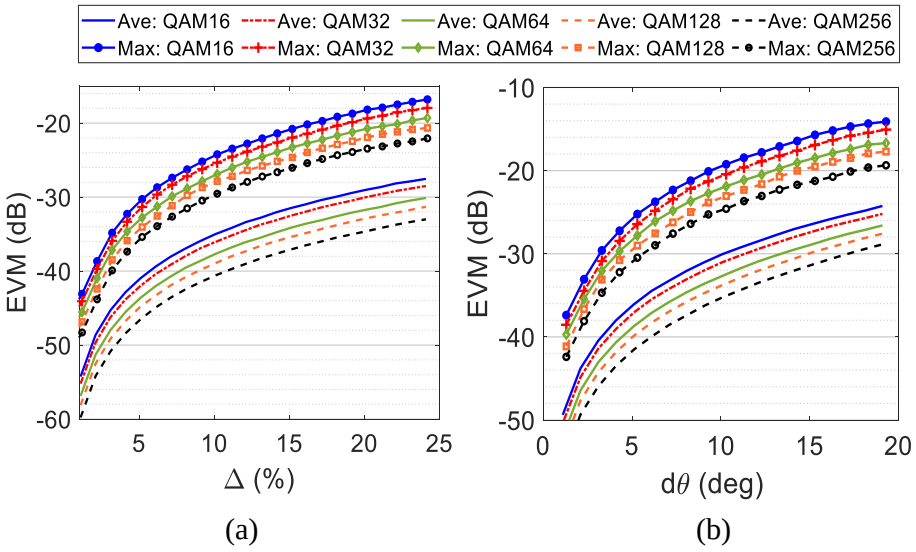


Figure 5.14 Impact of LO input imperfections on the transmitted signal's EVM: (a) Effect of amplitude variation. (b) Effect of phase variation.

with total randomness ($\sigma = \Delta/\sqrt{3}$), the energy associated with deterministic and statistical parts of the signal becomes NA^2 and $N\Delta^2/3$, respectively [256]. Since $\Delta < A$, higher number of contributing Tx units (N), causes the energy of deterministic part outweigh the random part. Similar analysis applies to phase errors ($d\theta_i$) as well.

For a small (minimum size) 15-element array, the EVM curves for different modulations show much less separation, highlighting the influence of the number of TX units in constellation formation and the associated error suppression. This effect is advantageous in large arrays, as implementation errors in LO distribution tend to cancel out rather than accumulate negatively. However, in larger arrays, LO imperfections are more likely to cause significant deviations at the TX unit inputs. A 5% amplitude error and a 5° phase error represent practical ranges for feed network implementation or the deviations achievable in distributed power generation techniques.

5.3.6 Power Amplifier

The symbol-by-symbol (de)activation of the PA, particularly in high data rate applications, demands careful design and consideration to ensure reliable performance and signal integrity. Directly switching the PA on and off at the output is inefficient and introduces significant losses. An alternative approach utilizes the high common-mode rejection ratio (CMRR) and inherent symmetry of differential modulators to embed the "off" state directly within the QPSK signal.

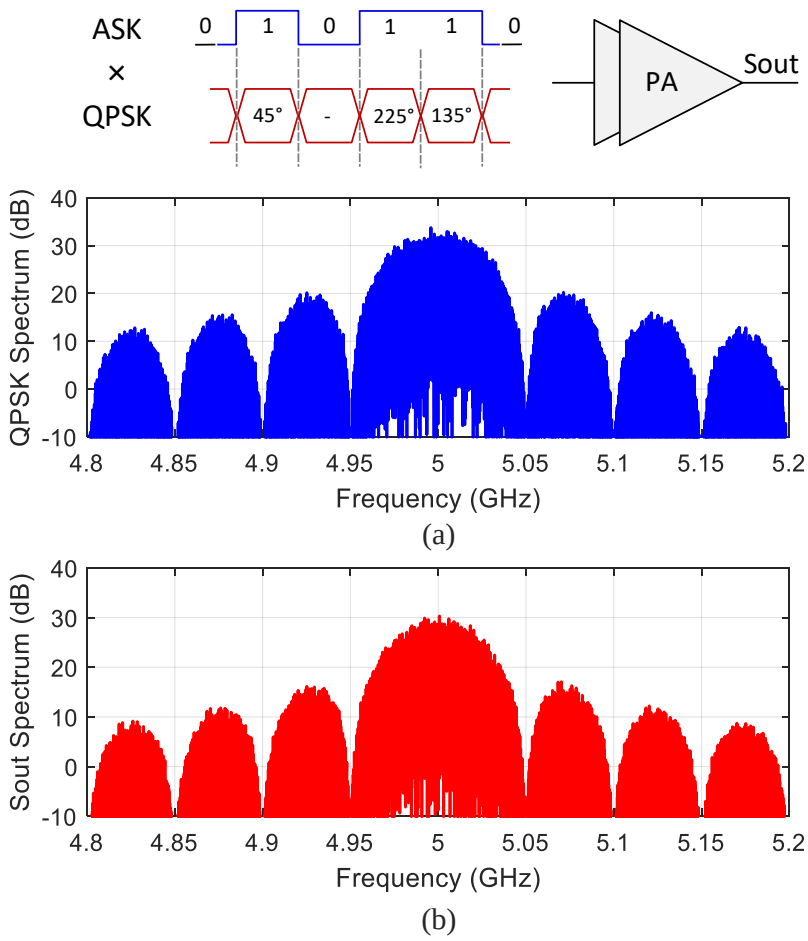


Figure 5.15 Spectrum analysis of power amplifier operating in the proposed topology for sample 5.6 GHz carrier frequency and 50 MHz symbol rate: (a) Spectrum of QPSK signal. (b) Spectrum of QPSK×ASK modulated signals.

In the proposed approach, as illustrated in Figure 5.15, the PA input is the product of an Amplitude Shift Keying (ASK) signal and a QPSK signal. Since both signals switch at the same symbol rate, their spectral nulls align, effectively preventing any significant bandwidth expansion. Figure 5.15 compares the spectra of a standard QPSK signal and a QPSK×ASK signal, both operating at a 100 MHz symbol rate centered at 5.6 GHz. The two spectra differ by only about 2 dB in power, due to the reduced average activation time of the PA resulting from the multiplication. As a result, the PA's operation condition in the proposed topology is similar with that of a conventional QPSK transmitter, with minimal spectral or efficiency drawbacks.

Additionally, the linearity of class-AB power amplifiers has been shown to be sufficient for low modulation orders [217]. In this class, power consumption is significantly reduced when

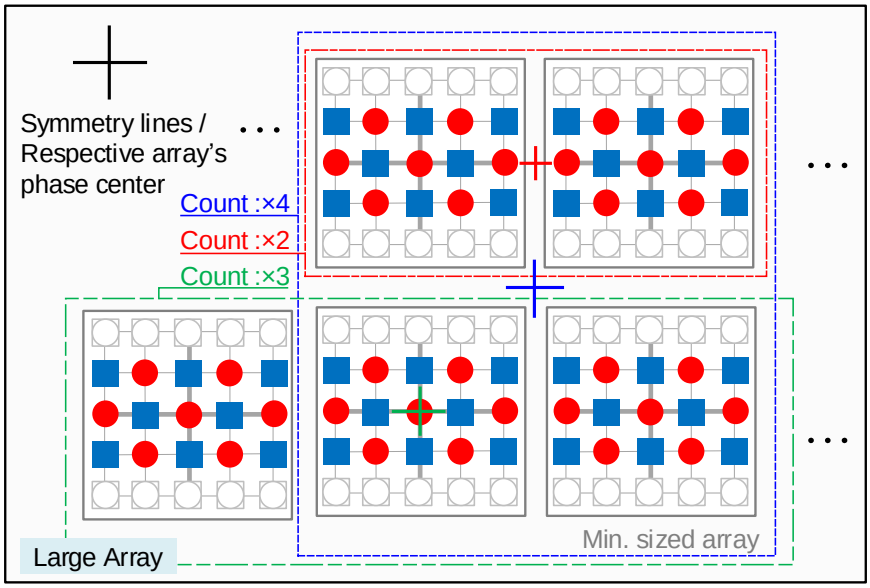


Figure 5.16 Large array formation from the minimum sized array (in Figure 5.7). For given array size small array groups to be repeated in x and/or y axis.

there is no input power, which further lower both power consumption and improve efficiency in the proposed topology. This effect is accounted for in the power consumption calculations presented in Table 5.1.

5.3.7 Large Array and Sparseness

An important byproduct of the proposed topology is the ability to control link budget (modify EIRP) through the (de)activation of TX units in a large array, rather than adjusting the input signal power. This method enables the power amplifiers (PAs) to operate at their optimal efficiency, which is especially beneficial in large-scale arrays. For example, as shown in Table 5.2, in the case of 64-QAM transmission, the number of active TX units can be increased in steps of 7 elements.

Table 5.3 summarizes the array EIRP values and control steps for 16-QAM to 1024-QAM modulations in a 10×10 array, assuming unit power and gain per TX unit. The minimum EIRP is calculated using the minimum number of TX units reported in Table 5.2, while the maximum EIRP is obtained by $Min.EIRP \times Count$ number of TX units involved in the transmission.

Figure 5.16 illustrates the formation of large arrays using minimal-sized array groups. Depending on the array size and the "count" number (as shown in Table 5.3), a larger array can be formed, producing the same modulation order but with higher EIRP and improved

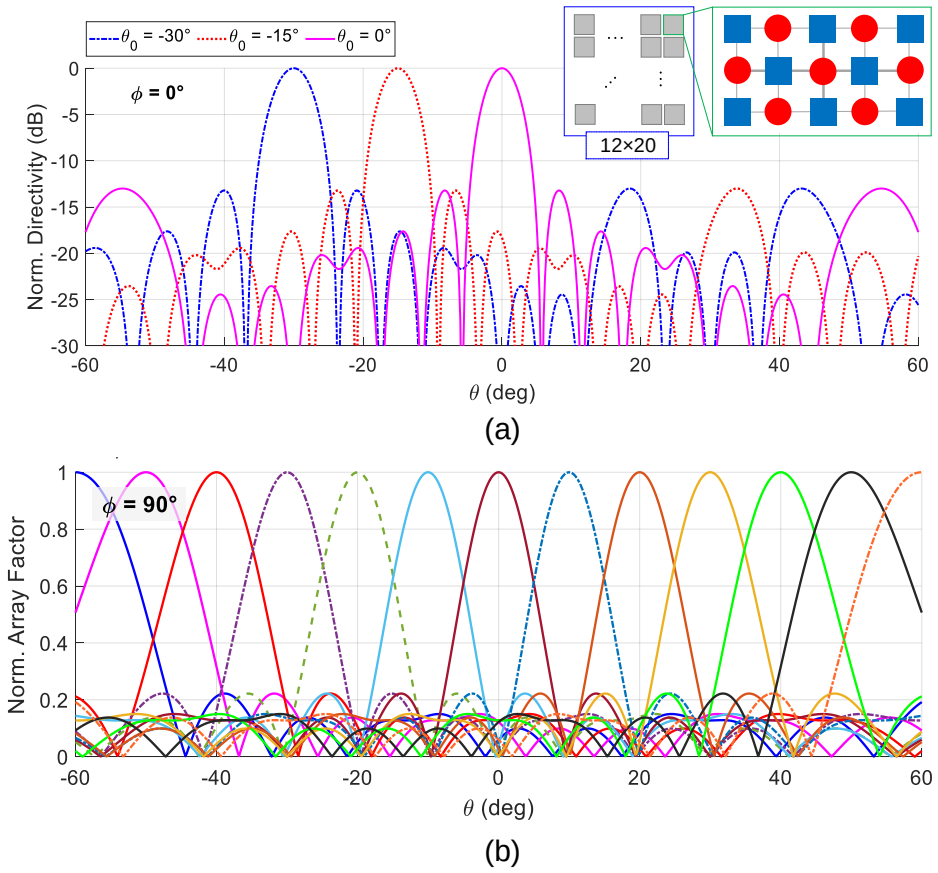


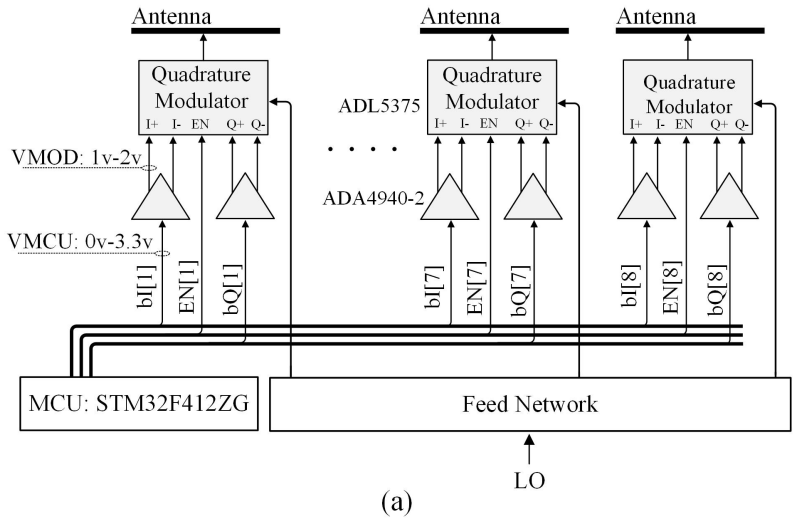
Figure 5.17 Beamfomring for the selected symbol's (8,7) phase distribution: (a) Radiation pattern variation study over various beamforming angles. (b) Resulting Array factor, over elevation angles (θ) in H-plane.

Table 5.3 EIRP variation for a 10×10 array with unit TX unit power and gain for various QAM modulation orders.

QAM	16	32	64	128	256	512	1024
Min. EIRP	2.89	4.12	5.66	6.98	8.57	9.93	11.54
Count	33	20	14	9	6	4	3
Max. EIRP	18.07	17.13	17.12	16.52	16.35	15.9	16.32

beamforming characteristics. Lower-order modulations provide greater flexibility in tuning, as each step corresponds to a smaller increment in the number of active TX units. The maximum EIRP across all modulation schemes exhibits a reduction of 2 dB to 3.7 dB, attributed to modulation and array efficiency effects (Table 5.2).

As illustrated in Figure 5.17, the radiation pattern of a sample 20×20 array transmitting the symbol $(8, 7)$ of a 256-QAM modulation scheme (see Figure 5.7). This configuration



(a)

MCU Operation Routine

- Mode select:
  A: Identical TX:U1-U7 operation (large array).
  B: Including TX-U8 to TX:U1-U7.
- Data rate select.
- Modulation order : Mode A (4,16,32,64), Mode B (4,16,32,64,128,256).

Timer interrupt to match intended data rate.

- Random selection of symbols for intended QAM modulated order: QAM- X: 1 – X. (In practice, based on data input).
- Write pins.

Stored transmitters activation/ phase chart for symbols

	TX	U1		U2		U3		U4		U5		U6		U7		U8 (1/4)	
		EN	Sb	EN	Sb	EN	Sb	EN	Sb	EN	Sb	EN	Sb	EN	Sb	EN	Sb
Mode 1	1	1	01	0	x	0	x	0	x	0	x	0	x	0	x	0	x
	2	1	00	1	00	1	11	0	x	0	x	0	x	0	x	0	x
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	0	x
	64	1	11	1	11	1	11	1	11	1	11	1	11	1	11	0	x
Mode 2	1	0	x	0	x	0	x	0	x	0	x	0	x	0	x	1	0
	2	1	0	0	x	0	x	0	x	0	x	0	x	0	x	1	0
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	x
	256	1	11	1	11	1	11	1	11	1	11	1	11	1	11	1	3

x : undefined, EN: [0, 1], S(binary) : [00, 01, 10, 11]

(b)

Figure 5.18 (a) Block diagram representation of the proof-of-concept prototype. (b) Programming routine of the microcontroller.

corresponds to a 16 times expansion of the base 5×5 transmit (TX) array, resulting in a total of 12×20 active TX units. The radiation pattern characteristics are determined by the phase distribution across the array and, as shown in Figure 5.17(a), remain unchanged

with the beamforming angle. Each constellation symbol activates a distinct subset of TX units leading to symbol-dependent variations in the radiation pattern. However, as shown in Figure 5.17(a), the beamforming angle has minimal impact on these characteristics. The corresponding array factor, shown in Figure 5.17(b), demonstrates stable and consistent beamforming performance across all practical elevation angles.

5.3.8 Reduced Array Size

A key advantage of the proposed topology is the symmetry and scalability of its TX units, making it well-suited for large array implementations. However, for smaller arrays, a simple modification can reduce the number of required TX units (N_{TX}) by nearly half.

As illustrated in Figure 5.5, the vector summation involves one unit vector extending from the origin to S1, with two unit vector separations between neighboring symbols—resulting in an odd total number of TX units. By introducing a TX unit with half the amplitude (equivalent to one-quarter power), the required number of TX units can be reduced to $(N_{TX}+1)/2$. For instance, with this adjustment, 256-QAM and 1024-QAM implementations would require only 8 and 16 elements, respectively, instead of the original 15 and 31. However, complications such as LO input power, amplifier gain and transfer delay in the modified TX unit should be carefully addressed to avoid distortion in the transmitted signal.

5.4 Experimental Results

To validate and evaluate the proposed transmitter array topology, a 2×4 transmitter prototype was designed to operate at 5.6 GHz. The block diagram of the array is shown in Figure 5.18(a). The ADL5375 quadrature modulator ICs from Analog Devices were used as QPSK TX units. These modulators receive the digital data inputs, including enable (EN), and differential I and Q signals from a microcontroller (MCU). An ADA4940-2 op-amp-based driver stage converts the single-ended $0V$ (low) to $3.3V$ (high) MCU data signals into differential signals ranging from $1V$ to $2V$ to meet the modulator's voltage specifications. The programming logic of the MCU is shown in Figure 5.18(b). The activation and phase states of each TX unit for all symbols in the target modulation order are pre-stored in the MCU and transmitted based on the predefined data rate. The ST-STM32F402ZG microcontroller was chosen for the MCU.

The fabricated prototype is shown in Figure 5.19. The feed network is designed to provide equal LO signal phase distribution. The TX units U1 to U7 receive identical LO power, while U8 receives 1/4 LO power for testing the reduced array size scenario, described in Section

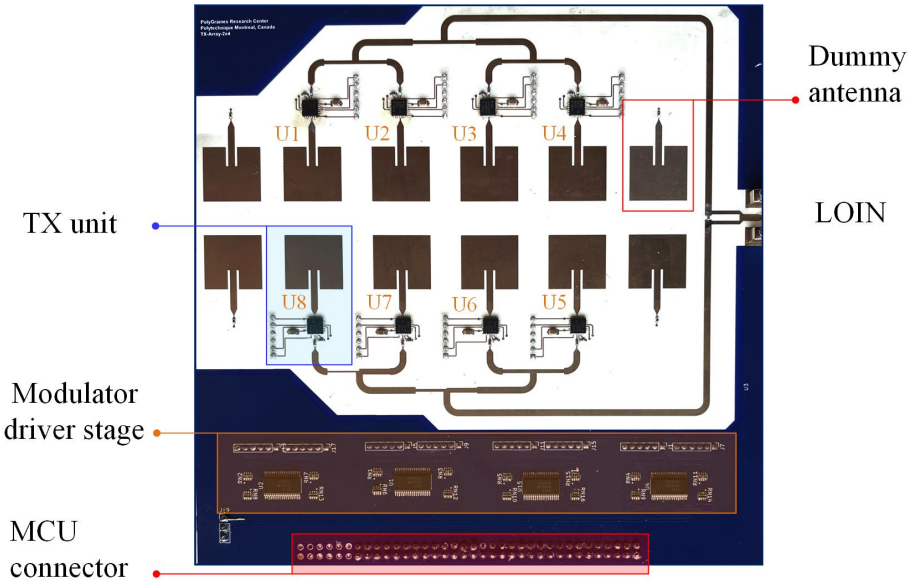


Figure 5.19 Top view photograph of the fabricated prototype.

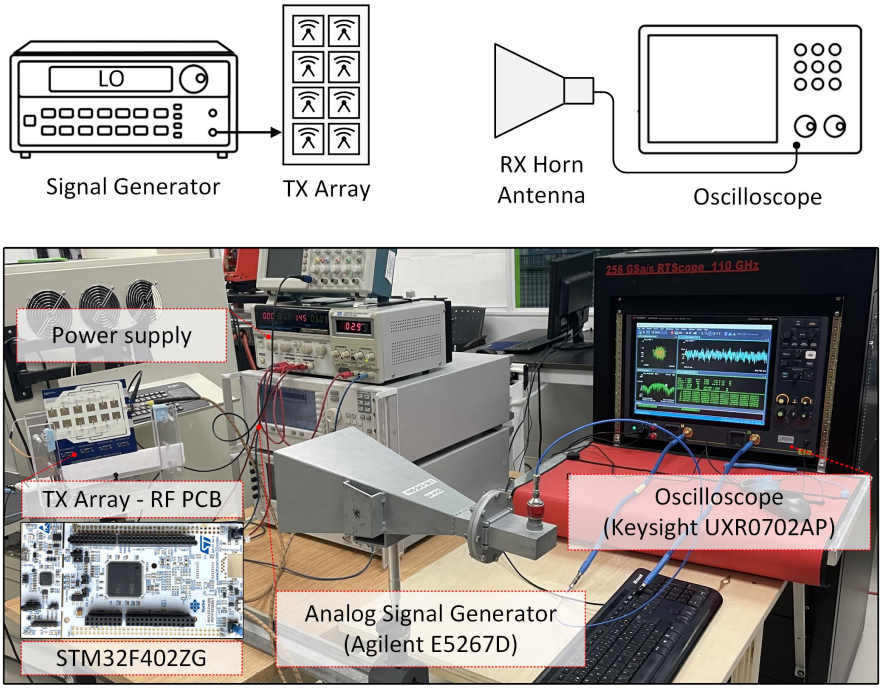


Figure 5.20 Measurement setup of the proposed transmitter array.

III.H. The activated TX units for each QAM modulation order are listed in Table 5.4. The antenna feeds, as shown in Figure 5.19, are applied from opposite sides to cancel LO leakage. The four antennas on the left and right sides support the inner 2×4 active antennas, ensuring consistent radiation patterns across the array. The driver stage and TX units are highlighted

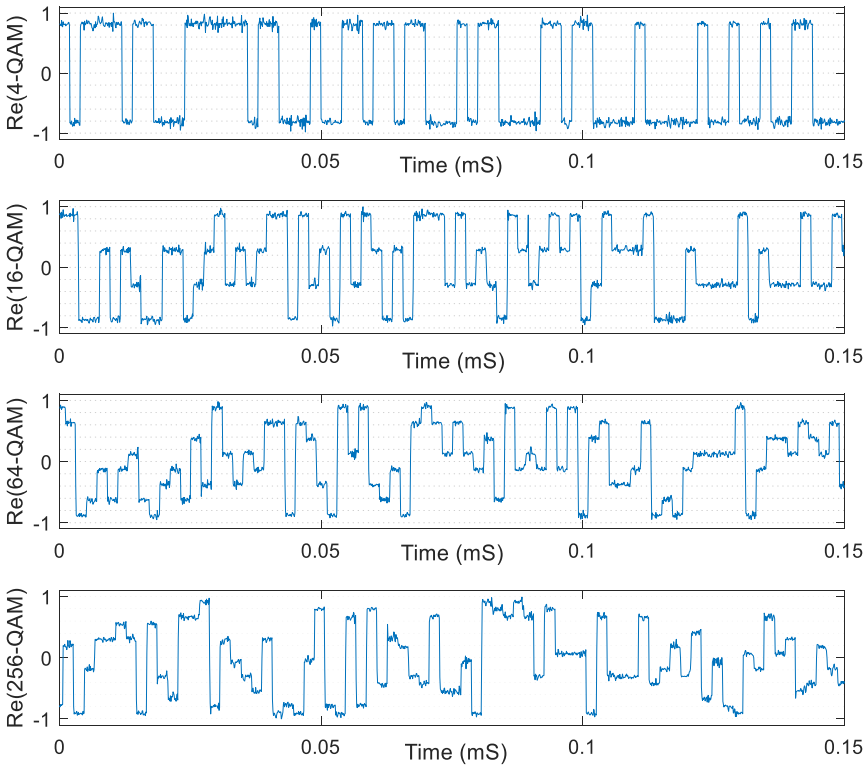


Figure 5.21 Measured time-domain received signal on an oscilloscope for different QAM modulation orders.

Table 5.4 The TX units in the prototype used to form each modulation order.

16-QAM	32-QAM	64-QAM	128-QAM	256-QAM
U3, U4, U5	U2 to U6	U1 to U7	U8, U1, U2, U3, U6, U7	U8, U1 to U7

in the diagram, with the MCU interfacing with the transmitter array via connectors.

In the measurement setup shown in Figure 5.20 an Agilent E5267D analog signal generator is used to generate the LO signal, and a horn antenna receiver is placed in the far-field of the prototype, and is made sure to have high signal-to-noise ratio (SNR) received signal to isolate the transmitter performance and minimize the impact of channel characteristics and signal power on the retrieved constellation. The received RF signals are processed by a Keysight UXR0702AP oscilloscope for down-conversion, digitization, and sampling.

The real part of the received signal in the time domain for 4, 16, 64, and 256-QAM modulations is shown in Figure 5.21. A receiver bandwidth four times wider than the symbol rate is used, and no filtering is applied at the receiver to minimize distortion effects on the time-domain signal. This configuration allows for clear observation of the actual transmit-

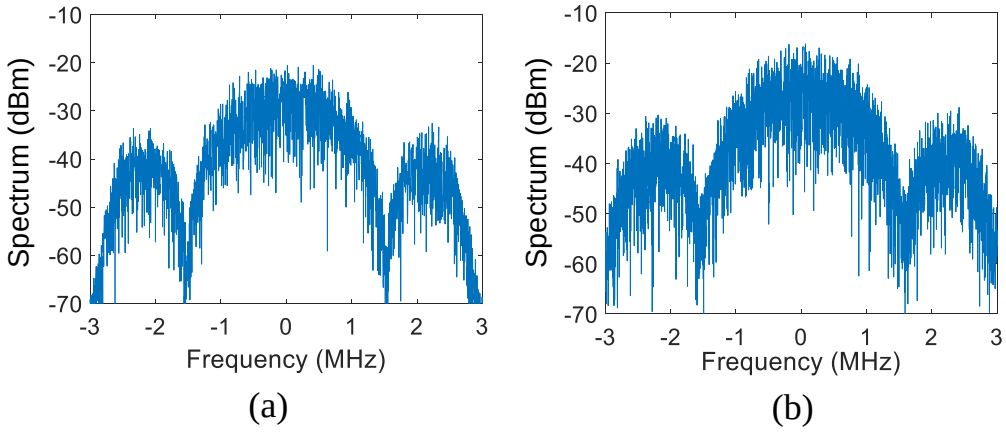


Figure 5.22 Measured signal spectrum for: (a) 4-QAM and (b) 256-QAM.

ted symbol states for each constellation. The signals display distinct levels with the required amplitudes, demonstrating accurate spatial power combination and effective constellation formation.The spectrum of the received signals for 4-QAM to 256-QAM modulations is shown in Figure 5.22, indicating a bandwidth consistent with a 1.5 Mbps data rate. The presence of side lobes is attributed to the square-wave nature of the digital input data. We note that the 1.5 Mbps data rate in the prototype is primarily constrained by the On/Off switching mechanism in the modulator, with the switching speed limited by a rise/fall time of 100 ns. However, state-of-the-art (SoA) modulator designs employ alternative mechanisms that do not have this limitation (Section III.F).

The retrieved constellations for up to 256-QAM are depicted in Figure 5.23, where the symbol points are evenly spaced with acceptable EVM values. For 4 to 64-QAM modulations in Figure 5.23, TX units U1, U3, U5, and U7 are active. For higher modulation orders, including 128-QAM and 256-QAM, as described in Section III.G, TX unit U8 with 1/4th LO power is incorporated in the transmission.

To evaluate the physical layer security features of the proposed topology, a 64-QAM modulated signal is transmitted, and the receiver is positioned at azimuth angles ranging from –80° to 80° relative to the transmitter's broadside, in 4° increments. The corresponding EVM values were recorded using an oscilloscope and are presented in Figure 5.24. Ideal constellation recovery occurs on the broadside and progressively deteriorates with increasing angular misalignment. The measured values closely match the ideal simulation results for the prototype, demonstrating an angular validity range of 20 ° within with the EVM remaining below -16 dB.

Table 5.5 presents a comparison of the proposed topology with existing works on higher-order

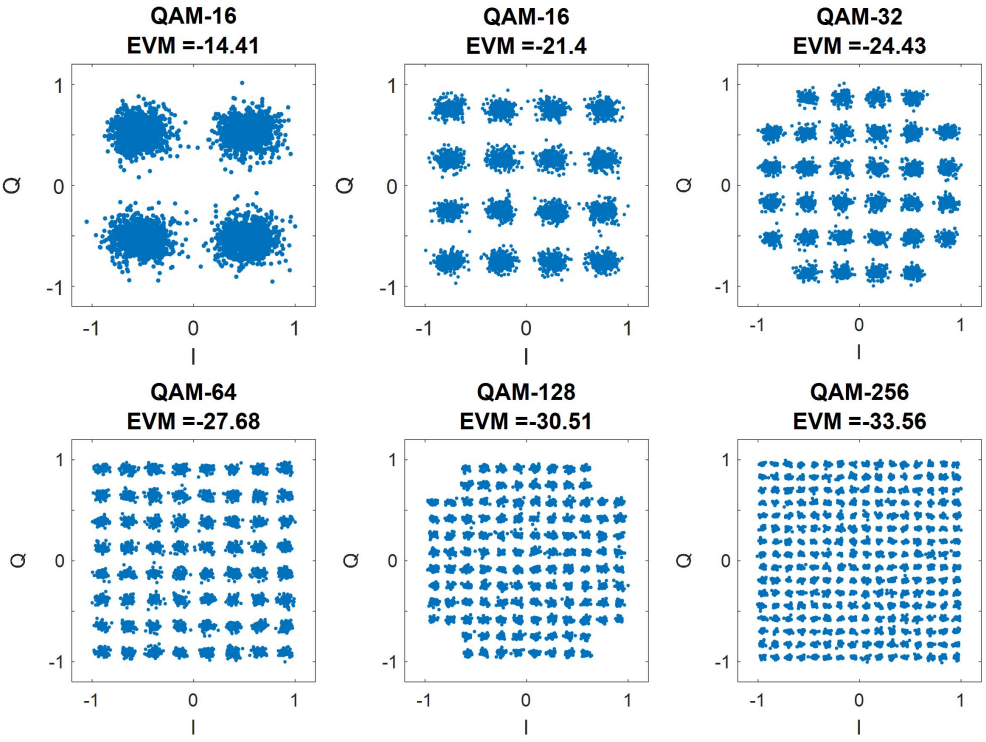


Figure 5.23 Retrieved constellation diagrams of the communication links for various QAM orders under broadside radiation.

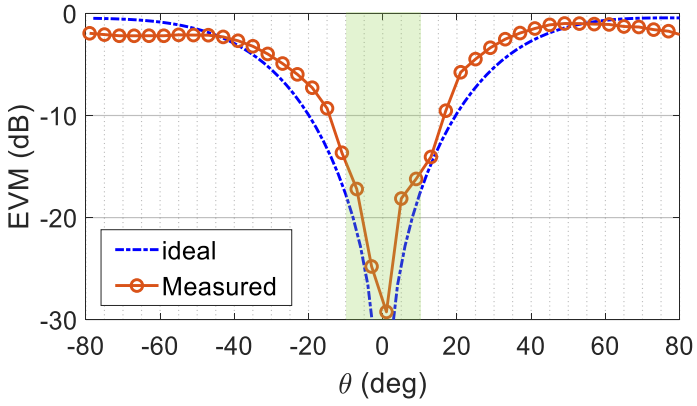


Figure 5.24 Retrieved EVM of a 64-QAM signal as a function of the receiver's azimuth angle deviation from broadside.

modulation formation and physical layer security. In the proposed topology, the increased number of contributing TX units, especially when utilizing a low modulation order like QPSK, enables a combination of beamforming, enhanced physical layer security, and flexible high-order QAM capabilities. This makes the approach particularly advantageous for power-efficient implementations.

5.5 Conclusion

This paper introduces a direct-RF topology utilizing QPSK TX units, designed to optimize power efficiency, structural compactness, and architectural simplicity, making it particularly suitable for large array implementations. The beamforming characteristics of the array, enhanced through spatial power combination and the proposed phase positioning of TX unit cells, are analyzed to improve side lobe levels (SLL) and the retrieval validity angle. The impact of error sources such as radiation pattern deviations and LO distribution imperfections is investigated, demonstrating a robust resilience with respect to these errors. A proof-of-concept prototype capable of generating 4 to 256-QAM constellations has been developed, and measurement results confirm the effectiveness of the proposed concept, showing high accuracy in constellation formation within the intended radiation angle.

Table 5.5 Comparison with state-of-the-art architectures.

Metrics	**This Work**	[225]	[230]	[251]	[245]	[227]	[249]
Physical layer security	Constellation distortion at off-axis angles	Constellation distortion at off-axis angles	No	Constellation distortion at off-axis angles	Time modulation/ spectral aliasing	Antenna switching subset	Time modulation/ spectral aliasing
Constellation Formation method	Variable number of similar QPSK combination	PA digital modulation, I/Q spatial combination	3 Direct-QPSK with dissimilar amplitudes combination	QPSK and 16-QAM combination	Conventional[a]	Conventional	Conventional
Direct-RF	QPSK	BPSK	QPSK	NO	NO	OOK*	NO
Target Modulation	4 to 256-QAM	4 and 16-QAM	64-QAM	64-QAM	N/A	SO-ASK	BPSK
Combination method	Spatial	Spatial	On Board	Spatial	Spatial	Spatial	N/A

[a] Using DAC for generating IF feed signal to the transmitter.
* On/Off Keying.

CHAPTER 6 ARTICLE 5: A PHASE SHIFTER-LESS ANALOG BEAMFORMING TOPOLOGY FOR LARGE RECEIVER ARRAYS—A PROOF OF CONCEPT

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Abstract: This paper proposes and demonstrates a low-power, phase shifter less analog beamforming topology customized for large active receiver (RX) arrays. The phased array topology includes a local down-conversion stage to each antenna. In-phase (I) and quadrature-phase (Q) local oscillator (LO) signals are distributed in a zigzag pattern across the array, forming two interleaved groups of I and Q receivers that implement a distributed direct quadrature demodulation topology. The proposed beamforming topology is based on the selective activation of RX units and incorporates polarity rotation and on/off switching stages applied to the received intermediate-frequency (IF) signals. Operating at the IF stage ensures consistent performance regardless of RF/LO frequencies and enables the use of compact, low-power, and robust circuitry. A comprehensive analysis is presented, addressing key performance factors such as channel orthogonality, array size scalability, and beamforming and power efficiency. To validate the proposed technique, a 2×8 array proof-of-concept prototype operating at 10 GHz is presented. Measurement results confirm robust performance across scanning angles of ±50°, consistent with theoretical predictions. Advantages such as scalable building blocks, superior power efficiency, and simplicity make the proposed topology a strong candidate for next-generation millimeter-wave (mmWave) and terahertz (THz) high-data-rate, large-array applications.

6.1 Introduction

The increasing demand for millimeter-wave (mmWave) and terahertz (THz) frequency bands is driven by the deployment of fifth-generation (5G) wireless networks and the anticipated evolution toward beyond-5G (B5G) and 6G communication technologies. These frequency bands are geared toward enhanced integration, augmented multifunctionality, and increased bandwidth, enabling high-speed, low-latency, and secure communication [257–266]. In this context, large-scale arrays in massive MIMO phased array variants are expected to play a pivotal role in future wireless networks, particularly through their beamforming capabilities.

Beamforming enables directional, point-to-point radiation, which helps compensate for high free-space path loss and the reduced power efficiency of RF front-end components.

However, conventional large-array wireless systems operating in the mmWave and THz frequency bands face significant challenges in meeting these stringent demands due to inherent limitations in power consumption, heat dissipation, and computational resources [257]. While innovative beamforming techniques have been proposed in the literature, they are either not scalable for operation in mmWave and THz bands or result in high power consumption when implemented in large arrays.

Digital beamforming offers optimal flexibility, performance, and multi-user support; however, its RF front-end complexity and high computational load make it impractical for large arrays, limiting its use to small arrays, base stations, and other fixed applications [259, 267–270]. Alternatively, analog and hybrid beamforming topologies utilize physical phase shifters placed in either the RF or LO signal paths, offering practical solutions for power-limited single-user and multi-user large-array implementations, respectively [271]. However, at mmWave and THz frequencies, the power consumption, limited performance, and size constraints of phase shifters—along with supporting circuitry such as polyphase local oscillators, buffers, and others—become major bottlenecks for scaling in both array size and operating frequency [272–275].

Phase shifting can be implemented along the RF, LO, or IF signal paths, each offering distinct characteristics and trade-offs. RF phase shifting offers low system complexity and relaxed linearity requirements; however, achieving broadband operation while maintaining low power consumption, compact size, and minimal phase-dependent gain variation remains a significant challenge [276]. In contrast, LO phase shifters are simpler to implement and, due to their indirect role in the signal path, introduce fewer distortive effects on the extracted data. To enhance power efficiency in LO-based beamforming systems, several techniques have been proposed—such as oversampling [277], constant-Gm vector modulation [278], and multi-phase mixing [279, 280]—which utilize multi-phase oscillators as alternatives to conventional vector modulator-based phase shifters [281]. However, circuits that require precise multi-phase LO generation are not scalable for large-scale arrays at mmWave frequencies [282]. The architecture proposed in [283] places the phase shifters before the LO multiplication stage for sub-THz beamforming; however, this approach reduces phase resolution and accuracy. IF beamforming is gaining interest in mmWave and THz applications, owing to its low noise, reduced power consumption, and improved RMS phase error performance [284–288]. Despite its advantages, IF beamforming requires a superheterodyne architecture and relatively high IF frequencies to support practical bandwidths. Additionally, its larger footprint poses

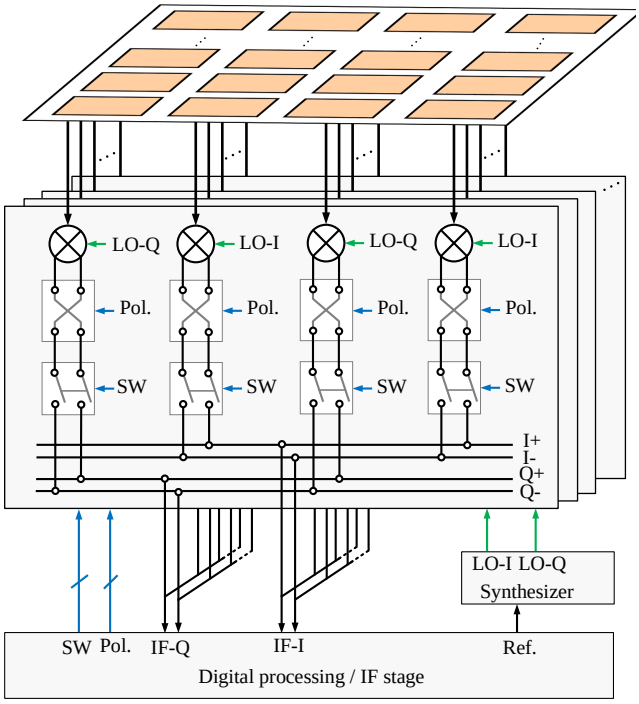
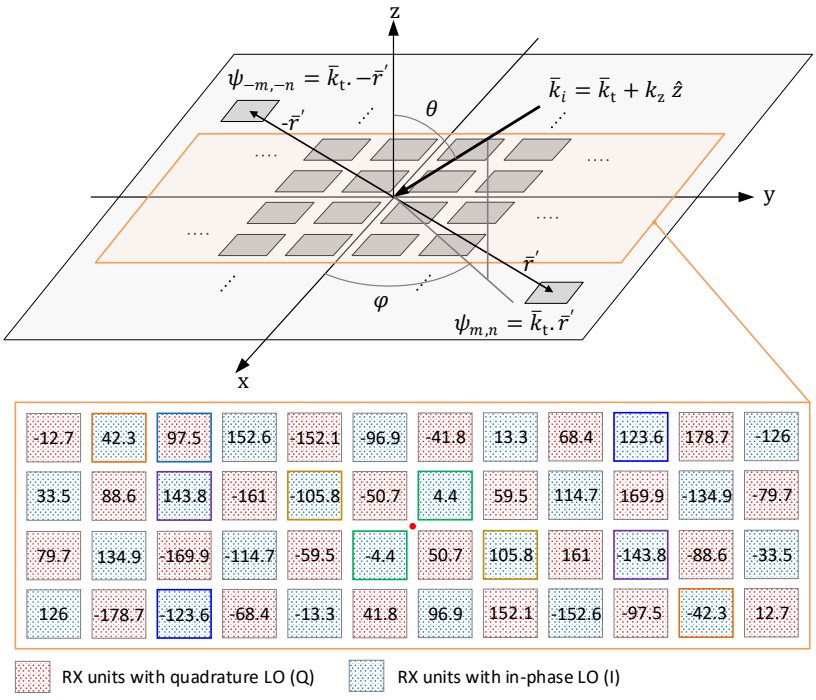


Figure 6.1 Conceptual representation of the presented beamforming topology.

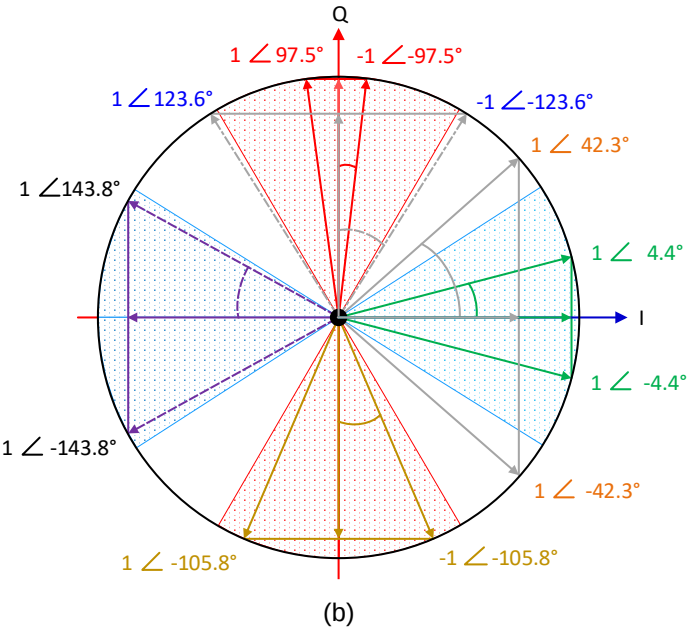
challenges for integration into 2D arrays.

Although phase shifters and beamforming techniques have matured over the years, they remain largely generic solutions optimized for small to moderate array sizes, resulting in cumulative power consumption reaching multi-watt levels in large-scale mmWave and THz arrays. In this work, we propose and demonstrate an IF beamforming topology specifically developed to minimize hardware complexity and power consumption, with performance characteristics specifically tailored for large-array implementations. The proposed scheme operates through selective deactivation of receiver units and polarity rotation functions. This solution eliminates the need for phase shifters and delivers an excellent power-to-performance ratio, enabling fully standalone and scalable large-array receivers.

The remainder of this paper is organized as follows. Section II describes the beamforming principle of operation. Section III presents a system-level analysis of array performance across various scenarios. Section IV presents the proof-of-concept implementation and measurement results, followed by conclusions in Section V.



(a)



(b)

Figure 6.2 Opposite phased antenna pairs and an example phase distribution for a 4×12 array with incident angle $\theta_i = 30°$, $\phi_i = 40°$.

6.2 Principle of Operation

The conceptual representation of the proposed receiver array is provided in Figure 6.1. The down-converted intermediate frequency (IF) signals first pass through a polarity rotation

stage for a selective 180° phase shift. Then, output signals selected to be included in the signal combination are categorized into two groups of in-phase and quadrature phase, implementing a direct-demodulation receiver topology. This topology inherently provides image rejection and supports zero-IF operation, making it suitable for wideband and low-power applications [289]. Beamforming is accomplished by controlling the polarity (Pol.) and On/Off (SW) states (Figure 6.1), based on the target beamforming angle. Considering the general configuration shown in Figure 6.2(a), an incident signal arriving from an arbitrary angle generates an RF phase profile across the array. For a receiver located in the far field of the transmitter, the incident wave can be approximated as a plane wave with constant amplitude and a planar phase front. Such a wave is characterized by a wave vector ($\bar{k}$) and polarization. Based on the desired receiving angle—or through angle-of-arrival (AoA) estimation techniques—the wave vector information can be determined. Accordingly, the corresponding desired or estimated RF signal phase values at each antenna location are calculated as follows:

$$\psi = \bar{k}.\bar{r}' \tag{6.1}$$

where $\bar{r}'$ is a vector from array phase reference to the antenna. The polarization alignment between the receiver antennas and the incident wave affects only the receiving efficiency and is not a limiting factor. Taking the 4×12 sub-array shown in Figure 6.2(a) as an example, with half-wavelength antenna spacing, the RF phase values for an incident angle of $\theta = 30°$, $\phi = 40°$ are calculated using (6.1). Here, the center of the array is used as the phase reference point. The RX units with I- and Q-LO values, highlighted in blue and red, respectively, are arranged in a checkerboard pattern to achieve sequential I and Q LO allocation across the array for maximum uniformity. The polarity (Pol.) and On/Off (SW) states, shown in Figure 6.1, are determined based on the phase deviation between the projected RF phase values and their respective LO phase polarity. For example, the green and purple cell pairs in Figure 6.2(a) exhibit phase deviations of 4.4° and 36.2°, respectively, both of which fall within the acceptable range. According to the graphical representation in Figure 6.2(b), the Pol. value for the purple cell pair is set to 1 (no rotation), allowing it to contribute constructively with the green cells in the IF-I part of the channel. Similarly, the Pol. values for the plausible red and yellow pairs are calculated. Cells with higher LO–RF phase deviation, such as the blue pair, are omitted to deactivate those units and reduce power consumption.

6.2.1 Direct-quadrature receiver operation

Correct retrieval of a quadrature phase–modulated RF signal requires: a) high isolation between the I and Q channels, and b) an acceptable amplitude balance, with $|I/Q| \approx 1$. Establishing phase coherence at the center of the array creates pairs of receiver units with opposite RF phase values. Through phase conditioning via polarity rotation, the vector IF output of each pair aligns to 0° or 90°, corresponding to the I and Q channels, respectively. Therefore, regardless of their absolute phase values, the accumulated IF outputs of the receiver pairs take on only two distinct phases, ensuring orthogonality between the I and Q channels. In Section II, we demonstrate that phase matching is inherently enforced through standard phase-frequency estimation algorithms. It is also worth noting that the beamforming characteristics are preserved in a superheterodyne (nonzero-IF) implementation, as phase synchronization occurs during the secondary mixing stage. As the array size increases, the randomness of the RF phase values also grows, leading to greater distribution diversity. This, in turn, enhances performance robustness across all beamforming angles. The phase rotation mechanism and IF output generation are detailed in Subsection B.

6.2.2 IF Generation

The receiver units in each group are hard-wired to collectively form the I and Q channels of the array. As shown in Figure 6.2, within each group, every two receivers with opposite RF phases are processed as a pair. The total IF power in each channel is calculated by summing the outputs of these receiver pairs within each group. The RF signal at the location of each pair is represented as follows:

$$\begin{aligned} A_{\text{RF-1}}(t) &= a(t)\cos\Big(\omega t + \phi(t) + \theta\Big), \\ A_{\text{RF-2}}(t) &= a(t)\cos\Big(\omega t + \phi(t) - \theta\Big) \end{aligned} \tag{6.2}$$

where θ is the RF phase deviation relative to the reference. Assuming $A_{\text{LO}}(t) = a_{\text{LO}}\cos(\omega t + \phi_0)$, the resulting IF outputs of the receivers are given by:

$\phi_0 = 0^\circ$ (I):

$$A_{\text{IF-1}}(t) = \frac{\alpha a(t)}{2}\Big[\cos\Big(\phi(t)\Big)\cos(\theta) - \sin\Big(\phi(t)\Big)\sin(\theta)\Big],$$
$$A_{\text{IF-2}}(t) = \frac{\alpha a(t)}{2}\Big[\cos\Big(\phi(t)\Big)\cos(\theta) + \sin\Big(\phi(t)\Big)\sin(\theta)\Big] \tag{6.3}$$

$\phi_0 = 90^\circ$ (Q):

$$A_{\text{IF-1}}(t) = \frac{\alpha a(t)}{2}\Big[\sin\Big(\phi(t)\Big)\cos(\theta) + \cos\Big(\phi(t)\Big)\sin(\theta)\Big],$$
$$A_{\text{IF-2}}(t) = \frac{\alpha a(t)}{2}\Big[\sin\Big(\phi(t)\Big)\cos(\theta) - \cos\Big(\phi(t)\Big)\sin(\theta)\Big] \tag{6.4}$$

where α is the mixing coefficient. From (6.3) and (6.4), by applying the same polarity switching to both receivers in a pair, we obtain the phase-corrected accumulated IF outputs from a receiver pair, as shown in (6.5).

$$I: \quad A_{\text{IF}}(t) = \alpha\, a_{\text{RF}}(t)\cos\Big(\phi(t)\Big)\cos(\theta),$$
$$Q: \quad A_{\text{IF}}(t) = \alpha\, a_{\text{RF}}(t)\sin\Big(\phi(t)\Big)\cos(\theta). \tag{6.5}$$

The $\cos(\theta)$ term represents the effect of RF–LO phase deviation. The value of θ determines the power efficiency of each receiver unit and serves as the metric for deactivating units. A 45° phase deviation causes a 50% IF power loss, while an extreme deviation of $\theta = 90^\circ$ results in zero IF output (Figure 5). A thorough system analysis of receiver performance and efficiency is provided in Section III.

6.3 System Analysis

6.3.1 Phase-Frequency Synchronization

The formulation in Section II assumes an asymmetric RF phase distribution centered around the array's midpoint. However, the initial RF phase is a random value. In a synchronous link utilizing feedback systems—such as a Costas loop—the phase-locked loop (PLL) within the receiver adjusts the voltage-controlled oscillator (VCO) phase to enable accurate separation of the I and Q data components [290]. A conventional quadrature receiver evenly splits the incoming IF signal between the I and Q channels, causing both paths to experience identi-

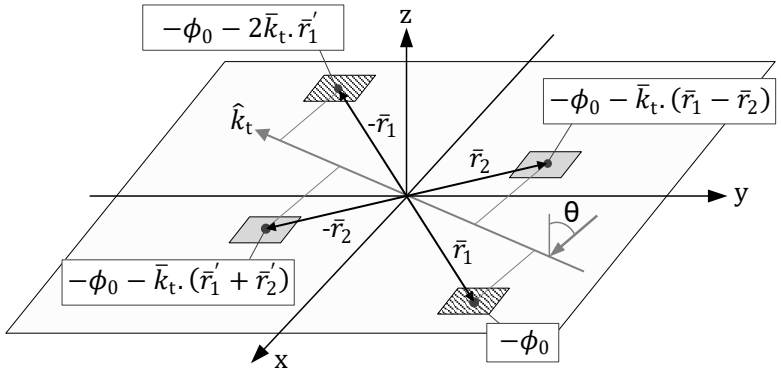


Figure 6.3 RF phase propagation from random point to antenna points.

cal phase mismatches that can be jointly compensated. To enable a similar compensation strategy within the proposed receiver configuration, the accumulated IF signals in the I and Q channels must exhibit comparable phase mismatch characteristics.

In this context, consider one receiver pair from each of the I and Q groups. Under plane-wave incidence, the RF signal phase exhibits a linear progression across the array elements. Taking an arbitrary reference point, the RF phase at each antenna element is illustrated in Figure 6.3. The phase at each antenna is determined by its relative position along the transverse wave vector ($\bar{k}_t$) with respect to the chosen reference. By combining the IF signals from the corresponding receiver pairs in the I and Q groups, we obtain:

$$
\begin{aligned}
&A_{\text{IF-}I,Q}(t) = 2a_{RF}(t)\cos\Big(\phi(t) + \phi_{I,Q}\Big),\\
&\phi_I = \Big(-\phi_0 + (-\phi_0 - 2\bar{k}\cdot\bar{r}_1)\Big)/2,\\
&\phi_Q = \Big((-\phi_0 - \bar{k}\cdot(\bar{r}_1 - \bar{r}_2)) + (-\phi_0 - \bar{k}\cdot(\bar{r}_1 + \bar{r}_2))\Big)/2.
\end{aligned}
\tag{6.6}
$$

In (6.6), ϕ_I and ϕ_Q are constant phase values, and they are equal for both the I and Q channels at any arbitrary incidence angle ($\bar{k}$) and for any receiver pair locations. This result can be extended to multi-receiver operation, since the phase component remains identical across all pairs, while IF accumulation affects only the amplitude.

6.3.2 Array Power Consumption and Beamforming Efficiency

Figure 6.4(a) illustrates the RF phase distribution for an incident angle of $\theta_i = 25°$, $\phi_i = 60°$. The RF–LO phase deviation (θ) directly affects the generated IF signal power and,

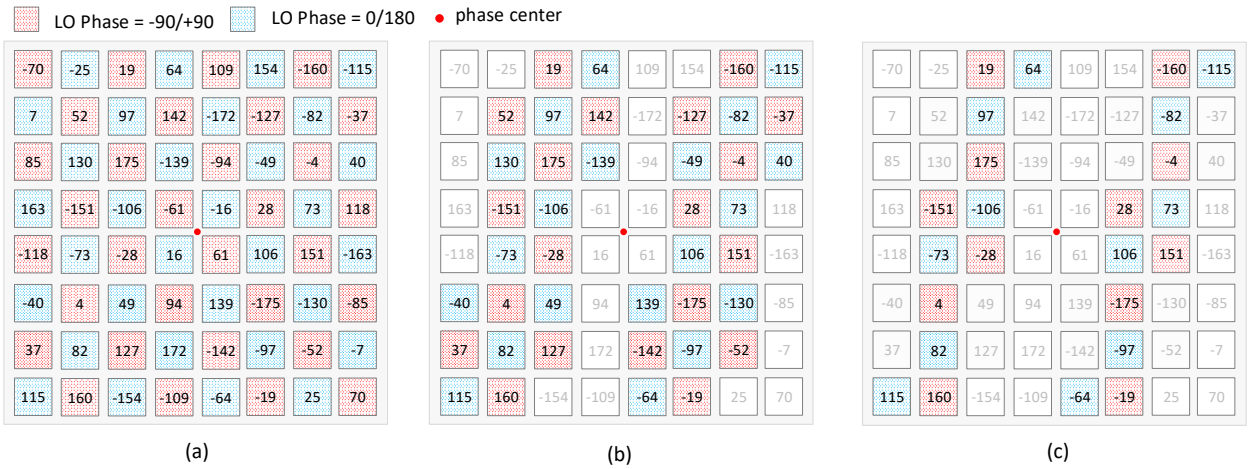


Figure 6.4 (a) RF phase distribution for incidence angle $\theta = 30°$, $\phi = 60°$. (b) Active receiver units for $\theta_c = 60°$. (c) Active receiver units for $\theta_c = 30°$.

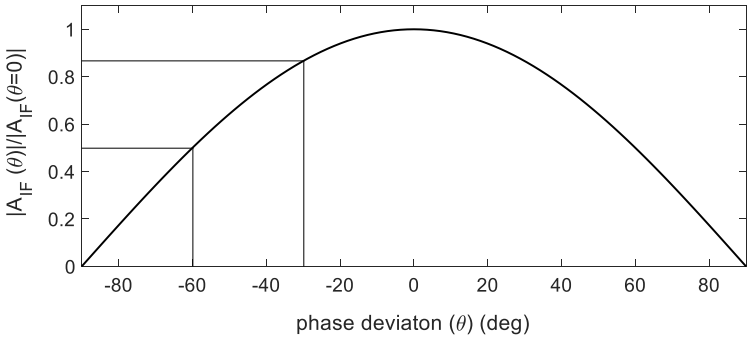


Figure 6.5 Receiver power efficiency as a function of RF–LO phase deviation.

consequently, the efficiency of each receiver unit. The relationship between receiver efficiency and phase deviation is depicted in Figure 6.5. Perfect phase alignment ($\theta = 0°$) corresponds to 100% efficiency, which gradually decreases to 0% as θ approaches 90°. Thus, phase deviation can serve as a selection criterion for deactivating inefficient receiver units.

As shown for an 8×8 array in Figure 6.4(b) and Figure 6.4(c), more than 80% and 40% of the receivers remain active when the phase deviation threshold (θ_c) is set to 60° and 30°, respectively.

Factoring the modulated signal $a(t)\cos\Big(\phi(t)\Big) + a(t)\sin\Big(\phi(t)\Big)$ out of (6.5) for the array, the array factor (AF) is defined as:

$$AF(\theta_c) = \sum_{\theta_i < \theta_c} \cos(\theta_i) \; + \sum_{\theta_j < \theta_c} \cos(\theta_j) \tag{6.7}$$

where θ_i and θ_j denote the RF–LO phase deviations across the I and Q receiver elements,

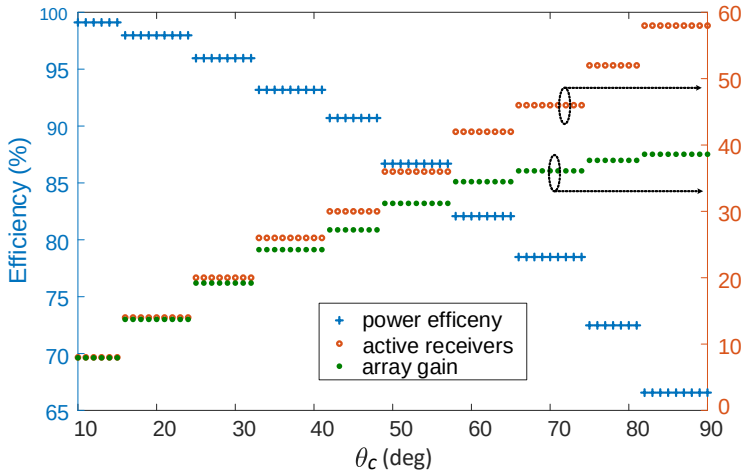


Figure 6.6 Beamforming efficiency and array factor as functions of θ_c.

respectively. Based on this, the *beamforming efficiency* is defined as the ratio of the achieved IF signal to that of an ideal phased array with the same number of active receivers.

$$\mathrm{Eff}(\theta_c) = \frac{AG(\theta_c)}{AG(\theta_c)\big|_{\theta_i=\theta_j=0}} \tag{6.8}$$

Here, the denominator corresponds to the case of zero phase deviation in the array factor calculation in (6.7). The definition in (6.8) therefore quantifies the beamforming loss relative to the ideal case.

The selection of the acceptable RF–LO phase deviation threshold (θ_c) involves trade-offs among IF power, power efficiency, and beamforming accuracy. This threshold can be optimized according to the requirements of a specific application. For example, meeting a stringent link budget may necessitate activating more receivers, which can result in reduced beamforming efficiency. Figure 6.6 illustrates the variation of the array factor and beamforming efficiency with θ_c for a sample incidence angle of $\theta_i = 30°$, $\phi_i = 60°$ on an 11×11 array. At low deviation tolerance, high beamforming efficiency is achieved. As the deviation angle increases, the effective down-converted IF signal from each receiver diminishes, leading to a gradual decline in overall efficiency, while the array gain approaches saturation. At a minimum, an efficiency of 65% (corresponding to approximately 40% power efficiency) is achieved for the 11×11 array when all 60 receivers in each group are activated. The step-like variations observed in Figure 6.6 arise from the fixed configuration of active receivers over small increments in θ_c; during these intervals, the deactivated receivers do not meet the activation criteria as θ_c increases.

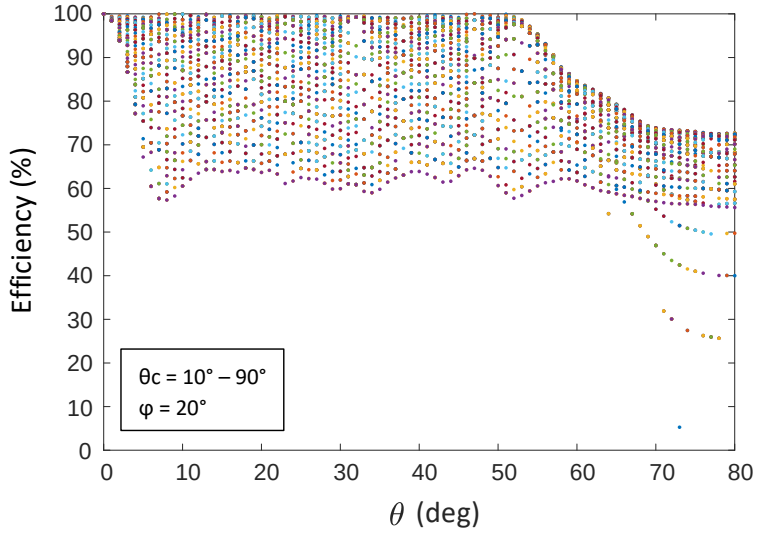


Figure 6.7 Beamforming efficiency as a function of elevation incidence angle (θ) for various phase deviation thresholds (θ_c).

The efficiency behavior is largely independent of the incident angle. Figure 6.7 illustrates the efficiency across elevation incidence angles ranging from 0° to 80°, evaluated for various practical deviation threshold values. The upper and lower data points correspond to small and large deviation angle limits, respectively. Consistent with the incident angle study in Figure 6.6, the efficiency remains above 60% for incidence angles below 60°. Near normal incidence, where phase variation across the array is minimal, optimal efficiency is maintained regardless of the phase deviation threshold. The dependency on the azimuth incidence angle (ϕ) is negligible compared to the already weak dependence on the elevation angle. Intuitively, this low angle dependency arises from (a) the large phase variation between antenna elements (e.g., approximately 40° at $\theta_i = 30°$) and (b) the large array size, which, combined with the semi-random nature of the phase distribution, contributes to robustness.

6.3.3 Quadrature Amplitude Balance

Typically, quadrature amplitude modulation (QAM) schemes in commercial applications require the amplitude imbalance between the I and Q channels to be less than 1 dB [289,291]. In the proposed architecture, the uniform distribution of I and Q receivers across the array inherently ensures good amplitude balance, regardless of the incidence angle or the selected θ_c. Without any fine-tuning of the selected receivers, an amplitude imbalance of less than 1 dB can be achieved. However, by leveraging RF phase distribution information, a fine-tuning procedure can be applied to further improve amplitude balance. For instance, Figure 6.8

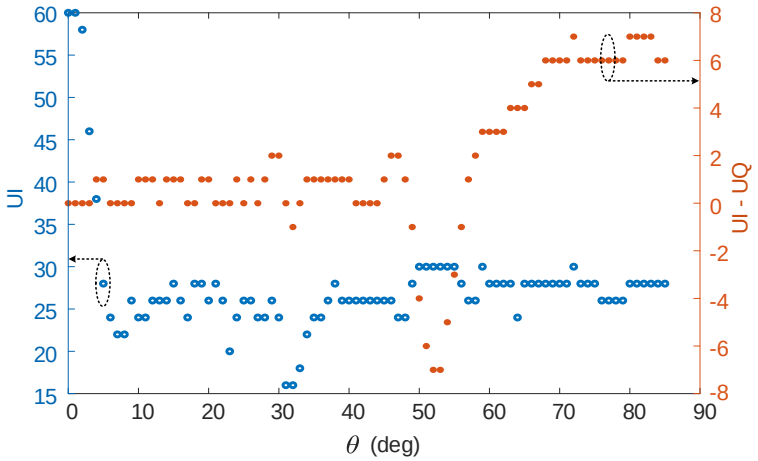


Figure 6.8 Number of active receivers for the I (UI) and Q (UQ) receiver groups in an 11×11 array with $\theta_c = 30°$.

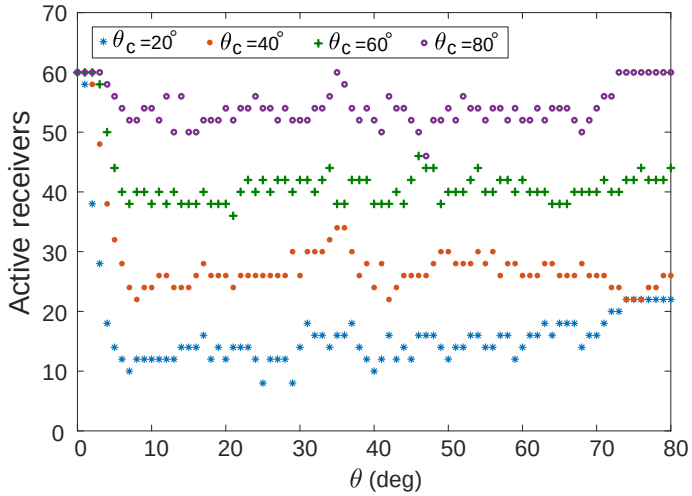


Figure 6.9 Number of active receiver elements in the case-study 11×11 array for different phase deviation thresholds (θ_c) over elevation incidence angle values.

illustrates the number of active receivers across various incidence angles for a fixed $\theta_c = 30°$. Taking the number of active receivers in the I channel (U_I) as a reference, the number of active receivers in the Q channel (U_Q) is adjusted accordingly to balance their respective IF amplitudes. This adjustment involves deactivating the least efficient active receivers and activating the most efficient inactive ones.

Figure 6.9 demonstrates performance independence by showing the number of active receivers across various incidence angles. For a given phase deviation threshold (θ_c), the number of active elements remains consistent across all practical incidence angles. This consistency ensures high IF power and a high signal-to-noise ratio (SNR) at the receiver while maintaining

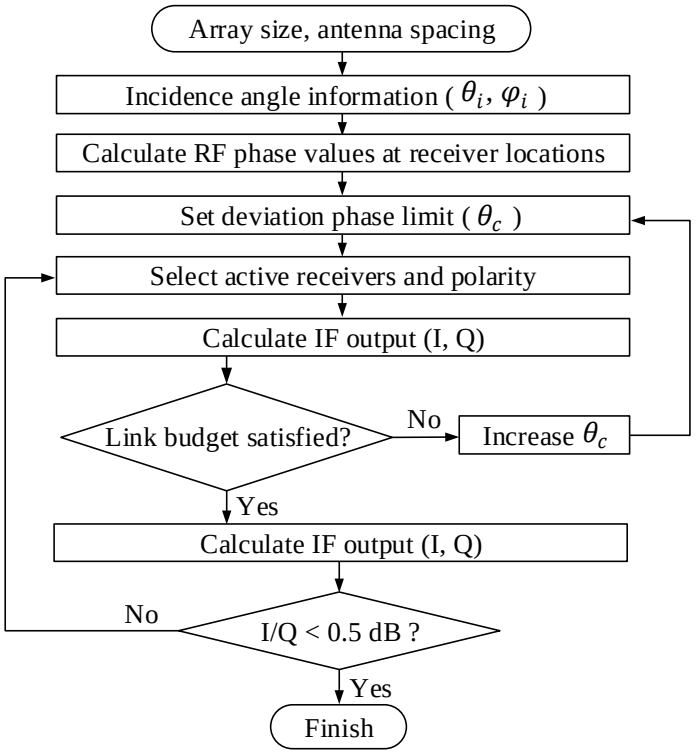


Figure 6.10 Activation and polarity selection algorithm in the proposed topology for a target beamforming angle.

efficiency. Consequently, similar to an ideal phased array, the system achieves high array gain with efficient beamforming for all practical incidence angles.

For incidence angles up to 45°, only minimal modifications, involving the addition or removal of one or two receivers, are needed to achieve amplitude balance. Following the descriptions presented thus far, the flowchart in Figure 6.10 summarizes the process of active element selection followed by fine-tuning. The resulting I/Q amplitude balance for 11×11 and 7×7 arrays across all incidence angles is shown in Figure 6.11. The larger array provides greater phase distribution randomness and increased flexibility in selecting contributing receivers, resulting in improved amplitude balancing performance. The ability to selectively deactivate receivers using low-complexity processing and cost-effective circuitry allows the system to achieve signal quality comparable to that of conventional quadrature receivers.

6.3.4 Array Pattern

Beamforming in a phased-array receiver primarily serves to (a) provide high gain, (b) suppress grating lobes, and (c) enable integrated adjustability for link-budget optimization. To evaluate beamforming in the proposed topology, we follow the logic outlined in Figure 6.10.

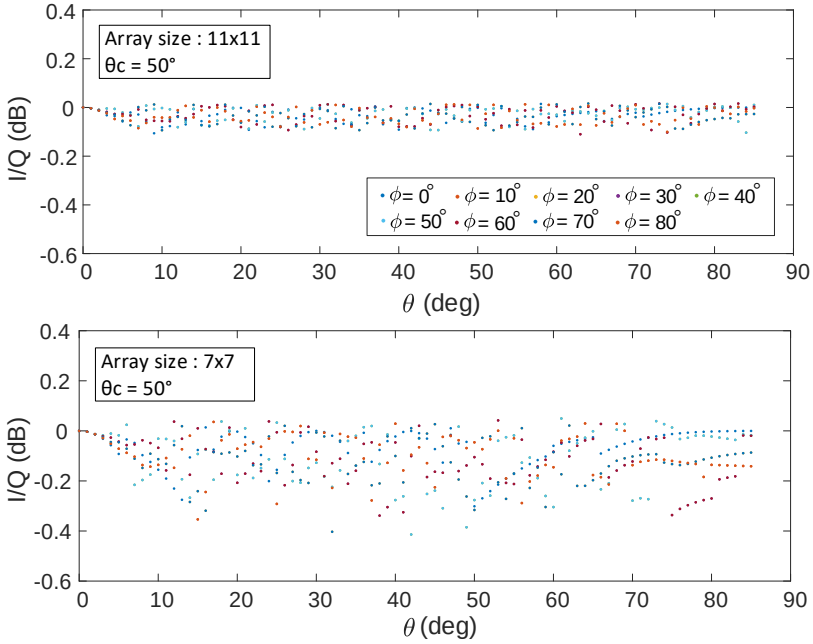


Figure 6.11 I/Q amplitude balance for 11×11 and 7×7 arrays under various incidence angles.

Table 6.1 Average beamforming loss for a 10×10 array under various phase deviation thresholds.

θ_c (deg)	40	50	60	70	80
Loss (dB)	3.78	3.06	2.61	2.23	2.00

First, the active receivers and their corresponding polarities are selected based on the desired beamforming angle. Then, using this fixed RX configuration, the IF signal is computed across all incidence angles.

The general beamforming characteristics of the proposed method are illustrated in Figure 6.12 using a sample beamforming angle of $\theta_i = 30°$, $\phi_i = 110°$, with a deviation threshold of $\theta_c = 50°$, and are representative of all beamforming angles. The radiation pattern exhibits grating-lobe-free directional radiation. However, the sidelobe level is generally higher compared to that of an ideal phased array, primarily due to the sparse distribution of active RX units across the array (as shown in Figure 6.4). The target beamforming angle is achieved with high accuracy; however, slight deviations may occur at certain angles due to the limited number of RF-phase sampling points across the array.

The radiation patterns for different numbers of activated receivers, corresponding to various angle deviation thresholds (θ_c) for the sample beamforming angle shown in Figure 6.12, are depicted in Figure 6.13. A lower θ_c activates fewer receivers, resulting in a reduced array

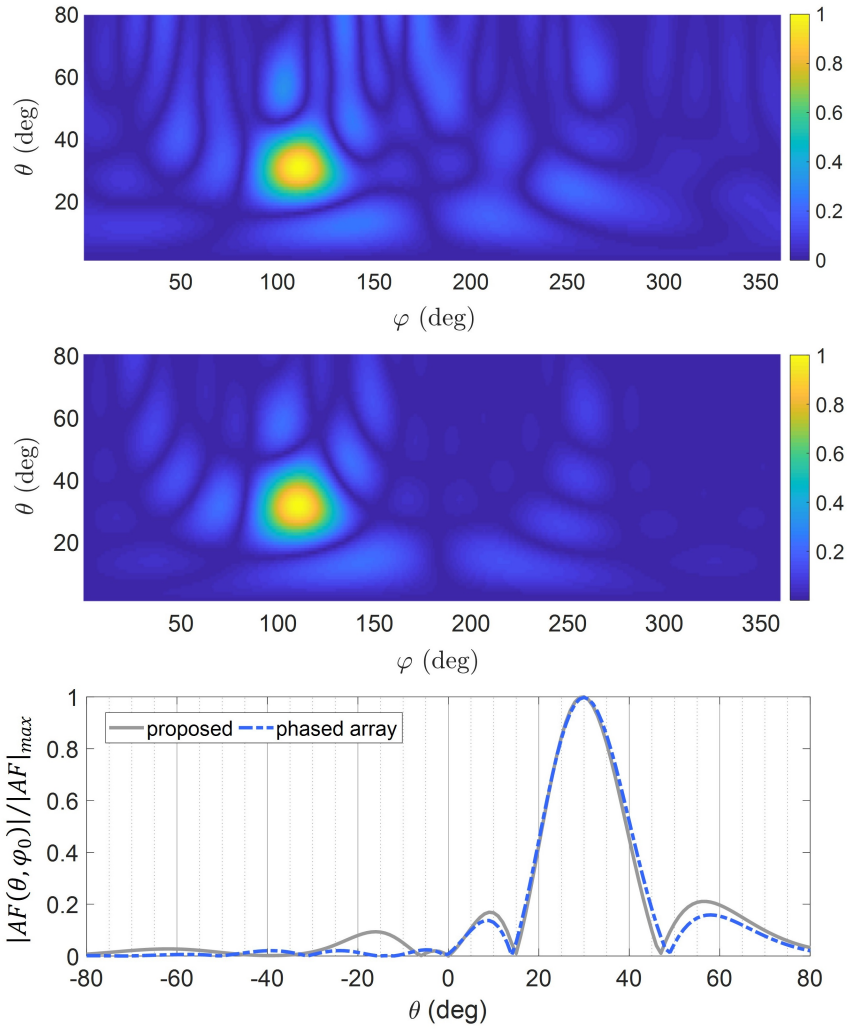


Figure 6.12 Beamforming comparison between the proposed technique and an ideal phased array of the same size for an incidence angle of $\theta_i = 30°$, $\phi_i = 110°$.

gain. However, the beamwidth remains consistent across all θ_c values, as it primarily depends on the array's electrical size. The gain drop is quantified as a loss value and presented in Table 6.1, representing the decrease relative to a fully activated phased array. A gain loss ranging from approximately 2 dB to 4 dB is observed, consistent across all beamforming angles.

A small peak and null-point variation is visible in Figure 6.13 due to the different subsets of RX units contributing to beamforming. This effect is examined in Figure 6.14(a) for various elevation angles (θ) and θ_c values. The deviation values remain below 15% of the half-power beamwidth (HPBW) in most cases and decrease with increasing θ_c. As shown in Figure 6.14(b), such deviations contribute to additional loss. For the majority of θ values, the

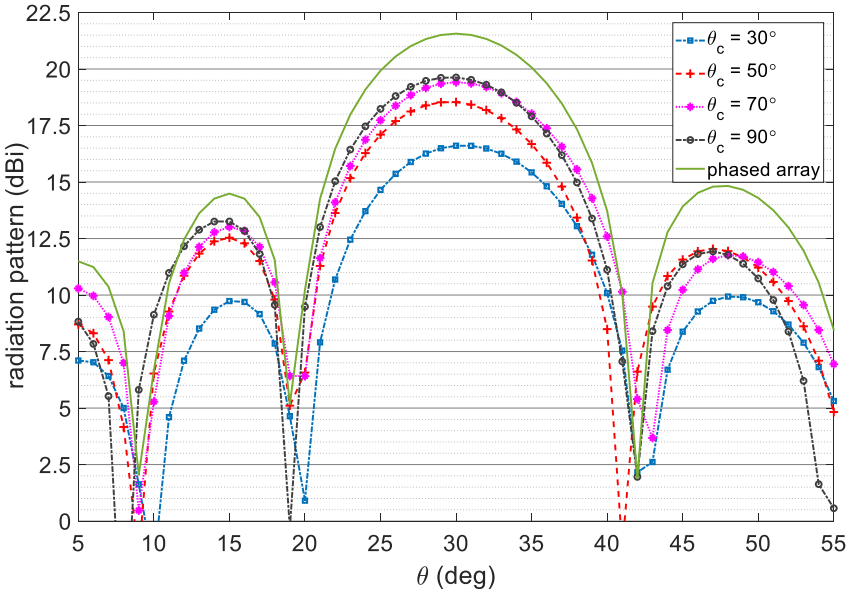


Figure 6.13 Radiation pattern comparison and array factor variation (dB) for different θ_c values at an incidence angle of $\theta_i = 30°$, $\phi_i = 110°$.

deviation and associated loss remain below a negligible 3% (< 0.2 dB). It is worth noting that increasing the array size reduces the HPBW, which in turn decreases the absolute deviation. Figure 6.14(c) compares the HPBW values of the proposed technique with those of an ideal phased array of the same size, showing a similar HPBW increase with beamforming angle (θ). This trend aligns with the identical beamwidth observed in Figure 6.13.

The number of bits in digital phase shifters determines the phase-shift resolution and precision, thereby limiting the number of beamforming directions. While this is not a significant issue for small array sizes, it becomes problematic as the array size increases, since the beamwidth narrows and higher phase resolution is required, demanding more complex and power-hungry phase shifters [272–275]. In contrast, the proposed topology inherently avoids this limitation, as beamforming angle accuracy improves with increasing array size (see Figure 6.14(a) and (b)).

High sparseness in an array leads to the formation of grating lobes. Similarly, in the proposed topology, as illustrated in Figure 6.4, reducing θ_c effectively limits the array to oblique strips of active regions, spaced proportionally to the transverse wavelength $\lambda_t = k_t/2\pi$. Figure 6.15 compares beamforming in a 12×12 array for a sample incidence angle under different θ_c values. Reducing θ_c from 50° to 10° gradually introduces and amplifies grating lobes in the radiation pattern. In this context, the trade-off between efficiency and performance can be tuned based on specific application requirements, such as in communication, radar, or power-constrained systems (see Figure 6.6).

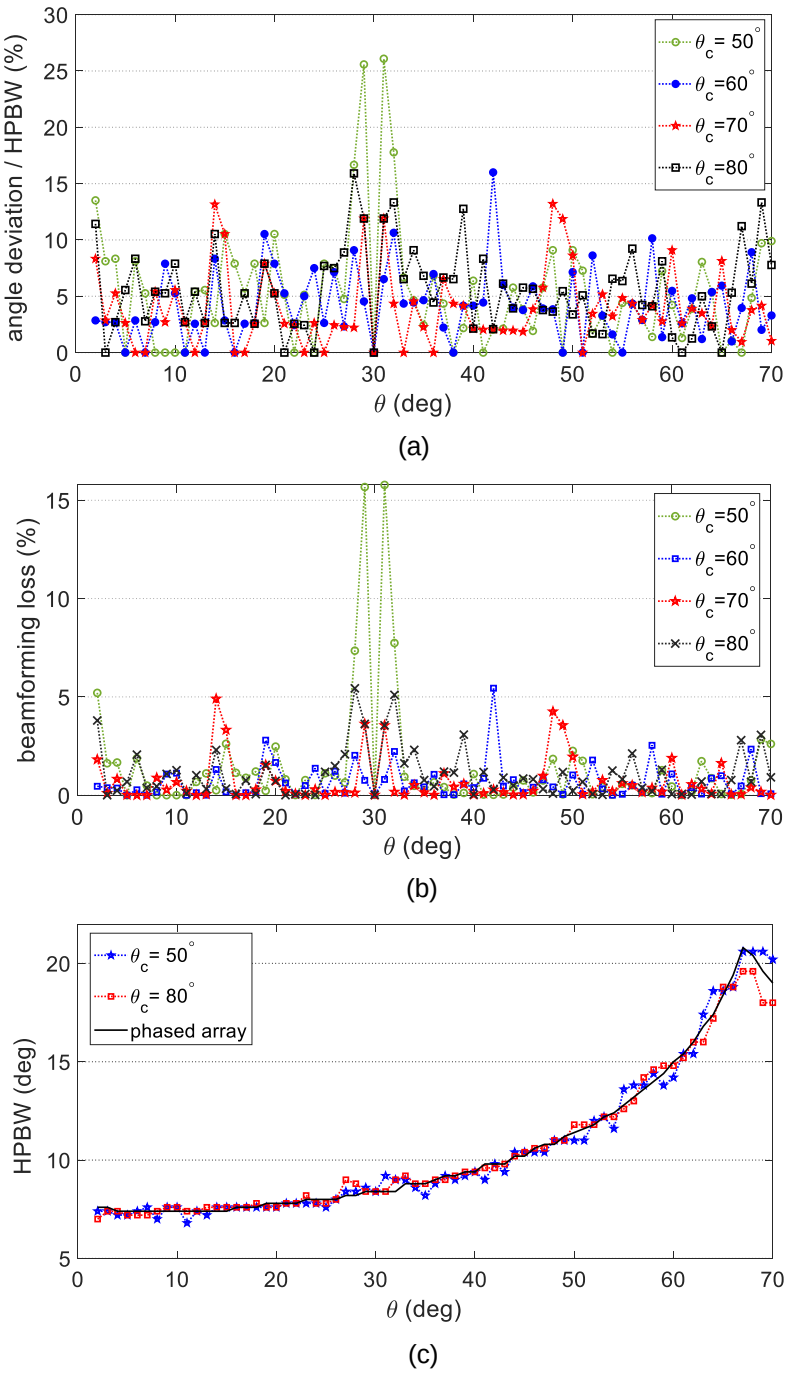


Figure 6.14 Beamforming characteristics of a 10×10 array with half-wavelength element spacing: (a) beamforming deviation from the target angle, (b) associated power loss due to the deviation, (c) half-power beamwidth (HPBW) variation with beamforming angle.

The array size directly affects beamforming performance. Larger arrays introduce higher phase randomness, which specifically improves beamforming angle accuracy. Figure 6.16 presents beamforming patterns for various array sizes under similar θ_c values. In a small

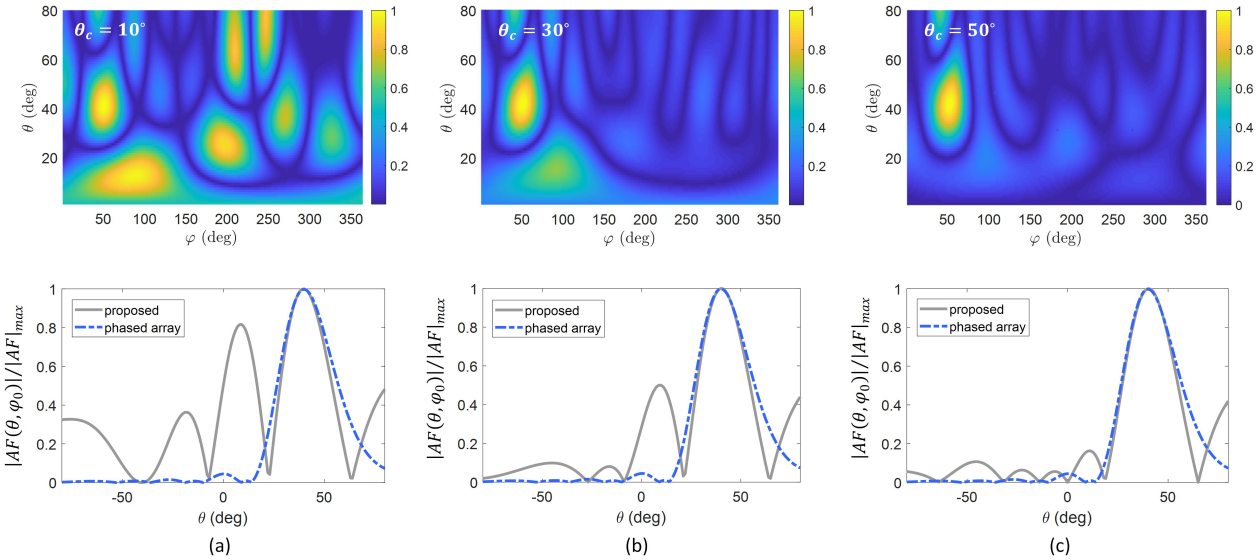


Figure 6.15 Effect of different θ_c values on beamforming performance for a sample beamforming angle of $\theta_i = 45°$, $\phi_i = 50°$, showing increased sidelobe levels and the emergence of grating lobes when $\theta_c = 10°$.

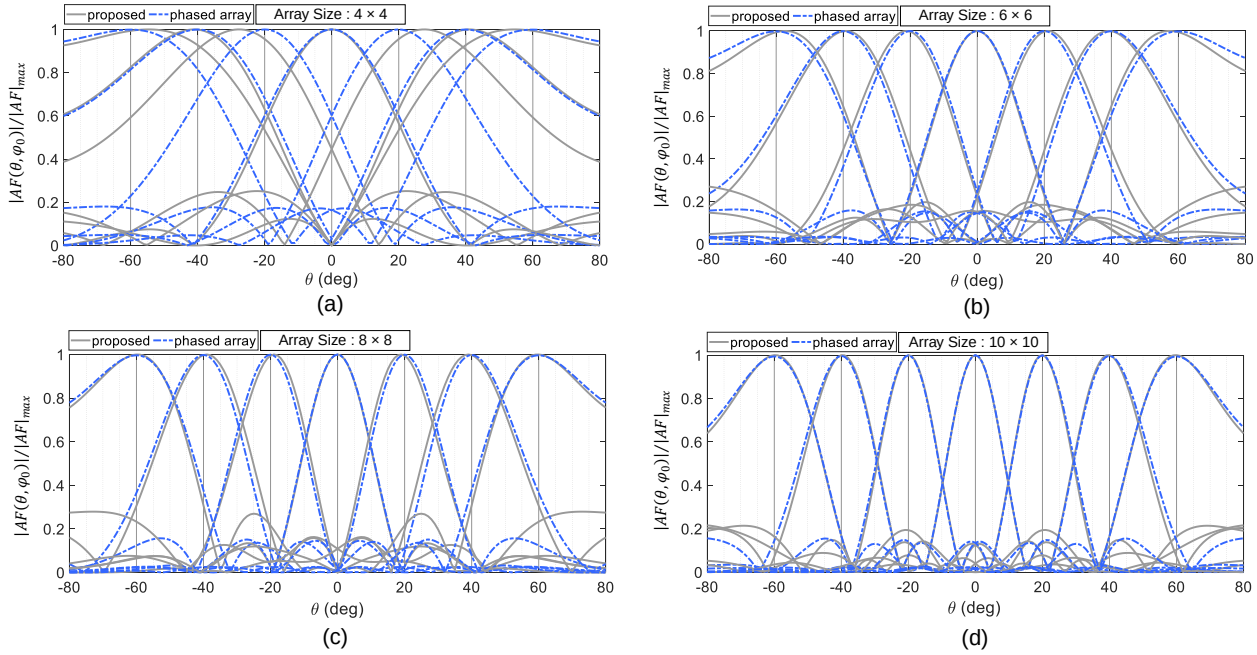


Figure 6.16 Effect of array size on beamforming performance compared with an ideal phased array of the same size for $\theta_c = 60°$.

4×4 array, the availability of RF phase values with $\theta_c = 50°$ limits the range of angles with accurate beamforming. As the array size increases to 12×12, as shown in Figure 6.16(b)–(d), both angle accuracy and sidelobe suppression improve progressively. Unlike conventional

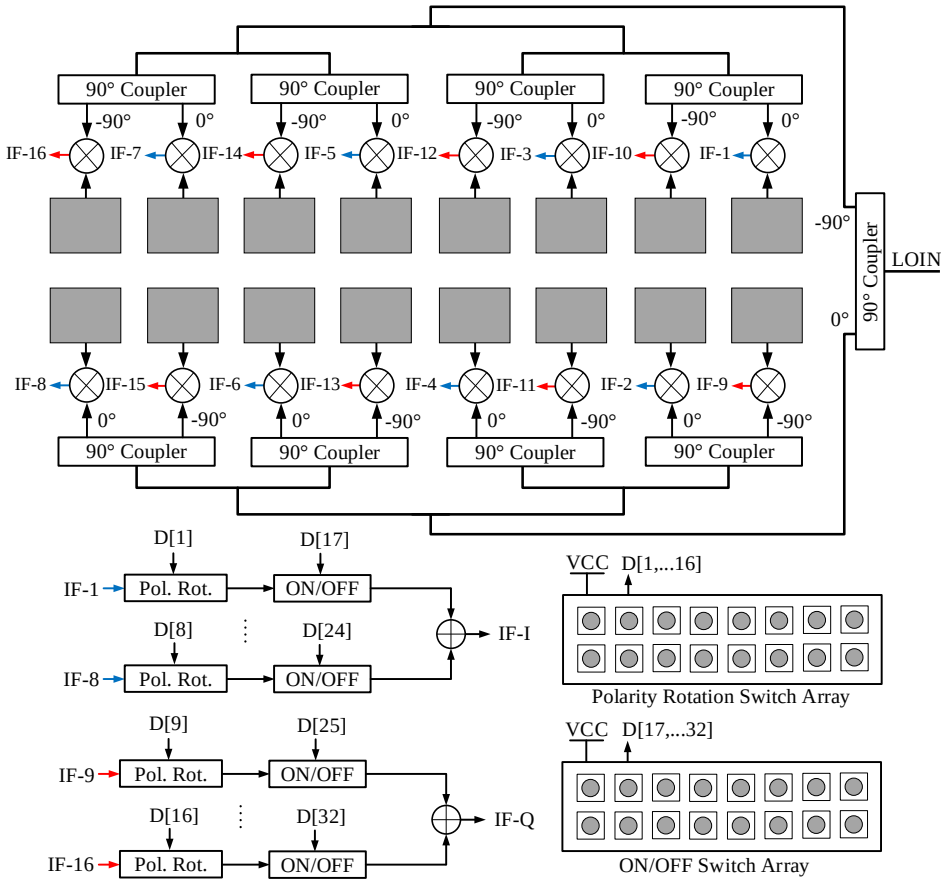


Figure 6.17 Diagram of the proof-of-concept prototype comprising a 2×8 array for 1D scanning, along with switch arrays for On/Off control and polarity selection.

approaches in the literature, the proposed technique exhibits a lower bound on array size for effective operation, with performance that scales positively with increasing array size.

6.4 Proof of Convept Realization and Results

To validate and evaluate the proposed receiver-array beamforming topology, a 2×8 prototype was designed to operate at 10 GHz. The block diagram of the array is shown in Figure 6.17. Rat-race hybrid couplers are integrated into the feed network to generate the zigzag I- and Q-LO phase distribution. Analog Devices HMC220B passive mixers are used to implement the receiver units in a mixer-first topology. Patch antennas are spaced at $\lambda/2.2$ at 10 GHz. The extracted IF signals pass through TI THS4524 operational amplifiers (op-amps), which perform single-ended-to-differential conversion and also function as On/Off switches.

The polarity-rotation stage is implemented using NXP NX3L2467PW DPDT switches. Fi-

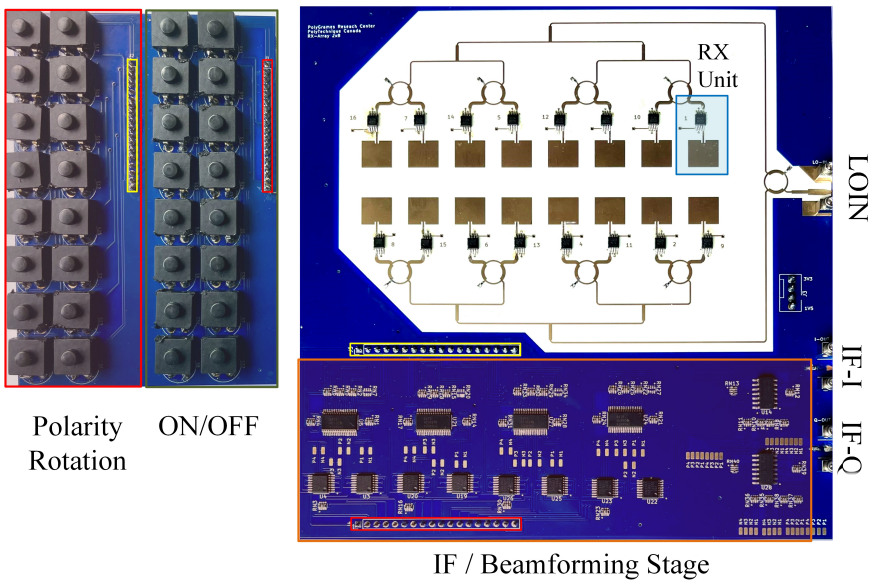


Figure 6.18 Top-view photograph of the fabricated prototype, showing the switch-pad PCB separated from the back of the main PCB.

nally, the I- and Q-channel IF signals are combined using a pair of TI LM224ADR op-amps. A top-view photograph of the proof-of-concept (PoC) prototype is shown in Figure 6.18. The main PCB is implemented on a Rogers RO4003 substrate ($\varepsilon_r = 3.55$) with a thickness of 30 mil. The switch-pad PCB is mounted on the back side of the main PCB via the highlighted connectors.

The antenna and feed-network input matching are shown in Figure 6.19(a) and (b). To ensure optimal performance, measurements were conducted at 9.85 GHz. The feed network was simulated using Ansys HFSS, and the resulting amplitude and phase distributions are presented in Figure 6.19(c) and (d), respectively, showing acceptable deviations of up to 2 dB in amplitude and 16° in phase at 9.85 GHz. Despite the symmetric layout of the feed network, these deviations are attributed to imperfections in the lumped components and variations in boundary conditions.

The measurement setup and connection diagram are shown in Figure 6.20. To measure beam-steering performance, the prototype is programmed for a target beamforming angle using the control switches. A transmitter horn antenna is aligned with the receiver and positioned in the far field—close enough to ensure a high signal-to-noise ratio (SNR) while maintaining a safe transmission power level.

The prototype is mounted on a gated stand that enables precise rotation with a 3° resolution and is surrounded by RF absorbers to minimize reflections. The RF and LO signals are

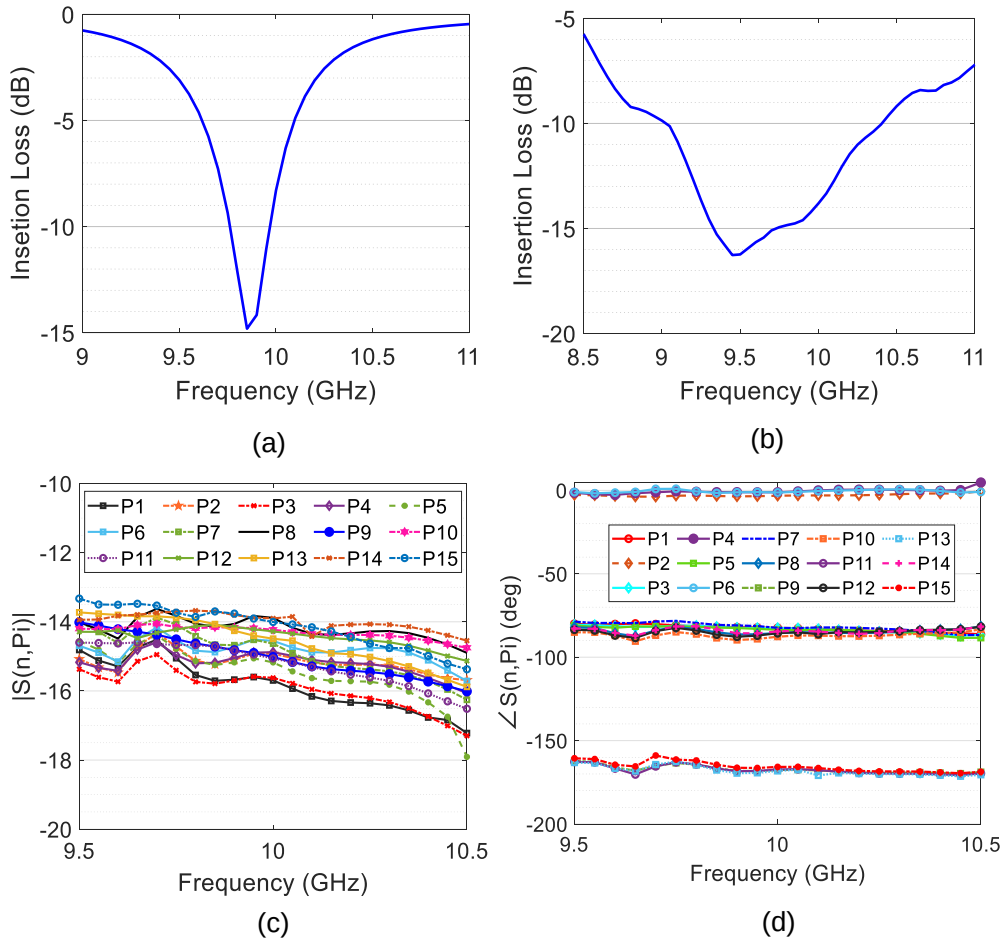


Figure 6.19 (a) Patch antenna input matching. (b) LOIN port input matching. (c) Simulation results of LO power distribution in the feed network. (d) Simulation results of LO phase distribution in the feed network.

generated using an Agilent E8267D vector signal generator and an Agilent E8257D analog signal generator, respectively.

The extracted IF signal at 500 kHz is fed into an Agilent signal analyzer for power measurement. Measurements were conducted for two θ_c values, 60° and 80°, and the results are presented in Figure 6.21. Due to system symmetry, only positive angles (outward from the equipment) were measured. In Figure 6.21, the On/Off status of each RX unit is indicated by 0 (Off) or ±1 (On), where −1 denotes polarity-rotation activation. The measurement results are consistent with theoretical predictions and comparable to those of ideal phased arrays. At higher beam-steering angles, the antenna element factor becomes more significant, leading to reduced power readings. Additionally, elevated sidelobe levels are observed for beamforming angles of 40° and 50°, which can be attributed to increased sensitivity to LO-distribution accuracy within the feed network, as shown in Figure 6.19(c) and (d).

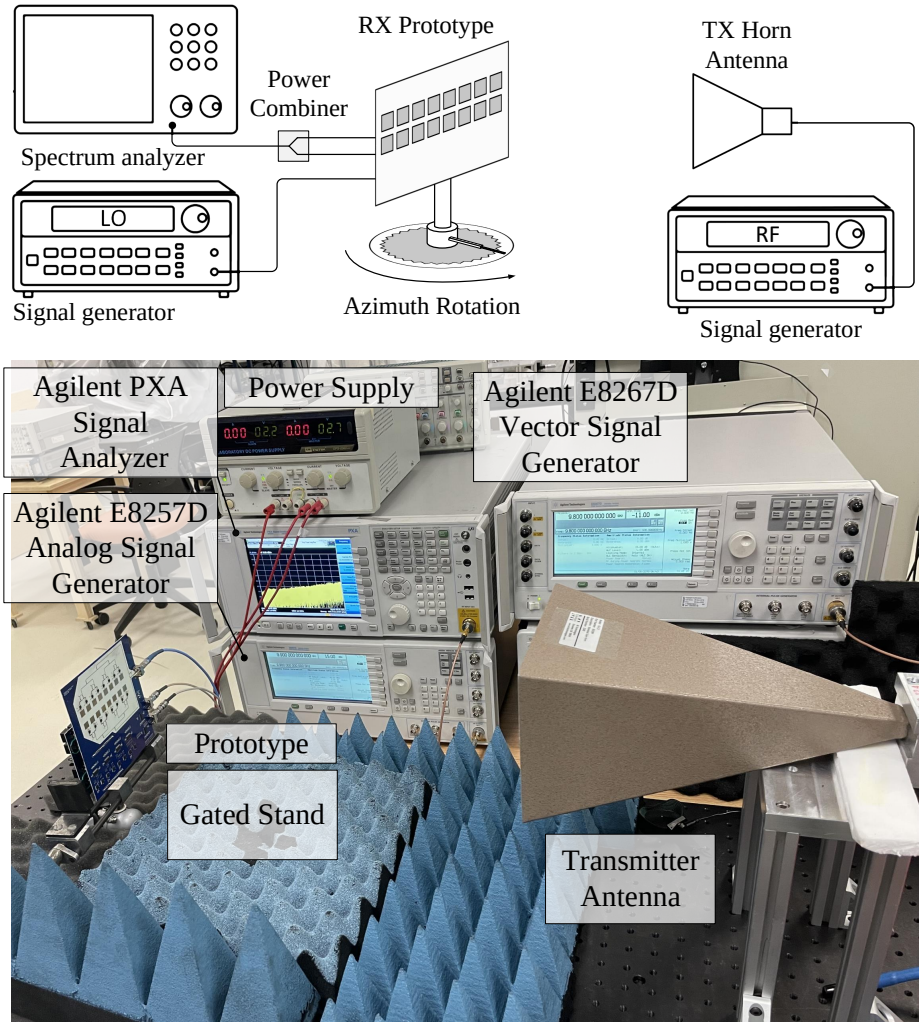


Figure 6.20 Connection diagram and photograph of the measurement setup.

Table 6.2 presents a comparison between the proposed topology and existing beamforming techniques. To the best of the authors' knowledge, this work represents the first phase-shifter-less beamforming approach that is fully compatible with integrated-circuit (IC) technology.

6.5 Conclusion

This article has presented a phase-shifter-less beamforming topology for phased-array receivers, based on intermediate-frequency (IF) signal manipulation using simple switching functions. A comprehensive system-level analysis was conducted, covering key performance aspects such as efficiency, beamforming accuracy, and scalability. By operating entirely in the IF domain and utilizing low-power, low-complexity circuitry in place of traditional phase shifters, the proposed architecture is particularly well suited for large-scale array implemen-

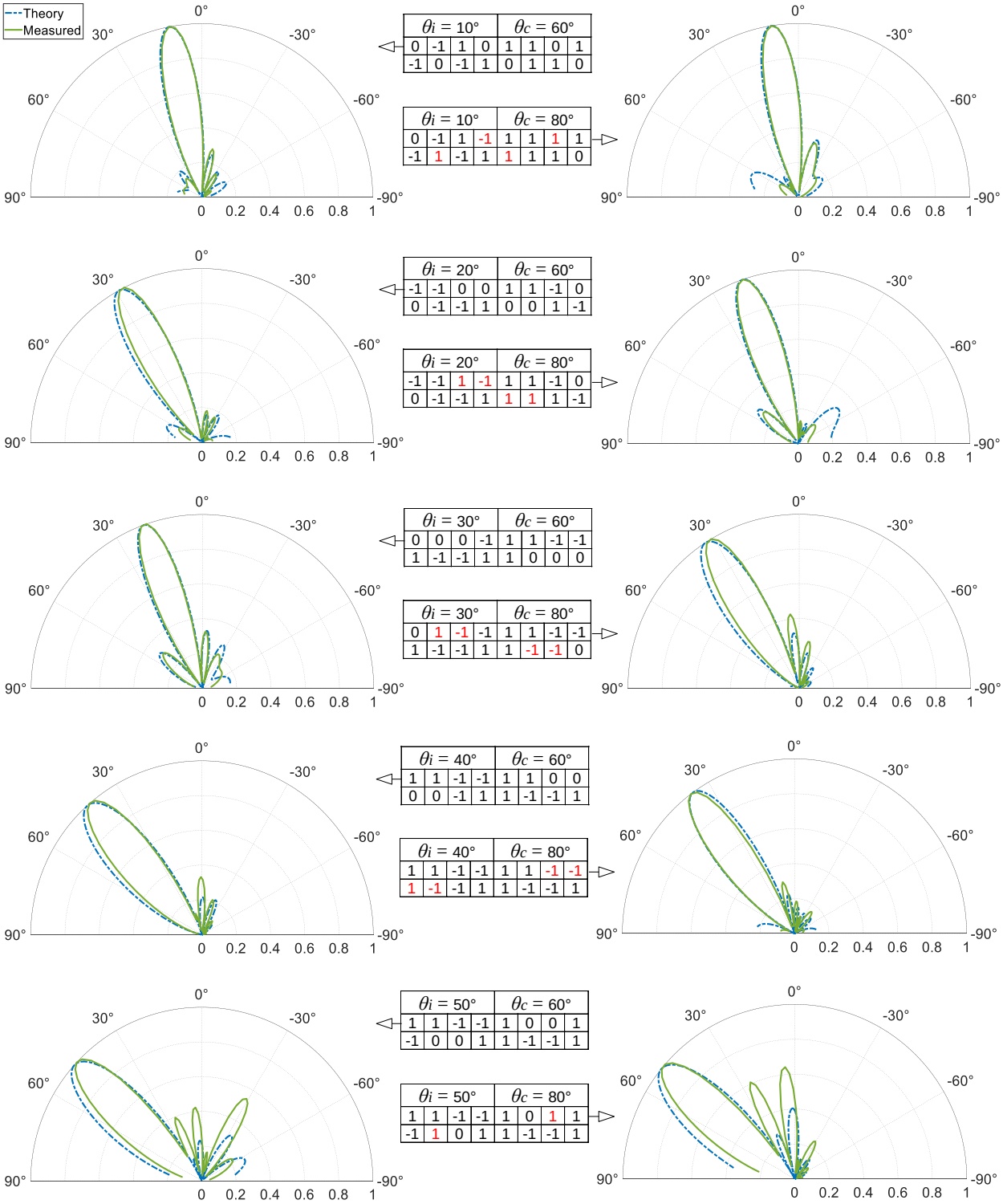


Figure 6.21 Beamforming results and comparison with an ideal phased array for two deviation thresholds, $\theta_c = 60°$ and $\theta_c = 80°$, along with theoretical results of the proposed topology. Red numbers in the tables indicate additional activated RX units resulting from the increase in θ_c.

tations, especially in mmWave and THz frequency bands. A 2×8 proof-of-concept prototype was developed, and the measured results validate the beamforming performance and overall effectiveness of the proposed approach, demonstrating strong agreement with theoretical predictions.

Table 6.2 Comparison with state-of-the-art architectures

Metrics	**This work**	[272]	[273]	[274]	[275]	[284]	[285]	[286]
Beamforming methodology	Switch+IF beamforming	LO beamforming	LO beamforming	LO beamforming	RF beamforming	VGA+IF beamforming	VGA+IF beamforming	VGA+IF beamforming
Power consumption	$\sim \mu$W	30 mW	54 mW	0	55 mW	30–42 mW	12 mW	35 mW
Frequency band	Baseband	53–62 GHz	86–96 GHz	114–147 GHz	200–250 GHz	Baseband	Baseband	Baseband
Gain (dB)	0	-7	-6	-16.5	-17	10.6–30	–	-20–20
Resolution	0.05×HPBW	5.6°	5.6°	5.6°	45°	6.8°	11°	20°
Technology	Hybrid, IC	40 nm CMOS	28 nm CMOS	65 nm CMOS	130 nm SiGe	40 nm CMOS	65 nm CMOS	40 nm CMOS

CHAPTER 7 GENERAL DISCUSSION

The development of large-scale transmitter and receiver arrays lies at the core of next-generation wireless communication and sensing systems. As data rates, bandwidth, and spatial resolution continue to increase, arrays at millimeter-wave and sub-terahertz frequencies must simultaneously achieve high performance, low power consumption, and compact integration. However, these objectives are inherently conflicting. High-frequency operation introduces significant losses and demands precise phase and amplitude control, while the sheer number of elements required in large arrays multiplies power, complexity, and calibration challenges. The need for scalable architectures that balance efficiency, linearity, and reconfigurability has therefore become one of the central research questions in the evolution of 5G and emerging 6G technologies.

At the system level, realizing dense arrays requires efficient signal distribution networks, reliable synchronization, and low-loss interconnects, all while maintaining manageable thermal and power budgets. Circuit-level challenges include the design of oscillators, mixers, and power amplifiers that sustain performance under large-scale integration, where mutual coupling, phase noise, and limited device gain impose strict constraints. Furthermore, array systems must increasingly serve multiple functions—communication, radar sensing, and localization—demanding architectures that can dynamically reconfigure across modes and frequency bands without prohibitive power or hardware overhead.

Addressing these challenges calls for innovations that go beyond incremental improvements in device efficiency. Solutions must instead rethink fundamental topologies—merging functions, reducing dependencies on global reference signals, and exploiting distributed architectures to achieve scalable, power-aware operation. This doctoral research has contributed to this effort by introducing novel receiver and transmitter array concepts that integrate self-oscillating, interferometric, and distributed approaches, aiming to reduce power consumption, simplify signal distribution, and enable secure and adaptable operation at high frequencies.

While significant progress has been made, the development of large, efficient, and multi-functional arrays remains an open and rapidly evolving field. Continued exploration of co-designed circuits, antennas, and signal processing architectures will be essential to fully unlock the potential of large-array systems in future wireless infrastructures.

CHAPTER 8 CONCLUSION

Summary of Works:

This doctoral research, addressed one of the central challenges in modern wireless systems: the practical realization of large arrays that combine high performance, energy efficiency, and compactness at millimeter-wave and sub-terahertz frequencies. While evolving 5G and emerging 6G technologies depend on such arrays for high data rate, coverage, and multifunctional integration, their adoption has been hindered by high power consumption, inefficient phase control, and circuit complexity.

To overcome these limitations, this work developed new receiver and transmitter architectures that allow us to fundamentally rethink array front-end design. For receiver arrays, two complementary low-power solutions were proposed. The Quadrature Harmonic Self-Oscillating Mixer (SOM) introduced a topology that merges oscillation and mixing, enabling direct-conversion reception without external LO distribution. Through coupled-oscillator configurations, this approach achieved scalable, reconfigurable arrays with exceptionally low DC power and independent element operation. In parallel, the Interferometric Receiver (IFRX) architecture demonstrated ultra-low-power detection with compact IC-compatible implementations, enhancing dynamic range by 14 dB and reducing footprint by over 70%, bringing passive interferometric systems close to heterodyne performance.

A major bottleneck in high-frequency arrays—phase shifter power and loss—was addressed through the development of a phase shifter–less beamforming method, which replaces RF phase control with low-power IF-domain switching. This technique achieved efficient beam steering with minimal loss and milliwatt-level power consumption, demonstrating a viable alternative for scalable high-frequency arrays.

On the transmitter side, a distributed array architecture was proposed to drastically reduce power amplifier losses and simplify the RF chain. By directly combining spatially distributed signals in free space, the system eliminated DAC-based upconversion and achieved high efficiency while inherently providing physical-layer security through spatial signal encoding.

Together, these contributions form a coherent framework for large-array systems that are both energy-efficient and functionally versatile. The solutions presented redefine key building blocks of wireless front-ends—oscillation, mixing, beamforming, and transmission—offering record-low power level solutions, improved integration density, and new functionalities validated through publications, patents, and experimental prototypes. This work establishes a

robust foundation for the next generation of integrated millimeter-wave and sub-terahertz arrays, bridging the gap between theoretical efficiency limits and practical, scalable system design.

Recommendations:

- **Full-scale large arrays at mmWave and THz frequencies:** Building on the proof-of-concept topologies developed in this research, the next step is to realize full-scale large arrays operating at millimeter-wave (mmWave) and terahertz (THz) frequency bands, where the proposed architectures were specifically designed to function. These high-frequency implementations will validate the scalability, efficiency, and multifunctionality of the designs in practical, real-world scenarios.
- **Distributed beamforming IC design for ISAC:** A key focus is the design of beamforming integrated circuits (ICs) in a distributed topology for mmWave large arrays. This approach aims to create a multi-functional integrated sensing and communication (ISAC) core, capable of simultaneous high-speed data transmission and environmental sensing, while maintaining extremely low power consumption. The distributed topology will enable independent element operation, reconfigurable activation, and efficient phase control, supporting large-array beamforming without the need for bulky or power-hungry components.
- **System-level integration and optimization:** Future research will also explore system-level integration, including packaging, interconnect optimization, antennas, and calibration techniques, to ensure that large arrays can achieve their full potential in terms of bandwidth, dynamic range, and energy efficiency. The outcomes will contribute to the development of next-generation wireless infrastructures, bridging the gap between experimental prototypes and commercially deployable mmWave and THz ISAC systems.
- **Sub-THz implementation considerations on performance:** As discussed in Chapter 2, scalable large-array implementations at millimeter-wave and sub-terahertz frequencies face practical limitations, particularly due to antenna integration technologies such as antenna-in-package (AiP). These technologies introduce insertion loss and RF phase variations. While calibration techniques can mitigate most of these effects, they have limited accuracy and allow residual errors. It is therefore important to evaluate the impact of such errors on the proposed architectures, especially the beamforming topology, which relies on receiver pairs maintaining opposite phase relationships for correct operation.

REFERENCES

[1] K. K. W. Low, S. Zihir, T. Kanar, and G. M. Rebeiz, "A 27–31-ghz 1024-element ka-band satcom phased-array transmitter with 49.5-dbw peak eirp, 1-db ar, and ±70° beam scanning," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 3, pp. 1757–1768, 2022.

[2] C.-N. Chen, Y.-H. Lin, L.-C. Hung, T.-C. Tang, W.-P. Chao, C.-Y. Chen, P.-H. Chuang, G.-Y. Lin, W.-J. Liao, Y.-H. Nien, W.-C. Huang, T.-Y. Kuo, K.-Y. Lin, T.-W. Huang, Y.-C. Lin, H.-C. Lu, T.-H. Tsai, and H. Wang, "38-ghz phased array transmitter and receiver based on scalable phased array modules with endfire antenna arrays for 5g mmw data links," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 1, pp. 980–999, 2021.

[3] A. Alhamed, G. Gültepe, and G. M. Rebeiz, "64-element 16–52-ghz transmit and receive phased arrays for multiband 5g-nr fr2 operation," *IEEE Trans. Microw. Theory Techn.*, vol. 71, no. 1, pp. 360–372, 2023.

[4] U. Kodak, B. Rupakula, S. Zihir, and G. M. Rebeiz, "60-ghz 64- and 256-element dual-polarized dual-beam wafer-scale phased-array transceivers with reticle-to-reticle stitching," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 2745–2767, Jul. 2020.

[5] T. Sowlati, "A 60-ghz 144-element phased-array transceiver for back-haul application," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3640–3659, Dec. 2018.

[6] A. H. Song, L. Wang, and Y. J. Cheng, "A scalable 32–38-ghz transmitter and receiver phased array with high radiation efficiency in uv-liga-based ceramic packaging," *IEEE Trans. Microw. Theory Techn.*, vol. 72, no. 8, pp. 4975–4985, 2024.

[7] S. Zihir, O. D. Gurbuz, A. Kar-Roy, S. Raman, and G. M. Rebeiz, "60-ghz 64- and 256-elements wafer-scale phased-array transmitters using full-reticle and subreticle stitching techniques," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4701–4719, 2016.

[8] K. Okada, J. Pang, A. Shirane, Z. Li, Y. Zhang, N. Oshima, S. Hori, and K. Kunihiro, "Millimeter-wave cmos phased-array transceivers for 5g and beyond," in *Proc. IEEE International Symposium on Personal, Indoor and Mobile Radio Communications (PIMRC)*, Kyoto, Japan, Sep. 2022, pp. 1–6.

[9] B. Sadhu, A. Paidimarri, D. Liu, M. Yeck, C. Ozdag, Y. Tojo, W. Lee, K. X. Gu, J.-O. Plouchart, C. W. Baks, Y. Uemichi, S. Chakraborty, Y. Yamaguchi, N. Guan, and A. Valdes-Garcia, "A 24–30-ghz 256-element dual-polarized 5g phased array using fast on-chip beam calculators and magnetoelectric dipole antennas," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3599–3616, 2022.

[10] H.-C. Park, D. Kang, J. Lee, D. Minn, Y. Aoki, K. Kim, S. Lee, D. Lee, S. Kim, J. Kim, W. Lee, C. Kim, S. Park, J. Park, B. Suh, J. Jang, M. Kim, K. Min, S. Jeon, A.-S. Ryu, Y. Kim, J. H. Lee, J. Son, and S.-G. Yang, "Millimeter-wave band cmos rf phased-array transceiver ic designs for 5g applications," in *IEEE Int. Electron Devices Meeting (IEDM)*, 2020, pp. 17.2.1–17.2.4.

[11] J. Park, S. Lee, J. Chun, L. Jeon, and S. Hong, "A 28-ghz four-channel beamforming front-end ic with dual-vector variable-gain phase shifters for 64-element phased-array antenna module," *IEEE J. Solid-State Circuits*, vol. 58, no. 4, pp. 1142–1159, Apr. 2023.

[12] S. Venkatesh, X. Lu, H. Saeidi, and K. Sengupta, "A high-speed programmable and scalable terahertz holographic metasurface based on tiled cmos chips," *Nat. Electron.*, vol. 3, no. 12, pp. 785–793, 2020.

[13] X. Chen, N. M. Monroe, G. C. Dogiamis, R. A. Stingel, P. Myers, and R. Han, "A 265-ghz cmos reflectarray with 98×98 elements for 1°-wide beam forming and high-angular-resolution radar imaging," *IEEE J. Solid-State Circuits*, vol. 59, no. 11, pp. 3655–3669, 2024.

[14] M. Gal-Katziri, C. Ives, A. Khakpour, and A. Hajimiri, "Optically synchronized phased arrays in cmos," *IEEE J. Solid-State Circuits*, vol. 57, no. 6, pp. 1578–1591, Jun. 2022.

[15] T. S. Rappaport, S. Sun, R. Mayzus, H. Zhao, Y. Azar, K. Wang, G. N. Wong, J. K. Schulz, M. Samimi, and F. Gutierrez, "Millimeter wave mobile communications for 5g cellular: It will work!" *IEEE Access*, vol. 1, pp. 335–349, 2013.

[16] Y. Bigdeli, P. Burasa, and K. Wu, "A scalable large array m-qam direct-rf transmitter topology with integrated physical layer security—a proof of concept," *IEEE Trans. Microw. Theory Techn.*, 2025.

[17] 5G Americas, "5g spectrum vision," 5G Americas, Tech. Rep., July 2019, white Paper, Available: https://www.5gamericas.org/wp-content/uploads/2019/07/5G_Americas_5G_Spectrum_Vision_Whitepaper-1.pdf.

[18] 3GPP, "Study on scenarios and requirements for next generation access technologies," 3rd Generation Partnership Project (3GPP), Technical Report (TR 38.913, Release 15) TR 38.913 V15.0.0, Sep. 2018. [Online]. Available: https://www.3gpp.org/ftp/Specs/archive/38_series/38.913/

[19] ITU-R, "Requirements, evaluation criteria and submission templates for the development of imt-2020," International Telecommunication Union, Radiocommunication Sector (ITU-R), Report M.2411-0, Nov. 2017. [Online]. Available: https://www.itu.int/pub/R-REP-M.2411

[20] Y. Bigdeli, S. A. Keivaan, P. Burasa, and K. Wu, "Towards the development of large-scale multifunction array transceiver systems," in *Proc. Asia-Pacific Microw. Conf. (APMC)*, 2023, pp. 890–892.

[21] A. Sethi, R. Akbar, M. Hietanen, J. P. Aikio, O. Kursu, M. Jokinen, M. E. Leinonen, T. Rahkonen, and A. Pärssinen, "Chip-to-chip interfaces for large-scale highly configurable mmwave phased arrays," *IEEE Journal of Solid-State Circuits*, vol. 58, no. 7, pp. 1987–2004, Jul. 2023.

[22] B. Sadhu, A. Paidimarri, W. Lee, M. Yeck, C. Ozdag, Y. Tojo, J.-O. Plouchart, X. Gu, Y. Uemichi, S. Chakraborty, Y. Yamaguchi, N. Guan, and A. Valdes-Garcia, "A 24-to-30 ghz 256-element dual-polarized 5g phased array with fast beam-switching support for >30,000 beams," in *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, vol. 65, 2022, pp. 436–438.

[23] X. Fu, D. You, X. Wang, Y. Wang, C. J. Mayeda, Y. Gao, M. Ide, Y. Zhang, J. Sakamaki, A. A. Fadila, Z. Li, J. Sudo, M. Higaki, S. Inoue, T. Eishima, T. Tomura, J. Pang, H. Sakai, K. Okada, and A. Shirane, "A low-power 256-element ka-band cmos phased-array receiver with on-chip distributed radiation sensors for small satellite constellations," *IEEE J. Solid-State Circuits*, vol. 58, no. 12, pp. 3380–3395, 2023.

[24] B. Rupakula, S. Zihir, and G. M. Rebeiz, "Low complexity 54–63-ghz transmit/receive 64- and 128-element 2-d-scanning phased-arrays on multilayer organic substrates with 64-qam 30-gbps data rates," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 12, pp. 5268–5281, 2019.

[25] S. Baek, J. Lee, K. Kim, S. Park, H. Oh, T. Kim, J. Jung, J. Kim, S. Jeon, J. H. Park, W. Lee, J. Park, D.-H. Lee, S. Lee, J. H. Lee, J. H. Kim, Y. Kim, S. Park, B. Suh, S. Oh, D. Lee, J. Son, Y. Chen, and S.-G. Yang, "A large-scale, low-power, compact 5g

mm-wave phased-array transceiver in 45 nm rfsoi cmos," *IEEE Trans. Microw. Theory Techn.*, vol. 73, no. 4, pp. 2097–2110, 2025.

[26] Y. Yin, Z. Zhang, T. Kanar, S. Zihir, and G. M. Rebeiz, "A 24–29.5 ghz 256-element 5g phased-array with 65.5 dbm peak eirp and 256-qam modulation," in *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, Los Angeles, CA, USA, Jun. 2020, pp. 687–690.

[27] P. Dufilie, E. Kowalski, M. D. Conway, D. Du Russel, and A. J. Fenn, "V-band stacked patch antenna phased array," in *IEEE Int. Symp. Phased Array Syst. Technol. (PAST)*, 2022, pp. 1–7.

[28] B. Sadhu, A. Paidimarri, A. O. Watanabe, D. Liu, X. Gu, C. W. Baks, Y. Tojo, Y. Fujisaku, I. De Sousa, Y. Yamaguchi, N. Guan, and A. Valdes-Garcia, "A heterogeneously integrated 256-element 5g phased array: Design, assembly, test," *IEEE J. Microw.*, vol. 5, no. 1, pp. 68–83, 2025.

[29] S. Shahramian, M. J. Holyoak, and Y. Baeyens, "A 16-element w-band phased-array transceiver chipset with flip-chip pcb integrated antennas for multi-gigabit wireless data links," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 7, pp. 3389–3402, Jul. 2018.

[30] S. Shahramian, M. J. Holyoak, A. Singh, and Y. Baeyens, "A fully integrated 384-element, 16-tile, w-band phased array with self-alignment and self-test," *IEEE J. Solid-State Circuits*, vol. 54, no. 9, pp. 2419–2434, 2019.

[31] Y. Yin, Q. Ma, K. Yan, A. Palazzolo, Z. Hu, S. Wang, and G. M. Rebeiz, "A ku-band dual-polarized 1024-element receive phased-array with four simultaneous beams," in *IEEE Int. Symp. Phased Array Syst. Technol. (ARRAY)*, 2024, pp. 1–4.

[32] E. V. P. Anjos, M. SalarRahimi, T. A. H. Bressner, P. Takhighani, A. Lahuerta-Lavieja, A. Elsakka, J. S. Siebenga, V. Volski, C. Fager, D. Schreurs, G. A. E. Vandenbosch, U. Johannsen, A. B. Smolders, and M. Geurts, "Format: A reconfigurable tile-based antenna array system for 5g and 6g millimeter-wave testbeds," *IEEE Syst. J.*, vol. 16, no. 3, pp. 4489–4500, 2022.

[33] A. Townley, P. Swirhun, D. Titz, A. Bisognin, F. Gianesello, R. Pilard, C. Luxey, and A. Niknejad, "A 94-ghz 4tx-4rx phased-array for fmcw radar with integrated lo and flip-chip antenna package," in *IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, 2016, pp. 294–297.

[34] A. Babakhani, X. Guan, A. Komijani, A. Natarajan, and A. Hajimiri, "A 77-ghz phased-array transceiver with on-chip antennas in silicon: Receiver and antennas," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2795–2806, Dec. 2006.

[35] X. Gao, L. Dai, and A. M. Sayeed, "Low rf-complexity technologies to enable millimeter-wave mimo with large antenna array for 5g wireless communications," *IEEE Commun. Mag.*, vol. 56, no. 4, pp. 211–217, 2018.

[36] K. Lim, S. Lee, Y. Lee, B. Moon, H. Shin, K. Kang, S. Kim, J. Lee, H. Lee, H. Shim, C. Sung, K. Park, G. Lee, M. Kim, S. Park, H. Jung, Y. Lim, C. Song, J. Seong, H. Cho, J. Choi, J. Lee, and S. Han, "A 65-nm cmos 2×2 MIMO multi-band LTE RF transceiver for small cell base stations," *IEEE J. Solid-State Circuits*, vol. 53, no. 7, pp. 1960–1976, Jul. 2018.

[37] A. Mohammadi and F. M. Ghannouchi, *RF Transceiver Design for MIMO Wireless Communications*, ser. Lecture Notes in Electrical Engineering. Berlin, Heidelberg: Springer Berlin Heidelberg, Feb. 2012, vol. 145.

[38] B. Yang, Z. Yu, J. Lan, R. Zhang, J. Zhou, and W. Hong, "Digital beamforming-based massive mimo transceiver for 5g millimeter-wave communications," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 7, pp. 3403–3418, Jul. 2018.

[39] S. Han, C.-l. I, Z. Xu, and C. Rowell, "Large-scale antenna systems with hybrid analog and digital beamforming for millimeter wave 5g," *IEEE Commun. Mag.*, vol. 53, no. 1, pp. 186–194, 2015.

[40] S. Payami, M. Khalily, A. Araghi, T. H. Loh, D. Cheadle, K. Nikitopoulos, and R. Tafazolli, "Developing the first mmwave fully-connected hybrid beamformer with a large antenna array," *IEEE Access*, vol. 8, pp. 141 282–141 291, 2020.

[41] H. Li, J. Chen, D. Hou, and W. Hong, "A w-band 6-bit phase shifter with 7 db gain and 1.35° rms phase error in 130 nm sige bicmos," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 10, pp. 1839–1843, Oct. 2020.

[42] B. Wang, H. Gao, M. K. Matters-Kammerer, and P. G. M. Baltus, "A 60 ghz 360° phase shifter with 2.7° phase resolution and 1.4° rms phase error in a 40-nm cmos technology," in *Proc. IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Jun. 2018, pp. 144–147.

[43] J. Pang, R. Wu, Y. Wang, M. Dome, H. Kato, H. Huang, A. Tharayil Narayanan, H. Liu, B. Liu, T. Nakamura, T. Fujimura, M. Kawabuchi, R. Kubozoe, T. Miura,

D. Matsumoto, Z. Li, N. Oshima, K. Motoi, S. Hori, K. Kunihiro, T. Kaneko, A. Shirane, and K. Okada, "A 28-ghz cmos phased-array transceiver based on lo phase-shifting architecture with gain invariant phase tuning for 5g new radio," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1228–1242, 2019.

[44] Y. Li, Z. Duan, Y. Fang, X. Li, B. Deng, Y. Dai, L. Sun, and H. Gao, "A 32–40 ghz 7-bit bi-directional phase shifter with 0.36 db/1.6° rms magnitude/phase errors for phased array systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 10, pp. 4000–4013, 2022.

[45] S. Li, Z. Zhang, B. Rupakula, and G. M. Rebeiz, "An eight-element 140-ghz wafer-scale if beamforming phased-array receiver with 64-qam operation in cmos rfsoi," *IEEE J. Solid-State Circuits*, vol. 57, no. 2, pp. 385–399, 2022.

[46] S. Pellerano, S. Callender, W. Shin, Y. Wang, S. Kundu, A. Agrawal, P. Sagazio, B. Carlton, F. Sheikh, A. Amadjikpe, W. Lambert, D. S. Vemparala, M. Chakravorti, S. Suzuki, R. Flory, and C. Hull, "A scalable 71-to-76 ghz 64-element phased-array transceiver module with 2×2 direct-conversion ic in 22nm finfet cmos technology," in *Proceedings of the IEEE International Solid-State Circuits Conference (ISSCC)*. IEEE, Feb. 2019, pp. 174–176.

[47] S. Shahramian, M. Holyoak, A. Singh, B. J. Farahani, and Y. Baeyens, "A fully integrated scalable w-band phased-array module with integrated antennas, self-alignment and self-test," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*. IEEE, 2018, pp. 74–76.

[48] J. Deng, P. Burasa, S. A. Keivaan, and K. Wu, "Waveguide receiver array for joint communication, sensing, and power transfer systems," *IEEE Trans. Microw. Theory Techn.*, vol. 73, no. 7, pp. 4204–4217, 2025.

[49] S. A. Keivaan, P. Burasa, and K. Wu, "Virtual receiver matrix and combinatory analog operations for future multifunction reconfigurable sensing and communication wireless systems," *IEEE Trans. Microw. Theory Techn.*, vol. 71, no. 1, pp. 424–433, 2023.

[50] Y. Bigdeli, P. Burasa, and K. Wu, "A miniaturized interferometric receiver for densely integrated large arrays," *IEEE Microw. Wireless Technol. Lett.*, pp. 1–4, 2025.

[51] ——, "Extending the dynamic range of square-law power detectors for large-scale receiver arrays," *IEEE Microw. Wireless Technol. Lett.*, vol. 35, no. 8, pp. 1226–1229, 2025.

[52] B. Sadhu, X. Gu, and A. Valdes-Garcia, "The more (antennas), the errier: A survey of silicon-based mm-wave phased arrays using multi-ic scaling," *IEEE Microw. Mag.*, vol. 20, no. 12, pp. 32–50, Dec. 2019.

[53] J. D. Dunworth, A. Homayoun, B.-H. Ku, Y.-C. Ou, K. Chakraborty, G. Liu, T. Segoria, J. Lerdworatawee, J. W. Park, H.-C. Park, H. Hedayati, D. Lu, P. Monat, K. Douglas, and V. Aparin, "A 28-ghz bulk-cmos dual-polarization phased-array transceiver with 24 channels for 5g user and basestation equipment," in *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, 2018, pp. 70–72.

[54] X. Gu, D. Liu, C. Baks, A. Valdes-Garcia, B. Parker, M. D. Tsai, and S. K. Reynolds, "A compact 4-chip package with 64 embedded dual-polarization antennas for w-band phased-array transceivers," in *Proceedings of the 64th IEEE Electronic Components and Technology Conference (ECTC)*, May 2014, pp. 1272–1277.

[55] S. Hansen, C. Bredendiek, G. Briese, A. Froehly, R. Herschel, and N. Pohl, "A sige-chip-based d-band fmcw-radar sensor with 53-ghz tuning range for high resolution measurements in industrial applications," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 1, pp. 719–731, Jan. 2022.

[56] X. Jia, X. Li, S. Erdogan, K.-S. Moon, J. W. Kim, K.-Q. Huang, M. B. Jordan, and M. Swaminathan, "Antenna with embedded die in glass interposer for 6g wireless applications," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 13, no. 2, pp. 219–229, 2023.

[57] M. Wei, N. Baniasadi, E. Chou, H. Beshary, S. Krishnamurthy, E. Alon, and A. Niknejad, "A d-band packaged cmos integrated transmitter for mu-mimo applications," in *IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, 2022, pp. 6–8.

[58] S. Li, T. Chi, J. S. Park, W. T. Khan, H. Wang, and J. Papapolymerou, "A fully packaged d-band mimo transmitter using high-density flip-chip interconnects on lcp substrate," in *IEEE MTT-S International Microwave Symposium Digest*, May 2016, pp. 1–4.

[59] W. T. Khan, A. Ç. Ulusoy, R. L. Schmid, and J. Papapolymerou, "Characterization of a low-loss and wide-band (dc to 170 ghz) flip-chip interconnect on an organic substrate," in *IEEE MTT-S International Microwave Symposium Digest*, Jun. 2014, pp. 1–4.

[60] Z. Cao, M. Stocchi, C. Wipf, J. Lehmann, L. Li, S. T. Wipf, M. Wietstruck, C. Carta, and M. Kaynak, "D-band flip-chip packaging with wafer-level cu-pillar bumps," in *IEEE Conf. Electr. Perform. Electron. Packag. Syst. (EPEPS)*, 2023, pp. 1–4.

[61] S. Beer, B. Ripka, S. Diebold, H. Gulan, C. Rusch, P. Pahl, and T. Zwick, "Design and measurement of matched wire bond and flip chip interconnects for d-band system-in-package applications," in *IEEE MTT-S Int. Microw. Symp. (IMS)*, 2011, pp. 1–4.

[62] S. Beer, C. Rusch, B. Göttel, H. Gulan, and T. Zwick, "D-band grid-array antenna integrated in the lid of a surface-mountable chip-package," in *Proceedings of the 7th European Conference on Antennas and Propagation (EuCAP)*. IEEE, Apr. 2013, pp. 1318–1322.

[63] X. Gu, A. Valdes-Garcia, A. Natarajan, B. Sadhu, D. Liu, and S. K. Reynolds, "W-band scalable phased arrays for imaging and communications," *IEEE Communications Magazine*, vol. 53, no. 4, pp. 196–204, Apr. 2015.

[64] X. Gu, D. Liu, C. Baks, J.-O. Plouchart, W. Lee, and A. Valdes-Garcia, "An enhanced 64-element dual-polarization antenna array package for w-band communication and imaging applications," in *Proceedings of the IEEE 68th Electronic Components and Technology Conference (ECTC)*. IEEE, May 2018, pp. 197–201.

[65] W. J. Lambert, A. L. Amadjikpe, J. Yao, S. C. J. Chavali, P. Sagazio, Y. S. Nam, M. Abu-Mahaimed, and S. Pellerano, "Scalable multichip packaging with integrated antenna array for a 73-ghz transceiver ic," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 1, pp. 387–398, Jan. 2021.

[66] A. Lamminen, J. Säily, J. Ala-Laurinaho, J. de Cos, and V. Ermolov, "Patch antenna and antenna array on multilayer high-frequency pcb for d-band," *IEEE Open Journal of Antennas and Propagation*, vol. 1, pp. 396–403, 2020.

[67] T. Dao, A. Kearns, D. R. Paredes, and G. Hueber, "Wideband high-gain stacked patch antenna array on standard pcb for d-band 6g communications," *IEEE Antennas and Wireless Propagation Letters*, vol. 23, pp. 478–482, 2024.

[68] F. Ahmed, M. Furqan, and A. Stelzer, "120-ghz and 240-ghz broadband bow-tie antennas in ewlb package for high-resolution radar applications," in *Proceedings of the 48th European Microwave Conference (EuMC)*. IEEE, Sep. 2018, pp. 1109–1112.

[69] S. Beer, H. Gulan, C. Rusch, and T. Zwick, "Integrated 122-ghz antenna on a flexible polyimide substrate with flip-chip interconnect," *IEEE Trans. Antennas Propag.*, vol. 61, no. 4, pp. 1564–1572, Apr. 2013.

[70] A. A. Farid, A. S. H. Ahmed, A. Simsek, and M. J. W. Rodwell, "A packaged 135-ghz 22-nm fd-soi transmitter on an ltcc carrier," in *IEEE MTT-S Int. Microw. Symp. Dig.* IEEE, Jun. 2021, pp. 713–716.

[71] A. Singh, M. Sayginer, M. J. Holyoak, J. Weiner, J. Kimionis, M. Elkhouly, Y. Baeyens, and S. Shahramian, "A d-band radio-on-glass module for spectrally-efficient and low-cost wireless backhaul," in *IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, 2020, pp. 99–102.

[72] P. Sullivan and D. Schaubert, "Analysis of an aperture coupled microstrip antenna," *IEEE Trans. Antennas Propag.*, vol. AP-34, no. 8, pp. 977–984, Aug. 1986.

[73] A. Dinkelacker, J. J. Kim, and J. F. Buckwalter, "An antipodal siw-fed vivaldi antenna at d-band in ltcc for flip-chip rfic integration," in *2025 IEEE/MTT-S International Microwave Symposium - IMS 2025*, San Francisco, CA, USA, 2025, pp. 670–673.

[74] X. Li, M. Al-Juwhari, M. Ahamed, M. Basha, J. Flemming, and M. Swaminathan, "Empty-siw (esiw) based beamformer system on glass package for g-band phased array applications," in *2025 IEEE/MTT-S International Microwave Symposium - IMS 2025*, San Francisco, CA, USA, 2025, pp. 659–662.

[75] R. Hasaba *et al.*, "Evaluation of stacked structure for 160 ghz end-fire type compact antenna-in-package considering thermal design," in *2025 IEEE/MTT-S International Microwave Symposium - IMS 2025*, San Francisco, CA, USA, 2025, pp. 663–666.

[76] Z. Hu, C. Wang, and R. Han, "A 32-unit 240-ghz heterodyne receiver array in 65-nm cmos with array-wide phase locking," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1216–1227, 2019.

[77] W. R. Deal, X. B. Mei, V. Radisic, K. Leong, S. Sarkozy, B. Gorospe, J. Lee, P. H. Liu, W. Yoshida, J. Zhou, M. Lange, J. Uyeda, and R. Lai, "Demonstration of a 0.48 thz amplifier module using inp hemt transistors," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 5, pp. 289–291, 2010.

[78] L. Samoska, W. R. Deal, G. Chattopadhyay, D. Pukala, A. Fung, T. Gaier, M. Soria, V. Radisic, X. Mei, and R. Lai, "A submillimeter-wave hemt amplifier module with integrated waveguide transitions operating above 300 ghz," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 6, pp. 1380–1388, 2008.

[79] H. Saeidi, S. Venkatesh, X. Lu, and K. Sengupta, "Thz prism: One-shot simultaneous localization of multiple wireless nodes with leaky-wave thz antennas and transceivers in cmos," *IEEE J. Solid-State Circuits*, vol. 56, no. 12, pp. 3840–3854, 2021.

[80] Y. Tousi and E. Afshari, "A scalable thz 2d phased array with +17 dbm of eirp at 338 ghz in 65-nm bulk cmos," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*. IEEE, Feb. 2014, pp. 258–259.

[81] D. Hou, Y.-Z. Xiong, W.-L. Goh, S. Hu, W. Hong, and M. Madihian, "130-ghz on-chip meander slot antennas with stacked dielectric resonators in standard cmos technology," *IEEE Trans. Antennas Propag.*, vol. 60, no. 9, pp. 4102–4109, Sep. 2012.

[82] K. Sengupta and A. Hajimiri, "A 0.28-thz power-generation and beam-steering array in cmos based on distributed active radiators," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3013–3031, Dec. 2012.

[83] S. Sengupta, D. R. Jackson, and S. A. Long, "A method for analyzing a linear series-fed rectangular microstrip antenna array," *IEEE Trans. Antennas Propag.*, vol. 63, no. 8, pp. 3731–3736, Aug. 2015.

[84] N. Buadana, S. Jameson, and E. Socher, "A multiport chip-scale dielectric resonator antenna for cmos thz transmitters," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 9, pp. 3621–3632, Sep. 2020.

[85] B. Yu, Z. Qian, C. Lin, J. Lin, Y. Zhang, G. Yang, and Y. Luo, "A wideband mmwave antenna in fan-out wafer level packaging with tall vertical interconnects for 5g wireless communication," *IEEE Trans. Antennas Propag.*, vol. 69, no. 10, pp. 6906–6911, Oct. 2021.

[86] A. Babakhani, "Direct antenna modulation (dam) for on-chip mm-wave transceivers," Ph.D. dissertation, California Institute of Technology, 2008.

[87] J. M. Edwards and G. M. Rebeiz, "High-efficiency elliptical slot antennas with quartz superstrates for silicon rfics," *IEEE Trans. Antennas Propag.*, vol. 60, no. 11, pp. 5010–5020, 2012.

[88] T. Deng, Y. Zhang, Z. Zheng, Q. Yan, and J.-F. Mao, "High-gain and high-efficiency sub-terahertz antenna-on-chip with microbumps for highly-integrated systems," *IEEE Transactions on Antennas and Propagation*, vol. 72, no. 5, pp. 4107–4115, May 2024.

[89] Y. Fang and Y. P. Zhang, "Theory of microbump antennas for broadside radiation," *IEEE Transactions on Antennas and Propagation*, vol. 72, no. 11, pp. 8353–8364, Nov 2024.

[90] D. B. Rutledge and M. S. Muha, "Imaging antenna arrays," *IEEE Trans. Antennas Propag.*, vol. AP-30, no. 4, pp. 535–540, Jul. 1982.

[91] N. G. Alexopoulos, P. B. Katehi, and D. B. Rutledge, "Substrate optimization for integrated circuit antennas," *IEEE Trans. Microw. Theory Techn.*, vol. MMT-31, no. 7, pp. 550–557, Jul. 1983.

[92] S. Thomas, S. Razavian, J. S. Virdi, W. Sun, B. F. Motlagh, and A. Babakhani, "A 400-ghz efficient radiator and ook transceiver for multi-gb/s wireless communication in silicon," *IEEE J. Solid-State Circuits*, pp. 1–17, 2024.

[93] T. Tajima, H.-J. Song, and M. Yaita, "Compact thz ltcc receiver module for 300 ghz wireless communications," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 4, pp. 291–293, 2016.

[94] D. Filipovic, G. Gauthier, S. Raman, and G. Rebeiz, "Off-axis properties of silicon and quartz dielectric lens antennas," *IEEE Trans. Antennas Propag.*, vol. 45, no. 5, pp. 760–766, 1997.

[95] M. Alonso-delPino, C. Jung-Kubiak, T. Reck, N. Llombart, and G. Chattopadhyay, "Beam scanning of silicon lens antennas using integrated piezomotors at submillimeter wavelengths," *IEEE Trans. Terahertz Sci. Technol.*, vol. 9, no. 1, pp. 47–54, Jan. 2019.

[96] H. J. Ng, M. Kucharski, W. Ahmad, and D. Kissinger, "Multi-purpose fully differential 61- and 122-ghz radar transceivers for scalable mimo sensor platforms," *IEEE J. Solid-State Circuits*, vol. 52, no. 9, pp. 2242–2255, Sep. 2017.

[97] H. J. Ng, J. Wessel, D. Genschow, R. Wang, Y. Sun, and D. Kissinger, "Miniaturized 122 ghz system-on-chip radar sensor with on-chip antennas utilizing a novel antenna design approach," in *IEEE MTT-S Int. Microw. Symp. Dig. (IMS)*. IEEE, May 2016, pp. 1–4.

[98] R. Wang, Y. Sun, M. Kaynak, S. Beer, J. Borngräber, and J. C. Scheytt, "A micromachined double-dipole antenna for 122–140 ghz applications based on a sige bicmos technology," in *IEEE MTT-S Int. Microw. Symp. Dig. (IMS)*. IEEE, Jun. 2012, pp. 1–3.

[99] M. de Kok, A. B. Smolders, and U. Johannsen, "A review of design and integration technologies for d-band antennas," *IEEE Open J. Antennas Propag.*, vol. 2, pp. 746–758, 2021.

[100] L. Chen, A. Cathelin, and E. Afshari, "A high-efficiency high-power 170–176-ghz frequency stabilized quadrature radiator," *IEEE J. Solid-State Circuits*, vol. 59, no. 1, pp. 243–252, Jan. 2024.

[101] A. Valdes-Garcia and et al., "A fully-integrated dual-polarization 16-element w-band phased-array transceiver in sige bicmos," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*. IEEE, 2013, pp. 375–378.

[102] B. Sadhu and et al., "A 28 ghz 32-element phased-array transceiver ic with concurrent dual-polarized beams and 1.4° beam steering resolution for 5g communication," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*. IEEE, 2017, pp. 128–129.

[103] W. Lee and et al., "A fully-integrated 94-ghz 16-element dual-output phased-array transmitter in sige bicmos with psat $>$ 6.5 dbm up to 105 °c," in *Proc. IEEE Compound Semiconductor Integrated Circuits Symp. (CSICS)*. IEEE, 2017, pp. 1–4.

[104] J. Plouchart and et al., "A fully-integrated 94-ghz 32-element phased-array receiver in sige bicmos," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*. IEEE, 2017, pp. 380–383.

[105] W. Lee and et al., "Fully integrated 94-ghz dual-polarized tx and rx phased array chipset in sige bicmos operating up to 105 °c," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2512–2531, Sep. 2018.

[106] J. Takahashi, M. Aikawa, and H. Matsumoto, "A technique for on-site calibration of active phased arrays using two probes," *IEEE Trans. Antennas Propag.*, vol. 54, no. 5, pp. 1505–1511, May 2006.

[107] J. W. Kim, Y. Park, H. C. Choi, and H. Choo, "An accurate mid-field calibration technique for large phased array antenna," *IEEE Trans. Antennas Propag.*, vol. 64, no. 10, pp. 4442–4447, Oct. 2016.

[108] A. Pinna, A. Polemi, and F. Paonessa, "Calibration and measurements of large multi-element array antennas," *IEEE Trans. Antennas Propag.*, vol. 68, no. 10, pp. 7364–7375, Oct. 2020.

[109] J. J. Schuss and et al., "Large-scale phased array calibration," *IEEE Trans. Antennas Propag.*, vol. 67, no. 9, pp. 5919–5933, Sep. 2019.

[110] H. M. Aumann, A. J. Fenn, and F. G. Willwerth, "Phased array antenna calibration and pattern prediction using mutual coupling measurements," *IEEE Trans. Antennas Propag.*, vol. 37, no. 7, pp. 844–850, Jul. 1989.

[111] T. Gao, J. Wang, Y. Guo, and X. Chen, "Large phased array antenna calibration using mutual coupling method," in *Proc. IEEE Antennas Propag. Soc. Int. Symp.* Boston, MA, USA: IEEE, Jul. 2001, pp. 223–226.

[112] T. Gao, "Frugal calibration of mutual coupling in large scale antenna array," in *Proc. IEEE Antennas Propag. Soc. Int. Symp.* Spokane, WA, USA: IEEE, Jul. 2011, pp. 1234–1237.

[113] T. Takahashi, H. Miyashita, Y. Konishi, and S. Makino, "Theoretical study on measurement accuracy of rotating element electric field vector method," *Electron. Commun. Jpn., Part I*, vol. 89, no. 1, pp. 22–33, Jan. 2006.

[114] Z. Zhang, J. Wang, Y. Guo, and X. Chen, "Large-scale phased array calibration based on amplitude-only measurement with the multiround grouped-rev method," *IEEE Trans. Antennas Propag.*, vol. 70, no. 7, pp. 6106–6118, Jul. 2022.

[115] J. Lu, M. Tang, and R. Ma, "A fast amplitude-only cyclic subarray calibration method for large phased arrays," *IEEE Trans. Antennas Propag.*, vol. 71, no. 5, pp. 4312–4324, May 2023.

[116] Y. Lee, S. Lee, J. Kim, and H. Choo, "Design and optimization of self-calibration method for multi-beam phased array antenna with large-scale aperture," *IEEE Trans. Antennas Propag.*, vol. 66, no. 8, pp. 4020–4032, Aug. 2018.

[117] S. Lim, Y. Kim, and H. Choo, "A portable low-overhead self-calibration system for k-band large-scale phased array transmission," *IEEE Trans. Antennas Propag.*, vol. 70, no. 3, pp. 2218–2229, Mar. 2022.

[118] K. Rambabu, B. Pan, and M. Schwerdt, "Calibration of aperture arrays in time domain using the simultaneous perturbation algorithm," *IEEE Trans. Antennas Propag.*, vol. 58, no. 6, pp. 1911–1919, Jun. 2010.

[119] E. Afshari and R. Han, "Progress towards mw-power generation in cmos thz signal sources," in *Proc. 8th Eur. Microw. Integr. Circuits Conf. (EuMIC).* IEEE, Oct. 2013, pp. 117–120.

[120] L. Zhang, K. Ma, H. Fu, Y. Wang, K. Wang, F. Meng, and X. Li, "A compact 140-ghz power amplifier with 15.4-dbm p_sat and 14.25% peaking pae in 28-nm bulk cmos process," *IEEE Trans. Microw. Theory Techn.*, vol. 72, no. 5, pp. 3016–3030, May 2024.

[121] A. Alizadeh, P. V. Rowell, Z. Griffith, M. E. Urteaga, and M. J. W. Rodwell, "A 78-mw 220-ghz power amplifier with peak 18.4% pae in 250-nm inp hbt technology," *IEEE Trans. Microw. Theory Techn.*, vol. 72, no. 10, pp. 5789–5798, Oct. 2024.

[122] Y.-H. Hsiao, Z.-M. Tsai, H.-C. Liao, J.-C. Kao, and H. Wang, "Millimeter-wave cmos power amplifiers with high output power and wideband performances," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4520–4533, Dec. 2013.

[123] S. Hwang, J. Jeon, S. Bae, B. Yoon, S. Kang, and J. Kim, "A 5.15–7.125 ghz differential power amplifier with enhanced linearity of average power region using dynamic cross-coupled capacitor," *IEEE Trans. Microw. Theory Techn.*, vol. 72, no. 1, pp. 575–588, Jan. 2024.

[124] Z. Zhang, J. Pang, and K. Okada, "A highly integrated 5g mm-wave phased array system at n257/n261 bands with 54 dbm linear eirp," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2022.

[125] A. Puglielli, G. LaCaille, A. M. Niknejad, G. Wright, B. Nikolic, and E. Alon, "Phase noise scaling and tracking in ofdm multi-user beamforming arrays," in *Proc. IEEE Int. Conf. Commun. (ICC)*, 2016, pp. 1–6.

[126] T. Holma and V. Ränki, "Phase noise in beamforming," *IEEE Trans. Wireless Commun.*, vol. 9, no. 12, pp. 3682–3689, Dec. 2010.

[127] M. Jung, W. Saad, Y. Jang, G. Kong, and S. Choi, "Performance analysis of large intelligent surfaces (liss): Asymptotic data rate and channel hardening effects," *IEEE Trans. Wireless Commun.*, vol. 19, no. 3, pp. 2052–2065, 2020.

[128] B. M. Hochwald, T. L. Marzetta, and V. Tarokh, "Multiple-antenna channel hardening and its implications for rate feedback and scheduling," *IEEE Trans. Inf. Theory*, vol. 50, no. 9, pp. 1893–1909, 2004.

[129] P. Mei, Y. Cai, K. Zhao, Z. Ying, G. F. Pedersen, X. Q. Lin, and S. Zhang, "On the study of reconfigurable intelligent surfaces in the near-field region," *IEEE Trans. Antennas Propag.*, vol. 70, no. 10, pp. 8718–8728, 2022.

[130] M. Di Renzo, A. Zappone, M. Debbah, M.-S. Alouini, C. Yuen, J. de Rosny, and S. Tretyakov, "Smart radio environments empowered by reconfigurable intelligent surfaces: How it works, state of research, and the road ahead," *IEEE J. Sel. Areas Commun.*, vol. 38, no. 11, pp. 2450–2525, 2020.

[131] M. Barbuto, Z. Hamzavi-Zarghani, M. Longhi, A. Monti, D. Ramaccia, S. Vellucci, A. Toscano, and F. Bilotti, "Metasurfaces 3.0: A new paradigm for enabling smart electromagnetic environments," *IEEE Trans. Antennas Propag.*, vol. 70, no. 10, pp. 8883–8897, 2022.

[132] F. Bilotti, M. Barbuto, Z. Hamzavi-Zarghani, M. Karamirad, M. Longhi, A. Monti, D. Ramaccia, L. Stefanini, A. Toscano, and S. Vellucci, "Reconfigurable intelligent surfaces as the key-enabling technology for smart electromagnetic environments," *Adv. Phys. X*, vol. 9, no. 1, p. 2299543, 2024.

[133] L. Zhuang, J. Ouyang, X. Li, S. Yang, and J. Hu, "Subspace-based inverse source method for fast synthesis of large-scale ris with advanced power pattern shaping," *IEEE Trans. Antennas Propag.*, vol. 73, no. 1, pp. 653–658, 2025.

[134] F. Yang and Y. Rahmat-Samii, *Surface Electromagnetics: With Applications in Antenna, Microwave, and Optical Engineering.* Cambridge Univ. Press, 2019.

[135] R. Janaswamy, D. V. Gupta, and D. H. Schaubert, "Adaptive correction to array coefficients through dithering and near-field sensing," *IEEE Trans. Antennas Propag.*, vol. 58, no. 11, pp. 3558–3567, 2010.

[136] P. Chakravorty and D. Mandal, "Radiation pattern correction in mutually coupled antenna arrays," *IEEE Trans. Antennas Propag.*, vol. 64, no. 9, pp. 4092–4095, Sep. 2016.

[137] X. Rao and V. K. N. Lau, "Distributed compressive csit estimation and feedback," *IEEE Trans. Signal Process.*, vol. 62, no. 12, pp. 3261–3271, Jun. 2014.

[138] S. Noh, M. D. Zoltowski, Y. Sung, and D. J. Love, "Pilot beam pattern design for channel estimation in massive mimo systems," *IEEE J. Sel. Top. Signal Process.*, vol. 8, no. 5, pp. 787–801, 2014.

[139] E. J. Black, "Holographic beam forming and mimo," Pivotal Commware, Tech. Rep., Dec. 2017. [Online]. Available: https://pivotalcommware.com/wp-content/uploads/2017/12/Holographic-Beamforming-WP-v.6C-FINAL.pdf

[140] W. Tang, M. Z. Chen, J. Y. Dai, Y. Zeng, X. Zhao, S. Jin, Q. Cheng, and T. J. Cui, "Wireless communications with programmable metasurface: New paradigms, opportunities, and challenges on transceiver design," *IEEE Wireless Commun.*, vol. 27, no. 2, pp. 180–187, 2020.

[141] P. Rocca, G. Oliveri, R. J. Mailloux, and A. Massa, "Unconventional phased array architectures and design methodologies—a review," *Proc. IEEE*, vol. 104, no. 3, pp. 544–560, Mar. 2016.

[142] J. Goodman, F. J. Leonberger, S.-Y. Kung, and R. A. Athale, "Optical interconnections for vlsi systems," *Proc. IEEE*, vol. 72, no. 7, pp. 850–866, Jul. 1984.

[143] K. Y. Lau, G. F. Lutes, and R. L. Tjoelker, "Ultra-stable rf-over-fiber transport in nasa antennas, phased arrays and radars," *J. Lightw. Technol.*, vol. 32, no. 20, pp. 3440–3451, Oct. 2014.

[144] J. Beas, G. Castañón, I. Aldaya, A. Aragón-Zavala, and G. Campuzano, "Millimeter-wave frequency radio over fiber systems: A survey," *IEEE Commun. Surveys Tuts.*, vol. 15, no. 4, pp. 1593–1619, 2013.

[145] M. R. M. Hashemi, A. C. Fikes, M. Gal-Katziri, B. Abiri, F. Bohn, A. Safaripour, M. D. Kelzenberg, E. L. Warmann, P. Espinet, N. Vaidya, E. E. Gdoutos, C. Leclerc, F. Royer, S. Pellegrino, H. A. Atwater, and A. Hajimiri, "A flexible phased array system with low areal mass density," *Nat. Electron.*, vol. 2, no. 5, pp. 195–205, 2019.

[146] M. Ryle and A. Hewish, "The synthesis of large radio telescopes," *Mon. Not. Roy. Astron. Soc.*, vol. 120, no. 3, pp. 220–230, Mar. 1960.

[147] K. M. Cuomo, S. D. Coutts, J. C. McHarg, and N. B. Pulsone, "Wideband aperture coherence processing for next generation radar (nexgen)," MIT Lincoln Laboratory, Tech. Rep. NG-3, Jul. 2004. [Online]. Available: https://www.ll.mit.edu/r-d/publications/wideband-aperture-coherence-processing-next-generation-radar-nexgen

[148] N. Yang, L. Wang, G. Geraci, M. Elkashlan, J. Yuan, and M. D. Renzo, "Safeguarding 5g wireless communication networks using physical layer security," *IEEE Commun. Mag.*, vol. 53, no. 4, pp. 20–27, Apr. 2015.

[149] A. D. Wyner, "The wire-tap channel," *Bell Syst. Tech. J.*, vol. 54, no. 8, pp. 1355–1387, 1975.

[150] S. Goel and R. Negi, "Guaranteeing secrecy using artificial noise," *IEEE Trans. Wireless Commun.*, vol. 7, no. 6, pp. 2180–2189, Jun. 2008.

[151] N. Yang, M. Elkashlan, T. Q. Duong, J. Yuan, and R. Malaney, "Optimal transmission with artificial noise in mimo wiretap channels," *IEEE Trans. Veh. Technol.*, vol. 62, no. 9, pp. 4237–4249, Nov. 2013.

[152] E. G. Larsson, O. Edfors, F. Tufvesson, and T. L. Marzetta, "Massive mimo for next generation wireless systems," *IEEE Commun. Mag.*, vol. 52, no. 2, pp. 186–195, Feb. 2014.

[153] Y. Ding and V. Fusco, "Physical layer security through directional modulation with spatio-temporal millimeter-wave transmitter arrays," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 7, pp. 2610–2620, Jul. 2019.

[154] Y. Bigdeli, P. Burasa, and K. Wu, "A phase-shifterless analog beamforming topology for large receiver arrays—a proof of concept," *IEEE Transactions on Microwave Theory and Techniques*, 2025, early access.

[155] D. Zhao, P. Gu, Y. Yi, J. Zhang, C. Xu, M. Yang, Z. Chen, Y. Chai, H. Liu, S. Jiang, X. Yan, and X. You, "A k-band hybrid-packaged temperature-compensated phased-array receiver and integrated antenna array," *IEEE Transactions on Microwave Theory and Techniques*, vol. 71, no. 1, pp. 409–423, 2023.

[156] S. A. Keivaan, P. Burasa, and K. Wu, "Virtual receiver matrix and combinatory analog operations for future multifunction reconfigurable sensing and communication wireless systems," *IEEE Trans. Microw. Theory Tech.*, vol. 71, no. 1, pp. 424–433, 2023.

[157] Y. Cui, F. Liu, X. Jing, and J. Mu, "Integrating sensing and communications for ubiquitous iot: Applications, trends, and challenges," *IEEE Network*, vol. 35, no. 5, pp. 158–167, 2021.

[158] L. Han and K. Wu, "Multifunctional transceiver for future intelligent transportation systems," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 7, pp. 1879–1892, 2011.

[159] ——, "Joint wireless communication and radar sensing systems – state of the art and future prospects," *IET Microwaves, Antennas Propag.*, vol. 7, no. 11, pp. 876–885, 2013.

[160] J. Moghaddasi and K. Wu, "Multifunctional transceiver for future radar sensing and radio communicating data-fusion platform," *IEEE Access*, vol. 4, pp. 818–838, 2016.

[161] K. Wu, "Mhz-through-thz (mtt) challenges and opportunities [president's column]," *IEEE Microw. Mag.*, vol. 17, no. 2, pp. 8–10, 2016.

[162] S. Li, Z. Zhang, B. Rupakula, and G. M. Rebeiz, "An eight-element 140-ghz wafer-scale if beamforming phased-array receiver with 64-qam operation in cmos rfsoi," *IEEE J. of Solid-State Circuits*, vol. 57, no. 2, pp. 385–399, 2022.

[163] Z. Hu, C. Wang, and R. Han, "A 32-unit 240-ghz heterodyne receiver array in 65-nm cmos with array-wide phase locking," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1216–1227, 2019.

[164] Y.-J. Chen and T.-S. Chu, "A 312ghz antenna array receiver in 65nm cmos utilizing self-oscillating 3x subharmonic mixer frontend," in *Dig. Pap. - IEEE Radio Freq. Integr. Circuits Symp.*, 2015, pp. 19–22.

[165] Y. Zhu, H. Wang, K. Kang, and O. Momeni, "A low power sub-harmonic self-oscillating mixer with 16.8db conversion loss at 310ghz in 65nm cmos," in *2019 IEEE Custom Integrated Circuits Conference (CICC)*, 2019, pp. 1–4.

[166] Y. Bigdeli, P. Burasa, and K. Wu, "Quadrature harmonic self-oscillating mixer for multifunction wireless communication and sensing systems," in *2022 IEEE MTT-S Int. Microw. Symp. (IMS)*, 2022, pp. 402–405.

[167] P. Burasa, N. G. Constantin, and K. Wu, "Low-power injection-locked zero-if self-oscillating mixer for high gbit/s data-rate battery-free active μrfid tag at millimeter-wave frequencies in 65-nm cmos," *IEEE Trans. Microw. Theory Tech.*, vol. 64, no. 4, pp. 1055–1065, 2016.

[168] P. Burasa, T. Djerafi, N. G. Constantin, and K. Wu, "High-data-rate single-chip battery-free active millimeter-wave identification tag in 65-nm cmos technology," *IEEE Trans. Microw. Theory Tech.*, vol. 64, no. 7, pp. 2294–2303, 2016.

[169] J.-Y. Kim and W.-Y. Choi, "30 ghz cmos self-oscillating mixer for self-heterodyne receiver application," *IEEE Microw. Wirel. Compon. Lett.*, vol. 20, no. 6, pp. 334–336, 2010.

[170] M. Pontón, S. Sancho, A. Herrera, and A. Suárez, "Wireless injection locking of zero-if self-oscillating mixers," *IEEE Trans. Microw. Theory Tech.*, vol. 70, no. 1, pp. 836–849, 2022.

[171] S. A. Winkler, K. Wu, and A. Stelzer, "Integrated receiver based on a high-order subharmonic self-oscillating mixer," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 6, pp. 1398–1404, 2007.

[172] L. Chiu, S. A. Winkler, Q. Xue, C. H. Chan, and K. Wu, "A low-power third-harmonic self-oscillating mixer using multi-harmonic load," *IEEE Microw. Wirel. Components Lett.*, vol. 22, no. 7, pp. 375–377, 2012.

[173] S. S. K. Ho and C. E. Saavedra, "A low-noise self-oscillating mixer using a balanced vco load," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 58, no. 8, pp. 1705–1712, 2011.

[174] A. Liscidini, A. Mazzanti, R. Tonietto, L. Vandi, P. Andreani, and R. Castello, "Single-stage low-power quadrature rf receiver front-end: The lmv cell," *IEEE J Solid-State Circuits*, vol. 41, no. 12, pp. 2832–2841, 2006.

[175] J. Deng, P. Burasa, and K. Wu, "Compact 140–220 ghz e/h waveguide phase shifter and its application to terahertz multiport circuits," *IEEE Trans. Terahertz Sci.*, vol. 13, no. 5, pp. 511–525, 2023.

[176] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. of Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, 2004.

[177] R. He and Y. Tousi, "Analysis of stable modes of a scalable coupled oscillator array," *IEEE Trans. Circuits Syst. II: Express Br.*, vol. 68, no. 2, pp. 647–651, 2021.

[178] S. Gierkink, S. Levantino, R. Frye, C. Samori, and V. Boccuzzi, "A low-phase-noise 5-ghz cmos quadrature vco using superharmonic coupling," *IEEE J. of Solid-State Circuits*, vol. 38, no. 7, pp. 1148–1154, 2003.

[179] Z. Hu, M. Kaynak, and R. Han, "High-power radiation at 1 thz in silicon: A fully scalable array using a multi-functional radiating mesh structure," *IEEE J. of Solid-State Circuits*, vol. 53, no. 5, pp. 1313–1327, 2018.

[180] S. ver Hoeye, L. Zurdo, and A. Suarez, "New nonlinear design tools for self-oscillating mixers," *IEEE Microw. Wirel. Components Lett.*, vol. 11, no. 8, pp. 337–339, 2001.

[181] S. A. Keivaan, P. Burasa, and K. Wu, "Virtual receiver matrix and combinatory analog operations for future multifunction reconfigurable sensing and communication wireless systems," *IEEE Transactions on Microwave Theory and Techniques*, vol. 71, no. 1, pp. 424–433, Jan. 2023.

[182] Y. Bigdeli, P. Burasa, and K. Wu, "Quadrature harmonic self-oscillating mixer: Toward large array multifunction receiver systems," *IEEE Transactions on Microwave Theory and Techniques*, vol. 72, no. 12, pp. 7061–7070, Dec. 2024.

[183] S. O. Tatu, A. Serban, M. Helaoui, and A. Koelpin, "Multiport technology: The new rise of an old concept," *IEEE Microwave Magazine*, vol. 15, no. 7, pp. S34–S44, Nov. 2014.

[184] P. Burasa, J. Deng, and K. Wu, "A 300-ghz dual-polarized cmos waveguide receiver for high-density terahertz integrated multichannel wireless systems-on-chip," *IEEE Transactions on Microwave Theory and Techniques*, vol. 73, no. 5, pp. 3044–3058, 2025.

[185] Z. Marvi and E. Ashoori, "Highly linear low power v-band down-conversion mixer in sige bicmos technology," in *Proc. IEEE Radio Wireless Symposium (RWS)*, Jan. 2020, pp. 159–161.

[186] J. Deng, P. Burasa, and K. Wu, "Joint multiband linear interferometric receiver for integrated microwave and terahertz sensing and communication systems," *IEEE Transactions on Microwave Theory and Techniques*, vol. 72, no. 9, pp. 5550–5562, Sep. 2024.

[187] B. Razavi, *Fundamentals of Microelectronics*, 3rd ed. Wiley, 2021.

[188] Q. Zhou, K.-Y. Wong, W. Chen, and K. J. Chen, "Wide-dynamic-range zero-bias microwave detector using algan/gan heterojunction field-effect diode," *IEEE Microwave and Wireless Components Letters*, vol. 20, no. 5, pp. 277–279, May 2010.

[189] S. Clochiatti *et al.*, "Low-noise resonant tunneling diode terahertz detector," *IEEE Transactions on Terahertz Science and Technology*, vol. 15, no. 1, pp. 107–119, Jan. 2025.

[190] S. Sakphrom and A. Thanachayanont, "A low-power cmos rf power detector," in *Proc. 19th IEEE Int. Conf. Electron., Circuits, Syst. (ICECS)*, Dec. 2012, pp. 177–180.

[191] S. A. Maas, *Nonlinear Microwave and RF Circuits*. Norwood, MA, USA: Artech House, 2003.

[192] Y. Bigdeli, S. A. Keivaan, P. Burasa, and K. Wu, "Towards the development of large-scale multifunction array transceiver systems," in *Asia-Pacific Microwave Conference Proceedings (APMC)*, Taipei, Taiwan, 2023, pp. 890–892.

[193] S. A. Keivaan, P. Burasa, and K. Wu, "Virtual receiver matrix and combinatory analog operations for future multifunction reconfigurable sensing and communication wireless systems," *IEEE Transactions on Microwave Theory and Techniques*, vol. 71, no. 1, pp. 424–433, Jan. 2023.

[194] Y. Bigdeli, P. Burasa, and K. Wu, "Quadrature harmonic self-oscillating mixer: Toward large array multifunction receiver systems," *IEEE Transactions on Microwave Theory and Techniques*, vol. 72, no. 12, pp. 7061–7070, Dec. 2024.

[195] J. Kim *et al.*, "An ultra-low-jitter, mmw-band frequency synthesizer based on digital subsampling pll using optimally spaced voltage comparators," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 12, pp. 3466–3477, Dec. 2019.

[196] L. Zhang *et al.*, "A compact 140-ghz power amplifier with 15.4-dbm psat and 14.25% peaking pae in 28-nm bulk cmos process," *IEEE Transactions on Microwave Theory and Techniques*, vol. 72, no. 5, pp. 3016–3030, May 2024.

[197] Y. Bigdeli, P. Burasa, and K. Wu, "Extending the dynamic range of square-law power detectors for large-scale receiver arrays," *IEEE Microwave and Wireless Technology Letters*, 2025.

[198] M. Saeed, A. Hamed, and R. Negra, "Compact, lumped-element six-port receiver with 25% bandwidth," in *European Microwave Conference (EuMC)*, Paris, France, 2015, pp. 1045–1048.

[199] H. L. Lee, D. H. Park, H. S. Jang, H. J. Dong, M. Q. Lee, and J. W. Yu, "Rf bio-radar system using a compact lumped six-port demodulator and quadrifilar helix antenna," in *Asia-Pacific Microwave Conference Proceedings (APMC)*, Seoul, Korea (South), 2013, pp. 987–989.

[200] S. A. Keivaan, P. Burasa, J. Deng, and K. Wu, "Concurrent detection of 2-d angle-of-arrival and polarization enabled by virtual transceiver matrix architecture," *IEEE Transactions on Microwave Theory and Techniques*, 2025.

[201] A. Serban *et al.*, "Six-port transceiver for 6–9 ghz ultrawideband systems," *Microwave and Optical Technology Letters*, vol. 52, no. 3, pp. 740–746, Mar. 2010.

[202] J. Lange, "Interdigitated stripline quadrature hybrid (correspondence)," *IEEE Transactions on Microwave Theory and Techniques*, vol. 17, no. 12, pp. 1150–1151, Dec. 1969.

[203] R. N. Simons, *Coplanar Waveguide Circuits, Components, and Systems.* Hoboken, NJ, USA: Wiley-Interscience, 2001.

[204] P. Burasa, J. Deng, and K. Wu, "A 300-ghz dual-polarized cmos waveguide receiver for high-density terahertz integrated multichannel wireless systems-on-chip," *IEEE Transactions on Microwave Theory and Techniques*, pp. 1–15, 2024.

[205] H. S. Lim, W. K. Kim, J. W. Yu, H. C. Park, W. J. Byun, and M. S. Song, "Compact six-port transceiver for time-division duplex systems," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 5, pp. 394–396, May 2007.

[206] J. Deng, P. Burasa, S. A. Keivaan, and K. Wu, "Waveguide receiver array for joint communication, sensing, and power transfer systems," *IEEE Transactions on Microwave Theory and Techniques*, vol. 73, no. 7, pp. 4204–4217, Jul. 2025.

[207] J. Deng, P. Burasa, and K. Wu, "Self-contained dual-input interferometric receiver for paralleled-multichannel wireless systems," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 71, no. 2, pp. 934–947, Feb. 2024.

[208] ——, "Joint multiband linear interferometric receiver for integrated microwave and terahertz sensing and communication systems," *IEEE Transactions on Microwave Theory and Techniques*, vol. 72, no. 9, pp. 5550–5562, Sep. 2024.

[209] E. Westberg, J. Staudinger, J. Annes, and V. Shilimkar, "5g infrastructure rf solutions: Challenges and opportunities," *EEE Microw. Mag.*, vol. 20, no. 12, pp. 51–58, 2019.

[210] A. Dogra, R. K. Jha, and S. Jain, "A survey on beyond 5g network with the advent of 6g: Architecture and emerging technologies," *IEEE Access*, vol. 9, pp. 67 512–67 547, 2021.

[211] C.-X. Wang, X. You, X. Gao, X. Zhu, Z. Li, C. Zhang, H. Wang, Y. Huang, Y. Chen, H. Haas, J. S. Thompson, E. G. Larsson, M. D. Renzo, W. Tong, P. Zhu, X. Shen, H. V. Poor, and L. Hanzo, "On the road to 6g: Visions, requirements, key technologies, and testbeds," *IEEE Commun. Surv. Tutorials*, vol. 25, no. 2, pp. 905–974, 2023.

[212] M. Z. Chowdhury, M. Shahjalal, S. Ahmed, and Y. M. Jang, "6g wireless communication systems: Applications, requirements, technologies, challenges, and research directions," *IEEE Open J. Commun. Soc.*, vol. 1, pp. 957–975, 2020.

[213] C. D. Alwis, A. Kalla, Q.-V. Pham, P. Kumar, K. Dev, W.-J. Hwang, and M. Liyanage, "Survey on 6g frontiers: Trends, applications, requirements, technologies and future research," *IEEE Open J. Commun. Soc.*, vol. 2, pp. 836–886, 2021.

[214] M. M. Kiasaraei, K. Nikitopoulos, and R. Tafazolli, "Toward ultra-power-efficient, tbps wireless systems via analogue processing: Existing approaches, challenges and way forward," *IEEE Commun. Surv. Tutorials*, vol. 26, no. 2, pp. 747–780, 2024.

[215] Y.-H. Hsiao, Z.-M. Tsai, H.-C. Liao, J.-C. Kao, and H. Wang, "Millimeter-wave cmos power amplifiers with high output power and wideband performances," *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 12, pp. 4520–4533, 2013.

[216] A. Roev, J. Qureshi, M. Geurts, R. Maaskant, M. K. Matters-Kammerer, and M. Ivashina, "A wideband mm-wave watt-level spatial power-combined power amplifier with 26% pae in sige bicmos technology," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 10, pp. 4436–4448, 2022.

[217] L. Zhang, K. Ma, H. Fu, Y. Wang, K. Wang, F. Meng, and X. Li, "A compact 140-ghz power amplifier with 15.4-dbm psat and 14.25% peaking pae in 28-nm bulk cmos process," *IEEE Trans. Microw. Theory Techn.*, vol. 72, no. 5, pp. 3016–3030, 2024.

[218] A. Alizadeh, P. V. Rowell, Z. Griffith, M. E. Urteaga, and M. J. W. Rodwell, "A 78-mw 220-ghz power amplifier with peak 18.4% pae in 250-nm inp hbt technology," *IEEE Trans. Microw. Theory Techn.*, vol. 72, no. 10, pp. 5789–5798, 2024.

[219] S. Hwang, J. Jeon, S. Bae, B. Yoon, S. Kang, and J. Kim, "A 5.15–7.125-ghz differential power amplifier with enhanced linearity of average power region using dynamic cross-coupled capacitor," *IEEE Trans. Microw. Theory Tech.*, vol. 72, no. 1, pp. 575–588, 2024.

[220] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*, ser. Artech House Microwave Library. Boston: Artech House, 2006.

[221] D. Widmann, T. Tannert, X.-Q. Du, T. Veigel, M. Grözing, and M. Berroth, "A time-interleaved digital-to-analog converter up to 118 gs/s with integrated analog multiplexer in 28-nm fd-soi cmos technology," *IEEE J. Solid-State Circuits*, vol. 59, no. 3, pp. 908–922, 2024.

[222] Y. M. Greshishchev, D. Pollex, S.-C. Wang, M. Besson, P. Flemeke, S. Szilagyi, J. Aguirre, C. Falt, N. Ben-Hamida, R. Gibbins, and P. Schvan, "A 56gs/s 6b dac in 65nm cmos with 256×6b memory," in *2011 IEEE Int. Solid-State Circuits Conf.*, 2011, pp. 194–196.

[223] K. Khalaf, V. Vidojkovic, K. Vaesen, M. Libois, G. Mangraviti, V. Szortyka, C. Li, B. Verbruggen, M. Ingels, A. Bourdoux, C. Soens, W. Van Thillo, J. R. Long, and

P. Wambacq, "Digitally modulated cmos polar transmitters for highly-efficient mm-wave wireless communication," *IEEE J. Solid-State Circuits*, vol. 51, no. 7, pp. 1579–1592, 2016.

[224] N. Deferm and P. Reynaert, "A 120 ghz fully integrated 10 gb/s short-range star-qam wireless transmitter with on-chip bondwire antenna in 45 nm low power cmos," *IEEE J. Solid-State Circuits*, vol. 49, no. 7, pp. 1606–1616, 2014.

[225] J. Chen, L. Ye, D. Titz, F. Gianesello, R. Pilard, A. Cathelin, F. Ferrero, C. Luxey, and A. M. Niknejad, "A digitally modulated mm-wave cartesian beamforming transmitter with quadrature spatial combining," in *2013 IEEE Int. Solid-State Circuits Conf. Digest of Technical Papers*, 2013, pp. 232–233.

[226] S. Carpenter, D. Nopchinda, M. Abbasi, Z. S. He, M. Bao, T. Eriksson, and H. Zirath, "A *d*-band 48-gbit/s 64-qam/qpsk direct-conversion i/q transceiver chipset," *IEEE Trans. Microw. Theory Tech.*, vol. 64, no. 4, pp. 1285–1296, 2016.

[227] A. Babakhani, D. B. Rutledge, and A. Hajimiri, "Transmitter architectures based on near-field direct antenna modulation," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2674–2692, 2008.

[228] P. Nazari, S. Jafarlou, and P. Heydari, "A cmos two-element 170-ghz fundamental-frequency transmitter with direct rf-8psk modulation," *IEEE J. Solid-State Circuits*, vol. 55, no. 2, pp. 282–297, 2020.

[229] C. Jiang, A. Cathelin, and E. Afshari, "A high-speed efficient 220-ghz spatial-orthogonal ask transmitter in 130-nm sige bicmos," *IEEE J. Solid-State Circuits*, vol. 52, no. 9, pp. 2321–2334, 2017.

[230] Z. Wang, H. Wang, Y. O. Hassan, and P. Heydari, "A bits-to-antenna f -band 120-gb/s cmos rf-64qam transmitter for futureg wireless links," *IEEE J. Solid-State Circuits*, pp. 1–17, 2025.

[231] S. Kang, S. V. Thyagarajan, and A. M. Niknejad, "A 240 ghz fully integrated wideband qpsk transmitter in 65 nm cmos," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2256–2267, 2015.

[232] L. Chen, S. Nooshabadi, A. Cathelin, and E. Afshari, "Variable-phase-shift based high data rate sub-thz fsk transmitter design: Theory and implementation," *IEEE Trans. Microw. Theory Tech.*, vol. 71, no. 2, pp. 669–681, 2023.

[233] S. Shopov, A. Balteanu, and S. P. Voinigescu, "A 19-dbm, 15-gbaud, 9-bit soi cmos power-dac cell for high-order qam w-band transmitters," in *2013 Proc. ESSCIRC*, 2013, pp. 69–72.

[234] T. Zhou, Y. Dong, S. Gong, S. Liang, K. Ding, X. Sun, S. Gu, B. Zhang, Z. Yang, and Y. Zhang, "A sub-terahertz high-speed traveling-wave switch modulator based on dynamically tunable double-resonant coupling units," *IEEE Trans. Microw. Theory Tech.*, vol. 71, no. 10, pp. 4346–4356, 2023.

[235] John G. Proakis and Masoud Salehi, *Digital Communications*, 5 ed. New York, NY, USA: McGraw-Hill, 2008.

[236] X. Que, Y. Wang, and S. Huang, "A 6-/12-dB back-off reconfigurable Doherty-like load modulated balanced amplifier with compact area and wide bandwidth," *Microelectronics Journal*, vol. 148, no. 7, p. 106198, apr 2024.

[237] C. J. Lee, H. Nam, D. Kim, S.-K. Kim, and D. Y. Lee, "A d-band variable gain low noise amplifier in a 28-nm cmos process for 6g wireless communications," *IEEE Trans. Microw. Theory Techn.*, vol. 71, no. 1, pp. 131–135, 2024.

[238] C. A. Balanis, *Antenna Theory: Analysis and Design*, 4th ed. Hoboken, NJ, USA: Wiley, 2016.

[239] I. F. Akyildiz, C. Han, Z. Hu, S. Nie, and J. M. Jornet, "Terahertz band communication: An old problem revisited and research directions for the next decade," *IEEE Trans. Commun.*, vol. 70, no. 6, pp. 4250–4285, 2022.

[240] K. Sengupta, X. Lu, S. Venkatesh, and B. Tang, "Physically secure sub-thz wireless links," in *2020 IEEE Int. Conf. Commun. Workshops*, 2020, pp. 1–7.

[241] N. Yang, L. Wang, G. Geraci, M. Elkashlan, J. Yuan, and M. Di Renzo, "Safeguarding 5g wireless communication networks using physical layer security," *IEEE Commun. Mag.*, vol. 53, no. 4, pp. 20–27, 2015.

[242] X. Chen, D. W. K. Ng, W. H. Gerstacker, and H.-H. Chen, "A survey on multiple-antenna techniques for physical layer security," *IEEE Commun. Surv. Tutorials*, vol. 19, no. 2, pp. 1027–1053, 2017.

[243] F. Fesharaki, T. Djerafi, M. Chaker, and K. Wu, "Low-loss and low-dispersion transmission line over dc-to-thz spectrum," *IEEE Trans. Terahertz Sci. Technol.*, vol. 6, no. 4, pp. 611–618, 2016.

[244] A. Puglielli, A. Townley, G. LaCaille, V. Milovanović, P. Lu, K. Trotskovsky, A. Whitcombe, N. Narevsky, G. Wright, T. Courtade, E. Alon, B. Nikolić, and A. M. Niknejad, "Design of energy- and cost-efficient massive mimo arrays," *Proc. IEEE*, vol. 104, no. 3, pp. 586–606, 2016.

[245] X. Lu, S. Venkatesh, B. Tang, and K. Sengupta, "Physical layer security through directional modulation with spatio-temporal millimeter-wave transmitter arrays," *IEEE J. Solid-State Circuits*, vol. 59, no. 9, pp. 2831–2847, 2024.

[246] J. Guo, L. Poli, M. A. Hannan, P. Rocca, S. Yang, and A. Massa, "Time-modulated arrays for physical layer secure communications: Optimization-based synthesis and experimental assessment," *IEEE Trans. Antennas Propag.*, vol. 66, no. 12, pp. 6939–6949, 2018.

[247] A. Kalantari, M. Soltanalian, S. Maleki, S. Chatzinotas, and B. Ottersten, "Directional modulation via symbol-level precoding: A way to enhance security," *IEEE J. Sel. Topics Signal Process.*, vol. 10, no. 8, pp. 1478–1493, 2016.

[248] N. Valliappan, A. Lozano, and R. W. Heath, "Antenna subset modulation for secure millimeter-wave wireless communication," *IEEE Trans. Commun.*, vol. 61, no. 8, pp. 3231–3245, 2013.

[249] J. Guo, S. Yang, Y. Chen, P. Rocca, J. Hu, and A. Massa, "Efficient sideband suppression in 4-d antenna arrays through multiple time modulation frequencies," *IEEE Trans. Antennas Propag.*, vol. 65, no. 12, pp. 7063–7072, 2017.

[250] Y. Tong and A. Tennant, "A two-channel time modulated linear array with adaptive beamforming," *IEEE Trans. Antennas Propag.*, vol. 60, no. 1, pp. 141–147, 2012.

[251] N. S. Mannem, T.-Y. Huang, E. Erfani, S. Li, D. Munzer, M. R. Bloch, and H. Wang, "A 25–34-ghz eight-element mimo transmitter for keyless high throughput directionally secure communication," *IEEE J. Solid-State Circuits*, vol. 57, no. 5, pp. 1244–1256, 2022.

[252] 3GPP, *NR; Base Station (BS) Radio Transmission and Reception*, 3rd Generation Partnership Project (3GPP) Std. TS 38.104, Jan. 2019.

[253] M. Alibakhshikenari, F. Babaeian, B. S. Virdee, S. Aïssa, L. Azpilicueta, C. H. See, A. A. Althuwayb, I. Huynen, R. A. Abd-Alhameed, F. Falcone, and E. Limiti, "A comprehensive survey on "various decoupling mechanisms with focus on metamaterial and

metasurface principles applicable to sar and mimo antenna systems"," *IEEE Access*, vol. 8, pp. 192 965–193 004, 2020.

[254] Y.-M. Zhang, Q.-C. Ye, G. F. Pedersen, and S. Zhang, "A simple decoupling network with filtering response for patch antenna arrays," *IEEE Trans. Antennas Propag.*, vol. 69, no. 11, pp. 7427–7439, 2021.

[255] Y. M. Pan, Y. Hu, and S. Y. Zheng, "Design of low mutual coupling dielectric resonator antennas without using extra decoupling element," *IEEE Trans. Antennas Propag.*, vol. 69, no. 11, pp. 7377–7385, 2021.

[256] A. Papoulis and S. U. Pillai, *Probability, Random Variables, and Stochastic Processes*, 4th ed. New York, NY, USA: McGraw-Hill, 2002.

[257] E. Westberg, J. Staudinger, J. Annes, and V. Shilimkar, "5g infrastructure rf solutions: Challenges and opportunities," *IEEE Microw. Mag.*, vol. 20, no. 12, pp. 51–58, 2019.

[258] A. Dogra, R. K. Jha, and S. Jain, "A survey on beyond 5g network with the advent of 6g: Architecture and emerging technologies," *IEEE Access*, vol. 9, pp. 67 512–67 547, 2021.

[259] C.-X. Wang, X. You, X. Gao, X. Zhu, Z. Li, C. Zhang, H. Wang, Y. Huang, Y. Chen, H. Haas, J. S. Thompson, E. G. Larsson, M. D. Renzo, W. Tong, P. Zhu, X. Shen, H. V. Poor, and L. Hanzo, "On the road to 6g: Visions, requirements, key technologies, and testbeds," *IEEE Commun. Surveys Tuts.*, vol. 25, no. 2, pp. 905–974, 2023.

[260] M. Z. Chowdhury, M. Shahjalal, S. Ahmed, and Y. M. Jang, "6g wireless communication systems: Applications, requirements, technologies, challenges, and research directions," *IEEE Open J. Commun. Soc.*, vol. 1, pp. 957–975, 2020.

[261] C. D. Alwis, A. Kalla, Q.-V. Pham, P. Kumar, K. Dev, W.-J. Hwang, and M. Liyanage, "Survey on 6g frontiers: Trends, applications, requirements, technologies and future research," *IEEE Open J. Commun. Soc.*, vol. 2, pp. 836–886, 2021.

[262] M. M. Kiasaraei, K. Nikitopoulos, and R. Tafazolli, "Toward ultra-power-efficient, tbps wireless systems via analogue processing: Existing approaches, challenges and way forward," *IEEE Commun. Surveys Tuts.*, vol. 26, no. 2, pp. 747–780, 2024.

[263] L. Han and K. Wu, "Multifunctional transceiver for future intelligent transportation systems," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 7, pp. 1879–1892, 2011.

[264] J. Moghaddasi and K. Wu, "Multifunction, multiband, and multimode wireless receivers: A path toward the future," *IEEE Microw. Mag.*, vol. 21, no. 12, pp. 104–125, 2020.

[265] S. A. Keivaan, P. Burasa, and K. Wu, "Virtual receiver matrix and combinatory analog operations for future multifunction reconfigurable sensing and communication wireless systems," *IEEE Trans. Microw. Theory Techn.*, vol. 71, no. 1, pp. 424–433, 2023.

[266] P. Heydari, "Terahertz integrated circuits and systems for high-speed wireless communications: Challenges and design perspectives," *IEEE Open J. Solid-State Circuits Soc.*, vol. 1, pp. 18–36, 2021.

[267] B. Yang, Z. Yu, J. Lan, R. Zhang, J. Zhou, and W. Hong, "Digital beamforming-based massive mimo transceiver for 5g millimeter-wave communications," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 7, pp. 3403–3418, 2018.

[268] B. Chan, B. Oyama, C. Monier, and A. Gutierrez-Aitken, "An ultra-wideband 7-bit 5-gsps adc implemented in submicron inp hbt technology," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2187–2193, 2008.

[269] L. Duncan, B. Dupaix, J. J. McCue, B. Mathieu, M. LaRue, V. J. Patel, M. Teshome, M.-J. Choe, and W. Khalil, "A 10-bit dc-20-ghz multiple-return-to-zero dac with >48-db sfdr," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3262–3275, 2017.

[270] Z. Shu, J. Zang, Q. Liu, T. Zhang, Y. Gao, C.-H. Heng, Y. Guo, and Z. Zhu, "A 2× time-interleaved 4-gs/s 14-bit dac with on-chip calibration of interleaving nonlinearities," *IEEE J. Solid-State Circuits*, pp. 1–15, 2025.

[271] H. Tataria, M. Shafi, M. Dohler, and S. Sun, "Six critical challenges for 6g wireless systems: A summary and some solutions," *IEEE Veh. Technol. Mag.*, vol. 17, no. 1, pp. 16–26, 2022.

[272] X. Zhang, B. Deng, L. Sun, D. Pan, and L. Cheng, "A w-band 0.18-db rms gain and 0.97° phase error active phase shifter in 28-nm cmos," *IEEE Microw. Wireless Technol. Lett.*, vol. 34, no. 7, pp. 923–926, 2024.

[273] S. Huang, Y. Wang, and G. Feng, "A compact 53–62 ghz phase shifter with series peaking technique in 40-nm cmos technology," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 71, no. 10, pp. 4407–4411, 2024.

[274] Z. Zhang, M. Yang, X. Geng, K. Wang, Q. Xie, and Z. Wang, "A 0.0325-mm^2 114-to-147-ghz 6-bit passive vector-modulated phase shifter with mn-embedded isolated power combiner achieving <3.7° rms phase error in 65-nm cmos," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 11, pp. 4394–4405, 2023.

[275] R. Ahamed, M. Varonen, D. Parveg, M. Najmussadat, Y. Tawfik, and K. A. I. Halonen, "A 200–250-ghz phase shifter utilizing a compact and wideband differential quadrature coupler," *IEEE Microw. Wireless Compon. Lett.*, vol. 32, no. 7, pp. 883–886, 2022.

[276] J. Pang, R. Wu, Y. Wang, M. Dome, H. Kato, H. Huang, A. T. Narayanan, H. Liu, B. Liu, T. Nakamura, T. Fujimura, M. Kawabuchi, R. Kubozoe, T. Miura, D. Matsumoto, N. Oshima, K. Motoi, S. Hori, K. Kunihiro, T. Kaneko, and K. Okada, "A 28ghz cmos phased-array transceiver featuring gain invariance based on lo phase shifting architecture with 0.1-degree beam-steering resolution for 5g new radio," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, 2018, pp. 56–59.

[277] R. Tseng, H. Li, D. H. Kwon, Y. Chiu, and A. S. Y. Poon, "A four-channel beamforming down-converter in 90-nm cmos utilizing phase-oversampling," *IEEE J. Solid-State Circuits*, vol. 45, no. 11, pp. 2262–2272, 2010.

[278] M. C. M. Soer, E. A. M. Klumperink, D.-J. van den Broek, B. Nauta, and F. E. van Vliet, "Beamformer with constant-gm vector modulators and its spatial intermodulation distortion," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 735–746, 2017.

[279] N. Oshima, M. Kitsunezuka, K. Tsukamoto, and K. Kunihiro, "A 30-mhz-to-3-ghz cmos array receiver with frequency and spatial interference filtering for adaptive antenna systems," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, 2016, pp. 326–329.

[280] P. Tahbazalli and M. S. Bakhtiar, "Wideband n-path-based phased-array receiver with gain and phase mismatch calibration," *IEEE Trans. Microw. Theory Techn.*, vol. 72, no. 7, pp. 4325–4336, 2024.

[281] S. Jeon, Y.-J. Wang, H. Wang, F. Bohn, A. Natarajan, A. Babakhani, and A. Hajimiri, "A scalable 6-to-18 ghz concurrent dual-band quad-beam phased-array receiver in cmos," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2660–2673, 2008.

[282] G. LaCaille, A. Puglielli, E. Alon, B. Nikolić, and A. M. Niknejad, "Optimizing the lo distribution architecture of mm-wave massive mimo receivers," *arXiv preprint arXiv:1911.01339*, Nov. 2019, accessed: Aug. 20, 2025.

[283] B. Yu, Z. Wang, O. Li, Q. Liu, H. Cai, Y. Zhou, G. Wang, B. Yan, R. Xu, and Y. Xu, "A 200-ghz four-element phased-array receiver system-in-package using htcc technology for sub-terahertz communications," *IEEE Trans. Microw. Theory Techn.*, vol. 72, no. 7, pp. 3920–3934, 2024.

[284] V. Szortyka, K. Raczkowski, M. Kuijk, and P. Wambacq, "A wideband beamforming lowpass filter for 60 ghz phased-array receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 9, pp. 2324–2333, 2015.

[285] M. Tabesh, J. Chen, C. Marcu, L. Kong, S. Kang, A. M. Niknejad, and E. Alon, "A 65 nm cmos 4-element sub-34 mw/element 60 ghz phased-array transceiver," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 3018–3032, 2011.

[286] K. Raczkowski, W. D. Raedt, B. Nauwelaers, and P. Wambacq, "A wideband beamformer for a phased-array 60ghz receiver in 40nm digital cmos," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, 2010, pp. 40–41.

[287] M. Hosoya, T. Mitomo, and O. Watanabe, "A 900-mhz bandwidth analog baseband circuit with 1-db step and 30-db gain dynamic range," in *Proc. Eur. Solid-State Circuits Conf. (ESSCIRC)*, 2010, pp. 466–469.

[288] S. D'Amico, A. Spagnolo, A. Donno, V. Chironi, P. Wambacq, and A. Baschirotto, "A low-power analog baseband section for 60-ghz receivers in 90-nm cmos," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 8, pp. 1724–1735, 2014.

[289] B. Razavi, *RF Microelectronics*, 2nd ed. Upper Saddle River, NJ, USA: Prentice Hall, 2012.

[290] J. P. Costas, "Synchronous communications," *Proc. IRE*, vol. 44, no. 12, pp. 1713–1718, Dec. 1956.

[291] 3GPP, "Nr; base station (bs) radio transmission and reception," 3rd Generation Partnership Project (3GPP), Tech. Spec. 38.104, Jun. 2024, [Online]. Available: https://www.3gpp.org.