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UNIVERSITÉ DE MONTRÉAL

**ANALYSE DE LA TESTABILITÉ DES CIRCUITS HAUTES
FRÉQUENCES**

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cette thèse intitulée:

**ANALYSE DE LA TESTABILITÉ DES CIRCUITS HAUTES
FRÉQUENCES**

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RÉSUMÉ

Avec la taille de plus en plus importante du marché des communications sans fil, le besoin de disposer d'outils de test performants des produits hautes fréquences se fait de plus en plus sentir. La détection et la localisation des défauts combinées à une précision des mesures sont devenues des impératifs incontournables dans une industrie de plus en plus compétitive. La présente thèse a pour objectif principal l'étude et la caractérisation du point de vue test des circuits intégrés fonctionnant en hautes fréquences.

Dans le chapitre 2, nous présentons une méthodologie permettant de détecter les défauts dans les circuits hautes fréquences linéaires. La méthodologie présentée utilise une analyse multifréquentielle de la sensibilité des paramètres S par rapport aux variations des composants internes du circuit (un amplificateur hautes fréquences linéaires). Cette analyse des paramètres S [Scattering parameters] nous a permis de déterminer six fréquences représentant les vecteurs de test dans le cas d'un amplificateur haute fréquence linéaire.

Une méthodologie plus adaptée aux circuits hautes fréquences non linéaires est présentée dans le chapitre 3. Elle est basée sur une analyse de la puissance. Une analyse de la sensibilité des niveaux de puissance par rapport aux variations de la valeur nominale des composants du circuit est effectuée. La fonction de transfert du circuit (dans notre cas, un amplificateur de puissance non linéaire hautes fréquences) est divisée en trois segments dans lesquels les variations de puissance seront effectuées. Les vecteurs de test déterminés avec cette méthodologie sont des niveaux de puissance.

Les méthodologies présentées dans les chapitre 2 et 3 constituent une avancée très importante vers une méthode de test intégrée des circuits hautes fréquences. Elles contribuent aussi à réduire considérablement le nombre de circuits intégrés défectueux dans une production à grande échelle.

Dans le chapitre 4, nous présentons une technique qui permet d'améliorer la précision des mesures effectuées sur certains circuits ITGE (Intégration à Très Grande Échelle) dans un environnement 50 ohms. Grâce à cette technique, on élimine les oscillations, les dépassements et les retards introduits par l'effet de la ligne de transmission et de la capacité parasite à l'entrée du comparateur de l'ATE (Automatic Test Equipment). Cette technique suggère l'insertion d'un circuit tampon haute vitesse entre le circuit à tester et la ligne de transmission d'impédance caractéristique 50 ohms. Le circuit tampon inséré présente des caractéristiques telles qu'il peut être connecté à la ligne de transmission sans introduire des distorsions. Afin de limiter l'effet de la capacité parasite à l'entrée du comparateur, nous suggérons aussi son utilisation dans une configuration de filtre passe tout.

ABSTRACT

The rapid growth of wireless communications has led to an increasing demand of reliable high frequency products. In order to satisfy this need in both quality and quantity, efficient methods of testing these products should be available in the industry. In this thesis, we present some methodologies that will help to improve the detection and localisation of faults in high frequency circuits. A solution to improve the test of some types of high frequency circuits with available test equipment is presented as well.

In chapter 2 and 3 we present two methodologies that will help to detect and localise faults in a high frequency circuit. They also help to have a very little rate of bad circuits after fabrication in a large scale production. These two methodologies are respectively addressed to high frequency circuits working in linear and nonlinear mode.

The methodology presented in chapter 2 is essentially addressed to linear high frequency circuits. It uses the concept of sensitivity combined to a multifrequency analysis of the S parameters. With this method we study the sensitivity of the S parameters of a linear high frequency amplifier according to the variation of the internal components of the circuit. This analysis helps us to deduct six critical test frequencies that can be used to detect and localize the defaults inside the considered circuit.

In chapter 3, we propose a methodology that is based on an in-segment power analysis of a nonlinear high frequency amplifier. The power transfer function is segmented into three functional area in which a sensitivity analysis of the power level is performed regarding the

variation of the components from their nominal values. In this case the test vectors are power levels.

In the chapter 4, we present a solution to the problems of ringings, overshoots, undershoots and timing delay problem when testing certain high frequency integrated circuits in a 50 ohms environment. The method proposed in this chapter uses a high speed buffer that will be inserted between the DUT (Device Under Test) and the transmission line. This buffer enables the DUT to drive the tester comparator through the transmission line without any impedance mismatch.

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CHAPITRE 1

INTRODUCTION GÉNÉRALE

1.1 Introduction

Le besoin de tester les systèmes électroniques est une nécessité dictée par un marché de plus en plus compétitif, où la qualité est devenue un facteur essentiel. De nos jours, assurer à un système électronique un niveau de qualité avant de le mettre sur le marché est devenu impératif. De nombreux chercheurs et ingénieurs oeuvrant dans la conception des systèmes électroniques affirment qu'une détection tardive des défauts est de plus en plus coûteuse. La détection d'un défaut au niveau carte est 10 fois plus coûteuse que la détection de la même défaut au niveau composant; elle est encore 100 fois plus coûteuse si elle est détectée lors de l'assemblage du système; et si elle est détectée chez le client, le coût est encore plus important [1]. Par conséquent, il est avantageux de détecter un défaut le plus tôt possible.

Le test de production d'un circuit est une sorte d'expérience dans laquelle un circuit est stimulé et les résultats qu'il produit sont analysés pour vérifier s'il se comporte correctement. Plusieurs types de tests peuvent être appliqués à un circuit intégré. Les tests paramétriques sont souvent appliqués pour vérifier les caractéristiques électriques des circuits, tels que les courants de fuites, les tensions de seuil, les impédances, etc.... Les tests

fonctionnels sont généralement appliqués pour vérifier si un circuit fonctionne correctement (selon les spécifications fonctionnelles). Quant aux tests structurels (l'objet d'une partie de cette thèse), ils sont appliqués pour tester la structure interne d'un circuit intégré.

La difficulté d'assurer un test adéquat pour un circuit intégré est une conséquence directe du développement de la technologie des circuits micro-électroniques. Ce développement de la technologie des semiconducteurs a rendu possible l'intégration de plusieurs centaines de milliers de transistors dans la même puce [3]. Cette possibilité d'intégration à haut niveau a cependant contribué à l'accroissement du nombre de circuits défectueux. Il est désormais nécessaire d'élaborer des stratégies de test susceptibles d'améliorer la fiabilité de ces circuits. Le test classique des circuits électroniques à base de composants discrets est généralement effectué en trois principales étapes [4]:

- le test des composants individuellement;
- le test des sous blocs;
- le test de la fonctionnalité du système dans son intégralité.

Avec l'avènement des circuits à intégration à très grande échelle (ITGE), cette approche se trouve limitée dans son efficacité. Cette limite s'explique par l'augmentation de la densité des circuits intégrés, la limitation du nombre de broches d'entrées et de sorties, et enfin la difficulté d'accès aux noeuds internes. Le test d'un circuit intégré aujourd'hui se fait en quatre étapes:

- la génération des vecteurs de test;

- l'application de ces vecteurs de test au circuit sous test;
- l'analyse de la réponse du circuit sous test;
- la localisation d'un éventuel défaut pour certains types de circuits.

Ainsi les différentes méthodologies de test actuellement disponibles sont essentiellement destinées à réduire au maximum la complexité de ces quatre étapes.

Dans ce chapitre, nous présenterons une brève revue de la littérature sur le test des circuits intégrés, nous aborderons ensuite les différents aspects de la testabilité des circuits hautes fréquences, nous discuterons enfin des objectifs et des motivations de la présente thèse.

1.2 Revue de la littérature

La littérature relative au test est abondante. Les premiers travaux dans le domaine remontent aux années soixante [5][7]. Depuis cette époque d'énormes efforts ont été déployés afin d'améliorer le test des circuits électroniques. Ainsi, la notion de "Conception Pour la Testabilité" (CPT) a été introduite [6][7][8][9][10][11][12]. La CPT a pour objectif de faciliter les procédures de test, de réduire la complexité des équipements de test et par conséquent les coûts inhérents au test. Elle vise à tenir compte très tôt des problèmes de test durant le cycle de conception du circuit. Les techniques de CPT ont atteint aujourd'hui un degré avancé de maturité avec la mise au point de plusieurs techniques de test. Cependant cette maturité concerne beaucoup plus les circuits numériques [11]. Par rapport aux circuits analogiques et mixtes les circuits numériques ont fait l'objet de plus recherches. On doit retenir que toutes les stratégies de test disponibles dans la littérature concernent les circuits

fonctionnant en basse et moyennes fréquences. Le test des circuits hautes fréquences se réduit jusqu'à présent en une série de mesures à effectuer sur le circuit.

1.2.1 Test des circuits numériques

Les circuits numériques présentent une certaine particularité: une grande partie des défauts peut aujourd'hui être modélisée facilement, ainsi plusieurs défauts sont ramenés aux modèles "collé à 1" ou "collé à 0". On parle de "collé à 1" ou "collé à 0" lorsqu'un noeud du circuit garde d'une manière anormale un état fixe soit "1" ou "0" quelque soit l'état de l'entrée. Aussi les circuits numériques offrent une observabilité et une contrôlabilité de leurs principaux noeuds [11]. La modélisation relativement facile des défauts, ajoutée à la contrôlabilité et à l'observabilité des noeuds expliquent en partie pourquoi le test des circuits numériques a atteint un niveau d'évolution avancé. Beaucoup de méthodes de test efficaces destinées aux circuits numériques ont été proposées à ce jour [20]. Parmi ces méthodes de test on peut citer: la méthode de Génération Automatique des Vecteurs de Test ou méthode ATPG, les méthodes de CPT non structurée, les méthodes de CPT structurée, et enfin les méthodes de test intégré ou "BIST" (Built-in-Self-Test).

1.2.1.1 Méthode ATPG (Génération Automatique de Vecteurs de Tests)

Plusieurs techniques et algorithmes traitant de la méthode ATPG sont disponibles dans la littérature [13][14][15][16]. Cette méthode consiste à tester un circuit en générant un vecteur de test pour chaque type de défaut. La génération des vecteurs de test peut se faire de manière aléatoire, pseudo-aléatoire, algorithmique, etc.... Avec cette méthode, seuls les

défauts pour lesquels des vecteurs de test sont générés sont détectables. La méthode ATPG est beaucoup plus efficace pour les circuits combinatoires du fait de l'initialisation requise dans les circuits séquentiels.

1.2.1.2 Méthode de CPT non structurée

Une des méthodes de CPT non structurée connue est la méthode d'insertion de point de test (IPT). Avec cette méthode on procède à l'insertion de points de test dans le circuit sous test afin de maximiser l'observabilité et la contrôlabilité des noeuds. Cette approche considérée comme ad-hoc est principalement destinée aux circuits combinatoires [17][18][19][20]. Elle évalue la testabilité du circuit afin de déterminer les parties difficiles à tester, pour ensuite y insérer de points de test [21]. On trouve également dans la littérature d'autres méthodes ad-hoc telles que le test par partitionnement, qui consiste à partitionner le circuit en plusieurs modules afin de les tester séparément.

1.2.1.3 Méthode CPT (Conception Pour la Testabilité) structurée

Plusieurs travaux ont été présentés ces dernières années sur la CPT structurée [22][23][24][25][26]. La méthode à balayage ou "Scan-Design" constitue une des principales formes de CPT structurée. Cette méthode ramène le circuit à tester en un circuit combinatoire testable avec la méthode "ATPG". L'idée principale sous-jacente à ces techniques est de relier les éléments de mémoires en forme de registre à décalage (appelée chaîne de balayage) durant le mode test. De cette manière, tous les éléments de mémoire deviennent directement contrôlables et observables à travers la chaîne de balayage.

L'enchaînement et le balayage des bascules peut être partiel ou intégral, on parle alors respectivement de balayage partiel ou de balayage intégral. Par ailleurs, on trouve une autre variante de la méthode à balayage appelée "Boundary-Scan". Cette variante est probablement la méthode de CPT structurée la plus utilisée dans l'industrie. Elle a été à cet effet adoptée par IEEE comme standard [27]. La méthode Boundary-Scan s'applique à l'extérieur du circuit contrairement au balayage intégral et au balayage partiel. Elle consiste à introduire des microcellules à chaque pin d'entrée et de sortie afin d'effectuer le balayage de ces microcellules. Il faut cependant noter que le "Boundary-Scan" est compatible avec les méthodes de balayage partiel et intégral. Une des raisons de la popularité de la méthode "Boundary-Scan" est le coût relativement bas de l'addition des registres de balayages aux plots d'entrées et de sorties.

1.2.1.4 Méthode de test intégré "BIST" (Built-In-Self-Test)

Le test intégré par rapport aux autres méthodes de CPT peut être considéré comme une technique active. Elle consiste à concevoir dans le circuit une structure qui lui permet de s'auto-tester sans apport extérieur [28]. Le test intégré se trouve être une méthode très rapide puisque le circuit est testé à sa fréquence de fonctionnement. Cette méthode intéresse beaucoup les ingénieurs de test. Elle permet de réduire considérablement le coût du test. Cependant, ce type de test se rapproche plus à un test fonctionnel. La structure interne de test permet uniquement de savoir si les paramètres choisis sont conformes ou non aux spécifications. Beaucoup de travaux ayant trait aux méthodes de test intégré ont été publiés ces dernières années [29][30][31][32][33]. En général, les approches BIST

peuvent être caractérisées par la nature de génération utilisée et par la forme du test appliqué. Ainsi on parle de BIST algorithmique versus aléatoire et de BIST exhaustif versus non exhaustif, les détails relatifs à ces types de BIST sont disponibles dans [21].

1.2.2 Test des circuits analogiques

Bien que largement disponibles et offrant des avantages considérables en terme de coût, de flexibilité et de fiabilité, les circuits analogiques présentent des difficultés considérables sur le plan test. Le test des circuits analogiques est plus difficile si on le compare au test des circuits numériques [6][34]. Ceci s'explique par les facteurs suivants:

- Les circuits analogiques sont caractérisés par plusieurs paramètres de natures différentes comme le gain, la phase, la fréquence de coupure, la bande passante, le taux de changement de la sortie, l'impédance d'entrée et de sortie, etc. De plus, le nombre et la nature de ces paramètres changent d'un circuit à un autre et d'une application à une autre. Ainsi le test analogique requiert des équipements dédiés aux circuits sous test. Tester avec précision tous ces paramètres et toutes ces spécifications peut en général être très coûteux voire impossible à réaliser.
- L'obligation d'élargir la marge de tolérance de la bande de décision pour chaque paramètre par rapport à la marge de tolérance définie par le concepteur du circuit. Cet élargissement de la marge de tolérance aura pour conséquence la diminution de la couverture de pannes.
- Les circuits analogiques présentent une accessibilité délicate, contrairement aux cir-

uits numériques, leurs performances peuvent subir des dégradations si on accède aux noeuds.

- Les circuits analogiques sont en fait des systèmes non linéaires fonctionnant en mode linéaire dans une plage bien définie. Le fonctionnement du circuit en mode non linéaire n'est pas en général bien compris par le concepteur. Ce manque de caractérisation en mode non linéaire peut introduire des complications au niveau du test.
- Le manque de modèle de défauts puissants et pratiques comme les modèles "collé à" couramment utilisés dans le test numérique rend encore la tâche des ingénieurs de test difficile.

Plusieurs travaux traitant du test des circuits analogiques ont été publiés au cours des dernières années [35][36][37][38][39][40][41]. Aujourd'hui les circuits analogiques peuvent être testés en utilisant des méthodes tels que le test fonctionnel (ou paramétrique), le test DC, le test " I_{DDQ} " ou méthode de contrôle du courant d'alimentation au point d'opération, et enfin le test intégré ou "BIST". Plusieurs règles de CPT ont été élaborées à partir de ces méthodes. Cependant, il n'existe aucune technique de test reconnue efficace pour tous les circuits analogiques.

1.2.2.1 Test paramétrique et fonctionnel

Le test fonctionnel consiste en la vérification de la fonction de chaque module pour des caractéristiques et conditions nominales définies, alors que le test paramétrique lui consiste

à vérifier les caractéristiques analogiques tels que les tensions, les courants, les impédances et les conditions de charge. Ces caractéristiques devraient se situer dans des limites de tolérance spécifiques [36][42][43]. Ce type de test bien que souvent utilisé connaît cependant des limites. Celles-ci s'expliquent par l'augmentation de la densité des circuits ITGE, du fait de l'isolation impossible des composants d'une part et la difficulté d'accès aux noeuds internes d'autre part.

1.2.2.2 Test DC

On trouve dans la littérature des travaux traitant du test DC [6][44][45]. Ce type de test consiste à tester le circuit en statique. Le test DC s'apparente beaucoup plus à un test de type paramétrique en DC.

1.2.2.3 Test “ I_{DDQ} ” ou contrôle du courant d'alimentation au point d'opération

La méthode de test “ I_{DDQ} ” constitue aujourd'hui l'une des méthodes de test les plus populaires. Elle est basée sur l'hypothèse qu'un circuit ne contenant aucun défaut consomme une faible quantité de courant à son point d'opération contrairement à un circuit contenant un défaut. La variation du flux du courant au point d'opération en présence d'un défaut permet de détecter ce dernier. Plusieurs publications sur la méthode “ I_{DDQ} ” sont disponibles dans la littérature relative au test [46][47]. Plusieurs fabricants la trouvent très intéressante du fait qu'elle offre une bonne couverture de panne [48].

1.2.2.4 Test intégré analogique ou “BIST” analogique

L'efficacité des techniques de test de circuits analogiques précédemment mentionnées dépend en général d'une bonne sélection des vecteurs de test. Ainsi le problème de la génération des vecteurs de test s'accroît proportionnellement avec la complexité des circuits. Le test intégré analogique tout comme le test intégré numérique consiste à concevoir dans le circuit à tester une structure qui lui permet de s'auto-tester en toute indépendance. Cette caractéristique explique l'intérêt que cette méthode suscite auprès des ingénieurs de test. Plusieurs travaux sur le test intégré analogique sont aujourd'hui disponibles dans la littérature [4][49].

1.2.3 Test des circuits mixtes

La demande croissante des circuits mixtes qui présentent une partie analogique et une partie numérique a récemment introduit un besoin pressant d'amélioration des méthodes de test de ces circuits. La difficulté du test des circuits mixtes réside plus dans les problèmes encourus pour tester les circuits analogiques. En effet, 90% des efforts sont engloutis par le test de la partie analogique. Dans la littérature le test des circuits analogiques et des circuits mixtes sont en général classés dans la même catégorie. On trouve désormais différentes méthodes de test des circuits mixtes dans la littérature [50][51][52][53]. On peut constater qu'il n'existe pas encore une méthode de test universellement acceptée pour tester les circuits mixtes. L'utilisation des techniques de traitement numérique des signaux

connus sous le nom de DSP (Digital Signal Processing) est de plus en plus fréquent dans le cadre du test mixte[52][53][54].

1.3 Test des circuits hautes fréquences

Avec des ventes annuelles estimées à environ 50 milliards de dollars, le marché des communications sans fils et des différents systèmes utilisant les circuits hautes fréquences est en pleine expansion. Un des principaux objectifs des fabricants de circuits intégrés consiste désormais en la mise sur le marché de circuits intégrés hautes fréquences performants et fiables. De ce fait, la testabilité des circuits hautes fréquences est devenue un enjeu de taille pour les ingénieurs. Jusqu'ici le concept de testabilité était plus utilisé pour les circuits intégrés numériques et analogiques fonctionnant à basses et moyennes fréquences. Les efforts pour produire des algorithmes et des outils de test performants ont été plus destinés à ces circuits. La complexité des circuits hautes fréquences, associée au manque d'outils de test performants rend le test des circuits hautes fréquences difficile, itératif, lent et par conséquent coûteux. On doit dire que la notion de hautes fréquences devient de nos jours très relative. Avec le développement de la technologie des semiconducteurs on a tendance à repousser de plus en plus en plus la frontière entre les basses fréquences et les hautes fréquences. Cependant dans ce présent travail nous considérons comme hautes fréquences toute fréquence supérieure à 200 MHz.

A ce jour, le test des circuits hautes fréquences se réduit à un test fonctionnel et paramétrique [55][56]. On trouve dans la littérature plusieurs travaux relatifs au test

fonctionnel et paramétrique des circuits hautes fréquences [55][56][57][58][59], contrairement au test structurel hautes fréquences qui reste encore un domaine inexploré. Peu de publications ont été consacrées au test structurel. Cependant on peut considérer une méthode récemment proposée par Jarwala et al. [60] comme une timide percée dans ce domaine. Jarwala et al. ont en effet proposé une stratégie de test de circuits hautes fréquences combinant la méthode “Boundary-Scan” et les méthodes de traitement numérique du signal. Cette stratégie s’inspire principalement de la méthode de balayage largement utilisée dans le test numérique. La stratégie proposée reste cependant très liée au test fonctionnel, car en réalité il s’agit de tester la fonctionnalité d’un système complexe composé de plusieurs modules, en évitant la procédure de test traditionnelle d’un tel système, jugée onéreuse. Cette procédure traditionnelle requiert le test individuel des modules pour ensuite tester le système dans sa globalité comme illustré par la Figure 1.1. Celle-ci représente le diagramme bloc d’un système générique hautes fréquence. Elle donne une idée de la procédure de test traditionnelle que Jarwala et al. ont tenté d’améliorer. Avec cette procédure on s’assure à laisser des points (P_1 , P_2 , P_3) de prélèvement du signal à l’entrée et à la sortie de chaque module du système pour tester leur fonctionnalité à partir des niveaux de signal détecté.

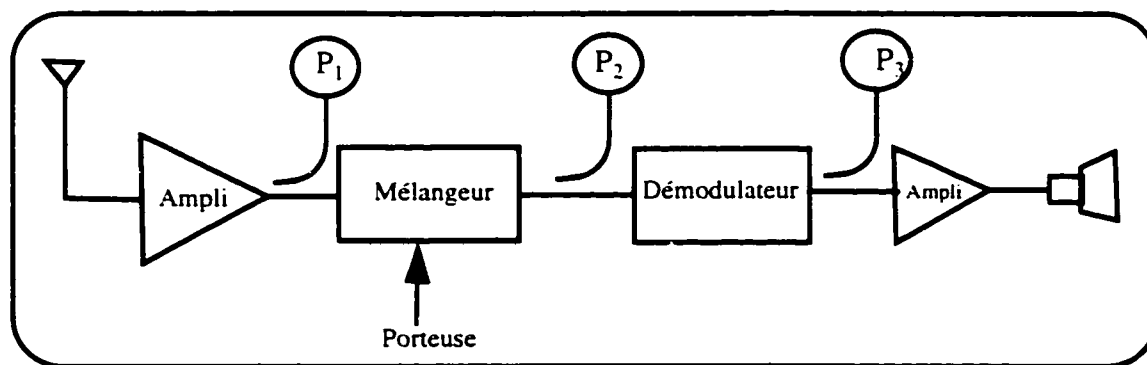


Figure 1.1 Diagramme bloc d'un système générique hautes fréquences, avec les différents points de test des modules

Le manque de littérature sur le test structurel hautes fréquences s'explique en partie par le faible niveau d'intégration des circuits hautes fréquences. Jusqu'à une date récente ce niveau était très bas par rapport aux circuits fonctionnant en basses et moyennes fréquences [61]. Ce faible niveau d'intégration n'a guère favorisé la recherche sur de nouvelles méthodologies élaborées de test des circuits hautes fréquences.

La Figure 1.2 illustre le modèle de test utilisé par l'industrie pour tester les circuits hautes fréquences lors d'une production à grande échelle. Les paramètres les plus importants du circuit à tester sont mesurés, et leurs valeurs comparées aux spécifications afin de pouvoir se prononcer sur leur fonctionnalité. Le circuit est déclaré bon si tous les paramètres mesurés se trouvent dans la plage de valeurs spécifiées. Si les valeurs mesurées sortent de cette plage, le circuit est dit mauvais, il est alors destiné au rebut. Il arrive parfois que les valeurs des paramètres soient légèrement aux alentours de la limite de tolérance et offrent une possibilité de récupération du circuit. On procède alors à un ajustement du circuit pour

le rendre utilisable. Cet ajustement consiste en de petits réglages du circuits pour forcer les paramètres de sortie du circuits à se rapprocher le maximum possible des plages de valeurs spécifiées.

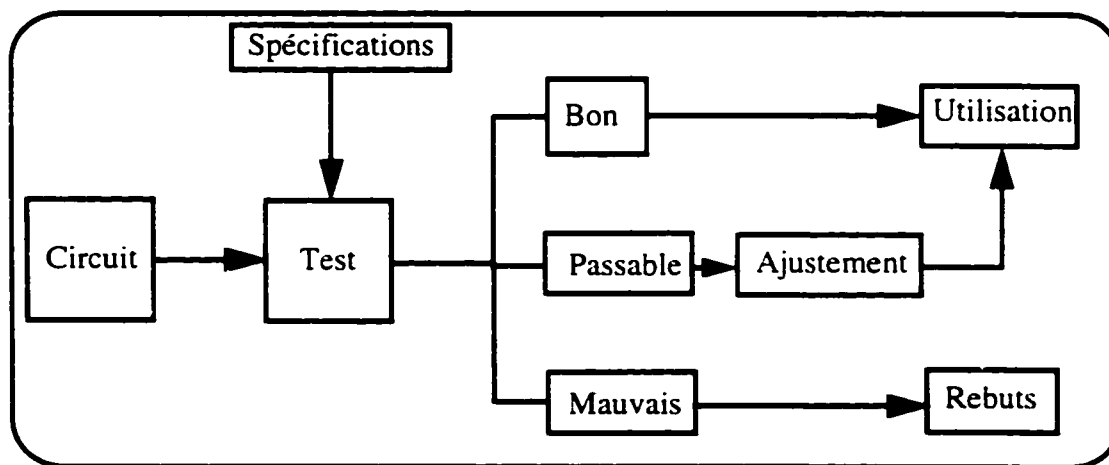


Figure 1.2 Modèle de test utilisé pour les circuits hautes fréquences

Une des particularités des circuits hautes fréquences est le nombre important de paramètres à mesurer [62]. Ce nombre croît proportionnellement à la complexité du circuit. La figure 1.3 présente les paramètres les plus importants à tester dans le cas d'un amplificateur hautes fréquences. Tous les paramètres définis à la Figure 1.3 ne sont pas mesurés avec les même types d'équipements, on peut déduire le coût relativement élevé du test des circuits hautes fréquences. Les équipements nécessaires pour caractériser avec efficacité un amplificateur linéaire et non linéaire hautes fréquences sont décrits par la figure 1.4. Afin de réduire le coût inhérent à ces équipements de test, Heutmacker et al. ont récemment suggéré des méthodes de caractérisation rapides et efficaces des circuits hautes fréquences en utilisant

les signaux numériques du type BPSK (Binary Phase Shift Keying). Leur méthode qui réduit le nombre d'instruments et de paramètres requis est principalement destinée aux amplificateurs de puissance hautes fréquences, qui sont aujourd'hui très sollicités dans les communications sans fils [63][64][65].

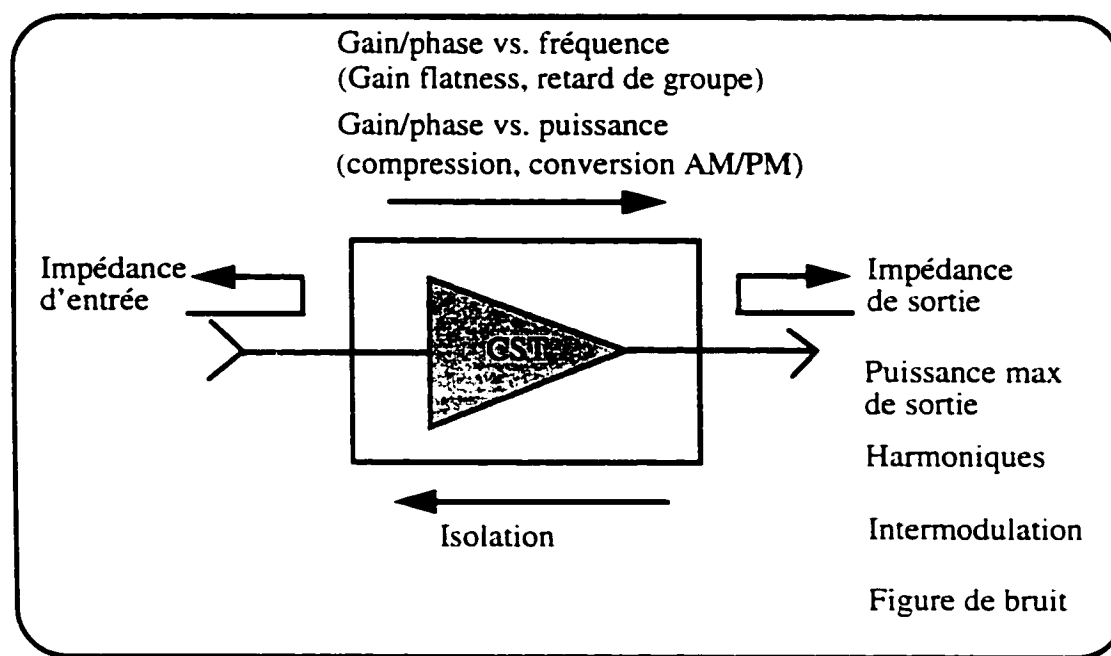


Figure 1.3 Mesures à effectuer sur un amplificateur hautes fréquences

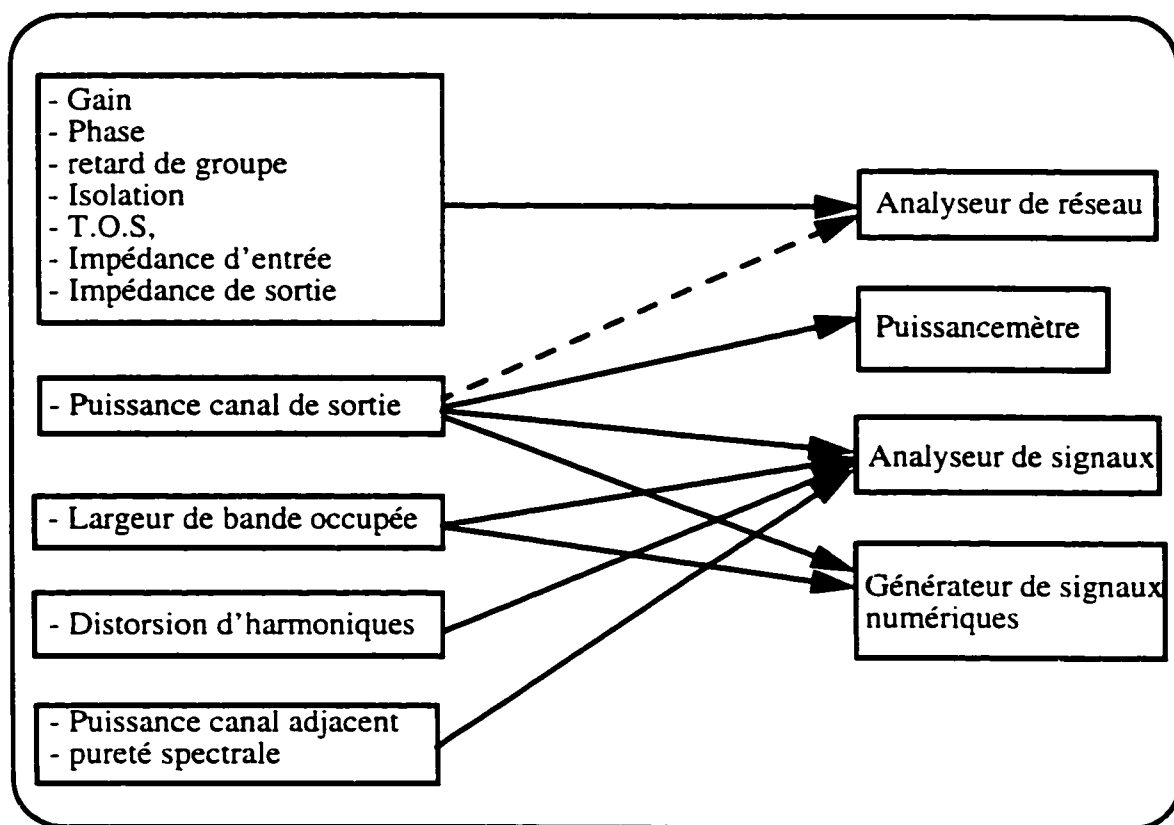


Figure 1.4 Instrumentation requise pour le test des différents paramètres d'un amplificateur hautes fréquences

Une autre particularité du test des circuits hautes fréquences est l'environnement standard d'impédance 50 ohms dans lequel fonctionnent les équipements de test. Afin d'avoir un maximum de transfert de puissance et une bonne transmission du signal entre les équipements et le circuit hautes fréquences sous test, ce dernier doit présenter des impédances de terminaisons égales à 50 ohms [83]. Avec une terminaison différente de 50 Ohms, on assiste à des distorsions et d'éventuelles oscillations qui auront pour conséquence la dégradation du signal et le manque de précision des mesures [84]. Ainsi la grande majorité des circuits hautes fréquences sont conçus en tenant compte de cette contrainte. On observe ainsi des étages d'adaptation à l'entrée et à la sortie des circuits hautes fréquences, qui permettront au circuit de présenter des terminaisons adaptées à l'environnement standard 50 ohms. Plusieurs travaux relatifs à ces circuits d'adaptation sont disponibles dans la littérature [77][78][88]. Cependant avec le développement de la technologie des semiconducteurs on a assisté à l'émergence de nouveaux types de circuits tels que les circuits "CMOS" qui présentent des difficultés à présenter des impédances de sorties égales à 50 ohms lorsqu'ils fonctionnent en hautes fréquences.

1.4 Objectifs et motivations de la thèse

La communauté de test se trouve de plus en plus confrontée à l'inefficacité et à l'inadaptation au besoin actuel du marché du modèle de test traditionnel des circuits hautes fréquences lors d'une production à grande échelle illustrée à la Figure 1.2. Afin d'aider l'industrie à être plus compétitive, il est devenu impératif de procéder à l'élaboration de

nouvelles stratégies de test. La présente thèse s'inscrit dans cette perspective. Elle vise principalement deux objectifs:

- Le premier découle de l'analyse du modèle de test présenté à la Figure 1.2. L'analyse de ce modèle met en évidence un handicap majeur dans le cadre d'une production à grande échelle. En effet, une fois le circuit déclaré mauvais, il est considéré comme perdu. A date il n'existe pas d'algorithme ou de stratégie de test capable de pouvoir localiser le défaut à l'intérieur du circuit à l'image des circuits numériques et analogiques fonctionnant à basses et moyennes fréquences. Le seul recours possible est l'observation exhaustive du dessin de masque afin de s'assurer que le défaut ne provient pas d'une connexion oubliée entre les couches etc... [65]. Si l'observation du dessin de masque s'avère infructueuse, on doit alors recommencer toute la procédure de conception, de fabrication et de test telle qu'illustrée à la Figure 1.5. Cette procédure s'avère très onéreuse car elle représente plusieurs heures de travail et n'offre pas une garantie de réussite en cas de reprise du processus de conception et de fabrication. Dans cette thèse nous proposons une approche permettant de détecter et de localiser les défauts dans les circuits intégrés dits défectueux. Cette localisation du défaut permet ainsi de concevoir une nouvelle fois le circuit en limitant au maximum le risque de fabrication de circuit défectueux. Le modèle illustré à la Figure 1.6 est une illustration de l'idée développée dans cette thèse. On note le module "Localisation des défauts" qui constitue l'un des objectifs de cette thèse. Ce module est réalisé en utilisant une analyse multifréquencielle de la sensibilité des paramètres $[S]$ pour les circuits hautes fréquences linéaires. Pour les circuits hautes fréquences non

linéaires, l'analyse de sensibilité est combinée à une analyse de puissance. Ce module permettra d'observer à la sortie des défauts affectant les composants internes du circuit. Nous ne considérons dans ce travail que le cas où le circuit ne présente qu'un seul défaut. En aidant à localiser un défaut dans un circuit et à expliquer son origine, avant la reconception et la fabrication on peut indirectement évaluer l'efficacité du procédé de fabrication. Elle permet aussi de réaliser d'énormes économies sur le coût de production d'un circuit intégré.

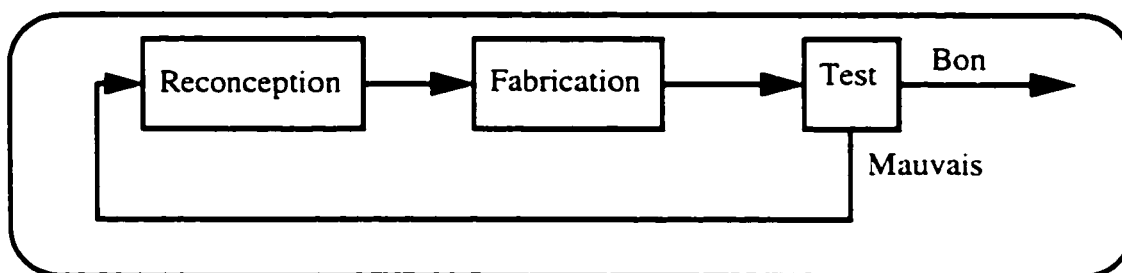


Figure 1.5 Boucle de reconception, fabrication et test dans le cas d'un mauvais circuit

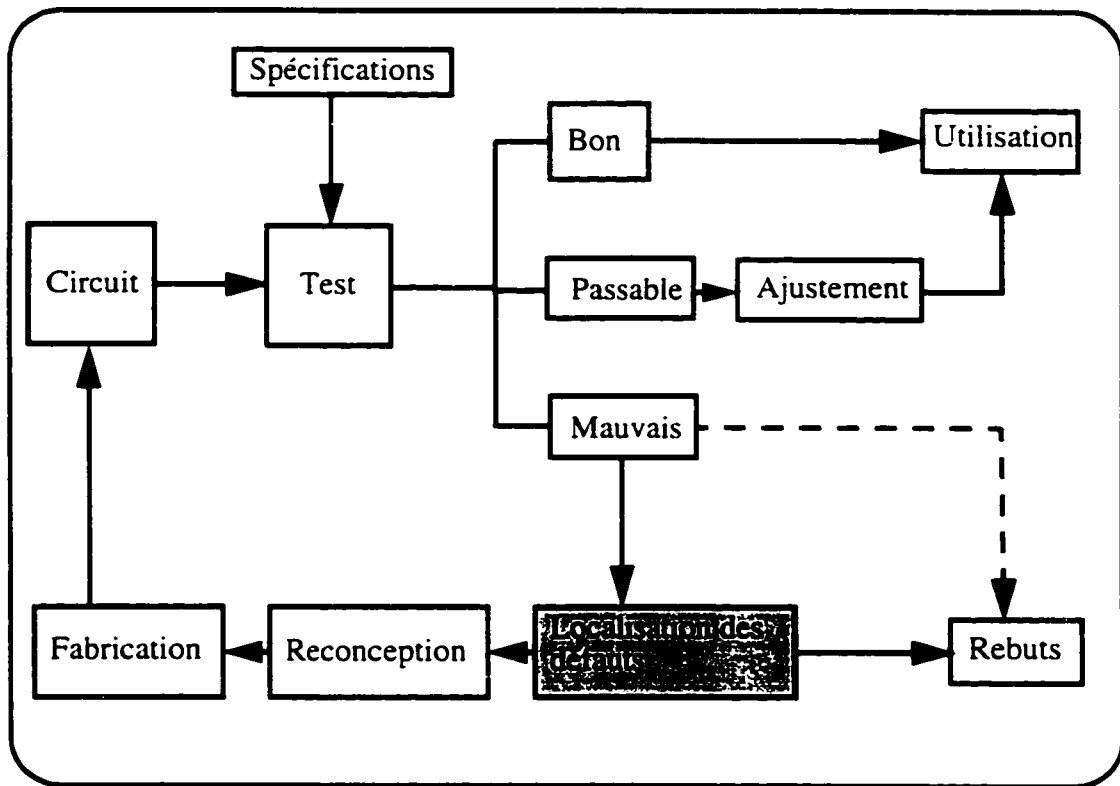


Figure 1.6 modèle de test modifié

- Le deuxième objectif visé dans cette thèse est l'amélioration de l'interface de test des circuits ITGE fonctionnant en hautes fréquences. Comme nous l'avons mentionné auparavant certains circuits ITGE fonctionnant en hautes fréquences présentent une incompatibilité avec l'environnement standard de 50 ohms. Certains de ces circuits présentent des impédances de sortie variables pouvant descendre jusqu'à 11 ohms. On assiste ainsi à des phénomènes de distorsions (dépassements, oscillations, etc...) qui affectent l'intégrité du signal. Dans cette thèse nous proposons d'étudier le pro-

blème d'adaptation en impédance des circuits ITGE qui présentent des problèmes de compatibilité avec les équipements de test afin d'assurer l'intégrité des signaux au niveau de l'interface de test. Afin de remédier à cette incompatibilité, nous proposons l'utilisation d'un circuit tampon qui servira à améliorer l'interface entre le circuit sous test et le testeur. Le circuit tampon est inséré entre le circuit à tester et la ligne de transmission. Un circuit tampon est généralement constitué d'un étage suiveur et d'un étage de puissance. Les circuits tampon présentent des impédances d'entrée élevées contrairement à leur impédances de sortie faibles. Par ailleurs ils permettent la transmission d'un signal avec un niveau de courant très important. On trouve dans la littérature des informations relatives aux circuits tampon avec leurs différentes caractéristiques [90] [91] [92]. L'originalité de la méthode proposée réside dans la vitesse du circuit tampon et aussi dans sa capacité de s'adapter à la ligne de transmission d'impédance caractéristique 50 ohms du point de vue courant de sortie et d'impédance. Il est important de souligner que la méthode proposée est basée sur l'hypothèse que la connection entre le circuit à tester et le circuit tampon est idéale. Avec la méthode proposée nous diminuons l'effet de la capacité parasite à l'entrée de testeur, en utilisant cette capacité parasite comme un élément d'une configuration de filtre passe-tout.

1.5 Conclusion

Au cours de ce chapitre, nous avons expliqué l'importance du test dans le processus de conception et de fabrication des circuits intégrés dans une production à grande échelle.

Nous avons passé en revue les différents travaux qui ont été présentés sur le test des circuits intégrés, les différents aspects du test des circuits hautes fréquences, avant d'expliquer les objectifs, et la particularité de cette thèse. Cette thèse se présente comme un travail exploratoire du test des circuits hautes fréquences dans son aspect divers. Son originalité vient des notions de testabilité et de test structurel qui sont pour la première fois introduites dans le domaine des hautes fréquences.

Le chapitre 2 sera consacré à l'analyse de la testabilité des circuits hautes fréquences linéaires. Il sera question de la méthodologie utilisée pour détecter et localiser les défauts dans un circuit hautes fréquences défectueux fonctionnant en mode linéaire. Cette approche utilise un ensemble de méthodes d'analyse et de modélisation. Elle permet d'établir une corrélation entre les défauts et les paramètres de sorties des circuits hautes fréquences linéaires.

Le chapitre 3, à l'image du chapitre 2, traitera de la détection et la localisation des défauts dans les circuits hautes fréquences non linéaires.

Les approches proposées dans les chapitres 2 et 3 constituent un jalon important vers la réalisation de méthodes de test structurel des circuits intégrés hautes fréquences lors de production à grande échelle.

Dans le chapitre 4, nous aborderons le problème de l'intégrité du signal au niveau de l'interface de test hautes fréquences des circuits ITGE. Dans ce chapitre nous présentons une technique qui permet d'améliorer l'intégrité des signaux lorsqu'ils traversent cette interface de test.

Les conclusions qui découlent de cette thèse seront présentées au chapitre 5. On y fera un rappel des points saillants et les possibles axes de recherches futurs.

CHAPITRE 2

ANALYSE ET AMELIORATION DE LA TESTABILITE DES CIRCUITS INTEGRES HAUTES FREQUENCES FONCTIONNANT EN MODE LINEAIRE

2.1 Résumé

Dans l'introduction générale nous avons évoqué la nécessité de disposer d'algorithmes nous permettant de procéder à une localisation des défauts dans les circuits intégrés hautes fréquences. La localisation d'un défaut et l'explication de son origine aideront à réduire considérablement le temps alloué au test et par conséquent le coût de production des circuits intégrés hautes fréquences. A travers l'article proposé dans ce chapitre, nous présentons une méthodologie qui est destinée à faciliter la localisation des défauts dans les circuits intégrés hautes fréquences. La méthodologie présentée est destinée principalement aux circuits hautes fréquences fonctionnant en mode linéaire. Un circuit est considéré fonctionnant en mode linéaire si le signal appliqué à l'entrée est récupéré à la sortie avec seulement des altérations au niveau amplitude et phase, sans génération de fréquences additionnelles.

En utilisant le concept de la sensibilité [Annexe I], nous avons établi les corrélations entre les composants internes du circuit hautes fréquences sous test et les paramètres de sortie.

La méthodologie est basée sur une analyse multifréquentielle de la sensibilité des paramètres S par rapport aux variations des composants internes du circuit. Les paramètres S [Annexe II] ont été choisis du fait qu'ils offrent une plus grande facilité de caractérisation des circuits hautes fréquences linéaires. Ils sont considérés aujourd'hui comme la façon la plus efficace de modéliser, et d'évaluer les performances des circuits hautes fréquences linéaires. La dépendance des paramètres S par rapport aux fréquences utilisées explique aussi l'aspect multifréquentiel de l'approche. Nous avons établi des corrélations entre les défauts affectant les différents composants internes du circuit et les différents paramètres S .

Notre analyse a porté principalement sur les amplificateurs hautes fréquences qui sont aujourd'hui parmi les circuits les plus sollicités.

La méthodologie présentée dans ce chapitre comporte une pertinence qui dépasse l'aspect test, elle permet aussi de tirer des informations intéressantes ayant trait à la conception et à la fabrication des circuits hautes fréquences. En effet, en arrivant à déterminer l'influence de la variation d'un élément ou d'une topologie sur les paramètres d'un circuit, on arrive à maximiser les performances de notre circuit. On peut ainsi facilement déterminer les dispositions à prendre au niveau conception, dessin de masque, et procédé de fabrication pour maximiser le rendement de la production d'un circuit. Nous brisons ainsi le mur qui existe entre la conception des circuits hautes fréquences et leur fabrication en tenant compte de l'aspect test et fabrication depuis la phase de conception. L'article présenté dans

le chapitre est intitulé "Joint Design and Test Consideration in High Frequency Circuits".

Il a été publié dans "Microwave and Optical Technology Letter" du mois d'octobre 1997.

2.2 Joint Design and Test Consideration in High Frequency Circuits

Joint Design and Test Consideration in High Frequency Circuits

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Abstract

RF systems technology is continually pushing maximum operating frequencies upward. This is constraint manufactures of RF products to specify their circuits in terms of scattering parameters. Integrating design and test is one of the highly desirable analog systems requirements. In this paper, a frequency domain analysis of RF systems is performed. This analysis is destined to ameliorate the design performance and to facilitate the test of a given product. It helps a design engineer to determine parameters influencing the circuit performances and the best topology that can be used to help improve these performances. On the other hand, it helps a test engineer to plan its test strategy and to predict which elements can be isolated by a given test set. By this analysis, we determine correlation between the different components in a circuit and their conjoint influence on the output.

1. Introduction

In integrated circuits, testability features become essential during the design and operational phases of systems. The trend towards miniaturization has decreased test access and increased test complexity. The densities of analog circuits continue to increase but the detection and isolation of faults in these circuits becomes more difficult due to the nature of analog faults and to the density of today's analog circuits. Integrating design and test is one of the highly desirable analog systems requirements. Until now design of analog circuits is still hand created by designers by using simulation and manual adjustment which is time consuming.

When the complexity and the operating frequency of a system increase, the possibility of testing this system becomes difficult with the available test equipments. Considering the complexity of analog testing and the high frequency constraints, testing RF systems introduces a new challenge to the test community. In the last years, the progress of analog and mixed signal devices and their application to wireless and cellular telephones introduces a mass market of these products. These RF systems technology is continually pushing maximum operating frequencies upward. This constraints manufactures of RF products to specify their circuits in terms of scattering parameters (S-parameters). This affects design engineers who must now switch their thinking from the well-known H, Y and Z parameters to the S parameters. The S parameters are most commode because they are easy to measure with modern network analyzers, their use in high frequency is conceptually simple, and they provide meaningful design information. Furthermore, flow

graph theory is readily applicable. In order to characterize the behavior of a two-port network, measured data of both its transfer and impedance functions must be obtained. At low frequencies, the Z, Y, H or ABCD parameters are examples of network functions used in the description of two-port networks. These parameters cannot be measured accurately at higher frequencies because the required short- and open-circuit tests are difficult to achieve over a broadband range of microwave frequencies. However, S parameters give an exact modeling of RF systems in the range of operating frequencies.

Most published testability analysis methods for analog circuits targeted medium and low frequency circuits. In the past few years some approaches were proposed in [1] and [2]. Test vector selection that allows maximization of the deviation between the output voltage of the good and faulty circuits is discussed. The approach presented in [1] is intended to derive the input stimuli $x(t)$ that magnify the difference between the response $y(t)$ of the good circuit and the response $y'(t)$ of the bad circuit. The algorithm is formulated as a quadratic programming problem to provide the solution that maximizes the quadratic difference $(y(t)-y'(t))^2$ by knowing the impulse responses $h(n)$ and $h'(n)$ of the good and bad circuits respectively. In [2], test frequencies are chosen only for the presence of single faults and no test point selection criteria are specified. Fault equivalence study in mixed signal circuits using a probabilistic computational technique is proposed in [3]. Concepts such as fault masking, fault dominance, fault equivalence, fault isolation defined to determine the relationship between faults and their effects at the output is presented in [4]. Test nodes and test frequencies selection was performed for every category of faults

(single, double, multiple). Testability analysis of analog circuits in the presence of soft, large-deviation, and hard faults is given in [5]. In [5], a set of test vectors is generated to observe and cover these faults. Some techniques for wireless communication systems are recently proposed. In [6], a Built-In-Self scheme to extract parameters such as signal to noise ratio, frequency response, intermodulation distortion for the receiver and transmitter section of an RF codec is presented using digital signal processing techniques. In [7], a test architecture which combines Boundary scan and a digital signal processing based functional testing of RF circuits is proposed to achieve system self-test.

Some of the approaches presented above are destined for low and medium frequency systems analysis. The others which utilize some digital signal processing techniques are only useful for systems containing the basic components to perform this type of processing. In this paper, a frequency domain analysis of RF systems is presented. This type of analysis is destined to ameliorate the design performance and to facilitate the test of high frequency circuits. The proposed testability analysis methodology helps improve the manufacturability of RF designs in the presence of high frequency constraints. It helps the design engineers to determine the parameters influencing the design performances and its sensitivity to the process variation. From the analysis results, the best topology of a circuit can be determined and the internal components can be matched and controlled to increase the circuit performances. On the other hand, this type of analysis permits to the test engineer to predict which components can be isolated by a given test set, and which kind of defects can be observed at a given test node. Analyzing testability in the frequency domain is an interesting approach to choose adequate test frequencies for increasing fault

diagnosis. On the other hand, not all test points and frequencies are equally useful, some selection criteria must be developed to ensure that a necessary, sufficient, and robust set is chosen. The proposed methodology uses the sensitivity concept as a mathematical tool to perform the analysis. In the next section we will give a brief description of the sensitivity and how it is used to observe defects. In section 3, we will explain the proposed approach and in section 4 we will give the simulation results.

2. Sensitivity concept

In designing electronic circuits, the circuit's performance deviations due to changes in the values of its elements should be known. The deviation of the elements' values with respect to their nominal values depends on the manufacturing process and on the temperature of the element. Sensitivity gives a measure of the circuit's performance change for a change in the circuit elements' values [8][9][10]. This helps the designer to choose adequate element tolerances. A good design of a circuit requires the use of optimization methods to improve the circuit's performance through the sensitivity analysis.

Definition 1 : Sensitivity represents the effect of a change in the element x to the resulting change in the circuit's performance parameters T .

The following equation defines the differential sensitivity of parameter T_j with respect to component x_i

$$S_{x_i}^{T_j} = \frac{x_i}{T_j} \frac{\partial T_j}{\partial x_i} = \left. \frac{\frac{\Delta T_j}{T_j}}{\frac{\Delta x_i}{x_i}} \right|_{\Delta x_i \rightarrow 0}$$

$\frac{\Delta T}{T}$: relative deviation of parameter T., $\frac{\Delta x_i}{x_i}$: relative deviation of component x_i .

$S_{x_i}^T$: differential sensitivity of parameter T with respect to component x_i .

The sensitivity gives an information about faults observability. In the next subsection we will show how the notion of observability is related to sensitivity.

Observability

It is important to notice that a parameter who reacts poorly to component deviation makes it impossible to observe a defect in this component. Let us now discuss this observation at length. The notion of observability can be introduced by the following definition:

Definition 2: The defect observability of a component x_i is defined as the sensitivity of the output parameter T_j with respect to the variations of component x_i .

As the absolute value of the sensitivity of an output parameter's variation with respect to a component's variation is high, the observability of a defect in a circuit is also high. In this case, we can see that the sensitivity gives information about component deviation observability. Our proposed approach analyzes the various symptoms that can be produced by a fault during the design and test phases. To increase the observability of a defective

component in the circuit, we have to test a parameter that has a high sensitivity (high value of sensitivity means its absolute value is high) with respect to this component.

3. An approach

A multifrequency technique is proposed to analyze RF circuits in order to help improve their design and testability. The objective is to determine the relationship between the output parameters and the circuit components. This relationship is well modeled by the sensitivity elements. As mentioned before, the output parameters for microwave systems are better represented by S parameters. Firstly, we determine the critical components influencing the performances of a design and the best topology and layout that can be used to improve the global performances of a design. In this step, we determine the correlation between the different components in a circuit and their conjoint influence on the output. In a second step, we address our analysis to help the test engineers to determine the adequate interval of frequency useful for testing and we show if a modification in the design structure ameliorate the observability of defects. This analysis addresses also how defects in passive elements (including mismatch between lines) are isolated from those in active elements (due to intrinsic and extrinsic parameters of transistors). We summarize the different analysis steps as follows:

A- Design analysis step:

1. Determine the critical parameters influencing the circuit performances.
2. Analysis of correlation between elements.

3. Choose the adequate topology and layout to keep the circuit insensitive to elements variation.

B- Test step:

1. Analyzing the circuit outside its interval of operation (the circuit is unstable and tested as an oscillator) in order to increase defects observability.
2. Analyzing the circuit with some structure modification (open circuit and short circuit of the feedback elements) and examining their influence on defects observability.
3. Analyzing the circuit inside its interval of operation and compare these results with those obtained in 1 and 2.
4. Isolating defects caused by passive elements and those caused by active elements.
5. Choosing the best test frequencies and the adequate S parameters to observe the different defects in a circuit.
6. Test frequencies compaction and test vector generation.

4. Simulation results

The circuit to be analyzed is an amplifier designed to work in the band of 1.7GHz-2.25GHz (see Figure 2.1). The amplifier is optimized and the value of the components are obtained using MDS (Microwave Design System) CAD tool. The circuit is simulated and the sensitivity in frequency domain of the magnitude and the phase of the S parameters in respect to the different elements are computed using MDS tool. The sensitivity is plotted in frequency domain and the frequencies where the sensitivity of each element reaches its

maximum is extracted. Table 1 gives the set of frequencies where the sensitivity of the phase and the magnitude of the S parameters are at their maximum. L and W represent the line length and width respectively of the transmission lines. From this table we can see that variations in passive components are better observable with S11 and S22 parameters. We observe that the magnitude of S11 and S22 are more sensitive than the phase of these parameters. On the other hand, parameter S21 is less sensitive to a variation in passive components. Table 2.2 gives the sensitivity of the S parameters in respect to the transistor internal elements (intrinsic and extrinsic). The model of the transistor used during this simulation is given in Figure 2.2. Now we analyze the results from the design point of view.

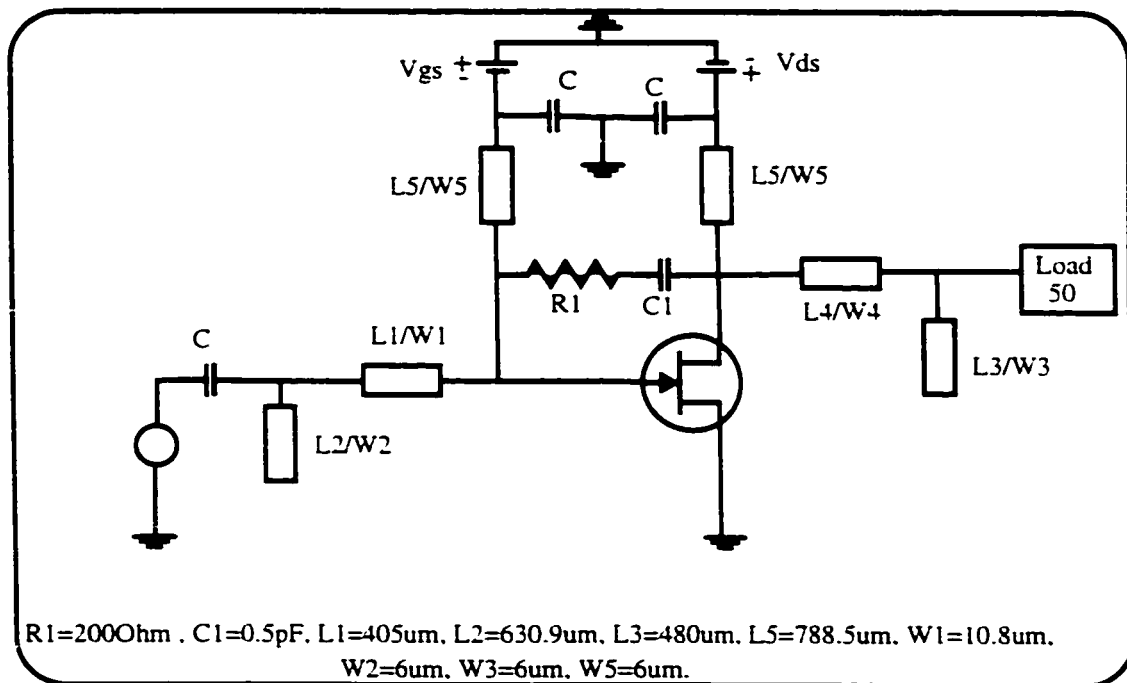


Figure 2.1 Amplification circuit

4.1 Design consideration

From the obtained sensitivity curves and tables different remarks can be done. It is clear that the problem of adaptation is caused by passive components: lines 1 through 5 and the feedback components $R1$ and $C1$. We can see that parameters $S11$ and $S22$ (which gives an indication about adaptation matching) are more sensitive to line lengths than widths. This is important to choose the layout topology that will be more precise in drawing the line length. We can also see that some elements such as $L1$ and $L2$ have opposite variations of sensitivity (when the sensitivity of one becomes positive the other one becomes negative). Figure 2.3 and Figure 2.4 give the sensitivity of the magnitude and the phase of $S11$ in respect to length $L1$ and $L2$. This is very helpful in design step to indicates that these components doesn't matter if they deviate from their nominal value but it must deviate in the same direction (both of them have positive or negative deviations). As a result, the composite effect of these two elements are eliminated or minimized due to their opposite sensitivity variation. This is gives a robust design if we choose the same materiel and technology (having the same process variation and temperature coefficients) to fabricate these elements. Other elements such as $L2$ and $L3$ have the same direction of sensitivity variation (see Figure 2.4 and Figure 2.5). In this case the designer has to choose two different kind of materials (having opposite process variation and temperature coefficients) in order to eliminate their composite effect at the output. We can also see that the sensitivity of the lengths $L1$, $L4$ and $L5$ have an opposite sign from the sensitivities of their widths respectively. But the sensitivity of the lengths are higher that those of the widths This

means that the global effect of a variation in length and width at the same direction is reduced but can not be totally eliminated due to the difference in sensitivity values.

Table 2 gives the sensitivity of the S parameters in respect to the internal transistor elements. As mentioned before, the equivalent model of the transistor used in this simulation is given in Figure 2.2. From these results we can see that S21 parameter has a low sensitivity (sensitivity=0.136) in respect to the gm parameter. This is achieved by using the feedback circuitry which reduces the influence of the gm parameter on the gain (S21) of the amplifier. Figure 2.6 gives the sensitivity of S21 (magnitude and phase) in respect to gm element. On the other hand the parameter gm influences the S11 and S22 parameters (see Table 2.2). In order to minimize the influence of the gm parameter variation on S11 and S22 of our design we have to choose a DC polarization giving a gm value that minimizes the value of S11 and S22. The minimum value of gm for a desired value of S21 is [8]:

$$gm(min) = \frac{1 - S_{21}}{Z_c + Z_0}$$

where Zc is the feedback impedance, Z0 is the characteristic impedance of the transmission line.

The intrinsic elements influencing the circuit performances are the drain conductance Gd and the drain gate capacitance Cdg. An important consideration in negative feedback design is the phase of S21 because our objective is to keep the phase of S21 close to 180°. By looking at Table 2.2, the intrinsic element Cdg and the extrinsic element Rs influence

on S_{21} phase variation around the frequency of about 2.066GHz. Figure 2.7 gives the sensitivity of the phase of S_{21} in respect to R_s element. The sensitivity values of the extrinsic elements (due to parasitic contacts of the transistor ports) L_g , R_g , L_s , R_d and L_d are small which indicated that their influence on the circuit performances is also small. After the design consideration, now we analyze the results from the test point of view.

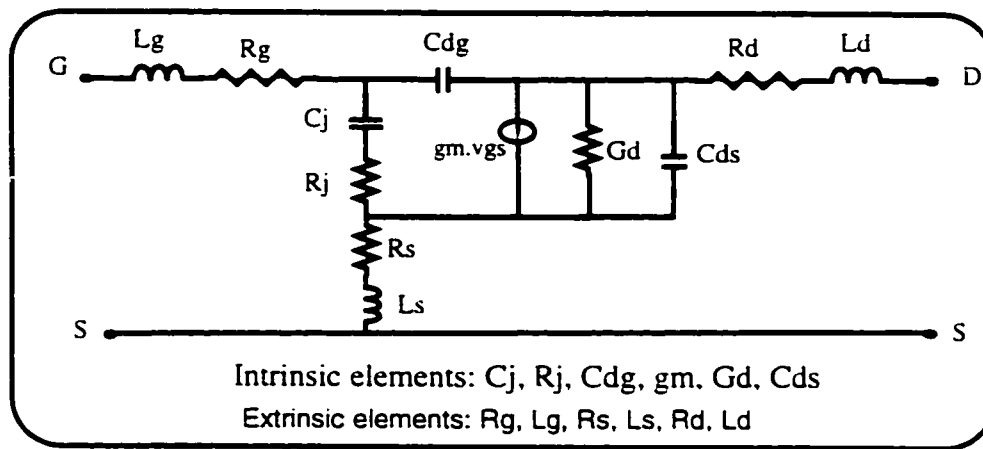


Figure 2.2 Transistor model

4.2 Test consideration

The objective during testability analysis is to choose the frequencies that give a high observability of defects in components and of process parameters variation. These frequencies are extracted where sensitivity is at its maximum. To test our amplification circuit different configurations are investigated in order to choose the best situation that helps improve defects observability. These configurations are summarized as follows:

Configuration 1: the amplifier is analyzed in a wide range of frequency 0.1GHz-15GHz

(the amplifier is designed to operate in the band of 1.7GHz-2.25GHz).

Configuration 2: The amplifier is analyzed by opening its feedback in the band [1.7GHz-2.25GHz].

Configuration 3: The amplifier is analyzed by short-circuiting its feedback in the band [1.7GHz-2.25GHz].

Configuration 4: The amplifier with the correct feedback circuitry and is analyzed in its band of operation [1.7GHz-2.25GHz].

In configuration 1, we want to investigate if the testability of the circuit is ameliorated outside its band of operation. Table 2.3 summarizes the results obtained when configuration 1 is used and shows the adequate S parameters to be measured, the maximum value of the sensitivity and the best frequency to observe a defect in a given component. We can see that these results do not have a practical meaning because the values of sensitivities are very high and can reach 868 in magnitude (see sensitivity of S11 in respect to L1). Consequently, if we want to test this circuit in a large band of frequency (outside the band of operation), the S parameters deviates considerably from their nominal value either when a very small (acceptable) deviation in components exists due to the very high value of sensitivities. For instance, if the length L1 deviates only of about 0.5% from its nominal value, the magnitude of S11 parameter deviates of about 434% which is not

realistic. In our opinion this situation occurred because the amplifier is unstable outside its band of operation. As a result, this configuration is not adequate for testing the circuit.

In configuration 2, we want to modify the structure of our design to increase the observability of defects. In this case, the feedback circuitry composed by R1 and C1 is opened and the amplifier is analyzed in its band of operation (1.7GHz-2.25GHz). Table 2.4 summarizes the selected S parameters to test each components and their best test frequencies. From this table we can see that the value of sensitivities are very low and are not adequate to observe defective components. As a result, this configuration does not ameliorate the testability of our circuit.

In configuration 3, the feedback circuitry is short-circuited and the amplifier is analyzed in its band of operation. Table 2.5 summarizes the results obtained using this configuration. We can see from this table that the sensitivity values are very low (except for the phase of S11) and are not adequate to observe defects in the different components. On the other hand, the sensitivity of the phase of S11 is very high and is not useful to observe defects in theses components because even when a negligible deviation in components exists, this gives a very large deviation in the phase of S11 parameter.

In configuration 4 which corresponds to that used during the normal operation (1.7GHz-2.25GHz) when the amplifier is connected with its feedback circuitry. Table 2.6 gives the highest values of sensitivities (sensitivity of the magnitude and phase of S parameters in respect to the different components) and their corresponding frequencies. These results are more realistic compared to those obtained from the last three configurations. From this

table, we can see that parameters S_{11} and S_{22} allow to observe defects in the passive components R_1 , C_1 and the length and width of the different transmission lines. We can also see that a variation in line length is easily observable than line width. This is justified by the fact that the impedances of lines are more sensitive to line length than line width. On the other hand, parameter S_{21} is less sensitive to passive components variations and is not used to observe defects in these components. From Table 2.1, we can see that defects on most of the passive components are observable by the magnitude of S_{11} and can share the same frequencies to observe them. The six frequencies selected for testing passive components are $f_{\text{GHZ}}=[2.0432, 2.1013, 2.1117, 2.1453, 2.1520, 2.1667]$. These frequencies can be compacted and reduced to only three frequencies $f_{\text{GHZ}}=[2.0432, 2.1013, 2.1453]$ without loss in fault coverage. The compaction is done by eliminating redundancy. Now, we select the frequencies for testing the transistor internal elements.

Testing the active device (transistor)

In integrated circuits different aspects influence the transistor characteristics. The fabrication process can determine the parasitic elements and the electrical parameters in a transistor. During our analysis the sensitivity of the S parameters to the transistor internal elements are computed. Table 2.2 gives the highest values of sensitivity and the corresponding test frequencies. Some conclusions can be extracted from our simulation and by looking to the transistor model of Figure 2.1.

If we look to the sensitivity of parameter S_{11} in respect to the intrinsic and extrinsic transistor elements, this parameter is mainly sensitive to R_s , C_{dg} , g_{m0} and G_d . The S_{11}

parameter gives an information about a mismatch that results at the input between the passive components and the transistor it self due to a variation in source contact resistance (R_s), gate-drain junction capacitance (C_{dg}), the drain conductance G_d and a variation on g_m . variations in the remaining elements L_g , R_g , R_j , C_j , L_s , C_d , L_d and C_{ds} are poorly observed at the output. From Table 2.2, the test frequencies for these elements and by measuring S_{11} parameter are: $f_{GHz}=[1.7611, 2.1888]$. The S_{22} parameter gives the same information as S_{11} parameter because the output effect is reflected to the input due to the feedback circuitry. The S_{21} parameter has a low values of sensitivity and does not allow observation of defects in transistor elements. This is due to the feedback circuitry which reduces the influence of the internal transistor elements on the amplifier gain (or S_{21}). The test vector used for the passive and the active elements in the amplifier is composed by 5 frequencies and needs only one parameter to be measured (magnitude of S_{11} parameter). These frequencies are $f_{GHz}=[1.7611, 2.0432, 2.1013, 2.1453, 2.1888]$.

5. Conclusion

Design and test consideration of RF systems is studied. The frequency domain analysis of RF systems is performed. This analysis helps improve the design performances and facilitates the test of RF circuits. During this analysis we determined the critical components influencing the circuit performances and the best topology that can be used to improve the global performances of a design. Correlation between components and their conjoint influence on the circuit were studied to minimize the composite effect of these components on the output. A study of the influence of the intrinsic elements of a transistor

was performed and distinguished from those caused by passive components. During test consideration, the circuit under test was analyzed in different configurations in order to choose the best situation that help improve defects observability. The test frequencies were extracted to observe defects in both passive and active components.

Table 2.1 Test frequencies for the passive components of the amplifier of Figure 2.1: the amplifier is analyzed in the band 1.7GHz-2.25GHz

Element	S11 max Sens & frequency (GHz)	θ S11 max Sens & frequency (GHz)	S22 max Sens & frequency (GHz)	θ S22 max Sens & frequency (GHz)	S21 max Sens & frequency (GHz)	θ S21 max Sens & frequency (GHz)
L1	-17.67 f=2.0432	-15.93 f=2.1453	10.11 f=2.0432	3.74 f=1.9548	0.191 f=2.25	-2.082 f=2.0432
L2	-12.78 f=2.1453	4.056 f=2.1264	2.1817 f=1.9548	1.7578 f=2.0432	-0.069 f=1.7	-0.919 f=2.25
L3	-2.151 f=2.1667	1.884 f=2.1453	2.081 f=1.9548	1.4785 f=2.005	-0.039 f=2.25	-1.4216 f=2.25
L4	10.36 f=2.1453	-3.8564 f=2.1264	-10.95 f=2.0432	-6.041 f=2.0432	-0.097 f=2.25	-1.4216 f=2.25
L5	13.9 f=2.1453	6.1596 f=6.1596	7.571 f=2.0432	3.6267 f=1.9548	-0.003 f=1.7	-1.3992 f=2.25
W1	5.6 f=2.1013	5.1 f=2.1453	-3.56 f=2.0432	-1.155 f=1.8482	0.028 f=2.25	0.452 f=2.25
W2	-2.0737 f=2.1453	0.736 f=2.1264	0.393 f=1.9548	0.317 f=2.0432	-0.015 f=1.7	-0.104 f=2.25
W3	-0.765 f=2.1667	0.585 f=2.1360	-1 f=2.0432	0.549 f=2.005	0.012 f=2.25	-0.057 f=2.25
W4	-2.7099 f=2.1453	0.872 f=2.1184	2.9334 f=1.9548	1.4622 f=2.0432	0.022 f=2.25	0.262 f=2.25
W5	-1.3669 f=2.1520	0.749 f=2.1264	-0.808 f=2.0432	0.464 f=2.005	-0.018 f=1.7	0.136 f=2.25
R1	-13.42 f=2.152	6.607 f=2.1264	-8.8213 f=2.0432	-3.382 f=1.9548	0.3127 f=2.25	1.21 f=2.25
C1	11.529 f=2.1178	-5.3982 f=2.1667	-6.8015 f=1.9548	-2.5308 f=2.0432	-0.527 f=1.7819	0.337 f=2.25

Table 2.2 Test frequencies for the transistor internal elements of the amplifier in Figure 2.1:

the amplifier is analyzed in the band 1.7GHz-2.25GHz

Element	IS11 max Sens & frequency (GHz)	IS11 max Sens & frequency (GHz)	IS22 max Sens & frequency (GHz)	IS22 max Sens & frequency (GHz)	IS21 max Sens & frequency (GHz)	IS21 max Sens & frequency (GHz)
Rj	0.015 f=1.822	0.02 f=1.7611	0.02 f=2.105	0.005 f=1.944	146x10-6 f=2.25	0.032 f=2.066
Cj	0.229 f=1.822	0.317 f=1.7611	0.299 f=2.005	0.073 f=1.944	0.002 f=2.25	0.471 f=2.066
Cdg	1 f=2.188	1.23 f=1.7161	1.188 f=2.005	0.286 f=1.944	0.011 f=2.25	1.6128 f=2.0666
gm0	5.06 f=1.761	1.4775 f=2.25	1.758 f=1.944	1.4955 f=2.005	0.136 f=2.25	0.024 f=2.25
Gd	4.75 f=1.7611	1.4 f=2.25	1.902 f=1.444	1.6482 f=2.005	0.13 f=2.25	0.076 f=2.0666
Cds	0.035 f=1.822	0.047 f=1.7611	0.112 f=2.005	0.026 f=1.944	0.201 f=1.7	0.0778 f=2.0666
Lg	0.004 f=1.7611	0.002 f=2.25	0.002 f=1.944	0.001 f=2.005	184x10 ⁻⁹ f=2.25	505x10-6 f=2.066
Rg	0.092 f=1.822	0.119 f=1.761	0.138 f=2.005	0.034 f=1.944	0.19 f=2.066	846x10-6 f=2.25
Rs	22.6 f=1.7611	6.072 f=2.1888	17 f=2.005	12.033 f=2.005	0.522 f=1.944	6.9 f=2.0666
Ls	0.108 f=1.822	0.134 f=1.7611	0.059 f=2.005	0.244 f=2.005	0.002 f=2.25	0.198 f=2.0666
Rd	0.685 f=1.7611	0.22 f=1.7611	0.882 f=2.005	0.362 f=1.944	0.016 f=2.006	6.58 f=2.0666
Ld	0.016 f=2.188	0.02 f=1.7611	0.028 f=1.944	0.0142 f=2.005	0.228 f=1.7	0.031 f=2.0666

Table 2.3 Test frequencies when the amplifier is tested outside its band of operation

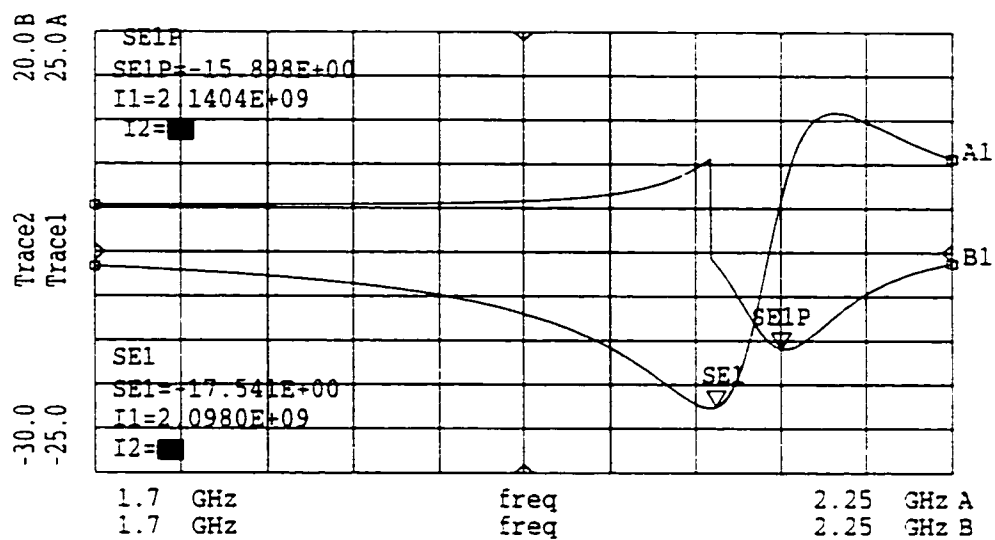
Element	IS11 max Sens & frequency (GHz)	IS11 max Sens & frequency (GHz)	IS22 max Sens & frequency (GHz)	IS22 max Sens & frequency (GHz)	IS21 max Sens & frequency (GHz)	IS21 max Sens & frequency (GHz)
L1	-868.57 f=10.881					
L2						-321.8 f=2.5708
L3					757.78 f=3.0201	
L4					365.67 f=3.0201	
L5		-876.46 f=10.881				
W1						76 f=2.5708
W2	29.478 f=2.5708					
W3				109.24 f=3.0201		
W4				-70.784 f=3.0201		
W5		-35.612 f=0.9236		-35.612 f=0.9236		
R1						164.01 f=2.5708
C1						100 f=2.5708

**Table 2.4 Test frequencies when the amplifier is tested with opening its feedback circuitry
(configuration 2)**

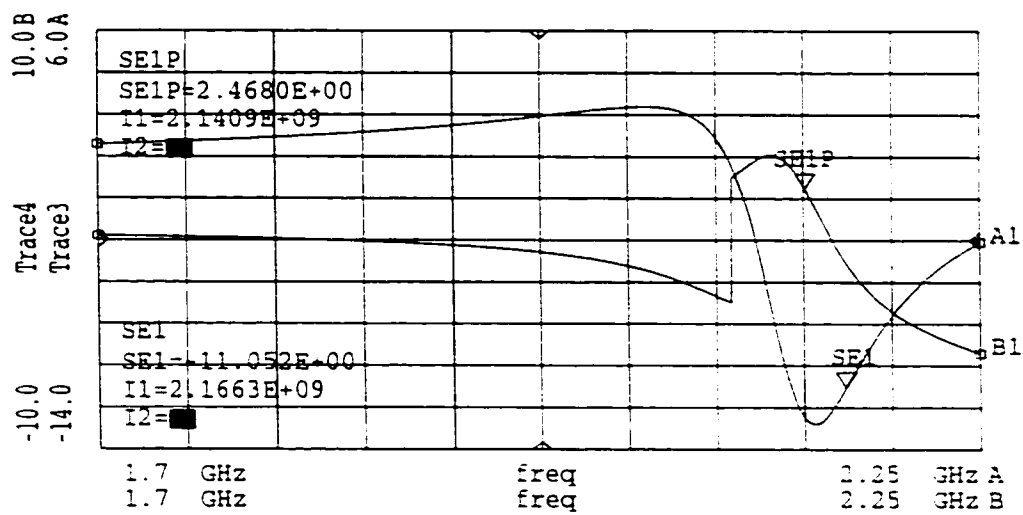
Element	IS11 max Sens & frequency (GHz)	θS11 max Sens & frequency (GHz)	IS22 max Sens & frequency (GHz)	θS22 max Sens & frequency (GHz)	IS21 max Sens & frequency (GHz)	θS21 max Sens & frequency (GHz)
L1	0.11 f=2.25	-0.527 f=2.25	0.256 f=2.25	0.216 f=2.25	0.758 f=2.25	-0.223 f=2.25
L2	-0.082 f=2.25	0.860 f=2.25	0.045 f=2.25	-0.161 f=2.25	-0.566 f=2.25	-0.262 f=1.7
L3	-0.021 f=2.25	-0.031 f=2.25	0.118 f=2.25	1.42 f=1.7	-0.173 f=2.25	-0.214 f=2.25
L4	0.144 f=2.25	0.036 f=2.25	-0.1 f=2.25	-0.169 f=2.25	0.064 f=2.25	-1.061 f=2.25
L5	0.064 f=2.25	1.061 f=2.25	-0.223 f=2.25	1.95 f=1.7	0.064 f=2.25	1.061 f=1.7
W1	-0.025 f=2.25	0.136 f=2.25	-0.063 f=2.25	-0.8 f=2.25	-0.176 f=2.25	-0.033 f=2.044
W2	-0.012 f=2.25	0.160 f=1.7	0.005 f=2.25	-0.024 f=2.25	-0.086 f=2.25	-0.033 f=2.25
W3	-0.008 f=2.25	0.003 f=1.7	0.033 f=2.25	0.379 f=1.7	0.048 f=2.25	-0.033 f=2.25
W4	-0.037 f=2.25	0.507 f=2.25	-0.014 f=2.25	0.134 f=1.7	0.2121 f=1.7	0.005 f=2.25
W5	-0.008 f=1.7	-0.141 f=1.7	-0.021 f=1.7	-0.258 f=1.7	-0.089 f=1.7	0.044 f=1.7

Table 2.5 Test frequencies when the feedback circuitry is short-circuited (condition 3)

Element	$ S_{11} $ max Sens & frequency (GHz)	θS_{11} max Sens & frequency (GHz)	$ S_{22} $ max Sens & frequency (GHz)	θS_{22} max Sens & frequency (GHz)	$ S_{21} $ max Sens & frequency (GHz)	θS_{21} max Sens & frequency (GHz)
L1	0.406 $f=1.8662$	22.17×10^3 $f=2.209$	-0.12 $f=2.25$	-0.0742 $f=1.7$	-0.665 $f=2.25$	0.404 $f=1.7$
L2	-0.077 $f=1.7$	-39.25×10^3 $f=2.209$	0.0484 $f=2.119$	-0.063 $f=2.25$	0.091 $f=1.7$	0.4 $f=2.25$
L3	0.026 $f=2.25$	1.3212 $f=2.209$	-0.126 $f=1.949$	-1.5297 $f=2.25$	0.097 $f=2.029$	0.17 $f=2.25$
L4	-0.053 $f=2.25$	-979.8 $f=2.209$	0.566 $f=2.25$	1.99 $f=2.25$	-0.459 $f=2.25$	0.307 $f=1.7$
L5	-0.064 $f=1.7$	1.03×10^3 $f=2.209$	-0.115 $f=1.7$	0.143 $f=2.25$	0.075 $f=1.7$	0.132 $f=1.7$
W1	0.144 $f=1.869$	4.461 $f=2.206$	0.034 $f=2.25$	0.03 $f=1.864$	0.224 $f=2.25$	-0.09 $f=1.7$
W2	-0.018 $f=1.7$	-5.35×10^3 $f=2.209$	0.09 $f=1.877$	-0.008 $f=2.25$	-0.022 $f=1.25$	0.051 $f=2.25$
W3	0.08 $f=2.12$	18.87 $f=2.209$	-0.048 $f=1.8134$	-0.3 $f=2.25$	0.035 $f=2.029$	0.031 $f=2.25$
W4	0.011 $f=2.25$	273.54 $f=2.209$	-0.142 $f=2.25$	0.391 $f=2.25$	0.118 $f=2.25$	-0.068 $f=1.7$
W5	0.004 $f=1.7$	216.4 $f=2.209$	-0.006 $f=2.25$	0.036 $f=2.25$	0.015 $f=2.25$	-0.03 $f=1.7$

Figure 2.3 Sensitivity of S_{11} in respect to $L1$

SE1: Sensitivity of magnitude, SE1P: Sensitivity of phase

Figure 2.4 Sensitivity of S_{11} in respect to $L2$

SE1: Sensitivity of magnitude, SE1P: Sensitivity of phase

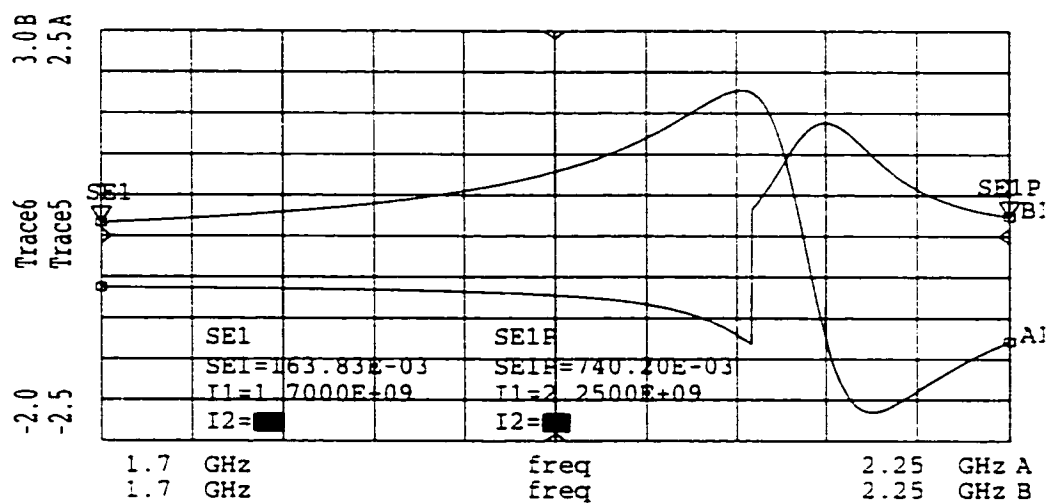


Figure 2.5 Sensitivity of S11 in respect to L3

SE1: Sensitivity of magnitude , SE1P: Sensitivity of phase

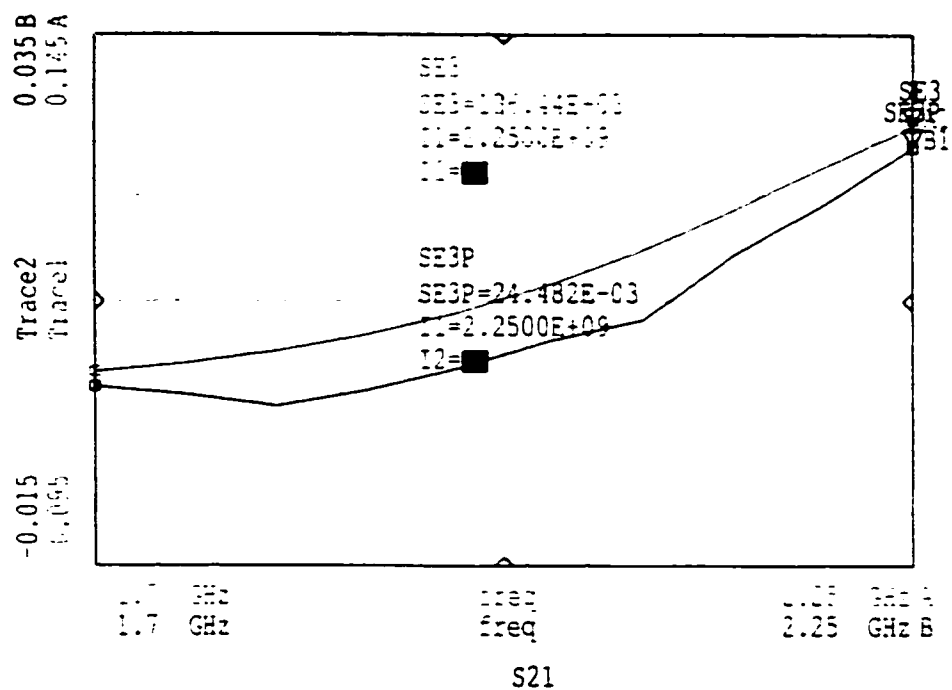


Figure 2.6 Sensitivity of S21 in respect to gm

SE3: Sensitivity of magnitude , SE3P: Sensitivity of phase

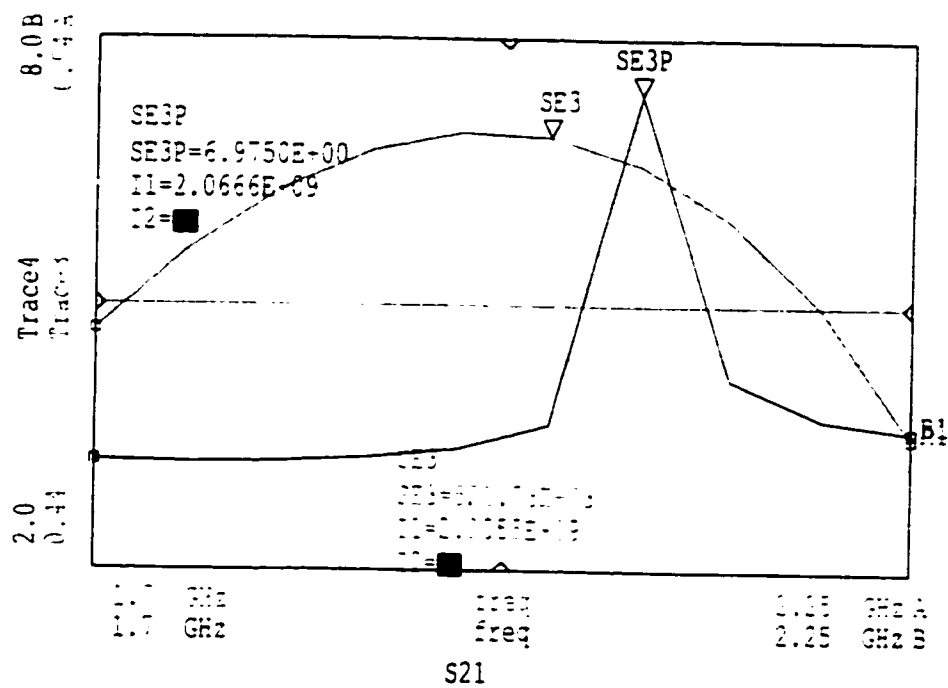


Figure 2.7 Sensitivity of S21 in respect to Rs

SE3: Sensitivity of magnitude , SE3p: Sensitivity of phase

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CHAPITRE 3

ANALYSE ET AMELIORATION DE LA TESTABILITE DES CIRCUITS INTEGRES HAUTES FREQUENCES FONCTIONNANT EN MODE NON LINEAIRE

3.1 Résumé

Dans le chapitre précédent nous avons présenté une méthodologie qui permet de procéder à la détection et à la localisation des défauts dans les circuits intégrés hautes fréquences. Cette méthodologie basée sur l'utilisation des paramètres S n'est applicable qu'aux circuits hautes fréquences linéaires.

Ainsi, dans ce présent chapitre nous exposerons une méthodologie adaptée aux circuits non linéaires. Un circuit est dit non linéaire lorsque le signal de sortie contient des fréquences additionnelles. Celles-ci sont issues de la génération d'harmoniques et de produits d'intermodulation [79][93]. Le circuit considéré durant notre analyse est un amplificateur de puissance hautes fréquences. Comme nous l'avons mentionné auparavant la localisation d'un défaut et l'explication de son origine aideront à réduire le temps alloué au test et par conséquent le coût de production des circuits intégrés hautes fréquences.

La méthode ici proposée combine l'analyse de sensibilité à l'analyse de la puissance. Le choix de la puissance à la place des paramètres S s'explique par le fait que les paramètres $[S]$ perdent de leur efficacité une fois que le circuit commence à fonctionner dans une zone non linéaire. Différents phénomènes doivent alors être pris en compte (niveaux de puissance, intermodulations, distorsions d'harmoniques etc...). Ces phénomènes dépendent beaucoup plus du niveau de puissance que des fréquences utilisées. On comprend donc aisément le pourquoi de la caractérisation en puissance pour les circuits non linéaires. Nous avons procédé à la segmentation de la courbe AM/AM (fonction de transfert en puissance) en trois différentes zones permettant d'observer le comportement des paramètres de sortie assignés à chaque segment. La segmentation de cette courbe AM/AM suit exactement les trois modes (linéaire, compression et nonlinéaire) de fonctionnement d'un amplificateur de puissance utilisé dans notre cas. Les paramètres de sortie seront observés dans les différents segments de la courbe AM/AM afin de pouvoir déterminer les points sensibles du circuit. On est ainsi à mesure de savoir dans quel segment et avec quel niveau de puissance un défaut sur un composant donné est observable. Contrairement à la méthodologie proposée pour les circuits linéaires où les vecteurs de test sont des fréquences, les vecteurs de test issus de cette analyse sont des niveaux de puissance.

L'article présenté dans ce chapitre est intitulé "Fault Detection in Nonlinear High Frequency Circuit Performing an In-Segment Power level Analysis" a été soumis pour publication dans *International journal on Wireless information and networks* de Kluwer Academic Publishers.

3.2 Fault Detection in Nonlinear high frequency circuit Performing an Segment Power level Analysis

Fault Detection in Nonlinear high frequency circuit Performing an In-Segment Power level Analysis

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Abstract

The rapid growth of wireless communication has led to an increasing demand for reliable and high performance RF products. One way of achieving high reliability and performances is having an efficient test procedure. Considering the complexity of analog testing and the high frequency constraints, testing RF circuits introduces a new challenge to the test community. In this paper, a test strategy for nonlinear RF circuits (power amplifier) is presented. This test strategy is based on analyzing the circuit output response to different levels of input power. The output response is divided into three segments representing the linear, transition and nonlinear behavior of the circuit. Each segment is analyzed to decide if it could be a test area. This test strategy helps to perform a quick and efficient test as well as to limit the number of test vectors and to predict which elements can be isolated from a given segment.

1. Introduction

In integrated circuits, testability features become essential during the design and operational phases of systems. The increasing complexity of analog integrated circuits demands new methodologies for both design and test. One of the highly desirable analog systems requirements is integrating design and test. Up to now the test of analog circuits is still hand created by designers by using simulation and manual adjustment which is time consuming, this task become more difficult as frequency increases.

Most published testability analysis methods for analog circuits targeted medium and low frequency circuits. In the past few years some approaches were proposed [1][2], in which test vector selection that allows maximization of the deviation between the output voltage of the good and faulty circuits is discussed. Fault equivalence study in mixed signal circuits using a probabilistic computational technique is proposed in [3]. Concepts such as fault masking, fault dominance, fault equivalence, fault isolation defined to determine the relationship between faults and their effects at the output are presented in [4]. Test nodes and test frequencies selection was performed for every category of faults (single, double, multiple). Testability analysis of analog circuits in the presence of soft, large-deviation, and hard faults is given in [5], a set of test vectors is generated to observe and cover these faults. Some techniques for wireless communication systems have been recently proposed. In [6], a Built-In-Self scheme to extract parameters such as signal to noise ratio, frequency response, intermodulation distortion for the receiver and transmitter section of an RF codec is presented using digital signal processing techniques. In [7], a test architecture which

combines Boundary scan and a digital signal processing based functional testing of RF circuits is proposed to achieve system self-test. Recently studies related to the characterization of RF amplifier in a test point of view have been presented [8-11]. But most of these papers deals with the use of digital modulated signal to evaluate the linearity of the RF amplifiers[8][9][10].

Some of the approaches presented above are destined for low and medium frequency systems analysis. The others which use some DSP (Digital Signal Processing) techniques are only useful for systems containing the basic components to perform this type of processing. Up to now few publications concerning RF circuits in testability point of view have been presented. Test procedures used with RF circuits are strictly functional based testing. This type of testing doesn't give deep informations on structural faults, since only the circuits output parameters specifications have to be met. This lack of approaches can be explained by the fact that RF circuits are orders of magnitude more complex than low frequency circuits. While working in Radio-Frequencies some aspects like high frequency coupling that are insignificant in low and medium frequencies have to be taken into account. Proper modeling of RF operating devices is then necessary.

In a previous paper [11], we presented a frequency domain analysis of RF systems. This type of analysis is destined to ameliorate the design performance and to facilitate the test of RF circuits. The proposed testability analysis methodology in [11] helps improve the manufacturability of RF designs in the presence of high frequency constraints. Firstly, we determine the critical components influencing the performances of a design and the best

topology and layout that can be used to improve the global performances. In this step, we determine the correlation between the different components in a circuit and their conjoint influence on the output. In a second step, we address our analysis to help the test engineers to determine the adequate interval of frequency useful for testing and we show if a modification in the design structure ameliorate the observability of defects. This analysis address also how defects in passive elements (including mismatch between lines) are isolated from those in active elements (due to intrinsic and extrinsic parameters of transistors).

The proposed methodology in [11] is based on the behavior of the S parameters of a given circuit. This limits its applicability to only linear RF circuits. In reality all electronics circuits presents a certain degree of nonlinearities [12]. The linear assumption that underlies most modern circuit theory is in practice only an approximation. Some circuits, such as small-signal amplifiers, are only very weakly nonlinear, however, and are used in systems as if they were linear. Although linear theory has some use in the design of nonlinear circuits like power amplifiers, it is by itself usually inadequate for determining all properties of some class of circuits that we need to know. It is therefore necessary to take into account nonlinearities that are introduced in the output signal. One can understand then the necessity of having a specific test strategy for nonlinear circuits like power amplifiers, which become very popular in the last years because of their application to wireless and cellular telephones.

In this paper, we propose a methodology for testing RF power amplifier with efficiency and with a limited number of test vectors. The proposed methodology is based on power analysis. We are not interested in diagnosis evaluation of power amplifiers that determine the deviation of every component on the circuit. Our methodology researches the adequate area, and characteristic for which a given fault is better observable. It is destined to improve the design performance and to facilitate the test of high frequency circuits. It also helps improve the manufacturability of designs in the presence of high frequency constraints. The design engineers can easily determine parameters influencing the design performances. On the other hand, this analysis allows the test engineer to predict which components can be isolated by a given test set, and which kind of defects can be observed from an output parameter. Analyzing testability in dynamic domains is an interesting approach to choose adequate test power levels for increasing fault detection in nonlinear circuits. The case of single faults is treated in this paper. In the next section we will briefly present the power amplifier. In section 3 we will explain our approach. The simulation results and discussion will follow in section 4.

2. RF Power Amplifiers

The development of cellular telephone and wireless communication market introduces an increasing need for RF power amplifiers. Power amplifier is in general specified by its low power gain G or linear gain, its 1-dB gain compression point P_{1dB} , and the Third order intercept point called P_{I3} .

- The power gain G is defined as the ratio of the output power to the input power. The power amplifier's output increases linearly with the input power at low power.
- 1-dB gain compression point P_{1dB} : is defined as the output power at which the gain has dropped by 1 dB below the linear gain (see Figure 3.1). The nonlinear behavior in amplifiers introduces distortion in the amplified signal. Typically the gain will drop rapidly for powers above P_{1dB} as illustrated in Figure 3.1. From the 1-dB gain compression point P_{1dB} we can evaluate the highest power level that is possibly available at the output of the amplifier. Its measurement represents one simple method of determining the nonlinearity. There is a close relationship between the low power gain linearity and the 1-dB gain compression point; the more the amplifier is able to amplify large signals in a linear way, the higher the 1-dB gain compression point is.
- Third order intercept point P_{I3} : a source of distortion in power amplifiers is caused by intermodulation products. When two or more sinusoids f_1 and f_2 are applied to a nonlinear amplifier, the output contains additional frequency components called intermodulation products. The most significant intermodulation products are the third order harmonic h_3 which emerges in the case of two close frequencies at the input of the amplifier. In a two tones excitation case with close input frequencies f_1 and f_2 where $h_3 = 2f_1 - f_2$, the third order harmonic h_3 is very close to the fundamental frequencies and fall within amplifier's bandwidth, producing distortion at the output. The third order intercept point P_{I3} is then defined as the point where the

power of the fundamental linear extrapolation and the power of the third order harmonic h_3 intercept, as it is represented at Figure 3.1. The third order intercept point power is typically 10 to 12 dB above the P_{1dB} and is a very useful parameter for calculating low level intermodulation effects. Therefore, it can be used to find not only the intermodulation output power but the ratio of linear to intermodulation power level. The power P_{I3} is a theoretical level. However, it is a useful quantity to estimate the third-order intermodulation level at different power levels [13]. One straightforward way to estimate third-order intermodulation level is to measure the isolation $Isol(f/h_3)$ between the fundamental and the third order harmonic h_3 . $Isol(f/h_3)$ which is expressed in dBc represents the power level difference between the fundamental f_1 and the third order harmonic h_3 .

- Power Amplifier also presents another characteristic called AM-to-PM conversion which is defined as the change in output phase for a 1-dB increment of the input power. As mentioned our work is strictly limited to power analysis, then the behavior of the AM-to-PM will be ignored.

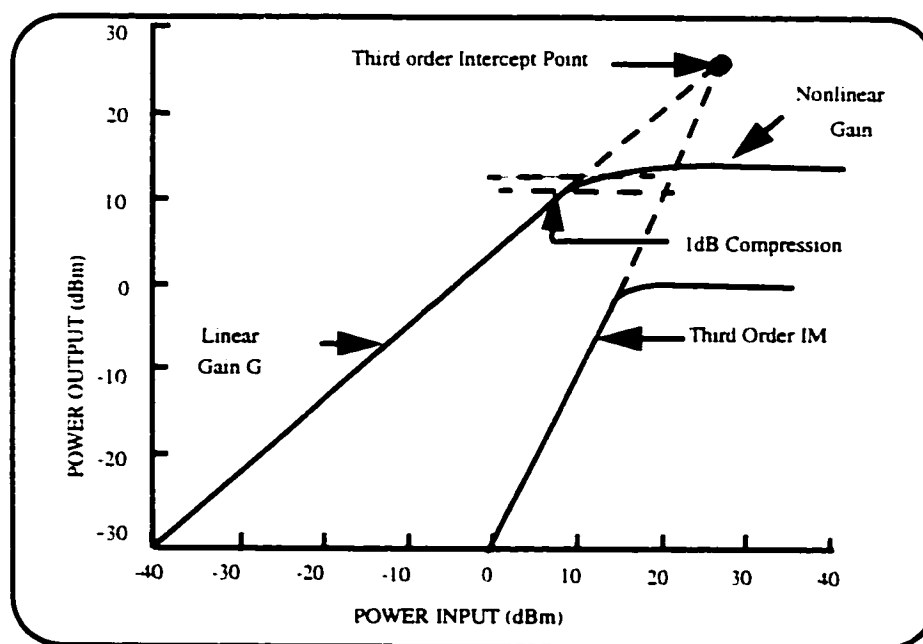


Figure 3.1 The variation of output power with input power for a nonlinear amplifier

3. Principle of the Approach

The approach that we propose in this paper is based on the segmentation of the power amplifier transfer function. Our objective is to choose the segment that increases the testability of the circuit in terms of searching for an effective way to observe defective components on the circuit. The test of a fault is easy if its effect can be observed at the output in a given segment. The analysis of the power transfer function makes us assume three basic segments for the power amplifier as illustrated in Figure 3.2: the linear segment, the compression or transition segment and the nonlinear segment. Specific parameters are chosen to help evaluating the observability of a given fault in each of these areas. Analysis

will be performed to observe the behavior of the parameters in function of the variation of the value of the components. The evaluation analysis is based on the deviation of a specific parameter from its nominal value regarding to the variation of the component's value. It is important to notice that a parameter who reacts poorly to component deviation makes it impossible to observe a defect in this component.

In the linear area the linear gain G will be observed. Since the output power increases linearly with the input power in this area, any variation of G when the value of a component is changing from its nominal value can be considered as default. The compression or transition zone is a very critical in power amplifier since it represents the area when the system start having nonlinear behavior. To characterize the amplifier in this area the variation of the P_{1dB} will be considered. Also a two tone excitation will be performed to analyze the isolation between the fundamental and the harmonics especially the third order harmonic h_3 which is the closest to the fundamental. The analysis in nonlinear zone will be quite similar to the compression zone. Two parameters are considered P_{6dB} and $Isol(f/h_3)$ at P_{6dB} . P_{6dB} is defined as the output power at which the gain has dropped 6dB below the linear gain between the fundamental and f_1 the third order harmonic h_3 which is a critical source of information about the strength of the harmonics in the amplifier bandwidth. The choice of P_{6dB} is arbitrary but it can be explained by the fact that at P_{6dB} the amplifier is really working in its nonlinear zone. These two parameters are considered because the amplifier is working in a strictly nonlinear area, the generation of harmonic is much higher

than in other areas, then the variation of the two parameters in function of the components variation is very interesting to know.

We can summarize our steps as follows:

1. Design and optimization of the performances of the power amplifier.
2. Assign specific parameters to each area of the transfer function.
3. Evaluation in each area of the variation of these parameters in function of component variations.
4. Analysis of the correlation between the component variations and the parameters variations.
5. Isolating defects caused by elements.
6. Choosing the best area and the best parameters to observe the different defects.

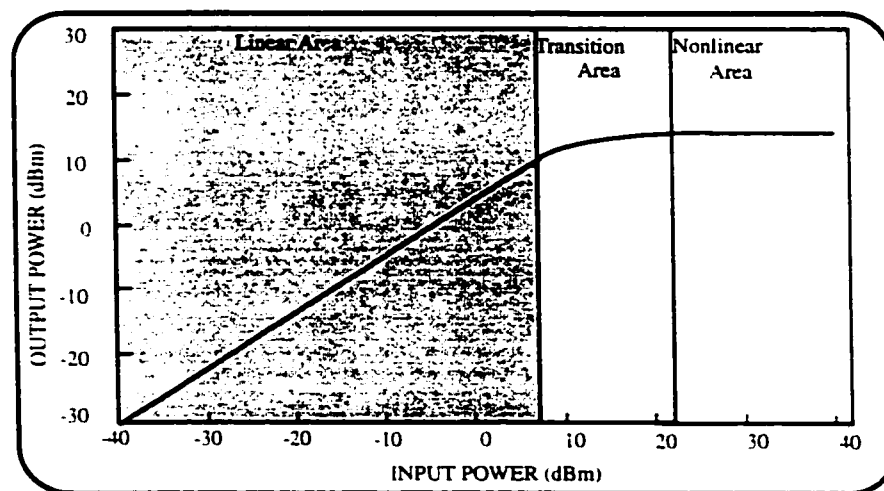


Figure 3.2 Segmentation of the power transfer function of a nonlinear amplifier into three testing areas

4. Simulation Results

The circuit to be analyzed is a class A power amplifier (see Figure 3.3) designed to work in the band of 1.6GHz-1.8GHz, with a central operation frequency of 1.7GHz. The power amplifier is optimized and the value of the components are obtained using MDS (Microwave & RF Design System) CAD tool. L and W represent the length and the width respectively of the transmission lines.

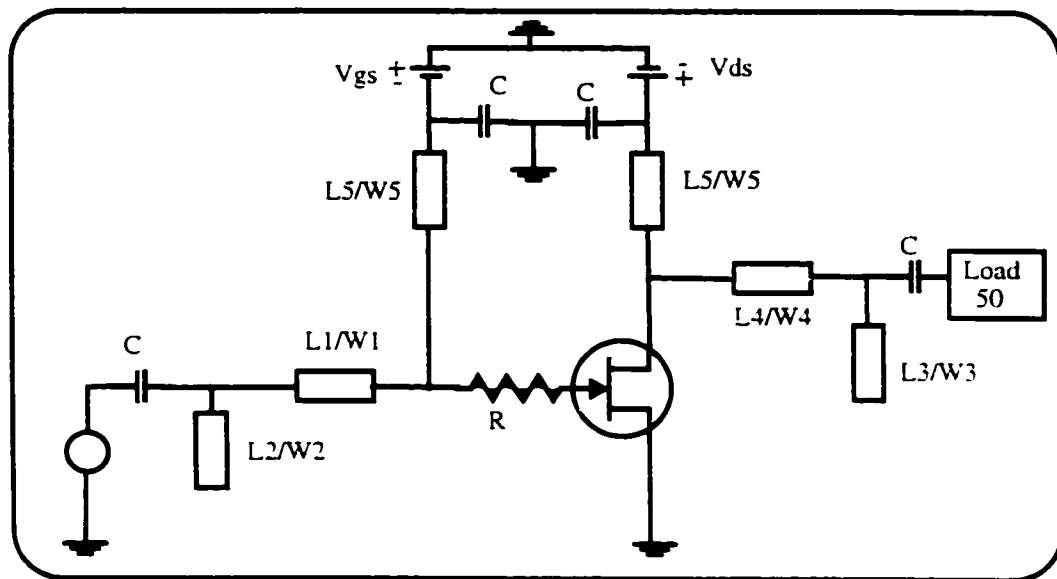


Figure 3.3 Power Amplification circuit

$R1=70\Omega$, $L1=298.9\text{mil}$, $L2=6.9\text{mil}$, $L3=1354\text{mil}$, $L4=454.83\text{mil}$, $L5=162.102\text{mil}$, $W1=7.6\text{mil}$,

$W2=253\text{mil}$, $W3=126.8\text{mil}$, $W4=83.6\text{mil}$, $W5=8.28\text{mil}$

The circuit is analyzed using Harmonic Balance which is one of the most important techniques for analyzing nonlinear circuits [12]. It is most useful for strongly or weakly nonlinear circuits that have single tone excitation. Figure 3.4 represents the power transfer function and different performances of the analyzed power amplifier, P_{in} and P_{out} which are expressed in dbm represent respectively the input and the output power of the circuits. Figure 3.5 and Figure 3.6 illustrate respectively the output spectrum of the power amplifier with two tones excitation at P_{3dB} and at P_{6dB} . f_1 and f_2 are the input frequencies and h_3 is the third order intermodulation product which we said before is very critical in the case of nonlinearities generation. Performances of the simulated power amplifier are also presented at Table 3.1. Analysis has been performed in the three areas. Variation of about 5% and 20% has been performed on components values. In Table 3.2 results of the analysis are presented. The first observation is that there is no common link between the different elements detected in the different areas. We observe from Table 3.2 that all components are covered, but in different areas and with different parameters. The test engineers then, in order to have an efficient test must use all the three testing areas. It is observed from this table that some component variations are more observable in some areas than others. R is more observable at the linear segment, but to test W1 we have to observe the value of the isolation between the fundamental and the third order harmonic in the nonlinear area. A component is considered observable if its variation from its nominal value provokes a variation of the value of the assigned output parameters in the segment it is observed. From the results we observed that the transmission lines' length influence more the output parameters than the width. This can be very important in a design point of view to choose

the layout topology that will be more precise in drawing the line lengths. As shown in Table 3.2 most of the elements have to be tested on different area depending on how important is the fault. For example a 5% variation on L2 is detected in the transition area with the $Isol(f/h_3)$, but a 20% variation is detected in the nonlinear area using P_{6dB} . Table 3.2 can be also analyzed in a design point of view. Since the amplifier is working in the linear and transition area a designer can interpret elements covered by the nonlinear zone as elements which don't present high influence on the functioning of the circuit, since this type of circuit doesn't function in its non linear area. Some defects on these components can be tolerated because the circuit will not be disturbed in its functioning by these faults.

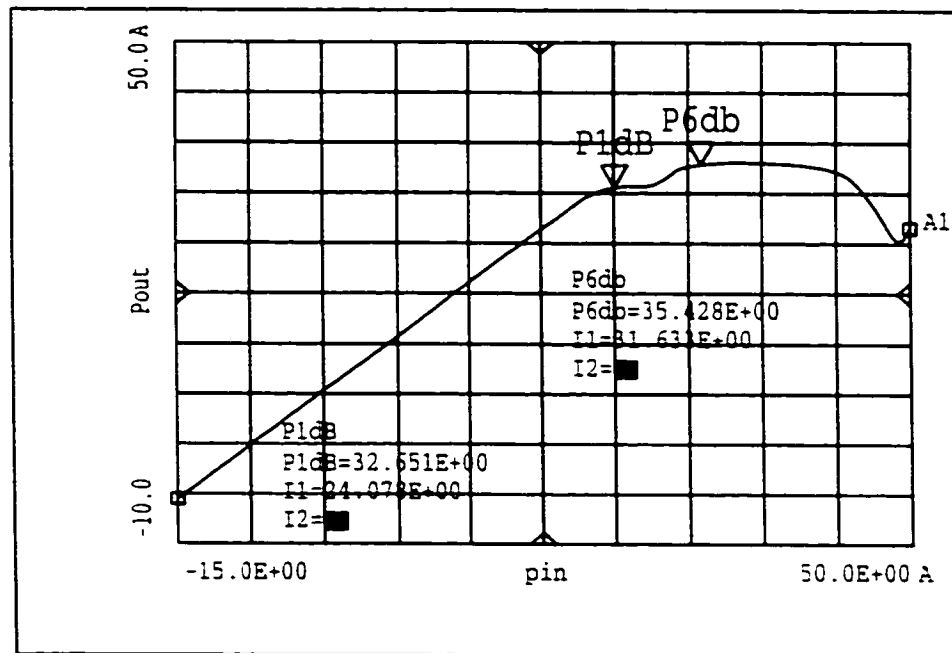


Figure 3.4 Simulated power transfer function of the power amplifier shown in fig 3

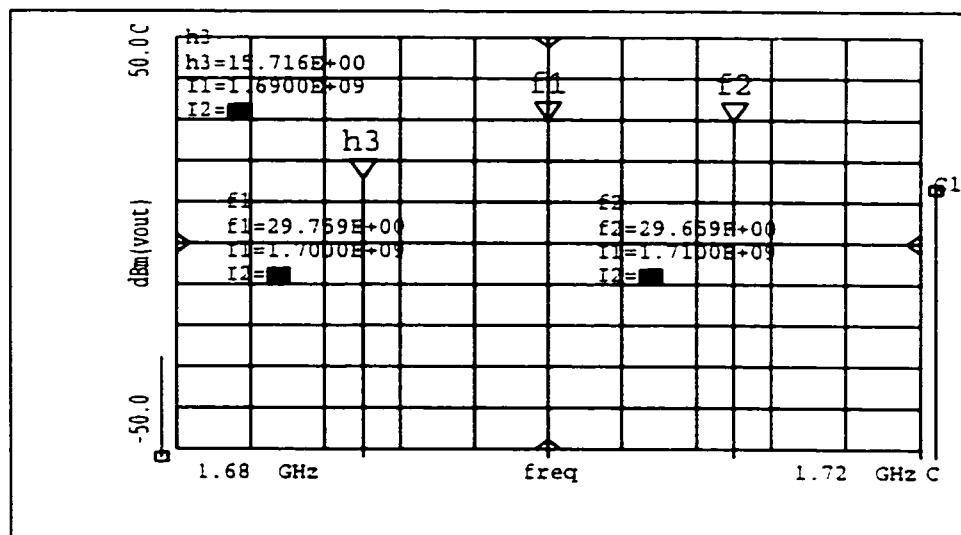


Figure 3.5 Output spectrum of the amplifier with two excitations at P_{1dB}

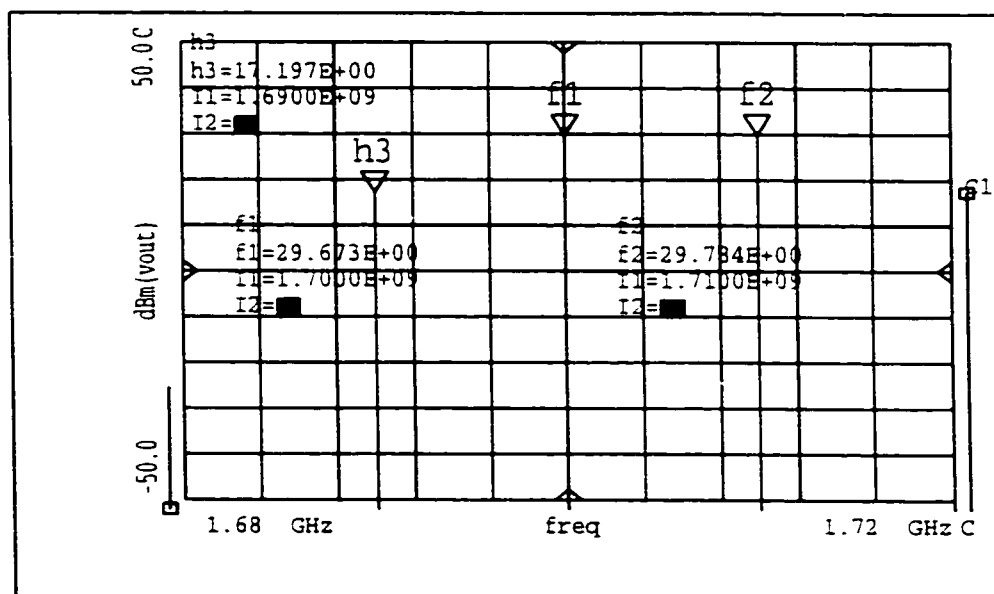


Figure 3.6 Output spectrum of the amplifier with two excitations at P_{6dB}

Table 3.1 Performances of the Simulated Power Amplifier

	Linear Area	Transition area	Nonlinear Area
Linear Gain G	10.31dB	N.A	N.A
P_{1dB}	N.A	35.576 dBm	N.A
Isol(f/h_3) at P_{1dB}	N.A	14.043 dBc	N.A
P_{6dB}	N.A	N.A	35.68 dBm
Isol(f/h_3) at P_{6dB}	N.A	N.A	12.476 dBc

Table 3.2 Fault detection in each segment

	Linear Area	Transition Area		Nonlinear Area	
	ΔG	ΔP_{1dB}	$\Delta \text{Isol}(f/h_3)$ at P_{1dB}	ΔP_{6dB}	$\Delta \text{Isol}(f/h_3)$ at P_{6dB}
Detected Elements	R(5%), R(20%), L1(20%), L3(20%), W2(20%)	L3(5%) L4(20%) W3(5%) W4(5%)	L2(5%) L5(5%) L5(20%) W2(5%) W3(20%) W5(5%) W5(20%)	L1(5%) L2(20%)	L2(5%) L4(5%) W1(5%) W1(20%) W4(20%)

5. Conclusion

In this paper we have presented a new method for performing quick and efficient testing for RF nonlinear power amplifier. This method is strictly based on power analysis and the segmentation of the power transfer function. The results obtained show the fact that the performances of the circuit are being influenced depending on the component which is varying and in the segment in which it is observed. With this methodology all considered components of a class A power amplifier has been covered. In a further work the power transfer function segmentation approach is expected to be improved in order to apply it on other types of nonlinear circuits like oscillators and mixers

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CHAPITRE 4

AMELIORATION DE L'INTERFACE DE TEST DES CIRCUITS VLSI FONCTIONNANT EN HAUTES FREQUENCES

4.1 Résumé

On ne cesse aujourd'hui d'observer l'augmentation de la rapidité de fonctionnement des circuits intégrés. Cette rapidité croissante n'est pas sans poser des problèmes de test et de mesures [82]. De nombreux phénomènes jusque là insignifiants en basses et moyennes fréquences doivent être tenus en considération. L'un des problèmes les plus pressants aujourd'hui est l'effet des distorsions subites par le signal au niveau de l'interface de test Circuit sous test-Testeur. Ces effets de distorsions compromettent sérieusement l'intégrité du signal. L'interface de test est constituée du circuit sous test, du testeur qui présente un comparateur à l'entrée et d'une ligne de transmission d'impédance caractéristique 50 ohms qui relie le circuit au comparateur qui est localisé à l'entrée du testeur. L'analyse de cet interface met en évidence le rôle fondamental de la ligne de transmission, et la nécessité d'une profonde connaissance de son comportement [Annexe III]. Il est donc très important de régler le problème de la désadaptation d'impédance entre le circuit et la ligne de transmission, ainsi que l'effet de filtre produit par la capacité parasite à l'entrée du

comparateur d'autre part. Comme nous l'avons mentionné plus haut les testeurs présentent des comparateurs à leurs entrées. Ce comparateur permet de reconnaître le niveau logique du signal d'entrée.

- L'adaptation d'impédance entre le circuit à tester et la ligne de transmission d'impédance 50 ohms constitue la première source d'imprécisions lors du test des circuits ITGE en hautes fréquences. Comme nous l'avons mentionné dans l'introduction, les instruments de test de circuits en hautes fréquences fonctionnent dans un environnement standard de 50 ohms. Ainsi il est impératif que les circuits sous test puissent respecter cette contrainte. Certains circuits ITGE présentent des impédances de sortie différentes de 50 ohms et des niveaux de courant de sortie très faibles, entraînant ainsi une incompatibilité avec les lignes de transmission auxquels ils sont connectés avant d'attaquer l'équipement de test. Cette incompatibilité va se traduire par des réflexions, des oscillations, et des dépassements qui seront alors à l'origine d'erreurs et peuvent dans certains cas détruire le comparateur.
- Quant à la capacité parasite à l'entrée du comparateur, elle va s'ajouter à l'impédance caractéristique de la ligne de transmission pour former un filtre passe-bas. Ce filtre passe-bas limitera l'interface de test en fréquence. L'effet de ce filtre peut aussi être à l'origine d'un retard de synchronisation au niveau du fonctionnement du comparateur qui se trouve à l'entrée du testeur.

L'article présenté dans ce chapitre traite de l'adaptation d'impédance entre le circuit sous test et la ligne de transmission et ensuite l'élimination de l'effet de la capacité parasite à

l'entrée du comparateur. Cet article expose une solution qui consiste en l'utilisation d'un circuit tampon haute vitesse afin de créer une compatibilité entre le circuit sous test et la ligne de transmission. Grâce à ce circuit tampon, nous ferons terminer le circuit sous test par une impédance de terminaison 50 ohms. L'utilisation d'un filtre passe-tout entre la ligne de transmission et l'entrée du comparateur est suggéré pour faire face à l'effet de filtre résultant de la capacité parasite. La conception de ce filtre passe-tout va inclure la capacité parasite comme un élément atténuant ainsi son effet.

L'article présenté dans ce chapitre est intitulé "A Unity Gain High Speed Buffer to Improve Signal Integrity in High Frequency Test Interface". Il a été soumis pour publication dans le *Journal of Electronic Testing: Theory and Application*.

4.2 A Unity Gain High Speed Buffer to Improve Signal Integrity in High Frequency Test Interface

A Unity Gain High Speed Buffer to Improve Signal Integrity in High Frequency Test Interface

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Abstract

The availability of faster electronic components allows the design of more effective high speed systems. However, engineers face ringings, overshoots and timing delay problems with these circuits. In this paper we present an output high speed buffer which helps to improve the test of faster device families. The high speed buffer helps cancel the transmission line effects while testing these devices. The buffer presented here has a unity gain, introduces small delay and presents a high output current. It is able to drive the comparator through the transmission line without any distortion of the signal. The output buffer which is designed for DUT-to-tester interface can be considered for interconnections between PCB as well. We also present in this paper a method that eliminates the low pass filter effect introduced by the association of the transmission line and the lumped capacitance at the input of the tester.

1.0 Introduction

With the increasing demand for high frequency circuits, a formidable challenge is presented to the VLSI circuits designers. The propagation of the signals from the DUT (Device Under Test) to the ATE (Automatic Test Equipment) may cause problems while testing these devices. In practice, transmission lines techniques are used to connect the DUT (Device Under Test) to the tester in order to maintain an efficient transmission of the signal. However, with the advent of devices possessing extremely fast rise and fall times, negative effects introduced by the transmission line become more pronounced. To minimize these undesirable events, additional care is required from designers. Some effects that are insignificant at low frequency domain need to be taken into consideration.

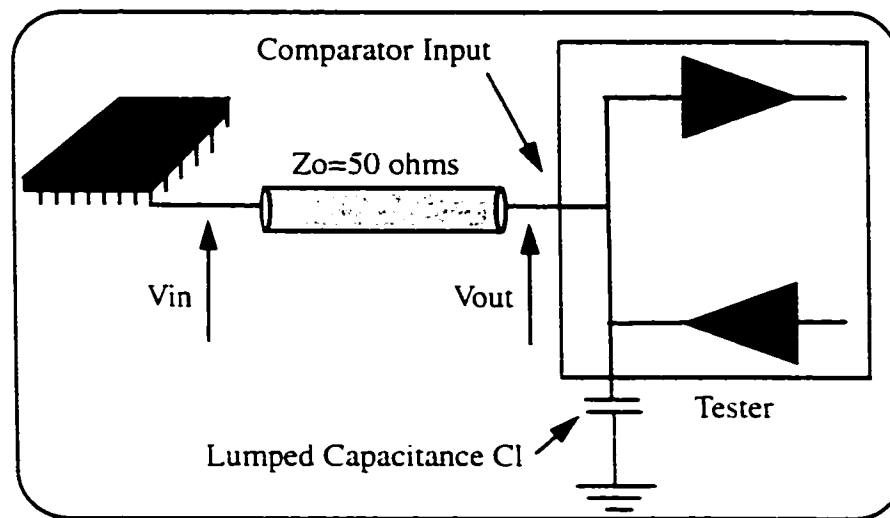


Figure 4.1 High Frequency Test Interface

Figure 1 represents a high frequency test interface for an IC circuit. The circuit is connected to a tester comparator through a 50Ω transmission line. C_l represents the capacitance at the

input of the comparator. The value of C_I can vary from one tester to another, but in most case it is better to have it low as it will be explain further in this paper. From the analysis of this high frequency test interface two problems emerge: an impedance mismatch introduced by the connection between the device under test output resistance and the transmission line, and the effect of the lumped capacitance at the input of the comparator. When the DUT is driving the comparator through the transmission line, one of the largest sources of inaccuracies is the impedance mismatch [1]. The output impedance of the device at high frequencies can be lower or higher than 50Ω , whereas the typical transmission line has a 50Ω impedance. The output voltage transition of the device under test will result in multiple reflections which show up as ringing [2]. Ringing causes unwanted crossings of logic thresholds, which can be detected by certain comparators with very sensitive input. In cases of severe ringing, overshoots or undershoots are produced, which can cripple the comparator by violating the minimum voltage level allowed at its input. The overshoots can also make the device appear faster causing timing errors in the determination of the device propagation delays. The overshoot is expressed from the reflection coefficient $\Gamma = (R_o - Z_o) / (R_o + Z_o)$, where R_o and Z_o are respectively the output impedance of the device under test and the characteristic impedance of the transmission line. The overshoots resulting from this reflection will be Γ times the original waveform to appear at the comparator input. The ringings and subsequent overshoots are illustrated in figure 2. This figure is obtained by performing a simulation of the interface presented in figure 1 using MDS (Microwave & RF Design System) CAD tool. We can notice on this figure the

degradation of the output signal due to ringings and overshoots as mentioned earlier can be easily noticed. In order to get a good transmission of the signal between the DUT and the tester, the ringings and the overshoots have to be settled. Some methods of hand analysis (which are not the purpose of this present work) are available [3][4][5], to help understand and predict the signal integrity through the interface. These methods also provide necessary informations to compile voltage versus time plots, which show the severity and occurrence of transmission line effects.

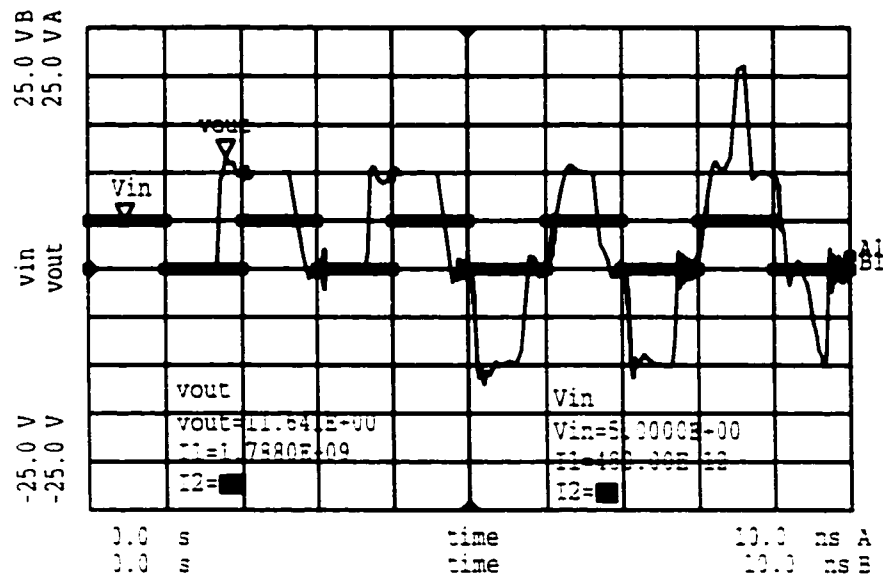


Figure 4.2 Ringings and overshoots observation

Typically, ATE system specifications include maximum input capacitance. This specification is the sum of the distributed capacitance of the transmission line plus the lumped capacitance at the comparator input. However, for a lossless transmission line, the distributed capacitance will have no effect on the transition time or bandwidth of the signal

propagating along. Therefore the distributed capacitance has little effects on the tester's ability to test high frequency devices [1]. The propagation delay down the transmission line from device to the comparator will be mostly affected by the lumped capacitance C_l which forms a low pass filter with the transmission line. Due to that low pass filter's step response time t_s : $t_s = 2.2 * Z_0 * C_l$ (defined from 10% to 90% of the amplitude of the output signal), any signal with transition time t_t applied to the input of the filter will be slowed down to t_{res} with $t_{res} = \sqrt{t_s^2 + t_t^2}$. In the presence of a high C_l , the rise and fall times are slowed due to the increased RC time. The effective lumped input capacitance of a tester's comparator should have as low value as possible in order to accurately test the high edge rate output signals of high frequency DUT. This analysis leads to the conclusion that a high frequency testing interface is not efficient as long as the effects of the impedance mismatch and the lumped capacitance at the input of the comparator are not cancelled.

Several approaches [1][7][8][9][10][11][12] have been used to study the effect of the transmission line in high frequency testing. In [1] a reduction of the transmission line length between DUT output and tester comparator input is proposed. This method has the significant advantage of minimizing the difference between the test environment and the end-use environment. One significant disadvantage of this method is that, in order to handle DUT I/O pins, the tester's drivers would also have to be placed very close to the DUT. Note that to date (14 years after this publication), no one has been able to build such a system in a cost-effective manner. Another approach presented in [8] is to compensate the reflections by manipulating the timing and by programming the reference voltage of the

tester comparators. Since the resulting DUT output waveforms can be predicted with reasonable accuracy, compensation can be incorporated in the test program to account for the waveform distortion. This approach requires knowledge of the tester input characteristics, device characterization and additional test engineering effort, since test system software and calibration do not automatically comprehend device specific compensation. Furthermore, although test program compensation can sometimes be used to achieve better DUT output delay measurement accuracy, it cannot generally correct inherent high speed functional test problems associated with reflections. An approach presented in [9] proposes to add clamping diodes at the tester's comparator circuits to clamp the ringing of the device under test output signals due to reflections. The effectiveness of this technique is however reduced when the time between DUT output signal transitions is less than the round trip delay of the interconnection transmission line; in this case, timing errors can be significant. Therefore, even though the magnitude of the reflections can be limited with this method, the length of the transmission line will still determine the maximum frequency (or minimum pulse width) that can be accurately tested. There are two other things to keep in mind about clamping diode terminations: the diode must be very fast compared to the rising edge time to have any effect, and also it must clamp to a level offset from ground by the forward voltage drop of the diode.

In the literature some transmission line terminations methods like parallel, Thevenin and RC network have been proposed (figure 4.3). The parallel termination resistor uses a single resistor tied to ground or V_{cc} , the value of the resistor equals Z_0 . With the Thevenin termination method one resistor is connected to ground and a second resistor to V_{cc} . To

avoid settling of the voltage at a point between the high and low logic levels that causes reduced noise margins, careful consideration of the ratio of resistors is required. For the RC networks, the resistor is used to match the impedance; meanwhile the capacitor helps to hold the dc signal component, allowing the ac to flow to ground during the switching of logic states. These methods although they reduce the effects of ringing, present some serious drawbacks (see table 1).

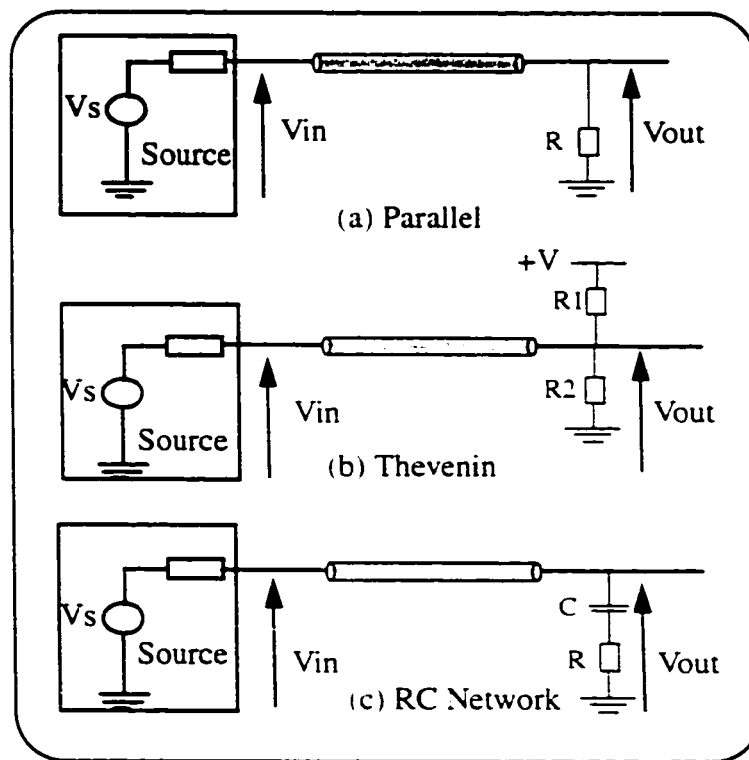


Figure 4.3 Different methods of transmission line matching

Table 4 1.Some suggested transmission line termination types and their properties

Termination Type	Added Parts	Delay Added	Power Required	Parts Values	Comments
Parallel	1	small	High	$R=Z_0$	Power Consumption is a problem
Thevenin	2	small	High	$R=2*Z_0$	High Power Consumption
RC Network	2	small	Medium	$R=Z_0$ $C=300\text{pf}$	Limited Bandwidth and Added Capacitance

An interesting way to solve the transmission line issue could be to terminate the transmission line by its characteristic impedance using a backmatch resistor, as described in figure 4.4. The concept of this method is to try to match the transmission line impedance with a Z_{out} impedance. Z_{out} represents the sum of the DUT output impedance (R_{out}) and a series resistor (R_s) impedance inserted between the DUT and the transmission line. The resistor should be located as close to the DUT as possible [13].

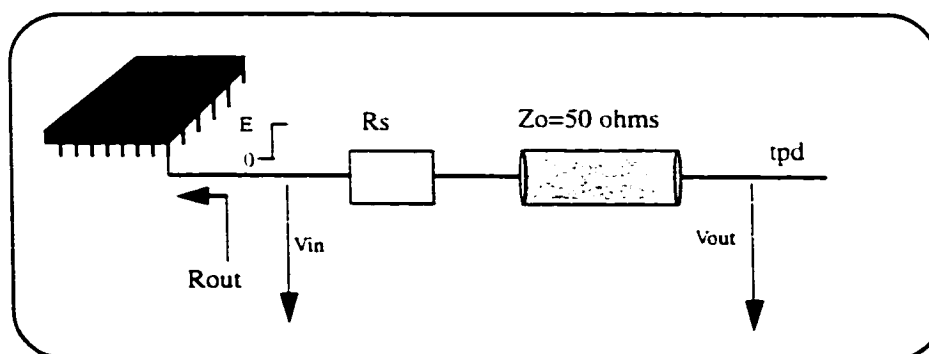


Figure 4.4Transmission line terminated using backmatch resistor technique

This method is very interesting when a minimum number of devices is required to terminate the transmission line and when the DUT output impedance is less than the characteristic impedance of the transmission line. Also with this method no quiescent power is dissipated. The AC power dissipation P can be estimated by the following equation:

$$P \approx f \left(\frac{\Delta V}{2R} \right)^2$$

In this equation, f represents the input pulse frequency, R is the termination resistance. ΔV represents the difference between V_{OH} and V_{OL} . This approximation works if the pulse width is greater than twice the line delay. With its low power dissipation, we can deduct that series termination should be recommended for low voltage logic.

The disadvantage of this technique is the effect of the resistor on any output level with current loads. The series resistor R_s will reduce the current level. The signal V_{out} at the input of the tester will change accordingly to the value of the impedance Z_{out} . When $Z_{out}=Z_o$, no reflection occurs as the source side is terminated. The forward wave will see the line as $Z_{out}=Z_o$, then V_{out} is identical to V_{in} at the output of the DUT circuit, only a propagation delay t_p may be introduced by the transmission line (figure 4.5). When the value of Z_{out} starts varying from Z_o , the impedance mismatch creates a series of pulses that reflect back and forth (ringing), as shown on figure 4.6. This explains why the backmatch resistor technique is preferred when the DUT output impedance R_{out} is less than the characteristic impedance of the transmission line.

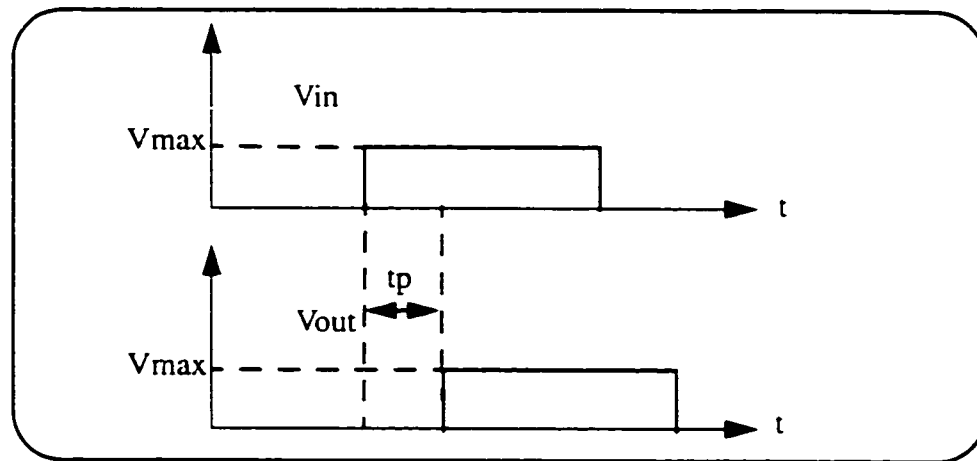


Figure 4.5 Input and output voltages V_{in} , V_{out} when $Z_{out}=Z_o$

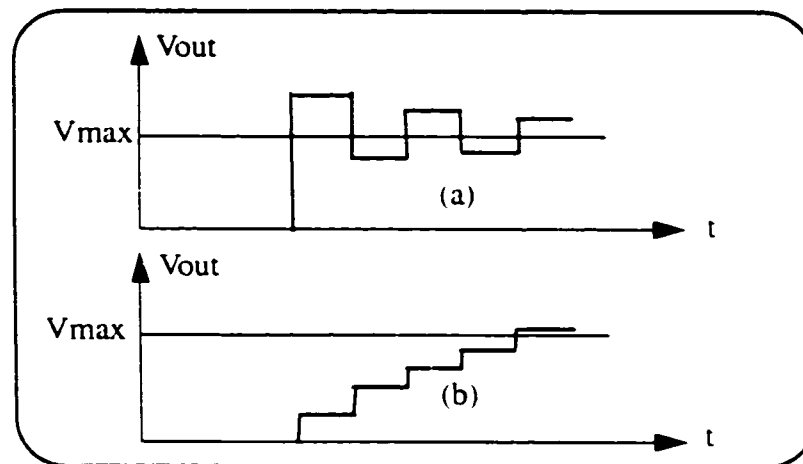


Figure 4.6 Voltage at the input of tester's comparator.

a) $Z_{out} < Z_o$, b) $Z_{out} > Z_o$

In this paper we present methods to improve the high frequency test interface, by eliminating the negative effects of the transmission line, and reducing the low pass filter introduced by the lumped capacitance at the input of the tester's comparator. To remove

the negative effects of the transmission line, we propose the use of a unity gain high speed buffer which helps cancel the effects of the impedance mismatch and the lumped capacitance during high frequency test. The method is based on terminating the transmission line by its characteristic impedance at the DUT side. For the low pass filter effect, the lumped capacitance at the input of the tester's comparator is used in an all pass filter configuration to cancel its effect. This paper is organized as follows. In section 2, we will present our method concerning the transmission line issue and also the experimental results. In section 3, the case of the lumped capacitance will be treated with some results, and the conclusion will follow in section 4.

2.0 The transmission line issue

It has been shown from the previous section that the ringings and overshoots are the consequences of the impedance mismatch between the transmission line and the output of the DUT. In order to eliminate these effects, we propose the insertion of a unity gain high speed buffer between the DUT and the transmission line. The buffer will provide a termination almost equal to 50 ohms for the transmission line. Therefore, any reflection from the open ended line at the comparator will be absorbed. Figure 4.7 shows the configuration we propose to solve this problem. V_s and R_{so} represent the signal delivered by the DUT and the output resistor of the DUT respectively. In the presence of the buffer, the DUT will always present an output impedance equal or less than 50 ohms, it will be then easy to match 50 ohms using a small resistor to the output.

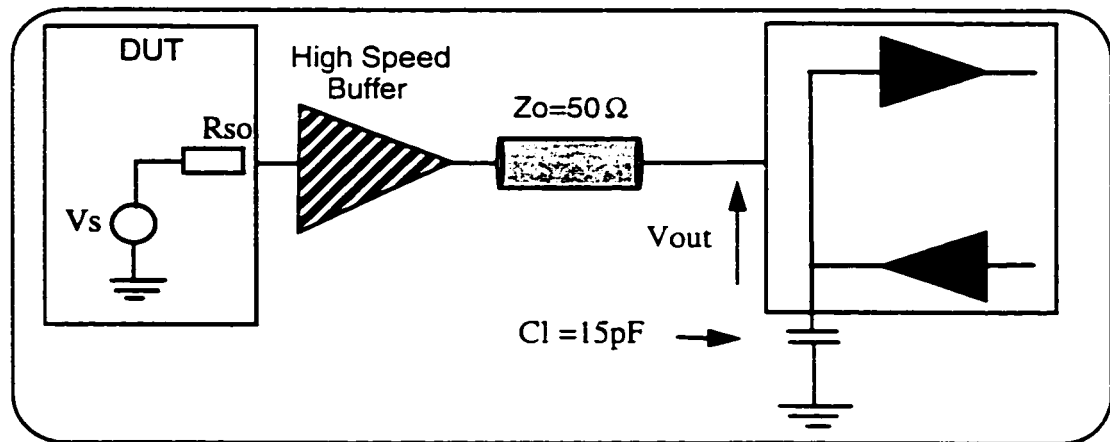


Figure 4.7 The proposed configuration using a high speed buffer inserted between the DUT and the transmission line

The simplified schematic of the proposed unity gain buffer is shown on figure 4.8. In its functionality, the buffer is divided into two main parts. The first part is a follower stage to help forward a “0” or a “1”, followed by a class AB output power stage. Transistors Q1 and Q2 are used for the purpose of the follower stage. The output of the two emitter followers are connected to currents source I1 and I2, respectively in parallel with the base of the transistors Q3 and Q4 of the output stage. The currents source I1 and I2 source /sink the quiescent base current when needed.

The presence of a “0” at input of the buffer will turn transistor Q1 “on”. it will allow all the current from I1 to flow to ground. Transistor Q3 will be then “off” because of the very low value of its current base. Meantime, Q2 is “off”, all the current available from I2 will flow to the base of Q4 to turn this transistor “on”. The output of the buffer is then set to “0”. In the event of a “1” at the input, the functionality of the buffer will be similar to the event of

a “0” at the input excepted that in this case transistor Q1 will be “off”, while Q2 will be “on”. With Q2 conducting, no current will flow to the base of Q4 to turn it on. Meanwhile the current available from I1 will flow in the base of transistor Q3 to turn it “on”. The output is then set at “1”.

In practice current sources I1 and I2 are obtained from current mirrors that are shown respectively by figure 4.9 and figure 4.10. Unlike source I2 which is a simple basic current mirror (figure 4.10), I1 is cascade of two current mirrors as shown on figure 4.9. The first stage is identical to sources I2, it has an output current almost equal to its input current I_{Ref}. This stage provides input current I_{Ref1} for the second stage. The use of a second stage is explained by the fact that source I1 must provide an outgoing current for that purpose the second stage is achieved using p transistors. The second stage uses a modification of the simple bipolar current mirror. An emitter-follower transistor, Q9, is added to supply the base currents. This additional transistor minimizes the errors due to finite base currents, resulting in $I_{out} = I_{in} (1 - 2/\beta)$, where β is p transistors current gain. Such an arrangement is almost always used for current mirrors when lateral transistors are used because of their low current gains. Figure 4.11 describes the full schematic of the buffer.

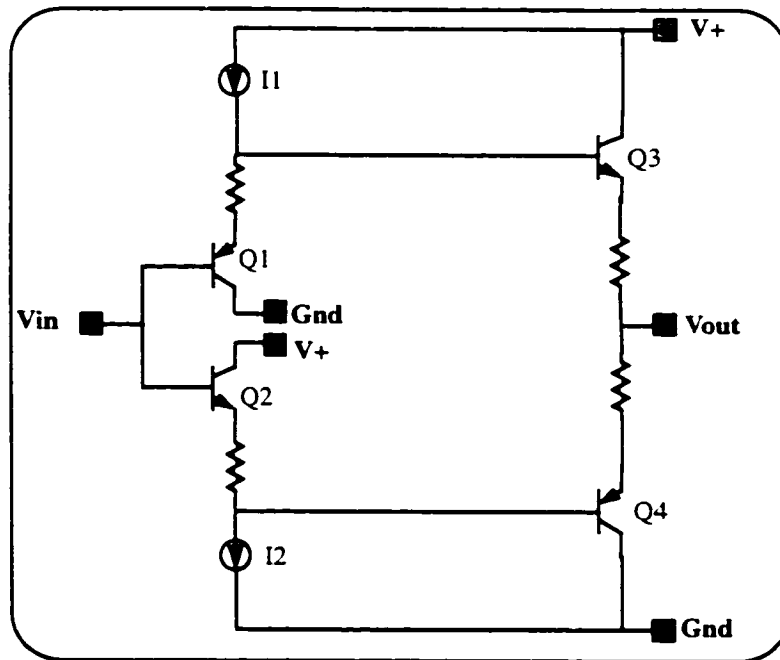
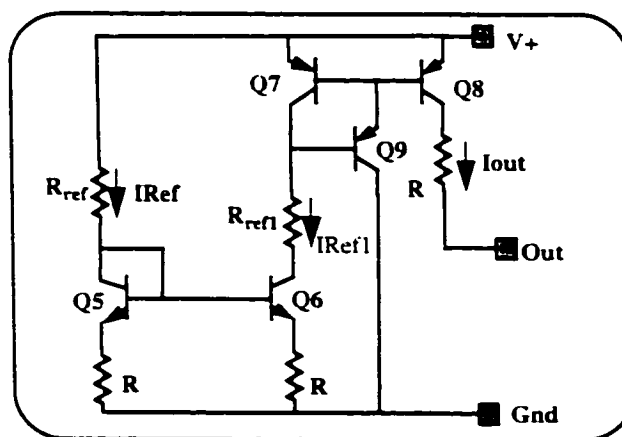


Figure 4.8 Simplified schematic of the buffer

Figure 4.9 Current mirror to supply $I1$

The buffer has been simulated using Hspice simulator in cadence environment. The technology used during the simulation is Nortel NT25 bipolar technology. Table 4.2 describes the characteristics from simulation. We can notice that the buffer has an high output current that will be able to drive a 50 ohms transmission line (Table 4.2). The buffer also presents a very small propagation delay, which is very important in terms of synchronization of the tester. The importance of the propagation delay is critical in this method. In the case of a longer propagation delay of the buffer, some synchronization problems might occur within the tester, resulting in measurement inaccuracy. Table 4.2 also shows a small output impedance.

Table 4 2.Performances and characteristics of the simulated high speed buffer

Parameter	
Power Supply	3.3 V
Output Current	> 90 mA
Rail to Rail Voltage	2.3 V
Input Resistance	1.2 M Ω
Output Resistance	39 Ω
Rise time	406 ps
Fall time	611 ps
Propagation Delay Time	317 ps
Technology	bipolar Technology

The buffer output signal for a 3.3V input square signal of 160MHz is observed on figure 4.12. The speed of the buffer in our case depends more of the model of transistor used. The

proposed configuration should theoretically function around 1 GHz, but in order to reach that speed the n transistors and p transistors used should be true complements. In the case of non complementarity between the n and p types of transistors, a distortion of the buffer output signal is observed, as the speed increases. This distortion is mainly due to the fact that one transistor is faster and presents a higher beta than the other. In our case we can observe the fact the n type transistor is faster than the p type transistor. As we mentioned earlier, the comparator's input presents a lumped capacitance. This capacitance can vary from one tester to another. In our case the lumped capacitance is fixed at 15pf. As we can notice the output signal of the buffer is identical to its input. However, the rise and fall times present a slight delay than can be ignored. Also there is a little loss of voltage level that can be observed at V_{OH} and V_{OL} .

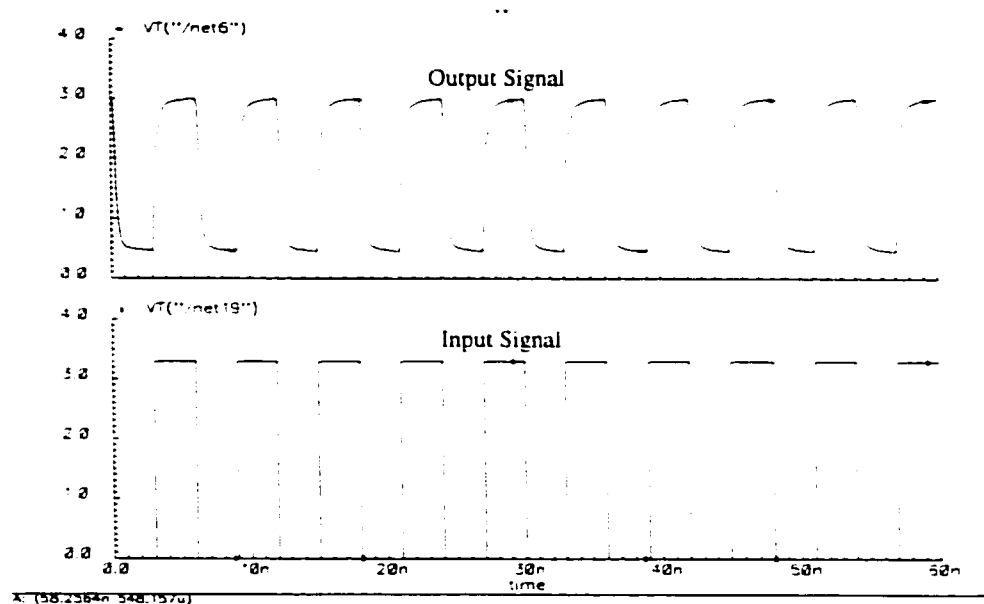


Figure 4.12 Input and Output signals of the buffer

Figure 4.13 illustrates the signal at the input of the tester's comparator when the signal at the output of the DUT is applied through the interface. Some residual overshoots and ringings at the input of the comparator are noticed. These residual overshoots are explained by the presence of reflections due to the impedance mismatch between the transmission line and the buffer. As it is shown on Table 4.2, the buffer output impedance R_{out} is 39 ohms. It takes then a 11 ohms series resistor R_s to make $Z_{out} = 50$ ohms. Once $Z_{out} = 50$ ohms the impedance matching is achieved. The signal then doesn't present any distortion (ringing or overshoot) as shown on figure 4.14. However the signal presents a delay. This delay is a composite delay of the one introduced by the buffer and the delay introduced by the transmission line. Since the buffer propagation delay is small, the observed delay is coming mostly from the transmission line. The length of the transmission line has to be then optimized in order to keep the delay introduced through the test interface reasonable. Figure 4.15 illustrates the layout of the high speed buffer that is currently under fabrication. The area of the circuit is $200\mu\text{m}$ over $235\mu\text{m}$.

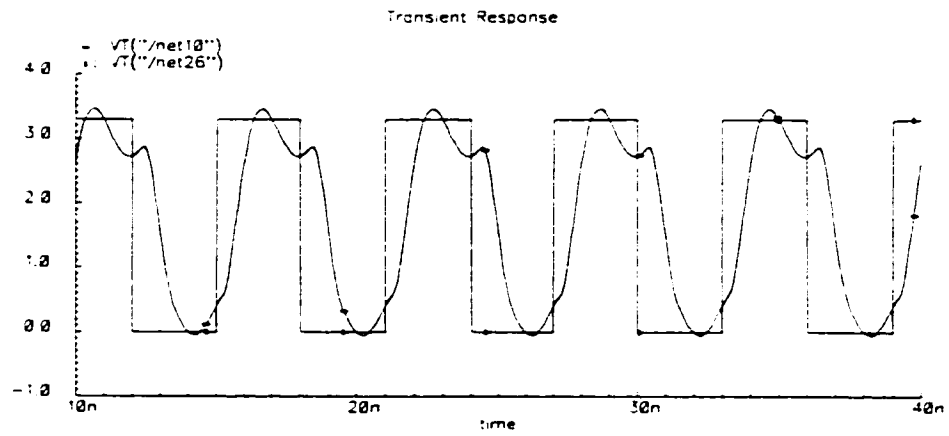


Figure 4.13 Signal at the input of the comparator without any series resistor

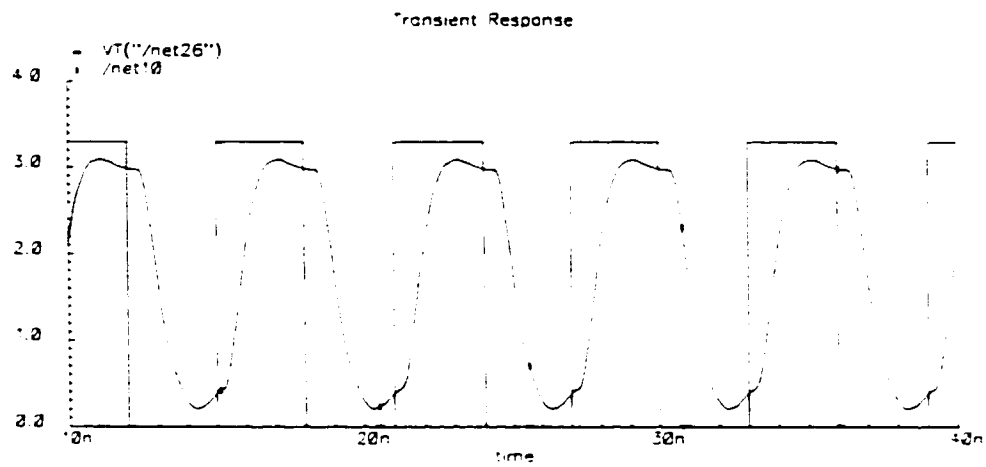


Figure 4.14 Signal at the input of the comparator with 11 ohms series resistor

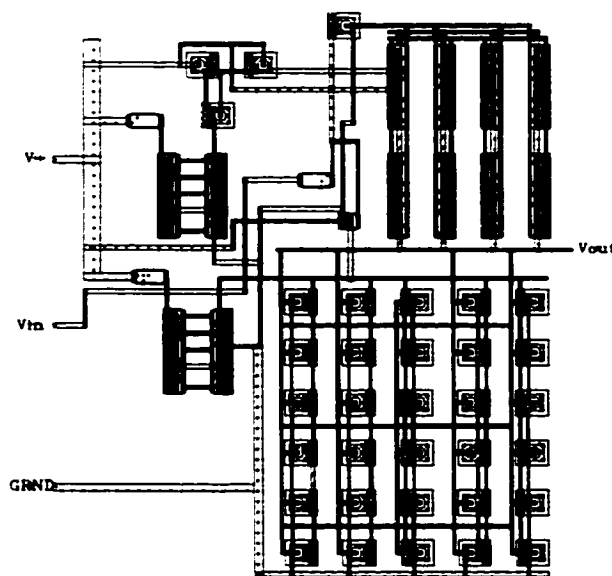


Figure 4.15 Layout of the high speed buffer

3.0 Cancelling the effect of the lumped capacitance

The primary effect of the lumped capacitance C_l is a delay approximately equal to $Z_o * C_l$. This lumped capacitance also acts with the transmission line impedance Z_o as a low pass filter, which limits the effective input bandwidth of the comparator as we mentioned before. The higher the value of C_l is, the lower the cut-off frequency is. Simulation with Hspice of the low pass filter formed by the impedance Z_o and the lumped capacitance C_l with different values of C_l shows a variation in the bandwidth of the filter. For example, using a 5v input signal for a $C_l=3\text{pf}$, the cut-off frequency f_c is at 286MHz, but if $C_l=30\text{pf}$ we observe that f_c falls drastically to 87MHz. If the lumped capacitance of the comparator is 30pF, the signal at the input of the comparator becomes a sinewave signal instead of a

square waveform as shown in figure 4.18. To reduce the effect of this lumped capacitance we use an all pass filter configuration in which the lumped capacitance C_l can be used as an element. The bandwidth of the all pass filter should be wide enough to conserve the fundamental sinewave and the important harmonics that constitute the input square waveform signal. Figure 4.16 represents the configuration of the proposed all pass filter which transfer function is:

$$H(s) = \frac{s^2 + s(1/R_x + 1/R_y)(1/C_l) + 1/(C_l C C_l R_y)}{s^2 + s(1/(\tau_1) + 1/(\tau_2) + 1/(\tau_2)) + (\tau_1 R_y C)}$$

In this equation we have $\tau_1 = R_x C_l$ and $\tau_2 = R_y C_l$.

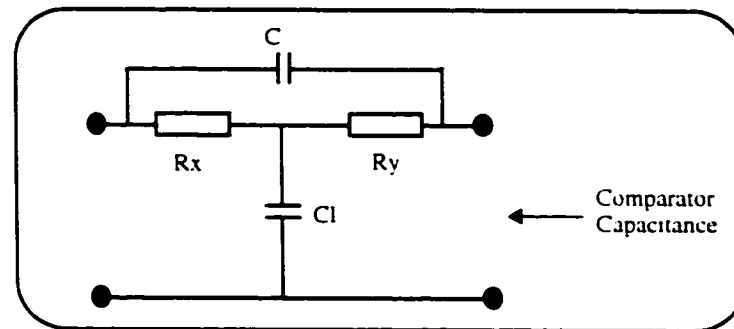


Figure 4.16 All pass filter used to cancel the lumped capacitance effect

The proposed filter is connected to the input of the comparator as shown in figure 4.17 and simulated with Hspice simulator. Results of simulation show a good improvement of the bandwidth as shown in figure 4.19 for $C_l=3\text{pF}$ and in figure 4.20 for $C_l=30\text{pF}$,

comparatively to figure 4.18. Figure 4.18 represents the signal at input of the comparator without the all-pass filter inserted in the interface.

4.0 Conclusion

Testing high frequency circuits presents serious difficulties. The main difficulties come from the impedance mismatch and parasitic capacitance. In this work we have presented a technique to improve the high frequency test interface by using a high speed buffer between the DUT and the transmission line in one hand, and in other an all pass filter that uses the lumped capacitance parasitic capacitance at the input of the tester between the transmission line and the tester. With this method, the signal integrity is improved through the high frequency test interface.

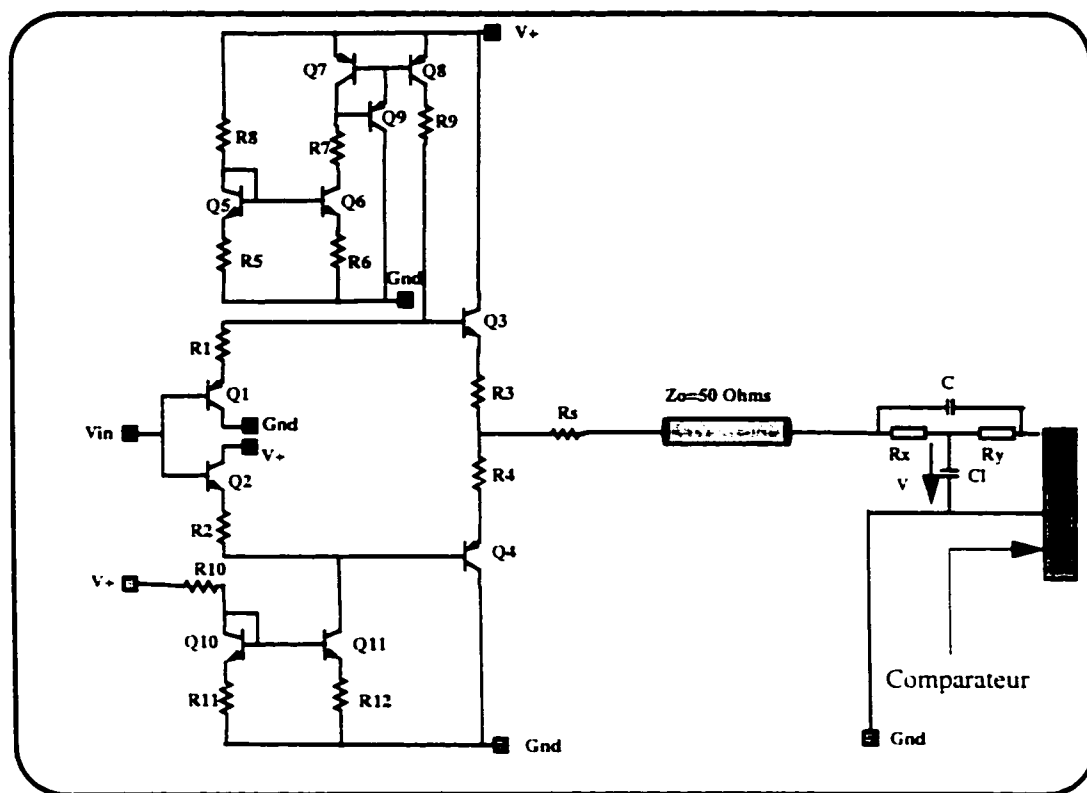


Figure 4.17 Complete electrical schematic of the proposed high frequency test interface

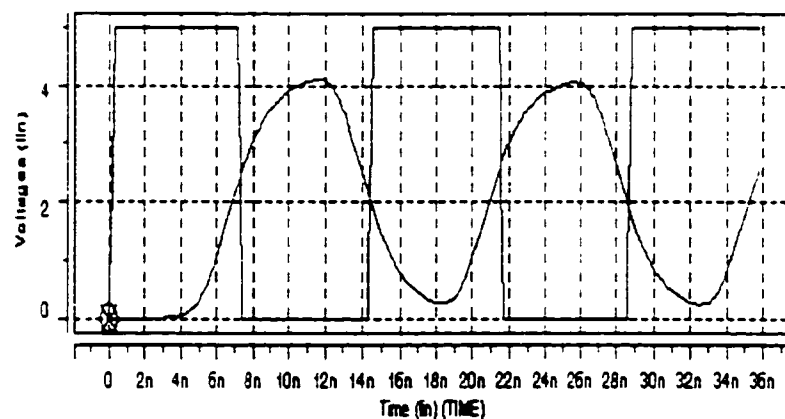


Figure 4.18 Input voltage of the tester comparator for $C1=30\text{pF}$

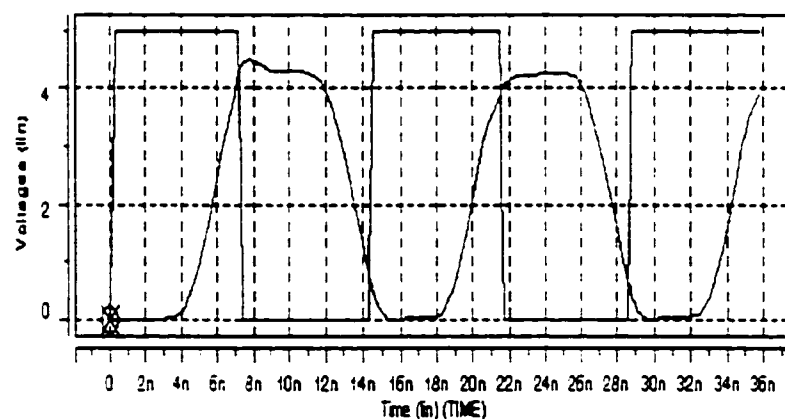


Figure 4.19 Input voltage of the tester comparator after adding the all pass filter for $C1=3\text{pF}$

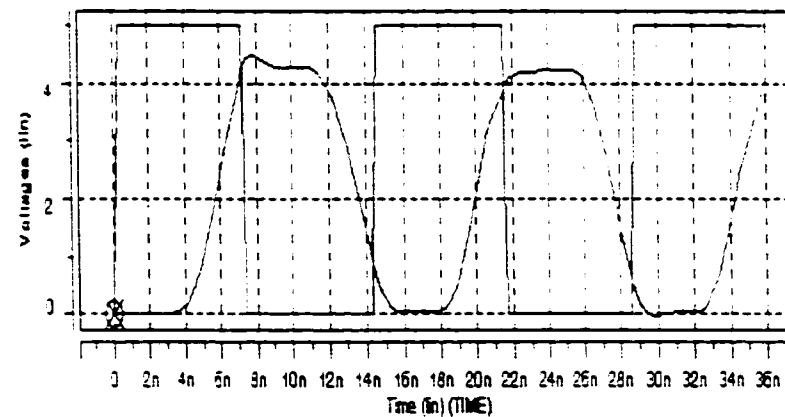


Figure 4.20 Input voltage of the tester comparator after adding the all pass filter for $C1=30\text{pF}$

5.0 Reference

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CHAPITRE 5

CONCLUSION

La présente thèse constitue à notre avis une avancée dans la compréhension de la testabilité des circuits intégrés hautes fréquences. Dans cette thèse nous avons étudié et analysé divers aspects du test des circuits intégrés hautes fréquences. Nous avons mis en évidence deux problèmes cruciaux rencontrés dans le cadre du test des circuits intégrés hautes fréquences lors d'une production à grande échelle. Le premier se situe au niveau du test structurel des circuits intégrés hautes fréquences. Un des plus sérieux handicaps auquel font face les concepteurs de circuits intégrés électroniques est la découverte d'un grand nombre de circuits de production de masse défectueux après fabrication, sans pour autant pouvoir localiser les défauts. Le deuxième problème tourne autour de l'interface utilisée pour tester certains circuits hautes fréquences avec les équipements fonctionnant dans l'environnement standard 50 ohms. Nous avons ainsi proposé un ensemble de méthodologies et de solutions pratiques destinées à améliorer le test de ces circuits en tenant compte des deux problèmes mentionnés plus tôt.

Dans le chapitre 2, nous avons analysé et proposé une méthodologie relative à la testabilité structurelle des circuits intégrés hautes fréquences fonctionnant en mode linéaire, dans le cadre d'une production à grande échelle. L'idée maîtresse qui sous-tend cette méthodologie est que l'optimisation de chaque étape du processus de fabrication des circuits prise

individuellement, ne donne qu'un bénéfice minime. Ainsi il est plus judicieux de considérer l'étape de conception, de fabrication et de test comme un tout. Ainsi les différents aspects du test devraient être pris en considération dès l'étape de conception. Cette méthodologie de test est basée sur une analyse de sensibilité, combinée avec une analyse fréquentielle pour les circuits hautes fréquences linéaires.

Le cas des circuits intégrés hautes fréquences fonctionnant en mode non linéaire a été traité dans le chapitre 3 . Ainsi, nous avons proposé une méthodologie similaire sur le plan objectif à celle proposée dans le chapitre 2. La méthodologie présentée dans ce chapitre est cependant basée sur une analyse de la puissance.

Les méthodologies présentées dans les chapitres 2 et 3 représentent une avancée très importante dans le domaine des tests des circuits hautes fréquences. Elles devraient permettre à l'industrie d'augmenter la fiabilité des circuits intégrés, en mettant sur le marché des circuits hautes fréquences robustes, tout en réduisant leur coût de production.

Dans le chapitre 4 nous avons présenté une solution permettant de rendre plus efficace l'interface de test de certains circuits ITGE. En effet de nombreux phénomènes inconnus en basses et moyennes fréquences apparaissent lorsque l'on veut tester certains types de circuits intégrés hautes fréquences avec les équipements disponibles sur le marché. Nous avons tenu à expliquer l'origine de ces phénomènes. Nous avons proposé une solution pratique pour remédier à cette situation afin de pouvoir conserver l'intégrité du signal et obtenir des mesures plus précises. La solution proposée repose en partie sur la conception et l'insertion d'un circuit tampon à haute vitesse entre le circuit sous test haute fréquence

et la ligne de transmission d'impédance caractéristique 50Ω . L'autre aspect de la solution proposée est la prise en considération de la capacité parasite à l'entrée du comparateur dans une structure de filtre passe tout. La solution ainsi proposée permet dans sa globalité de régler un problème pratique auquel l'industrie s'est heurtée. Ainsi nous avons créé une compatibilité de facto entre ces circuits et le matériel disponibles.

Par ailleurs, il est très important de souligner que cette thèse ouvre des perspectives de recherches futures. Lors des analyses développées aux chapitres 2 et 3 nous n'avons pris en compte que le cas où on fait face à un seul défaut dans le circuit. Ainsi, une étude plus poussée traitant du cas des défauts multiples serait d'un grand intérêt pour rendre ces méthodologies plus rigoureuses. La probabilité de rencontrer plusieurs défauts dans le circuit est réelle dans le cas d'une production à grande échelle. Le deuxième point qu'il serait aussi très intéressant d'explorer dans des travaux futurs est une caractérisation de la sensibilité de la quantité moyenne de puissance dissipée localement ou globalement dans le circuit par rapport aux variations des différents éléments. Ainsi on pourrait déterminer par exemple la variation de la densité de puissance dissipée par un composant lorsqu'elle varie autour de sa valeur nominale. Cette caractérisation combinée avec les méthodologies présentées devrait aider à augmenter de manière assez efficace le dictionnaire de pannes dans le cas des circuits intégrés hautes fréquences. Le troisième point à développer dans le but de rendre notre analyse plus performante est une compaction sous forme de base de données accessible en temps réel durant le test des circuits. Concernant le circuit tampon proposé dans le cadre de l'amélioration de l'interface de test, il serait très intéressant de le

réaliser avec une technologie disposant de transistors de types n et p complémentaires. La non complémentarité des transistors de type p et n limite considérablement la vitesse du circuit tampon et par conséquent de l'interface.

En s'attaquant aux problèmes de la testabilité des circuits intégrés hautes fréquences, cette thèse se veut comme pionnier dans la recherche de solutions efficaces, fiables dans le domaine du test hautes fréquences.

ANNEXE I

NOTION DE SENSIBILITÉ

La sensibilité est un concept très utilisé dans la conception de circuit, elle donne une vue interne des relations liant les paramètres d'un circuit et sa performance.

- La sensibilité permet au concepteur de bien comprendre comment les paramètres peuvent affecter la performance et aussi le rendement.
- La sensibilité peut être utilisée dans le choix de différentes structures de circuits qui ont toutes la même performance nominale.
- La sensibilité est utilisée dans l'optimisation pour déterminer les gradients de performance.

Sensibilité Classique

La plus simple et plus utilisée définition de la sensibilité est la dérivée de la performance, $G(P)$, associée à un paramètre donné p_i

$$S_{p_i}^G = \frac{\partial G(P)}{\partial p_i}$$

Cette formule mesure la sensibilité de variation de la performance à la plus petite variation du paramètre p_i .

On normalise la sensibilité pour enlever l'influence des valeurs du paramètre et de la performance sur la valeur de la sensibilité. La sensibilité normalisée est alors:

$$SN_{pi}^G = \frac{\partial G}{\partial pi} \cdot \frac{pi}{G}$$

Ainsi, on peut interpréter la sensibilité plus simplement: si $SN_{pi}^G = +2$, alors un changement de 1% de la valeur du paramètre implique un changement de +2% de la performance. De ce fait, les paramètres qui possèdent une sensibilité faible, n'influent pas sur la variation de la performance. Dans un contexte de fabrication, ces paramètres n'ont pas besoin d'être bien contrôlés. Au contraire, les paramètres dont la sensibilité est élevée, sont dits critiques pour la performance. Dans le processus de fabrication, ces paramètres doivent être soigneusement contrôlés en réduisant leur sensibilité par des changements dans le design ou la fabrication.

ANNEXE II

S-PARAMETERS

By far the most accurate and conveniently measured microwave two-port parameters are the scattering parameters. These parameters completely and uniquely define the small signal gain and the input/output emittance properties of any linear two-port network. Simply interpreted, the scattering parameters are merely insertion gains, forward and reverse, and reflection coefficients, input and output, with the driven and non-driven ports both terminated in equal impedances; usually 50 ohms, real. This type of measurement system is particularly attractive because of the relative ease in obtaining highly accurate 50 ohms measurement hardware at microwave frequencies.

Proceeding more specifically, S-parameters are defined analytically by:

$$b_1 = S_{11} a_1 + S_{12} a_2$$

$$b_2 = S_{21} a_1 + S_{22} a_2$$

or, in matrix form,

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

where (referring to Figure II.1):

$$a_1 = (\text{Incoming power at Port 1})^{1/2}$$

$$b_1 = (\text{Outgoing power at Port 1})^{1/2}$$

$$a_2 = (\text{Incoming power at Port 2})^{1/2}$$

$$b_2 = (\text{Outgoing power at Port 2})^{1/2}$$

E_1, E_2 = Electrical Stimuli at Port 1, Port 2

Z_0 = Characteristic Impedance = $(50 + j0)$ Ohms

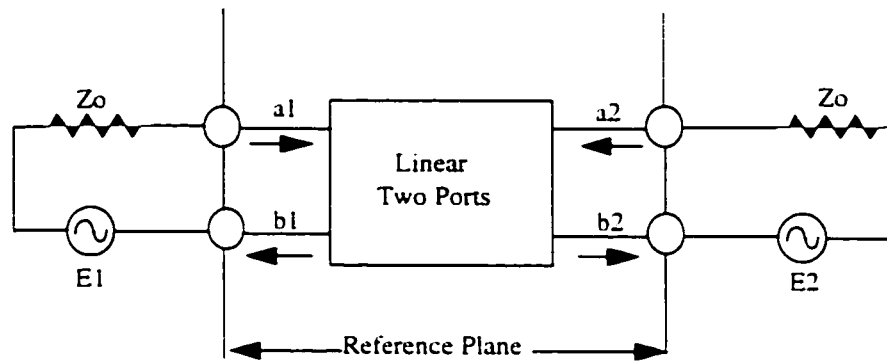


Figure II.1 S-Parameters Definition Schematic

From Figure 1 and defining linear equations for $E_2 = 0$, then $a_2 = 0$, and:

$$S_{11} = \frac{a_1}{b_1} = [\text{Outgoing input power}/\text{Incoming input power}]^{1/2}$$

S_{11} is considered as the ratio of the reflected voltage over the incident voltage. this ratio is commonly called Input reflection coefficients

$$S_{21} = \frac{a_2}{b_1} = [\text{Outgoing Input Power}/\text{Incoming Input Power}]^{1/2}$$

$$S_{21} = \frac{a_1}{b_1} = [\text{Forward Transducer Gain}]^{1/2}$$

or in the case of S_{21} :

$$\text{Forward Transducer Gain} = |S_{21}|^2$$

Similarly at Port 2 for $E_1 = 0$, $a_1 = 0$:

$$S_{12} = \frac{b_1}{a_2} = [\text{Outgoing Input Power/Incoming Output Power}]^{1/2}$$

S_{12} is called Reverse Transducer Gain.

$$S_{22} = \frac{b_2}{a_2} = [\text{Outgoing Output Power/Incoming Output Power}]^{1/2}$$

S_{22} is called Output Reflection Coefficient.

Since many measurement systems actually "read out" the magnitude of S-parameters in decibels, the following relationships are particularly useful:

$$|S_{11}| \text{ dB} = 10 \log |S_{11}|^2 = 20 \log |S_{11}|$$

$$|S_{22}| \text{ dB} = 20 \log |S_{22}|$$

$$|S_{21}| \text{ dB} = 20 \log |S_{21}|$$

$$|S_{12}| \text{ dB} = 20 \log |S_{12}|$$

Using scattering parameters, it is possible to calculate the reflection coefficients and transducer gains for arbitrary load and source impedance where the load and source impedances are described by their reflection coefficients Γ_L and Γ_S respectively:

$$\begin{aligned} S_{11} &= \frac{b_1}{a_1} = \frac{S_{11}(1 - S_{22}\Gamma_L) + S_{21}S_{12}\Gamma_L}{1 - S_{22}\Gamma_L} \\ &= S_{11} + \frac{S_{21}S_{12}\Gamma_L}{1 - S_{22}\Gamma_L} \end{aligned}$$

Transducer Power Gain = [Power Delivered to Load/Power Available from Source]

$$\begin{aligned} &= \left| \frac{b_2}{b_S} \right| (1 - |\Gamma_S|^2)(1 - |\Gamma_L|^2) \\ &= \frac{|S_{21}|^2(1 - |\Gamma_S|^2)(1 - |\Gamma_L|^2)}{|(1 - S_{11}\Gamma_S)(1 - S_{22}\Gamma_L) - S_{12}S_{21}\Gamma_L\Gamma_S|} \end{aligned}$$

ANNEXE III

TRANSMISSION LINE CHARACTERIZATION

When discussing transmission lines one should reflect on the following definition. A transmission line is two or more conductors separated by some insulating medium, used to carry a signal. At first glance this seems rather trivial, upon closer examination one finds a host of physical nuances which make the transmission line a sophisticated element to describe, among which are:

- Line resistance present in any non-ideal conductor.
- Line conductance ($(1/R) = G$) present in any non-ideal insulating medium resulting in leakage currents.
- Line inductance present in any current carrying conductor undergoing a change in magnetic flux.
- The line capacitance present between the two conductors separated by the insulating medium.

Figure III.1 shows the model of a transmission line. The circuit consist of two series elements (Z, L) and two shunt elements (C, G). The line has characteristic inductance and capacitance per unit length.

L and C are frequency dependent components of the line. For frequency above approximatively 100KHz, Z_0 , the charateristic impedance of the line, is equal to the square

root of L/C and is independent of the line length. The propagation constant (t_{pd}) or time delay constant is the square root of $L \cdot C$, and is a function of the length.

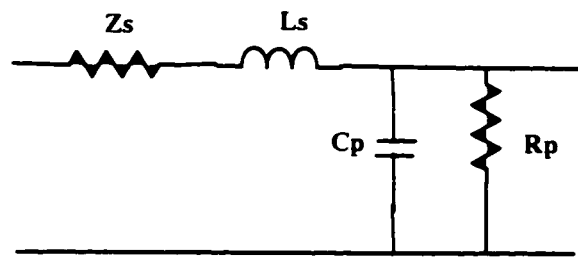


Figure III.1: Transmission Line Circuit

Transmission Line Reflections

Reflections on a line are caused by mismatch in between the line and the load. If all the power delivered to the line is absorbed by the load then there will be no reflected power back at the source side of the line. Figure III.2 represents a transmission line connected to a source which presents an impedance of Z_s . The transmission line is also loaded with an Z_l impedance.

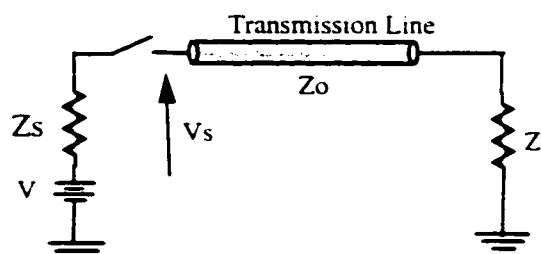


Figure III. 2: Transmission Line

The current delivered to the load is $I_L = I_{INC} - I_{RFL}$ (incident current minus reflected current), while the load voltage is, $V_L = V_{INC} + V_{RFL}$ (incident voltage plus reflected voltage). We need to find an equation that relates incident voltage to reflected voltage. Therefore noting that the load current $I_L = (V_{INC} - V_{RFL})/Z_o$ (incident voltage minus reflected voltage divided by the characteristic impedance) we can see the following relationship.

$$\frac{V_{INC} + V_{RFL}}{Z_L} = \frac{V_{INC} - V_{RFL}}{Z_o}$$

Solving for V_{INC}/V_{RFL}

$$Z_o(V_{INC} + V_{RFL}) = Z_L(V_{INC} + V_{RFL})$$

$$V_{RFL}(Z_o + Z_L) = V_{INC}(Z_L - Z_o)$$

$$\frac{V_{RFL}}{V_{INC}} = \frac{Z_L - Z_o}{Z_L + Z_o} = \Gamma_L$$

This expression is called the load reflection (Γ_L). Note a Γ_s also exists which relates the ratio of source impedance to the line impedance. This expression is called the source reflection coefficient and is shown in the following equation

$$\Gamma_s = \frac{Z_s - Z_o}{Z_s + Z_o}$$

One can see that there are three distinct possibilities which require inspection. First, the situation where the load impedance equals the line impedance ($Z_L = Z_o$) and $\Gamma_L = 0$ (no reflections- a properly terminated line); second, where the load impedance is greater than the line impedance $Z_L > Z_o$ and Γ_L is positive, generating a reflection whose polarity matches that of the incident voltage, and finally, where the load impedance is less than the

line impedance and Γ_L is negative, generating a reflection whose polarity is opposite to that of the incident voltage. Let's take a closer look at the last two cases.

Assume that $Z_L = 4Z_0$, and that the source impedance = line impedance. V = source voltage, and V_L = load voltage (see figure III.3).

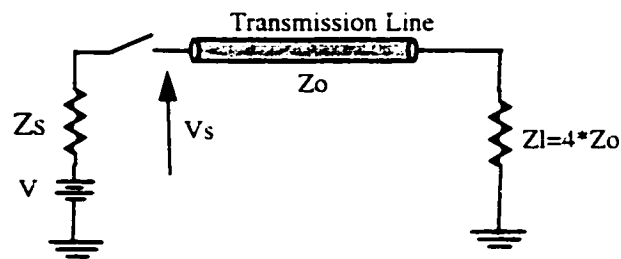


Figure III.3: Transmission Line circuit with $Z_L = 4Z_0$ and $Z_s = Z_0$

Thus at $t=0$ a voltage wave of $1/2(V)$ (because Z_s and Z_0 from a voltage divider on V) begins to travel down the line and arrives at Z_L one tpd or propagation delay later. When the wave encounters the load impedance mismatch, a reflected wave equal in magnitude to $(V/2) \cdot 0.6$ is reflected back toward the source, and arrives at the source, again one tpd later. This cause the voltage at the source to rise therefore creating classic overshoot condition.

Since the source and the line impedance are matched no further reflections are generated and the line has reached its steady state condition. See figure III.4

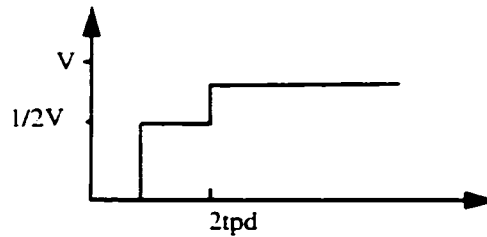


Figure III.4: Voltage versus Time Plot of $Z_L = 4Z_0$ and $Z_s = Z_0$

The next scenario is when $Z_L < Z_0$. For this case assume the following conditions. See figure III.5. we will have $\Gamma_L = -0.6$

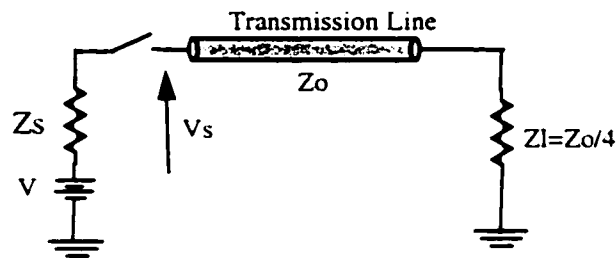


Figure III.5: Transmission Line Circuit $Z_L = Z_0/4$ and $Z_s = Z_0$

At time $t=0$ a voltage wave equal in magnitude to $1/2V$ begins to travel down the line arriving at the load one delay time later. The impedance mismatch generates a reflected wave equal in magnitude to the reflected wave discussed in the first example, but opposite in polarity. At time $2tpd$ this wave reaches the source and sums with the existing voltage present from $t=0$ ($V/2$), reducing its value to $(Vs/5)$, or $((V/2)-0.6)+V/2$. This is classic undershoot condition See Figure III.6.

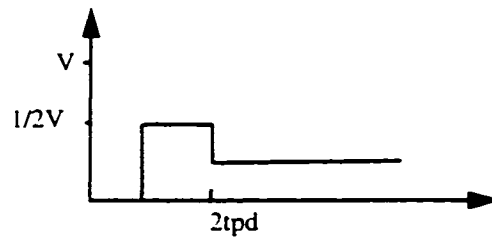


Figure III.6: Voltage versus Plot of $Z_L = Z_0/4$ and $Z_s = Z_0$

At this point we need to reflect on one of the equations described earlier. The equation states that $V_L = V_{INC} + V_{RFL}$. We can see this holds true as noted in the preceding examples, where V_L and V_s either increased or decreased with the corresponding mismatches in impedance.

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