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POLYTECHNIQUE MONTRÉAL
affiliée à l'Université de Montréal

Contact interface engineering and thermal stability of direct-conversion CdZnTe X-ray detectors

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Mémoire présenté en vue de l'obtention du diplôme de *Maîtrise ès sciences appliquées*
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Ce mémoire intitulé :

Contact interface engineering and thermal stability of direct-conversion CdZnTe X-ray detectors

présenté par **Luc MONTPETIT**
en vue de l'obtention du diplôme de *Maîtrise ès sciences appliquées*
a été dûment accepté par le jury d'examen constitué de :

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RÉSUMÉ

L'adoption de la modalité d'imagerie médicale par tomographie calculée (CT) a permis, dans les dernières décennies, une révolution au niveau des processus de diagnostics. En effet, la reconstruction 3D des corps acquis permet non seulement une haute précision morphologique, mais offre également aux cliniciens des informations compositionnelles critiques. Malheureusement, les hauts dosages de rayons X nécessaires à l'obtention d'images de qualité limitent l'utilisation à grande échelle de cette modalité, étant donné les risques prévalents de complications associées aux radiations. L'utilisation de détecteurs à conversion directe afin de remplacer les détecteurs courants à base de scintillation promet de réduire les doses de radiation nécessaires à l'obtention d'images précises, en permettant le comptage de photons (PC) et d'obtenir l'information spectrale d'absorption. Les semiconducteurs à base de CdZnTe (CZT) sont à l'avant-garde des technologies de PC, dus à leur potentiel d'offrir un signal à haute résolution et faible bruit, conféré par leur numéro atomique élevé, leur haut niveau d'interaction avec les photons à haute énergie, et leur large résistivité intrinsèque. Malgré les qualités prometteuses pour le PC et l'implémentation au sein des scanners CT, maints défauts découlant du procédé de croissance du CZT, de sa manutention, ainsi que de la fabrication des détecteurs, doivent encore être optimisés. Les défauts au sein du cristal de CZT, tels que les inclusions de Te et les dislocations, en plus des défauts inhérents à la fabrication des détecteurs, tels que les états de surface et dislocations d'interface, agissent comme centres de génération de charges et de recombinaison de paires électron-trou, augmentant le courant noir et limitant, par le fait même, la collection des charges sous radiation. Ce projet tend alors à améliorer les détecteurs à radiation à base de CZT par le biais de l'ingénierie d'interface, afin d'obtenir des dispositifs avec un faible courant noir. Du coup, il tend également à comprendre les facteurs influençant ce dernier.

En premier lieu, un procédé de fabrication de détecteurs à base de CZT a été développé afin d'obtenir de manière répétable des dispositifs de haute qualité, permettant ainsi de mener les études subséquentes sur les méthodes de fabrication et de passivation. Les méthodes retenues évitent notamment les techniques de gravure purement chimiques, dans le but de préserver la stœchiométrie des surfaces. La stabilité thermique desdits détecteurs a été évaluée afin de déterminer les facteurs limitants lors des différentes étapes de fabrication desdits détecteurs. Des détecteurs à base de CZT et d'or, comprenant une électrode par dépôt autocatalytique pour un contact ohmique et une autre électrode déposée par faisceau d'électrons pour un contact Schottky, ont été utilisés. Ils ont été soumis à des séquences de recuit sous un vide

de 1.2×10^{-5} torr à des températures allant de 373 K à 623 K. Les temps de recuit ont été maintenus constants entre 60 et 70 minutes, en variant le temps d'approche. Les caractéristiques électriques des détecteurs, à chaque étape, ont été mesurées par des balayages courant–voltage. Les détecteurs ont démontré des performances stables jusqu'à des recuits à 473 K, après quoi une détérioration marquée des performances a été observée, simultanément à un changement soudain du mode de conduction. Notamment, une augmentation du courant noir en sous-biais négatif a été observée, accompagnée de larges fluctuations de courant. Ainsi, l'état des surfaces et des interfaces entre le CZT et l'or déposé par faisceau d'électrons a été investigué par TEM, XPS et AFM. Bien qu'aucune modification morphologique à l'interface n'ait été observée, une accumulation de Zn à la surface des électrodes ainsi que du CZT, couplée à une zone de déplétion en Zn directement sous les électrodes, a été mesurée. Ces changements de composition sont plausibles de causer une décroissance de la barrière Schottky ainsi qu'une augmentation du biais d'interface, menant à une baisse des performances électriques. Or, l'impact du changement de composition est couplé à une variation inhérente de l'épaisseur de la couche interfaciale ainsi que de la densité d'états d'interface, dont les effets sont similaires. Des changements significatifs au niveau de la morphologie des surfaces d'électrodes ont également été notés, notamment une croissance d'un ordre de grandeur de la rugosité des contacts.

En second lieu, des dispositifs visant à réduire la proéminence des sources de courant noir, notamment les surfaces et interfaces, ont été développés. À la lumière des résultats, le SiN_x déposé par pulvérisation cathodique RF, ne nécessitant aucun apport thermique externe, a été utilisé pour concevoir des structures de dispositifs destinées à passiver les défauts de surface et à accroître la barrière Schottky effective, limitant ainsi l'injection parasitaire de charges. Les deux stratégies développées ont montré une amélioration marquée du courant noir, en particulier pour les dispositifs fabriqués sur du CZT présentant une rugosité plus élevée. Ces améliorations sont cohérentes avec la passivation des états de surface et des terminaisons non liées par la couche diélectrique. Pour les dispositifs intégrant une couche de passivation uniquement entre les électrodes, les courants de surface ont été largement réduits, bien que le courant noir global n'ait présenté qu'une réduction modeste. À l'inverse, les couches interfaciales d'amplification de barrière, d'épaisseur comprise entre 3 nm et 10 nm, ont systématiquement généré une réduction du courant noir sous polarisation négative comme positive. En revanche, les couches diélectriques plus épaisses n'ont pas montré d'amélioration par rapport aux couches plus minces, un effet attribué au claquage diélectrique. Ainsi, on estime que les sources principales de courant noir dans les dispositifs sont dominées par l'injection de charges à l'interface ainsi que par les effets de bulk. De plus, les disposi-

tifs intégrant des couches diélectriques plus épaisses présentaient une limitation accrue du transfert de charges aux interfaces en raison des effets capacitifs, soulevant des préoccupations quant à une polarisation excessive des détecteurs sous bias, menant à une réduction du champ électrique interne. La qualité du SiN_x déposé semble avoir un impact significatif sur la performance des dispositifs. Une augmentation des courants de surface après dépôt des couches interfaciales suggère la formation de chemins de fuite à l'intérieur même du diélectrique, menant possiblement à un claquage diélectrique et à une diminution des performances. Néanmoins, ce travail propose un cadre de recherche prometteur pour améliorer la performance des détecteurs à rayonnement à base de CZT en réduisant le courant noir. Il met également en évidence la nécessité de développer adéquatement les procédés de dépôt des diélectriques afin de minimiser les effets indésirables.

ABSTRACT

The widespread adoption of computed tomography (CT) for medical imaging has drastically transformed the diagnostic process in modern medicine. The 3D reconstruction provides insightful information regarding the composition and morphologies of the patients. However, the incidental X-ray dose absorbed by patients during scans remains high in order to achieve high-quality images, increasing the prevalence of complications associated with repeated exposure. The use of optimized direct-conversion detectors to replace current scintillator-based X-ray detectors has been proposed as a promising solution to reduce X-ray doses, leveraging their photon-counting (PC) capability to obtain spectroscopic information along with attenuation data to generate high-quality images. CdZnTe (CZT) has been shown to be a promising material for X-ray detection due to its potential to deliver low-noise, high-resolution signals, owing to its high atomic number, strong photon-matter interaction, and high intrinsic resistivity. Despite the attractive intrinsic properties of CZT for the fabrication of PC detectors and their implementation in PC CT, several challenges inherent to the growth, processing, and fabrication of detectors remain to be solved. Extended bulk defects such as Te inclusions and dislocations, as well as processing-related defects such as surface states and interface dislocations, act as generation centres for dark current and electron-hole pair recombination, thus limiting charge collection efficiency and increasing background current. This work focuses on improving CZT radiation detectors through interfacial engineering to achieve low-background-current devices, and on understanding the factors influencing it thereof.

First, a device processing protocol was developed to ensure consistent and repeatable detector performances, enabling further comprehensive studies in the aftermath. the process avoided the used of chemical etching solely to maintain surface stoichiometry. It further used a lift-off process to optimize the deposited electrode's resolution. The thermal stability of these detectors was evaluated to assess the available thermal budget during the fabrication process flow. CZT detectors comprising a metal–semiconductor–metal structure; one electroless Au contact and one rectifying e-beam deposited Au contact, were sequentially annealed in vacuum at 1.2×10^{-5} Torr at increasing temperatures from 373 K up to 623 K. The annealing times were maintained constant between 60 and 70 minutes for all steps, while the ramp-up rate was varied. Current–voltage characteristics were measured after each annealing temperature. The detectors were found to exhibit stable performance up to 473 K, beyond which performance deterioration and changes in conduction mechanisms were observed. Specifically, the reverse-bias dark current increased, alongside larger current fluctuations, after annealing at

523 K. Simultaneously, the surface and interfacial properties of the Au–CZT contact were investigated by TEM, XPS, and AFM before and after all step. Although no morphological changes were observed at the interface, Zn enrichment was measured atop the pixels and CZT surface, accompanied by a Zn-depletion zone at the interface. These compositional changes are thought to drive a decrease in effective barrier height and an increase in interfacial voltage drop, although their impact cannot be dissociated from the effects of interfacial layer thickness and interface state density. Significant morphological changes were also noted atop the e-beam electrodes, including an order-of-magnitude increase in surface roughness.

In light of these results, devices aimed at reducing prominent sources of dark current, notably stemming from surface and interface, were developed. Leveraging SiN_x dielectric deposited by reactive RF magnetron sputtering, requiring no external substrate heating, three detectors were designed to passivate surface defects and states, as well as enhance the blocking behaviour of Schottky contacts to minimize carrier injection. Both engineering strategies exhibited effective dark current reduction, notably in detectors fabricated on CZT with higher surface roughness and presumed lower material quality. These improvements are consistent with the passivation of surface defects and dangling bonds. For devices with interpixel passivation, the surface leakage current was largely reduced, while the total dark current showed no notable reduction. On the other hand, barrier enhancement layers, whoms thicknesses spanned from 3 nm to 10 nm, produced systematic reductions in dark current under both forward and reverse bias, although increased dielectric thickness did not consistently lead to improved performance, likely due to dielectric breakdown. The dark current is thus thought to be primarily dominated by interface carrier injection and bulk-related mechanisms. However, devices with additional dielectric layers also showed enhanced interfacial charge trapping due to capacitive effects, raising concerns about detector polarization under prolonged bias and reduced electron-hole pair collection. Furthermore, the dielectric quality seems to limit the device performance. Indeed, the deposition of interfacial barrier layers led to increased surface leakage current, suggesting the formation of leakage pathways that facilitate dielectric breakdown and performance degradation. Nonetheless, these results provide a promising framework to improve CZT detector performance by reducing dark current through surface and interface passivation, but they also highlight the need to thoroughly engineer dielectric deposition processes to eliminate adverse effects.

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LIST OF SYMBOLS AND ACRONYMS

AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
CMP	Chemical Mechanical Polish
CT	Computed Tomography
CVD	Chemical Vapour Deposition
CZT	Cadmium Zinc Telluride, CdZnTe
DQE	Detective Quantum Efficiency
FIB	Focused Ion Beam
FPXI	Flat Panel X-ray Imaging
IPA	Isopropyl Alcohol
ITD	Interfacial Thermionic Diffusion
MIS	Metal-Insulator-Semiconductor
MP	Mechanical Polish
MRI	Magnetic Resonance Imaging
MSM	Metal-Semiconductor-Metal
PCCT	Photon-Counting Computed Tomography
PCD	Photon-Counting Detector
RIE	Reactive Ion Etching
RMS	Root Mean Square
RPM	Rotation per Minute
SEM	Scanning Electron Microscope
SLC	Surface Leakage Current
SMU	Source Measure Unit
SNR	Signal-to-Noise Ratio
TEM	Transmission Electron Microscope
THM	Travelling Heater Method
XPS	X-ray Photoelectron Spectroscopy

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CHAPTER 1 INTRODUCTION

Modern medical imaging has transformed diagnostics by revealing the internal structures of the body with remarkable clarity. Driven by the need to ever-improve diagnostic accuracy, methods and tools have been the focus of intense research in both academic and industrial sectors. Among those, computed tomography (CT) has remained at the forefront due to its operational flexibility and ease of implementation, notably compared to modalities such as magnetic resonance imaging (MRI). This imaging modality enables 3D reconstruction of the imaged body by acquiring a set of angular perspectives using X-rays, which can later be stitched together to obtain a complete view. This addition of frames is the main drawback to CT imaging. Indeed, radiation doses can reach a staggering 11 mSv [16, 17] for a 3D trunk image, more than two orders of magnitude larger than what is required for planar X-ray imaging (FPXI) of the same structure [17, 18]. As such, repeated CT scans on singular individuals have been shown to increase the prevalence of brain cancer and leukemia in otherwise healthy patients. [16, 19, 20]. These clinical studies highlight the need to limit radiation exposure to warrant the widespread implementation of CT imaging, while still obtaining high-quality images for accurate diagnostics.

While several aspects of CT can be optimized, much of the current focus is directed towards advancing radiation detector technology to meet the demands of next-generation CT scanners. Conventional systems implement indirect radiation detectors by coupling scintillator to Si photodiodes [18]. Although these detectors offer a relatively high detective quantum efficiency (DQE), non-collimated scattering events as well as the isotropic scintillation process lead to low image contrast and notable artifacts [18, 21]. Furthermore, due to the intermediary scintillation step, these detectors work by integrating the energy spectrum, which can then be translated to the linear attenuation coefficient of each imaged voxel, and ultimately to the CT number (in units of Hounsfield) [18]. Dual-energy CT has demonstrated improved material discrimination by linear combination of the CT numbers at both energies; however, this approach often requires higher radiation dose [19]. This raises the question: What if one could extract all the spectral information with just one scan? This is the feat that photon counting CT (PCCT) achieves.

PCCT relies on direct conversion detectors. Instead of converting radiation into light and then into electrical current, these detectors, also referred to as solid state detectors, absorb

the incident radiation via the photoelectric effect and generate electron hole pairs, which can be collected under an applied electric field to produce a current [6, 22, 23]. From the known electron-hole pair creation energy of the photon counting detector (PCD) compound, the number of incident photons at each energy of the spectrum can be counted [22, 24–27], thereby providing spectroscopic information alongside attenuation information at several energy bins. From the attenuation curves of various materials, the attenuation at multiple energy bins can be measured, and a linear combination, with or without energy weighting, of the CT numbers can be performed to obtain detailed information about the imaged body [18, 19, 28, 29]. PCDs further offer other advantages. Notably, energy discrimination allows for the minimization of the effects of Compton scattered photons by setting a minimum energy threshold, thereby reducing the need for extensive collimation that would otherwise distort the signal [18]. Moreover, these detectors offer superior spatial resolution due to minimized pixel crosstalk and the possibility of designing smaller pixels without loss of geometric efficiency [19]. The sampling rate can also be improved due to the absence of scintillator afterglow, enabling high flux operation [19, 21]. PCDs are also capable of correcting for beam hardening [18, 19]. The synergistic effects of these advantages enable PCDs to lower the noise floor and better detect low-energy photons, where contrast is highest, thus supporting low-dose operation of PCCT [18, 19, 30].

Material quality is paramount to achieve the feat aforementioned. Several material characteristics are required to optimize the photon-counting capability of the detectors [22]. First, the material compound should present a high atomic number to achieve high radiation absorption, and a high photoelectric effect in the X-ray imaging range of 10-150 keV [31]. Second, the material should have a bandgap such that the energy required for electron-hole pair generation is 5 eV or less, in order to generate a large number of electron-hole pairs per interaction. Yet, it should be large enough to minimize thermal carrier at equilibrium and dark current [23]. Third, the material should present a high mobility-lifetime product ($\mu\tau$) such that the drift length is sufficiently high to ensure collection of the photogenerated carriers and high frequency operation. Fourth, the material should be homogeneous to ensure consistent performance across devices. Several semiconductors and compound semiconductors have attracted interest; Si, Ge, GaAs, a-Se, HgI_2, TIBr, CdTe, and its ternary alloy CdZnTe [23, 24]. However, many present inherent physical setbacks that prevent their implementation in PCCT; low attenuation coefficient at high energies (a-Se, Si) [21, 23], high dark current (Ge) or low-carrier mobility (GaAs, HgI_2, TIBr).

CdTe and CdZnTe (CZT) have been at the forefront of the candidates for direct conversion.

Despite their moderate $\mu\tau$ product, and especially the discrepancy between both electron and hole mobilities, these II-VI alloys present an attractive combination of high atomic number, high density, and wide bandgap [22,24,25]. As such, detectors fabricated using these compounds can be operated at room temperature due to their intrinsically low dark current. By alloying Zn within the CdTe matrix, CZT exhibits a higher bandgap, resulting in higher resistivity and lower dark current. These come at the expense of hole mobility [24]. More importantly, the addition of Zn inhibits bias-induced polarization of the detectors, which leads to degraded spectroscopic performance [32]. Regardless of their potential, the widespread adoption of CdTe and CZT as PCDs has suffered many setbacks inherent to bulk material growth and processing: Te precipitation, dislocation networks, twin grain boundaries, and deep-level defects [22, 33, 34]. In spite of these defects, two commercial CdTe-based PCCT systems had been cleared for clinical application by the FDA as of 2022, with four CZT-based systems at the advanced prototype demonstration stage [28]. Although these recent implementations exhibit the great potential of these alloys, they are likely attributed to large advancements in electronic readout circuits. Several engineering challenges pertaining to material growth, processing, and subsequent detector fabrication and design remain in order to unlock the alloy's complete potential.

Objectives

While significant progress has been made in material growth and readout electronics, further improvements in device performance will rely heavily on advancements in post-growth processing and detector design. Addressing issues such as high dark current and poor interfacial properties is essential for enabling high-quality, low-dose imaging. This work, therefore, aims at developing device processing techniques tailored to improve the performance of CZT detectors in CT applications. Alas, the range of available processing techniques has been reported to be limited by the low thermal budget of CZT, particularly of fabricated detectors. Albeit, the latter has been the subject of contradictory reports. Thus, understanding the available thermal budget is paramount to extending the range of detector fabrication techniques available to us. In light of these results, a specific process can be developed to enhance the performance of the detectors by reducing their dark current. The specific objectives are

1. Develop an in-house CZT detector processing protocol,
2. Outline the impact of thermal treatment on the electrical performance and the metal-semiconductor interface to determine the optimal thermal budget of fabricated detectors,

3. Improve device structures to reduce the dark current, permitting increased signal-to-noise (SNR) ratio operation.

These objectives are considered in chapter 3, chapter 4 and chapter 5 respectively. First, the fundamentals of detector physics, including interface formation, sources of background current and notable defects are discussed, concluding with a complete conduction mode. The implementation of CZT as a direct conversion radiation detector is further outlined in section 2. Then, chapter 3 overviews several of the techniques and tools developed to fabricate and characterize detectors used to complete the following objectives, and culminates with a comprehensive fabrication process flow. Finally, chapter 6 summarizes the work completed and proposes future research directions to address the shortcomings of the present work.

CHAPTER 2 LITERATURE REVIEW

Several metrics are used to quantify the performance of radiation detectors. Among these, the detective quantum efficiency (DQE) is particularly important, as it ultimately governs the performance of an imaging system [23, 25]. This project focuses on improving the SNR of CZT detectors and understanding the factors that influence it. These two metrics can be directly related, knowing a system's input $\mathrm{SNR_{in}}$ [18]

$$\mathrm{DQE} = \left(\frac{\mathrm{SNR_{out}}}{\mathrm{SNR_{in}}}\right)^2. \tag{2.1}$$

While other performance metrics are occasionally discussed in relation to their impact on SNR, they are considered outside the primary scope of this work.

Regardless of the apparent advantage of CZT radiation detectors over their scintillation counterparts, their intrinsic noise level should be minimized to optimize image quality. Indeed, the final image quality is highly reliant on the detector's SNR [18]. The signal's contrasts, C, is given by

$$C = \frac{I_s - I_b}{I_b}, \tag{2.2}$$

where I_s is the signal strength and I_b is the background signal strength. If σ_b is the noise standard deviation in the background, the SNR can be calculated as

$$SNR = \frac{CI_b}{\sigma_b} = \frac{I_s - I_b}{\sigma_b} = C\sqrt{N_b}, \tag{2.3}$$

where N_b is the number of incident photons. This relation works because the charge collection is discrete and follows a Poisson distribution, such that $I_b = \sigma_b^2$ [18]. Whilst increasing the incident photon flux would improve the SNR, it goes against the purpose of implementing next-generation scanners, leading to an increase in required radiation dosage to achieve high-quality images. Equation (2.3) suggests a synergetic effect between a detector's contrast and its SNR. Inherently, reducing the background signal leads to an image improvement in both contrast and SNR.

This literature review outlines the fundamental concepts pertaining to the background current generation, as well as the photodetection process. First, section 2.1 discusses the process of background current, generally referred to as dark current. The latter generally stems

from a combination of two processes, namely thermal current generation, outlined in section 2.1.1, and from carrier injection [23] arising from the interface formation; discussed in 2.1.2. The impacts of defects are discussed in relation to their effect on dark current generation. Second, direct-conversion CZT detectors are discussed in section 2.2. Notably, the process by which charge carriers are generated is shown in 2.2.1, followed by a review of the state of CZT radiation detectors. Although improvement to the CNR would be possible through a reduction of the background noise, sources of noise are intrinsic to electronic devices [35]. Among them, Johnson-Nyquist (thermal) noise typically dominates at room temperature. This continuous noise originates from particulate Brownian motion within the semiconductor, leading to a distribution of thermal energy and statistical carrier density fluctuations [35, 36]. The latter is followed by Shot noise, which is discontinuous. It originates from the quantization of charge carriers [37]. Nonetheless, the root of these noises pertains to the fundamental physics realm and can hardly be improved.

2.1 Conduction sources in Metal-Semiconductor devices: thermal currents and interface engineering

To contextualize the origins of background current in semiconductor detectors, this section outlines the intrinsic sources of conduction within the device. Emphasis is placed first on thermally induced charge carrier motion, followed by the role of contact interface formation. These mechanisms are examined in terms of their contribution to dark current and their relevance to overall detector performance.

2.1.1 Thermal agitation of charge carriers in semiconductors

Minimizing dark current is essential to improving detector performance, particularly in applications where reducing radiation dose is a priority. Since dark current arises even in the absence of illumination, its origin must be understood from a fundamental, material-level perspective. In semiconductors, this background conduction is partially attributed to thermally excited charge carriers. At non-zero temperatures, thermal agitation provides sufficient energy for electrons to overcome the bandgap, resulting in spontaneous electron-hole pair generation. This process sets a baseline current in all semiconductor devices, which directly contributes to noise and limits achievable SNR. The behaviour of these thermally generated carriers can be described using equilibrium band theory, statistical distributions, and basic transport relations, as illustrated in Figure 2.1a. The latter presents the theoretical equilibrium band alignment of a given undoped perfect semiconductor at room temperature.

The Fermi energy probability function

$$f_F(E) = \frac{1}{1 + \exp(\frac{E - E_F}{kT})}, \tag{2.4}$$

is also displayed alongside the intrinsic carrier concentration in each band, $n_i,\ p_i$. The Fermi energy E_F lies in the middle of the bandgap, halfway between the valence band energy E_v and the conduction band energy E_c. At room temperature, the statistical distribution of charge carriers follows a Fermi-Dirac probability function such that the electron and hole concentrations are, respectively [2]

$$n_i = N_C \exp(\frac{E_F - E_c}{kT}), \quad p_i = N_v \exp(\frac{E_v - E_F}{kT}), \tag{2.5}$$

after a Boltzmann distribution approximation. N_C and N_v are the effective density of states in the conduction and valence bands, respectively. The density of charge carriers in both bands is thus directly correlated to thermodynamic effects, with an increase in temperature leading to an increase in carrier concentration owing to a flattening of $f_F(E)$. For an applied electric field of ε, the drift current density within the semiconductor is

$$J_{\text{drift}} = e(\mu_n n + \mu_p p)\varepsilon, \tag{2.6}$$

where μ_n and μ_p are the electron and hole mobilities. Notwithstanding the impact of interfaces, the background current I_b (dark current) is therefore a result of the statistical energy distribution at non-zero temperatures.

The addition of defects and impurities within the crystal matrix has troublesome effects on the carrier dynamics within the devices. As shown in figure 2.1b, the addition of shallow donor-type and acceptor-type defects with energy levels mutually lying in the conduction and valence band distorts the Fermi-Dirac probability distribution by impacting the density of states in both bands. Accordingly, these defects are said to be carrier-generative, contributing to an increase in the electron and hole density, $n_d \geq n_i,\ p_d \geq p_i$. As a consequence of equation (2.6), the drift current under an applied electric field also increases. Moreover, the presence of ionized defects within the bandgap of the semiconductor (complete ionization of donor-type defects, as near-complete ionization of acceptor-type defects has been demonstrated theoretically [2, 6]) acts as carrier recombination centres, reducing the photocurrent under radiation. The sources of defects, in and out of the bandgap, are discussed in detail in section 2.2.2 alongside their impact on the photocollection efficiency.

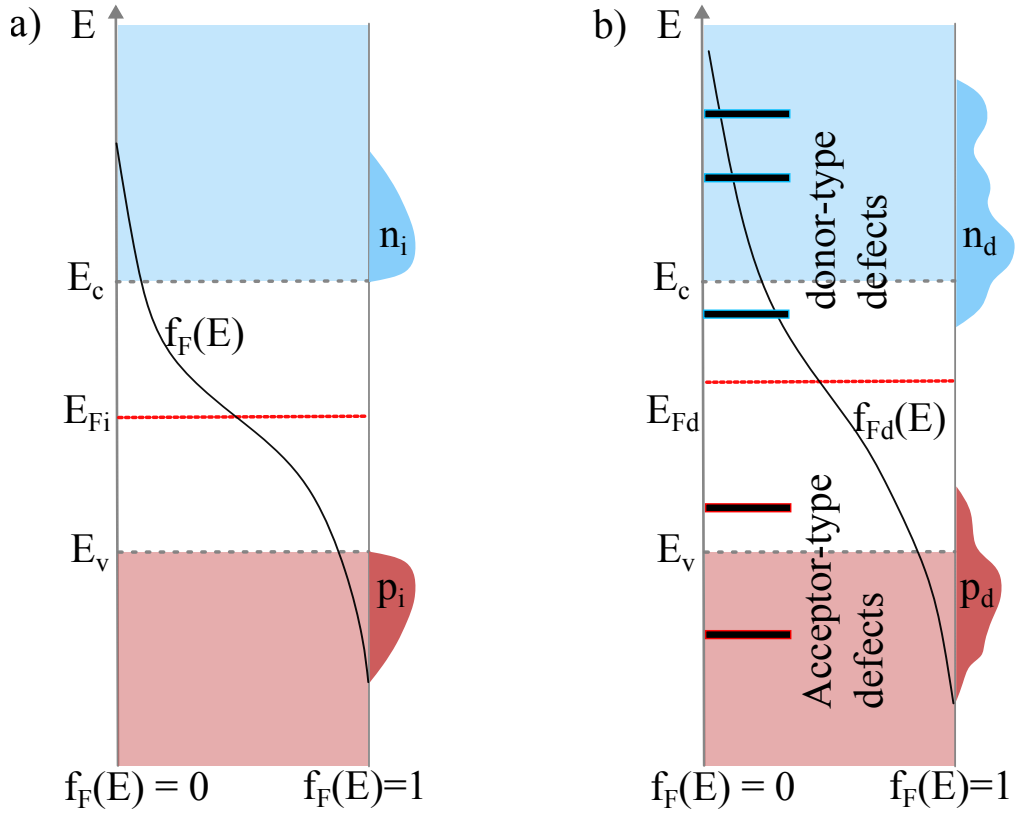

Figure 2.1 Band alignment, Fermi distribution and electron-hole carrier concentrations in a semiconductor in a)equilibrium, and b) with defects of both n-type and p-type. The addition of defects does not change the band structure, yet influences the Fermi distribution of carriers, and thus increases the respective concentration of electrons and holes in their respective bands. Figure inspired by [2].

2.1.2 Schottky contact formation and carrier transport mechanisms at metal-semiconductor interfaces

Detectors are commonly based upon the fabrication of p-n junctions (or p-i-n for increased efficiency), or of Schottky diodes. While p-n junctions typically offer better performance in detection efficiency due to the increased degrees of freedom in design, dopant implantation in bulk CZT wafers has been shown to be detrimental to the performance of detectors, particularly due to the added defects induced in implantation and annealing [38, 39]. Hence, most CZT radiation detectors consist of a Metal-Semiconductor-Metal (MSM) structure [22,24,25]. The latter further has the advantage of fabrication simplicity, as discussed in section 3.1. Let us first consider the formation of a singular metal-semiconductor interface. Consider a system

comprised of a metal with work function $e\phi_m$, and a semiconductor with valence band energy E_v and conduction band energy E_c such that its electron affinity is $e\chi$, its work function $e\phi_s$ and Fermi energy E_f. In equilibrium, before contact, the energy band diagram is shown in figure 2.2a.

After contact, the system establishes a new equilibrium without any potential applied. The Fermi levels align to maintain consistency in the system. To maintain the integrity of the semiconductor and metal's properties, the vacuum level changes; yet it must remain continuous. This effect leads to band bending of the semiconductor levels at the interface, as depicted in figure 2.2b for an n-type semiconductor. To maintain charge neutrality, negatively charged carriers flow to lower energy states in the metal. This effectively creates a depletion region of width W, whose width is intrinsically bounded by the built-in voltage V_{bi} and, subsequently, the applied voltage. $e\phi_n$ is the electron work function.

This depletion region is key to performant detectors as the generation of electron-hole pairs occurs in it. Not only does the presence of defects in the depletion region contribute to parasitic carrier generation, as shown in section 2.1.1, but they also serve as recombination centres for electron-hole pairs. At the interface, the barrier height is given by

$$e\phi_{B0} = e(\phi_m - \chi). \tag{2.7}$$

In principle, this equation holds true for ideal systems. Section 2.1.3 and 2.1.4 add complexity to this model to more accurately represent experimental conditions.

Detectors are commonly operated in reverse bias; that is, a negative potential is applied to the metal electrode [2]. Whereas the application of a positive bias narrows the depletion region, a negative bias widens it, optimizing the electrical conversion of incident photons, whilst maintaining a relatively low background current. A wider depletion region increases the active volume for photon absorption and enhances the internal electric field, which in turn accelerates the separation and collection of photo-generated carriers [6]; a process discussed in section 2.2.1. This reduces recombination losses and improves the quantum efficiency of the device. Additionally, the increased electric field lowers the junction capacitance, enabling faster detector response time. These characteristics make reverse-bias detectors particularly advantageous for applications where a high SNR is essential [6, 24].

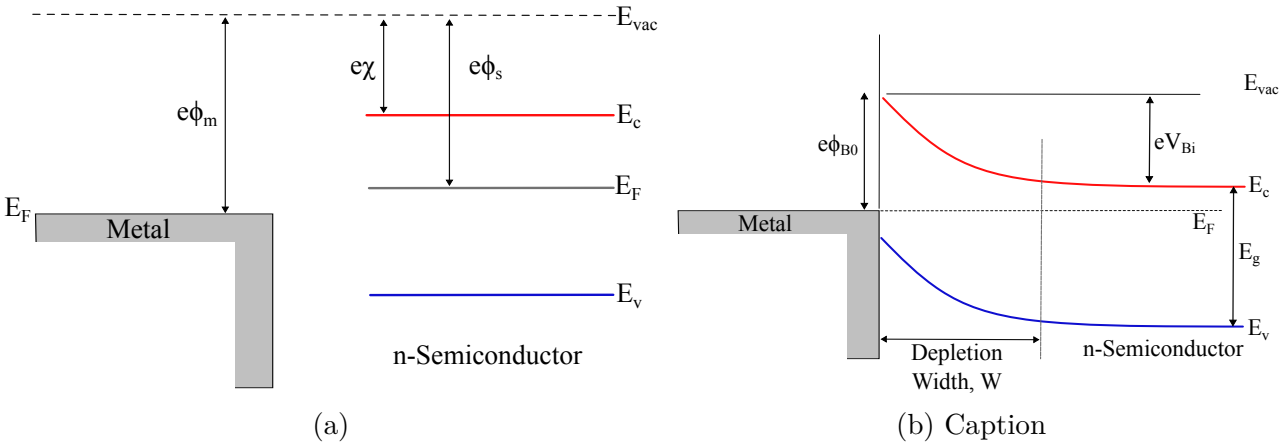

Figure 2.2 Energy band alignment of a n-type semiconductor-metal interface at a) equilibrium before contact, and b) at equilibrium after creating a Schottky junction. The Fermi levels align, creating a barrier height $e\phi_{B0}$ at the interface.

2.1.3 Interface states, surface states, and their impacts on detector performances

The presence of surface defects, not only inherent from the growth of the material as discussed in section 2.2.2, has detrimental effects on the performance of detectors. Such defects arise from the processing steps required to develop complete detectors. First and foremost, the dicing of wafers from source ingots induces a high density of defects at the surface [40]. Consequently, the wafers are generally polished to remove such a highly defective layer before anything meaningful can be done. While this lapping certainly reduces the density of defects, it also gives rise to other types of defects, whether it be due to pressure or strain in the lapping process [41]. Nonetheless, the polishing process has been shown to significantly improve the surface quality of CZT, as of all bulk semiconductor [40, 42]. Similarly to bulk defects (section 2.1.1), defects at the surface induce surface states, which modify the intrinsic DOS in the conduction band, valence band, and bandgap [2]. Moreover, the crystals' incomplete termination at the dicing points leads to the formation of dangling bonds, themselves considered surface states. These unterminated bonds further lead to a rehybridization of orbitals and to a surface structure rearrangement that causes strain effects, changing the surface energy of the substrates [43]. Regardless, the impact reinforces the notion that the surface should be considered distinct from the bulk of the material due to its unique properties. Their impacts can drastically change both the interfacial properties and behaviour, as well as the properties of the inter-electrode gaps. They may act as discrete energy generation-recombination centres, raising the background current levels and inhibiting the collection of electron-hole

pairs.

Interface states

The presence of a thin interfacial layer at the interface between the semiconductor and metal is generally considered accurate, given the reactive nature of the semiconductors with oxygen and current microfabrication processes [2, 5, 6]. Interface states are sandwiched between a semiconductor and the metal interface; defect states can overshadow any effects of the barrier height by inducing Fermi-level pinning. The effects occur when the density of interface states D_{it} is large. Figure 2.3 illustrates the position and impact of the interface states on the equilibrium semiconductor-metal band alignment (with image force lowering $\Delta\phi_0$). The energy of the states ϕ_{0a} is assumed to be an acceptor state. The relation between surface potential, n-type semiconductor bandgap and interface state energy can be shown to be

$$E_g - e\phi_{0a} - e\phi_{Bn} = \frac{1}{eD_{it}}\sqrt{2e\epsilon_s N_d(\phi_{Bn} - \phi_n)} - \frac{\epsilon_i}{eD_{it}\delta}\{\phi_m - (\chi + \phi_{Bn})\}. \tag{2.8}$$

where ϵ_s and ϵ_i are the semiconductor and interfacial layer's dielectric constants. Notably, for $D_{it} \to \infty$, the barrier barrier height

$$e\phi_{Bn} = \frac{1}{e}(E_g - e\phi_{0a}), \tag{2.9}$$

is independent of the metal work function. On the other hand, if $D_{it} \to 0$, equation (2.8) effectively collapses to equation (2.7). This phenomenon has been described as Fermi-level pinning. The presence of interface states has further implications on the carrier transport mechanisms, and is discussed in section 2.1.4

Due to the low electronegativity difference between Cd and Te, CZT is prone to Fermi-level pinning alongside III-IV compounds and group IV semiconductors [5]. Consequently, interfaces and surface processing steps should be thoroughly optimized to minimize their impact on the design and performance of the detectors.

Surface states

The impact of surface state between metal electrodes should not be understated in the performance of the detectors, as one prominent source of surface leakage current [33]. Moreover, the defective surfaces undoubtedly exhibit donor or acceptor behaviour due to the presence of charges at the surface. To maintain the charge neutrality principle, a depletion layer,

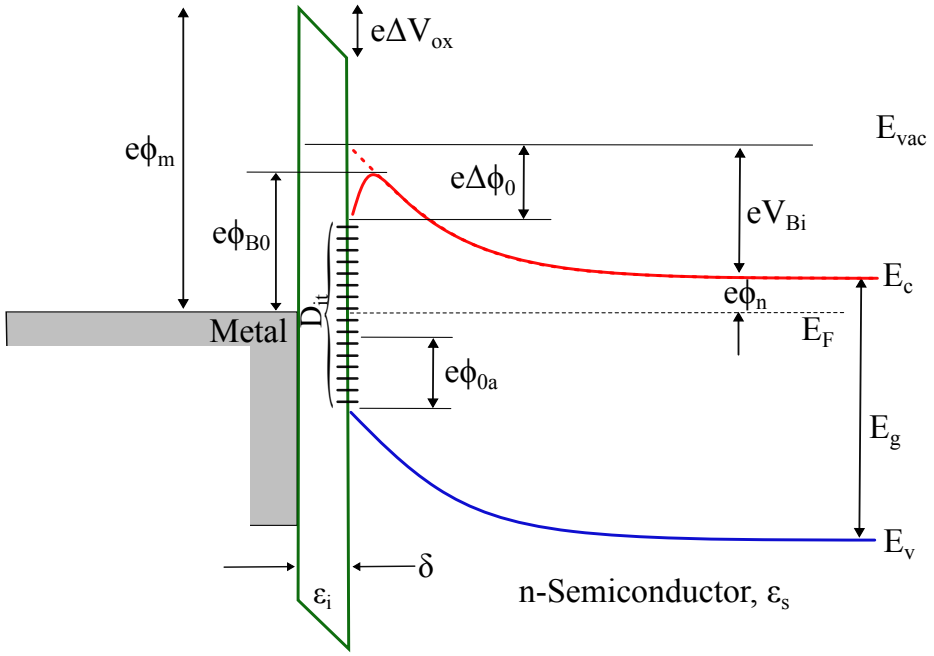

Figure 2.3 Equilibrium band alignment of an n-type semiconductor-metal interface with interface states, interfacial layer and image-force lowering. The image force lowering is $\Delta\phi_0$, the energy of the acceptor interface states is ϕ_{0a}, and they have an interfacial density of D_{it}. Figure inspired by [3].

commonly referred to as the surface space charge layer, is formed. This depletion layer further causes band bending at the surface, a result of which is Fermi level pinning. Upon the application of a voltage, carriers accumulate at the surface, resulting in a significantly greater surface density of carriers than in the bulk. This accumulation exhausts all mobile carriers from the depletion layer and amplifies the surface band bending effects. The surface conductance of the substrate is incidentally modified, as shown in figure 2.4 for p-type Si. For highly defective surfaces where the band bending is significant, the surface conductance is shown to increase exponentially [4], facilitating the conduction of parasitic charges at the surface and electrode edges [6].

2.1.4 Current transport mechanisms

There are 5 different transport mechanisms allowing carriers to flow through the interface defined in the previous sections. All are depicted in figure 2.5. The different mechanisms are:

i. Thermionic emission:

The limiting process of thermionic emission is the actual transfer of charge carriers

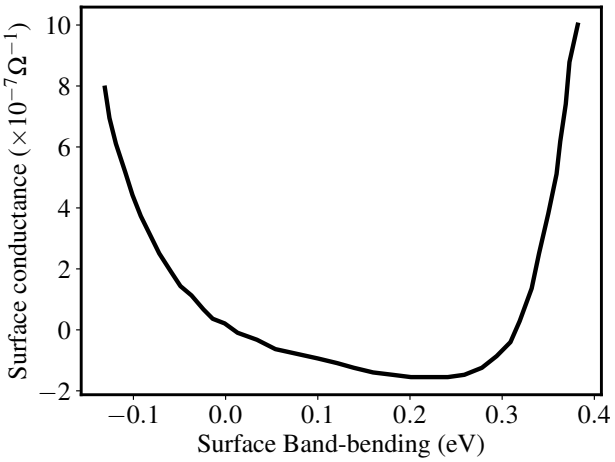

Figure 2.4 Variation of surface conductance of p-type Si for changing band-bending from surface states at room temperature. Figure recreated from [4].

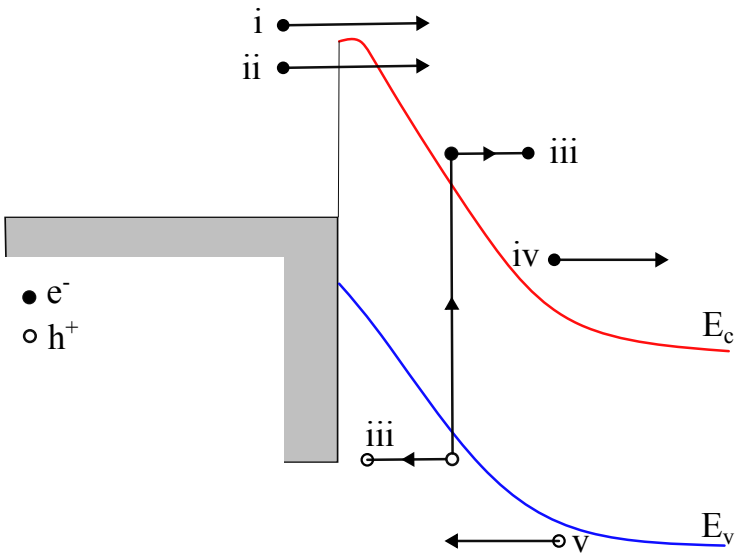

Figure 2.5 Charge transport mechanism in reverse bias Schottky barrier interface. i. Thermionic emission. ii. Tunnelling. iii. Generation. iv. Electron diffusion. v. Hole diffusion. Figure inspired from [5, 6]

across the interface. Consequently, charge carrier drift and diffusion are negligible. Only carriers with energy above the barrier height are collected.

ii. Tunnelling:
Quantum mechanical tunnelling of charge carriers is possible under certain conditions, allowing them to penetrate the barrier without carrying enough energy to overcome it.

iii. Recombination (fwd. bias)/Generation (rev. bias):
Recombination currents rely on the presence of localized defect states with energy in the bandgap (near the middle of the bandgap is ideal) in the depletion region to facilitate the charge transport through the interface. Recombination current often leads to a departure from the typical exponential behaviour of the interface's IV characteristics. Generation currents are more important in low-mobility, high-barrier semiconductors and contribute to the background current of detectors.

iv/v. Electron/hole diffusion:
Diffusion currents are limited by the mobility of the charge carriers within the depletion region. It is directly proportional to the applied electric field and the carrier concentration gradient.

While the thermionic emission model has been shown to accurately depict the interfacial current of high-mobility semiconductors (Si, GaAs, etc.) as the mobility is assumed to be infinite, it falls short for systems with lower mobility, where the latter becomes the limiting factor, like in CZT. Models combining thermionic emission and diffusion, such as the interfacial-layer thermionic-diffusion mode [3, 44] have been developed to overcome these drawbacks.

Interfacial-layer thermionic-diffusion theory

Building upon the metal-semiconductor structure with an interfacial layer, the impact of interface states on the carrier dynamics under electric field can be more easily understood, forgoing the intrinsic dynamics of contacts between both materials [5]. Under this assumption, a model including both effects of thermionic emission and diffusion currents as well as the screening effects of the interfacial layer has been developed by Wu [3, 44]. The latter elaborates on the basis developed by Cowley and Sze [45] by including the screening effects of interfacial layers, and has been shown to accurately model current behaviours in CZT-metal structures [33, 46–48]. Let a metal-semiconductor system be with an interfacial layer

thickness of δ (typically a few tenths of nm). The total current density is then given by

$$J_t = \frac{A^* T^2 \theta_n}{1 + \theta_n V_R / V_D} \exp\left\{-\frac{e(\phi_B + V_i)}{k_B T}\right\}\left(\exp\left\{\frac{eV}{k_B T}\right\} - 1\right), \tag{2.10}$$

where V_D is the effective carrier diffusion velocity in the depletion region, V_R is the thermal velocity of charge carriers in the current flow direction, θ_n is the transmission coefficient across the interface, notably due to phonon scattering [5]. A^* is simply Richardson's constant for the semiconductor. V_i is the voltage drop across the interface, and V is the applied voltage. This equation gives rise to an interplay between diffusion and thermionic current such that if $\theta_n V_R \ll V_D$, then

$$J_{IT} = A^* T^2 \exp\left\{-\frac{e\phi_B}{k_B T}\right\}\left(\exp\left\{\frac{eV}{k_B T}\right\} - 1\right) \tag{2.11}$$

is the thermionic diffusion current as derived by Bethe, assuming no interfacial voltage drop and 100% transmission across the interface. On the other hand, if $V_D \ll \theta_n V_R$, then equation (2.10) becomes

$$J_D = q N_C V_D \exp\left\{-\frac{e\phi_B}{k_B T}\right\}\left(\exp\left\{\frac{eV}{k_B T}\right\} - 1\right), \tag{2.12}$$

is the current diffusion theory derived by Schottky [37] assuming no voltage drop across the interface.

Specifically, in the reverse bias operation mode of detectors, the following form is obtained:

$$J_{rev} = \frac{-A^* T^2}{1 + \theta_n V_R / V_{D,rev}} \exp\left(\frac{-q\phi_{Bn,rev}}{k_B T}\right), \tag{2.13}$$

where

$$\phi_{Bn,rev} = C_2(\phi_M - \chi) + (1 - C_2)(E_g/q - \phi_{0a}) - \Delta\phi'_{0,rev} + X_e^{1/2}\delta k_B T - (1 - 1/n_0)V_{rev}, \tag{2.14}$$

is the reverse bias barrier height. It differs from the forward barrier height by the inclusion of a $\Delta\phi'_{0,rev}$, the image force lowering factor alongside a $(1 - 1/n_0)$ voltage-dependent factor to characterize the additional voltage drop across the interface in reverse bias. In both cases, these factors effectively reduce the apparent barrier height. The image force lowering is considered negligible compared to the interfacial voltage drop. $\chi_e^{1/2}$ is dependent on the interfacial barrier height and tunnelling effective mass of the charge carriers, and factors in

the transmission coefficient at the interface $\theta_n = \exp X_e^{1/2}\delta$. Finally, C_2, is defined as

$$C_2 = \frac{\epsilon_i}{\epsilon_i + q^2\delta D_{it}} = \frac{1}{n_0}, 0 \leq C_2 \leq 1. \tag{2.15}$$

Notwithstanding its impact on interfacial voltage drop in reverse bias, this parameter effectively defines the predisposition to Fermi-level pinning of the device. We again note that for $D_{it} \to \infty$, $C_2 \to 0$ and the Fermi level is pinned. On the other hand, for $C_2 \to 1$, $D_{it} \to 0$ and the effective barrier height is (2.7). Moreover, an increase in density of states translates to additional interfacial voltage drop, detrimental to the performance of high-voltage operation detectors.

This model highlights the need to thoroughly engineer the interfacial properties of CZT radiation detectors to obtain low background current throughout the operational range.

2.2 CZT as a direct conversion X-ray detector

CZT has remained the forerunner candidate for the implementation of solid-state detectors in CT scanners. Its 1.57 eV bandgap (for $Cd_{0.9}Zn_{0.1}Te$) [24] allows to have a relatively low density of thermalized carrier at room temperature such that it exhibit intrinsically low dark current and a high resistivity of $2 \times 10^{10}\ \Omega - \text{cm}$ (non-compensated) [25]. However, CZT presents a large disparity in charge transport characteristics between electrons and holes, $\mu\tau$ of 10^{-2} and 10^{-4}-10^{-5} cm^2/V respectively [24]. Nonetheless, the combination of high atomic number and high density conveys this II-VI alloy's favourable attenuation characteristics, as shown in figure 2.6 [7]. The latter shows the mass attenuation coefficient of CdTe from 10 keV to 500 keV. We note the large attenuation potential of the alloy in the range of 10-150 keV. More importantly, most of the absorbed radiation is through the photoelectric effect, and not scattering. The low scattering loss inherent to CdTe and CZT in the CT radiation energy range bestows high intrinsic quantum efficiency, and the high density suggests that thin detectors (mm-range) can be used.

This section aims to describe the efforts to make CZT suitable for PCCT. First, the underlying principles of direct-conversion detectors are outlined in section 2.2.1. Second, the challenges inhibiting the widespread implementation, so far, of CZT as radiation detectors are analyzed. Third, conventional detector structures are shown in section 2.2.3.

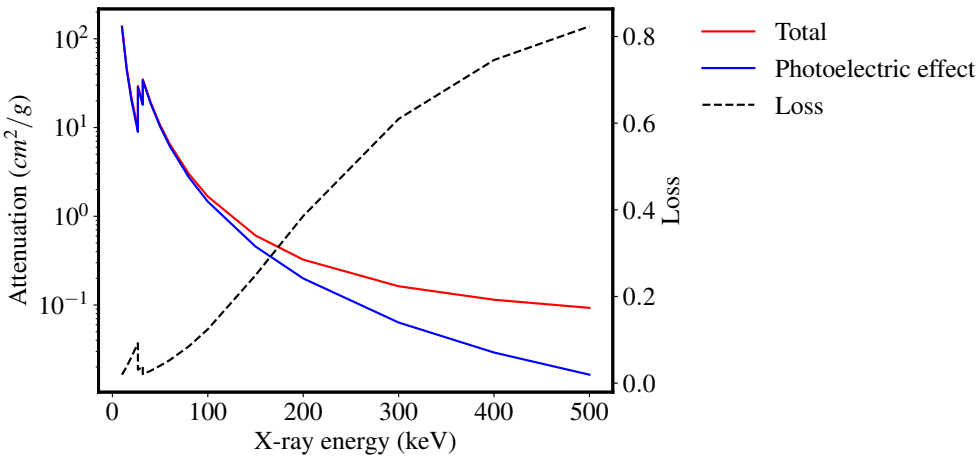

Figure 2.6 Mass attenuation coefficient of CdTe binary alloy in the X-ray imaging spectrum and the relative importance of photoelectric absorption. The losses due to scattering within the crystal become dominant at energies above 250 keV. Curves reconstructed from NIST dataset [7].

2.2.1 Physical principles of direct conversion detectors

Direct-conversion detectors rely on the immediate generation of electron-hole pairs in a semiconductor material upon absorption of an incident photon, enabling the direct transformation of photon energy into electrical charge without the intermediate step of scintillation. From photon to current, three different processes are critical:

1. Carrier generation,
2. Carrier transport,
3. Carrier collection.

Figure 2.7 showcases these different processes in a reverse-bias metal(Schottky)-semiconductor-metal(ohmic) detector, such as CZT-based radiation detectors. The generation of electrically charged carriers is driven by the photoelectric effect. The process can be intrinsic or extrinsic. In the prior, an electron-hole pair is generated by the absorption of a photon with energy $h\nu$. If the energy of the photon is greater than the bandgap of the material E_g, the photon is fully absorbed in the material, leaving behind the additional charges available for electrical flow in the conduction and valence bands. A similar process is observed in extrinsic carrier generation, only it relies on the presence of defects within the bandgap to generate electron-hole pairs at the defect-energy levels. This process is what allows certain detectors to operate at energies below their bandgap. The efficiency of this process is characterized

by the quantum efficiency η, or how many carriers are generated for each incident photon. Whilst the minimal energy required for the generation of an e-h pair is the bandgap energy of a semiconductor, this relation was found not to hold true empirically [49]. In fact, as per the Klein rule, the average electron-hole pair creation energy ε is systematically found to be around $3 \times E_g$ [26] due to losses from phonon scattering, carrier thermalization and inefficient ionization [23, 26, 49]. As such, the number of charges created by an incident photon is $Q_0 = eh\nu/\varepsilon$, where ε_{CZT} for CZT was reported to be 4.64 eV [27].

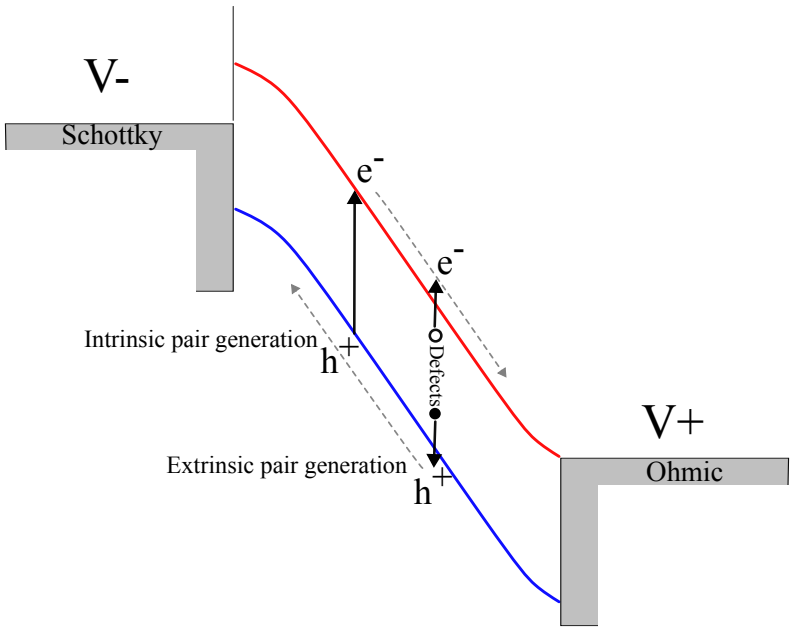

Figure 2.7 Photoconversion processes in a reverse bias photoconductor with a metal(Schottky)-semiconductor-metal(ohmic) structure, as those developed in CZT radiation detectors. Photo-generated carriers can be intrinsic or extrinsic. They drift towards the electrodes, where they are collected and the current measured.

Once the carriers are generated, they are swept towards the electrodes. The photocurrent, as a function of the incident photon power P_{opt} and applied field E_{rev}, is given by

$$I_p = e\left(\eta \frac{P_{opt}}{h\nu}\right) \frac{(\mu_n + \mu_p)\tau E_{rev}}{L}, \tag{2.16}$$

where τ is the carrier lifetime, L is the detector thickness, μ_n and μ_p are the electron and hole mobility. Equation (2.16) assumes only intrinsic carrier generation. Moreover, if we assume the an interaction depth of x, The equation becomes

$$= e\left(\eta \frac{P_{opt}}{h\nu}\right) \tau \left(\frac{1}{t_{rn}} + \frac{1}{t_{rp}}\right). \tag{2.17}$$

The electron and hole transit times are defined as

$$t_{rn} = \frac{x}{\mu_n E_{rev}},\ t_{rp} = \frac{L-x}{\mu_p E_{rev}}. \tag{2.18}$$

These equation highlights the importance of carrier mobilities on the photocurrent and detector speed, and suggest that the application of a large electric field can overcome some of the drawbacks of CZT. Nonetheless, this model is oversimplified. Detectors are characterized by their charge collection efficiency (CCE), given by the Hetch equation [50]

$$\text{CCE} = \frac{\mu_h \tau_h E_{rev}}{L}\left(1 - \exp\left\{-\frac{x}{\mu_h \tau_h E_{rev}}\right\}\right) + \frac{\mu_e \tau_e E_{rev}}{L}\left(1 - \exp\left\{-\frac{L-x}{\mu_e \tau_e E_{rev}}\right\}\right) \tag{2.19}$$

which measures the efficiency of all processes from generation to collection [24]. Even then, the effect of charge trapping, carrier recombination, among many, are ignored. Yet, equation (2.19) is still predominantly used to characterize the performance of highly-defective CZT detectors.

2.2.2 Limitations of CZT

Despite being at the forefront of the possible candidate for direct-conversion radiation detectors, the implementations of CdTe alloys in commercial CT scanners has been slow, with two systems fully FDA approved [28] as of February 2025. The slow transition from research to clinical use is largely attributed to intrinsic limitations of the material itself; many of which originate from crystal growth and processing (CMP, interface control, etc.) challenges and their subsequent effects on detector physics and system performance. CZT crystals are notoriously difficult to grow without the formation of defects, which can include tellurium inclusions, precipitates, grain boundaries, dislocations, and sub-grain structures [22]. These defects are typically introduced during the solidification process and are exacerbated by thermal gradients, compositional inhomogeneities, and growth instabilities [22]. While decades of research have focused on refining Bridgman (LPB, HPB, VBM) and THM techniques to suppress these imperfections, achieving consistently high-quality, large-volume CZT crystals remains a major bottleneck in scalable production. Moreover, the detector processing steps, predominantly etching steps, as developed in section 3.1, also induce defects such as dislocations, surface non-uniformity and dangling bonds.

At the microscopical level, these structural imperfections introduce in the CZT matrix both

shallow and deep-level defect states within the bandgap, serving as both carrier trapping and recombination centres [39]. It has been noted that CZT possesses very asymmetric charge transport properties, with the electron mobility being intrinsically 2-3 orders of magnitude larger than the hole mobility. This increase in trapping centre density results in a reduced carrier mobility-lifetime, where the deep-level traps completely recombine with free carriers and shallow traps reduce the effective carrier velocity [51]. An ever-increasing recombination rate on the carrier's mobility lifetime product leads to an incomplete charge collection, specifically hole collection. Moreover, trapping centres were shown to be spatially correlated due to aggregation around extended defects such as grain-boundaries, leading to large electric field inhomogeneities [25].

At the detector level, the presence of such shallow defects stems spontaneous generation of parasitic charge carriers due to shallow trapping centers, as discussed in section 2.1.1, increasing the background current of the detectors. Moreover, the large mismatch in carrier mobility leads to polarization of the detector. From equations (2.18), the transit time of holes and electrons, under a constant electric field, is shown to be directly impacted by the mobility. As such, the transit time of electrons in the material is found to be orders of magnitude smaller than that of holes; with that of holes often being below their carrier lifetime. Consequently, holes commonly recombine before they are collected. This reduced drift speed leads to poor transient response and hole tailing at best [22, 24, 51]. Under many circumstances, high photon flux, high bias, etc., an accumulation of negative changes at the interface is observed, generating of an opposite electric field to the applied one. This detector polarization effect collapses the electric field in the detector, rendering them useless [25].

2.2.3 Devices architecture and designs

Diverse direct-conversion detector designs have been developed to address some of the issues previously mentioned, alongside others that fall outside the scope of this project. The detector structures commonly encountered are: planar electrode, coplanar grids, pixel arrays and Frisch-grid. Figure 2.8 presents a schematic of those. Several metals have been explored, such as Al, In, Mo, Ni and Ti, but Pt and Au remain the predominant choice due to their high work functions enhancing barrier height, reducing carrier injection and dark current thereof [24, 52–55]. The simplest structure is the planar electrode, figure 2.8a. Comprised of two blanket electrodes spanning the full width of the mm-size detectors, the advantage of this device resides in its fabrication simplicity, requiring no extensive electrode patterning steps, and only metal deposition. In this design, the anode and cathode can be reversed.

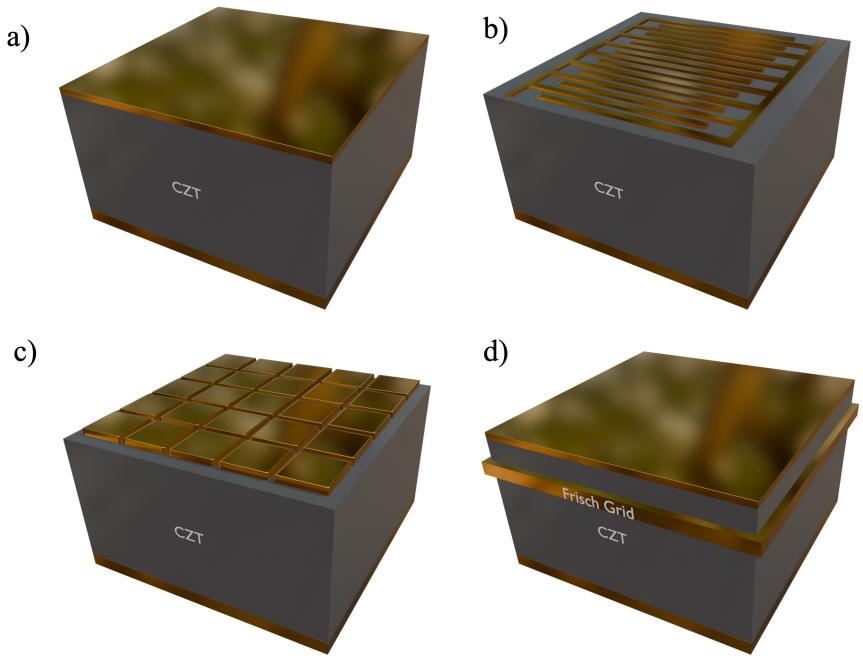

Figure 2.8 CZT detector structures commonly used in CZT radiation detectors. a)Planar. b) coplanar grid. c) pixel arrays. d)Frisch-grid. Pt and Au are both preferred materials; they may be deposited by physical deposition or by electroless deposition.

Notwithstanding sharp-edge effects at the electrode borders, the electric field in this design is assumed to be linear; thus, it suffers from all issues previously stated in section 2.2.2. Moreover, one should carefully assess the sidewall quality and conductivity to avoid possible shorting scenarios under high bias. The second structure, the coplanar grid, figure 2.8b, consists of two sets of planar interdigitated combs on the anode, and a complete blanket electrode as the cathode. Two different positive biases are applied to the comb-like electrodes, while the cathode is maintained at a negative voltage. This structure is fairly popular due to its potential to eliminate the hole current contribution, and thus many of the issues aforementioned. Indeed, the weighting potential profile drawn from this design is such that the electric field near the anode changes rapidly, and is more gradual at the cathode side. Consequently, hole drift is minimized and only electron current is accounted for [56,57]. This design is highly susceptible to surface processing and surface leakage currents [58]. The pixel array configuration is the most common device structure [24], figure 2.8c. Consisting of a positively biased pixelated electrode and a negatively biased blanket electrode, it allows to obtain the spatial position of the incident photon [24, 58]. Moreover, this structures offers a wide engineering flexibility, allowing to design the pixels size for different applications. Indeed, the pixels dimensions and interpixel pitch can be engineered to optimize spatial

resolution, noise levels or background current. In the case of radiation detector for medical applications, pixel dimensions in the 100-500 μm range have been shown to optimize the spatial resolution, minimize the pixel cross-contribution to signal current and offer relatively low background current [18, 22, 25, 59, 60]. Similarly to the coplanar grid, the non-linear electric field within the semiconductor allows to minimize hole trapping [61, 62]. Moreover, this structure

Finally, Frish-grid electrodes were specifically designed to eliminate the contribution of holes to the total current [58]. A metallized ring surrounding the detector is deposited. The structure can be used in conjunction with any other coplanar electrode design [63]. Through the biasing of the metal ring, one effectively generates an electric field between the anode and the ring, geometrically modifying the weighting potential between the cathode and anode such that the variation between the anode and the grid is much larger than between the grid and the cathode. This effectively inhibits the drift of generated holes, and enhances the collection of electrons at the anode [64, 65].

As seen in the aforementioned device structures, the hole trapping issue has seeded the development and widespread adoption of device structures enabling the unipolar mode of the detectors; that is, only the electron current is measured.

CHAPTER 3 CZT DETECTORS FABRICATION AND CHARACTERIZATION

To achieve the objectives outlined in section 1, CZT detectors were fabricated and tested following a tailored microfabrication process. The development of the overall process flow specific to CZT detectors was carried out collaboratively with our team, among whom I shared the responsibility of engineering the fabrication standard operating procedures (SOP). These SOPs were established to ensure consistent process execution, reduce fabrication-induced variability, and maintain high electrical performance across devices. The procedures encompass all critical fabrication steps, including surface preparation, photolithography, metallization, and post-processing, and have been optimized for compatibility with CZT substrates and device requirements.

The sections that follow describe the fabrication and characterization approach in more detail. First, section 3.1 introduces the fundamental concepts relevant to the fabrication of the detectors. Second, section 3.2 shows the specific process flow developed for this work. Third, section 3.3 discusses the different tools and techniques used to evaluate the detector's performance and quality.

3.1 Overview of microfabrication processes and their implementation for CZT processing

This section overviews the fundamental techniques used to fabricate CZT radiation detectors. Most detectors implemented in practical applications require high spatial resolution, and have very low tolerances in their design [19]. Consequently, the detectors are commonly fabricated in clean-room facilities, providing an environment free of particles and contaminants that may hinder the detector's performance and throughput, and ensuring consistent fabrication. All three major steps of the fabrication process are considered below and, if applicable, CZT-specific considerations are discussed. First, the lithography section 3.1.1 is presented, followed by the deposition of thin films and metal contacts in section 3.1.2. Finally, the various etching processes are described in section 3.1.3.

3.1.1 Photolithography

The manufacturing of micron-scale structures, such as pixel structures discussed in section 2.2.3, requires specific procedures and equipment. Lithography, and specifically photolithography, is the most widely used process to pattern structures at such scale [8]. It is, itself, comprised of three major steps: resist deposition, exposition and development. The process is summarized in figure 3.1.

Resist Deposition

The first step of a successful photolithography consists of covering the samples with a photosensitive organic compound, referred to as a photoresist. Sample dehydration should be done before to ensure good adhesion to the substrate. While there are many ways to deposit conformal thin layers of this semi-viscous compound, spin-coating remains the prevalent one in academic contexts due to its simplicity and low cost. Drops of the photoresist are deposited in the sample's centre, which is then spun at high RPM (1000-4000) to evenly spread a thin layer on the sample. The layer's thickness varies between 1 µm and 5 µm depending on the resist's viscosity and RPM. The resist is then baked to evaporate the solvent and create a hard film. A layered resist stack with different properties can be used depending on the intended applications. For example, the deposition of pixel electrodes has very tight tolerances. Thus, a lift-off process is used. To improve the attack of the solution, a 2-layer stack with a lift of resists (LOR) underneath is used. The latter is not photosensitive and dissolves at a higher rate than the patterning resist, and creates an undercut allowing effective liftoff processes. Regardless, the uniformity of the resists is paramount in the following steps to minimize defects and obtain well-resolved structures [8].

Exposition

The exposition step is the most critical in the lithography process. The process uses a combination of a photon source, a pattern stencil and a stage (for alignment). The stencil, also known as a photomask, is comprised of a transparent medium (Soda Lime glass) on which a chrome layer is deposited in the desired pattern to block the incident photons from reaching the photoresist. Upon exposure to a specific dose (in mJ/cm^2), the photoresist undergoes a chemical change, making it soluble in developer. If the resist's tone is positive, the exposure degrades its development inhibiting agent, and the exposed pattern is obtained after development. On the other hand, if the resist's tone is negative, the exposure causes its polymerization, rendering it insoluble in developer. A Hg lamp is used to generate the UV

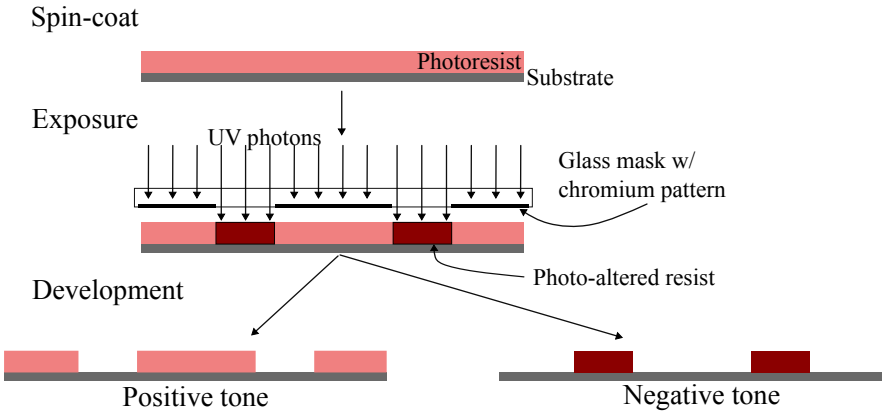

Figure 3.1 Generalized photolithography process from resist spin-coating to development. The pattern can be positive or negative. Figure inspired from [8].

lamp for exposure; the i-line at 365 nm is primarily used, though many other wavelengths ranging from near-UV to extreme UV can be used. In fact, the major factor limiting the dimensions of resolvable structures is the exposure wavelength due to diffraction at the exposure opening. The smallest structure possible to resolve, assuming all other ideal conditions, is roughly equal to the exposure wavelength. Three main modes can be used to expose the samples through the mask. First, in contact mode, the mask (its chromium layer side) and sample are physically pressed together to minimize beam distortion and achieve the best possible resolution for the wavelength. However, this method accelerates the deterioration of the photomasks. Second, the sample can be exposed in proximity, where a set gap is left between the mask and the sample. This mode is sufficient for large structures, as it prevents mask deterioration, but offers slightly less lateral resolution due to diffraction. Third, projection exposure can be used. In this mode, the mask and sample are separated by an imaging optic apparatus. This setup, despite its added complexity, offers the most flexibility and allows for mask pattern downsizing, easing mask fabrication. It also offers the largest mask lifetime of all three modes. [8]

Resist development

By submerging in an organic solvent, the targeted sections of the photoresist, whether it be a positive or negative pattern, are dissolved, revealing the pattern [8].

3.1.2 Thin film deposition

The processes by which thin films are deposited to form electrodes or passivation layers are shown below. Specifically, the physical evaporation methods of e-beam and sputtering are

discussed, alongside the chemical method of electroless deposition. Although other processes such as chemical vapour deposition (CVD) and atomic layer deposition (ALD) are widely employed in the broader semiconductor industry, their application in bulk CZT radiation detector fabrication remains limited [22].

E-beam evaporation

E-beam evaporation is a form of thermal evaporation in which a focused electron beam is used to locally heat and vaporize a target material within a crucible. This technique is well-suited for the deposition of elemental metals whose evaporation temperatures typically range from 600°C to 1200°C. The process is carried out in a high-vacuum environment, typically maintained at or below 10^{-6} Torr. Under these conditions, the mean free path of the vaporized atoms exceeds the distance between the source and substrate, allowing for ballistic transport with minimal scattering. Upon reaching the substrate, the atoms rapidly decelerate, lose kinetic energy, and condense onto the surface. Some residual energy may contribute to lateral diffusion or the formation of interfacial defects at the semiconductor–metal interface [8].

As per all thermal evaporation methods, the deposition occurs in a planar fashion, with atoms emitted in a cone-like flux centred around the crucible axis. Consequently, variations in film thickness can occur due to angular flux divergence, particularly across large or irregular surfaces. To mitigate thickness non-uniformity and improve liftoff quality, bilayer resist stacks are typically used. Additionally, due to the relatively large thickness of CZT substrates ($\approx$2 mm), misalignment of the substrate normal to the evaporation source can result in unwanted metal deposition on the sidewalls. This increases sidewall conductivity and may lead to electrical shorting. To address this, sample edges are commonly masked during deposition. In some cases, shadow masks are used to pattern metal contacts directly by shading the pattern directly during the deposition, eliminating the need for lithographic processing. E-beam evaporation is widely used in detector fabrication due to its simplicity, high deposition rates, low operational costs and the high purity of resulting films. However, it is limited in its ability to deposit compound materials, and the adhesion of films to CZT surfaces is generally lower than that achieved with other physical deposition techniques such as sputtering [8].

Sputtering

Sputtering, another physical vapour deposition technique, provides superior film adhesion and enables the deposition of a wide variety of materials, including metals, alloys, ceramics, and dielectrics. Unlike thermal evaporation, it relies on ion bombardment rather than

thermal energy to eject material from a target. The process is typically conducted in an inert gas atmosphere, commonly Ar or Xe, where a plasma is sustained. Positively charged ions within the plasma are accelerated toward a negatively biased target, physically ejecting atoms from its surface through a momentum transfer. Since the process is not dependent on the vapour pressure of the target material, sputtering enables the deposition of materials with low volatility or complex stoichiometry. Radio-frequency (RF) magnetron sputtering is often employed to reduce target and substrate heating and broaden material compatibility. Sputtered atoms have lower mean free paths compared to their evaporated counterpart due to the higher deposition pressure, such that the atoms arrive at the substrate at a variety of incident angles, leading to enhanced step coverage [8].

In addition to physical sputtering, reactive sputtering can be employed by leveraging chemical reactions within the plasma to deposit off-stoichiometric compounds. Reactive gases such as N_2 or O_2 are introduced in the plasm and ionized so that they chemically react with the sputtered atoms, enabling the formation of materials such as SiN_x, Al_2O_3 and TiN. For instance, the SiN_x passivation layer used in Section 3.2 was deposited via reactive sputtering from a pure Si target in an Ar:N_2 gas mixture (5:2 ratio) [66, 67], without any external substrate heating. While sputtering introduces risks such as film contamination and substrate damage from ion bombardment, it remains a preferred method in industry due to its versatility, precise control over deposition parameters, and ability to maintain stoichiometric or engineered film compositions [8].

Electroless deposition

Electroless deposition is a chemical method for depositing metal films from a solution. It is particularly well-suited for CZT detectors and is widely used in research and industrial contexts [68]. The process is autocatalytic, relying on a reducing agent in the solution to provide the electrons necessary for the metal reduction reaction, thereby overcoming the self-limiting characteristic of immersion plating and allowing thick films to be deposited [8]. The technique allows for precise tuning of interfacial properties by minimizing the time between surface treatment and deposition. Alloying different metals can allow good control over the Schottky barrier at the interface and, in certain conditions, near-ohmic contacts can be achieved [69]. As discussed in section 2.2.3, Au and Pt are the most commonly electroless-deposited electrodes for CZT. This method provides excellent interfacial bonding, often attributed to intermixing of the metal and CZT at the interface [54, 70]. However, the acidic and corrosive nature of the deposition bath can cause degradation or roughening

of the CZT surface. Higher bath temperatures can exacerbate this effect by promoting the formation of voids at the metal–semiconductor interface [70]. The best results are typically obtained using gold chloride diluted in HCl and water, or platinum salts $PtCl_4$) dissolved in methanol or dimethylformamide (DMF). Due to the aggressive nature of the chemical bath, compatibility with standard photoresists is limited, restricting the use of conventional lithographic processes. As a result, alternative techniques such as scanning pipette deposition have been developed for pixel-level definition [71]

3.1.3 Surface conditioning and etching

We showed in section 2.1.3 the impact of surface defects on the dark current and quality of the detectors. To reduce the density of these defects, etching processes are employed to condition the surface, thereby achieving high-performance detectors. Initially, these defects are typically induced by the dicing process. Thick CZT detectors used for radiation detectors are sourced from bulk ingot, and are sawed along the preferred face orientation (typically (111) for better charge collection efficiency [22]). The dicing process undoubtedly produces high-roughness surfaces that should be polished or etched prior to further processing. Indeed, high-roughness surfaces have been, assuming surface stoichiometry is maintained, directly correlated to deteriorated performances and high dark current [40, 42, 72]. While the range of etching methods is limited only by the engineer's imagination, the processes typically fall into one of two general categories: wet etching and dry etching. Some methods combine both. First, mechanical polishing (MP) is performed on the surface to reduce roughness and achieve specular surfaces. Then, depending on the device design, the surface is further chemical-mechanical polished (CMP) or wet-etched or dry-etched. The specific processes developed for CZT are discussed below.

Mechanical and Chemical-Mechanical Polishing

MP is a standard step in semiconductor processing used to remove surface material and planarize substrates. This purely mechanical approach employs successively finer abrasives to achieve specular surfaces, typically starting with 800-grit and 1200-grit abrasive pads, followed by alumina slurries with particle sizes ranging from 3 µm down to 0.05 µm. The process combines two-body and three-body abrasive wear, where both the polishing pad and suspended particles contribute to surface removal. Despite the widespread use of alumina slurries, MP alone has been shown to leave relatively high surface roughness and introduce a defective interfacial layer on CZT wafers [41, 73]. To mitigate these drawbacks, CMP has emerged as the preferred method for achieving low-roughness surfaces while minimizing

polishing-induced damage. In CMP, chemical etchants are introduced alongside mechanical abrasion to assist in material removal and surface smoothing. Br–MeOH solutions are commonly employed due to their high electrochemical potential on CZT, but as discussed in Section 3.1.3, they tend to leave the surface Te-rich and thus more conductive. As a result, alternative compounds such as nitric acid or a more environmentally friendly mixture of H_2O_2 and citric acid have been investigated to better preserve surface stoichiometry. CMP using such approaches has achieved sub-nanometer surface roughness; often below 0.5 nm, and has been correlated with improved detector performance, particularly lower dark current and SLC levels [74]. However, both MP and CMP processes have been reported to embed slurry particles into the CZT surface and induce microstructural damage, which may affect subsequent device fabrication and performance [22, 41].

Wet etching

Despite its hazardous nature, bromine has been shown to be the most effective chemical to etch CZT. To control the etching rate and the hazard of the substance, Br is typically diluted in methanol to percentages ranging from 2% to 5%. The substrate is simply immersed in the solution for 20s to 5min, depending on the needs, and the required etching depth. For example, solutions of 5% Br:MeOh have been shown to etch CZT at a rate of 12 µm/min [75]. However, the dynamic of the etching process has yet to be fully elucidated. Consequently, the process is hard to control, and its repeatability is even harder to maintain. Moreover, the effects of the etching on the substrate's morphology have been the subject of contrary reports, with some claiming it roughens the surface and others the opposite [76, 77]. The main drawback associated with the etching of CZT is the preferential etching of Cd compounds, resulting in a Te-rich layer at the surface [22, 76]. Whilst the impact of the etching solution is confined the the first 4-5 nm of the surface [78], after which stoichiometry is restored, Te is part of the metalloïds and consequently has a much higher conductance than bulk CZT and detrimental effects on the performance of detectors.

To restore the surface properties of intrinsic CZT and lower the surface conductance, the substrate's surface is often oxidized. Many methods have been developed to oxidize the Te-rich surface. However, the two standouts are wet oxidation in a NH_4F/H_2O_2 [79] solution and O_2 plasma [80]. Both methods have been shown to fully oxidize the elemental Te, with TeO_2 is shown to reach 90 at.% [81] at the surface; its percentage to decrease with depth. However, the lack of control over the method's output in terms of film composition and performance is detrimental to the progress of device development. For example, film compositions are

predominantly TeO_2-rich but may contain non-negligible at.% of $CdTeO_3$. The remaining Te may be bound to $CdTeO_3$ [79, 82], which has different electrical properties. Also, depending on the pre-etching process, etching time, concentration and oxidation process, the thickness of the layer was shown to span values from 2 nm to 100 nm [78, 79]. Furthermore, in the days following the oxidation, the oxidation percentage of the elemental Te was shown to increase [83], thereby reducing the detector background current in the hours to days following the oxidation, likely due to the reaction with environmental oxygen [78].

Dry etching

Several of the limitations inherent to wet processing can be mitigated through the use of dry techniques. In particular, dry processes generally preserve surface stoichiometry more effectively. By harnessing plasmas and ion bombardment, these methods enable the physical removal of surface layers without the need for corrosive chemicals [8]. While reactive ion etching (RIE) has been widely adopted in microfabrication to selectively target specific materials, its use in CZT detector processing has not yet been demonstrated. To date, studies on CZT have focused on physical sputtering with Ar and chemical plasma etching using O_2 plasma [80, 84–87]. In the case of Ar, ionized Ar^+ ions transfer momentum to the surface to remove material purely by physical means, without chemical selectivity. At plasma powers below 100 W, this process has been shown to reduce both surface roughness and the thickness of the defective surface layer, correlating with a decrease in dark current and surface leakage current (SLC) [84, 85]. Conversely, higher Ar plasma powers were observed to increase surface roughness and reduce the contact potential difference (CPD) between the CZT and Au contacts, resulting in a moderate increase in detector dark current, albeit with fewer surface trapping centres. A detailed account of our Ar plasma surface conditioning experiments can be found in [86]. In the case of oxygen plasma etching, an increase in CdTe-oxide species was reported, along with reductions in both dark current and SLC [80, 87]. However, delayed oxygen diffusion into the surface following treatment may compromise long-term device performance stability [80].

3.2 Detector fabrication process flow

Among the several steps aforementioned, only a select few were systematically implemented for the fabrication process of pixelated detectors used throughout this thesis; predominantly to maintain surface stoichiometry and ensure consistent detector performance. Figure 3.2 outlines the complete fabrication process flow of CZT radiation detectors, from ingot to finalized device. It also outlines parallel processing steps to develop new device structures,

which will be implemented in chapter 5.

First, wafers are cut from CZT bulk ingots such that they are (111)-oriented. The thickness of these wafers typically ranges from approximately 1 mm for low-energy applications to several centimetres for use in nuclear imaging [22]. Since CZT crystallizes in a zincblende structure [22,24], the (111) face is either Cd-terminated or Te-terminated, commonly referred to as the A-face and B-face, respectively.

The wafer dicing process leaves the crystal surfaces in a highly defective state. Consequently, the wafers are polished using either MP or CMP. As discussed in Section 3.1.3, CMP produces smoother surfaces and is generally preferred for high-quality detector fabrication. Both faces of the wafer are polished to ensure symmetry and optimal surface properties. Subsequently, an ohmic contact is formed on the A-face by electroless gold deposition. To improve the contact's ohmicity, the surface may be etched using a Br-based solution prior to deposition. In this work, these three initial steps: cutting, polishing, and gold deposition, were performed by 5N+ prior to wafer delivery.

To remove organic contaminants or particulates that may have accumulated during handling and storage, the wafers were cleaned using a sequential ultrasonic solvent bath: 5 minutes in acetone, followed by 5 minutes in isopropyl alcohol (IPA), and finally 5 minutes in deionized (DI) water. Sonication was kept gentle throughout due to the brittle nature of CZT. The cleaning concluded with a DI water rinse and nitrogen gas drying.

We developed the following fabrication steps to define pixelated electrodes. Before any processing, the devices were dehydrated on a hot plate at 140°C for 5 min. A lithography process for lift-off was performed by spin-coating two photoresist layers: a photosensitive resist (AZ5214 EIR) over a non-photosensitive resist (LOR5A). The resist stack was exposed using a positive-tone pattern in contact mode. Upon development, the higher development rate of LOR created an undercut profile that facilitates solvent penetration during lift-off. This undercut enables cleaner pattern definition and improves spatial resolution of the fabricated structures [8]. A thin gold layer was deposited using electron-beam evaporation to define the pixel electrodes, which were resolved by lift-off in Remover 1165.

Optional process steps were introduced to fabricate alternative device architectures, such as MIS and passivated configurations, developed in chapter 5. Specifically, step 4 consists of

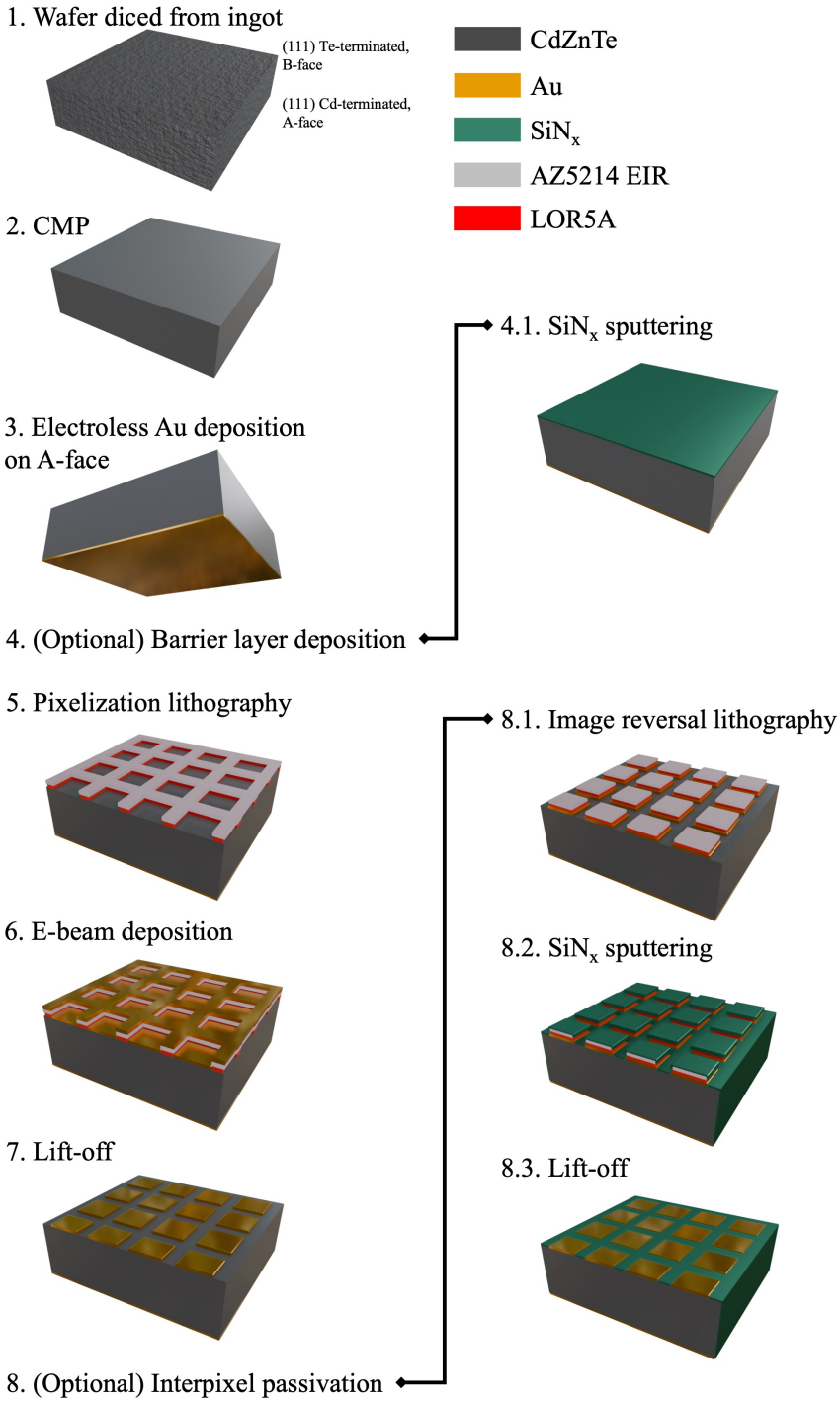

Figure 3.2 Fabrication process flow of CZT pixelized detectors. Step 1-3 were performed prior to the reception of the wafers. Steps 4-8 were optimized for fabrication in cleanroom facilities. Step 4 and 8 are optional processes to fabricate alternative device structures.

depositing a continuous insulating layer, here SiN_x by RF magnetron sputtering, to simulta-

neously passivate surface states and enhance the barrier height seen by charge carriers at the metal–semiconductor interface. Step 8 consists of passivating the interpixel surface region to reduce surface leakage currents. This involves a three-step process. First, photolithography for lift-off is performed using the same LOR and AZ resist stack, with the goal of exposing only the interpixel spacing. This can be achieved either by using a dedicated mask or by modifying the spin–bake–expose sequence to induce image reversal in the AZ 5214 EIR, effectively converting it into a negative-tone resist. A semi-conformal SiN_x layer is then deposited by RF sputtering. Due to the LOR undercut, solvent can access the base of the photoresist during lift-off, resulting in selective coverage of the interpixel regions with the insulating layer. Some deposition on the device sidewalls is expected due to the semi-directional nature of sputtering, though this layer is expected to be thinner than the one formed on the top surface. A detailed description of the device configurations resulting from these optional steps is provided in Section 5.1.2.

3.3 Characterization

Several characterization methods were employed to evaluate the quality of the wafers and the electrical characteristics of the radiation detectors. First, electrical characterization is discussed in section 3.3.1. Second, the characterization of surface roughness by atomic force microscopy (AFM) is discussed in section 3.3.2.

3.3.1 Current-Voltage characterization of CZT detectors

In chapter 2, the fundamental physics governing the background current, noise and photocurrent of metal-semiconductor-metal devices was developed. We emphasized the importance of minimizing the background signal (dark current) of the detectors to improve their imaging quality. The measurement of current-voltage (I-V) characteristics of detectors enables the assessment of their electrical response under various conditions and their corresponding electrical performance. A critical assessment of the device's current performance under variable conditions permits the extraction of key parameters, highlighting the behaviour of the detectors.

First, the device's dark current is measured to gauge their background current levels. These measurements are performed in complete darkness to avoid any photo-generation of electron-hole pairs in the depletion region. The measurements are conducted at room temperature. Although radiation detectors are operated in reverse bias, the I-V characteristics are measured

by sweeping from reverse bias to forward bias, providing insightful information regarding the detector's interface and current conduction mechanisms. Second, in the absence of a radiation source, the photo-response of the detectors is measured using a simple, broadband white light (ThorLabs MCWHL5-C1) from collimated LED's at 6500 K. Its emission spectrum sharply peaks at a wavelength of 440 nm, with a FWHM of 20 nm [88]. While the incident photon energy (2.8 eV) is orders of magnitude lower than the radiation energies used in medical imaging, averaging 70 keV [19], the method allows to qualitatively assess the detector's photocurrent, and compare it across different devices. Due to the large discrepancy between the used photon energy and that employed in medical imaging, measuring the CCE was deemed outside the scope of this project. Third, the SLC is assessed through measuring the current between coplanar electrode pairs. This pairwise measurement allows for minimizing the bulk current generation process and enhances the effect of sheet resistivity, surface conductance and interface defects in the dark current generation process.

I-V test setup

The electrical characterizations of the devices were performed, in most instances, using a Keithley 2470 Graphical SourceMeter unit (SMU). In some cases, a Keithley 4200-SCS Semiconductor Parameter Analyzer, with a 4201-SCS SMU unit, was also used. Both were paired with micro-probes to interface with the device under test. The probes were connected to the SMU or SCS via high-voltage triaxial cables. Micron-thin probes were used to interface with the contacts, minimizing electrode damage during tests. To measure the operational dark current (sometimes referred to as top-bottom configuration), the devices were first bonded to a copper tape, held on an insulating glass slide, from the blanket electrode side (electroless, A-face), as shown in figure 3.3. Once a good contact was obtained, the micro-probes were applied onto the device's pixel (probe I) and to the copper tape (probe II). The back-side electrode (copper tape side) was chosen to be the anode side, and was systematically grounded in the measurements. A voltage sweep was applied to the pixelized electrodes. To measure the background current, the devices were enclosed in a black box to eliminate all external lighting sources. To measure the photocurrent, the white light was oriented onto the pixel of interest using a set of lenses and mirrors. The photon flux was not measured. To measure the pairwise current, the micro-probes were contacted on coplanar electrodes, as shown in figure 3.4. The current sweep was maintained at lower voltages to avoid any breakdown of shorting effects due to the high electric field.

Most I-V characteristics shown in the present thesis were acquired using a set 500 ms de-

lay between measurements to allow for stabilization of the current level and proper carrier dynamics. While this delay may be small compared to some reported times to reach equilibrium [46], it provided a good balance between current stability and acquisition time. Some sweeps shown have also been acquired without any set delay, allowing the Keithley algorithm to determine the appropriate timing for the measurement based on its electronic limitations. These sweeps were 2.5x faster than in delay mode on average, enhancing the effects of electron and hole asymmetric transport and leading to capacitance effects and hysteresis in the current-voltage characteristics. Such I-V curves are shown in section 5.2.1.

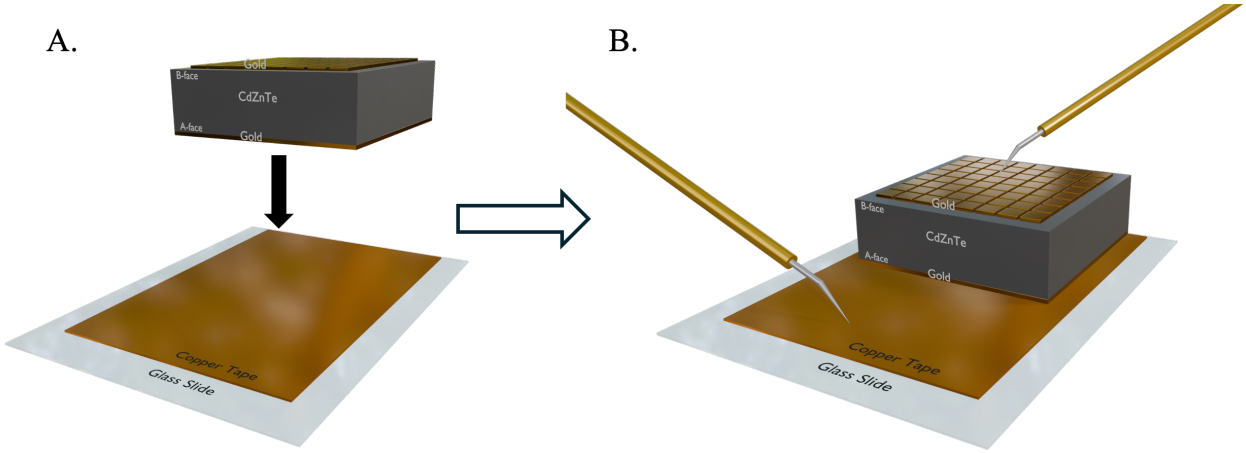

Figure 3.3 Top-Bottom (operation conditions) testing configuration and preparation. The device is bonded onto a copper tape (A), then micro-probes are used to apply bias through the copper tape and top pixels.

For the 2470, the voltage source uncertainties in the 1000V range is 0.02% ± 100 mV, offering a resolution of 50 mV. The measured current resolution is 10 fA in the 10 nA range (0.10% ± 250 pA accuracy), 100 fA in the 100 nA range (0.06% ± 300 pA accuracy), 1 pA in the 1 µA range (0.025% ± 300 pA accuracy), 10 pA in the 10 µA range (0.025% ± 700 pA accuracy) and 100 pA in the 100 µA range (0.02% ± 6 nA accuracy) [89]. Its open-circuit current was measured to be 20 pA throughout the complete voltage range.

3.3.2 Atomic Force Microscopy: overview and applications to CZT wafers

Several parameters factor into the performance of photodetectors. As thoroughly discussed, the surface condition prior to deposition of further compounds plays a critical role in the subsequently formed interface. Notably, increased surface roughness has been intrinsically linked to higher dark current levels and surface leakage current [40, 72, 90]. Moreover, the

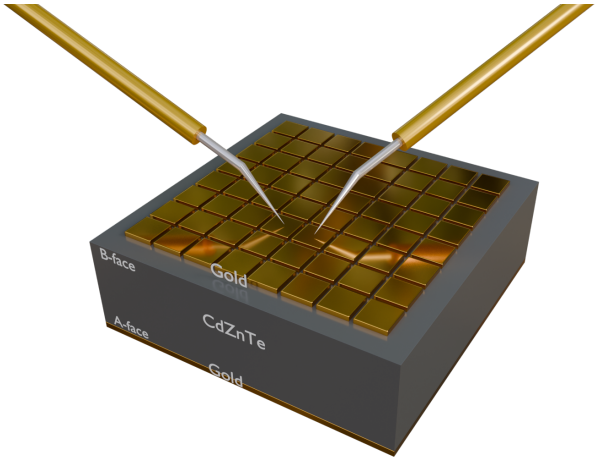

Figure 3.4 Pairwise (top-top) testing configuration. Surface leakage current between adjacent pixels is measured.

presence of surface defects has been strongly tied to spectroscopic peak tailing and poor energy resolution due to the increase in carrier trap density inherent to deteriorated morphology [22,91]. Consequently, it is imperative that one considers the CZT surface roughness to assess the forthcoming interface quality. Atomic force microscopy (AFM) remains the gold standard for measuring atomic-scale surface morphology of semiconductors [92].

AFM fundamental principles are built upon scanning probe microscopy (SPM) techniques developed in the early 1980s [93]. The specifics were developed by Binnig et al. in 1986 [94]. Figure 3.5 illustrates the working principle of the technique. A semi-flexible cantilever supports a nm-size tip raster-scanned across the sample's surface. As the tip approaches the sample's surface, several forces act upon it; electrostatic, repulsive/attractive contact or Van der Waals. The interaction causes the cantilever to bend up and down. The cantilever deflections are measured using a combination of a laser beam and a position-sensitive photodetector. A feedback loop is used to maintain the tip's distance from the surface (or contact force: mode dependent) throughout the scan, building a 3-dimensional topographic image of the surface with atomic resolution [95].

The surface morphologies presented in the following sections were acquired with a Bruker ICON FastScan^{TM}, equipped with a Bruker TESPA cantilever-tip combination. The latter has a tip radius of 8 nm. Bruker's proprietary QNM PeakForce tapping mode was used to acquire quantitative nanoscale measurements (QNM) alongside the surface morphology [92].

In this mode, the cantilever oscillates close to its resonant frequency, periodically contacting the sample's surface. This ensures cohesion of the sample's surface and avoids inherent dragging from contact scans, offering non-destructive imagery. The tip wear is thus minimized. This mode was chosen to minimize the possibility of CZT dust generation, ensuring the safety of all operators. It further provides, by measuring the phase shift from the resonance frequency, other quantitative surface metrics such as adhesion and modulus, which are useful for assessing the quality of surface preparation [92].

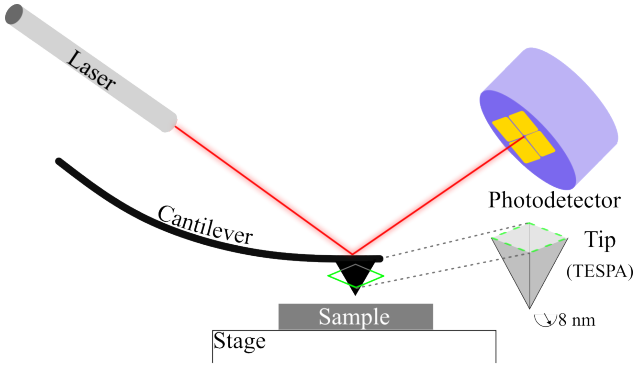

Figure 3.5 Principle of AFM. Tapping mode was used to map the surface morphology. The tip deflection is measured using a laser and a photodetector. Tip radius was 8 nm.

CHAPTER 4 LOW-TEMPERATURE ANNEALING AND ITS IMPACT ON THE METAL-SEMICONDUCTOR INTERFACE OF CDZNTE

The demand for high-performance CZT room-temperature radiation detectors for next-generation imaging systems is closely tied to new engineering challenges, particularly the need for precise fabrication control to consistently produce low-noise detectors capable of operating across a wide radiation energy range. Given the still imperfect nature of CZT, several processing steps are required to fully optimize the potential of the detectors. Spanning from CMP to metal electrode deposition, including intermediate plasma processes or chemical etch, the range of fabrication processes possible to use is largely limited by the low thermal budget of CZT detectors. Their thermal stability should therefore be well understood to develop processes capable of fulfilling the needs of modern detectors.

Over the past decade, several studies have mapped the thermal stability spectrum of the CZT-metal conundrum for various annealing conditions and metals. Yet, a dichotomy remains: should one avoid processes above 423 K°C? The response to this question seems to rely on the fabrication process and the annealing process. For instance, Chattopadhyay et al. (2000) [96] reported an increase in leakage current after vacuum annealing of sputtered Au electrodes, in contrast to Mergui et al. (1992) [97], who observed a decrease for electroless Au electrodes annealed in air at 423 K°C. Mergui et al. also noted a transition from performance degradation to improvement in vacuum between 413 K and 433 K [97]. Shi et al. (1997) [98] reported reduced dark current up to 423 K, followed by degradation beyond 448 K in vacuum. More recently, Park et al. (2010) [99] demonstrated that In–CZT detectors degraded after vacuum annealing but improved with low-temperature annealing in air. Finally, Wang et al. (2022) [48] that leakage current in electroless Pt contacts decreased up to 423 K, with degradation occurring at higher temperatures. It is generally reported that the low temperatures used in those studies have little to no effect on the bulk properties. Interface effects have been shown to be the source of improvement or degradation thereof. Improvements after annealing in air have been attributed to the formation of a thin oxide layer at the interface between CZT and Au [98–100]. On the other hand, the degradation has been attributed to a Schottky barrier height reduction [48, 96, 97, 100], and that etching of the surface restores the initial detector's leakage current [98].

In this study, we investigate the electrical performance of Au electrodes deposited by electron-

beam evaporation on the B-face of CZT following sequential annealing at 373 K, 423 K, 473 K, 523 K, 573 K, and 623 K under vacuum. The impact of thermal treatment on dark current behaviour, conduction mechanisms, electrode morphology, bulk and surface properties, and the Au–CZT interface is analyzed using current–voltage (I–V) measurements, optical and infrared imaging, X-ray photoelectron spectroscopy (XPS), and transmission electron microscopy (TEM). We show a large thermal instability of the interface owing to a decrease in surface stoichiometry and contact quality, leading to decreased electrical performance after annealing at 523 K.

4.1 Device processing and Analysis methods

Two distinct samples were sourced from a single In-doped CZT wafer grown by THM. The devices were fabricated according to the process flow outlined in section 3.2. Notably, an 8x8 Au pixel array was deposited by e-beam evaporation on the B-face of the (111)-faceted samples. At the same time, electroless Au deposition was used to deposit a blanket electrode on the A-face of the devices. Figure 4.1b depicts the device structure under test. The surfaces were CMP'ed down to a 0.05 µm alumina slurry prior to the metallization. Figure 4.1a shows the typical morphology of the CZT surface after CMP, acquired by AFM. The surface roughness is 0.6 nm (RMS). Regardless, polishing lines from the CMP process are still predominantly visible, but span a limited depth profile of 2-3 nm at most. While the presence of prominent defects at the surface was shown to increase dark current [40, 72] and promote charge trapping, maintaining surface stoichiometry and avoiding wet etching processes was deemed favourable [101]. The device duplication ensures steady performance statistics and the avoidance of detector performance singularities arising from defects.

4.1.1 Thermal processing

The thermal cycles were developed to resemble those of typical vacuum deposition methods [8]. Both samples were processed in parallel and subjected to the same thermal treatment. The devices were sequentially annealed under vacuum at 1.2×10^{-5} torr, at increasing temperatures, from 373 K to 623 K. An MTI Corporation VBF1200 Vacuum Oven coupled to a turbomolecular pump was used to conduct the annealing steps. The furnace temperature was regulated using an Eurotherm temperature controller. Table 4.1 details all annealing steps and conditions. First, the devices were loaded into a quartz ampoule, then pumped down to the working pressure. The temperature was increased to the target in 20 min., followed by a 30 min. treatment at the target. The temperature was ramped down for 10 min. at a rate of 2 K/min while venting the chamber with N_2. The samples were removed directly after

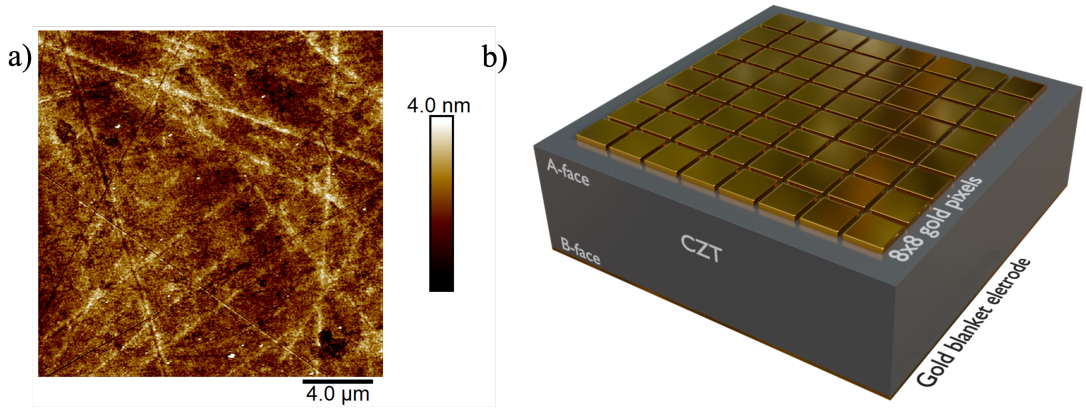

Figure 4.1 a)Typical surface morphology of the CZT prior to pixel deposition, measured by AFM. The surface was CMP'ed with 0.05 µm alumina slurry, yet still shows polishing lines of 2-3 nm depth. $R_{RMS} = 0.6$ nm. b) 3D rendering of the devices annealed. They are comprised of 8x8 gold pixels on the B-face, and a blanket gold electrode on the A-face.(dimensions not to scale)

the ramp-down segment. Due to furnace thermal capacity limitations, to avoid cracking, the ramp-up was limited to 10 K/min for steps #5 and #6. The steady temperature segment time was adjusted accordingly to maintain the total process time to, respectively, 65 min. and 70 min.

Table 4.1 Detailed sequential annealing steps. The annealing chamber was pumped down to 1.2×10^{-5} Torr for the process and was vented with N_2 during the ramp-down.

Step #	Annealing Temp. (°C - K)	Ramp up rate (K/min)	Annealing time (min)	Ramp down rate (K/min)	Total process time (min)
1	100 - 373	4	30	2	60
2	150 - 423	6.5	30	2	60
3	200 - 473	9	30	2	60
4	250 - 523	10	27	2	60
5	300 - 573	10	27	2	65
6	350 - 623	10	27	5	70

4.1.2 Characterization of the devices

After each annealing step, the devices were removed from the quartz ampoule for testing. The dark current of the devices was measured from -1000 V to 500 V, in steps of 5V, using a Keithley 2470 SMU (70 mA/cm^2 compliance) paired to a set of microprobes. The

I-V characteristics were acquired both in top-bottom and pair-wise configurations. The latter was used to asses surface leakage current. For top-bottom measurements, as shown in section 3.3.1, the devices were temporarily bonded to a copper tape to ensure proper contact with the back electrode. The voltage drop across the interface and barrier height lowering were assessed using the ITD theory, developed by Wu [3], itself inspired by the development of Cowley and Sze [45]. However, while the complete ITD equation, (2.10) has been shown to accurately describe carrier transport at the metal-CZT interface, the complete theory is comprised of too many free parameters, and is prone to over-fitting when used as is. Moreover, understanding the implications of each parameter, and specifically their impact on the conduction behaviour, is cumbersome due to their high level of cross-correlation. Principtato et al. developed a novel method to extract of decoupling the analysis of key parameters within the ITD model [47], namely, the interfacial voltage drop coefficient $\Gamma = 1 - C_2$ (C_2 was defined in section 2.1.4) and the ratio of diffusion current to thermionic current. They defined [47]

$$H(V,T) = \frac{k_b T}{eJ}\frac{\partial J}{\partial V}. \tag{4.1}$$

Applying this equation to (2.13) yields

$$H(V,T) = \frac{k_B T}{eV_D}\frac{\partial V_D}{\partial V}\frac{1}{1 + V_D/\theta_n V_R} + \Gamma. \tag{4.2}$$

A fundamental issue remains to determine the effective diffusion velocity of charge carriers V_D. Yet, due to the high voltage approximation, that is we have complete depletion of the bulk for applied voltage exceeding 70 V [46], we can approximate the electric field to be constant in the depletion region, and equal to its maximum value E_{max}, itself equal to the field at the cathode E_C [5, 6, 45],

$$V_D = \mu_n E_C, \tag{4.3}$$

where μ_n is the electron mobility (1000 cm^2 $\text{V}^{-1}\text{s}^{-1}$ [24]). Since $E_C \propto V/L$, defining $\alpha = \mu/L$ (a constant), equation (4.2) becomes

$$H(V,T) = \frac{k_B T}{eV}\frac{1}{1 + \alpha V/\theta_n V_R} + \Gamma, \tag{4.4}$$

To simplify the notation, we further define $\beta = \alpha/\theta_n V_R$ to obtain

$$H(V,T) = \frac{k_B T}{eV}\frac{1}{1 + \beta V} + \Gamma. \tag{4.5}$$

The two parameters Γ and β can be calculated to obtain the barrier lowering due to the voltage drop at the interface layer; a critical parameter to understand the transport mechanisms at the interface, and the ratio of diffusion current to thermionic current in the detectors $V_D/\theta_n V_R$ [3, 44, 46, 47]. Unless specified otherwise, the current shown is the mean value, acquired from over 10 pixels, spanning both devices.

The material characteristics of the devices were also investigated before and after the annealing sequence to assess their impact on the CZT's properties. Infrared microscopy was used to assess any variations in the position and density of extended defects, notably Te inclusions and dislocations. Optical microscopy, in conjunction with AFM, was used to investigate any changes in electrode morphology. Spectroscopic information regarding surface composition was acquired by XPS. The electrode edge profile was acquired by profilometry to assess the prevalence of sharp-edge effects on the dark current levels. Finally, interfacial properties were acquired by TEM, following FIB lamella preparation.

4.2 Results & Discussion

4.2.1 Electrical

First, the background current in dark conditions was measured up to the operation voltages of the CZT detector [25]. Figure 4.2a presents the complete I-V characteristics of the devices after each annealing step. Despite the thermal treatment, the rectifying function of the e-beam Au-CZT interface is maintained. Moreover, the devices exhibit no breakdown at voltages lower than 1000 V. Nevertheless, some small fluctuations are observed in both forward and reverse bias up to annealing temperatures of 473 K, becoming increasingly large thereafter. Figure 4.2b shows the mean and standard deviation of the dark current measured at -1000 V. The dark current is found to remain below 0.5×10^{-5} A/cm^2, with fluctuations remaining below 0.9×10^{-7} A/cm^2 up to annealing temperatures of 473 K. Onset dark current increase to $(0.6 \pm 0.1) \times 10^{-5}$A/cm^2 is observed after 523 K. A large dark current, $(2.0 \pm 0.6) \times 10^{-5}$A/cm^2 is observed after annealing at 573 K alongside large statistical fluctuations. A reduction in the average current follows after annealing at 623 K, but increased fluctuations are simultaneously observed, reaching $(1 \pm 1) \times 10^{-5}$A/cm^2. These degraded performances at high reverse voltage are further carried through to lower applied bias, with the dark current remaining systematically after annealing at 523 K. Furthermore, they exhibit a clear deviation from the ideal forward behaviour displayed up to annealing temperatures of 473 K. Indeed, the current is found to increase rapidly at 0^+ V,

but then plateaus up to 100 V. The plateauing current increases with annealing temperature.

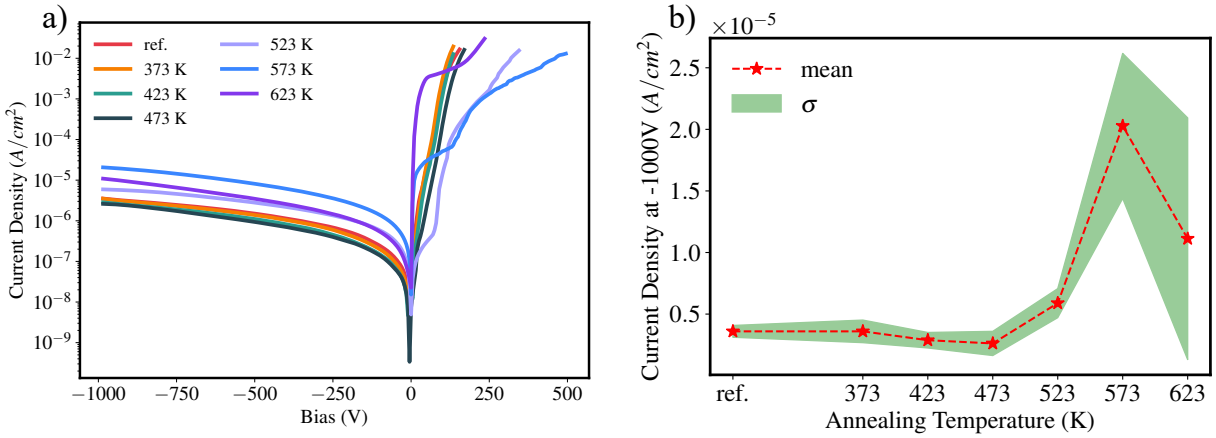

Figure 4.2 a) Experimental current density–voltage sweeps from -1000 V to 500 V. Sweeps were acquired using a Keithley 2470 SMU paired with micro-manipulators. Devices were tested after each annealing step. b) Mean and standard deviation of current density at -1000 V over both devices for each annealing step. The detectors exhibit a clear deterioration in performance after annealing at 573 K, as evidenced by both current levels and fluctuations from pixel to pixel.

Similar conclusions can be drawn from figure 4.3, which focuses on the reverse and forward bias operation of the detector, acquired in 1 V intervals to better highlight the variations at lower voltages, particularly in forward bias. In reverse bias, the observations are consistent with the high-voltage operation of the detector; a small reduction in dark current is observed up to 423 K, followed by a notable degradation of the performance at 523 K and onward. At first glance, we also note a consistent slope at 20 V_{rev}+ for annealing temperatures of 573 K and below; a shallower slope is observed after the last step. Section 4.2.1 shows the barrier height-lowering effect of the detectors. In forward bias, consistent performances are observed up to annealing temperatures of 423 K. Thereafter, a small reduction is observed at 473 K, yet maintaining consistent exponential behaviour. A systematic change in behaviour is observed after annealing at temperatures above 523 K. Indeed, the current saturates towards linear increases at increasing values of 2×10^{-7}, 1.5×10^{-5} and 3×10^{-3} A/cm^2 at 523 K, 573 K and 623 K respectively.

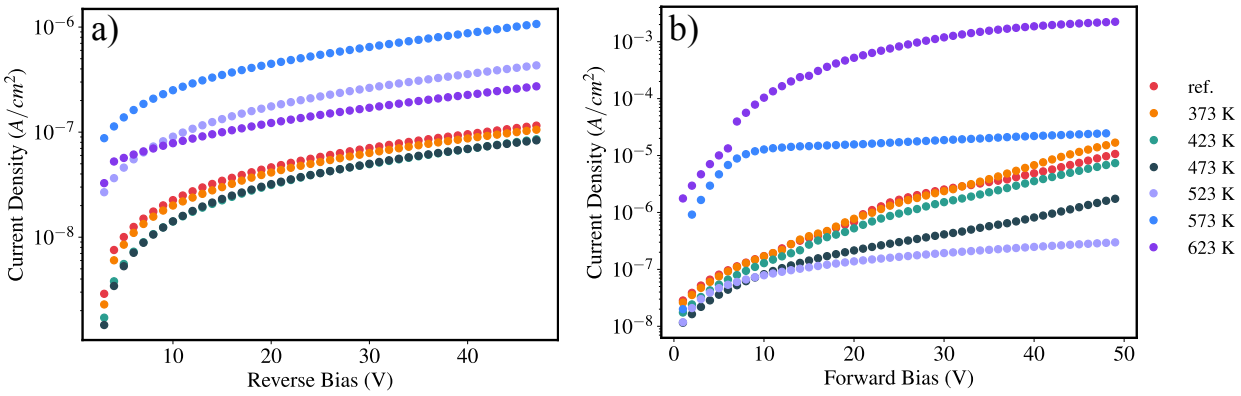

Figure 4.3 Dark current density in a) reverse bias, and b) forward bias after each annealing step. The devices present consistent performance in both regimes up to 473 K, after which a degradation of the performance is observed. Furthermore, while the forward current behaviour remains consistent up to 473 K, a systematic change in behaviour is observed thereafter.

Barrier height lowering

To determine the effects on interfacial behaviour on the current transport mechanisms after each annealing step, the H-function (4.1) was applied to the high reverse voltage I-V measurements shown in figure 4.2a. Equation (4.5) was then fitted to the dataset to determine the barrier-lowering factor Γ. We note a reasonably good fit to the measured data up to E-fields of 4000 V/cm, after which large fluctuations, accentuated by the derivatives, are observed. As such, the fit was performed on the "ideal" voltage section, which is higher than 1000 V/cm to ensure the complete depletion approximation is valid, and below 4000 V/cm. Figure 4.4a presents the acquired reference data as well as those acquired after annealing at 573 K and 623 K. Their fit are also shown alongside the Γ value for all annealing steps. Furthermore, the absence of diffusion current, only thermionic current is observed, and the H-function tends towards a steady value $H(V,T) = \Gamma$. To determine the point at which the current is only thermionic emission limited (TE-point), the fitted functions were extrapolated to higher electric fields, as shown in figure 4.4b. The fit uncertainties are also displayed. The barrier-lowering factor is found to systematically increase for increasing annealing temperatures. Nonetheless, a clear upward trend in interfacial voltage drop is calculated. Table 4.2 summarizes the calculated Γ values. We observed that, despite the upwards trend, large uncertainties in the H-function fit, owing to fluctuations in the experimental data, undermine the information provided due to significant overlap between several annealing steps. It is worth noting that the source of uncertainties lies solely in the fitting parameters, and does

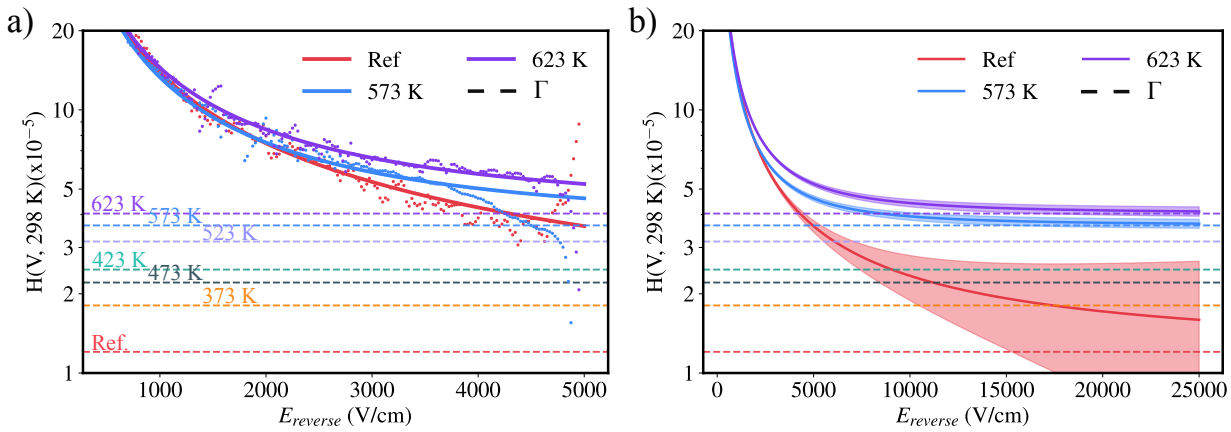

Figure 4.4 Evaluation of the reverse bias parameter by H-function (4.1). The function was applied to the datasets. Equation (4.5) was then fitted to extract the barrier-lowering factor Γ and the ratio of diffusion current to thermionic current. The fit was performed from 1000 V/cm to ensure the complete detector depletion approximation was valid, to 4000 V/cm, from where instabilities were observed. a) presents the original data and fit, alongside the Γ steady point for each annealing temperature. b) extrapolates the fitted curves, with uncertainties, to higher fields. An annealed device tends to thermionic emission faster, and at a lower temperature than the reference. The latter further shows higher uncertainty, owing to large fitting errors in the diffusion/thermionic current factor

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not propagate from device uncertainties. Thus, the uncertainties in the values calculated at 523 K and above may be largely underestimated.

Table 4.2 Calculated barrier height lowering coefficient Γ from experimental data.

Temp. (K)	Γ
Ref.	1 ± 2
373	2 ± 3
423	2 ± 2
473	2.21 ± 0.07
523	3.2 ± 0.1
573	3.6 ± 0.2
623	4.0 ± 0.2

Whilst an accurate assessment of the thermionic emission to diffusion current ratio would provide great insights into the interfacial behaviour after each treatment, the method was found not to be robust enough to provide an accurate reading of this metric, particularly in the case of devices subjected to treatment at 473 K and below. Thereafter, the acquired data

showed fewer fluctuations in the H function. Regardless, the thermally treated sample tends to steady H-function, and thermionic emission limited current, at a lower applied electric field than untreated samples, as depicted in figure 4.2b. Uncertainties aside, the reference sample is measured to reach steady state at E $\geq$ 25 kV/cm. On the other hand, after annealing at 623 K, the H-function flattens around 15 kV/cm.

Surface leakage current

Pair-wise I-V measurements were performed to assess the surface leakage current of the device, and to provide the ability to decouple possible effects from the back electroless contact on the device performance. The pair-wise current measurements were performed by measuring the current voltage characteristics between pixel pairs, at increasing distance, as illustrated in figure 4.5b. The pairs were sequentially tested from I-II to I-VIII, effectively in a back-to-back (B2B) Schottky configuration, where the current is effectively limited by the reverse-biased junction. Figure 4.5a reports the dark current measured between pixel-pairs I-II at 180 V. Similar to the top-bottom configuration tests, current levels within normal fluctuations are measured consistently up to annealing temperatures of 423 K, oscillating between 5 nA and 8 nA. The current then plummets to 2 nA after annealing at 473 K. The current marginally increases at 523 K, then sharply at 573 K. While these observations do not correlate directly with those measured in the top-bottom configuration, they exhibit reasonably close behaviour accounting for the impact of both the reverse- and forward-biased junctions. Contrariwise, the measured current at 623 K, 2.2 nA, departs from expectations.

The current decay for pixel pairs increasingly further apart is displayed in figure 4.5c. The current values were normalized to the current between pair I-II for each annealing temperature. At first glance, the decay rate between pixel pairs is faster for annealing temperatures of 473 K and below. An inverse exponential function $I_{tt,norm} = \exp\{-bV\} + A$, where b it the decay rate and A is an hypothetical interface-limited current such that $\partial I/\partial X_{I-K} = 0, K \in \{II, III, ...\}$ is independent of distance, yet its physical interpretations are not concrete. In any case, table 4.3 summarizes the fit parameters. Up to 473 K, the decays are found to follow an inverse exponential rule. However, the decay is better modelled by a linear function at 523 K and onward.

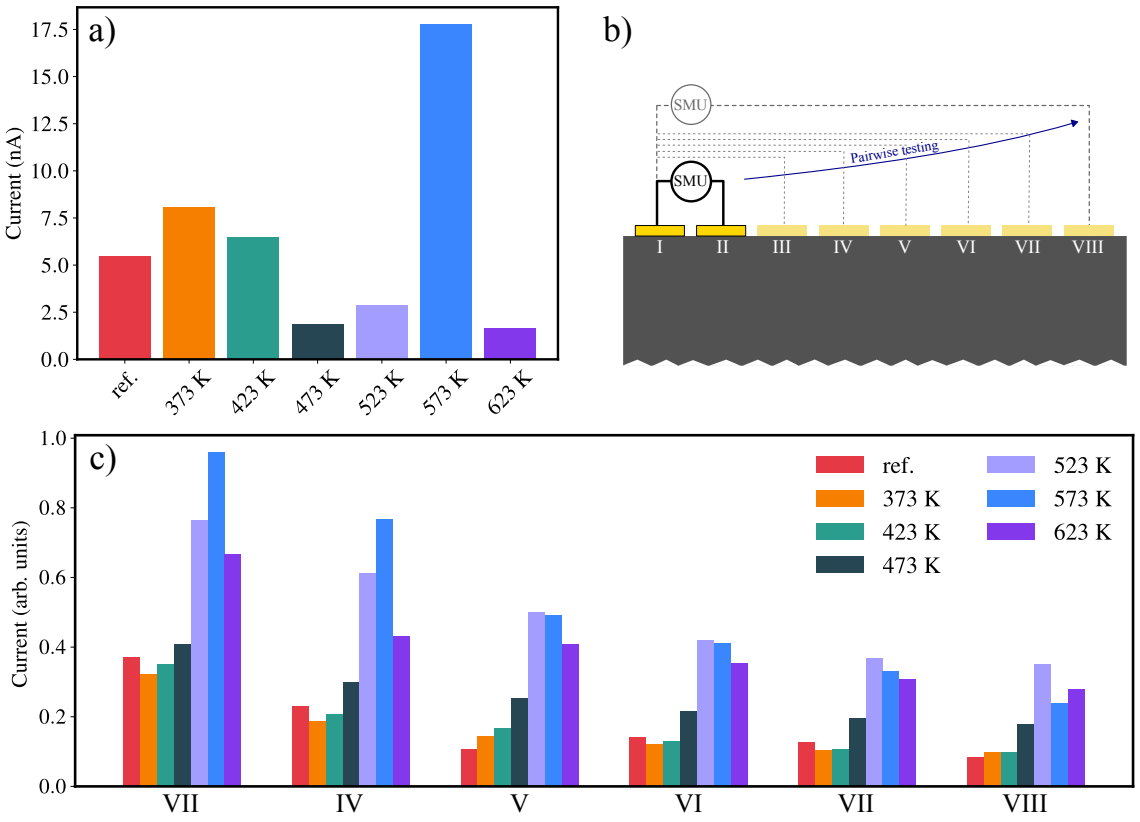


Figure 4.5 Pairwise dark current at 180 V. b) Schematic of the testing setup. Pixel pairs were tested as such: I-II (pictured), I-III, . . . , I-VIII. a) Dark current of pixel pair I-II. c) Dark current of pixel pair I-III to I-VIII normalized to the current measured between pixels I and II. After annealing at 573K, not only was the dark current 17.5 nA for pixel pair I-II, compared to 5 nA for the reference, it also presented the slowest decay in current for successive pairs.

Table 4.3 Pairwise current decay fitting parameters, as modelled by $I_{tt,norm} = \exp\{-bV\} + A$.

Temp. (K)	Decay rate (b)	A
Ref.	1.1	0.08
373	1.4	0.09
423	1.2	0.09
473	1.2	0.2
523	0.16	-0.03
573	0.24	0.06
623	0.24	-0.05

4.2.2 XPS spectroscopy

XPS was used to acquire the surface compositional ratios before and after all annealing steps. The spectra were acquired on the edge of the device; that is, away from the gold electrodes. The analysis positions were sputtered using Ar to clean the surface of any contaminants before the spectra were recorded. Figure 4.6 shows the elemental peaks of Cd_{3d} (a), Te_{3d} (b) and Zn $_{2p}$. We note a decline in count/s for both the Cd_{3d} and Te_{3d} after sequential annealing. On the other hand, the Zn $_{2p}$ is found to double. The resultant elemental compositions are summarized in table 4.4. The at.% of Zn is found to increase to 16.8% from 7.6%. Simultaneously, the Te and Cd at.% are found to decrease by 6.7% and 2.5%, respectively. This suggests the supplemental Zn accumulation at the surface is not due to a Zn substitution in Cd interstitial sites in the crystal matrix, but simply to a supplemental Zn migration to the surface during the process. The self-diffusion process of Zn within the CZT matrix is rather complex, and has been shown to be driven by native defects concentration, rather than stoichiometric deviations [102–104]. However, the studies suggesting these driving forces have been carried out at higher temperatures and pressures. As such, elucidating the driving forces behind Zn surface enrichment and the conditions of the present study necessitates further research.

Table 4.4 Elemental composition in atomic percentage for different samples.

Sample	Cd_{3d} (at.%)	Te_{3d} (at.%)	Zn_{2p} (at.%)
Ref.	40.1	52.3	7.6
623 K	37.6	45.6	16.8

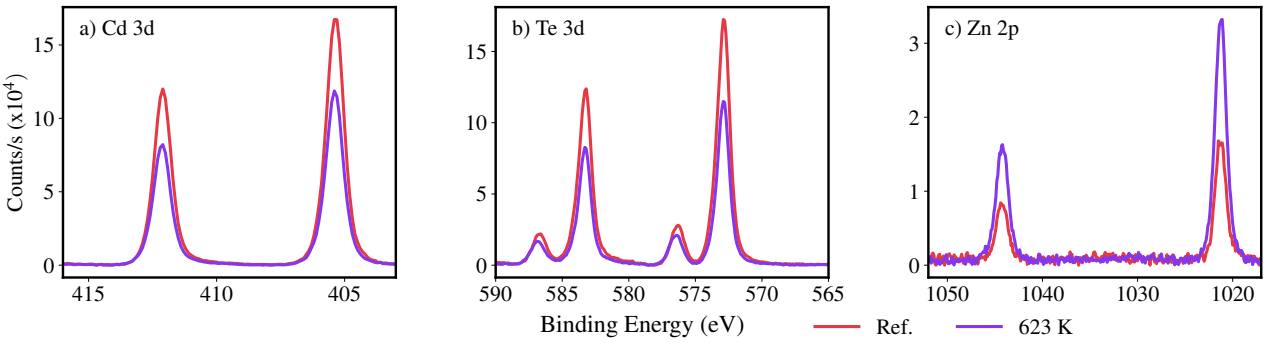


Figure 4.6 XPS spectra of the CZT surface before and after all sequential annealing steps. Showing a) the Cd_{3d} peaks, b) the Te_{3d} peaks, and c) the Zn_{2p} peaks. While a marginal difference in Cd at.% is measured, a significant Te at.% reduction is observed as a result of an increase in Zn at.%. *Measurement and data processing performed by Dr. Sudarshan Singh*

4.2.3 Optical microscopy

Optical imaging was employed to monitor morphological changes on the device's CZT surface and e-beam Au pixels, arising from the annealing sequence. The optical images of the e-beam-deposited gold pixels, shown in figure 4.7a–c, reveal significant changes in pixel surface morphology induced by annealing. Prior to annealing (figure 4.7a), the electrodes appear uniform, exhibiting smooth surfaces consistent with the morphology expected from high-quality e-beam deposition. Following annealing (figures 4.7b–c), the electrode surfaces become distinctly roughened and are uniformly covered with dot-like structures, particularly along the CZT's native polishing lines. As further evidenced by AFM, this morphological shift corresponds to a transition from a low-roughness surface (figure 4.7d, Rq = 1.0 nm, Z-range = 25 nm) to a highly degraded surface (figure 4.7e, Rq = 3.3 nm, Z-range = 111 nm) populated by pit-like features approximately 1 µm in diameter. Additionally, post-annealing imaging reveals the propagation of pre-existing CZT defects through the electrode layer. As illustrated in figure 4.7c, a Te inclusion originating from the CZT substrate appears to breach the gold contact layer. This "punch-through" defects lead to localized surface deformations and visibly alter the morphology in the immediate vicinity of the affected pixels.

Potential evolution of the CZT bulk and growth-inherent extended defects was assessed by infrared (IR) microscopy. Due to its large bandgap, CZT has very little absorption in the infrared window. As such, bulk and surface defects, notably Te inclusions, appear dark due to their higher absorption. Figure 4.8 presents images acquired before (4.8a, 4.8b) and after (4.8c, 4.8d) annealing, at the same location and magnification. Images 4.8a and 4.8c are

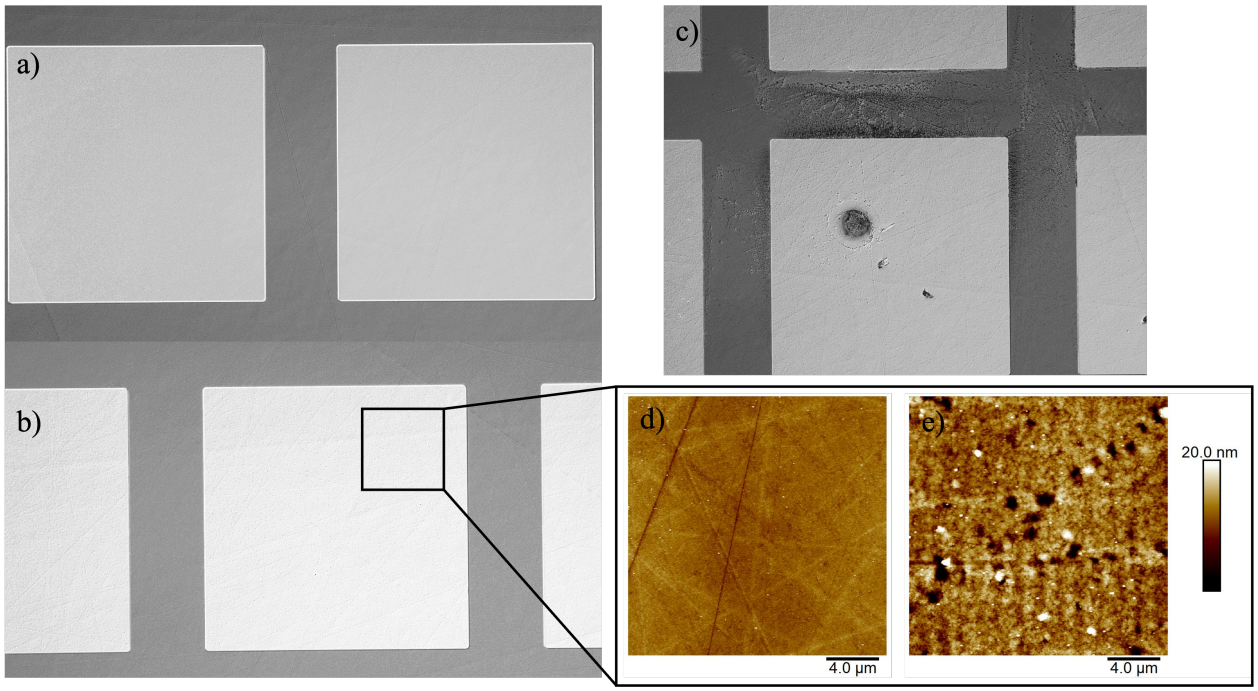


Figure 4.7 Optical images acquired a) before, and b), c) after all annealing steps. The pixels show noticeable degradation after the thermal process. We observe dot-like structures throughout their surface, with an increased density along polishing lines (b). Defect "punch-through" is also observed, leading to noticeable morphological changes to the pixel and its immediate vicinity. d) AFM morphology of the Au pixel prior to annealing (R_{RMS}=1.0 nm). e) AFM pixel morphology after annealing (R_{RMS}=3.34 nm).

focused at the surface, while 4.8b and 4.8d capture the bulk of the crystal. Variation in the sharpness and illumination pre- and post-annealing images are attributed to changes in the imaging system. Indeed, the pre-annealing images were acquired in reflection mode using an InGaAs camera and halogen illumination, thereby revealing the prominent back electrode defects visible in figure 4.8b. Images post-annealing were recorded in transmission mode using an IR microscope equipped with a halogen bulb and an infrared camera (COHU solid-state camera 4815), which provided better focal point control but slightly worse resolution. Regardless, no noticeable changes are observed after annealing; there are no recorded variations in the density, position nor dimensions of the Te inclusions.

4.2.4 Electrode edge profile

The pixel's edge profiles were measured using a Dektak profilometer, as shown in figure 4.9. It is widely known that the sharp edges surrounding the metal electrodes are a major contributor to surface leakage currents and dark current [6]. Indeed, the sharp edges induce

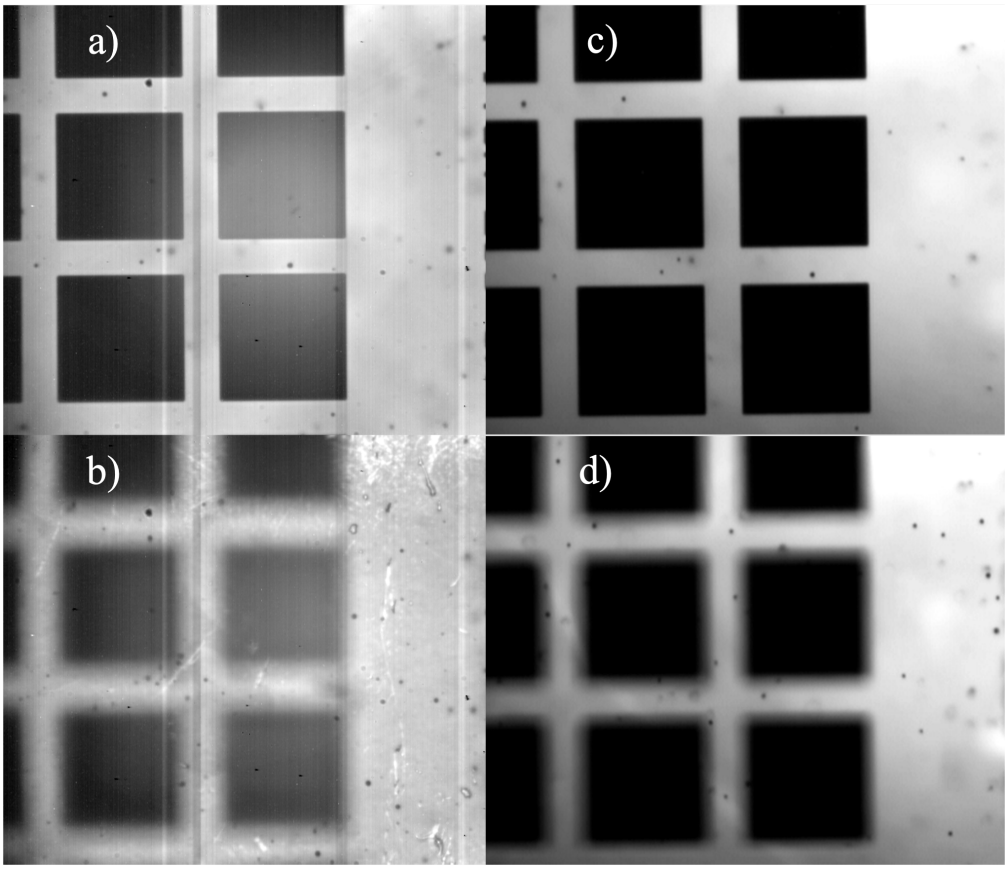


Figure 4.8 IR images obtained in transmission mode. a), b) before and c), d) after all annealing steps. Neither the density nor the sizes of tellurium inclusions were impacted by the processes. The images were acquired on the same device, in the same region. The camera was changed between both acquisitions, owing to the difference in focus and clarity.

curvatures in the depletion region due to locally high electric field; contributing to large edge currents in reverse bias; this effect is referred as sharp-edge effect by Sze [6]. However, due to the dimensions of the pixels in the present situation, it is uncertain whether this effect is marginal or not. However, this effect can be considered negligible in the present case, as no noticeable change in the edge profile was observed after any of the treatments, as shown in figure 4.9.

4.2.5 TEM

TEM has remained the gold standard to observe interfacial quality and interfacial composition of metal-semiconductor structures. By extracting a very small lamella from the sample, the analyzed sample becomes virtually transparent to electrons, and structure down to the nanometre size can be observed [105]. The process to fabricate the lamella first consisted of

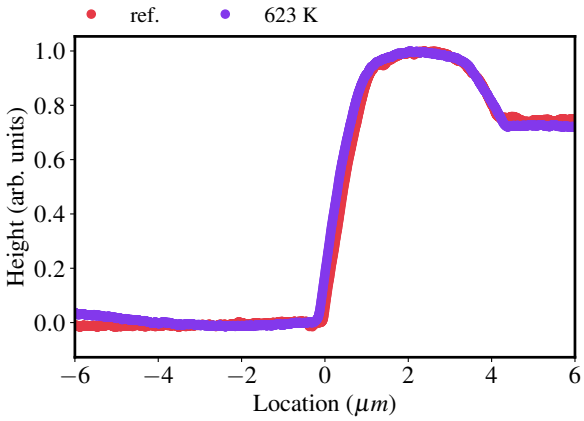


Figure 4.9 Pixel electrode edge profile as measured by profilometry (Dektak). The total heights were normalized due to small fluctuations between samples. Despite all treatment, the edge profile remains intact.

protecting the sample from the extensive ion milling. As such, carbon was first deposited onto the sample to create a contrast barrier before Pt was deposited to protect it during milling. Lamellas were then milled out of the zone of interest using focused ion beam (FIB) and placed on a Cu TEM grid using Pt as adhesive. Both sides of the lamella were thinned down to a thickness varying between 60 nm and 100 nm. The final ion milling was performed at 2 kV to minimize excessive surface damage. Finally, the TEM images were acquired with a JEOL JEM-F200, MET-CFEG, operated at 200 kV. EDS maps of the interface were also acquired using the same microscope with two JEOL JED-2300 Dry SDD EDS detectors providing an energy resolution of 127 eV, and processed with *DigitalMicrograph* software from Gatan.

Figure 4.10 shows all images and EDS spectrum acquired by TEM before (4.10a, 4.10c) and after the annealing process (4.10b, 4.10d) The CZT surface prior to any processes is shown to be highly defective, whether it be under deposited electrodes or not [106]. Specifically, many dislocations are observed close to the surface, to a depth varying between 200 nm and 600nm. Thereby, these defects are not induced by metal deposition, but are attributed to the polishing processes and shallow alumina particles indentation, also owing to the polishing lines observed in figure 4.1a [41]. No evolution of these defects is recorded after the annealing process, as shown in figure 4.10c. The variation in Au thickness is attributed to fabrication fluctuations. It is found to be polycrystalline in both cases.

On the contrary, the EDS map following the annealing process shows a distinctive compositional evolution at the interface, as compared in figures 4.10b and 4.10d. Despite exhibiting consistent compositional ratios in the bulk, we note an increase in Zn concentration at the Au electrode surface, coupled to a nm-thick Zn-depleted zone at the interface. The catalytic nature of Au in enhancing solid-phase diffusion processes has been widely recognized [107], often necessitating the implementation of diffusion barriers in microfabrication processes [108]. It is impossible to distinguish possible AuZn binary phases [109], whether it be pre- or post-annealing, due to the strong Zn background signal owing to a partial overlap of the Au and Zn spectral peaks.

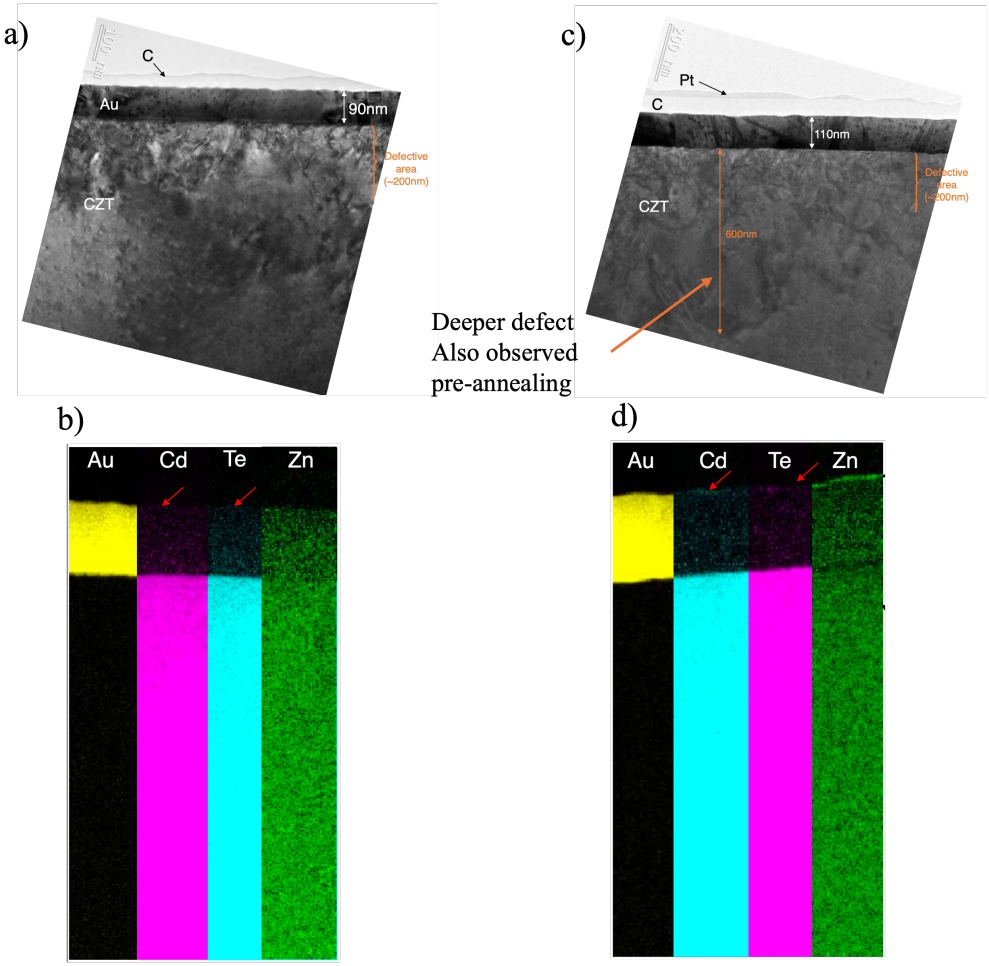


Figure 4.10 Interfacial characterization of the e-beam Au-CZT interface by TEM. a) TEM image pre-annealing showing CMP-induced defect below the Au pixels. b) EDS map of the interface pre-annealing. c) TEM image post-annealing, no additional defects or defect annihilation are observed. d) EDS map of the interface post-annealing. We note a Zn migration to the pixel's surface, leading to a Zn depletion zone in the nm below the pixel. *Lamella preparation, image acquisition and processing performed by Dr. Éloïse Rahier.*

4.3 Discussion - Interplay between electrical behaviour and material modifications

While a direct correlation between device electrical performance and the material characteristics modified through the annealing process cannot yet be firmly established, the data presented here offers valuable insight into interfacial dynamics, stability, and their impact on device behaviour after thermal annealing. Three primary contributors can be proposed for the observed changes in electrical performance: modifications at the e-beam-CZT interface, alterations to the CZT bulk properties and variations at the electroless Au-CZT interface.

4.3.1 Bulk modifications

While bulk modification effects cannot be entirely excluded, they are considered unlikely under the experimental conditions described herein. The total thermal energy supplied to the samples in vacuum remained fairly low, and the temperature range reached remains insufficient to induce significant bulk atomic rearrangements in CZT, with typical temperatures employed during the post-growth ingot annealing phase ranging between 600°C and 850°C [22, 110]. This interpretation is further supported by IR transmission images, which reveal no discernible differences in the density, size or spatial distribution of Te inclusions after the annealing sequence. Literature also supports the hypothesis of surface-only changes under similar conditions, with reports of devices recovering their initial performance simply through surface polishing and reprocessing [98]. These findings strongly suggest that the driving forces behind the observed electrical variations originate from the evolution of interfacial characteristics rather than modifications to the CZT bulk.

4.3.2 Distinct electrode contributions

It is plausible that modifications to both devices' contacts contribute to the evolution of the device's dark current throughout the annealing sequence. Possible oxidation of the interface and Au interlayer diffusion have been previously advanced to stem similar observations [96]. Considering the diffusivity of Au in CZT is given by [100]

$$D_{Au} = 9 \times 10^{-3} \exp\left\{\frac{-1.7}{kT}\right\}, \tag{4.6}$$

gold diffusion at 623 K is calculated to be 1.6×10^{-16} cm^2/s. Whilst the diffusivity is considerably larger at 623 K than at 423 K by 7 orders of magnitude, TEM-EDS measurements confirm no significant Au intermixing in the CZT matrix even after all thermal steps. These

results are consistent with those from other TEM interfacial microanalyses after thermal treatment [100]. Regardless, due to the inherent intermixing of Au arising from the electroless process, any additional Au diffusion should only marginally impact performances. Moreover, the vacuum annealing conditions should inhibit possible oxidation scenarios of the contacts. These observations shift the focus towards the top interface, where the Au pixel deposited by e-beam appears to be more sensitive to morphological and chemical changes during annealing. As evidenced by AFM and optical imaging, figure 4.7, the smooth pre-annealing surface undergoes substantial roughening, with widespread formation of nanoscale pits and defect propagation from the CZT substrate, indicating interfacial degradation that may drive electrical changes.

4.3.3 Variations of electrical performances

In reverse bias, the current–voltage behaviour suggests a fluctuating barrier height throughout the whole process. Indeed, the initial current reduction is consistent with an increase of the Schottky barrier, though the large uncertainties associated with interfacial voltage drops prevent a precise quantification. After annealing at 473 K, the increase in current, alongside higher current variability, suggests a barrier height reduction, potentially driven by defect proliferation at or near the interface. The Zn depletion below the Au pixels measured after the complete sequence leads to a reduction of the effective barrier height ($E_{g,CZT} = 1.57$ eV, $E_{g,CdTe} = 1.44$ eV [24]), thus allowing for the conduction of lower-energy carrier to go through the barriers, enhancing carrier injection. This interfacial compositional change impacts several of the parameters considered when calculating the reverse bias Schottky barrier height from equation (2.14), notably the bandgap, electron work function, interface state energy, $\chi_2^{1/2}$ and $C_2 = 1 - \Gamma$ to only name a few.

It remains challenging to decouple the lowering of Γ from the parameters influencing it, particularly given that interfacial dielectric properties and state densities are difficult to probe directly post-process. TEM imaging suggests compositional variation at the interface, possibly tied to shifts in the effective dielectric constant. However, the changes may also be driven by an increase in interface state density and/or an increase in interfacial layer thickness. Although our extraction method likely underestimates Γ, in contrast with other techniques such as that employed in [33, 47], the obtained values fall within the typical range reported for CZT detectors (1×10^{-5} to 1×10^{-3}) [3, 33, 47, 81, 82]. Importantly, while earlier works, such as [5, 6], emphasized Fermi-level pinning as a dominant mechanism in Schottky barrier formation, our results align more closely with the view that the barrier height in CZT detectors

is primarily governed by the metal-semiconductor work function difference.

Though forward bias behaviour is not the primary focus of this study, it provides complementary insight into conduction mechanisms. Up to 473 K, the small current lowering in forward bias supports the hypothesis of increased barrier height derived from the reverse bias analysis. Above 523 K, however, current levels plateau, suggesting the onset of recombination-limited transport, driven by an increased density of carrier traps in the depletion region [5, 6]. The precise role of contact quality degradation in this regime remains unclear. One possibility is that surface defect propagation under annealing, such as Te inclusion punch-through, disrupts the local electric field distribution, but this cannot be confirmed without further structural analysis. Alternatively, interfacial compositional changes such as Zn depletion, be it nm-thick, can change the weighting potential applied to charge carriers due to band offsets, and induce non-ideal conduction behaviour [6, 111].

SLC

A spike in SLC after annealing at 573 K suggests a decrease in sheet resistivity, which appears to be restored after annealing at 623 K, possibly due to the oxidation of the Zn-rich layer and the resulting increase in resistivity. More notably, a change in conduction regime is observed: up to 473 K, the reverse current follows an inverse-exponential trend, while after annealing at 523 K and onward, the current decreases linearly with distance. This indicates a sudden shift in the current-limiting mechanism. Understanding the specific factors responsible for this transition would require detailed analysis of current pathways, which is a challenging task given the defect-prone micron-thick top surface of CMP-processed CZT.

CHAPTER 5 PHYSICAL PASSIVATION AND BARRIER ENHANCEMENT LAYERS FOR IMPROVED CZT X-RAY DETECTORS

The need to control the surface depletion layer and band bending inherently caused by surface and interface dangling bonds, as discussed in section 2.1.3, becomes paramount when aiming to reduce the dark current in CZT detectors. Electronic passivation is a convenient and cost-effective way to restore the performance of semiconductor-based devices with sub-optimal surface state density [112, 113]. First, electronic passivation works by saturation of the dangling bonds at the surface [111]. Second, the passivation layer counterbalances the accumulation of carriers at the surface by the formation of a depletion width that ensures charge neutrality and neutralizes free carriers, effectively preventing band bending and maintaining surface resistivity [111]. In addition to these charge neutralization properties, passivation layers can also be used to enhance the rectifying behaviour of Schottky interfaces between the substrate and the metal contacts (granted that proper band alignment is obtained) [5, 113], effectively creating a Metal-Insulator-Semiconductor (MIS) device.

Typically, CZT detectors are passivated using wet-etching methods followed by a wet passivation process, predominantly using Br-based solutions [79]. The process of Br etching and passivation is discussed in section 3.1.3 alongside the method's drawbacks and advantages. In short, this method, like many wet processes, does not provide a high level of control over the resulting intrinsic oxide layer due to its dependence on the initial states of the substrate. Also, the oxide layers have been shown to be unstable over time. As such, physical passivation has emerged as a promising candidate to overcome the instability of wet processes [80]. The deposition of thin films to achieve surface passivation allows to have full control over the passivation compound's composition, independently of the substrate's composition or defects. Moreover, the fabrication of an MIS structure has the potential to simultaneously passivate surface defects, while also serving as a carrier blocking layer at the metal-semiconductor interface, as shown in figure 5.1 [6, 44, 113]. The latter illustrates the barrier enhancement property of thin insulating layers on n-type semiconductors. Notably, the insulating layer should be thin enough to allow the conduction of charge carriers with high enough energy, thereby avoiding acting as a capacitor, while blocking the injection and collection of low thermal energy electrons that contribute to the dark current. [113]

Figure 5.2 highlights the key device processing steps implemented to reduce the prevalence

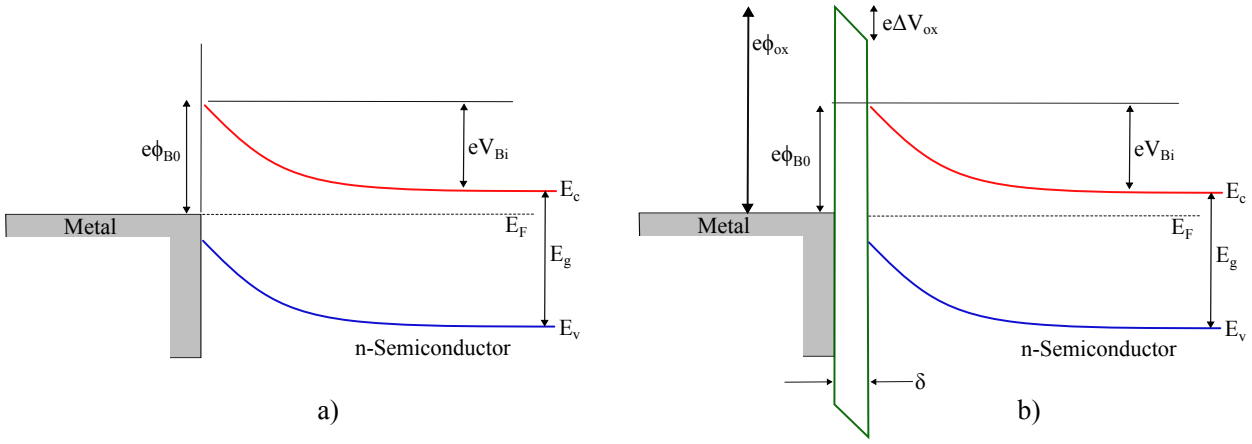


Figure 5.1 Theoretical equilibrium band alignment of metal-semiconductor (n-type) interface without (a) and with barrier enhancement layer (b), forming a MIS structure. The illustration does not include non-ideal effects such as surface states and image force lowering for clarity. Band alignment inspired form [6].

of surface and interface defects, thereby reducing dark current. The predominant processes for improving the performance of CZT detectors have remained polishing and wet processes, such as etching and oxidation; discussed in section 3.1.3. Moreover, none have exhibited widespread adoption by the community like NH_4F/H_2O_2 oxidation of Br-etched surface [79]. Nonetheless, a handful of groups have proposed and demonstrated the usefulness of inter-contact physical passivation by deposition of insulating layers on CZT. In 1999, Mescher et al. [87] showed a 3 nA reduction in dark current, from 4.5 nA to 1.5 nA, at 100 V after depositing 100 nm of SiN_x in between strip electrodes. The dielectric's deposition was done by reactive RF magnetron sputtering. They simultaneously measured an increase in the sheet resistance of the CZT Br-etched surface from 1 GΩ/square to 460 GΩ/square [87]. Diamond-like Carbon (DLC) thin films were deposited by Min et al. [114] due to the possibility of depositing quality dielectric at a temperature of 200°C [115]. Different thicknesses were deposited, with the thicker oxides leading to lower dark current [114]. Zannetti et al. [116] investigated the use of Al_2O_3 between drift-strips electrode to minimize surface leakage current (SCL). They showed an increase in the sheet resistance to 2000 Ω/square, compared to 120 Ω/square for the wet-passivated surface. At 50V, the dark current was shown to be reduced to 5.4 nA from 37 nA for wet-passivation [116]. The deposition of dielectric barrier enhancement layers has not been thoroughly evaluated in the community, yet blocking layers have been explored by Voss et al. [12]. a-Si was deposited on the anode side to act as an electron blocking layer. a-Se was deposited on the cathode side to act as a hole-blocking layer. Metal contacts were deposited thereafter. The band alignment of the layers with respect to CZT is shown in figure 5.3. A decrease in the dark current is shown, alongside the carrier

blocking effectiveness of the layer. However, the current level is shown to be on par with electrodes deposited on polished CZT.

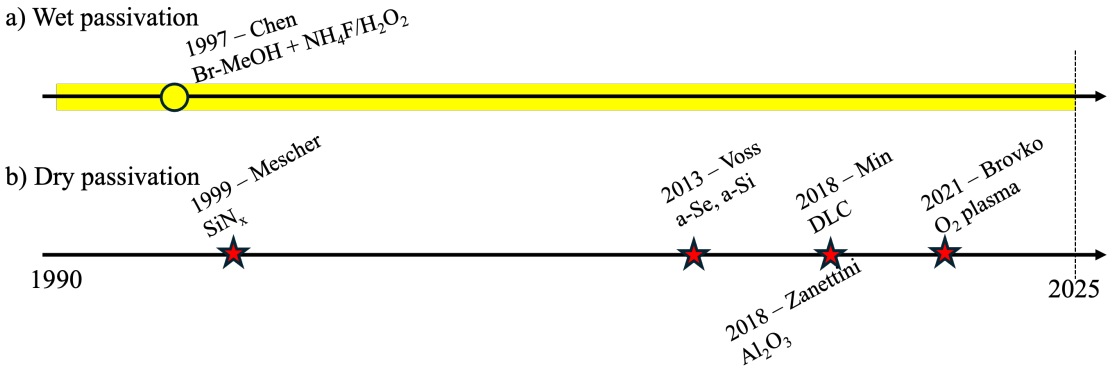


Figure 5.2 Implementation timeline of key processing steps to reduce the prevalence of surface and interface stated through a) wet processes and b) dry processes, on CZT detector's performance. While polishing and wet passivation have been key to the development of detectors for the past 35 years, only a handful of studies have proposed dry passivation.

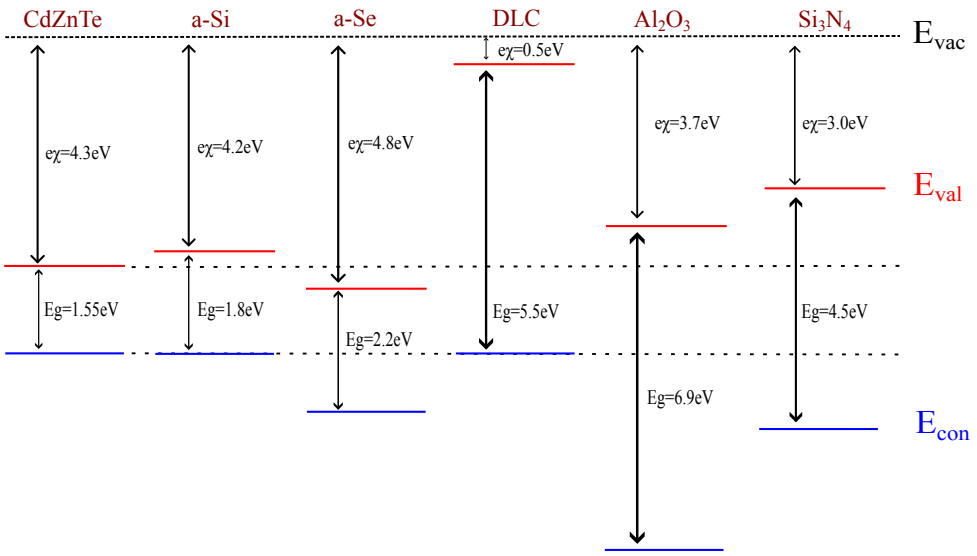


Figure 5.3 Theoretical band alignment of the thin film compound used for passivation of CZT detectors. [9–14]

In this study, the passivation capacity of SiN_x thin film deposited by reactive RF magnetron sputtering is investigated. The deposition of these compounds requires no extrinsic substrate heating to achieve good deposition *a priori*, and thereby the processing should maintain the

intrinsic performances of CZT, as outlined in chapter 4. As shown in figure 5.3, SiN_x presents optimal band alignment with CZT, suggesting it could serve as both an electron and a hole blocking layer, while also passivating dangling bonds. Al_2O_3 also presents a promising band alignment, and was explored by my colleague.

Several device architectures are developed, namely devices with simple interpixel passivation, MIS devices, as well as a combination of both. The impact of passivation on the detector's dark current is measured by measuring the high voltage current. First, an overview of the different devices is presented in section 5.1. Second, their electrical characteristics are shown in section 5.2. Finally, the passivation capacity of the deposited SiN_x is assessed and discussed in section 5.3.

5.1 Device processing and structures

Fourteen devices were fabricated in this study, many of which were fabricated on CZT sourced from two different ingots. Section 5.1.1 first compares the different CZT wafers used. Section 5.1.2 then outlines the specific device structures and electrode configurations developed in this study. Finally, section 5.1.3 discusses the process of SiN_x insulator deposition and characterization.

5.1.1 CZT variability and characteristics

The wafers used to complete this study were sourced from 2 different generations of wafers supplied by 5N+. Table 5.1 presents the main characteristics of both. Figure 5.4 presents the main differences between both wafers, as well as their surface morphology measured by AFM. Wafer A was MP while wafer B was CMP using an acidic 50 nm alumina slurry, owing to their roughness differences spanning an order of magnitude. Wafer A shows a surface roughness of 3.2 nm (RMS) and wafer B shows a roughness of 0.6 nm (RMS) for a 20x20 μm^2 area. Wafer A also shows a surface roughness of 3.0 nm (RMS) and wafer B and roughness of 0.6 nm (RMS) for a 5x5 μm^2 area. While both wafers are (111)-face, they also differ in thickness, metal choice, and doping. Wafer A is 2.30 mm thick and wafer B is 2.08 mm thick. Electroless deposition was used to deposit blanket electrodes on the A-face of both wafers (as-supplied); Pt was deposited on wafer A, and Au on wafer B. Whereas wafer B is known to be In-doped (n-type), no data was supplied for wafer A.

IR microscopy was used to assess the crystal quality and density of defects within both wafers. Due to its large bandgap, CZT has very little absorption in the infrared window. As such, bulk and surface defects, notably Te inclusions, appear dark due to their higher absorption.

Table 5.1 Characteristics of both wafers used to conduct this study. Both wafers were diced such that their surface crystal orientation is (111).

Wafer	Known composition	Doping	Metallization process	Surface preparation	Surface roughness
A	$Cd_{0.9}Zn_{0.1}Te$	Unknown	Electroless Pt on A-face	MP	3.2 nm (RMS)
B	$Cd_{1-x}Zn_xTe$	Indium	Electroless Au on A-face	CMP	0.6 nm (RMS)

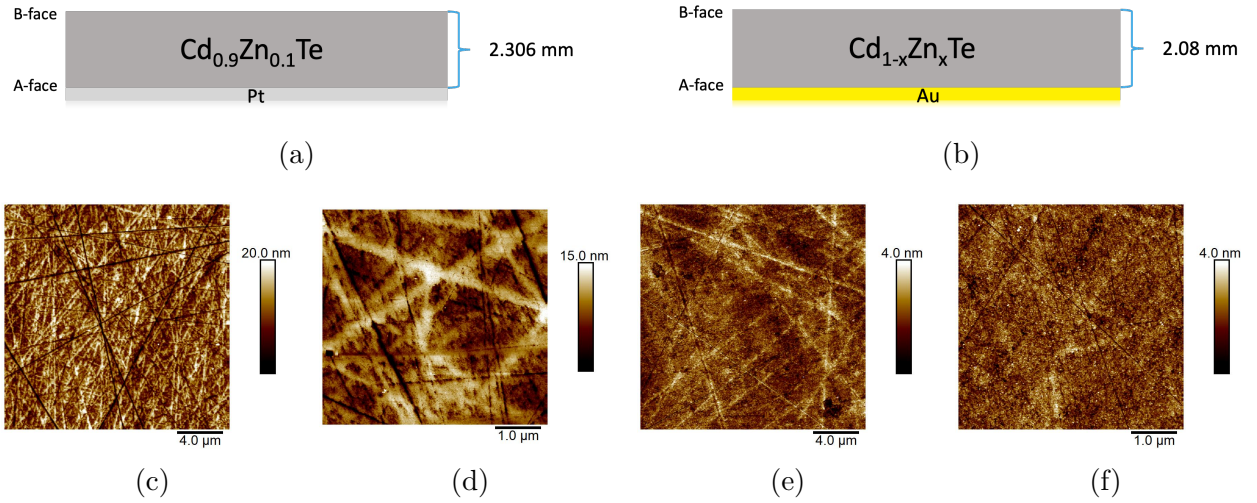
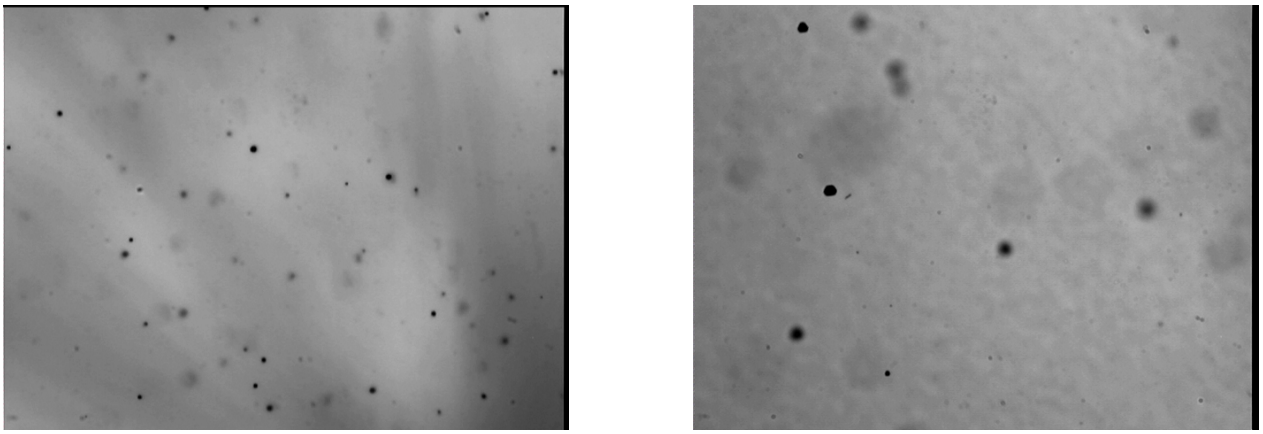


Figure 5.4 a) Side profile schematic of wafer A. b) Side profile schematic of figure B. Surface morphology of the wafers, measured by AFM; c) 20x20 µm^2 of wafer A (R_{RMS}=3.2 nm); d) 5x5 µm^2 of wafer A (R_{RMS}=3.0 nm); e) 20x20 µm^2 of wafer B (R_{RMS}=0.6 nm); f) 5x5 µm^2 of wafer B (R_{RMS}=0.6 nm).

The infrared images of the CZT samples were recorded in transmission mode using an IR microscope equipped with a halogen bulb and an infrared camera (COHU solid state camera 4815), as shown in figure 5.5 Both images were acquired at the same magnification. The density of Te inclusions in wafer A was shown to be higher than its counterpart, yet the size of the inclusions in the latter is larger. Non-uniformity in the Pt back electrode of wafer A is the cause of background fluctuations in figure 5.5a. Figure 5.5b was acquired without any electrode on the A-face.

Wafer B ought to be of better quality than wafer A, being the result of several years of iterations and improvement in the growth and wafer processing from 5N+. The mean resis-

tivity of wafer B was measured to be 5.8 Ω-m, and the maximum mobility-lifetime product ($\mu\tau$) 3.6×10^{-3} cm^2V^{-1} (J. Bolke, personal communication, October 2024). The lack of precise information regarding wafer A, including its composition, electronic characteristics, and processing, led us to strictly use wafer B once it became available.



(a) (b)

Figure 5.5 IR transmission microscopy images of wafers A (a) and B (b). Both images were acquired at the same magnification. No defects, other than Te inclusions (black points) are observed. While the density of inclusions is lower in wafer B, their size is larger. The background non-uniformity is due to fluctuations in Pt electrode thickness. Image b) was acquired without electrodes.

5.1.2 Device structures

Figure 5.6 illustrates a profile view of all the structures fabricated. The reference devices (i) are comprised of simple pixel electrodes deposited on as-cleaned CZT B-face. The passivated devices are comprised of pixel electrodes deposited on as-cleaned CZT B-face, followed by a 50 nm insulator deposition in the interpixel gaps. As discussed in section 3.1.2, the semi-conformal nature of sputtering deposition simultaneously leads to the deposition of a thin insulator on the CZT sidewalls. The MIS devices (iii) are comprised of a thin insulating layer (3-10 nm) sandwiched between the as-cleaned CZT B-face and the deposited electrodes. Finally, the MIS+passivated (iv) device merges both structures; pixel electrodes are evaporated after the deposition of a thin insulating layer on the CZT surface. A thicker insulating layer (50 nm) is then deposited in the interpixel gaps. A detailed discussion of the fabrication process flow was provided in section 3.2.

Three different photomasks were used to deposit electrodes. The resulting pixel patterns are

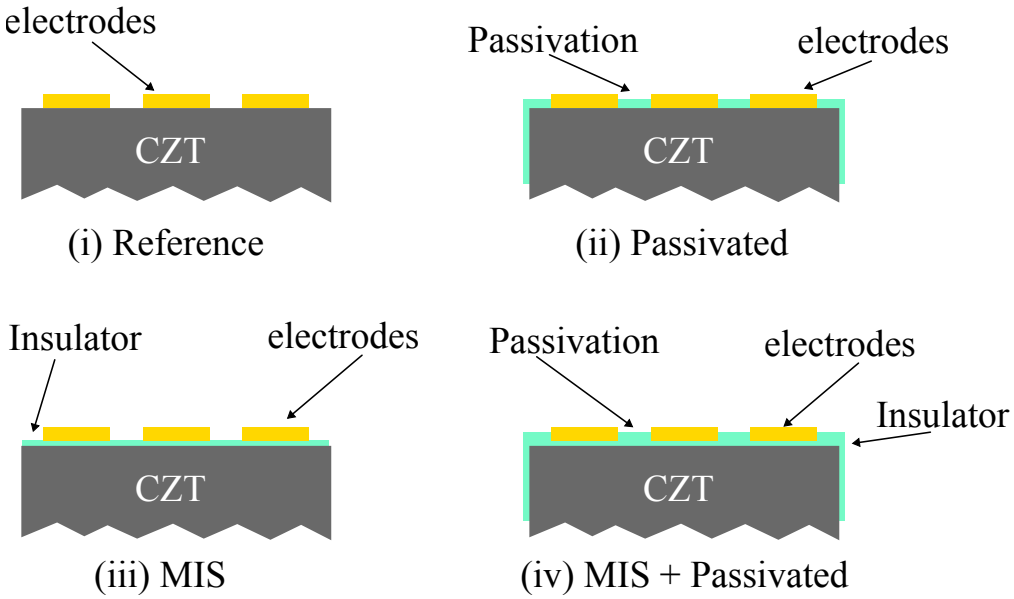


Figure 5.6 Lateral schematic of the device structures fabricated in this study. The insulator and passivation layer are comprised of SiN_x deposited by reactive RF magnetron sputtering. The Au pixel electrodes were deposited by e-beam.

shown in figure 5.7. Configuration I is comprised of 400x500 μm^2 rectangular pixels with a 50 µm interpixel gap. This pattern was only used in conjunction with wafer A. Configurations II and III are comprised of 400x400 μm^2 square pixels, separated by an interpixel gap of 50 µm and 100 µm, respectively. These patterns were developed to better align with contemporary detector geometries, and were used in conjunction with wafer B.

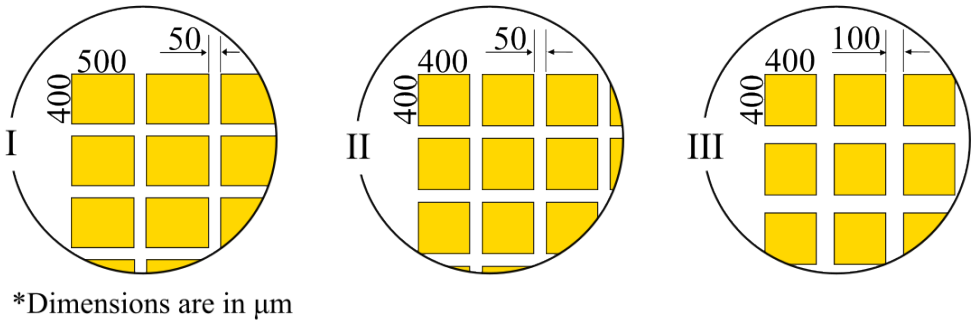


Figure 5.7 Different electrode configurations. Pattern I was used in conjunction with wafer A. Patterns II and III were used in conjunction with wafer B. The latter was specifically used to enhance passivation effects on the surface leakage current.

10 different device types were fabricated, blending wafers, device structures and electrode

patterns. Table 5.2 provides an overview of all the different devices. For each combination of wafer and electrode, a reference device was fabricated (D1, D5 and D9). A lack of precise information regarding the composition, electronic characteristics and processing of wafer A led us to strictly use wafer B once it was available. Consequently, only D1 to D4 were fabricated on wafer A, the remaining devices (D5 to D10) were fabricated on wafer B. The insulator thickness in the MIS structure was varied, from 3 nm to 10 nm. Moreover, due to the promising nature of the MIS structures, 2 distinct sets of devices were fabricated and tested. D5.1 to D8.1 were processed in July 2024, while D5.2 to D8.2 were processed in October 2024. A larger pixel pitch was used in D10 to enhance the insulator's interpixel passivation effects. Finally, the marginal electrical performances offered by the added complexity of the MIS+passivated structure, as discussed later in section 5.2.3 refrained us from repeating the structure on wafer B.

Table 5.2 List of devices fabricated to investigate passivation properties of SiN_x in passivated detectors and MIS structures.

Device	Wafer	Structure	Electrode Pattern
D1	A	Reference	I
D2	A	Passivated	I
D3	A	3 nm MIS	I
D4	A	3 nm MIS + Pass.	I
D5.1, D5.2	B	Reference	II
D6.1, D6.2	B	3 nm MIS	II
D7.1, D7.2	B	6 nm MIS	II
D8.1, D8.2	B	10 nm MIS	II
D9	B	Reference	III
D10	B	Passivated	III

5.1.3 Deposition and characterization of SiN_x

SiN_x was deposited by RF magnetron reactive sputtering from a pure Si target. No bias, nor any heat, was applied intentionally to the substrate. An RF power of 200 W was applied to the Si target, resulting in a constant DC bias of 0.74 V. A plasma was formed at an Ar/N_2 reactive gas ratio of 20/8, at a deposition pressure of 3 mTorr. The Si target was cleaned for 5 min. in an Ar plasma at 20 mTorr prior to deposition. The deposition chamber was vacuumed to a pressure of 1.2 $\times 10^{-6}$ torr before starting gas flows.

Ellipsometry was used to measure the thickness of the deposited layers and assess their quality. The deposition specifications were optimized on Si(100) wafers. A J.A. Woollam RC2-XI

variable angle ellipsometer was used for the measurement. The complex reflectance ratio is defined as $\rho = \frac{r_p}{r_s} = \tan\Psi\ e^{i\Delta}$, where r_p and r_s are the normalized amplitudes of the p and s polarized reflected light. Ψ and Δ respectively parametrize the reflectance amplitude and phase shift induced by the measured sample [117]. By fitting a dielectric function model to the complex refraction index parameters extracted from ρ, the thickness of the deposited layers, alongside key dielectric parameters, can be assessed [117]. Table 5.3 compares the optical parameters extracted by fitting a Cody-Lorentz and a Tauc-Lorentz SiN_x model to the measured depolarization ratio of a 100 nm thick layer deposited on Si(001) with 1.5 nm native oxide. Several models were tested, yet these provided the lowest mean-squared-error (MSE), and a greater level of detail. The Ψ and Δ curve fits are available in appendix A.

Whilst ellipsometry offers several advantages, such as the ability to measure several key parameters simultaneously and instantaneously, it only offers an optical assessment of the deposited layers. Nonetheless, the rapid iterations made it possible to optimize the deposition time and conditions rapidly. The fit MSE is found to be similar for both models; the increased number of fitting parameters in Cody-Lorentz explains its lower MSE, yet makes the result interpretation more cumbersome. A description of all fit parameters can be found at [1]. Notably, both models suggest a thickness of 113 nm and an $\epsilon_\infty = 2.0 - 2.1$ (real dielectric constant for $E \to \infty$). In the Tauc-Lorentz model, both ϵ_∞ and E_g were found to be below expected values for standard Si_3N_4 [118], which suggests possible deviation from stoichiometric composition ratios, but also the possibility of a defective layer deposition.

Table 5.3 Extracted optical parameters from Cody-Lorentz (CL) and Tauc-Lorentz (TL) model fits to the complex dielectric function of Si_3N_4. All data modelled on Si(100) with 1.5 nm native oxide. The definition of each parameter can be found in [1].

Parameter (CL/TL)	**Cody-Lorentz**	**Tauc-Lorentz**	**TL - Litt. [118]**
MSE	6.904	7.345	–
Roughness (nm)	1.49 ± 0.03	1.87 ± 0.03	–
Thickness (nm)	113.42 ± 0.01	113.50 ± 0.01	–
ϵ_∞	2.0 ± 0.3	2.175 ± 0.004	3.1 ± 0.2
UV Pole Amp. (eV)	10 ± 40	–	–
UV Pole En. (eV)	10 ± 10	–	–
IR Pole Amp. (eV)	0.039 ± 0.005	–	–
Amp1 / Amp. (eV)	70 ± 100	47.0 ± 0.2	59 ± 8
Br / Brod. (eV)	2.8 ± 0.5	2.042 ± 0.009	0.5 ± 0.1
E01 / E_o (eV)	7.6 ± 0.3	7.732 ± 0.005	6.8 ± 0.2
Eg1 / E_g (eV)	2.87 ± 0.02	3.223 ± 0.005	4.50 ± 0.06
Ep1 / E_p (eV)	8 ± 7	–	–

5.2 Results

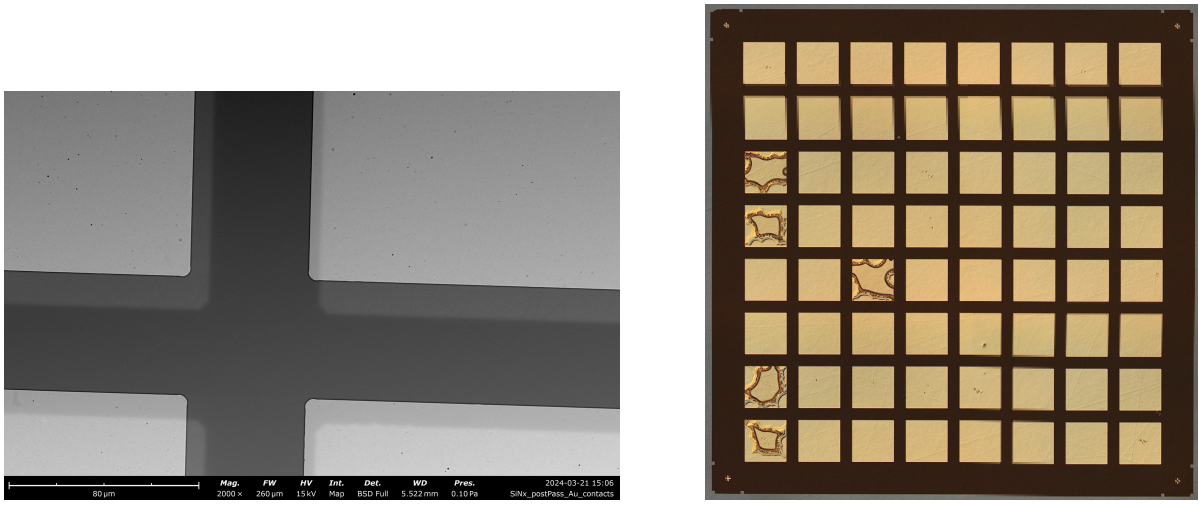
The electrical performance of all devices was investigated using a Keithley 2470 SMU (unless specified otherwise), paired with probes mounted on micro-manipulators. The dark current measurements were performed in a black box to block out all external illumination. The following sections are divided by device structures. First, section 5.2.1 presents the results of passivated devices. Then, a detailed discussion of MIS-structure devices is offered in section 5.2.2. Finally, section 5.2.3 presents an attempt to merge both structures. A comparative assessment of the architectures, along with a discussion of the results, is presented in section 5.3.

5.2.1 Metal-Semiconductor and Passivation devices

To assess the quality of the interpixel passivation layer, optical and SEM images were acquired. Figure 5.8a, acquired by SEM, shows the interpixel passivation of D2. Despite a systematic 15 µm misalignment in both directions, the film is determined to be of good quality, with a uniform coverage throughout the device. The alignment issues stem from the sub-optimal passivation lithography process. No passivation-dedicated mask was available for pixel pattern I, as such, the passivation lithography was done in image-reversal mode, and without proper alignment marks. Nonetheless, the adhesion of the film is satisfactory, providing sufficient interpixel coverage to achieve its intended purpose.

On the other hand, the use of a direct lithography process for passivation with electrode pattern III allowed for good alignment of the SiN_x in between the Au pixels, as shown in figure 5.8b for D10. The latter shows minimal dielectric overlap with the electrodes. Only 5 pixels were found to be still covered with dielectric after liftoff; yet, simply a longer liftoff may fix this issue. Again, the adhesion of the layer was adequate, with uniform coating throughout the device.

The high-voltage operation of both passivated devices was measured, as shown in figure 5.9. In both cases, the electrical characteristics of the devices were measured prior to passivation to minimize the possibility of a singular device with higher dark current than average. The IV sweeps were performed in auto-mode and with a delay for D2 and D10, respectively, leading to some of the behaviour variations. The differences between both modes are detailed in section 3.3.1. Five pixels, evenly distributed on top of the devices, were measured and averaged. Figure 5.9a compares the electrical performances of the device pre- and post-passivation, and overlays the results on D1's standard deviation (which includes the pre-passivation measure-



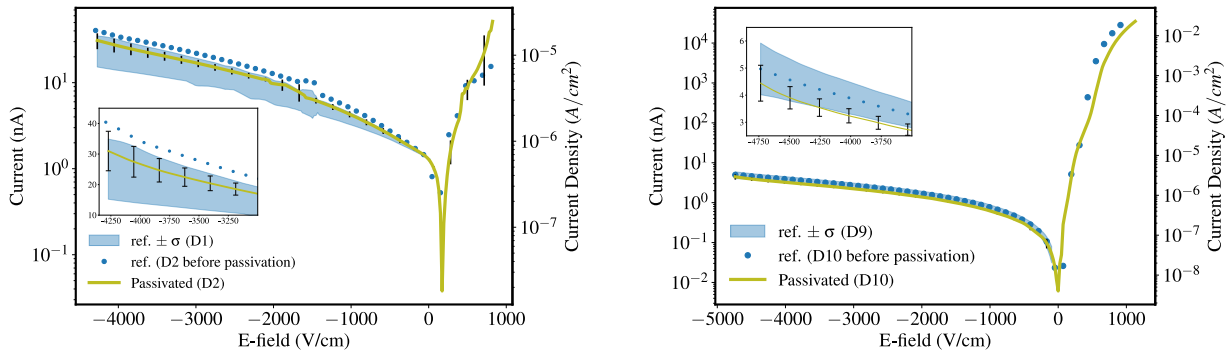
(a) (b)

Figure 5.8 Visual assessment of the passivation layer quality. a) SEM image of the interpixel gap of D2. A 15 µm misalignment is observed in both directions, yet the deposition is uniform. b) Optical microscopy image of the complete device. The passivation layer (dark) is well aligned with the pixels. Only 5 pixels were partially covered by SiN_x after liftoff.

ments from D2 amongst others). Notably, the dark current is reduced to 31 nA from 40 nA after the passivation at 1000 V reverse bias, as shown in the inset. Whilst the post-passivation performances are found to be on-par with the reference's average, its dark current is found to be lower, within uncertainties, than its specific pre-passivation current. Moreover, the dark current is found to be lower throughout the complete reverse bias regime. No noteworthy changes are observed in forward bias. The expected Schottky electrical behaviour of the interface is observed. A current minimum shift towards positive voltages is observed, attributed to the increased voltage sweep speed, which generates capacitive effects at the interfaces and current hysteresis.

Unfortunately, the 25% reduction in dark current is overshadowed by the upper-tier current level of the device prior to passivation, which is more than one standard deviation higher than the bulk of pixels tested. Consequently, the device structure was repeated on wafer B, with an electrode pattern susceptible of enhancing the passivation effects, D10. Figure 5.9b again illustrates the high-voltage electrical performance of the devices before and after passivation. They are overlaid on the reference's standard deviation. Unlike D2, the pre-passivation dark current of D10 is measured to be virtually on par with the average measured on all similar reference devices. The dark current at -1000 V is measured to be 4.5 nA, a marginal 0.5 nA

reduction from its pre-passivation value of 5 nA. No conclusive evidence suggests a noteworthy dark current reduction within uncertainties, as shown in the figure 5.9b's inset. There is substantial overlay between the reference's and passivated's performances. The electrical behaviour of the interface is observed to be characteristically Schottky.



(a) (b)

Figure 5.9 Electrical characterization of devices passivated by depositing 50 nm of SiN_x on a) wafer A, and b) wafer B. The insets present a focused view of the high-voltage operation of the devices. The improvements on wafer A are

The photocurrent of D9 and D10 was measured using a broadband white light, with constant power, as depicted in figure 5.10. The interpixel passivation does not hinder the photocarrier collection efficiency. Both averaged IV sweeps overlay one another for most of the voltage range, diverging by a few tens of nA outside of the operating range, specifically in forward bias. Both detectors present a similar "breakdown point" at -3500 V/cm.

To further understand the electrical benefits of interpixel physical passivation on the SLC, the pair-wise dark current was measured. Figure 5.11 displays the pair-wise electrical performance of both D9 and D10. Figure 5.11a shows the complete IV sweep from -200 V to 200 V fro adjacent pixels. Aside from the current fluctuations below -160 V, the dark current exhibits the expected back-to-back Schottky behaviour. The dark current is found to be lower throughout the complete voltage range. Following section 3.3.1, figure 5.11b compares the pair-wise dark current at -180 V for pixel pairs at increasing distance. At every pixel pair, the passivated dark current is measured to be 40%-55% of the reference's one. Yet, the current value decay rate is measured to be faster: accounting for 55% of the references for adjacent pixels, and declining to 40% for pixels 5 apart.

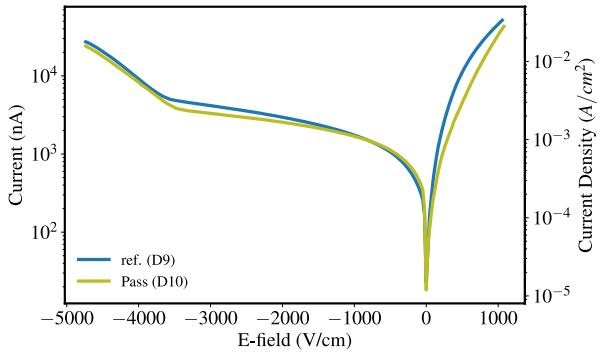


Figure 5.10 Photoresponse of device passivated with SiN_x. Passivation does not hinder carrier collection under illumination.

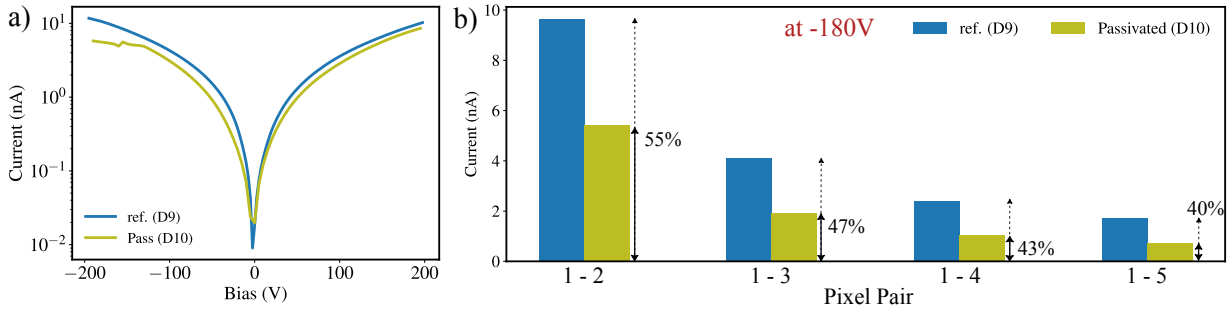


Figure 5.11 Measurement of surface electrical characteristics by pair-wise IV testing. a) Adjacent pixel IV sweep. The passivation shows, in addition to the fluctuation at negative voltages, a reduction in the dark current. b) Dark current at -180 V for pixel pairs at increasing distances. The current is found to reduce faster in the passivated device than in the reference.

5.2.2 Metal-Insulator-Semiconductor devices

The second device structure fabricated and investigated in this work is the MIS configuration. This architecture was introduced to reduce the dark current typically observed in standard metal–semiconductor contacts by incorporating a thin insulating layer between the metal electrode and the CZT substrate, which simultaneously passivates surface and interface states and acts as a barrier enhancement layer for charge carriers.

First, the electrical performance of D3 is compared to that of its reference counterpart in figure 5.12. At an applied field of -4350 V/cm, it exhibits a current of 2.5 nA. The latter represents an order of magnitude reduction compared to the 20 nA measured in the reference device. This reduction is not limited to a single bias point; the current remains consistently

lower throughout the entire voltage range. Although the overall Schottky behaviour is preserved, the absolute current levels are reduced relative to the reference.

We further note a shift in the position of the current minimum. While the reference device exhibits a current minimum at 0 V/cm, D3 displays a clear shift towards negative voltages. To assess long-term stability, electrical measurements were repeated in the weeks following fabrication. The device performance remained stable, with consistent current levels, even when remeasured after one year, showcasing the reliability of the MIS structure over time.

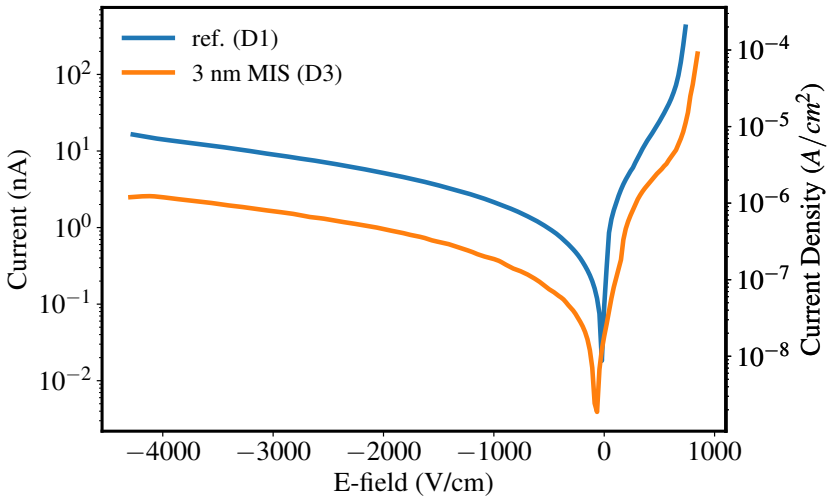


Figure 5.12 Electrical characteristics of devices comprised of both a 3nm insulating layer of SiN_x. The device was built on wafer A.

Encouraged by the promising reduction in dark current, further efforts were made to optimize the MIS fabrication process and to evaluate the influence of the insulator thickness. Devices 6, 7, and 8 were fabricated on wafer B to investigate reproducibility and performance consistency. On the surface of these devices, respectively, 3 nm, 6 nm and 10 nm thick layers of SiN_x were deposited before the deposition of metal contacts. Each device was subjected to electrical testing, and five individual pixels were measured per device to obtain a representative assessment of the overall electrical behaviour. The results, shown in Figure 5.13, present averaged IV characteristics across the tested pixels. Two distinct sets of MIS devices were fabricated under identical process conditions to assess fabrication repeatability.

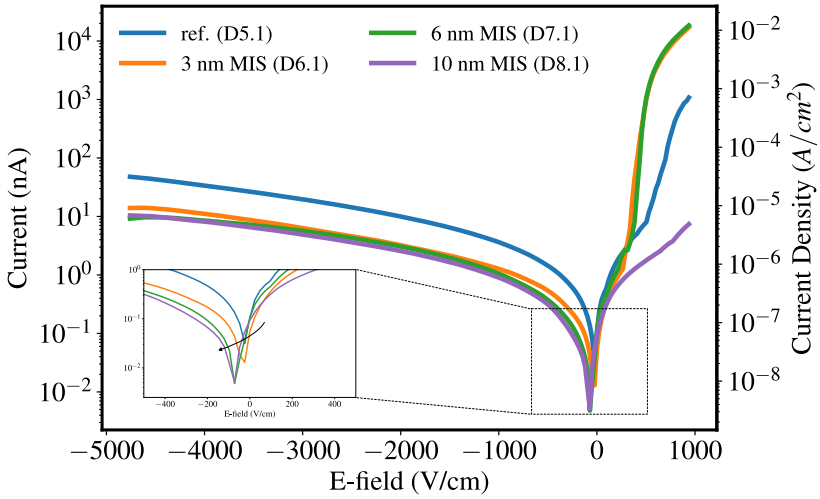
Figure 5.13a presents the electrical performances of the first set of MIS devices. At 1000 V

reverse bias, the dark currents are measured to be 47 nA for D5.1, 14 nA for D6.1, 9 nA for D7.1, and 10 nA for D8.1. A clear reduction in dark current is observed with the introduction of the insulating layer, with the most significant improvement occurring between the unpassivated (D5.1) and 6 nm (D6.1) structures. However, increasing the thickness to 10 nm (D8.1) does not yield further improvement, suggesting a threshold beyond which additional thickness no longer benefits current suppression. The typical Schottky behaviour of the interface is preserved across all devices. No significant variations are observed in forward bias. A systematic shift in the current minima toward more negative voltages is observed, increasing with the insulator thickness, and is attributed to the altered space charge distribution at the interface.

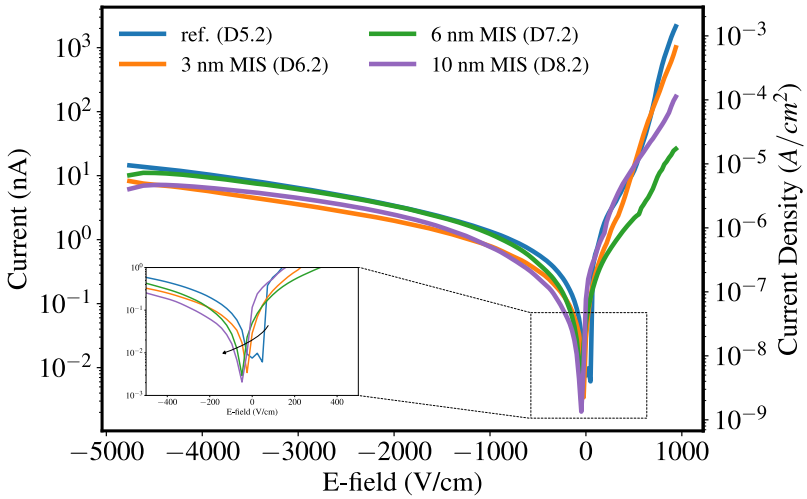
Figure 5.13b shows the electrical performance of the second set of MIS devices. At 1000 V reverse bias, the measured dark currents are 14 nA for D5.2, 8 nA for D6.2, 10 nA for D7.2, and 8 nA for D8.2. The overall trends are consistent with the first set, aside from D7.2: the insulating layer leads to reduced dark current. However, apart from high voltages where a sudden reduction of the current is observed, D7.2 closely matches the IV characteristics of the reference device. The forward bias characteristics remain inconclusive. As previously observed, a current minima shift toward negative voltages is present and scales with increasing insulator thickness.

Although the deposition of an interfacial layer leads to a reduction in dark current, local variations in dark current among the measured pixels should be assessed. Figure 5.14 compares the dark current-voltage characteristics of the reference and 10 nm MIS devices for both sets. While both Schottky, the references present drastically different saturation currents, a variation of 31 nA between the two devices, as depicted in the inset. However, the forward current of both devices is found to be exactly the same. It is ought to be believed that the devices share consistent interfacial properties, owing to the same fabrication procedure, but local variations in the crystal lead to different saturation values. On the other hand, the reverse bias current of both MIS-type devices is found to overlap for the majority, differing by only a few nA at high voltages. Both devices thus share similar barrier enhancement properties; however, fluctuations in the composition and electrical characteristics of the SiN_x layer may lead to increased forward current in one or another. Finally, the same voltage shift, emblematic of interface charge accumulation, is observed.

The current distributions at an applied electric field of -4500 V/cm (-900 V) are shown in figure 5.15 for each device. The mean values and standard deviations were extracted from



(a)



(b)

Figure 5.13 Dark current of MIS structure devices. The addition of an insulating layer systematically reduces the current values in reverse bias. Yet, the improvements are far more pronounced in the first set of devices (a), mainly due to a higher reference value.

all measured pixels and used to generate normal distributions for improved clarity and readability. With the exception of D7.1 and D7.2, which fall within one standard deviation of each other, the mean dark current values show notable fluctuations between the two sets. D6.1 and D6.2 overlap within three standard deviations, while D8.1 and D8.2 lie within two. Most notably, the reference devices exhibit both the most considerable standard deviations

and mean current values that fall well outside the standard deviation ranges of the other devices.

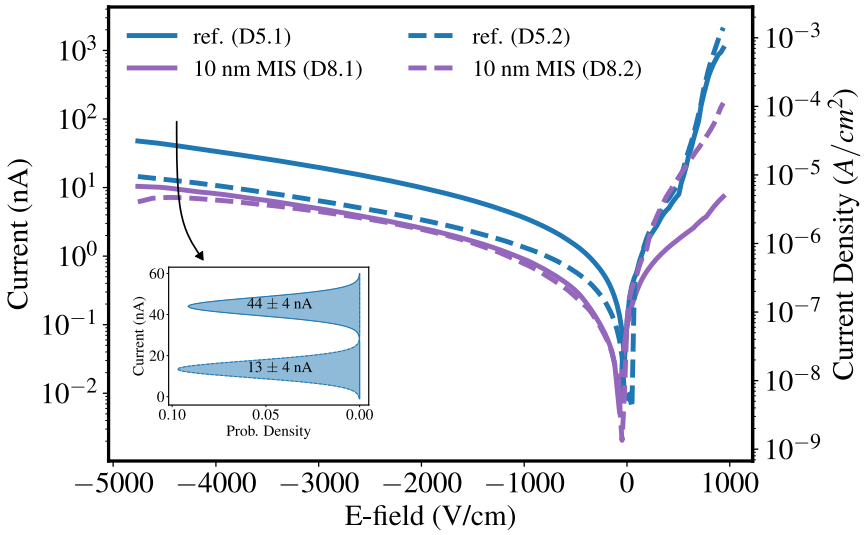


Figure 5.14 Variability of the dark current of reference devices and 10 nm MIS. The inset shows a bi-normal distribution of currents, attributed to the first and second devices fabricated.

The response under illumination of the MIS detectors was assessed, as shown in figure 5.16, comparing the dark and photocurrent for both sets. The deposition of a 10 nm interfacial insulating layer is found to systematically inhibit the forward bias current, reducing it by more than an order of magnitude for both sets. Yet, it is observed to have negligible impacts in reverse bias operation. The current discrepancies between the two sets are attributed to different illumination intensities.

The SLC was measured by measuring the current between adjacent pixels using a Keithley 4200 parameter analyzer paired with the same microprobe station. The current was swept from -200 V to 200 V, and back, without any predefined delay. Figure 5.18 shows the measured current-voltage characteristics. For the devices fabricated on wafer B (figure 5.18a), increasing the surface leakage current is found to scale with the insulator thickness. The insulating layer minimally increases the current by two orders of magnitude at 200 V. A similar effect is observed for the device fabricated with wafer A (figure 5.18b). Moreover, large current fluctuations, instability and hysterisis effects are observed from the deposition of 3 nm onward. These, paired with an increase in the SCL, suggest an increase not only

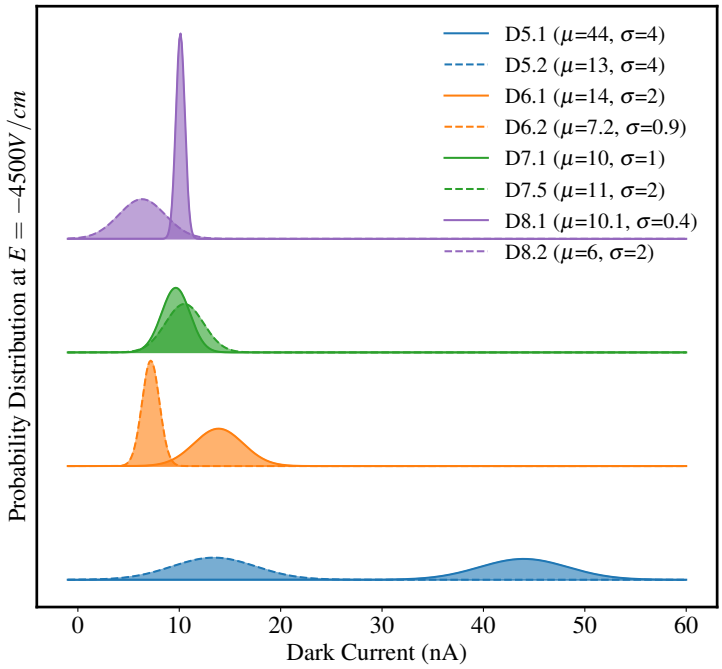


Figure 5.15 Current distribution at -4500 V/cm for all devices fabricated on wafer B. The mean and standard deviations were extracted from the acquired IV sweeps, and the normal distributions were generated to improve clarity and readability.

in surface conductivity, but also the addition of electrically unstable defects at the surface, promoting surface leakage currents.

5.2.3 Metal-Insulator-Semiconductor and Passivation devices

A single device comprised of an MIS structure, then passivated, was fabricated. To assess the quality of the passivation layer, SEM images were acquired. As shown in figure 5.19, the deposited passivation layer is of poor quality. First, the deposited width is observed to be systematically narrower than the interpixel spacing. This issue stems from the lack of a passivation mask for this specific electrode pattern. The image reversal lithography process was not fully optimized, leading to fluctuations in the developed structure's widths. Second, in several regions, significant undulation is present along the dielectric edge. Moreover, the adhesion of the passivation is unsatisfactory, with signs of flaking observed at multiple locations across the device. Some pixels are found to be completely devoid of passivation, indicating either a failure during deposition or partial delamination. In general, the passivation quality

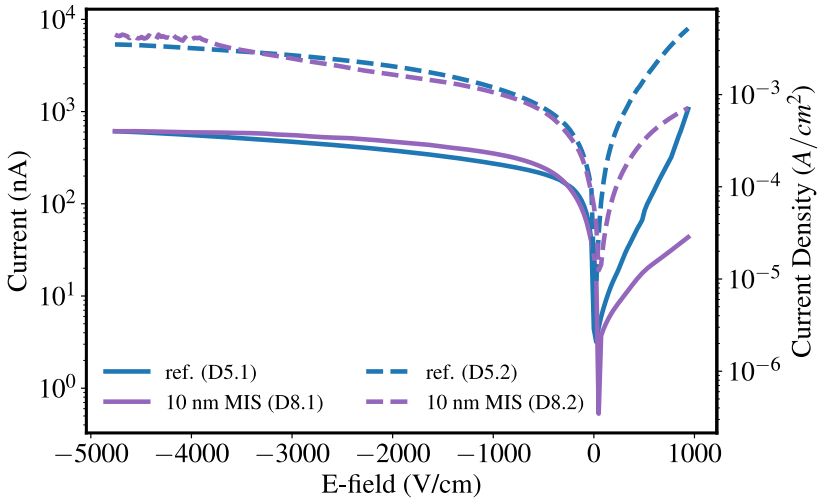
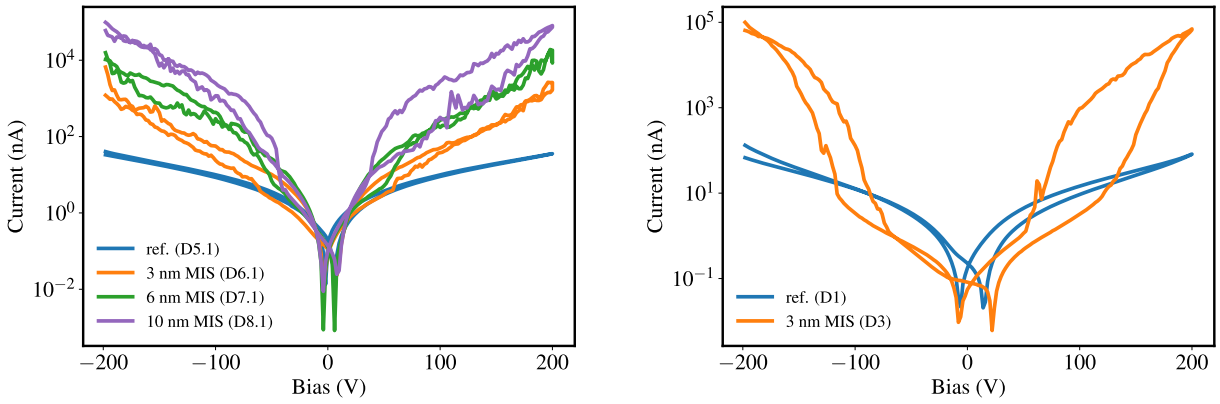


Figure 5.16

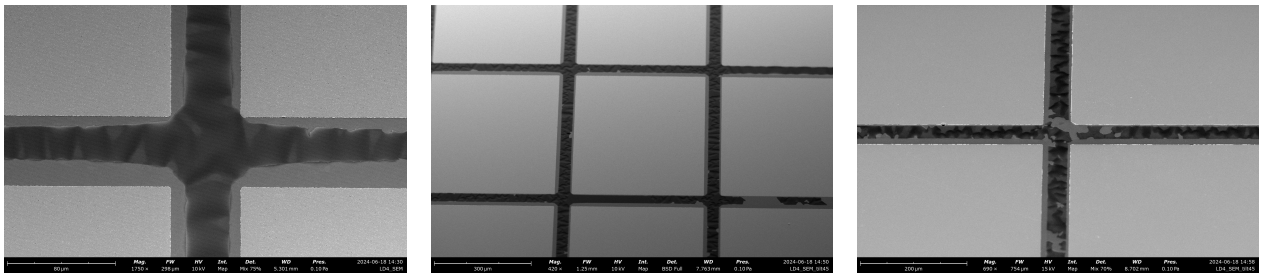
Figure 5.17 The photocurrent as measured under broadband white light. The barrier layer is found to have no impact on the photocurrent in reverse bias. While systematically lowering the forward current. The variations between rounds of devices are attributed to a different illumination intensity.



(a) (b)

Figure 5.18 Surface leakage current between adjacent pixels of MIS detectors a) increasing insulator thicknesses, and b) on wafer A. The IV sweeps were acquired in dual-sweep mode using a Keithley 4200 parameter analyzer. The deposited insulating layer is found to systematically increase the surface leakage current.

for this MIS-based structure is insufficient, and process optimization would be required to achieve reliable and uniform coverage.



(a) (b) (c)

Figure 5.19 Visual assessment of the interpixel passivation layer by SEM. Not only does the deposited layer not fully cover the interpixel spacing, but the adhesion of the film is poor, leading to peeling effects and poor passivation. Some pixels were found not to be passivated.

The electrical characteristics of the detectors were also assessed. Figure 5.20 graphs the acquired IV curves of D1 as well as D4 in dark conditions, and under illumination. The dark current is found to be lower throughout the voltage sweep range. At -1000 V, the dark current is measured to be 9 nA, an 11 nA reduction from the reference value. Although this improvement is better than observed for passivated devices, the dark current remains higher than previously established for simple MIS structures on wafer A. Also, the addition of the passivation layer to MIS structures minimizes the shift of current minima toward negative voltages observed in all MIS devices. Similarly to the other MIS-type devices, the forward bias current is inhibited by the addition of an insulating layer. The device also maintains a good photocurrent in reverse bias,

5.3 Discussion & Overview

The addition of an insulating layer significantly improved the performance of detectors fabricated on wafer A, independently of the device structure, whereas only modest improvements were observed on wafer B. This discrepancy suggests that the effectiveness of passivation varies between substrate types. We noted that wafer A should be of lower quality than wafer B in section 5.1.1, and exhibited surface roughness of an order of magnitude higher than the latter. Higher surface roughness is typically associated with a greater density of surface defects and dangling bonds, which can act as carrier traps and recombination centres. Incidentally, the detectors built on wafer A benefit from passivation, which inhibits those defects. In contrast, wafer B's smooth surface presents fewer opportunities for passivation, resulting in fewer notable improvements. There may also be intrinsic material differences, such as a

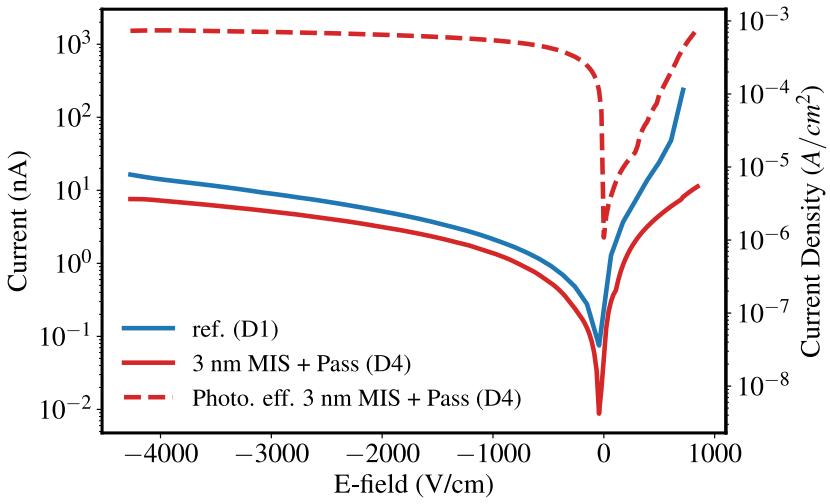


Figure 5.20 Electrical characteristics of devices comprised of both a 3nm insulating layer and a 50 nm passivation layer of SiN_x. The device was built on wafer A. A decrease in dark current is measured from the reference. The photocurrent remains high.

higher density of Te inclusions compared to wafer B, alongside processing acuity, which may explain the greater differences.

Pair-wise testing of detectors with and without the insulator layer supports the idea that surface passivation effectively neutralizes surface dangling bonds, thereby restoring surface resistivity and reducing surface leakage currents, in line with theoretical expectations [4]. However, the neutralization of surface states appears to only have a marginal effect on the overall dark current of the devices. This suggests that, while surface leakage sources are mitigated, intrinsic bulk carrier concentration and contact-related carrier injection mechanisms may still dominate the total dark current of the detectors [82]. Nonetheless, passivation is likely to play a significant role in ensuring uniform electric field distribution within and promoting device stability, specifically by encapsulating and isolating the surface from ambient conditions. The latter is relevant for the implementation of the devices into radiation detection systems, where long-term stability and reliable performance are essential [30].

The deposition of a thin barrier enhancement interfacial layer showed promising improvements to the performance of the devices, narrowing the current distribution gap between each pixel on a detector, ensuring consistent performance, while also providing some current reduction in the reverse bias operation range. Moreover, a consistent voltage shift

was observed with increasing insulator thickness in these MIS-structure devices. This behaviour is attributed to capacitive effects arising from charge accumulation at the insulator/semiconductor interface. Specifically, the enhanced barrier potential from the insulator may prevent lower-energy thermal carriers from traversing the interface, resulting in an accumulation of charge carriers at the boundary and, consequently, in a voltage offset of the current minima. Interestingly, this shift was not observed under illumination, suggesting photo-generated carriers possess enough energy to overcome the interfacial barrier. Unfortunately, this capacitive effect may induce implementation drawbacks. Specifically, the accumulation of charges at the interface leads to detector polarization under a constant electric field, which may collapse the electric field within the detectors, degrade the operation frequency, compromise the energy resolution, and lead to unstable performance [51].

5.3.1 Limitations and Shortcomings

Despite the promising trends observed, several limitations restrict further improvement of the device's performance. First, the quality of the silicon nitride (SiN_x) insulator layer is suspected to be sub-optimal, as discussed in section 5.1.3, especially in the MIS structures where the layer is particularly thin. Substandard dielectric quality can lead to the formation of localized leakage paths or premature dielectric breakdown under high-voltage operation, compromising long-term reliability and leading to increased leakage currents [119]. The lack of a robust and defect-free insulator may also introduce uncertainty in the conduction mechanism across the MIS interface, making it difficult to predict the device behaviour under bias stress.

Second, the unpolished sidewalls of the detectors appear to be a significant source of surface leakage current. Previous experiments, involving varied electrode configurations, have shown that configurations with electrodes closer to the sidewalls exhibit higher dark current levels. These observations suggest that the sidewalls, which feature high defect densities and rough morphologies after sawing, contribute substantially to parasitic charge carriers [120]. Design elements such as guard rings or pseudo-Frisch grids may be required to isolate the active detector region from these leaky paths [63, 121].

Third, the interplay between insulator thickness and charge transport raises questions about the long-term behaviour of these devices. While a thicker insulator was shown to improve passivation and increase the effective barrier height for carriers to conduct, it may also increase the device's capacitive response, leading to polarization or delayed signal collection.

Thus, an optimization is required to balance out passivation quality, barrier height, and charge transport efficiency. Finally, the limited quality of the insulator introduces uncertainty in the nature of conduction across the interfaces, particularly under high-voltage conditions. Notably, the increased leakage current witnessed in some configurations hints at a possible breakdown of the insulating layer. Finally, the intrinsic variability of the performances across devices points to multiple uncontrolled variables, such as processing-induced inhomogeneities and local defects, which need to be better understood and controlled in future iterations of the devices.

CHAPTER 6 CONCLUSION AND RECOMMENDATION

CZT has attracted the interest of many as a direct-conversion radiation detector. Its intrinsic combination of high atomic mass and high density conveys a high attenuation power, particularly suitable for X-ray diagnostic imaging. Its integration into MSM direct-conversion detectors exhibits a high generation of electron-hole pairs, promoting its use as PCD to be implemented in PCCT. However, defects inherent to the growth process have hindered the development of commercial detectors. Further, the optimal device processing framework has yet to be addressed to determine the synergetic effects of processing steps on the electrical performance of radiation detectors. Following the development of a radiation detector fabrication process flow, the objectives of this Master's thesis were to elucidate the underlying connections between processing fabrications and the dark current of detectors. This was achieved by analyzing the impacts of thermal treatments, often inherent to fabrication processes such as thin layer depositions or etching, on the surface and interfaces of fabricated detectors and their electrical performance thereof. In light of these results, we determined that processes requiring little to no thermal input prevented performance deterioration, and thus device structures were developed to address a source of dark current in the detector: surface and interface.

6.1 Thermal stability of CZT X-ray detectors

The reported low thermal budget of CZT detectors was investigated by elucidating the impacts of thermal treatments inherent to several fabrication processes on their electrical performance. Detectors comprised of Au electrodes deposited onto CZT (B-face) by e-beam were subjected to sequential annealing processes of increasing temperature, from 373 K to 623 K, in vacuum. The dark current of the device after each annealing step was measured. The present study reveals a clear deterioration of the e-beam Au-CZT interface after annealing at 523 K and above, accompanied by an increase in the radiation detector's background current. The systematic current-voltage measurements reveal consistent performance up to annealing temperatures of 473 K, after which onset dark current increments are observed for annealing temperatures of 523 K and above. At these temperatures and above, the reverse bias dark current is found to increase and exhibit significant fluctuations. Moreover, the forward bias behaviour was found to shift at the same temperatures, deviating from the purely ITD model, showing linear plateaus in the mid-voltage ranges; an indication of recombination-limited currents. Further analysis showed a clear positive trend between an-

nealing temperature and interfacial voltage drop. The changes are predominantly driven by morphological and compositional changes at the e-beam-Au interface, where TEM revealed a Zn-depleted zone at the interface, owing to a Zn migration to the Au pixel surface. This compositional change potentially drives a reduction in effective barrier height at the interface, which, alongside defect proliferation, enhances parasitic carrier injection and generation, as well as increases the interfacial voltage drop. However, the intrinsic interplay between interface thickness, composition and state density prevents us from establishing a clear link between each parameter and its impact.

Despite these observations, several uncertainties remain. It is not possible to determine the exact temperatures that trigger the compositional and morphological surface evolution, or whether these changes result from thermal accumulation across multiple processing steps, which limits the ability to accurately cross-correlate the observations. It is also impossible to quantify the energy flux directed towards the detector during the annealing cycles, and whether nitrogen venting at higher temperatures effectively modifies the results.

6.2 Impacts of passivation layers on dark current

To avoid high processing temperatures, we developed 3 different device structures prone to improving the dark current of MSM CZT radiation detector using SiN_x deposited by reactive RF magnetron sputtering, requiring no extrinsic substrate heating for deposition. Specifically, the electrical current reduction resulting from the dielectric deposition as a passivation layer between electrodes, as well as a barrier enhancement layer, was measured. Both engineered strategies exhibit effective dark current reduction, notably in detectors fabricated on CZT with higher surface roughness and presumed lower material quality. These improvements are consistent with the passivation of surface defects and dangling bonds, leading to a suppression of surface leakage currents and a more uniform electric field distribution. However, the overall contribution of surface leakage to the total dark current appears to be limited, with intrinsic bulk conduction and contact-related injection remaining dominant, as indicated by the marginal improvement from inter-pixel passivation. The inclusion of a thin interfacial barrier enhancement layer further contributed to device improvements, reducing current spread variation pixels and slightly lowering the dark current under reverse bias. Additionally, increasing the thickness of the insulator in MIS-structured devices resulted in only marginal performance improvements, suggesting that the benefit comes mainly from passivating surface states rather than blocking carrier injection. However, thicker layers also caused a systematic voltage shift, attributed to capacitive effects due to charge accumula-

tion at the insulator/semiconductor interface. This points to a higher barrier for thermally generated carriers, but also raises concerns about detector polarization under prolonged bias, which could compromise electric field stability, electron-hole pair collection, and long-term performance.

Regardless of the performance improvement, these results are affected by the quality of the dielectric layer, as depicted by the correlated increase in SLC with layer thickness and the ellipsometry measurements. This raises many questions regarding the conduction mechanisms and breakdown behaviour within the dielectric, particularly due to the possible incorporation of contaminants within the dielectric; for example, the formation of leakage pathways caused by metallic or dopant impurities, or the ionization of defects with energy levels within the bandgap, both of which increase conductivity. Whilst the current reduction is promising for improving the SNR of devices, the dielectric quality should be improved to ensure proper SLC annihilation and consistent performance across devices.

6.3 Future research

Whilst maintaining deposition temperatures below the critical point aforementioned through the deposition of SiN_x by reactive RF magnetron sputtering preserved the integrity of the detectors, the dielectric quality was found to be sub-par. This raises the question of optimal engineering trade-offs; whereas deposition at elevated temperature may hinder the detector stability, the dark current reduction gains may significantly offset these deterioration. For example, alumina deposited by atomic layer deposition (ALD) exhibits promising performance in terms of systematically reducing dark current and SLC, despite the requirement of high-quality films to be deposited at 523 K. Indeed, the high dielectric quality achieved by this highly conformal method offers an optimal trade-off between deposition temperature and passivation performance. As shown in figure 6.1, measured on a device fabricated by my colleague Dr. Sudarshan Singh [15], passivation using Al_2O_3 thin layers presents a factor of 5 improvement in dark current at -1000 V for devices fabricated on high quality wafer B, whereas the improvement on wafer B inherent to SiN_x were marginal. Further research in the conduction mechanisms and the specific mechanism by which the dark current is improved is required. Nonetheless, the high-quality deposition should be sought to ensure consistent design and device performance.

Furthermore, it would be beneficial to understand the correlation between the electrical performances, surface and interfacial changes at each temperature. This would permit accurate

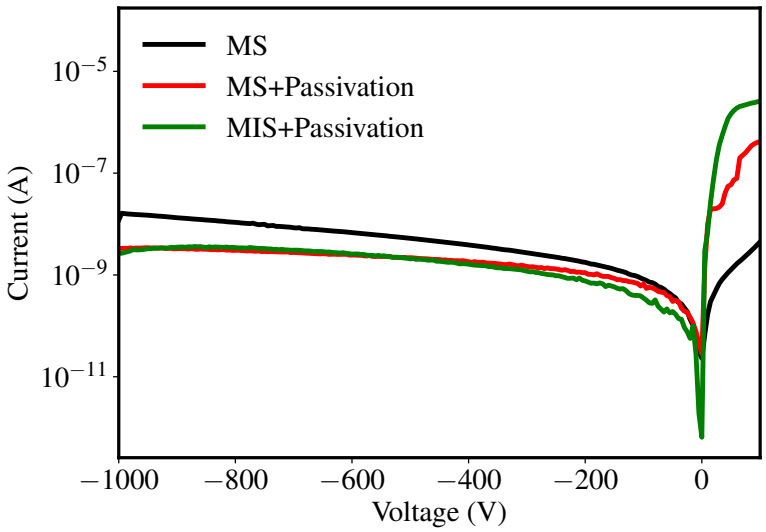


Figure 6.1 Dark current inherent to devices fabricated using ALD deposited alumina at 523 K on wafer B. Despite the increased deposition temperature, the passivation of both structures suggests a factor 5 reduction in dark current at -1000 V. Figure recreated from [15].

discrimination against performance-degradation temperature in the choice of the fabrication processes. Whilst this research focused on thermal stability, it was not in its capacity to dissociate the effects caused by thermal accumulation. Consequently, preparing different samples, each to be annealed and tested at a specific temperature, is critical to fully understanding the effects of high-temperature processes and decoupling them from the effects of, for example, passivation. Finally, several aspects of the CZT detector processing remain to be investigated. For once, the defect-prone top layer, as evidenced by the TEM images, undoubtedly degrades the performance of the detectors, both due to electron-hole pair recombination, but also due to parasitic carrier generation. Developing means of thinning down this layer, without inducing other defects, is paramount to achieve high-quality contacts enabling photon counting in CZT radiation detectors and their use in PCCT.

REFERENCES

[1] J. W. Co., "CompleteEASE Data Analysis Manual," Oct. 2011.

[2] D. A. Neamen, *Semiconductor physics and devices : basic principles*, 3rd ed. Boston: McGraw-Hill, 2003, section: xxiv, 746 pages : illustrations (certaines en couleur) ; 24 cm.

[3] C. Wu, "Interfacial layer-thermionic-diffusion theory for the Schottky barrier diode," *Journal of Applied Physics*, vol. 53, no. 8, pp. 5947–5950, Aug. 1982.

[4] W. Mönch, *Semiconductor Surfaces and Interfaces*, ser. Springer Series in Surface Sciences. Berlin, Heidelberg: Springer Berlin Heidelberg, 2001, vol. 26. [Online]. Available: http://link.springer.com/10.1007/978-3-662-04459-9

[5] E. H. Rhoderick and R. H. Williams, *Metal-semiconductor Contacts*, 2nd ed., ser. Monographs in Electrical and Electronic Engineering. New York: Clarendon Press, 1988, no. 19, google-Books-ID: 0zcoAQAAMAAJ.

[6] S. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 1st ed. Wiley, Oct. 2006.

[7] NIST, "CdTe attenuation dataset." [Online]. Available: https://physics.nist.gov/cgi-bin/Xcom/xcom3_2

[8] M. J. Madou, *Fundamentals of Microfabrication and Nanotechnology. Volume II: Manufacturing Techniques for Microfabrication and Nanotechnology*, 3rd ed. Boca Raton: CRC Press, Jun. 2011, vol. 2.

[9] S. R. Desai, H. Wu, C. M. Rohlfing, and L.-S. Wang, "A study of the structure and bonding of small aluminum oxide clusters by photoelectron spectroscopy: Al_xO_y (x=1–2, y=1–5)," *The Journal of Chemical Physics*, vol. 106, no. 4, p. 1309–1317, Jan. 1997.

[10] C. Fares, F. Ren, D. Hays, B. Gila, and S. Pearton, "Effect of deposition method on valence band offsets of SiO_2 and Al_2O_3 on $(Al_{0.14}Ga_{0.86})_2O_3$," *ECS Journal of Solid State Science and Technology*, vol. 8, p. Q3001–Q3006, Dec. 2018.

[11] J. Robertson and M. J. Rutter, "Band diagram of diamond and diamond-like carbon surfaces," *Diamond and Related Materials*, vol. 7, no. 2, p. 620–625, Feb. 1998.

[12] L. F. Voss, A. M. Conway, A. J. Nelson, P. R. Beck, R. T. Graff, R. J. Nikolic, S. A. Payne, A. Burger, and H. Chen, "Current reduction of CdZnTe via band gap engineering," *IEEE Transactions on Nuclear Science*, vol. 60, no. 2, p. 1208–1212, Apr. 2013.

[13] R. M. Krishna, "Crystal growth, characterization and fabrication of CdZnTe-based nuclear detectors," PhD, University of South Carolina, University of South Carolina, 2013. [Online]. Available: https://scholarcommons.sc.edu/etd/2410

[14] I. S. K. Kerkines and A. Mavridis, "On the electron affinity of SiN and spectroscopic constants of SiN," *The Journal of Chemical Physics*, vol. 123, no. 12, p. 124301, Sep. 2005.

[15] S. Singh, L. Montpetit, Rahier, M. R. M. Atalla, and O. Moutanabbir, "Synergetic Effect of High-Temperature Aluminium Oxide Passivation on CZT Detectors [Manuscript in preparation]," 2025.

[16] D. Bos, N. Guberina, S. Zensen, M. Opitz, M. Forsting, and A. Wetter, "Radiation Exposure in Computed Tomography," *Deutsches Ärzteblatt International*, vol. 120, no. 9, pp. 135–141, Mar. 2023.

[17] C. H. McCollough and P. S. Rajiah, "Milestones in CT: Past, Present, and Future," *Radiology*, vol. 309, no. 1, p. e230803, Oct. 2023.

[18] J. L. Prince and J. M. Links, *Medical imaging signals and systems*, second edition ed. Boston: Pearson, 2015, section: xvii, 519 pages : illustrations ; 27 cm.

[19] M. Danielsson, M. Persson, and M. Sjölin, "Photon-counting x-ray detectors for CT," *Physics in Medicine & Biology*, vol. 66, no. 3, p. 03TR01, Feb. 2021.

[20] M. S. Pearce, J. A. Salotti, M. P. Little, K. McHugh, C. Lee, K. P. Kim, N. L. Howe, C. M. Ronckers, P. Rajaraman, A. W. Craft, L. Parker, and A. Berrington de González, "Radiation exposure from CT scans in childhood and subsequent risk of leukaemia and brain tumours: a retrospective cohort study," *The Lancet*, vol. 380, no. 9840, pp. 499–505, Aug. 2012.

[21] A. Datta, Z. Zhong, and S. Motakef, "A new generation of direct x-ray detectors for medical and synchrotron imaging applications," *Scientific Reports*, vol. 10, no. 11, p. 20097, Nov. 2020.

[22] T. E. Schlesinger, J. E. Toney, H. Yoon, E. Y. Lee, B. A. Brunett, L. Franks, and R. B. James, "Cadmium zinc telluride and its use as a nuclear radiation detector material," *Materials Science and Engineering: R: Reports*, vol. 32, no. 4-5, pp. 103–189, Apr. 2001.

[23] S. Kasap, J. B. Frey, G. Belev, O. Tousignant, H. Mani, J. Greenspan, L. Laperriere, O. Bubon, A. Reznik, G. DeCrescenzo, K. S. Karim, and J. A. Rowlands, "Amorphous and Polycrystalline Photoconductors for Direct Conversion Flat Panel X-Ray Image Sensors," *Sensors*, vol. 11, no. 5, pp. 5112–5157, May 2011, number: 5 Publisher: Molecular Diversity Preservation International.

[24] S. D. Sordo, L. Abbene, E. Caroli, A. M. Mancini, A. Zappettini, and P. Ubertini, "Progress in the development of CdTe and CdZnTe semiconductor radiation detectors for astrophysical and medical applications," *Sensors*, vol. 9, no. 05, p. 3491–3526, 2009.

[25] C. Szeles and J. J. Derby, *CdZnTe and CdTe Crystals for Medical Applications*, 2nd ed., ser. Devices, Circuits and Systems. Boca Raton: CRC Press, 2022.

[26] R. C. Alig and S. Bloom, "Electron-Hole-Pair Creation Energies in Semiconductors," *Physical Review Letters*, vol. 35, no. 22, pp. 1522–1525, Dec. 1975, publisher: American Physical Society.

[27] S. K. Chaudhuri, R. Nag, U. N. Roy, R. B. James, and K. C. Mandal, "Determination of electron-hole pair creation energy in Cd0.9Zn0.1Te0.98Se0.02 quaternary semiconductor for room-temperature gamma-ray detection," *Electronics Letters*, vol. 60, no. 17, p. e70007, 2024.

[28] J. Greffier, A. Viry, A. Robert, M. Khorsi, and S. Si-Mohamed, "Photon-counting CT systems: A technical review of current clinical possibilities," *Diagnostic and Interventional Imaging*, vol. 106, no. 2, pp. 53–59, Feb. 2025.

[29] K. Hameed, R. Zainon, and M. Tamal, "Assessing tissue differentiation capabilities in X-ray imaging through cadmium zinc telluride (CZT) photon counting detectors." *Radiation Physics and Chemistry*, vol. 222, p. 111867, Sep. 2024.

[30] E. Shefer, A. Altman, R. Behling, R. Goshen, L. Gregorian, Y. Roterman, I. Uman, N. Wainer, Y. Yagil, and O. Zarchin, "State of the Art of CT Detectors and Sources: A Literature Review," *Current Radiology Reports*, vol. 1, no. 1, pp. 76–91, Mar. 2013.

[31] M. Hoheisel, "Review of medical imaging with emphasis on x-ray detectors," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 563, no. 1, p. 215–224, Jul. 2006.

[32] F. Principato, A. Turturici, M. Gallo, and L. Abbene, "Polarization phenomena in Al/p-CdTe/Pt X-ray detectors," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 730, pp. 141–145, Dec. 2013.

[33] A. Bolotnikov, G. Camarda, G. Wright, and R. James, "Factors limiting the performance of CdZnTe detectors," *IEEE Transactions on Nuclear Science*, vol. 52, no. 3, p. 589–598, Jun. 2005.

[34] A. E. Bolotnikov, S. O. Babalola, G. S. Camarda, H. Chen, S. Awadalla, Y. Cui, S. U. Egarievwe, P. M. Fochuk, R. Hawrami, A. Hossain, J. R. James, I. J. Nakonechnyj, J. MacKenzie, G. Yang, C. Xu, and R. B. James, "Extended defects in CdZnTe radiation detectors," in *IEEE Transactions on Nuclear Science*, vol. 56, Aug. 2009, pp. 1775–1783, iSSN: 00189499 Issue: 4.

[35] G. Dörfel, "The early history of thermal noise: The long way to paradigm change," *Annalen der Physik*, vol. 524, no. 8, pp. 117–121, 2012.

[36] J. B. Johnson, "Thermal Agitation of Electricity in Conductors," *Physical Review*, vol. 32, no. 1, pp. 97–109, Jul. 1928, publisher: American Physical Society.

[37] W. Schottky, "On spontaneous current fluctuations in various electrical conductors," *Journal of Micro/Nanolithography, MEMS, and MOEMS*, vol. 17, no. 4, p. 041001, Oct. 2018, publisher: SPIE.

[38] G. M. Khattak and C. G. Scott, "Deep traps in CdTe induced by ion implantation and annealing," *Journal of Physics and Chemistry of Solids*, vol. 61, no. 11, pp. 1839–1846, Nov. 2000.

[39] Y. Li, G. Zha, Y. Guo, S. Xi, L. Xu, H. Yu, and W. Jie, "Effects of deep-level traps on the transport properties of high-flux X-ray CdZnTe detectors," *Materials Science in Semiconductor Processing*, vol. 133, p. 105974, Oct. 2021.

[40] A. Hossain, A. E. Bolotnikov, G. S. Camarda, Y. Cui, D. Jones, J. Hall, K. H. Kim, J. Mwathi, X. Tong, G. Yang, and R. B. James, "Novel approach to surface processing for improving the efficiency of CdZnTe detectors," *Journal of Electronic Materials*, vol. 43, no. 8, pp. 2771–2777, 2014, publisher: Springer New York LLC.

[41] Y. Li, R. Kang, H. Gao, and D. Wu, "Damage mechanisms during lapping and mechanical polishing CdZnTe wafers," *Rare Metals*, vol. 29, no. 3, pp. 276–279, Jun. 2010.

[42] A. Bensouici, V. Carcelen, J. L. Plaza, E. Dieguez, and M. Elaatmani, "Study of effects of polishing and etching processes on $Cd_{1-x}Zn_xTe$ surface quality," *Journal of Crystal Growth*, vol. 312, no. 14, pp. 2098–2102, Jul. 2010.

[43] L. Kosyachenko, "Charge transport generation-recombination mechanism in Au/n-CdZnTe diodes," *Solar Energy Materials and Solar Cells*, vol. 82, no. 1–2, p. 65–73, May 2004.

[44] C. Wu, "Interfacial layer theory of the Schottky barrier diodes," *Journal of Applied Physics*, vol. 51, no. 7, pp. 3786–3789, Jul. 1980.

[45] A. M. Cowley and S. M. Sze, "Surface States and Barrier Height of Metal-Semiconductor Systems," *Journal of Applied Physics*, vol. 36, no. 10, pp. 3212–3220, Oct. 1965.

[46] A. E. Bolotnikov, S. E. Boggs, C. Hubert Chen, W. R. Cook, F. A. Harrison, and S. M. Schindler, "Properties of Pt Schottky type contacts on high-resistivity CdZnTe detectors," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 482, no. 1-2, pp. 395–407, Apr. 2002.

[47] F. Principato, M. Bettelli, A. Zappettini, and L. Abbene, "A Novel Extraction Procedure of Contact Characteristic Parameters from Current–Voltage Curves in CdZnTe and CdTe Detectors," *Sensors*, vol. 23, no. 13, Jul. 2023, publisher: Multidisciplinary Digital Publishing Institute (MDPI).

[48] S. Wang, X. Cao, C. Xie, J. Zhang, X. Liang, L. Wang, Z. Xu, X. Song, and P. Qiu, "Effect of low-temperature rapid annealing on structural and electrical properties of electroless platinum contacts on CdZnTe detectors," *Materials Science in Semiconductor Processing*, vol. 150, Nov. 2022, publisher: Elsevier Ltd.

[49] W. Shockley, "Problems related to *p-n* junctions in silicon," *Solid-State Electronics*, vol. 2, no. 1, pp. 35–67, Jan. 1961.

[50] K. Hecht, "Zum Mechanismus des lichtelektrischen Primärstromes in isolierenden Kristallen," *Zeitschrift für Physik*, vol. 77, no. 3, pp. 235–245, Mar. 1932.

[51] D. S. Bale and C. Szeles, "Nature of polarization in wide-bandgap semiconductor detectors under high-flux irradiation: Application to semi-insulating $Cd_{1-x}Zn_xTe$," *Physical Review B*, vol. 77, no. 3, p. 035205, Jan. 2008, publisher: American Physical Society.

[52] V. Gnatyuk, O. Maslyanchuk, M. Solovan, V. Brus, and T. Aoki, "CdTe X/γ-ray Detectors with Different Contact Materials," *Sensors*, vol. 21, no. 10, p. 3518, May 2021.

[53] F. Principato, G. Gerardi, A. A. Turturici, and L. Abbene, "Time-dependent current-voltage characteristics of Al/p-CdTe/Pt x-ray detectors," *Journal of Applied Physics*, vol. 112, no. 9, p. 094506, Nov. 2012.

[54] M. Bettelli, N. S. Amadè, S. Zanettini, L. Nasi, M. Villani, L. Abbene, F. Principato, A. Santi, M. Pavesi, and A. Zappettini, "Improved electroless platinum contacts on CdZnTe X- and γ-rays detectors," *Scientific Reports*, vol. 10, no. 1, Dec. 2020, publisher: Nature Research.

[55] V. M. Sklyarchuk, V. A. Gnatyuk, and W. Pecharapa, "Low leakage current Ni/CdZnTe/In diodes for X/γ-ray detectors," *Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 879, pp. 101–105, Jan. 2018, publisher: Elsevier B.V.

[56] P. N. Luke, M. Amman, J. S. Lee, B. A. Ludewigt, and H. Yaver, "A CdZnTe coplanar-grid detector array for environmental remediation," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 458, no. 1, pp. 319–324, Feb. 2001.

[57] P. N. Luke, "Unipolar Charge Sensing with Coplanar Electrodes- Application to Semiconductor Detectors."

[58] Z. Li, J. Cheng, F. Liu, Q. Wang, W. W. Wen, G. Huang, and Z. Wu, "Research on the Technological Progress of CZT Array Detectors," Feb. 2024, iSSN: 14248220 Issue: 3 Publication Title: Sensors Volume: 24.

[59] S. Tsigaridas, S. Zanettini, M. Bettelli, N. S. Amadè, D. Calestani, C. Ponchut, and A. Zappettini, "Fabrication of Small-Pixel CdZnTe Sensors and Characterization with X-rays," *Sensors*, vol. 21, no. 2932, Apr. 2021.

[60] L. Abbene, N. Zambelli, G. Gerardi, G. Raso, G. Benassi, M. Bettelli, F. Principato, and A. Zappettini, "High bias voltage CZT detectors for high-flux measurements,"

in *2016 IEEE Nuclear Science Symposium, Medical Imaging Conference and Room-Temperature Semiconductor Detector Workshop (NSS/MIC/RTSD)*, Oct. 2016, pp. 1–6.

[61] H. H. Barrett, "Charge Transport in Arrays of Semiconductor Gamma-Ray Detectors," *Physical Review Letters*, vol. 75, no. 1, pp. 156–159, 1995.

[62] P. N. Luke, "Electrode configuration and energy resolution in gamma-ray detectors," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 380, no. 1, pp. 232–237, Oct. 1996.

[63] U. N. Roy, G. S. Camarda, Y. Cui, and R. B. James, "Performance Study of Virtual Frisch Grid CdZnTeSe Detectors," *Instruments*, vol. 6, no. 4, p. 69, Dec. 2022, number: 4 Publisher: Multidisciplinary Digital Publishing Institute.

[64] D. McGregor, Z. He, H. Seifert, R. Rojeski, and D. Wehe, "CdZnTe semiconductor parallel strip Frisch grid radiation detectors," *IEEE Transactions on Nuclear Science*, vol. 45, no. 3, pp. 443–449, Jun. 1998.

[65] D. McGregor and R. Rojeski, "Performance of CdZnTe geometrically weighted semiconductor Frisch grid radiation detectors," *IEEE Transactions on Nuclear Science*, vol. 46, no. 3, pp. 250–259, Jun. 1999.

[66] M. A. Signore, A. Sytchkova, D. Dimaio, A. Cappello, and A. Rizzo, "Deposition of silicon nitride thin films by RF magnetron sputtering: a material and growth process study," *Optical Materials*, vol. 34, no. 4, pp. 632–638, Feb. 2012.

[67] C.-Y. Chou, C.-H. Lin, W.-H. Chen, B.-J. Li, and C.-Y. Liu, "High-dielectric-constant silicon nitride thin films fabricated by radio frequency sputtering in Ar and Ar/N2 gas mixture," *Thin Solid Films*, vol. 709, p. 138198, Sep. 2020.

[68] S. J. Bell, M. A. Baker, D. D. Duarte, A. Schneider, P. Seller, P. J. Sellin, M. C. Veale, and M. D. Wilson, "Comparison of the surfaces and interfaces formed for sputter and electroless deposited gold contacts on CdZnTe," *Applied Surface Science*, vol. 427, pp. 1257–1270, Jan. 2018.

[69] B. Ghosh, "Work function engineering and its applications in ohmic contact fabrication to II–VI semiconductors," *Applied Surface Science*, vol. 254, no. 15, pp. 4908–4911, May 2008.

[70] S. J. Bell, M. A. Baker, D. D. Duarte, A. Schneider, P. Seller, P. J. Sellin, M. C. Veale, and M. D. Wilson, "Characterization of the metal–semiconductor interface of gold contacts on CdZnTe formed by electroless deposition," *Journal of Physics D: Applied Physics*, vol. 48, no. 27, p. 275304, Jun. 2015, publisher: IOP Publishing.

[71] N. Zambelli, G. Benassi, E. Gombia, M. Zanichelli, and D. Calestani, "Electroless gold patterning of CdZnTe crystals for radiation detection by scanning pipette technique," *Crystal Research and Technology*, vol. 49, no. 8, pp. 535–539, 2014.

[72] H. S. Kim, S. H. Park, Y. K. Kim, J. H. Ha, S. M. Kang, and S. Y. Cho, "Correlation between the surface roughness and the leakage current of an SSB radiation detector," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 579, no. 1, pp. 117–119, Aug. 2007.

[73] Z. Zhang, B. Wang, P. Zhou, R. Kang, B. Zhang, and D. Guo, "A novel approach of chemical mechanical polishing for cadmium zinc telluride wafers," *Scientific Reports*, vol. 6, p. 26891, May 2016.

[74] S. U. Egarievwe, A. Hossain, I. O. Okwechime, R. Gul, and R. B. James, "Effects of Chemomechanical Polishing on CdZnTe X-ray and Gamma-Ray Detectors," *Journal of Electronic Materials*, vol. 44, no. 9, pp. 3194–3201, Sep. 2015.

[75] S. Singh, L. Montpetit, and O. Moutanabbir, "[unpublished data]etching rate of $Cd_{1-x}Zn_xTe$ in Br:MeOH for increasing concentration," Dec. 2023.

[76] A. Brovko, A. Adelberg, and A. Ruzin, "Effects of surface treatment on static characteristics of In/Cd1-xZnxTe/In and In/Cd1-xMnxTe/In devices," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 957, p. 163387, Mar. 2020.

[77] S. U. Egarievwe, A. Hossain, I. O. Okwechime, A. A. Egarievwe, D. E. Jones, U. N. Roy, and R. B. James, "Effects of chemical treatments on CdZnTe X-Ray and gamma-ray detectors," *IEEE Transactions on Nuclear Science*, vol. 63, no. 2, p. 1091–1098, Apr. 2016.

[78] M. L. Drabo, S. U. Egarievwe, I. O. Okwechime, D. E. Jones, A. Hossain, and R. B. James, "Analysis of te and teo2 on CdZnTe nuclear detectors treated with hydrogen bromide and ammonium-based solutions," *Journal of Materials Science and Chemical Engineering*, vol. 5, no. 44, p. 9–18, Apr. 2017.

[79] K.-T. Chen, D. T. Shi, H. Chen, B. Granderson, M. A. George, W. E. Collins, A. Burger, and R. B. James, "Study of oxidized cadmium zinc telluride surfaces," *Journal of Vacuum Science Technology A*, vol. 15, no. 3, p. 850–853, May 1997.

[80] A. Brovko, O. Amzallag, A. Adelberg, L. Chernyak, P. Raja, and A. Ruzin, "Effects of oxygen plasma treatment on cd1-xznxte material and devices," *Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 1004, 2021.

[81] X. Song, X. Liang, J. Min, J. Zhang, S. Li, P. Qiu, C. Feng, C. Xie, L. Dai, J. Chen, Y. Shen, and L. Wang, "Study on the density of trap states between CdZnTe and passivation layer based on mis structure," *Materials Science in Semiconductor Processing*, vol. 148, p. 106809, Sep. 2022.

[82] M. Bettelli, S. Zanettini, L. Abbene, F. Casoli, L. Nasi, G. Trevisi, F. Principato, A. Buttacavoli, and A. Zappettini, "High performance platinum contacts on high-flux CdZnTe detectors," *Scientific Reports*, vol. 13, no. 1, p. 17963, Oct. 2023.

[83] J. Zázvorka, J. Franc, L. Beran, P. Moravec, J. Pekárek, and M. Veis, "Dynamics of native oxide growth on CdTe and CdZnTe X-ray and gamma-ray detectors," *Science and Technology of Advanced Materials*, vol. 17, no. 1, p. 792–798, Nov. 2016.

[84] X. Cao, J. Zhang, S. Wang, Z. Xu, and L. Wang, "Effect of Ar Plasma Treatment on the Interface and Performance of CdZnTe Detectors," *Crystal Research and Technology*, vol. 58, no. 5, May 2023, publisher: John Wiley and Sons Inc.

[85] B. Song, J. Zhang, X. Liang, S. Zhao, J. Min, H. Shi, J. Lai, and L. Wang, "Effects of the inductively coupled Ar plasma etching on the performance of (111) face CdZnTe detector," *Materials Science in Semiconductor Processing*, vol. 109, Apr. 2020, publisher: Elsevier Ltd.

[86] L. Montpetit, S. Singh, M. R. Atalla, C. Lemieux-Leduc, G. Nadal, and O. Moutanabbir, "CdZnTe surface conditioning using Ar plasma," in *2024 IEEE Nuclear Science Symposium (NSS), Medical Imaging Conference (MIC) and Room Temperature Semiconductor Detector Conference (RTSD)*, Oct. 2024, pp. 1–1, iSSN: 2577-0829.

[87] M. J. Mescher, T. E. Schlesinger, J. E. Toney, B. A. Brunett, and R. B. James, "Development of dry processing techniques for CdZnTe surface passivation," *Journal of Electronic Materials*, vol. 28, no. 6, p. 700–704, Jun. 1999.

[88] "Thorlabs Collimated LEDs, 6500 K Datasheet. MCWHL5-C1, MCWHL5-C2, MCWHL5-C4, MCWHL5-C5, publisher = THORLABS, author = THORLABS, month = nov, year = 2015,."

[89] Keithley, "2470 Graphical SourceMeter SMU Instrument Datasheet," 2023. [Online]. Available: www.TEK.com

[90] A. Hossain, A. Dowdy, A. E. Bolotnikov, G. S. Camarda, Y. Cui, U. N. Roy, R. Tappero, X. Tong, G. Yang, and R. B. James, "Topographic Evaluation of the Effect of Passivation in Improving the Performance of CdZnTe Detectors," *Journal of Electronic Materials*, vol. 43, no. 8, pp. 2941–2946, Aug. 2014.

[91] M. C. Duff, A. Burger, M. Groza, V. Buliga, J. P. Bradley, Z. R. Dai, N. Teslich, S. A. Awadalla, J. Mackenzie, and H. Chen, "Characterization of detector grade CdZnTe material from Redlen Technologies," in *Hard X-Ray, Gamma-Ray, and Neutron Detector Physics X*, vol. 7079. SPIE, Aug. 2008, p. 70790T, iSSN: 0277786X.

[92] E. Erickson and P. De Wolf, *The Definitive AFM Modes Handbook*, ser. Atomic Force Microscopy, S. Hopkins, Ed. Santa Barbara, CA, USA: Bruker. [Online]. Available: www.bruker.com/AFMmodes

[93] V. Bellitto, Ed., *Atomic Force Microscopy : Imaging, Measuring and Manipulating Surfaces at the Atomic Scale*. IntechOpen, 2012, accepted: 2021-04-20T15:28:11Z Journal Abbreviation: Imaging, Measuring and Manipulating Surfaces at the Atomic Scale.

[94] G. Binnig, C. F. Quate, and C. Gerber, "Atomic Force Microscope," *Physical Review Letters*, vol. 56, no. 9, pp. 930–933, Mar. 1986, publisher: American Physical Society.

[95] R. R. L. D. Oliveira, D. a. C. Albuquerque, T. G. S. Cruz, F. M. Yamaji, F. L. Leite, and F. L. Leite, "Measurement of the Nanoscale Roughness by Atomic Force Microscopy: Basic Principles and Applications," in *Atomic Force Microscopy: Imaging, Measuring and Manipulating Surfaces at the Atomic Scale*, V. Bellitto, Ed. IntechOpen, Mar. 2012.

[96] K. Chattopadhyay, X. Ma, J.-O. Ndap, A. Burger, T. E. Schlesinger, C. M. R. Greaves, H. L. Glass, J. P. Flint, and R. B. James, "Thermal treatments of CdTe and CdZnTe detectors," San Diego, CA, Nov. 2000, pp. 303–308.

[97] S. Mergui, M. Hage-Ali, J. M. Koebel, and P. Siffert, "Thermal annealing of gold deposited contacts on high resistivity p-type CdTe nuclear detectors," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 322, no. 3, pp. 375–380, Nov. 1992.

[98] Z. Q. Shi, C. M. Stahle, and P. Shu, "Chemical Etching and Post-Annealing for High Performance CdZnTe Strip Detectors," *MRS Online Proceedings Library*, vol. 487, no. 1, pp. 159–164, Dec. 1997.

[99] S. H. Park, J. H. Ha, J. H. Lee, H. S. Kim, Y. H. Cho, S. D. Cheon, and D. G. Hong, "Effect of temperature on the performance of a CZT radiation detector," *Journal of the Korean Physical Society*, vol. 56, no. 4, pp. 1079–1082, Apr. 2010.

[100] K. H. Kim, S. Hwang, P. Fochuk, L. Nasi, A. Zappettini, A. E. Bolotnikov, and R. B. James, "The Effect of Low-Temperature Annealing on a CdZnTe Detector," *IEEE Transactions on Nuclear Science*, vol. 63, no. 4, pp. 2278–2282, Aug. 2016, publisher: Institute of Electrical and Electronics Engineers Inc.

[101] A. Burger, H. Chen, K. Chattopadhyay, D. Shi, S. Morgan, W. Collins, and R. James, "Characterization of metal contacts on and surfaces of cadmium zinc telluride," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 428, no. 1, p. 8–13, Jun. 1999.

[102] K. Kim, A. E. Bolotnikov, G. S. Camarda, A. Hossain, and R. B. James, "Overcoming Zn segregation in CdZnTe with the temperature gradient annealing," *Journal of Crystal Growth*, vol. 442, pp. 98–101, May 2016.

[103] N. Aslam, E. Jones, T. Noakes, J. Mullin, and A. Willoughby, "The diffusion of zinc in cadmium telluride," *Journal of Crystal Growth*, vol. 117, no. 1-4, pp. 249–253, Feb. 1992.

[104] R. A. Reynolds and D. A. Stevenson, "Self-diffusion of zinc and tellurium in zinc telluride," *Journal of Physics and Chemistry of Solids*, vol. 30, no. 1, pp. 139–147, Jan. 1969.

[105] N. Instruments, "Transmission Electron Microscopy." [Online]. Available: https://www.nanoscience.com/techniques/transmission-electron-microscopy/

[106] Rahier, S. Koelling, G. Nadal, S. Singh, L. Montpetit, and O. Moutanabbir, "CdZnTe extended defect generation in polishing processes [Manuscript in preparation]," 2025.

[107] A. Hiraki, M. Nicolet, and J. W. Mayer, "Low-temperature migration of silicon in thin layers of gold and platinum," *Applied Physics Letters*, vol. 18, no. 5, pp. 178–181, Mar. 1971.

[108] M.-A. Nicolet, "Diffusion barriers in thin films," *Thin Solid Films*, vol. 52, no. 3, pp. 415–443, Aug. 1978.

[109] "Au (Gold) Binary Alloy Phase Diagrams," in *Alloy Phase Diagrams*, ser. ASM Handbook, H. Okamoto, M. Schlesinger, and E. Mueller, Eds., Apr. 2016, vol. 3, pp. 152–174.

[110] M. Fiederle, V. Babentsov, J. Franc, A. Fauler, and J.-P. Konrath, "Growth of high resistivity CdTe and (Cd,Zn)Te crystals," *Crystal Research and Technology*, vol. 38, no. 7-8, pp. 588–597, 2003.

[111] W. Mönch, *Semiconductor Surfaces and Interfaces*, ser. Springer Series in Surface Sciences, G. Ertl, R. Gomer, H. Lüth, and D. L. Mills, Eds. Berlin, Heidelberg: Springer Berlin Heidelberg, 2001, vol. 26.

[112] X. Huang, E. Lindgren, and J. R. Chelikowsky, "Surface passivation method for semiconductor nanostructures," *Physical Review B*, vol. 71, no. 16, p. 165328, Apr. 2005, publisher: American Physical Society.

[113] "Metal-Semiconductor-Metal (MSM) Photodetector," in *Complete Guide to Semiconductor Devices*. IEEE, 2010.

[114] J.-h. Min, X.-y. Liang, Z.-x. Liu, J.-j. Zhang, Y. Zhao, L.-j. Wang, and Y. Shen, "Passivation effect and stability of diamond-like carbon film on CdZnTe devices," *Journal of Electronic Materials*, vol. 47, no. 8, p. 4388–4393, Aug. 2018.

[115] N. Ohtake, M. Hiratsuka, K. Kanda, H. Akasaka, M. Tsujioka, K. Hirakuri, A. Hirata, T. Ohana, H. Inaba, M. Kano, and H. Saitoh, "Properties and classification of diamond-like carbon films," *Materials*, vol. 14, no. 2, p. 315, Jan. 2021.

[116] S. Zanettini, F. Pattini, N. S. Amade, M. Sidoli, N. Zambelli, G. Benassi, M. Bettelli, S. Rampino, E. Gilioli, N. Protti, S. Fatemi, and A. Zappettini, "Al_2O_3 coating as passivation layer for CZT-based detectors," in *2018 IEEE Nuclear Science Symposium and Medical Imaging Conference, NSS/MIC 2018, November 10, 2018 - November 17, 2018*, ser. 2018 IEEE Nuclear Science Symposium and Medical Imaging Conference, NSS/MIC 2018 - Proceedings. Sydney, NSW, Australia: Institute of Electrical and Electronics Engineers Inc., 2018.

[117] G. G. Politano and C. Versace, "Spectroscopic Ellipsometry: Advancements, Applications and Future Prospects in Optical Characterization," *Spectroscopy Journal*, vol. 1, no. 3, pp. 163–181, Dec. 2023, number: 3 Publisher: Multidisciplinary Digital Publishing Institute.

[118] G. E. Jellison, Jr. and F. A. Modine, "Parameterization of the optical functions of amorphous materials in the interband region," *Applied Physics Letters*, vol. 69, no. 3, pp. 371–373, Jul. 1996.

[119] S. Lombardo, J. H. Stathis, B. P. Linder, K. L. Pey, F. Palumbo, and C. H. Tung, "Dielectric breakdown mechanisms in gate oxides," *Journal of Applied Physics*, vol. 98, no. 12, p. 121301, Dec. 2005.

[120] V. Sklyarchuk, P. Fochuk, Z. Zakharuk, R. Grill, V. Kutny, A. Rybka, D. Nakonechny, A. Zakharchenko, Y. Nykoniuk, A. E. Bolotnikov, and R. B. James, "Effect of side-surface passivation on the electrical properties of metal-Cd(Zn)Te-metal structures," in *Hard X-Ray, Gamma-Ray, and Neutron Detector Physics XV*, vol. 8852. SPIE, Sep. 2013, p. 88521I, iSSN: 0277786X.

[121] A. Bolotnikov, G. Carini, A. Dellapenna, G. Deptuch, J. Fried, S. Herrmann, M. Laassiri, W. Lee, P. Maj, A. Moiseev, G. Pinaroli, M. Sasaki, L. Smith, E. Tamura, and E. Yates, "3x3 array module of 8×8×32 mm3 position-sensitive virtual frisch-grid CdZnTe detectors for imaging and spectroscopy of cosmic gamma-rays," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 1064, p. 169328, Jul. 2024.

APPENDIX A APPENDIX 1: ELLIPSOMETRY Ψ AND Δ CURVES OF SIN_X

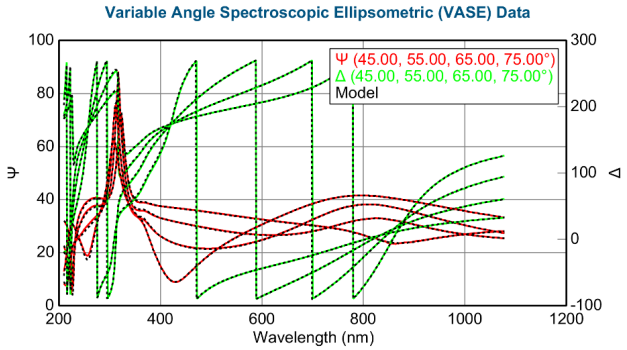


Figure A.1 Ψ and Δ curve and their respective fit from a Tauc-Lorentz dielectric function for SiN_x. The MSE is 7.345.

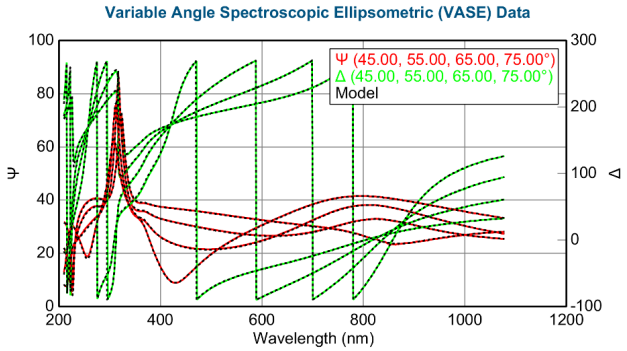


Figure A.2 Ψ and Δ curve and their respective fit from a Code-Lorentz dielectric function for SiN_x. The MSE is 6.904.