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LOW POWER LOW VOLTAGE SIGMA-DELTA MODULATORS

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DÉPARTEMENT DE GÉNIE ÉLECTRIQUE
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MÉMOIRE PRÉSENTÉ EN VUE DE L'OBTENTION
DU DIPLÔME DE MAÎTRISE ÈS SCIENCES APPLIQUÉES
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Ce mémoire intitulé:

LOW POWER LOW VOLTAGE SIGMA-DELTA MODULATORS

Présenté par: ZHIJUN LU

en vue de l'obtention du diplôme de : Maîtrise ès sciences appliquées

a été dûment accepté par le jury d'examen constitué de :

M. AUDET, Yves, Ph.D., président

M. SAWAN, Mohamad, Ph.D., membre et directeur de recherche

M. FAYOMI, Christian, Ph.D., membre

DEDICATION

To all my friends

ACKNOWLEDGEMENTS

I sincerely thank my supervisor, Professor Mahamad Sawan, for his excellent supervision and guidance throughout the course of this master thesis work. His kindness, patience and encouragement during my master degree study at Ecole Polytechnique deserve my deepest gratitude. His guidance and insight ensured our project's success. It was both an honor and privilege to work with him.

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RÉSUMÉ

Les techniques de modulation de sur-échantillonnage et de filtrage de bruit sont devenues très populaires dans le domaine des convertisseurs analogiques-numériques (CAN) de haute résolution, et des générateurs de signaux. Le sur-échantillonnage et le filtrage de bruit représentent les techniques de base des CAN sigma-delta ($\Sigma\Delta$). La popularité de ces techniques découle du fait que leur implémentation n'est pas reliée beaucoup à la précision des modules analogiques et du gain des amplificateurs. Ceci est principalement dû à l'utilisation des modules de traitement de signal numérique. De nos jours, les modulateurs $\Sigma\Delta$ sont intégrés en utilisant des techniques de capacités commutées, qui sont bien adaptées pour le traitement de signaux en technologies CMOS standard. Une des caractéristiques importantes des circuits à capacités commutées est que leur précision ne dépend pas de la valeur absolue des capacités mais de la valeur de rapport de capacités.

Le but de ce mémoire de maîtrise est la conception de modulateurs analogique à numérique de très faible puissance. En plus de la faible puissance, ces modulateurs devront opérer à de basses tensions d'alimentation et posséder de larges plages dynamiques d'entrée et de sortie. Ces conditions sont principalement dictées par les applications visées, qui se situent dans le domaine des systèmes électroniques implantables.

Deux modulateurs ΣΔ à faible puissance et basse tension d'alimentation sont développés, l'un de deuxième ordre et l'autre de quatrième ordre. Les deux modulateurs sont réalisés en utilisant un intégrateur à capacité-commutée de demi-délai, qui est basé sur la technique d'amplificateur opérationnel à transconductance (OTA) à commutation. L'utilisation de ce genre d'intégrateur permet de réduire la consommation de puissance et de surmonter les problèmes reliés aux commutateurs, qui nécessitent des tensions élevées indispensables pour les faire fonctionner à basse tension. Outre cet intégrateur, nous avons utilisé un multiplicateur de tension pour alimenter l'étage d'entrée de l'amplificateur OTA. Ce multiplicateur sert à doubler les tensions au niveau de l'étage d'entrée de l'OTA dans le but d'améliorer la plage dynamique des modulateurs. Ces modulateurs fonctionnent avec une basse tension d'alimentation (0.9V) et possèdent de larges plages dynamiques de mode commun d'entrée (0-1.2V) et de sortie (0.05V-0.85V).

Le modulateur ΣΔ deuxième ordre est fabriqué en technologie CMOS 0.18 um de TSMC disponible à travers la société canadienne de microélectronique (SCM). Sa surface active est de 800μm×800μm. Les résultats de simulation démontrent que le rapport signal sur bruit (Signal-to-Noise Ratio, SNR) de ce modulateur est égal à 74 dB dans la plage de fréquences de 0 à 10 KHz. La valeur mesurée du SNR est de l'ordre de 65 dB. La dissipation totale de puissance estimée par simulation est égale à 38 μW en utilisant le calculateur de l'outil de Cadence et celle mesurée est égale à 66 μW. De plus, le modulateur ΣΔ de quatrième ordre proposé a été implémenté et caractérisé. Ses résultats

de simulation montrent une consommation de puissance de 86 µW et un SNR de 90 dB dans la même bande de fréquence d'intérêt. Le modulateur a été originalement conçu pour des applications biomédicales, mais il peut être utilisé dans toute application nécessitant une conversion analogique à numérique dans les basses fréquences.

ABSTRACT

The oversampling and noise shaping modulation techniques are becoming popular to design high resolution analog-to-digital converters (ADCs) and signal generators. Oversampling and noise shaping are the two key techniques employed in the sigma-delta ($\Sigma\Delta$) ADCs. The reason for their popularity comes from their implementations, which rely less on the matching of analog components and amplifier gains, and more on digital signal processing. Nowadays, switched-capacitor technique has been a popular method of implementing analog signal processing circuits in standard CMOS technologies. One of the important reasons for the success of switched-capacitor circuits is that the accuracy of signal processing function is proportional to the accuracy of capacitor ratios.

The aim of this master thesis is to design very low power analog-to-digital modulators. The proposed circuits work under low supply voltages since they are designed for implantable sensing applications. Under low voltage supply, the required modulators should have wide signal input and output swing ranges.

Two low power low voltage analog-to-digital $\Sigma\Delta$ modulators are implemented. The first one is a second-order modulator, and the second is a fourth-order. Both of them are designed by using half delay switched-capacitor integrator based on switched-opamp technique. Also, we used voltage multiplier to boost the voltage in order to power up the input stage of the operational transconductance amplifier (OTA). A half delay integrator,

based on switched-opamp technique, is used to save power and solve low voltage switch driving problem. Voltage multiplier provides boosted voltage to OTA input pair to guarantee the operation of the modeling with rail-to-rail signal swing, thus enlarge dynamic range of modulators. The modulators work under low voltage supply (0.9V) with a wide input (0-1.2V) and output (0.05-0.85V) voltage ranges.

The proposed 2^{nd}-order modulator, has been implemented and fabricated using the 0.18 μm CMOS technology offered by Taiwan Semiconductor Manufacturing Co.,LTD (TSMC), which achieves a simulated peak SNR of 74 dB with the signal bandwidth 10 kHz and measured value is 65 dB. The simulated total power dissipation is around 38 μW and the measured value gives 66 μW. The chip core area is 800μm×800μm. In addition, the proposed 4^{th}-order modulator has been implemented and characterized. Its simulation result gives a power dissipation of 86 μW and a SNR of 90 dB within the same bandwidth. The modulator, originally designed for biomedical sensing applications, can be used for any low pass analog-to-digital conversion applications.

CONDENCÉ EN FRANÇAIS

I. INTRODUCTION

La croissance rapide du marché des systèmes électroniques portatifs a créé un grand besoin pour le développement de convertisseurs analogique-numérique (CAN) de haute résolution, de basse tension d'alimentation, et de faible puissance. La modulation sigma-delta (ΣΔ) représente un moyen promoteur pour le développement de ce genre de CAN. La figure 1 montre un schéma bloc simplifié d'un CAN ΣΔ composé principalement d'un filtre anti-recouvrement, d'un échantillonneur-bloqueur, d'un modulateur ΣΔ et d'un filtre passe-bas numérique de décimation de valeurs obtenues.

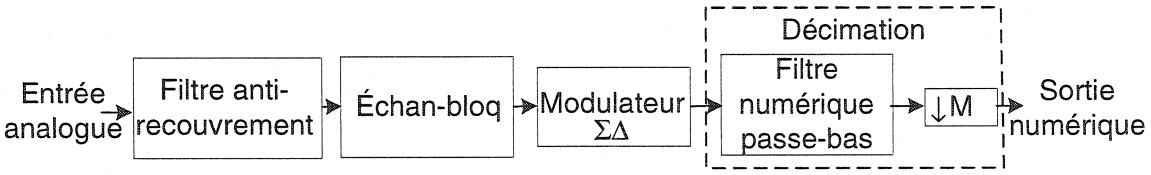

Figure 1 Schéma bloc d'un CAN ΣΔ.

Comme le modulateur ΣΔ est basé sur la technique de sur-échantillonnage, l'utilisation de filtre anti-recouvrement est non nécessaire. Selon le théorème d'échantillonnage de Nyquist, il est possible d'éviter le problème de recouvrement si la technique de sur-échantillonnage est utilisée. Dans de tels cas, l'échantillonnage est effectué, d'une manière inhérente, par un circuit modulateur ΣΔ basé sur la technique de capacités-

commutés (CC), qui comprend des amplificateurs opérationnels (amp-op), des condensateurs, des commutateurs, et des horloges sans recouvrement.

La frontière entre la partie analogique et la partie numérique du convertisseur se situe à la sortie du modulateur ΣΔ pour les modulateurs simples à une seule boucle. Le bloc de décimation comprend un filtre passe-bas et un sous-échantillonneur, qui constituent la partie numérique du modulateur. Le rôle de ce filtre consiste à éliminer le bruit de quantification en dehors de la bande passante.

La figure 2 montre le schéma fonctionnel de base d'un modulateur ΣΔ composé d'un intégrateur, un comparateur, et un convertisseur numérique à analogique (CNA) de rétroaction de 1-bit.

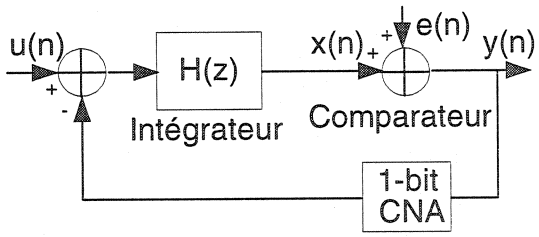

Figure 2 Schéma fonctionnel linéaire de base d'un modulateur ΣΔ

La fonction de transfert $S_{TF}(z)$ de ce système et celle du bruit $N_{TF}(z)$ sont données par les équations suivantes :

$$S_{TF}(z) \equiv \frac{Y(z)}{U(z)} = \frac{H(z)}{1+H(z)} \tag{1}$$

$$N_{TF}(z) \equiv \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} \tag{2}$$

À partir de l'équation (2), on peut déduire que le zéro de la fonction de transfert du bruit $N_{TF}(z)$ est égale au pole de H(z). En d'autres termes, si H(z) s'approche à l'infini, la valeur de $N_{TF}(z)$ devient égale à zéro. Dans le domaine fréquentiel, la fonction de transfert du modulateur ΣΔ peut être exprimée par l'équation suivante:

$$Y(z) = S_{TF}(z)U(z) + N_{TF}(z)E(z) \tag{3}$$

Pour minimiser le bruit de quantification, le module de *H(z)* devrait être très grand dans la bande de fréquence qui s'étend de 0 à f_0. Une grande valeur de *H*(z) permet aux fonctions de transfert $H_{TF}(z)$ et $N_{TF}(z)$ de prendre respectivement les valeurs approximativement 1 et 0 dans la bande de fréquence d'intérêt, et par conséquent, elle permet de réduire le bruit de quantification. Comme, la rétroaction du modulateur ne permet pas de filtrer le bruit de hautes fréquences, le convertisseur ΣΔ nécessite un filtre additionnel passe-bas numérique. Le principe de base du modulateur ΣΔ peut être bien expliqué à l'aide des figures 3 et 4.

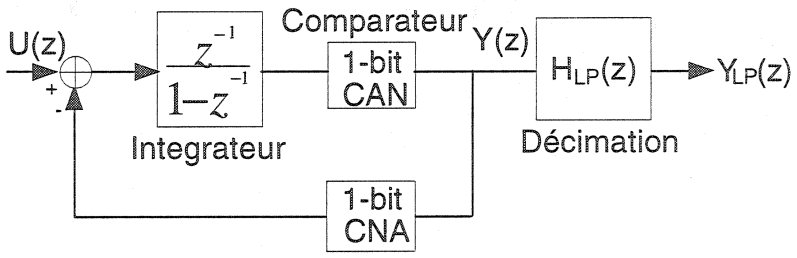

Figure 3 Diagramme bloc du modulateur ΣΔ

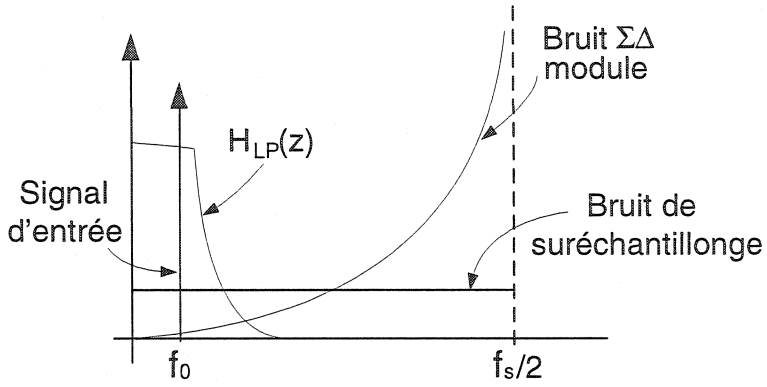

Figure 4 Principe de sur-échantillonnage et filtrage de bruit

Le travail présenté dans ce mémoire consiste à développer un modulateur ΣΔ de basse tension d'alimentation et de faible consommation de puissance. Ce travail s'inscrit dans le cadre des travaux de recherche en bioélectronique de notre équipe de recherche PolySTIM, qui est axé sur la réalisation de systèmes électroniques implantables (SEI) de hautes performances. Parmi les applications de ces systèmes, on trouve la stimulation fonctionnelle électrique (SFE) qui permet la restauration de la fonctionnalité des organes paralysés chez les humains [18]. La stimulation fonctionnelle électrique nécessite tout d'abord, la détection et la mesure du signal bioélectrique du nerf. Ce signal est ensuite amplifié et converti en données numériques qui sont transmises à un contrôleur externe par l'intermédiaire d'un lien inductif, puis traitées par un module de traitement de signal spécifique. Le modèle de base d'une application typique de SFE est illustré sur la figure 5. Nous proposons un modulateur ΣΔ de $2^{éme}$-order pour réaliser la conversion analogique à numérique de signaux mesurés en raison de ses multiples avantages. En premier lieu, elle permet la réalisation de conversion de haute résolution avec de faible

consommation de puissance pour des applications à basses fréquences. En second lieu, sa modulation du rapport-cyclique (PWM) est très adéquate pour la transmission de données sans fil. Comme l'énergie totale, nécessaire au fonctionnement de l'implant, est transférée par le lien inductif à travers la peau, et que le modulateur ΣΔ doit fonctionner sur une longue durée, le circuit résultant ne doit pas consommer très peu d'énergie.

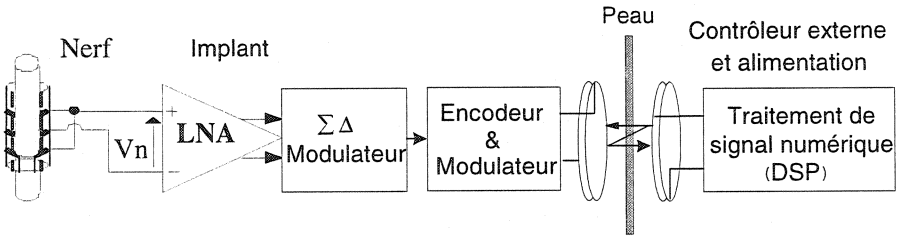

Figure 5 Diagramme bloc d'une chaîne implantable de mesure de signaux bioélectriques

Le modulateur ΣΔ présente aussi les avantages suivants: simplification du filtre anti-recouvrement [6], simple programmation (contrôle du SNR par la modification du OSR ou par le changement de l'ordre du modulateur), et sa monotonicité inhérente [33]. Pour des considérations de faible puissance et de basse tension d'alimentation, un modulateur ΣΔ deuxième ordre est tout d'abord favorisé pour réaliser un modulateur de $4^{ème}$ ordre. Le modulateur proposé est axé principalement sur un faible consommation puissance, une basse tension d'alimentation, et finalement, une large gamme dynamique.

II. IMPLEMEMTATION DU CIRCUIT À BASSE TENSION D'ALIMENTATION ET À FAIBLE CONSOMMATION DE PUISSANCE

Les modulateurs ΣΔ proposés sont de deuxième et de quatrième ordres et sont mis en oeuvre par l'intermédiaire de deux techniques. Ces dernières sont un intégrateur à demi-délai basé sur un amplificateur opérationnel commuté (amp-op-C) et un doubleur de tension. Ainsi, la première technique est utile pour la dissipation de puissance et la réduction du nombre de commutateurs critiques. Quant à la deuxième technique, elle est indispensable pour atteindre la gamme dynamique de « rail-to-rail » et pour concevoir un bon commutateur conductif.

1. Conception des différents blocs de circuit

Le diagramme bloc d'un modulateur ΣΔ de deuxième ordre est montré à la figure 6. Ceci est constitué de deux intégrateurs à demi-délai, d'un comparateur et d'un CNA à 1 bit. Le circuit de capacités commutées est exploité pour mettre en application l'intégrateur grâce à sa précision élevée et à sa caractéristique inhérente d'échantillonnage. Trois différentes unités de gain (A1~A3) sont présentées et ajustées dans le chemin direct et dans la boucle de rétroaction respectivement. Ceci réduit la possibilité de saturation de l'intégrateur et améliore la linéarité du CAN.

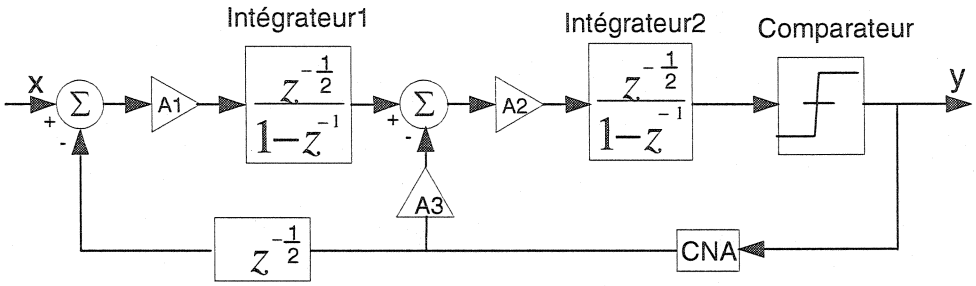

Figure 6 Diagramme bloc du modulateur ΣΔ de second ordre basé sur des intégrateurs à demi-délai

2. Intégrateur à demi-délai

La technique de l'amp-op commuté s'est avérée une solution prometteuse pour opérer à basse tension et la moins coûteuse pour réaliser des circuits de capacités commutées avec la technologie standard CMOS. Cette technique élimine fondamentalement les commutateurs critiques garantissant ainsi une tension d'alimentation minimale nécessaire au fonctionnement à basse tension du circuit à condensateurs commutés sans problème de fiabilité [33]. La figure 7 illustre un intégrateur conventionnel, peu sensible, basé sur la technique de capacités commutées. Il est à noter que la sortie de l'intégrateur conventionnel est disponible à tout moment pour être traitée à l'étape suivante. En conséquence, premièrement, la sortie de l'intégrateur à demi-délai est disponible au circuit de l'étage suivant pendant la phase de la mise en veilleuse (Idle) Φ_2 de d'intégrateur. L'amp-op est fondamentalement en état de veilleuse pendant la phase Φ_2 après avoir exécuté la phase d'intégration (Φ_1). Deuxièment, la sortie de l'intégrateur à demi-délai est prise par le circuit de l'étage suivant durant sa phase d'intégration (Φ_2).

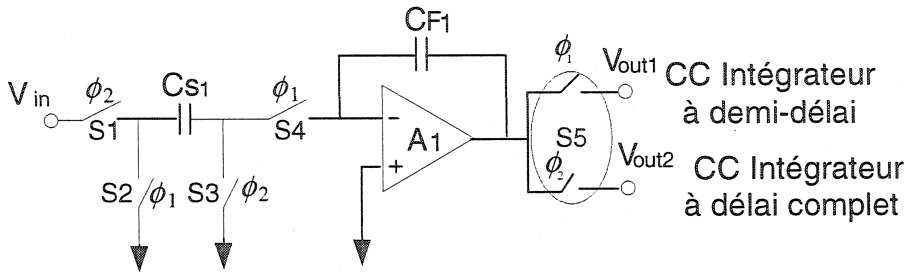

Figure 7 Intégrateur conventionnel basé sur des capacités commutées (CC)

La figure 8 illustre un intégrateur basé sur l'amp-op commuté qui est équivalent à l'intégrateur conventionnel et il est réalisé par des capacités commutées. Cet intégrateur à délai complet est mis en oeuvre avec un amp-op commuté en ajoutant une cellule additionnelle au circuit à demi-délai. Cette cellule est réalisée avec un amp-op commuté supplémentaire (A_e).

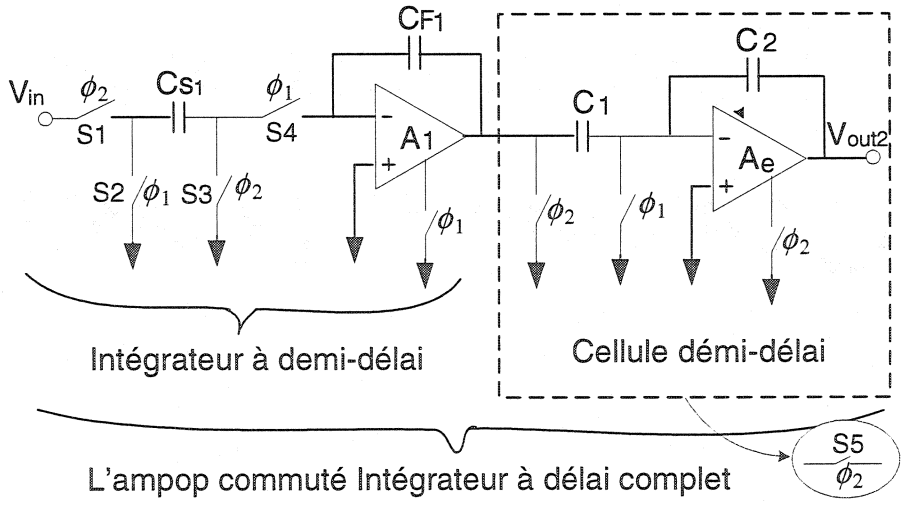

Figure 8 L'intégrateur basé sur l'amp-op commuté

Nous avons choisi de réaliser l'intégrateur basé sur l'amp-op commuté à demi-délai sans utiliser la cellule «switched-opamp» à demi-délai (amp-op commuté supplémentaire). La fonction de la cellule à demi-délai a été remplacée par la fonction marche et arrêt de l'amp-op commuté (A1). Cette structure équivaut à l'intégrateur conventionnel de demi-délai réalisé par des capacités commutées. De plus, la puissance dissipée d'un intégrateur basé sur l'amp-op commuté à demi-délai est réduite de 50% comparé à un intégrateur conventionnel basé sur les condensateurs commutés. La raison est que l'amp-op A1 arrête de fonctionner après la phase d'intégration.

Il est à noter que le mode entièrement différentiel est adopté pour réduire les harmoniques paires causées par la distorsion. De plus, une rétroaction du mode commun (CMFB) est indispensable pour fixer la tension DC du nœud de sortie. Afin de réaliser une opération «rail-to-rail» de classe AB avec une basse tension d'alimentation, il est nécessaire de fournir un doubleur de tension aux deux branches d'entrée de l'OTA. Les branches de sortie fonctionnent toujours sous une basse tension d'alimentation afin de réduire la puissance dissipée.

3. Le circuit doubleur de tension

Nous avons conçu un modulateur ΣΔ fonctionnant à une basse tension d'alimentation de 900 mV. Afin de maximiser la gamme de traitement des signaux, comme il a été mentionné ci-dessus, un doubleur de tension sur puce est introduit. D'une part, il produit la tension amplifiée ainsi que les horloges amplifiées aux deux branches d'entrée de

l'OTA et d'autre part, la faible tension d'alimentation ainsi que la transconductance du commutateur en technologie CMOS peuvent être sensiblement altérées. Afin de permettre l'opération en basse alimentation, le doubleur de tension sur puce produit une tension élevée entre la grille et la source du commutateur pour améliorer sa transconductance.

4. Autres modules importants

Le générateur d'horloge fournit des signaux sans recouvrement avec des horloges complémentaires et d'autres avec délai, qui commandent les portes de transmission. Ces horloges avec délai réduisent l'injection de charge (clock feedthrough). Ces signaux d'horloges sont montrés à la figure 9.

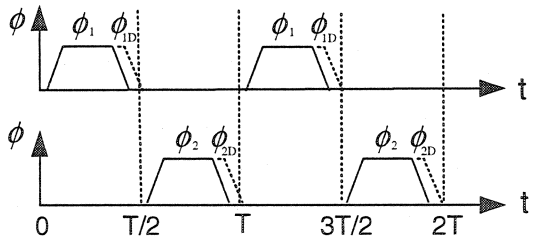

Figure 9 Horloges sans recouvrement typiques ainsi que les horloges avec délai.

Considérant la linéarité du quantificateur, le circuit de rétroaction du CNA à un bit est mis en oeuvre à l'aide d'un commutateur CMOS commandé par la sortie du comparateur. Les tensions de références de rétroaction V_{low} et V_{high} dépendent de la gamme dynamique du signal de sortie.

III. SIMULATION ET RÉSULTATS EXPÉRIMENTAUX

Le modulateur ΣΔ de deuxième ordre a été fabriqué en technologie CMOS 0.18 um de TSMC disponible par le biais de la Société canadienne de microélectronique (SCM). De plus, le modulateur ΣΔ de quatrième ordre proposé a été implémenté et caractérisé. D'abord, nous montrons les résultats de la simulation ainsi que les résultats expérimentaux du modulateur ΣΔ de deuxième ordre respectivement. Ensuite, nous présenterons les résultats de simulation du modulateur ΣΔ quatrième ordre.

1. Simulation et résultats expérimentaux du modulateur ΣΔ de deuxième ordre

Le modulateur ΣΔ de deuxième ordre et de faible puissance a été simulé. Il a réalisé une gamme dynamique de 78 dB, un SNR maximale de 74 dB et un SNDR de 65 dB en considérant une largeur de bande de signal de 10 KHz. Aussi, la puissance dissipée totale (dynamique et statique) est de 38 μW. L'aire totale du modulateur ΣΔ de deuxième ordre est de 800 μm x 800 μm. Les résultats expérimentaux indiquent que ce modulateur réalise un SNR de 65 dB et un SNDR de 46 dB. La différence entre les résultats de simulation et les résultats expérimentaux est due aux effets de la capacité additionnelle de chaque « pad » ainsi que la capacité du « wire-bonding ».

2. Résultats de simulation du modulateur ΣΔ de quatrième ordre

Le modulateur ΣΔ de quatrième ordre proposé est basé sur l'architecture de « MASH » qui est composée de deux modulateurs ΣΔ de deuxième ordre avec un circuit numérique

d'annulation. Les résultats de simulation montrent une consommation de puissance de 86 μW et un SNR de 90 dB dans la même bande de fréquence.

IV. CONCLUSION

Les modulateurs proposés, qui utilisent des intégrateurs à demi-délai, basés sur la technique de l'amplificateur opérationnel commuté dissipent moins de puissance et réduisent au minimum le nombre de commutateurs critiques. Un doubleur de tension a été utilisé pour pouvoir atteindre la gamme dynamique « rail-to-rail » ainsi que pour avoir un bon commutateur conducteur. La puissance dissipée du modulateur de deuxième ordre est à peu près de 38 μW. Les valeurs maximales simulées de SNR et de SNDR sont de 74 dB et de 65 dB respectivement. Les résultats expérimentaux ont montré que le SNR et le SNDR par rapport à ce modulateur sont de 65 dB et de 46 dB respectivement dans une charge capacitive sur chaque pin. Bien qu'il y ait des différences entre les résultats de simulation et les résultats expérimentaux, nous avons pu démontrer la faisabilité de la conception d'un modulateur ΣΔ à basse tension et à faible puissance dissipée en ayant recours à la technique de l'amp-op commuté avec un doubleur de tension intégré sur la puce. Le modulateur qui était à l'origine conçu pour des applications biomédicales, peut être utilisé pour toutes les applications de basse fréquence de conversion analogique à numérique.

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LIST OF ABBREVIATIONS

A/D, AD	Analog-to-Digital
ADC	Analog-to-Digital Converter
BW	Signal Bandwidth
CMFB	Common Mode Feedback
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common Mode Rejection Ratio
D/A, DA	Digital-to-Analog
DAC	Digital-to-Analog Converter
DCC	Digital Cancellation Circuit (Circuitry)
DR	Dynamic Range
DSP	Digital Signal Processing
FES	Functional Electrical Stimulation
GBW	Unit Gain Bandwidth
IC	Integrated Circuit
ICMR	Input Common Mode Range
MASH	Multi-Stage Noise Shaping
MOSFET	Metal Oxide Field Effect Transistor
MUX	Multiplexer
NMOS	Channel-N Metal Oxide Semiconductor
OSR	Oversampling Ratio

OTA	Operational Transconductance e Amplifier
PMOS	Channel-P Metal Oxide Semiconductor
PSD	Power Spectral Density
PSRR	Power Supply Rejection Ratio
PWM	Pulse Width Modulated
SC	Switched-Capacitor
SCI	Switched-Capacitor Integrator
SC-CMFB	Switched-Capacitor Common Mode Feedback
SNDR	Signal to Noise and Distortion Ratio
SNR	Signal to Noise Ratio
SO	Switched-Opamp
SOI	Switched-Opamp Integrator

LIST OF APPENDIXES

CHAPTER 1

INTRODUCTION

1.1 Motivation

Nowadays more and more portable electronic applications such as communication devices, computing, electronic medical devices, etc., are being available on the market. Both low power and low voltage techniques are becoming primary concerns when designing integrated circuit (IC) for such applications, due to design requirements such as small size, low weight and long lifetime of power supply devices [33] [36] [19].

The explosive growth in the portable electronic system market has led to the need of low power and low voltage analog-to-digital converters (ADCs) with high resolution [33]. Sigma-delta ($\Sigma\Delta$) modulation has become a popular means of implementing high resolution ADCs by using oversampling technique and feedback noise shaping, and using digital lowpass filter easily remove the noise that has been pushed out of the signal bandwidth. It is possible to achieve a suitable dynamic range according to the specification requirements with modest oversampling ratio (OSR) [7]. Furthermore, oversampling architectures are potentially an efficient means of implementing high-resolution ADCs. In fact, an increase in oversampling rate can be used to reduce the complexity of required analog circuits, transferring much of the signal processing into the digital domain where power consumption can be dramatically reduced by scaling the technology and reducing the supply voltage [36]. Therefore, choosing sigma-delta

architecture for ADCs offers several main advantages comparing with conventional Nyquist ADC:

- Relaxed requirements of analog circuitry. Analog requirements, such as precise component matching and large amplifier gain, can be reduced at the expense of more complicated digital signal processing (DSP). This tradeoff becomes more desirable for modem submicron technologies with low power supply where complicated high-speed digital circuitry is more easily realized in less area, but the realization of high-resolution analog circuitry is complicated under low power supply voltages [6][20]. With oversampling and noise shaping data converters, the analog components have reduced requirements on matching tolerance and amplifier gains. The analog part of these converters is relatively simple and occupies a small area, unlike their Nyquist rate counterparts [36].
- Minimum requirements for analog anti-aliasing filters. We compare the frequency spectrum of conventional Nyquist ADC and an oversampling ADC. Usually the Nyquist rate is much less than the sampling rate. Antialiasing filter requirements of oversampling ADCs are much more relaxed than those of Nyqist rate converters. The reason for this is that the sampling frequency is much higher than the Nyquist rate in oversampling converters. In most cases, a simple single pole RC-filter suffices to avoid aliasing without causing any phase distortion in the signal band [31].
- Easily programmable. It is easy to modify signal-to-noise ratio (SNR) by modifying OSR or changing the order number of modulator (noise shaping) [33].

- Generally, in the case of implementation, the sigma-delta modulators use switched capacitor technique, dedicated sampling/holding circuits are not required, because sampling is performed inherently using the switched-capacitor circuit [33].

Figure1.1 shows the simplified block-diagram of an ΣΔ ADC system. It consists of an anti-aliasing filter, a sample and hold circuit, the ΣΔ modulator itself, a digital low pass filter and a down sampler.

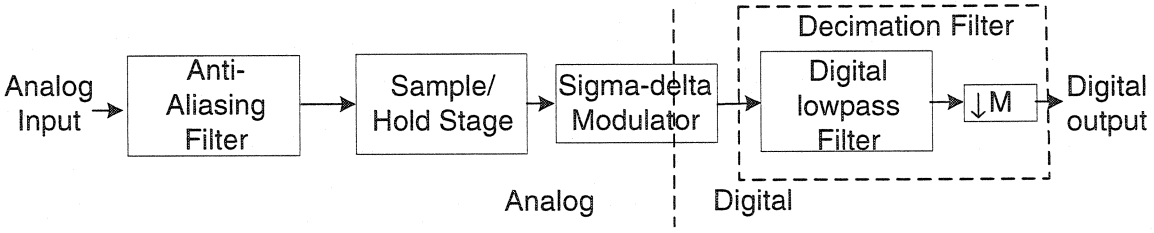


Figure 1.1 The simplified ΣΔ ADC system

The anti-aliasing filter is in most cases very simple since ΣΔ architecture is based on oversampling technique. According to Nyquist sampling theorem, it is easy to avoid aliasing by using oversampling technique. The sampling is inherently performed in a switched-capacitor circuit. A switched-capacitor circuit is realized with the use of some basic building blocks such as opamps, capacitors, switches, and nonoverlapping clocks. The boundary between analog and digital is at the output of the delta-sigma modulator for single loop modulators. The decimation filter includes the low pass filter and the down-sampler forming the digital circuit part. The work presented in this master thesis is to design novel low power ΣΔ modulators.

Furthermore, the special motivation to build low power low voltage 2^{nd}-order ΣΔ modulator is to contribute to the bioelectronics projects conducted by our PolySTIM research team.

With the development of the bioelectronics devices, the integration of complex functions in single chip makes functional electrical stimulation (FES) becoming a more and more promising technique to restore functions of paralyzed human body organs [18]. Also monitoring a signal from nerve is one of the important requirements for these FES applications [18]. The nerve signal is first amplified by a low noise amplifier and then converted to digital format. The digital signal is modulated and encoded and then sent to an external controller through an inductive link, and processed there by a DSP block. The basic model of such applications is shown in Figure 1.2. One 2^{nd}-order ΣΔ modulator is proposed to realize the conversion from analog to digital due to its following advantages: first it is capable of achieve a high resolution in low frequency applications without consuming much power; secondly, it is a pulse width modulated (PWM) signal that is suitable for wireless transmission, and further signal processing can be achieved in the external controller.

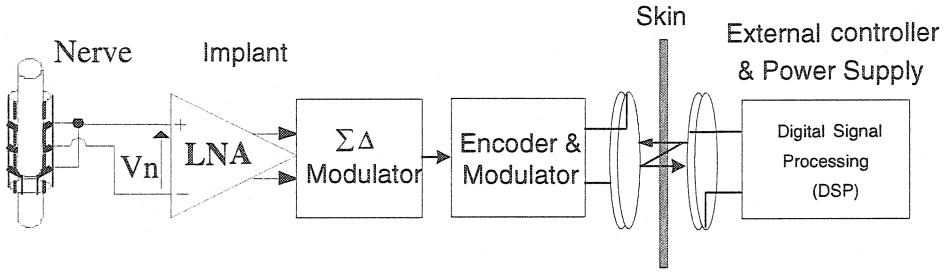


Figure 1.2 Block diagram of a typical implantable monitoring chain

As the power of the whole implantable circuitry is provided through a transcutaneous link via the skin, low power consumption of these blocks is demanded to relax the requirement of power transferring of the transcutaneous link and prolong the longevity of external battery.

1.2 Research goals

The aim of this project is to design a low power low voltage ΣΔ modulator in standard CMOS process. We will focus on developing techniques at both the architecture and circuit design levels to minimize power dissipation in ΣΔ modulators, and to satisfy other requirements in its specification. In particular, research requirements are summarized below:

- Low power consumption and low supply voltage, because energy is transmitted from outside the human body through the skin. Special attention must be paid for the monitoring part of implantable devices to reduce such power dissipation.
- Enlarge signal swing range for high dynamic range.
- High power supply rejection ratio (PSRR) to avoid degrading SNR, since the variation of the power supply caused by the bi-directional link must not affect the stimulation operations.
- High common mode rejection ratio (CMRR) to overcome the relatively high common mode input voltage.
- Fully integrated device in a low-die-area in order to reduce the physical dimensions of the implant.

1.3 Master thesis organization

The organization of this master thesis is as follow. We introduce in chapter 2 the low and high orders ΣΔ modulator topologies firstly. Then, we discuss different methods of single-loop and multi-stages ΣΔ modulators and their comparison.

We discuss power consumption issues of analog circuit in chapter 3, such as power dissipation vs. supply voltage and power dissipation vs. dynamic range (DR). Next, we introduce the limitations imposed by the restriction of low supply voltage. Third, the main previous works that include voltage multiplier and switched-opamp (SO) technique will be presented. Finally, the literature review of low power and low voltage ΣΔ modulators will be given, and the advantages and disadvantages of various low voltage techniques will be discussed.

In chapter 4, we focus on how to realize a low power low voltage second-order ΣΔ modulator with half delay integrators based on switched-OTA. First, we describe low power low voltage ΣΔ modulator and its limitation. Furthermore, we illustrate detailed circuit implementation of novel and existing building blocks, such as a new class AB switched operational transconductance amplifier (switched-OTA), common mode feedback (CMFB) circuit, quantizer, charge pump.

Chapter 5 deals with the implementation of a low power low voltage fourth-order ΣΔ modulator with multi-stage noise shaping (MASH), which uses two second-order (2-2

cascaded structure) ΣΔ loops in a MASH configuration. The modulator still uses half delay integrators based on switched-OTA with digital cancellation circuitry (DCC). Then, we analyze how to choose coefficients to solve saturation problem.

We present results of two proposed ΣΔ modulators in chapter 6. First, we give the simulation results and testing results of novel second-order ΣΔ modulator with fully differential OTA. Then, we present simulation results of proposed fourth-order ΣΔ modulator. Also we give the comparison between testing and simulation results. Finally, the conclusion of our study is presented.

CHAPTER 2

FUNDAMENTALS OF ΣΔ MODULATORS

2.1 Introduction

Analog-to-digital conversion is an essential function in modern signal processing systems. ΣΔ modulations are widely used to implement the interfaces between analog and digital signals in microelectronic systems. This approach is relatively insensitive to imperfections in circuit components and offers numerous advantages for the realization of high resolution ADCs in the low voltage environment as mentioned in chapter 1. Therefore, ΣΔ modulation is increasingly demanded by advanced CMOS technology and portable systems [33] [36].

We discuss in this chapter the fundamental issues of ΣΔ modulators. We begin with the basic concepts used to evaluate modulator performance. Then, the operation principle of a ΣΔ modulator is described. The basic linear models, which include 1^{st} and 2^{nd}-order modulators, are reviewed. Furthermore, high-order ΣΔ modulators architectures are introduced. Finally, tradeoffs among a variety of ΣΔ architectures are explored.

2.2 Sigma-delta modulator performance metrics

For sigma-delta modulator, the key parameters are dynamic range (DR), power dissipation (power consumption), Nyquist rate and oversampling ratio (OSR). In

addition, in the ADC design, we usually specify the peak SNR (signal-to-noise ratio) and the peak SNDR (signal-to-noise distortion ratio).

2.2.1 Dynamic range and peak SNR/SNDR

DR and peak SNR/SNDR are related specifications. DR is the ratio in power between the maximum input signal level that the modulator can handle and the minimum detectable input signal. SNR is the ratio of the input signal power at the output of the modulator to the noise power, including circuit noise and quantization noise but excluding the power of harmonics distortion signal. SNDR is defined as the ratio of the input signal power at the output of the modulator to the sum of the noise and harmonic distortion powers.

Peak SNR, SNDR and DR are reported in Figure 2.1. In this Figure, SNR and SNDR are function of input signal power in dB relative to the full scale of the modulator. For small signal levels, distortion is not important implying that SNDR usually follows the SNR curve. As the signal level increases, distortion degrades SNDR performance more than the SNR one.

The resolution of the modulator expressed in bits is a closely related specification to dynamic range. The resolution in bits (N) is defined in Equation 2.1, where DR is the dynamic range of the modulator expressed in dB. The correspondence is such that each bit of resolution is equivalent to 6 dB of dynamic range [33].

$$N = \frac{DR - 1.76}{6} \tag{2.1}$$

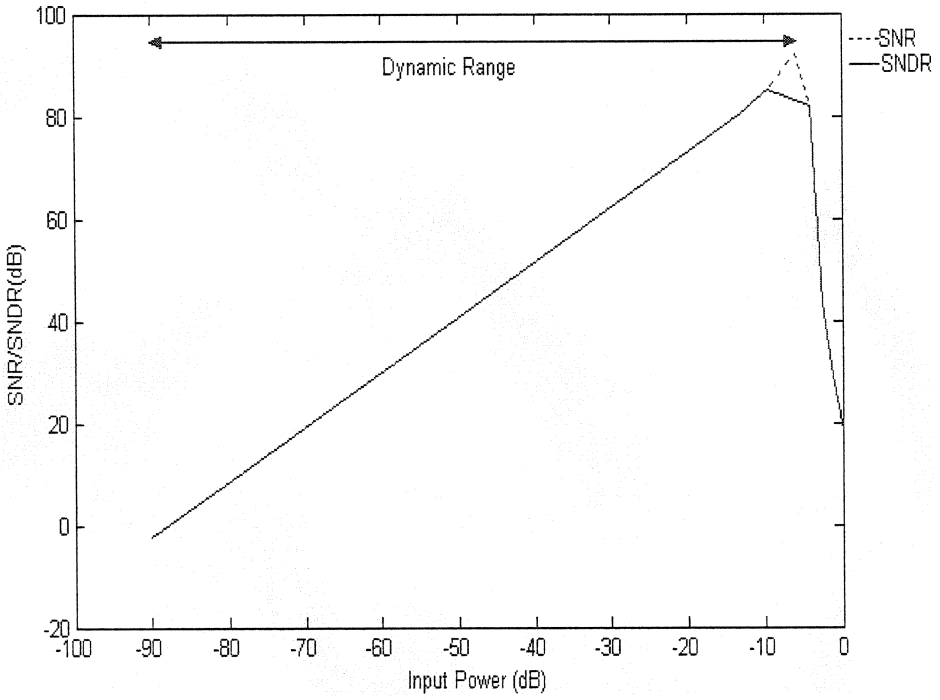


Figure 2.1 SNR and SNDR curves

2.2.2 Oversampling ratio and Nyuist rate

Assume that f_0 is the signal bandwidth and the sampling clock rate is f_s. Oversampling occurs when the signals of interest are band limited to f_0 yet the sample clock rate is at f_s, where $f_s > 2f_0$. We define the oversampling ratio, OSR, as

$$OSR \equiv \frac{f_s}{2f_0} \tag{2.2}$$

Nyquist rate equals twice of input signal bandwidth. Nyquist rate is a measure of the speed of a ΣΔ modulator. The Nyquist sampling theorem states that to avoid aliasing, an

input signal must be sampled at a rate that is twice its bandwidth. The rate (f_N), twice its signal bandwidth ($2f_0$) is defined as Nyquist rate.

2.2.3 Power consumption

According to most applications, the ADC design must meet the main performances such as SNR, Nyquist rate and linearity while minimizing power consumption. Power consumption is discussed in further detail in Chapter 3.

2.3 Sigma-delta modulators

ΣΔ modulation technique includes oversampling and noise shaping techniques. A/D (analog-to-digital) conversion uses a digital low pass filter to attenuate the noise that has been pushed out of interest band. It is possible to achieve a high dynamic range at relatively modest oversampling ratios.

2.3.1 Principle of sigma-delta modulators

Although ΣΔ modulators usually employ two levels quantization, we assume the modulator contains a multi-level as shown in Figure 2.2. The input to the circuit feeds to the quantizer via an integrator, and the quantized output feeds back to subtract from the input signal. This feedback forces the average value of the quantized signal to track the average input. Any persistent difference between them accumulates in the integrator and eventually corrects itself.

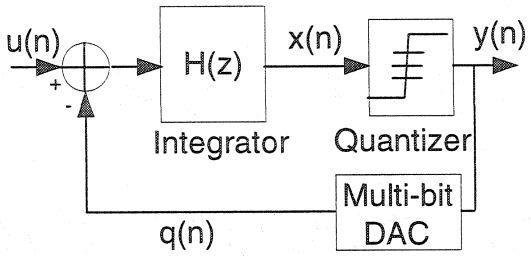


Figure 2.2 A simplified block diagram of a ΣΔ modulator with multi-bit quantizer

However, most present oversampling modulators make use of one-bit inherently linear quantizer because its two output levels as shown in Figure 2.3. We can derive a signal transfer function, $S_{TF}(z)$, and a noise transfer function, $N_{TF}(z)$

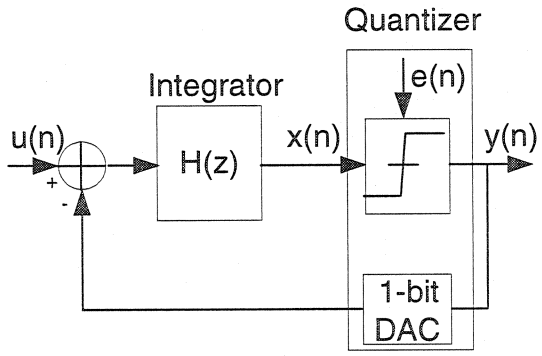


Figure 2.3 Linear model in time-domain of a ΣΔ modulator

$$S_{TF}(z) \equiv \frac{Y(z)}{U(z)} = \frac{H(z)}{1+H(z)} \tag{2.3}$$

$$N_{TF}(z) \equiv \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} \tag{2.4}$$

From Equation (2.4), the zeros of the noise transfer function, N_{TF}(z), will be equal to the poles of H(z). In other words, when H(z) goes to infinity, N_{TF}(z) will go to zero. The transfer function of ΣΔ modulator in the frequency domain can be expressed by [20]

$$Y(z) = S_{TF}(z)U(z) + N_{TF}(z)E(z) \tag{2.5}$$

The diagram of ΣΔ modulator in frequency domain is shown in Figure 2.4. Noise shaping the quantization noise is a useful manner, we choose H(z) which magnitude is large from 0 to f_0 (i.e. over the signal frequency bandwidth). With such a choice, the signal transfer function, S_{TF}(z), will approximate unity over the signal frequency bandwidth. Furthermore, the noise transfer function, N_{TF}(Z), will approximate zero over the same band. Thus, the quantization noise is reduced over the signal bandwidth while the signal itself is unaffected. The high frequency noise is not reduced by the feedback. However, additional low-pass digital filtering will be performed in order to remove entire out of band quantization noise. This main function of ΣΔ modulator can be shown in Figure 2.5.

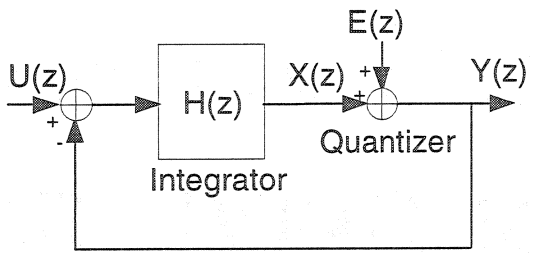
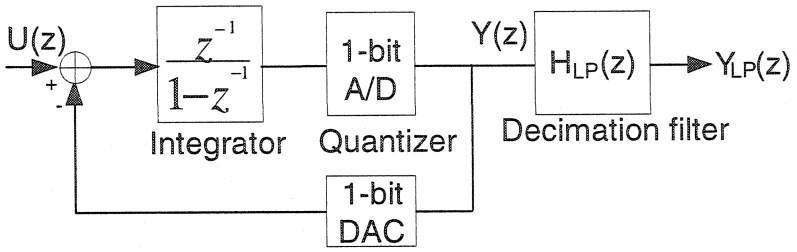
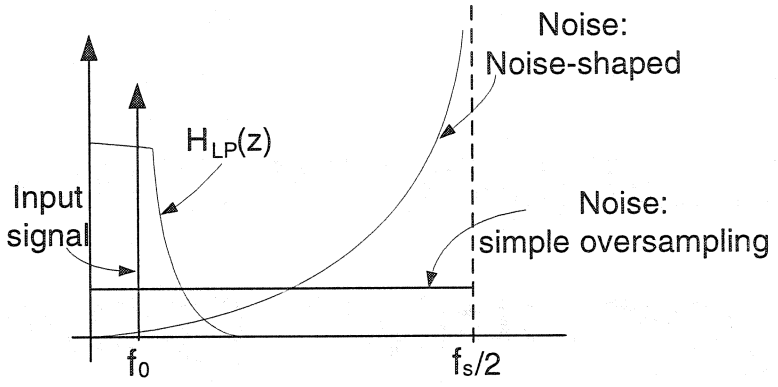


Figure 2.4 Frequency domain of ΣΔ modulation



(a)



(b)

Figure 2.5 Principle of ΣΔ modulator (a) Diagram of ΣΔ program (b) Principle of oversampling & noise shaping

2.3.2 First-order ΣΔ modulator with one-bit DAC feedback

2.3.2.1 First-order ΣΔ modulator

A 1st-order ΣΔ modulator in time domain is shown in Figure 2.6. This basic modulator contains one-bit quantization (i.e. only two output levels). Here, an integrator and a one-bit ADC are in the forward path, and a one-bit digital-to-analog converter (DAC) with a substractor (delta) is in the single feedback loop system. The parameter 'n' is an integer

of time. The one-bit ADC is simply a comparator that converts an analog signal into either a high or a low level signal. The one-bit DAC controlled by comparator output y(n) determine if + $(1/2)V_{REF}$ or $-(1/2)V_{REF}$ is summed with the input signal u(n).

If the one-bit DAC is ideal, the time domain difference equation can be described as follows (The following equation deduction is given in Appendix A)

$$y(n) = u(n-1) + [e(n) - e(n-1)] \tag{2.6}$$

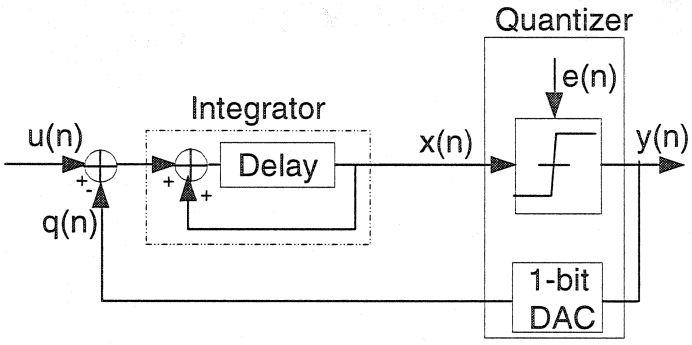


Figure 2.6 A first-order ΣΔ modulation in time domain

Therefore, the output of the modulator consists of a quantized value of the input signal delayed by one unit sample time, plus a difference of the quantization error between the present and previous values. Thus, the real power of ΣΔ modulation is that the quantization noise, *e(n)*, almost cancels itself out (*e(n)-e(n-1)*).

In the frequency domain, the 1st-order modulator can be modeled in z-domain (Figure 2.5 a), with an ideal discrete-time integrator (i.e. have a pole at z =1) represented with the following transfer function [20]

$$H(z)=\frac{z^{-1}}{1-z^{-1}} \tag{2.7}$$

The one-bit ADC is modeled as a simple error source, E(z), and the DAC is considered to be ideal. Therefore, using simple feedback theory, Y(z) becomes

$$Y(z)=\frac{z^{-1}}{1-z^{-1}}\big(U(z)-Y(z)\big)+E(z) \tag{2.8}$$

and solving for Y(z) yields,

$$Y(z)=z^{-1}U(z)+(1-z^{-1})E(z) \tag{2.9}$$

To compare with equation (2.5), the signal transfer function, S_{TF}(z), and the noise transfer function, N_{TF}(z), are respectively given by

$$S_{TF}(z)=z^{-1} \tag{2.10}$$

$$N_{TF}(z)=1-z^{-1} \tag{2.11}$$

We see here that the signal transfer function is simply delay, while the noise transfer function is a discrete-time differentiator. It is clear that the transfer function from U(z) to Y(z) follows that of a low-pass filter (z^{-1}), and the noise transfer function follows that of a high-pass filter ($1-z^{-1}$). Plotted together in Figure 2.7, it can be seen that in the region where the signal is of interest band, the noise power has a small value while the signal

has a high gain, and region that at high frequencies, beyond the bandwidth of the signal, the noise power increases. The modulator has essentially pushed the noise power out of the signal bandwidth. This high-pass characteristic named noise shaping is a powerful concept used within oversampling ADCs. Then, additional decimation filter (low pass filter) followed modulator, can remove the quantization noise that has been pushed out of signal bandwidth, which permits the signal to be downsampled and yields the final high-resolution output.

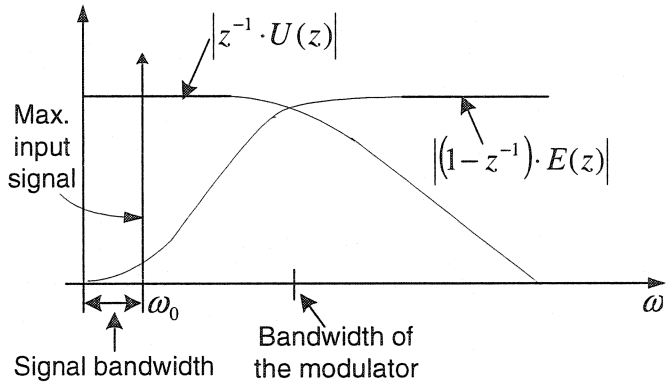


Figure 2.7 Frequency response of the first-order ΣΔ modulator

As the analysis presented in the Appendix A indicates, the maximum SNR of 1st-order ΣΔ modulator can be estimated as

$$SNR_{\max} = 10\log\left(\frac{P_s}{P_e}\right)$$

$$= 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log\left(\frac{3}{\pi^2}(OSR)^2\right)$$

$$= 6.02N + 1.76 - 5.17 + 30\log(OSR) \qquad (2.12)$$

Equation (2.12) shows that doubling the OSR gives an SNR improvement of 9dB or, equivalently, a gain of 1.5 bits/octave for a first-order modulator, e.g., 1st-order modulator with one-bit quantizer can bring maximum SNR of 62 dB with giving OSR 100.

At the circuit level, it is possible to realize a first-order modulator using switched-capacitor technique. An example of a first-order modulator with one-bit quantizer used in feedback loop is shown in Figure 2.8.

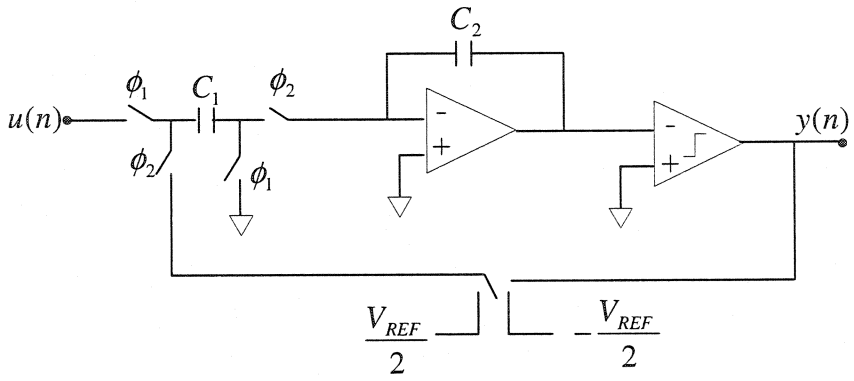


Figure 2.8 Implementation of a 1st-order ΣΔ modulator using a switched-capacitor integrator

The one-bit ADC is a simple comparator, and one-bit DAC is simple two level voltage-controlled switches that select either $(1/2)V_{REF}$ and $(-1/2)V_{REF}$ to be summed with the input. Remember that the function of switched-capacitor is to accumulate differences between the input signal and the output of the DAC. Such an approach using switched-capacitor technique will be adopted in the present design work.

2.3.2.2 The advantage of one-bit DAC

The advantage of a one-bit D/A is that it is inherently linear. This linearity is a result of a one-bit D/A converter having only two output values, since two points define a straight line. No trimming or calibration is required. This inherently linearity is one of the major motivations for making use of oversampling and noise shaping techniques with one-bit converters. From calculation of equation (2.12) with OSR of 100, the 1st-order modulator output from a one-bit converter can be filtered to obtain the equivalent of a 10-bit (62 dB) converter as mentioned above section. In fact, many audio converters presently use one-bit converters for realizing high multi-bit linear converters with noise shaping. Recently, 20-bit linearity has been reported without the need for any trimming [24]

2.3.3 Second-order ΣΔ modulator with one-bit DAC feedback

A second-order ΣΔ modulator is shown in Figure 2.9. As the analysis presented in the Appendix A indicates, assuming appropriate coefficients are chosen in this second-order ΣΔ modulator, its ideal transfer function in frequency domain can be expressed by

$$Y(z) = \left(z^{-1}\right)^2 U(z) + \left(1 - z^{-1}\right)^2 E(z) \tag{2.13}$$

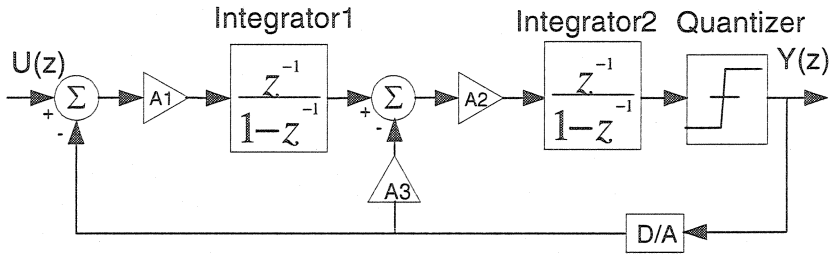


Figure 2.9 Block Diagram of a second-order ΣΔ modulator

The noise transfer function of second-order noise shaping, $N_{TF}(z)$, is a second-order high-pass function. For this second-order ΣΔ modulator, the signal and noise transfer functions are respectively given by

$$S_{TF}(z) = z^{-2} \tag{2.14}$$

$$N_{TF}(z) = (1 - z^{-1})^2 \tag{2.15}$$

As shown for the case of the first-order modulator (Appendix A), the maximum SNR performance of a second-order ΣΔ modulator is given by

$$SNR_{\max} = 10\log\left(\frac{P_s}{P_e}\right)$$

$$= 10log\left(\frac{3}{2}2^{2N}\right) + 10\log\left(\frac{5}{\pi^4}(OSR)^5\right)$$

$$= 6.02N + 1.76 - 12.9 + 50\log(OSR) \tag{2.16}$$

We find here that doubling the OSR improves the SNR by 15 dB, or equivalently, a gain of 2.5 bits/octave for a second-order modulator. This result should be compared to the 1.5 bits/octave when oversampling with first-order noise shaping.

Now, the maximum SNR equations of 1st-order and 2nd-order modulators have been presented, it would be useful to have the conclusions of $SNR_{\max}$ performance:

- For a given signal bandwidth (BW), the SNR increases as the sampling rate f_s increases or OSR increases.

- The SNR also increases with the increase of the modulator's order (complexity increase).

The conclusions of SNR_{max} performances of different order ΣΔ modulators are shown in Figure 2.10. It is necessary to design higher order noise shaping to improve SNR of ΣΔ modulators.

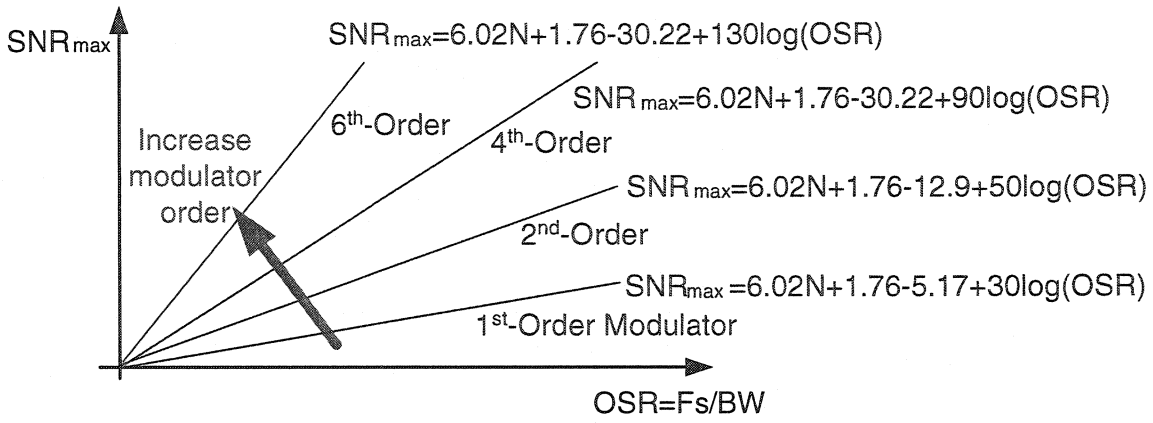


Figure 2.10 The SNR performance of different order ΣΔ modulators

2.3.4 Higher-order sigma-delta modulators

The order of a ΣΔ modulator denoted by N, is the number of integrators in the forward path. The architectures of implementing high-order ΣΔ modulators can be mainly classified: 1) single-loop which uses one ADC and one DAC along with a series of integrators (Figure 2.11), 2) Multi-stage noise shaping (MASH) consists of a cascade of several ΣΔ modulators (Figure 2.12). In general, it can be shown that an N^{th}-order noise-shaping modulator improves the SNR by 6N+3 dB/octave, (or N+ 0.5 bits/octave) [16].

2.3.4.1 High-order single-loop sigma-delta modulators

The second-order single loop ΣΔ modulator shown in Figure 2.9 is widely used because it is easy to implement, insensitive to component mismatch [6] and stable. If a large SNR is desired, a high OSR will be required. According to the second-order noise shaping performance, table 2.1 shows the required OSR in 10k Hz signal bandwidth.

Table 2.1 OSR vs. SNR of a 2^{nd}-order ΣΔ modulator

OSR	Sampling rate	SNR
56	1.12 MHz	82 dB
97	1.94 MHz	94 dB
169	3.38 MHz	106 dB
1000	20 MHz	152 dB

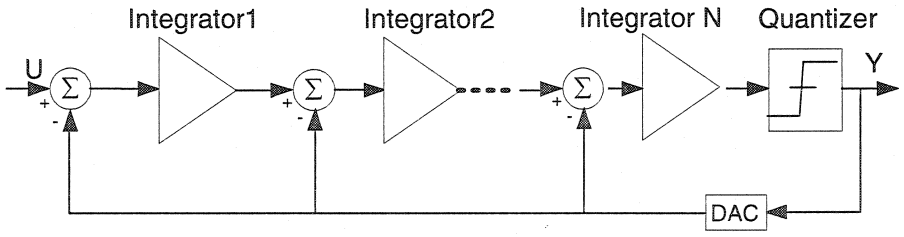


Figure 2.11 ΣΔ modulator block diagram

As a result, a single loop second-order modulator is impractical for high-speed applications since high sampling rate may be limited by slew rate and settling time of OTA [16]. To avoid this limit, higher order modulators are needed to meet the high SNR requirement if the OSR increasing is bounded.

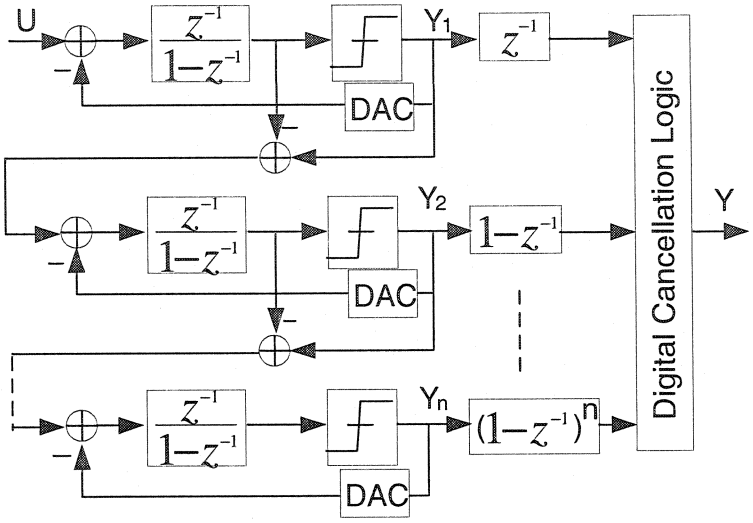


Figure 2.12 Multi-stage Nth-order MASH structure noise shaping modulator

Figure 2.11 shows an N^{th}-order single modulator, which consists of four parts: A series of integrators, each integrator input is the difference between the previous integrator output and the DAC output; an AD conversion with DAC feedback (Quantizer); and the subtractors. The subtractor is used to evaluate the difference between the input signal and the feedback value. This difference value is fed into the following integrator. The output of the last integrator is fed into the ADC. Finally, the output of the ADC is fed back to the DAC and the resulting analog signal is subtracted from input signal. However, to increase beyond a second-order loop, stability of these high-order single loop ΣΔ modulators may be an issue. In this case, special attention must be paid to build such circuits. One approach to achieving a stable 4^{th}-order single loop design was reported in [12]. The designers must scale the integrator gains and place clippers on the outputs of each of the integrators to assure that the modulator remains stable.

2.3.4.2 High-order multi-stage noise shaping architecture

Another approach for realizing high-order modulator is to use a cascade-type structure where the overall modulator is constructed using low-order ones. The advantage of this approach is that since the lower-order modulators are more stable, the overall system should remain stable. Such an arrangement has been called multi-stage noise shaping (MASH) [30].

MASH circuit may contain multi-stage (or cascade) 1st-order or 2nd-order ΣΔ modulators. Figure 2.13 illustrates a 2-2 cascaded architecture of a ΣΔ modulator. Assuming $E_1(z)$ and $E_2(z)$ are quantization errors from first and second modulator loop respectively. The outputs, $Y_1(z)$ and $Y_2(z)$, are fed into a digital cancellation circuitry (DCC). This DCC based on the prediction of the analog interstage gain g, aims to cancel the quantization error $E_1(z)$ from first stage, only left the quantization error $E_2(z)$ from the second stage, which will be almost shaped out the interesting band. The transfer functions from the input and through the quantization noises sources to the output of DCC are derived in the equations below.

$$Y_1(z) = z^{-2}U_{in}(z) + \left(1 - z^{-1}\right)^2 E_1(z) \tag{2.17}$$

$$Y_2(z) = z^{-2}\, g\, E_1(z) + \left(1 - z^{-1}\right)^2 E_2(z) \tag{2.18}$$

$$Y(z) = H_{D1}(z)\, Y_1(z) + H_{D2}(z)\, Y_2(z)$$

$$= z^{-4}U_{in}(z) + z^{-2}\left(1 - z^{-1}\right)^2\left(1 - \frac{g}{g'}\right)E_1(z) - \frac{\left(1 - z^{-1}\right)^4}{g'}E_2(z) \tag{2.19}$$

where $H_{D1}(z) = z^{-2}$, $H_{D2}(z) = (1 - z^{-1})^2 / g'$. H_{D1}(z) and H_{D2}(z) are the transfer functions of the DCC, which will be used to cancel out the quantization noise E_1(z) from the first modulator loop. It can be observed in equation 2.19, the second term E_1(z) will be effectively cancelled out if the analog gain g matches the gain g' of the digital circuitry. Therefore, such 2-2 cascade architecture achieves 4th-order performance by using 2nd-order modulators and still having 2nd-order modulator's stability. However, any mismatch between g and g' will result in an incomplete cancellation of the quantization noise E_1(z) to leak out. In other words, such mismatch between analog and digital circuit causes a leakage of quantization noise from first stage to the output, and damage the overall 4th-order modulator SNR performance. This mismatch issue in MASH (2-2 cascaded) architecture design is the subject of chapter 5.

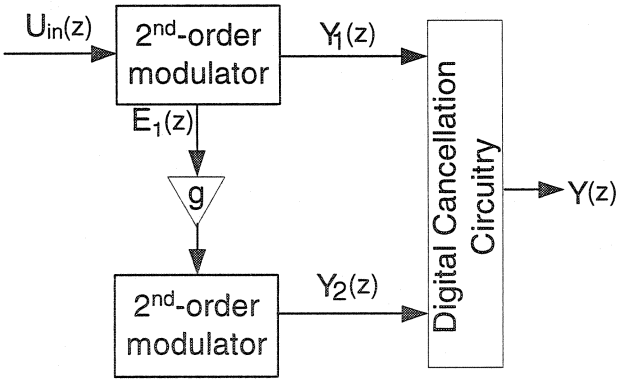


Figure 2.13 Example of a 4th-order 2-2 cascade (MASH) architecture

Cascaded N stages of low-order ΣΔ modulators require digital cancellation circuitry. Suppose each analog stage matches to digital cancellation circuit, low-order noises from 1st to (N-1)th stage's quantizers can be absolutely cancelled out. Thus, MASH

architecture has the advantage that realizing high-order noise filtering can be achieved using low-order modulators. The low-order modulators are much less susceptible to instability as compared to a single loop high-order modulator.

2.3.5 Architecture tradeoff

Tradeoff between the modulator order and its OSR is an important specification to meet a given SNR requirement. As described above, single bit quantizer and two level DAC of single loop structure is inherently linear. The advantage of single loop architecture has been favored for high OSR applications and its insensitivity to mismatch in circuit components. High-order modulators (N>2) are conditionally stable [40]. In fact, to stabilize a high-order single loop architecture, the complicated transfer functions in the forward path of modulator is required, and it causes the modulator SNR to be decreased [16].

MASH architecture that cascading several low-order ΣΔ modulators allows building high-order structures. Two cascaded stages only permit efficient matching of elements and adequate SNR. However, as the order of modulator is increased, the constraints on mismatches become more severe. Mismatch between the analog and digital circuitry in MASH structure causes the leakage of quantization errors from low-order stage into output. This leakage can damage the SNR. Then a significant attention must be paid to avoid such mismatch.

Both single loop and MASH architecture may employ either single bit or multi-bit quantizer. Constructing the multi-bit A/D and D/A converters significantly increases the SNR performance. However, this architecture usually loses inherent linearity, resulting in distortion problem. Some forms of calibration can be used to alleviate the problem [31]. These calibrations are more severe than calibrating mismatches between the analog and digital interstage gain of cascade modulators.

Finally considering the advantages of low-order modulator and the one-bit inherently linear quantizer, as well as 2^{nd}-order $\Sigma\Delta$ modulator is widely used with stability and insensitivity to component mismatch [6]. We privilege the 2^{nd}-order modulator to implement the low power low voltage high linearity $\Sigma\Delta$ modulator, which is the subject of chapter 4.

CHAPTER 3

LOW VOLTAGE ANALOG CIRCUIT DESIGN TECHNIQUES

3.1 Introduction

Microelectronics portable applications have led to the need of low power low voltage ADCs. In digital circuits, lowering the supply voltage may decrease the power consumption. But, in analog circuits, significant impacts may occur. First, the power dissipation may increase. Second, the signal dynamic range will be reduced. Third, the gate-source voltage V_{GS} of CMOS switch may be reduced below the threshold voltage V_{TH}, which results in failing to turn on this switch. Thus, the tradeoff between low power low voltage and the circuit performances should be considered carefully.

This chapter is organized as follows. Firstly, power consumption of analog circuit, in function of supply voltage and dynamic range (DR) is analyzed. Then dynamic analog circuit and low voltage operation issues (switch driving and signal swing range limitations) are examined. Thirdly, the main previous works, which include voltage doubler and switched-opamp technique, will be presented. Finally, the literature of low power low voltage $\Sigma\Delta$ modulators will be reviewed.

3.2 Fundamental power limits

Minimizing power dissipation in analog ΣΔ modulation circuits requires considering several factors that affect the power budget and limitations. In fact, the power dissipation of a switched-capacitor integrator (SCI) is proportional to its capacitive loading. Therefore, to minimize the power dissipation of such integrator, small capacitor size should be used. However, this design approach is limited primarily by the *kT/C* thermal noise in the first integrator, the main power limitation in a ΣΔ modulator is the thermal noise, which can be decreased only by the cost of capacitor area and power consumption. In other words, if the thermal noise is significantly smaller than the quantization noise, the capacitor size is over-dimensioned and power is being wasted. For low power design, the modulator is generally designed by controlling the thermal noise to be equal or just slightly larger than the quantization noise [33] [36]. In a fully differential SCI (Figure 3.1) design of ΣΔ modulators, for low power consideration, we assume noise floor is dominated by the thermal noise in the baseband, and the maximum signal voltage swing is V_{sw} ($V_{sw} \leq V_{DD}$). Then, signal power, thermal noise and DR can be expressed by the following equations [35].

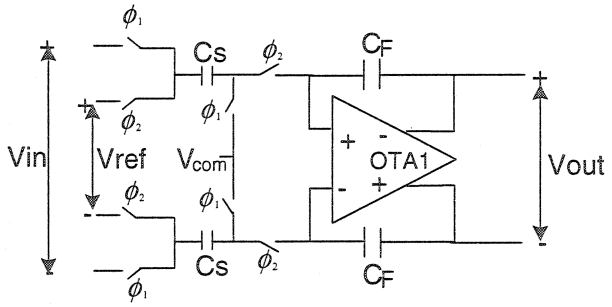


Figure 3.1 Fully differential switched-capacitor integrator

$$P_S = \frac{V_{sw}^2}{2} \tag{3.1}$$

$$P_{N-thermal} = \frac{4kT}{(OSR)C_S} \tag{3.2}$$

$$DR = \frac{P_{in}}{P_{noise}} = \frac{P_S}{P_{N\_thermal}} = \frac{V_{sw}^2 (OSR)C_S}{8kT} \tag{3.3}$$

Where $V_{sw} \leq V_{DD}$, k = 1.38×10^{-23}, T = 300^{o} and OSR represents oversampling ratio. The power consumption can be estimated approximately by the following expression [33][29].

$$P \propto kT(DR)^2 f_N \frac{V_{ov}}{V_{DD}} \tag{3.4}$$

Where f_N is Nyquist sampling rate, DR is dynamic range and V_{ov} is the V_{GS} -V_T of the input stage transistors. Equation (3.4) shows the tradeoff between power, dynamic range and bandwidth. It indicates that increasing the DR or f_N (equivalent to the signal bandwidth) requires more power, but the power dissipation is inversely proportional to V_{DD} with the condition to keep the DR to be constant.

It should be mentioned that the V_{DD} plays an ambiguous role. Lowering V_{DD} reflects to lower the power dissipation because the product of voltage and current is smaller. Therefore, it looks like the power is proportional to the V_{DD}. This is only true as long as the input signal power can remain constant which is impossible, since reducing V_{DD} will

reduce the input signal swing range of the system, and thus result in reducing the input signal amplitude and its power.

Although, low V_{DD} causes power consumption increasing, there are methods and techniques that can be beneficial to low power consumption. First, biasing transistors of opamp in weak inversion region has been exploited to reach low power in [17], but the disadvantage is that the small currents imply low bandwidth [2]. Weak inversion operation does not allow us to obtain the required performances in our case. Second, using half-delay integrator combination with switched-opamp technique [33] [34] significantly allows us to save power, which will be discussed in section 3.5. Regarding the low voltage operation switch conduction and signal swing range are among the issues that must be addressed and will be elaborated in following sections.

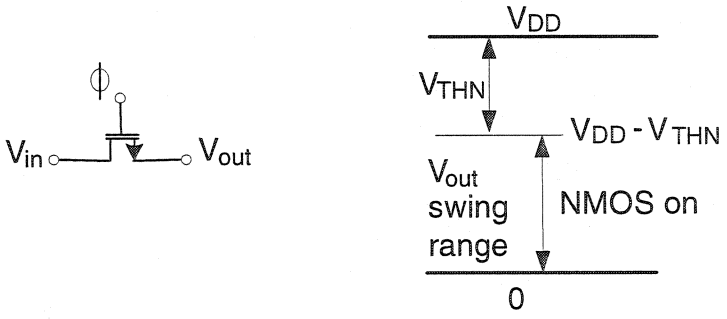
3.3 Dynamic analog circuit and low voltage limits

Switched-capacitor technique has been an efficient way to implement low power $\Sigma\Delta$ modulator in CMOS technology [21] [1]. Switched-capacitor circuit includes capacitors, switches and opamps. Reducing supply voltage does not affect capacitors too much, but it will cause switch conduction and signal swing range reduction problems.

3.3.1 MOSFET switch

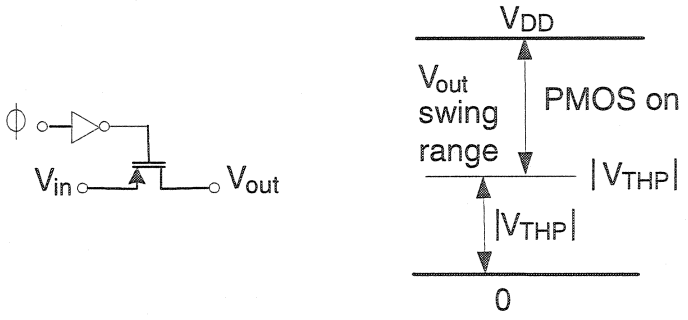
A fundamental component of any dynamic circuit is the switch. The high OFF-to-ON resistance ratio of MOSFET transistors makes them suitable for use in switching

applications. A switch can be implemented using a single NMOS or PMOS transistor. A NMOS transistor based switch works under power supplies of 0 to V_{DD} and its threshold voltage is V_{THN} in Figure 3.2. The switch can be turned off by putting 0 V on its gate, and turned on by turning its gate voltage to V_{DD}. The NMOS transistor conducts an input signal located between 0 up to V_{DD}-V_{THN}, (Figure 3.2b). Figure 3.3a shows PMOS transistor can be turned off and on by putting V_{DD} and 0 V respectively, the PMOS transistor conducts for an input signal varying from $|V_{THP}|$ up to V_{DD} ($V_{DD}>|V_{THP}|$, the threshold of PMOS is V_{THP}), which is shown in Figure 3.3 (b).



(a) (b)

Figure 3.2 (a) NMOS switch, (b) Signal swing limitation of NMOS switch



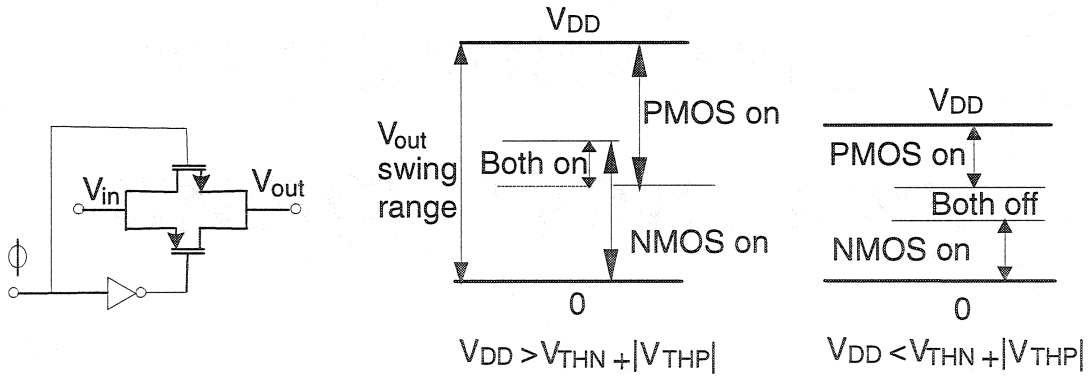
(a) (b)

Figure 3.3 (a) PMOS switch, (b) Signal swing limitation of PMOS switch

CMOS switch based on a transmission gate includes both NMOS and PMOS transistors, mounted in parallel as shown in Figure 3.4 (a). NMOS transistor conducts from 0 up to V_{DD}-V_{THN} and the PMOS transistor conducts from $|V_{THP}|$ to V_{DD}. Combining NMOS and PMOS allows obtaining full rail-to-rail signal transmission. CMOS switch is one of the alternatives as long as the condition illustrated in equation (3.5) is satisfied, which is shown in Figure 3.4 (b).

$$V_{DD} > V_{THN} + |V_{THP}| \tag{3.5}$$

However, reducing the supply voltage to $V_{DD} < V_{THN} + |V_{THP}|$ implies a dead zone which leads to both of NMOS and PMOS turned off, as shown in Figure 3.4 (c). In this case, the signal is no longer obtained at the output of the CMOS switch.



(a) (b) (c)

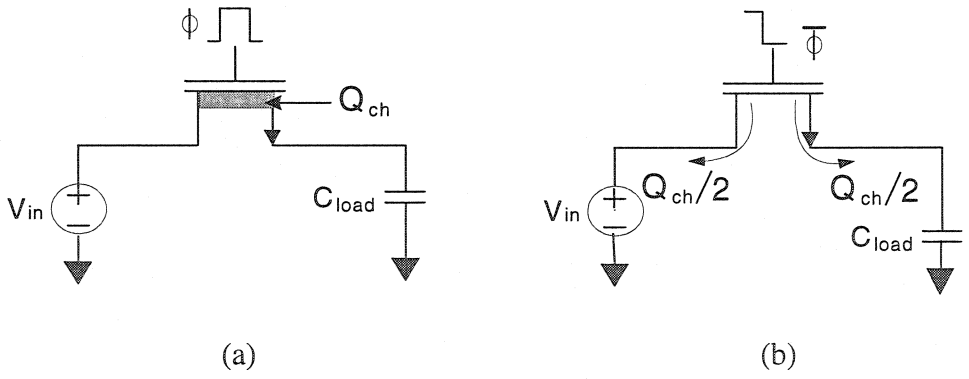
Figure 3.4 (a) CMOS switch (b) Full signal swing range of CMOS switch, (c) The signal swing limitation of CMOS switch at low voltage operation

3.3.2 Charge injection errors

Charge injection, also commonly called clock feedthrough. This error is due to unwanted charges being injected into the circuit when the switch transistor turns off. Charge injection, one of the nonideal effects of MOS switches may ultimately limit the use of MOS switches in some applications.

This phenomenon can be understood with the help of Figure 3.5, when NMOS switch is on and its drain source voltage V_{DS} is small, V_{TH} is the NMOS transistor threshold voltage, then the charge under the gate oxide resulting from the inverted channel is approximated as:

$$Q_{chan} = C_{ox}WL(V_{GS} - V_{TH}) \tag{3.6}$$



(a) (b)

Figure 3.5 Charge injection in a n-channel transistor: (a) NMOS is on, (b) NMOS is off

When the MOSFET turns off, this charge is injected into the capacitor C_{load} and into the voltage source V_{in}. Assume that V_{in} is a low-impedance source-driven node. The injected charge will have no effect on this node. However, the charge injected into C_{load} result in a

change in voltage across it. It has been shown, that if the clock signal turns off fast, the channel charge distributes fairly equally between the adjacent nodes [3]. Thus, half of the channel charge is distributed into C_{load}. As the accumulated charge in n and p-channel are electrons and holes respectively, the charge injection in n and p-channel switch will result in negative and positive spikes correspondingly [3]. Their amplitude, for instance in NMOS switch, can be calculated as:

$$\Delta V_{charge\_N} = -\frac{C_{ox} \cdot W \cdot L \cdot (V_{GS} - V_{THN})}{2C_{load}} \tag{3.7}$$

Assume the clock swing is between V_{DD} and V_{SS}, input signal is v_{in}, it can be written as:

$$\Delta V_{charge\_N} = -\frac{C_{ox} \cdot W \cdot L \cdot (V_{DD} - v_{in} - V_{THN})}{2C_{load}} \tag{3.8}$$

The threshold voltage $V_{TH} = V_{TH0} + \gamma[\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}]$ and $V_{SB} = v_{in} - V_{SS}$ can also be substituted into (3.8) to form:

$$\Delta V_{charge\_N} = -\frac{C_{ox} \cdot W \cdot L \cdot (V_{DD} - v_{in} - [V_{THN0} + \gamma(\sqrt{|2\phi_F| + v_{in} - V_{SS}} - \sqrt{|2\phi_F|})])}{2C_{load}} \tag{3.9}$$

where V_{THN0} is NMOS switch threshold voltage with zero V_{SB} (i.e. source-to-substrate voltage), γ denotes the body effect constant and Φ_F represents the electrostatic potential of the substrate. The Eq. (3.9) illustrates that the problem associated with charge injection. The charge injection voltage across C_{load} is nonlinear with respect to v_{in} due to the threshold voltage. Thus, it can be said that charge injection is signal dependent,

harmonic distortion results [11]. In sampled-date systems, charge injection results in nonlinearity errors.

The simplest way to reduce charge injection errors is to use larger capacitors. Unfortunately, this large capacitance would require a large amount of silicon area. Also would spend extra power dissipation and slow down the circuit [20].

Another technique for minimizing charge injection error is to use CMOS switch [3]. This approach requires precise control on the complementary clocks (the clocks must be switched at exactly the same time) and assumes that the input signal v_{in} is small, since the symmetry of CMOS switch of turning on and off waveform is dependent on the input signal. The charge injections in n and p-channels will basically cancel each other. However, generally input signal swing range is not small. In our design, signal will vary from rail-to-rail, in this case the dummy switch technique [3] [2] [11] and fully differential circuit topologies [3] [25] can be used.

Dummy switch technique is illustrated in Figure 3.6. Here, a half size transistor with its drain and source shorted is placed in series with the desired switch M_1. When M_1 turns off, the dummy switch absorbs its channel charge in output direction. Thus, the charge injection error can be cancelled [11].

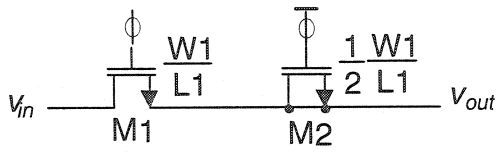


Figure 3.6 Use of a half size dummy switch to cancel charge injection

Fully differential circuit topologies are used to minimize charge injection effects, as seen in Figure 3.7. Since the nonideal charge injection effects appear as a common-mode signal to the amplifier, and will be reduced by the common-mode rejection ratio (CMRR) of the amplifier [25].

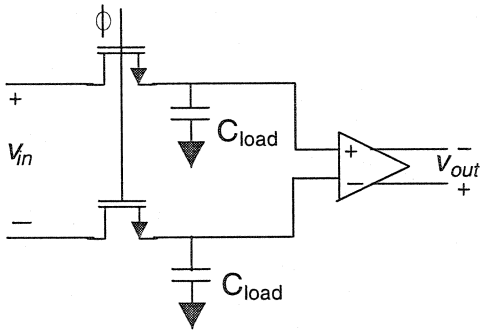


Figure 3.7 Use of a fully differential circuit to minimize charge injection

3.3.3 Voltage requirements of analog circuit

All the transistors of analog amplification circuits that operate in DC voltage, must be "on" to carry quiescent current. The gate-source voltage of each transistor requires larger voltage than its threshold one (V_{TH}) in order to ensure the transistor being active. Furthermore, the transistors usually must operate in deep saturation region for amplification. These requirements are presented in the following equations.

$$V_{eff} = V_{GS} - V_{TH} \geq \Delta V \tag{3.10}$$

$$V_{DS} \geq V_{eff} + \Delta V \tag{3.11}$$

Where V_{eff} is proportional to $V_{GS} - V_{TH}$, which is often called the effective gate-source voltage, and ΔV denotes a voltage safety margin of deep saturation to accommodate the possible deviation corresponding to the environment variation. The transistor that operates in deep saturation region can bear a variation on both gate-source and drain-source voltages, thus ensure stable and robust operation of the transistor. The value of ΔV depends on the CMOS technology and the supply voltage.

In order to maximize the signal swing range at the low voltage supply, it is necessary to obtain wide input voltage range. Traditional rail-to-rail common mode input range is obtained by parallelizing a N-type input pair with a P-type input pair. The complementary of the two pairs makes the rail-to-rail operation possible.

Figure 3.8 illustrates voltage requirements of the design of the input stage. Input common mode range (ICMR) of n and p-channel pairs is restricted as defined in the following equations.

$$V_{DD} \geq V_{CMR\_n} \geq V_{SS} + V_{gsn} + V_{dsn} \tag{3.12}$$

$$V_{SS} \leq V_{CMR\_p} \leq V_{DD} - V_{gsp} - V_{dsp} \tag{3.13}$$

To obtain a full rail-to-rail input voltage range, we combine both of complementary stages and at least one of them to stay in "on" state. This requires

$$V_{CMR\_p-\max} \geq V_{CMR\_n-\min} \tag{3.14}$$

Substitute equations (3.12) and equation (3.13) into (3.14), we have:

$$V_{DD} - V_{SS} \geq V_{gsp} + V_{gsn} + V_{dsp} + V_{dsn} \tag{3.15}$$

Equation (3.15) illustrates the lowest limit of the voltage supply for n and p-channel parallel pair structure to realize rail-to-rail signal swing range. However, if the system design requires very low voltage supply ($V_{DD}<V_{gsp}+V_{gsn}+V_{dsp}+V_{dsn}$), one dead zone that both pairs are turned off happens when the supply voltage V_{DD} is decreased below than $V_{gsp}+V_{gsn}+V_{dsp}+V_{dsn}$. Thus, the traditional rail-to-rail ICMR structure fails with very low voltage supply. Therefore, we propose to use an on-chip voltage multiplier providing local boosted supply voltage and clocks to the input stage and "critical" switches respectively.

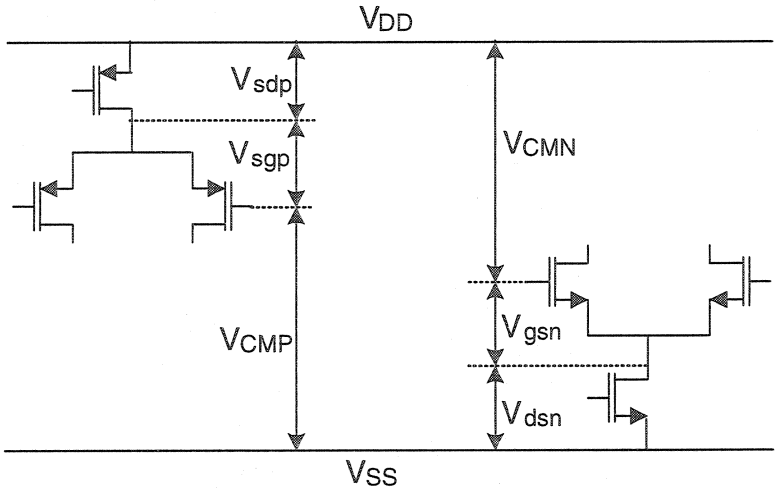


Figure 3.8 Common mode voltage ranges of n- and p-channel pair-transistors

3.4 Low voltage circuit techniques

3.4.1 Voltage multiplier

The voltage doubler appears as a very important block in low voltage applications where the supply voltage is reduced to very low level. It can be used in mixed-mode circuits to supply the analog part or the most critical blocks. As stated above, an on-chip voltage doubler is integrated to provide the boosted voltage to the opamp input stage. It can be seen in Figure 3.9.

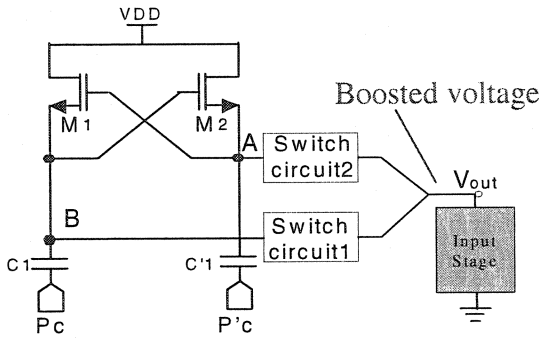


Figure 3.9 The voltage doubler circuit

A circuit, viable in a CMOS technology as a clock booster, has been proposed in [15]. This circuit has the particularity of cross-connecting NMOS transistors shown in Figure 3.9. Cross-coupled transistors M_1 and M_2 combining with capacitor C_1 and C'_1 generate a bootstrapped complementary clock signal at the nodes *A* and *B*. In order to obtain a doubled dc voltage from the output, we still need to build "switch circuit 1" for switching on if B node is high, and "switch circuit 2" for switching on if A node is high. Then, higher voltage of nodes *A* and *B* can be chosen and transferred to the output node at any

instant, thus a boosted DC voltage is obtained at output V_{out}. The principle presented here is not restricted to voltage doublers but can also be used for triplers and other multipliers. Two doublers can also be cascaded to reach four times the input voltage.

3.4.2 Switched-capacitor integrators and switched-opamp technique

3.4.2.1 Switched-capacitor integrators

A conventional insensitive SCI is illustrated in Figure 3.10. Notice that the output of the conventional SCI is available for processing by the following stage at any time instance. As a result, conventional full-delay SCI has its output collected by the following stage at integrator idle phase (Φ_2), the opamp is basically idle during Φ_2 after it performs the integration phase (Φ_1). On the other hand, conventional half delay integrator has its output collected by the following stage during its integration phase (Φ_1).

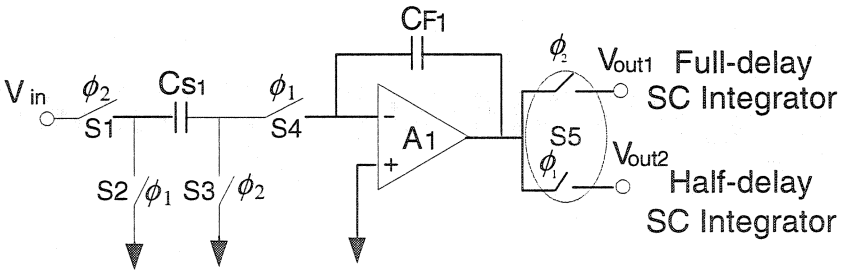


Figure 3.10 Conventional switched-capacitor integrator (SCI)

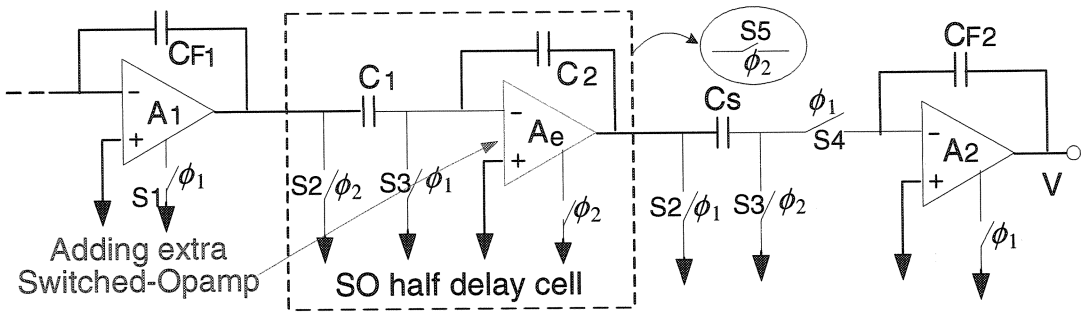
3.4.2.2 Half delay integrator based on Switched-opamp technique

The switched-opamp technique has been shown to be a promising low cost low voltage solution to realize switched-capacitor circuits in CMOS processes [34]. The switched-opamp technique basically eliminates this "critical" switch S_5 (Figure 3.10), which is

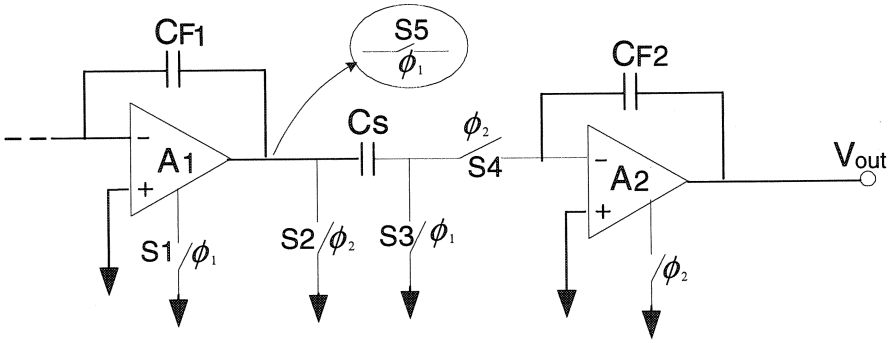
located at output of opamp A_1 by taking advantage of switched-opamp that have to switch on and off during clock cycle time. Therefore, SCI can be realized by using switched-opamp integrator (SOI).

Figure 3.11 (a) illustrates that the "critical" switch S5 has been replaced by a "SO half delay cell" to realize a full-delay SOI, which consists of a half-delay SOI and a "SO half delay cell" with an extra switched-opamp (A_e) inside. As a consequence, it reduces the percentage of overall saved power. This can be easily avoided by using half-delay SOI [33]: "critical" switch S5 is simply removed from half-delay SCI (Figure 3.10) and opamp A_1 is changed by switched-opamp, then, a half-delay SOI is implemented, which is shown in Figure 3.11 (b). Thus, the function of switch S5 is realized by switched-opamp A_1 turned on and off, since switched-opamp A_1 and "critical" switch S_5 turning on and off are controlled by the same clock phase ϕ_1. It can be seen there is no extra switched-opamp in half-delay SOI. To allow half-delay SOI, the switched-opamp A_1 and its behind "critical" switch S5 must be switched on and off by the same clock phase.

More importantly, the power consumption of a half-delay SOI is reduced by 50% compared with a full-delay conventional SCI [34], since half-delay SOI turns off the opamp after integration. Therefore, switched-opamp technique can be used for saving power, and eliminating "critical" switch.



(a)



(b)

Figure 3.11 Switched-opamp technique: (a) Full delay SOI with extra switched-opamp (b) Half delay SOI without extra switched-opamp

However, the switched-opamps are turned off during half phase of every clock cycle, it suffers from speed limitation due to slew rate and settling time, designer must pay attention to this point.

3.4.2.3 Switched methods in switched-opamp technique

Some works have reported switching methods of switched-opamp circuits. First, the switched-opamp is done by turn on and off the bias currents [9] [32]. This is achieved

when the gate-source bias voltage of transistor M_{10} is turned on (Figure 3.12). This Figure shows the topology of a two stages switched-OTA with its biasing circuit.

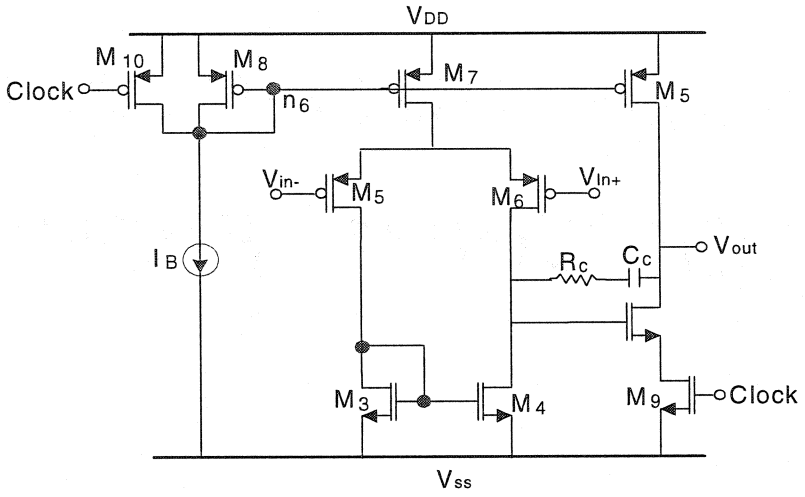


Figure 3.12 Current switching method in the switched–opamp technique [9]

The other switching method is to cut off the current path from the power supply to the circuit with a switch [33], which is illustrated in Figure 3.13. It is favorable method, since it has advantages: The amplifier turn-on time is shorter than in the case of current switching. The buffers drive all switches. Therefore, their turn-on and turn-off speed is under better control than in the current switching case. The opamps are switched on and off by cutting the current paths from the V_{DD} and V_{SS} by switches S1 and S2 respectively at the same instant time.

It is important to note that V_{DD}_c is the internal supply node connected with V_{DD} by a controlled PMOS switch S1 with clock $\bar{\phi}$. Also, Vss_c is the internal supply node connected with Vss by a controlled NMOS switch S2 with clock ϕ.

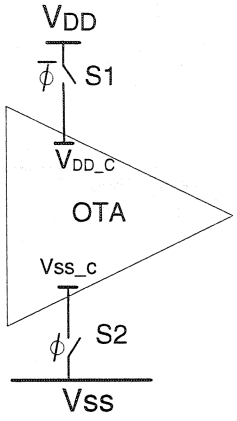


Figure 3.13 The voltage switching method

In theories, all circuits in a switched-opamp implementation can be switched on and off. Not only for the differential integrating opamps but also for the bias circuits, and the common mode feedback amplifiers. Even if input stages to comparators can be switched, it is not recommended to switch their bias circuits, since turning the bias off results in slow switching method.

3.5 Recently reported design techniques

Several previous circuit topologies, operating at low voltage supply have been published recently. These topologies are based on one of these techniques: Low threshold voltage devices, on-chip voltage multiplier to drive the switches or the bootstrapping switch and switched-opamp technique.

In low threshold voltage devices, a special technology is required. The leakage current of circuits made by such technology is increased during the "off" period. Thus, this

technique is usually unacceptable for its increasing process complexity and increased cost reasons.

Employ voltage multiplier to generate higher supply voltages for "critical" circuit, the other switches and rest circuits still work under low voltage supply for saving power [19]. The penalty is to increase the chip area, since voltage multiplier requires large capacitor values. Another similar way is to replace "critical" switches by using local voltage boosting at the gates of the switches (boosting-strapping switch) [10]. This is a graceful solution, but this technique requires complex circuitry to replace simple switches. Thirdly, switched-opamp technique working at half phase of a clock cycle, allows saving power, it is a true low power technique. The switched-opamp technique was first introduced in [9] and further developed in [5] by making the circuit fully differential and separating the input and output common-mode levels. The reported switched-opamp circuits include filters [6] [9], ΣΔ modulators based on switched-opamp technique [32] combined with a DC voltage level shift [34], [37] have been proven to allow proper operation under low V_{DD} conditions, where low threshold voltage devices and voltage boosting techniques are avoided. The designed ΣΔ modulators work under low voltage such as 0.7 V and 0.9 V, and their power consumption are only 80 μW and 40 μW respectively. However, it is obvious that the input voltage range is significantly reduce to 0-0.28 V under 0.9 V [34], and 0-0.21V under 0.7 V operation in the [37].

The ultra low supply voltage fails to turn on the switch transistors even if transmission gates are used. Working under low voltage supply, it is necessary to maximize the input and output range of OTA in order to achieve a sufficient dynamic range, since the signal swing range is reduced as the voltage supply is reduced. So, solving switch driving problem and achieving a sufficient dynamic range are required when voltage supply is becoming lower and lower.

In this master thesis, we propose a low power low voltage ΣΔ modulator, which is based on a novel rail-to-rail class AB OTA with boosted voltage. This OTA is used to increase the signal dynamic range.

CHAPTER 4

LOW VOLTAGE SECOND-ORDER ΣΔ MODULATOR

4.1 Introduction

The work presented in this chapter is to design a novel low power low voltage 2nd-order ΣΔ modulator for bioelectronics implants (Figure 1.2), conducted by our PolySTIM research team, as mentioned in chapter 1. The modulator should at least have ten bits of resolution, equivalent to 60 dB signal-to-noise-ratio (SNR) for a 10 kHz signal bandwidth. For supply voltages from VDD (0.9 V) to ground VSS (0V), the power consumption is desired to be less than 100 μW. Table 4.1 summarizes the main specification of the ΣΔ modulator design.

Table 4.1 Specification of the 2nd-order ΣΔ modulator

Parameters	Target Specification
Voltage supply	VDD = 0.9 V & VSS = 0 V
Signal bandwidth	10 kHz
Sampling frequency	2 MHz
Peak SNR	60 dB
Power consumption	<100 μW

Chapter 4 is organized as follows: First, the principle of low voltage low power ΣΔ modulator and its limitation are briefly described in section 4.2. Next, we present an improved 2nd-order ΣΔ modulator for implantable biomedical application in section 4.3, which includes PSRR, charge injection and switch method effect analysis. Finally, summary is given out.

4.2 Low voltage ΣΔ modulator

The basic block diagram of a 2nd-order ΣΔ modulator is shown in Figure 4.1, which consists of two half delay integrators, one comparator and feedback unit. Switch-capacitor circuit is exploited to implement the integrator due to its high precision and low power consumption. Three different gain units (A_1~A_3) are introduced to adjust the forward loop (A_1 and A_2) and feedback loop (A_3) respectively. This reduces the possibility of saturation of the integrator, thus improves the linearity of the A/D converter. ΣΔ modulator operating at low supply voltage (900 mV) is desired. In chapter 3, some works have been reviewed to implement the low voltage ΣΔ modulator, which is based on an integrator built with switch-capacitor technique.

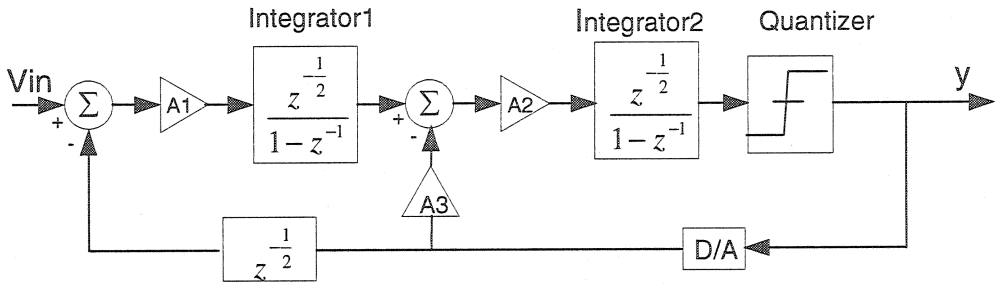


Figure 4.1 Block diagram of 2nd-order ΣΔ modulator with half delay integrators

However, with decreasing the supply voltage, the transconductance of the CMOS switch can be impaired significantly. To allow low voltage operation, two techniques have been presented in chapter 3. Boosted voltage method uses an on-chip voltage doubler to generate high gate-source voltage on the switch to improve its transconductance. The second method is based on a switched-opamp technique, which results in a true, very low voltage operation without using a voltage multiplier or other low threshold (V_{th}) devices [34]. However, as the conventional P-type input stage is adopted in OTA design, these reported sigma-delta converters suffer a narrow input voltage range from ground to V_{inmax}, where

$$V_{in\max} = V_{DD} - V_{dsp} - V_{gsp} \tag{4.1}$$

Providing the modulator is working under 900 mV voltage supplies and threshold voltage of PMOS transistor equals 450 mV, the input range calculated from equation (4.1) is less than 300 mV, which significantly impairs SNR of the modulator. Therefore, an OTA with rail-to-rail input and output ranges under low voltage operation is indispensable to enlarge the dynamic range of the modulator.

4.3 Improved second order ΣΔ modulator

4.3.1 System consideration

Traditional rail-to-rail input range OTA is obtained by parallel connected a N-type input pair with a P-type input pair. The complementary input range of the two pairs makes the rail-to-rail operation possible. Nevertheless, one dead zone that both pairs are turned off

may happen when the supply voltage is decreased to lower than $V_{THP}+V_{THN}$, which is around 900 mV in our case. Thus, to enlarge input range of low voltage OTA, we propose to use a local bootstrapped supply voltage to the input stage of OTA, which will be explained in the following section. It is feasible in functional electrical stimulation (FES) applications since higher voltage has to be adopted somewhere to provide high enough current for stimulating electrodes. Also the clock signals of the voltage doubler are already available due to the switch-capacitor technique used to realize the integrator of the modulator. In addition, the proposed rail-to-rail solution has a simple circuitry comparing with the conventional rail-to-rail OTA techniques that utilizes duplicated current sinks/sources, current control or minimum-select circuits to realize constant G_m. The system block diagram of the proposed 2nd-order ΣΔ modulator with half delay integrators is shown in Figure 4.2.

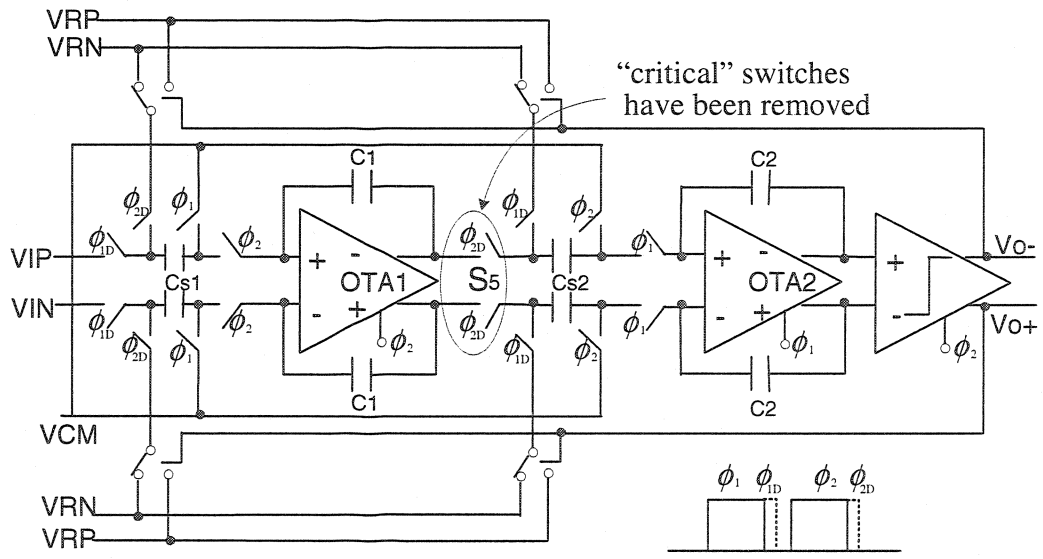


Figure 4.2 Half delay switched-OTA integrator cell with delayed clocks

Fully differential mode is adopted to reduce the even orders harmonics of distortion and improve the common mode rejection ratio (CMRR) [20]. The switches are made of CMOS transmission gates, which are controlled by a four phase clocking scheme, two non-overlapping clocks (ϕ_1 and ϕ_2) and two delayed clocks (ϕ_{1D} and ϕ_{2D}). The delayed clocks reduce the charge injection of the "critical" switches along the signal path [3]. V_{RP} and V_{RN} represent the reference voltages, which are selected by the outputs of the modulator and fed back to the integrators. The gain units A1 (A2) in Figure 4.1 are realized by configuring the ratio between capacitors C_{s1} (C_{s2}) and C_1 (C_2).

From a viewpoint of saving power-consumption, switched-opamp technique is used to implement switched-OTA integrator shown in Figure 4.2. As above mentioned in chapter 3, this technique is introduced in [9] to realize a true low-voltage operation by adding an extra switched-opamp to replace the "critical" switch S_5. As a consequence, it causes an increased power and area allocation. This can be avoided in our case, since $\Sigma\Delta$ modulator topology uses half delay integrators based on switched-opamp technique. Also, both of two switches S_5 and switched-OTA_1 work at the same phase ϕ_2 (Figure 4.2), thus the two "critical" switches S_5 can be eliminated and their function is realized by turning on and off the switched-OTA_1. Therefore, full-delay switched-opamp integrator [9] [32] is replaced by using a half-delay one [34]. Half delay integrator based on switched-opamp technique allows reducing power consumption and eliminating the critical switches S_5. In addition, a good conductivity of other "critical" switches can be easily obtained by using bootstrapped control clocks, which come from the above mentioned voltage doubler.

4.3.2 Rail-to-rail class AB OTA

The OTA is a critical block needed to implement an integrator. Figure 4.3 presents the proposed rail-to-rail class AB OTA, which is inspired from [34]. It is a one-stage fully differential OTA with a modest gain, thus only one pole exists in the signal path. Consequently, no frequency compensation is needed.

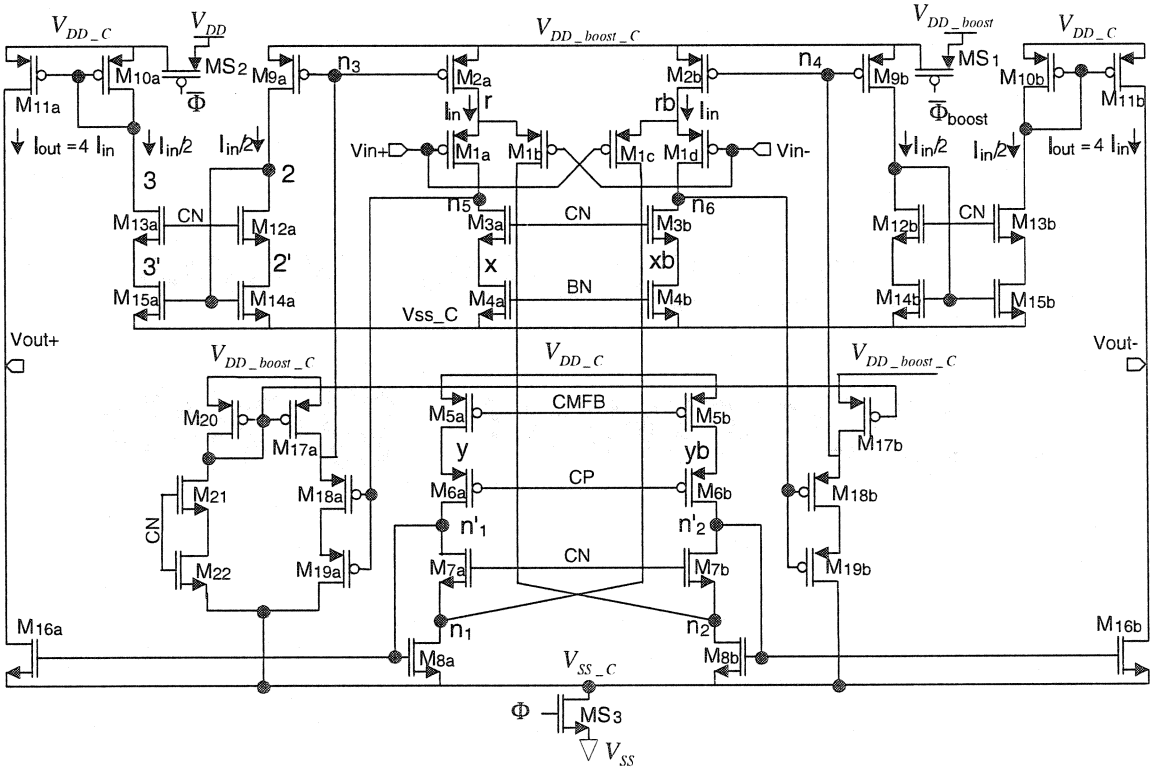


Figure 4.3 The fully differential low-voltage class AB OTA

To realize a rail-to-rail operation of the class AB OTA, their input-pair branches are connected to a bootstrapped voltage ($V_{DD\_boost\_C}$) shown in Figure 4.3, which is provided by an on-chip voltage doubler. The output branches are still working under the low-voltage supply (V_{DD_C}) in order to reduce the power consumption of the OTA. This could

be done by introducing two current mirrors, which consist of transistors M_9~M_{14}, between the input pairs and the class AB output stage. The current mirrors transmit current signal while build a bridge between two supply-voltage levels. Slew rate and settling time of the OTA are the two critical transient characteristics of operating a switch-capacitor integrator. They are dependent on the flowing currents of output and the transconductance of the input-pair.

Considering power consumption, the criterion of choosing the current mirror ratio is to increase the amount of current flowing in the output, while decreasing that of the current-mirror bridge. Here, the ratio of our proposed OTA is chosen as

$$g_{m2a} : g_{m9a} : g_{m10a} : g_{m11a} = 2:1:1:8 \tag{4.2}$$

where, g_{mi} represents transconductance of the *ith* MOS transistor. Therefore, the overall transconductance of the OTA is written as

$$G_m = \frac{i_{out}}{V_{in}} = \frac{g_{m11a}}{g_{m10a}} \cdot \frac{g_{m9a}}{g_{m2a}} \cdot (g_{m1b} + g_{m1c}) = 8 g_{m1b} \tag{4.3}$$

Since only P-type input pair is employed, the transconductance value can remain constant in the rail-to-rail OTA, regardless of the input common mode voltage.

When increasing the input common mode voltage, the raised voltage of node n_5 (n_6) may push the transistor M_{1a} (M_{1d}) operating in triode region instead of saturation region. To avoid this situation happening, a voltage level shifter, which consists of transistors

M_{17}~M_{22}, is added in this OTA. After an adjustment, it causes a 900 mV voltage drop between nodes n_3 and n_5. Three switches (M_{S1}~M_{S3}) are directly added on the supplies and ground of the proposed rail-to-rail class AB OTA to turn it on or off. Note that the clock signal of switch M_{S1} has to use a bootstrapped clock for completely turning off the switch. In Figure 4.3, if clock ϕ turns on and off NMOS switch MS_3 for connecting and disconnecting ground, then clock $\overline{\phi}$ and $\overline{\phi_{boost}}$ turn on and off PMOS switches MS_2 and MS_1 for connecting and disconnecting voltage supply V_{DD} and boosted voltage supply V_{DD}_boost of output and input stages respectively.

4.3.3 Clock generation

The clock generator (Figure 4.4), provides nonoverlapping clocks with their complementary clocks to control transmission gates, and delayed clocks (Figure 4.5) to minimize charge injection. The clock Pc and its complementary P'c are used to drive charge pump (voltage doubler) shown in Figure 4.6. These clocks (Pc and P'c) dissipate more power than other clocks generated to control transmission gates. Most part of dynamic power is attributed to generate boosted voltage and boosted clocks to input stages of two switched-OTAs.

4.3.4 Voltage doubler and its effect on SNR

As explained in chapter 3, an on-chip voltage doubler is integrated to provide the boosted voltage and clocks to the OTA input stage. Figure 4.6 shows a schematic of the adopted voltage doubler [14]. Cross-coupled transistors M_1 and M_2 combined with capacitor C_1

and C'_1 generate a bootstrapped complementary clock signal at the nodes *A* and *B*. The configuration of transistors M_3 and M_4 ensure the higher voltage of nodes *A* and *B* being transferred to the output node at any instant, thus a boosted DC voltage is obtained at that node. Transistors M_5 and M_6 are added to keep the higher voltage at the bulk node in order to reduce the leakage current of M_3 and M_4. Also the capacitor C_s is used to preserve the bulk's voltage. The capacitor C is only present to smooth output voltage. Clock generator as mentioned above section drives Pc and P'c.

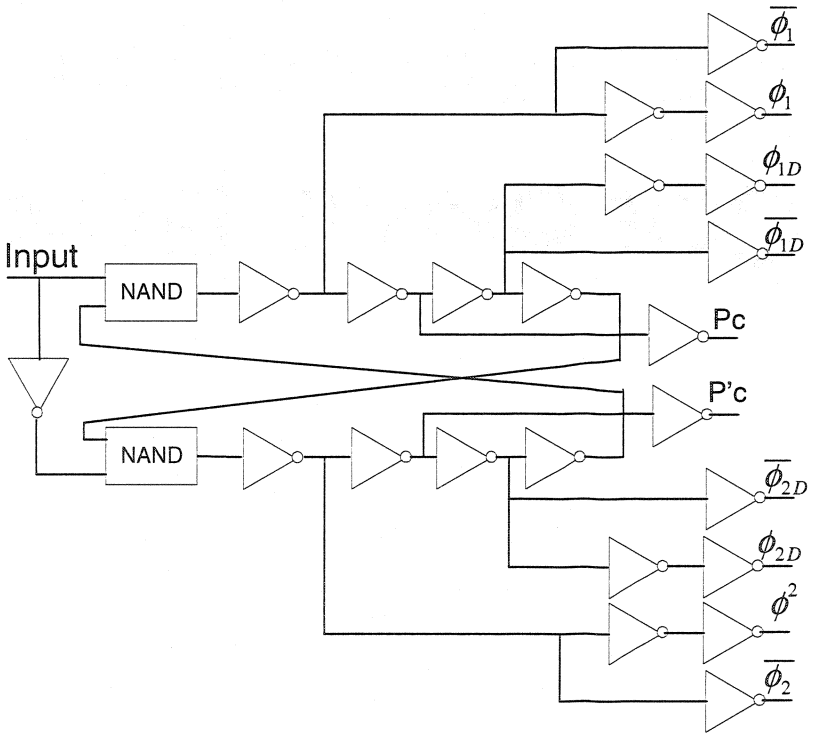


Figure 4.4 Clocks generation circuit

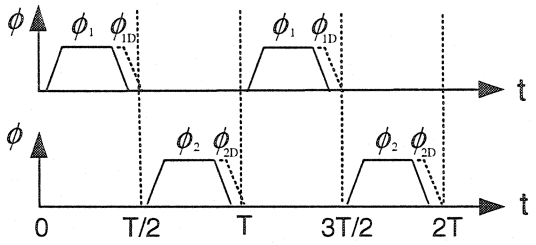


Figure 4.5 Waveforms of a typical two-phase and nonoverlapping clock scheme

Boosted clock generation circuitry is built by transistor M_7 and capacitor C_3. The gate of transistor M_7 is connected with node B. Transistor M_7 is turned on and off by V_g combination with clock $\overline{\phi_1}$. The non-overlap boosted clock generation circuit consists of transistor M_8 and capacitor C_4. The gate of transistor M_8 is connected to node A. Voltage doubler generates boosted voltage to supply input stage of the OTAs and boosted clocks to turn on and off input stage of the switched-OTAs.

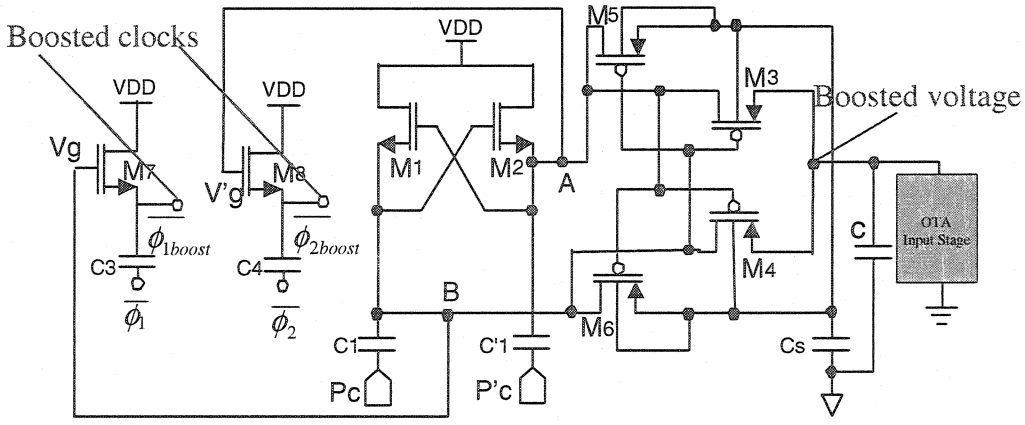


Figure 4.6 Voltage doubler circuit

However, the boosted voltage from voltage doubler contains ripples and glitches that attribute to the capacitors are charged and discharged. Clearly, to have a low ripple we must replace the filtering capacitance (C) with a bigger one, which will waste power on it. Fortunately, the ripples from boosted voltage are almost suppressed by the virtue of high power supply rejection ratio (PSRR) at the OTA input stage. The PSRR of the boosted voltage can be calculated by

$$PSRR^{+}(V_{DD\_boost}) = A_V \cdot \frac{V_{DDb}}{V_{out}} \tag{4.4}$$

where A_V denotes DC gain of the OTA, V_{DDb} is noise signal from V_{DD} from boosted voltage and V_{DDb}/V_{out} presents power supply rejection. $PSRR^{+}(V_{DD\_boost})$ depends on power supply rejection as follows.

From the low frequency small-signal model analysis of Figure 4.3, as the analysis presented in the Appendix A, the following equation can be given

$$\frac{V_{out}}{V_{DDb}} \cong \frac{1}{g_{ds11a} + g_{ds16a}} \left(\frac{g_{m11a} g_{ds9a}}{2 g_{m10a}} - \frac{g_{m16a} g_{ds1c}}{g_{m8a}} \right) \tag{4.5}$$

where, $g_m = \sqrt{2k_n'} \sqrt{W/L} \sqrt{I_D}$ and $g_{ds} = \lambda I_D$, therefore

$$\begin{aligned} &\frac{g_{m11a} g_{ds9a}}{2 g_{m10a}} - \frac{g_{m16a} g_{ds1c}}{g_{m8a}} \\ &= \frac{\sqrt{2k_{p11a}'} \sqrt{16(W_{11a}/L_{11a})} \sqrt{4I_{in}} \cdot \lambda I_{D9a}}{2\sqrt{2k_{p10a}'} \sqrt{2(W_{10a}/L_{10a})} \sqrt{I_{in}/2}} - \frac{\sqrt{2k_{n16a}'} \sqrt{16(W_{16a}/L_{16a})} \sqrt{4I_{in}} \cdot \lambda I_{D1c}}{\sqrt{2k_{n8a}'} \sqrt{4(W_{8a}/L_{8a})} \sqrt{I_{in}}} \end{aligned} \tag{4.6}$$

In the OTA design, PMOS transistors M_{10a} and M_{11a} are chosen with same size but different multipliers. Likewise, design rule are adopted for NMOS transistor M_{16a} and M_{8a}. Therefore, substituting $W_{11a}/L_{11a}= W_{10a}/L_{10a}$ and $W_{16a}/L_{16a}= W_{8a}/L_{8a}$ into Eq.(4.6), it can be rearranged as

$$\frac{g_{m11a} \cdot g_{ds9a}}{2g_{m10a}} - \frac{g_{m16a} \cdot g_{ds1c}}{g_{m8a}} = 4\lambda I_{D9a} - 4\lambda I_{D1c} \tag{4.7}$$

Both of PMOS transistors M_{9a} and M_{1c} have the same quiescent current ($I_{D9a}=I_{D1c}=I_{in}/2$), then, equation (4.5) can be zero approximately, which means that the power supply rejection V_{DDb}/V_{out} is almost equal to infinite value. In practice, high $PSRR^+$ at the OTA input stage is large enough to suppress noise from boosted voltage power. Therefore, there is no significant degradation to SNR (or SNDR) by using voltage doubler. The simulation result shows a $PSRR^+(V_{DD\_boost})$ of 97 dB for single output and 251 dB for fully differential output. These values demonstrate the same result as the above analysis.

4.3.5 Common mode feedback

In fully differential circuits, a common mode feedback (CMFB) is indispensable to fix the output node's DC voltage. It can be implemented by means of error amplifier based approach or switched-capacitor common mode feedback (SC-CMFB). The latter method is the most popular one due to its simplicity and low power consumption. The conventional SC-CMFB circuit [3] controls the current sources in the output stage of an OTA. However, since the class AB topology is utilized at the output stage of proposed OTA, the feedback signal has to be lead to the current sources in the input stage of this

OTA (M_{5a} and M_{5b} in Figure 4.3). The modified SC-CMFB circuit exchanged the position of reference voltage (*Vref*) and output voltages (Vout-, Vout+), as shown in Figure 4.7, which allows building a negative feedback in the class AB OTA. Vctrl is driven by desired control voltage labeled "CMFB" from OTA (Figure 4.3). The labels CN and BN in Figure 4.7 represent the bias voltages that are generated by an on-chip bias circuit, which is described in next section.

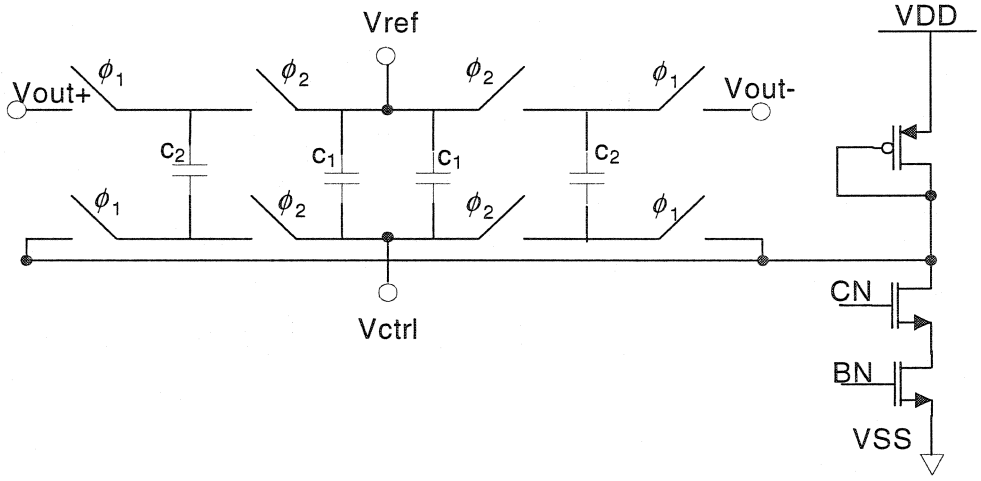


Figure 4.7 Common mode feedback circuit

4.3.6 Bias circuit design

An on-chip bias circuit is needed to supply the biasing voltages to all the class AB OTAs and all the CMFB circuits in the system. Thereby, it is very import to design bias circuit working stable. Figure 4.8 shows an on chip bias circuit. The prototype of this bias circuit is adopted from [20].

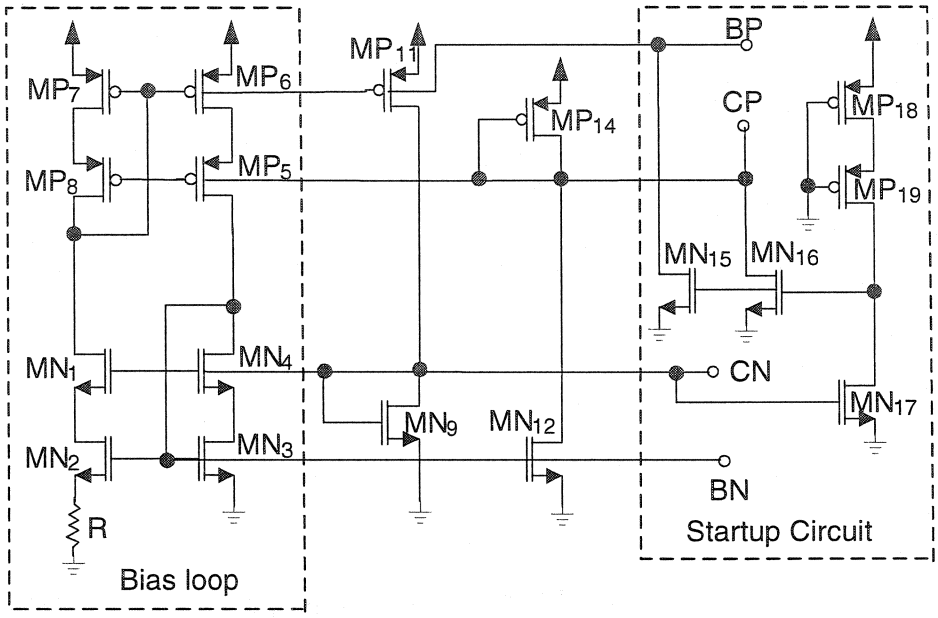


Figure 4.8 A constant transconductance bias circuit

This bias circuit consists of four different loops: Main bias loop with positive feedback, the start-up loop and the two loops used for establishing the bias voltages for the cascode transistors. The most important advantage of this bias circuit is that it realizes a stable transconductance of each transistor. In the bias loop, if the transistors MP6 and MP7 have the same ratio W/L, it will make both sides of circuit having the same current due to the current mirror. For transconductance of transistor MN3, we have the very important equation

$$g_{m3} = \frac{2\left[1 - \sqrt{\frac{(W/L)_3}{(W/L)_2}}\right]}{R} \tag{4.8}$$

It shows that transconductance of MN3 is determined by geometric ratio only, independent of power-supply voltage, process parameters, temperature, or any other parameters with large variability. Suppose $(W/L)_2 = 4(W/L)_3$, we then have simply

$$g_{m3} = \frac{1}{R} \tag{4.9}$$

Note that not only g_{m3} is stabilized, but all other transconductances are also stabilized since all transistor currents are derived from the same biasing network. Therefore, the ratio of the currents is mainly dependent on geometry. For each n-channel transistor, the transconductance can be given as

$$g_{mi} = g_{m3} \times \sqrt{\frac{(W/L)_i I_{Di}}{(W/L)_2 I_{D2}}} \tag{4.10}$$

And for each p-channel transistor

$$g_{mi} = g_{m3} \times \sqrt{\frac{\mu_p (W/L)_i I_{Di}}{\mu_n (W/L)_2 I_{D2}}} \tag{4.11}$$

The diode-connection transistors MN9 and MP14 generate the high-swing cascode bias voltage. It should be noted that the bias circuit of Figure 4.8 employ positive feedback, and designer must pay attention to its design to avoid unstable performance. Instability is avoided by making MN2 wider than MN3, which has been pointed out. However, the circuit can be operated in primeval stable state in which all currents are zero. To get it out

of this state, it is necessary to add a start-up circuit which is composed of transistors MN15~MP19 as shown in Figure 4.8. The start-up circuit only affects the bias circuit when all currents in the loop are zero. In this case, MN17 is off, as the transistor MP18 and MP19 are always on, the gates voltage of MN15 and MN16 are pulled high and turn on, then currents is injected into the bias loop circuit, thus the bias circuit start up. Then MN17 turns on, sinking all of the currents from MP18 and MP19, pulling the gates of MN15 and MN16 low, and finally turning them off. So, start up circuit will not affect the bias loop any more. In order to saving power, the PMOS MP18 and MP19 are usually chosen by small W/L. The labels BN, CN, CP, BP denote the bias voltages in Figure 4.8.

4.3.7 Comparator and D/A feedback circuits

An important component of analog-to-digital converter (ADC) is a quantizer. As mentioned in [2], Nyquist converters need precise analog components in their conversion circuits. Typically, a quantizer design includes a very precise sample and hold circuit and a high-accuracy comparator working at Nyquist sampling frequency. The accuracy requirement of the comparator depends on the accuracy requirement of the converter, e.g. a 10-bit ADC requires a comparator with at least 10-bit accuracy. In contrast, in ΣΔ modulators, the comparator is required to work at a high oversampling frequency but its resolution can be as small as 1 bit. In fact, most present oversampling converters make use of one-bit quantizers (i.e. only two output levels) due to reasons already discussed in chapter 2. Therefore, the comparator design in ΣΔ modulators focuses more on a high-speed operation instead of accuracy.

The quantizer design in this work, the comparator is implemented by using a low power high-speed comparator, which prototype is adapted from [42], as is shown in Figure 4.9. The operation of the comparator is described as follows:

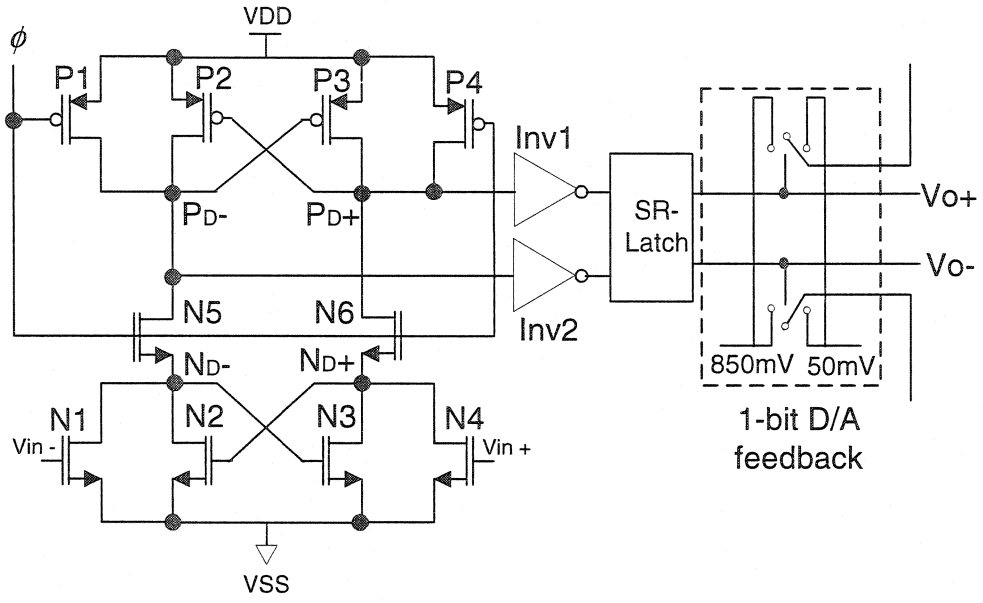


Figure 4.9 Schematic of comparator with one-bit DAC

N1 and N4 are the discharge current controlling transistors that are connected to the n-channel flip-flop formed by N2 and N3. Likewise, P1 and P4 are the precharge transistors that are connected to the p-channel flip-flop formed by P2 and P3. N5 and N6 are transfer gates for strobe. Two inverters Inv1 and Inv2 that act as buffers isolate the comparator from the output load and amplify the comparator output. Where ϕ is driven by clock from clock generator as given in section 4.3.3. In addition, one SR-Latch, connected with two outputs of the comparator, is introduced to avoid the appearance of unwanted transition associated with the clock signal.

The dynamic operation of this circuit is divided into precharge phase and evaluation phase. During the precharge phase, clock Φ is low, strobe transistors N5 and N6 are "off" and the comparator does not respond to any input signal. Precharge transistors P1 and P4 are "on", the drains P_D- and P_D+ of P2 and P3 are charged up to voltage supply level. On the other side, N1 and N4 discharge the drains N_D- and N_D+ of N2 and N3 to ground.

During the evaluation phase, clock Φ goes high, strobe transistor N5 and N6 are turned "on". Both the PMOS drain voltages, P_D- and P_D+ , drop from positive level, and both the NMOS drain voltages N_D- and N_D+ rise from ground together initially. Suppose V_{in}+ is higher than that at V_{in}-, due to N4 having a larger gate voltage, N4 draws more current than N1. Thus, P_D+ drops faster than P_D- and N_D- rises faster than ND+. As P_D+ drops a threshold voltage below V_{DD}, P2 turns on and charge P_D- to high voltage level while P_D+ keeps going to ground. Also, as N_D- rises a threshold voltage above ground, N3 turns on and discharge N_D+ to ground while N_D- keeps rising to V_{DD}. The regenerative action of P2 and P3 together with that of N2 and N3 pulls N_D+ down to ground, and pulls N_D- to V_{DD}. Hence, following the inverters Inv1 and Inv2, V_o+ is pulled up to V_{DD} and V_o- is pulled down to ground. It is similar that the operation for the case when the voltage at V_{in}- is higher than that at V_{in}+.

The one-bit D/A feedback circuit utilizes voltage-controlled switches driven by the comparator outputs. Feedback reference voltages depend on the output signal swing range. In our case, high and low reference voltages are 850 mV and 50 mV respectively.

4.3.8 Reduction of charge injection effects

The charge injection, one of the non-ideal effects of MOS switches in modulator, result in decreasing SNR or SNDR. In Figure 4.2, each switched-capacitor integrator should be designed for cancellation of charge injection errors. Assume v_{in} is signal voltage along signal path, C_S represent sampling capacitor. From introduction of charge injection (section 3.3.1), each CMOS switch transmission gate gives the error

$$\Delta V_{charge} = -\frac{(Q_{chan})_N}{2C_S} + \frac{(Q_{chan})_P}{2C_S}$$

$$= -\frac{C_{ox}}{2C_S}\{W_N L_N (V_{DD} - v_{in} - V_{THN}) - W_P L_P (v_{in} - |V_{THP}|)\} \tag{4.12}$$

For a partial cancellation of charge injection error, even if the NMOS and PMOS devices are designed to have equal sizes,

$$W_N L_N = W_P L_P \tag{4.13}$$

The charge injection can not be almost cancel out, unless

$$v_{in} \equiv \frac{V_{DD}}{2} \tag{4.14}$$

In switch-capacitor circuit, the charge injections of the switches in the signal path are signal dependent distortion (introduced in section 3.3.2), even if the transmission gate are not sufficient to avoid such signal dependent error. Since the input signal voltage (v_{in}) is not always in the middle of power supply due to signal swing from rail to rail, the charge

injection cancellations are seldom to be achieved by using transmission gate, thus results in harmonic distortion.

To minimize such charge injection errors, the simplest way of the sampling capacitor (Cs_1) size must be increased (Figure 4.2), but this will require more power consumption. Therefore, this can be achieved through delayed clocks (ϕ_{1D} and ϕ_{2D},) [23]. When switches labeled ϕ_1 are first turned off, the charge injection from those switches remains, to a first order, independent of the input signal. Because one of capacitor plates is now floating, turning off switches labeled ϕ_{1D} shortly after does not introduce charge injection errors [38] [39].

Signal independent charge injection error [3] is introduced by switched-OTA (Figure 4.3). Three switches (MS1, MS2 and MS3) are used to turn on and off quiescent current path of OTA. PMOS switch MS1 interrupts boosted voltage V_{DD}_boost and introduces charge injection error. If the charge injection in voltage across a corresponding capacitance C_{load}, from charge injection analysis of chapter 3, such error can be written as

$$\Delta V_{charge1} \cong \frac{C_{ox} \cdot W_1 \cdot L_1 \cdot (V_{DD\_boost} - V_{DD} - |V_{THP0}|)}{2C_{load}} \tag{4.15}$$

The PMOS switch MS2 interrupts supply voltage V_{DD} (0.9V). The charge injection error in voltage across C_{load} is

$$\Delta V_{charge2} = \frac{C_{ox} \cdot W_2 \cdot L_2 \cdot (V_{DD} - |V_{THP0}|)}{2C_{load}} \tag{4.16}$$

Finally, the NMOS switch MS3 interrupts V_{SS}. The charge injection in voltage across C_{load} is approximated by

$$\Delta V_{charge3} = -\frac{C_{ox} \cdot W_3 \cdot L_3 \cdot (V_{DD} - V_{THN0})}{2C_{load}} \tag{4.17}$$

Equations (4.15), (4.16) and (4.17) show that these charge injections from switched-OTA are signal independent effect, simply an offset occurs which is much easier to manage than signal dependent charge injection. Therefore, the half size dummy switch technique (introduced in section 3.3.1) is used in each switched-OTA to minimize signal independent charge injection.

4.4 Summary

We presented in this chapter the implementation of a low power low voltage 2^{nd}-order ΣΔ modulator with rail-to-rail input and output ranges. To optimize the SNR, fully differential mode is adopted to reduce distortion from the even orders harmonics and improve the CMRR. A class AB OTA with rail-to-rail input stage is realized by on-chip voltage doubler, which provides boosted voltage to input stage of OTA to enlarge input range. Half-delay integrator based on switched-opamp technique is mainly employed for saving power and eliminating the critical switches behind switched-OTA. Delayed clocks and dummy switch technique are used in modulator in order to minimize charge injection effects as much as possible. With operating voltage supply of 900mV, a low power 2^{nd}-order ΣΔ modulator based on switched-opamp technique has been implemented and

fabricated by using 0.18 μm CMOS technology offered by TSMC. Its simulation and experimental results will be presented in chapter 6.

CHAPTER 5

0.9 V LOW POWER FOURTH-ORDER ΣΔ MODULATOR

5.1 Introduction

Based on the 2nd-order ΣΔ modulator introduced in previous chapter, a 4th-order ΣΔ modulator is implemented utilizing 2-2 cascade architecture (MASH) that has been mentioned in chapter 2. In this architecture, the 4th-order modulator based on cascaded two 2nd-order ΣΔ modulators with digital cancellation circuit (DCC). The modulator is designed using switched-capacitor circuit with half delay integrator based on switched-opamp technique, and the strategy of integrators scaling is exploited in the system to minimize power consumption as much as possible. Also, a voltage doubler is still employed in the system to provide boosted voltage to power up the input stage of OTA. This modulator has been implemented by using the 0.18 μm CMOS technology.

In this chapter, the system consideration of the 2-2 cascade 4th-order ΣΔ modulator based on 2nd-order modulator is described first, followed by a discussion of the first and second loops of the 4th-order modulator. Next, the digital cancellation circuit implementation is introduced. Finally, the summary is given out.

5.2 Fourth-order sigma-delta modulator

5.2.1 System consideration

Multi-stage noise shaping (MASH) architecture is adopted in the design of the 4th-order modulator. Figure 5.1 shows the structure of the presented 4th-order modulator, which consists of two 2nd-order ΣΔ modulators (first and second loop respectively) and a digital cancellation circuitry, where g_1~g_3 represent the coefficients in each loop respectively. g_4 is a coefficient between two loops. From viewpoint of saving power consumption, half delay integrator based on switched-opamp technique is adopted to implement the 2nd-order ΣΔ modulator. Half-delay units appear in the loop, which have been explained in chapter 3. To obtain a higher SNR, optimized coefficients must be chosen by considering the saturation [16] [40] of the integrators and the DCC gain (g_d), which determines the complexity of the multiplier and registers being employed.

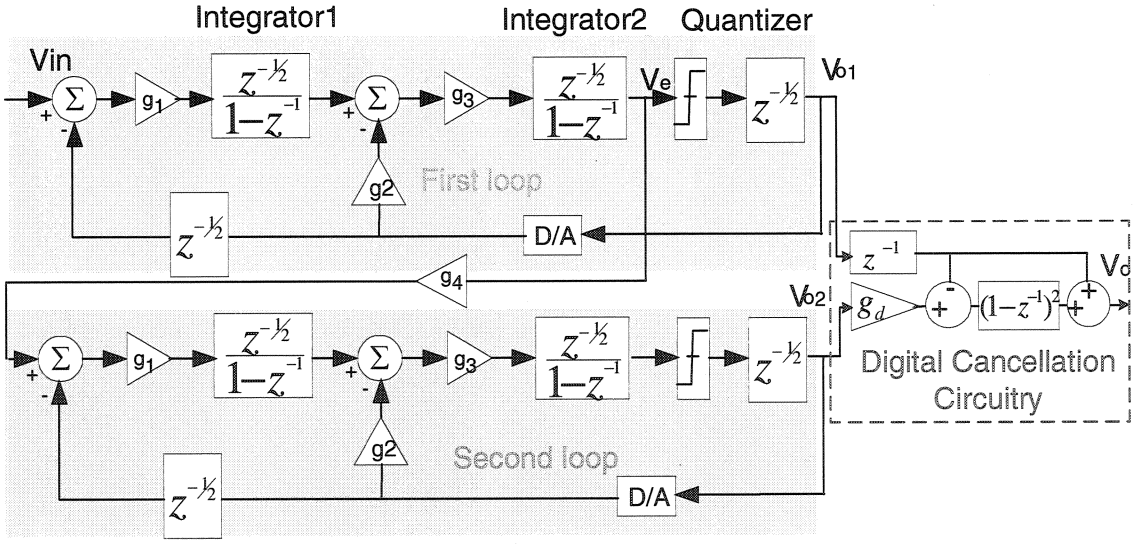


Figure 5.1 Block diagram of 4th-order ΣΔ modulator with half delay integrator

This can be analyzed by going through the derivation of signal and noise transfer function of the 2nd-order modulator as follows

$$V_{o1}(Z)=\frac{g_1 g_3 V_{in}(Z^{-\frac{1}{2}})^3+E_{n1}Z^{-\frac{1}{2}}(1-Z^{-1})^2}{1+(g_2 g_3-2)(Z^{-\frac{1}{2}})^2+(1+g_1 g_3-g_2 g_3)(Z^{-\frac{1}{2}})^4} \tag{5.1}$$

$$V_{o2}(Z)=\frac{g_1 g_3 g_4 V_e (Z^{-\frac{1}{2}})^3+E_{n2}Z^{-\frac{1}{2}}(1-Z^{-1})^2}{1+(g_2 g_3-2)(Z^{-\frac{1}{2}})^2+(1+g_1 g_3-g_2 g_3)(Z^{-\frac{1}{2}})^4} \tag{5.2}$$

where $V_{o1}(z)$ and $V_{o2}(z)$ represent the digital outputs of the first and second loop respectively, $E_{n1}(z)$ and $E_{n2}(z)$ denote the first and second loop quantization errors respectively, $V_e(z)$ is the voltage of first loop before fed into comparator. From Eq.(5.1), to obtain a 2nd-order noise shaping, the following conditions need to be satisfied.

$$g_1 g_3=1 \; and \; g_2 g_3=2 \tag{5.3}$$

However, g_3 block is followed by a comparator, which has a nonlinear function, the value of g_3 is not so critical in this case, as long as the difference of two inputs can be distinguished by the comparator. But in the MASH 4th-order modulator, the value of g_3 affects the error fed into the next 2nd-order modulator (second loop), thus equations (5.3) turn into

$$g_1 g_3 g_4 g_d=1 \; and \; g_2 g_3 g_4 g_d=2 \tag{5.4}$$

where g_d represents a gain implemented in DCC block, and g_4 denotes a coefficient between two loops, as shown in Figure 5.1.

By satisfying conditions given by equation (5.4) and passing through DCC, the second order noise ($(1-z^{-1})^2$) will be removed and the 4th-order noise-shaping function can be written as [27]:

$$V_o(Z)=\left[g_1 g_3\left(Z^{-\frac{1}{2}}\right)^4 V_{in}(Z)+g_d(1-Z^{-1})^4 E_{n2}(Z) \right] Z^{-\frac{1}{2}} \tag{5.5}$$

Thus the overall SNR of the 4th-order modulator depends on ratio of g_1g_3/g_d, however larger g_1 value may result in saturation of the following integrator, which attenuates SNDR also. Same tradeoff should be considered to choose g_3 and g_d. In our case, those values are shown in Table 5.1.

Table 5.1 Coefficients used in the design of 4th order ΣΔ modulator

Coefficient	g_1	g_2	g_3	g_4	g_d
Value	0.5	1	1	0.5	4

5.2.2 First and second loop circuitry

First and second loop circuit constructed by cascading two 2nd-order modulators, which are based on switched-capacitor technique and by means of half delay integrator with switched-opamp technique to reduce power consumption. Voltage doubler is exploited to enlarge input range of employed OTAs. The implementation of 2nd-order ΣΔ modulator with half delay integrators has been presented in chapter 4. It is important for low power

design to carefully choose sampling capacitors in the loop of 4th-order modulator. In fact, the maximum SNR of 4th-order ΣΔ modulator is given by the following equation

$$SNR_{\max} = 6.02N + 1.76 - 30.22 + 90\log(OSR) \tag{5.6}$$

From equation above, the maximum SNR_{max} reaches 157.56 dB when OSR equals 100. It can be shown that increasing two orders can make the quantization noise negligible comparing with the 2nd-order ΣΔ modulator. Thus, decreasing the thermal noise will be unavoidable in high-order modulator. To decrease such thermal noise, increasing sampling capacitor size is usually used. However, big sampling capacitance increases the power consumption. From low power consideration, thermal noise will be dominative by choosing adapted sampling capacitance. In other words, if the thermal noise is significantly smaller than the quantization noise, the capacitor size should be over-dimensioned, and results in power being wasted. Therefore, SNR performance will be limited by thermal noise in low power modulator circuit system design.

In MASH structure, two low power comparators are used, and their power consuming is much less than that of the integrators. Also, to decrease power consumption of the integrators, half delay integrator technique is utilized, and the following principles were applied:

- First, the size of the capacitors inside loop is made much smaller than the first sampling capacitance. Because the thermal noise depends mainly on the sampling

capacitor size of first integrator, thermal noise can be strongly suppressed by big sampling capacitance of first integrator [16] [8].

- Second, the transconductance of each inside opamp can be designed at low value, which is proportional to the bias current consumption. Thus, these opamps are scaled down and corresponding power consumption is reduced [33]. Finally, only the first integrator with bigger input sampling capacitance consumes high power amount.

5.2.3 Digital cancellation circuitry

As explained earlier (section 2.3.4), in cascaded 4^{th}-order modulator, the second-order quantization noise of first and second loops are removed through a digital cancellation circuitry, which improves the overall SNR. Structure of the DCC block is highly dependent on transfer function of the 2^{nd}-order modulators. Figure 5.2 presents the block scheme of the DCC module. Also its circuit implementation is given out in Figure 5.3, where d_{in1} and d_{in2} represent the one-bit output from both 2^{nd}-order modulators respectively. The gain of "4" block (Figure 5.2) is easily realized by shifting d_{in2} two bits into left. And to prevent overflow problem of addition and subtraction, the operands are expanded one-bit before the operation, represented by the MUX (multiplexer) in Figure 5.3, and provided negative number is represented by two's complement. The DCC block has been implemented by the Veriloga code (Appendix B) and synthesized using standard

0.18 μm CMOS cells. The corresponding circuit consists of 18 D-Flip-flops under 0.9 V power supply, and consumes only 4 μW when operating at 2 MHz clock.

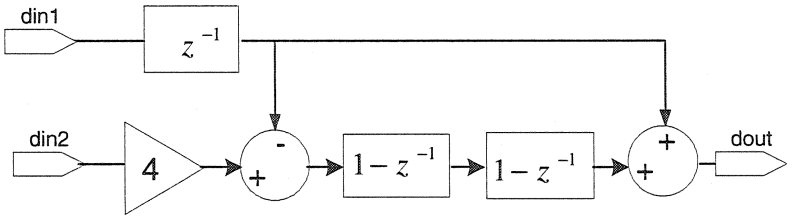


Figure 5.2 Block scheme of DCC

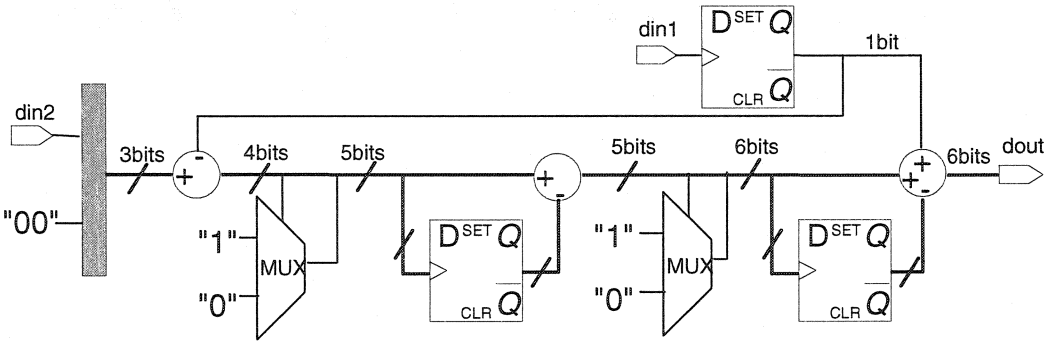


Figure 5.3 DCC implementation

5.3 Sensitivity to mismatch

The 2-2 cascade 4th-order modulator uses two 2nd-order ΣΔ modulators to achieve 4th-order noise shaping. The stability is inherently stable as same as the 2nd-order modulator. However, the cascaded modulator is sensitive to mismatches between the interstages of analog and digital circuitries. Such mismatches in MASH structure can cause low-order noise to leak through from the first loop, which reduces the SNR performance. These mismatches must be minimized. To alleviate this mismatch problem, often the first stage

is chosen to be a higher-order modulator [20] [41]. In our case, the 2^{nd}-order modulator in the first loop does not have serious leakage effect comparing with the design of a 1^{st}-order modulator [28].

5.4 Summary

A 4th-order ΣΔ modulator with fully differential OTA and rail-to-rail output swing operating at 900mV supply has been implemented using 0.18 μm technology. Due to half delay integrator based on switched-opamp technique, each integrator only work 50% of clock cycle time, therefore total power consumption of the 4^{th}-order ΣΔ modulator with half delay integrator is dropped down comparing with using full-delay integrator. By using SpectreS simulator, the simulation results are given in chapter 6.

CHAPTER 6

SIMULATION & EXPERIMENTAL RESULTS

6.1 Introduction

The proposed 2nd-order ΣΔ modulator has been implemented and fabricated using the 0.18 μm CMOS technology offered by Taiwan Semiconductor Manufacturing Co., LTD (TSMC). The 2nd-order ΣΔ modulator chip microphotograph is shown in Figure 6.1. The proposed 4th-order modulator has been implemented in the same CMOS technology and was characterized without fabrication. Appendix C illustrates the detailed schematic of each block of modulators. Appendix D gives the layout of the 2nd-order modulator and OTA respectively. The circuits were simulated and analyzed by means of simulator SpectreS. First, simulation and experimental results of the 2nd-order modulator are presented. Then, simulation results of the 4th-order modulator are given out.

6.2 Simulated characteristics of the second-order modulator

As mentioned in chapter 4, having stable bias voltages in the circuit is one of the most important factors to guarantee the design success of the system. Figure 6.2 shows the simulation result of the bias circuit. First, the start-up circuit injects the currents to the current mirror loop, in order to make the bias circuit work. Then, after around 150 ns, the biasing voltages are stable. Therefore, all the transistors in the circuit should generally be in deep saturation region except the inverters and other digital cells.

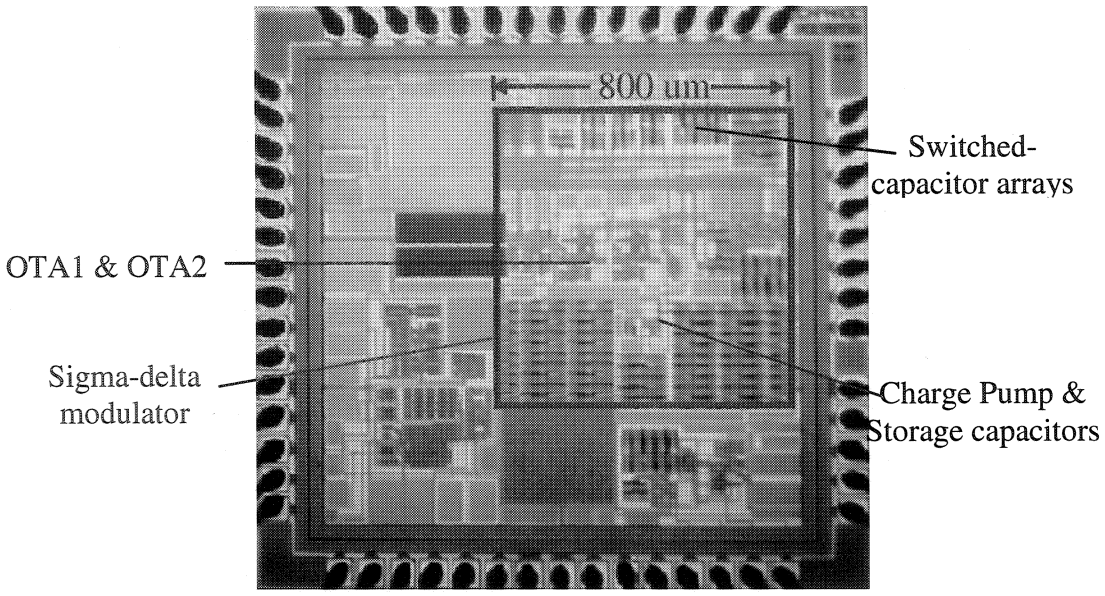


Figure 6.1 Photograph of the 2nd-order modulator

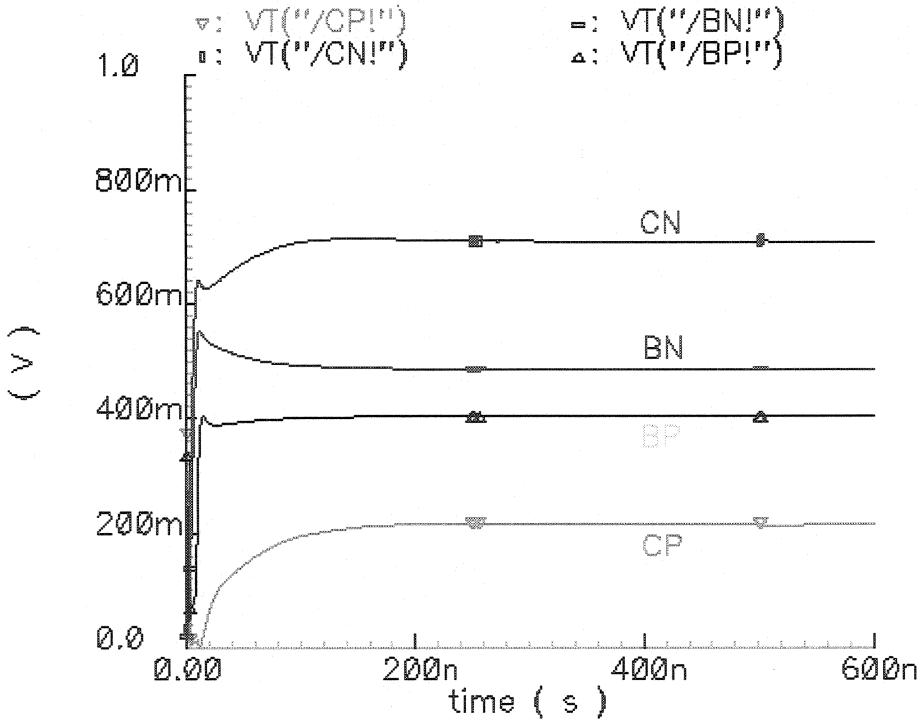


Figure 6.2 Bias Voltages

Figure 6.3 shows the transient behavior of the OTA. The boosted voltage supply from the voltage doubler contains ripples because the capacitors in voltage doubler are charged and discharged. The effects from boosted voltage ripples are avoidable in our design because the OTA has the high $PSRR^{+}$ at input stage, which has been explained in section 4.3.4.

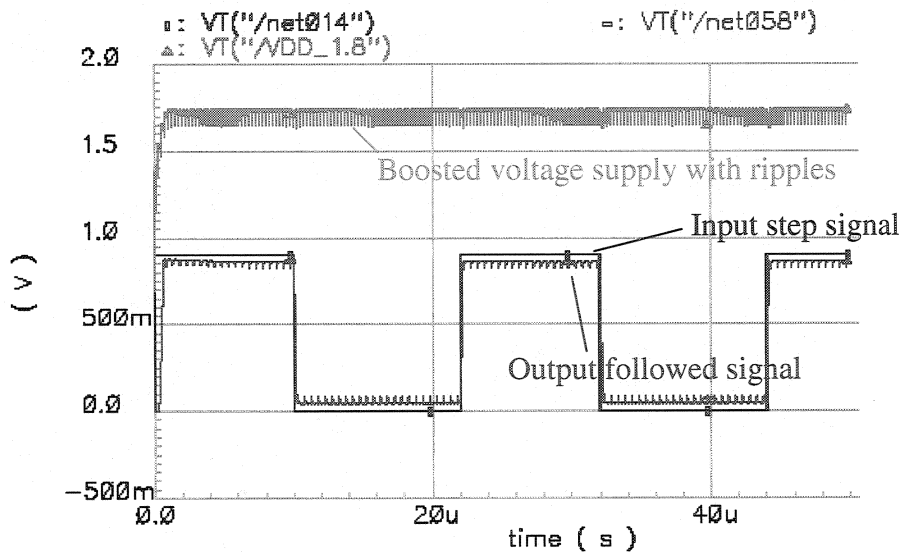


Figure 6.3 Transient behavior of the OTA

The DC gain is around 46 dB. The unity gain bandwidth is 3.16 MHz, and the phase margin is greater than 69° in 2pF load. The signal dynamic range is from 50 mV to 850 mV that is mainly limited by the class AB output stage. The slew rate and settling time of the OTA are around 12 V/μs and 180 ns respectively, which are enough to operate with a 2 MHz sampling frequency and a 900mV supply voltage. The PSRR and CMRR are available with signal frequency from 0 to 30 kHz. The simulated performance of the OTA is summarized in second column of Table 6.1.

Table 6.1 Performance of the Class AB OTA

Parameters	Simulated results	Measured results
Voltage supply	V_{DD}=900 mV, Vss=0	
DC Gain	46.3 dB	36 dB
Unity Gain Bandwidth (GBW)	3.16 MHz	1.98 MHz
Phase margin	69.8° (C_L=2pF)	61°
Slew Rate	12 V/μs (C_L=2pF)	3.96 V/μs
Settling time	180 ns (C_L=2pF)	800 ns
Input range	0 V-1.2 V	0 V-1.1 V
Output range	50 mV–850mV	60 mV–830mV
$PSRR^+$(V_{DD_boost})	97 dB (C_L=2pF)	76 dB
$PSRR^+$(V_{DD})	75 dB (C_L=2pF)	59 dB
CMRR	73.06 dB (C_L=2pF)	59 dB

The frequency of the applied input signal is 2.39 kHz. The noise power is taken into account from 0 to signal bandwidth of 10 kHz. By simulation of using simulator SpectreS, the peak SNR and SNDR achieve 74 dB and 65 dB respectively, which are obtained by MATLAB program calculation and spectrum analysis from the data of Cadence simulation. Figure 6.4 is the output spectrum when the input signal corresponding to the peak SNDR is applied. Figure 6.5 shows the simulated SNR and SNDR versus signal power in a bandwidth of 10 kHz. The total power consumption is around 38 μW that includes all the dynamic and static power dissipation by Cadence simulation of using calculator. The simulated results of the 2^{nd}-order modulator are shown in Table 6.2. The consumed power of each block is given in Table 6.3.

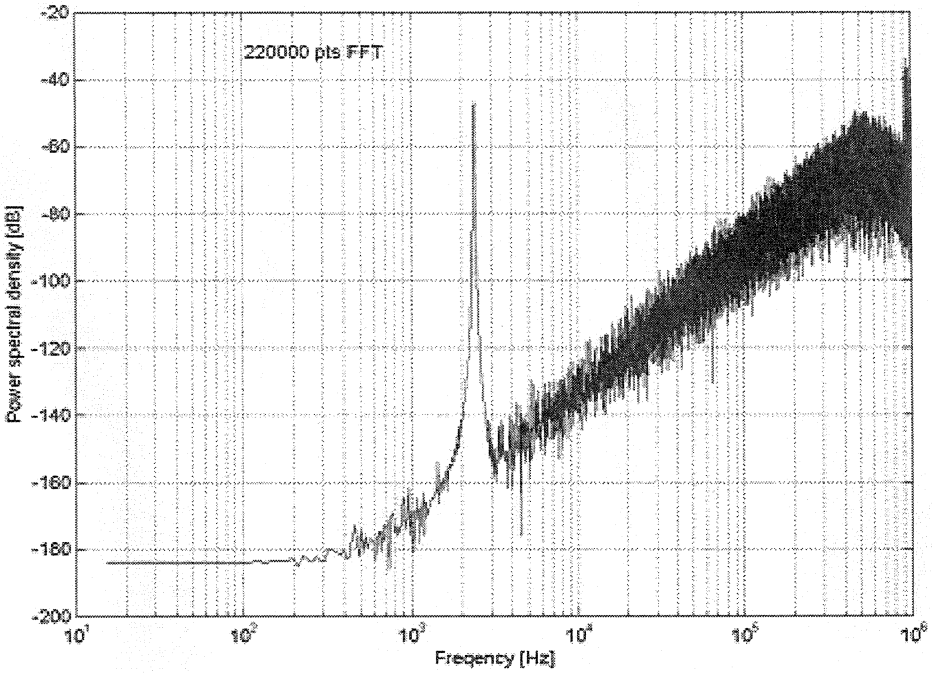


Figure 6.4 2nd-order ΣΔ modulator simulated output spectrum

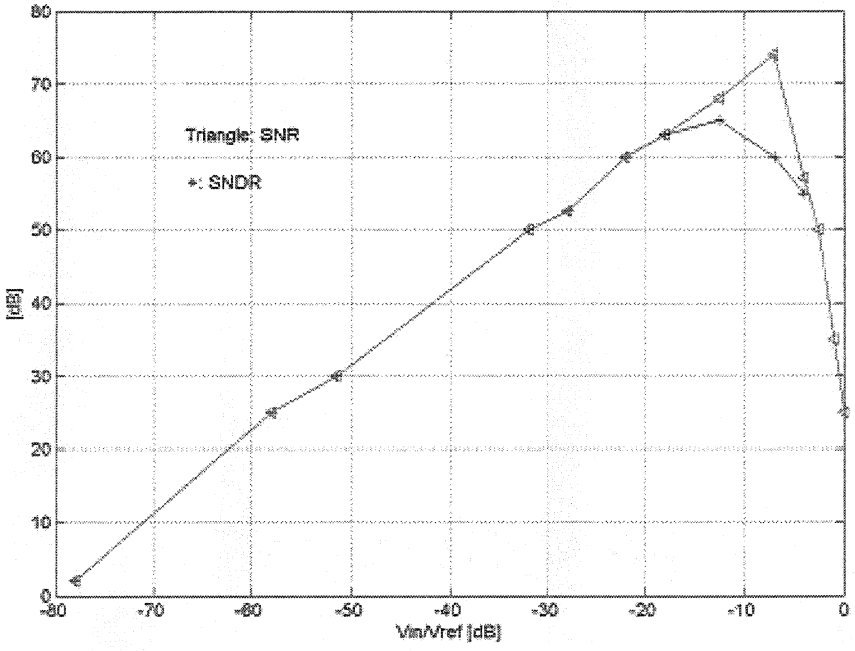


Figure 6.5 Simulated SNR versus the input signal power

Table 6.2 Simulation results of the 2nd-order ΣΔ modulator

Characteristics	Value
Power supply	VDD=0.9 V, VSS=0 V
Signal Band Width	10 kHz
Sampling frequency	2 MHz
OSR	100
DR	78 dB
Peak SNR	74 dB
Peak SNDR	65 dB
Power consumption	37.7 μW
Layout core area size	800μm×800μm

Table 6.3 The consumed power of each block

Name	Consumed power
OTA1 & OTA2	12.3 μW
Bias circuit	4.7 μW
Comparator	0.3 μW
Voltage doubler	6.5 μW
Dynamic Power	13.9 μW

Various modulators dedicated to analog to digital conversions, with different signal bandwidth, dynamic range and power consumption are often compared using the following Figure of merit [35]

$$FM = \frac{4kT \times DR \times f_N}{P} \tag{6.1}$$

where $k = 1.38\times10^{-23}$, $T = 300^{\circ}$, f_N represents the Nyquist sampling frequency and P is the total power consumption. The current design achieves the Figure of merit (FM) of 550 in simulation result.

6.3 Experimental results of 2nd-order modulator

The common mode voltage (V_{CM}) of 2nd-order modulator is set to 450 mV, which is brought about by the 900mV of analog circuit voltage supply V_{DD}. In order to avoid interference between digital and analog circuitries, we use two separate voltage supplies (V_{DD_D} and V_{DD}). V_{DD_D} denotes digital voltage supply. V_{DD} is analog voltage supply. On the test board, the modulator is operated at these voltage supplies of 900 mV. The measurement results of the OTA are shown in the third column of Table 6.1.

From the Table 6.1, we know that measured results do not meet the expected ones. This mismatch is due to the capacitances effects from both of pads and wire-bonded package. These extra load capacitances degrade the quality of OTA slew rate, DC gain and settling time. Therefore, it results in decreasing the SNR and increasing power dissipation. In

addition, OTA gain decreasing depends on both of transconductance decreasing and load capacitance increasing.

Due to pads' parasitic capacitances and resistances that result in OTA slew rate and DC gain degradation, one 500 kHz clock is used to drive the 2nd-order modulator through the clock generator. If the OSR is still 100, then the signal bandwidth is limited at 2.5 kHz. The total dissipated power is 65.6 μW including digital and analog circuits. The SNR almost drop to 65 dB, and the SNDR is around 46 dB. The experimental results of 2nd-order modulator are summarized in second column of Table 6.4.

Table 6.4 Measurement & simulation results of the 2nd-order ΣΔ modulator with extra capacitance per pad node

Parameter	Measured results	Simulated results
Power supply	VDD=0.9 V, VSS=0 V	
Signal Band Width	2.5 kHz	
Sampling frequency	500 kHz	
OSR	100	
Peak SNR	65.03 dB	67.32 dB
Peak SNDR	46.12 dB	49.87 dB
Power consumption	65.60 μW	59.50 μW

We simulated the 2nd-order ΣΔ modulator with the load capacitance of 10 pF at each pad location. The simulated results are given in third column of Table 6.4, which shows us that the results are similar to the measured ones. It demonstrates that there are effects from capacitance in pads and wire-bonded devices. Figure 6.6 shows the measured SNR and simulated SNR with extra load capacitances.

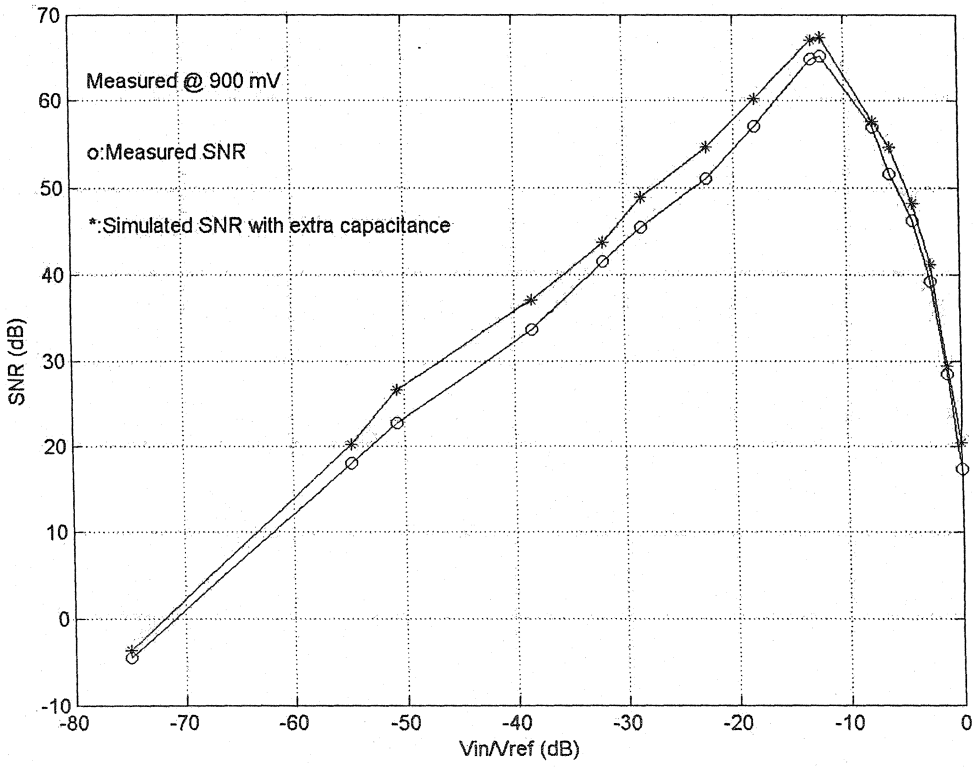


Figure 6.6 Measured SNR & Simulated SNR with extra load capacitors in each pad

Compare with another low power low voltage ΣΔ modulator implementation presented in [10], the current design achieves the same FM in simulation, but the measurement results gave a degraded FM to 12.6×10^{-6}. Table 6.5 summarizes the results and comparisons of

main parameters such as the power supply voltage, the DR, the signal BW, the power consumption (P), and FM.

Table 6.5 Comparison of our design with the closest available results

VDD (V)	DR (dB)	BW (Hz)	P (μW)	FMx10^{-6}	Reference
0.9	78	10k	37.7	550	Our work simulation result
0.9	70	2.5k	65.6	12.6	Our work measurement result
1	88	25k	950	550	[10]
0.7	75	8k	80	104.73	[37]
1.5	74	300-3400	100	28.28	[32]
1.8	50	150-200	2.2	0.3	[17]

The modulator presented in [17] was implemented in a 0.8 μm technology. The input differential pair of the amplifier works in weak inversion. The modulator achieves very low power consumption 2.2 μW. However, it has a DR of around 50 dB and a very narrow signal bandwidth 150-200Hz. This design gave only a Figure of merit of 0.3×10^{-6}.

6.4 Simulation results of 4th-order modulator

The proposed 4th-order ΣΔ modulator has been implemented and characterized using a 0.18 μm CMOS technology (Figure 6.7). The simulation results of the proposed 4th-order modulator are summarized in Table 6.6. The Figure 6.8 shows that the peak SNR of

this ΣΔ modulator is up to 90 dB. The layout core area size of the 4th-order modulator is around 1350μm×820μm and the overall consumed power is only 85.7 μW.

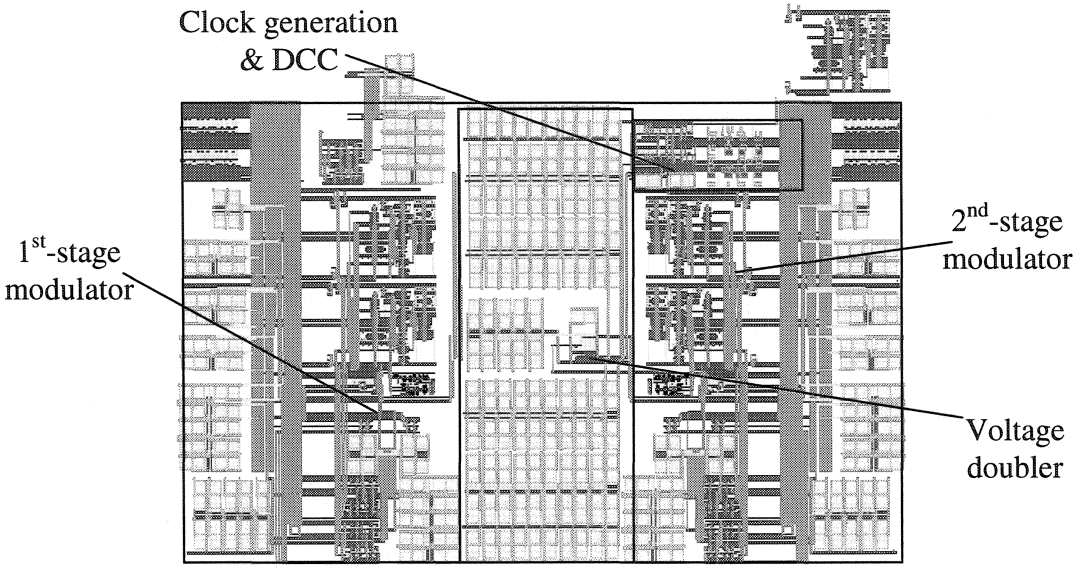


Figure 6.7 Layout of the proposed 4th-order ΣΔ modulator

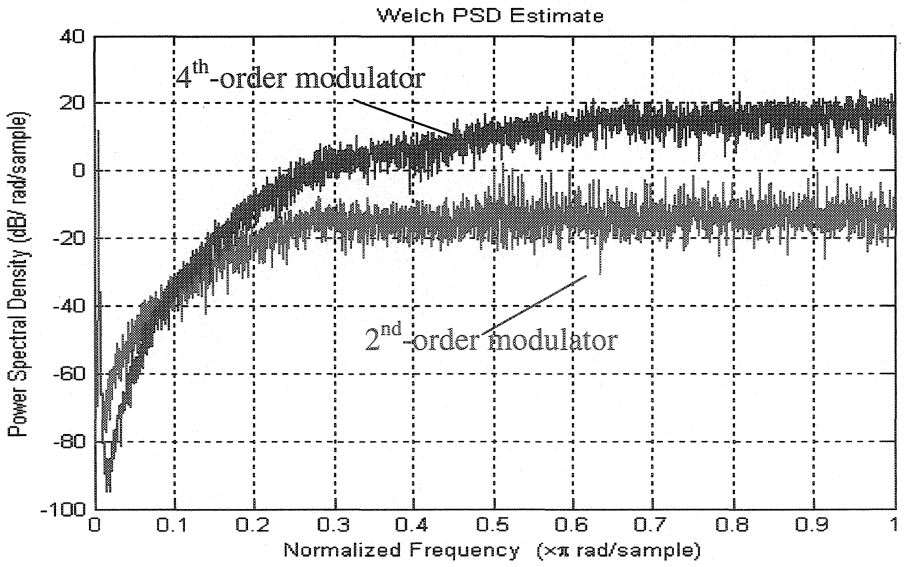


Figure 6.8 SNR figures of the proposed ΣΔ modulators

Table 6.6 Simulation results of the proposed 4th-order modulator

Characteristics	Simulation results
Power supply	VDD=0.9 V, VSS=0 V
Signal Band Width	10 kHz
Sampling frequency	2 MHz
OSR	100
Peak SNR	90 dB
Power consumption	85.7 μW
Layout core area size	1350μm×820μm

6.5 Summary

The proposed low power low voltage 2^{nd}-order ΣΔ modulator with rail-to-rail dynamic range has been implemented. Half delay integrators based on switched-opamp technique are exploited in the system for saving power consumption. Voltage doubler has been used for rail-to-rail signal swing. The 2nd-order ΣΔ modulator, which is implemented and fabricated in using a 0.18 μm CMOS technology, has a layout core area of 800μm×800μm. The tested results showed that this modulator achieves a SNR of 65 dB and SNDR of 46 dB respectively. Based on 2^{nd}-order modulator design, a 4^{th}-order ΣΔ modulator has implemented in a 0.18 μm CMOS technology, it achieves a SNR of 90 dB with dissipation 85.7 μW in simulation results.

Finally, it should be noted that unexpected effects from extra capacitances in pads and wire-bonded devices degrade measured results, in order to avoid such problems and reach expectation, it is crucial to design buffers between the layout circuits and the pads.

CONCLUSION

This master thesis concerns the design of a low power low voltage ΣΔ modulators dedicated to build analog-to-digital converters. We studied fundamental limitations of such low power low voltage circuit applications. The principal of ΣΔ modulator and corresponding low voltage approach are reviewed, and the fundamental power limits and low voltage requirements are discussed. Therefore, two low voltage techniques, switched-opamp technique and voltage doubler, are reported. Then, a fully deferential low power low 2^{nd}-order voltage ΣΔ modulator dedicated to biomedical applications was implemented and fabricated. Also, based on the 2^{nd}-order modulator, a 4^{th}-order ΣΔ modulator was designed and simulated.

In order to achieve the low power designs, half delay integrator based on switched-opamp technique is employed. Also, the number of critical switches was minimized by this technique. In addition, the low supply voltage and wide input voltage range are realized by using a local boosted voltage to the input stage of OTA without significantly degrading SNR and thus enlarge dynamic range of modulators. These characteristics were achieved without degrading the SNR. On the other hand, the fully differential mode is adopted in most circuit to reduce the distortion of even orders harmonics and improve the common mode rejection ratio. The noise from boosted voltage of voltage doubler is almost suppressed due to the high $PSRR^{+}$ of the OTA input stage. Also, delayed clocks

and dummy switch techniques are exploited in switched-capacitor circuits to minimize charge injection effects.

Although the proposed low power low voltage ΣΔ modulators were originally designed for biomedical devices such as bioelectronics sensing, they can be used for several other applications requiring low power low voltage analog-to-digital conversion circuits.

Based on the analysis and results reported in this master thesis, the following topics are recommended for future research works to further improve the performance of the proposed ΣΔ modulators.

- Due to the OTA DC gain and its slew rate degradation, the modulator experimental results did not meet the simulation ones. These degradations are due to the output load effects from capacitances of pads including wire-bonded device. Therefore, it is necessary to add buffers between the circuit and those pads.

- For the 4^{th}-order modulator, mismatch between interstage gains will cause quantization noise leakage from the first loop to the output, and then results in an incomplete cancellation of the quantization noise from the first loop. To further improve the performance of the proposed 4^{th}-order modulator, such gain mismatch should be minimized using some calibration strategies, which include

both analog circuits trimming or digital least-mean-square (LMS) based calibration [13] [26].

- To design completely ADC, following the sigma-delta analog-to-digital modulator is a low pass digital decimation filter [4] as mentioned in chapter 1 (Figure 1.1). The function of a decimation filter is to remove all of the out-of-band signals and noise, and to reduce the sampling rate (over sampling ratio) OSR, by averaging OSR values of the coarsely quantized sigma-delta output, the filter gives a high resolution output at the low rate.

- Finally, the $\Sigma\Delta$ multi-bit modulation technique [8] [22] can be employed to design high precise ADCs. However, care must be taken to ensure that the multi-bit modulator remains linear. Therefore, calibration techniques of such topologies are indispensable due to degrading linear multi-bit D/A converters [13].

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APPENDIXES

APPENDIX A

Formula deduction

Section A1

Here, we present a derivation of the equation (2.6) that given in chapter 2. An integrator and 1-bit ADC are in the forward path, and a 1-bit DAC is in the feedback path of a single-feedback loop system (Figure 2.6 in chapter 2). The variables labelled are in terms of time, T, which is the inverse of the sampling frequency, and n, which is an integer. The output of the integrator, $x(nT)$, can be described as.

$$x(nT) = u(nT - T) - q(nT - T) + x(nT - T) \tag{A1.1}$$

where, $u(nT - T) - q(nT - T)$ is equal to the integrator's previous input, and $x(nT-T)$ is its previous output.

$$e(nT) = y(nT) - x(nT) \tag{A1.2}$$

From (A1.1) and (A1.2), we have

$$y(nT) = e(nT) + u(nT - T) - q(nT - T) + x(nT - T) \tag{A1.3}$$

In reality, a 1-bit DAC consists of a couple of switches connecting $(1/2)V_{REF}$ or $-(1/2)V_{REF}$ to a common node, so assume that the DAC is ideal. Therefore,

$$y(nT) = q(nT) \tag{A1.4}$$

$$y(nT - T) = q(nT - T) \tag{A1.5}$$

Then, Eq.(A1.3) can be expressed by

$$y(nT) = e(nT) + u(nT - T) - y(nT - T) + x(nT - T) \tag{A1.6}$$

$$y(nT) = u(nT - T) + e(nT) - e(nT - T) \tag{A1.7}$$

Assume time T is unit, then

$$y(n) = u(n - 1) + [e(n) - e(n - 1)] \tag{A1.7}$$

Section A2

This section presents derivation of result given in equation (2.12) for SNR of ideal 1st-order sigma-delta modulator.

The quantization noise power is given by:

$$P_{qe} = \frac{\Delta^2}{12} \tag{A2.1}$$

For the power density, we note that the power is spread evenly between $\pm f_s/2$, resulting in a density of

$$S_e^2(f) = \frac{P_{qe}}{f_s} \tag{A2.2}$$

Because $z = e^{j\omega T} = e^{j2\pi f / f_s}$, substituting with the result from 1st-order noise transfer function ($N_{TF}(z) = 1 - z^{-1}$), we can write the equation as follows

$$\begin{aligned} N_{TF}(f) &= 1 - e^{-j2\pi f / f_s} \\ &= \frac{e^{j\pi f / f_s} - e^{-j\pi f / f_s}}{2j} \times 2j \times e^{-j\pi f / f_s} \\ &= \sin\left(\frac{\pi f}{f_s}\right) \times 2j \times e^{-j\pi f / f_s} \end{aligned} \tag{A2.3}$$

To find the magnitude of the noise transfer function, we have high pass function

$$\left|N_{TF}(f)\right| = 2\sin\left(\frac{\pi f}{f_s}\right) \tag{A2.4}$$

We suppresses the quantization noise power over the signal frequency band from 0 to f_0, we have

$$P_e = \int_{-f_0}^{f_0} S_e^2(f)\,|\,N_{TF}(f)\,|^2\,df = \int_{-f_0}^{f_0} \left(\frac{\Delta^2}{12}\right)\frac{1}{f_s}\left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^2 df \qquad \text{(A2.5)}$$

and making the approximation that $f_0 << f_s$ (OSR>>1) and $\sin(\frac{\pi f}{f_s}) \approx \frac{\pi f}{f_s}$, we will get following result

$$P_e \cong \left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^2}{3}\right)\left(\frac{2f_0}{f_s}\right)^3 = \frac{\Delta^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3 \qquad \text{(A2.6)}$$

Assuming the maximum signal power is as [20],

$$P_s = \frac{\Delta^2 2^{2N}}{8} \qquad \text{(A2.7)}$$

From equation (A2.6) and (A2.7), the maximum SNR of 1st-order sigma-delta modulator is given by

$$SNR_{\max} = 10\log\left(\frac{P_s}{P_e}\right) = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log\left(\frac{3}{\pi^2}(OSR)^2\right) \qquad \text{(A2.8)}$$

Finally, we have equivalence,

$$SNR_{\max} = 6.02N + 1.76 - 5.17 + 30\log(OSR) \qquad \text{(A2.9)}$$

Equation (A2.9) shows that doubling the OSR given an SNR improvement of 9dB or, equivalently, a gain of 1.5bits/octave for a first-order modulator.

Section A3

This section presents a derivation of the results given in equation (2.13) of chapter 2, which is an ideal transfer function of second-order ΣΔ modulator shown in Figure 2.9 (chapter 2):

$$B(z) = [U(z) - Y(z)]\frac{A_1 z^{-1}}{1 - z^{-1}} \tag{A3.1}$$

$$Y(z) = [B(z) - A_3 Y(z)]\frac{A_2 z^{-1}}{1 - z^{-1}} + E(z) \tag{A3.2}$$

Substitute Eq.(A3.3) into Eq.(A3.) it can be rewritten as

$$Y(z) = \{[U(z) - Y(z)]\frac{A_1 z^{-1}}{1 - z^{-1}} - A_3 Y(z)\}\frac{A_2 z^{-1}}{1 - z^{-1}} + E(z) \tag{A3.4}$$

Rearrange Eq.(A3.5), then

$$Y(z)[1 - 2z^{-1} + (1 + A_1 A_2)z^{-2} + A_2 A_3 z^{-1} - A_2 A_3 z^{-2}] = A_1 A_2 z^{-2} U(z) + E(z)(1 - z^{-1})^2 \tag{A3.6}$$

If $A_2 A_3 = 2$ and $1 + A_1 A_2 = A_2 A_3$, ideal transfer function in frequency domain can be expressed by

$$Y(z) = \left(z^{-1}\right)^2 U(z) + \left(1 - z^{-1}\right)^2 E(z) \tag{A3.7}$$

Section A4

From the section A.3, the signal and noise transfer function of second-order ΣΔ modulator can be given respectively by

$$S_{TF}(z) = z^{-1} \tag{A4.1}$$

$$N_{TF}(z) = (1 - z^{-1})^2 \tag{A4.2}$$

Assuming appropriate coefficients are chosen in the second-order ΣΔ modulator, the transfer function of second-order ΣΔ modulator in frequency domain can be expressed by

$$Y(z) = \left(z^{-1}\right)^2 U(z) + \left(1 - z^{-1}\right)^2 E(z) \tag{A4.3}$$

Again, similar inference of maximum SNR of 1st-order ΣΔ modulator is used, the maximum SNR performance of 2nd-order sigma-delta modulator is easily to be given by

$$SNR_{\max} = 10\log\left(\frac{P_s}{P_e}\right) = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log\left(\frac{5}{\pi^4}(OSR)^5\right) \tag{A4.4}$$

or, equivalently

$$SNR_{\max} = 6.02N + 1.76 - 12.9 + 50\log(OSR) \tag{A4.5}$$

From equation (A4.5) we find that doubling the OSR improves the SNR by 15 dB, or equivalently, 2.5 bits/octave for a second-order modulator.

Section A5

In the section A.5, we present the derivation of equation (4.5) in chapter 4. The simplified low frequency small-signal model for input stage is illustrated in Figure A.5.1.

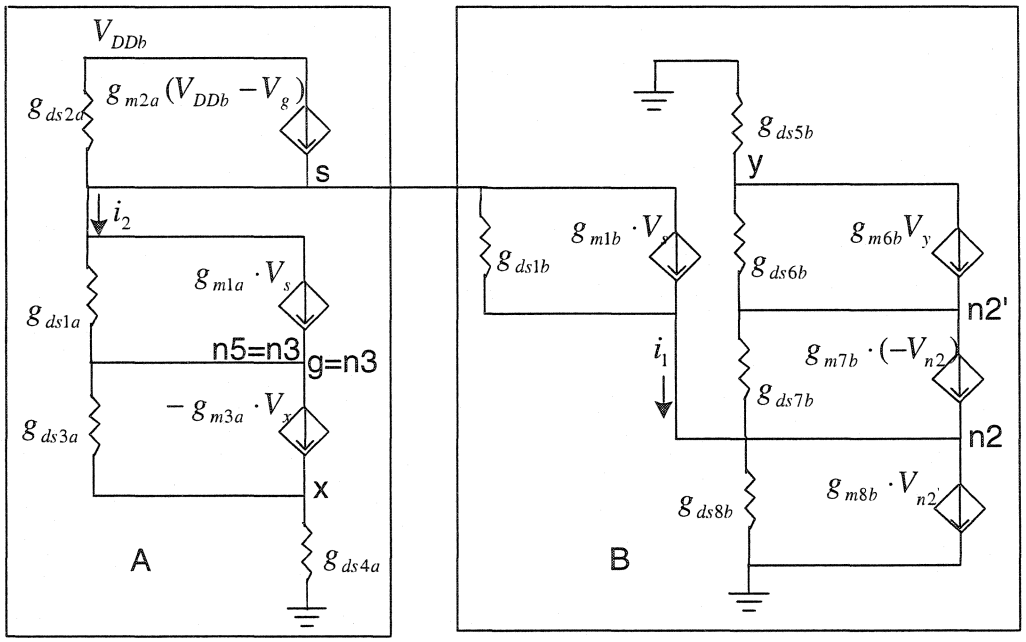

Figure A5.1 Equivalent small signal model for the input stage of OTA

From part A of Figure A5.1, we have four equivalents

$$(V_{n2'}-V_y)\cdot g_{ds6b}-g_{m6b}\cdot V_y=V_y\cdot g_{ds5b} \tag{A5.1}$$

$$(V_{n2}-V_{n2'})\cdot g_{ds7b}-g_{m7b}\cdot V_{n2}=V_y\cdot g_{ds5b} \tag{A5.2}$$

$$(V_s-V_{n2})\cdot g_{ds1b}+g_{m1b}\cdot V_s=V_{n2}\cdot g_{ds8b}+V_{n2'}\cdot g_{m8b}+V_y\cdot g_{ds5b} \tag{A5.3}$$

$$(V_s-V_{n2})\cdot g_{ds1b}+g_{m1b}\cdot V_s=V_{n2}\cdot g_{ds8b}+V_{n2'}\cdot g_{m8b}+(V_{n2}-V_{n2'})\cdot g_{ds7b}+V_{n2}\cdot g_{m7b} \tag{A5.4}$$

Assume $g_1=i_1/V_s$, from equations Eq.(A5.1) ~ Eq.(A5.4) calculation, we have

$$g_1 = \frac{i_1}{V_s} = g_{m1b} \tag{A5.5}$$

From part B of Figure A5.1, and solving for $V_{n3} = V_{n5} = V_g$, we have two equivalents

$$(V_g - V_x) \cdot g_{ds3a} - V_x \cdot g_{m3a} = V_x \cdot g_{ds4a} \tag{A5.6}$$

$$(V_s - V_g) \cdot g_{ds1a} + V_s \cdot g_{m1a} = V_x \cdot g_{ds4a} \tag{A5.7}$$

From Eq.(A5.6) and Eq.(A5.7), g_2 can be expressed as

$$g_2 = \frac{i_2}{V_s} \cong \frac{g_{m1a} \cdot g_{ds3a} \cdot g_{ds4a}}{g_{ds1a} \cdot g_{m3a}} \tag{A5.8}$$

Thus

$$V_s = \frac{g_{ds1a} \cdot g_{m3a} + g_{ds1a} \cdot g_{ds3a} + g_{ds1a} \cdot g_{ds4a} + g_{ds3a} \cdot g_{ds4a}}{(g_{ds1a} + g_{m1a})(g_{m3a} + g_{ds3a} + g_{ds4a})} V_g \tag{A5.9}$$

because $g_m >> g_{ds}$, then we have

$$V_s \cong \frac{g_{ds1a}}{g_{m1a}} V_g \tag{A5.10}$$

Then, we have

$$(V_{DDb} - V_s) \cdot g_{ds2a} + g_{m2a}(V_{DDb} - V_g) = V_s \cdot (g_1 + g_2) \tag{A5.11}$$

Substituting (A5.5), (A5.8) and (A5.10) into (A5.11) and rearranging gives

$$V_g \cong \frac{g_{m2a} + g_{ds2a}}{g_{m2a} + g_{ds1a}} \cdot V_{DDb} \tag{A5.12}$$

Figure A5.2 illustrate the simplified equivalent small signal model for current mirror circuit part (C_{gs} and C_{gd} are not included)

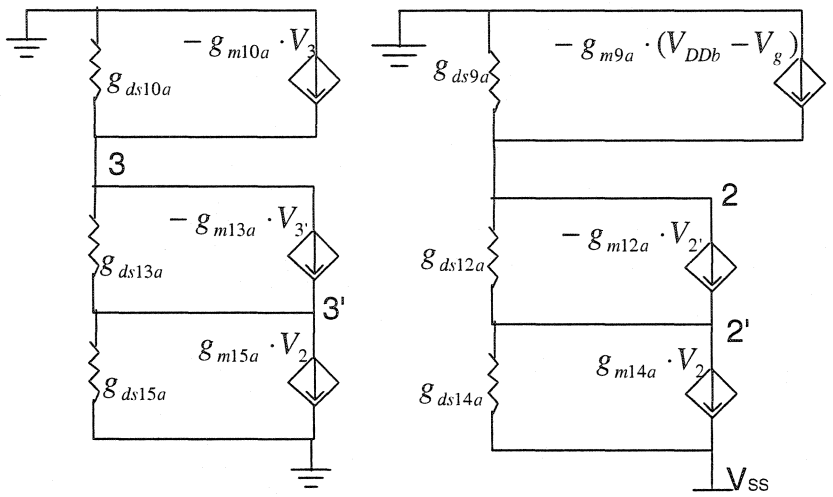

Figure A5.2 Simplified equivalent small signal model for current mirror circuit of OTA

$$(V_2 - V_{2'})\cdot g_{ds12a} - g_{m12a}\cdot V_{2'} = V_{2'}\cdot g_{ds14a} + g_{m14a}\cdot V_2 \tag{A5.13}$$

$$(V_{DDb} - V_2)\cdot g_{ds9a} + g_{m9a}(V_{DDb} - V_g) = V_{2'}\cdot g_{ds14a} + g_{m14a}\cdot V_2 \tag{A5.14}$$

From Eq.(A5.13) and Eq.(A5.14), V_2 can be expressed as

$$V_2 \cong \frac{g_{ds9a}}{2g_{m14a}} V_{DDb} \tag{A5.15}$$

Again, from Figure A5.2, we have equations as follows

$$(V_3 - V_{3'})g_{ds13a} - g_{m13a}V_{3'} = g_{ds15a}V_{3'} + g_{m15a}V_2 \tag{A5.16}$$

$$(0 - V_3)g_{ds10a} - g_{m10a}V_3 = g_{ds15a}V_{3'} + g_{m15a}V_2 \tag{A5.17}$$

Substituting (A5.15) into (A5.16) and (A5.17), then rearrange and use g_{m14a}= g_{m15a}, we then have

$$V_3 \cong -\frac{(g_{m13a} - g_{ds15a})g_{ds9a}}{2g_{m13a}\cdot g_{m10a}} V_{DDb} \cong -\frac{g_{ds9a}}{2g_{m10a}} V_{DDb} \tag{A5.18}$$

$$V_{n1'} = V_{n2'} \cong \frac{g_{ds1}}{g_{m8a}} V_{DDb} \tag{A5.19}$$

Figure A5.3 is a simplified equivalent low frequency and small signal model of the output stage

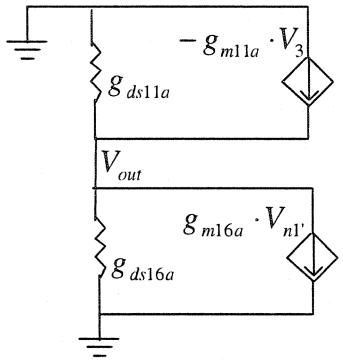

Figure A5.3 Simplified equivalent small signal model for output stage of OTA

From Figure A5.3, we have equation

$$-V_{out} \cdot g_{ds11a} - V_3 \cdot g_{m11a} = V_{out} \cdot g_{ds16a} + V_{n1'} \cdot g_{m16a} \tag{A5.20}$$

After rearranging, V_{out}/V_{DDb} is given by

$$\frac{V_{out}}{V_{DDb}} \cong \frac{-V_3 \cdot g_{m11a} - V_{n1'} \cdot g_{m16a}}{g_{ds11a} + g_{ds16a}} \tag{A5.21}$$

From equation (A5.18), (A5.19) and (A5.21), the equation of V_{out}/V_{DDb} is expressed by

$$\frac{V_{out}}{V_{DDb}} \cong \frac{1}{g_{ds11a} + g_{ds16a}} \left(\frac{g_{m11a} \cdot g_{ds9a}}{2g_{m10a}} - \frac{g_{m16a} \cdot g_{ds1c}}{g_{m8a}} \right) \tag{A5.22}$$

APPENDIX B

Veriloga for Digital Cancellation Circuitry (DCC)

```
module cancellation (din1,din2,rst, dout, clk);
input din1;
input din2;
input rst;
output [3:0] dout;
input clk;


reg  din1_d1,din1_d2;
reg [2:0] din2_d1;
reg [2:0] temp1,temp1d;

reg [3:0] dout;

always @ (posedge clk) begin
  if (rst == 1) begin
    din1_d1 = 0;
    din1_d2 = 0;
    din2_d1 = 0;
    temp1d = 0;
  end
  else begin
    temp1 = {din2,2'b00}-din2_d1;
    dout = din1_d2+temp1d-temp1;
    temp1d = temp1;
    din2_d1 = {din2,2'b00};

    din1_d2 = din1_d1;
    din1_d1 = din1;
 end
end
endmodule
```

APPENDIX C

Schematics of modulators

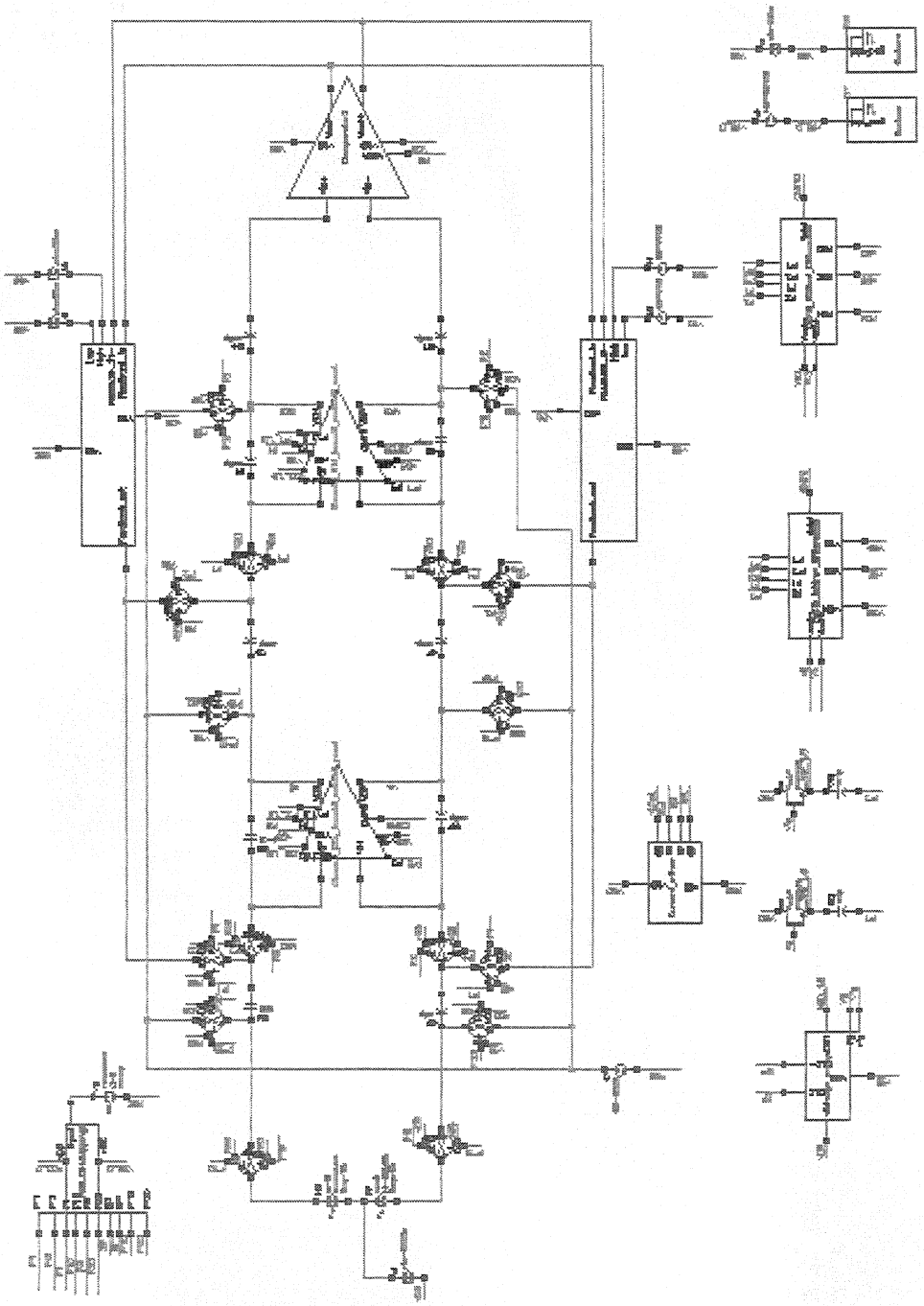

Figure C.1 2nd-order sigma-delta modulator

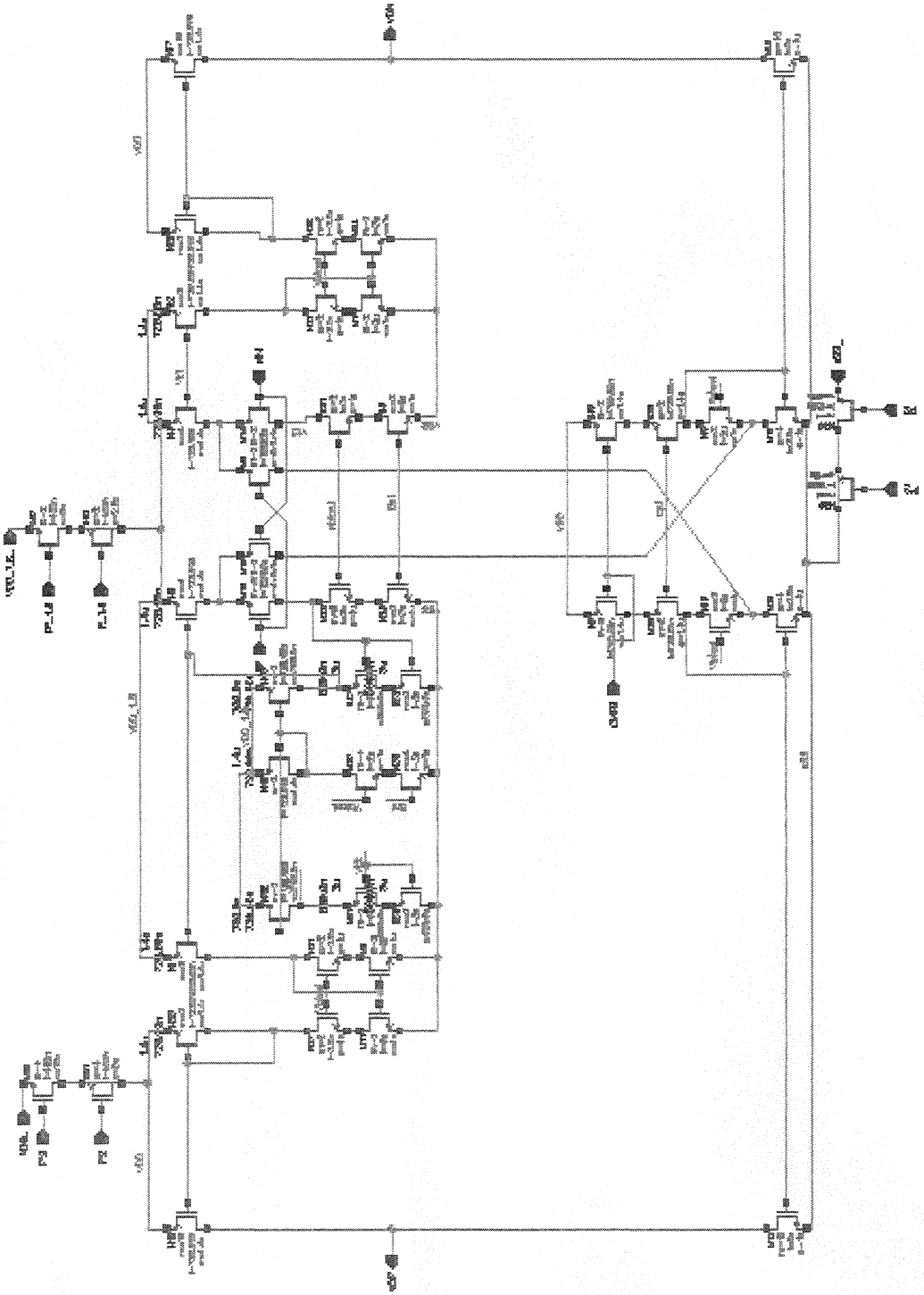

Figure C.2 OTA

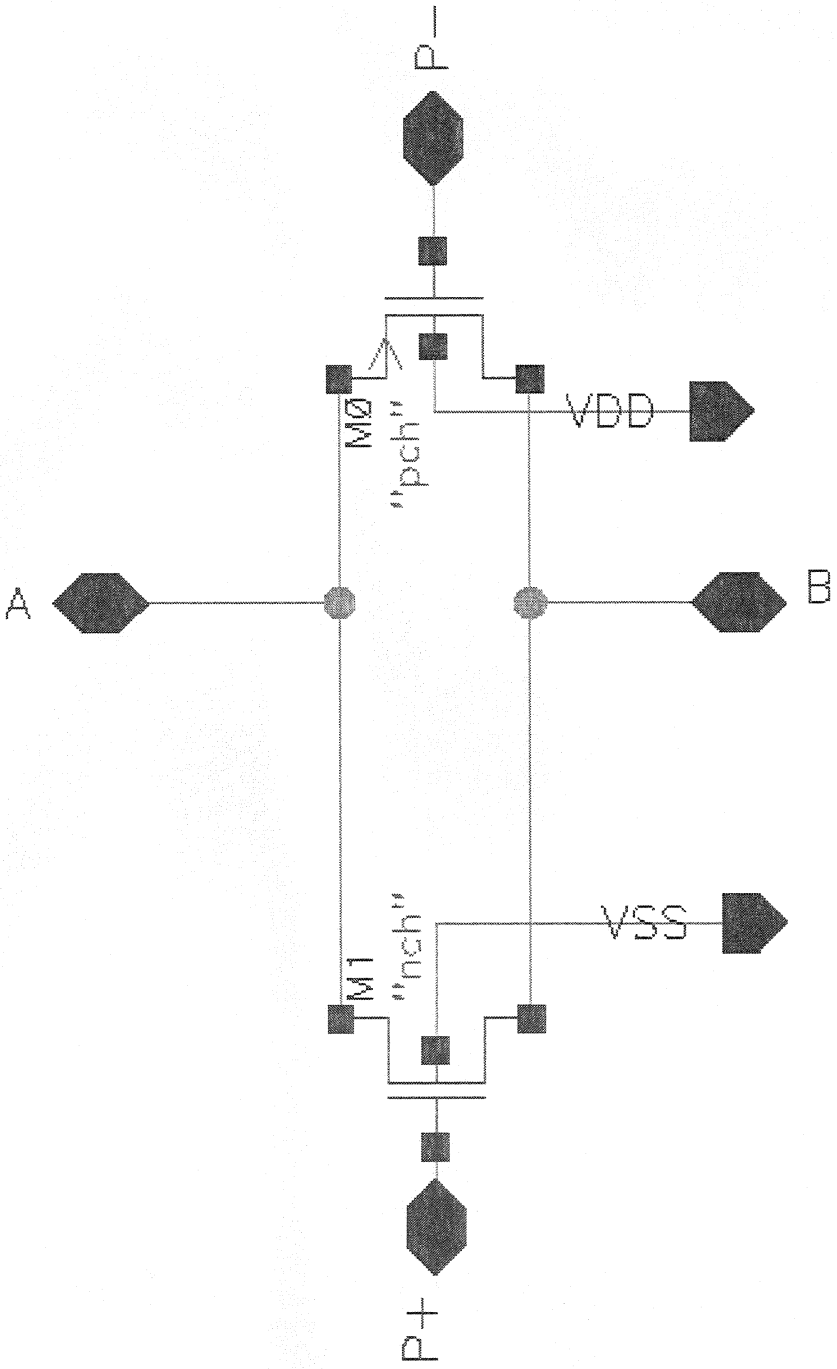

Figure C.3 CMOS switch of switched-capacitor circuit

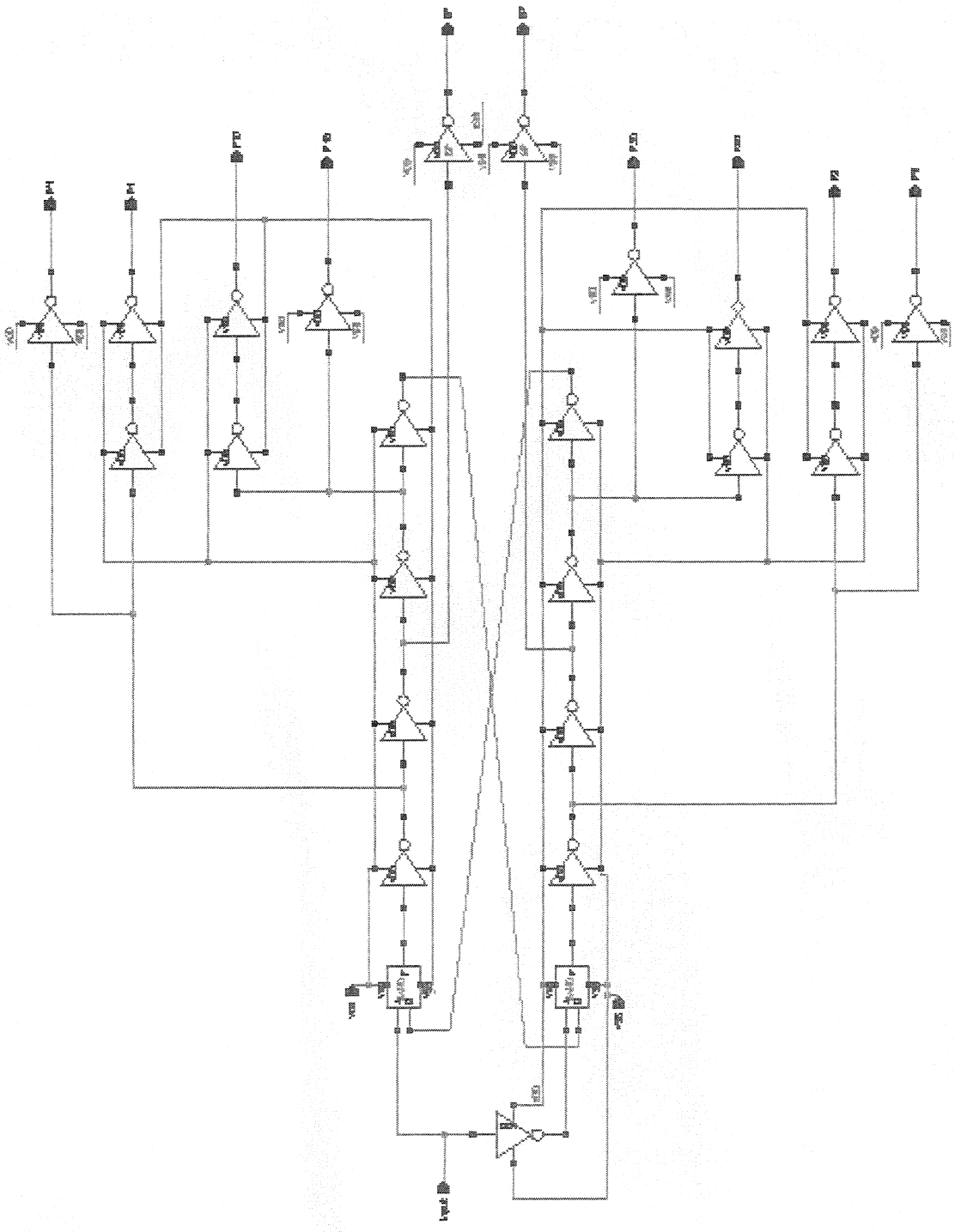

Figure C.4 Generator circuit

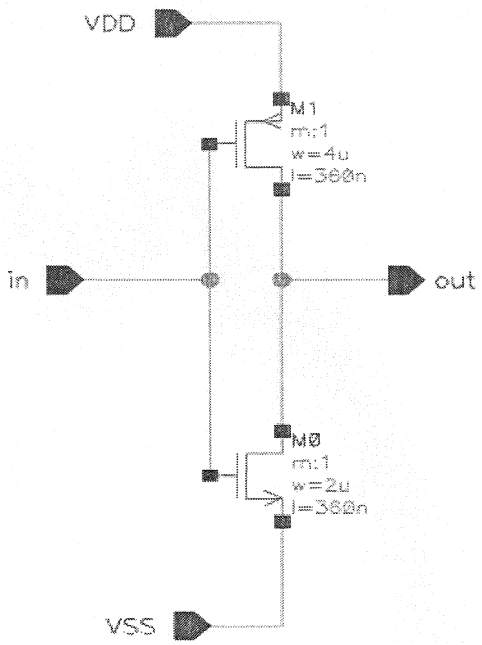

Figure C.5 Inverter in generator (clocks for transmission gates)

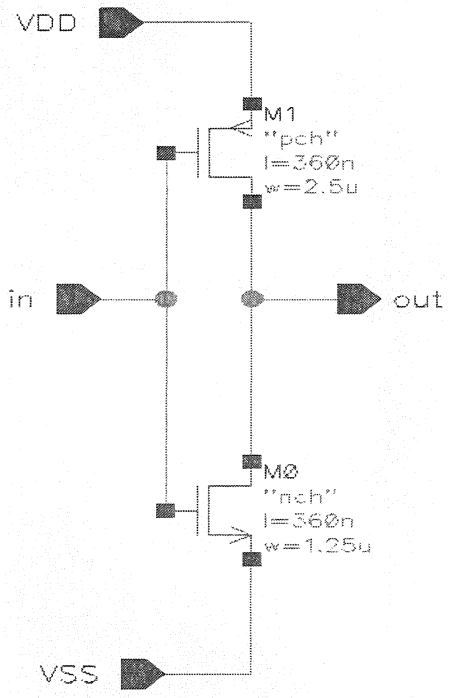

Figure C.6 Inverter in generator (clocks for charge pump)

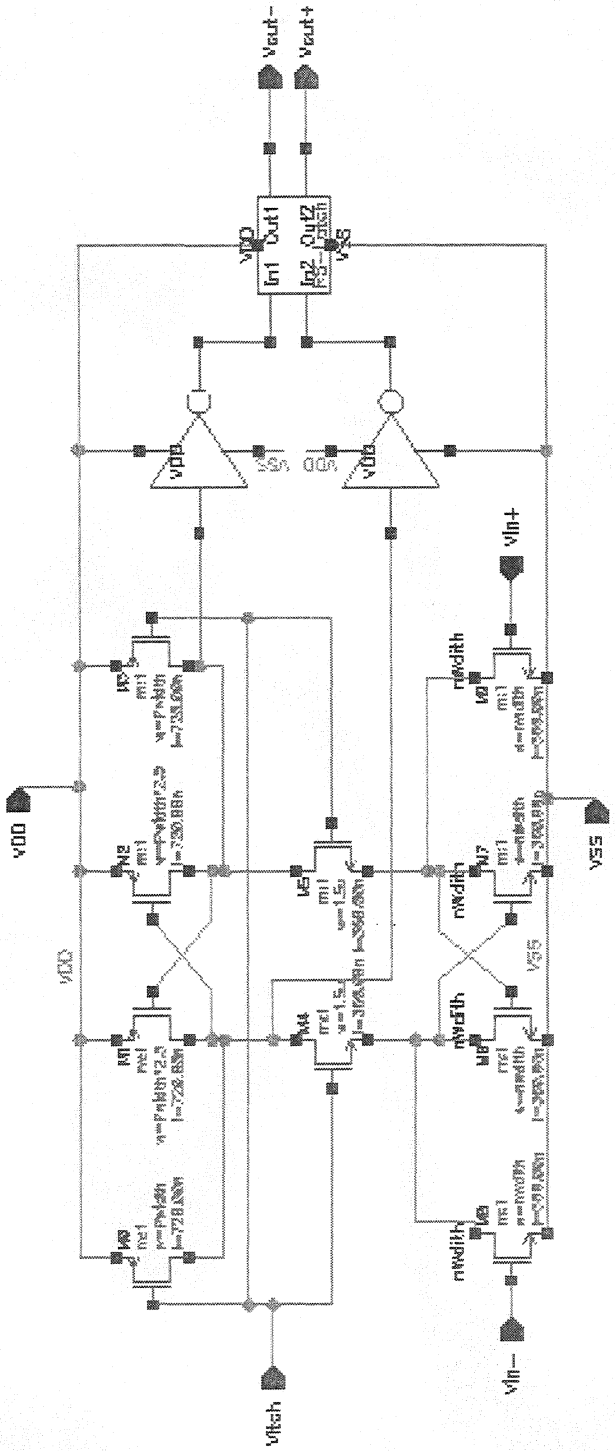

Figure C.7 Comparator

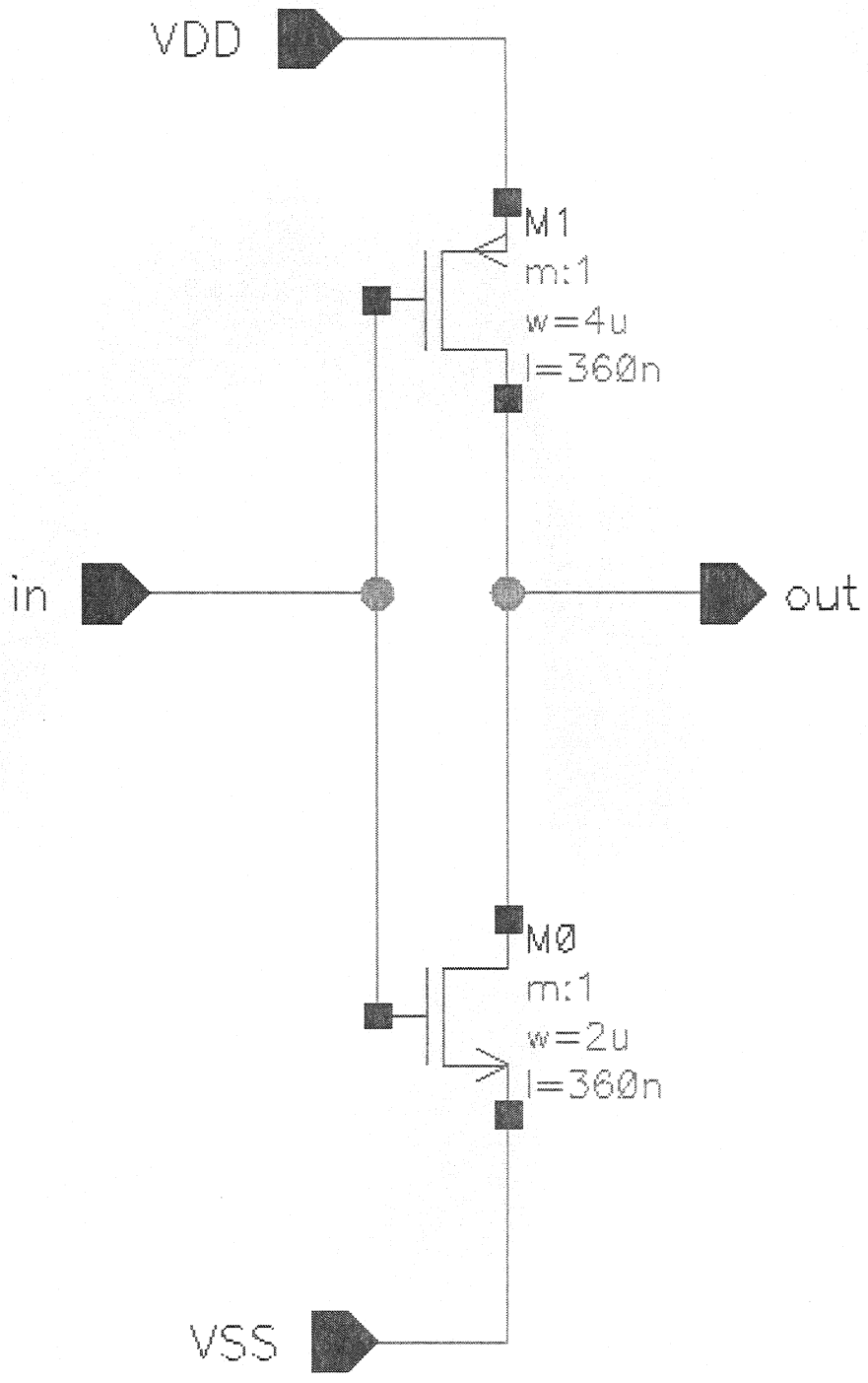

Figure C.8 Inverter in comparator block

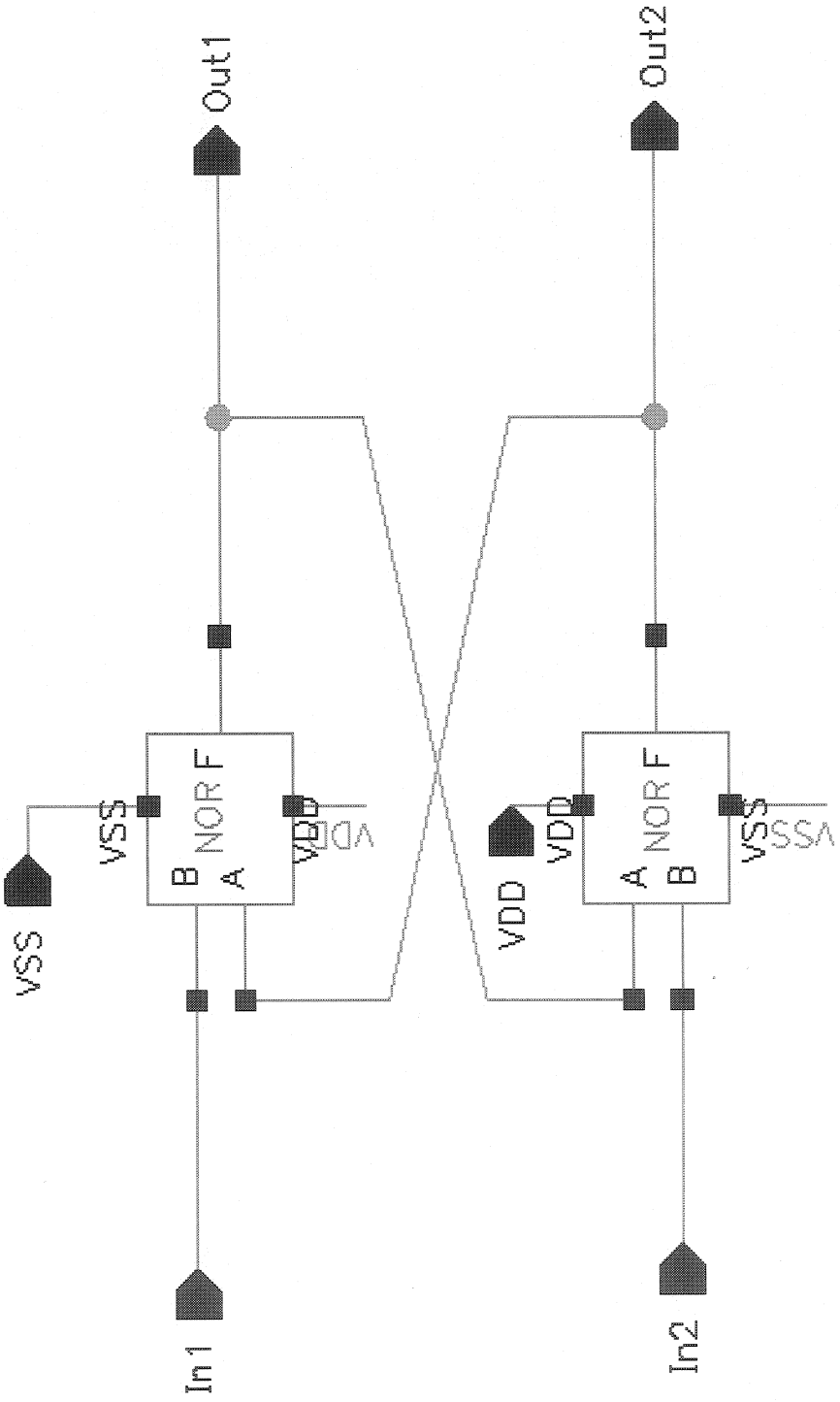

Figure C.9 RS-latch in comparator

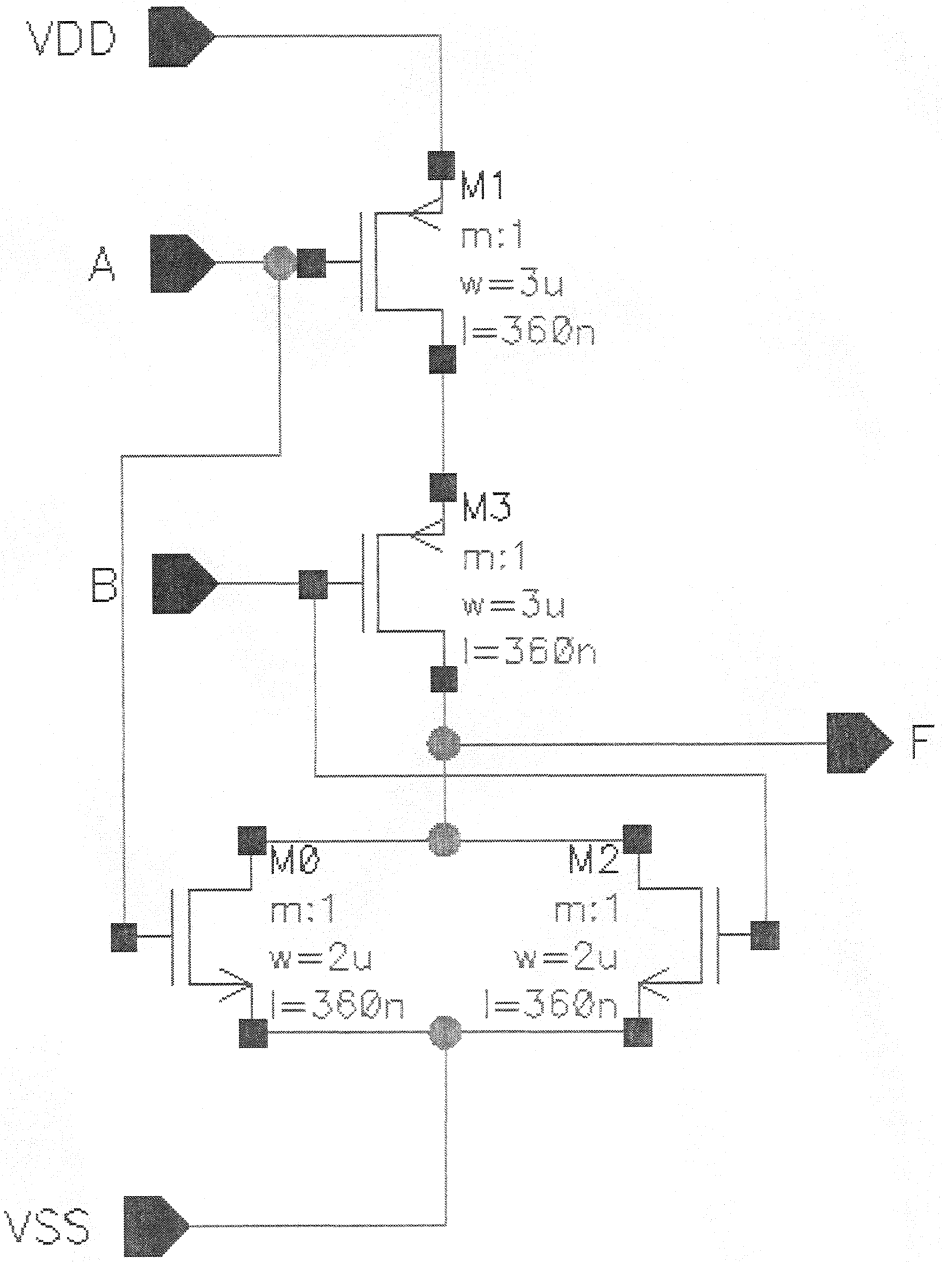

Figure C.10 NOR-gate in RS-latch

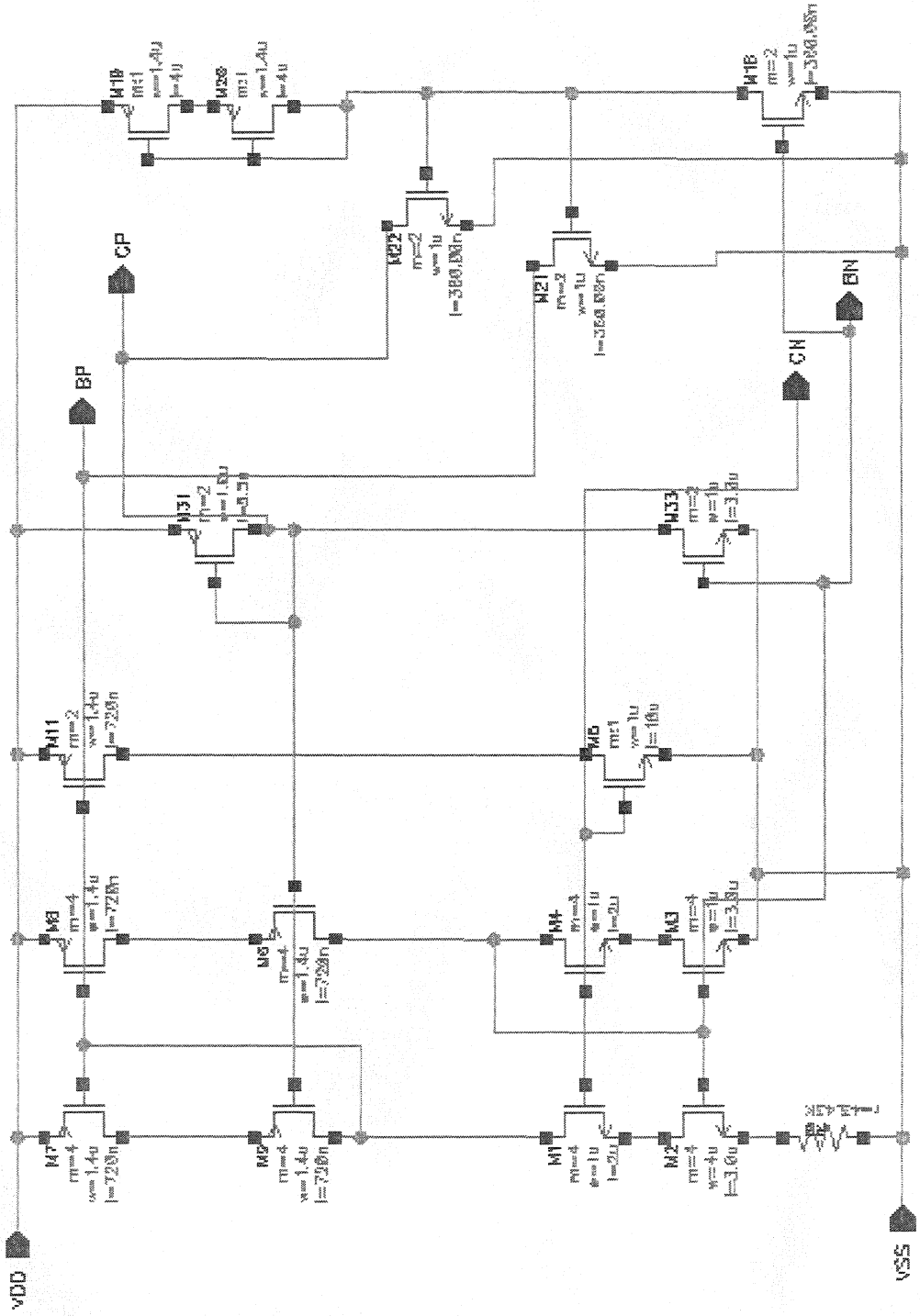

Figure C.11 Bias circuit

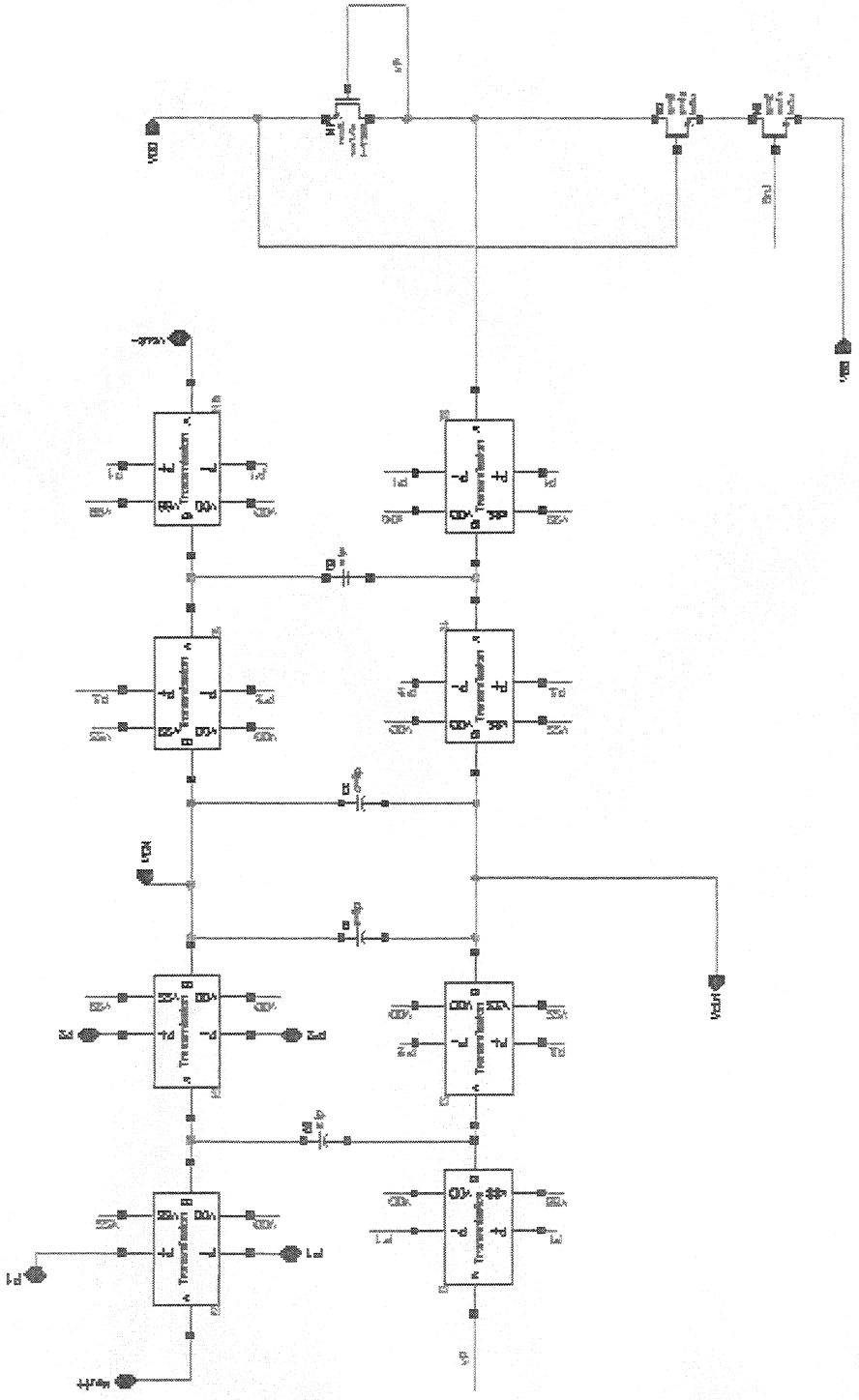

Figure C.12 CMFB circuit

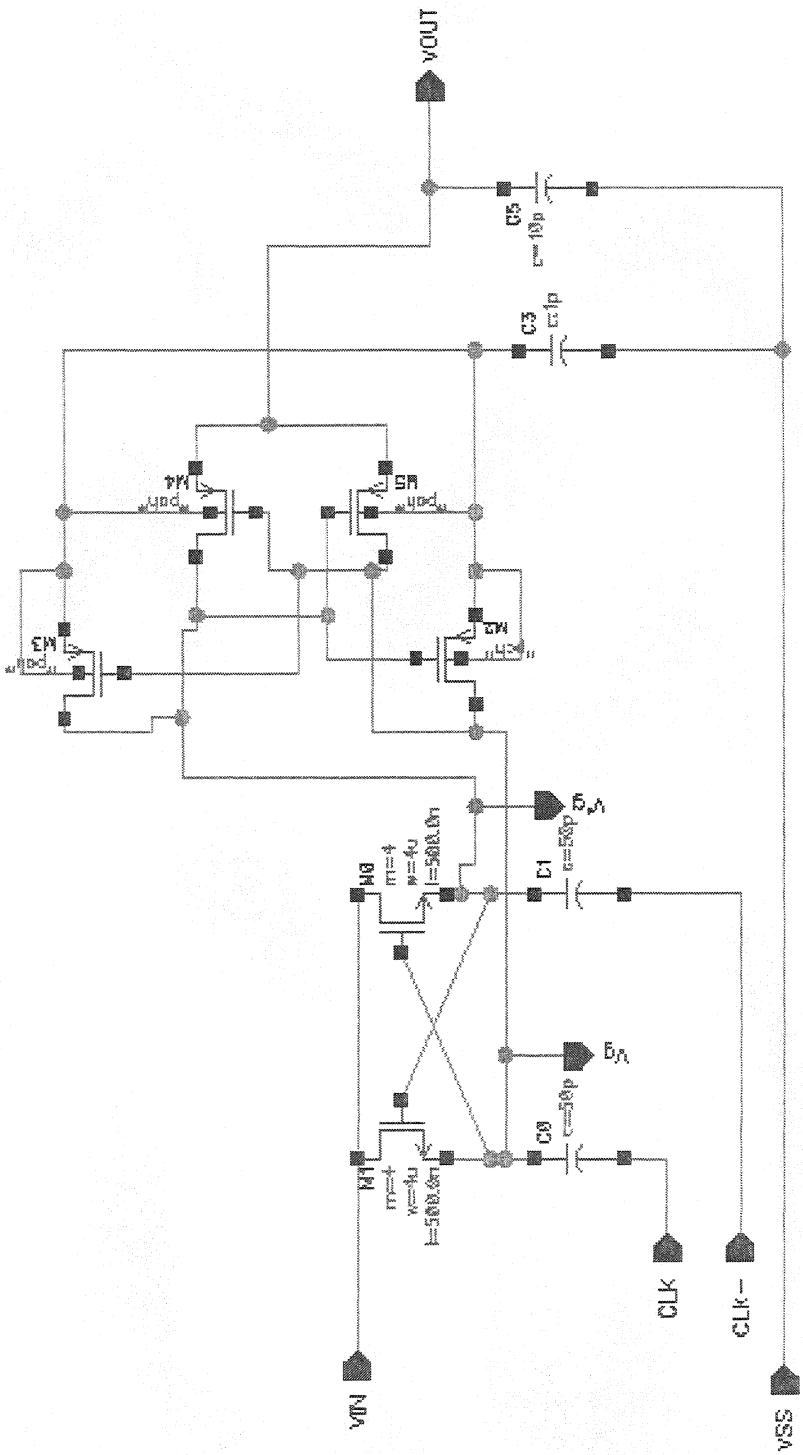

Figure C.13 Voltage doubler

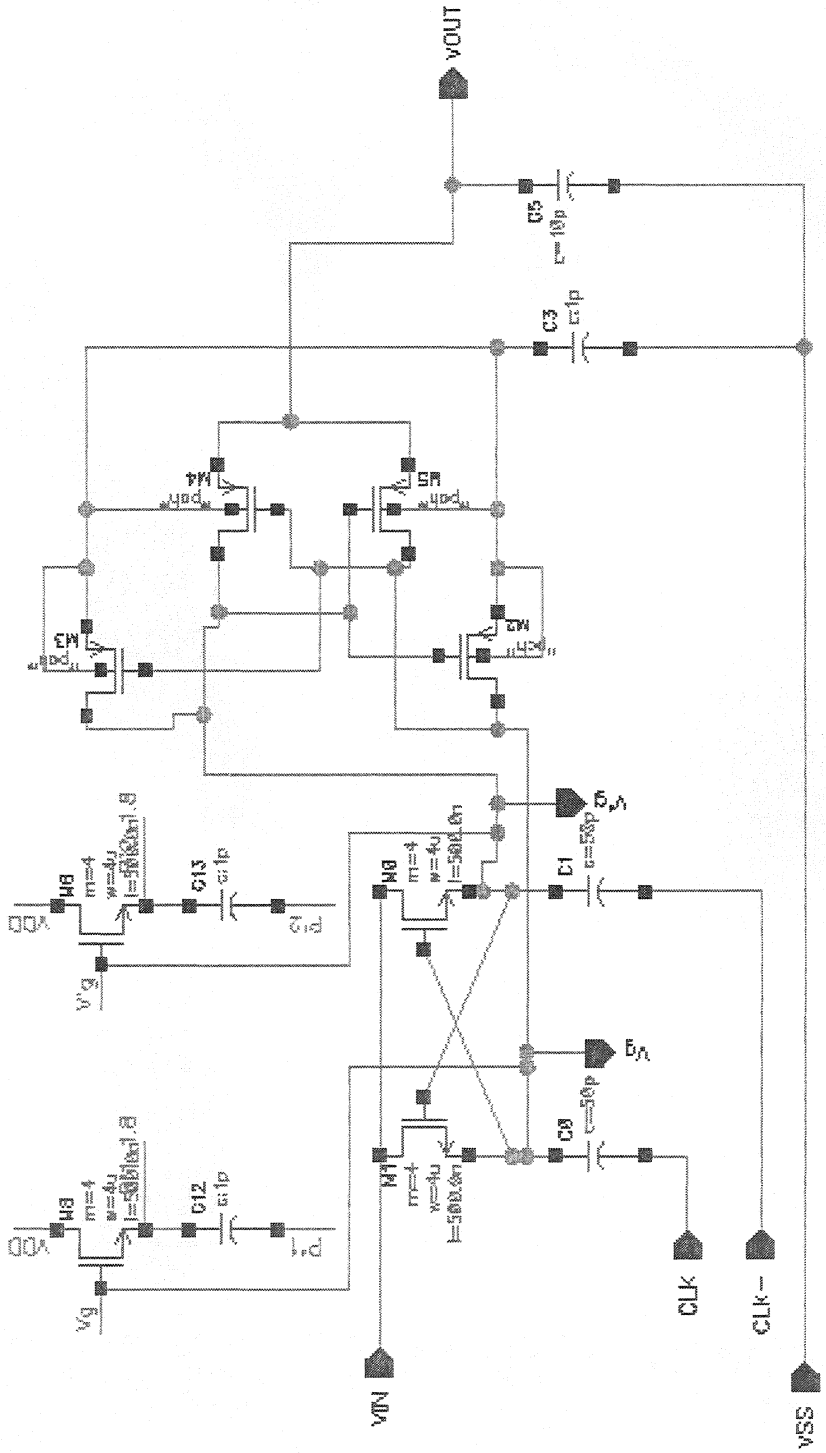

Figure C.14 Voltage doubler with boosted clock circuit

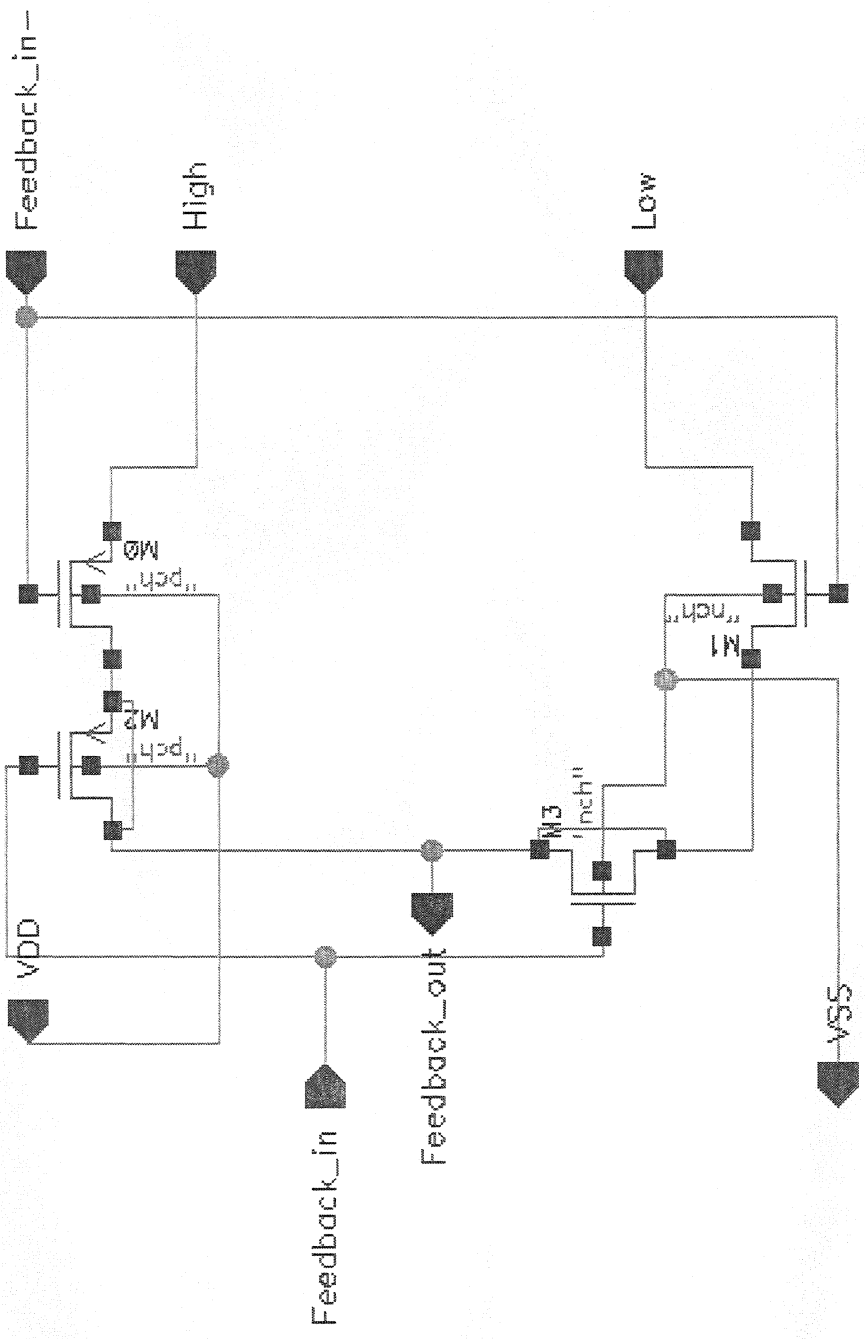

Figure C.15 One-bit DAC

APPENDIX D

Layout of modulators

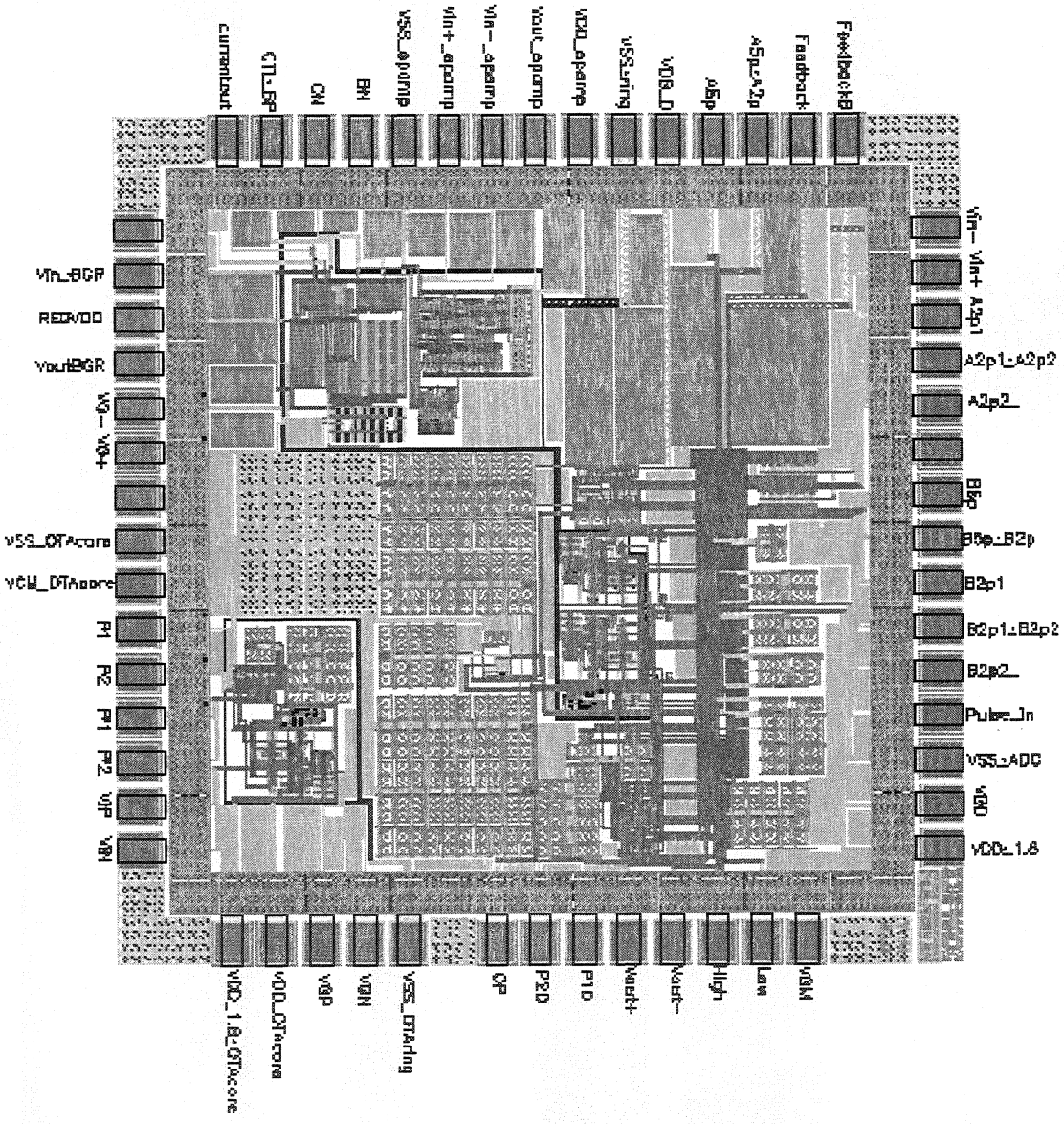

Figure D.1 Chip layout of 2nd-order ΣΔ modulator

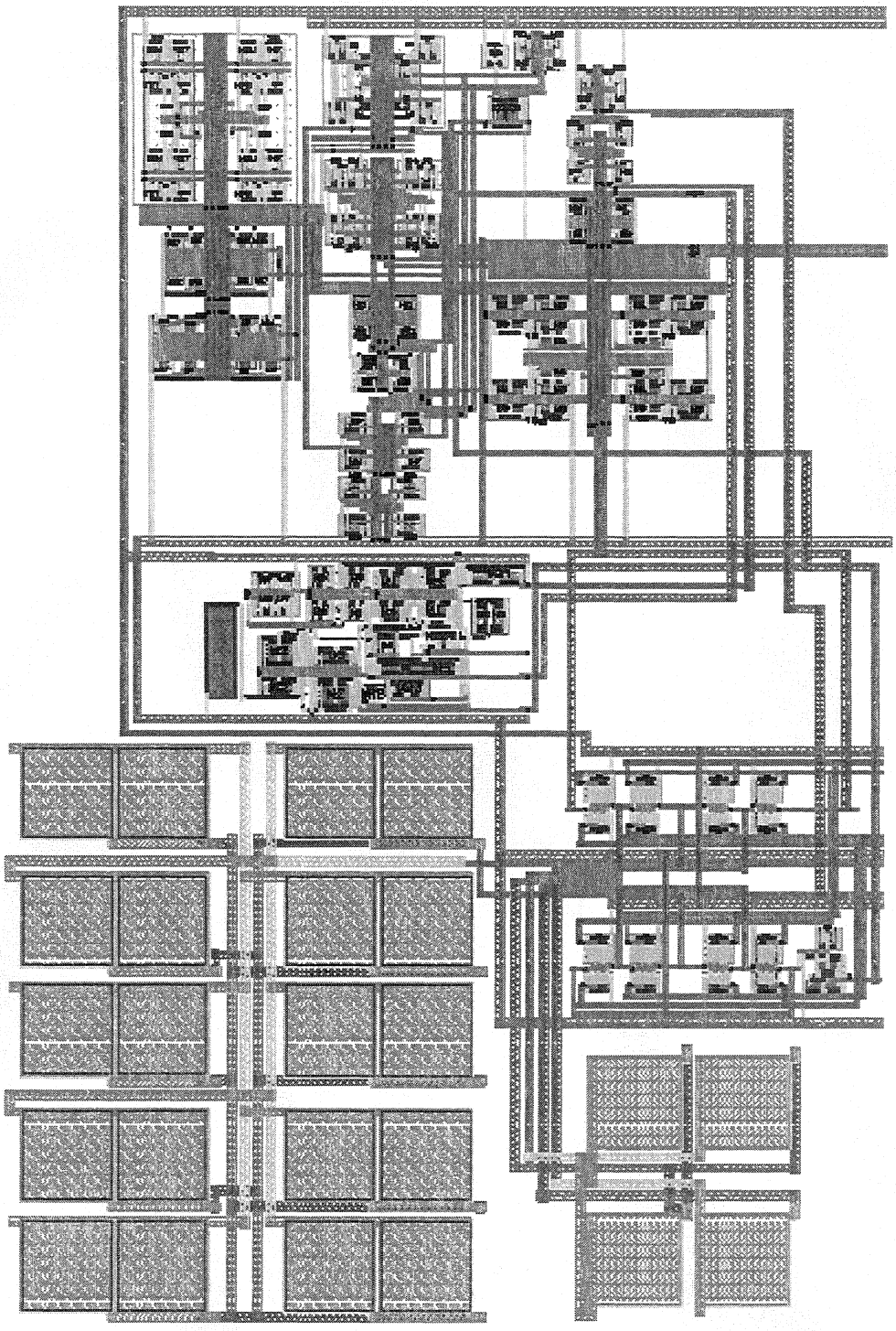

Figure D.2 OTA layout

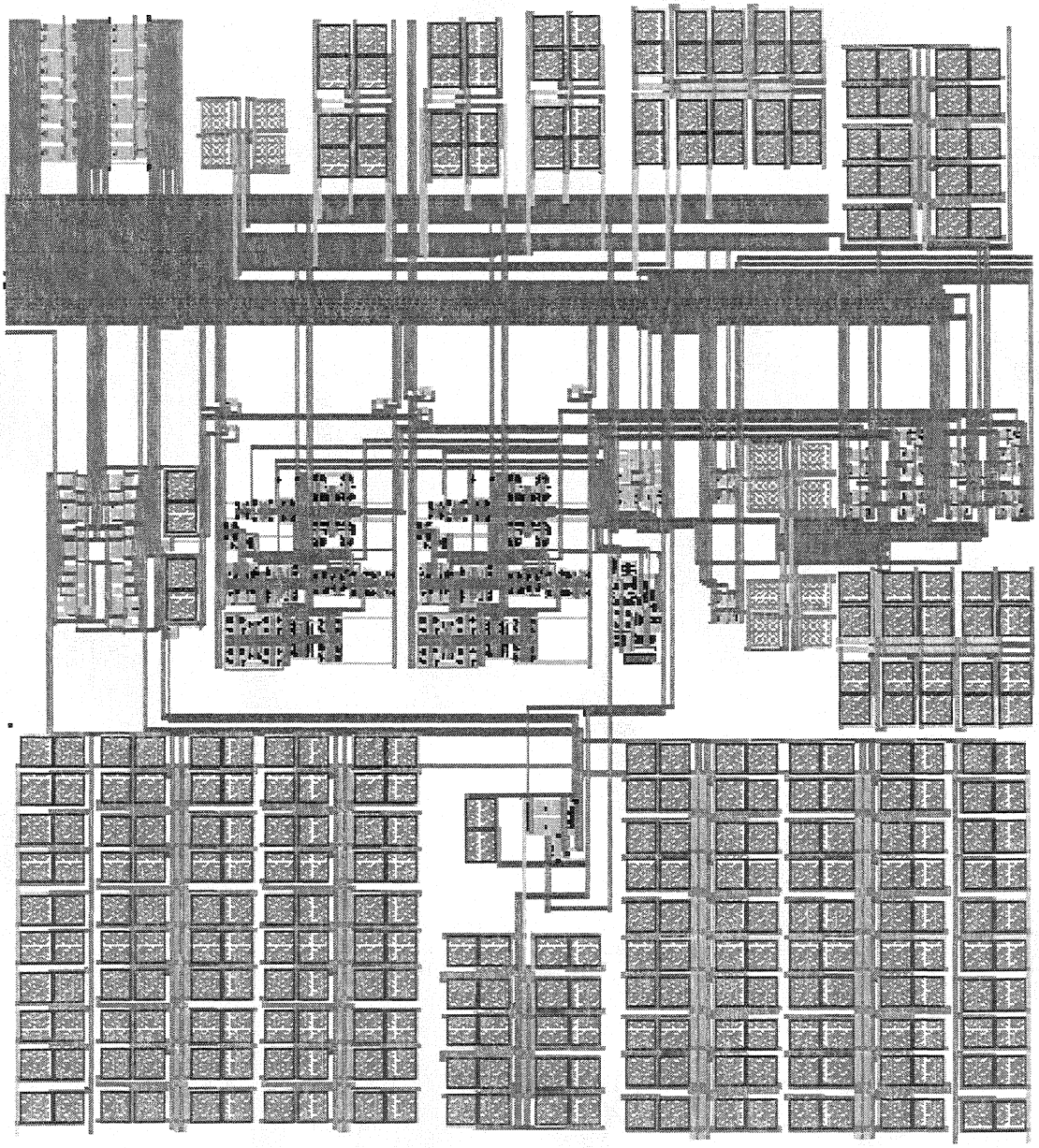

Figure D.3 Second-order ΣΔ modulator layout