Results in Engineering 27 (2025) 105965

Contents lists available at ScienceDirect

Results in Engineering

journal homepage: www.sciencedirect.com/journal/results-in-engineering

Research paper

Reliability analysis based on cascaded-Foster thermal networks for systems-in-package (SiP)

Djallel Eddine Touati [a,*], Aziz Oukaira [b], Mohamed Ali [c], Ahmad Hassan [c], Yvon Savaria [c], Ahmed Lakhssassi [a]

[a] Department of Engineering and Computer Science, University of Quebec in Outaouais, Gatineau, J9A 1L8, QC, Canada
[b] Electrical Engineering Department, Université de Moncton, Moncton, E1A 3E9, NB, Canada
[c] Electrical Engineering Department Polytechnique Montreal, Montreal, H3T 1J4, QC, Canada

ARTICLE INFO

Keywords:
3D SiP
Failure mechanisms
Foster model
Monte-Carlo simulation
Reliability
System-in-package (SiP)

ABSTRACT

This paper presents a fast and comprehensive method for reliability prediction of 3D System-in-Package (3D SiP) technologies. The proposed approach accounts for both critical wear-out failure mechanisms and mission-specific profiles. A novel reliability assessment framework is introduced to address the limitations of traditional methods, which often overlook the variability in failure mechanisms and wear-out rates across different layers within the same mission profile. A key contribution of this work is the coupling between the mission profile and dominant wear-out rates, enabling simultaneous consideration of multiple failure mechanisms, such as those affecting through-silicon vias (TSVs) and solder joints, under real-time operating conditions. The framework offers a multilayer analysis that uses unified units for each layer and incorporates a precise thermal model, enabling the rapid prediction of thermal behavior throughout the system's lifetime. Additionally, the proposed method can be easily integrated into circuit simulators and utilized as a real-time reliability estimator. This capability enables researchers and engineers to further investigate interactions between failure mechanisms across different layers of the SiP under realistic and dynamic operational conditions. By identifying the dominant failure mechanism in each layer, the method supports early-stage design decisions to mitigate potential reliability issues. The reliability estimation process involves selecting the mechanism with the shortest predicted lifespan for each layer and constructing the overall reliability curve using a series configuration of the reliability block diagram. Long-term mission profiles are translated into thermal loads through a cascaded Foster thermal network, with Monte Carlo simulations applied to determine the system's failure distribution.

1. Introduction

System-in-package (SiP) technology allows the assembly of multiple dies in a single package. Integration is best achieved with 3-dimensional stacked dies connected using Through-Silicon Vias (TSVs) [1]. Their features make them suitable for applications that require compact modules integrating mixed-signal circuits and passive components, such as mobile phones and versatile sensor interfaces [2].

However, satisfying the SiP design specifications is challenging despite their promising features, especially for applications that require high reliability and lower cost, geometrical scaling, high power density, and the operation of multiple dies at high frequencies with varying power consumption significantly affect the reliability of SiPs. Thermal gradients primarily cause these issues among layers and temperature fluctuations. Therefore, estimating the lifetime of SiPs has become a significant concern in designing these complex systems with effective target lifetimes. Accordingly, enhancing tools that analyze reliability in a SiP's design phase is mandatory, mainly when it works in harsh operating conditions.

The failure rate of an electronic product can be visualized by the so-called Bathtub Curve (BC). This graphical representation is made up of three stages: a decreasing failure rate results in the so-called infant mortality, a useful life represented by a constant failure rate caused by random failures, and a late lifetime behavior described by an increasing failure rate due to the wear-out processes [3]. Since wear-out plays a crucial role in determining an electronic product's reliability and sustainability during long-term operation [4], this is the main concern of this paper.

Several studies have analyzed the failure mechanisms of 3D stacks to improve their reliability [5–9,38]. It has been reported that solder joints

* Corresponding author.
E-mail address: toud05@uqo.ca (D.E. Touati).

https://doi.org/10.1016/j.rineng.2025.105965
Received 9 January 2025; Received in revised form 5 June 2025; Accepted 23 June 2025
Available online 27 June 2025
2590-1230/© 2025 The Authors. Published by Elsevier B.V. This is an open access article under the CC BY license (http://creativecommons.org/licenses/by/4.0/).

may cause reliability issues, and the selection of solder joints' metallurgy type plays a decisive role in improving the lifetime of the package. The impact of solder joints on reliability has been investigated in several previous research works [9–11,39].

In [9], simulations with ANSYS/LS-DYNA were carried out to predict the transient mechanical behavior of solder to evaluate the drop impact solder reliability of 3D-Integrated Circuits (ICs). Authors in [10] assessed the effects of thermal cycling on the lifespan of solder joints. However, tests based on drop impact reliability are not suitable for systems that are subjected to high temperature fluctuations in actual field operation, since they cannot predict what the system will experience in real-life operation [27–30].

TSVs play a key role in 3D packaging since it offers high-density interconnections. However, it comes with reliability challenges [11,12]. Finite Element Analysis (FEA) is used to investigate the effect of temperature cycling on 3D TSV. Work reported in [11] showed that the most stress is located on the outermost corner of the TSV, which causes serious reliability issues for the package. New studies propose thermal cycling in a based model to enhance the reliability of 3D ICs [12]. It has been shown in [13] that electromigration failure in TSVs is a significant reliability concern in 3D IC packages.

In addition, the impact of jumps in junction temperature (thermal cycling) on reliability lifetime was investigated in [14,15]. In Yang et al. [14] a one-year mission profile was converted into thermal load. Then Monte-Carlo simulation was applied to estimate the failure probability of a photovoltaic (PV) inverter. To evaluate the reliability of the DC-to-DC converter, authors in [15] use Monte-Carlo simulations to assess uncertainties induced by the mission profile and statistical parameters of the lifetime model. Although these two studies are based on mission profile and distributed failure rate, they consider only one failure caused by thermal cycling.

Various failure mechanisms in either solder or TSV, caused by high heat flux produced at dies, threaten the reliability of 3D SiP. It is important to develop a new lifetime model that considers various failure mechanisms at critical layers of the 3D SiP and carries out a statistical analysis showing the impact of each failure mechanism on the reliability of the 3D SiP.

Despite significant advancements in reliability analysis for 3D ICs and SiPs, most existing studies focus on individual failure mechanisms, often limited to thermal cycling effects, without addressing the concurrent and compound impact of multiple mechanisms such as electromigration in TSVs and fatigue in solder joints. Moreover, there remains a lack of unified, real-time reliability assessment frameworks that can simulate actual operating conditions by tightly coupling mission profiles with layer-specific wear-out rates. Current approaches also often fall short in capturing the complex interactions between temperature dynamics, mechanical stress, and electrical load across heterogeneous layers. To fill this research gap, this paper proposes a novel, fast, and comprehensive reliability prediction method for 3D SiPs that integrates multiple critical wear-out mechanisms, such as those affecting TSVs and solder joints, within a unified framework. The key contributions of this work are as follows: Coupling of mission profiles and dominant wear-out mechanisms: The method introduces a direct link between real-world mission profiles and the dominant failure mechanisms in each layer of the SiP, enabling simultaneous consideration of multiple, coexisting reliability threats under actual operating conditions. Layer-specific reliability modeling: The framework identifies the most vulnerable layers in the system and computes their wear-out rates based on realistic thermal behavior, using unified units and modeling approaches for consistent cross-layer analysis. Integration into circuit simulation environments: The proposed method can be easily incorporated into standard circuit simulation tools and employed as a real-time temperature estimator, facilitating deeper analysis of interaction effects between different failure mechanisms during actual use conditions. Statistical reliability estimation through Monte Carlo simulation: The method converts year-long mission profiles into thermal loads via a cascaded Foster thermal network, then performs Monte Carlo simulations to estimate the statistical distribution of failures based on the weakest link (minimum lifespan) in a reliability block diagram.

This paper proposes a novel 3D SiP reliability assessment method to address the abovementioned challenges. Starting from the mission profile for one year of the system studied, the proposed approach converts it into thermal load using the thermal circuit-based model in reasonable simulation time. Then, Monte Carlo simulations are performed to obtain statistical parameters that combine the lifetime distributions of failure mechanisms in TSV and solder joints.

This paper introduces a fast reliability prediction method for 3D System-in-Package (3D SiP) that considers critical wear-out failure mechanisms and mission profiles. This method mitigates the lack of coupling between the mission profile and the dominant wear-out rate for each layer determining the reliability of 3D SiPs. The paper will also propose an effective and comprehensive framework to analyze multi-layered SiP reliability over their lifetime. This framework adopts unified units for each layer in the system, leveraging an accurate thermal model to facilitate rapid predictions of SiP thermal behavior. The method identifies the dominant failure mechanism in each layer to aid designers in preemptively addressing damages caused by failures early in the design process. It relies on selecting the mechanism that causes the minimum lifespan for each layer and plotting the reliability curve according to the reliability block diagram's series configuration. The long-term mission profile is converted to thermal load using a cascaded Foster thermal network, followed by Monte-Carlo simulations to determine the overall failure distribution.

The rest of this paper is organized as follows: Section 2 describes a framework for evaluating the proposed SiP reliability metric, including converting a mission profile into thermal load and reliability modeling. Section 3 presents simulation results and a discussion. Finally, Section 4 presents the conclusions.

2. The proposed reliability analysis approach

Reliability analysis and lifetime prediction of a 3D SiP requires detailed knowledge of the structure of the SiP and the used thermal model's ability to predict the dissipated power and estimate the transient temperature of the layers based on a given power profile. In addition, physical lifetime models are needed to describe the lifespan due to various failure mechanisms in fragile parts such as TSVs and solders.

We present an approach shown in Fig. 1 to predict the lifespan and assess the reliability of a 3D SiP.

The proposed approach starts by defining the mission profile of the studied 3D SiP shown in Fig. 2. In the structure depicted in Fig. 2, the dissipated power of each chip was determined and stored in the lookup table (LUT). The recorded data are then fed into the thermal circuit to predict the long-term thermal loads of the layers. The thermal loads obtained in the previous step (phase 1) are irregular. However, failure mechanism models, particularly thermal cycling, are related to several static parameters, such as the number of cycles at a certain amplitude. To obtain these parameters, the Rainflow algorithm [17,36] is applied to thermal loads. The Rainflow-counting algorithm, developed by Tatsuo Endo and Masanori Matsuishi in 1968 [16], is a widely recognized method in fatigue analysis. It is used to convert a load sequence of varying stress into a set of constant amplitude stress reversals, allowing the estimation of fatigue damage and the life of materials under cyclic load; thus, the layers' temperature cycles and associated numbers can be determined. The defined loads are then used as input data to predict the TSV and solder failure models. Therefore, the impact of temperature on TSV and solder lifetime can be determined. This paper assumes that failure mechanisms in TSVs or solders follow Weibull distributions [18]. The Weibull model describes the mean time to failure of each layer. In the last phase, the mean time to failure distributions obtained in the previous step are unified by Monte Carlo simulations.

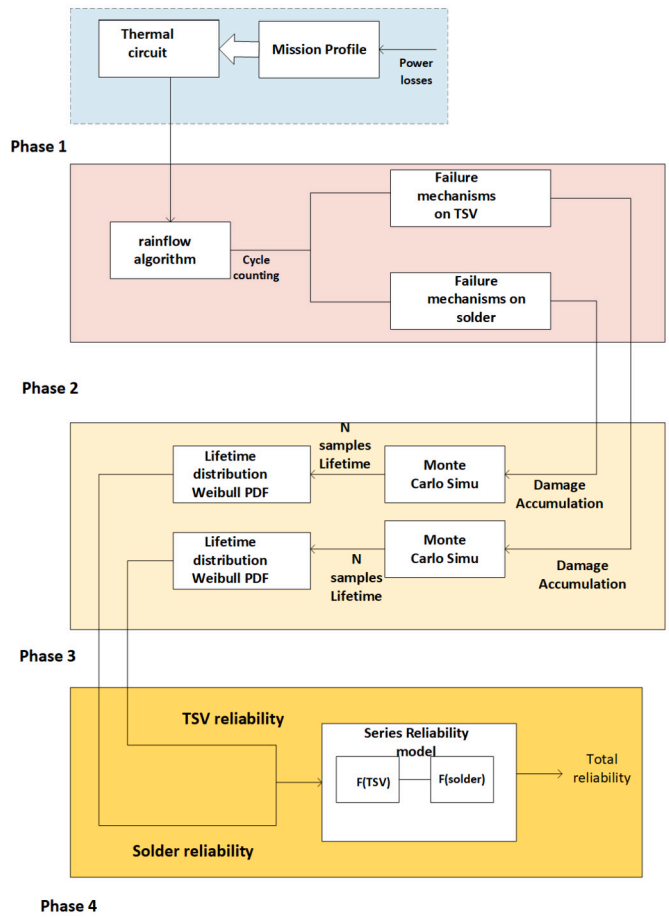

Fig. 1. Steps of the proposed framework for reliability assessment of SiPs.

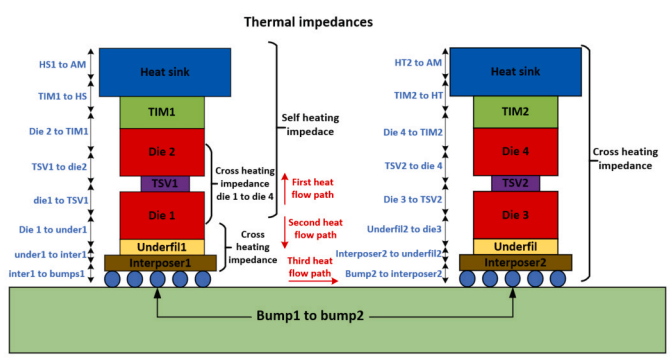

Fig. 2. Structure of the studied SiP and its thermal impedance configuration.

2.1. Prediction of the thermal behavior of SiP

The structure of the studied 3D SiP package is shown in 2. It comprises two sets of vertically stacked dies and various layers to ensure the connection between the dies and the reliability of the package. Two mounted heat sinks cool the package. The heat flux generated by dies due to power losses flows through different thermal paths. It causes heating of all layers contained in the package and thermal gradients due to various layers' thermal conductivity and capacitance. To estimate the temperature of target layers, we propose a model shown in Fig. 3. The transient thermal impedance between two consecutive layers is modeled as a lumped RC Foster circuit. The power losses from the dies are used as inputs to the thermal model, and the response to these inputs represents the transient thermal impedance between two layers, as described by the following equation.

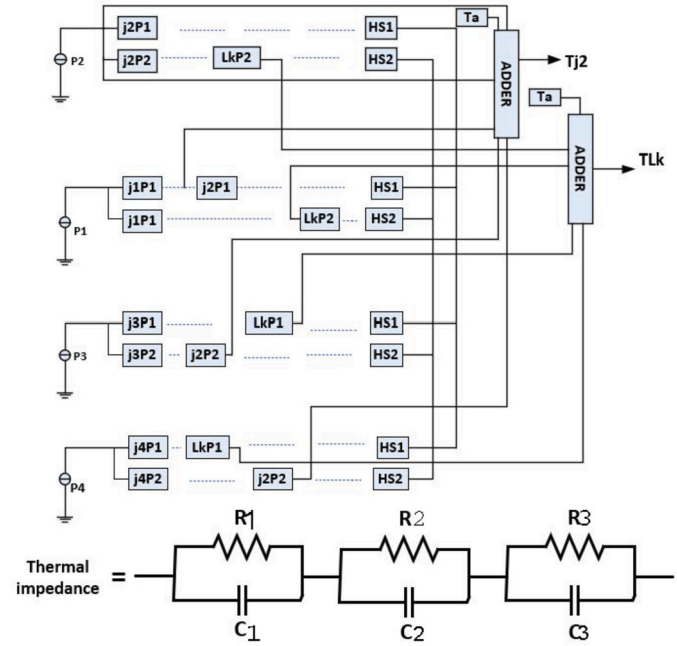

Fig. 3. Multi-layered thermal circuit.

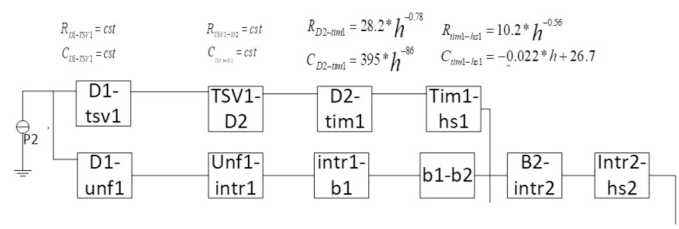

Fig. 4. Thermal branch with *htc* boundary conditions.

$$Z_{thL1-L2}(t) = \frac{T_{L1} - T_{L2}}{P_{loss}} = \sum_{k=1}^{3} R_k (1 - e^{\frac{t}{\tau_k)}} \quad (1)$$

Where $Z_{thL1-L2}(t)$ is the thermal impedance between layer 1 and 2, T_{L1} and T_{L2} are the transient temperatures of layer 1 and 2, respectively, P_{loss} describes the power dissipation in dies, τ_k is the thermal time constant of $k^t h$ term, and R_k is the thermal resistance between layer 1 and 2.

However, in real life, the SiP may experience various external conditions, such as nonlinear cooling techniques and changes in ambient temperature. These conditions are considered boundary conditions and profoundly impact the model's accuracy [32] and the reliability of the SiP, as we will present in the reported results. The RC thermal parameters are derived and expressed as a function of boundary conditions to ensure prediction accuracy. Fig. 4 shows the case of one thermal branch in which the RC thermal parameters have been expressed as a function of the heat transfer coefficient (htc) [35]. In Fig. 4, the term 'cst' denotes a scenario where the thermal resistance and capacitance remain constant, irrespective of variations in the heat transfer coefficient (htc), which characterizes the nonlinear cooling of the package and is represented as h for conciseness, acknowledging space limitations.

The transient thermal behavior of each layer in the studied package was extracted from COMSOL Multiphysics® by fitting Equation (1). To extract transient impedance, the RC thermal parameters should be obtained first. Fig. 5 shows the transient temperature performance of our proposed model implemented in Simulink® and the Finite Element Method (FEM) in the COMSOL tool. The transient temperature curve estimation of die 2 for different levels of loss power shows a good agreement. It is worth mentioning that the FEM simulation in COMSOL took

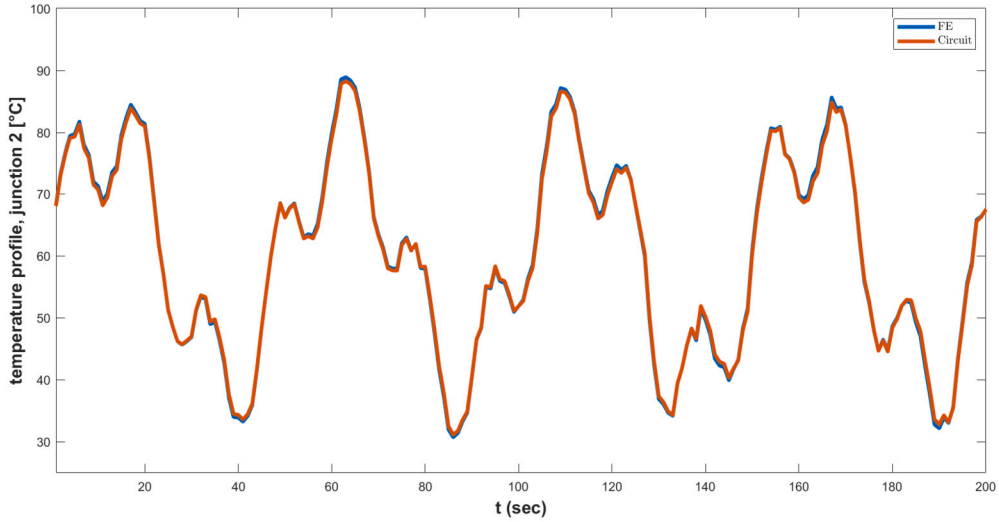

Fig. 5. FEM validation of the proposed thermal circuit.

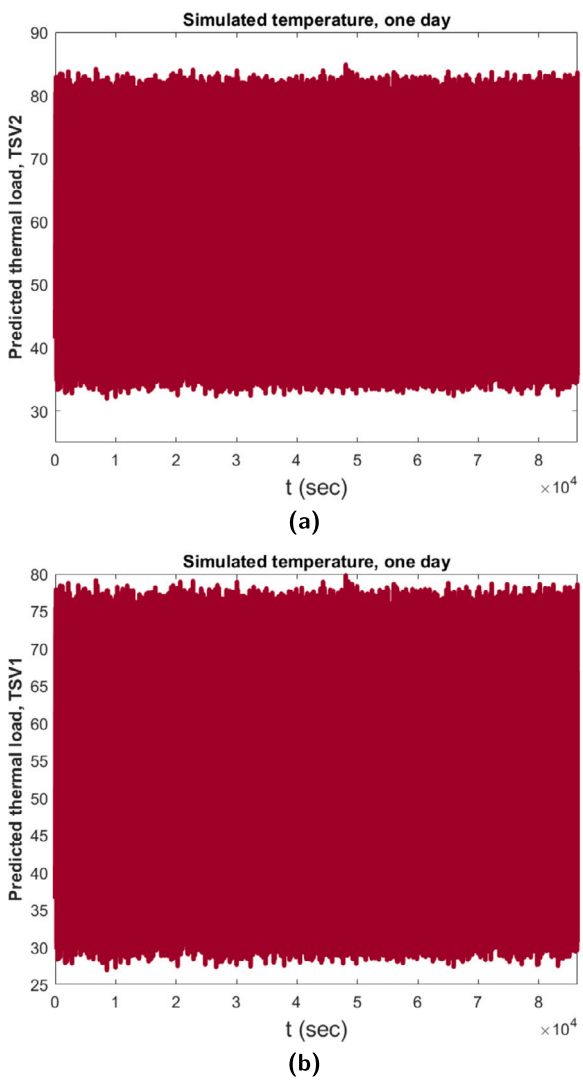

Fig. 6. Thermal load over time : (a) TSV2, and (b) TSV1.

about 3 hours to converge and required a huge amount of memory, up to 3.4 GB (proportional to the simulated time, which is relatively short here).

In contrast, the proposed model took about 4 seconds to evaluate and consumed only 2.3 MB. These considerable savings in computing time and memory are crucial when considering the package's long-term thermal behavior prediction. Also, Fig. 5 shows that the layer undergoes thermal cycling, and peaking can lead to serious long-term reliability issues.

In the proposed approach, knowledge of the mission profile of the studied package is required throughout the entire operation. In this respect, an offline calculation of the dissipated power of each chip was performed to create a look-up table (LUT). Then, the dissipated power values during 12 months of operation were injected into the thermal circuit to be translated into thermal profiles of the layers. Fig. 6.a, and Fig. 6.b show the thermal loading profiles of TSV2 and TSV1 for a specific operating time duration. To provide a clearer view of the data, Fig. 7.a and Fig. 7.b zoom in on a 30-second segment of these profiles, highlighting the temporal variations within this narrower time frame.

2.2. Cycle counting

By applying the mission profile to the thermal circuit in the previous step, the temperature of junctions, TSVs, and solder joints can be obtained. However, the temperature profiles are variable and irregular due to the package's operating conditions, as seen in Fig. 4, and 5. In this case, it is desirable to have a cycle-counting algorithm to identify statistical parameters of the irregular temperature-load profiles. Thus, relevant information such as the number of cycles, mean cycle temperature T_m and amplitude ΔT can be obtained and applied to selected failure mechanism models of solders and TSVs. We use the Rainflow-counting algorithm to divide the thermal load profiles of solder joints and TSVs into regular thermal cycles. Fig. 8 shows the application of the Rainflow method to the temperature load profile shown in Fig. 6.

2.3. SiP failure mechanisms

Empirical models have been applied to predict the layers' Mean time to failure (MTTF) for a one-year mission profile. According to Ikonen et al. [31], these models are easy to apply because they do not require prior knowledge of the semiconductor material's physical properties. 3D SiP is considered one of the most vulnerable semiconductor packaging types. Its layers are made with materials of different electrical and thermal properties assembled to form various failure mechanisms. However, some failures are more dominant than others over particular layers. As in Arrhenius's equation, semiconductor-based packages' reliability and time to failure are tightly linked to operating temperature.

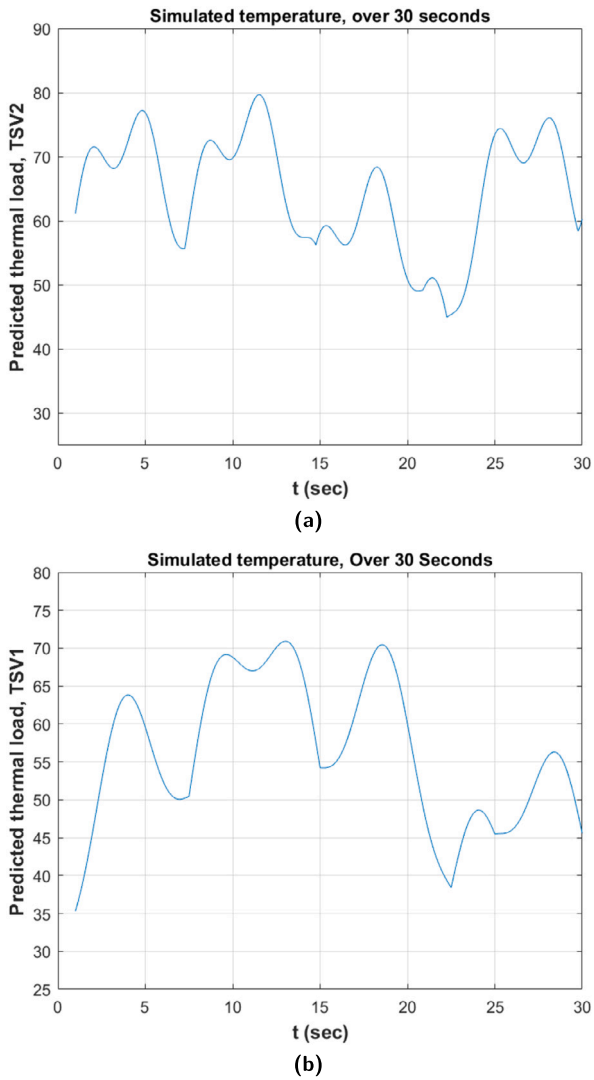

Fig. 7. Thermal load over 30 seconds: (a) TSV2, and (b) TSV1.

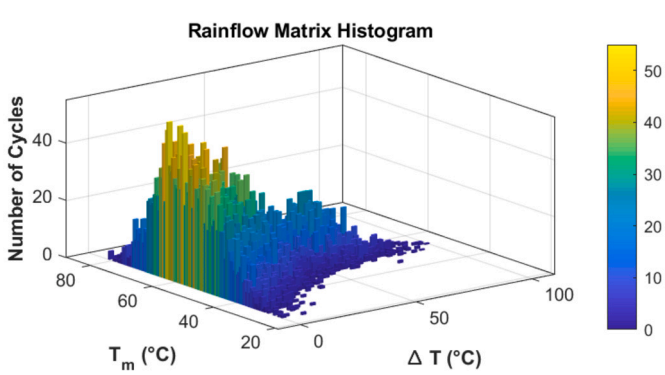

Fig. 8. Application of the Rainflow algorithm on the thermal load of TSV1.

The latter should be represented in terms of MTTF to assess the reliable lifetime of the studied package. Many models in the literature were reported to estimate MTFF due to a failure mechanism. In this paper, we apply straightforward models on TSV and solder to predict their lifetime to failure.

2.3.1. Electromigration

Electromigration (EM) is the movement of metal atoms in metals under high temperatures and large current densities, which can lead to thermal runaway and a short or open-circuit failure. EM is one of the significant reliability problems in semiconductor-based packages. EM may occur in solder joints [19–21] or TSVs [22,23]. As mentioned before, a metric that allows us to predict the lifetime reliability of a package is the mean time to failure. Black's equation, shown in Equation (2), describes the MTTF for EM.

$$MTTF_{EM_{solder,TSV}} = AJ^{-n}e(\frac{E_a}{KT}) \tag{2}$$

In the above equation, J, K, and T represent the current density, Boltzmann constant, and absolute temperature in Kelvin, respectively. The parameters n and E_a represent the current density power factor and activation energy of EM, respectively. These two parameters depend on many factors, including current density, geometry, etc., which can be obtained experimentally. A is a constant fitting parameter.

2.3.2. Stress migration

Stress Migration (SM), known as thermomechanical stress, is another dominant failure mechanism of semiconductor-based packages in TSV. SM is induced by mechanical stress due to a mismatch of the Coefficient of Thermal Expansion (CTE) between layers and operating temperature. The following empirical model is used to predict the MTTF due to SM: [27]

$$MTTF_{SM_{TSV}} = A\sigma^{-n}e(\frac{E_a}{KT}) \tag{3}$$

Where σ is the thermo-mechanical stress due to the mismatch between CTE of TSV and silicon die, and is given by:

$$\sigma \propto (T_0 - T_{TSV})(CTE_{Si} - CTE_{TSV}) \tag{4}$$

Where T_0 is the temperature of the metal at deposition, and T_{TSV} is the absolute temperature of interest, which reflects the cumulative thermal variations experienced by the TSV. It is derived from the Rainflow cycle counting algorithm, and serves as a critical parameter in assessing stress migration failure. By substituting eq. (4) in eq. (3), we get the final expression of the model for determining $MTTF_{SM_{TSV}}$, as shown in eq. (5).

$$MTTF_{SM_{TSV}} = A|T_0 - T_{TSV}|^{-n}e(\frac{E_a}{KT}) \tag{5}$$

2.3.3. Thermal cycling (TC)

Results from the expansion and contraction of layers due to heating and cooling of the package lead to fatigue accumulation in every temperature cycle. After several cycles, the stress caused by Thermal Cycling (TC) can induce mechanical fatigue, eventually leading to package failure. A failure mechanism related to TC causes damage to all layers of the package. However, according to McPherson et al. [24], Frank et al. [25], essential damage is induced by TSV and solder joints. In this research, only the effects of TC in TSV and solder joints are considered, as they are the main causes of package failure, for the sake of simplicity. The number of cycles to failure N_f is modeled by the Coffin-Manson equation, expressed as follows:

$$N_f = a(\Delta T_{layer})^{-q} \tag{6}$$

Where a and q are empirically determined constants, depending on material properties and test conditions, and δ T layer is a jump in the temperature within the cycle.

Equation (6) indicates that an increase in the layer's temperature imposes a higher failure rate, which results in a lower MTTF. Hence, the failure mechanism model due to thermal cycling could be defined as follows: [26]

$$MTTF_{TC_{TSV,so}} = A(\Delta T_{layer})^{-q} \tag{7}$$

In the above equation, A is constant depending on the material.
The above models cannot be directly applied to estimate the lifetime of the target layer or system because they do not provide failure distributions due to the arbitrary process variation over time (parameters related to MTTF equations, such as temperature and electrical parameters). This paper models the lifetime distributions using the Weibull distribution for three failure mechanisms.

2.4. SiP reliability modeling and computing

As mentioned before, in this paper, we assume that all failure mechanisms have Weibull distribution. Thus, we can estimate the reliability of any layer in the package. The reliability function is defined as the probability of surviving until the specified lifetime, with the Weibull distribution computed as follows:

$$R(t) = e^{-(\frac{t}{\eta})^{\beta}} \tag{8}$$

Where η is the scale parameter that depends on process variations, t is the current time, and β is the slope parameter of the Weibull distribution. Since η varies in each time interval obtained by the cycle-counting algorithm due to the changes in the temperature of layers, the reliability at the qth interval can be calculated from time 0 up to time t using the following formula:

$$R(t) = e^{-(\frac{\tau_1}{\eta_1}+\ldots+\frac{\tau_{q-1}}{\eta_{q-1}}+\frac{t-\sum_{i=1}^{q-1}\tau_i}{\eta_i})^{\beta}} \tag{9}$$

Where τ_i is the duration of the ith interval obtained by the Rainflow algorithm, and η_i is the Weibull scale parameter computed in this interval time by using the formula of mean time to failure associated with Weibull distribution [28]:

$$\eta_i = \frac{MTTF_i}{\Gamma(1+(\beta)^{-1}} \tag{10}$$

In the proposed framework, for each failure mechanism applied to a specific layer, we generate time samples following a Weibull distribution for Monte-Carlo analysis as follows:

$$TS = -\frac{\eta_i}{(ln(1-(\chi))^{\beta}} \tag{11}$$

where χ is a random number generated from a uniform distribution between 0 and in the interval $[0, 1]$. This method estimates the lifetime distribution of each layer in the package due to each failure mechanism. Then, for each layer, we select the failure whose MTTF value is minimal, as shown in Fig. 9, to calculate the system's total reliability. In reliability engineering, the Weibull distribution is a preferred choice for modeling failure data due to its flexibility and ability to represent various failure behaviors. It has proven useful in depicting failures attributed to wearout [37].

In this work, it is assumed that the SiP malfunctions if one of the layers fails. Therefore, the whole reliability of SiP can be obtained as follows:

$$R_{SiP} = \prod_{k=1}^{4} R_{L,k} \tag{12}$$

Where $R_{L,k}$ is reliability in layer k due to failure L its MTTF in that layer is minimal.

3. Experimental results and analysis

The results obtained in this study are based on the system shown in Fig. 2 and the mission profile of the versatile sensor interface. Two case studies were conducted to show the impact of failure mechanisms on the reliability of solder and TSV. A reliable comparison and validation of the proposed framework require extensive in-field failure data and trustworthy information about the cause of damage and its location. This prior knowledge is not trivial to obtain. We evaluate the reliability of a typical System-in-Package (SiP) to demonstrate the effectiveness of the proposed framework for reliability assessment. The choice of SiP is motivated by its susceptibility to multi-mechanism failures and its sensitivity to environmental conditions. To address this, we apply the Physics-of-Failure (PoF) models to both solder joints and TSVs, as these are the most vulnerable components in the SiP structure. The SiP under study consists of two stacks, each containing two dies, along with additional layers such as TSVs and solder joints. The thermal model for the system is depicted in Figs. 2 and 3. In the first stage of the proposed framework, the mission profile of the versatile sensor interface is input into the power compiler to calculate the power consumption. A testbench with a dissipated power of 10^6 vector is used, and the resulting power data are fed into the thermal circuit shown in Fig. 3 to calculate the thermal distribution of the SiP. As described earlier, the thermal distribution obtained at this stage is irregular and requires refinement through cycle counting. To achieve this, we applied MATLAB's Rainflow Counting algorithm to extract key statistical parameters, including the mean temperature, the number of cycles, and the temperature amplitude of cycles for both the solder and TSV layers. Upon calculating the statistical parameters for the entire mission profile, the Mean Time to Failure (MTTF) for each time step is estimated by applying the relevant failure mechanisms. At each time step, the four previously described failure mechanisms are applied to both solder joints and TSVs. Subsequently, Monte Carlo sampling is employed to generate a comprehensive set of lifetime samples for these components. These sampled data are then fitted to a Weibull distribution to characterize the reliability and predict the failure behavior of the system. In our first experiment, the ambient temperature was set to 25 °C. In the second, more practical experiment, the ambient temperature is allowed to vary in accordance with environmental conditions. To account for a range of potential operating environments, we selected a set of standard environmental conditions for the analysis. In the second experiment, designed to reflect practical conditions, the ambient temperature varies according to environmental factors. To encompass a range of potential operating environments, we selected a set of standard environmental conditions. Through iterative testing, we determined that a time step of 3 minutes strikes an optimal balance between simulation accuracy and computational efficiency. Increasing the time step beyond 3 minutes adversely affected prediction accuracy, while reducing it further did not significantly enhance the predicted lifetime but substantially increased simulation time. The mission profile has been transformed into thermal loads according to the method explained in Section 2.1. The regular loading, obtained by the Rainflow algorithm, on TSV1 and TSV2 is shown in Fig. 10. The regular thermal loading profiles for solder layers 1 and 2 are shown in Fig. 11.

The obtained results show that the minimum MTTF of the TSV is caused by stress migration (SM), while the minimum MTTF of the solder is due to thermal cycling (TC). The lifetime distributions generated by Monte-Carlo simulations for these two cases are shown in Figs. 12 and 13, respectively. MTTFs for each layer under different failure mech-

```
Algorithm : MC based failure distribution
1: Input : Mission profile
2: Output: failure that causes a minimum life of a layer and MTTF due to
this failure, MTTF of SiP
3: For k ⟵ 1 to 4 do \\ Loop Through a layers ( solder, TSV)
4: For l ⟵ 1 to 3 do \\ Loop Through a failure mechanisms
5: Apply the failure model from section II-C to compute MTTF (l,k)
6: For m ⟵ 1 to N do \\ N=10^5 Monte Carlo simulation
7: lifespan ⟵ random_time samples( MTTF(l,k)) \\ using equations 10
and 11
8: Lifetime distribution of layer K due to failure l
9:end For
9: return minMTTF of layer
10: end For
11 : end For
12: return MTTF of SiP
13 : End
```

Fig. 9. Pseudocode of the algorithm for selecting the failure cause min lifetime distribution.

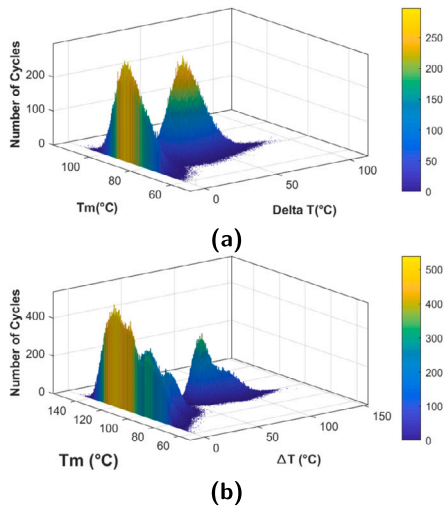

Fig. 10. Thermal load: (a) TSV1, and (b) TSV2.

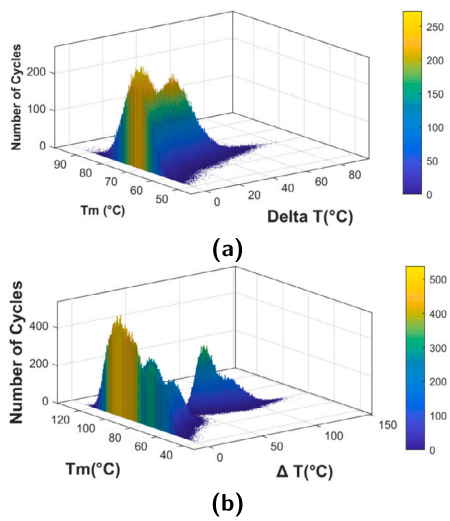

Fig. 11. Thermal load: (a) Solder1, and (b) Solder2.

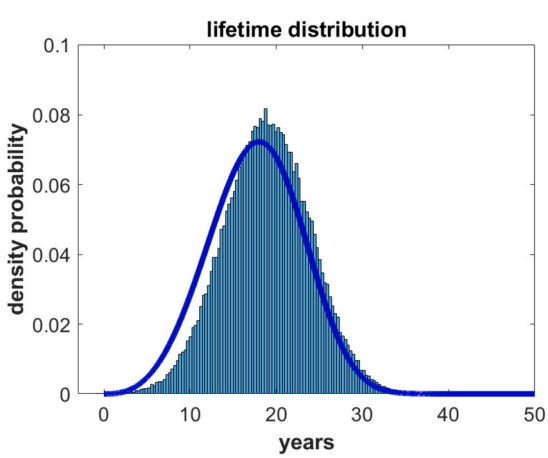

Fig. 12. Lifetime distribution of TSV2 due to Stress Migration (SM).

anisms are shown in Fig. 14. All failures affect the layers at various degrees.

The second stack, shown in Fig. 14, contains TSV2 and solder2. It has a relatively short lifetime compared to the first stack because it is exposed to a thermal load with very high peaks and large temperature

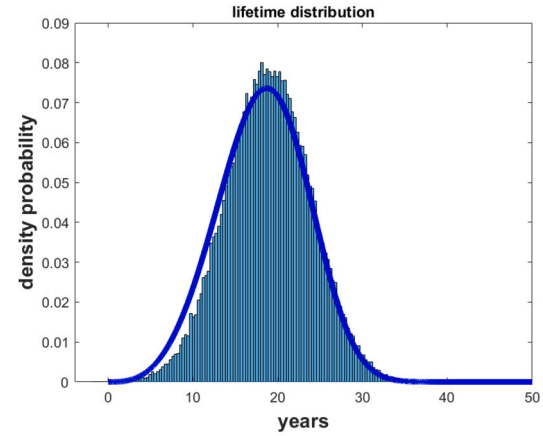

Fig. 13. Lifetime distribution of Solder 2 due to Thermal Cycling (TC).

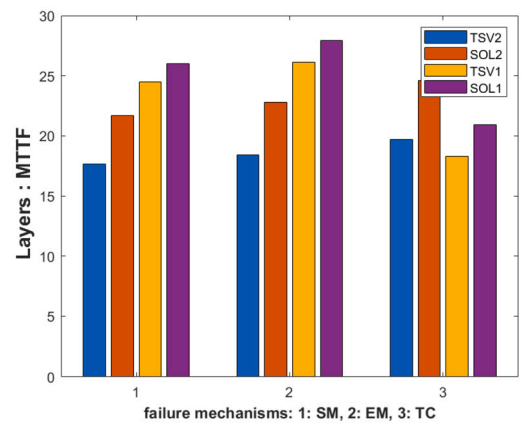

Fig. 14. MTTF of layers due to different failure mechanisms with constant ambient temperature.

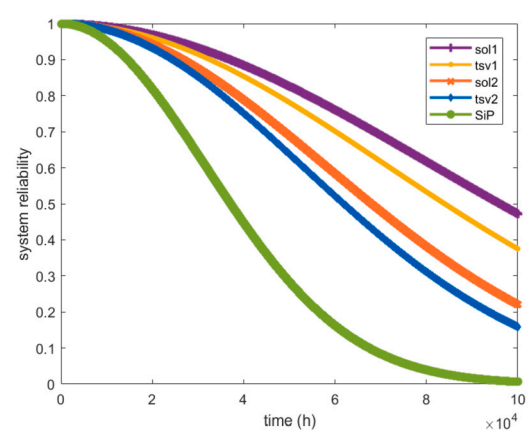

Fig. 15. Reliability of SiP and TSV and solder layers with constant ambient temperature.

cycles. These results also show that SM and EM greatly affect all layers; however, SM has a greater impact on the layers than EM. It is also important to note that both layers of solder in the two stacks are impacted more by TC, while those of TSV are affected much more by SM, even though the four layers are subjected to different thermal loads.

The reliability of SiP depends on the reliability of each layer (solder joints and TSV layers), and any layer malfunction causes system failure. Fig. 15 shows the reliability of both the layers and the SiP. The first stack in this figure (solder1 and TSV1) is more reliable than the second stack (solder2 and TSV2), due to the higher thermal load applied to the sec-

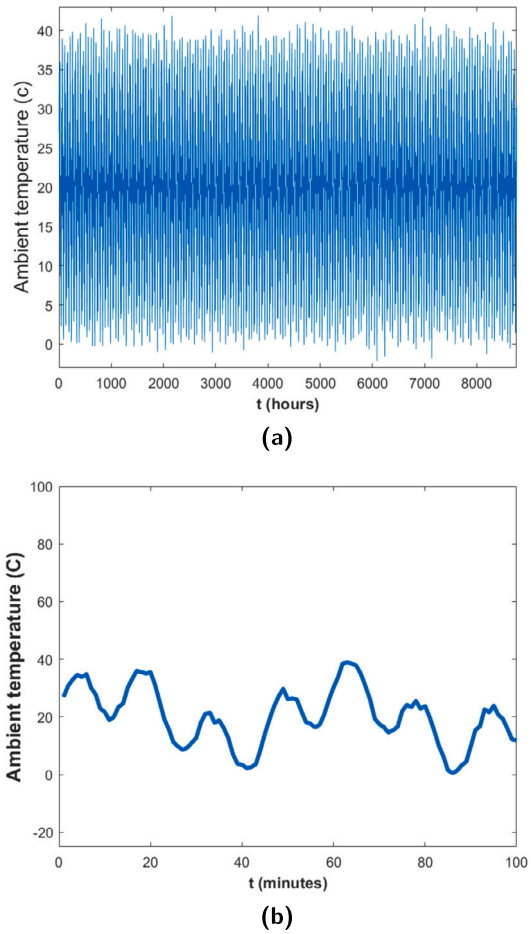

Fig. 16. Ambient temperature: (a) Entire profile, and (b) Over the first 100 minutes.

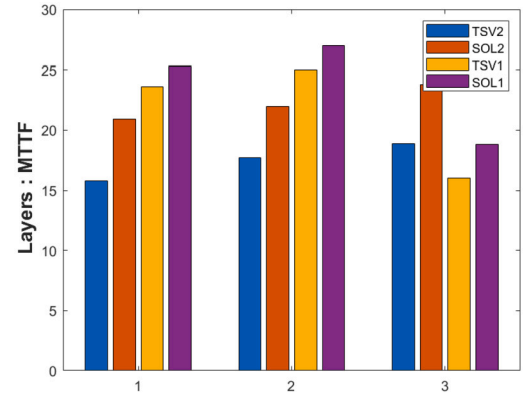

Fig. 17. MTTF of layers due to different failure mechanisms with varying ambient temperature.

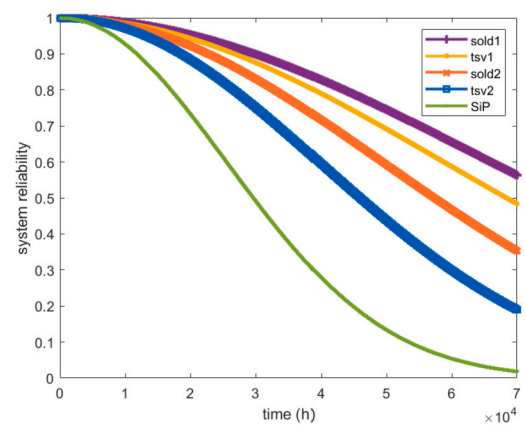

Fig. 18. Impact on SiP reliability of TSV and solder layers with varying ambient.

ond stack. In addition, the reliability of the whole SiP is lower than the reliability of each individual layer, indicating that the reliability of each layer has a dominant impact on the overall SiP reliability. The previous experiment assumes that the ambient temperature is constant. However, the mission profile depends on the workload and the ambient temperature. Therefore, we carried out another experiment in which the ambient temperature varied between -2 °C and 42 °C, as shown in Fig. 16. The results obtained from this second experiment (Fig. 17), (Fig. 18) show that the change in the ambient temperature affects both the solder and TSV layers, but it impacts soldiers more than TSVs. Despite this effect, the dominant failure mechanism across all configurations remains stress migration (SM), with a greater impact on the TSVs. The reliability of the whole SiP is shown in Fig. 18. As we can see, the system is less reliable than in the case of fixed ambient temperature shown in Fig. 15. The ambient temperature cycles dominate the reliability of all layers and, hence, reduce the reliability of SiP.

4. Discussion

A reliable comparison and validation of the proposed framework require extensive in-field failure data and trustworthy information about the manufacturing process, the cause of damage, and its location. This prior knowledge is not trivial to obtain [34].

Table 1 compares the proposed framework with other similar works. In Fu et al. [32], the MTTF of SiP is estimated by using the coupling between the thermal distribution developed using the software ANSYS Multiphysics. Thus, the parameters of the physics-of-failure (PoF) models are extracted with ANSYS and applied as inputs to calculate the lifetime of different failure mechanisms. Although this method is accurate, it is slow and fails to converge, especially when considering the instantly dynamic variation of the temperature and workload in long-run conditions. Moreover, as discussed in Section 1, the assumption of linear damage accumulation does not hold. The works reported in [33] and [34] focus on fitting failure distributions. The Monte Carlo simulation method randomly samples the failure density function of any failure mechanism acting on a given layer or point of the system. It obtains the time-to-failure of this given layer caused by the given mechanism. To fit the data generated by Monte-Carlo simulation, authors in [33] proposed the MaxEnt PDF fitting algorithm. While in [34], the authors used the Bayesian network to select the best distribution fit among the lognormal, Weibull, and gamma analytical models. In our proposed work, the accurate thermal model permits us to include the mission profile in reliability studies. Thus, the PoF models can count any variation in the operating system conditions in the lifecycle of the SiP. The samples generated by the Monte-Carlo simulation are fitted by the Weibull distribution. We chose this distribution because it is most often used to study the reliability of electronic devices and because it is versatile. Besides, as shown in Figs. 12 and 13, the data is well-fitted by the Weibull distribution. While the proposed framework provides valuable insights into the reliability of System-in-Package (SiP) technologies, its performance in real-world scenarios remains unverified. To enhance the framework's applicability and accuracy, future work should focus on developing adaptive models that can update reliability predictions in real-time based on evolving process data from manufacturers. This approach would enable continuous validation and refinement of the framework under practical operating conditions.

Table 1
Performance Summary and Comparison.

Ref.	Reliability model	Concern	Metric	Considerations
Fu G	System-level, PoF	Stress selecting for virtual qualification test	Constant failure rate	no
Wan B	System-level, PoF	PoF sampling and simulation method, and data fitting with MC	Lifetime distribution	no
Sun B	System-level, PoF	Combination of PoF data with Bayesian model	Lifetime distribution	no
This Work	System-level, PoF	Thermal variation and uncertainties	lifetime distribution and reliability metric based on minimal MTTF	Mission profile, temperature variation, and world

5. Conclusion

This paper proposed a novel 3D SiP reliability assessment method to mitigate the problems resulting from the lack of coupling between the mission profile and the dominant wear-out rate for each layer, determining the reliability of 3D SiPs. As part of that method, an effective and comprehensive framework tailored for analyzing multi-layered SiP reliability insights over the lifetime of SiP is proposed. This framework adopts unified units for each layer in the system. Leveraging an accurate thermal model, the proposed framework facilitates rapid predictions of SiP thermal behavior. Additionally, The proposed method emphasized identifying the dominant failure mechanism in each layer, thus aiding designers in preemptively addressing damages caused by failures early in the design process. Furthermore, the framework's adaptability allows for seamless integration of additional sources of failures and layers, enhancing its versatility across various systems. Our findings underscore the significant impact of ambient temperature on the reliability of SiPs, particularly affecting solder joints, thereby highlighting the importance of considering environmental factors in assessing SiP lifetime.

CRediT authorship contribution statement

Djallel Eddine Touati: Writing – original draft, Formal analysis, Methodology, Conceptualization, Investigation.

Declaration of competing interest

The authors whose names are listed immediately below certify that they have NO affiliations with or involvement in any organization or entity with any fi nancial interest (such as honoraria; educational grants; participation in speakers' bureaus; membership, employment, consultancies, stock ownership, or other equity interest; and expert testimony or patent-licensing arrangements), or non-financial interest (such as personal or professional relationships, affi liations, knowledge or beliefs) in the subject matter or materials discussed in this manuscript.

Data availability

No data was used for the research described in the article.

References

[1] J.U. Knickerbocker, P.S. Andry, B. Dang, R.R. Horton, S.L. Wright, Three-dimensional silicon integration IBM, J. Res. Dev. 52 (6) (2008) 553–569.
[2] M. Ali, A. Hassan, M. Honarparvar, M. Nabavi, Y. Audet, M. Sawan, Y. Savaria, A versatile SoC/SiP sensor interface for industrial applications: implementation challenges, IEEE Access 10 (2022) 24540–24555.
[3] G.A. Klutke, P.C. Kiessler, M.A. Wortman, A critical look at the bathtub curve, IEEE Trans. Reliab. 52 (1) (2003) 125–129.
[4] V. Chandra, Monitoring reliability in embedded processors-a multi-layer view, in: Proceedings of the 51st Annual Design Automation Conference, 2014, June, pp. 1–6.
[5] H.C. Cheng, H.K. Cheng, S.T. Lu, J.Y. Juang, W.H. Chen, Drop impact reliability analysis of 3-D chip-on-chip packaging: numerical modeling and experimental validation, IEEE Trans. Device Mater. Reliab. 14 (1) (2013) 499–511.
[6] H.C. Cheng, Y.M. Tsai, S.T. Lu, IMC growth reaction and its effects on solder joint thermal cycling reliability of 3D chip stacking packaging, Microelectron. Reliab. 53 (1) (2013) 30–40.
[7] K.N. Tu, Reliability challenges in 3D IC packaging technology, Microelectron. Reliab. 51 (3) (2011) 517–523.
[8] K.N. Tu, Reliability challenges in 3D IC packaging technology, Microelectron. Reliab. 51 (3) (2011) 517–523.
[9] H.C. Cheng, H.K. Cheng, S.T. Lu, J.Y. Juang, W.H. Chen, Drop impact reliability analysis of 3-D chip-on-chip packaging: numerical modeling and experimental validation, IEEE Trans. Device Mater. Reliab. 14 (1) (2013) 499–511.
[10] H.C. Cheng, Y.M. Tsai, S.T. Lu, W.H. Chen, Interconnect reliability characterization of a high-density 3-D chip-on-chip interconnect technology, IEEE Trans. Compon. Packag. Manuf. Technol. 3 (12) (2013) 2037–2047.
[11] H.E. Cheng, R.S. Chen, Interval optimal design of 3-D TSV stacked chips package reliability by using the genetic algorithm method, Microelectron. Reliab. 54 (12) (2014) 2881–2897.
[12] H. Wang, D. Huang, R. Liu, C. Zhang, H. Tang, Y. Yuan, STREAM: stress and thermal aware reliability management for 3-D ICs, IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst. 38 (11) (2018) 2058–2071.
[13] S. Wang, M.B. Tahoori, Electromigration-aware local-via allocation in power/ground TSVs of 3-D ICs, IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 25 (10) (2017) 2881–2892.
[14] Y. Yang, A. Sangwongwanich, F. Blaabjerg, Design for reliability of power electronics for grid-connected photovoltaic systems, CPSS Trans. Power Electron. App. 1 (1) (2016) 92–103.
[15] D. Zhou, H. Wang, F. Blaabjerg, Mission profile based system-level reliability analysis of DC/DC converters for a backup power application, IEEE Trans. Power Electron. 33 (9) (2017) 8030–8039.
[16] M. Matsuishi, T. Endo, Fatigue of metals subjected to varying stress, in: Proc. Kyushu District Meeting, 1968, pp. 37–40.
[17] X.H. An, S.D. Wu, Z.G. Wang, Z.F. Zhang, Significance of stacking fault energy in bulk nanostructured materials: insights from Cu and its binary alloys as model systems, Prog. Nat. Sci. 101 (2019) 1–45.
[18] A. Basavalingappa, J.M. Passage, M.Y. Shen, J.R. Lloyd, Electromigration: lognormal versus Weibull distribution, in: 2017 IEEE International Integrated Reliability Workshop (IIRW), IEEE, 2017, October, pp. 1–4.
[19] F.Y. Ouyang, H. Hsu, Y.P. Su, T.C. Chang, Electromigration induced failure on lead-free micro bumps in three-dimensional integrated circuits packaging, J. Appl. Phys. 112 (2) (2012).
[20] Y. Li, D. Goyal (Eds.), 3D Microelectronic Packaging: from Fundamentals to Applications, vol. 57, Springer, 2017.
[21] Y.W. Chang, C.C. Hu, H.Y. Peng, Y.C. Liang, C. Chen, T.C. Chang, J.Y. Juang, A new failure mechanism of electromigration by surface diffusion of Sn on Ni and Cu metallization in microbumps, Sci. Rep. 8 (1) (2018) 5935.
[22] J.P. Gambino, S.A. Adderly, J.U. Knickerbocker, An overview of through-silicon-via technology and manufacturing challenges, Microelectron. Eng. 135 (2015) 73–106.
[23] J.B. Bernstein, M. Gurfinkel, X. Li, J. Walters, Y. Shapira, M. Talmor, Electronic circuit reliability modeling, Microelectron. Reliab. 46 (12) (2006) 1957–1979.
[24] J.W. McPherson, Reliability Physics and Engineering: Time-to-Failure Modeling, Glaser, Springer, New York, 2010, p. 117.
[25] T. Frank, S. Moreau, C. Chappaz, P. Leduc, L. Arnaud, A. Thuaire, G. Poupon, Reliability of TSV interconnects: electromigration, thermal cycling, and impact on above metal level dielectric, Microelectron. Reliab. 53 (1) (2013) 17–29.
[26] F. Akkara, S. Su, H. Ali, P. Borgesen, Effect of cycling amplitude variations on SnAgCu solder joint fatigue life, IEEE Trans. Compon. Packag. Manuf. Technol. 8 (11) (2018) 1896–1904.

[27] JEDEC Standard, Failure mechanisms and models for semiconductor devices, JEP122-A, 2016.
[28] R.A. Johnson, I. Miller, J.E. Freund, Probability and Statistics for Engineers, vol. 2000, Pearson Education, London, 2000, 642p.
[29] R.P. Reddy, A. Acharyya, S. Khursheed, A cost-aware framework for lifetime reliability of TSV-based 3D-IC design, IEEE Trans. Circuits Syst. II, Express Briefs 67 (11) (2020) 2677–2681.
[30] P. Vivet, E. Guthmuller, Y. Thonnart, G. Pillonnet, C. Fuguet, I. Miro-Panades, F. Clermidy, IntAct: a 96-core processor with six chiplets 3D-stacked on an active interposer with distributed interconnects and integrated power management, IEEE J. Solid-State Circuits 56 (1) (2020) 79–97.
[31] M. Ikonen, Power cycling lifetime estimation of IGBT power modules based on chip temperature modeling, 2012.
[32] G. Fu, Y. Su, W. Guo, B. Wan, Z. Zhang, Y. Wang, Life prediction methodology of system-in-package based on physics of failure, Microelectron. Reliab. 88 (2018) 173–178.
[33] B. Wan, Y. Wang, Y. Su, G. Fu, Reliability evaluation of multi-mechanism failure for semiconductor devices using physics-of-failure technique and maximum entropy principle, IEEE Access 8 (2020) 188154–188170.
[34] B. Sun, Y. Li, Z. Wang, D. Yang, Y. Ren, Q. Feng, A combined physics of failure and Bayesian network reliability analysis method for complex electronic systems, Process Saf. Environ. Prot. 148 (2021) 698–710.
[35] D.E. Touati, A. Oukaira, A. Hassan, M. Ali, Y. Savaria, A. Lakhssassi, Thermal analysis of system in package considering boundary conditions for long-term reliability studies, IEEE Access (2024).
[36] Sun Igor Rychlik, A new definition of the rainflow cycle counting method, Int. J. Fatigue 9 (2) (1987) 119–121.
[37] Harry F. Martz, Reliability theory, in: Robert A. Meyers (Ed.), Encyclopedia of Physical Science and Technology, third edition, Academic Press, 2003, pp. 143–159.
[38] István Bozsóki, Balázs Illés, Attila Géczy, Numerical simulation of Sn grain growth in composite solder joint using a modified cellular automaton model, Results Eng. 26 (2025) 104669.
[39] Niño Rigo Emil G. Lim, Aristotle T. Ubando, Jeremias A. Gonzaga, Flip-chip package solder-underfill reliability using finite element analysis, Results Eng. 24 (2024) 103556.