

Received 7 April 2025, accepted 2 May 2025, date of publication 7 May 2025, date of current version 16 May 2025.

Digital Object Identifier 10.1109/ACCESS.2025.3567633

RESEARCH ARTICLE

11.2 V Supply, 0.21% Biphasic Stimuli Charge-Balanced Neurostimulator With Switching Spike Suppression: An Application to Intraspinal Microstimulation for Restoring Motor Function

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This work was supported in part by Westlake University under Grant 10318A992001.

This work involved human subjects or animals in its research. Approval of all ethical and experimental procedures and protocols was granted by the Animal Care and Ethics Committee of Iran Neural Technology Research Centre with IACUC No. INTC-2024-0018.

ABSTRACT In this paper, a new high-voltage and high-current compliance integrated electrical neurostimulator with charge balancing stimuli is presented. The proposed stimulator uses a stacked structure to provide the 11.2 V power supply delivering a biphasic stimulation current of 3.2 mA. It includes a novel charge balancing method to secure safe symmetric and asymmetric biphasic pulse trains with a low charge mismatch of 0.21%. Also, the proposed device properly cancels the switching current spikes generating biphasic stimuli. In addition, two methods based on a gate driver circuit and zero current switching are proposed securing advanced stimulator feature which are validated through extensive testing phase, including a simulation of 29 million periodic stimulation cycles delivering a current of 3.2 mA. The stimulator demonstrates robust performance with an average residual DC current of 11.4 nA after the charge balancing phase. The stimulator is implemented using the standard TSMC 180 nm 1.8 V/3.3 V LV CMOS technology. It operates at a low power budget of 90 μ W. The main core of the circuit occupies an area of 0.181mm². The fabricated chip has been packaged and successfully tested in a motor function of intraspinal paralysis application.

INDEX TERMS Electrical neural stimulator, charge balancing, active and passive charge balancing, spike, high-voltage compliance.

I. INTRODUCTION

Functional electrical stimulation (FES) has been attracted a lot of attention for its potential use in treating numerous neural disorders and nervous system dysfunctions [1], [2], [3] such as chronic pain [4], Parkinson's disease [5], epilepsy [6], [7], tremor [8], dystonia [9], tinnitus [2], stroke [10], bladder dysfunction [11], obstructive sleep

apnea [12], and obesity [13]. FES has also been used to restore sensory and motor functions lost through injury or disease like implantable visual prosthesis [14], [15], [16], cardiac pacemaker [17], cochlear implant [12], [18], [19] seizure control [20], [21], proprioceptive prosthesis [22], bladder stimulators [11], phrenic nerve stimulators [23], vestibular Prostheses [24], and neuromuscular stimulation for restoring voluntary control of locomotion [25], [26], [27], [28], [29], [30]. These prostheses establish a direct link between the neural stimulator and the nervous system.

The associate editor coordinating the review of this manuscript and approving it for publication was Xiaodong Liang¹.

Neural stimulation is based on electrical injecting charge to the nerve tissues. The charge can be injected either by voltage stimulation (VS) or by current stimulation (CS). The most common charge injection is by the current stimulation (CS). In VS, charge injection is performed by a constant voltage which is applied between the stimulating electrode and return electrode [31]. The VS has the advantage of higher energy efficiency [32], [33] but has the disadvantage of a lack of control over the charge delivered to the tissue due to variability of the neurological impedance [34]. The impedance of neural tissue can significantly change over time and particularly in the period immediately after the implantation [35], [36]. The most common charge injection method is the biphasic charge-balanced current stimulation (CS). In CS, the charge is delivered by a constant current source and its quantity is directly controlled by the amplitude and duration of the stimulation under variable impedance [37], [38], [39]. Higher voltage compliance of the current-mode stimulators allows delivering a wider range of currents to the load. However, there are several challenges facing neural stimulator design. Reducing the size of the device, power consumption, minimizing residual DC-current [16], safe electrical stimulation are some of the crucial issues that should be addressed in the design of the neural stimulator.

Voltage compliance, is another crucial issue in the design of neural stimulator, in particular when a large number of electrodes is required and consequently the size of each electrode should be significantly decreased due to small area of the target such as in retinal implant [40], [41], [42]. This leads to high load impedance that the stimulator should derive.

The selection of appropriate technology that aligns with the desired current and high voltage compliance is an important issue in the design of the neural stimulator chip. One approach is to use high-voltage CMOS process [6], [15], [17], [18]. High-voltage CMOS offers advantages like reduced design complexity and higher reliability, but it has some drawbacks such as larger area, higher cost, and increased power consumption.

Low-voltage technology has emerged as an alternative to address these issues [8], [12], [19], [20], [21], but the low-voltage transistors have limitations in supply voltage and tolerance. Design techniques like using larger technology nodes [22] and CCII topologies [23] have been introduced, but voltage compliance and current capabilities may still be insufficient. The stacked transistor method is a solution to address high voltage compliance and output current requirements [31], [35], [43], [44], [45]. This technique increases the voltage tolerance for transistors in low-voltage processes and enables full integration with the control unit system without requiring specific hybrid technology, such as the Chipset platform. In this work, to obtain a constant stimulation current over a high impedance range, a high voltage-tolerant stimulus drivers using low-voltage technology is employed.

Voltage spikes which are generated during the switching, are problematic, as can lead to unbalanced biphasic stimulus, tissue damage, and transistor failure due to exceeding the maximum tolerable range of transistors. Several solutions have been introduced to address this issue, including reducing the switching speed for a smoother transition [16], implementing output filtering, and employing proper circuit design techniques [19]. In this work, two methods for spike voltage reduction during switching process is introduced which includes using gate drive circuits with appropriate rise and fall time control and Zero-Current Switching (ZCS) method.

Ensuring safe long-term electrical stimulation is a primary consideration in the neural stimulator design. Charge-balanced stimulation is crucial to prevent tissue damage from net charge exceeding a certain threshold [24]. Hence, charge-balanced biphasic stimulation pulses are used to recover delivered charge and thus mitigate toxicity from electrochemical reactions occurring at the metal-tissue interface.

Several techniques for charge-balancing have been proposed to achieve safely charge-balanced biphasic stimulation. Passive and active charge balance are two general techniques to cancel the residual DC current [20], [21], [25], [26], [28], [29], [46], [47], [48], [49], [50]. In passive charge-balancing technique, a large dc blocking capacitor is inserted in series with each electrode. For functional electrical stimulation (FES) applications, these capacitors are about a few microfarads [51]. These capacitors cannot be fully integrated with stimulation circuitry and must be implemented off-chip. Off-chip dc blocking-capacitors is a serious limitation for developing multichannel implantable stimulators. To overcome this problem, high-frequency current-switching (HFCS) was proposed for dc blocking [51]. In this technique, the stimulation current pulse during cathodic phase was generated by summation of the two high-frequency current pulse trains. The proposed approach could reduce the capacitance value to the picofarad range. A few charge balancing scheme based on electrode shortening has been also implemented in [17], [47], [52], and [53]. In this method, the electrodes are shorted after stimulation period for a certain period of time. However, electrode shorting may result in some unwanted stimulation and spikes. The general disadvantage of all passive discharge techniques is the large current spikes during the switched discharge process, which may result in tissue damage during long-term stimulation, transistor failure, and may cause unwanted neural response to neighboring sites.

Several active charge balancing circuits have been also proposed in [8], [12], [15], [16], [17], [18], [26], and [27] for active monitoring the charge delivering to the tissue during both phase of biphasic neural stimulation to avoid charge accumulation, including pulse insertion [42] offset regulation [26], [28], [29], [54], pulse modulation [28], [29], hybrid method (pulse modulation and offset regulation) [30] and digital approaches to avoid charge mismatch [31]. These

methods define a safe voltage range for the tissue. After each cycle, the residual voltage is compared to the safe range. If it exceeds the safe range, indicating charge imbalance. In pulse insertion method, low amplitude pulses with a short pulse width are generated after each cycle to decrease the residual voltage and achieve charge balance. Offset regulation method injects or draws current to apply a compensating stimulation pulse when the residual voltage exceeds the safe range. For pulse modulation, the current level in the anodic or cathodic phase is adjusted based on the exceeded voltage on the tissue after each cycle.

In some cases, instead of changing the amplitude, the stimulator adjusts the pulse width to achieve charge-balanced biphasic stimulation [19], [32]. Other methods have also been presented in [8] and [27]. The proposed stimulator in [8] utilizes a capacitor-reuse technique with a residual charge detector to achieve active charge balancing. It consists of a digital controller and an integrated Analog-to-Digital Converter (ADC) for the residual charge detector. The stimulator in [27] proposes a new method involving a CC mode and a VC mode stimulator to achieve accurate anodic pulse generation. The CC operation compensates for most of the stimulation charge, while the VC operation ensures high-charge balancing precision. All the above-mentioned active methods suffer from design complexity, unwanted spikes and stimulations, and large occupation area. Moreover, the charge balancing circuit consumes additional power to operate which will increase the total power consumption. Furthermore, since implementing these methods need additional components, they typically result in higher overall system costs. Thus, designing charge balancing circuit can be challenging and requires careful parameter selection and optimization.

In this paper, a high-current and high-voltage compliance neurostimulator that utilizes a novel simple method for charge balancing is proposed based on a new switching method for the stimulator. Additionally, a control unit which receives parallel programming data for control of the whole implant chip operation is presented. The proposed circuit offers several advantages compared to the previous works, including minimized design complexity, particularly in the charge balancing aspect, significant reduction of residual voltage for each stimulation cycle, suppression of voltage spiking, and potential avoidance of tissue and transistor damage, leading to higher reliability.

The remaining parts of this paper are organized as follows: In Section II, an overview of the overall structure of the proposed stimulator is provided. Section III describes the proposed operation for generating stimulation sequences. Section IV includes the design structures for each circuit. This is followed by measurement results, which include in vitro and in vivo experiments, presented in Section V. Finally, conclusions are the subjects of Section VI.

II. NEUROSTIMULATOR ARCHITECTURE

The block diagram of the proposed neurostimulator is shown in Fig. 1. It consists of several key building blocks, including

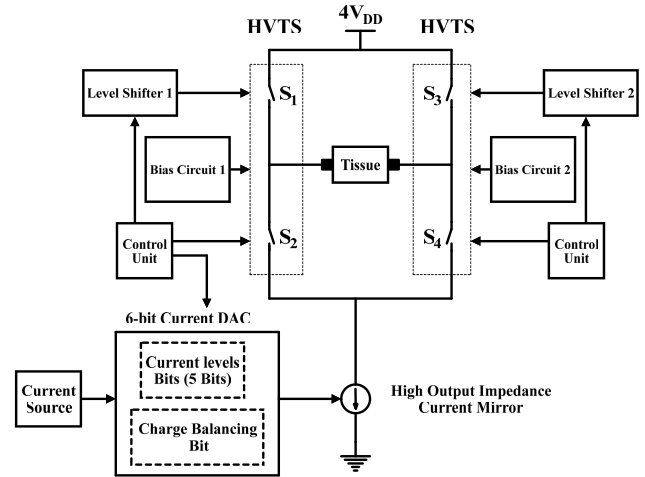


FIGURE 1. Block diagram of the proposed neuro stimulator.

high-voltage tolerant switches (HVTS) with a bias circuit, a control unit, two level shifters, a current source, a 6-bit current-mode digital-to-analog converter (DAC), and a high output impedance current mirror. The proposed stimulator utilizes a single-supply H-bridge structure to generate the biphasic stimulation waveform. This approach allows to have higher voltage compliance and, consequently, higher stimulation current. HVTS is employed to withstand the higher voltage supply in the stimulator.

The level shifters play a crucial role by adding a DC offset voltage of $(n - 1) V_{DD}$ to the input signal from the control unit, where n is the coefficient of the voltage amplification for power supply. They upshift the low-level voltage to a high-level voltage to control the upper switches in the HVTS. The control unit is responsible for generating signals to manage the switching time and control the turn-on and turn-off duration of the switches. A current source is utilized to generate a stable and constant current for the stimulation. The 6-bit current-mode DAC is employed in the proposed stimulator. It utilizes 5 bits to control the current level and resolution based on the desired purpose, and 1 bit is dedicated to charge balancing. The output of the DAC is connected to a high output impedance current mirror to ensure that a constant and stable stimulus current is delivered to the tissue.

III. CIRCUIT DESIGN

Fig. 2 illustrates the whole transistor-level schematic diagram of the proposed stimulator, including the current reference, current DAC, current mirror, and the output stage. The design considerations of each part are explained in the following sub-sections.

A. CURRENT REFERENCE, GAIN CONTROL, AND DAC

As shown in Fig. 2, the modified sub-threshold current reference [33] which includes a start-up circuit, current mirror, and a gain control scheme. In this configuration, all the transistors within the current reference operate in the

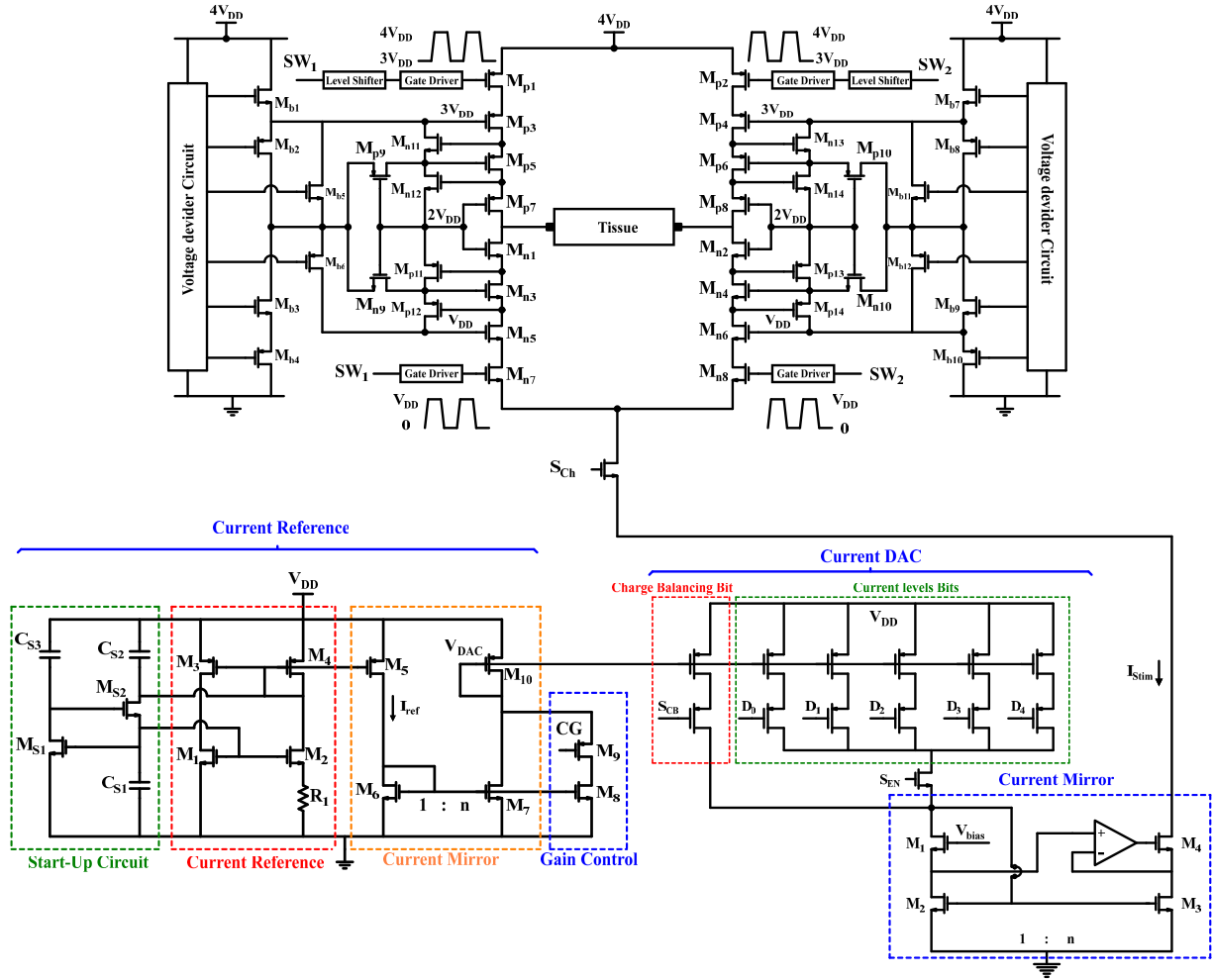


FIGURE 2. Schematic circuit diagram of the proposed neuro-stimulator including the current reference, currentDAC, current mirror, and the out stage of the stimulator.

sub-threshold region. By operating in this region, the current source achieves reduced power consumption. The current flowing through an NMOS transistor in the sub-threshold region can be expressed as [34]:

$$I_D = I_0 \exp\left(\frac{V_{GS} - V_{th}}{nv_T}\right) \quad (1)$$

where I_D , V_{GS} , V_{th} , n , and V_T represent the drain current, Gate-Source voltage, threshold voltage, a constant value between 1.5 and 3, and the thermal voltage, respectively. I_0 is a parameter related to W/L , and W/L indicates the ratio of transistor's width and length. According to (1), the Gate-Source voltage will be

$$V_{GS} = nv_T \ln\left(\frac{I_D}{I_0}\right) + V_{th} \quad (2)$$

According to (1) and (2), the resistor current (R_1 , Fig2) can be given in (3).

$$I_{R_1} = \frac{V_{GS1} - V_{GS2}}{R_1} = \frac{nv_T}{R_1} \ln\left(\frac{S_2}{S_1}\right) \quad (3)$$

where S_i indicates the ratio of W/L . Based on Eq. (3), the current source can be designed for the desired output current.

Fig. 2 also shows a capacitive coupled network utilized in the current reference to ensure the fast startup. To complete the current source, a current mirror and a current gain control section are employed. The current mirror amplifies the output current and transfers it to the DAC. Additionally, transistor M_9 is used for current gain control to generate current for various applications. Transistors M_8 and M_9 are acting as another current mirror branch. If there is a need for more current, the transistor M_9 will be turned on, and more current can be flowed.

As shown in Fig. 2, a 6-bit current DAC is used in the proposed stimulator. Each branch of the DAC consists of two PMOS transistors. The upper transistors form a current mirror with the current source (M_{10}). The bottom transistors act as switches to control the current amplitude (D_{0-5}) and charge balancing (CB bit) based on the digital code from the control unit.

B. CURRENT MIRROR

A high output impedance high-swing current mirror is implemented using a gain boosting technique [23], as depicted in Fig. 2, to mirror the current from the DAC. This current mirror has a high output impedance to ensure having an accurate and stable current at the output stage. In order to reduce the size of the DAC transistors, the output transistors of the current mirror are sized appropriately to mirror n times the DAC current (nI_{DAC}). The output resistance of the gain boosting technique can be expressed as follows:

$$R_{out} \cong g_{m1}r_{ds1}r_{ds2}(1 + A) \quad (4)$$

where g_{m1} , r_{ds1} , r_{ds2} , and A represent the transconductance of M_1 , output resistance of M_1 , output resistance of M_2 , and DC gain of the Op-amp, respectively. Additionally, the amplifier used in the current mirror is a folded cascade configuration, chosen for its high DC gain [36].

C. HIGH-VOLTAGE DRIVER

To achieve a high-voltage-tolerant power supply, a current driver based on stacked transistors and a high output impedance current mirror or the HVTS is proposed (Fig. 2). In this circuit, a current mirror is implemented at the bottom side of the current driver to provide the desired stimulation current level. The output stage consists of four PMOS stacked transistors for the pull-up switch and four NMOS stacked transistors, along with a high output impedance current mirror, for the pull-down switches. This strategy allows for a voltage tolerance of four times the nominal supply voltage ($4 \times V_{DD}$) [35]. A bias circuit drives the stacked transistors to limit the maximum voltage across each stacked terminal to the nominal supply voltage (V_{DD}), as per industry limits. The high output impedance current mirror facilitates to deliver equal anodic and cathodic current. To achieve a high-voltage-tolerant driver using the stacked transistors' strategy in a low-voltage process, the maximum voltage across the upper stacked transistor should be limited by the breakdown voltage of the n-well's parasitic diode. To reduce the overdrive voltage of the stacked transistors and increase the output voltage compliance, the substrate of the stacked transistors is connected to their source terminals. Furthermore, the stacked transistors are implemented using the 3.3V PMOS and NMOS process with the deep n-well layer.

Since the output stage delivers the stimulation current, addressing and minimizing spikes is of the utmost importance, especially for high stimuli current levels. There are two main reasons for producing voltage spikes. First is the effect of parasitic source inductance (L_S) and drain inductance (L_D). During the switching procedure, the rate of current change over time (di/dt) can be high. The voltage equation for the inductance can be expressed as:

$$V = L \times di/dt \quad (5)$$

where L is the sum of L_S and L_D and di/dt is the rate of current change over time. Based on (5), the drain-source

voltage may exceed the nominal voltage (spikes) when the transistor switches from 0V to V_{DD} or V_{DD} to 0V. It will result in a high turn-off/on peak voltage, becoming more severe in low-voltage processes due to limitations in tolerated voltage. It should be noted that in spite of the fact that the parasitic inductance is very small, the rate of current change over time can be extremely high, leading to peak voltages.

Another factor contributing to the production of spikes is parasitic capacitances (C_{gs} , C_{gd}). In this case, when a voltage change occurs, the parasitic capacitance can store and release energy, causing voltage spikes. The magnitude of the voltage spike is determined by the formula $V = Q/C$, where Q is the charge stored in the parasitic capacitance, and C is the parasitic capacitance value. Larger parasitic capacitance values and faster voltage changes can result in higher voltage spikes. To mitigate these spikes and maintain the drain-source voltage (V_{DS}) within a safe range, the transition time of the on/off control pulse should be appropriately selected. If the transition time (fall/rise time) of the input signal for the switches is considered as T , an approximate expression for V_{DS} (or V_{SD}) of each switch in the stacked method can be written as

$$V_{DS} = \pm \frac{NV_{DD} - (N-1)V_{DD}}{T}t + NV_{DD} - (I_D R_t + \frac{I_D}{C_t}t) \quad (6)$$

where N is the number of stacking, I_D is the drain current, R_t is the total resistor seen from the drain, and C_t is the total capacitor seen from the drain. The negative and positive signs mentioned in the context indicate whether the level is increasing or decreasing. According to Eq. (6), the rise/fall time should be appropriately adjusted to reduce the switching speed, ensuring a smooth transition and minimizing charge buildup and current spike levels. In other words, Increasing the rise and fall times of the switching pulses reduces the di/dt and dv/dt during the transitions. Slower transitions lead to lower induced voltages from the parasitic inductance, as per the formula: $V = L \cdot di/dt$. Slower transitions also result in less abrupt changes in voltage, reducing the impact of parasitic capacitance.

In the proposed high-voltage-tolerant buffer, some methods are introduced to eliminate spikes at the output and prevent transistors from exceeding voltage limitations. The first approach involves using gate drive circuits with appropriate rise and fall time control, which can help shape the switching transitions and reduce the di/dt and dv/dt . A ring oscillator or inverter chain gate driver is designed to create a time-delayed and inverted signal at the output. This output signal can be used to drive the gate of the power device, providing the necessary switching transitions. This method introduces a significant series resistance in addition to the gate resistance, increasing the time constant and reducing the switching speed to achieve a smooth transition.

Another method to control spikes is Zero-Current Switching (ZCS). In this method, the switching (power) device is turned off/on when the current through it is zero, minimizing

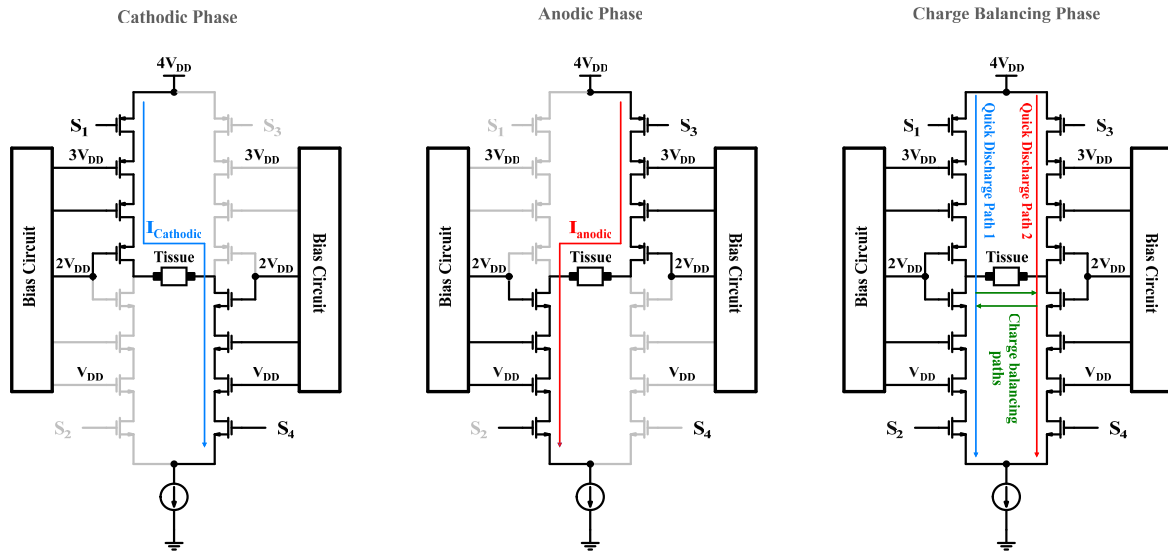


FIGURE 3. Stimulus driver during (a) anodic stimulation, (b) cathodic stimulation, and (c) charge balancing phases.

the turn-off/on switching spikes. Moreover, the ZCS method aims to minimize switching losses by ensuring that the current through the power device is zero during the switching transition. The main principle of ZCS is to turn off/on the power device when the current through it is zero, thereby avoiding high current spikes and reducing switching losses. Moreover, the use of ZCS reduces stress on the power devices due to soft-switching, which can improve their reliability and lifetime. A proper configuring of the applied control signal is essential to design and implement this method. Thus, the implementation and design of the control unit are crucial. The subsequent subsection will cover the design considerations for the control unit and how voltage spikes can be prevented by properly configuring the applied control signal sequences.

D. PROPOSED CHARGE BALANCING

In this work, a simple charge balancing technique which does not require any extra circuit or switches, that are used in passive charge balancing technique, is proposed. The proposed charge balancing process which is activated after the anode and cathode stimulation phases, is illustrated in Fig. 3. Moreover, Fig. 4 compares the proposed charge balancing method with the conventional shortening method.

Due to imperfections in the fabrication process of integrated circuits and clock feed-through, mismatch in the biphasic waveform always occurs. This results in an accumulation of residual charges at the electrode-tissue interface during long-term stimulation, leading to irreversible reactions with electrode dissolution and tissue damage [26]. The difference between the injected charge during the cathode and anode stimulation phases results in a difference between across the tissue after the stimulation phases ($V_A \neq V_B$, Figs. 3 and 4).

Moreover, the switches S_1 and S_2 may show different resistances, causing different voltage drops for switches. The proposed charge balancing procedure (Fig. 3(c) and Fig. 4(b)) is as follows:

- All switches (S_{1-4}) in the HVTS part are initially closed.
- A small controlled current level is set by closing the charge balancing switch (CB) in the DAC and opening the switches D_0 - D_4 in the current DAC (Fig. 4(b)).
- After closing all switches (S_{1-4}) and charge balancing switch (CB), the current will flow in two main paths. The first patch is a direct patch from the upper switches to the bottom switches (i.e., S_1 to S_2 and S_3 to S_4). This can help the stimulator to have a quick discharge path to ensure safety, especially after applying a high current level stimulation.

Since there is a difference potential between two stimulating electrodes (due to residual average mismatch charge), there is also a current flow through tissue. The current will flow from the higher-charge point to the lower-charge point. It should be noted that in the charge balancing process, the switches S_1 , S_2 , S_3 , and S_4 are first closed and then the CB switch closed to avoid spikes on the switches (it will be explained in the next session). Furthermore, it is worth mentioning that in the proposed method, the electrodes are not directly connected to the ground. Shortening the electrodes directly to the ground may lead to an instantaneous large-current spikes, especially when the residual voltage is high. Thus, in the proposed method, the high output impedance current mirror is performed, acting as high-resistor (impedance) which removes the potential of spikes happening. Fig. 4(b) shows the proposed charge balancing method. Also, in order to prevent large current spikes during the switched discharge process, a current-limited discharge circuit has been provided to control discharging in particular for improved a high voltage application. The limiting currents

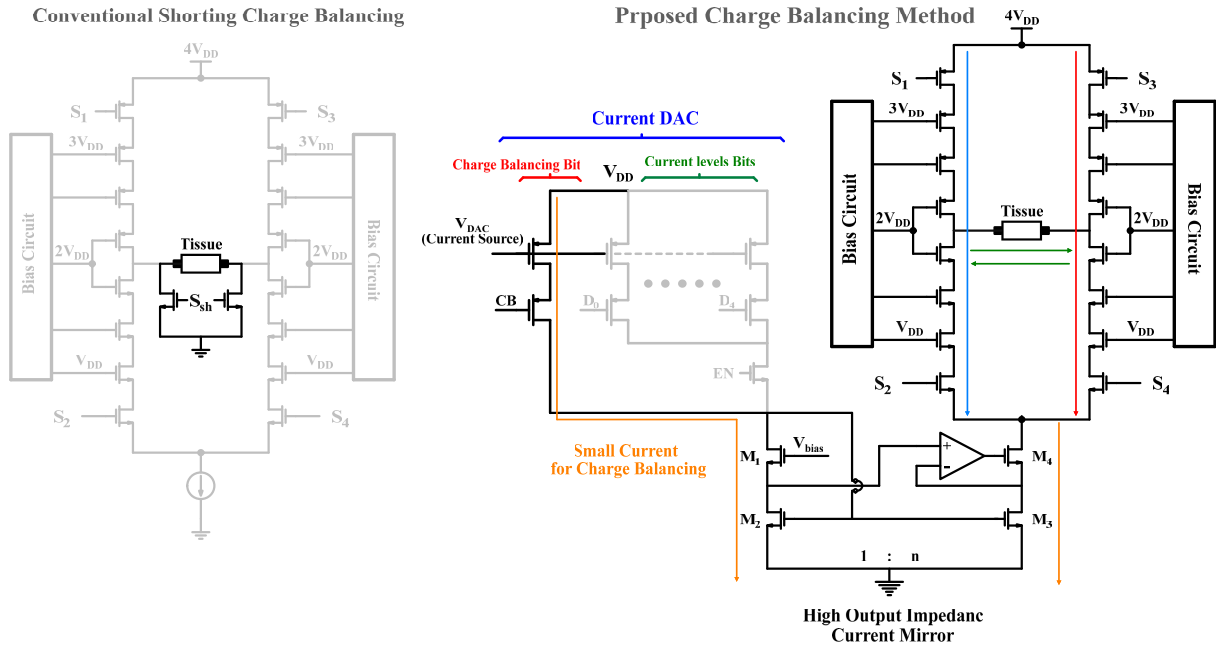


FIGURE 4. (a) Conventional electrode shorting and (b) the proposed method for charge balancing.

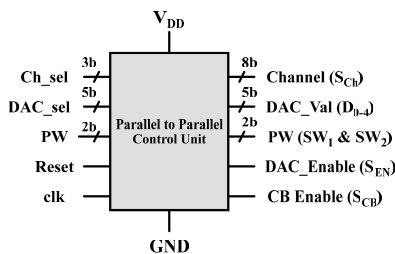


FIGURE 5. Block diagram of the proposed parallel to parallel controller including input and output pins.

can be set by turning on the charge balancing bit (CB) in the DAC as shown in Fig. 4(b). The size of the CB switch is considered to be as small as possible to reduce the power consumption of the stimulator and improves efficiency. The current level is set to be $100 \mu\text{A}$ while the charge balancing time is $700 \mu\text{s}$. The charge balancing time is fixed and for all the pulse widths has the amount of $700 \mu\text{s}$.

E. CONTROL UNIT

One of the critical components of the stimulator system is the control unit (CU). The CU is responsible for controlling the various parts and switches within the stimulator system based on the input command. The stimulator operates by turning the switches on and off to generate the desired stimulation waveform. The CU governs parameters such as pulse width for both the cathodic and anodic phases, pulse interval, interphase delay, current amplitude, and charge balancing phase.

Fig. 5 shows the input and output of the CU. Three input bits dedicated to channel selection (Ch_sel), five bits for

adjusting the stimulus current amplitude (DAC_sel), two other bits for control of the HVTs. In addition, there are three pins for Reset, Clock (clk), and V_{DD} . Reset pin can be used to clear any internal registers or flip-flops and return the control unit to a known state and clock pin synchronizes the operations within the control unit, allowing actions to be performed on each clock cycle. Output pins consist of 8 bits for channel selection (S_{Ch}), 5 bits for controlling the current amplitude (D_{0-4}). A pin (S_{EN}) is considered for the current amplitude outputs.

This pin enables or disables the current amplitude outputs based on the control signal generated by the control logic. These outputs drive the selected channel, enabling the desired functionality specific to that particular channel (allowing for potential expansion to accommodate multiple channels).

Additionally, 5 outputs are allocated for controlling the current amplitude (D_{0-4}). To control the switches and determine the pulse width duration, 2 outputs are utilized (SW_{1-2}). These outputs drive the switches and facilitate the adjustment of the desired pulse width for the selected channel. Finally, an output is designated for charge balancing (S_{CB}). This output controls the charge balancing functionality, ensuring balanced charging of the selected channel.

F. SEQUENCE OF CONTROL SIGNALS

The sequence of control signal generated by the CU is a crucial factor for the proposed neurostimulation. By generating the appropriate output control signals for controlling the switching of each component in the stimulator system, it is possible to mitigate voltage spikes during the stimulation process. Fig. 6 depicts the block diagram of the stimulator system, including all the controllable switches such as the



1. The DAC value for the current level (D_{0-4}) is set, and following a delay ($1\mu s$), the EN signal activates switch S_{EN} . The stimulation current is generated by the current mirror as it flows through S_1 and S_3 to create the first phase of the stimulation (cathodic). During this step, the switches remain on according to the pulse width.
2. To generate the interphase delay, S_{EN} is initially opened, and after a short delay ($1\mu s$), switches S_1 and S_3 are turned off. The switches remain open according to the duration of the interphase delay.
3. The next step involves generating the second phase of stimulation (anodic). Initially, switches S_2 and S_4 are closed by the control signals (SW_{1-2}). The DAC value for the current level (D_{0-4}) is set. Then, after a short delay ($1\mu s$), S_{EN} is closed. Consequently, the current flows through S_2 and S_4 to generate the anodic phase.
4. The subsequent step is the charge-balancing phase. Initially, all switches are turned off. Then, after a delay,

In this work, the level shifter introduced in [37] is utilized in the proposed electrical neurostimulator. The level shifter plays a crucial role in adding a specific DC level to the control signal. The input pulse signal, generated by the control unit, changes between 0 and V_{DD} . By employing the level shifter, a DC voltage of $(n-1)V_{DD}$ is added to the input

signal, resulting in signal levels ranging from $(n-1)V_{DD}$ to nV_{DD} . This modified pulse signal is essential for controlling the upper PMOS switches. The bulk terminals of the MOS devices in the level shifter are connected to the source using the deep n-well structure.

IV. EXPERIMENTAL RESULTS

The proposed electrical neurostimulator, which is composed mainly of two chips, has been designed and fabricated using TSMC 180nm 1.8V/3.3V LV CMOS technology. Fig. 8 shows the microphotograph of both chips forming the stimulator. These stimulation and control unit chips occupy areas of 1.7mm^2 and 0.95mm^2 , including the pads, respectively. However, the main core of the stimulator and control unit, measures 0.181mm^2 and 0.108mm^2 , respectively.

A. ELECTRICAL VERIFICATION

The measured output waveforms of the proposed control unit for one cycle are shown in Fig. 9. The clock frequency used for this measurement is set to 1MHz. The total power consumption of the control unit circuit under 2.75V supply voltage is $35\mu\text{W}$. As depicted in Fig. 9, the sequence and order of turning on for the stimulator switches can be observed which introduces the ZCS method. The delays between switch activation and deactivation are considered to be between 1 and $5\mu\text{s}$, which can ensure that the other switch turns on/off completely.

To evaluate the output result of the proposed stimulator, the common electrode-tissue model is utilized for in vitro testing, which includes a $1.7\text{k}\Omega$ resistor in series with a parallel 100nF capacitor and $10\text{M}\Omega$ resistor [19]. Fig. 10 shows the test bench setup of the whole stimulation system. The electrical neurostimulator was assembled together with a miniature control PCB to run the in vitro testing. Fig. 11 illustrates the measured output voltages of the proposed stimulator for different current stimuli.

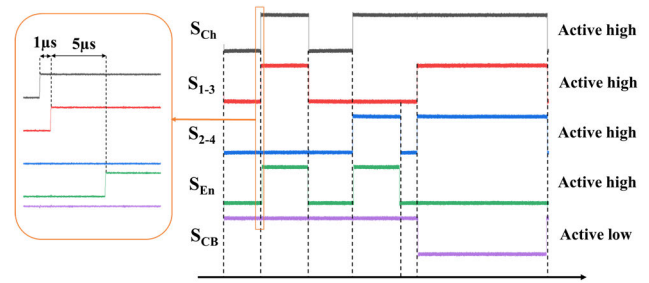


FIGURE 9. Measured control unit performance for one stimulation cycle.

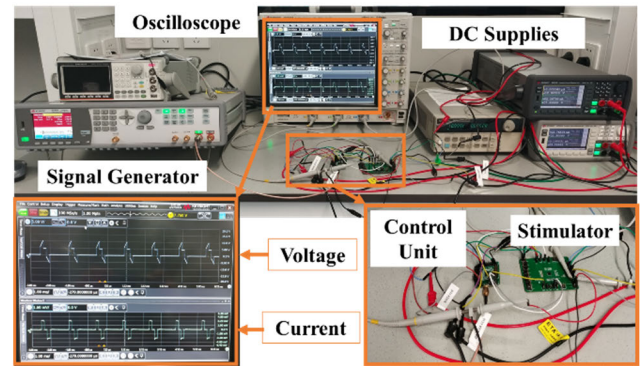


FIGURE 10. Test bench of the proposed stimulator with control unit.

current is achieved by activating all 5 bits in the current DAC and the current gain (CG) pin in the current source. In this case, the current DAC outputs a current of $400\mu\text{A}$. The output transistors of the current mirror are appropriately sized to mirror 8 times the current from the DAC ($8 \times I_{DAC}$). Also, the output current waveform of 3.2mA is shown in Fig. 12 which represents the maximum stimulation current the device can reach. Based on measurement results for the proposed stimulator, the total maximum power consumption of the circuit is about $90\mu\text{W}$ during the highest current stimulation

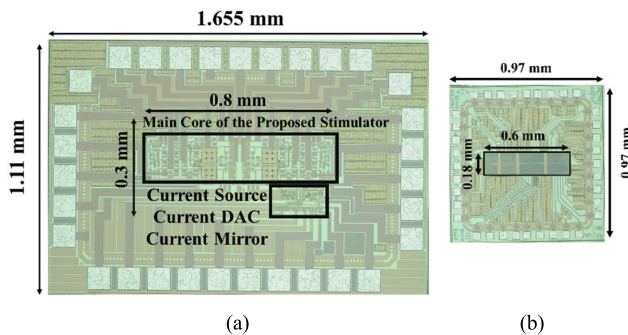


FIGURE 8. Microphotograph of the fabricated implants parts: (a) stimulator and (b) control unit.

The results shows that the voltage compliance at the output can reach 10.2V under a power supply of 11.2V (The supply voltage for the design is considered to be 2.8V). This indicates that the headroom voltage is 1V as the active cascode circuit is employed to implement the current mirror. The highest

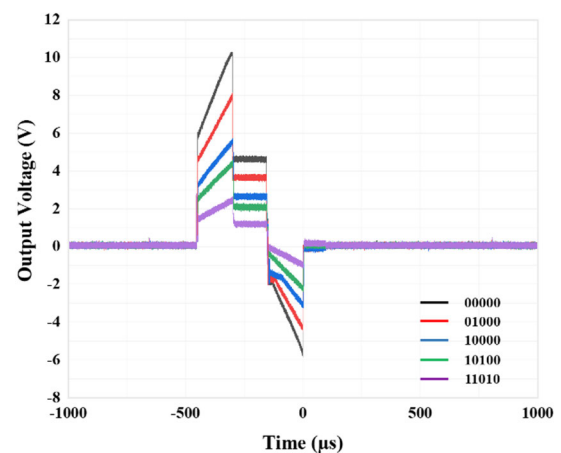


FIGURE 11. Measured stimulator output voltages considering different stimulus currents.

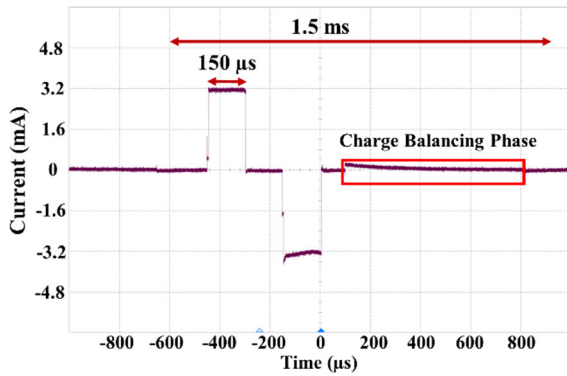


FIGURE 12. Example of a measured stimulation current waveform.

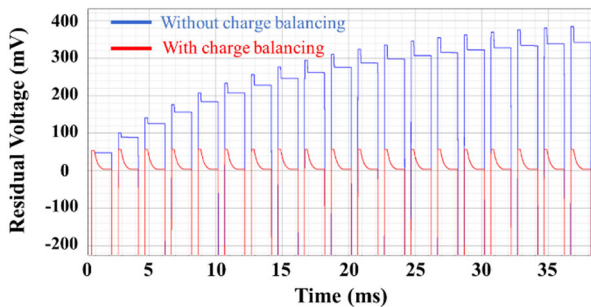


FIGURE 13. The residual voltage on the tissue before (blue) and after (red) applying the charge-balancing technique.

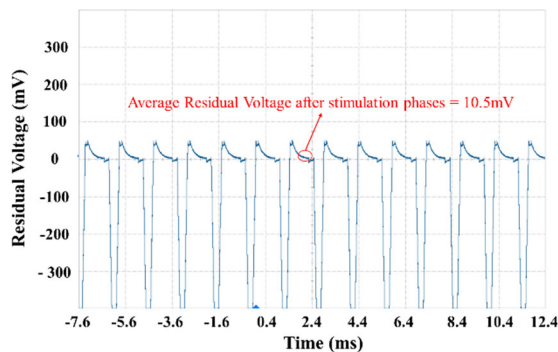


FIGURE 14. Measured residual voltage at 3mA stimulus current.

Fig. 13 compares the residual voltage on the tissue before (blue) and after (red) applying the charge-balancing method. The capacitive part of the tissue causes this residual voltage. The proposed charge-balancing method significantly reduces the residual voltage on the tissue for each cycle. Fig. 14 presents the measured residual on a 100nF capacitor at a stimulus current of 3.2mA for biphasic stimulation. As shown in Fig. 14, the average residual voltage for the biphasic stimulation is 10.5mV, which falls within the safety limit of approximately $\pm 100\text{mV}$ [26]. Based on the pulse width of $150\mu\text{s}$, for highest current the injected charge for one biphasic stimulation can be calculated as $3200\mu\text{A} \times 150\mu\text{s} = 480\text{nC}$. According to the average residual

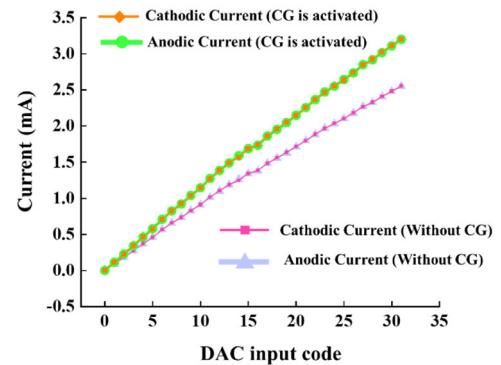


FIGURE 15. Cathodic and anodic current versus DAC inputcode.

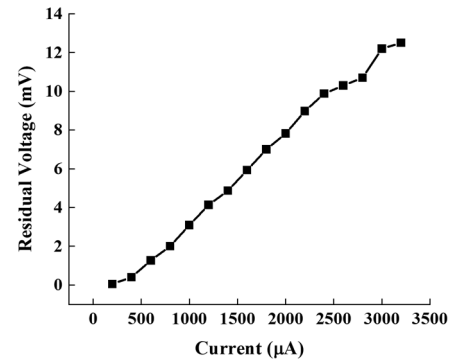


FIGURE 16. Measured residual voltage versus the injected current.

voltage, the charge error is $10.5\text{mV} \times 100\text{nF} = 1.05\text{nC}$. Therefore, the charge mismatch is about $1.05/480 = 0.21\%$ and the time constant (RC) is $1.7\text{k}\Omega \times 100\text{nF} = 170\mu\text{s}$. Since it takes $4 \times RC$ to discharge the capacitor to have a charge-balanced stimulation, the time of the balancing phase is $700\mu\text{s}$.

Fig. 15 illustrates the output current for both the anodic and cathodic phases when the CG bit is activated and deactivated. The results show good linearity between the output currents and the input bits of the current DAC. Additionally, the current mismatch between the two phases is negligible. Fig. 16 demonstrates the measured residual voltage on the tissue as a function of the injected current. Fig. 16 indicates that the residual voltage increases with the increment of the output current, reaching its maximum when the current reaches $3200\mu\text{A}$. For smaller currents, the residual voltage is reduced, leading to a decrease in charge error upon operating in low current levels.

To ensure the long life and reliability of the chip, it was kept turned on for 12 hours with the highest current (3.2mA) and a period of 1.5ms under 11.2V power supply. This resulted in the generation of 29 million periodic stimulation cycles. Based on the measurements, the variation in the output current, output voltage, and residual voltage was negligible, indicating stability over this extended testing period. The residual voltage after 12 hours and 29 million stimulation cycles was found to be less than 11mV .

TABLE 1. Performance comparison with the stat-of-art publications.

Reference	[12]	[19]	[20]	[21]	This work
Year	2023	2023	2024	2024	2025
Technology	0.18 μm LV CMOS	65 nm CMOS	0.18 μm LV CMOS	0.18 μm LV CMOS	0.18 μm LV CMOS
Supply Voltage (V)	± 6	11	9	≈ 20	11.2
Current (mA)	± 3.6	0 ~ 0.16	0 ~ 0.07	0 ~ 1	0~3.2
Output Voltage (V)	± 3.6	10.4	7.5	16.5	10.2
Charge Mismatch (%)	0.926	N/A	1.73	2.7	0.21
Residual DC Current (nA)	163	95	123	38	13.4
Area (mm ²)	0.052	0.0141	0.024	0.83	0.181
FOM ($\times 10^6$)	0.0132	0.0016	0.0004	0.022	0.217

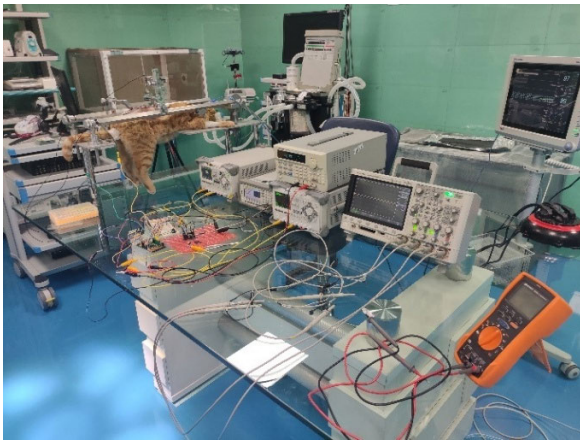
**FIGURE 17.** Experimental setup for restoring motor function using intraspinal microstimulation by the fabricated chip.

Table 1 provides a comparison of the performance of the proposed stimulator with other similar works. The main parameters and characteristics of the stimulators are shown, allowing for a comprehensive evaluation. The current and voltage compliance of the proposed stimulator are comparable to those of other recent works. The stimulator achieves a high voltage compliance of 10.2V, which indicates its ability to provide a sufficient voltage output to the tissue. Additionally, it generates a high current of 3.2mA, suggesting its capability to deliver substantial stimulation currents. Furthermore, the proposed stimulator demonstrates the best results in terms of charge mismatch among all the reported stimulators, even without employing the electrode shortening method. This indicates that the stimulator achieves a high accuracy level in delivering the desired charge to the tissue. A figure of merit (FOM) is defined to evaluate performance of the design as follows:

$$FOM = \frac{V_{OP} \times I_{Stim}}{V_{Supply} \times I_{DC}} \quad (7)$$

where V_{OP} , I_{Stim} , V_{Supply} and I_{DC} are operating voltage maximum stimulation current, supply voltage, and Residual DC Current, respectively. Note that a larger FOM indicates a better performance. Based on the FOM, the proposed stimulator has better performance than the recent work in total.

B. ANIMAL EXPERIMENTS

The experiments were conducted on the spinally-intact adult cat (domestic short hair, 2.5–4.0 kg body weight). All surgical procedures and experimental protocols involving the use of animal models in this study are approved by the Animal Care and Ethics Committee of Iran Neural Technology Research Centre with IACUC number INTC-2024-0018. Moreover, the study is carried out in compliance with the ARRIVE guidelines.

The cat was initially anesthetized with ketamine (20 mg kg⁻¹) injected intramuscularly into the cranial thigh muscle. The animals were then intubated and maintained at a surgical level of anesthesia with isoflurane (1.0%–3.0% in O₂). Blood oxygen saturation level (SpO₂) and heart rate signals were monitored continuously throughout the surgical process and experimental tests. A partial dorsal laminectomy was performed to expose the L4–S1 segments, the dura mater of dorsal surface of the spinal cord was opened with iridectomy scissor, and the spinal cord was covered with saline to prevent its dehydration. The cat was positioned in a modified stereotaxic setup (SN-1N, Narishige Group Product) which allows the hindlimbs to hang free while the head and spinal vertebrae (L3 and L7) are clamped rigidly to the frame. In the weight-bearing tests, the bilateral hindlimbs of the animals were positioned on split-belt motorized treadmill. The lower-limb motion was estimated by DeepLabCut [55]. The experimental setup is shown in Fig. 17.

The stimulus microelectrode was implanted into at the base of the ventral horn of the L4–L5 segments. The electrodes were made from epoxy lite-insulated tungsten microelectrodes (length range 61–70 mm, impedance range

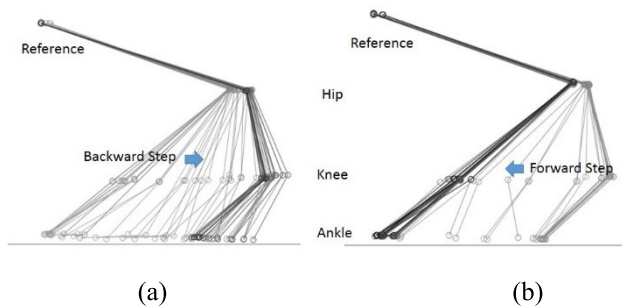


FIGURE 18. Step-like movement generated by ISMS using proposed neuro-stimulator. (a) Backward Step. (b) Forward Step.

50–100 k Ω , shank diameter 125 μm , 15–20° tapered tip, and rounded tip with ~ 3 -micron diameter at the tip; serial: UE WMEFSEANNF, FHC Inc., Bowdoin, ME, USA). The spinal cord was stimulated with pulse amplitude modulation at a constant frequency (50 Hz) and constant pulse width (250 μs). The amplitude was monotonically increased from 100 μA to 500 μA with a 100- μA steps and then decreased to 100 μA . The stimulation duration is 1 s at each step.

Fig. 18 shows the step-like movements produced by the ISMS using the fabricated neurostimulator chip of the proposed design in this work. The circles show the markers placed to the ankle, knee, hip, and a reference during measuring the movement trajectory using DeepLabCut. Fig. 18 (a) shows the forward step of step-like movement during different trials of experiment and Fig. 18 (b) shows the backward step. A short step-like movement generated by ISMS using proposed neuro-stimulator can be seen in the video (Supplementary Movie).

V. CONCLUSION

A high-current and high-voltage compliance electrical neurostimulator that was implemented using TSMC 180nm 1.8V/3.3V LV CMOS technology has been proposed. The proposed system utilized a novel method for charge balancing without the need for any extra circuit based on considering a new switching method for the stimulator. It resulted in a low charge mismatch of 0.21%. To prevent current spiking (or glitch) and potential tissue damage, smooth ON/OFF transitions utilizing gate driver and ZCS approaches have been employed. The neurostimulator allows to achieve a high-voltage compliance of 10.2V and delivers a maximum current of 3.2 mA. In this work, the application of the fabricated chip in ISMS for restoring motor function is demonstrated. However, the neurostimulator can be used for deep brain stimulation for treatment of Parkinson's disease and for control of epileptic seizures. It has been demonstrated that the proposed neurostimulator is able to successfully produce lower-limb movements through ISMS of the cat lumbar spinal cord.

ACKNOWLEDGMENT

The authors would like to acknowledge funding support from Westlake University.

CONFLICT OF INTERESTS

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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