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A Low-Power, Low-Noise Recycling Folded-Cascode Operational Transconductance Amplifier for Neural Recording Applications

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Abstract: We present in this paper a low-noise, low-power CMOS operational transconductance amplifier designed for the preconditioning stage of implantable neural recording microsystems. The proposed single-stage amplifier utilizes a combination of recently published techniques, including cross-coupled devices in a recycling folded-cascode topology with positive feedback, to achieve high DC voltage gain and unity-gain bandwidth while minimizing power consumption. A mixed N-type and P-type MOSFET input stage enhances input common-mode performance. Designed and implemented in a 0.18- μm CMOS process with a 1.8 V supply, post-layout simulations demonstrate an open-loop voltage gain of 97.23 dB, a 2.91 MHz unity-gain bandwidth (with a 1 pF load), and an input-referred noise of 4.75 μV_{rms} . The total power dissipation, including bias circuitry, is 5.43 μW , and the amplifier occupies a chip area of 0.0055 mm². Integrated into a conventional neural recording amplifier configuration, the proposed amplifier achieves a simulated input-referred noise of 5.73 μV_{rms} over a 1 Hz to 10 kHz bandwidth with a power consumption of 5.6 μW . This performance makes it suitable for amplifying both action potential and local field potential signals. The amplifier provides an output voltage swing of 0.976 V_{pp} with a total harmonic distortion of −62.68 dB at 1 kHz.

Keywords: implantable microsystem; neural signals; neural amplifiers; low-power and low-noise operational amplifier; recycling folded-cascode



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1. Introduction

The recording of brain activities is increasingly important across various fields, including neuroscience research, neural disease diagnosis and treatment, and neuroprosthetics [1–6]. An implantable neural recording microsystem typically consists of recording microelectrode arrays (MEAs), a signal preconditioning module (analog front-end amplifier), a neural processing unit, and a wireless interfacing module (Figure 1a). The analog front-end amplifier is essential for amplifying weak neural signals and filtering out unwanted frequencies. Extracellular neural signals generally have amplitudes up to 1 mV, concentrated in the 0.1 Hz to 10 kHz range (Figure 1b) [7–9]. These signals include action potentials (APs), indicating the firing of individual neurons, and local field potentials (LFPs), representing grouped neuronal activity. Effective analysis often requires separating LFPs (0.1 Hz to 100 Hz) from APs (100 Hz to below 10 kHz) through preamplification and linear filtering [7–9].

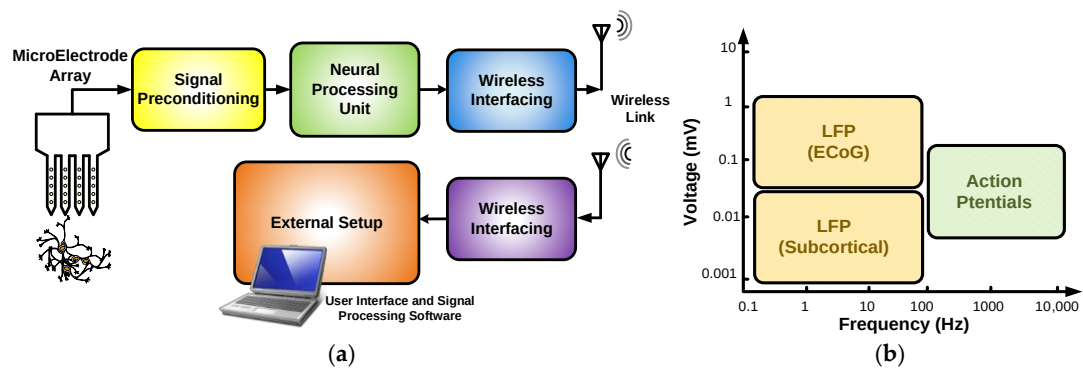


Figure 1. (a) Simplified block diagram of an implantable neural recording microsystem. (b) Amplitude and frequency characteristics of recorded neural signals.

As stated above, the neural signal preconditioning module is essential for amplifying and filtering signals in implantable biomedical microsystems, typically using a preamplifier and a bandpass filter. In some cases, the voltage gain and cut-off frequencies of the signal preconditioning module can be adjusted or programmed. Key attributes of this module include the ability to amplify signals within a specific frequency range, low input-referred noise (IRN) for detecting small spikes, minimal off-chip components to reduce size, and a wide dynamic range for capturing spikes and LFPs ranging from $\pm(1\text{--}2)$ mV in amplitude at its input terminals. It should also have a high common-mode rejection ratio (CMRR) to reduce power line noise interference and a robust power-supply rejection ratio (PSRR) to handle power supply noise [9]. Additionally, the input impedance must exceed that of the electrode–tissue interface to avoid signal loss. Consequently, given these existing trade-offs, designing fully integrated neural recording amplifiers and their building blocks, including operational transconductance amplifiers (OTAs), that meet these requirements (low voltage, low power, minimal area, and low IRN) is a significant challenge. In fact, as shown in Figure 2, it is important to recognize that design parameters frequently involve trade-offs with one another, transforming the design process into a complex, multi-dimensional optimization task. Effectively addressing these challenges demands a blend of intuition and expertise to achieve a balanced and acceptable compromise [10]. Table 1 summarizes the requirements of neural recording applications and shows the performance requirements for OTAs in these applications [1,3].

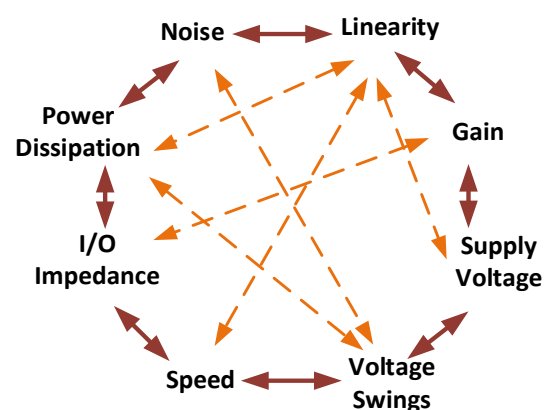


Figure 2. Analog design octagon [10].

Table 1. Target specifications of OTAs to be used in neural recording systems.

Parameter	Target Specifications
Silicon Area (per channel)	$<0.05 \text{ mm}^2$
Power (per channel)	$<50 \text{ } \mu\text{W}$
Bandwidth	Related to signal type (a few MHz are more than enough)
IRN (per channel)	$<10 \text{ } \mu\text{V}_{\text{rms}}$
CMRR	$>80 \text{ dB}$
Input Impedance	$>100 \text{ M}\Omega$
Voltage Gain	$>60 \text{ dB}$

A variety of circuit techniques and structures have been developed to enhance the performance of OTAs for use in neural recording amplifiers. Each of these approaches aims to improve one or more of the design requirements, such as improving voltage gain and circuit linearity, reducing circuit noise and power consumption, as well as the chip silicon area. Regarding circuit noise reduction, various approaches have been reported. In general, the overall noise of an OTA is a combination of thermal and flicker noise. Flicker noise, often referred to as $1/f$ noise, is particularly critical for circuits designed for low-noise, low-frequency operation at relatively modest frequencies [11]. Besides the size of transistors and their operating points, the polarity of transistors also plays a significant role in noise performance. In the realm of neural signal amplifiers, P-channel input MOSFETs are commonly favored over their N-channel counterparts due to their inherent advantages. These include a reduced common-mode (CM) input voltage level, diminished low-frequency noise, and a higher upper -3 dB frequency, particularly when employed in cascode topologies. This combination of attributes results in an extended unity-gain bandwidth, making P-channel MOSFETs an attractive choice for applications demanding high-performance analog front-ends [12,13]. It is important to note that this polarity-based noise difference is not universal across all fabrication processes. While input transistors significantly contribute to the IRN, an inadequately designed circuit can lead to the noise from load transistors being amplified by the transconductance ratio. Hence, it is essential for designers to consider the noise of all transistors employed in the circuit design [14].

To minimize power consumption, circuit noise, and consumed silicon area, various techniques have been employed in previous studies. For example, the CMOS amplifier proposed in [15] aims to optimize area efficiency for neural recording by utilizing indirect negative feedback, resulting in a low -3 dB cutoff frequency. This allows for minimal capacitance, easily implementable on-chip. Additionally, the circuit proposed in [15] incorporates attenuators within the feedback loop to further decrease the silicon area required for capacitors while enhancing the circuit's input impedance. The work presented in [16] aims to design a high-gain recording read-out circuit with a minimized noise efficiency factor (NEF) by biasing the system in the subthreshold region to lower power consumption, even at high supply voltages. Key contributions include developing a low-power, low-noise neural signal recording circuit; achieving high linearity in signal digitization at a low sampling rate; and creating a graphical user interface for signal processing and analysis. In [17], source degeneration was applied to a double recycling folded-cascode (RFC) amplifier to lower IRN, although this method also resulted in a reduced output swing and voltage gain. Additionally, studies in [18–20] explored the use of chopper amplifiers with positive feedback to meet noise specifications and address the low

input impedance characteristic of chopper amplifiers. However, these amplifiers necessitate a clock and supplementary circuits, which can increase both power consumption and overall complexity. In [21], the implementation of current splitting and scaling techniques in a current mirror OTA has resulted in an improved trade-off between power and IRN. However, this also leads to an increase in chip area and voltage headroom requirements. The open-loop amplifier presented in [22] boasts a low NEF alongside high CMRR and PSRR. However, open-loop configurations exhibit greater sensitivity to process, voltage, and temperature variations compared to closed-loop designs, resulting in diminished linearity. In [23], a fully differential amplifier is introduced, which combines an instrumental amplifier with a programmable voltage gain amplifier. However, the inherent asymmetry in the instrumental amplifier structure significantly compromises the amplifier's linearity.

This work presents a low-noise, low-power amplifier utilizing an RFC architecture for neural recording applications. To enhance performance and reduce chip area, the input stage employs a combination of N-type and P-type MOSFETs compared to conventional all-P-type designs. The incorporation of recycled current and cross-coupled transistors with positive feedback significantly improves voltage gain, DC performance, unity-gain bandwidth, and overall circuit linearity. The remainder of the article is structured as follows. Section 2 introduces the CMOS RFC OTA, emphasizing its recent advancements. Section 3 explores the structure and analysis of the proposed fully differential RFC amplifier, providing a thorough comparison with the conventional folded-cascode amplifier. Section 4 presents the circuit-level post-layout simulation results, including the integration of the designed OTA into a standard neural recording amplifier (NRA) structure. Finally, Section 5 offers the concluding remarks of the paper.

2. Introduction to CMOS RFC OTA

The OTA is a common component in integrated circuits that are designed to handle large output loads, typically in the form of capacitors rather than resistors. OTAs are frequently used in neural recording circuits. These amplifiers can be implemented through single-stage, two-stage, or multi-stage designs. While multi-stage amplifiers can significantly boost DC gain, their stability in closed-loop configurations can be a major issue. Frequency compensation methods can be employed to establish a dominant pole and ensure stability with a sufficient margin [24]. However, these techniques unavoidably decrease the unity-gain bandwidth and speed of the OTA. Additionally, the analysis and design of multi-stage amplifiers can be complex. Single-stage OTAs inherently exhibit a dominant real pole, eliminating the need for complex frequency compensation techniques. This inherent stability stems from the presence of a single high-impedance node within the signal path. This characteristic renders single-stage OTAs highly suitable for closed-loop applications. Two prominent architectures for single-stage OTAs are the telescopic-cascode and the folded-cascode topologies. While the telescopic-cascode OTA offers superior performance in terms of speed, DC gain, and reduced IRN and power consumption, the folded-cascode configuration exhibits a distinct advantage in low-voltage scenarios. Its reduced power supply voltage requirement and enhanced output voltage swing make it a more viable option in modern CMOS technologies where supply voltages have dwindled below one volt. In such low-voltage regimes, the output voltage swing of the telescopic-cascode OTA becomes severely limited, rendering it impractical for most applications [24].

The circuit diagram in Figure 3 illustrates the structure of a fully differential RFC OTA as described in reference [24]. In this design, the input devices are divided into M_1 , M_2 , M_{1a} , and M_{2a} to utilize the idle M_3 and M_4 current source transistors from the conventional folded-cascode amplifier in the signal path. Essentially, the RFC amplifier consists of a conventional folded-cascode amplifier and a current-mirror OTA. The conventional

folded-cascode amplifier is constructed using M_1 – M_{11} transistors, while the current-mirror OTA is formed by M_{1a} , M_{2a} , and M_{3-11} devices. According to [24] the RFC OTA offers several advantages over the traditional folded-cascode design, such as improved unity-gain frequency and slew rate (SR). Additionally, the DC gain is more than doubled due to lower bias current in the output transistors, which results in higher output resistance. However, this structure may experience a decrease in phase margin due to additional poles. Despite this, the reduction in phase margin may be beneficial for fast-settling applications, where a phase margin of 60 to 70 degrees is ideal, even though the standard folded-cascode OTA typically has a large phase margin of over 80 degrees. In recent years, numerous researchers have focused on enhancing the circuit characteristics of folded-cascode OTA and its more recent variant, the RFC one. The following paragraphs provide a brief overview of several noteworthy circuits that have been developed.

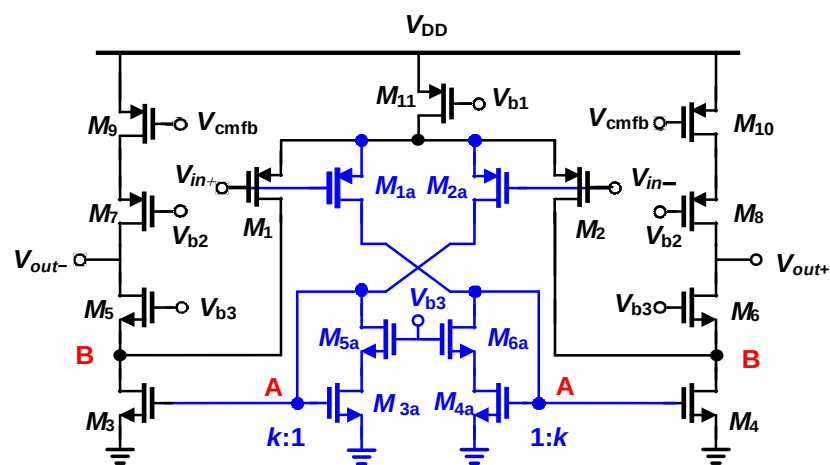


Figure 3. Fully differential RFC OTA [24].

Ref. [25] introduced a two-path OTA by dividing the input transistors of a conventional telescopic-cascode design, combining elements of both telescopic-cascode and folded-cascode architectures. Building upon this, a fully differential recycling telescopic-cascode OTA is presented in [26]. This design incorporated an additional current-mirror OTA by splitting the input transistors while also employing current recycling, cross-coupled transistors, and local positive feedback to improve both small-signal and large-signal characteristics. The design in [27] expands on this concept by splitting the input transistors into three differential pairs to implement a double-RFC OTA. Two of the differential pairs function similarly to an RFC amplifier, while the third pair drives active current mirrors. This innovative arrangement allows for the reuse of shunt bias currents twice, thereby improving OTA performance without incurring additional power or area overhead. The double recycling approach has been further refined in studies referenced in [28–30]. A constant-gm rail-to-rail OTA based on an RFC architecture was proposed in [31]. To improve SR, ref. [32] introduced additional signal paths in a fully differential RFCA. Subsequently, ref. [33] employed complementary input pairs for enhanced gain-bandwidth. Asymmetrical current splitting in a single-ended RFCA was investigated in [34] to boost small-signal transconductance and DC gain. Furthermore, ref. [35] introduced local positive feedback to a conventional folded-cascode OTA, resulting in improved DC gain, gain-bandwidth, and SR compared to traditional and some advanced recycling designs. Building upon this, ref. [36] presented a bulk-driven double-RFC OTA for biomedical applications, leveraging positive feedback and self-biased cascode transistors to enhance performance at lower supply voltages.

In reference [37], a fully differential Class A single-stage OTA is presented for high-speed switched-capacitor applications. The authors aimed to optimize both large- and small-signal performance by incorporating several innovative techniques: current recycling, enhanced phase margin through high-speed current mirrors, and cross-coupled local positive feedback transistors. This multi-pronged approach enabled the realization of fast-settling performance with sufficient accuracy while minimizing power dissipation. A single-stage Class AB OTA, featuring a symmetric design and a significantly enhanced SR, was reported in [38]. The input stage of this RFC amplifier employs floating gate voltage cells to facilitate Class AB operation. To further augment the SR, the output stage incorporates nonlinear current mirrors and self-biasing techniques. This design achieves an impressive SR, approximately 15 times greater than that of a conventional folded-cascode amplifier, albeit at the cost of slightly increased power dissipation. Furthermore, an adaptive biasing Class AB input stage, utilizing flipped voltage follower (FVF) cells and local common-mode feedback (CMFB) techniques, was implemented to realize a single-ended RFC OTA in [39]. This approach led to notable improvements in both small-signal transconductance and SR. In [40], a single-ended class AB amplifier was introduced that achieved optimal performance in terms of SR and small-signal parameters through adaptive biasing and local common-mode feedback techniques. Additionally, dynamic biasing of cascode transistors using quasi-floating gates was utilized to enhance performance. In [41], various configurations based on this technique were proposed. In [42], a fully differential class AB RF amplifier with adaptive input biasing and an auxiliary amplifier was introduced to improve DC gain. In [43], a multi-path fully differential bulk-driven class AB OTA utilizing FVF cells for class AB operation was proposed, resulting in improved small-signal performance and SR in weak inversion. Finally, in [44], a single-ended bulk-driven class AB OTA combining a double-RFC amplifier with FVF cells and partial positive feedback was suggested.

3. Proposed Fully Differential RFC OTA

Figure 4a illustrates the presented RFC OTA architecture, which can be considered as a modified version of the amplifier presented in [26]. The transistors M_1 – M_{11} correspond to their counterparts in a conventional folded-cascode design, which is also shown in Figure 5. The input stage, comprising M_{1a} , M_{1b} and M_{2a} , M_{2b} devices, is divided for efficient current recycling and reduced output transistor biasing current, thereby enhancing output resistance. All input transistors are oversized to minimize flicker noise and operated in the subthreshold region. Unlike traditional approaches favoring P-type MOSFETs for input transistors, the proposed design incorporates both N-type and P-type devices to expand the input range. While P-type MOSFETs are often preferred for lower flicker noise, this assumption is not universally valid, and a poorly designed circuit can amplify noise from load transistors. Hence, the noise contribution of all important transistors should be carefully considered. To create a two-path amplifier, transistors M_{7a} , M_{7c} and M_{8a} , M_{8c} are paired. Transistors M_{5a} and M_{6a} form a cascode current mirror for improved matching, while M_{5b} , M_{6b} , M_{7b} and M_{8b} devices implement a cross-coupled configuration instead of a current mirror to introduce local positive feedback at the gates of M_7 and M_8 devices [45]. The aspect ratio of M_7 family transistors compared to each other, and similarly the aspect ratio of M_8 family transistors to each other, are shown by the coefficients k and m in Figure 4a. Further explanations regarding these coefficients and their relationship to each other will be provided in the following paragraphs.



Figure 4. (a) Proposed single-stage RFC OTA. (b) Biasing circuit.

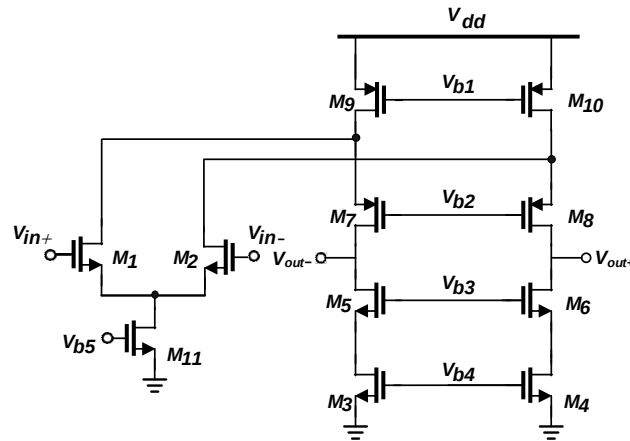


Figure 5. Conventional folded-cascode OTA.

As mentioned above, to minimize power consumption and IRN, the input devices were biased in the subthreshold region by maximizing their transconductance and dimensions. This approach concurrently reduced transistor mismatch, enhancing common-mode parameters like CMRR and PSRR while lowering input-referred offset voltage. The biasing voltages V_{b1} through V_{b5} are supplied by a constant current biasing circuit with an ideal current source, which is shown in Figure 4b. Wide-swing cascode current mirrors are used to improve the matching between biasing and main transistors without the swing reduction at the output node of the designed amplifier [26].

In the presented circuit, the bias values and dimensions of the devices used in the conventional folded-cascode amplifier are selected in such a way that the following equation holds for the currents of transistors M_{1a} , M_{7a} , M_{2a} , and M_{8a} :

$$\begin{cases} I_{d1a} = I_{d7a} = 0.5I_{d9} \\ I_{d2a} = I_{d8a} = 0.5I_{d10} \end{cases} \quad (1)$$

The parameters k and m can be selected independently. However, if the relationship $k = m + 1$, as suggested in reference [26], is satisfied, then for the currents flowing through the transistors used in the proposed symmetric circuit, as well as their corresponding transconductance, the following relationships hold:

$$\begin{cases} I_{d7b} = \frac{m}{k} I_{d7a}, & g_{m7b} = \frac{m}{k} g_{m7a} \\ I_{d8b} = \frac{m}{k} I_{d8a}, & g_{m8b} = \frac{m}{k} g_{m8a} \\ I_{d7c} = \frac{1}{k} I_{d7a}, & g_{m7c} = \frac{1}{k} g_{m7a} \\ I_{d8c} = \frac{1}{k} I_{d8a}, & g_{m8c} = \frac{1}{k} g_{m8a} \\ I_{d1b} = I_{d7b} + I_{d7c} = \frac{m}{k} I_{d7a} + \frac{1}{k} I_{d7a} = (m+1)/k I_{d7a} \\ I_{d2b} = I_{d8b} + I_{d8c} = \frac{m}{k} I_{d8a} + \frac{1}{k} I_{d8a} = (m+1)/k I_{d8a} \end{cases} \quad (2)$$

Given the choice of $k = m + 1$ in the proposed circuit, it can be easily proven that

$$\begin{cases} I_{d1b} = I_{d7a} = I_{d1a} \\ I_{d2b} = I_{d8a} = I_{d2a} \end{cases} \quad (3)$$

To set the output voltage of the presented amplifier to the desired value (V_{cmo}), a CMFB circuit introduced in [26] is utilized. In this design, V_{cmo} is set to $V_{dd}/2$ as the intended output CM voltage by the biasing circuit. As detailed in [26], a single tail current source at the input transistors' sources cannot effectively define the common-mode voltage at the output nodes. This is due to the near-zero voltage gain of the CMFB loop resulting from two opposing CMFB paths. To address this effect, separate tail current sources for the input

transistors are employed in this work. These sources, in conjunction with the negative CMFB loop implemented by the main amplifier, establish the CM voltage at the output nodes. Specifically, transistors M_{13} and M_{14} , identical devices, are utilized at the source of the M_{11} tail current source to form the CMFB circuit. M_{13} and M_{14} operate in the deep triode region, creating a resistance at the source of M_{11} , as follows:

$$R_n = R_{on13} \parallel R_{on14} = \frac{1}{\mu_n C_{ox} \left(\frac{w}{L}\right)_{13,14} (V_{out+} + V_{out-} - 2V_{th,13,14})}. \quad (4)$$

In this context, μ_n represents the mobility of electrons, C_{ox} signifies the oxide capacitance per unit area, and $\left(\frac{w}{L}\right)_{13,14}$ and $V_{th,13,14}$ denote the aspect ratio and threshold voltage of transistors M_{13} and M_{14} , respectively. The operation of the CMFB circuit can be described as follows: A decrease in the common-mode voltage at the output nodes leads to a corresponding increase in the equivalent on-resistance of transistors M_{13} and M_{14} , resulting in a larger voltage drop across these devices. Consequently, the bias current of the M_{11} tail current source decreases. Conversely, the bias current of transistors M_{5a} through M_{8a} is determined by the M_{12} tail current source and the aspect ratio of the current mirror transistors, which remains relatively constant during common-mode operation. As a result, the drain current of M_{3a} and M_{4a} becomes higher than that of M_{5a} and M_{6a} devices. To satisfy Kirchhoff's current law at the output nodes, the CM voltage of the output nodes must increase due to the channel length modulation effect of MOSFETs. This necessitates a negative CMFB loop to regulate the output CM voltages. A similar but opposite scenario occurs when the output CM voltage goes above V_{cmo} . It should be noted that during differential signal amplification of the designed circuit, R_n remains constant, and the CM voltage at the output nodes does not change significantly.

To calculate the DC voltage gain of the presented circuit, Figure 6, which shows the half-circuit differential model of the circuit in AC mode, as well as the small-signal model of the presented circuit in the half-circuit differential model, is drawn. As shown in Figure 6a, four nodes of X, Y₁, and Y₂ and the output voltage in the signal paths have contribution on signal amplification. As indicated in Figure 6a, the signal path from input to output is established through two different routes, denoted by paths 1 and 2. In general, for multi-path amplifiers, such as the two-path configuration presented in this paper, if the voltage gain signs of both paths are identical, the overall voltage gain is indeed the sum of the individual path gains [10]. It is important to note that each signal path may have variations in the number of transistors and other utilized elements, which can introduce zeros in the overall transfer function. By utilizing the small-signal model of Figure 6b (along with acceptable approximations such as ignoring the transistor's body effect) and based on the superposition theorem, the voltage gain of the circuit can be obtained as follows:

$$A_v(s) = \frac{A_1}{\left(1 + \frac{s}{\omega_{out}}\right)\left(1 + \frac{s}{\omega_{Y1}}\right)} + \frac{A_2}{\left(1 + \frac{s}{\omega_{Y2}}\right)\left(1 + \frac{s}{\omega_X}\right)\left(1 + \frac{s}{\omega_{out}}\right)}, \quad (5)$$

where A_1 is the voltage gain of path 1. In the calculation of A_1 , transistor M_{1a} acts as the primary amplifying element, and the voltage gain is calculated based on the principles of a common-source amplifier as follows:

$$|A_1| = g_{m1a} R_{out}. \quad (6)$$

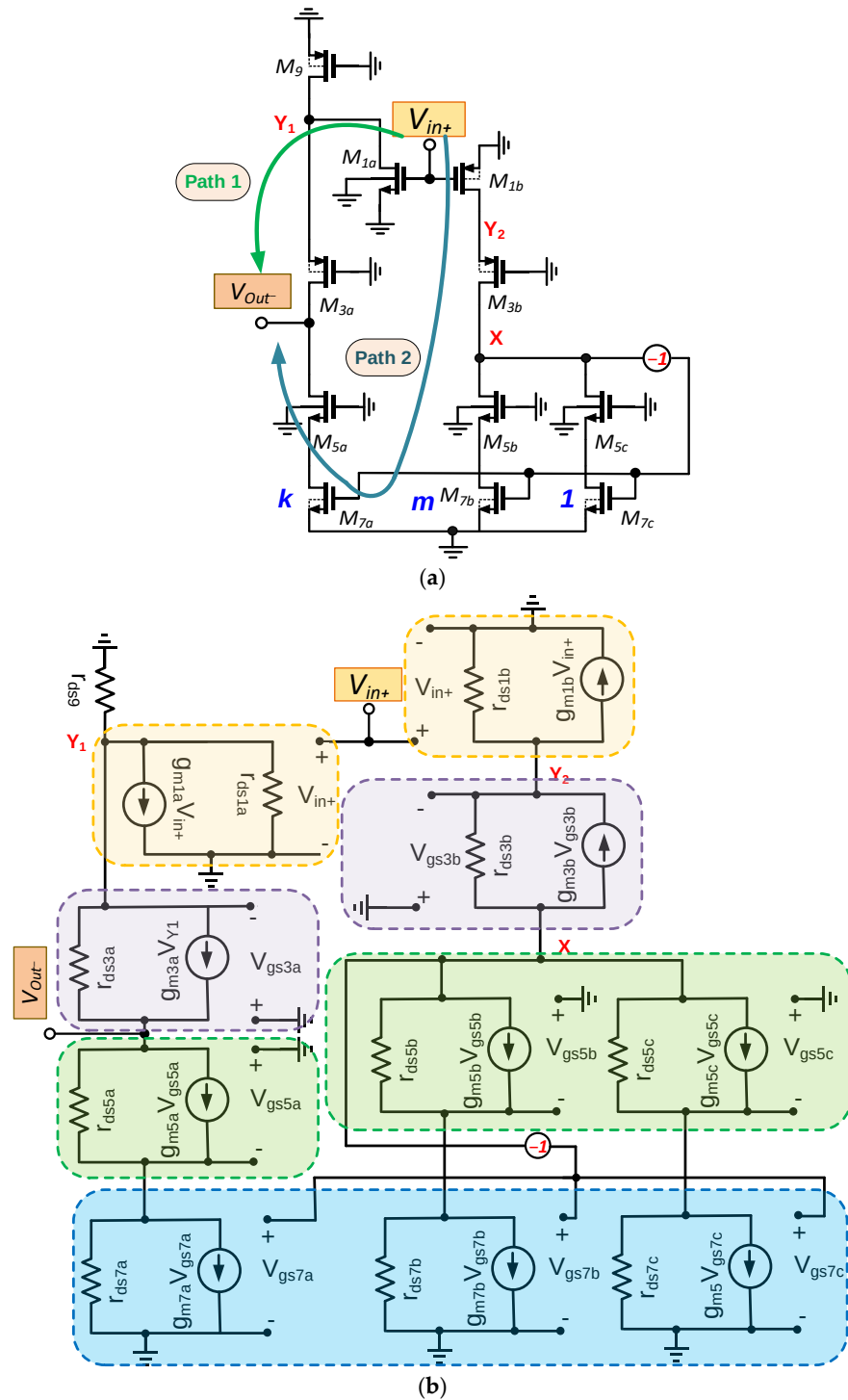


Figure 6. (a) Half-circuit differential model of the proposed circuit in AC mode and (b) its small-signal model.

A_2 in Equation (5) is the path 2 voltage gain. In the calculation of A_2 , a transistor combination involving M_{1b} and M_{3b} devices acting as a cascode structure is encountered. The voltage gain of this section is approximated as the transconductance of transistor M_{1b} multiplied by the resistance seen from node X. Furthermore, due to the signal path extending from node X to the output node, transistor M_{7a} , in common-source configuration, causes the voltage gain of path 2 to be calculated as follows:

$$|A_2| = \frac{V_{out-}}{V_X} \times \frac{V_X}{V_{Y2}} \times \frac{V_{Y2}}{V_{in+}} = g_{m7a} R_{out} \times g_{m3b} R_X \times g_{m1b} \frac{1}{g_{m3b}}. \quad (7)$$

As depicted in Figure 7, the current I_{test} flows through transistors M_{5b} , M_{5c} , and M_{3b} . It is important to note that the contribution of transistor M_{3b} in this current division is represented by the resistance R_{seen} . However, since R_{seen} is significantly larger than the resistances resulting from the currents I_{d5b} and I_{d5c} , its effect can be safely neglected. Consequently, the current I_{test} can be calculated as follows, based on Figure 7:

$$I_{test} = I_{d5b} + I_{d5c} \quad (10)$$

It is evident that the currents in the series transistors, specifically the pairs M_{5b} and M_{7b} , and M_{5c} and M_{7c} , are equal. Consequently,

$$I_{test} = I_{d7b} + I_{d7c}, \quad (11)$$

where

$$\begin{cases} I_{d7b} = g_{m7b} V_{gs7b} - \frac{V_{gs5b}}{r_{ds7b}} \\ I_{d7c} = g_{m7c} V_{gs7c} - \frac{V_{gs5c}}{r_{ds7c}} \end{cases} \quad (12)$$

By neglecting the channel length modulation effect and considering that V_{gs7b} and V_{gs7c} are equal to V_{test} in magnitude, the resistance R_x can be easily calculated as follows:

$$R_x = \frac{1}{g_{m7b}} \parallel \frac{1}{g_{m7c}}. \quad (13)$$

The output resistance of the proposed amplifier can also be calculated by performing some KVLs and KCLs, as described in reference [10], using Figure 6b, as follows:

$$R_{out} = (g_{m3a} r_{ds3a} (r_{ds9} \parallel r_{ds1a}) \parallel g_{m5a} r_{ds5a} r_{ds7a}). \quad (14)$$

Consequently, by combining Equations (13) and (14), A_2 is calculated as follows:

$$|A_2| = g_{m1b} g_{m7a} R_{out} \left(\frac{\frac{1}{g_{m7b} g_{m7c}}}{\frac{1}{g_{m7b}} + \frac{1}{g_{m7c}}} \right) = \left(\frac{k}{1+m} \right) g_{m1b} R_{out}. \quad (15)$$

It should be noted that although there is a difference between the time constant of Y_1 and Y_2 nodes, but if it is assumed that the poles of these nodes are approximately equal, the transfer function of the designed circuit is simplified to the following:

$$A_v(s) = A_{dc} \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_{y1}}\right) \left(1 + \frac{s}{\omega_x}\right) \left(1 + \frac{s}{\omega_{out}}\right)}, \quad (16)$$

where

$$\begin{cases} A_{dc} = A_1 + A_2 = (g_{m1a} + g_{m1b}) R_{out} \\ \omega_z = \frac{1}{R_x C_x} \frac{g_{m1a} + g_{m2a}}{g_{m1a}} \end{cases} \quad (17)$$

It should be noted that in the context of the proposed amplifier, g_m signifies the small-signal transconductance of the transistors, while r_{ds} denotes their small-signal drain-source resistance. Assuming a dominant pole at the output node, the unity-gain bandwidth can also be calculated using the following formula:

$$\omega_t \approx \frac{G_m}{C_L} \approx \frac{g_{m1a} + g_{m1b}}{C_L}. \quad (18)$$

In the noise analysis, the input transistors and the current mirror devices contribute the most to the noise analysis, and the effects of other devices can be neglected. The IRN

is generally composed of thermal noise and flicker noise. The power spectral density of the input-referred thermal noise can be calculated using Equation (19), and the power spectral density of the input-referred flicker noise can be calculated using Equation (20) by performing some mathematical operations. Consequently, the total power spectral density of the IRN can be obtained by combining the above-mentioned equations.

$$\overline{V_{n,in,th}^2} = \frac{4kT\gamma g_{m1a}R_{out}^2 + 4kT\gamma g_{m1b}R_{out}^2\left(\frac{k}{1+m}\right)^2 + 4kT\gamma g_{m7a}R_{out}^2\left(1 + \frac{1}{k} + \frac{m}{k}\right)^2}{A_V^2}, \quad (19)$$

$$\overline{V_{n,in,\frac{1}{f}}^2} = \frac{\left(\frac{K_n}{C_{ox}(WL)_{1a}}g_{m1a} + \frac{K_p}{C_{ox}(WL)_{1b}}g_{m1b}\left(\frac{k}{1+m}\right)^2 + \frac{K_n}{C_{ox}(WL)_{7a}}g_{m7a}\left(\frac{k+1+m}{k}\right)^2\right)\frac{R_{out}^2}{f}}{A_V^2}, \quad (20)$$

where K_n and K_p are the process-dependent flicker noise parameters for N-channel and P-channel devices, respectively; C_{ox} is the gate oxide capacitor per unit area; T is the absolute temperature; k is the Boltzmann constant; and γ is the excess noise factor. It should be noted that there are some trade-offs between noise, stability, and voltage gain in choosing m and k values. The pole associated with node X is typically smaller than the other non-dominant poles, as the transconductance of M_{7b} and M_{7c} is smaller than the transconductance of M_{3a} and M_{3b} devices (Equation (2)). Therefore, to achieve a sufficient phase margin and ensure stable behavior, the values of m and k must be carefully chosen. Increasing m , and consequently k , enhances the DC gain and IRN. However, this also reduces the equivalent second pole, which is primarily determined by R_X . This trade-off can be managed by judiciously selecting the aspect ratio of the cross-coupled transistors. In this paper, to simultaneously satisfy the amplifier's stability, voltage gain, and noise requirements, we have selected $m = 1/3$ and $k = 4/3$ as suggested in [26].

4. Post-Layout Simulation Results

The proposed fully differential RFC OTA has been implemented at the schematic level using the TSMC 0.18 μm CMOS process and then simulated with the Spectre simulator in the Cadence environment. The dimensions of the devices utilized in the proposed RFC OTA (shown in Figure 4a) are reported in Table 2. The load transistors are larger than the input transistors, although their aspect ratios are 5 to 10 times smaller. This size difference is primarily due to the need for higher output resistance in the load transistors to achieve greater voltage gain. Increasing the length of these devices achieves higher output resistance. Increasing the W/L ratio of the input transistors could further reduce input noise, but at the cost of increased chip area. While a higher W/L ratio can improve noise performance and transconductance, it is important to consider the trade-offs regarding input parasitic capacitance, power consumption, and chip area. The optimal W/L ratio depends on the specific application. This design prioritizes a balance between noise performance and chip area, offering a competitive advantage in size compared to similar designs while maintaining acceptable noise levels. It is important to note that in the analysis of the proposed amplifier, a DC simulation was conducted to evaluate the voltage levels at various nodes and the current flow through different branches. The objective was also to verify the operating region of the employed transistors. The simulation results indicate that the input transistors are biased in the subthreshold region, ensuring proper functionality. Moreover, all four input transistors carry an equal amount of current. The power supply (V_{dd}) was set to 1.8 V, and the total current drawn from the power supply was measured at 3.02 μA . Out of this total, 270 nA can be attributed to the bias circuit. Consequently, without the bias circuit, the power consumption of the circuit amounts to 4.5 μW . Table 3 reports the bias voltage values of the circuit shown in Figure 4b for a 1.8 V supply with

$\pm 10\%$ variations. To regulate the current flow within the proposed OTA, current mirror transistors (M_7 , M_{7a} , M_{7b} and M_8 , M_{8a} , M_{8b}) with ratios of k , m , and 1 are strategically positioned in the current paths. This arrangement ensures a specific ratio of current passing through the branches. In the following paragraphs, firstly, the simulation results of the proposed RFC OTA under different conditions are presented. Then, in the next subsection, the behavior of the presented OTA is further examined more accurately by employing the circuit in a conventional NRA structure.

Table 2. Aspect ratio of the devices employed in the proposed fully differential RFC OTA.

Transistor Name	Dimensions (W/L)	Transistor Name	Dimensions (W/L)
$M_{1a, 2a}$	15 $\mu\text{m}/0.5 \mu\text{m}$	$M_{7a, 8a}$	60 $\mu\text{m}/10 \mu\text{m}$
$M_{1b, 2b}$	30 $\mu\text{m}/0.5 \mu\text{m}$	$M_{7c, 8c}$	45 $\mu\text{m}/10 \mu\text{m}$
$M_{3a, 4a}$	20 $\mu\text{m}/2 \mu\text{m}$	$M_{7b, 8b}$	15 $\mu\text{m}/10 \mu\text{m}$
$M_{3b, 4b}$	20 $\mu\text{m}/2 \mu\text{m}$	$M_{9, 10}$	3 $\mu\text{m}/2 \mu\text{m}$
$M_{5a, 6a}$	20 $\mu\text{m}/2 \mu\text{m}$	M_{11}	2 $\mu\text{m}/0.5 \mu\text{m}$
$M_{5c, 6c}$	15 $\mu\text{m}/2 \mu\text{m}$	M_{12}	1 $\mu\text{m}/0.5 \mu\text{m}$
$M_{5b, 6b}$	5 $\mu\text{m}/2 \mu\text{m}$	$M_{13, 14}$	2.5 $\mu\text{m}/2 \mu\text{m}$

Table 3. Different bias voltage of circuit shown in Figure 4b under different supply voltages.

Supply Voltage (V)	1.62	1.8	1.98
V_{b1}	1.093	1.203	1.453
V_{b2}	1.016	1.273	1.391
V_{b3}	0.873	0.874	0.875
V_{b4}	0.799	0.801	0.802
V_{b5}	0.749	0.752	0.753

4.1. Post-Layout Simulation Results of the Presented RFC OTA

The design of low-noise and low-power OTAs involves several important considerations, one of which is the chip area and its feasibility. The layout view of the RFC OTA proposed in this work is shown in Figure 8, including the bias circuit. The right portion of the layout corresponds to the CMFB and bias circuits, while the left portion corresponds to the main circuit. Silicon areas occupied by the core circuit are almost 0.0055 mm², while with the inclusion of the CMFB circuit, it is almost 5570 μm^2 , which is very low compared to other existing configurations.

The frequency response of the open-loop voltage gain for the proposed amplifier, when connected to a load capacitance of 1 pF, is depicted in Figure 9. This analysis reveals that the DC gain for the proposed RFC OTA is approximately 97.23 dB, compared to about 80.8 dB for traditional OTAs. Consequently, the proposed OTA achieves a DC gain that is approximately 16.43 dB higher than that of the conventional folded-cascode OTA. It is important to note that the voltage gain of this OTA is a result of balancing various factors, including power consumption and amplifier bandwidth. The simulated phase margins for the proposed RFC OTA and the conventional OTA are 70° and 78°, respectively. The phase margin of the proposed OTA is smaller due to the presence of more non-dominant poles and zeros. Nevertheless, as will be addressed in the following subsection, the simulated neural recording amplifier operates with a feedback factor (FF) of 0.01, resulting in a closed-loop voltage gain of 40 dB. Therefore, there are no stability concerns associated with the observed open-loop phase margins. In fact, the closed-loop

phase margins with a 0.01 FF are approximately 86° for the RFC OTA and 89° for the conventional OTA. It should also be noted that the value of load capacitance depends on the next stage of the neural recording microsystem (which is usually an ADC). As the value of this capacitance is sometimes large, an extra buffer stage will be needed in some cases between the amplifier and the proceeding stages in order for the amplifier to exhibit suitable settling behavior [15], though not needed in this work, as the settling simulations confirm. For thoroughness, further simulation results, summarized in Table 4, compare the proposed and conventional OTAs under varying load capacitor conditions. It should be added that analytical calculations accurately predicted the amplifier's behavior across most parameters, except for the unity-gain bandwidth. This discrepancy stems from the large size of the current mirror transistors, which, due to their low current, contribute to increased parasitic capacitance and resistance at node X. As a result, the second pole is shifted to lower frequencies, reducing the unity-gain bandwidth compared to traditional OTAs. Nevertheless, when designing the presented OTA for typical applications without stringent flicker noise requirements, a larger unity-gain bandwidth compared to conventional OTAs can be achieved.

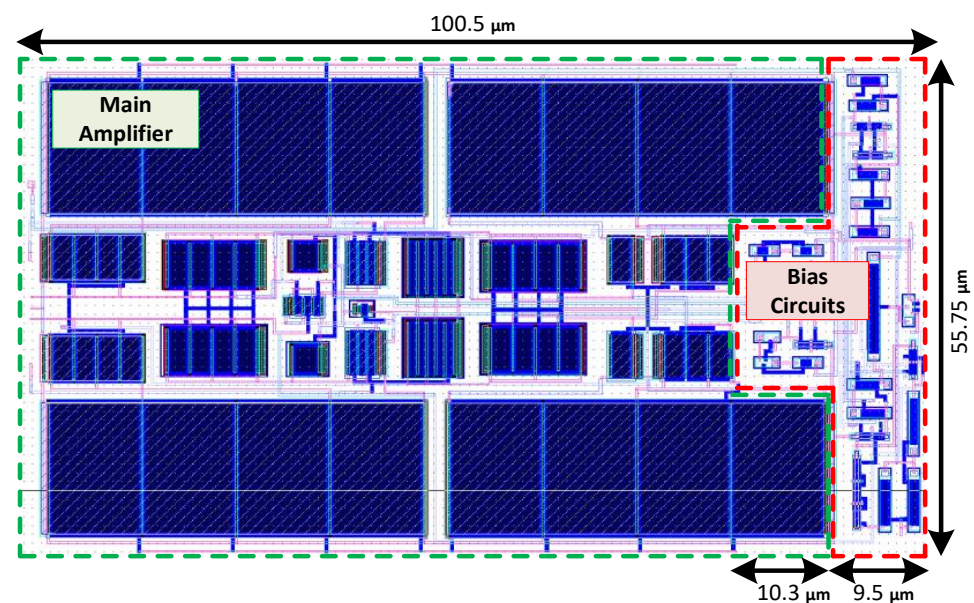


Figure 8. Layout view of the proposed low-noise and low-power fully differential RFC OTA.

Table 4. UGBW and phase margin of the proposed amplifier for different load capacitances.

Load Capacitance (pF)	Conventional FC Amplifier		Proposed RFC Amplifier	
	UGBW (MHz)	Phase Margin ($^\circ$)	UGBW (MHz)	Phase Margin ($^\circ$)
0.1	5.53	72	4.12	65
1	4.6	78	2.91	70
2	1.2	80	1.35	73
5	0.67	86	0.62	79

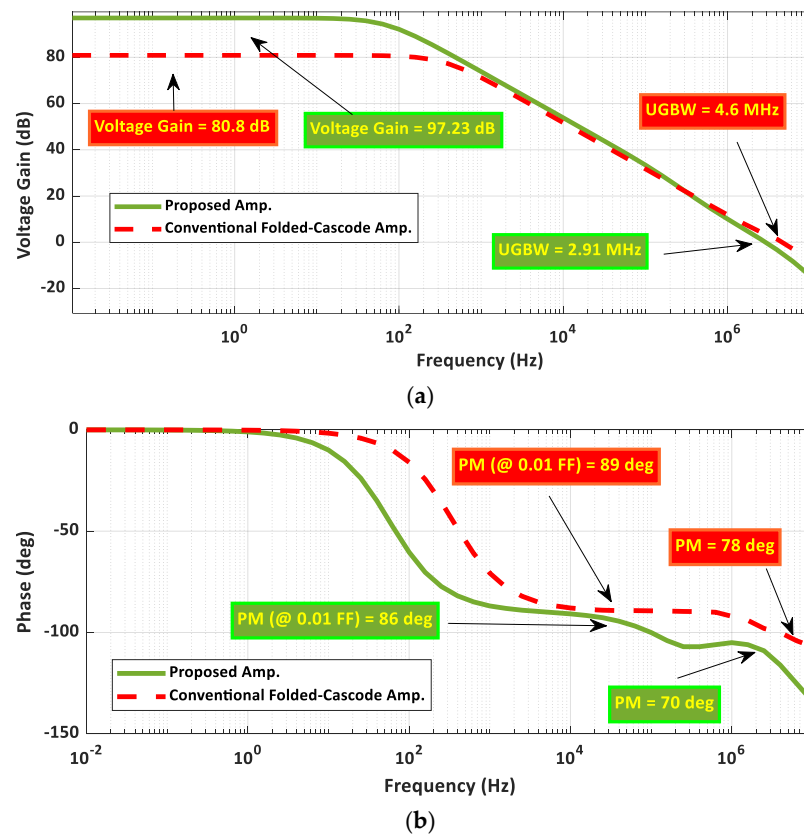


Figure 9. Open-loop frequency response of the designed RFC OTA and conventional folded-cascode amplifier in typical conditions: (a) voltage gain and (b) phase.

As mentioned before, the IRN is a critical parameter in low-noise and low-power OTAs. To achieve a low noise figure, careful attention must be given to various aspects during the design of the operational amplifier. In this study, a noise analysis simulation was conducted for the proposed low-noise and low-power RFC OTA, and the frequency graph of the IRN is illustrated in Figure 10. The simulated IRN was obtained within the frequency range of 1 to 10 kHz, measuring at $4.75 \mu\text{V}_{\text{rms}}$. This result is considered favorable, particularly considering the utilization of both N-type and P-type MOSFETs as the input transistors. It is worth noting that one of the key challenges in OTA design, with respect to noise, is striking a balance between IRN and other circuit specifications. Therefore, the simulation was repeated by modifying different components such as transistor dimensions and bias voltages, ensuring that the changes made do not significantly impact the input noise.

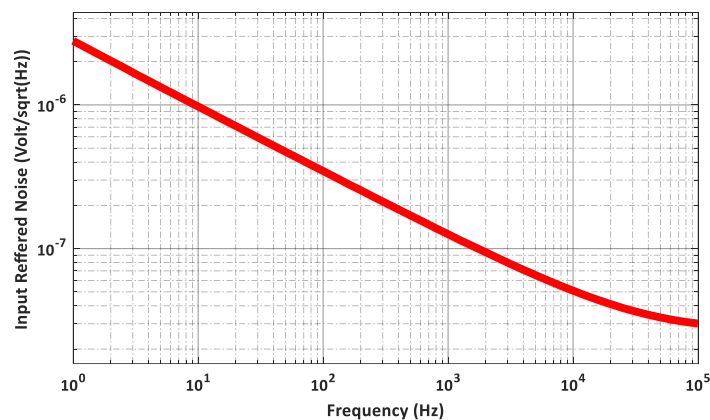


Figure 10. Simulated IRN of the designed fully differential RFC OTA (volt/sqrt(Hz)).

To demonstrate the time-domain characteristics of the designed RFC OTA, some post-layout simulations have been conducted. These simulations aim to showcase the amplifier's correct operation, including its output voltage swing, SR behavior, and delay time. To determine the maximum output voltage swing, a sinusoidal low-amplitude input signal with a 1 kHz frequency has been applied to the designed OTA, and a voltage output graph was plotted as a function of time. As depicted in Figure 11, the proposed amplifier exhibits a maximum swing of $0.976 V_{pp}$ with the total harmonic distortion (THD) of -62.68 dB in open-loop configuration. Moreover, Figure 12 shows the THD of the proposed amplifier versus input signals with different amplitudes. According to this figure, the proposed LNA has a low THD value compared to the conventional folded-cascode amplifier for the input signals with the same amplitudes.

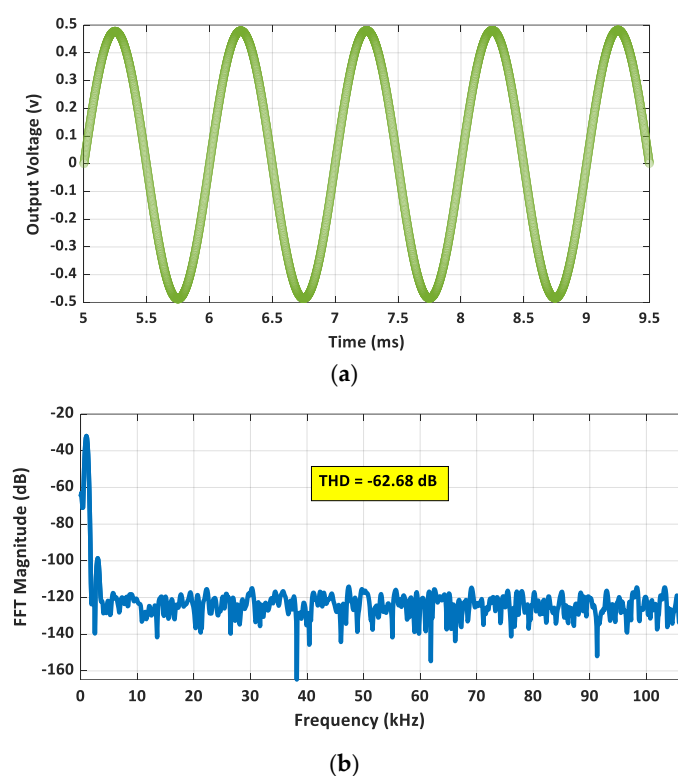


Figure 11. (a) Output voltage of the proposed OTA in time-domain to obtain the maximum swing. (b) Simulated output PSD of the proposed amplifier.

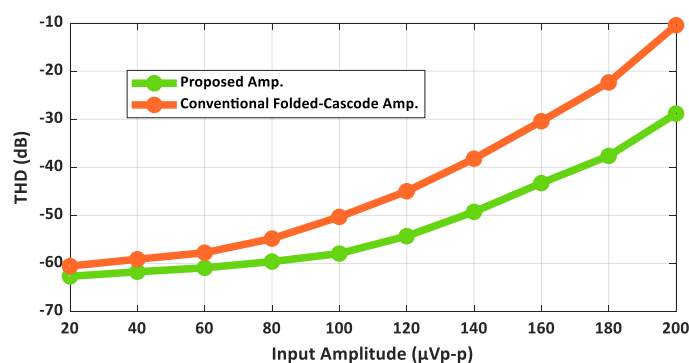


Figure 12. Total harmonic distortion of the proposed OTA in different input signal amplitudes.

Figure 13 shows the variation in voltage gain of the designed amplifier under different input CM voltages. As can be seen, the performance of the presented circuit at input CM voltages between approximately 0.8 V and 1.7 V is acceptable. However, by removing the

input NMOS transistors, not only does the voltage gain decrease, but the input range in which the circuit can operate correctly also reduces by about 40%. It should be noted that the NMOS input transistors utilized in Figure 4a suffer from the body effect, which impacts both the threshold voltage and the noise performance of the amplifier. The body effect increases the threshold voltage, reducing the transconductance of the input pair, which in turn affects the thermal noise contribution. Additionally, since flicker noise is inversely proportional to the gate area and overdrive voltage, the body effect can slightly degrade the input-referred noise at low frequencies. However, this trade-off is justified by the extended input common-mode range achieved in this design. If a twin-well CMOS process is used, the body effect can be mitigated by connecting the NMOS bulk to the source, reducing the minimum required operating voltage and further widening the input range. It should also be noted that in addition to the approach used in this work to widen the input voltage range, several other techniques can be employed. Level-shifting techniques, such as resistive dividers or capacitive coupling, can adjust the input signal to a compatible range, while adaptive biasing dynamically adjusts bias currents to maintain linearity across a wider input range [46]. Floating-gate transistors offer flexibility by dynamically adjusting threshold voltages, though they require specialized fabrication processes [47]. Each of these methods has its own advantages and challenges, and researchers can refer to the one that best suits their design requirements. These techniques provide viable pathways to enhance the input range without significantly compromising other performance parameters.

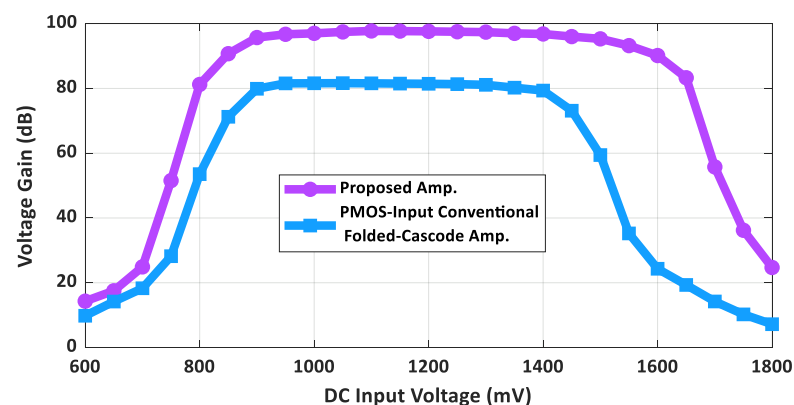


Figure 13. Voltage gain variation in the proposed OTA under different input CM voltages.

SR is another crucial parameter in designing amplifiers. To measure the SR of the proposed OTA when connected to a 1 pF load, a pulse with an amplitude of 1.8 V was applied to the input, and the resulting output voltage was analyzed over time. The output waveform is illustrated in Figure 14. The minor peaking visible in the transient response results from capacitive coupling and does not affect circuit functionality. In practical implant scenarios, this artifact would be eliminated through proper layout techniques and subsequent signal processing stages. To calculate the SR, the variations from 10% to 90% of the output waveform were selected, yielding an SR value of 80 V/ μ s in typical NMOS/typical PMOS (TT) condition at 27 °C. Moreover, the delay in response to the input signal is calculated by applying a pulse signal with the maximum amplitude of the supply voltage to the amplifier's input. A differential output and input diagram, shown in Figure 15, is then drawn. The maximum value of the differential output signal is measured to be 1.216 V. By determining the point where both signals have a voltage value of zero volts, the distance between the two signals can be calculated, providing the delay. It is recommended to perform these calculations for both the rising and falling states. In this simulation, calculations were conducted for both rising and falling modes, and a nearly equal delay was obtained with negligible difference. Therefore, only the delay for the

falling mode is reported. In the scenario where both the input and output graphs reach the zero point, the time for the input signal is measured as 1 millisecond, while the time for the output signal is measured as 1.000005 milliseconds. Consequently, the delay, which is the difference between these two times, is determined to be 5 ns.

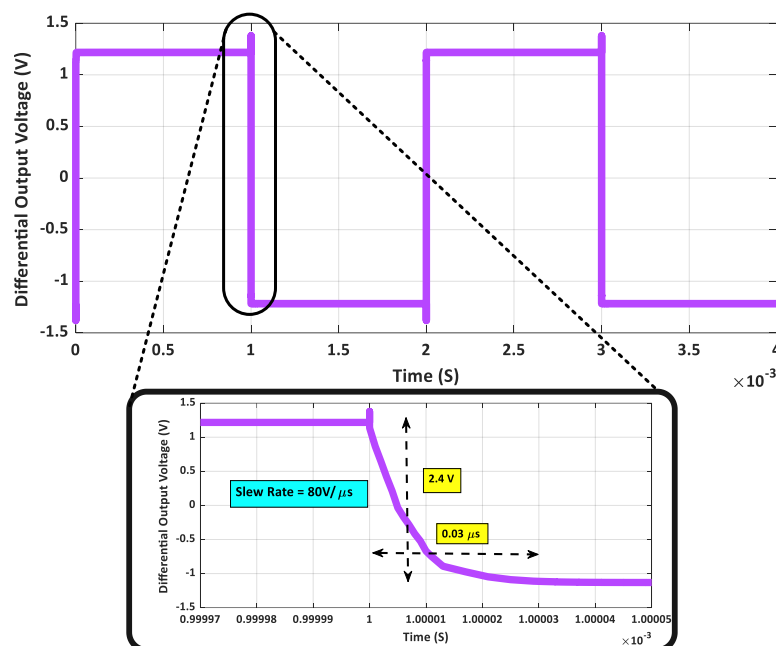


Figure 14. Differential output signal of the proposed RFC amplifier for studying its SR behavior.

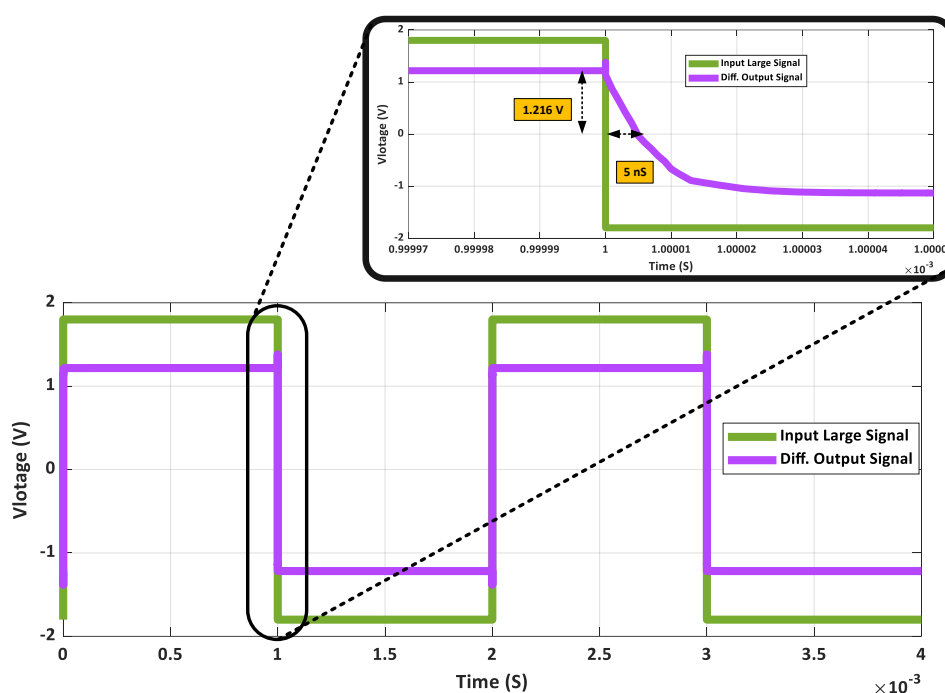


Figure 15. Output and input voltages of the designed RFC amplifier for delay calculation.

Temperature sweep analysis is a crucial analysis performed in chip manufacturing for semiconductor devices. This analysis examines how temperature variations affect the voltage gain, among other factors. Figure 16 illustrates the voltage gain variations in the OTA design in response to temperature changes. The temperature range considered for this analysis spans from -20°C to $+60^{\circ}\text{C}$. The detailed results are presented in Table 5, indicating that the maximum change in voltage gain is 3.95 dB over an 80-degree

Celsius temperature range, which is deemed acceptable. Considering that the designed circuit is intended for implementation in live tissue, such as the human body, the target temperature is set at 37 degrees Celsius. The closest simulated temperature is 40 degrees Celsius, at which the voltage gain is measured to be 96.21 dB. Therefore, it is desirable to observe minimal changes in the voltage gain of this operational amplifier when subjected to temperature variations around body temperature.

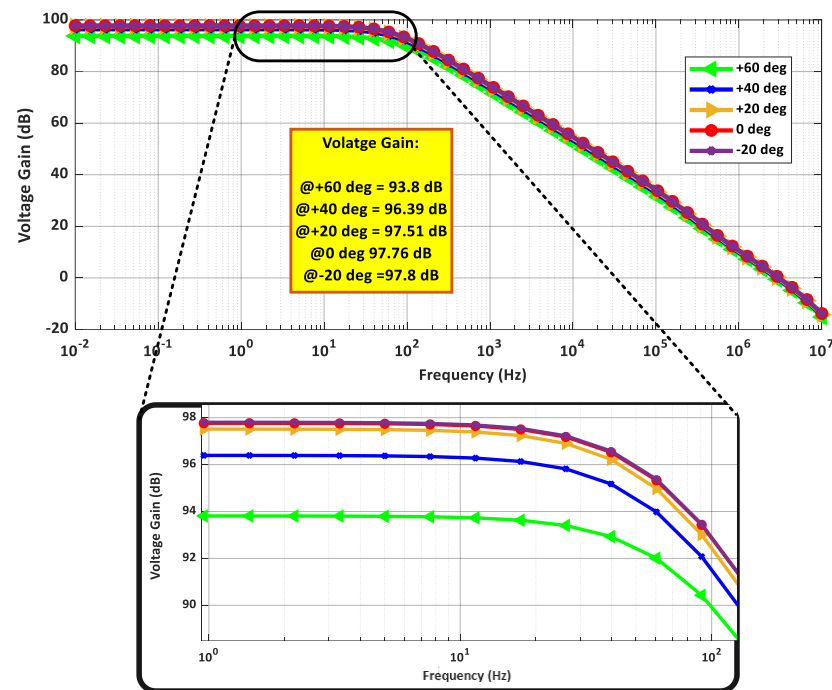


Figure 16. The curve of changes in voltage gain in relation to temperature changes.

Table 5. Voltage gain variations in the proposed RFC OTA in different operating temperatures.

Temperature (°C)	Voltage Gain (dB)
−20	97.66
0	97.36
+20	97.21
+40	96.21
+60	93.71

In integrated circuit design, corner analysis is performed to study circuit operation under extreme conditions. A circuit operating in different corners may exhibit variations in speed and voltage compared to specified values. Circuit failure in any corner indicates insufficient design margin. This section presents corner simulations of the proposed amplifier, specifically focusing on the voltage gain of the presented low-noise, low-power amplifier across TT, SS, FF, FS, and SF process corners. As shown in Figure 17, the corner analysis simulation was successful, with the amplifier performing well in all corners. Although there is an approximately 10 dB difference in voltage gain between the FF and TT corners, this voltage gain remains higher than that of a conventional folded-cascode amplifier. It is important to note that the bias circuit was included in these corner simulations, and its behavior is subject to process variations. While faster transistors in the FF corner might suggest higher voltage gain, the complex interplay of factors such as bias voltage shifts and changes in output resistance can influence the final voltage gain value.

Specifically, the increased output current in the FF corner can lower the output resistance, thus affecting the voltage gain. This phenomenon, where the FF corner does not necessarily exhibit the highest voltage gain, has been reported in other works [26,45,48–50].

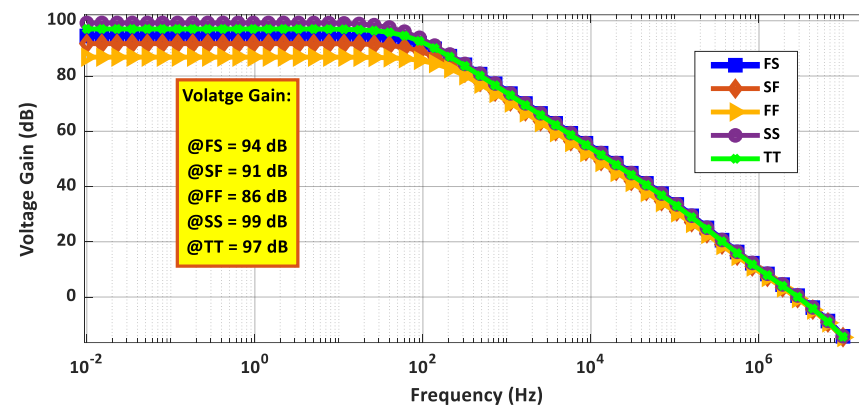


Figure 17. Frequency response of the presented OTA in different process corners.

To accurately assess the impact of fabrication process variations on the designed RFC OTA, a Monte Carlo analysis was conducted. This analysis assumes that variations in key transistor parameters, including channel length and width, channel doping concentration, mobility, oxide thickness, and threshold voltage, follow independent normal Gaussian distributions with their respective standard deviations. Figure 18 illustrates the post-layout simulated voltage gain of the proposed amplifier over 1000 Monte Carlo iterations. The results demonstrate that the influence of these non-idealities on the amplifier's performance is minimal. Specifically, the voltage gain of the designed circuit exhibits a mean value of 69,400 (96.8 dB) with a standard deviation of approximately 1500, indicating a robust and consistent gain performance across the simulated process variations.

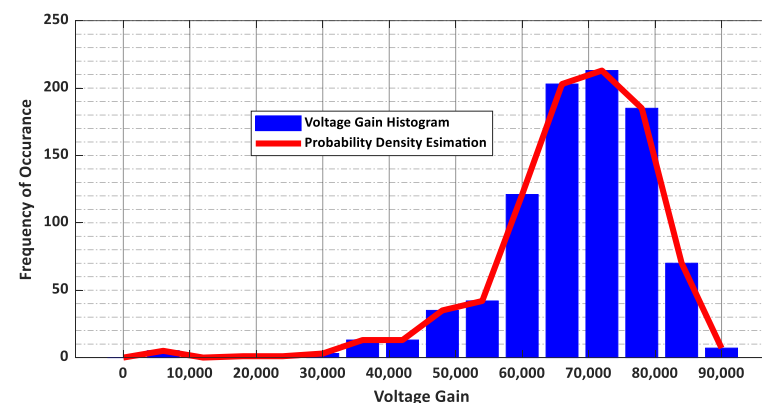


Figure 18. Monte Carlo simulation for the voltage gain of OTA.

Table 6 presents a comprehensive overview of the simulation results obtained for the proposed RFC OTA. These results provide a detailed understanding of its performance characteristics across a range of operating conditions. While the FF corner is often associated with faster transistor speeds and, consequently, higher voltage gain and unity-gain bandwidth (UGBW), the obtained results demonstrate that this is not always the case. The combined effects of low temperature ($-20\text{ }^{\circ}\text{C}$), the specific supply voltage (1.98 V), and variations in bias voltages can significantly impact transistor parameters such as carrier mobility and transconductance. These variations, coupled with the circuit's complexity, can lead to deviations from expected behavior. Similar observations have been reported in the literature [26,45], emphasizing the importance of considering these factors in corner

analysis. Careful analysis of the data indicates that the proposed amplifier is suitable for integration into a neural recording system. To further validate its performance, a comparative analysis was conducted between the proposed RFC OTA and several recently published, similar works. The results of this comparison are meticulously tabulated in Table 7. To facilitate a clearer comparison of the proposed OTA's performance with other works, figures of merit (FoMs) have been used, which are defined as follows [48]:

$$FoM1 = \frac{(UGBW \text{ (MHz)})(Load \text{ Capacitance (pF)})}{Power \text{ Consumption (mW)}}, \quad (21)$$

$$FoM2 = \frac{(Slew \text{ Rate (V/}\mu\text{s)})(Load \text{ Capacitance (pF)})}{Power \text{ Consumption (mW)}}, \quad (22)$$

$$FoM3 = \sqrt{FoM1 \times FoM2}. \quad (23)$$

Table 6. Simulation results summary of the proposed OTA across process and voltage variations.

	Conventional FC Amplifier	Proposed RFC Amplifier			Performance Improvement
Parameter	Temperature (°C)				
	27	60	27	−20	27
Supply Voltage (V)	1.8	1.62	1.8	1.98	N/A
Process Corners	TT	SS	TT	FF	TT
Power Consumption (μW)	4.75	5.77	5.43	5.72	−14%
Voltage Gain (dB)	80.8	97.3	97.23	93.28	+20%
UGBW (MHz) (C _L = 1 pF)	4.6	3.218	2.91	2.72	−36%
Phase Margin (°) (C _L = 1 pF)	78	67	70	71	−10%
IRN (nV / √Hz) (@50 kHz)	48.87	47.4	32.8	42.3	+32%
IRN (μV _{rms})	7.12	6.87	4.75	6.268	+33%
SR (V / μs) (C _L = 1 pF)	1.6	53	80	90	50 times
Delay Time (ns) (C _L = 1 pF)	50	8	5	15	10 times
THD (dB)	−60	−63.36	−62.68	−70.42	+4.5%

An important point regarding the comparison of the presented circuit and other similar works is that the FoMs available in the literature do not consider the voltage gain, linearity of the circuit, chip area, and other similar parameters. Therefore, relying solely on FoM1 and FoM2 is not entirely appropriate. Additionally, many circuits reported in the literature do not specify the SR, making it impossible to use FoM2 and ultimately FoM3, which provides a more comprehensive comparison between different circuits. In light of this, based on the reported values for voltage gain, linearity, and chip area of the designed circuit, it can be claimed that this work presents an OTA with suitable performance that could be a good candidate for use in circuits designed for amplifying neural signals. In the subsequent subsection, the simulation results obtained when the proposed RFC OTA is employed in a conventional neural recording system will be reported. This analysis will provide valuable insights into the amplifier's real-world performance and its potential applications in the field of neural recording.

Table 7. Performance comparison of the designed RFC OTA with some similar works.

Parameter	[14]	[15]	[26]	[31]	[43]	[49]	[50]	[51]	This Work
Technology (μm)	0.055	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.18
Supply Voltage (V)	1.2	1.8	1.8	0.8	0.6	1	0.5	0.4	1.8
Output Swing (v_{pp})	N/A	0.95	N/A	0.52	0.51	N/A	0.5	N/A	0.976
Amp. Gain (dB)	82.6	59.1	103.2	59.4	75.4	70	78	54.9	97.23
UGBW (MHz)	N/A	3.75	0.5	10.2	0.074	0.3	0.075	0.013	2.91
SR (V/μs)	N/A	N/A	N/A	4.8	0.00573	N/A	0.0086	N/A	80
Power Cons. (μW)	0.83	21.9	1.67	32	0.18	0.38	0.045	0.03	5.43
IRN (μV_{rms}) @ Bandwidth	2.1	N/A	3.77	N/A	$\frac{410}{nV_{rms}/\sqrt{Hz}}$	$15^a - 0.7^b$	$\frac{650}{nV_{rms}/\sqrt{Hz}}$	$\frac{700}{nV_{rms}/\sqrt{Hz}}$	4.75
	0.5–100 Hz		0.1 Hz–20 kHz		40 kHz	0.1–100 Hz	1 kHz	10 kHz	1 Hz–10 kHz
THD (dB)	−69	−50	−43.5	N/A	N/A	N/A	−40	N/A	−62.68
C_L (pF)	1	0.3	2.5	8	20	10	15	15	1
Silicon Area (μm ²)	N/A	11,600	N/A	N/R	14,000	N/A	19,311	3224	5570
FoM1 (MHz × pF/mW)	N/A	51	740	2550	4950	789	2500	7050	535
FoM2 ($V \times pF/\mu s \times mW$)	N/A	N/A	N/A	1200	636	N/A	2860	N/A	14,730
FoM3 ($\frac{pF}{mW} \times \sqrt{\frac{V \times MHz}{\mu s}}$)	N/A	N/A	N/A	1750	1774	N/A	2670	N/A	2810
Sim./Meas.	Sim.	Post-Layout Sim.	Sim.	Post-Layout Sim.	Post-Layout Sim.	Post-Layout Sim.	Meas.	Post-Layout Sim.	Post-Layout Sim.

^a Without Chopper; ^b with Chopper.

4.2. Post-Layout Simulation Results of the Designed Fully Differential RFC OTA Utilized in a Conventional NRA Structure

In this subsection, the distinct behaviors of the presented RFC OTA are further explored by integrating the circuit into a conventional NRA structure. The general architecture of the NRA that utilizes capacitive feedback, proposed in [8], is depicted in Figure 19. In this circuit, M_{P1} to M_{P4} devices are employed to create a pseudo resistor referred to as R_f , with a value in the range of several hundreds of GΩ. The relationship between the output and input voltages in Figure 19 is given by the following [8,9]:

$$\frac{V_{out}}{V_{in}}(s) = \frac{C_1}{C_2} \times \frac{1 - s\left(\frac{C_2}{G_m}\right)}{\left(1 + \frac{1}{sR_fC_2}\right)\left(1 + s\frac{C_LC_1}{G_mC_2}\right)} = A_m \frac{1 - \frac{s}{\omega_z}}{\left(1 + \frac{\omega_{pL}}{s}\right)\left(1 + \frac{s}{\omega_{pH}}\right)} \quad (24)$$

where the low cutoff frequency (f_L) is determined by R_f and C_2 , while the mid-band gain depends on the ratio of C_1/C_2 . The high cutoff frequency (f_H) is calculated as the ratio of the OTA unity gain frequency to the mid-band gain. Additionally, there is a right-half-plane zero (f_z). However, with the appropriate selection of capacitors and OTA transconductance values, this zero can be made large enough to have minimal impact on amplifier performance. To achieve this, capacitors should be chosen as follows [8,9]:

$$C_2 \ll \sqrt{C_L C_1}. \quad (25)$$

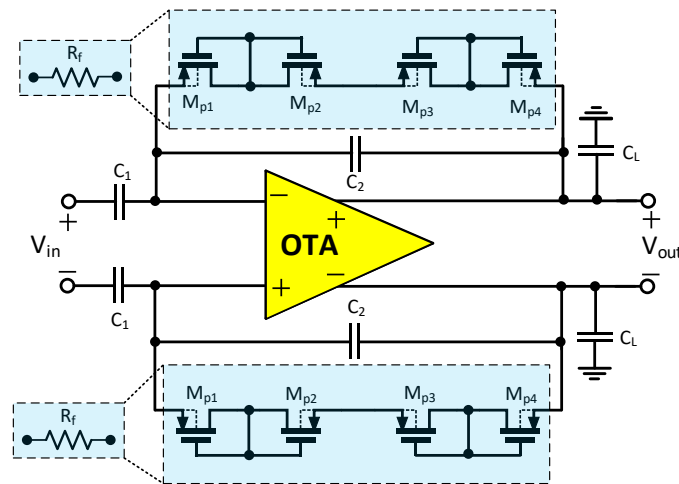


Figure 19. Capacitive feedback NRA [8].

In the NRA illustrated in Figure 19, the primary sources of noise are the IRN of the OTA and the thermal noise from the pseudo-resistors. Consequently, the IRN of the neural amplifier depicted in Figure 19 can be expressed as follows [8,9]:

$$\overline{V_{ni,amp}^2} = \left(\frac{C_1 + C_2 + C_{in}}{C_1} \right)^2 \left(\overline{V_{ni,OTA}^2} + \overline{V_{nR2}^2} \right). \quad (26)$$

Accordingly, the ratio of capacitors C_1 and C_2 has a great effect on the IRN of the amplifier. Therefore, the input capacitors must be relatively large, which also increases the closed-loop voltage gain. Of course, the compromise of the input impedance and the surface area of the chip should also be considered [8].

The NRA shown in Figure 19 is designed and simulated with specific capacitor values ($C_L = 1$ pF, $C_1 = 50$ pF, and $C_2 = 0.5$ pF) to achieve a 40 dB closed-loop gain within the desired signal bandwidth. These capacitors are realized using metal-insulator-metal technology. The designed RFC OTA in this work, which is discussed in the preceding section, serves as the core component of the designed NRA. The frequency response of the simulated NRA is illustrated in Figure 20, revealing a mid-band gain of approximately 39.8 dB across the frequency range of 1.1 Hz to 16 kHz, effectively covering both neural LFP and AP signal frequencies.

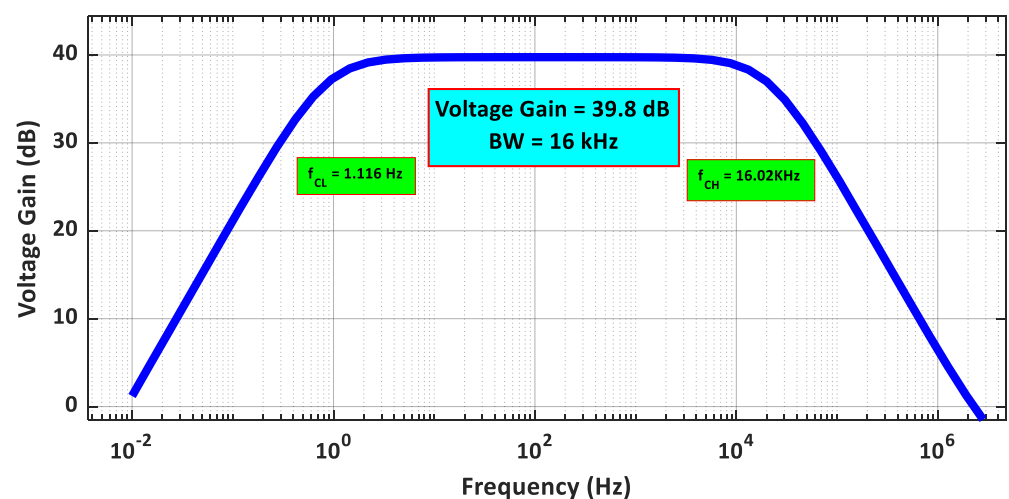


Figure 20. Closed-loop frequency response of the designed NRA at typical condition.

Figure 21 illustrates the simulated input-referred voltage noise spectrum of the designed NRA. The thermal noise level is measured around $30 \text{ nV}/\sqrt{\text{Hz}}$. Integrating the area under the curve shown in Figure 21 from 1 Hz to 10 kHz results in a noise voltage of $5.73 \text{ } \mu\text{V}_{\text{rms}}$, which is lower than the typical extracellular neural background noise of around $10 \text{ } \mu\text{V}_{\text{rms}}$ in this bandwidth [15]. The NEF serves as a criterion for evaluating the noise-to-power trade-off, defined as follows [8]:

$$NEF = V_{ni,rms} \sqrt{\frac{2I_{tot}}{\pi \times V_T \times 4kT \times BW}}, \quad (27)$$

where $V_{ni,rms}$ is the IRN, I_{tot} is the total current including the bias circuit, BW is the LNA bandwidth in Hertz, T is the absolute temperature, V_T is the thermal voltage, and k is the Boltzmann's constant. Another key metric for evaluating noise efficiency is the power efficiency factor (PEF), defined in [52]. PEF considers both power consumption and supply voltage, providing a more comprehensive assessment,

$$PEF = NEF^2 \times V_{dd}, \quad (28)$$

where V_{dd} is the supply voltage. The PEF provides valuable insights into the trade-off between noise performance and power consumption in LNA design. The noise efficiency factor of the designed circuit is calculated to be 3.45 based on the amplifier's current consumption, and the achieved PEF is about 21.4. Circuit simulations indicate that the primary source of circuit noise is thermal noise, contributing 80% of the input-referred noise, and if $1/f$ noise were completely eliminated, the circuit would have an IRN of $4.5 \text{ } \mu\text{V}_{\text{rms}}$.

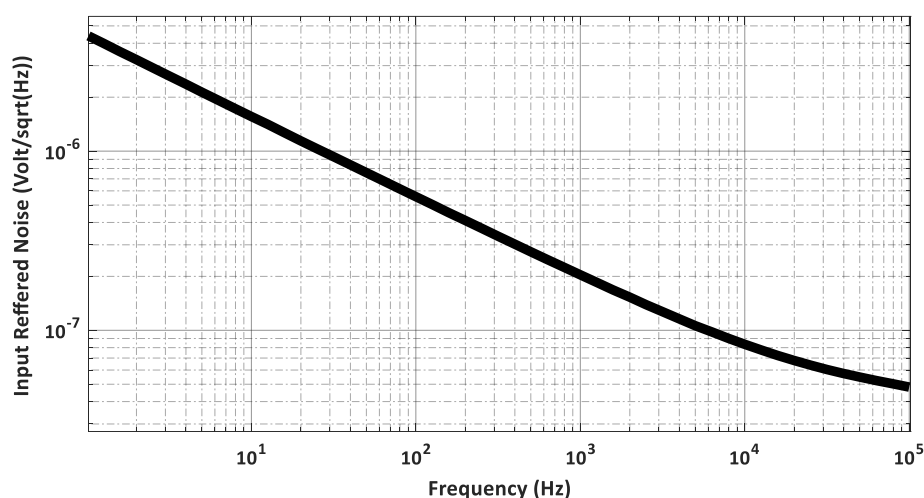


Figure 21. Simulated IRN of the designed NRA in the frequency range of 1 to 10 kHz.

Figure 22 presents the results of a Monte Carlo simulation for CMRR and PSRR at a frequency of 50 Hz, based on 1000 runs that account for both device mismatches and process variations using the Monte Carlo models of device components within the 180 nm CMOS process. The mean values achieved for CMRR and PSRR of the designed NRA at this frequency are 96.6 dB and 99.75 dB, respectively. Figure 23 illustrates the mean values of CMRR and PSRR from the Monte Carlo simulation results, plotted against the input signal frequency.

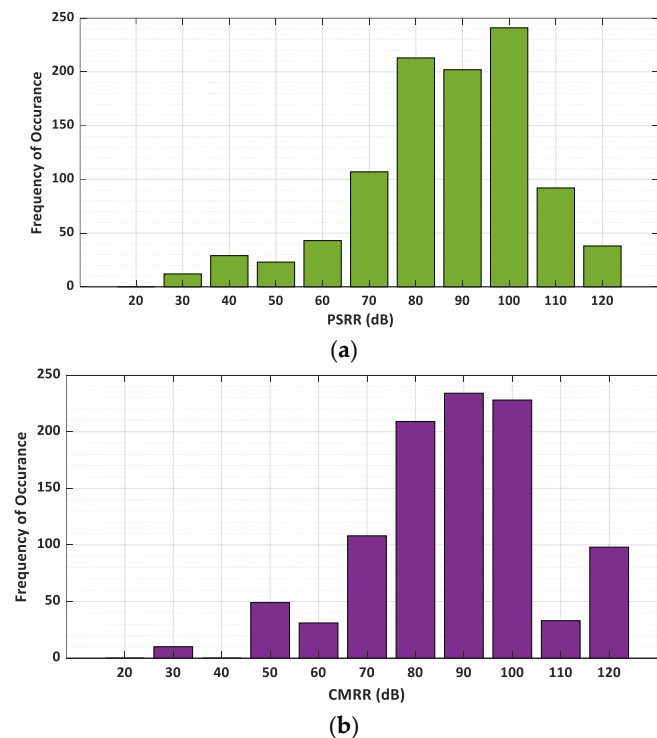


Figure 22. Post-layout simulation results of sensitivity analysis of (a) CMRR and (b) PSRR through 1000 Monte Carlo runs.

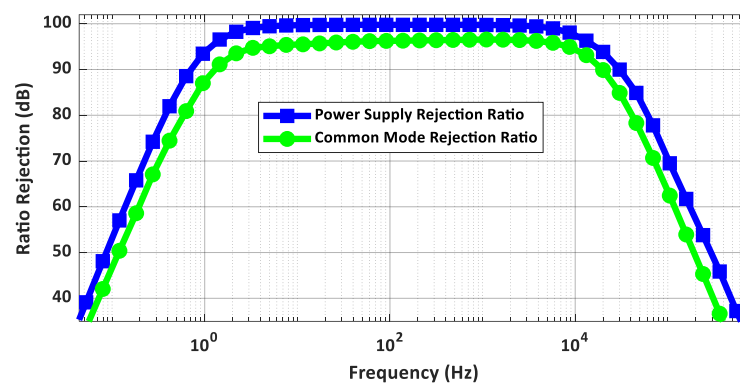


Figure 23. Mean value of CMRR and PSRR in Monte Carlo simulations of the designed NRA with 1000 runs versus the frequency.

Figure 24 illustrates the time-domain response of the NRA, which employs the proposed RFC OTA. This figure is a critical representation of how the NRA processes neural signals, particularly in the context of its application in biomedical electronics. In this simulation, the input neural signal consists of a small slice extracted from a prerecorded dataset of neural activity recorded from the auditory cortex of a guinea pig. This choice of input signal is particularly important, as it mimics real neural activity and provides a robust basis for evaluating the NRA's performance in a biologically relevant scenario. The recorded neural signal is characterized by its low amplitude, which is typical for neural recordings. Consequently, the NRA is designed to amplify the signal to facilitate further processing without introducing excessive noise or distortion. In this particular simulation, the NRA achieves a substantial gain of 40 dB. This high gain level is essential for making the weak neural signals detectable and usable for subsequent stages of signal processing, such as filtering, digitization, or feature extraction. The time-domain response depicted in Figure 24 demonstrates the amplifier's ability to amplify the input signal waveform.

By examining this response, one can assess key performance parameters such as linearity, bandwidth, and transient response, which are crucial for ensuring that the nuances of the neural signal are preserved during amplification.

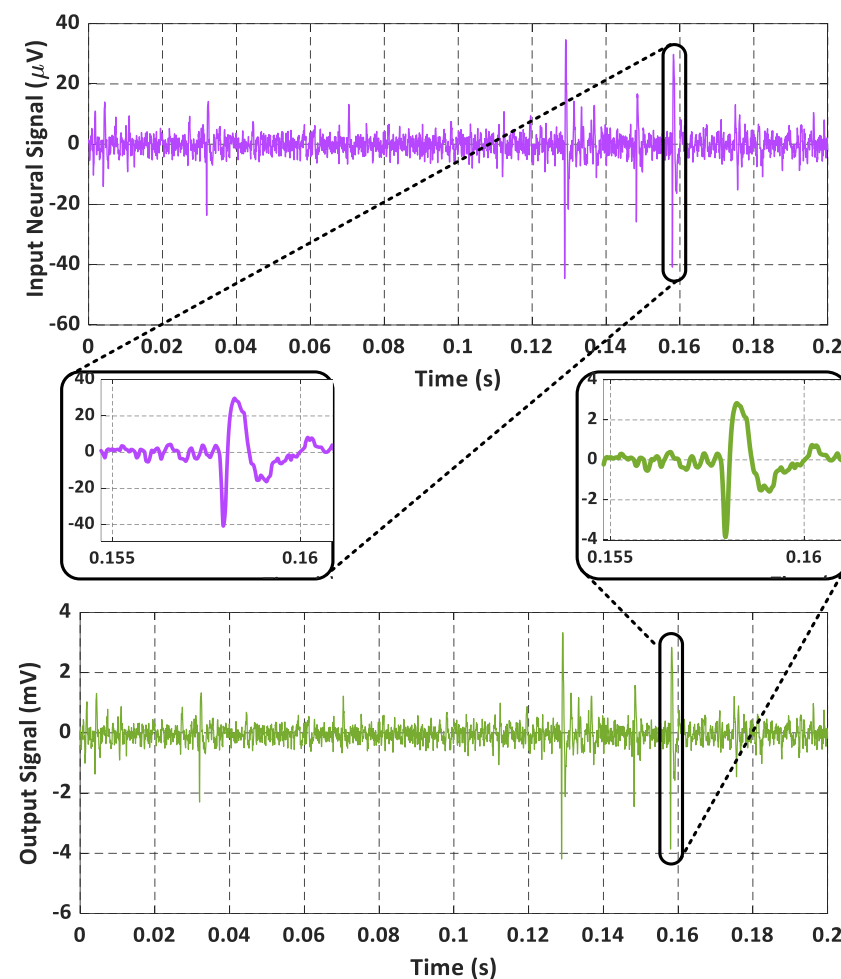


Figure 24. Simulated time-domain transient response plot of the designed NRA circuit showing input (top) and output (bottom) signals.

Table 8 presents a comprehensive summary of the simulation results obtained for the designed NRA. It is crucial to emphasize that the proposed RFC OTA, extensively discussed in Section 3, serves as the fundamental building block of the designed NRA. To evaluate its performance, a comparative analysis with several recently published neural recording amplifiers has been conducted, the results of which are also tabulated in Table 8. It is important to note that some of the specifications listed in this table are based on experimental results. It is acknowledged that there may be some deviation between post-layout simulation and experimental outcomes, as indicated in Table 8. A thorough examination of the table reveals that the proposed NRA exhibits a level of performance that is competitive with the best reported similar works in the contemporary literature. The designed NRA exhibits an NEF of 3.45 and a PEF of 21.4, which are comparable to or better than those reported in other similar designs. These NEF and PEF values suggest competitive noise performance. Moreover, the ratio between the bandwidth and power consumption of the designed NRA unequivocally positions it among the most power-efficient solutions in this domain. Furthermore, essential specifications such as CMRR and PSRR are well within the acceptable range for an implantable NRA, reinforcing the suitability of the designed NRA for such demanding environments.

Table 8. Comparative performance of the designed NRA with some similar works.

Parameter	[8]	[15]	[21]	[26]	[53]	[54]	[55]	[56]	[57]	[58]	[59]	This Work
Technology (μm)	1.5	0.18	0.18	0.18	0.18	0.18	0.13	0.18	0.18	0.04	0.13	0.18
Supply Voltage (V)	± 2.5	1.8	1.4	1.8	1.8	1.2	2	1	1.8	1.2	0.8	1.8
Amp. Gain (dB)	39.8	79.8–87	39.22	39.92	40.4	39.2	43–55	45–55	40–46	37	35.5	39.74
BW (HZ)	0.025–7.2k	11/90–6.2k/10k	3–5k	0.41–10.3k	0.2–8k	0.25–28k	40–320	0.8/300–4.1/8.2k	0.54–6.1k	0.2/550–260/3.8k	1–7.5k	0.7–12.69k
Power Cons. (μW)	80	36.7	2.98	1.7	13.9	2.4	6.3	3.6	6.84	2.47	1.6	5.6
IRN (μV_{rms})	2.2	4	3.03	3.34	2.1	5.79	2.4–3.45	2.1	3.1	1.7	4.19	5.73
CMRR (dB)	≥ 83	N/A	> 70	68.6	> 72	N/A	112	98.28	66	107	67	96.63
PSRR (dB)	≥ 85	N/A	> 77	73.3	N/A	N/A	101	92.48	84	> 70	N/A	99.75
NEF	4	6.8	2.4	1.23	2.51	3.16	13.2	1.7	2.97	4.1	11.58	3.45
PEF	80	83.2	8.1	2.73	11.4	12	52.8	2.89	10.17	20.17	107	21.4
Structure	One-stage	Two-stage	One-stage	One-stage	Two-stage	One-stage	Three-stage	Three-stage	Two-stage	Two-stage	One-stage	One-stage
Sim./Meas.	Meas.	Post-layout Sim.	Post-layout Sim.	Post-layout Sim.	Post-layout Sim.	Meas.	Meas.	Post-layout Sim.	Meas.	Meas.	Meas.	Post-layout Sim.

5. Discussion

This work presents a neural signal amplifier designed with a focus on low power consumption and compact area, which inherently imposes constraints on both the achievable IRN and technology selection. Regarding the choice of 0.18 μm CMOS technology, while newer technologies like CNTFETs offer potential advantages [60], the mature 0.18 μm process remains the preferred choice for implantable biomedical applications due to its proven reliability, cost-effectiveness, and well-characterized design rules. This technology continues to be widely adopted in state-of-the-art bioelectronics research, offering an optimal balance between performance and practical implementation requirements. The current IRN performance is acceptable given the design constraints, but several optimization techniques could be explored. Increasing the W/L ratio of input transistors could reduce IRN, though this would increase chip area and power consumption—particularly important considerations given the choice of 0.18 μm technology, where area optimization is crucial. Bias point optimization presents another avenue for noise reduction without significant power penalty [46]. Advanced noise reduction techniques could be implemented within the 0.18 μm framework: Chopper stabilization [59] effectively mitigates flicker noise through modulation techniques, though it requires careful design to avoid introducing new noise sources. Bandpass filtering [8] can suppress out-of-band noise while maintaining signal integrity in the neural frequency range. Correlated double sampling [61] and auto-zeroing [62] techniques offer noise cancelation but increase design complexity. Input impedance optimization [9] can also help minimize signal loss and noise pickup. Notably, the technology choice impacts the implementation of these techniques—the 0.18 μm process provides sufficient performance headroom for such enhancements while maintaining the reliability required for biomedical applications. Future work could explore these optimizations while maintaining the practical advantages of mature CMOS technology, potentially achieving better noise–power–area tradeoffs than what might be possible with emerging technologies in real-world implantable scenarios.

6. Conclusions

A novel CMOS OTA presented in this paper offers a promising solution for the preconditioning stage of implantable neural recording microsystems. Through the utilization of an RFC topology with positive feedback and cross-coupled transistors, the amplifier achieves a remarkable balance between low-noise performance and low power consumption, which are critical requirements for such applications. The single-stage configuration implemented in a standard 0.18- μm CMOS process with a 1.8 V supply voltage demonstrates impressive performance metrics, including a high open-loop voltage gain of 97.23 dB, a unity-gain bandwidth of 2.91 MHz, and an input-referred noise of 4.75 V_{rms} , all while consuming 5.43 μW of power and occupying a compact chip area of 0.0055 mm^2 . Furthermore, the integration of the proposed amplifier into a conventional neural recording amplifier configuration showcases its effectiveness in amplifying action potential and local field potential signals with a power consumption of 5.6 μW and a simulated input-referred noise of 5.73 μV_{rms} over a bandwidth of 1 Hz to 10 kHz. The amplifier's output voltage swing of 0.976 V_{pp} and total harmonic distortion of -62.68 dB at 1 kHz further validate its suitability for high-quality signal processing in neural recording applications. Overall, the performance characteristics and efficiency of the designed CMOS OTA position it as a valuable contribution to the field of analog IC design, particularly in the development of low-power, high-performance amplifiers for implantable neural recording systems.

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Abbreviations

The following abbreviations are used in this manuscript:

MEA	Microelectrode Array	SR	Slew Rate
AP	Action Potential	FVF	Flipped Voltage Follower
LPF	Local Filed Potential	CMFB	Common-Mode Feedback
IRN	Input-Referred Noise	CM	Common-Mode
CMRR	Common-Mode Rejection Ratio	THD	Total Harmonic Distortion
PSRR	Power Supply Rejection Ratio	TT	Typical NMOS/Typical PMOS
OTA	Operational Transconductance Amplifier	SS	Slow NMOS/Slow PMOS
NEF	Noise Efficiency Factor	SF	Slow NMOS/Fast PMOS
RFC	Recycling Folded-Cascode	FS	Fast NMOS/Slow PMOS
NRA	Neural Recording Amplifier	FF	Fast NMOS/Fast PMOS
		PEF	Power Efficiency Factor

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