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PIXEL AND READOUT CIRCUIT OF A WIDE DYNAMIC RANGE LINEAR-LOGARITHMIC CURRENT-MODE IMAGE SENSOR

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DEDICATION

To my parents

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RESUME

Le capteur d'images est la partie principale de tout système d'acquisition d'images, quelle que soit son application. Jusqu'à la fin des années 1990, les capteurs de type CCD ont dominé le marché en raison de leur qualité d'image exceptionnelle. À l'opposé des capteurs CCD, les capteurs CMOS offrent des possibilités intéressantes d'intégrer les circuits de traitement de signal sur un même substrat en vue d'obtenir une caméra sur puce. Entant que ces capteurs opèrent avec des tensions d'alimentations plus faibles que celles requise par les capteurs CCD, elles possèdent une faible consommation de puissance. De plus, les coûts associés à la fabrication des capteurs CMOS sont plus faibles que ceux engendrés par les capteurs CCD. Ces caractéristiques font en sorte que les capteurs d'images CMOS se prêtent à un plus grand nombre d'application que leurs équivalents CCD.

Dans ce projet, l'objectif principal est de concevoir un capteur d'images ayant une plage dynamique élevée. Il possède l'avantage de deux modes d'opération, linéaire et logarithmique, ainsi qu'une lecture en mode courant afin d'augmenter sa plage dynamique. Les tensions d'alimentation des technologies CMOS diminue de plus en plus, et de ce fait la plage dynamique du pixel. En fonctionnant en mode courant, on arrive à atténuer cet effet. Le projet consiste à concevoir des circuits : convoyeur de courant, 'delta-reset-sampling' et un comparateur de courant qui sont efficaces pour les modes d'opération linéaire et logarithmique du pixel et permettent de détecter dans quels des deux modes se situe le pixel de façon à réaliser, à l'étage subséquent, une conversion analogique-numérique adéquate. Le pixel à trois transistors fonctionnant en mode courant utilise un transistor PMOS dans la région linéaire pour la lecture et un transistor PMOS de reset qui permet une réponse linéaire-logarithmique combinée. L'une des contributions à la non-linéarité de la réponse provient de l'effet provoqué par la résistance 'on' du transistor 'select'. Pour éliminer cet effet, nous appliquons une fonction de linéarisation qui est effectuée dans le domaine numérique. Le mode d'opération du pixel est déterminé dans le circuit de lecture de colonne et un signal est envoyé à l'unité de traitement numérique comme indicateur de mode.

Un prototype a été conçu et fabriqué en CMOS 0.35µm standard, 3.3V. Les résultats expérimentaux sont concluants et montrent une plage dynamique intrascènede 100 dB.

ABSTRACT

Digital cameras are rapidly becoming a dominant image capture devices. They are enabling many new applications. Charge-coupled devices (CCDs) have been the basis for solid state imaging since the 1970s. However, during the last decade, interest in CMOS imagers has increased significantly since they are capable of offering System-on-Chip (SoC) functionality. This can greatly reduce camera cost, power consumption, and size. Furthermore, by integrating innovative circuits on the same chip, the performance of CMOS image sensors could be extended beyond the capabilities of CCDs. Dynamic range is an important performance criterion for all image sensors.

This thesis presents a current-mode CMOS image sensor operating in linear-logarithmic response. The objective of this design is to improve the dynamic range of the image sensor, and to provide a method for mode detection of the image sensor response. One of the motivations of using current-mode has been the shrinking feature size of CMOS devices. This leads to the reduction of supply voltage which causes the degradation of circuit performance in term of dynamic range. Such problem can be alleviated by operating in current-mode. The column readout circuits are designed in current-mode in order to be compatible with the image sensor. The readout circuit is composed of a first-generation current conveyor, an improved current memory is employed as a delta reset sampling unit, a differential amplifier as an integrator and a dynamic comparator. The current-mode three-transistor active pixel sensor uses a PMOS readout transistor in the linear region of operation and a PMOS reset transistor that allows for a linear-logarithmic response. One of the non-linearity contributions is the effect caused by the ‘on’ resistance of the select transistor. To eliminate this effect, we apply a linearization function that can be performed in the digital domain. The pixel response operation is determined in the column readout circuit and a signal is sent to the digital processing unit as an indicator.

These circuits were implemented using a standard CMOS technology with no process modification. A prototype has been designed and fabricated in a standard AMS 2P4M, 3.3V, CMOS 0.35μm process from Austrian Microsystem. The experimental results

demonstrate the functionality of the circuits and a intrascene dynamic range of more than 100 dB.

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ABREVIATIONS

ADC	Analog to Digital Converter
AMS	Austrian Micro System
APS	Active Pixel Sensor
CCD	Charge Coupled Device
CCI	First generation Current Conveyor
CDS	Correlated Double Sampling
CM	Common Mode
CMC	Canadian Microelectronics Corporation
CMFB	Common Mode Feed Back
CMOS	Complementary Metal Oxide Semiconductor
CMP	Comparator
DC	Direct Current
DPS	Digital Pixel Sensor
DPU	Digital Processing Unit
DR	Dynamic Range
DRS	Delta Reset Sampling
FF	Fill Factor
FPN	Fixed Pattern Noise
IC	Integrated Circuit
LPW	Lumens per Watt

MI	Mode Indicator
MOS	Metal Oxide Semiconductor
NMOS	N-type Metal Oxide Semiconductor
PMOS	P-type Metal Oxide Semiconductor
PPS	Passive Pixel Sensor
SNR	Signal to Noise Ratio
SoC	System-on-Chip

INTRODUCTION

Image sensors have become a significant silicon technology driver due to the high demand from different applications. Charge-Coupled Device (CCD) and Complementary Metal-Oxide Semiconductor (CMOS) image sensors are two different technologies for capturing images digitally. Both types of imagers are implemented in silicon and convert light into electric charge and process it into electronic signals.

The CCD reported in the early 70's has been for a long time the technology of choice in high quality image sensing. However, it has some functional limitations. The CCD fabrication process does not allow cost-efficient integration of on-chip ancillary circuits such as signal processors, and Analog-to-Digital Converters (ADCs). As a result, a CCD-based camera system requires not one image sensor chip, but a set of chips, which increases power consumption and hampers miniaturization of cameras [1-2].

In recent years, CMOS image sensors have attracted the attention in the field of electronic imaging. The major reason for the growing interest in CMOS image sensors is customer demand for miniaturized, more integration (more functions on the chip), low-power, and cost effective imaging systems [3]. The quality of an image sensor is largely defined by its dynamic range. As it increases, the sensor can detect a wider range of illuminations and consequently produce images of greater detail and quality. The logarithmic response CMOS image sensor provides a wide dynamic range using the subthreshold region of operation of a transistor. However, at low-illumination levels, their sensitivity is reduced. To alleviate this problem, pixels that combine a logarithmic response at high-illumination with a linear response at low-illumination levels have been designed [4]. Thus, a wide dynamic range is achieved using combined linear-logarithmic response Active Pixel Sensor (APS).

The vast majority of the reported image sensors are implemented in voltage-mode, examples can be found in [3,5–8]. The shrinking feature size of CMOS devices necessitates the reduction of supply voltage to reduce the power dissipation. However, the reduction of supply voltage leads to degrade circuit performance in terms of signal to noise ratio and dynamic range [9-10]. Such drawbacks can be alleviated by operating in the current domain. Current mode operation of various analog circuits is known to offer several advantages, including lower supply voltage, increased dynamic range, smaller area and broad design techniques such as translinear and switched-current circuits. In addition, operations such as addition and subtraction can be more easily implemented in current mode [11-12]. However, current mode imaging structures have suffered from high Fixed Pattern Noise (FPN) due to device parameter variation [10,13-14]. These variations can be removed at the column readout level.

This chapter introduces the motivation and objective of the thesis. It presents the principle of the CMOS image sensors. First, the general structure and the functionality of the basic CMOS image sensors are explained. Then, it summarizes the performance of the wide dynamic range image sensors. Finally, an overview of the current mode and linear-logarithmic image sensors are presented. The chapter concludes with an outline of the thesis.

Motivation

The motivation of this work is to design a wide dynamic range active pixel sensor. The wide dynamic range allows images to represent more accurately the range of intensity levels found in real scenes with little loss of contrast information. Feature size of CMOS technologies is shrinking allowing more functionality at lower cost, however, supply voltages are reduced which causes degradation of signal to noise ratio and dynamic range of imagers. Current-mode pixel allows wide dynamic range at low supply voltage while

improving the signal to noise ratio [9-10]. The linear response of the pixel is also responsible for a high signal to noise ratio.

Objective

The objective of this thesis is to design a wide dynamic range pixel of an image sensor with analog detection of the operating mode of the linear-logarithmic pixel and a delta reset sampling circuit. It demonstrates the implementation and the operation of a mode indicator column circuit which is designed and fabricated in a standard CMOS process. The process technology used for this work is Austrian Micro System (AMS) CMOS 0.35 μm. In this design, the image lag created by the dependence of the reset photosite voltage on the light intensity also affects the image quality. Thus, an offset removal circuit in the column level is required.

CHAPTER 1

IMAGE SENSOR ARCHITECTURE

1.1 Basic Structure of the CMOS Image Sensors and Pixels

The basic structure of a CMOS image sensor is shown in Figure 1.1. As seen, it contains a two dimensional array of pixels and peripheral circuits. Converting the image into electrical signals is performed by a group of pixels that are arranged in a structure of a rectangular form called array. The number of pixels in an array depends on the complexity and the quality of the sensor. To process signals coming from the pixels, one or more pixels are selected depending on a scanning mechanism. The Y-addressing circuit outputs row control the signal to a row to be selected. The X-addressing circuit scans the sampled signals during the horizontal scanning period [2,15-16]. The pixels in the same column share an output bus into the column in order to reduce the number of connections within the matrix.

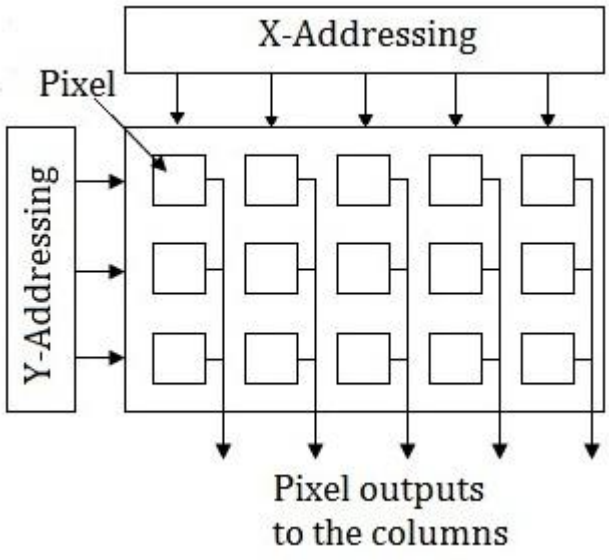


Figure 1. 1 General structure of a CMOS image sensor

Since the array of pixels largely determines the imaging quality of a CMOS sensor [17], it is important to detail the internal structure.

The pixel structure used can be categorized into three types:

- Passive Pixel Sensor (PPS)
- Digital Pixel Sensor (DPS)
- Active Pixel Sensor (APS)

The structure of a passive pixel is very simple. It is composed of a photodiode connected to the integration node, PD, and a select transistor, as shown in Figure 1.2. Signal amplifier is placed in the column level. The main advantage of PPS is its small pixel size with a large Fill Factor (FF), the ratio of the photodiode area to the pixel area. However, noise injected onto the column readout contributes to noise in the output signal. This Signal to Noise Ratio (SNR) issues halted its development [2,15,17].

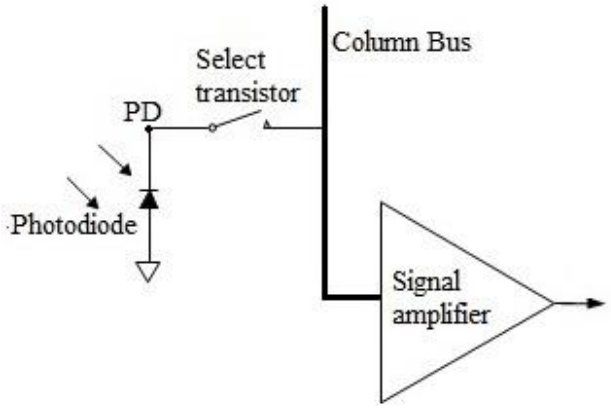


Figure 1. 2 Passive pixel

A digital pixel consists of an ADC in addition to the items in PPS. The idea of performing analog-to-digital conversion at pixel level, which led to what was called digital-pixel-sensor, was first introduced by Boyd Fowler [18] in 1994. It offers several advantages. The elimination of column readout noise increases signal to noise ratio. Since the analog-to-digital conversion is performed within each pixel rather than in column or on the chip level, then the conversion error due to device mismatch is reduced.

Another advantage of this pixel sensor is low power consumption. Since the pixel level ADC can work at very low frequency compared to chip level ADC, the total power consumption can be greatly reduced even with each pixel having its own ADC. The main drawbacks of this kind of pixel are a large pixel size and a low fill factor. The integration of analog-to-digital conversion in pixel level increases the number of transistors of each pixel block. High fixed pattern noise is due to threshold voltage variation of pixel level transistors [2,19-20].

A popular implementation of a CMOS image sensor is based on APS. Figure 1.3 shows a basic active pixel structure. In this concept, a photogenerated charge is amplified in a pixel. As shown in Figure 1.3, a typical three-transistor (3T) APS includes a photodiode, a reset transistor, M_{RS}, a source follower transistor, M_{SF}, as a buffer amplifier to isolate the integration node, PD, from the column bus and a row select transistor, M_{SEL}. The source follower is a voltage buffer, which has a current amplification capability. The advantages of the APS because of the added source follower are the increase of speed and the reduction of noise in the signal readout path [2,15-16]. As a result, the APS improves the image quality compared to the PPS.

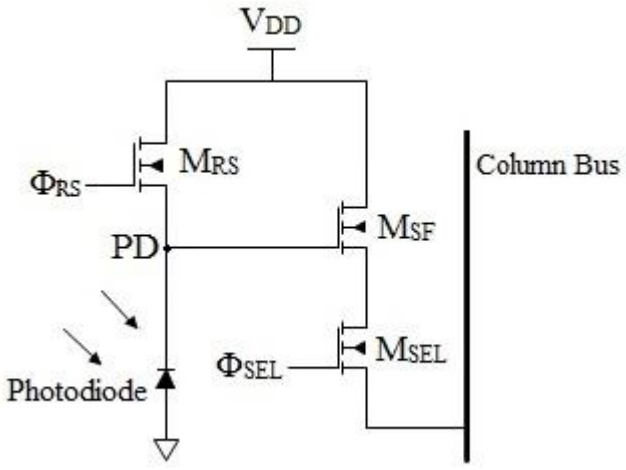


Figure 1. 3 Voltage mode N-type active pixel architecture

Generally, an APS operation is divided into two main stages, reset and integration. During the reset stage, M_{RS} is turned on and the integration node is reset. Then, M_{RS} is turned off and the integration stage starts. During this stage, the photodiode junction

capacitance is charged at a constant integration time. The voltage of the PD decreases according to the input light intensity and the integration time. This voltage is readout in the column output line by enabling M_{SEL}. When the readout process is finished, M_{SEL} is turned off and M_{RS} is turned on again to repeat the process [16-17].

1.2 Fill Factor

In order to maximize the quantity of the light absorbed by the pixel, it is important that the circuitry in the pixel takes up as little space as possible. The photodetector should ideally occupy the majority of the pixel area. This is particularly relevant to the sensors that are optimized for high image quality, such as those used in digital still camera applications [15-16]. The fill factor of a pixel is defined as the ratio of the photosensitive area to the total pixel area. The higher the fill factor, the more sensitive the sensor is. The passive pixels have a large fill factor because there is only one transistor in the pixel, while the fill factor of active pixels varies up to about 70% [16-17]. Finally, the digital pixels have the lowest fill factor because of additional transistors required for analog to digital convertor [15-17].

1.3 Image Sensor Characteristics and Performance

There are several characteristics that qualify the performance of a CMOS image sensor. In this section, the principal performance indicators related to the image sensor circuits are introduced.

1.3.1 Dark Current

Dark current is one of the important parameters to characterize the performance of an image sensor. Its behaviour is composed of several contributions. The dark current produced by a photodiode in absence of the light is dominant, especially with long

exposure time [21]. Spatially uniform dark current can be cancelled by subtraction from optical black pixels. However, dark current varies from pixel to pixel and thus the variation reduces the uniformity of the image for low illumination. In order to have the best image quality, the dark current should be extremely low. Dark current is strongly dependent on the temperature and should be taken into account [15]. Dark current also presents a fundamental limit on sensor dynamic range by reducing the signal swing.

1.3.2 Resolution

One of the important aspects of image sensor performance is its resolution. An image sensor is a spatial and temporal sampling device [2]. The resolution of an image sensor is defined as the number of pixels in the array. Assuming a fixed array size, to increase the resolution, the area occupied by a pixel should be reduced. For this purpose we can optimize the layout design, reduce the number of transistors in the pixel and reduce the size of transistors used. Although the spatial resolution increases with the number of pixels in the array, it depends also on the geometry of the pixels and the optical systems used.

1.3.3 Dynamic Range

The dynamic range of a sensor quantifies its ability to acquire scenes with a wide range of illumination. It is usually less than the dynamic range of a scene. The dynamic range of a sensor is particularly limited by the fabrication technology. It is defined by a pixel's largest non-saturating photocurrent that it can generate divided by its smallest detectable photocurrent [2,17]. The dynamic range can be simply expressed as:

$$DR = 20\log\frac{i_{\max}}{i_{\min}} \quad , \tag{1.1}$$

where i_{max} is the maximum non-saturating photocurrent and i_{min} is the minimum detectable photocurrent.

It is important to note that dynamic range is not the same as signal to noise ratio (SNR). The SNR is measured as the ratio between the signal and the noise for a given light intensity, whereas the dynamic range is the ratio between two light intensities. Good dynamic range is necessary to image a scene with the required details and contrast which can be obtained by design optimizations [22]. The human eye has a dynamic range of about 90 dB, however most of the sensors have a dynamic range of about 65-75 dB which is not sufficient for some applications [16-17]. Two methods for dynamic range improvement are considered. One is to reduce the dark current and expand the dynamic range toward darker scenes. The other is to increase the saturation level of the signal and improve the dynamic range toward brighter scenes [23]. Each of them can be achieved by optimizing the electronic circuits. The smallest signal range depends on the noise. So, the dynamic range is indirectly influenced by the noise. It is impossible to increase the dynamic range by increasing the integration time, because the dark current is integrated in the same way [2].

In addition, although using the smaller CMOS technology will increase the fill factor, the lowest supply voltage reduces the dynamic range. Such drawbacks can be alleviated by operating in the current domain. Early circuit design principles and techniques for current-mode processing are becoming powerful tools for the development of high performance analogue circuits and systems. The performance features of current-mode techniques include increased dynamic range and improved linearity, resulting in optimum design [9]. The pixel working in current-mode will be explained later.

The low dynamic range performance of voltage-mode image sensor cannot meet the requirement of many applications. It is desired to have high dynamic range image sensor to distinguish low contrast signal from high background illumination. In order to increase the dynamic range of the standard image sensor, various solutions and methods have been proposed [16,24-28], using a long integration time, a variable integration time and multiple exposures. However, most result in increased pixel area or integration time, decreased resolution, sensitivity or frame rate. One of the solutions to extend the dynamic

range is to compress the response using a logarithmic sensor. Various designs of logarithmic response image sensor have been developed [29-33]. The basic architecture and functionality of this pixel will be explained in the next section.

1.4 Linear Active Pixel Sensor

One of the main components of the sensors is the pixel linear response. Linear operation of the sensor can achieve large output signals and thus a high signal to noise ratio [34]. Figure 1.3 shows the architecture of a general three transistor APS including pixel reset, M_{RS}, source follower amplifier, M_{SF} and row select, M_{SEL}. The pixel is reset by activating φ_{RS}, which charges the capacitance of the node PD to voltage near V_{DD}. After switching off the reset transistor, during which the photodiode is exposed to the light, the diode voltage variation, V_{PD}, is linearly dependent on the light intensity. After passing a certain integration time, the charge on the photodiode node, PD, is readout through M_{SF} by switching on M_{SEL}. The pixel output voltage is proportional to the light intensity and the integration time. Then, the pixel is reset again for a new cycle.

The dynamic range of a linear region CMOS pixel sensor is limited; for levels of illumination above a certain limit the capacitance completely discharges during the integration phase. Thus, it is not possible to distinguish differences in the input illumination above this limit, as the output voltage saturates to zero. This results in loss of details in brighter regions. Several techniques have been proposed to improve the dynamic range in [35- 38,61]; however this can be achieved by increasing the number of bits per pixel used to represent the image and multiple sampling techniques, which significantly adds to the cost of the final imager [39]. One of the solutions to increase the dynamic range is to design sensors with a non-linear response that compress the dynamic range of the input signal, which is usually achieved by using pixel operating in logarithmic response as explained in the next section.

1.5 Logarithmic Active Pixel Sensor

The logarithmic (log) APS, introduced around 1983 [40], is essentially a nonlinear readout technique. Its function is a result of the subthreshold operation of a diode-connected MOS transistor, added in series to the photodiode [23]. Pixels in logarithmic mode operate continuously and convert the logarithm of the photocurrent into a corresponding voltage without integration process.

Figure 1.4 shows the basic architecture of a logarithmic APS. This three transistor pixel continuously converts incident light into a voltage that is proportional to the logarithm of the light intensity [41]. This pixel does not require reset and operates continuously. The photocurrent, I_{ph}, is small enough to cause the load transistor, M_1, to operate in the subthreshold region. So, the photocurrent, I_{ph}, is equal to the subthreshold current. The V_{PD} is logarithmically dependent on the light intensity, due to the subthreshold operation of M_1 [16,23].

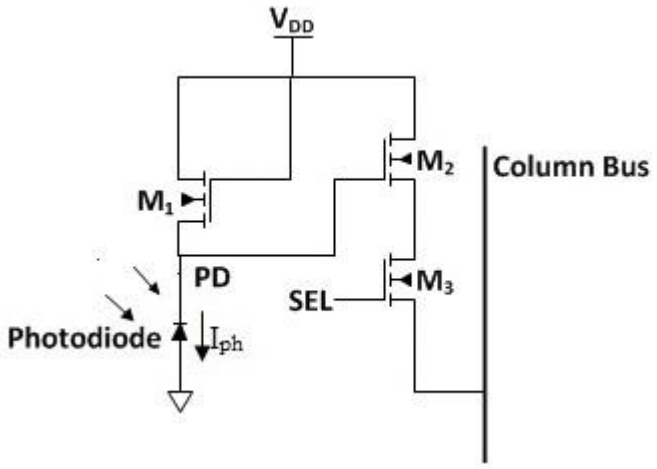


Figure 1. 4 Basic logarithmic pixel architecture

The photodiode output voltage is given by the following equation

$$V_{PD} = V_{DD} - \frac{nKT}{q}\ln\left(\frac{I_{ph}}{I_{D0}}\right) - |V_{th}| \quad , \tag{1.2}$$

where KT/q represents a thermal voltage depending on the temperature in volt, I_{D0} is the current at $V_{th}=V_{GS}$, and I_{ph} is the photocurrent. n denotes the slope factor given by

$$n = 1 + \frac{C_D}{C_{ox}} \ , \tag{1.3}$$

where C_D is the capacitance of depletion layer and C_{ox} is the capacitance of the oxide layer.

Any variation in photocurrent will be logarithmically compressed. Then, the dynamic range of the photocurrent will be increased without having to substantially increase the output voltage swing.

Light levels can range from 10^{-3} lux at night to 10^{5} lux in bright sunlight with the direct viewing of the light source [16]. The advantage of the logarithmic sensors is a simple pixel structure, which has the same number of transistor as a three-transistor APS, while the dynamic range is exponentially increased. In this sensor, ten bits of resolution are sufficient to scene illumination with one percent accuracy for over five decades of luminance. However, to have the same accuracy with a linear sensor, 23 bits are necessary which is not suitable for high speed imaging, data transmission and data storage [22,41]. Another advantage of this technique is to allow for continuous photodiode operation. The photocurrent can be readout anytime and there is no integration involved.

While the logarithmic sensor has the above-mentioned advantages, it suffers from drawbacks such as temperature dependence and low swing of the output, and high fixed pattern noise [16]. The problem of fixed pattern noise is due to the high sensitivity of the MOS subthreshold characteristic to the process variation [23, 41-42]. Also, this form of compression leads to low contrast and loss of details. The response of the logarithmic pixels is light dependent. This means that at low illumination levels, the readout time would be very slow, depending also on the photodiode capacitance, to be able to detect the small currents. Then, in a constant time, the photodiode capacitance is not capable of

being fully depleted. This can lead to image lag and low sensitivity [43]. To alleviate the problem of low light detection, pixels have been designed to operate in combined linear and logarithmic response at low-illumination and high-illumination level respectively. The operating of these combined response pixels will be described in the following sections.

1.6 Image Sensor with Combined Linear-Logarithmic Response

As described in the previous sections, logarithmic response pixels have been used in order to wider dynamic range [23,41]. However, a drawback of these pixels is their limited sensitivity at low light levels [42]. To overcome this disadvantage, the pixels with combined linear and logarithmic response have been proposed [4]. A linear-logarithmic sensor behaves linearly at low light and logarithmically in bright light. A CMOS imager with combined linear-logarithmic operation has been proposed by [43], as shown in Figure 1.5. The operation is explained as follows [42]. The photodiode resets to a voltage V_{bias} that is higher than V_{DD} so that when φ_{RS} is high, V_{PD} is biased to a voltage which is less than the voltage required for sub-threshold conduction across the transistor M_1. Photocurrent produced across the diode will cause to decrease V_{PD} linearly until it reaches to point where sub-threshold conduction occurs. Beyond that point, V_{PD} will vary logarithmically. If the illumination is low, the V_{PD} will not saturate within the integration time. Then the pixel output will response like a three-transistor APS, so called linear operation. However, if the illumination is high, the photodiode will soon become saturated and the V_{PD} will put M_1 into sub-threshold region, operating the pixel in logarithmic mode response. Linear integration mode operation of the sensor can achieve large output signals and thus a high signal to noise ratio. On the other hand, the logarithmic mode of the pixel operation allows a wide dynamic range [34].

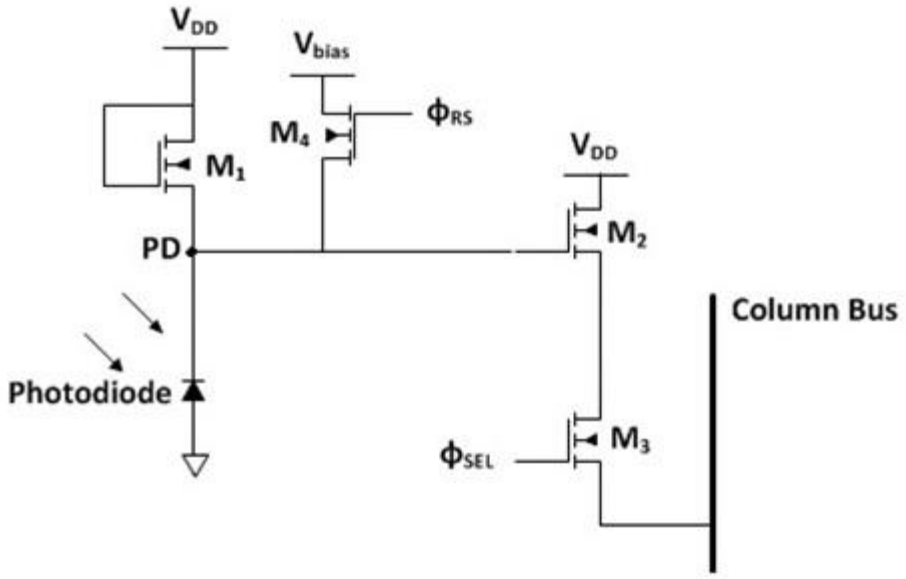


Figure 1. 5 Schematic of a linear-logarithmic pixel

The linear range is adjustable through V_{bias} so that the larger the offset between V_{DD} and V_{bias}, the greater the width of the linear region. This method combines the advantages of linear and logarithmic pixels with a smooth transition between the two modes of response. Then, a dynamic range of over 100dB can be obtained [44-46,62].

1.7 Current-Mode Response Image Sensor

The majority of the reported image sensors are implemented in voltage-mode [3,5-8]. As technology scales down, it necessitates the reduction of supply voltage to reduce the power dissipation. However, the reduction of supply voltage leads to a degraded circuit performance in terms of signal swing, signal to noise ratio and dynamic range [9-10].

In current-mode image sensors, the signal swing is not affected by such trends. Also, they need less silicon area and have higher operation speed [47]. A current-mode APS provides an alternative to the traditional voltage mode.

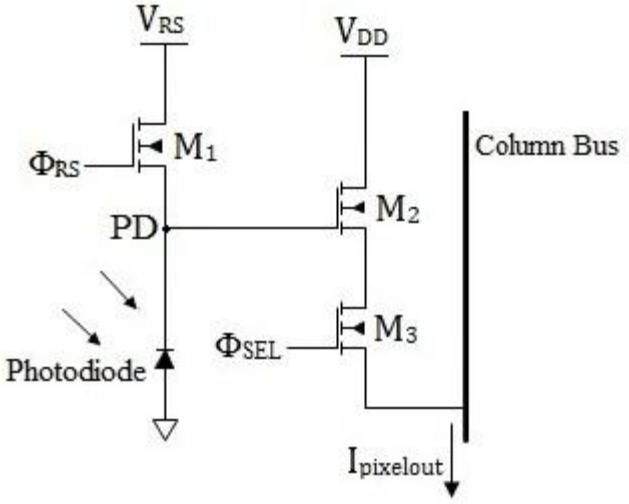


Figure 1. 6 Current-mode image sensor

Figure 1.6 shows the architecture of a current-mode image sensor. It is composed of a photodiode, a reset transistor M_1, an active device M_2, and a row select transistor, M_3. In current-mode pixels, the output voltage in the column bus is fixed. So, it prevents from charging and discharging the column capacitance during readout to maximise the operating speed [10-11,46].

Many current-mode imaging structures have suffered from high Fixed Pattern Noise (FPN) due to device parameter variation and have nonlinear transfer characteristics which have limited the effectiveness of noise suppression circuitry [10-11,13-14]. Active device transistor, M_2, operates in the triode region to convert the photovoltage, V_{PD}, to an output current, $I_{pixelout}$, linearly. For pixel operating in current mode, the column readout circuits work in the current domain.

1.8 Conclusion

In this chapter, we had an overview on the basic CMOS image sensors. The various possible structure of pixels used in sensors was presented. In order to characterize the

CMOS image sensor performance, we introduced its performance indicators. Then, we explained about the current-mode technique and its advantages.

In this thesis a linear-logarithmic active pixel sensor operating in current mode is designed. A high dynamic range is achieved by pixel in both linear and logarithmic modes of operation. If the pixel in the linear image saturates, it is replaced by a corresponding logarithmic operation without the need for a frame memory. In addition, in current-mode pixels, the column bus voltage is fixed. So, a change in the current level through a node is not necessarily accompanied by a change in the voltage level at that node. Hence, parasitic capacitance would not degrade the operating speed. Also, using current-mode have reduces the power consumption because even if the power supply voltage is low, the required dynamic range is achieved. Based on these advantages, we can conclude that it is useful to design our image sensor in linear-logarithmic operation using the CMOS current-mode technology. Next, chapter 2 presents the architecture of a linear-logarithmic APS having a current-mode output.

CHAPTER 2

DESIGN OF IMAGE SENSOR AND READOUT CIRCUIT

2.1 Introduction and Design

Chapter 1 introduced the physical structure of image sensors and their functionality. Based on these concepts, this chapter describes the design steps of the image sensor and readout circuit in detail. The objective of designing the image sensor is to increase the dynamic range. As mentioned in Chapter 1, using current-mode because of the reduction of supply voltage in the shrink size CMOS devices has the advantage of high dynamic range. In addition, the image sensors operating in the combine mode of linear-logarithmic has improved dynamic range compare to the sensors operating in a single mode. Then, in this design, we use the current-mode linear-logarithmic image sensor to have the operating response with high dynamic range. Accordingly, all the circuit in the column are designed in current-mode which is compatible with the image sensor.

Figure 2.1 shows the block diagram of the proposed imaging system, working on current mode.

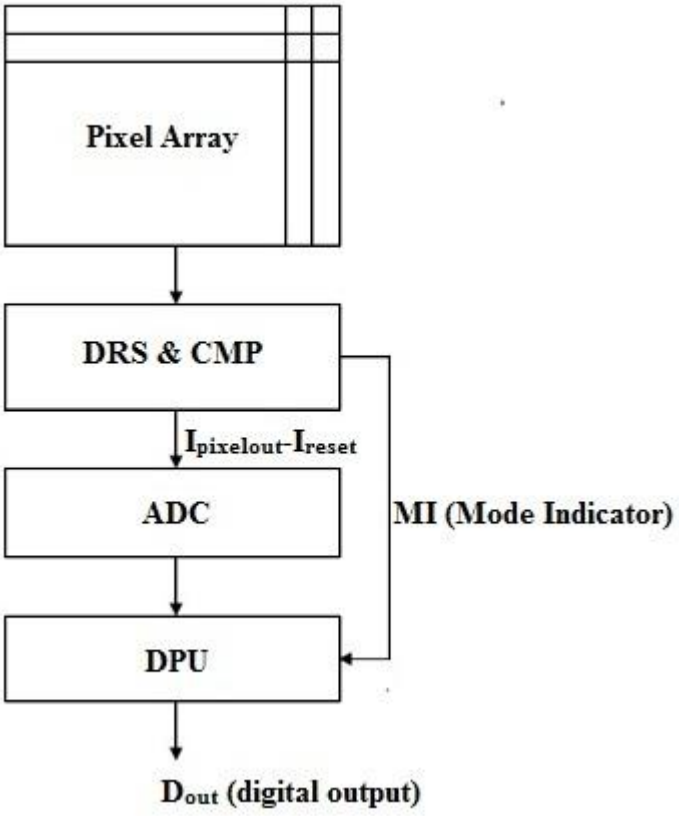


Figure 2. 1 Current-mode imaging system architecture

As mentioned in chapter 1, the designed pixel operates in current-mode with linear-logarithmic response. At the end of the integration time of the pixel, two successive pixel output currents are sampled by the Delta Reset Sampling (DRS) to determine the operating mode response of the pixel. Two roughly similar samples indicate that the pixel is in the logarithmic mode. The response mode is detected by the comparator, CMP. After the reset phase, another sample is sent to the DRS to reduce the FPN and the image lag effect. The current mode DRS sends an offset free current to the current mode analog to digital convertor. The corrected output current is independent of the voltage threshold variations of the pixel read out transistor [13]. The comparator Mode Indicator flag (MI) indicates to the Digital Processing Unit (DPU) when the pixel is operating in the logarithmic mode so that the ADC digital output is converted accordingly.

In the following sections, we will describe the architecture and functionality of the designed pixel sensor and then the related readout circuits. We will discuss about the causes of non-linear output current transfer characteristic and develop an analytical solution that can be implemented in the digital domain.

2.2 Pixel Architecture and Operation

The proposed three-transistor pixel architecture is shown in Figure 2.2.

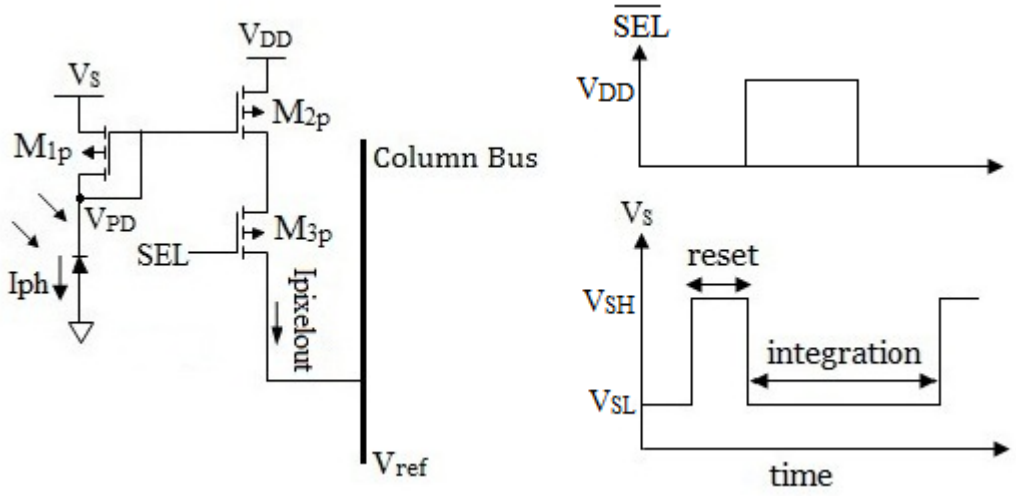


Figure 2. 2 Proposed pixel architecture

The pixel consists of a photodiode, a diode connected transistor M_{1p}, transistor M_{2p} operating in the linear region and a row select switch M_{3p} to connect the pixel to the column bus. The integration voltage, V_{PD}, is converted to an output current, $I_{pixelout}$, by transistor M_{2p}, acting as a transconductance amplifier. In order to increase the dynamic range, the active pixel has been designed in current-mode with a linear-logarithmic response. In current mode pixels, the fixed output voltage V_{ref} prevents from charging and discharging the column capacitance during readout to maximise the operating speed [10]. The drain voltage of M_{2p} should not be far from V_{DD} to ensure that M_{2p} is in the linear region. Under the assumption that V_{ref} is constant, the drain voltage of M_{2p} is

approximately equal to V_{ref}. So, V_{ref} must be close to V_{DD}. The transconductance G_{pix}, given by (2.1), is approximately linear;

$$G_{pix} = \frac{\Delta I_{pixelout}}{\Delta V_{PD}} \approx -\frac{\mu_{2p} C_{ox} W_{2p}}{L_{2p}} \left(V_{DD} - V_{ref}\right) \quad . \tag{2.1}$$

Select switch M_{3p} connects pixel to the output bus. Ideally, M_{3p} has zero on-resistance; meaning that the voltage drop across is 0V. This approximation seen in (2.1) becomes less valid at low supply voltages. The finite on-resistance of M_{3p} produces non-linear effects. The analytical solution for this effect is provided in the next section.

The bias voltage, V_S, determines through transistor M_{1p} the pixel reset-integration phase. The V_{SL} and V_{SH} indicate the low and high level of the bias voltage, V_S, respectively. V_{SH} is chosen to ensure that the gate voltage of M_{2p} is enough to remain 'on' during the reset phase. V_{SL} is selected to set the photodiode current at which the pixel operating mode changes from linear to logarithmic, during the integration time. So, to ensure that M_{2p} is always above threshold:

$$V_S < V_{DD} - \left|V_{thp}\right| \quad . \tag{2.2}$$

The pixel shown in Figure 2.2 operates as follows. At the end of the reset, after charging up the node capacitance C_{PD} through the reset transistor M_{1p}, the photodiode is exposed to the incident light during integration time. It generates the photocurrent I_{ph} that discharges C_{PD}. Then, the photodiode voltage V_{PD} decreases proportionally to the light intensity and the integration time t_{int}.

In the case where the light intensity is not sufficiently strong to decrease V_{PD} substantially, M_{1p} remains in the cut off region. So, the voltage of the photodiode V_{PD} is linearly dependent on the light intensity. It is given by

$$V_{PD} = \frac{1}{C_{PD}} \int_{t_{int}} I_{ph} dt \quad . \tag{2.3}$$

For high intensity incident light, V_{PD} becomes logarithmically dependent on the light intensity, due to the subthreshold operation of the diode connected, M_{1p}, transistor. It is expressed as the equation (1.2), explained in Chapter 1.

The transistor M_{2p} being in linear mode of operation will output a current, $I_{pixelout}$, linearly proportional to V_{PD}, as described by the following equation:

$$I_{pixelout} = \frac{\mu_{2p} C_{ox} W_{2p}}{L_{2p}} \left[(V_{GS} - V_{th}) V_{DS,M_{2p}} - \frac{V_{DS,M_{2p}}^2}{2} \right] \quad , \tag{2.4}$$

where μ_{2p} is the hole mobility, C_{ox} is the oxide capacitance, V_{th} is the threshold voltage, W_{2p} and L_{2p} are the transistor's width and length and V_{GS} is V_{PD}-V_{DD}.
This linearity allows for easy suppression of the variations, appearing as fixed pattern noise, using a current mode delta reset on the column circuit.

Figure 1.A, in Appendix, shows the layout view of the pixel with the labelling of the transistors and inputs. In this design, we have chosen traditional n-well/p-substrate photodiode as photo-detector. This kind of photodiode has relatively good performance compared to other traditional photodiode implementations. Also, it has much lower leakage current and higher sensitivity to visible light compare to n+/p-substrate photodiode. In this layout, the light sensitive area is 53.28μm^2 in which the total area of the pixel is 144 μm^2. So, the fill factor calculated as the percentage of the ratio of these two values is 37%.

Table 2.1 shows the design parameters and characteristics of the pixel. For all the three transistors, the minimum channel length is used. The V_{SL} and V_{SH} are determined as mentioned above. Also, the column reference voltage, V_{ref}, is set up to the value to keep the transistor M_{2p} in linear region as explained before.

Table 2. 1 Characteristics and design parameters of the pixel

Channel Length	0.35 µm
Channel Width	M_{1p}=0.8, M_{2p}=0.95, M_{3p}=0.45 µm
V_S (control voltage)	V_{SL}(integration)=2.35V, V_{SH}(reset)=2.7 V
V_{ref} (output voltage)	3.1 V
Pixel Size	12×12 μm^2
Fill Factor	37%

2.2.1 Pixel Non-linearitiy Analysis

Figure 2.3 shows the output current as a function of time for the linear operating response of the pixel. As it is shown, the different curves are for different widths of the transistor M_{3p}. It can be noticed that the output is not completely linear. The simulation proves that increasing its width even as high as ten times does not solve the linearity problem while increasing dramatically the pixel area.

A first degree contribution to this nonlinearity is the ‘’on’’ resistance of the select transistor, M_{3p}, which exhibits an increasing drain-source voltage drop as the output current increases. To eliminate the effect caused by M_{3p} ‘on’ resistance, R_{on}, we rely on the digital domain after ADC conversion to apply a linearization function.

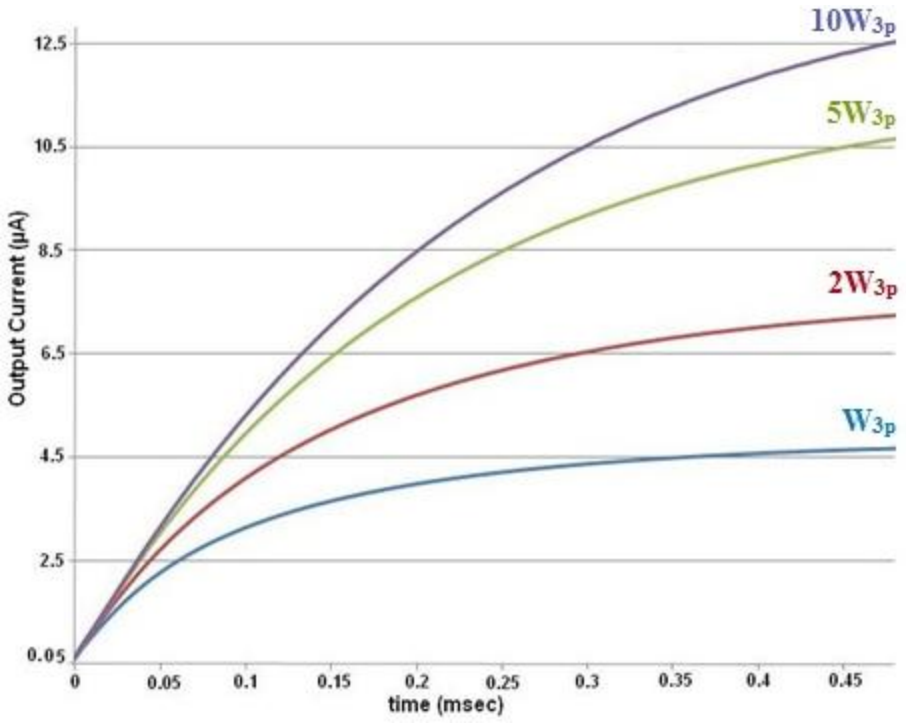


Figure 2. 3 Simulated linear current response for different width of M_{3p}

Another non-linearity effect comes from the variation of the photodiode voltage as a function of time, as shown in Figure 2.4. Since the technology used for chip design does not offer photodiode model, the schematic level simulation have to be carried out using a simplified photodiode model that was approximated as a capacitor in parallel with an ideal current source to discharge the diode capacitance. It is suspected that the slight nonlinearity comes from the photodiode capacitance variation as a function of V_{PD}.

Another cause of non-linearity is the hole mobility degradation of transistor M_{2p} as a function of V_{GS}. It has also been recognized as an important source of non-linearity for current-mode active pixel [10,13,48].

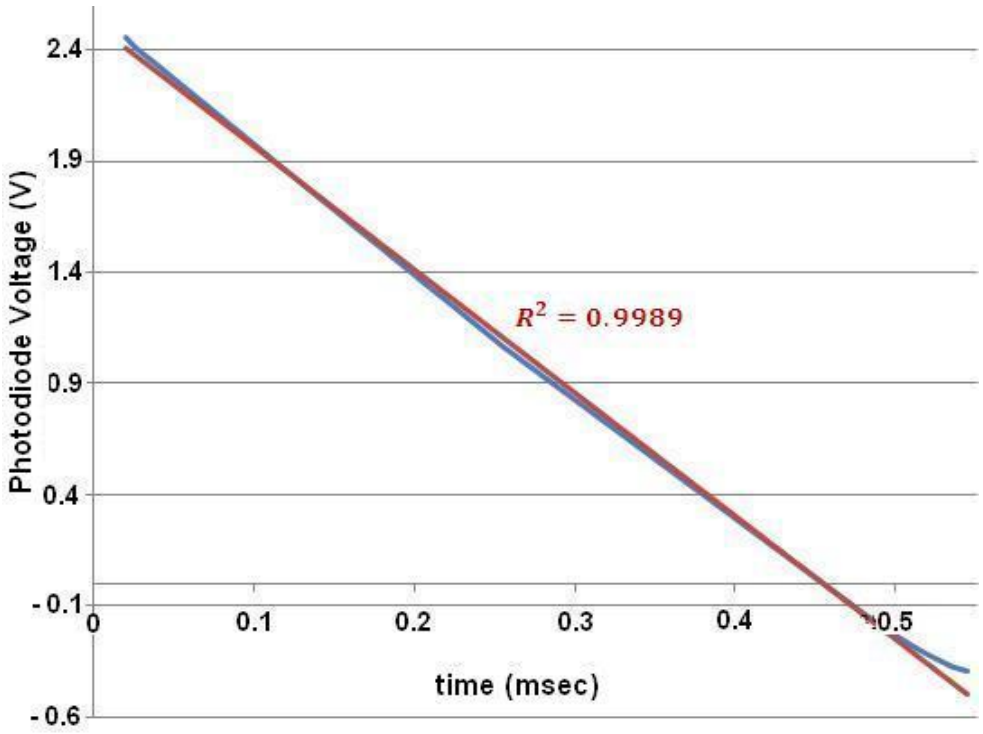


Figure 2. 4 Simulated photodiode voltage variations as a function of time

2.2.2 Analytical Solution

To remove the non-linearity effect coming from the R_{on}, we use an analytical solution that can be implemented in the digital domain [46]. The transistor M_{2p} works in the linear region, so the relationship between its output current and its gate voltage, V_{PD} is linear as shown in equation (2.4). The square term is neglected as $V_{DS,M_{2p}}$ has a small value. From Figure 2.2, we have:

$$V_{DD} - V_{ref} = V_{DS,M_{2p}} + R_{on} I_{pixelout} \quad . \tag{2.5}$$

In ideal case, assuming that the pixel output current is linear and there is no voltage drop over R_{on}, $V_{DS,M_{2p}}$ is equal to 0.2V. According to the equation (2.4) we have:

$$I_{lin} = \frac{\mu_{2p} C_{ox} W_{2p}}{L_{2p}} (V_{GS} - V_{th}) 0.2 \quad , \tag{2.6}$$

in which the last term of the equation is neglected.

Deducing $V_{DS,M_{2p}}$ from both of the equation (2.4) and (2.5), and replacing V_{DD}-V_{ref} by 0.2V, we have the following equation

$$\frac{I_{pixelout}}{\frac{\mu_{2p} C_{ox} W_{2p}}{L_{2p}} (V_{GS} - V_{th})} = 0.2 - R_{on} I_{pixelout} \quad . \tag{2.7}$$

Using the last two equations results in the linearization function for a non-negligible R_{on} as in the following

$$I_{lin} = \frac{I_{pixeloout}}{1 - 5 R_{on} I_{pixelout}} \quad . \tag{2.8}$$

This correction can be performed numerically by the digital processing unit. Also, we can use the geometric series to obtain approximately the same result as the fractional form. It is therefore easier to implement in digital circuit than the fractional form. The geometric series of the equation (2.8) will be as the following

$$\frac{I_{pixelout}}{1 - 5 R_{on} I_{pixelout}} = I_{pixelout} \sum_{n=0}^{\infty} \left(5 R_{on} I_{pixelout}\right)^n \quad \text{,for } \left|5 R_{on} I_{pixelout}\right| < 1 \quad . \tag{2.9}$$

The condition will be satisfied since the R_{on} is on the order of ohms and $I_{pixelout}$ is on the order of micro-ampere.

Before digitizing the analog current $I_{pixelout}$, a current memory performing a Delta Reset is employed to remove the FPN due to variations of transistors M_{1p} and M_{2p} threshold

voltage [28]. Therefore the output current converted by the current mode ADC is I_{out}-I_{reset}. In the context of an ASIC CMOS sensor with on-chip ADC and digital processing, the linearization function (2.8) must be realized effectively with an easy to implement arithmetic logic unit.

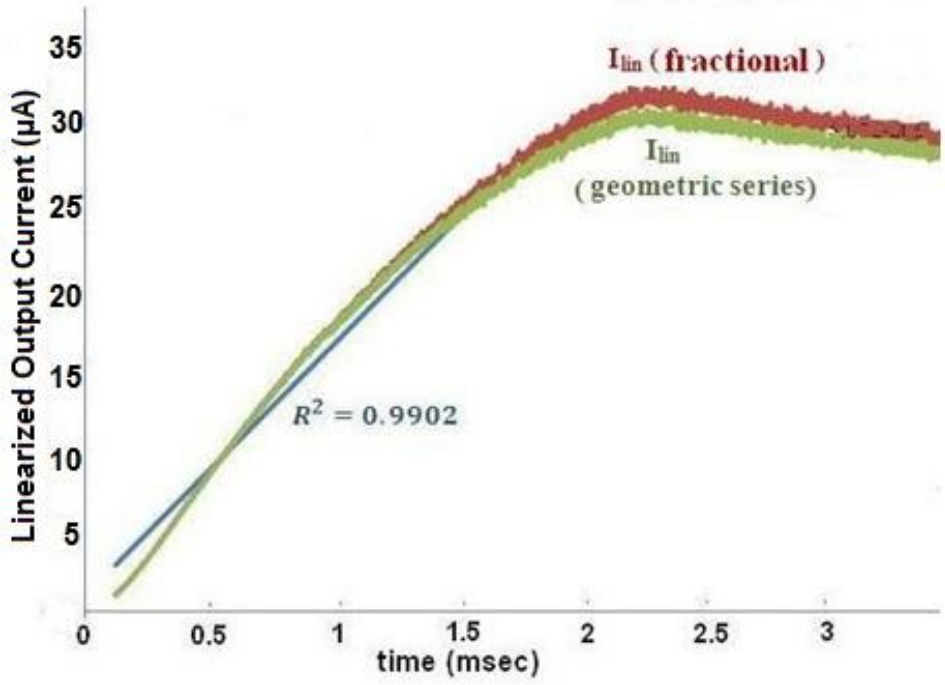


Figure 2. 5 Experimental results of the linearized pixel output current

Figure 2.5 shows the linearized experimental results with both fractional equation (2.8) with a residue of 0.9902, and its geometric series, equation (2.9). A geometric series of 16 terms must be used to obtain approximately the same result as the fractional form. However for an ADC of up to 10 bits, a lookup table could also be used with the advantage of a higher conversion rate. This result obtained when V_{SL} set to zero. Then, the pixel operates in the linear mode response and depending the light intensity it saturates after passing time.

According to the Figure 2.2, when the light intensity increases, the photodiode voltage, V_{PD}, decreases. The maximum pixel output current, $I_{pixelout}$, is obtained when the forwarding bias current of the photodiode is equal to I_{ph}, according to the photodiode

characteristic. After that V_{PD} remains constant and the $I_{pixelout}$ is constant as well. In the Figure 2.5, it is seen that $I_{pixelout}$ is starting to decrease. This behaviour comes from the threshold voltage temperature dependence of M_{1p} and M_{2p} which affects directly the output current [49]. This part of the output characteristics cannot be linearized using our simple mathematical solution.

2.3 Current-Mode Column Readout Circuits

This section describes the design of the column readout circuit for a current-mode linear-logarithmic pixel. The design includes the circuits required to copy the output current of the pixel into the column, to remove the offset and to determine the operating mode of the pixel. After photocurrent integration in the pixel, readout is performed by transferring the pixel output current to the column circuit. One of the important circuits in the column is a delta reset sampling used to cancel device parameter variations. A current conveyor is used to fix the pixel output voltage and provide a copy of the pixel output current [10].

2.3.1 Current Conveyor

The first part of readout circuitry in current-mode pixels is a current conveyor circuit. The concept of current conveyor is the current conveyed between two ports at different impedance levels [50]. It was initially proposed by Smith and Sedra in 1968 [51-52]. The current conveyor offers several advantages over the conventional opamp. It can provide a higher voltage gain over a larger signal bandwidth under small or large signal conditions [9].

Figure 2.6 represents a block box of current conveyor. If one of the input terminals is connected to a voltage, an equal voltage will appear on the other input terminal. In a dual manner, if a current is applied through one input, an equal current will flow through another input and the same current is conveyed through output terminal. Its operation is

explained in [9,50]. The potential of X, v_X, being set by v_Y is independent of the current being forced into port X. Similarly, the current through input Y, i_Y, being fixed by i_X is independent of the voltage applied at Y.

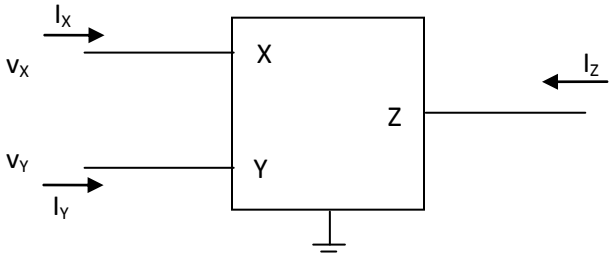


Figure 2. 6 Basic block diagram of a current conveyor

Current conveyor can be applied in a variety of analog circuits. It can be used to have a fixed voltage node and to copy the input signal as shown in Figure 2.7 for the first generation Current Conveyor (CCI). Assuming that transistors M_3-M_5 are matched, it can be shown that the currents through them are equal. This forces transistors M_1 and M_2 to have equal currents and thus equal V_{GS} drops. Thus X and Y track each other in both voltage and current.

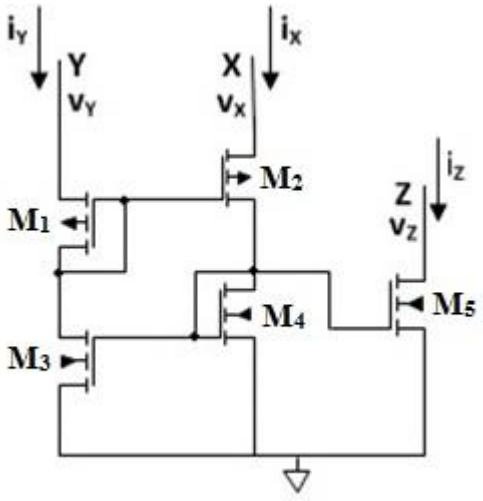


Figure 2. 7 CMOS implementation of CCI

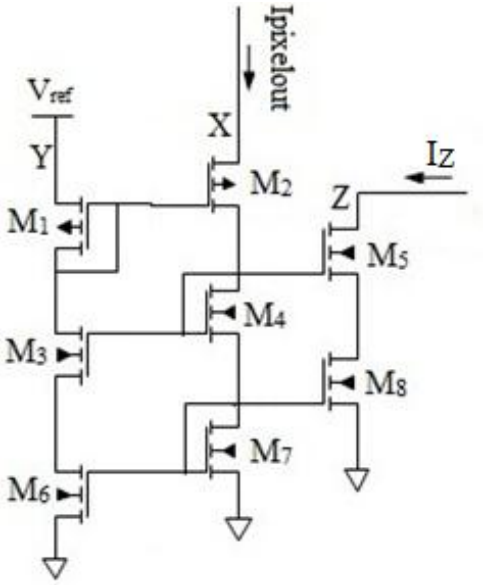


Figure 2. 8 Current conveyor

In this design, we use the cascoded current conveyor, adding the transistors M_6-M_8, as shown in Figure 2.8. This architecture reduces the channel length modulation, and the output current is more precise. We connect the first branch, Y, into an external biasing voltage as V_{ref}. The next branch, X, is connected to the pixel output. Then, the voltage of the column bus will be the same as V_{ref}. Accordingly, the pixel output current will be copied in the branch Z by adjusting the transistors dimensions as in Table 2.2, so that I_Z is equal to $I_{pixelout}$.

Table 2. 2 Parameters values of the current conveyor circuit

Parameter	**Value**
V_{ref}	3.1V
$W_{M1,M2}$	2μm
$W_{M3,M4,M5,M6,M7,M8}$	1μm
L (all transistors)	3μm

2.3.2 Current-Mode Offset Cancellation Circuit

A common approach used in voltage mode active pixel sensors is to eliminate offset caused by random variations in the threshold voltage of the pixel transistors with Correlated Double Sampling (CDS). The CDS circuit, usually located at the bottom of each column, subtracts the reset value from the signal pixel value [16]. In current mode active pixel sensors a DRS circuit is used as an offset suppression circuitry. It is implemented in a switched-current memory cell shown in Figure 2.9.

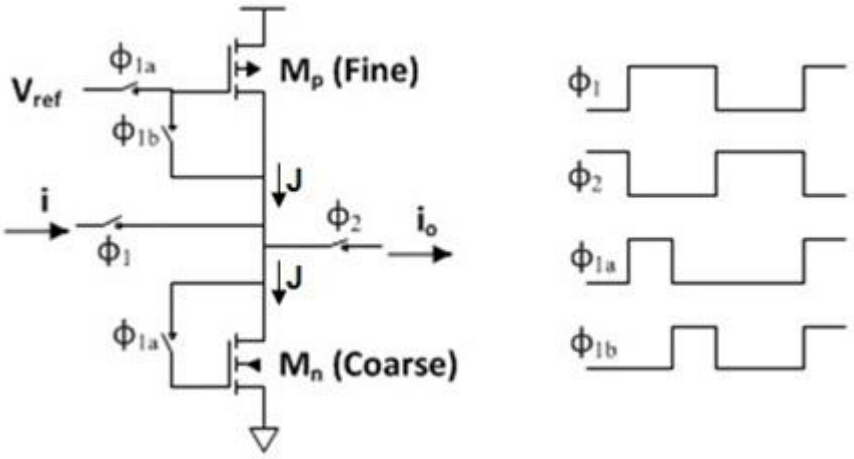


Figure 2. 9 Basic two-step sampling current memory cell

Error cancellation is achieved by switches through a non-overlapping two-step sampling process. In this so-called S^2I memory cell [53], the signal is sampled by the NMOS memory, M_n, during the first (coarse) step, φ_{1a}. When the cell has settled, all of the signal current together with the bias current, J, flows into the coarse memory. Then, during the second (fine) step, φ_{1b}, the error is sampled and stored in the PMOS memory, M_p, while the bias current flows through the transistors. On the output phase, the subtraction of these two signals appears at the output which is also free of the bias current.

The applications for switched-current systems will be much the same as for switched-capacitors. Linear floating capacitors are not needed in switched-current circuits. In principle, voltage swings need not to be large as signals are represented by currents [9].

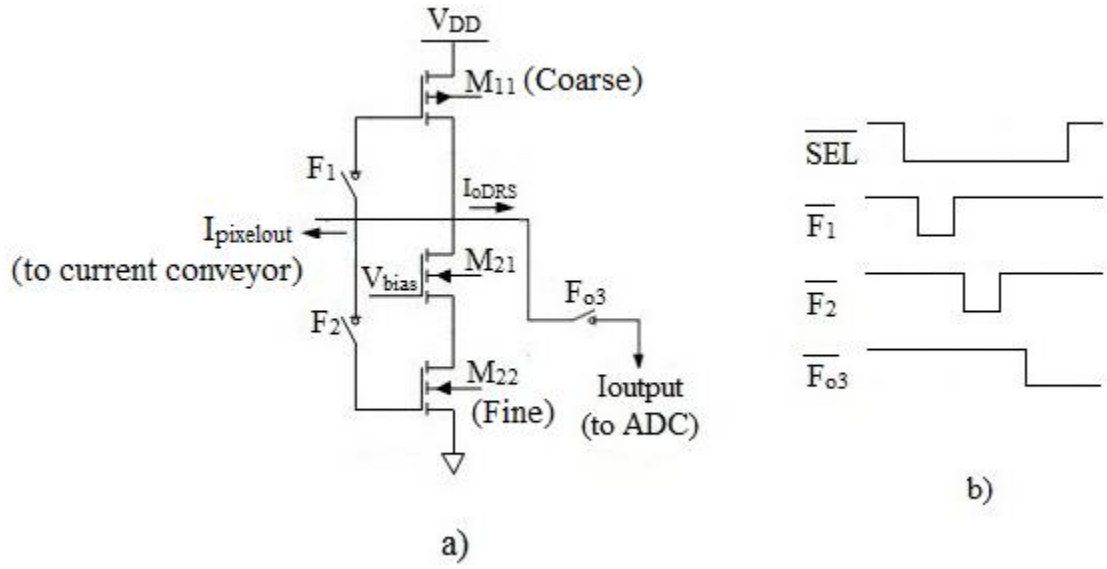


Figure 2. 10 a) Proposed switched-current memory cell (DRS) b) Clock waveforms

Figure 2.10 a) shows the modified current memory cell working as delta reset sampling circuit, different from the basic one. It is connected to the designed current conveyor, node Z of the Figure 2.8, in which the pixel output current passes. The incoming current of the DRS, $I_{pixelout}$, is controlled by SEL switch which is in the pixel, Figure 2.2.

In this design, M_{11} operates as the coarse memory while M_{22}, which is cascoded with M_{21} to reduce the effect of channel length modulation, works as the fine memory. The error of channel length modulation created by M_{11} will be removed from fine memory in subtraction cycle. Then, we only use the cascode version for the fine part. The width of cascode transistor M_{21} is adjusted to minimise the drain-source voltage of M_{22}, while adjusting V_{bias} to ensure that the transistor is saturated in the range of the input current. The clock waveforms are shown in Figure 2.10 b). The select switch transistor located in the pixel, Figure 2.2, acts as the input switch for the DRS circuit. While the select signal is low, the two sampling of coarse and fine memory are done respectively.

In our work, the design procedure was adopted for optimizing the cell performance as shown in Table 2.3. In memory cell design, transistor sizing is a very important procedure to get behaviour close to optimum performance.

Table 2. 3 Parameters designed values

Parameter	Value
W_{M11}	3.2μm
W_{M21}	2.0μm
W_{M22}	1.0μm
L (all transistors)	9.0μm

2.4 Mode Indicator Circuits

In order to determine the operating mode of the pixel, we need a circuit block to detect the pixel output current and recognize its operating mode. For this purpose a current comparator circuit is needed to compare two successive currents. If these two currents are similar, then the pixel is in the logarithmic mode of operation. Otherwise, it is in the linear operating mode. However, these sampled current must be kept in order to be compared. Consequently, we introduce an integrator with capacitive feedbacks before the comparator circuit. The functionality of each circuit is explained in the following sections.

2.4.1 Integrator

This block consists of a simple one stage fully differential amplifier with Common Mode Feedback (CMFB). A differential feedback loop with high loop gain is used to control the common mode output voltage [54]. Figure 2.11 shows the schematic of the circuit.

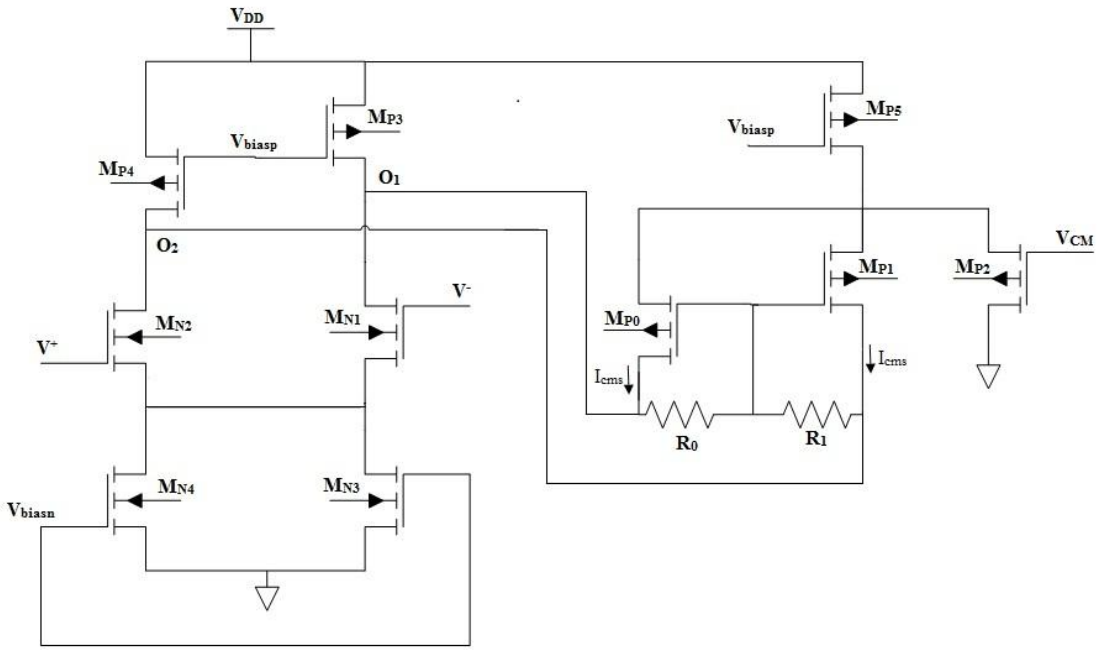


Figure 2. 11 One stage fully differential amplifier with CMFB

The simple fully differential amplifier consists of a differential pair M_{N1}-M_{N2}, active loads M_{P3} and M_{P4}, and tail current sources M_{N3} and M_{N4}. For the op-amp, an ideal operating point biases M_{N1}-M_{N4} and M_{P3}-M_{P4} in the active region and sets the DC common mode (CM) output voltage, V_{OC}, to the value that maximizes the swing at the op-amp outputs for which all transistors operate in the active region. However, V_{OC} is very sensitive to mismatch and component parameter variations, so that accurately setting it to a desired voltage is impossible in practice. To set V_{OC} to a desired DC voltage that biases all transistors in the active region and maximizes the output voltage swing, either V_{biasp} or $V_{GS\text{-}MN3}$ must be adjusted. Adjusting $V_{GS\text{-}MN3}$ to force V_{OC}=V_{CM} requires the use of feedback in practice which will be referred to as the common-mode feedback (CMFB). A straightforward way to detect the common-mode (CM) output is to use two equal resistors [54], R_0 and R_1, as shown in Figure 2.11. This CMFB uses resistive divider and a modified CM sense amplifier that injects currents into the opamp to control the opamp CM output voltage. The voltage between the two resistors is

$$V_{oc} = \frac{(V_{o1} + V_{o2})}{2} \quad . \tag{2.10}$$

This modified CM-sense amplifier directly injects currents to control the opamp CM output. The dimensions of the transistors are shown in Table 2.4. The current injected by M_{P0} and M_{P1} into either output is

$$I_{cms} = \frac{I_{MP5}}{4} - \frac{g_{m-MP0}}{2}(V_{oc} - V_{CM}) \quad . \tag{2.11}$$

Transistors M_{N3},M_{N4}, M_{P3} and M_{P4} act as current sources. The CMFB loop will adjust I_{cms} so that:

$$|I_{D-MP3}| + |I_{D-MP4}| + 2I_{cms} = I_{D-MN3} + I_{D-MN4} \quad . \tag{2.12}$$

If $V_{oc}=V_{CM}$, M_{P0}, M_{P1}, and M_{P2} give $2I_{cms}=I_{MP5}/2$. Therefore, I_{MP5} should be chosen so that:

$$|I_{D-MP3}| + |I_{D-MP4}| + \frac{I_{MP5}}{2} = I_{D-MN3} + I_{D-MN4} \quad , \tag{2.13}$$

when all devices are active. Accordingly, in the CM-sense circuit, $(W/L)_{MP0}=(W/L)_{MP1}=0.5(W/L)_{MP2}$. Table 2.4 shows the design parameters and transistors dimensions in order to operate the differential amplifier with common-mode feedback properly.

Table 2. 4 Transistor's parameter values of the differential amplifier with CMFB

Parameter	Value	Parameter	Value
$W_{MP3,4}$	5.0μm	W_{MP5}	11.2μm
$L_{MP3,4}$	0.7μm	L_{MP5}	3.0μm
$W_{MN1,2}$	6.4μm	$W_{MP0,1}$	4.0μm
$L_{MN1,2,3,4}$	2.0μm	$L_{MP0,1,2}$	2.0μm
$W_{MN3,4}$	11.4μm	W_{MP2}	8.0μm
V_{biasp}	2.3V	$R_{0,1}$	200KΩ
V_{biasn}	0.7V		

Capacitors are then introduced between the inputs and outputs to sample the current coming from the DRS circuit. Figure 2.12 shows the integrator.

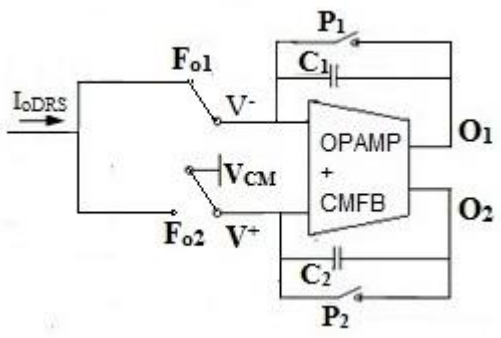
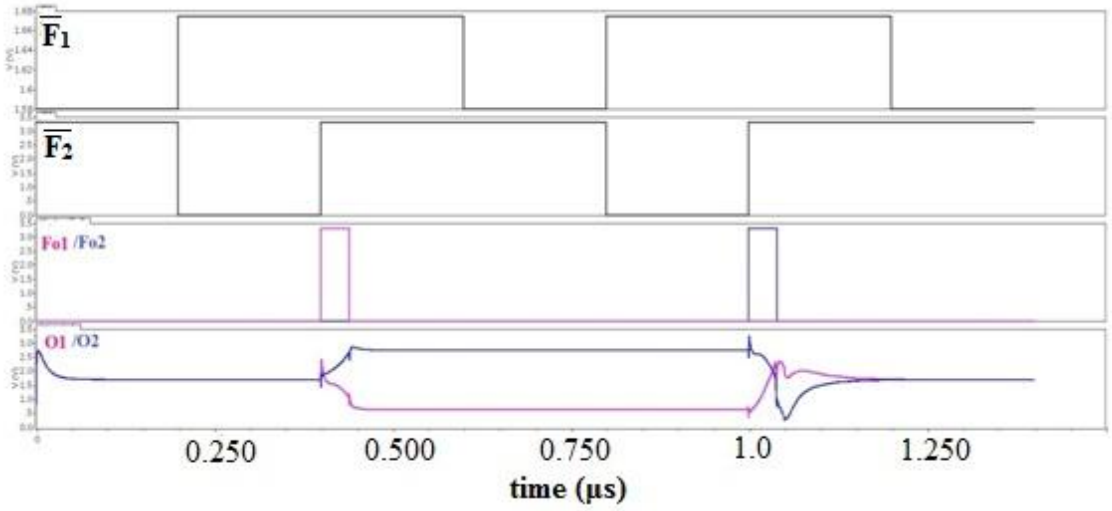


Figure 2. 12 Differential integrator

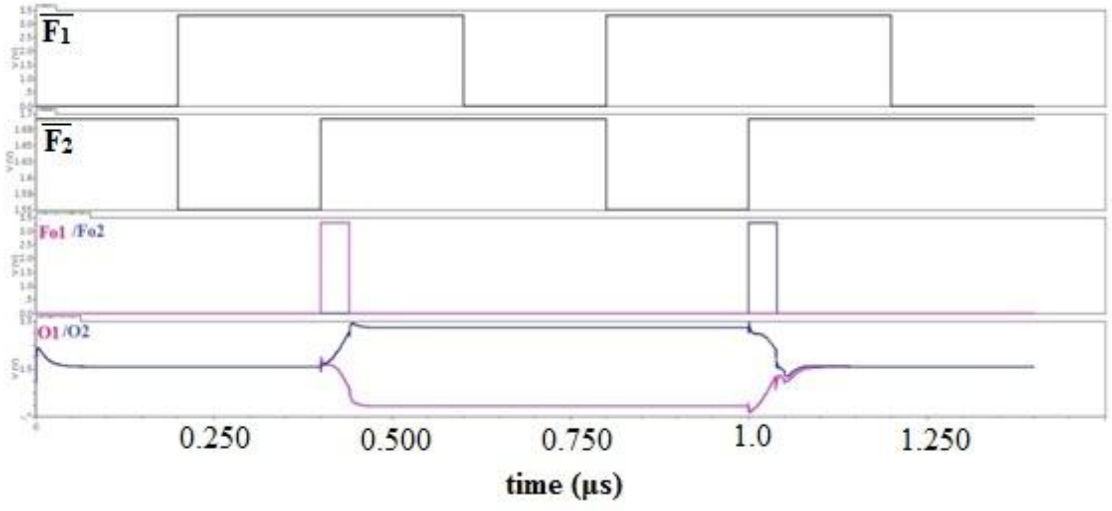
In this circuit, we used two switches, F_{o1} and F_{o2}, in order to transfer the sampled current coming from DRS circuit. During each phase of input F_{o1} or F_{o2}, one is connected to the I_{oDRS}, while the other input is connected to the common mode voltage, V_{CM}. The current sampled creates voltages across capacitors C_1 and C_2. The switches P_1 and P_2 reset the capacitors before starting the output phases, so the inputs and outputs of the integrator are on a common mode voltage level.

First, switches P_1 and P_2 are closed and the capacitors are reset. Then, we open them and the first sample charges up C_1 during F_{o1}. During this time, C_2 charges at the same rate as

C_1. Due to the CMFB, while O_1 is decreases, O_2 increases, so the average output remains V_{CM}. During F_{o2}, the second current sampled discharges C_2 and C_1. If the second sample is larger than the first one, the slope of the discharge will be greater. In this case, the pixel operates in linear mode response. Otherwise, the second sample is similar to or smaller than the first one when the pixel is in the logarithmic response.



a)



b)

Figure 2. 13 Integrator output for the pixel operating in a) linear operating mode and b) logarithmic operating mode

Figure 2.13 a) and b) shows the simulation results of these two conditions, respectively. As seen, in the linear operating mode of the pixel, at the end of the stage F_{o2}, O_1 is greater than O_2 while in the logarithmic response O_1 is smaller than O_2. The constant output values appearing before F_{o1} pulse and after F_{o2} pulse are fixed by the CMFB at 1.65V. The maximum and minimum values of output voltage at the end of a current sampling are limited by the op-amp dynamic range which is approximately 1.3V.

Figure 2.14 shows the output swing of the differential amplifier with CMFB. One of the inputs sets to 1.65V while the other sweeps from 0V to 3.3V. The differential output varies from 1.074V to 2.375V.

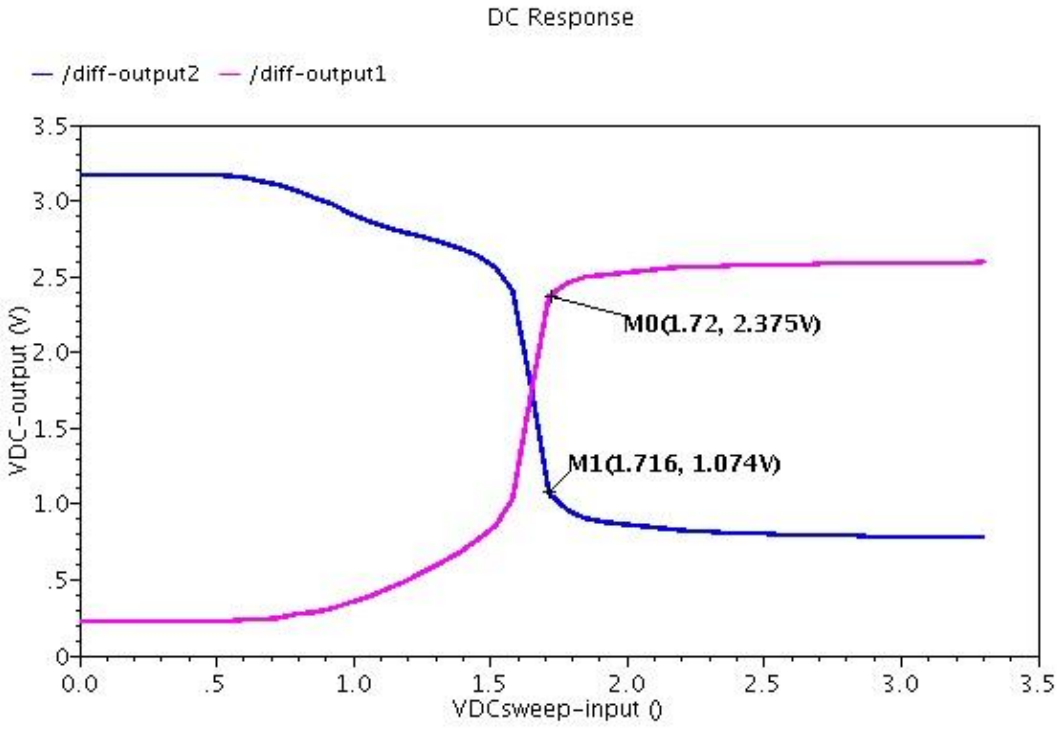


Figure 2. 14 Output swing of the differential amplifier

Figure 2.A, in Appendix, shows the layout view of the integrator. We use inter-digitization finger technique to improve transistor matching in the differential pair and the CM amplifier, and also common centroid structures to improve matching between components in the layout. The resistors are implemented by n-well layer.

2.4.2 Comparator

Comparators are widely used in many analog circuits. The low power comparator operation is based on a positive feedback loop of two back-to-back inverters in order to convert a small input-voltage difference to a full scale digital level in a short time. Its operation is controlled by clock signal pulses. When the clock is low (reset phase), the output node is reset to V_{DD}. During the reset phase of the comparator and after it has finished regeneration, there is no supply current [55-56].

There is a large variety of CMOS latched comparators. One of them is static latched comparator in which the regeneration is done by two class A cross-coupled inverters. These comparators are always consuming current even after regeneration therefore; it is not attractive for low power operation [57]. Another type of comparators are more power efficient than the static comparators [58]. However, there is still supply current in the reset phase and after the comparator has finished regeneration. In the dynamic latched comparators, there is only current flowing during the regeneration [58-59]. Figure 2.15 shows the schematic diagram of a dynamic latched comparator.

The differential pair transistors, M_{N11} and M_{N12}, are input transistors. M_{N14}/M_{P12} and M_{N15}/M_{P11} compose a latch structure. M_{N13} is used for power reduction and the other transistors are used for reset. The comparator is controlled by a single clock phase. During the reset phase, when clock is low, transistors M_{P13}/M_{P14} and M_{P17}/M_{P16} reset the output nodes and drains of the M_{N11}/M_{N12} to V_{DD}. M_{N13} is off and no supply current exists. When the clock goes high, the reset transistors are opened and the current starts flowing in M_{N13} and in the differential pair. Depending on the input voltage, one of the cross-coupled inverter that makes the regeneration, M_{N14}/M_{P12} or M_{N15}/M_{P11}, receives more current and determines the final output state. After regeneration is completed, one of the output nodes is at V_{DD}, and the other output and both drains of the differential pair are at 0V. In this situation, there is no supply current, which maximizes the power efficiency [58-59].

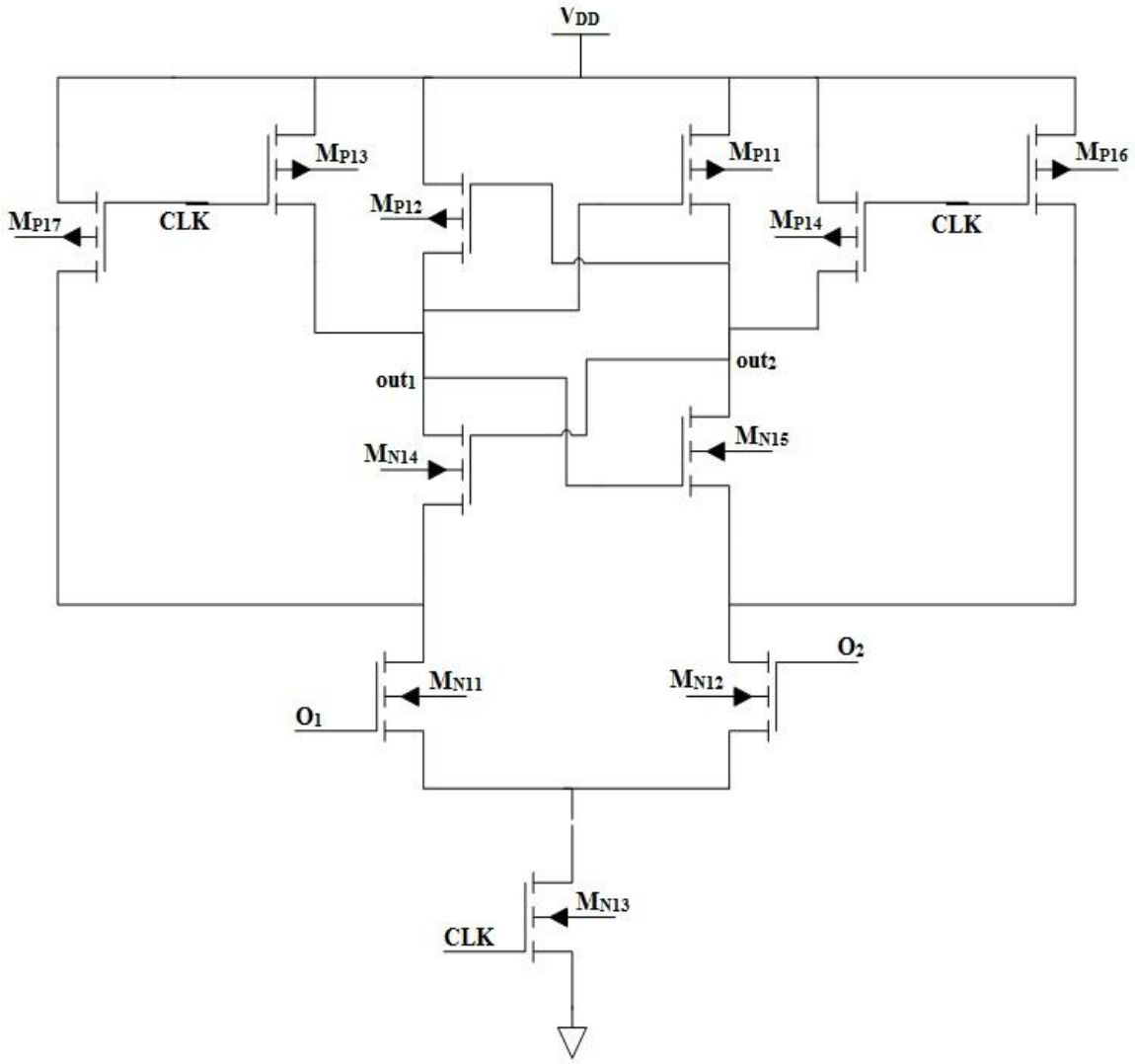


Figure 2. 15 Dynamic latched comparator

According to the pixel response, when it is in linear operating mode, the two successive currents are different and the first one is smaller than the second one. So, the comparator output should be “1”. However, in the logarithmic mode of operation, these currents are sometimes equal or the second current sampled is smaller than the first one. In this state, the comparator output changes to “0”. These normal operating states of the comparator can be altered by the mismatch resulting from variations of the fabrication process, which deteriorates the accuracy of the comparator.

The copied output currents, I_{oDRS}, are integrated into the capacitors C_1 and C_2 which determine O_1 and O_2. The charging and discharging of capacitors C_1 and C_2 of the integrator during a given time, Δt, is expressed as the following equation.

$$I_1\Delta t = C_1\Delta V1 \quad , \quad I_2\Delta t = C_2\Delta V2 \quad . \tag{2.14}$$

Table 2.5 shows the possible comparator output cases. The unwanted output states marked with an "X" must be avoided in order to prevent a wrong conversion at the DPU level [62].

Table 2. 5 Comparator output for different input cases

CASE	I_{oDRS}	Input voltages	out
1	$I_1=I_2$	$O_1<O_2$	"0"
		$O_1>O_2$	X
2	$I_1>I_2$	$O_1<O_2$	"0"
		$O_1>O_2$	X
3	$I_1<I_2$	$O_1<O_2$	X
		$O_1>O_2$	"1"

Corner analysis simulations have been done in order to solve the problem of the unwanted output states of case 1 and case 2. According to the simulation results, we deduced that a capacitor ratio, C_2/C_1, of 1.12 is required to overcome the mismatch effect responsible for those unwanted output states. In the linear operating mode of the pixel, the case "3" unwanted output state may happen for small currents. However, this problem can be controlled by increasing the integration time to ensure that O_1 is larger than O_2.

The capacitor value is calculated using

$$C = C_{ox} W \cdot L \quad , \tag{2.15}$$

where C_{ox} is the capacitance of the oxide layer per unit area. Its value in AMS 0.35μm process is 0.86 fF/μm^2, L and W are length and width of capacitor, respectively. The parallel plate capacitors are implemented using two poly layers. The two layers act as the parallel plates. We use W=L so that a square capacitor implementation is possible. Values of W = L calculated using the equation mentioned above is an approximate value. In this design, using common centroid method and the equation (2.15) for W=L, we split each capacitor into 12 alternate components. For each component, we have W_1=L_1=7.5μm and W_2=L_2=7.9μm. Then, C_1 and C_2 are approximately 580.5fF and 644.1fF respectively.

2.5 Conclusion

In this chapter, the implementation of CMOS pixel and the column circuits are presented. In this design, the current-mode pixel has the combined linear-logarithmic operating response with the advantages of a high dynamic range. The output current suffers from image lag and the offset created by the voltage threshold variation of the pixel readout transistor. In order to reduce these effects, we used a DRS circuit which sends a corrected output current to the current-mode ADC. The pixel output current should be linearly proportional to the photodiode voltage for easy suppression of the variation. Then, an analytical solution is presented to overcome the nonlinearity coming from the ‘’on’’ resistance of the select transistor is introduced.

The DRS is also used to determine the operating mode of the pixel response in order to be converted properly by the DPU. In addition, to determine the pixel operating mode, we used an integrator and a comparator circuit in the column level. In the next chapter, the experimental results of the fabricated prototype will be presented.

CHAPTER 3

EXPERIMENTAL RESULTS

This chapter presents the experimental results obtained on the response of the pixel over light illumination, the delta reset sampling function, and the comparator operation. The chip is fabricated in a two-poly, four-metal CMOS 0.35 μm process from AMS accessed through the Canadian Microelectronics Corporation (CMC). The device is then enclosed with a 68-pin DIP package.

The principal objective is to verify the operating mode of the pixel and the functionality of the surrounding circuits. Besides, some of the theoretical concepts of Chapter 2 are validated. The prototype contains a 3x3 pixel array, a current conveyor, a DRS circuit, a differential amplifier with CMFB, and a CMP. It is noted that only the pixel in the middle of the array is functional. The others are used as dummy to obtain the same mechanical stress around a pixel as it would be found in a pixel array. The standard MOS transistor models for circuit simulation does not include any stress effects. Therefore, it cannot correctly predict the circuit performance under variable applied mechanical stress, leading to imprecise simulations.

3.1 Test Requirements

For the purpose of the test, the chip was mounted on a Board. The instruments utilized are the Agilent E3631A and the Xantrex LXQ 20-3 DC Power Supply for bias, supply and ground voltages, the Tektronix MSO 3012 16 CH and the Hewlett Packard 54645D Mixed Signal Oscilloscope for measurement of the pixel response and column circuit outputs, the Tektronix AFG 3021B Single Channel Arbitrary Function Generator and the Agilent 33220A Arbitrary Waveform Generator for square-wave generation using an external clock to trigger, the Tektronix TLA715 Logic Analyzer to generate the digital waveforms. The TLA Pattern Generator Module generates the digital synchronization signals.

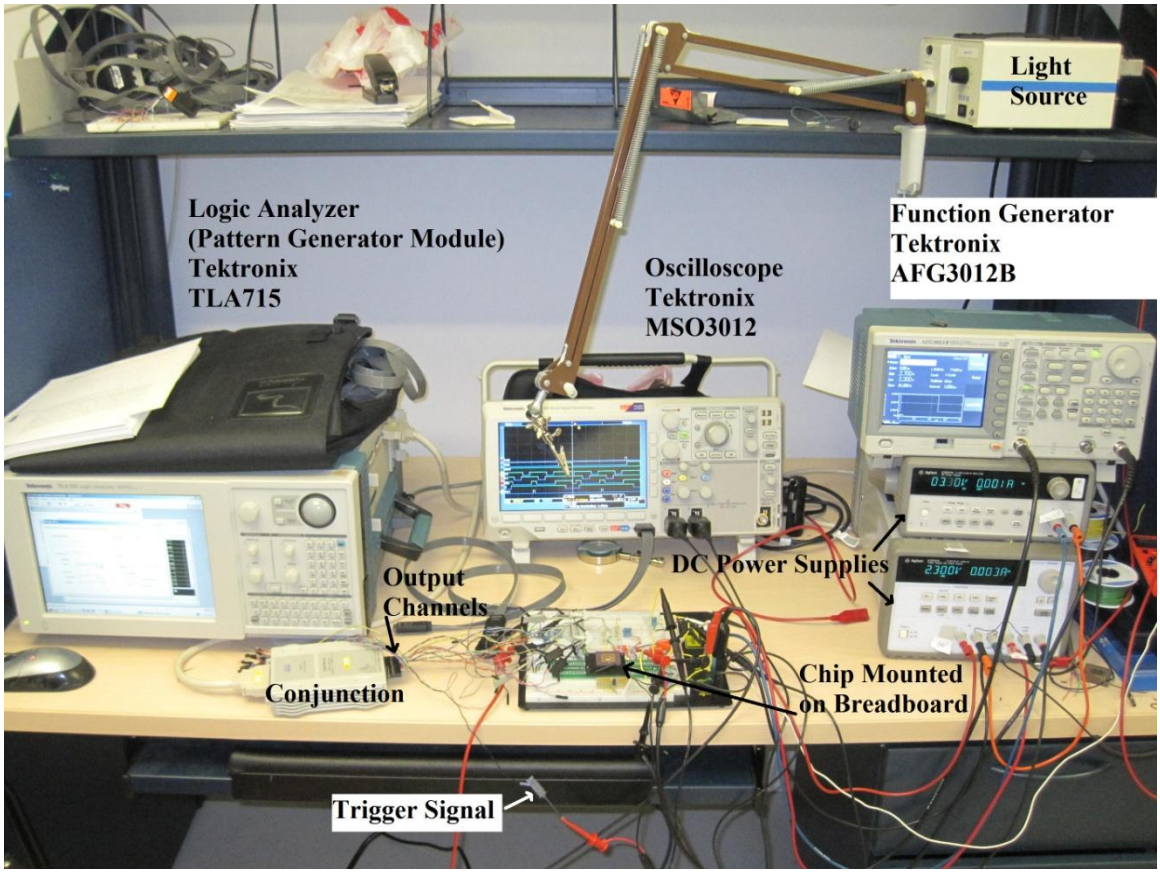


Figure 3. 1 Test bench used to characterise the pixel and the column circuits

Figure 3.1 shows the photo of the test bench used to characterise the pixel and the column circuits. A light source provides an illumination onto the image sensor IC to stimulate photo detectors. The chip mounted on a bread board is connected to power supplies, the pattern generator and the oscilloscope for measurements. A DC power supply of 3.3V is used. The test results show that the expected functionality was achieved for the pixel and the column circuits.

3.2 Pixel Results

The fabricated prototype includes a pixel, a current conveyor, delta reset sampling, a differential operational amplifier and comparator. The pixel consists of a photodiode, a diode connected transistor M_{1p}, transistor M_{2p} operating in the linear region and a row select switch M_{3p} to connect the pixel to the column bus as shown in Figure 2.2. The bias voltage, V_S, determines through transistor M_{1p} the pixel reset and integration phase. Since the output of the pixel is current, it is necessary to have an external circuit, shown in Figure 3.2, in order to display and measure on the oscilloscope. Therefore, the external circuit includes a transimpedance amplifier with a resistor of 1-2 MΩ in the negative feedback to convert the output current into a voltage.

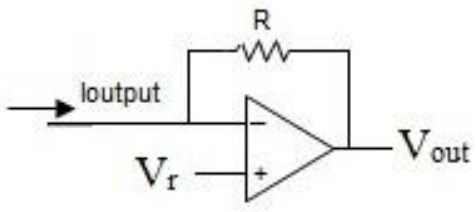


Figure 3. 2 The schematic of the external testing circuit

A large resistor is used in order to detect low currents. The input reference voltage, V_r, is set to a fixed voltage.

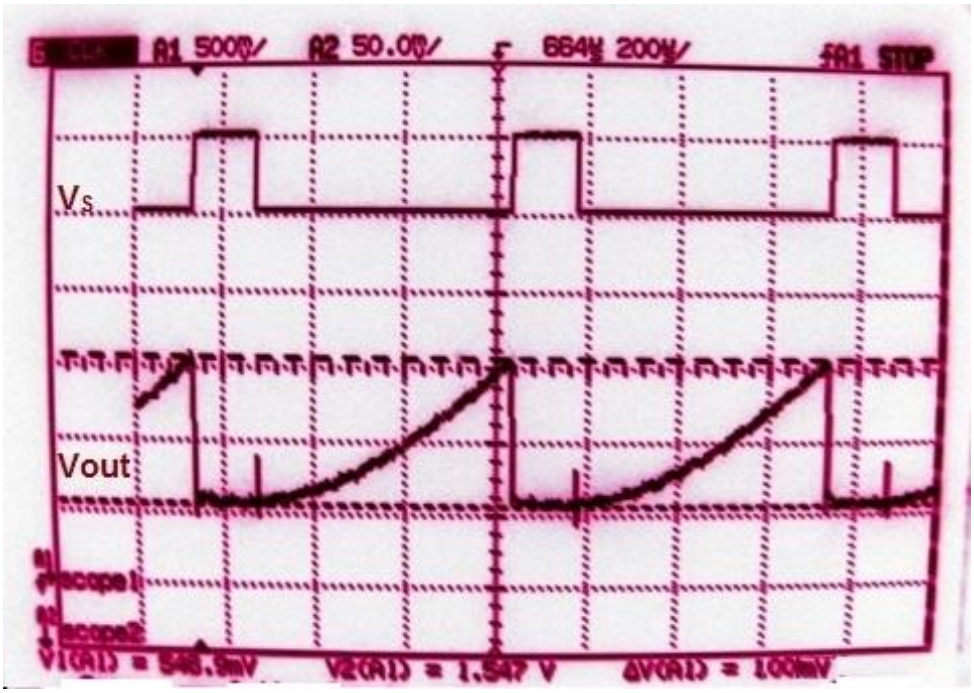
3.2.1 Pixel Output Measurements without DRS

In order to verify the functionality of the pixel, according to the Figures 2.10 a) and 2.12, we keep the switches F_2, F_{o1} and F_{o2} open. Also, the biasing voltage of the transistor M_{21} must be removed. So, it is set to zero. F_1 and F_{o3} are kept closed. The V_{ref} of the current conveyor circuit, Figure 2.8, determines the pixel output voltage. To keep M_{2p} in the linear region, V_{ref} is set to 3.1V. Also, the input voltage of the external transimpedance amplifier is set to 3.1V, the same as V_{ref}, to keep the transistor M_{11} in cut off region. Therefore, the DRS circuit is completely disabled and only the pixel output current is sent to the output. The oscilloscope probe is connected to the output of the transimpedance amplifier, V_{out}.

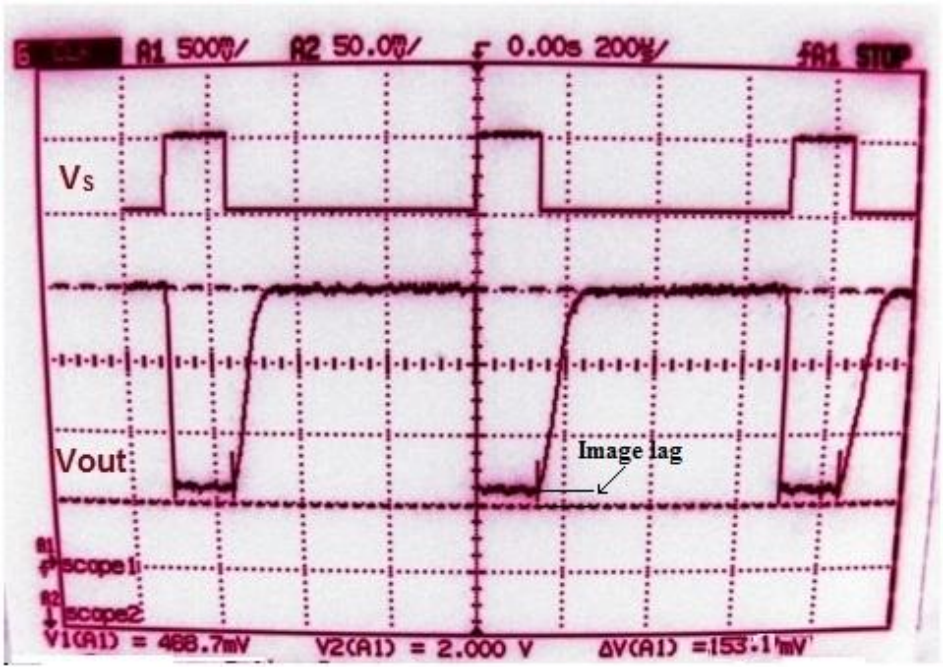
As seen in Figure 3.3, we measure different output levels of the pixel response for different light intensities. Also, at the end of the reset time, the voltage values are not the same for different light levels. According to the Figure 2.2, when the transistor M_{1p} acts as a reset transistor for the pixel, the current passing through, charges the node capacitance of PD. Depending on the photonic current, I_{ph}, hence, light intensities, different reset values of V_{PD} are reached which create different pixel reset output currents. This effect appears as image lag, as seen in Figure 3.3 b) and Figure 3.4, which is increased by increasing the light intensity. Also, as light intensity increases, depending on V_S, the pixel eventually enters into the logarithmic mode and consequently the output current saturates.

Adjusting the high and low levels of V_S, V_{SH} and V_{SL}, depends on the threshold voltage of M_{2p} and at which level of illumination the logarithmic mode is required, respectively. We set V_{SH} so that M_{2p} works in linear mode from the beginning of the integration time. In this case it is set to 2.7V. If V_{SL} is set to zero, the pixel always works in linear region since the diode connected transistor, M_{1p}, is always cut off. So, for high light intensities the pixel saturates while it is in linear region and the current will not change by

increasing the illumination level. Therefore, we adjust V_{SL} to 2.35V in order to have the pixel operating in logarithmic mode for high level of illumination.



a)



b)

Figure 3. 3 Pixel responses for a) low and b) high light intensity

The white light source is a lamp equipped with a detachable filter centered at 525nm with a 50 nm bandwidth. However, the available light source with the filter has insufficient intensity to achieve five order of illumination intensity. Since, the stronger light source with λ=525nm is not available for the experiments, the practicable solution is to remove the filter for the highest light intensities.

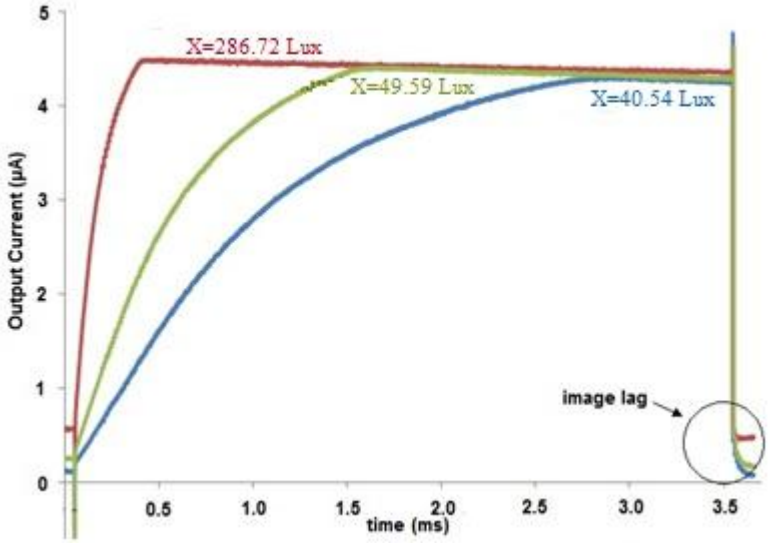


Figure 3. 4 Experimental results of the pixel output currents

Figure 3.4 also shows the response of the pixel with varying light intensities. We measured the power of the light with the wattmeter and then transform it into Lux, the unit of illumination, with the following equation:

$$\frac{P}{S} \times 685(Lumens/Watt) \times 0.862 = X(Lux) \quad , \tag{3.1}$$

where P is the power measured and S is the wattmeter sensor area of $0.5025 \times 10^{-4}\ m^2$. The standard factor of 685 is in Lumens per Watt (LPW), which corresponds to the maximum luminous efficiency of the standard observer. Calculating LPW requires using the simple mathematical formula. The constant value of 0.862 is the photonic factor (V(λ)) which is the wavelength dependant attenuation.

According to the Figure 3.4, as the light intensity increases, the pixel reaches the logarithmic mode of operation (saturated output current) earlier. In the linear operating mode (before saturation) of the pixel, the output is not entirely linear. The non-linearity comes mainly from the hole mobility degradation of transistor M_{2p} as a function of V_{GS} and the ‘’on’’ resistance of the select transistor M_{3p} which exhibits an increasing drain-source voltage drop as the output current increases. A solution for the non-linearity imposed by the transistor M_{3p} ‘on’ resistance has been explained in the previous chapter, using a digital correction method.

3.2.2 Dark Current Measurement

In the absence of light, in dark condition, there is a small current affecting the pixel output called the dark current. It is one of the important parameters that characterizes the performance of an image sensor. Various factors contribute to the dark current. One of them is the current coming from the depletion region of the photodiode touching the oxide layer [21]. The dark current is usually represented as the pixel output function of the integration time.

Figure 3.5 shows the pixel response in dark condition. To measure the dark current, we apply a square wave of the function generator as V_S with the SEL switch “on”. The DRS circuit is disabled by removing V_{bias}, opening F_2, closing F_1 and setting V_r of the external transimpedance amplifier to 3.1 V. Then, we measure the slope of the output curve which is $\Delta V_{out,m}/\Delta t$. In this case, we have $\Delta V_{out,m}$=16.8 mV and Δt=3.93s.

In the simulation of the pixel we consider the circuit shown in Figure 3.6. In order to have, in this circuit, the value of the measured photodiode voltage, $\Delta V_{PD,m}$, in dark condition, we replace the photodiode and the transistor M_{1p}, shown in Figure 2.2, by a voltage source. Then, we sweep the voltage V_{PD} while measuring V_{out}.

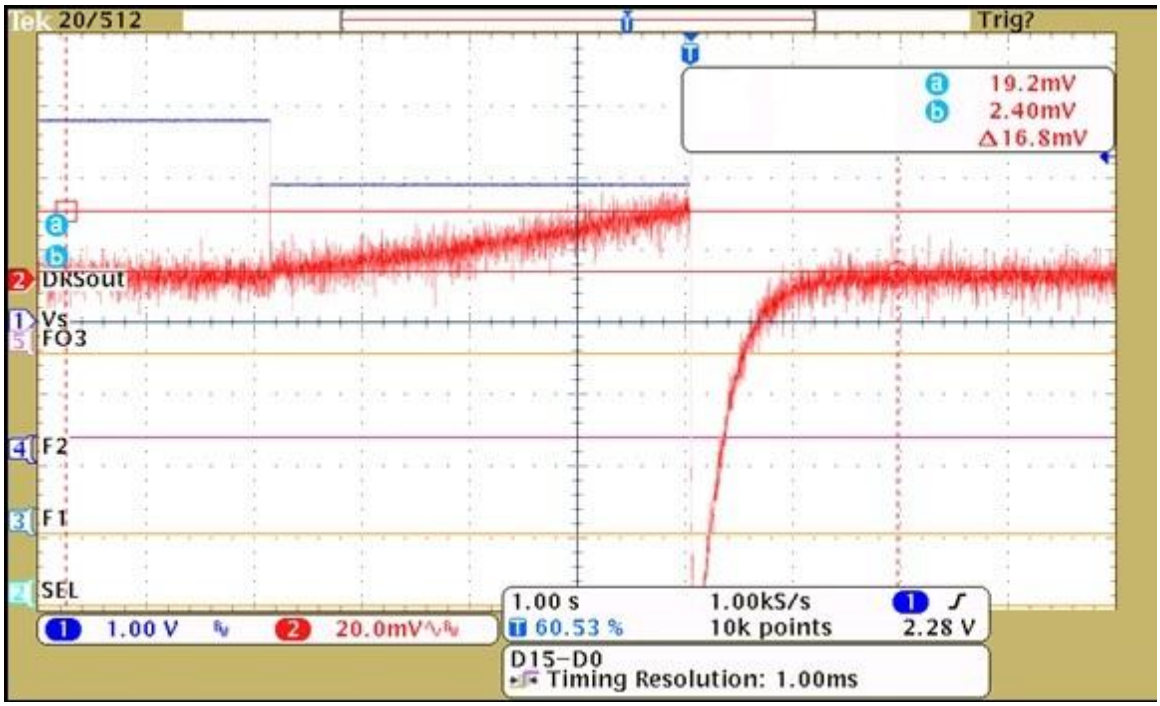


Figure 3. 5 Pixel response in the dark condition

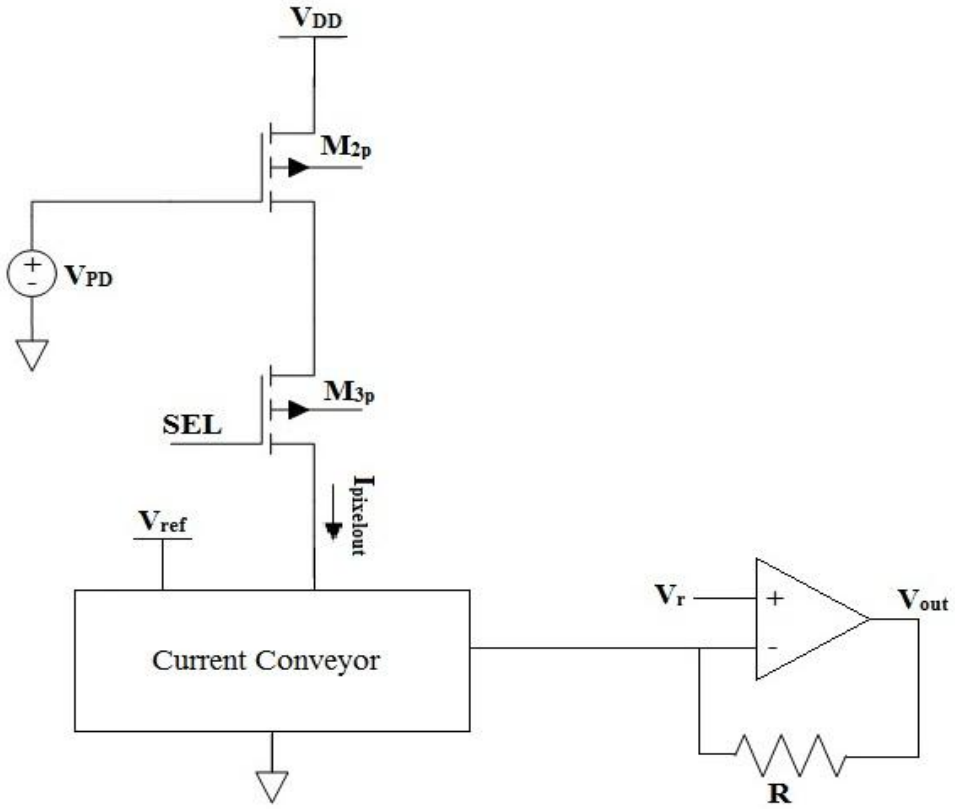


Figure 3. 6 Modified pixel schematic to measure the ratio of $\Delta V_{PD}/\Delta V_{out}$

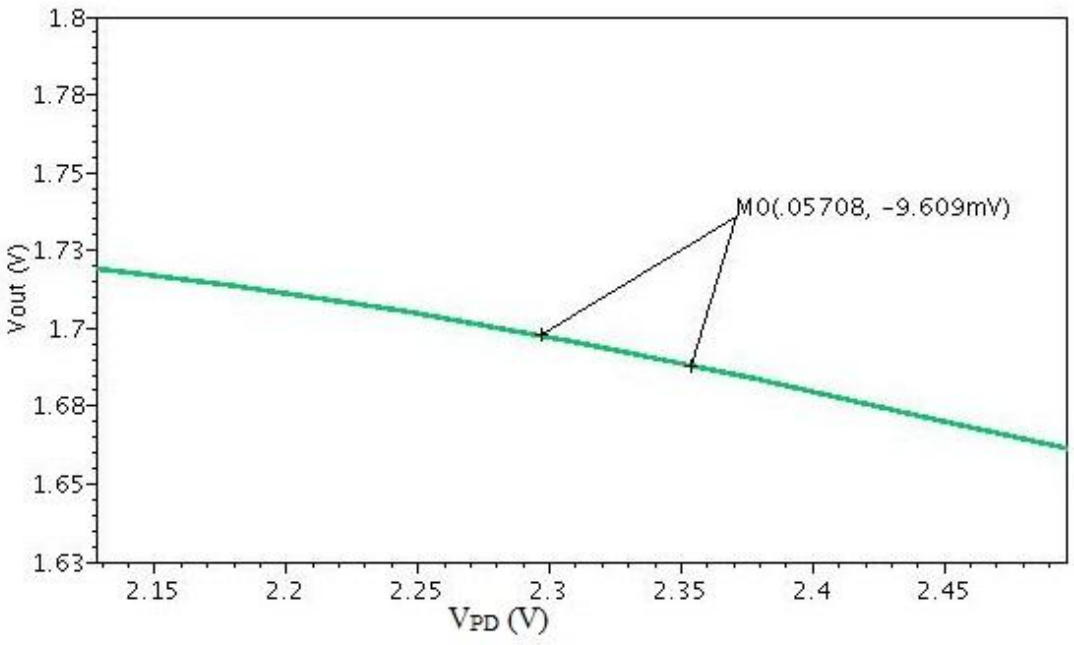


Figure 3. 7 Simulation results of the pixel response

Figure 3.7 shows the simulation result. A slope of $(\Delta V_{PD}/\Delta V_{out})_{measured}$ of 5.94 is measured. From the measurements and the simulation result, we deduce the measured photodiode voltage variation which is determined by the equation below:

$$\Delta V_{PD,m} = \left(\frac{\Delta V_{PD}}{\Delta V_{out}}\right)_{simulated} \Delta V_{out,m} \quad . \tag{3.2}$$

Therefore, we have $\Delta V_{PD,m}$ equal to 99.8 mV.

Now, we measure the capacitance of the “PD” node, according to the DC simulation result of the pixel in the reset mode, we obtained 60.56fF. Consequently, using the following equation, the dark current is deduced;

$$C\Delta V_{PD,m} = I_{dark}\Delta t \quad . \tag{3.3}$$

So, we find I_{dark} = 1.538fA.

3.3 Performance of the DRS Circuit

A delta reset sampling circuit is a current memory cell, capable of memorizing the current. The circuit is a sample/hold cell that samples a current by storing the gate voltage of a MOS transistor according to the current flowing through. It is used in each column to remove the offset voltage variations [60]. The DRS scheme is composed of a coarse and a fine sub memory cells. It is performed in two steps. Initially, the sample current is memorized in the coarse memory cell (M_{11}) during the first step. Then, in the second step, the error signal is memorized in the fine memory cell (M_{22}). During the output phase, the subtraction of these two signals appears at the output. M_{21} is used to reduce the effect of channel length modulation on M_{22}. In this project we use it for two purposes, as explained in the following.

One of the functionality of the DRS circuit is the offset removal circuit. In a simple 3T pixel structure, image lag created by the dependence of the reset photosite voltage on the light intensity affects the image quality. For this purpose, the DRS circuit samples the current at the end of the integration time and subtracts it from the reset value. Therefore, the DRS output current is free of image lag.

Another functionality of the DRS circuit is to sample two successive output currents, $I_{pixelout}$, at the end of the integration time. They are subtracted and the result is transferred to the next stage in order to determine the operating mode of the pixel. Two roughly similar samples indicate that the pixel is in the logarithmic mode. It will be explained in the next sections.

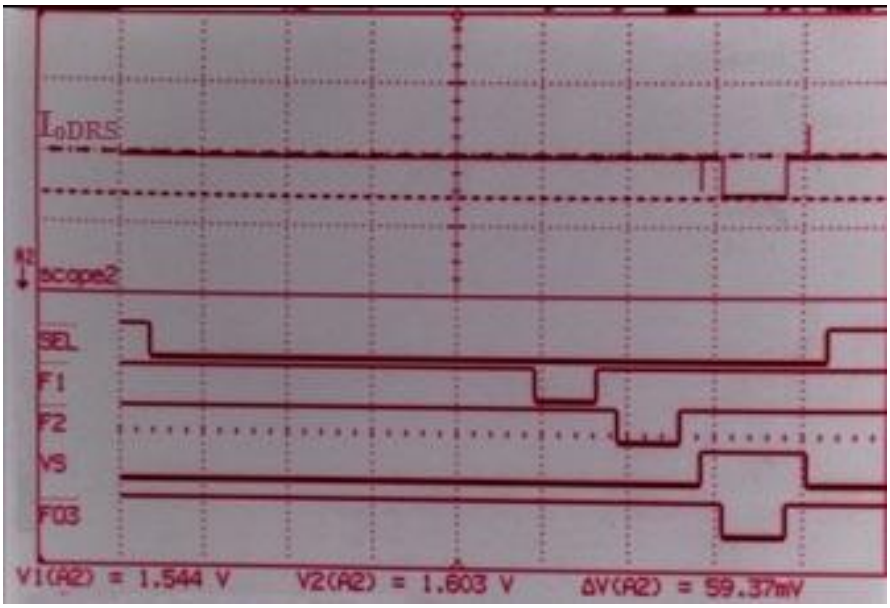
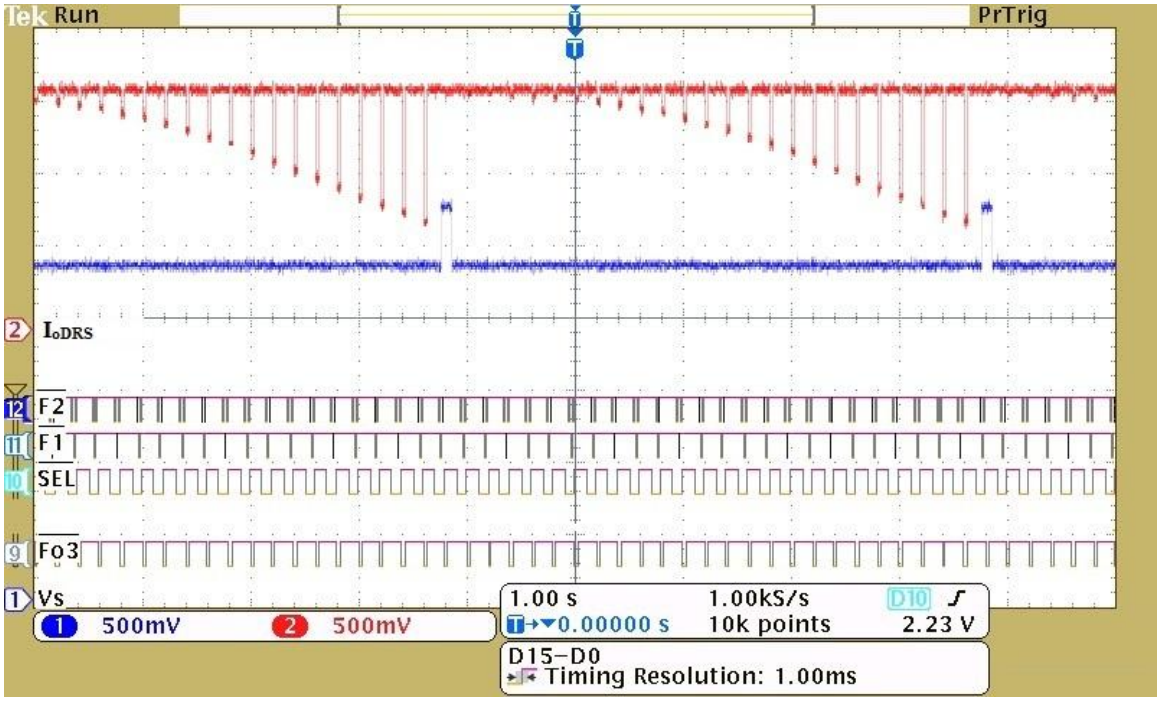


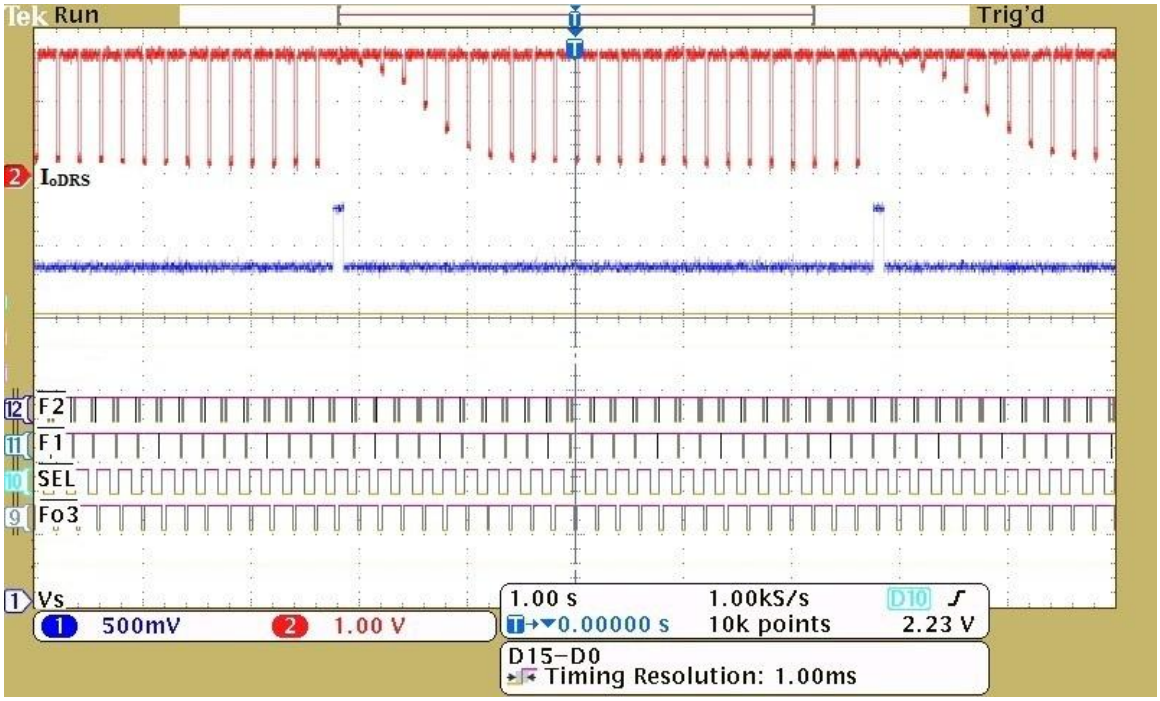
Figure 3. 8 Experimental result of DRS functionality

Figure 3.8 shows the DRS as an offset removal circuit. If the light intensity increases, the current pulse amplitude, I_{oDRS}, increases. The timing diagrams of the control signals and the readout signal are shown. The current sampling is done at the end of the integration time by changing the state of F_1 and F_2. Then the pixel is reset by changing the Vs level from low to high. At this time, F_{o3} is closed and the reset-phase output current is subtracted from the previously memorized uncorrected output current. So, the final output current is independent of charge injection errors and image lag. The DRS input current is controlled by the switch SEL in the pixel. The output current is converting to a voltage by a transimpedance amplifier, as shown in Figure 3.2, in order to be displayed and measured on the oscilloscope.

Figure 3.9 a) and b) shows the pixel output current which sampled by DRS during integration time for linear and linear-logarithmic operating mode, respectively. As seen, for low level of the light intensity, the curve is not linear due mainly to the select transistor “on” resistance and the carrier mobility dependence on the gate voltage. At high illumination, the pixel output current reaches saturation when the logarithmic mode is in effect.



a)



b)

Figure 3. 9 Sampled DRS output during integration for a) linear b) linear-logarithmic operating mode

3.3.1 Pixel Output Measurements with DRS

In order to include the delta reset sampling circuit in the response measurement, the switches F_1, F_2 and F_{o3} are activated. Also, according to the schematic in the Figure 2.10a), the biasing voltage of the NMOS transistor in the fine branch, M_{21}, is set to 2V. Therefore, we have the pixel response in the presence of the DRS and the output current is offset free.

A light source is used to illuminate the pixel. In order to measure the power of the light intensity, the light source is driven from a DC voltage source. The power value of the light intensity is measured for regular increment of the driving voltage. In this case, the maximum value of the voltage source for the light is 5V. For each luminance power value, we measure the pixel output current.

Table 3.1 shows the pixel output current, in the linear-logarithmic mode of operation as a function of the luminance power. Since the light intensity changes along the spectrum, we used a green light filter to pass only the wavelengths in the green light range. Therefore, spectral content of the light beam is constant. However, in order to obtain more light intensity, the filter is removed for the two most intense illumination levels. In order to detect a wide range of light intensities, we enable the logarithmic mode of operation by adjusting the low level of Vs. It is set to a value so that the pixel can detect high level light intensities, as mentioned in the section 3.2.1. Increasing the low level of Vs, enable the pixel to enter sooner in the logarithmic mode operation. For the results of Table 3.1, we set the low level of Vs to 2.35V while the high level of Vs, for the reset phase, is set to 2.7V. Also, the integration time is set to 133 ms in order to that the pixel be able to detect the lowest level of illumination.

Table 3. 1 Pixel output current versus the variation of the light power

	Voltage Source (V)	Light Power (mW)	Pixel Output Current (μA) for t_{int}=133 (ms)
With the filter to pass only the green light (λ=525 (nm))	0.268	0.005	0.077
	0.331	0.0123	0.317
	0.340	0.0132	0.395
	0.350	0.0148	0.581
	0.360	0.0163	0.666
	0.367	0.0175	0.706
	0.375	0.0189	0.796
	0.380	0.0198	0.891
	0.390	0.0217	0.941
	0.400	0.0239	0.951
	0.406	0.0252	0.961
	0.459	0.040	1.031
	0.565	0.080	1.071
	0.699	0.160	1.106
	0.871	0.320	1.131
	0.800	0.358	1.141
	0.950	0.424	1.151
	1.010	0.513	1.166
	1.091	0.640	1.181
	1.360	1.28	1.186
	1.702	2.56	1.196
	2.120	5.12	1.216
	2.650	10.24	1.226
	3.333	20.48	1.246
	4.311	40.96	1.251
	5.000	62.3	1.271
Without the filter for high light intensities	2.510	122.15	1.281
	3.510	294.41	1.291
	5.000	445.66	1.296

The integration time, t_{int}, is fixed so that the pixel can detect low-light intensity. It should be noted that, it is impossible to measure the dark current of the pixel in the presence of the delta reset sampling circuit. The reason is the effect of feed-through coming from the output switch, F_{o3}. Figure 3.10 shows the offset as a result of the feed-through.

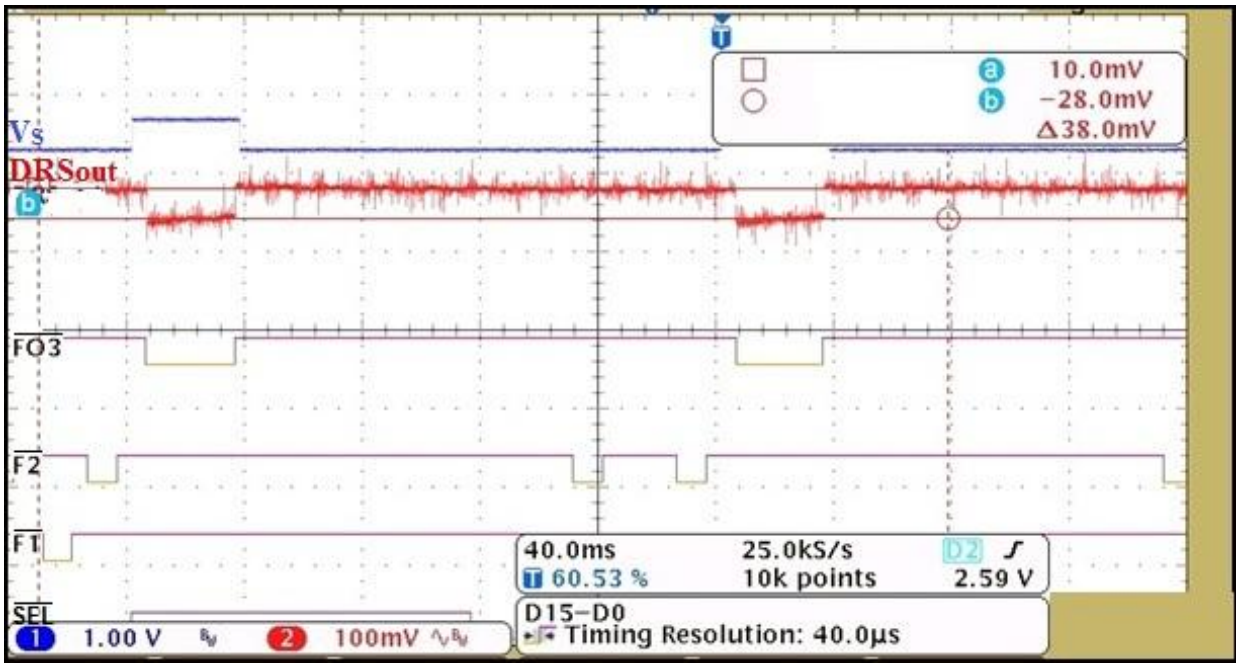


Figure 3. 10 Offset output current

As shown on Figure 3.10, a 38 mV offset voltage due to feed-through, should be divided into the resistance in the feedback of the external transimpedance amplifier, 2MΩ, to obtain the output current. As a result, it is 19 nA as an offset of the output current created by the F_{o3}. We remove this offset value from every measured output currents of the pixel, as calculated in Table 3.1.

Figure 3.11 shows the pixel output current as a function of the power light intensity per photosensitive area. As seen, the output current variation is reduced when the pixel enters into the logarithmic mode of operation, around 255 lux for V_{SL}=2.35 V. The light intensity varies over five orders of magnitude. Therefore, the pixel dynamic range is about 100dB.

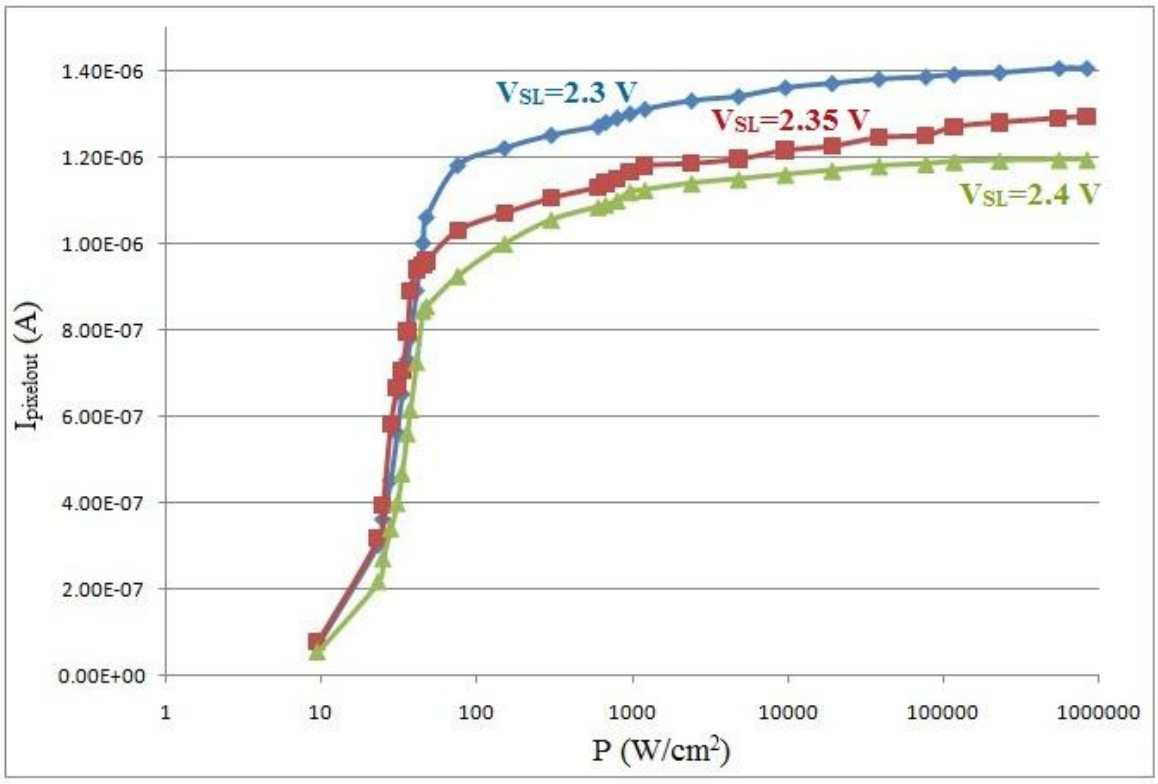


Figure 3. 11 Pixel output current as a function of light intensity for different V_{SL}

In addition to the curve obtained from the values in Table 3.1, two other curves are shown in Figure 3.11 in which the values are measured for V_{SL}=2.3 V and V_{SL}=2.4 V, in order to see the V_{SL} effect on the pixel operating mode. As shown, the pixel enters to the logarithmic mode of operation later for the smaller V_{SL}. Therefore, the portion of the linear region in pixel operation is greater and also the maximum current reached is larger.

Applying the equation (2.8) into the pixel output current of the Figure 3.11, we obtain the Figure 3.12. The $R_{on\text{-}M3}$ in this equation is 17.3kΩ, which is obtained in simulation results from transistor parameters. The linearization transfer is done with a residue of 0.9981 for the linearized function, and is shown only for the linear part of the pixel response. The residue shows that other causes of non-linearity are in effect, as explained in chapter 2.

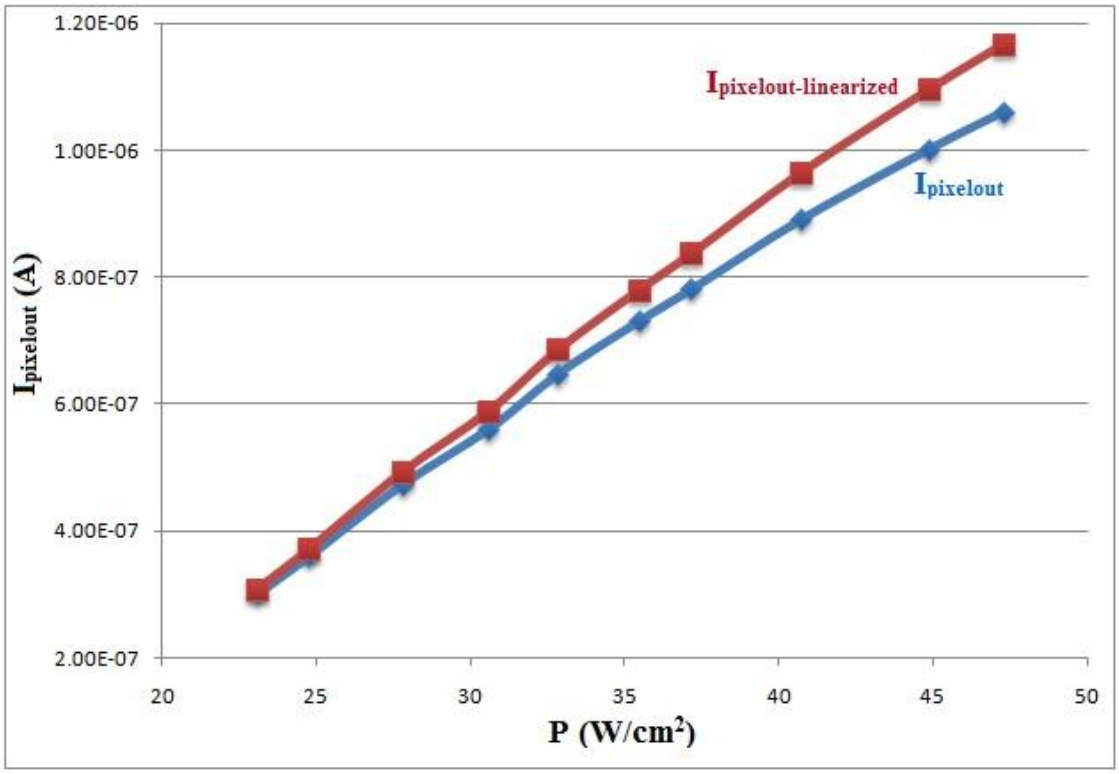


Figure 3. 12 Linearized pixel output current

3.4 The Mode Indicator Column Circuits

3.4.1 Integrator

It is made of one stage fully differential amplifier with common mode feedback. The design and functionality of the circuit were explained in Chapter 2. As shown in Figure 2.13, the integrator is connected to the DRS circuit using the switches F_{o1} and F_{o2} in order to memorize two sampled current of I_{oDRS}. The two outputs of the integrator, O_1 and O_2 resulting from the integration of I_{oDRS}, feed the comparator (CMP). They determine the output of the CMP which is the pixel mode indicator (MI). Experimental results will be shown in the following section in the presence of the comparator circuit.

3.4.2 Dynamic Comparator

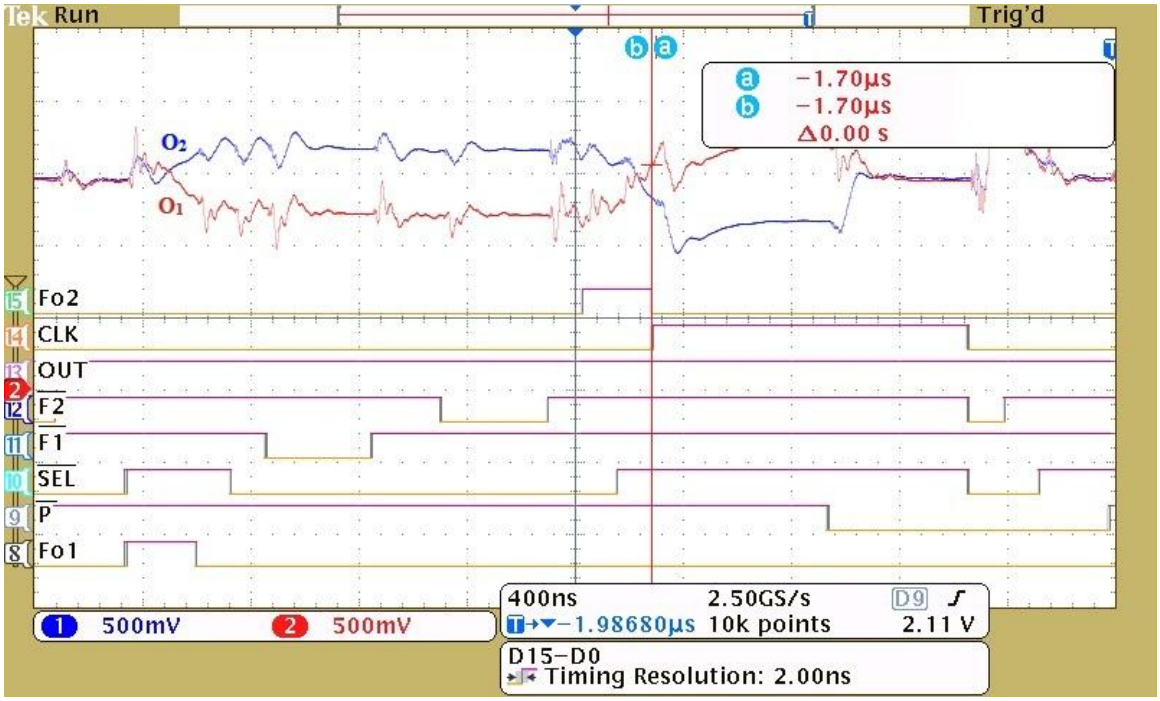
In this state, we will measure the comparator output in order to determine the pixel mode response. We use the Pattern Generator to create the synchronization clocks for the switches. We set the maximum voltage of these synchronizations to 3.3V and the minimum to zero. To generate the V_S signal, a function generator is used in burst mode and it is synchronized with the pattern generator. The adjusted parameters of the function generator are listed in the Table 3.2.

Table 3. 2 Function generator parameters to create V_S

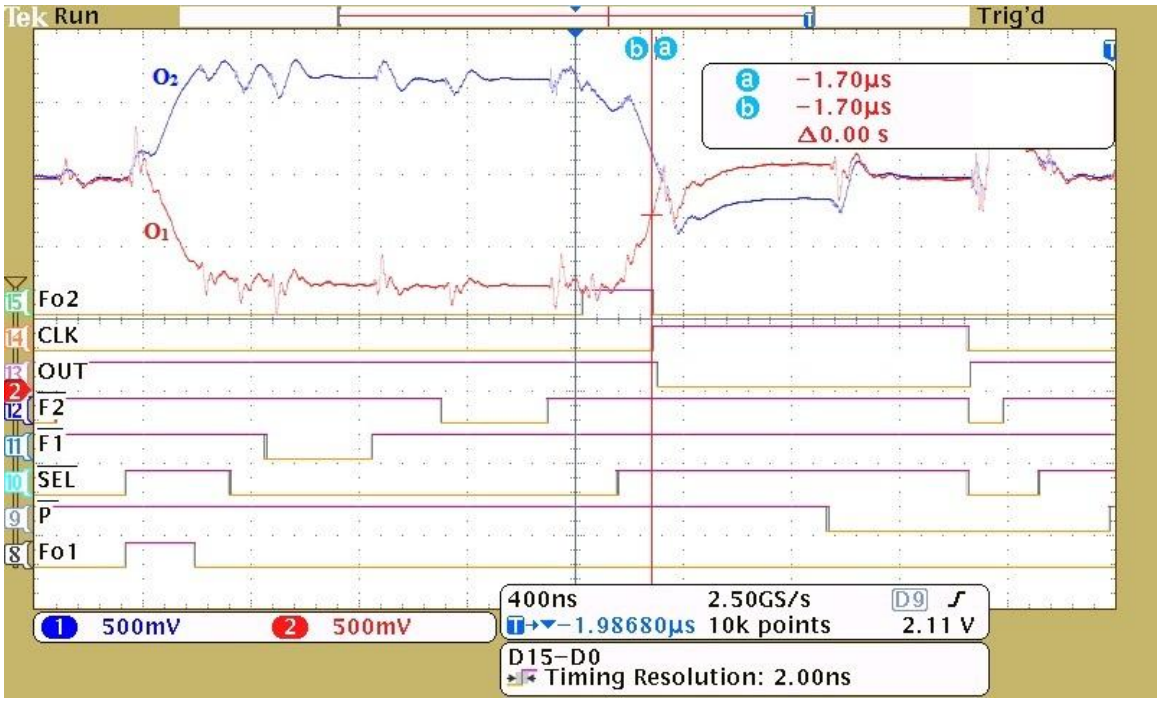
Run mode ⟶	Burst
Function ⟶	Pulse
Clock ⟶	External

Figure 3.13 a) and b) show the timing diagrams and the differential integrator outputs, O_1 and O_2, and the comparator output, OUT. The comparator has two outputs that changes according to Figure 2.15. If the current in the left branch is more than the current in the right branch, out_1 decreases faster than out_2. When out_1 is less than the threshold voltage of M_{N15}, M_{N15} is turned off. At the end of the regeneration time, out_2 increases to V_{DD} while out_1 decreases to zero.

In Figure 3.13 a), since the light intensity is low, the pixel works in linear mode. Therefore, after DRS, the first sampled current is smaller than the second one. According to the equation (2.14), when I_1 is smaller than I_2, for a given time, the voltage variation of ΔV_2 is larger than ΔV_1. So, at the end of a sampling period, when the CLK signal turns high, O_1 is larger than O_2. At the end of the regeneration phase, the comparator output (OUT in Figure 3.13), is "1" considering the comparator output, out_2, which increases to V_{DD} in this condition.



a)



b)

Figure 3. 13 Experimental results obtained from the integrator and the dynamic comparator for a) the linear and b) the logarithmic mode of the pixel response

Figure 3.13 b) shows the results in high light level in which the pixel operates in logarithmic mode. Therefore, when the CLK signal is high, during the regeneration phase of the comparator, M_{N14} is turned off and the comparator output turns to "0" since O_1 is smaller than O_2.

3.5 Results Comparison

The results of the proposed pixel and the existed CMOS APS pixels are compared in Table 3. 3.

Table 3. 3 Pixel performance comparison

Reference	Pixel operating Mode	Pixel response	CMOS Technology	Pixel type and Architecture	Dynamic Range (intrascene)
[14]	Voltage-Mode	Linear-Logarithmic	0.35 µm 2P4M, 3.3V	5Tr - APS	112 dB
[29]		Logarithmic	0.35 µm 1P5M, 3.3V	5Tr with comparator-A PS	137 dB with variable integration time
[30]		Logarithmic	0.25 µm	4Tr - APS	137 dB
[31]		Logarithmic	0.25 µm	5Tr combining the lateral PNP - APS	120 dB
[32]		Logarithmic	0.5 µm	5T - APS	120 dB
[61]		Linear	0.18 µm 2P3M	6 Tr- APS	94 dB with two exposure
[10]	Current-Mode	Linear	0.35 µm 2P4M, 3.3V	3Tr - APS	64 dB
[33]		Linear	0.25 µm ,2.5 V	1.5Tr - APS	63 dB
				3Tr - APS	58.3 dB
This work		Linear-Logarithmic	0.35 µm 2P4M, 3.3V	3Tr - APS	100dB

In this work, the pixel circuit uses a linear-logarithmic response to provide a high dynamic range in current-mode operation from a simple 3T APS architecture. As shown in Table 3. 3, the voltage-mode APS presents a higher the dynamic range, at the expense of a more complex architecture, taking up a larger area. It is seen that in current-mode APS, the dynamic ranges are low since the simple pixel architecture is working only in the linear region. Compared to the other pixels of Table 3. 3, the proposed pixel works in current-mode and shows a fairly high dynamic range due to the combined linear-logarithmic pixel response.

3.6 Conclusion

Test of the prototype has demonstrated the functionality of the circuit described in Chapter 2. The current mode combined linear-logarithmic response pixel provides a high dynamic range of 100dB. In order to determine the operating mode of the pixel, a fully differential amplifier acting as an integrator and a dynamic comparator circuit is used. The purpose of the common mode feedback used of the integrator is to keep the output average of O_1 and O_2, $(O_1+O_2)/2$, to V_{CM}. The comparator mode indicator flag indicates to the digital processing unit when the pixel is operating in the logarithmic mode so the ADC digital output is converted accordingly.

CONCLUSION AND FUTURE WORK

As the imaging market continues to expand with new emerging applications, CMOS image systems have become a major research topic because it allows a high level of integration of on- chip logic, memory and signal processing functionalities. One of the major challenge facing CMOS image sensors is the limitation of the dynamic range, as CMOS scaling process advanced and the supply voltage decreases. To increase the dynamic range, some solutions and methods have been proposed in standard image sensors. However, most of them result in an increased pixel area or integration time at the expense of reduced resolution, sensitivity and frame rate. Contributions of this thesis have been made to develop a methodology to design a CMOS image sensor with high dynamic range capability. In addition, we have also designed circuit blocks needed for extracting and interpreting the analog signal produces by the pixel. A prototype chip was fabricated using the 0.35 μm AMS CMOS processing technology.

The design of this CMOS image sensor includes many analog circuit blocks such as the current conveyor, the current memory cell, the fully differential integrator and the comparator. Based on our analyses, we have proposed some new idea to improve the circuits.

In this dissertation several new ideas/contributions have been proposed:

- A current-mode pixel is proposed which alleviate the drawbacks of small CMOS technologies by improving the dynamic range.
- A 3T linear-logarithmic pixel is proposed to achieve a high dynamic range in order to distinguish from low contrast signal to high background illumination. In this architecture, the diode connected transistor is also used as the reset transistor by varying its source voltage. Therefore, the pixel area is reduced compare to the architecture using four transistors per pixel.
- The proposed image architecture has pixel operating mode detection capability. The circuits introduced in column level, determines that the pixel works in linear

or logarithmic mode. For this purpose, we used a differential operational amplifier with a dynamic comparator.

- A digital linearization method is used. One of the non-linearity effects comes from the 'on' resistance of the select transistor in the pixel. This non-linearity is removed by a simple analytical solution using the output current as feedback.
- An Improved current memory precision is used to remove the offset and image lag as well as to sample two successive current in order to determine the pixel mode operation. Using a cascode architecture reduces the channel length modulation and consequently increases the accuracy of the copied current.

We have also presented a literature review of various CMOS image sensors and introduced the principles of operations in Chapter 1. Based on this introduction, Chapter 2 explained the overall architecture adopted for the image sensor. More specifically, a new 3T architecture active pixel designed has the advantages of both current-mode and linear-logarithmic architectures. The dynamic range obtained is over five order of magnitude of illumination. The current conveyor circuit is used in order to fix the column voltage as well as to copy the pixel output current. The performance of our image sensor is depended on the accuracy of the current memory cell. We have chosen a fully differential amplifier with a dynamic comparator to determine in which mode the pixel works. The result is sent to digital processing unit so that ADC digital output is converted accordingly.

In Chapter 3 we presented the experimental results obtained from the fabricated prototype. It is measured on a single active pixel sensor with a light sensitive area of $53.28\mu m^2$. First, we deactivated the DRS to characterize the pixel. The image lag effect was observed. We also determined the dark current of the pixel by measuring the pixel output in the absence of light. Then, we activate the DRS and measured the pixel output current sampled by this circuit with offset removal. Finally, two successive current sampled by DRS sent to the comparator and its output indicated the pixel operating mode.

Our work focused on the design of a high dynamic range pixel and circuit blocks compatible for this architecture. Future work should be conducted in the following areas:

- We have designed a single active pixel and its reading circuit used in the current-mode linear-logarithmic CMOS image sensors. It will be necessary to complete the design of the full array.
- The performance of the switching must be improved. One may need to experiment with more effective techniques to reduce the feed-through effect to improve the performance of these critical circuits so as to improve the overall system performance.
- The pixel output current dynamic range should be improved. Possible future exploration includes the improvement of the performance and resolution of the DRS circuit and switches at the column level.

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APPENDIX

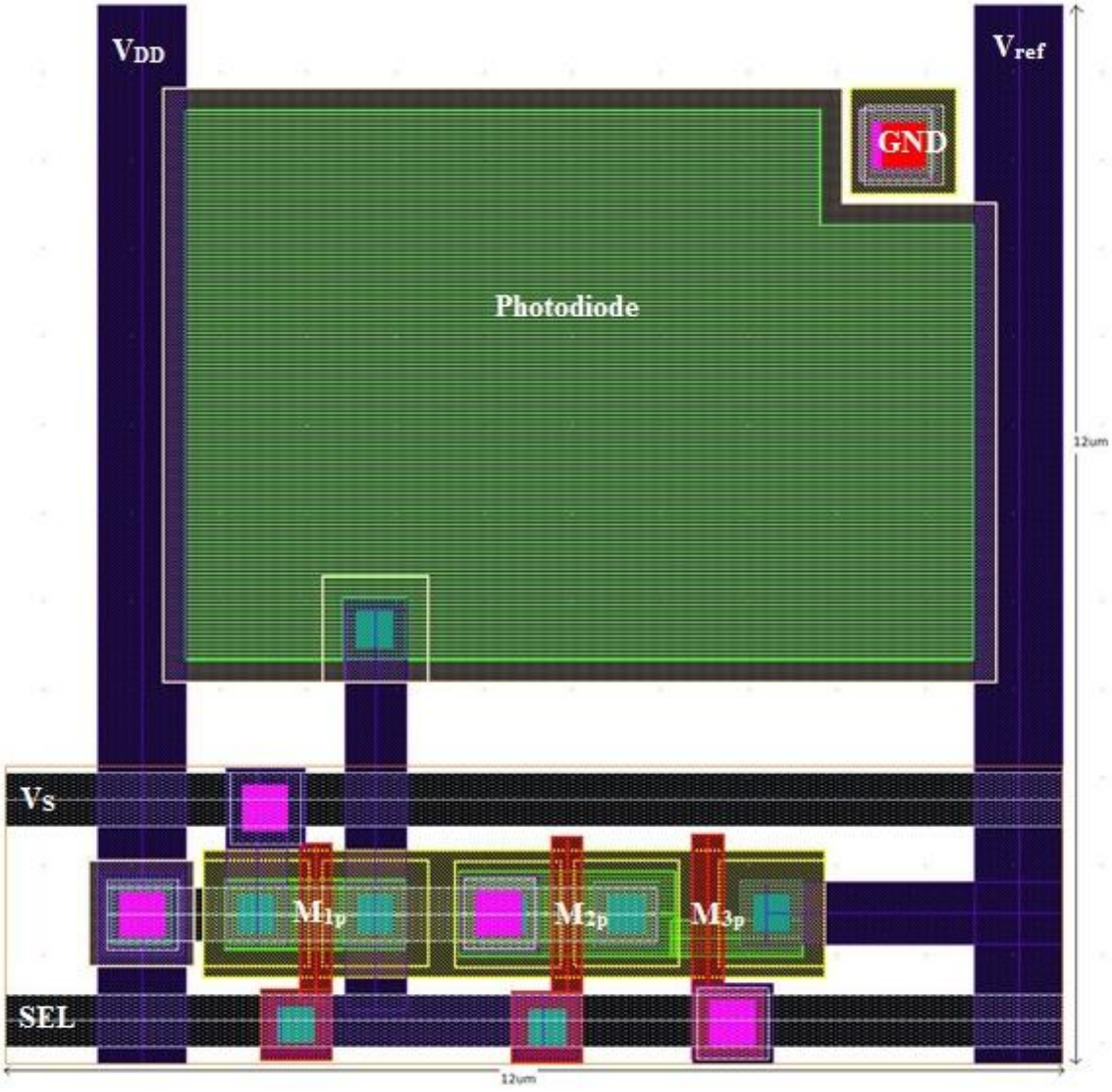

Figure 1.A Layout view of the pixel architecture

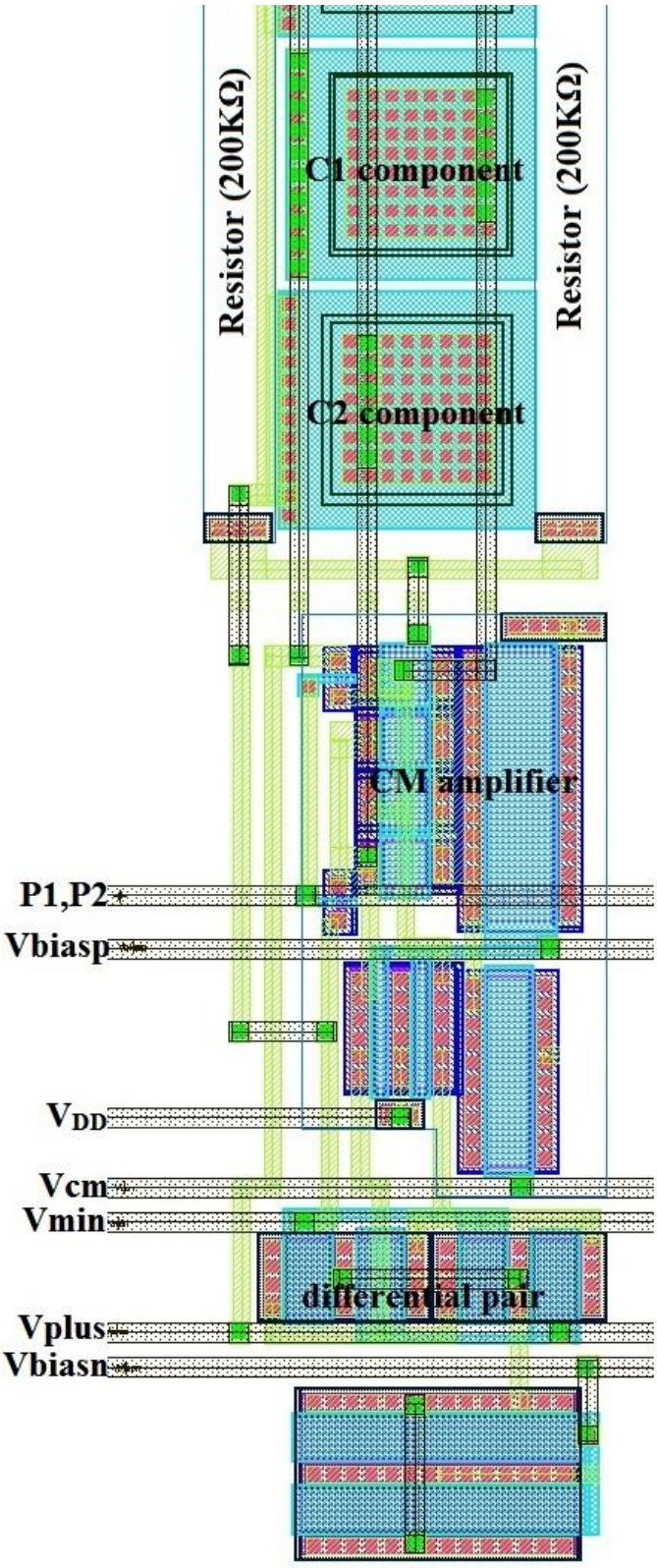

Figure 2.A Layout view of the integrator block