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POLYTECHNIQUE MONTRÉAL

affiliée à l'Université de Montréal

Implementing a reliable and ultra-low power adaptive RF energy harvester for IoT applications

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Département de génie électrique

Thèse présentée en vue de l'obtention du diplôme de Philosophiæ Doctor

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Cette thèse intitulée:

Implementing a reliable and ultra-low power adaptive RF energy harvester for IoT applications

présentée par **Akram Mohamed Ahmed Araby REFAEI**

en vue de l'obtention du diplôme de Philosophiæ Doctor

a été dûment acceptée par le jury d'examen constitué de:

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DEDICATION

To my beloved parents,

To my lovely two sisters

To my best friend, Diya…

ACKNOWLEDGEMENTS

First, I would like to express my sincere gratitude to my supervisors, Professor Yvon Savaria, and Professor Yves Audet for giving me the opportunity to pursue my Ph.D. degree under their supervision. I am thankful for their time, support, and guidance throughout my Ph.D. years.

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I would like to thank my colleagues in the research group for saving no time or effort in assisting me throughout my research tasks.

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RÉSUMÉ

La demande de systèmes de récolte d'énergie efficaces et performants pour alimenter les dispositifs intelligents portables modernes est en constante augmentation. Différentes sources d'énergie peuvent être exploitées, telles que les sources thermiques, vibratoires et les radiofréquences (RF) ambiantes. Les récupérateurs d'énergie radiofréquence (RFEH) sont couramment utilisés car ils fournissent une alimentation sans fil. Cette thèse explore de nouvelles méthodes pour concevoir des systèmes de récupération d'énergie radiofréquence à la fois sensibles et à haute efficacité avec une unité de gestion de l'alimentation adaptative. La première méthode proposée consiste à incorporer la différence de phase entre les chemins d'entrée et à la convertir en tension continue. Un redresseur triphasé est choisi et étudié à la fois théoriquement et expérimentalement pour valider ce concept. Le redresseur est combiné à un déphaseur conçu sur mesure qui divise uniformément la puissance reçue, fournissant trois signaux avec un déphasage de 120° simultanément. Des diodes Schottky (SMS7621-005LF de Skyworks) sont sélectionnées pour le redresseur en raison de leur faible chute de tension directe. Un prototype a été construit sur un substrat de laminés RT/Duroid® 5880 d'une épaisseur de 0,005 pouces pour minimiser les pertes diélectriques. Le récupérateur d'énergie RF fonctionne bien dans la bande ISM à une fréquence de 435,6 MHz. Avec une puissance RF disponible de 8 dBm, le prototype atteint une efficacité impressionnante de 56% avec une charge de 6 kΩ et une tension de sortie de 5,2 V. De plus, le système maintient une efficacité supérieure à 20% sur une large gamme de puissances d'entrée disponibles (IPR) couvrant une plage de 28 dBm. Le RFEH démontre également une sensibilité de -10 dBm qui lui permet de produire une tension de 1V.

La deuxième méthode proposée met en œuvre un redresseur en échelle, introduit pour la première fois dans les RFEH, qui intègre un varactor pour réduire la capacitance d'entrée à de faibles niveaux de puissance. Fabriqué avec la technologie GF FDX 22 nm, le RFEH fonctionne dans la bande GSM à 990 MHz. Le redresseur à deux étages, occupe une surface effective (hors pads) de 0,002 mm². La puce est soudée par fil à un boîtier CQFP44, et le PCB est fabriqué à partir d'un substrat laminé RT/Duroid® 5880 d'une épaisseur de 0,005 pouces pour minimiser les pertes diélectriques. Le prototype montre une sensibilité remarquable, atteignant 1 V à -22,5 dBm. Il affiche également

un rendement maximal de conversion de puissance (PCE) de 26% à -13 dBm avec une charge de 50 kΩ, ce qui le rend adapté aux dispositifs ultra-basses puissances.

Pour intégrer les avantages de ces nouveaux redresseurs, une unité de gestion de l'alimentation adaptative est conçue et optimisée. Elle utilise deux chemins pour chaque type, et en fonction du redresseur qui présente la tension de sortie la plus élevée, un circuit de reconfiguration sélectionne cette sortie pour l'unité de gestion de l'alimentation (PMU). Dans le cas où le RFEH est connecté à un système sur puce (SoC) nécessitant une tension fixe et une réserve d'énergie stable, un système de gestion de l'alimentation est conçu avec une protection contre les sous-tensions (UVLO) et un convertisseur buck-boost capacitif pour garantir que la tension à la charge est fixe et stable. En général, le système est idéal pour alimenter des dispositifs ultra-basses puissances dédiés à l'internet des objets (IoT).

ABSTRACT

The demand for efficient and high-performance energy harvesting systems is increasing to power modern wearable smart devices. Various energy sources can be harnessed, including thermal, vibrational, and ambient Radiofrequency (RF). RF energy harvesters (RFEH) are commonly used because they provide wireless power delivery. This thesis investigates new ways of designing both sensitive and high-efficiency radio frequency energy harvesting systems with adaptive power management units. The first proposed method is to incorporate the phase difference between the input paths and convert this to a DC voltage. A three-phase rectifier is chosen and investigated theoretically and experimentally to have a proof of concept for this idea. The rectifier is combined with a custom-designed phase shifter that evenly splits the received power, simultaneously delivering three signals with a 120° phase shift. Schottky diodes (SMS7621-005LF from Skyworks) are selected for the rectifier due to their low forward voltage drop and high sensitivity. A prototype was built on an RT/Duroid® 5880 Laminates substrate with a thickness of 0.005 inches to minimize dielectric losses. The RF energy harvester performs well in the ISM band at a frequency of 435.6 MHz. At 8 dBm of available RF power, the prototype achieves an impressive end-to-end efficiency of 56% with a 6 kΩ load and an output voltage of 5.2 V. Moreover, the system maintains an efficiency above 20% across a wide input power range (IPR) of 28 dBm. The RFEH also demonstrates a sensitivity of 1 V at -10 dBm.

The second proposed way features a ladder rectifier, introduced in RFEHs, which includes a varactor to reduce the input capacitance at low power levels. Fabricated using the GF FDX 22 nm technology, the RFEH operates in the GSM band at 990 MHz. The rectifier, having two stages, occupies an effective area (excluding pads) of 0.002 mm². The chip is wire-bonded to a CQFP44 package, and the PCB is constructed using an RT/Duroid® 5880 Laminates substrate with a thickness of 0.005 inches to minimize dielectric losses. The prototype demonstrates a remarkable sensitivity of -22.5 dBm, while producing a 1 V output. It also shows a peak power conversion efficiency (PCE) of 26% at -13 dBm with a 50 kΩ load, making it well-suited for ultra-low-power devices.

To incorporate both benefits of these new rectifiers, an adaptive power management unit is designed and optimized to combine the performance of these two rectifiers. It uses the two rectifiers at the input from each type. Based on the one with a higher output voltage, a reconfiguration circuit sets its output to the power management unit (PMU). In case the RFEH is connected to a System-on-Chip (SoC) that requires a fixed voltage and a stable energy reservoir, the power management system is designed with an Undervoltage lockout (UVLO) and a capacitive buck-boost converter to make sure that the voltage at the load is fixed and stable. The system is ideal for powering ultra-low-power devices of the Internet of Things (IoTs).

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LIST OF SYMBOLS AND ABBREVIATIONS

RFEH	Radio Frequency Energy Harvester
WPH	Wireless power harvesting
PCE	Power conversion efficiency
WSNs	Wireless sensor networks
IoT	Internet of Things
Γ	Reflection Coefficient
FSPL	Free space path loss
EMF	Electromagnetic field
WPT	Wireless power transfer
IMN	Impedance matching network
MPT	Microwave power transmission
UHF	Ultrahigh frequency
TUF	The transformer utilization factor
Q	Quality factor
PMA	Power Matters Alliance
PTU	Power Transmitter Unit
ULPD	Ultra-low-power diodes
CCD	Cross-coupled differential rectifiers
FCC	Federal Communications Commission
TSV	Through Silicon Via
SBD	Schottky Barrier Diode
IFA	Inverted-F antenna
HFSS	High-Frequency Structure Simulator
AiP	Antenna-in-Package
AoC	Antenna-on-chip

CHAPTER 1 INTRODUCTION

1.1 Motivation

IoT systems are becoming popular in the modern lifestyle. To power these chips, the system should have a replaceable battery or an energy harvester system to keep them working. There are different types of energy harvesters, such as solar, thermal, vibrational, and radio frequency energy harvesters, as shown in Table 1.1. This project focuses on developing a sensitive radio frequency energy harvester that can harvest the ambient signals and convert them to DC power with high conversion efficiency. However, conventional radio frequency energy harvester (RFEH) suffers from high current leakage and low sensitivity [1], [2], [3]. This leads to unpractical RFEHs with low power conversion efficiency and big losses. In addition, these systems are usually incompatible with different types of harvesters, such as thermal and vibrational, since they do not generate a highly boosted voltage to power different circuits [4].

To tackle these drawbacks, the author proposes a reliable and ultra-low-power energy harvester that addresses the low efficiency and sensitivity issues. Moreover, the design generates a good boosting ratio to fully integrated with other on-chip systems, such as control systems or other harvesters. The design has a small area as well, which makes it a reliable and inexpensive option for the industry.

Table 1.1: Different types of energy harvesters [2]

	Solar Energy[20]-[23]	Thermal Energy[25]	Ambient RF Energy[18][35]	Piezoelectric Energy	
				Vibration[27][28]	Push Button[29]
Power Density	100 mW/cm^2	60 µW/cm^2	0.0002 ~ 1 µW/cm^2	200 µW/cm^3	50 µJ/N
Output	0.5 V (single Si cell) 1.0 V (single a-Si cell)	-	3 ~ 4 V (Open circuit)	10 ~ 25 V	100 ~ 10000 V
Available Time	Day time (4 ~ 8 Hrs)	Continuous	Continuous	Activity dependent	Activity dependent
Weight	5 ~ 10 g	10 ~ 20 g	2 ~ 3 g	2 ~ 10 g	1 ~ 2 g
Pros	▪ Large amount of energy ▪ Well developed tech.	▪ Always available	▪ Antenna can be integrated onto frame ▪ Widely available	▪ Well developed tech. ▪ Light weight	▪ Well developed tech. ▪ Light weight ▪ Small volume
Cons	▪ Need large area ▪ Non-continuous ▪ Orientation issue	▪ Need large area ▪ Low power ▪ Rigid & brittle	▪ Distance dependent ▪ Depending on available power source	▪ Need large area ▪ Highly variable output	▪ Highly variable output ▪ Low conversion efficiency (high volt./low amps.)

1.2 Significance of the Work

The author is working on a reliable ultra-sensitive radio frequency energy harvester. To address the different performance aspects two designs were implemented using the GF 22nm FDX technology, which is known for its good power consumption and low current leakage. These two designs are then integrated in a hybrid system to regulate the output voltage and provide circuit protection for the load.

The first design is a three-phase rectifier. It consists of an antenna connected to a phase shifter, which generates three different phases feeding the inputs of a triple branch rectifier. The three-phase rectifier is implemented and verified on Cadence at both pre- and post-layout stages. The outputs from these three phases are connected through the load and a smoothing capacitor.

The second proposed rectifier design is based on a varactor ladder rectifier. The varactor is well known for its low capacitance in a low input range. This makes it an excellent candidate for sensitive rectifiers, which require low capacitance for a high sensitivity outcome. The varactor's capacitance increases with the input level until it saturates.

Furthermore, both designs have been integrated in a full system to reconfigure the right output of the rectifier and direct it to a power management unit to regulate the voltage and deliver a stable supply to the load. The proposed RFEHs can be integrated on-chip with multisource harvesters to supply systems that work in different environmental conditions without weaknesses. In addition to that, the design is compact, and it is feasible to be implanted into the human body to send and receive vital signals about the body's health with a complete battery-less system.

1.3 Research Objectives

This thesis proposes new radio frequency energy harvesters that can harvest the ambient radio frequency signal power from the surroundings. The aim of this work is to develop a sensitive system with high power conversion efficiency. The design should be reliable and compact to be integrated with sensor nodes and IoT devices. The focus of this research can be summarized as three objectives:

1- Propose and validate a high-efficiency radio frequency energy harvester:

The design of this radio frequency energy harvester is based on a three-phase rectifier topology modified to be useful in radio frequency scenarios. The author does not exclusively limit the investigations for this design, but the initial results are promising. The design can convert around 80% of the power to DC power to be stored in a supercapacitor or any storage element. One of the main advantages of such a design is that it is compatible with the antenna array concept. Multiple elements can feed the rectifier input terminals and pass the power to the diodes. After that, the input signals interfere to constructively build the output DC power. As you may expect, this technique's output power density is high, and most of the harvested power is converted to DC.

2- Propose and validate a high-sensitive radio frequency energy harvester:

The design is based on a modified version of a ladder rectifier. The pumping capacitor is replaced with a varactor to enhance the performance of the rectifier in a low input power range. In addition to that, the rectifier has reduced area compared to the conventional one which suggests lower cost. The system is compact and can be integrated with other SoC included. The aim of such a design is to harvest even the smallest amount of the available ambient power and convert it to DC power. This design also suggests a high conversion efficiency in this small power range. This topology can be used to power control circuits or start-up circuits from a cold start.

3- Propose and validate a hybrid system that can reconfigure the best rectifier based on the input and regulating the output voltage:

The author is working on good specs and a practical, reliable design for day-to-day use. The design should be adapted to the fluctuations occurring in the environment. To do so, the system should include an adaptive control circuit that tracks the best rectifier output to be directed to a power management unit. This unit regulates the output voltage and delivers a stable signal to supply the load. In such cases, the system can maintain high efficiency and sensitivity with a wide input power range.

1.4 List of Publications

In pursuit of the aforementioned objectives, the following three publications propose a full adaptive radio frequency energy harvesting system for IoT applications:

A. Refaei, S. Genevey, Y. Audet, and Y. Savaria, "High-efficiency wide input power range three-phase radio frequency energy harvester for IoT applications," *IEEE Trans. Microw. Theory Techn.*, doi: 10.1109/TMTT.2024.3456690.

A. Refaei, S. Genevey, Y. Audet, and Y. Savaria, "Varactor-based ladder rectifier radiofrequency (RF) energy harvester for IoT applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, 2024 [Submitted].

A. Refaei, S. Genevey, Y. Audet, and Y. Savaria, " An Adaptive RF Energy Harvester Operating Over -30 to 0 dBm Input Range for IoT Applications," *IEEE Access*, 2024 [Submitted].

1.5 Thesis Organization

This Ph.D. thesis includes seven chapters. The Introduction presents this research's motivation and significance. The research objectives and the list of publications are also discussed. This chapter provides a window into what this research aims to achieve and a summary of the outcomes.

In chapter two, we present a system design overview of radio frequency energy harvesters (RFEHs), including the different block designs, variations, and theoretical background. Then, each sub-block of the system is illustrated and explained in more detail, starting with antenna design considerations, matching network design considerations, rectifier design considerations, adaptive circuit design considerations, and storage element types.

Chapter three shows the first article explaining the first proposed rectifier design. The three-phase rectifier objective is to provide high efficiency for RFEHs. The article presents different approaches to integrating the three-phase rectifier with the antenna and the matching network to optimize the efficiency. The phase shifter design, the matching network, and the three-phase rectifier are all

explained and discussed theoretically from design perspectives. Then, the experimental prototype is shown, with the components' values and the measurement setup used. The result of this rectifier is presented in detail with a performance comparison with state-of-the-art articles reporting similar specifications.

Chapter four presents the second article explaining the second proposed rectifier design. The varactor-based ladder rectifier objective is to provide high sensitivity for RFEHs. The article presents the theoretical background behind the design. Then, the proposed design is discussed in detail, explaining the principle of operation. The implemented prototype, the component values used, and the measurement setup are illustrated. The result of such a rectifier is then presented with a performance comparison.

Chapter five introduces the adaptive system for the RFEH. It discusses the overall system architecture with information on how the system performs. Simulations characterize the high-efficiency path and the high-sensitivity path. Moreover, Chapter Five presents the input reconfiguration circuit and the integrated output optimization system. Such a system aims to provide a stable voltage at the load for different conditions. The output optimization system sub-blocks are the UVLO and the buck/boost converter, which are presented with details and simulation results.

Chapter six is a general discussion that summarizes the research objectives, the implications and significance of our work, and the limitations. Chapter seven summarizes our contributions and achievements in this research project. It also presents future aspects of the implemented designs that can be improved later.

CHAPTER 2 LITERATURE REVIEW

2.1 Radio Frequency Energy Harvester Principles

The radiofrequency energy harvester systems can be broken down into several components: the receiving antenna, the impedance matching network (IMN), the rectification block, the storage element with the power management unit, and the portable device or IoT (load), as indicated in Figure 2.1.

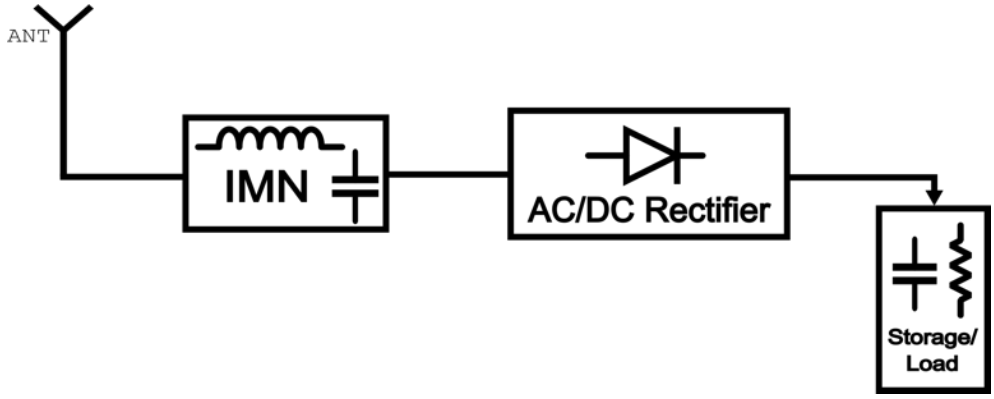

Figure 2.1: Conceptual block diagram of an RF energy harvesting system

In theory, the system performance is dominated by the Friis equation in Figure 2.2, which reflects how the system responds [5]. This equation gives a good insight into the power available on the receiving side. This power can be calculated by getting the transmitted power, the transmitting gain, the receiving gain, and the path losses. Two main definitions of RFEHs need to be addressed. The first one is the sensitivity (P_{AV}), which is the lowest possible RF power that can be harvested and converted into measurable DC power. It can be estimated using the transmitted power (P_T), the antenna gain (G_T, G_R), the frequency of operation (f), the distance (d), and the losses as indicated in equation (2.1). The second important definition is the efficiency of the harvested DC power to the available RF power. It can be calculated using the efficiency formula, which is broken down into three terms: the matching network efficiency, the rectifier efficiency, and the power management unit (PMU) efficiency [6], as shown in equation (2.2). There is reflection between

the matching network and the rectifier due to the mismatch in the impedance. This reduces the input power at the rectifier side.

$$P_{AV} = P_T + G_T + G_R - Path\ loss \qquad \text{or} \qquad P_{AV} = P_T G_T G_R \left(\frac{c}{4\pi df}\right)^2 \tag{2.1}$$

$$\eta_{System} = \frac{P_{OUT}}{P_{AV}} = \eta_{Matching\ Network} \times \eta_{Rectifier} \times \eta_{PMU} = \frac{V_{OUT}^2}{R_L \times P_{AV}} \tag{2.2}$$

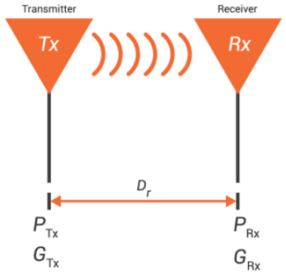

Figure 2.2: Transmitter and receiver block diagram

The antenna of the RFEH can be single-ended or differential based on the rectifier type [7]. There are lots of antennas that can be used based on the application, for example, metamaterial antenna [8], multiport pixel antenna [9], planar antenna array [10] … etc. The matching network can be a pi or L matching network based on the application [11]. The radio frequency rectifier can be a Dickson charge pump [12], a cross-coupled rectifier [13], a voltage multiplier [14] … etc. The power management unit adapts the RFEH system to the environmental conditions, such as the available power, and to the application requirements, such as the required voltage, the run time, and the power dissipated [15]. Radio Frequency energy harvesters can be used in several applications, such as sensor nodes [16], implanted devices [17], and IoT applications [18].

In this literature review, the author breaks down the different subblocks of the system, explaining each block's design topologies, specifications, and challenges. Moreover, the survey includes solutions introduced to overcome these challenges.

2.2 Antenna Design Considerations

The antenna is the first receiving block in the radio frequency energy harvester. Several types of antennas are suitable, for instance, differential antennas [19], spiral antennas [20], planar antenna arrays [10]…etc. A patch antenna is used with two output ports for the differential antennas. Both ports have the same gain, effectively doubling the output gain at the two ports. They have opposite phases with a phase shift of 180 degrees, as indicated in Figure 2.3. The patch antenna ports are connected to a Greinacher voltage doubler rectifier, as shown in Figure 2.4. This differential design is repeated twice over the same patch antenna, with a total of four ports. This doubles the gain one more time. The positive/ negative terminals of the rectifier double the output voltage. Moreover, two rectifiers are connected in series, doubling the output again. In total, we have a voltage gain of four [19].

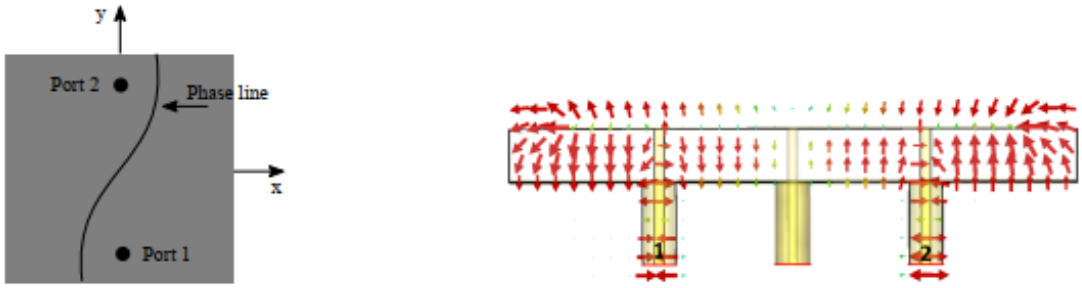

Figure 2.3: The phase line and phase diagram of a differential antenna [19]

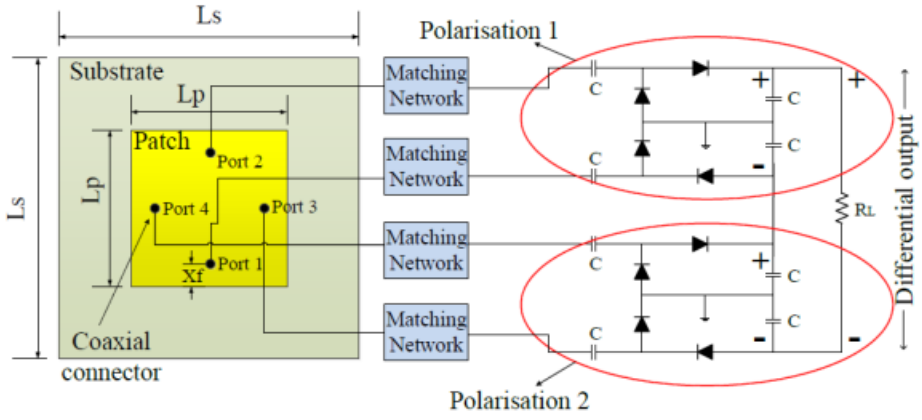

Figure 2.4: The circuit schematic of the Greinacher voltage doubler with differential antenna [19]

The spiral antennas are designed using metamaterials, which are modeled as shown in Figure 2.5. Metamaterials are those materials that change their electric and magnetic moments when interacting with electromagnetic waves [8]. This, in turn, changes the antenna's permeability and permittivity. The metamaterial antenna has a reduced size and good efficiency, which makes it a good choice for RFEHs.

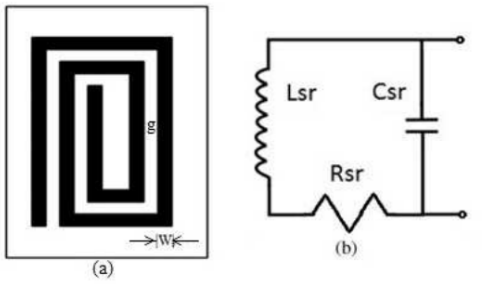

Figure 2.5: The spiral antenna structure and circuit model [8]

For planar antenna arrays, a multi-port pixel rectenna shows good performance results. A paper of reference [9] investigates the performance of a single-port antenna versus a multiport antenna. It suggests, with experimental results, that using an antenna array with three ports improves efficiency over a single-port antenna design. The system indicated in Figure 2.6 shows higher sensitivity as well compared to any single-port system.

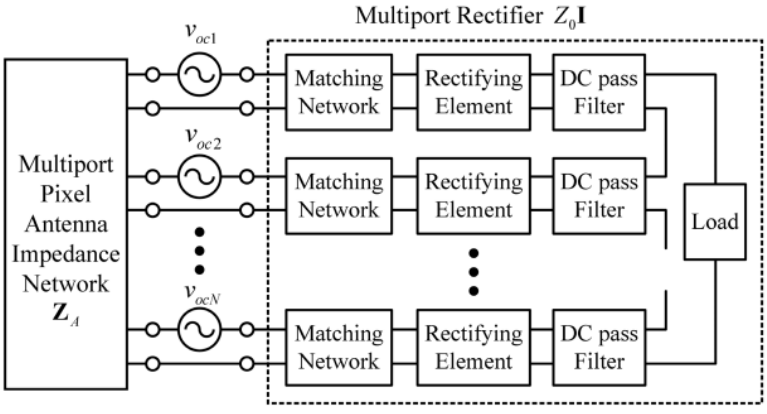

Figure 2.6: Multiport pixel RFEH system diagram [9]

There are two main schemes regarding the summation of RFEHs: the first one is RF combining, and the second is DC combining [21]. For the DC combining, each antenna in the array is connected to a rectifier; then all the output voltages are added up using a DC combining circuit, as shown in Figure 2.7. For the RF combining scheme, the multiple antennas are connected in parallel using an RF combining circuit, as shown in Figure 2.8. The paper suggests through very rigorous analysis and steps that using RF combining scheme can lead to higher power conversion efficiency. They performed experimental analysis on the two schemes, varying the number of the receiving antennas. The RF combining scheme shows better efficiency for more than six receiving antennas.

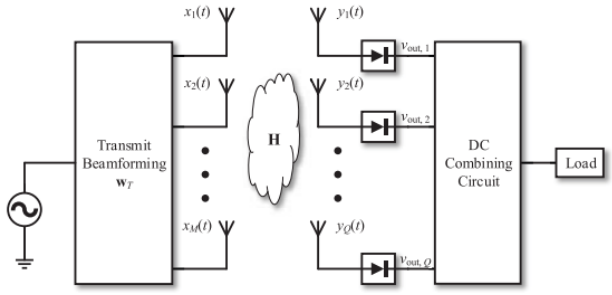

Figure 2.7: DC combining circuit scheme used in RFEHs [21]

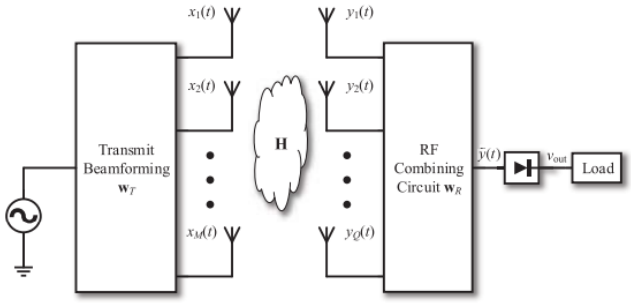

Figure 2.8: RF combining circuit scheme used in RFEHs [21]

2.3 Matching Network Design Considerations

The impedance matching network is a block integrated between the antenna and the rectifier, as shown in Figure 2.9, to ensure maximum power transfer [22]. For the RFEH efficiency to be high,

the rectifier impedance should be matched with the antenna impedance to avoid any reflections to the antenna side.

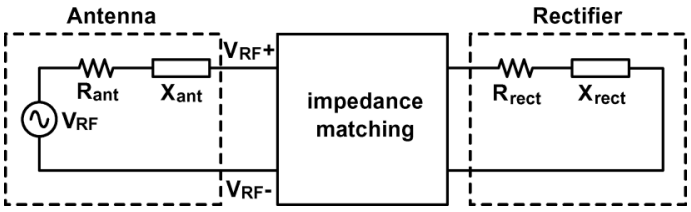

Figure 2.9: The impedance matching network (IMN) model [22]

As the name suggests, the L matching network consists of an inductance, L, and a capacitance, C, components connected in an L shape. There are several configurations, as indicated in Figure 2.10. We use the low pass configuration to avoid blocking any low-frequency harmonic components of the input voltage [6].

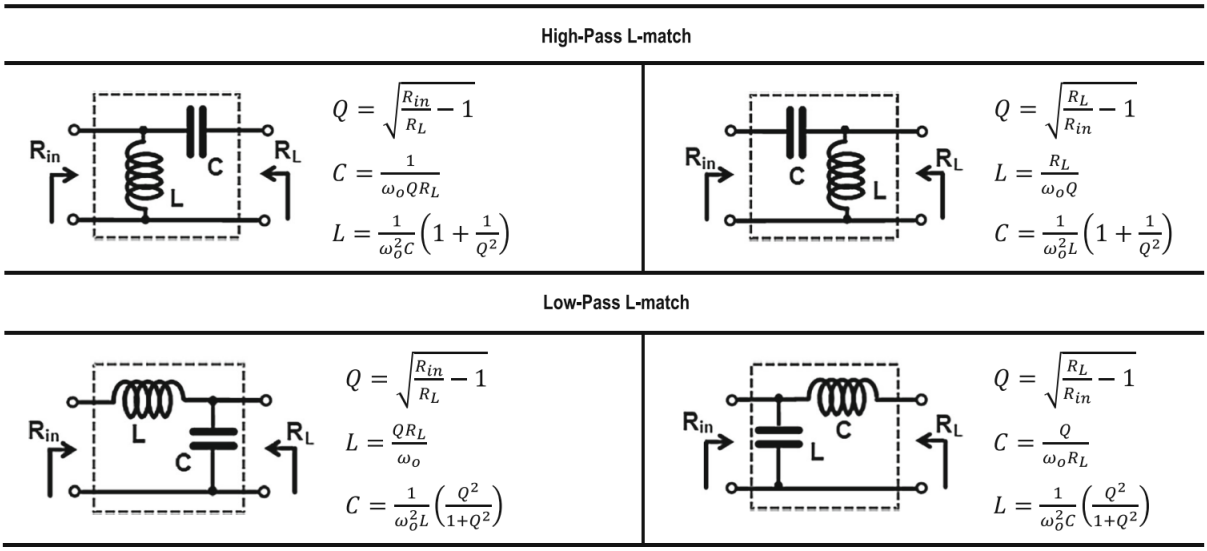

Figure 2.10: The L shape IMN different configurations [6]

The T and Pi matching networks are considered more complex alternatives than the L matching network. They do not change the impedance match. Instead, they change the Quality factor of the network and subsequently improve the boosting ratio. For an ideal matching, the antenna voltage amplitude (V_{ANT}) can be expressed as indicated in equation (2.3) [23]:

$$V_{ANT} = \sqrt{8 \times Z_{ANT} \times P_{AV}} \tag{2.3}$$

Where Z_{ANT} is the antenna resistance and P_{AV} is the available power

The quality factor is one of the main things to consider in the matching network design since it has a direct relation with the boosting ratio of the network [22]. It is defined as the ratio between the stored energy in the L or C components to the losses or the power dissipated in that component as indicated in equation (2.4) where ω is the frequency of operation, L is the inductance, C is the capacitance, R is the resistance that represents the losses in the component, X_L is the inductive reactance and X_C is the capacitive reactance. It has a direct relation with the inductance or the capacitance values. However, it has a value of around 50 for the good inductors and 500 for the good capacitors around 900MHz [23]. The combined L and C quality factor is determined by an equivalent value governed by the maximum power transfer theorem. This can ensure 100% transfer ratio between the received power from the antenna to the rectifier input. In the case of zero mismatch or perfect matching, the voltage gain is represented as shown in Figure 2.11, and the rectifier input voltage is around 10 times the antenna input voltage if the quality factor is around 20. A gain of 10V/V is generally the limit that is considered practical in most real-life scenarios.

$$Q = \frac{1}{2}\frac{\omega L}{R} = \frac{X_L}{2R} \; or \; Q = \frac{1}{2}\frac{1}{\omega RC} = \frac{X_C}{2R} \tag{2.4}$$

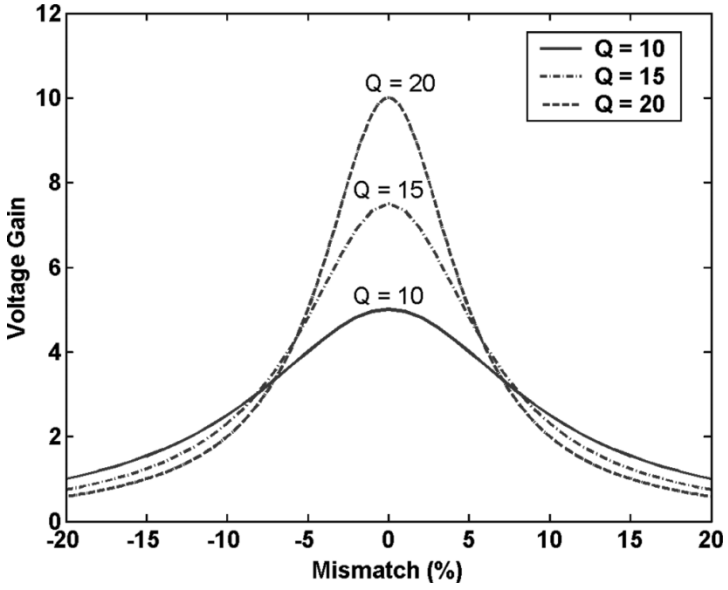

Figure 2.11: The voltage gains versus the mismatch with different quality factors [22]

To design an excellent matching network, a few parameters must be considered, such as the input impedance of the rectifier, the quality factor of the provided components, the required boosting ratio based on the rectifier specs, and the frequency of operation [23]. The most accessible parameter in these equations is the source or antenna resistance. It is assumed to be 50 ohms. The frequency of operation is also set to be in the WIFI range. This work uses four frequencies: 900 MHz, 1.8 GHz, 2.1 GHz, and 2.4 GHz. The input impedance of the rectifier can be divided into two parts: the real part and the imaginary part. The author ran test benches to see the range of values for our rectifiers' real and imaginary parts. The rectifier resistance range is from 500 to 2 kΩ, and it decreases in regular working operation [16]. The input capacitance, on the other hand, increases with the increase of the input power level. As equation (2.6) suggests, the input resistance (R_{IN}) of the rectifier must be kept high compared to the source or antenna resistance (R_S) to obtain a good boosting ratio. On the other hand, the quality factor (Q) of the components has a limit, as shown in equation (2.7). After that limit, increasing the resistance will not make any more boosting. The author investigated many references [24], [25], [26] that made investigations on how we choose the (R_{IN}) and the input capacitance (C_{IN}), and they showed that the best practice is to pick them on the same level as the threshold voltage of the rectifier transistor. Given these parameters, the matching inductor (L_m) and the matching capacitor (C_m) can be calculated and finely tuned to give the best performance as indicated in equations (2.8) & (2.9).

$$A_{V,boost} = \frac{V_{REC}}{V_{ANT}} = \sqrt{R_{IN}/R_S} \tag{2.6}$$

$$Q = \frac{1}{2}[R_{IN}C_{IN}\omega + \sqrt{R_{IN} - R_S/R_S} \tag{2.7}$$

$$L_m = \frac{R_{IN}}{\omega}\frac{1}{R_{IN}C_{IN}\omega + \sqrt{R_{IN} - R_S/R_S}} \tag{2.8}$$

$$C_m = \frac{1}{R_S\omega}\sqrt{R_S/(R_{IN} - R_S)} \tag{2.9}$$

2.4 Rectifier Design Considerations

For the radio frequency energy harvester to work optimally, the rectifier forward ON- resistance, the input capacitance, and the reverse leakage current should be kept as small as possible [27]. On the other hand, the output voltage and the efficiency need to be high to be suitable for IoT applications. The efficiency curves are affected by the turn-on voltage of the diodes and the leakage current, as shown in Figure 2.12. At low power levels, the efficiency degradation is dominated by the threshold voltage needed to pass the current to the next stage. However, this problem no longer dominates at a higher input power level, and the leakage current is the major factor affecting efficiency. As a result, there is an optimal point where the efficiency is maximum for the input power [23]. A serial arrangement of the rectifier can be adopted to increase the voltage gain and get a higher voltage. However, since the added transistors add more voltage drop, the system sensitivity decreases, but the overall efficiency improves on a higher level. A parallel arrangement of the rectifier should be adopted to improve the sensitivity, but it will lead to less output voltage. A configurable system with parallel and series arrangements can optimize the sensitivity curve over a wide range, as shown in Figure 2.13 [6]. Moreover, having a reconfigurable matching network can help maintain the lowest possible reflection losses.

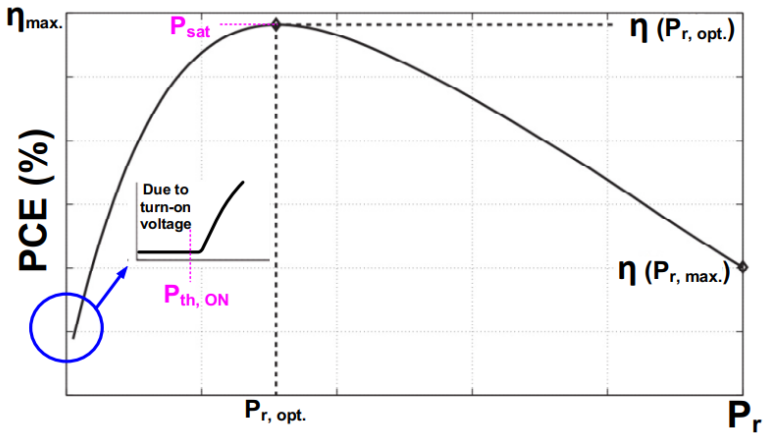

Figure 2.12: The power conversion efficiency typical curve versus the available power [23]

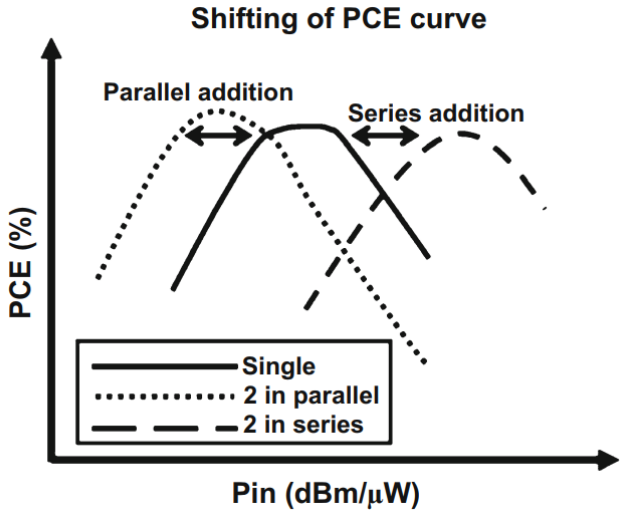

Figure 2.13: The power conversion efficiency curve versus the available power showing the rectifier configuration effect [6]

Several types of rectifiers are used for RFEH, such as voltage multipliers and CMOS cross-coupled differential rectifiers [28]. The most common voltage multipliers are Greinacher doublers and Dickson charge pumps. Table 2.1 summarizes the key differences between such rectifiers.

For the Greinacher doubler, the input AC signal is applied to the rectifier, as shown in Figure 2.14. Each cell has two diodes and two capacitors. In the positive RF cycle, the capacitor starts charging. Therefore, the second diode in the figure will be short-circuited until the capacitor reaches the maximum value of the source. In the negative half cycle, the first diode will be short-circuited, and the current will continue. As a result, the two capacitors will be connected in series, and the resultant voltage over the cap will be double the input voltage. Assuming no losses in the diodes and zero drop voltage, the output voltage keeps increasing linearly with the number of stages, N, and $V_{out}=N*V_{source}$. Since the capacitor works as a smoothing element here due to the charging and discharging times, the AC signal is converted to DC [29].

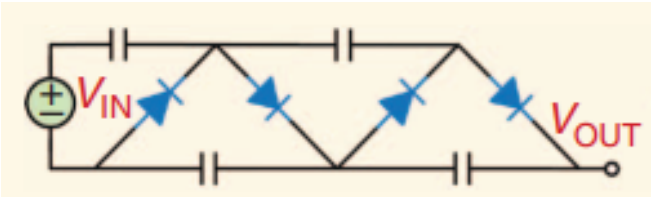

Figure 2.14: The Greinacher doubler schematic with two stages [29]

For Dickson charge pumps, the design is similar, for example, Greinacher, except that it requires a clock signal that is applied to the capacitor, as shown in figure 2.15. The clock signal charges and discharges the capacitor based on the state zero or one. When enough voltage exists between the capacitor terminals, the diode works and moves to the next stage. It accumulates the voltage step by step since the diode orients it in one way [29].

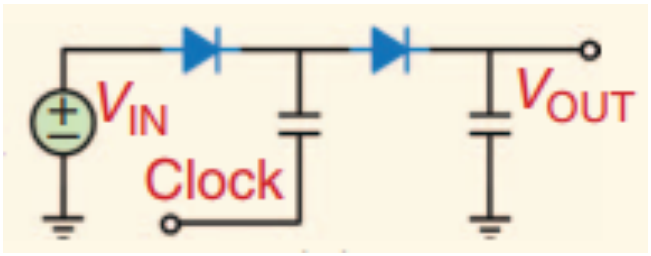

Figure 2.15: Dickson charge pump schematic [29]

The CMOS cross-coupled rectifiers [23] consist of two back-to-back inverters with pumping capacitors at the input side. At the positive input cycle, the bottom inverter NMOS will turn on, and the top inverter PMOS will also turn on. This will allow the top charged capacitors to pass the voltage value to the output stage or discharge, and at the same time, the bottom capacitor will start charging. The top inverter NMOS and the bottom inverter PMOS will turn on in the second half cycle. This makes the bottom charged capacitor pass the voltage value to the output stage, and the top capacitor starts charging or holds the voltage, and so on. By accumulating the voltage over the two cycles and N number of stages, the voltage gets boosted and converted from AC to DC. This type of rectifier is considered the most common and efficient type for radio frequency energy harvesters.

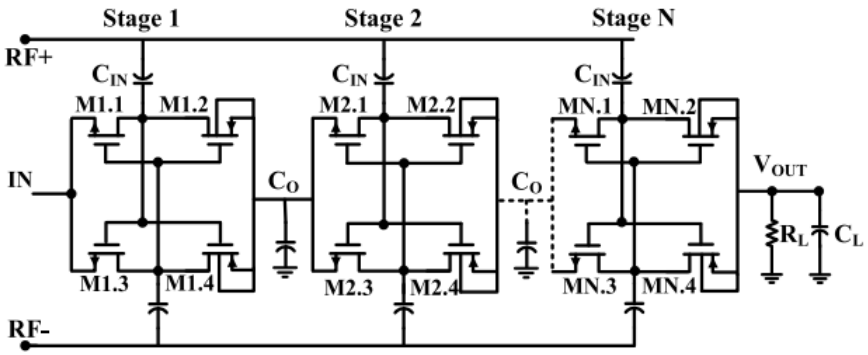

Figure 2.16: Cross-coupled rectifier schematic [23]

Table 2.1: RF energy harvester different rectifier topologies performance

	[18] 2021 TCAS-I	**[30] 2017 TCAS-II**	**[16] 2019 JSSC**	**[31] 2019 TCAS-I**	**[32] 2017 JSSC**
Technology	TSMC 130 nm	TSMC 65nm	TSMC 65nm	TSMC 130nm	TSMC 180nm
Topology	Cross-coupled dynamic + Static VT compensation	Cross-coupled	Cross-coupled	Dickson	Greinacher doubler
Frequency	915MHz	900MHz	2.4GHz	896MHz	915MHz
Effective Area	0.029mm^2	0.048mm^2	0.000125mm^2	0.053mm^2	1.08mm^2
Techniques	VT compensation	Dual-path	Modeling and parasitic aware design	VT compensation	Tuned MN
No. of Rectifier Stages	10	5	1	4	8
Any Additional Requirments	-	-	MPPT	-	Deep n-well
Sensitivity @ Vout and Rload	-29 dBm @ 1V & 100MΩ	-17.7 dBm @ 1V & ∞	-17.1 dBm @ 0.4V & ∞	-20.5 dBm @ 1V & 1MΩ	-14.8 dBm @ 1V & 1MΩ
Peak PCE & Load	42.4% @ -16 dBm & 0.	34.5% @ -2 dBm & 147kΩ	48.3% @ -3 dBm & PMU	43% @ -11 dBm & 1MΩ	25% @ -5 dBm & PMU

Rectifiers inherit limitations due to the high R-on resistance and reverse leakage current. Several techniques are used to improve the performance of conventional rectifiers. The first common technique is threshold voltage compensation since Vth is one of the main limitations that reduces the harvester efficiency [33]. The second common approach is using ultra-low power diodes (ULPD) [34]. The third approach is using gate/ body biasing [22].

Regarding threshold voltage compensation [35], NMOS and PMOS transistors are connected, as shown in Figure 2.17. The source of the NMOS is connected to the ground, and the source of the PMOS is connected to V_{out} and the load capacitance. The drains of the two transistors are connected to the input capacitance. The objective is to reduce the threshold voltage by boosting the VGS of both transistors. The NMOS gate is connected to the highest voltage in the Vout node schematic, while the NMOS source is grounded. The PMOS gate works the same way, where the gate is connected to the lowest voltage node in the circuit while the PMOS source is V_{out}. This design can help improve the system sensitivity, efficiency, and boosting ratio. However, one of the main criticisms of this design is that it does not improve the leakage of the transistors. Current can be discharged to the ground if the output voltage is high enough to turn on the NMOS transistor in the positive cycle, and the same may apply to the PMOS in the negative cycle.

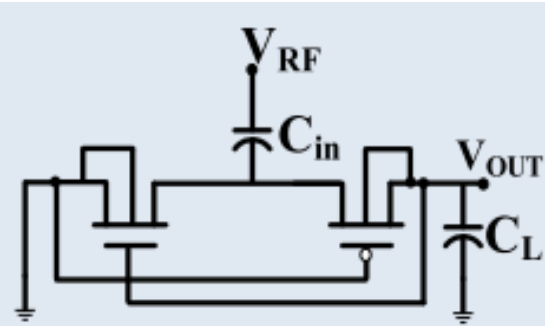

Figure 2.17: Threshold voltage compensation scheme [35]

Regarding ultra-low power (ULP) diodes, two PMOS and NMOS transistors are connected, as shown in Figure 2.18. The objective is to reduce the leakage current in the reverse mode of operation and keep good conductivity in the forward mode. In other words, a low resistance needs to be seen in the forward mode from the input side, and a high resistance needs to be seen in the reverse mode from the output side. In the standard configuration in the forward mode, the gate

voltage increases when the input is high since it is connected to the drain, and the transistor becomes on. This passes the signal from the input to the output with a resistance $1/g_m$. In ultra-low power diode configuration, when the signal goes up, the NMOS gate increases, and the transistor turns on since the source voltage is still zero. The PMOS also turns on since the gate is zero and the source is high. The ULP diode eventually turns on with the same voltage drop as a standard diode. However, In the reverse mode, both transistors turn off strongly since the voltage at the output is higher than the voltage at the input, blocking any chance of high leakage from the output back to the input [36].

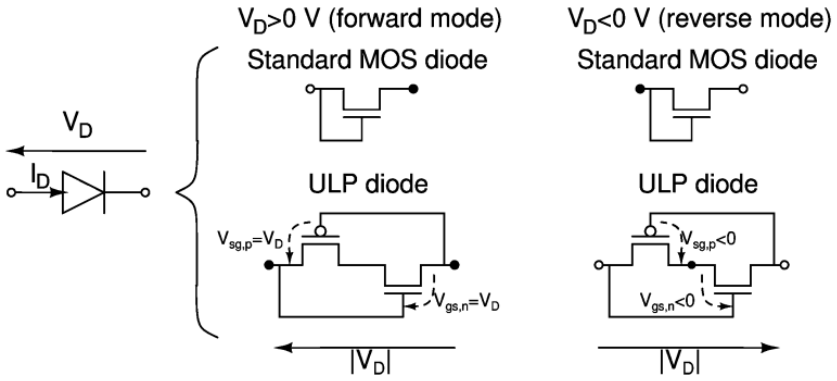

Figure 2.18: ULP diode operation modes [36]

Regarding gate biasing [22], the basic idea is to generate a bias between the gate and the drain to increase the difference between the gate voltage, or VG, and the source voltage, or VS. The capacitor gate terminal is connected to the connected diode since this node is floating, as shown in Figure 2.19. As the sinusoidal input voltage increases, the VG increases and goes higher than the input. This boosts the output voltage and improves the design efficiency and sensitivity. The load capacitor, $C_{L,}$ should be higher than the compensating capacitor to smooth the voltage and accumulate it through the stages.

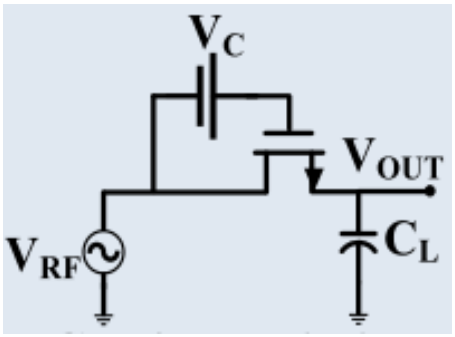

Figure 2.19: Gate biasing schematic [22]

Regarding the body terminal connection, we will present some of the comparisons from the literature to analyze and choose accurately, as indicated in Figure 2.20. Conventionally, the body connection of the transistor is connected to the source terminal. for normal operation, the NMOS body is connected to the ground, and the PMOS body is connected to the VDD. This reduces the leakage current through the transistor and protects the structure. However, the threshold voltage should be as minimum as possible for energy harvesting applications to minimize the conduction losses. The threshold voltage equation (2.10) below suggests that V_{th} can be reduced if V_{SB} is positive. In dynamic body biasing [37], the body of the NMOS and PMOS is connected to the input. At the ground input level, the body and the source of the NMOS will be the same, reducing any leakage, and the NMOS will be off. However, the PMOS will be operating, and V_{thp} will be lowered due to the difference between the source and the body voltages. At VDD or high input level, there will be a difference between the body and the grounded source of the NMOS, which will lower its threshold voltage and, therefore, increase its conduction current. The opposite will occur on the PMOS side. This technique shows better power consumption and higher conduction current, as shown in Table 2.2, making it a good candidate for radio frequency energy harvesting.

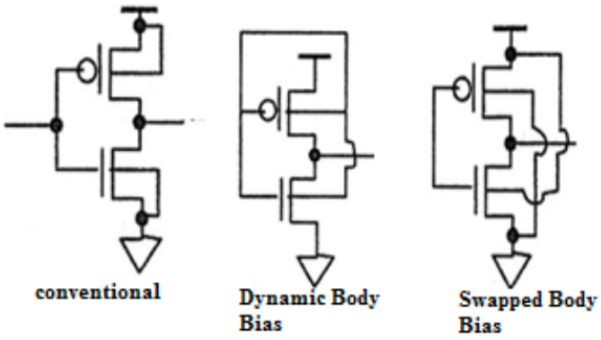

Figure 2.20: Different body connection schemes [37]

$$V_{th} = V_{t0} + \gamma\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|} \tag{2.10}$$

Table 2.2: Power Consumption of swapped body bias (SBB) dynamic threshold (DT) at different supply voltage [37]

voltage(mv)	Power(nw)		% Reduction
	SBB	DT	
300	3.154	2.995	5
350	57.93	13.2	77.2
400	159.1	48.15	69.7
450	390.2	152.2	60.99
500	863.2	425.4	50.7

2.5 Adaptive Control Circuit and Summation Block Design Considerations

Radiofrequency energy rectifiers provide the mechanism and the principle of operation to convert the RF signals into DC power. Much research has been conducted to maximize the performance of the RFEH system. One way to enhance the performance is to have a multi-band energy harvester [38], for example, 900MHz, 1.4GHz, 2.1GHz, and 2.45GHz. A matching network and a rectifier are implemented so that each band can harvest the power separately. Regarding the antenna, there are a few options: implementing a single antenna for each band [39], implementing a wide band antenna that can cover the frequency range [1], or implementing a multi-port antenna [2].

The basic idea of summation is to add two configurations with different advantages and make them work together to provide better performance. For example, as seen in Figure 2.21, the PCE trend of Figure 2.21a has better efficiency at a lower input power level or high sensitivity. Figure 2.21b provides better efficiency at a higher power level. The objective is to get to the third curve, figure 2.21c, which represents the summation of both [30].

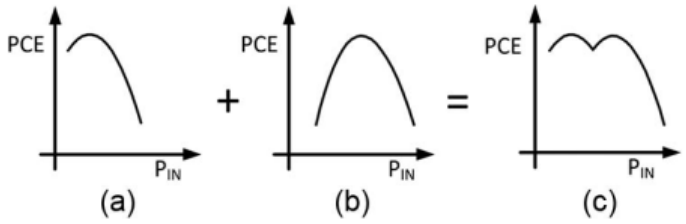

Figure 2.21: The PCE versus the available power, a) at low input power level, b) at higher input power level, and c) the summation curve of both regimes [30]

One way to do so is to implement two different rectifiers of the same type. In Figure 2.22, the low power path has low voltage threshold transistors that make the rectifier more sensitive but at the same time leakier. This should not be a significant issue at low power levels since the input and output power are low. However, at a higher power level, the leakage becomes more dominant than the drop voltage due to the threshold, and high voltage threshold transistors are preferred to reduce this leakage. The summation block combines both goods with a reference circuit. Suppose the output voltage of the high-power pass is higher than the reference path. In that case, the high-power path is chosen since it gives better efficiency than the reference path made of regular voltage threshold transistors and potentially better than the low voltage threshold path. On the contrary, if the output of the high-power path is lower than the reference, the switches work and turn off the high path and direct the signal into the low-voltage threshold path [30].

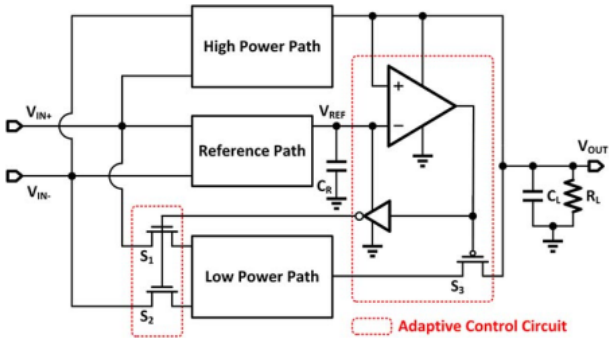

Figure 2.22: The adaptive control circuit for RFEH [30]

The paper of reference [30] reports the power conversion efficiency results of the system for different transistor types. This gives an insight into the operation of the rectifier while changing the threshold or drop voltage. Low threshold (LVT) general-purpose transistors work well in the low range, and high threshold (HVT) low-power transistors work better in the higher range, as shown in figure 2.23. After applying the summation scheme, we can see the blue curve in figure 2.24 switches between the low to the high-power path to maintain a wide overall conversion efficiency of around 30%. Moreover, the system demonstrates higher output voltage than the regular single rectifier, as seen in Figure 2.25. This is an example of implementing a summation block that depends on the type of the transistors used in the rectifier.

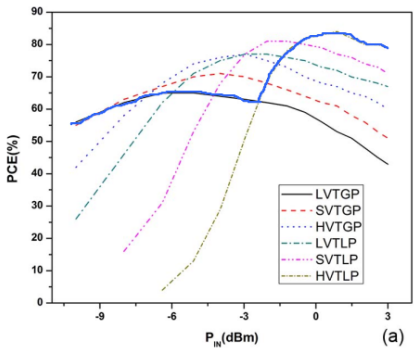

Figure 2.23: PCE curves for different Vth transistors versus the available power [30]

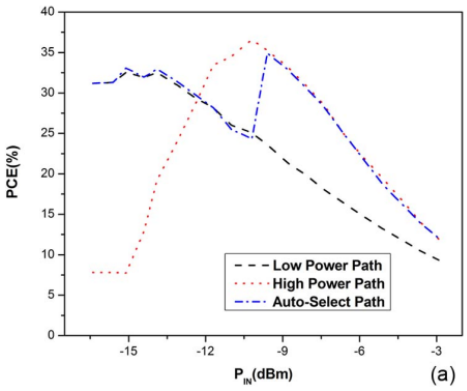

Figure 2.24: PCE curves for low and high-power paths with auto-select path versus the available power [30]

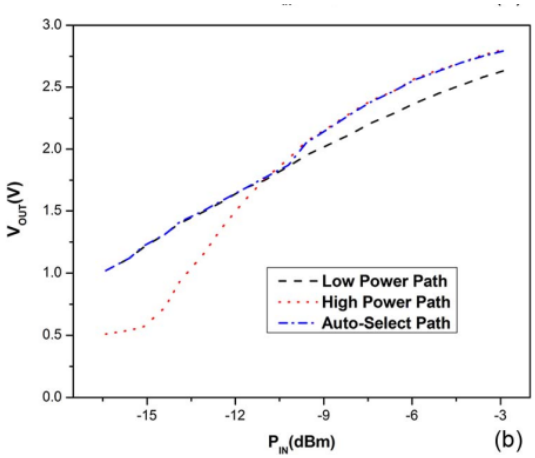

Figure 2.25: The output voltage for low, and high-power and auto select path versus the available power [30]

In reference [32], the author implements a reconfigurable rectifier and a reconfigurable matching network, as shown in Figure 2.26. The rectifier can vary from one to eight stages. The on-chip matching network also changes based on input power. This has been done using a rectifier controller to change the stages based on the available power, as in Figure 2.27. Their investigations show that increasing the number of stages improves the S_{11} parameter, as shown in Figure 2.28. This, in return, improves the sensitivity, and subsequently, the system has good efficiency and output voltage at a lower input power range if the maximum number of stages is configured. On the other hand, lowering the number of stages impacts the efficiency and the S_{11} parameter at a

lower range but improves them at a higher range. The controller changes the number of stages based on the output voltage. As it increases, the controller decreases the number of stages in action to maintain high performance. Moreover, the design includes a load or storage controller taking control over the output. There are two paths: the main path and the secondary path. When there is available power, and the load is saturated, the secondary path starts working and storing some energy when the available power is low. The matching network can be tuned using a digital circuit to allow maximum power transfer at every configuration.

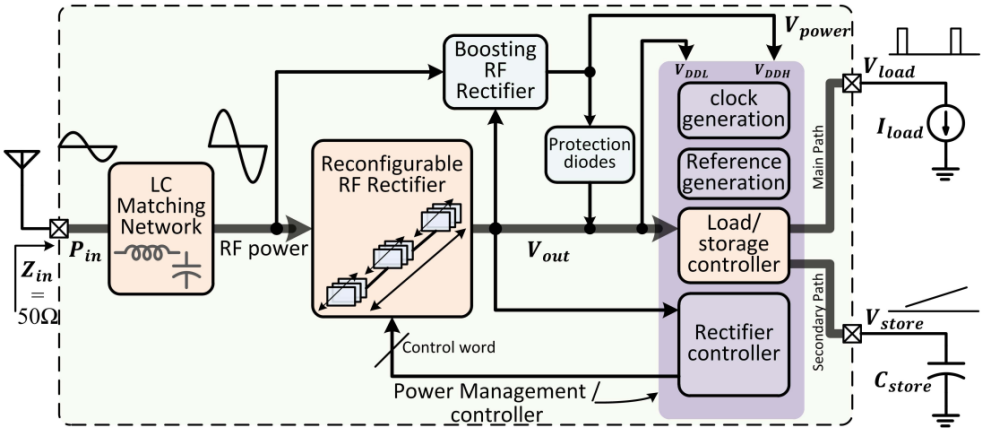

Figure 2.26: Reconfigurable RFEH system with multi-output path select [32]

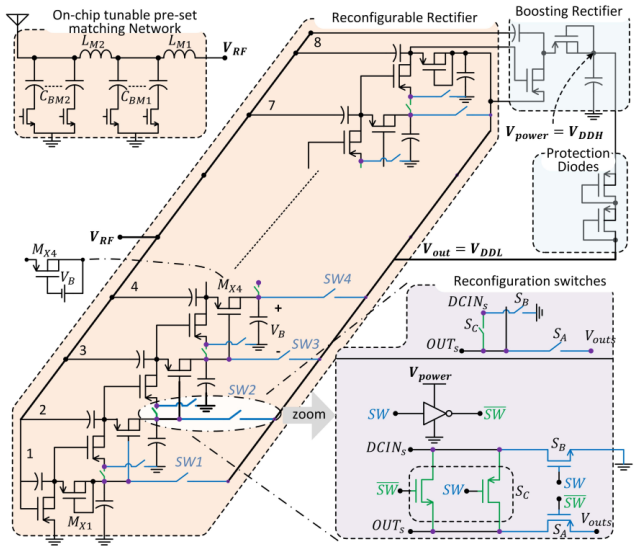

Figure 2.27: Reconfigurable RFEH system with tunable matching network and rectifier switches [32]

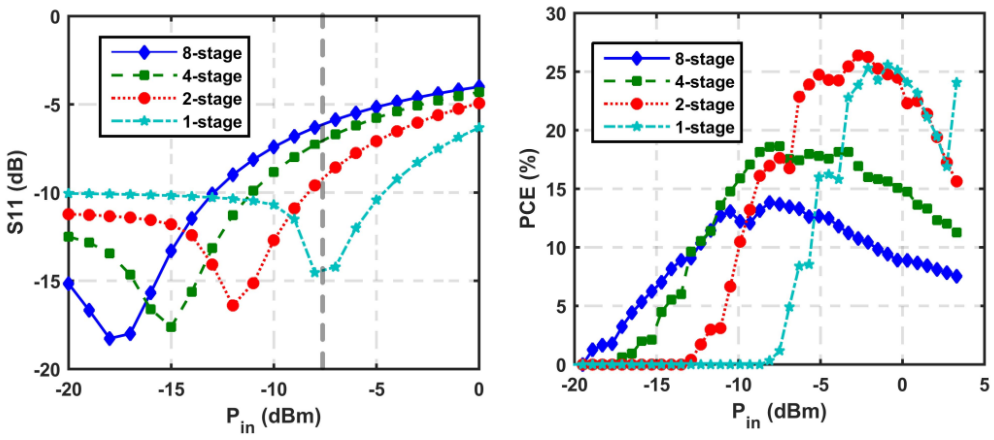

Figure 2.28: S_{11} and PCE parameter versus the available power for different rectifier stages [32]

An example of a multi-band design is presented in Figure 2.29. A dual-band antenna port is used for 900MHz and 2.45GHz. The configuration is known as diplexer as it simply isolates the two frequencies into two different ports for each [38]. The next step is to connect each port with a separate matching network and a rectifier to maximize the output. Using the diplexer can enable the harvester to work in environments where different sources exist with different frequencies. In Figure 2.30, we see that the S21 parameter has a maximum of 900MHz, around 0 dB, and the S31 parameter has a maximum of 2.45GHz. A DC summation network is presented in Figure 2.31 to connect the different rectifiers. The simplest way is to connect the rectifiers using a diode. If one band is unavailable, the diode will pass the output to the next one. This means that for each lost band, a voltage threshold is lost. To overcome this problem, the diode is connected between each combination of the rectifiers. This article [39] proposes a new smart way to pass the power between the bands using switches between the bands. If the output voltage from a certain band goes below a certain value, the switch turns on and becomes a short circuit. If all the bands work, the switches turn off, allowing the voltage to accumulate through the different stages and summed. They demonstrated that using this technique results in the highest efficiency.

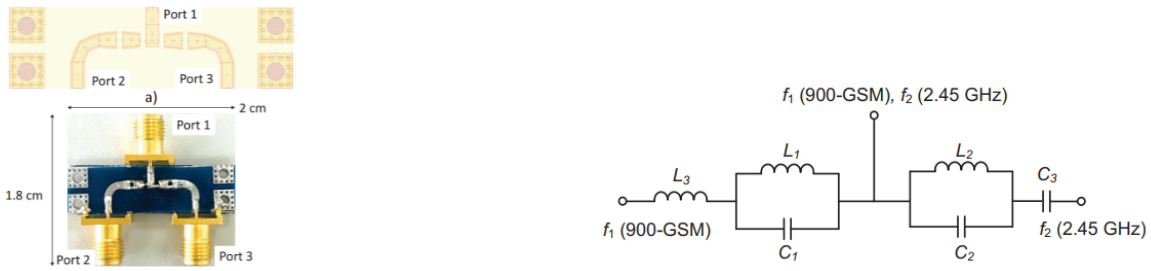

Figure 2.29: The diplexer footprint and design with the equivalent electrical model [38]

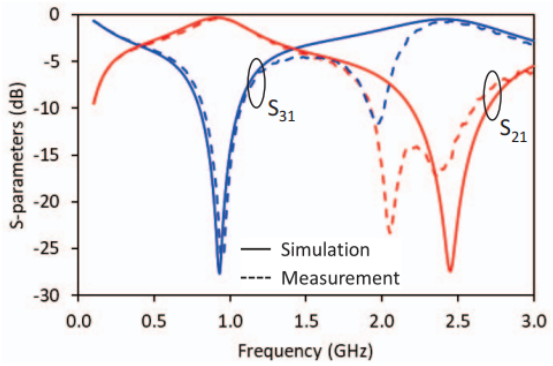

Figure 2.30: The S parameters for the diplexer versus the frequency [38]

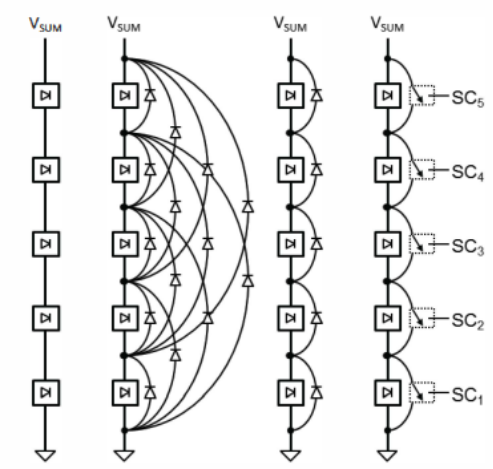

Figure 2.31: The proposed RFEH smart switch for DC combining [39]

2.6 Summary

This chapter discusses a review of state-of-the-art works on various topics related to this thesis. The RFEH system has been presented with all related conceptual building blocks. The chapter discusses a theoretical background with the fundamental equations of the system. Then, each system block is presented with design considerations such as the antenna, the matching network, the rectifier, and the adaptive control system. The antenna can be fabricated with different configurations like a differential spiral and antenna array, each type inheriting advantages and disadvantages. Then, the matching network designs are discussed to show the different techniques to ensure maximum power delivery. The rectifier limitations and design concepts are investigated to guide the reader of this thesis to the key points and the challenges in the rectifier stage. A comparison table with the most recent results for different types of rectifiers is presented with the key performance elements. Different adaptive networks and summation circuits are illustrated, highlighting the advantages and disadvantages of each. In the following chapters, the author presents new techniques and designs to overcome the limitations of the different topologies presented in this literature review.

CHAPTER 3 ARTICLE 1: HIGH-EFFICIENCY WIDE INPUT POWER RANGE THREE-PHASE RADIO FREQUENCY ENERGY HARVESTER FOR IOT APPLICATIONS

This chapter reproduces an article published in IEEE Transactions on Microwave Theory and Techniques on 19th September 2024.

- A. Refaei, S. Genevey, Y. Audet, and Y. Savaria, "High-efficiency wide input power range three-phase radio frequency energy harvester for IoT applications," IEEE Trans. Microw. Theory Techn., doi: 10.1109/TMTT.2024.3456690.

3.1 Abstract

The need for efficient and high-performance energy harvesting systems is rising to power modern wearable smart devices. Several energy sources can be harvested such as thermal, vibrational, and ambient Radiofrequency (RF). RF energy harvesters (RFEH) are widely adopted as they wirelessly deliver power. This paper proposes a new RFEH design based on the three-phase rectifier topology. The rectifier is integrated with a custom-designed phase shifter that can split received power equally and deliver three signals with 120° phase shift at the same moment. Due to their low forward drop voltage and high sensitivity, the rectifier diodes are chosen to be Schottky diodes SMS7621-005LF from Skyworks. A prototype is fabricated on an RT/Duroid® 5880 Laminates substrate with 0.005 inches thickness to reduce the dielectric losses. The RF energy harvester shows promising results in the ISM band at a 435.6 MHz frequency. At 8 dBm available RF power, the prototype demonstrates a high efficiency of 56% end to end at 6 kΩ load and 5.2 V output voltage. In addition, the system maintains an efficiency higher than 20% over a wide available input power range (IPR) of 28 dBm. The RFEH reports a 1 V sensitivity at -10 dBm. This system is ideal for supplying ambient sensor nodes and systems-on-chip (SoCs) in urban areas where RF electromagnetic waves are widely available.

3.2 Introduction

IoT systems and smart devices are increasingly becoming popular in the modern lifestyle. The world is more dependent on them to take important measurements for instance temperature, humidity and gas concentration and send it to a base station where this information is being analyzed and processed for different purposes. Internet of Things (IoT) devices either need replaceable batteries or an energy harvesting system to keep working. There are different types of energy harvesters, such as solar, thermal, vibrational, inductive coupling and radiofrequency energy harvesters.

The focus of this paper is to develop a radiofrequency energy harvester that can harvest ambient signals and convert them into DC power with a high conversion efficiency. Ambient Radiofrequency electromagnetic waves are everywhere where humans live, and they provide significant energy [5]. RF waves can be harvested and converted into a DC voltage to supply energy to low power devices and sensor nodes. Table 3.1 shows examples of typical sensor node specifications from the literature [40-43]. Their power consumption is in range of tenth of μW, while the supply voltage to these sensor nodes is around 1 V and the load impedance is on the order of few kΩ.

TABLE 3.1

TYPICAL SENSOR SPECS

Sensor Information	**[40] [2011]**	**[41] [2008]**	**[42] [2013]**	**[43] [2013]**
DC Supply (V)	1	0.3	0.8	0.45
Power Consumption (μW)	150	10	15	14
Equivalent Impedance (kΩ)	7	9	11	14

Radiofrequency energy harvesting systems can typically be broken down into five components, a receiving antenna, an impedance matching network (IMN), a rectification block, a storage element and the load as shown in Figure 3.1. In theory, the system performance is determined by the Friis equation as follows:

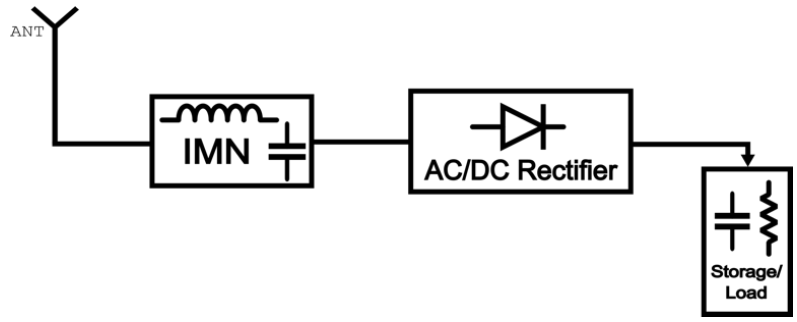

Figure 3.1: Conceptual block diagram of an RF energy harvesting system

$$P_{AV} = P_T G_T G_R \left(\frac{c}{4\pi df}\right)^2 \tag{3.1}$$

where P_{AV} is the available power received, P_T is the transmitted power, G_T is the gain of the transmitting antenna, G_R is the gain of the receiving antenna, d is the distance between the receiver and the transmitter, and f is the frequency of operation and c is the speed of light. Equation (3.1) reflects how the system responds based on the transmitted

power, the transmitting and receiving antennas' gains, the frequency of operation and the distance [5]. Equation (3.1) has two degrees of freedom, the amplitude, and the phase. The incoming wave amplitude or phase can be constructively employed to increase the system efficiency. This paper focuses on the idea of the phase integration to the rectifier side.

The antenna of the RFEH can be single ended or differential based on the rectifier type [7]. Several types of antennas can be used based on the application. For example, metamaterial antenna [8], multiport pixel antenna [9], and planar antenna array [10] have been reported. The matching network can be a π, T or L matching network based on the application [11]. The radiofrequency rectifier can be a Dickson charge pump [12], a cross-coupled rectifier [13], or a voltage multiplier [14],...etc. The power management unit adapts the RFEH system to environmental conditions such as the available power and to the application requirements such as the required voltage, run time and power dissipated [15]. Radiofrequency energy harvesters can be used in several applications, such as sensor nodes [16], implanted devices [17], and IoT applications [20].

Two main definitions of RFEHs need to be addressed. The first is sensitivity, which is the lowest RF power that can be harvested and converted into usable DC power with 1 V at the output. The second important definition is the power conversion efficiency (PCE) which is the ratio of DC output power (P_{OUT}) obtained from the available power (P_{AV}). It can be calculated using the system

efficiency (η_{RFEH}) formula that can be broken down into three terms: the matching network efficiency ($\eta_{Matching\ Network}$), the rectifier efficiency ($\eta_{Rectifier}$), and the power management unit (PMU) efficiency (η_{PMU}) as follows [6]:

$$\eta_{RFEH} = \frac{P_{OUT}}{P_{AV}} = \eta_{Matching\ Network} \times \eta_{Rectifier} \times \eta_{PMU} = \frac{V_{OUT}^2}{R_L \times P_{AV}} \quad (3.2)$$

where V_{OUT} is the output voltage, and R_L is the load resistance.

For the radiofrequency energy harvester to work optimally, the rectifier forward ON resistance, the input capacitance, and the reverse leakage current should be kept as small as possible [27]. Schottky diodes are considered one of the best available options in this regard. The high output voltage and the good efficiency are needed to best serve IoT applications. As mentioned previously, several conventional types of rectifiers can be used for RFEH. For instance, voltage multipliers and CMOS cross-coupled differential rectifiers are popular solutions. The most used voltage multipliers are Greinacher doubler and Dickson charge pumps [28]. Conventional rectifiers inherit some limitations due to their high R_{on} resistance and reverse leakage current. In addition, they are usually not compatible with different types of harvesters such as those for thermal and vibrational energy since they have low efficiency and output voltage to power on different circuits [6]. Several techniques were used to improve the performance of conventional rectifiers. The first common technique relies on threshold voltage compensation techniques since V_{th} is one of the main limitations that reduce the harvester efficiency [33]. The second common approach uses ultra-low power diodes (ULPD) [34]. The third approach employs gate/ body biasing [22]. Unfortunately, all these techniques usually add complications to the design and are also restricted to the rectifiers' theoretical limits.

In this paper, we introduce a reliable high efficiency wide input range RF energy harvester for IoT sensors. The design is based on a three-phase rectifier topology which is being presented for the first time for RFEHs. The author proposes not only a novel RF energy harvester design approach, but also a new design methodology that opens the door for real improvements in the efficiency of RFEHs.

The paper is organized as follows: Section II presents the proposed RFEH system tackling its different parts such as the phase shifter, the matching network, and the rectifier design. Section III

describes the implemented prototype, the measurement setup, and the results obtained along with the performance summary. Section IV concludes by summarizing our main findings.

3.3 Proposed Three-phase RFEH Design

Three-phase rectifier is commonly used in AC/DC power converters due to its high-power conversion efficiency [44], [45]. This type of rectifier can reach efficiency up to 99.7% making it a good candidate for full wave rectifiers since it delivers higher power into the load than single phase rectifier [46]. In addition, they do not require additional complex rectification blocks since they have a lower ripple factor. The only obstacle to making them suitable for radiofrequency energy harvesters is that they require a three-phase power supply instead of differential or single ended sources commonly used in radiofrequency harvesters.

To tackle this problem, the author is proposing different approaches to generate the required phases as shown in Figure 3.2a and Figure 3.2b. In Figure 3.2a, a single antenna feeds input power into n paths; each one is combined with a phase shifter to provide the required phase shift for the rectifier. In Figure 3.2b, an antenna array with a phase shifter in each path is implemented to feed the rectifier such as in the case of Butler matrices. Multi-port antennas could be suitable for this implementation as well. After that, each path is attached to a matching network to ensure maximum power transfer between each path and the rectifier. The voltage is measured at the output as the difference between the two output terminals.

This paper focuses on the first scheme. We scrutinize this one with n equal to 3 and show its performance and capabilities leaving exploration of other configurations for future work.

3.3.1 Phase Shifter Design

The phase shifter can be considered as a transmission line that has a certain physical length and width. In a physical sense, it is composed of a ground plane, a substrate with a relative dielectric constant ε_r, and a conducting metal. At the desired frequency (f), the length of the metal (l) corresponds to a phase ($\emptyset$) in the angular domain or a delay in the time domain from the input signal as follows [47]:

$$\emptyset = \sqrt{\varepsilon_r k_0 l} \qquad where \quad k_0 = 2\pi f/c \tag{3.3}$$

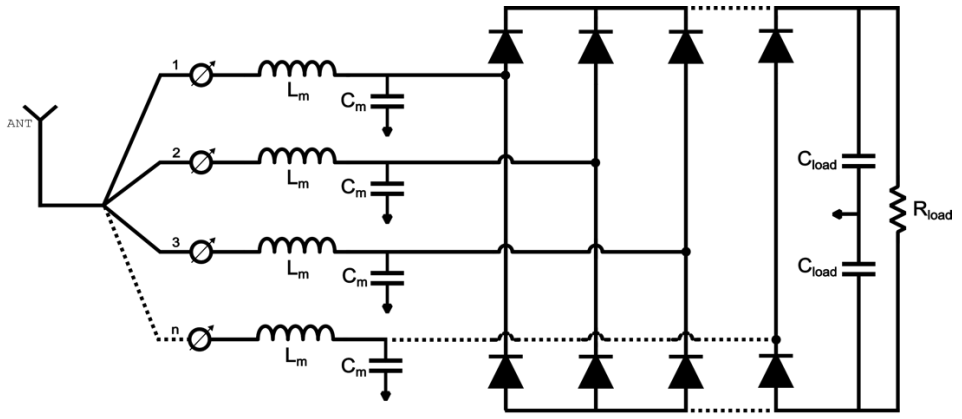

Figure 3.2a: n- phase single antenna radiofrequency energy harvesting circuit diagram

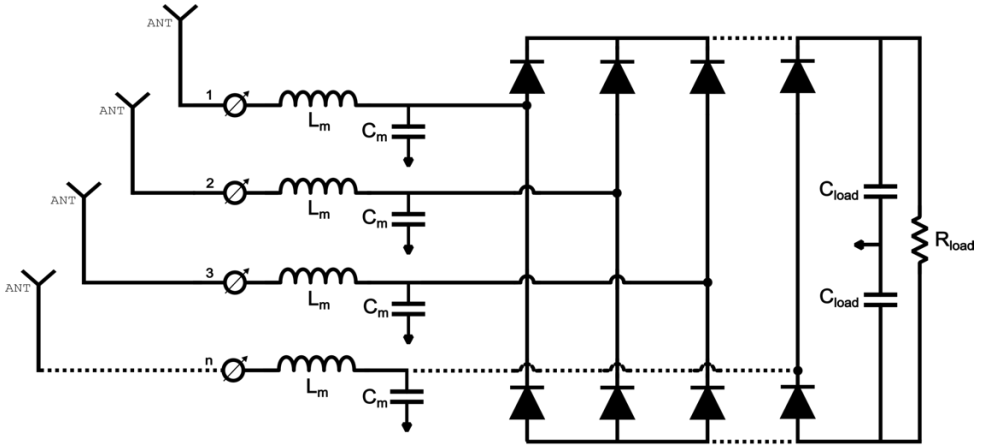

Figure 3.2b: n-phase antenna array radiofrequency energy harvesting circuit diagram

Each phase shifter acts as an arm that controls the shift angle. The phase shifter is required to split the power equally to the three branches and generates three phases of the input signal as follows 120°, 240°, 360°. All these branches are matched to an output impedance of $\sqrt{n}\,Z_0$ based on Wilkinson power divider formula where n is the number of branches and Z_0 is the characteristic impedance of the line [48]. This is the same impedance value set for the input of the matching network. The phase shifter shown in Figure 3.3 is optimized using Agilent Advance Design System (ADS) software to balance the phase and the power. The design parameters used in the simulations are summarized in Table 3.2. The footprint has a total estimated area of 4.5 cm × 3.5 cm.

TABLE 3.2
ADS DESIGN PARAMETERS OF THE PHASE SHIFTER

Parameters	Values
Substrate Material Name	RT/Duroid® 5880
Dielectric Constant (ε_r)	2.2
Substrate Thickness	0.127 mm
Impedance Termination at the Input	50 Ω
Impedance Termination at the Output	86.6 Ω

3.3.2 Matching Network Design

The matching network is very critical in radiofrequency energy harvesters design since it is the block responsible for boosting the amplitude of the small input signal to a level where the rectifier can work. From [49], the antenna voltage (V_{ANT}) can be expressed as:

$$V_{ANT} = \sqrt{8 \times Z_{ANT} \times P_{AV}} \tag{3.4}$$

where Z_{ANT} is the antenna impedance.

The voltage at the rectifier input (V_{REC}) is related to the antenna voltage (V_{ANT}) using the voltage gain boost ($A_{V,boost}$) provided by the L matching network as follows:

$$A_{V,boost} = \frac{V_{REC}}{V_{ANT}} = \sqrt{\frac{Z_{REC}}{Z_{ANT}}} = \sqrt{Q^2 + 1} \cong Q \tag{3.5}$$

For $Z_{REC} \gg Z_{ANT}$, where Z_{REC} is the input impedance of the rectifier, and Q is the quality factor of the L-matching network.

This shows how critical the quality factor of the network and the input impedance of the rectifier are to the gain boost. To match the power, L-matching network configuration is chosen as shown in Figure 3.4.

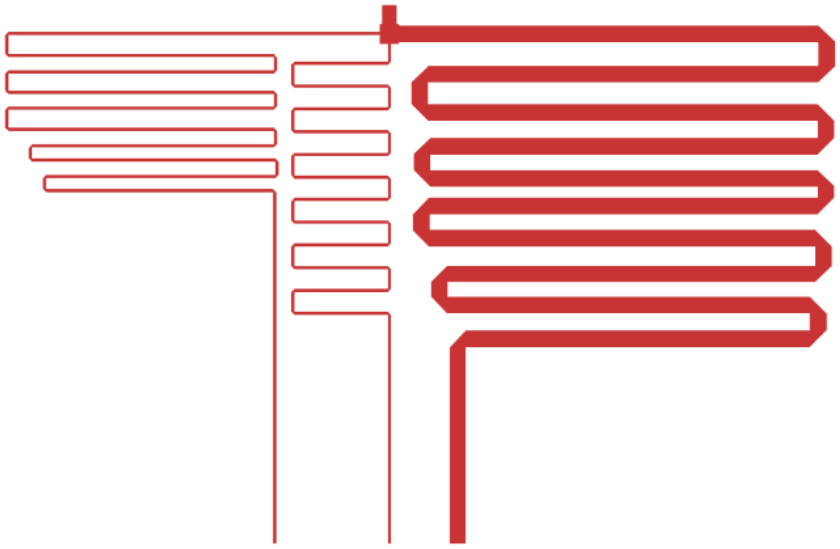

Figure 3.3: The three-phase shifter footprint

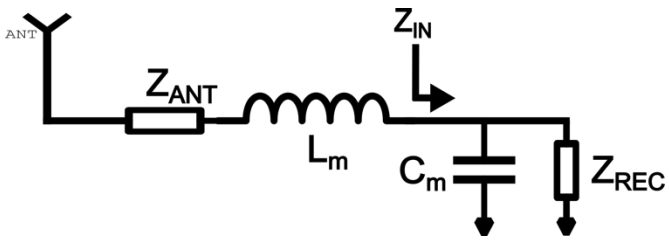

Figure 3.4: L-matching network configuration

In designing an L-matching network, the objective is to make $Z_{IN} = Z_{ANT} - jX_{L_m}$.

where X_{L_m} is the matching inductor reactance.

Also, Z_{IN} can be written as:

$$Z_{IN} = \frac{Z_{REC}(jX_{C_m})}{Z_{REC}+jX_{C_m}} = \frac{Z_{REC}X_{C_m}^2}{Z_{REC}^2+X_{C_m}^2} + j\frac{Z_{REC}^2X_{C_m}}{Z_{REC}^2+X_{C_m}^2} \quad (3.6)$$

where Z_{IN} is the input impedance seen after the matching inductor, X_{C_m} is the matching capacitor reactance.

Then from (6), we can deduce:

$$Z_{ANT} = \frac{Z_{REC} X_{C_m}^2}{Z_{REC}^2 + X_{C_m}^2} \quad \& \quad X_{L_m} = -\frac{Z_{REC}^2 X_{C_m}}{Z_{REC}^2 + X_{C_m}^2} \tag{3.7}$$

Rearranging these terms, one can show that:

$$\frac{Z_{ANT}}{Z_{REC}} = \frac{1}{\left(\frac{Z_{REC}}{X_{C_m}}\right)^2 + 1} \quad \& \quad -\frac{X_{L_m}}{Z_{ANT}} = \frac{Z_{REC}}{X_{C_m}} = Q \tag{3.8}$$

Therefore, $Q = \sqrt{\frac{Z_{REC}}{Z_{ANT}} - 1}$ which agrees with the gain boost formula of (5). As a result, knowing Z_{REC} at a certain load and input power level can lead to good matching given that the equivalent quality factor of the network is less than the maximum allowable quality factor of the network components.

3.3.3 Three-Phase Rectifier Design

Three-phase rectifier design is based on three diode branches. Each branch is connected to equal input power and a 120° phased signal. To understand the operation of this rectifier, a three-phase rectifier efficiency derivation is presented. At the rectifier terminals, and for simplicity, we assume the power is divided equally by three at each 120° of the cycle 2π, and assuming no losses due to reflection or transmission in the phase shifter:

$$P_1 = v_1(\theta) \times i_1(\theta) \tag{3.9}$$

where $v_1(\theta) = \sqrt{3} V_1 \sin(\theta)$

$$P_1 = P_2 = P_3 = \frac{P_{AV}}{3} = \frac{1}{3} v_{ANT} \times i_{ANT} \tag{3.10}$$

$$i_{ANT} = i_1 + i_2 + i_3 \tag{3.11}$$

The rectification element is based on Schottky diode, with V_{on} represents the main losses in the element, as a result, $V_{OUT} = V_1 - V_{on}$ [50, 51].

At the output of the rectifier:

$$P_{OUT} = v_{OUT} \times i_{OUT} \tag{3.12}$$

$$v_{OUT} = \frac{3}{\pi}\int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} \sqrt{3}(V_1 - V_{on})\sin(\theta)d\theta = \frac{3\sqrt{3}}{\pi}(V_1 - V_{on}) \tag{3.13}$$

And subsequently:

$$i_{OUT} = \frac{3\sqrt{3}}{\pi} I_1 \tag{3.14}$$

At the input of the rectifier:

$$P_{in_{REC}} = v_{rms_{REC}} \times i_{rms_{REC}} \tag{3.15}$$

$$v_{rms_{REC}} = \sqrt{\frac{3}{\pi}\int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} (\sqrt{3}V_1 \sin(\theta))^2 d\theta} = 1.659V_1 \tag{3.16}$$

And subsequently:

$$i_{rms_{REC}} = 1.659I_1 \tag{3.17}$$

And the rectifier efficiency can be expressed as:

$$\eta_{REC} = \frac{P_{OUT}}{P_{in_{REC}}} \tag{3.18}$$

To further explore the advantage of using such type of rectifiers, an example of the efficiency is provided with practical values extracted from the literature and the measurements. When the conduction current of Skyworks SMS7621-005LF Schottky diodes is expressed as (i_d), the diode equation can be written as:

$$V_{on} = nV_T\, ln(\frac{i_d}{I_s} + 1) \tag{3.19}$$

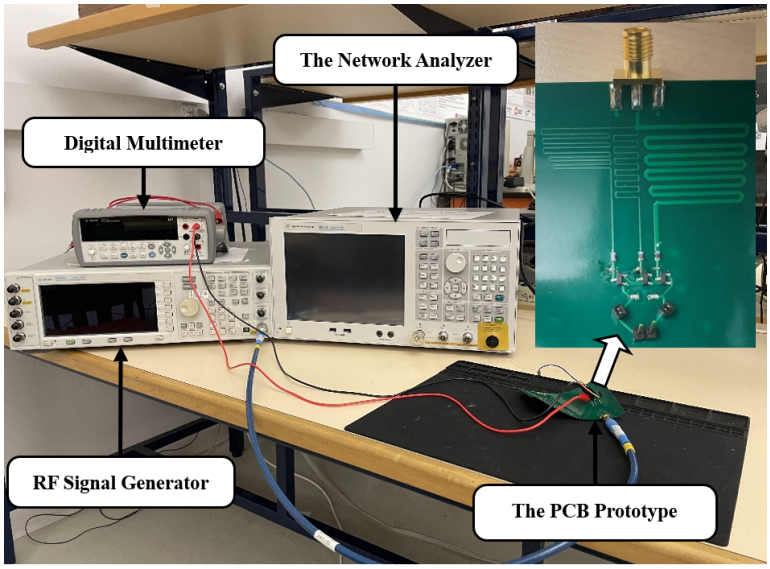

Figure 3.5: The measurement setup with the prototype shown on the top right corner

where I_s is the saturation current, V_T is the thermal voltage and n is the emission coefficient. Based on the parameters available in the market, at $i_{OUT} = 1\ mA$, one can find that $V_{on} = 0.28\ V$ [52].

At peak PCE of our RFEH, $v_{OUT} = 5.8\ V$ and $i_{OUT} \approx$ 1 mA , the efficiency of the rectifier can be calculated as:

$$\eta_{REC} = \frac{P_{OUT}}{P_{in_{REC}}} = \left(\frac{3\sqrt{3}}{\pi}(V_1 - V_{on}) \times \frac{3\sqrt{3}}{\pi} I_1\right) \div (1.659V_1 \times 1.659I_1) = 94.4\ \% \qquad (3.20)$$

Which represents the upper efficiency limit of the rectifier of our RFEH.

3.4 Experimental Results and Discussion

3.4.1 Implemented Prototype

The design is implemented using Skyworks SMS7621-005LF Schottky diodes which is one of the best choices for discrete diode components for RF energy harvesters due to low leakage and drop voltage. The matching network components chosen are listed in table 3.3:

TABLE 3.3
THREE PHASE RFEH PROTOTYPE COMPONENT VALUES

Component	**Value**
Matching Network Inductor	56 nH
Matching Network Capacitor	0.33 pF
Load Capacitor	1 pF
Diode Pair Used	SMS7621-005LF

The matching network inductor is from Coilcraft 0603HP with a quality factor greater than 60 and the matching capacitor is from Murata Electronics with a quality factor over 400 and their values are carefully chosen to minimize the losses at the ISM band. A female socket is used for the load and headers are soldered to measure the output voltage at different loads.

3.4.2 Measurement Setup

The measurement setup is shown in Figure 3.5. The measurements were performed with a single-tone sinusoidal wave RF signal generator (E443BC Agilent Keysight) with a 50 Ω output impedance as an RF source. A network analyzer (E5071C Agilent Technologies) is used to characterize the input impedance and the S_{11} parameter for different frequencies and available input power. To measure the output and characterize the performance, a digital multimeter (34411A Agilent Keysight) and an Oscilloscope (RTM3004 ROHDE & SCHWARZ) are used for this purpose since they provide accurate and reliable measurements.

3.4.3 Measurement Results

Figure 3.6 shows the S_{11} parameter versus the available input power. The input power range is from -20 dBm to 15 dBm. The S_{11} parameter gets to the bottom at 0 dBm with -47 dB, and the highest value is at -20 dBm with -8 dB. This shows that the impedance matching achieves the maximum power transfer at 0 dBm and in general, the reflections are kept at a minimum level. The output voltage is measured at different load conditions. The load values are chosen based on the most recent sensor node equivalent impedance available in the literature. The system is optimized to deliver the maximum power transfer over this load range.

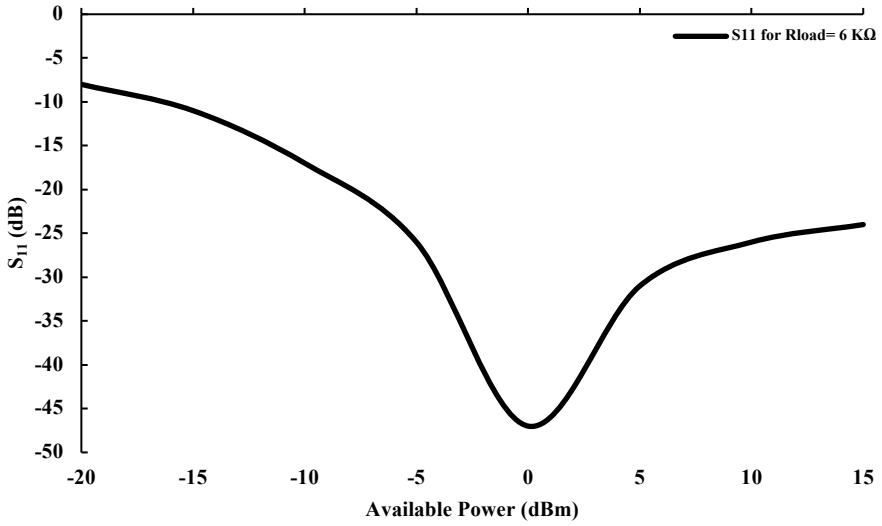

Figure 3.6: Measured S_{11} parameter versus the available power at 435.6 MHz

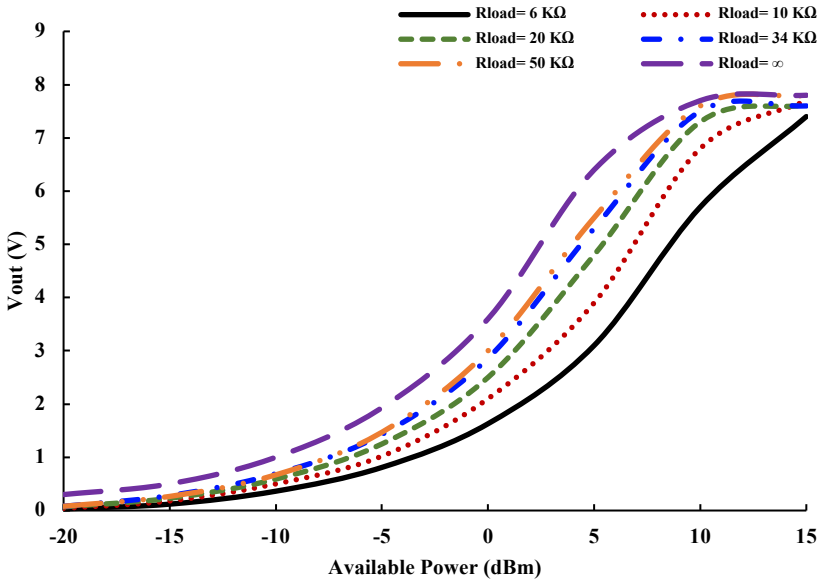

Figure 3.7: Measured output voltage versus the available power for different load conditions

Figure 3.7 shows the output voltage when the available power varies from -20 dBm to 15 dBm. The open circuit voltage peaks around 10 dBm with 7.9 V. The minimum detectable voltage is 0.3 V at -20 dBm. The system shows a sensitivity of 1 V at available power of -10 dBm. When a load is

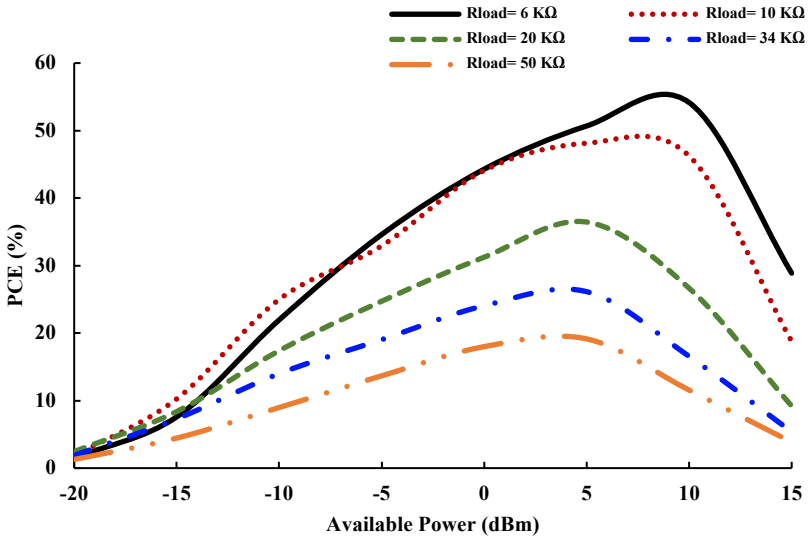

Figure 3.8: Measured power conversion efficiency (PCE) versus the available power for different load conditions

connected to the output side, it is expected that the higher the resistance value, the higher the output voltage. This is characterized by measuring the harvester response for different load conditions, 6 KΩ, 10 KΩ, 20 KΩ, 34 KΩ, 50 KΩ to give an insight into the intrinsic performance of the rectifier.

The overall power conversion efficiency as a function of the available input power is reported in Figure 3.8 for the same load conditions. From the graph, the maximum power transfer occurs at a load of 6 KΩ, with a peak power conversion efficiency of 56% end to end. Not only does this rectifier provide high efficiency, but it also delivers it with high output current load. The lower efficiency at a small input power level is mainly due to the 320 mV V_{on} of the diodes. The efficiency curve keeps rising for different loads up to 5 dBm input power, where the leakage starts dominating, and the efficiency curve changes direction. The S_{11} parameter also influences the behavior of the PCE curve, which will be studied next. From these sets of curves, the maximum efficiency versus the input power level across different loads can be drawn as in Figure 3.9 to give an insight into the range over which this RFEH has a high efficiency. This figure shows that a remarkable PCE of over 20% is obtained over a wide range of input power that spans from -12 dBm to 17 dBm. This wide range (29 dBm) of high efficiency makes the proposed design RFEH ideal for sensor nodes

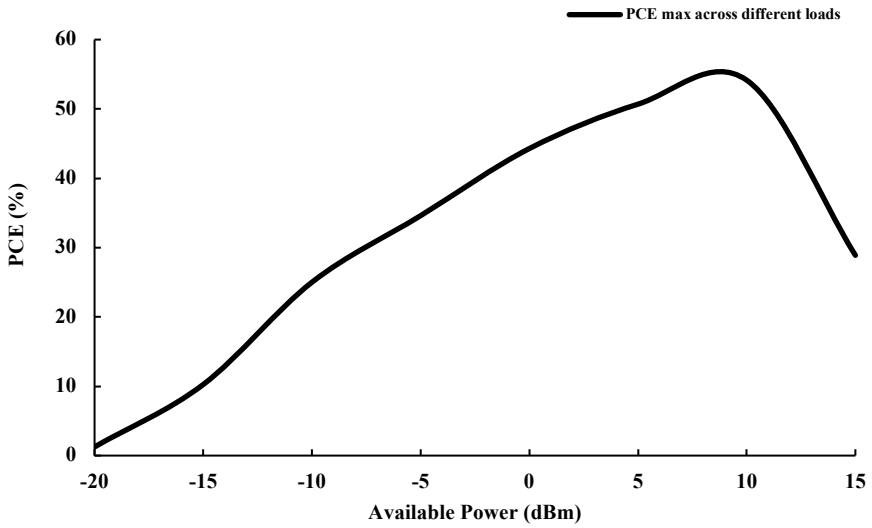

Figure 3.9: Measured maximum power conversion efficiency (PCE) versus the available power

operating in environments where the input power level fluctuates due to the distance and the strength of the signal.

Since the PCE and S_{11} parameter are related, Figure 3.10 gives an insight into the effect of the S_{11} parameter on the behavior of the energy harvester. At low input power levels, the S_{11} parameter has a high value but at the same time, the rectifier has a V_{on} that imposes a floor for the RFEH to start operating. Above the sensitivity floor of the RFEH, as the available power increases, the S_{11} parameter decreases which means that the reflection losses are lower, and more power is transferred from the source to the load. At high input power levels, the current leakage becomes critical and eventually the PCE starts decreasing. The reported S_{11} parameter curve proves that the rectifier is well-matched to the source in the ISM band with acceptably small reflections over a wide input power range.

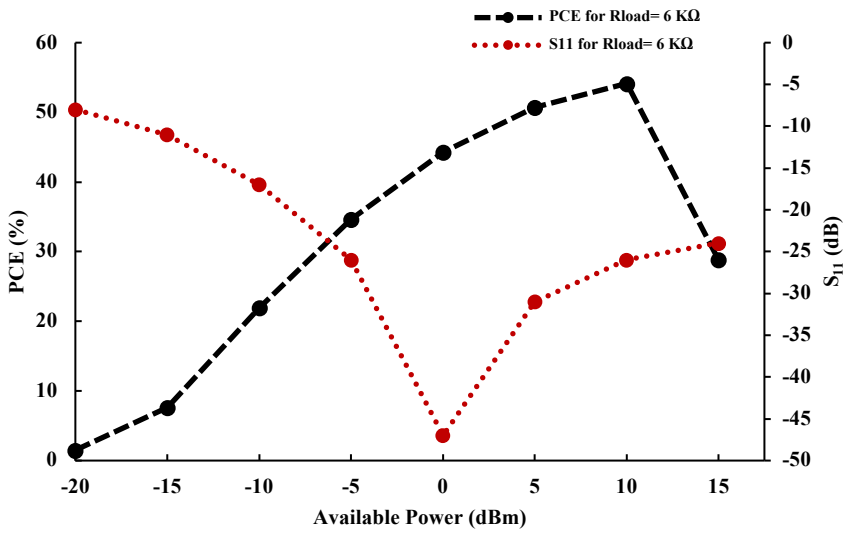

Figure 3.10: Measured power conversion efficiency and S_{11} parameter versus the available power for R_{load}= 6 kΩ

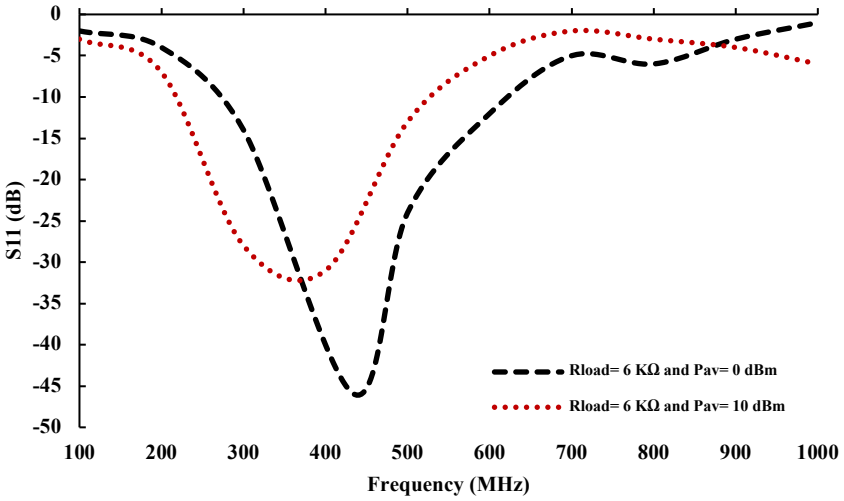

Figure 3.11: Measured S_{11} parameter versus the frequency of operation for R_{load}= 6 kΩ and P_{AV}= 0, 10 dBm

Figure 3.11 indicates the S11 parameter versus frequency of operation from 100 MHz to 1GHz for R_{load}= 6 kΩ and 0, 10 dBm available power. The S_{11} parameter reaches the minimum at 0 dBm with -47 dB. When the available power increases to 10 dBm, the curve shifts a little to the left and

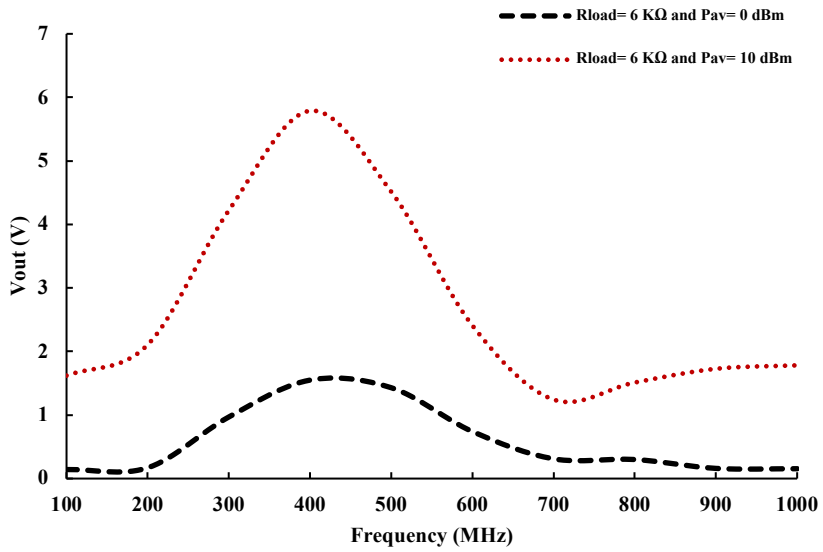

Figure 3.12: Measured output voltage versus frequency of operation for R_{load}= 6 kΩ and P_{AV}= 0, 10 dBm

reaches -31 dB at a frequency of 350 MHz. The frequency response in general indicates that the system resonates well around 400 MHz band.

Figure 3.12 reports the output voltages as a function of the frequency of operation from 100 MHz to 1 GHz. This figure is measured for R_{load}= 6 kΩ and 0, 10 dBm available power. In the case of 0 dBm, the output voltage peaks around 1.6 V for frequencies between 400 MHz and 450 MHz. For 10 dBm, the output voltage is around 5.6 V for frequencies between 400 MHz and 450 MHz.

Figure 3.13 shows the power conversion efficiency versus frequency of operation for R_{load}= 6 kΩ and 0, 10 dBm available power. The PCE is around 40% for frequency range between 400 MHz and 450 MHz for R_{load}= 6 kΩ and 0 dBm. The PCE stays above 20% from 330 MHz to 550 MHz for the same conditions. At 10 dBm, the system achieves the highest PCE of 56% in a frequency range between 400 MHz and 450 MHz while keeping a PCE above 20% from 280 MHz to 550 MHz. The RFEH system still supplies significant output voltages for different frequencies in case this designated band is not available. The PCE curve shifts to the left since the S11 parameter shifted to lower frequencies as the input power increases from 0 dBm to 10 dBm.

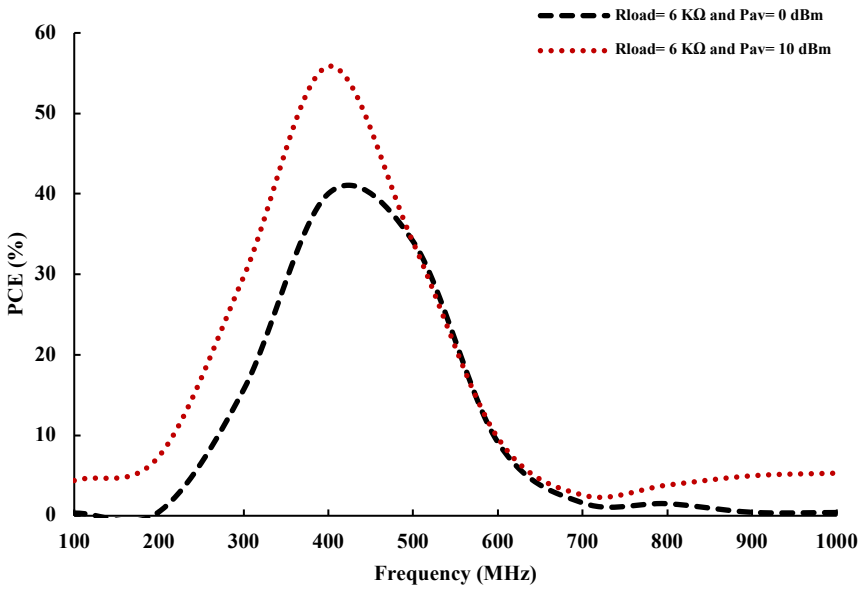

Figure 3.13: Measured power conversion efficiency (PCE) versus frequency of operation for R_{load}= 6 kΩ and P_{AV}= 0, 10 dBm

3.4.4 Performance Summary

Performance summary and comparison with the state-of-the-art are presented in Table 3.4. The performance is discussed from the technology, the frequency of operation, the additional requirements, sensitivity, and the power conversion efficiency perspectives. RFEHs can be implemented using discrete components or CMOS technology. In the proposed design, SMS7621 diodes are used, and compared to previously reported design solutions. As indicated, the design shows a high end-to-end peak PCE of 56% compared to the literature. Power conversion efficiency can be further improved by choosing better diodes or using CMOS techniques to decrease the leakage. The system shows a wide input power range for PCE > 20% over a 29 dB input power range, which is the highest compared to the prior work as indicated in the table. It allows the design to work in environments where the signal is fluctuating.

The design also has a good sensitivity of -10 dBm, which could be improved by using more sensitive diodes or native transistors. The frequency response of the design is studied to show the performance over different frequency bands. The design shows good matching condition in the frequency band from 280 MHz to 550 MHz with the S_{11} parameter reaching the minimum at 0 dBm with -47 dB. The output voltage is reported along with the efficiency versus frequency of

operation and it indicates that the system operates over a wide frequency range. This design proves through this first prototype that it can be reliable and provide good performance.

3.5 Conclusion

In this paper, the author presented a new RFEH design that exploits the different locally generated phases of the input signal to deliver high power efficiency at the output. This technique has never been reported before in the field of RF-DC converter. The input signal is split equally in magnitude to three paths shifted in phase by 120°. Each path is then matched to one rectifier branch using an L-matching network to ensure maximum power transfer. The rectifier diodes are Schottky diodes SMS7621 from Skyworks. These diodes are suitable for sensitive RF applications as they provide relatively low forward voltage drops and minimum leakages. The phase shifter, the matching network and the rectifier are analyzed. A PCB demonstration prototype is fabricated on RT/Duroid® 5880 Laminates substrate with 0.005 inches thickness to ensure minimum dielectric losses. The prototype shows promising results in the 435.6 MHz ISM band. The RFEH system achieves a high efficiency of 56% at 6 kΩ with a 5.2 V output voltage. It also maintains a good efficiency higher than 20% over a wide input power range of 29 dB. The harvester sensitivity is 1 V at -10 dBm. The frequency response of the system exhibits the resonance around the ISM band. Thanks to low S_{11}, the system keeps a good efficiency and output voltage over a wide frequency range from 280 MHz to 550 MHz. All these performance metrics make this system attractive for SoCs and IoT applications. In addition, it uses low-cost components and is easy to tune while delivering high performance, which makes it suitable for mass production. According to the authors' knowledge, this is the first RF energy harvester that integrates more than two phases (differential phases) in a RFEH design. Based on the results obtained from this proof of concept, the authors believe that three or four-phase designs are very promising in terms of performance. This area has not yet been explored in literature and future work can be performed to further analyze and optimize more design configurations.

TABLE 3.4
PERFORMANCE SUMMARY AND COMPARISON

Reference	**This Work [2023]**	**[53] [2021]**	**[54] [2018]**	**[14] [2017]**	**[55] [2015]**	**[56] [2013]**	**[57] [2013]**	**[58] [2013]**
Technology	SMS7621	0.18 µm	0.18 µm	0.18 µm	0.18 µm	Schottky Diodes	HSMS286C	SMS7630
Frequency	435.6 MHz	403.5 MHz	400 MHz	402 MHz	433 MHz	512 MHz	540 MHz	539 MHz
Additional System Requirements	Phase Shifter	DC-DC Converter	PMU	Control Loop	-	MCU	-	PMM
Sensitivity	-10 dBm (@ 1 V)	-24 dBm (@ 1.8 V)	-11.5 dBm	-12 dBm (@ 1.3 V)	-19 dBm (@ 1 V)	-14 dBm (@ 1.8 V)	-15 dBm (@ 1.1 V)	-8.8 dBm
Reported Input Power Range for PCE > 20% (dB)	29	15	13.5	10	10	-	8	-
Peak PCE	56% (@ 6 kΩ, 5.2 V, 8 dBm)	40.2% (@ 1.8 V, -9.1 dBm)	37% (@ 2.1 V, -8 dBm)	31.9% (@ 30 kΩ, 2.8 V, -1 dBm)	34% (@ 100 kΩ, 2 V, - 7 dBm)	19.5% (@ 1 MΩ)	45% (@ 50 kΩ, 4.2 V, - 5 dBm)	26% (@ - 18 dBm)
System Architecture	Three-Phase Rectifier	Cross Coupled Rectifier	Cross Coupled Rectifier	Dickson Charge Pump	Dickson Charge Pump	Greinacher Doubler	Dickson Charge Pump	Half Wave Rectifier

CHAPTER 4 ARTICLE 2: VARACTOR-BASED LADDER RECTIFIER RADIO FREQUENCY ENERGY HARVESTER FOR IOT APPLICATIONS

This chapter reproduces an article submitted to IEEE Transactions on Circuits and Systems on September 18[18] 2024.

- A. Refaei, S. Genevey, Y. Audet, and Y. Savaria, "Varactor-based ladder rectifier radiofrequency energy harvester for IoT applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*.

4.1 Abstract

The demand for highly sensitive energy harvesting systems is increasing, driven by the need to power modern wearable smart devices. Radiofrequency (RF) energy harvesters (RFEHs) are particularly popular due to their capability to deliver power wirelessly. This brief introduces a highly sensitive RFEH designed for ultra-low-power applications. The design incorporates a novel varactor-based ladder rectifier, a first in RFEHs, to reduce the input capacitance at low input power levels. It is fabricated using the GF FDX 22 nm technology and operates in the GSM band at 990 MHz. The rectifier, with two stages, has an effective area (excluding pads) of 0.002 mm². The chip is wire-bonded to a CQFP44 package, mounted on a PCB made from RT/Duroid® 5880 laminates substrate with a thickness of 0.005 inches to minimize dielectric losses. The prototype achieves an impressive end-to-end sensitivity of 1 V at -22.5 dBm. Additionally, the system demonstrates a peak power conversion efficiency (PCE) of 26% at -13 dBm when driving a 50 kΩ load, making it not just suitable, but highly practical for supplying ultra-low-power devices.

4.2 Introduction

In contemporary living, the widespread adoption of IoT systems and intelligent devices are evident. There is a growing reliance on these technologies to provide seamless features that help people to be more productive. To sustain the functionality of Internet of Things (IoT) devices, it is essential for the system to incorporate either a replaceable battery or an energy harvesting

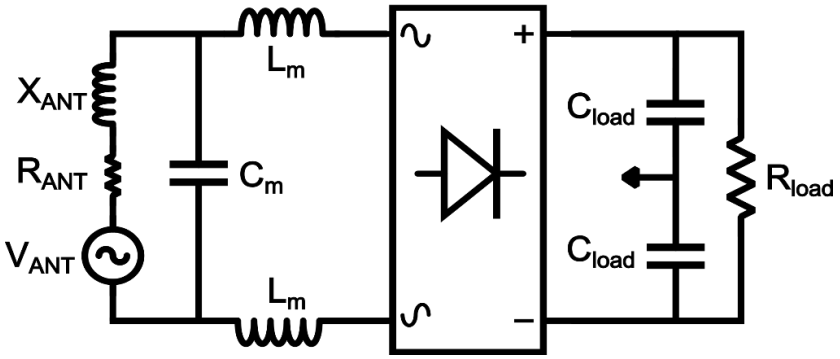

Figure 4.1: Block diagram of a typical RF energy harvesting system

mechanism. Various types of harvesters can convert energy from sunlight, vibrational, thermal, and radiofrequency sources. This brief aims to develop an energy harvester to convert ambient radiofrequency electromagnetic waves to usable DC power. Radiofrequency energy harvesters (RFEHs) typically have five main components: a receiving antenna, an impedance matching network (IMN), a rectification block, a storage element, and a load, as illustrated in Figure 4.1.

The antenna receives incident RF power available in the environment within a certain frequency range. It can be either single-ended or differential [7]. Then, it passes the AC signal to the matching network. The matching network ensures that the rectifier input impedance is matched to the antenna impedance with maximum power transfer [11]. The rectifier converts the AC signal to a DC signal to be stored or consumed by the load. It can be a Dickson charge pump [12], a cross-coupled rectifier [13], a voltage multiplier [14],...etc.

Conventional RFEHs suffer from high forward ON resistance, input capacitance and reverse leakage current [28]. The boost gain ($A_{V,boost}$) can be defined as the ratio between the rectifier input voltage (V_{REC}) and the antenna voltage (V_{ANT}) as follow:

$$A_{V,boost} = \frac{V_{REC}}{V_{ANT}} \tag{4.1}$$

According to [35], when $X_{REC} \gg R_{REC}$ and the interface is at resonance, $X_{REC} = X_{ANT}$, it holds that:

$$A_{V,boost} \approx \frac{X_{REC}}{R_{ANT}+R_{REC}} \tag{4.2}$$

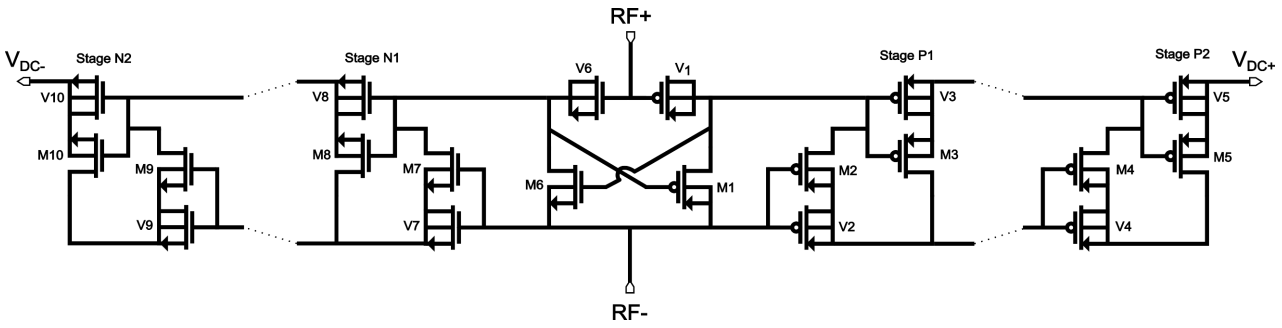

Figure 4.2: Schematic of multi-stage varactor-based ladder rectifier, transistors labeled with 'V' are varactors.

where X_{REC} is the rectifier input impedance, X_{ANT} is the antenna input impedance, R_{REC} is the rectifier input resistance, and R_{ANT} is the antenna input resistance.

Combining these two equations, the minimum available power (P_{AV}) can be expressed as:

$$P_{AV} = \left(\frac{R_{ANT} + R_{REC}}{X_{REC}}\right)^2 \frac{V_{REC}^2}{8R_{ANT}} \tag{4.3}$$

This equation shows that reducing the rectifier's input capacitance can significantly improve the system's sensitivity.

Additionally, rectifiers often lack compatibility with various harvester types such as thermal and vibrational systems because of their inability to generate sufficient power for diverse circuits [4]. Numerous techniques have been employed and investigated to enhance the performance of conventional rectifiers. Authors in [33] introduced a technique to compensate for the rectifier's forward drop voltage. The second common strategy is the utilization of ultra-low power diodes (ULPD) to decrease the leakage current in the reverse operation [34]. The third approach involves gate/body biasing [22]. Regrettably, these techniques tend to introduce additional design complexities to the system and are constrained by the theoretical limits of rectifiers.

This brief introduces a robust and highly sensitive RF energy harvester designed for IoT applications. The design is based on a varactor ladder rectifier design, that is introduced to RFEH for the first time. The brief's structure follows: Section II shows the proposed RFEH system, addressing the governing equations and circuit implementations. Section III details on the implemented prototype, the measurement setup, the results, and a performance summary. Finally, Section IV summarizes our main findings and the conclusion.

4.3 Proposed varactor-based ladder rectifier design

Ladder rectifiers were introduced in [59] as sub-threshold voltage rectifiers to supply orthogonal current-reuse neural amplifiers. The circuit shows a low 75 mV start-up voltage that attracted the authors' attention as a potential design for RFEHs. Ladder rectifiers consist of an input cross-coupled rectifier (CCR) cell and two ladder charge pumps (LCP), as shown in Figure 4.2. The input cell works as a full wave rectifier that uses self-threshold voltage cancellation technique to reduce the effect of turn-on voltage. The two ladder charge pumps can be decomposed into P-type and N-type cells to build the output DC voltage on complementary phase to double the rectified voltage and lower the cascaded number of stages.

Each transistor in the ladder charge pump has a MOS capacitor between its gate and source terminals that plays an essential role in the operation of this circuit. When the input increases at the positive RF cycle, the capacitor starts charging, and a current goes through the transistor from the drain to the source. The opposite occurs at the complementary negative cycle, and the other transistor is now conducting current. The resulting current is the sum of both currents at each stage. The output DC voltage and the efficiency depend on the number of stages and the losses due to leakage current. As the number of stages increases, the output voltage is boosted, but the leakage due to each transistor is also higher. A balance between the required output voltage and the leakage should be established [59].

The input capacitors and LCP caps are replaced with varactors in the proposed rectifier. The varactor has a varying capacitance Cgs based on the input voltage (Vgs) as shown in figure 4.3. As the input voltage increases, the varactor capacitance increases from 126 fF until it saturates to 3.75 pF. At low input voltage (Vgs), the varactor has a small capacitance between its terminals. This increases the system's sensitivity because the lower the input capacitance, the higher the boosting ratio and the available power that can be harvested. As the input voltage increases, increasing the capacitance can maintain a high conversion efficiency between the AC and the DC output of the rectifier. This fits perfectly with the varactor's operation, making it suitable for this circuit.

TABLE 4.1

VARACTOR BASED LADDER RECTIFIER RFEH PROTOTYPE COMPONENT VALUES

Device	**Value**
Width/Length of n-channel varactors	600 μm/100 nm
Width/Length of p-channel varactors	600 μm/28 nm
Width/Length of n-channel switches	20 μm/100 nm
Width/Length of p-channel switches	20 μm/20 nm
Matching Network Inductor	4.3 nH
Matching Network Capacitor	0.33 pF
Load Capacitor	1 pF
Balun	0900BL15C050

4.4 Experimental results and discussions

4.4.1 Implemented prototype

The proposed varactor-based ladder rectifier consists of two stages of ladder charge pump fabricated using GF FDX 22nm technology. The sizing of each transistor is summarized in Table 4.1, along with the PCB components list. Figure 4.3 shows the micrograph of the chip. The effective area, excluding the pads, is 0.002 mm^2. The chip is wire-bonded to CQFP44 package. The PCB is fabricated on RT/Duroid® 5880 Laminates substrate with 0.005 inches thickness to reduce the dielectric losses.

The inductor used in the matching network is from Coilcraft 0603HP, with a quality factor > 60. The capacitor from Murata Electronics has a quality factor > 400. Both elements were carefully chosen to minimize the losses at the GSM band.

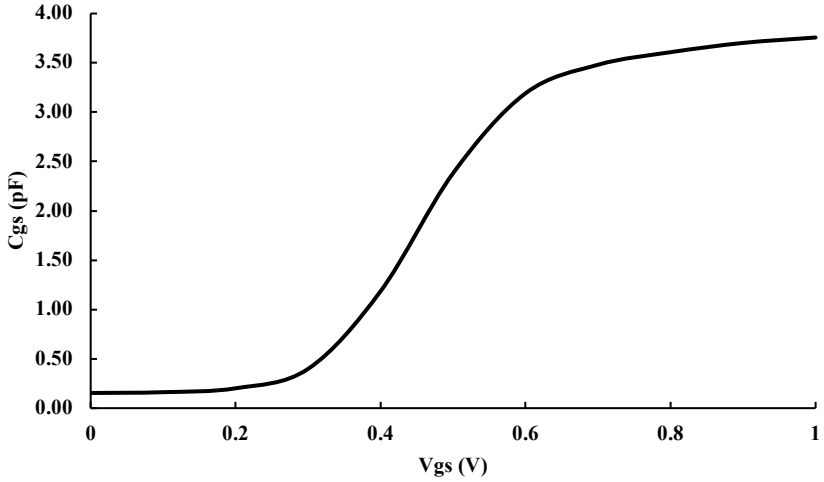

Figure 4.3: The varactor capacitance versus the input voltage

4.4.2 Measurement setup

The setup for the measurement and the micrograph of the chip are shown in Figure 4.4. Single-tone sinusoidal wave RF signal generator (E443BC Agilent Keysight) with a 50 Ω output impedance serves as the RF source. A network analyzer (E5071C Agilent Technologies) is used to characterize the input impedance and the S11 parameter for different frequencies and available power. The frequency of operation for the signal generator is set to 990 MHz. A digital multimeter (34411A Agilent Keysight) and Oscilloscope (RTM3004 ROHDE & SCHWARZ) are used to measure and characterize the output voltage.

4.4.3 Measurement results

Figure 4.5 illustrates the output voltage across the available power range from -25 dBm to -5 dBm. It is measured under varied load conditions, with the chosen load values of 50 KΩ, 20 KΩ, 15 KΩ, and 6 KΩ. The system is fine-tuned to operate within this load range, ensuring maximum power transfer efficiency. The open circuit voltage peaks at approximately -5 dBm, with 2.8 V. The lowest viable voltage is observed at -24 dBm, at which an output voltage of 0.3 V was measured, while the output voltage stands at 1 V when the input is at -22.5 dBm. When a load is connected to the output, it is anticipated that the output voltage will increase with higher resistance values. Various load conditions, including 50 KΩ, 20 KΩ, 15 KΩ, and 6 KΩ were tested to provide insights into the inherent performance of the rectifier. The system shows good matching conditions for 50 KΩ load and achieves 1.5 V for -5 dBm of input available power.

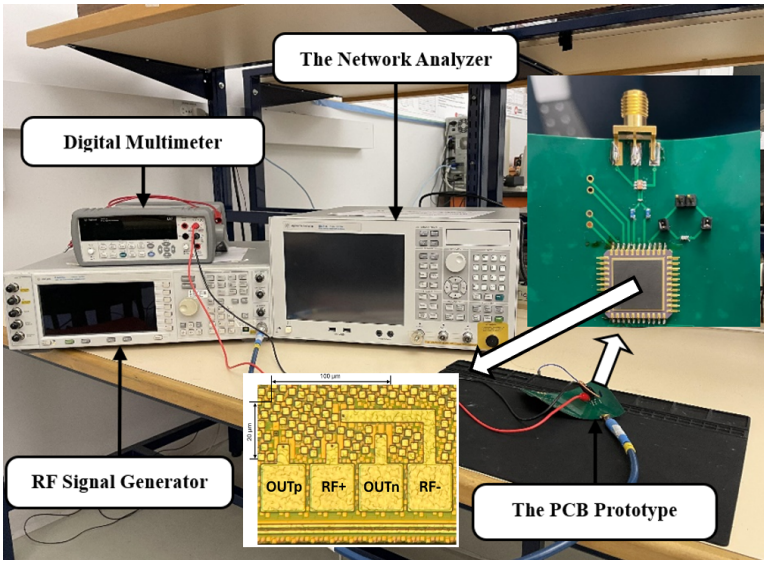

Figure 4.4: The measurement setup with the chip package shown on the top right corner

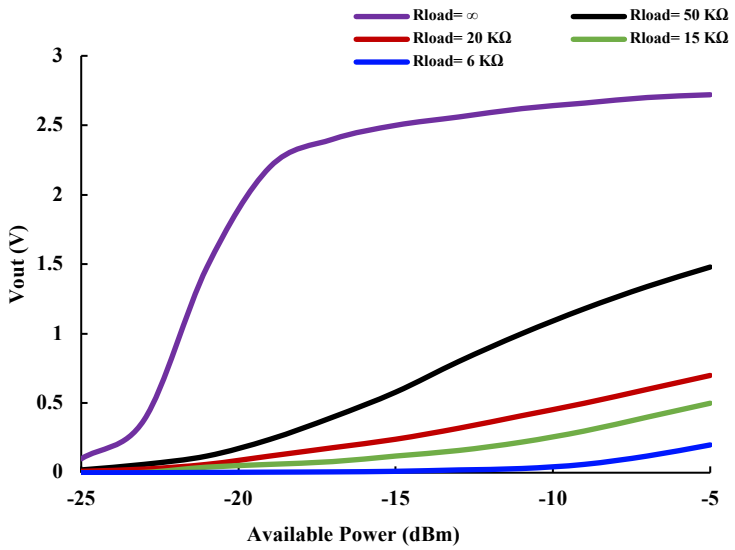

Figure 4.5: Measured output voltage of the proposed RFEH versus the available power for different load conditions

Figure 4.6 reports the overall power conversion efficiency with respect to the available power, with the same loads' conditions. According to this figure, the peak power conversion efficiency is achieved for a load of 50 KΩ, yielding an efficiency of 26% at -13 dBm. The figure provides insights into the range where this RFEH maintains high efficiency. It reveals a noteworthy PCE exceeding 20% from -15.5 dBm to -8 dBm.

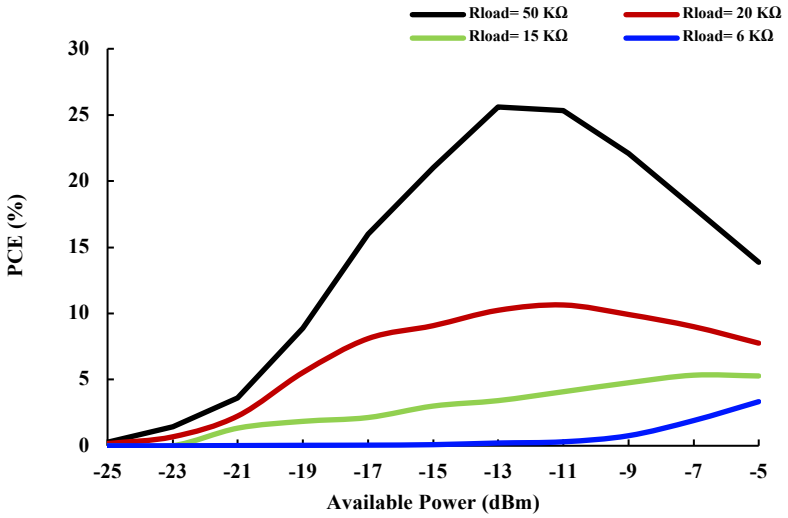

Figure 4.6: Measured power conversion efficiency (PCE) of the proposed RFEH versus the available power for different load conditions

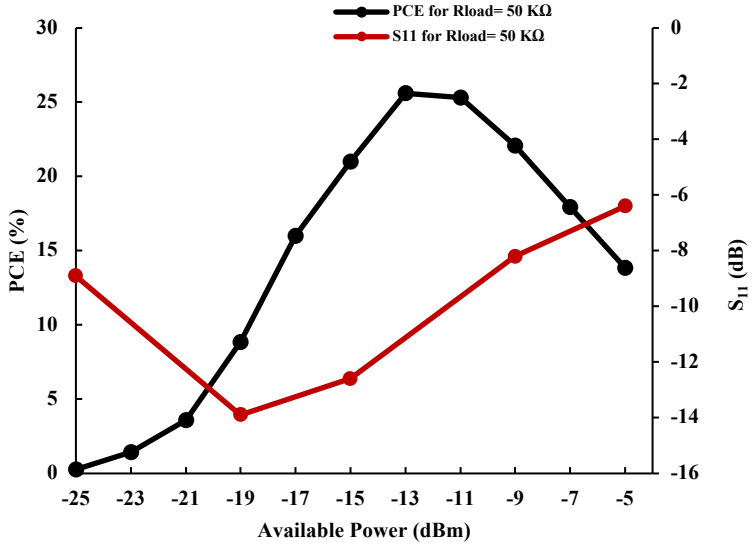

Figure 4.7: Measured power conversion efficiency and S11 of the proposed RFEH versus the available power for Rload= 50 kΩ

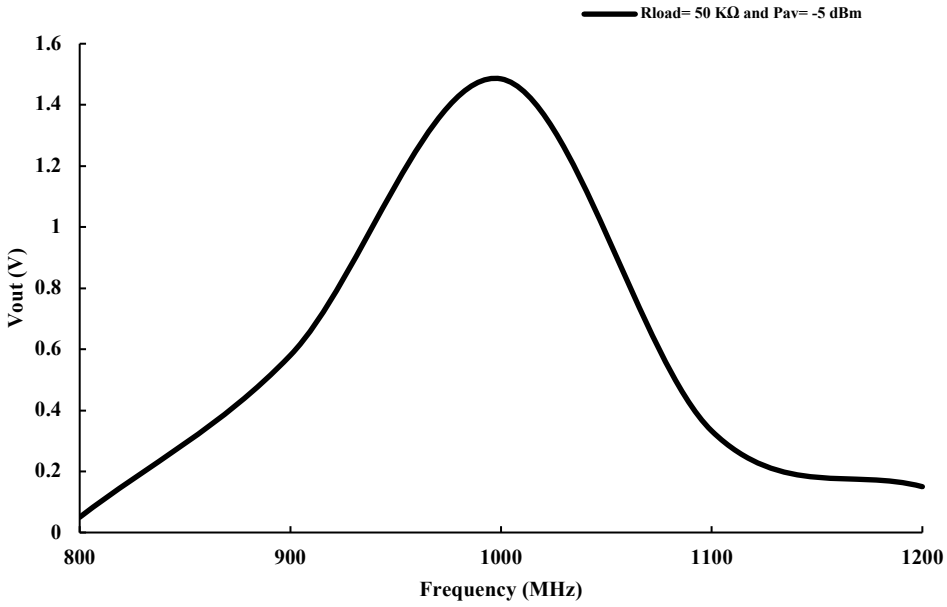

Figure 4.8: Measured output voltage of the proposed RFEH versus the frequency of operation for Rload= 50 kΩ and PAV= -5 dBm

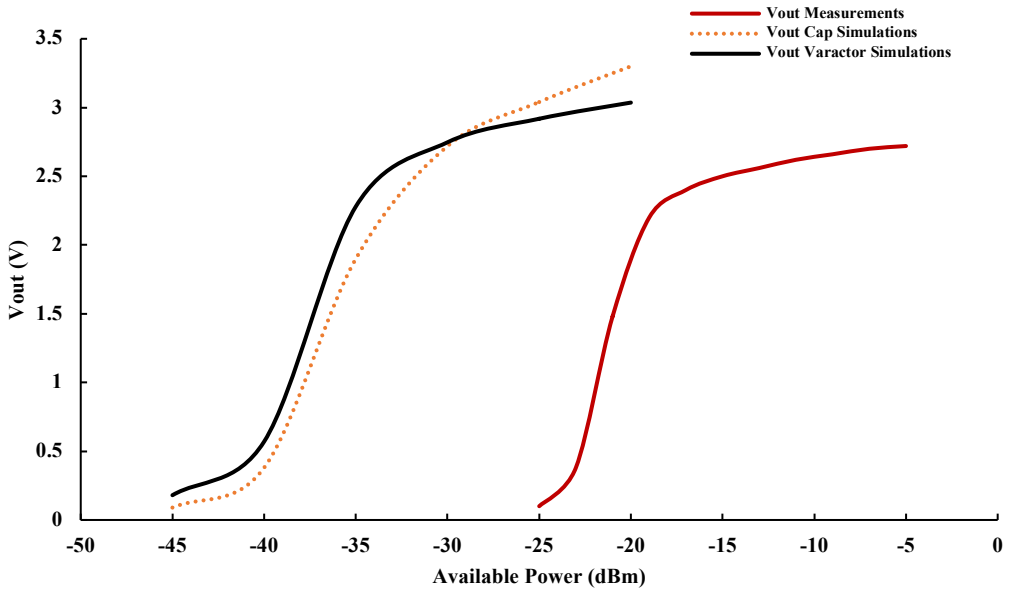

Figure 4.9: The output voltage versus the available power in simulations, for the normal capacitor, and the varactor and in measurements at open circuit condition

As the PCE and the measured S11 parameter exhibit a correlation, Figure 4.7 provides insights into how the S11 parameter influences the behavior of the RFEH. At the lowest input power levels, S11 has a value of -8.9 dB, added to the turn-on voltage of the transistors, resulting in the lowest efficiency. Afterward, S11 decreases to reach a bottom of -13.9 dB at an available power of -19 dBm, indicating reduced reflection losses and increased power transmission from the source to the load. This marks the phase where PCE begins to ascend until the S11 parameter increases again to reach -6.4 dB at -5 dBm.

In Figure 4.8, the output voltage versus the frequency of operation is illustrated within a frequency range from 800 MHz to 1200 MHz. This measurement is conducted with an Rload of 50 kΩ and an available power of -5 dBm. The output voltage reaches its highest point, approximately 1.5 V, at a frequency of 990 MHz. Moreover, the system keeps an output voltage higher than 1 V for frequencies ranging from 930 MHz to 1050 MHz.

4.4.4 Performance summary

A performance summary with a comparison of state-of-the-art technologies is presented in this section. Figure 4.9 reports the output voltage versus the available power at open circuit condition for simulations and measurements. In simulations, the design is tested using normal capacitors, and the second time using a varactor to highlight the boost in the voltage. The varactor-based design achieves a sensitivity of -39 dBm at 1 V compared to -22.5 dBm in measurements. The difference between the simulations and the measurements return to the package losses, PCB losses, and the Balun losses. The design performance can be further improved using a differential antenna or an RF source instead of a balun at the input. A smaller package could also reduce the wire bonding parasitic losses as well. Table II shows the comparison with different rectifier topologies for instance, cross-coupled, Dickson and Greinacher doubler. The design shows a notable sensitivity of -22.5 dBm at 1 V compared to the literature. Moreover, the design has a compact area of 0.002 mm^2. This makes it more integrated in multi-source systems. In addition, it has a peak PCE of 26% at the lowest available power of -13 dBm and for a load of 50 KΩ. Therefore, it exhibits more current driving capabilities at lower input RF power levels than the cited articles.

TABLE 4.2

PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE OF ART

Reference	**This Work**	**[30] 2017 TCAS-II**	**[16] 2019 JSSC**	**[31] 2019 TCAS-I**	**[32] 2017 JSSC**
Technology	GF FDX 22 nm	TSMC 65 nm	TSMC 65 nm	TSMC 130 nm	TSMC 180 nm
Topology	Varactor-Based Ladder	Cross-Coupled	Cross-Coupled	Dickson	Greinacher doubler
Frequency	990 MHz	900 MHz	2.4 GHz	896 MHz	915 MHz
Effective Area	0.002 mm^2	0.048 mm^2	0.000125 mm^2	0.053 mm^2	1.08 mm^2
Techniques	Variable capacitor	Dual-path	Parasitic aware design	VT compensation	Tuned MN
No. of Rectifier Stages	2	5	1	4	8
Additional Requirements	-	-	MPPT	-	Deep n-well
Sensitivity @ Vout and Rload	-22.5 dBm @ 1 V & ∞	-17.7 dBm @ 1 V & ∞	-17.1 dBm @ 0.4 V & ∞	-20.5 dBm @ 1 V & 1 MΩ	-14.8 dBm @ 1 V & 1 MΩ
Peak PCE & Rload	26% @ -13 dBm & 50 KΩ	34.5% @ -2 dBm & 147 kΩ	48.3% @ -3 dBm & PMU	43% @ -11 dBm & 1 MΩ	25% @ -5 dBm & PMU

4.5 Conclusion

This brief presents a highly sensitive RF Energy Harvester (RFEH) based on a varactor ladder rectifier topology. The rectifier consists of an input employing a cross-coupled topology, and two NMOS and PMOS type cells with MOS varactors self-adjusting their capacitances with the ladder rectifier operation at low and high input power. The design is implemented on the GF FDX 22 nm technology and works in the GSM band at 990 MHz. The implemented design reports a remarkable end-to-end sensitivity of 1 V at -22.5 dBm. Furthermore, it shows a peak PCE of 26% at a low input power level of -13 dBm and a 50 kΩ load. A comparison with the state of the art is presented to highlight the key features of this design.

CHAPTER 5 ARTICLE 3: AN ADAPTIVE RADIO FREQUENCY ENERGY HARVESTER OPERATING OVER -30 TO 0 DBM INPUT RANGE FOR IOT APPLICATIONS

This chapter reproduces an article submitted to IEEE Access on October 30th 2024.

- A. Refaei, S. Genevey, Y. Audet, and Y. Savaria, "An Adaptive Radio Frequency Energy Harvester Operating Over -30 to 0 dBm Input Range for IoT Applications," IEEE Access.

5.1 Abstract

The demand for efficient and high-performance energy harvesting systems is increasing to power modern wearable smart devices. RF energy harvesters (RFEH) are commonly used because they provide wireless power delivery. This paper proposes a new way both to design sensitive and high-efficiency radio frequency energy harvesting systems with adaptive power management units (PMUs) for the Internet of Things (IoTs). It incorporates two different rectifiers, a three-phase rectifier and a varactor-based ladder rectifier in a hybrid system that reconfigure the operation based on the rectifier that delivers higher power. The three-phase rectifier provides high power conversion efficiency (PCE) since it uses a phase shifter that evenly splits the received power, delivering three signals with a 120° phase shift simultaneously. The varactor-based ladder rectifier incorporates a varactor to reduce the input capacitance at low available input power that enhances the sensitivity. The system has a buck/ boost converter to regulate the output voltage and supply a fixed voltage to the load. This system is designed using GF FDX 22 technology that enables low leakage and ultra-low power operation while maintaining a compact area of 0.017 mm^2. For a fixed load of 50 KΩ, the system achieves a sensitivity of -8 dBm at 1 V and a peak PCE of 24% at 1.47 V. When regulating the output voltage for a fixed 0.6 V over a range from -30 dBm to 0 dBm, the overall system consumes a maximum of 73% of the available power at -24 dBm and 12% at 0 dBm.

5.2 Introduction

Energy harvesting, particularly from radio frequency (RF) signals, is a burgeoning field poised to revolutionize how we power low-energy devices. The technology is especially useful for

applications on the Internet of Things (IoT), biomedical implants, and industrial monitoring systems, where connecting devices to a wired power source is impractical or impossible. RF energy harvesting leverages the abundance of RF signals in urban environments, capitalizing on the omnipresent electromagnetic waves emitted from wireless communication systems, including Wi-Fi, cellular networks, and other RF-emitting devices. This availability makes RF energy harvesting a promising renewable energy source, especially in areas where traditional energy harvesting methods, such as solar power, thermal gradients, or mechanical vibrations, may not be viable due to environmental limitations [60].

A key advantage of RF energy harvesting is that it can be employed where other energy sources are not feasible, such as indoors or in locations with limited sunlight or motion. However, RF signals often exhibit low power density, requiring advanced power management techniques and highly efficient RF-to-DC conversion circuits to harvest usable energy at low RF power levels [61]. Although RF energy harvesters can perform well in low-power conditions, they must also be able to handle situations where a dedicated RF power transmitter is present, which could supply a substantial amount of power to the RF energy harvesting system. Without adequate adaptability, a sudden increase in power density may lead to energy wastage or even damage to the energy harvester due to the inability to efficiently convert higher power levels or protect the load [35]. Therefore, the performance of an RF energy harvesting system must balance between low-power sensitivity and high-power robustness [62], [63].

The available power (P_{AV}) at the RF energy harvesting antenna varies significantly. It is influenced by factors such as distance from the RF source, antenna orientation, and changing network traffic conditions [64]. Predicting (P_{AV}) in practical applications is a challenge, and RF energy harvesters are typically designed for high sensitivity, enabling the harvesting of weak signals to open new applications. However, if these designs are not capable of adapting to varying power levels, their power conversion efficiency (PCE) suffers significantly as (P_{AV}) increases, a topic that will be further discussed in this paper [65], [66].

To address the fluctuating nature of input power, several approaches have been proposed in the literature. For instance, a dual-mode reconfigurable RF rectifier was introduced in [67] to extend

the operating power range of RF energy harvesters, allowing them to function efficiently at both low and high input power levels. Other works focus on integrating power management systems that support only resistive loads in the RF energy harvesting front end, ensuring that harvested energy is either stored or used efficiently [68], [70]. Off-chip matching networks and cascaded boost converters have been utilized to optimize energy transfer to resistive loads while maintaining high PCE across varying conditions [70].

The core component of any RF energy harvesting system is the RF-to-DC rectifier, which converts RF signals into DC power. The design of this rectifier is critical to the overall system performance, as it directly impacts both sensitivity and PCE. Early designs, such as the Dickson and full-bridge rectifiers, suffer from significant voltage drops across diodes, resulting in poor sensitivity and inefficiency at low RF power levels [71]. This makes them unsuitable for applications where ambient RF energy is scarce. To overcome these limitations, fully cross-coupled rectifiers (FX) have been developed, offering enhanced sensitivity and higher PCE even at low power levels by leveraging differential RF power applied across four transistors [71], [28]. Recent advances in RF energy harvesting have focused on the development of highly sensitive and efficient circuits for biomedical devices, wireless sensors, and RFIDs, which operate at frequencies such as 900 MHz, 1.4 GHz, 2.1 GHz, and 2.45 GHz [28], [72]. For each frequency band, a dedicated matching network and rectifier are required to harvest power separately [73]. These applications require energy harvesters to maintain high performance in variable and often unpredictable environments. Moreover, they necessitate the development of self-startup features and energy storage solutions to ensure the continuous operation of low-power electronics, even in the absence of a stable power source [74]. [75], [76]. In terms of antenna designs, multiple approaches have been explored, including using a single antenna for each band [38], utilizing a wideband antenna that covers a broader frequency range [39], or employing a multi-port antenna to capture multiple frequency bands simultaneously [1].

To address the challenges of sensitivity at low power levels and robustness at higher power densities, this paper presents a comprehensive RF energy harvesting system that integrates hybrid rectifiers to operate efficiently across a wide range of input power levels. The proposed

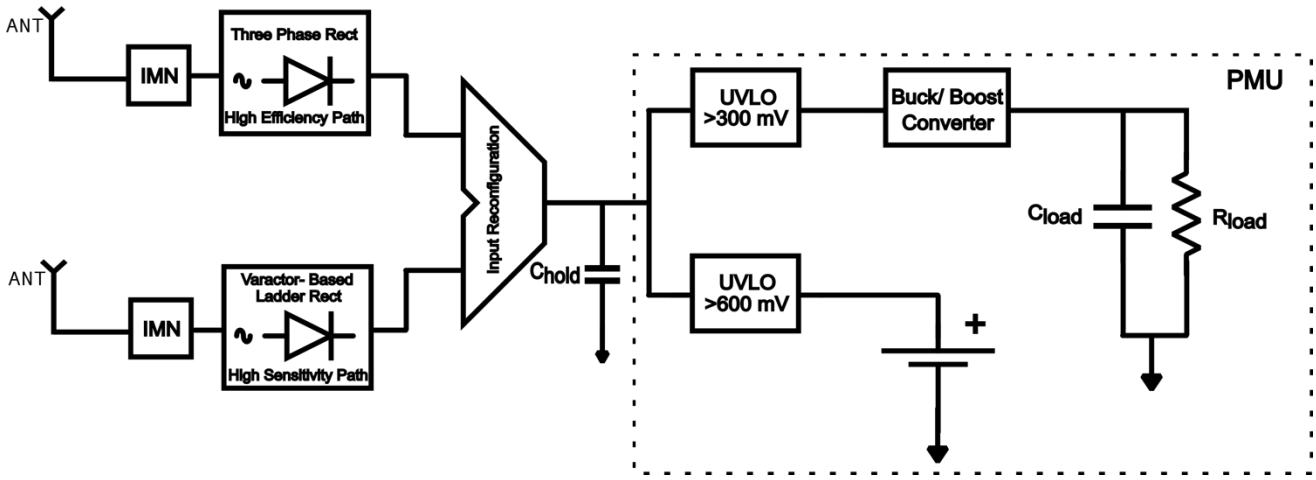

Figure 5.1: System block diagram of the proposed adaptive RF energy harvester

system is designed to power an SoC while dynamically adapting to fluctuations in P_{AV}, ensuring both high sensitivity and robustness to higher power levels. The paper is organized as follows: Section II covers the adaptive system design; Section III explains the output optimization power management unit. Section IV details the post-layout simulation results, and Section V concludes with a discussion on performance and applications.

5.3 The proposed system for the adaptive RFEH

Since the design of the radio frequency energy harvesters depends on the surrounding changes for instance the available power, the available band and the required voltage, The authors investigated the literature [2], [30], [77], [78], [15], [79] to conclude the optimization matrix that can be adopted to get good results. The proposed system integrates a hybrid system to achieve both high sensitivity and efficiency. The first rectifier is a three-phase rectifier, that provides high efficiency. The second rectifier is a varactor-based ladder rectifier that provides high sensitivity. Based on the available input power, the input reconfiguration will compare between the output of both rectifiers and passes it to the power management unit.

The power management unit functionality is to track the changes at the input and optimize the efficiency to ensure stable operation at the load. It consists of a couple of undervoltage lockout UVLOs, a capacitive buck/ boost converter and a storage element as shown in Figure 5.1. To make it simple, the authors assume that the load requires a constant 0.6 V to operate properly. Any voltage above or below this value should be bucked/ boosted for proper functionally. For the first UVLO in

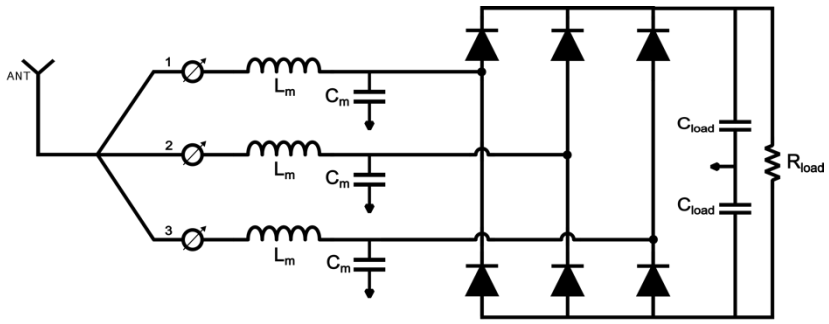

Figure 5.2: Three-phase single antenna RF energy harvester circuit diagram

the load path, if the voltage is less than 0.3 V, the UVLO ensures that the input is disconnected from the output to prevent any issue that could happen to the load when connected to very low supply. 0.3 V is half of the reference voltage (0.6 V), and it is the minimum voltage that the implemented buck/ boost converter can operate with. At this point, the load can be connected to the storage element until the input power level returns to a moderate or high level. If the voltage is above 0.3 V, the UVLO connects the input to the output and the buck/ boost works in the boost mode to fixate the output at 0.6 V. When the output of the rectifiers is high enough to 0.6 V, the second UVLO starts operating and stores the extra energy in a storage element to be used later when there is no supply from the rectifiers. This happens while the first UVLO is still working and feeding the load. The system ensures continuous operation for the load at low, moderate and high input power levels. Each block in the system diagram will be explained in detail later in this paper.

5.3.1 The three-phase rectifier principle of operation

The three-phase rectifier is commonly used in AC/DC power converters due to its high-power conversion efficiency and can produce efficiency up to 99.7%. The antenna feed is divided into three branches and each branch is connected to a matching network as shown in Figure 5.2. The output is taken as a differential voltage between the two diodes' sides. The diodes are implemented on GF FDX 22 technology using diode-connected transistors. The transistors size is chosen carefully since if they are too wide, the conducting current is higher, the RON is lower, but the leakage current is higher as well. On the other hand, when the transistors' width is too small, the leakage current is lower, but the R_{ON} and consequently the drop voltage are higher leading to an efficiency reduction [80].

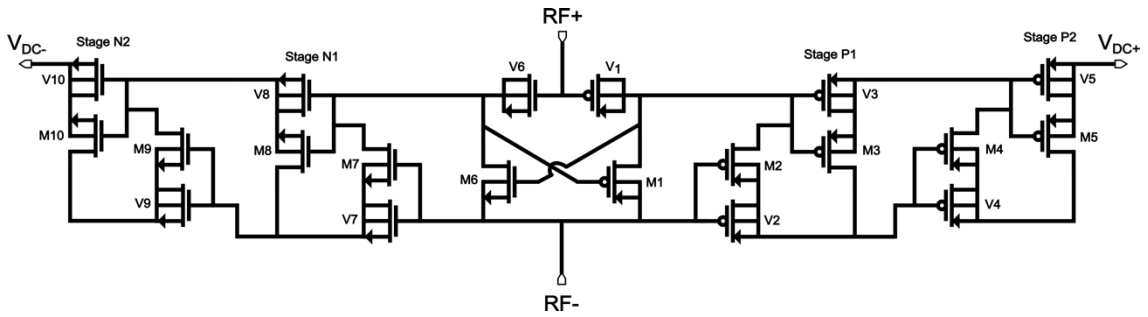

Figure 5.3: The varactor-based ladder rectifier RF energy harvester

5.3.2 The varactor-based ladder rectifier principle of operation

The varactor-based ladder rectifier consists of two primary parts: the input stage and the ladder stage, as illustrated in Figure 5.3. The input stage incorporates a cross-coupled rectifier design. Each segment of the ladder rectifier is made up of two complementary sections, with a varactor placed between the gate and source in each. This arrangement reduces capacitance when input power is low, improving sensitivity. The RF signal includes both positive and negative cycles. During the positive cycle, the varactor charges, raising V_{gs} and allowing current Ids to pass through the transistor to the next section. In the negative cycle, a negative input is applied, and the current flows to the following stage. The output voltage depends on the number of stages and losses from leakage current. While more stages can increase output voltage, they also lead to more leakage from each transistor. As a result, a balance is needed between the target output voltage and leakage. Furthermore, transistor sizing plays a key role; wider transistors lower switching resistance and reduce voltage losses but also increase leakage current [81].

5.3.3 The input reconfiguration

Figure 5.4 shows the overall input reconfiguration block. The functionality of this block is to compare between the two outputs of the rectifiers and passes it to the power management unit. It consists of a low power comparator designed to compare between the rectifiers outputs and sends a control signal of either a one or zero to an analog mux. If $RECT_2 > RECT_1$, the CNTL is one and $RECT_2$ passes to the output of the block. If $RECT_2 < RECT_1$, the CNTL is zero and $RECT_1$ passes to the output.

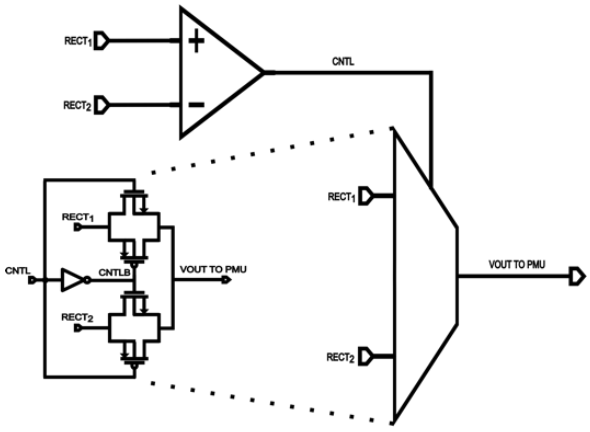

Figure 5.4: Input reconfiguration block diagram

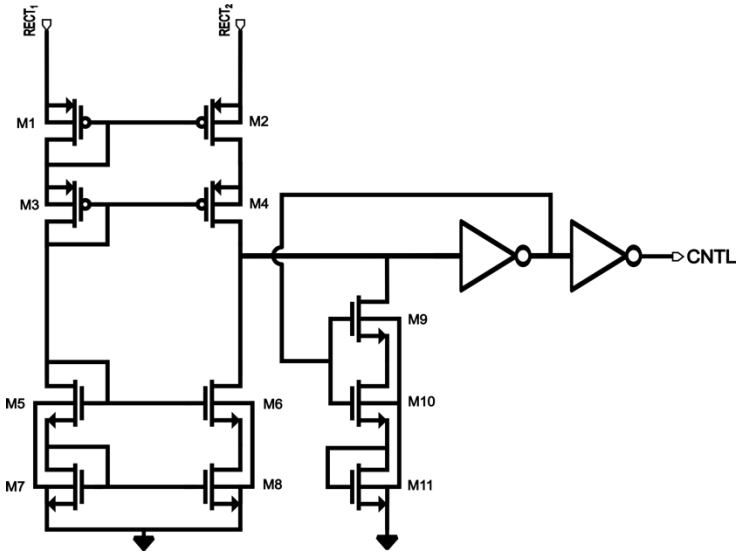

Figure 5.5: The ultra-low power comparator circuit used for input reconfiguration

Figure 5.5 shows the comparator used in the input reconfiguration block. The power consumption of this comparator is very critical since the power budget in radio frequency energy harvesters in low. The comparator works in the subthreshold region to reduce the losses. The choice of both SLVT and HVT transistors is to create an offset voltage for the comparator to appropriately select the higher voltage to path. Although this is might not be accurate for regular analog circuits, our results show that it is so efficient to compare between voltages in the range of 0.2 V to 0.7 V which is the typical range at which a decision on which rectifier's output should pass. Lower than 0.2 V, it is the varactor that is dominating and higher than 0.7 V, the three-phase will always result in higher efficiency. The current is directly drawn from the rectifiers themselves, leaving no need for external supply for the comparator to work. The comparator draws a current in range of hundreds of pA that only counts for small percentage of the system output current [30].

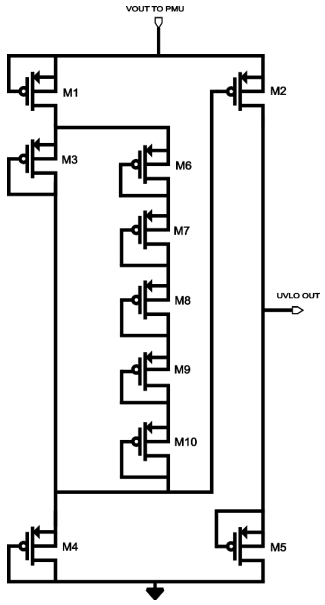

Figure 5.6: The undervoltage lockout (UVLO) circuit used in the output optimization power management unit

5.4 The output optimization power management unit (PMU)

5.4.1 The undervoltage lockout (UVLO)

A typical undervoltage lockout (UVLO) is built using a bandgap followed by a comparator with hysteresis. A reference voltage generated by the bandgap is compared to the supply voltage. If the supply is below certain level, it is locked out and disconnected from the load. When the supply starts increasing again and passes a certain value, it is reconnected, and a normal operation is restored [82]-[84]. The comparator is combined with hystersis and digital logic to adjust the points at which the supply is locked out and restored. The disadvantage with this design is that it consumes a power in range of μW which does not make it attractive for low power applications. To overcome this problem, the authors use the circuit presented in Figure 5.6 as a UVLO. The design used is suitable for ultra-low power applications since it uses two transistors with different threshold voltages to create a reference voltage. The reference voltage tracks the supply until it reaches its designed value and then it becomes a constant [85]. The UVLO consumes a current of tens of pA which makes it a good choice for the purpose of energy harvesters.

5.4.2 The buck/ boost converter

The radio frequency energy harvester needs to regulate the output to ensure stable operation on the load side. This requires a certain block that fixates the output voltage at the load despite the input changes. One possible way to do so is by implementing a low dropout regulator. The supply voltage (the output of the rectifier in our case) will be compared with a specific reference voltage. The output will be fixed at a certain level if it is higher. When the supply decreases, the output voltage will start decreasing as well. This is a suitable method to ensure that the load is not connected to a critically high output voltage [86]. The disadvantage of using this LDO is the low efficiency, especially when the difference between the supply voltage and the reference voltage is very large. Moreover, the circuit's power consumption does not suit the power range for radio frequency energy harvesters.

An alternative to using an LDO is a four-switch buck boost converter. This type of converter can provide an accurate output voltage and works with a wide range of input voltage. However, it has a large area and high power consumption, and it requires a complex control circuit for the system to work correctly. The next option is to use a capacitive-based buck-boost converter. Typically, such a converter consumes much less power than the previous two types and has a smaller footprint. This makes it attractive for RFEHs. The capacitive buck boost converter consists of a latch, which is based on a cross-coupled topology. When the latch input and output terminals are connected forward, it works as a boost converter. When the terminals are reversed, it works as a buck converter. The complete capacitive buck boost converter diagram is shown in Figure 5.7.

The control loop primarily consists of a comparator, an oscillator and flying capacitors. The latch input and output are connected to an analog MUX to set the correct operation whether it is buck or boost. The control signal for this MUX is shared with the control signal from the comparator in the control loop. For a certain reference voltage, the control loop will move up or down until the output voltage reaches the reference voltage [87].

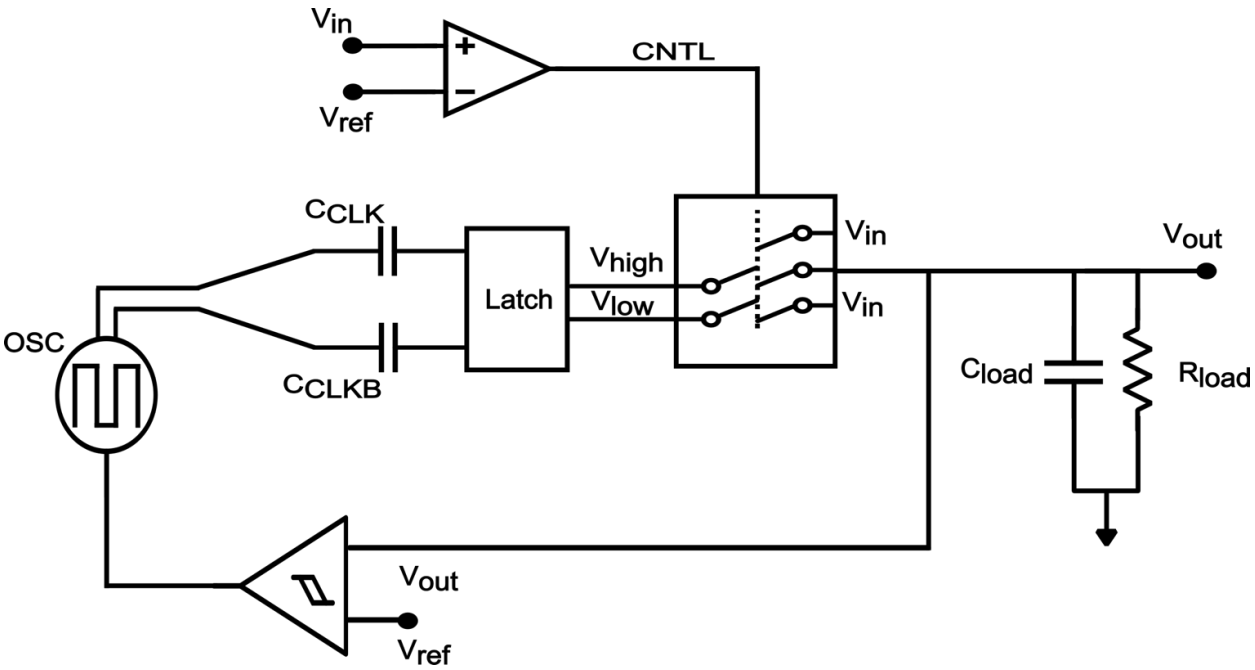

Figure 5.7: The buck/ boost converter block diagram

The latch and the flying capacitors require a clock signal to operate. The oscillator is a gated free running inverter-based oscillator as shown in Figure 5.8. The circuit consists of an adequate number of inverters in a closed loop. Increasing the number of inverters increases the delay and lowers the frequency. The advantage of using this topology is that it offers a wide range of tunning capabilities and low power consumption. The operation of this block depends heavily on the control signal from the feedback loop.

The main circuit in the buck- boost converter is based on the cross coupled latch circuit as shown in figure 5.9. In the boost mode, the output of the rectifier is connected to V_{low} signal and the output is taken from the V_{high} side. The oscillator starts generating the CLK and CLKB signals. When the CLK is high and CLKB is low, M_2 starts operating passing the input voltage (V_{low}) to flying capacitor node.

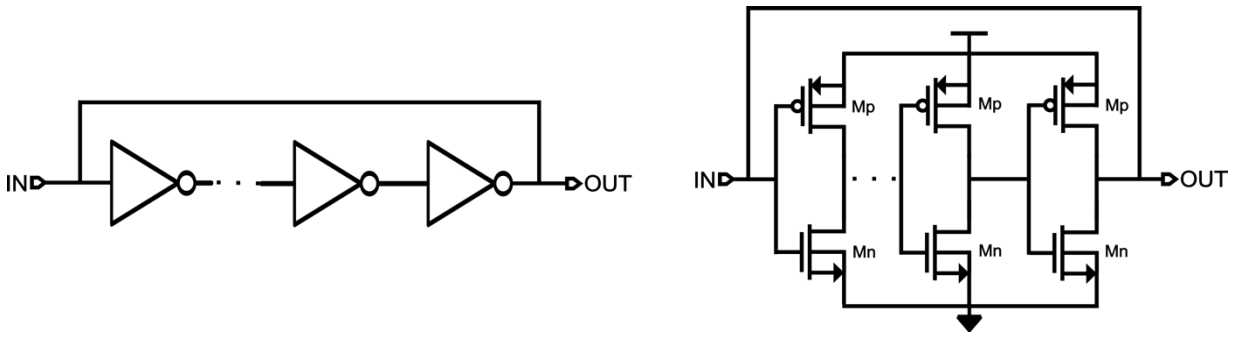

Figure 5.8: The inverter-based oscillator circuit

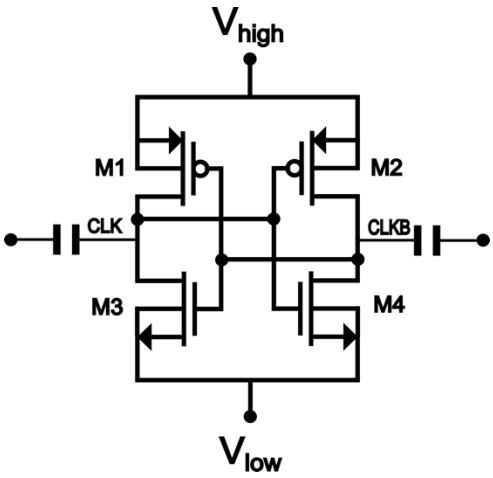

Figure 5.9: The latch circuit

At the same moment, M_3 starts operating and passes the V_{low} from the previous cycle to the output voltage (V_{high}). On the next cycle, M_1 starts operating and passes the V_{low} to the flying capacitor and at the same moment M_4 passes the flying capacitor voltage to the output voltage resulting in doubling the voltage at the output node.

In the buck mode, the input and the output are reverted. Now, the input voltage is connected to V_{high} signal, and the output voltage is connected to V_{low} signal. When the CLK is high and CLKB is low, M_2 starts operating passing discharging the voltage on the flying capacitor from the previous cycle to V_{low} node. At the same moment, M_3 starts operating and passes the V_{high} to the flying capacitor node. On the next cycle, M_1 starts operating and passes the voltage on the flying capacitor to the V_{low} node and at the same moment M_4 passes the V_{high} voltage to the flying capacitor resulting in halving the voltage at the output node.

5.5 The post-layout simulation results

5.5.1 The three-phase rectifier results

Figure 5.10 shows the output voltage when the available power varies from -30 dBm to 0 dBm. This is characterized by measuring the harvester response for different load conditions, 25 KΩ and 50 KΩ, to give an insight into the rectifier's intrinsic performance. The maximum reachable voltage is around 2.87 V for a 50 KΩ load.

The power conversion efficiency (PCE) as a function of the available input power is illustrated in Figure 5.11 under identical load conditions. The graph indicates that maximum power transfer is achieved at a load of 25 KΩ, with a peak PCE of 27.35% from end to end. In case of 50 KΩ, a peak PCE of 23.8% around -5 dBm is reported. The efficiency continues to increase with varying loads up to an input power of -5 dBm, at which point leakage effects become significant, causing the efficiency to decrease. The figure demonstrates that a PCE exceeding 20% is maintained across a broad input power range, from -15 dBm to 2 dBm. This 17 dBm range of high efficiency makes the proposed RFEH design highly suitable for sensor nodes in environments where input power levels fluctuate due to varying distances and signal strengths.

5.5.2 The varactor-based ladder rectifier results

Figure 5.12 depicts the output voltage across an available power range from -30 dBm to 0 dBm, measured under different load conditions, specifically with load values of 25 KΩ and 50 KΩ. The system is optimized to operate within this load range, ensuring maximum power transfer efficiency. The minimum viable voltage is recorded at -24 dBm, with an output voltage of 0.2 V.
Figure 5.13 reports the power conversion efficiency with respect to the available power, with the same loads' conditions. According to this figure, the peak power conversion efficiency is achieved for a load of 50 KΩ, yielding an efficiency of 22% at -20 dBm. The figure provides insights into the range where this RFEH maintains high efficiency.

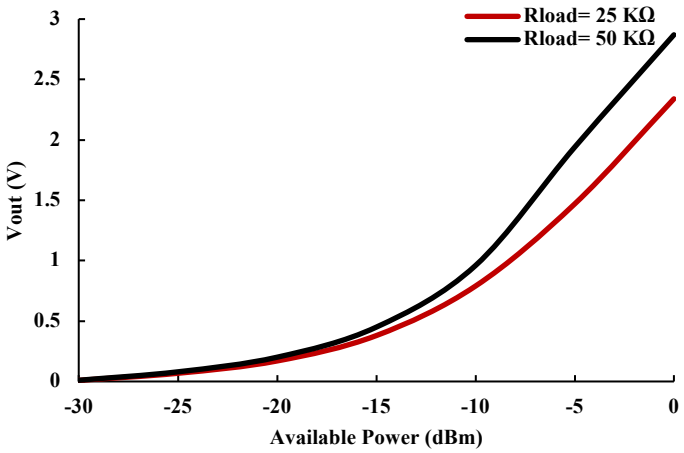

Figure 5.10: Output voltage of the three-phase rectifier versus the available power for R_{load}= 25, 50 kΩ

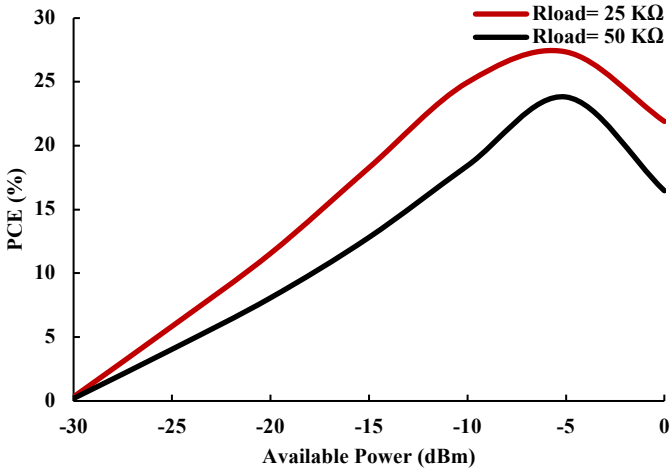

Figure 5.11: Power conversion efficiency (PCE) of the three-phase rectifier versus the available power for R_{load}= 25, 50 kΩ

From the previous results, we can draw Figure 5.14 that shows efficiency curves of both rectifiers on the same graph as a function of available input power. The varactor-based rectifier excels in low power region while the three-phase provides better efficiency at higher input power. The crossing between the two curves occurs at -11 dBm where the output voltage of both rectifiers is around 1 V. The input reconfiguration circuit that will be discussed next is to switch between one rectifier output and the other to keep the efficiency at its maximum over the available input power while at the same time the load is fixed.

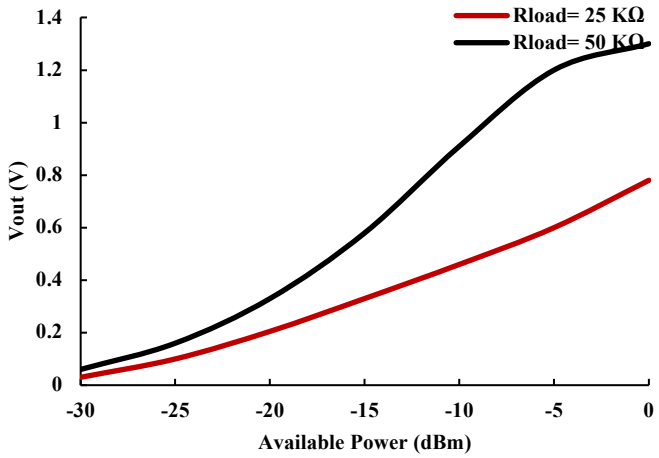

Figure 5.12: Output voltage of the varactor-based ladder rectifier versus the available power for R_{load}= 25, 50 kΩ

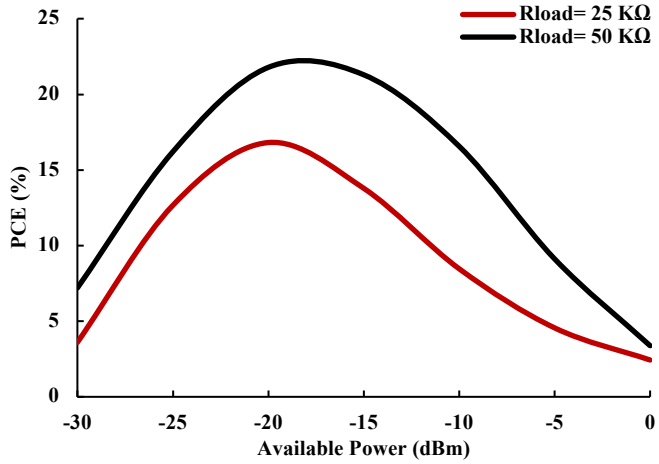

Figure 5.13: Power conversion efficiency (PCE) of the varactor-based ladder rectifier versus the available power for R_{load}= 25, 50 kΩ

5.5.3 The input reconfiguration results

The input reconfiguration circuit power consumption as a percentage of available power is presented in Figure 5.15 as a function of available power. At -30 dBm, the power consumption of the circuit represents 10% of the available power only. While the two output voltages gets closer to one another, the circuit consumes less power of around 0.3% of the available power.

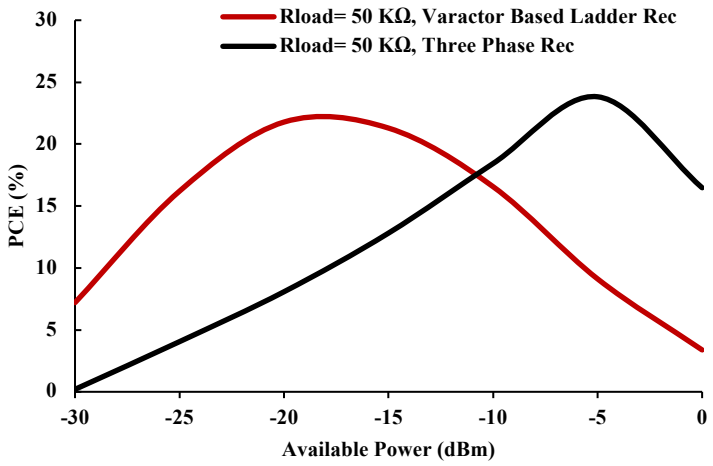

Figure 5.14: A theoretical combination of the PCE of both rectifiers versus the available power for R_{load}= 50 kΩ

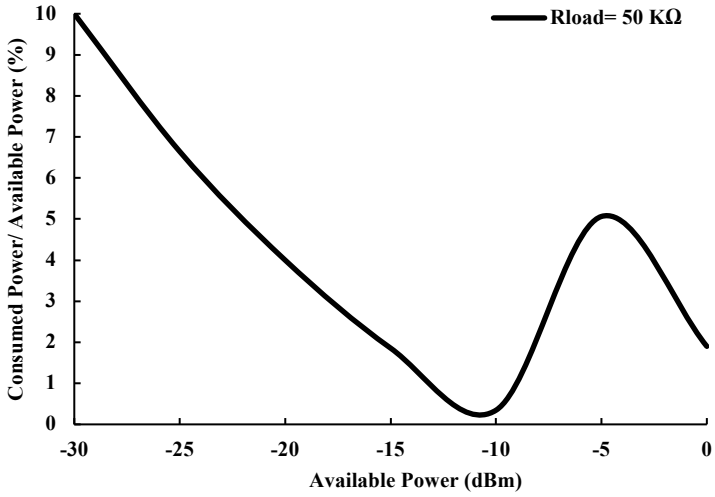

Figure 5.15: The input reconfiguration power consumption as a percentage of the available power versus the available power for R_{load}= 50 kΩ

Overall, the circuit consumes less than 10% of the available input power, which makes it ideal for such an ultra-low-power system. Figure 5.16 presents the output voltage, showing the transition from the varactor to the three-phase to keep tracking the highest voltage. Figure 5.17 reports the system's efficiency while the input reconfiguration block is working. The efficiency is extended and kept around 20% from -20 dBm to -5 dBm.

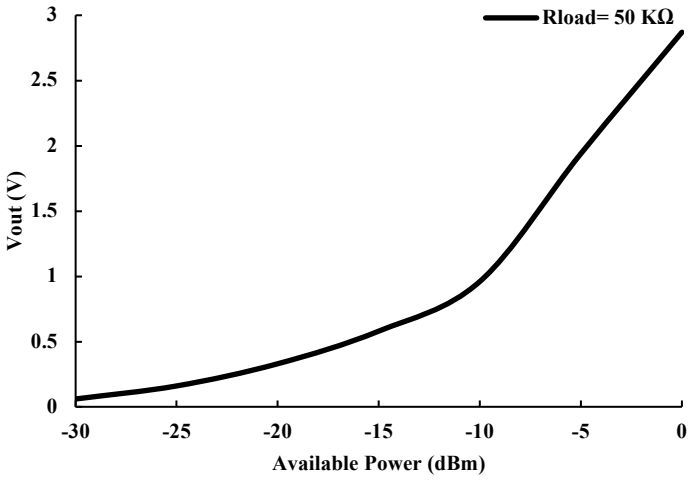

Figure 5.16: The overall output voltage of both rectifiers at the input of the power management unit (PMU) versus the available power for Rload= 50 kΩ

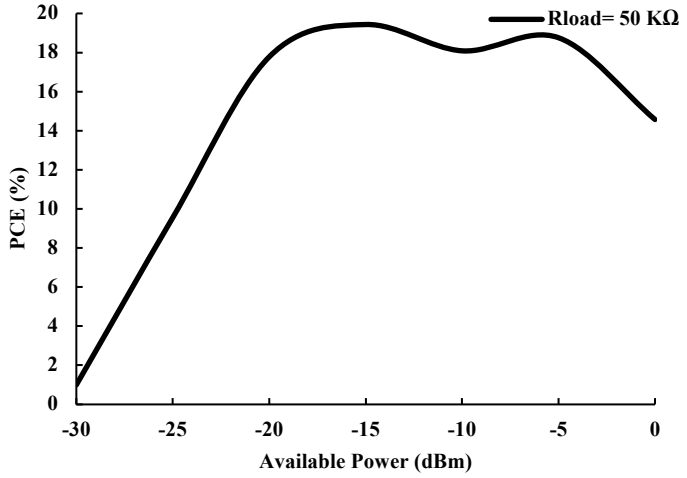

Figure 5.17: The overall PCE of both rectifiers at the input of the power management unit (PMU) versus the available power for R_{load}= 50 kΩ

5.5.4 The undervoltage lockout (UVLO) results

There are two UVLOs in the system, the first one with threshold of 0.3 V and the second one with 0.6 V. Figure 5.18 shows the output of the two UVLOs as a function of the rectifiers' output. When the rectifiers' output is below 0.3 V, UVLOs are blocking the rectifiers' output voltage to be connected to the load side ensuring the load protection. The output of UVLOs is close to zero in that region. Once this threshold is passed and since the priority is for the load, the first UVLO starts conducting

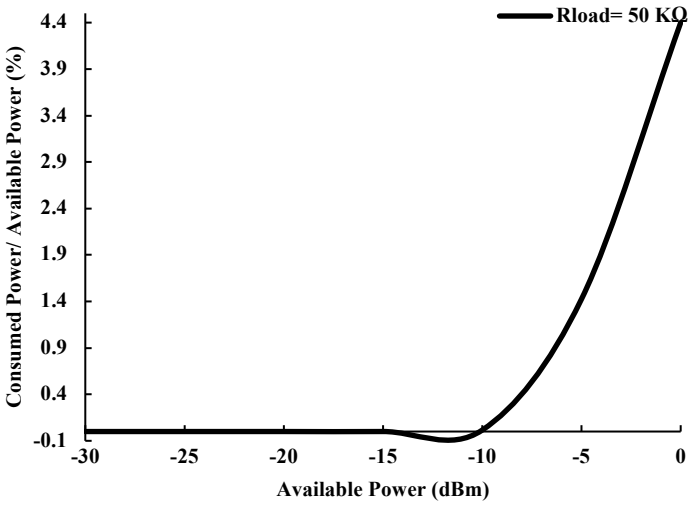

Figure 5.18: The undervoltage-lockout (UVLO) power consumption as a percentage of the available power versus the available power for Rload= 50 kΩ

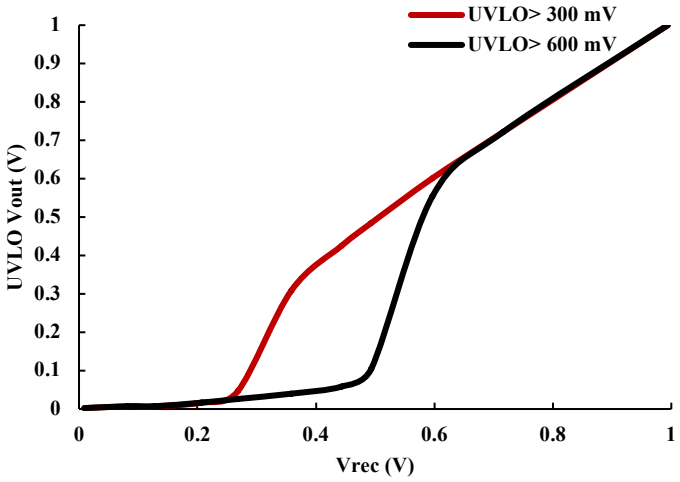

Figure 5.19: Transfer characteristics of the used undervoltage-lockout UVLO

the rectifier's output to the load and the UVLO output jumps to have an equal value as the input while the second UVLO output is maintained close to zero. The second UVLO starts conducting at the second threshold of 0.6 V giving this extra power to the storage element. Figure 5.19 shows the power consumption of both UVLOs as a percentage of available power as a function of available input power. The circuit is very efficient consuming less than 1% of the available power up to -10 dBm with a maximum of 4.5% at 0 dBm.

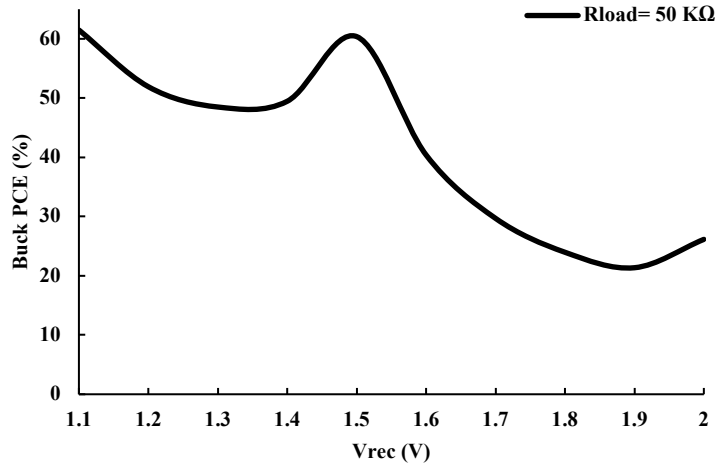

Figure 5.20: The efficiency of the buck/ boost converter in the buck mode versus the input of the power management unit (PMU) for R_{load}= 50 kΩ

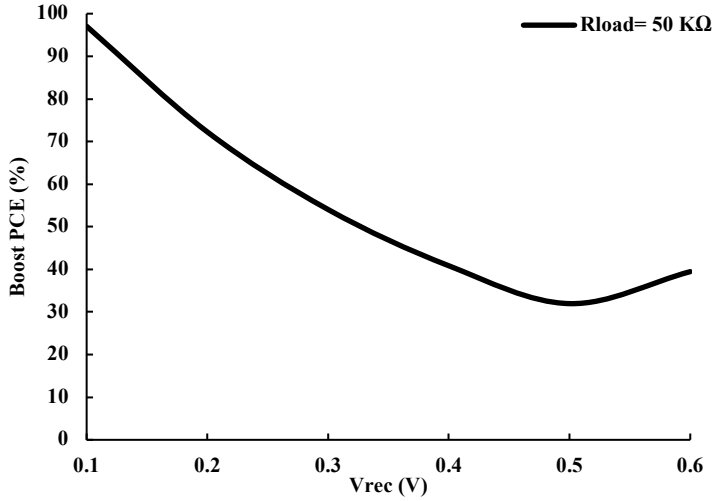

Figure 5.21: The efficiency of the buck/ boost converter in the boost mode versus the input of the power management unit (PMU) for R_{load}= 50 kΩ

5.5.5 The buck/ boost converter results

Figure 5.20 shows the efficiency of the buck/ boost converter as a function of the rectifier output voltage in the buck mode while the load is fixed at 50 KΩ and the output voltage is 0.6 V. The converter shows a peak efficiency of 61% at 1.1 V and 27% at 2 V. The lowest efficiency is 21% at 1.9 V. In the boost mode for the same load conditions, the efficiency drops from 97% at a rectifier output voltage of 0.1 V to 39% at 0.6 V as shown in Figure 5.21 In case of proposed system, the output voltage of the rectifier varies based on the available power.

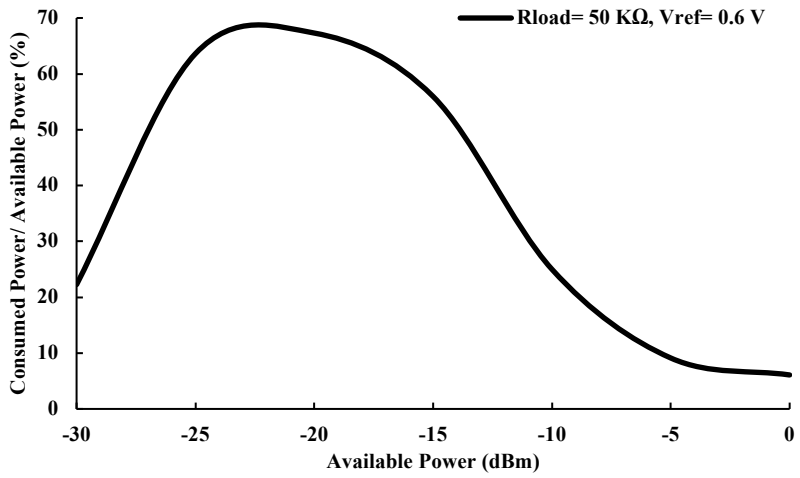

Figure 5.22: The buck/boost converter power consumption as a percentage of the available power versus the available power for R_{load}= 50 kΩ, and Vref= 0.6 V

As a result, it is convenient to report the power consumption of the converter as a percentage of the available power with respect to the input available power for our condition of 0.6 V and 50 KΩ. In Figure 5.22, the buck/ boost converter consumes a maximum of 67% of the available at -20 dBm which makes it the most power-hungry block in the proposed system. On the other hand, the converter consumes only 22% at -30 dBm and only 6% at 0 dBm that makes it very efficient at these power levels.

5.5.6 The overall system results and performance summary

In the overall system performance analysis, the proposed adaptive RFEH layout in GF FDX 22 nm is shown in Figure 5.23. The blocks in Figure 5.23 from one to six are as follow in order, three phase rectifier, input reconfiguration, varactor-based ladder rectifier, UVLO > 300 mV, UVLO > 600 mV and buck/ boost converter with total area of 170 µm × 100 µm. The power consumption of all the blocks with relative to the available input power is shown in Figure 5.24. The system can regulate a voltage of 0.6 V with 50 KΩ load connected to it while consuming a maximum of 71% of the available power. The system is so efficient, and it consumes only 30% at -30 dBm and only 12% of the available power at 0 dBm. Table 5.1 shows a summary of the performance results in comparison with the state-of-art. The system sensitivity is -8 dBm for a load of 50 KΩ and 1 V output voltage. The peak PCE is 27% for a load of 25 KΩ and 1.47 V output voltage at -5 dBm. The system provides load regulation feature while keeping the minimum area of 0.017 mm2 compared to the literature.

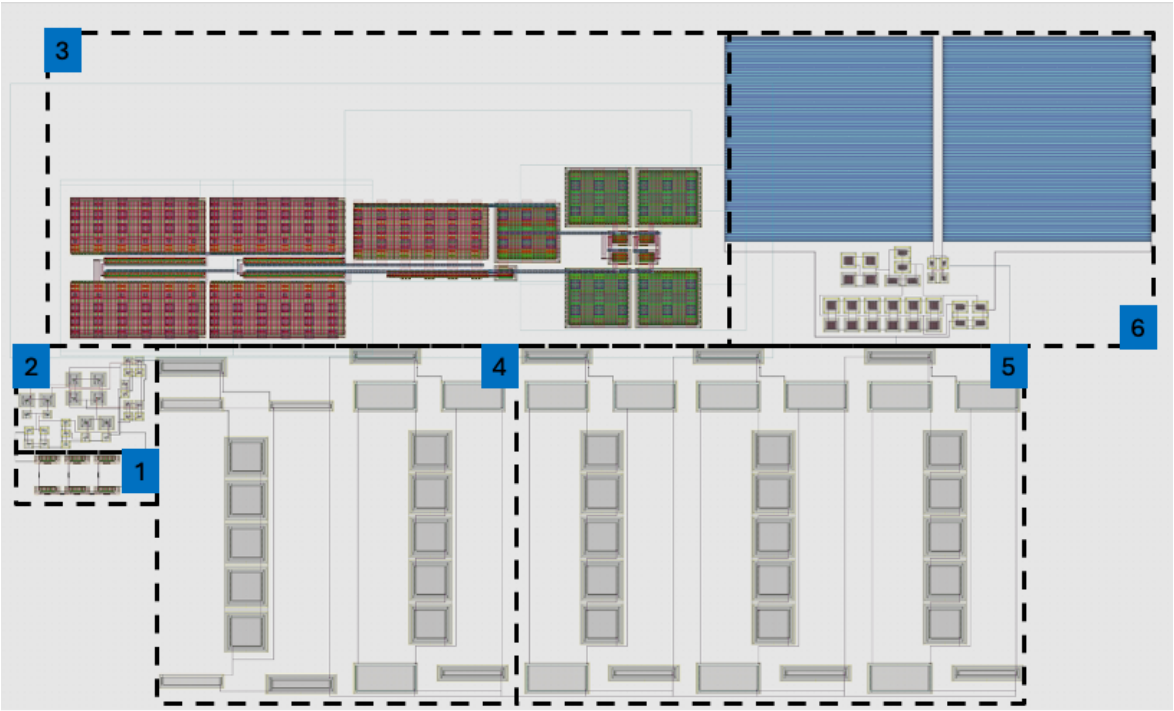

Figure 5.23: The proposed adaptive RFEH layout in GF FDX 22 nm (170 µm × 100 µm)

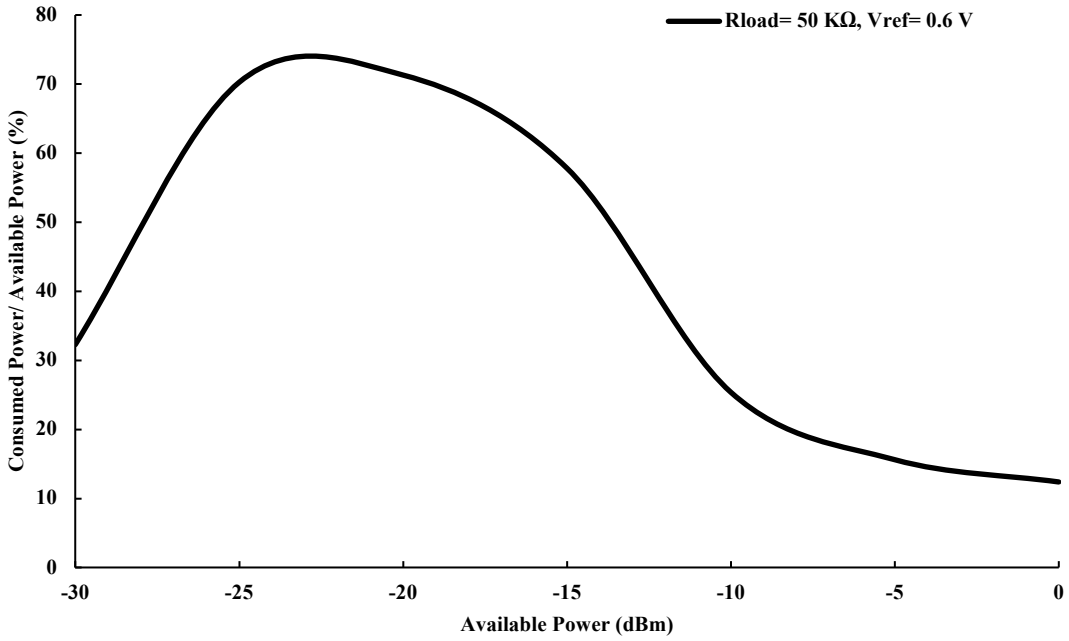

Figure 5.24: The overall adaptive RFEH power consumption as a percentage of the available power versus the available power for R_{load}= 50 kΩ, and Vref= 0.6 V

5.6 Conclusion

In conclusion, the growing demand for efficient and high-performance energy harvesting systems, particularly for powering wearable smart devices and IoT applications, has driven significant advancements in RF energy harvesting (RFEH) technology. This paper presents a novel hybrid RF energy harvesting system with an adaptive power management unit (PMU), combining a three-phase rectifier for high power conversion efficiency and a varactor-based ladder rectifier for enhanced sensitivity. By leveraging the strengths of both rectifiers and dynamically reconfiguring the system based on input power, the proposed design achieves efficient wireless energy harvesting. The integrated buck/boost converter ensures stable output voltage of 0.6 V for powering System-on-Chip (SoC) devices, while the undervoltage lockout mechanism provides protection and energy storage capabilities. The implementation using GF FDX 22 technology enables ultra-low-power operation with minimal leakage. Performance metrics demonstrate the system's potential for powering ultra-low-power devices and Internet of Things (IoT) applications, achieving a sensitivity of -8 dBm and a peak power conversion efficiency of 24% for a load of 50 KΩ. With its compact area of 0.017 mm^2.

TABLE 5.1
PERFORMANCE SUMMARY AND COMPARISON

Reference	**This Work [2024]**	**[32] [2017]**	**[30] [2017]**	**[88] [2013]**	**[89] [2017]**
Technology	GF FDX 22 nm	0.18 µm	65 nm	0.13 µm	0.18 µm
Frequency	900 MHz	900 MHz	900 MHz	900 MHz	930 MHz
Input Power Range (IPR)	-30 dBm to 0 dBm	-20 dBm to 0 dBm	-18 dBm to -3 dBm	-	-20 dBm to 0 dBm
Additional System Requirements	Phase Shifter, PMU	-	-	Capacitor Biasing Network	Integrated Passive Device
Sensitivity @ Vout and R_{load}	-8 dBm @ 1 V, 50 kΩ	-14.8 dBm @ 1 V, 1 MΩ	-17.7 dBm @ 1 V& ∞	-19.3 dBm @ 1 V	-15.4 dBm @ 1 V, 500 kΩ
Effective Area	0.017 mm^2	1.08 mm^2	0.048 mm^2	4 mm^2	11.6 mm^2
Peak PCE	27% (@ 25 kΩ, 1.47 V, -5 dBm)	25% (@ -5 dBm)	36.5% (@ 147 kΩ, 2.2 V, -9 dBm)	9.1% (@ 1.15 MΩ, 1.15 V, -19.3 dBm)	25.2% (@ 500 kΩ, 1.15 V, - 1 dBm)
System Architecture	Adaptive Hybrid System (Three Phase+ Varactor Based Rectifiers)	Reconfiguration Rectifier	Cross Coupled Rectifier	Dickson Charge Pump	Native NMOS Dickson
Load Regulation Capability	Yes	Yes	No	No	No

CHAPTER 6 GENERAL DISCUSSION

This chapter begins by outlining how this thesis addresses our doctoral research objectives in the context of existing literature. It then explores the broader implications and significance of the research and proposed work. Finally, the chapter closes by recognizing the limitations of our methods and circuits that the research community can further improve.

6.1 Addressing Research Objectives

The IoT technology pushes the need for battery-less systems to supply the current demand for wireless ICs. People depend more on wireless technology daily, such as air pods, IoT sensors, smart watches, etc. Moreover, more than ever, the environment is crowded with urban RF signals. This creates real chances for radio frequency energy harvesters to thrive. Chapters one and two of the thesis introduce the reader to the work of designing radio frequency energy harvesters. It investigates many ideas with their limitations and challenges. The comprehensive literature review on the state-of-the-art paved the way for introducing our objectives and designs in the following chapters.

In chapter three, the first objective of designing a three-phase radio frequency energy harvester is introduced. The design uses a three-phase rectifier topology with a phase shifter to generate the required phases between the input terminals. The input signal is split equally in magnitude across three paths, each shifted by 120° in phase. An L-matching network optimizes power transfer by matching each path to a dedicated rectifier branch. The rectifier uses SMS7621 Schottky diodes from Skyworks, which are ideal for sensitive RF applications due to low forward voltage drops and minimal leakage. The design components, including the phase shifter, matching network, and rectifier, are thoroughly analyzed. A demonstration prototype is fabricated on an RT/Duroid® 5880 Laminates substrate with a thickness of 0.005 inches, minimizing dielectric losses. Tests with this prototype show promising performance in the 435.6 MHz ISM band, achieving a high efficiency of 56% at a 6 kΩ load with a 5.2 V output. Additionally, the system maintains an efficiency above 20% across a wide input power range of 29 dB, demonstrating a sensitivity of 1 V at -10 dBm. With low S11 values, the design sustains high efficiency and stable output voltage across a broad

frequency range from 280 MHz to 550 MHz, with resonance centered in the ISM band. This design shows promising efficiency with a simple and compact design.

In chapter four, the second objective of designing a varactor-based ladder rectifier is introduced. The rectifier utilizes a cross-coupled topology at its input, paired with NMOS and PMOS cells featuring MOS varactors. These varactors self-tune their capacitance based on the ladder rectifier's operation across varying input power levels, ensuring efficient performance at both low and high-power inputs. Designed with GF FDX 22 nm technology, this rectifier operates within the GSM band at 990 MHz. The design achieves impressive end-to-end sensitivity, reaching 1 V at an input power of -22.5 dBm. Additionally, it demonstrates a peak power conversion efficiency (PCE) of 26% at a low input power level of -13 dBm with a 50 kΩ load. A comparative analysis with existing designs is provided to underscore this design's unique capabilities and advantages over current technologies. The rectifier demonstrates good sensitivity and a good boosting ratio as well.

In chapter five, the third objective of designing a hybrid system between both proposed designs to regulate the output voltage to a specific value required by the load is presented. The system includes a buck/boost converter to maintain a stable output voltage of 0.6 V, suitable for powering System-on-Chip (SoC) devices, and an Undervoltage lockout mechanism to protect the load and support energy storage. This design uses GF FDX 22 nm technology to support ultra-low-power operation with minimal leakage. Performance metrics highlight its suitability for powering ultra-low-power and IoT devices, achieving a sensitivity of -8 dBm and a peak power conversion efficiency of 24% with a 50 kΩ load, all within a compact area of just 0.017 mm².

6.2 Implications and Significance

This thesis presents the development of an ultra-sensitive, reliable radio frequency energy harvester (RFEH). Two innovative designs are implemented using GF 22nm FDX technology to optimize performance, chosen for its efficient power consumption and minimal current leakage. These designs are integrated into a hybrid system to stabilize the output voltage and ensure circuit protection for the load. The first design utilizes a three-phase rectifier, with an antenna connected to a phase shifter that generates three separate phases, each feeding into a triple-branch rectifier. This three-phase rectifier is verified with Cadence through pre- and post-layout simulations, with

its three outputs directed through a load and smoothing capacitor to ensure steady power flow. The second design is a varactor ladder rectifier, leveraging the varactor's low capacitance at low input levels for enhanced sensitivity. This low capacitance is crucial for high-sensitivity applications, as it allows the varactor to increase capacitance with input level until saturation. The two designs are combined in a comprehensive system that reconfigures the rectifier's output and directs it to a power management unit. This setup regulates the voltage to deliver a stable supply to the load. The proposed RFEH system is designed for on-chip integration with multisource harvesters, providing a flexible power solution that can operate effectively across varied environmental conditions. Additionally, the proposed system is ideal as a prototype for a product that can be commercialized and made available to customers.

6.3 Limitations

The three-phase rectifier paper discusses the implementation of integrating three-phase shifters into the energy harvester. However, only one design with many variations was studied. This does not give enough insight into the improvements the phase difference can make in such systems. Moreover, the phase shifter needs to be fabricated separately, and using a proper network analyzer and an oscilloscope, the S_{11} parameter and the phase shift can be graphed to improve the functionality of this block. A closer analysis of the extra losses added from the third branch and the phase shifter compared to the theoretical limit of conventional rectifiers has also not been studied. The phase shifter footprint is also large and needs to be smaller for more compact designs.

For the varactor ladder rectifier, the packaging losses and PCB should be analyzed to improve the performance of such systems. The varactor should be fabricated separately to report the exact values for the capacitance before and after fabrication. Also, the conventional design must be fabricated to compare the modified rectifier to the original one.

The results reported for the full system are post-layout simulations. The system needs to be fabricated to test its actual performance. In addition, even though the technology used provides low leakage and a small footprint, the maximum voltage that can be harvested is limited to close to 3 Volts. This restricts the available input range and does not make it desirable for RFEHs.

CHAPTER 7 CONCLUSION AND RECOMMENDATIONS

7.1 Summary of work and contributions

This chapter summarizes and concludes the work and contribution of this thesis in section 7.1. Section 7.2 presents our future work and insights into the trend of designing RFEHs. In section 7.3, the author lists the deliverables, and the journal papers prepared to share the contributions made in this thesis. This thesis presents different approaches to designing RFEHs with high efficiency and sensitivity. The contributions are detailed as follows:

1- The first approach is by integrating the phase shift between the input signals to build up a DC level. This approach is based on the classic three-phase rectifier that provides high AC/ DC conversion efficiency. The initial prototype offers a peak power conversion efficiency of 56% with a 6 kΩ load and 5.2 V of output voltage at 8 dBm of input available power. Moreover, the system keeps an efficiency higher than 20% for 29 dB of the reported input power range, making it ideal for ambient conditions where the signal fluctuates.

2- The second approach is introducing the ladder rectifier to RFEHs since it is known for its high boosting ratio and, therefore, its high sensitivity. The pumping capacitor should be replaced with a varactor to reduce the capacitance at low input power levels. The initial prototype provides a sensitivity of -22.5 dBm with open circuit conditions at 1 V. Moreover, this compact system makes it easy to integrate with other systems since it has only a 0.002 mm^2 effective area.

3- The third approach uses the proposed rectifiers to design a full prototype for a product that can power a device with a fixed load value and required voltage. The rectifiers matching conditions are adjusted to work for a load of 50 kΩ and a fixed output voltage of 0.6 V. For this condition, the system achieves a sensitivity of -8 dBm at 1 V and a peak PCE of 24% at 1.47 V. For a range from -30 dBm to 0 dBm, the overall system consumes a maximum of 73% of the available power at -24 dBm and 12% at 0 dBm. Moreover, the system protects the load by integrating UVLOs to separate the load from the supply in case the power available is not enough to power the system. The excess power is redirected to

a second path, which goes to an energy reservoir to store and use when the available power is insufficient. This system uses the FDX 22 technology, enabling low leakage and ultra-low power operation while maintaining a compact area of 0.017 mm^2. These results show a comprehensive approach to designing an RFEH. The thesis also presented a comparison between this system and the state-of-the-art systems, showing the key figures for designing an RFEH, such as the sensitivity, peak PCE, and area. With the load regulation capabilities and the novel adaptive hybrid system, the presented prototype proves its competency and provides a new solution for the challenges facing the design of RFEHs.

7.2 Future work

In this thesis, we introduced new ways of designing radio frequency energy harvesters for IoT applications. The new designs have improved the sensitivity and efficiency significantly. However, more research and development could be conducted to enhance the performance of these designs further:

1- The multi-phase rectifier can be investigated with an antenna array to see the performance of such a configuration versus the proposed three-phase single antenna feed design.
2- In this thesis, the author focused on investigating the phase shift effect on the performance of radio frequency energy harvesters. However, it will be interesting to study the amplitude shift and build-up to improve the system's efficiency.
3- The three-phase RFEH is used in a single-tone frequency. Future work should be conducted on multi-tone systems using summation networks or integrating these tones in a single operating system.
4- The varactor effect can be studied in other types of rectifiers, such as the Dickson charge pump, the Greinacher voltage multiplier, and cross-coupled rectifiers.
5- Finally, the system can be adapted into an actual product by designing a custom antenna that can be integrated with the RFEH along with a real sensor, such as a temperature or humidity sensor at the output.

7.3 Knowledge Dissemination

The methodologies and results developed in this doctoral research have been shared with the scientific community and industry practitioners through journal articles.

Contribution point (1), regarding designing high-efficiency rectifiers for the RFEH systems, has been published in IEEE Transactions in Microwave Theory and Techniques as a journal article listed below:

Refaei, S. Genevey, Y. Audet, and Y. Savaria, "High-efficiency wide input power range three-phase radio frequency energy harvester for IoT applications," IEEE Trans. Microw. Theory Techn., doi: 10.1109/TMTT.2024.3456690.

Contributions point (2), regarding the design of high sensitivity rectifiers for RFEH systems, have been reported in a journal article submitted to IEEE Transactions on Circuits and Systems II, Express Briefs as listed below:

Refaei, S. Genevey, Y. Audet, and Y. Savaria, "Varactor-based ladder rectifier radiofrequency (RF) energy harvester for IoT applications," IEEE Trans. Circuits Syst. II, Exp. Briefs, 2024.

Contribution point (3), regarding integrating both rectifiers in a fully adaptive system and regulating the output voltage, has been submitted to IEEE Access journal as listed below:

Refaei, S. Genevey, Y. Audet, and Y. Savaria, " An Adaptive RF Energy Harvester Operating Over -30 to 0 dBm Input Range for IoT Applications," IEEE Access, 2024.

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