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RESEARCH ARTICLE

A Systematic Approach for PLL-Based Zeta Power Converter Control

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ABSTRACT This paper presents a systematic approach for Zeta power converter control, a versatile solution designed for systems where the power supply is prone to fluctuations. The optimized controller exploits a detailed model of the power stage and adjusts the system parameters to ensure stability over a wide range of loads and loading conditions. A detailed model for the Zeta converter is developed, considering important power stage parameters such as the ON resistance of power transistors and inductor series resistance. The control strategy utilizes a phase-locked loop, which includes a loop filter along with an additional lead compensator circuit to improve the loop phase margin, thereby enhancing the system's dynamic response and stability. The proposed graphical approach facilitates intuitive controller design and tuning, providing a robust framework for managing converter dynamics. The system stability and performance are validated through extensive transient simulations using a standard 180 nm CMOS technology, demonstrating the converter's effectiveness in maintaining stable output under variable input conditions. Experimental results show that the proposed closed-loop Zeta converter can achieve a peak efficiency of 94% when the load resistance is 10 Ω, and it can handle current loads up to 3A. The system operates at a switching frequency of 85 kHz and can support an input voltage range from 6V to 34V while maintaining stable output. During reference tracking tests, the system demonstrates excellent transient response, with a settling time of 12.5 ms and a peak overshoot of 3.9V. Additionally, compared to similar works, the system exhibits superior normalized transient load regulation, highlighting the robustness of the proposed control strategy.

INDEX TERMS Automotive power distribution, CMOS technology, dc–dc converters, Zeta converter, power stage modeling, renewable energy systems, transient simulation, voltage controlled oscillator.

I. INTRODUCTION

Effective power management in Power Distribution Grids (PDGs) is crucial, especially in automotive applications where power from different sources must be reliably distributed to various loads, including hydraulic actuators [1], [2], [3], [4]. DC-DC power converters play a critical role in these systems by directly interfacing with loads and regulating the input voltage supply (v_{in}) from power buses, which often experience transient surges leading to overvoltage or undervoltage variations [5], [6]. These surges can result from PDG reconfigurations or load variations, highlighting the necessity for dynamic and robust control over the converters to ensure operational reliability [7], [8].

With its unique features, the Zeta converter stands out as a versatile solution. Unlike buck and boost converters, which are limited to either stepping down or stepping up the input voltage, the Zeta converter provides both step-up and step-down responses with a continuous, non-pulsating output current [9]. This feature, combined with its ability to handle fluctuating input voltages while ensuring a stable output, makes it ideal for industrial applications with variable

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power conditions, such as battery-operated devices and solar energy systems, where v_{in} can fluctuate significantly [10].

Despite their advantages, one of the primary challenges associated with Zeta converters, particularly in power distribution grids (PDGs), is the need for a control strategy capable of effectively managing rapid changes in input conditions without sacrificing stability or performance. Traditional control methods, such as PID (Proportional-Integral-Derivative) and sliding-mode control, often struggle to maintain consistent performance across a wide range of input voltages and loads. This limitation arises from their response constraints and reliance on complex components [11], [12], [13], [14]. This issue becomes even more pronounced in automotive applications, where transient surges and dynamic load variations are common, necessitating a more adaptive and efficient control approach.

Recent advances in control techniques for DC-DC converters have highlighted the potential of time-based methods, which significantly improve efficiency and response under variable operating conditions. Unlike traditional controllers, such as PID and sliding-mode control, which may face challenges with maintaining stability and adaptability across a wide range of input voltages and loads [11], [12], [13], [14], time-based control approaches leverage time as a processing variable. This strategy eliminates the need for complex analog components, resulting in reduced design complexity and enhanced speed of response.

One of the key innovations in this area is the implementation of phase-locked loop (PLL) systems. These systems synchronize the phase and frequency of an output signal with a reference signal for precise control. PLL-based controllers, which utilize this system, have shown promise in delivering stable and efficient performance in power converters by leveraging these advantages [15].

Motivated by the need for a robust solution to address the specific challenges posed by fluctuating input conditions in PDGs, this paper proposes a PLL-based control strategy tailored for the Zeta converter. This approach aims to harness the converter's dual step-up and step-down capabilities to maintain stability and reliable output, even in demanding automotive applications. The proposed method achieves efficient and adaptive control while minimizing computational overhead, marking a significant step forward in converter control methodologies for dynamic applications.

The proposed Zeta converter model considers the ON-resistance of the power transistors and the inductor's series resistance. Building upon previous research [15], the PLL-based controller, initially designed for buck converters, has been re-optimized by adjusting its parameters and adding a lead compensator circuit to suit the Zeta converter better. A graphical approach to the Zeta converter control design is introduced, utilizing Bode plots to visually align system gain and phase margins, ensuring optimal stability and performance. This simple approach facilitates an understanding of system dynamics without the computational overhead and complexities associated with more advanced control strategies like sliding-mode control (SMC) [16], [17], [18]. The fabricated controller prototype, developed using the X-FAB 180 nm technology, allows for observing the system's response to hardware imperfections and non-idealities, comprehensively assessing the robustness and reliability of the proposed control strategy.

The paper is organized as follows: Section II provides background information regarding the various DC-DC converter topologies and their control mechanism. Section III presents the power stage analysis, including the modeling step. Section IV details the proposed graphical approach for the control system design. Section V describes the PLL-based controller and its circuit implementation. Section VI discusses the experimental setup and presents results from testing the fabricated chip, including the system's performance metrics and robustness evaluation. Section VII offers concluding remarks and directions for future research. Finally, an appendix presents the mathematical derivation of the steady-state equation expressing the operation of the Zeta converter.

II. BACKGROUND INFORMATION

Integrating renewable energy sources, such as fuel cells and photovoltaic systems, into PDG emphasizes the necessity for advanced converter technologies. These renewable sources often produce low and unstable voltage levels that fluctuate due to environmental conditions, including variable loads, solar irradiance, and temperature variations [19]. Therefore, there is a need for converters capable of managing these fluctuations while maintaining stable output voltages for various applications [20], [21], [22], [23]. The demand for flexible power conversion solutions is also significant in portable electronics, where battery voltage can vary with charge levels. Converters that adaptively switch buck and boost modes ensure a consistent output voltage across a wide range of input conditions [24].

To address the challenges posed by fluctuating input voltages in PDGs, especially in industrial applications, selecting an appropriate converter topology [25] is crucial. These applications often face surge conditions where the input voltage v_{in} may exceed or fall below the desired constant output voltage v_o. Such scenarios require converters to efficiently manage these fluctuations without compromising stability or output quality. When v_o is lower than v_{in}, step-down topologies, such as the buck converter, are preferred due to their simplicity and the absence of a need for high-gain conversion [26]. On the other hand, when v_{in} drops below v_o, it is essential to use a topology capable of handling both step-up and step-down functions.

While cascading buck and boost converters is an option, it tends to be inefficient due to increased losses [27]. The non-inverting buck-boost converter is known for having a minimal number of passive components, which simplifies control. However, it suffers from significant switching and conduction losses related to its H-bridge design and high

inductor currents [27]. The Ćuk converter [28] provides continuous input and output currents but produces a negative output voltage and experiences high current stress on the switch, making it less suitable [28], [29].

Focusing on SEPIC and Zeta converters highlights their capability to electrically isolate input and output voltages while providing non-inverting outputs [30], [31]. The Zeta converter is particularly notable for its robustness in managing fluctuating input voltages, ensuring a stable output that makes it well-suited for industrial applications that require a continuous, non-pulsating current [32], [33]. This characteristic of delivering a non-pulsating current significantly reduces noise and alleviates output capacitance requirements, enabling linear controllers to maintain stability across a broad spectrum of input conditions [1]. In contrast, the SEPIC converter exhibits a pulsating output. It involves complex control challenges due to the presence of an intrinsic right-half-plane zero, which renders it less favorable for applications that demand precise and steady voltage regulation [34], [35], [36]. Given these considerations, the Zeta converter is frequently the preferred option for achieving consistent and reliable voltage regulation.

With the choice of the Zeta converter established, designing an effective control strategy becomes crucial for maintaining its performance under dynamic conditions. Conventional controllers, such as proportional-integral-derivative (PID) and sliding-mode control (SMC), have been employed for DC-DC converters with varying levels of success [37], [38], [39]. For instance, [37] reformulates the sliding control law to regulate frequency, achieving impressive efficiencies of up to 95%. Nonetheless, challenges arise with trade-offs related to overshoot and settling time, as demonstrated in applications of SMC to a two-stage DC-DC boost converter [38]. Furthermore, conventional SMC designs often require high and variable switching frequencies, complicating filter design and potentially leading to increased switching losses [39].

In contrast, [40] investigates a programmable integrated PID controller for a DC-DC converter, which regulates a pulse width modulator (PWM) based on counter values and digital inputs. This controller demonstrates efficiency variations between 75% and 92% for output voltages ranging from 0.2V to 3.3V. Additionally, [41] suggests that employing multi-mode operations, including PWM and pulse frequency modulation (PFM), can enhance system efficiency; however, this improvement comes at the cost of increased complexity.

Recent advances have emphasized time-based methods for controlling DC-DC converters, utilizing time-domain processing of voltage signals to enhance regulatory efficiency and responsiveness. The evolution of these techniques is well-documented in prior research [11], [12], [13]. The work in [11] presents a theoretical framework for time-based control, which involves the conversion of voltage signals into current, followed by processing through a current-controlled oscillator (CCO) and a current-controlled delay line (CCDL). This approach effectively transforms the voltage difference into a phase difference, which is then analyzed by a phase detector to produce a PWM signal. This method simplifies the overall design and reduces power consumption and silicon area.

Building on this foundation, a 4-phase buck converter is implemented with time-based control, incorporating 16 current sources within a frequency-locked loop (FLL) to effectively address voltage offsets and enhance performance [12]. The technique is further advanced through a dual-mode mechanism that seamlessly switches between PWM and PFM, optimizing efficiency under varying load conditions and minimizing switching losses [13].

In contrast, an alternative method employs a voltage-controlled delay line (VCDL) paired with a preamplifier and phase-frequency detector (PFD) to ensure high precision and stability in phase generation during high-frequency switching. This approach illustrates a different strategy to achieve time-based control without relying on conventional analog components [14].

This paper presents an innovative PLL-based control strategy for Zeta converters designed to tackle the challenges associated with fluctuating input conditions in PDGs and industrial applications. By integrating essential components such as phase detectors and oscillators for effective phase and frequency synchronization, the proposed approach enhances the performance and stability of Zeta converters, offering a robust and adaptive solution that maximizes efficiency and responsiveness. This study aims to address the limitations of conventional control methods, significantly contributing to the reliability of power systems reliant on renewable energy sources while emphasizing the need for improved DC-DC converter operations under varying conditions, thus advancing practical applications in the power systems domain.

III. POWER STAGE ANALYSIS OF THE ZETA CONVERTER

This section, along with the appendix, provides an in-depth analysis of the Zeta converter's power stage, focusing on the derivation of the transfer function and the impact of parasitic resistances on system performance. The exploration explains how the converter's architecture and various resistive elements influence overall system dynamics and analyzes various design considerations necessary for developing effective control strategies.

A. POWER STAGE TRANSFER FUNCTION

The architecture of any DC-DC converter system consists of a power stage, a control unit, and a modulation mechanism. Figure 1 shows the power stage configuration of the Zeta converter.

A standard method for modeling this power stage utilizes the steady-state averaging (SSA) technique. This technique involves deriving the state-space equations specific to the Zeta converter, computing the steady-state average of the converter's dynamics, establishing the steady-state equations,

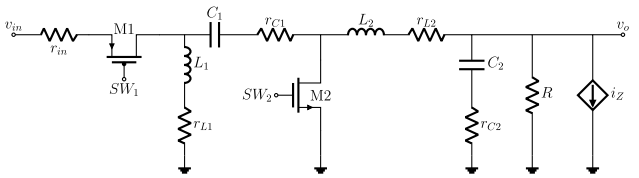


FIGURE 1. Zeta converter circuit used in the steady-state average technique.

and developing linearized small-signal state-space equations to extract the corresponding transfer functions. The reader can refer to the Appendix for detailed derivations of the SSA analytic expressions for the Zeta converter.

The transfer function of the Zeta converter, denoted as v_{od}, represents the ratio between the output voltage and the duty cycle of the PWM signal applied to the gate of the power transistor M1, which corresponds to the switching signal SW1. The parameter values used in the enhanced model are consistent with those in the reference study [33]: $C_1 = 100\,\mu$F, $C_2 = 200\,\mu$F, $R = 5\,\Omega$, $r_{C1} = 0.19\,\Omega$, $r_{C2} = 0.095\,\Omega$, $L_1 = 100\,\mu$H, $L_2 = 55\,\mu$H, $r_{L1} = 1\,$mΩ, $r_{L2} = 0.55\,$mΩ, $V_{\text{in}} = 20\,$V, and $v_{\text{o}} = 5\,$V. A 5V output v_{o} is obtained by setting the duty cycle to 0.21.

These parameters were chosen because they align with the steady-state averaging technique commonly used in the literature, particularly in [33]. This study builds upon that work by incorporating additional parasitic elements, such as inductor series resistance and the power transistor ON resistance, to more accurately model real-world performance. Although this parameter set is appropriate for demonstrating the effects of parasitic components, other values could also be selected to explore how different configurations impact the system's stability and behavior. The analysis allows plotting the system response illustrated in Figure 2, where the effects of varying these parameters are examined in detail.

B. EFFECTS OF PARASITIC RESISTANCES

In any practical converter system, parasitic resistances significantly influence the overall performance and stability of the system. Understanding how these resistances affect the Zeta converters behavior is critical for designing an effective control strategy. In this subsection, we examine the effects of key parasitic elements–specifically, the ON resistance of the power transistors and the inductor resistances–on the converter's transfer function. By analyzing how these resistances alter the gain and phase margins, we gain valuable insight into the system's sensitivity to parasitic effects and the necessary considerations for optimizing control performance.

The plots illustrate how varying the ON resistance r_{ds} of the power transistors and the inductor resistance can impact v_{od}. Initially, the effects of r_{ds} values of 0 mΩ, 100 mΩ, and 200 mΩ were examined while keeping the inductor resistance constant. The gain margins for these conditions are infinite, while the phase margins vary from 51.65° at $r_{ds} = 0\,m\Omega$ to 56.96° at $r_{ds} = 200\,m\Omega$.

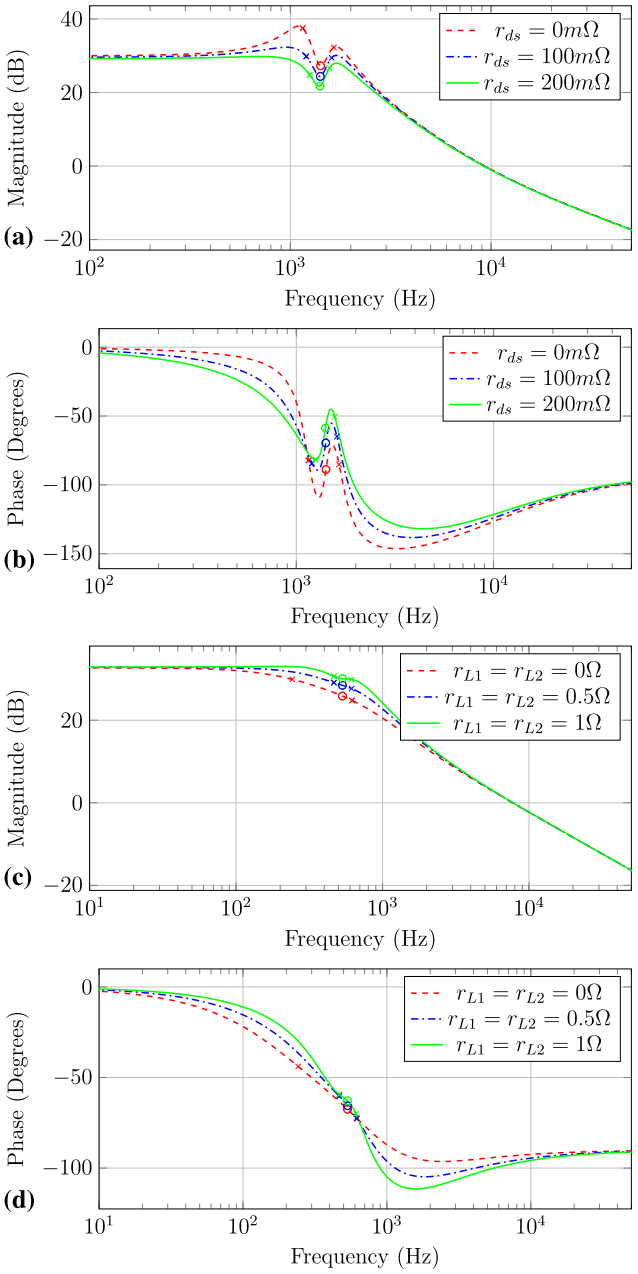


FIGURE 2. Bode plot analysis of the transfer function v_{od}. The plots characterize the effects of the power transistors ON resistances on (a) he magnitude and (b) the phase of the transfer function and the effects of the inductor resistance on (c) the magnitude and (d) the phase of the transfer function.

Subsequently, the inductor resistances $r_{L1} = r_{L2}$ were varied to 0 Ω, 0.5 Ω, and 1 Ω, while keeping r_{ds} fixed. The gain margins for these conditions are infinite, while the phase margins vary from 86.88° at $r_{L1} = r_{L2} = 0\,\Omega$ to 82.71° at $r_{L1} = r_{L2} = 1\,\Omega$.

Although the variation in gain margin is small, the shape of the bode plots is significantly different at frequencies below the crossover frequency. For example, the magnitude plot shows a deviation of around 4 dB at 1 kHz due to r_{ds} variation. This indicates that the system's low-frequency

behavior is highly sensitive to changes in both r_{ds} and the inductor resistances, which can substantially impact the overall stability and performance of the Zeta converter, and affect the design and effectiveness of the controller required for optimal system operation. This underscores the importance of including such considerations in the modeling process to ensure accurate control strategy development and validation.

IV. PLL-BASED CONTROLLER

PLL-based controllers have been presented in [11], [12], [14], and [15]. These approaches typically rely on time-domain circuits such as voltage-controlled oscillators (VCOs), phase detectors, and voltage-controlled delay lines to control DC-DC converters.

The control strategy in this work is built around a phase-locked loop (PLL) system, where a PFD and a lead-compensator circuit play critical roles in influencing the loop phase margin and enhancing system stability. While traditional PLL-based controllers have been widely used in DC-DC converters, as seen in [11], [12], and [14], the innovation in this work lies in several key aspects.

Firstly, integrating the lead compensator is a critical improvement in this design. The lead compensator has been incorporated here to enhance the transient response and increase the phase margin, essential for ensuring stability under dynamic conditions. Rather than addressing parasitic elements directly, the lead compensator works by improving the system's ability to handle fast changes in input or load conditions, reducing overshoot, and minimizing settling time. This makes it particularly valuable in real-world applications such as renewable energy systems, where input fluctuations are common. By introducing a phase lead, the compensator increases the system's bandwidth. It allows it to respond more quickly and accurately to changes, ensuring efficiency and stability over various operating conditions.

Secondly, a phase frequency detector (PFD) with a low-pass filter marks another distinction. While previous works, such as [11] and [12], rely on phase detectors and multiphase compensators, the proposed design employs a PFD and a low-pass filter. This configuration provides precise control over phase and frequency, improving transient response and phase margin. The ability to dynamically adjust and maintain the phase margin is a distinct advantage over traditional approaches, especially when dealing with fluctuating input conditions.

Thirdly, combining techniques for higher efficiency and stability sets this work apart. This design integrates a VCO-based controller, a PFD, and a lead compensator, offering a refined approach to DC-DC converter control. The system improves stability in response to parasitic effects and maintains high efficiency across various operating conditions. This combination provides practical solutions for applications such as renewable energy systems, where fluctuating inputs require robust and adaptive control mechanisms. In [15], a PLL-based buck converter was implemented using a VCO instead of traditional voltage comparators, similar to the delay-line-based PWM control approach in [14]. The current work builds on this by integrating the lead compensator to improve system stability and performance, particularly accounting for parasitic elements.

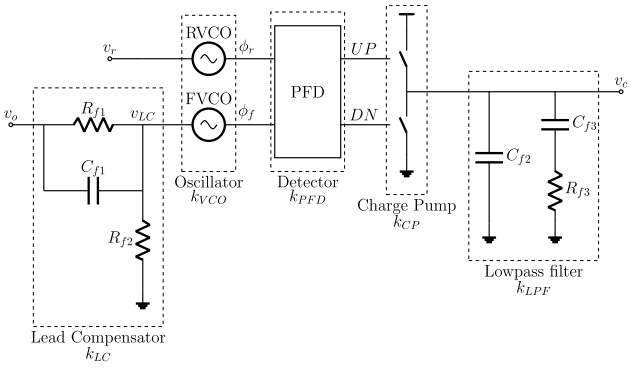


FIGURE 3. Block diagram of the proposed controller.

The block diagram of the proposed PLL-based controller is shown in the figure 3. The model is similar to the one proposed in [15], with the added input low-pass filter.

The proposed controller operates as follows: The output voltage of the power stage, denoted v_o, is first processed through a lead compensator. In this configuration, the resistors R_{f1} and R_{f2} act as a voltage divider to effectively manage voltage levels, while the capacitor C_{f1} introduces a low-frequency zero, in the range of hundreds of Hertz, to enhance the dynamic response of the system. The output from the lead compensator, denoted v_{LC}, and the reference voltage v_r, are transformed into their corresponding phases, ϕ_f and ϕ_r, respectively, by matched voltage-controlled oscillators (VCOs).

The phase frequency detector (PFD) generates an *UP* signal when $\phi_f < \phi_r$, and a *DN* signal when $\phi_f > \phi_r$. These signals control the charge pump source and sink switches, respectively. Depending on the phase comparison outcome, they modulate the control voltage v_c to increase or decrease it. This dynamic adjustment mechanism ensures the control voltage is continuously modified to maintain system stability and optimal performance.

To provide a clear understanding of how each component contributes to the overall functionality of the controller, the transfer functions of these components are detailed below:

- Lead Compensator (*LC*):

$$k_{LC}(s) = \beta \frac{s\tau + 1}{\beta s\tau + 1}$$

  where $\tau = R_{f1}C_{f1}$ and $\beta = \dfrac{R_{f2}}{R_{f2} + R_{f1}}$.
- Voltage-Controlled Oscillator (*VCO*):

$$k_{VCO}(s) = \frac{K_V}{s}$$

  where $K_V = \dfrac{df_{VCO}}{dv_{LC}}$ is the gain of the VCO.

TABLE 1. Poles and zeroes information of the controller building blocks.

Component	Zeroes	Poles
VCO	None	0
LPF	$-\frac{1}{\tau_{33}}, \infty$	$0, -\frac{1}{\tau_{33}} - \frac{1}{\tau_{32}}$
PFD	None	None
LC	$-\frac{1}{\tau}$	$-\frac{1}{\beta\tau}$
CP	None	None

$\tau_{33} = R_{f3}C_{f3}$
$\tau_{32} = R_{f3}C_{f2}$

- Phase Frequency Detector (*PFD*):

$$k_{PFD}(s) = \frac{1}{2\pi}$$

- Charge Pump (*CP*):

$$k_{CP}(s) = I_{cp}$$

where I_{CP} is the charge pump current.

- Low Pass Filter (*LPF*):

$$k_{LPF}(s) = \frac{1}{C_{f2}} \cdot \frac{s + \frac{1}{R_{f3}C_{f3}}}{s\left(s + \frac{1}{R_{f3}C_{f3}} + \frac{1}{R_{f3}C_{f2}}\right)}$$

The poles and zeroes information of the controller are summarized in Table 1. The overall transfer function, which defines the relationship between the control voltage v_c and the output voltage v_f, is derived as the product of the transfer functions of the individual components:

$$\frac{v_c}{v_o}(s) = k_{LC}(s) \times k_{VCO}(s) \times k_{PFD}(s) \times k_{CP}(s) \times k_{LPF}(s) \tag{1}$$

This breakdown explains the controller's operation and facilitates tuning and optimization for more robust and responsive system control.

A. CIRCUIT IMPLEMENTATION

1) VOLTAGE CONTROLLED OSCILLATOR

The voltage-controlled oscillator circuit, as presented in Figure 4, comprises three primary stages: the control stage, the delay stage, and the output buffer stage.

a: CONTROL STAGE

The control stage generates two analog voltages that regulate the source and sink currents of the delay stages. A PMOS transistor is incorporated in this stage, with its gate connected to the input voltage to facilitate VCO functionality at zero input voltage. Figure 5 illustrates the input-output characteristics of the control stage.

b: DELAY STAGES

These stages consist of conventional current-starved inverters. The switching speeds of each stage, both for high-to-low and low-to-high transitions, are influenced by the source and sink currents, respectively. The currents are determined by:

- The width-to-length (W/L) ratio of transistors $P_{up,(n)}$ and $N_{dn,(n)}$.
- The gate capacitance of the subsequent stage.
- The control voltages P and N.

Increasing the source current can be achieved through an increased W/L ratio of $P_{up,(n)}$, reduction in the W·L product of $P_{dn,(n+1)}$ and $N_{up,(n+1)}$ for the subsequent stage, and a decrease in control voltage $V_{P(n)}$. Similarly, an increase of the sink current can be realized by increasing the W/L ratio of $N_{dn,(n)}$, reducing the W·L product of the next stage's transistors, and increasing the control voltage $V_{N(n)}$. Additionally, the number of stages, which is always odd, significantly impacts the VCO frequency. Reducing the number of stages increases the oscillator frequency, demonstrating the inverse relationship between stage count and frequency. This configuration ensures tailored frequency adjustments to meet specific operational requirements.

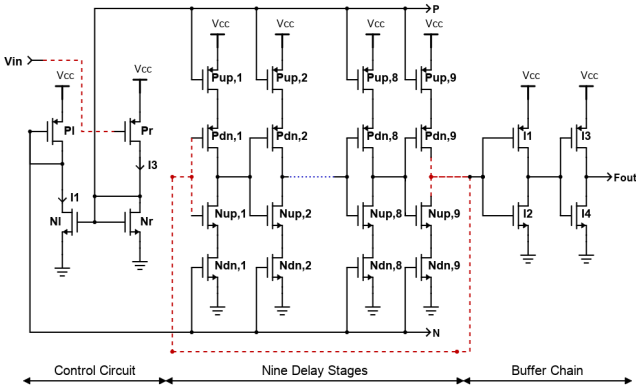


FIGURE 4. Voltage-controlled oscillator circuit implementation.

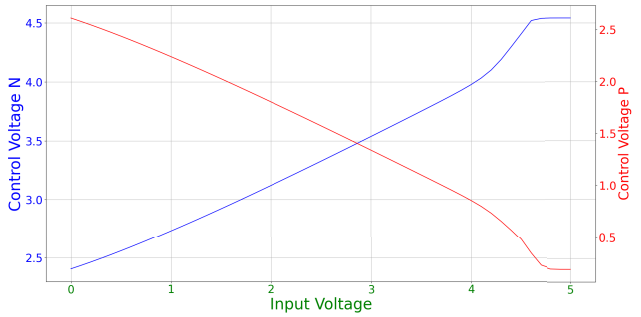


FIGURE 5. Variations of the control voltages P and N to the input voltage V_{IN}.

2) PHASE FREQUENCY DETECTOR

A typical PFD implementation is shown in Figure 6, where the PFD and charge pump's dead zone problems are mitigated using the delay block. The dead zone in a PFD occurs when

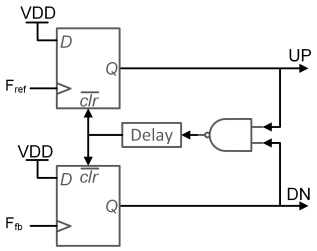


FIGURE 6. Circuit implementation of the phase frequency detector.

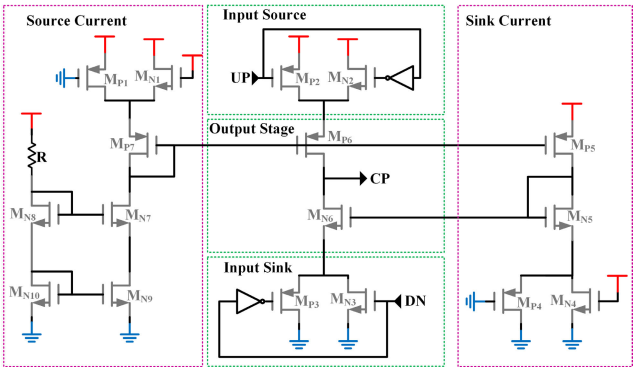


FIGURE 7. Charge pump transistor-level implementation.

the phase difference between the reference and VCO signals is too small to generate an output, leading to instability in Phase-Locked Loops (PLLs). Introducing a delay block in the reset path ensures the detection of even small phase differences, thereby eliminating the dead zone and enhancing PLL performance [42].

3) CHARGE PUMP

Figure 7 illustrates the implementation of the charge pump circuit. To generate the source current, a cascode current source configuration is used, while the sink current is produced by directing the current through a network of transistors: M_{P7}, M_{P5}, M_{N5}, and M_{N6}. To mitigate the negative effects of charge injection and clock feed through, two techniques are employed:

1) **Switch in Source Approach:** This method switches the charge away from the output using the input source and input sink blocks, as recommended in [43]. It reduces the direct path of the charge to the output, minimizing disturbances.
2) **Transmission Gate Switching:** Instead of using a single transistor for switching, this method uses transmission gates composed of M_{P2}, M_{N2}, M_{P3}, and M_{N3}. Transmission gates enhance the control over the switching process, offering a more balanced and efficient charge transfer mechanism, further reducing potential errors from charge injection and clock feed through.

Implementing these techniques will allow the charge pump to operate more stably and efficiently, ensuring the voltage levels within the circuit are maintained with integrity and reliability.

V. PHASE MARGIN GRAPHICAL APPROACH

One of the main challenges in control systems is tuning the parameters of the controllers. After identifying the controller type, parameter tuning becomes an optimization problem. In the literature, commonly used methods for controller design include the boundary locus approach [44] or calculating specific controller parameters to achieve desired gain and phase margins [45]. The following efficient algorithm is proposed for the phase margin method involves the following steps:

1) Produce the Bode plot for the power stage transfer function, denoted as G. Extract the gain and its rate of change at the crossover frequency, f_c.
2) Produce the Bode plot for the inverse transfer function of the controller, denoted as $\frac{1}{H}$. Determine the rate of change of $\frac{1}{H}$ at f_c.
3) Adjust the poles and zeros of H such that the Bode plots of G and 1/H intersect at f_c. At their intersection, ensure that the rate of change of $\frac{1}{H}$ equals the rate of change of $G + 20$ dB/dec.
4) Validate the system response by examining the gain margin and phase margin of the open loop, as well as the step response of the closed loop.

The crossover frequency is when the loop gain (GH) equals 0 dB. In simple terms, it is the point where the gain Bode plots of G and 1/H intersect. Additionally, the rate of change of the gain plot can help determine the phase value. When the rate of change is $+20$ dB/dec $\times K$, the phase approaches $+90° \times K$. By comparing the differential rate of change between G and $\frac{1}{H}$, the system's phase can be estimated. This methodology helps to ensure that the system's phase margin approaches 90°, resulting in better stability and performance.

VI. EXPERIMENTAL SETUP AND MEASUREMENT RESULTS

This section details the closed-loop Zeta converter system's experimental setup, measurement results, and proposed control methodology. The objective is to validate the theoretical analysis and design outlined in the preceding sections through comprehensive testing and evaluation. It begins with selecting parameters and deriving the transfer function, followed by the experimental setup. It concludes by discussing the measurement results, including efficiency, reference tracking, line regulation, and load regulation.

A. PARAMETER SELECTION AND TRANSFER FUNCTION

To test the methodology proposed in Section V, a Zeta converter is considered as shown in Figure 1 characterized by the following parameters: $C_1 = C_2 = 220\mu F$, $r_{C1} = r_{C2} = 300m\Omega$, $L_1 = L_2 = 220\mu H$, $r_{L1} = r_{L2} = 10m\Omega$, $r_{ds} = 250m\Omega$ and $f_{sw} = 85KHz$.

TABLE 2. Frequency, gain, phase, and pole/zero information of the Zeta converter.

Frequency (Hz)	Gain (dB)	Phase (degrees)	Type
467	31	-63	Double Pole
532	30	-59	Double Zero
608	31	-63	Double Pole
1657	16	-116	Zero

TABLE 3. Frequency, gain, phase, and pole/zero information for the inverse controller transfer function.

Frequency (Hz)	Gain (dB)	Phase (degrees)	Type
0	N/A	N/A	Double Zero
7.7×10^{-11}	-252	135	Pole
318	-0.58	45.82	Pole
28,012	5.73	60.39	Zero
106,421	17.32	120.42	Zero
∞	N/A	N/A	Pole

By substituting these component values into Equation 8 from the Appendix, the transfer function of the Zeta converter will be the following, as shown in the equation at the (bottom) of the next page.

From this transfer function, the pole-zero information of the Zeta converter can be obtained, as summarized in Table 2. The response is almost flat for frequencies below 467 Hz, and the rate of change is practically zero. Thus, if the crossover frequency is planned in this region, a 20 dB/Dec rate of change of $\frac{1}{H}$ is needed, achievable by a low-frequency integrator. Between 467 Hz and 532 Hz, the system has a double pole, where the rate of change of the power stage would be -40 dB/Dec. If the crossover frequency is established in this region, a rate of change of -20 dB/Dec is required for $\frac{1}{H}$, achievable by a differentiator. Between 532 Hz and 608 Hz, the power stage shows a double zero, which causes the system response to revert to a rate of change of 0 dB/Dec. At this point, using an integrator is enough to control the system. As the frequency increases from 608 Hz to 1657 Hz, the rate of change becomes -40 dB/Dec, requiring a differentiator. Beyond 1657 Hz, the number of poles will exceed the number of zeros by one, resulting in a rate of change of -20 dB/Dec, and the controller's required rate of change will be 0 dB/Dec, achievable using a proportional controller.

The following specifications were used for the controller: $K_V = 27.5$ MHz/V, $I_{cp} = 16$ mA, $R_{f3} = 45$ kΩ, $C_{f2} = 46.6$ pF, and $C_{f3} = 125$ pF. When modulating the power stage, a transfer function gain of 0.18 was used for the pulse width modulator. Using these controller parameters and the transfer function relations outlined in Section IV, the following transfer function was derived:

$$H(s) = \frac{9.1932 \times 10^9 s^2 + 1.8386 \times 10^{13} s + 8.9283 \times 10^3}{0.0904\, s^4 + 61290.8\, s^3 + 7.9872 \times 10^9 s^2}$$

With all the necessary information, the Bode plot depicted in Figure 8 can now be generated. This plot reveals that the Zeta converter's transfer function and the controller's inverse transfer function intersect at a crossover frequency of 6.1 KHz. The system's gain margin is 26.71 dB, and the phase margin is 56.02 degrees, demonstrating the accuracy of the analysis.

In the design, the switching frequency was set to 85 kHz. A common guideline to ensure stability in a Zeta converter is to set the crossover frequency below 0.1 times the switching frequency. Consequently, a target crossover frequency below 8 kHz was aimed for. This target is achieved by optimizing the ratio of R_{f1} to R_{f2} in Figure 3.

B. EXPERIMENTAL SETUP

A closed-loop Zeta converter was implemented to assess the system's performance using both the power stage and controller transfer functions. The block diagram of the system is shown in Figure 9, and the test setup details are provided in Figure 10. The Zeta converter's performance was evaluated through real-time simulations and hardware-in-the-loop testing. To push the controller's limits without the risks associated with extreme voltage values at high-duty cycles, PLECS (Piecewise Linear Electrical Circuit Simulation) [46] was used for rapid prototyping, allowing for precise control and measurement of the converter's behavior under various conditions and enabling a thorough analysis of its performance and stability.

The controller was implemented using high-voltage X-FAB 180 nm technology, as illustrated in Figure 11. This technology was selected for its capability to handle high-voltage operations while providing robust performance and reliability. The manufactured chip, shown in the left micrograph with the corresponding layout implementation on the right, has an active design area of the controller of $0.057mm^2$. This highlights the successful integration of the controller into a compact and efficient design. This chip implementation underscores the practical applicability of the design beyond mere simulation, validating the controller's effectiveness in real-world scenarios.

In the experimental setup, the RT Box 1 scales down the output voltage and reference signals using the lead compensator R_{f1}, R_{f2}, and C_{f1}. Both signals are sent through the analog breakout board to the VCOs inside the chip. The chip analyzes these signals and generates the corresponding analog control signal. The function generator produces a Sawtooth signal, which is compared with the chip's analog control voltage through an off-chip LM311P comparator to create the pulse width modulated (PWM) signal. The RT Box 1 reads the PWM signal via the digital breakout board interface and modulates the power stage of the Zeta converter. The output of the Zeta converter, along with other signals, is sent to the oscilloscope for proper measurements and analysis.

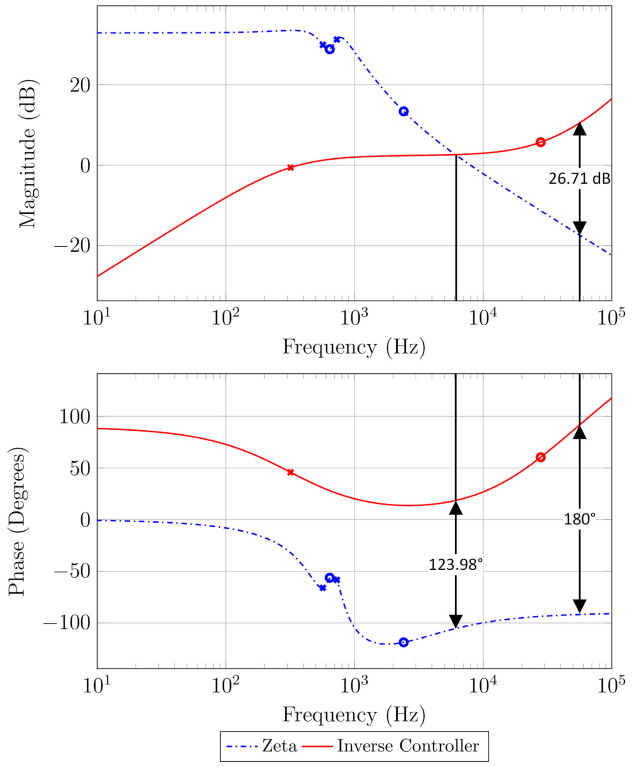


FIGURE 8. Graphical analysis of the closed-loop system. Bode plot of the Zeta converter (dashed blue) and the inverse controller (red). From this approach, the gain margin is 26.71 dB, and the phase margin is $180° - 123.98° = 56.02°$.

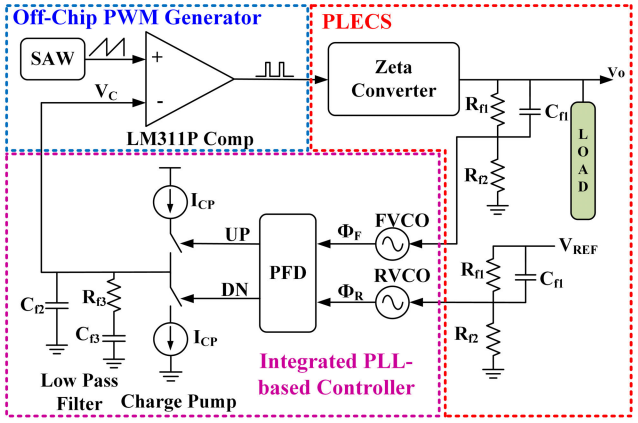


FIGURE 9. Block diagram of the proposed closed-loop Zeta converter system implementation.

C. MEASUREMENT RESULTS

For the rest of the measurements, the output of the Zeta converter is generated by the RT Box 1 as shown in Figure 9. Due to the RT Box 1's analog output limit of 10 V, the signal was scaled down within the RT Box 1 by a factor of 10. Correspondingly, the measurement values were increased at

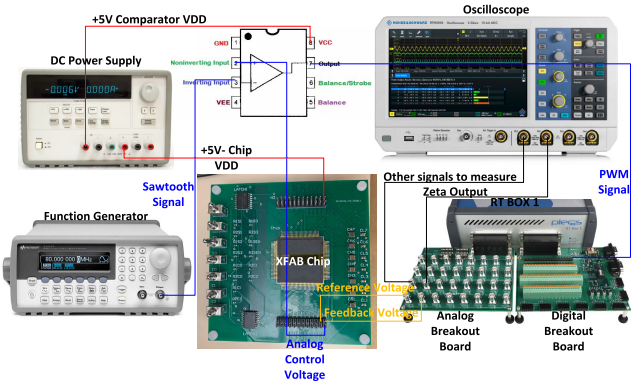


FIGURE 10. Testbench setup.

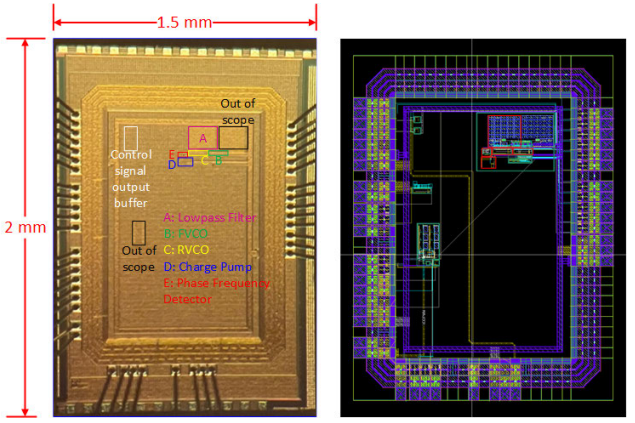


FIGURE 11. Micrograph of the fabricated chip (left) and its layout implementation (right).

the oscilloscope by a factor of 10 by adjusting the probe setup option.

The measurements began with an efficiency test. Using the PLECS RT Box 1, the efficiency was determined by combining measurements and emulation. First, the efficiency for various duty cycle ratios was measured with a constant load resistance value of 20 Ω.

Figure 12 presents the efficiency measurements of the Zeta converter across various duty cycles. It was observed that the efficiency is lower at both extremes of the duty cycle range. At low-duty cycles, the efficiency is reduced primarily due to resistive losses. Specifically, the output voltage is low at these duty cycles, meaning that a higher proportion of the input power is dissipated in the components' equivalent series resistance (ESR) rather than converted to useful output power. This is evident from the reported results, in which efficiency values are around 37% when the duty cycle is 0.05.

At high-duty cycles, the efficiency degradation can be attributed to capacitor charging dynamics and inductor-related limitations. Despite the ideal model for transistors in

$$\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{4.78159 \times 10^4 s^3 + 5.51494 \times 10^8 s^2 + 1.09226 \times 10^{12} s + 5.58216 \times 10^{15}}{s^4 + 4.24921 \times 10^3 s^3 + 2.76155 \times 10^7 s^2 + 5.16123 \times 10^{10} s + 1.26020 \times 10^{14}}$$

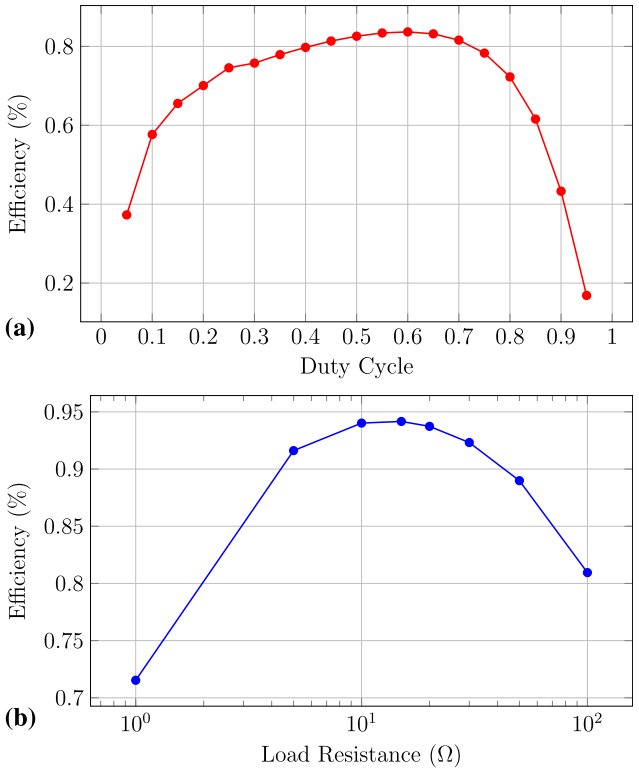
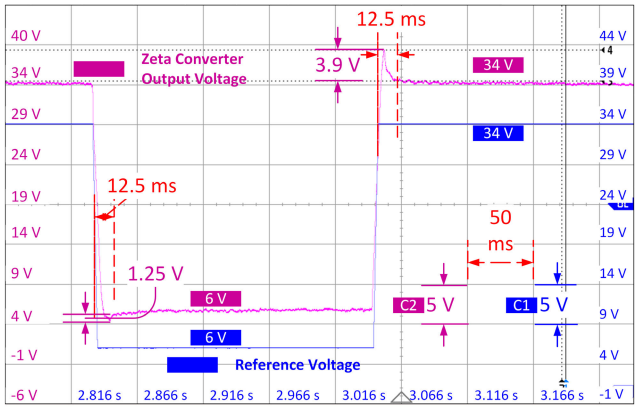
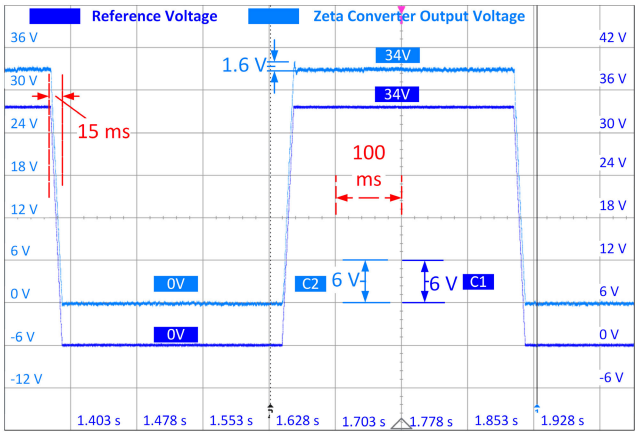


FIGURE 12. Effects of (a) the duty cycle and (b) the load resistance on the system's efficiency.



(a) System response to a reference voltage change from 6V to 34V with a load resistance of 100 Ω^*.



(b) System startup response with a reference voltage change from 0V to 34V and a load resistance of 10 kΩ^*.

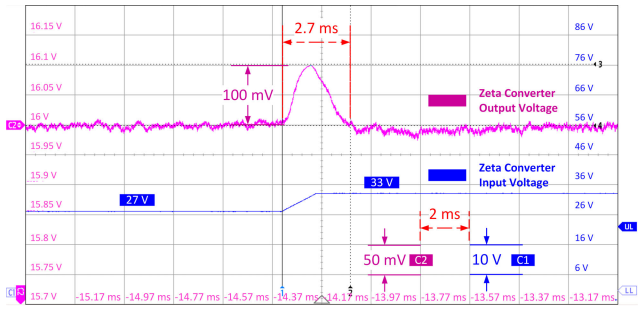
FIGURE 13. System responses for a Zeta converter: (a) reference tracking showing both buck and Zeta modes (pink curve - left y-axis, blue curve - right y-axis), and (b) startup response (light blue curve - left y-axis, dark blue curve - right y-axis).

the PLECS in which the power transistors act as a resistor when the gate voltage is greater than 0 (resistor when on, open circuit when off), the output voltage does not increase proportionally with the duty cycle as expected from the theoretical relationship $v_{out} = \frac{v_{in} \cdot D}{1-D}$. For instance, at a duty cycle of 0.95, the theoretical output voltage should be 532V, given an input voltage of 28V, but the RT Box 1 indicates a value of 90.33V. This significant discrepancy suggests that the capacitor is not fully charging during the switching cycles, leading to incomplete energy transfer. Additionally, the inductor may not transfer sufficient energy to the load within the switching period, causing further differences between the ideal model and the physical system.

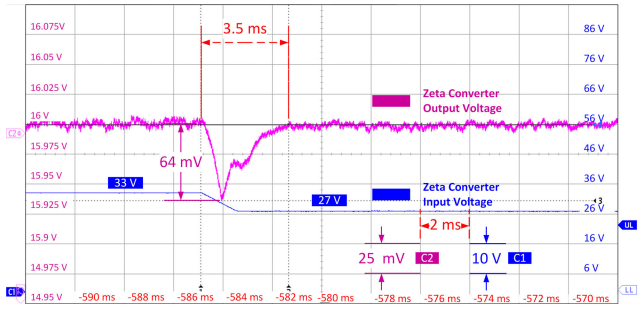
The efficiency curve peaks around mid-range duty cycles (0.5 to 0.7), where the balance between input power and resistive losses is optimized. For example, at a 0.6 duty cycle, the efficiency reaches approximately 83.68%, the highest observed efficiency for that loading condition. This analysis highlights the need to consider both low- and high-duty cycle effects when designing and optimizing power converters to ensure maximum efficiency across the entire operating range.

Next, the efficiency measurements were continued by focusing on the effect of load changes on the efficiency, as shown in Figure 12. At high resistance values, the efficiency is reduced, primarily due to high resistive losses relative to the output power. When the load resistance is low, the current through the converter increases significantly, leading to a substantial voltage drop across the power transistors and the capacitor's series resistance determined by its ESR. This causes the output voltage to drop, which in turn reduces the efficiency. High current levels worsen resistive losses, thus degrading the overall efficiency. By varying the duty cycle and load resistance, the system achieved a peak efficiency of 94% at a load resistance of 10 Ω, corresponding to a load current of 3A.

The second set of measurements conducted was reference tracking. In this setup, a reference signal was generated from the RT Box 1, and the output of the Zeta converter was measured. The input voltage of the Zeta converter was set at 28 V. The load resistance was set at 100 Ω, then the reference signal was varied from 6 V to 34 V. Figure 13a shows that the Zeta converter (Pink - left y-axis) successfully tracked the reference signal (Blue - right y-axis), verifying its buck functionality at 6 V and boost functionality at 34 V. The peak overshoot was measured at 3.9 V, with a settling time of 12.5 ms. A similar set of measurements was conducted to evaluate the system's startup response, showcasing the versatility of the proposed Zeta

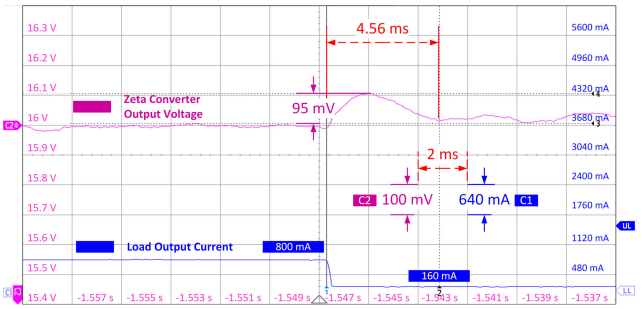


(a) System response to a line regulation change from 27V to 33V*.

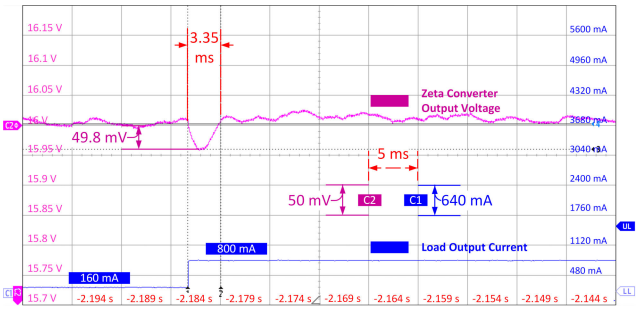


(b) System response to a line regulation change from 33V to 27V*.

FIGURE 14. Closed-loop transient line regulation for a Zeta converter response to a 6V change in input voltage: (a) with source changing from 27V to 33V (pink curve and left y-axis, blue curve, and right y-axis) and (b) source changing from 33V to 27V, with a 16V reference voltage and load resistance of 100 Ω.



(a) System response to a load regulation change from 800mA to 160mA*.



(b) System response to a load regulation change from 160mA to 800mA*.

FIGURE 15. Closed-loop transient load regulation for a Zeta converter response to a 640mA change in load current: (a) with current changing from 800mA to 160mA (pink curve and left y-axis, blue curve, and right y-axis) and (b) load current changing from 160mA to 800mA, with a 16V reference voltage and an input voltage of 28V.

converter under varying operating conditions. In this test, the reference voltage was set to drop to 0 V, and the load resistance was increased to 10 kΩ. As shown in Figure 13b, the Zeta converter (Light blue - left y-axis) successfully tracked the reference signal (Dark blue - right y-axis) with a reduced overshoot of 1.6 V. This reduction in overshoot is attributed to the higher load impedance, which moderates the converter's response and results in smoother startup behavior. It should be noted that because the power stage and load were modeled using a PLECS, the limitation in output current was primarily due to the IR drop across the ON resistance of the power stage and the inductor and capacitor series resistances. An attempt was made to replicate the reference tracking experiment from 0 V to 34 V with a 5Ω load. Still, the performance was unsatisfactory due to the reduction in phase margins, which affected the converter's ability to handle the lower load impedance. However, although not shown in the figure, we achieved good performance at 5Ω when the target output voltage was reduced to 20V, indicating the converter's capability to adapt under certain constraints.

The next test conducted was the line regulation. The same parameters were maintained as in the first reference tracking test. However, this time, the reference signal was kept fixed at 16 V, and the Zeta converter input voltage was varied from 27 V to 33 V (Figure 14a) and then from 33 V back to 27 V (Figure 14b). For a given duty cycle of the PWM signal, when the input voltage of the power stage increases, the Zeta converter output voltage initially increases, surpassing the reference. The control loop then reduces the output voltage and returns it to its target value. During this period, the output voltage increases by 100 mV, which took around 2.7 ms to return to its nominal value, as shown in Figure 14a. The opposite occurs when the input voltage decreases from 33 V to 27 V. In this case, the peak undershoot is 64 mV, which took 3.5 ms to settle, as shown in Figure 14b.

The last test conducted was the load regulation. The same parameters were maintained as in the line regulation test. However, the Zeta converter input voltage was kept at 28 V this time. The load current was varied from 800 mA to 160 mA (Figure 15a) and then from 160 mA back to 800 mA (Figure 15b). For a given duty cycle of the PWM signal, when the load current of the power stage decreases, the Zeta converter output voltage initially increases, surpassing the reference. The control loop then activates to reduce the output voltage and return it to its target value. During this period, the output voltage increases by 95 mV, which took around 4.56 ms to return to its nominal value, as shown in Figure 15a. The opposite occurs when the load current increases from 160 mA to 800 mA. In this case, the peak undershoot is 49.8 mV, which took 3.35 ms to settle, as shown in Figure 15b.

*Note (for readability): the distinct pink y-axis on the left is for the Zeta converter, and the blue y-axis on the right is for other types of measurements.

To quantify the transient performance of the closed-loop system and make a proper comparison with papers using different parameters of the power stage and the controller, two parameters were introduced: the normalized transient line regulation (NT_{line}) and the normalized transient load regulation (NT_{load}). They are defined as follows:

$$NT_{\text{line}} = \frac{\Delta V_{\text{out}} \times \text{Number of Cycles to Recover}}{\Delta V_{\text{in}}}$$

$$NT_{\text{load}} = \frac{\Delta V_{\text{out}} \times \text{Number of Cycles to Recover}}{\Delta I_{\text{load}}}$$

where:

- ΔV_{out} is the change in output voltage during the transient.
- ΔV_{in} is the change in input voltage causing the transient.
- ΔI_{load} is the change in load current causing the transient.
- Number of Cycles to Recover is the number of switching cycles required for the output to return to its steady-state value, calculated as the product of the switching frequency f_{sw} and the recovery time T_{rec}.

NT_{line} and NT_{load} represent the ratio of the output voltage deviation to the input voltage change or load current change and the recovery time measured in cycles. Smaller values indicate better performance, as they signify that the system stabilizes quickly and with minimal deviation when subjected to significant source voltage or load variations. These parameters offer a fair comparison by normalizing transient response characteristics, which makes assessing different controllers' effectiveness easier regardless of specific operating conditions or configurations.

While steady-state line and load regulation are commonly implemented in the literature [4], their values are less relevant because an RT Box 1 was used instead of discrete components for the power stage, eliminating wire IR losses.

The performance metrics were assessed under various testing conditions to thoroughly evaluate the system's dynamic behavior, primarily focusing on the normalized line and load transients. The line and load regulation tests were repeated across various switching frequencies to further analyze the system's stability under different operating conditions, as illustrated in Figure 16. The experiment aimed to achieve two objectives: first, to evaluate the Zeta converter's performance at different frequencies, and second, to validate the proposed normalized parameters–normalized load regulation and normalized line regulation–as reliable metrics for system assessment. While it was initially anticipated that these transients would remain consistent across varying conditions, the results revealed some minor variations. However, such slight deviations do not significantly impact the system's performance. The observed fluctuations can likely be attributed to the frequency-dependent characteristics of the inductor and capacitor, affecting energy transfer efficiency during transients. Despite these variations, the system demonstrated consistent and stable regulation, underscoring the robustness of the design and confirming the validity of the normalized

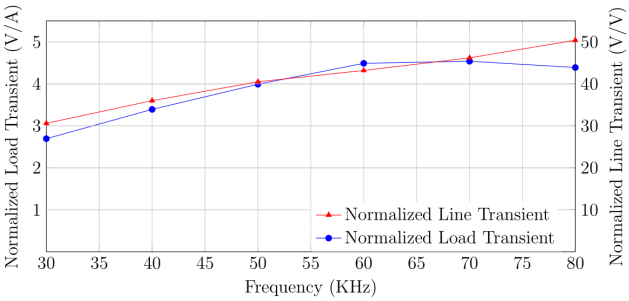


FIGURE 16. Normalized Line and Load Transient (NLT) values of the Zeta converter under various frequencies.

transient parameters across a broad range of operating frequencies.

The performance of this work is compared with other references in the literature in Table 4. It presents various controllers' performance metrics, particularly emphasizing the normalized line and load transients and the peak efficiency.

Table 4 shows that this work and the work in [47] were implemented using CMOS technology, while the other works used discrete components. The control strategies vary significantly between each work, ranging from voltage mode control [47], current mode control [48], dual control loop strategies [48], [49], to sliding mode control [50]. The switching frequency, input voltage, output voltage, and load resistance differ significantly between each design.

The line transient response provides critical information. Despite being subjected to the most significant input voltage change, the SMC controller achieved the lowest output voltage change but at the expense of a considerable recovery time. The normalized transient line regulation could not be obtained for the SMC controller as its switching frequency is not constant. Compared to other references, this work achieved the best normalized transient response, demonstrating minimal output voltage change and the fastest recovery time relative to significant input variations.

Regarding load regulation, the system achieved the lowest voltage spikes in response to significant changes in load current. The system performed second in normalized transient load regulation among the other references. The best one is [47], requiring fewer cycles to achieve recovery. Regarding efficiency, while the reported values across various studies were commendable, [49] achieved a notable peak efficiency of 94.2%. Our work closely follows with a peak efficiency of 94% at a 3A load, demonstrating highly competitive performance and validating the effectiveness of our control strategy.

This work demonstrates superior performance in normalized transient line and load regulation, indicating that the system stabilizes quickly and with minimal deviation. These results, combined with competitive efficiency, highlight the proposed controller's robustness and effectiveness in practical applications.

TABLE 4. Comparison of various controllers.

Reference	[47]	[49]	[48]	[51]	[50]	This Work
CMOS technology	0.25 HV	Discrete	Discrete	simulation	Discrete	X-Fab 0.18 HV
Controller feedback	voltage	dual	dual	current	SMC	voltage
F_{sw} (KHz)	500	100	50	20	N/A	85
V_g (V)	9 - 21	48	$9^{(b)}$	$10^{(b)}$	$15^{(b)}$	28
V_o (V)	6	400	$129^{(b)}$	$15^{(b)}$	$100^{(b)}$	0 - 34
R_L (Ω)	30 $\leftrightarrow$ 300	1.39 $\leftrightarrow$ $533^{(a)}$	$24^{(b)}$	1 $\leftrightarrow$ 1000	$1000^{(b)}$	10 $\leftrightarrow$ 10000
Core Area (mm^2)	1.22	N/A	N/A	N/A	N/A	0.069
Line Transient (V)	N/A	48 $\leftrightarrow$ 58	9 $\leftrightarrow$ 15	10 $\rightarrow$ 18	0 $\rightarrow$ 100	27 $\leftrightarrow$ 33
$\pm$ Spike (mV)	N/A	N/A	1000	$750^{(a)}$	4	-64 $\leftrightarrow$ 100
T_{rec} (μs)	N/A	N/A	5000	$7500^{(a)}$	14000	3100
Normalized Line Transient	N/A	N/A	41.66	14	N/A	4.39
Load Transient (mA)	$\pm$ 980	$\pm$ 3000	$\pm$ 750	+120	$\pm$ 166	$\pm$ 640
$\pm$ Spike (mV)	$\pm$ 250	$\pm$ 10000	$700^{(a)}$	$250^{(a)}$	$1700^{(a)}$	+95 -50
T_{rec} (μs)	26-30	4000	$30000^{(a)}$	$5000^{(a)}$	$10000^{(a)}$	4000
Normalized Load Transient	3.31	1333	1400	208	N/A	50.4
Peak Efficiency (%)	86.4 @ 500mA	94.2 @ 240W	N/A	N/A	N/A	94 @ 3A

[a] Estimated from paper plots
[b] Nominal values mentioned in the paper

VII. CONCLUSION

This paper presented a systematic approach for controlling a Zeta power converter using a PLL-based controller. This work highlights the versatility and robustness of the Zeta converter in applications requiring reliable voltage regulation under fluctuating conditions. The proposed model considers essential parameters such as the ON resistance of power transistors and inductor series resistance, ensuring accurate system behavior representation.

The effectiveness of the control strategy was demonstrated through extensive measurements and empirical validation using the PLECS RT Box 1 combined with a prototype integrated circuit fabricated with the X-Fab 180nm technology. The proposed graphical design approach using Bode plots facilitated intuitive controller tuning, achieving an excellent tradeoff between stability and performance.

Experimental results showed that the proposed system achieved superior normalized transient line and load regulation, with minimal deviation and quick stabilization under significant input voltage and load variations. The efficiency measurements indicated that the system performs exceptionally well across a wide range of duty cycles and load resistances, achieving a peak efficiency of 94% with a load resistance of 10 Ω.

The PLL-based Zeta converter control approach offers a promising solution for renewable energy systems, automotive power distribution grids, and other applications demanding consistent voltage regulation. Future research will focus on further optimizing the control strategy and exploring its application in more complex power management scenarios.

APPENDIX: ZETA CONVERTER MODELING USING STEADY-STATE AVERAGE TECHNIQUE

The architecture of DC-DC converters consists of a power stage, a control unit, and a modulation mechanism. Figure 1 presents the system architecture of the power stage configuration of the Zeta converter.

A prominent method for modeling these converters utilizes the steady-state averaging (SSA) technique, which is applied as follows [33], [52]:

1) Derive the state-space equations specific to the Zeta converter.
2) Compute the steady-state average of the converter's dynamics.
3) Establish the steady-state equations.
4) Develop linearized small-signal state-space equations and extract the corresponding transfer functions.

A. STATE-SPACE EQUATIONS FOR THE ZETA CONVERTER

The following state-space equations describe the dynamic behavior of the DC-DC Zeta converter:

$$\begin{cases} \dfrac{dx(t)}{dt} = \mathbf{A}\mathbf{x}(t) + \mathbf{B}u(t) \\ \mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) + \mathbf{D}u(t) \end{cases} \tag{2}$$

Equation 2 represents the nonlinear continuous-time dynamics of the converter, which can be linearized using small-signal perturbation methods to obtain:

$$\begin{cases} \mathbf{x} = \mathbf{X} + \tilde{\mathbf{x}} \\ \mathbf{u} = \mathbf{U} + \tilde{\mathbf{u}} \\ \mathbf{d} = \mathbf{D} + \tilde{\mathbf{d}} \\ \mathbf{y} = \mathbf{Y} + \tilde{\mathbf{y}} \end{cases} \tag{3}$$

The inductor and capacitor components principally govern the operational dynamics of DC-DC converters. For the Zeta converter shown in Figure 1, the system's state ($\mathbf{x}(t)$), input ($\mathbf{u}(t)$), and output ($\mathbf{y}(t)$) variables can be presented as follows:

$$\mathbf{x}(t) = \begin{pmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{pmatrix}, \quad \mathbf{u}(t) = \begin{pmatrix} V_{in} \\ i_Z \end{pmatrix}, \quad \mathbf{y}(t) = \begin{pmatrix} v_o \end{pmatrix}. \tag{4}$$

Note that i_Z is added to model the output impedance. In normal operation, the current source is removed.

B. SSA OF THE ZETA CONVERTER

Following the establishment of the system's state-space representation, the subsequent phase involves calculating the matrices $\mathbf{A_S}$, $\mathbf{B_S}$, $\mathbf{C_S}$, and $\mathbf{E_S}$ that fulfill the requirements set by equation 2. Operating in continuous conduction mode, a DC-DC converter transitions between two operational states based on the modulation of the control signal's pulse width. Accordingly, the matrices $\mathbf{A_S}$, $\mathbf{B_S}$, $\mathbf{C_S}$, and $\mathbf{E_S}$ are determined for both the charging phase (when SW1 is activated and SW2 is deactivated) and the discharging phase (when SW1 is deactivated and SW2 is activated). The application of circuit analysis techniques yields the steady-state average (SSA) parameters as follows:

$$
\begin{aligned}
\mathbf{A} &= \begin{bmatrix} \mathbf{A_1} & \mathbf{A_2} & \mathbf{A_3} \end{bmatrix},\\
\mathbf{B} &= \begin{bmatrix} \frac{D}{L_1} & 0 \\ \frac{D}{L_2} & \frac{Rr_{C2}}{L_2(R+r_{C2})} \\ 0 & 0 \\ 0 & -\frac{R}{C_2(R+r_{C2})} \end{bmatrix},\\
\mathbf{C} &= \begin{bmatrix} 0 & \frac{Rr_{C2}}{(R+r_{C2})} & 0 & \frac{R}{(R+r_{C2})} \end{bmatrix},\\
\mathbf{E} &= \begin{bmatrix} 0 & -\frac{Rr_{C2}}{(R+r_{C2})} \end{bmatrix},\\
\mathbf{A_1} &= \begin{bmatrix} -\frac{r_{L1}+D(r_p+r_{in})+(1-D)(r_N+r_{C1})}{L_1} \\ -\frac{D(r_p+r_{in})+(1-D)r_N}{L_2} \\ \frac{1-D}{C_1} \\ 0 \end{bmatrix},\\
\mathbf{A_2} &= \begin{bmatrix} -\frac{D(r_p+r_{in})+(1-D)r_N}{L_1} \\ \frac{(Dr_p+Dr_{in}+Dr_{C1}+r_{L2}+r_N-Dr_N)(R+r_{C2})+Rr_{C2}}{-L_2(R+r_{C2})} \\ -\frac{D}{C_1} \\ \frac{R}{C_2(R+r_{C2})} \end{bmatrix},\\
\mathbf{A_3} &= \begin{bmatrix} -\frac{1-D}{L_1} & 0 \\ \frac{D}{L_2} & -\frac{R}{L_2(R+r_{C2})} \\ 0 & 0 \\ 0 & -\frac{1}{C_2(R+r_{C2})} \end{bmatrix}.
\end{aligned} \tag{5}
$$

where r_p, r_n represent the ON resistance of the pMOS and nMOS transistors, respectively.

C. STEADY STATE EQUATIONS

For a steady state average, the derivative is zero. Therefore:

$$
\begin{aligned}
0 &= \mathbf{AX} + \mathbf{BU}\\
\mathbf{X} &= -\mathbf{A^{-1}BU}
\end{aligned} \tag{6}
$$

Substituting equation 2 in equation 6 yields to:

$$
V_o = V_{in}\left(\frac{D}{1-D}\right) \times \left(\frac{1}{q}\right)
$$

where:

$$
q = 1 + \frac{r_{L2}}{R} + \frac{r_{C1}+r_N}{R}\left(\frac{D}{1-D}\right) + \frac{r_{in}+r_P+Dr_{L1}}{DR}\left(\frac{D}{1-D}\right)^2
$$

D. LINEAR SMALL-SIGNAL STATE-SPACE EQUATIONS

The small signal model is obtained by substituting equation 2 in equation 3, and neglecting the double disturbance term. Which yields to:

$$
\begin{aligned}
\frac{d\tilde{x}}{dt} &= \mathbf{A}\tilde{\mathbf{x}} + \mathbf{B}\tilde{\mathbf{u}} + \tilde{d}\mathbf{B_d}\\
\tilde{y}(t) &= \mathbf{C}\tilde{\mathbf{x}} + \mathbf{E}\tilde{\mathbf{u}}
\end{aligned} \tag{7}
$$

where$\mathbf{B_d} = (\mathbf{A_1} - \mathbf{A_2})\,\mathbf{X} + (\mathbf{B_1} - \mathbf{B_2})\,\mathbf{U}$ By applying Laplace transform on equation 7, three transfer functions can be obtained:

$$
\begin{aligned}
v_{ov} &= \frac{\tilde{v}_o(s)}{\tilde{v}_{in}(s)} = \mathbf{CI_AB_S} + E_S\\
v_{oi} &= \frac{\tilde{v}_o(s)}{\tilde{i}_Z(s)} = \mathbf{CI_AB_Z} + E_Z\\
v_{od} &= \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \mathbf{CI_AB_d}
\end{aligned} \tag{8}
$$

where $\mathbf{B} = [\mathbf{B_S}\ \mathbf{B_Z}]$ and $\mathbf{E} = [\mathbf{E_S}\ \mathbf{E_Z}]$ and $\mathbf{I_A} = (s\mathbf{I} - \mathbf{A})^{-1}$

Analyzing the transfer function is difficult since the equations are too complicated

$$
\frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{(a_1 + b_1 s)\left(c_1 + d_1 s + e_1 s^2\right)}{K_1\left(f_1 + g_1 s + h_1 s^2 + i_1 s^3 + j_1 s^4\right)} \tag{9}
$$

where:

$$
\begin{aligned}
a_1 &= Rv_{in}\\
b_1 &= Rv_{in}C_2r_{C2}\\
c_1 &= R + r_{L2} + r_n + Dr_{C1} - 2Dr_{L2} + Dr_{in} - Dr_n + Dr_p\\
&\quad + D^2R - D^2r_{C1} + D^2r_{L1} + D^2r_{L2} - 2DR\\
d_1 &= C_1Rr_{C1} - D^2L_1 + C_1Rr_{L1} + C_1r_{C1}r_{L2} + C_1r_{L1}r_{L2}\\
&\quad + C_1r_{C1}r_n + C_1r_{L1}r_n + C_1D^2Rr_{C1} + C_1D^2r_{C1}r_{L2}\\
&\quad - C_1D^2r_{C1}r_{in} + C_1D^2r_{C1}r_n - C_1D^2r_{C1}r_p - 2C_1DRr_{C1}\\
&\quad - C_1DRr_{L1} - 2C_1Dr_{C1}r_{L2} - C_1Dr_{L1}r_{L2} - 2C_1Dr_{C1}r_n\\
e_1 &= C_1L_1(R + r_{L2} + r_n - Dr_{L2} - DR)\\
f_1 &= R + r_{L2} + r_n + Dr_{C1} - 2Dr_{L2} + Dr_{in} - Dr_n\\
&\quad + Dr_p + D^2R - D^2r_{C1} + D^2r_{L1} + D^2r_{L2} - 2DR\\
g_1 &= L_2 + D^2L_1 + D^2L_2 - 2DL_2 - C_1D^2r_{C1}^2\\
&\quad + C_1Rr_{C1} + C_2Rr_{C2} + C_1Rr_n + C_2Rr_n + C_1r_{C1}r_{L2}\\
&\quad + C_2r_{C2}r_{L2} + C_1r_{L1}r_{L2} + C_1r_{C1}r_n + C_1r_{L1}r_n
\end{aligned}
$$

$$
\begin{aligned}
&+ C_1 r_{L2} r_n + C_1 D r_{C1}^2 - C_2 D^2 R r_{C1} + C_2 D^2 R r_{C2} \\
&+ C_2 D^2 R r_{L2} - C_2 D^2 r_{C1} r_{C2} + C_2 D^2 r_{C2} r_{L1} + C_2 D^2 r_{C2} r_{L2} \\
&+ C_2 D R r_{C1} - 2 C_2 D R r_{C2} - 2 C_2 D R r_{L2} + C_1 D R r_{in} \\
&+ C_2 D R r_{in} + C_1 D R r_p + C_2 D R r_p + C_2 D r_{C1} r_{C2} \\
&+ C_1 D r_{C1} r_{L1} - C_1 D r_{C1} r_{L2} + C_1 D r_{C1} r_{in} \\
&+ C_2 D r_{C2} r_{in} - C_1 D r_{C1} r_n - C_2 D r_{C2} r_n \\
&+ C_1 D r_{C1} r_p + C_1 D r_{L1} r_{in} + C_1 D r_{L2} r_{in} - C_1 D r_{L1} r_n \\
&- C_1 D r_{L2} r_n + C_1 D r_{L1} r_p + C_2 R r_{L2} - C_2 D R r_n \\
&+ C_1 D r_{L2} r_p + C_2 D r_{C2} r_p - 2 C_2 D r_{C2} r_{L2} \\
&+ C_2 r_{C2} r_n - C_1 D R r_n + C_1 R r_{L1} + C_2 D^2 R r_{L1} - C_1 D R r_{C1}
\end{aligned}
$$

$$
\begin{aligned}
h_1 = {} & C_1 C_2 D R r_{L2} r_{in} + C_1 L_2 r_{C1} + C_2 L_2 r_{C2} + C_1 L_1 r_{L2} \\
&+ C_1 L_2 r_{L1} + C_1 L_1 r_n + C_1 L_2 r_n + C_2 D^2 L_1 r_{C2} \\
&+ C_2 D^2 L_2 r_{C2} - 2 C_2 D L_2 R - C_1 D L_2 r_{C1} - 2 C_2 D L_2 r_{C2} \\
&+ C_1 D L_1 r_{in} + C_1 D L_2 r_{in} - C_1 D L_1 r_n + C_1 D L_1 r_p \\
&+ C_1 D L_2 r_p + C_2 D^2 L_1 R + C_2 D^2 L_2 R + C_1 C_2 R r_{C1} r_{C2} \\
&+ C_1 C_2 R r_{C2} r_{L1} + C_1 C_2 R r_{L1} r_{L2} + C_1 C_2 R r_{C1} r_n \\
&+ C_1 C_2 R r_{C2} r_n + C_1 C_2 R r_{L2} r_n + C_1 C_2 r_{C1} r_{C2} r_{L2} \\
&+ C_1 C_2 r_{C2} r_{L1} r_{L2} + C_1 L_1 R + C_1 C_2 r_{C2} r_{L1} r_n \\
&+ C_1 C_2 r_{C2} r_{L2} r_n + C_1 C_2 D R r_{C1}^2 + C_1 C_2 D r - C_1 C_2 D^2 R r_{C1}^2 \\
&- C_1 C_2 D^2 r_{C1}^2 r_{C2} - C_1 C_2 D R r_{C1} r_{C2} - C_1 C_2 D R r_{C1} r_{L2} \\
&+ C_1 C_2 D R r_{C1} r_{in} + C_1 C_2 D R r_{C2} r_{in} - C_1 C_2 D R r_{C2} r_n \\
&+ C_1 C_2 D R r_{C1} r_p + C_1 C_2 D R r_{C2} r_p - C_1 C_2 D R r_{L1} r_n \\
&- C_1 C_2 D R r_{L2} r_n + C_1 C_2 D R r_{L1} r_p + C_1 C_2 D R r_{L2} r_p \\
&- C_1 C_2 D r_{C1} r_{C2} r_{L2} + C_1 C_2 D r_{C1} r_{C2} r_{in} - C_1 C_2 D r_{C1} r_{C2} r_n \\
&+ C_1 C_2 D r_{C2} r_{L2} r_{in} - C_1 C_2 D r_{C2} r_{L1} r_n - C_1 C_2 D r_{C2} r_{L2} r_n \\
&+ C_1 D L_1 r_{C1} - C_1 D L_2 r_n + C_1 C_2 R r_{C1} r_{L2} + C_1 C_2 R r_{L1} r_n \\
&+ C_1 C_2 D r_{C1} r_{C2} r_{L1} + C_1 C_2 D r_{C2} r_{L2} r_p + C_1 C_2 D r_{C2} r_{L1} r_{in} \\
&+ C_1 C_2 D r_{C2} r_{L1} r_p + C_1 C_2 D r_{C1} r_{C2} r_p + C_1 C_2 r_{C1} r_{C2} r_n \\
&+ C_2 L_2 R + C_1 C_2 D R r_{C1} r_{L1} - C_1 C_2 D R r_{C1} r_n \\
&+ C_1 C_2 D R r_{L1} r_{in}
\end{aligned}
$$

$$
\begin{aligned}
i_1 = {} & C_1 L_1 L_2 + C_1 C_2 L_1 R r_{C2} + C_1 C_2 L_2 R r_{C1} + C_1 C_2 L_1 R r_{L2} \\
&+ C_1 C_2 L_2 R r_{L1} + C_1 C_2 L_1 R r_n + C_1 C_2 L_2 R r_n \\
&+ C_1 C_2 L_2 r_{C1} r_{C2} + C_1 C_2 L_1 r_{C2} r_{L2} + C_1 C_2 L_2 r_{C2} r_{L1} \\
&+ C_1 C_2 L_1 r_{C2} r_n + C_1 C_2 L_2 r_{C2} r_n + C_1 C_2 D L_1 r_{C1} r_{C2} \\
&- C_1 C_2 D L_2 r_{C1} r_{C2} + C_1 C_2 D L_1 r_{C2} r_{in} + C_1 C_2 D L_2 r_{C2} r_{in} \\
&- C_1 C_2 D L_1 r_{C2} r_n - C_1 C_2 D L_2 r_{C2} r_n + C_1 C_2 D L_1 r_{C2} r_p \\
&+ C_1 C_2 D L_2 r_{C2} r_p + C_1 C_2 D L_1 R r_{C1} - C_1 C_2 D L_2 R r_{C1} \\
&+ C_1 C_2 D L_2 R r_{in} - C_1 C_2 D L_1 R r_n - C_1 C_2 D L_2 R r_n \\
&+ C_1 C_2 D L_1 R r_p + C_1 C_2 D L_1 R r_{in} + C_1 C_2 D L_2 R r_p
\end{aligned}
$$

$$
j_1 = C_1 C_2 L_1 L_2 (R + r_{C2})
$$

$$
\begin{aligned}
k_1 = {} & R + r_{L2} + r_n + D r_{C1} - 2 D r_{L2} + D r_{in} \\
&- D r_n + D r_p + D^2 R - D^2 r_{C1} + D^2 r_{L1} + D^2 r_{L2} - 2 D R
\end{aligned}
$$

The derivation presented here offers a more comprehensive transfer function for the Zeta converter, which builds upon the initial model described in reference paper [33]. This updated version explicitly accounts for the impact of the ON resistance of power transistors r_{ds}, as well as the series inductor resistances r_{L1} and r_{L2} – parameters that are frequently overlooked in simplified models.

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