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Compensation of Timing-Skew Mismatches in Time-Interleaved ADCs

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Département de génie électrique

Thèse présentée en vue de l'obtention du diplôme de *Philosophiæ Doctor*

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Compensation of Timing-Skew Mismatches in Time-Interleaved ADCs

présentée par **Hamidreza MAFI**

en vue de l'obtention du diplôme de *Philosophiæ Doctor*

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DEDICATION

In the memory of my father and my sister,

To my mother and my brother

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RÉSUMÉ

L'épine dorsale des systèmes de communication filaires et optiques actuels et émergents repose essentiellement sur des convertisseurs analogique-numérique (CAN) avec des taux d'échantillonnage ultra-élevés dépassant 20 Géch/s. L'utilisation des CAN permet le traitement des signaux et des données dans le domaine numérique via des approches de traitement du signal numérique (TSN). Le principal avantage des méthodes TSN est leur robustesse aux variations des procédés de fabrication, de la tension d'alimentation et de la température (PVT). Sachant que certaines composantes de la dissipation de puissance des CAN augmentent linéairement avec la fréquence d'échantillonnage, et au-delà, quand on s'approche des limites de vitesse de la technologie, certaines architectures induisent une consommation qui croît encore plus vite, voire exponentiellement avec la vitesse, un entrelacement temporel peut répondre aux besoins de débits plus élevés tout en maintenant la consommation d'énergie dans la zone de progression linéaire. Les CAN entrelacés dans le temps (CAN-ET) se composent d'un ensemble de sous-CAN nominalement identiques (SCAN) fonctionnant simultanément en parallèle. Les CAN-ET utilisent également un modèle de synchronisation spécial pour que les SCAN échantillonnent séquentiellement et de manière répétée le signal d'entrée. Les CAN-ET sont connus pour être vulnérables aux disparités entre leurs SCAN.

Les imperfections rencontrées parmi les SCAN, y compris les disparités de *décalage*, *gain* et *biais temporels*, dégradent la résolution effective souhaitée. Cela nécessite l'utilisation de méthodes d'étalonnage pour récupérer la résolution effective cible. Les procédés d'étalonnage de décalage temporel nécessitent généralement des moyens d'estimation et de compensation des disparités de décalage temporel pour récupérer la résolution effective cible. Les approches à signaux mixtes et entièrement numériques sont les deux principales classes d'étalonnage des décalages temporels. L'approche entièrement numérique apparaît comme un choix judicieux pour les cibles de haute définition. D'un autre côté, les techniques à signaux mixtes constituent la meilleure option pour les applications à haut débit.

Cette thèse propose des méthodes entièrement numériques et à signaux mixtes pour compenser le décalage temporel dans les CAN-ET afin de surmonter les limites actuelles des techniques existantes. Premièrement, cette thèse propose un concept de décalage temporel pour désensibiliser le mécanisme d'estimation du biais temporel à l'autocorrélation du signal d'entrée. La méthode proposée fonctionne sans avoir besoin de SCAN supplémentaires et sans aucune manipulation de la conception du CAN-ET. Le rapport signal sur bruit et sur distorsion (SNDR) d'un CAN-ET 10 bits dans un test spécifique a été amélioré de 37,44 dB

à plus de 56,64 dB lorsque le décalage temporel présente un écart type de 10% de l'intervalle d'échantillonnage du CAN-ET.

Ensuite, les approches de séparation de sources, ainsi que la transformée de Hilbert, sont adaptées pour reconnaître et supprimer l'erreur générée par le biais de synchronisation. La séparation des sources désensibilise la méthode proposée à la variation de fréquence du signal d'entrée et évite l'introduction de tout retard grâce à l'utilisation de deux filtres à réponse impulsionnelle finie (FIR). Avec cette technique, le SNDR est amélioré de 23.06 dB à plus de 66.82 dB dans un exemple de TI-ADC 12-bits lorsque l'écart type des disparités de décalage de synchronisation est de 10% de l'intervalle d'échantillonnage du CAN-ET. ne limite pas le nombre de SCAN.

La séparation des sources est également développée par une approche de décomposition polyphasée, associée à un mécanisme de modulation, pour soulager son exigence de vitesse. Ensuite, les filtres FIR adaptatifs sont utilisés pour supprimer les erreurs résultant de la discordance de synchronisation dans la sortie numérique du CAN-ET. Les approches proposées basées sur la séparation des sources fonctionnent sans nécessiter de SCAN supplémentaire et sans aucune manipulation de la structure du CAN-ET. Avec cette technique, le SNDR passe de 24.29 dB à plus de 60.14 dB dans un CAN-ET 12 bits lorsque l'écart type du décalage temporel est de 10% de la période d'échantillonnage du CAN-ET.

De plus, l'approche proposée utilise une matrice de modulation pour détecter les erreurs. De plus, le mécanisme proposé est réalisé par les approches de décomposition polyphasée pour soulager l'exigence de vitesse de la technique proposée. Cette méthode effectue sa tâche de compensation sans avoir besoin de SCAN(s) supplémentaire(s) et sans aucune manipulation de la conception du CAN-ET. Cette technique améliore le SNDR de 22.97 dB à 68.6 dB dans un CAN-ET 12 bits lorsque l'écart type du décalage temporel est réglé à 10% de la période d'échantillonnage du CAN-ET.

Enfin, le suréchantillonnage et la mise en forme du bruit des mécanismes sont utilisés pour atténuer les effets des erreurs résultant de l'élargissement du pas minimum des lignes à retard variables (VDL) tout en évitant d'utiliser des méthodes de routage d'horloge complexes. La méthode proposée entraîne le bruit de conversion induit par les erreurs de temps d'échantillonnage (introduites en augmentant les pas de retard) en dehors des fréquences de fonctionnement. Cette technique est plus adaptée aux CAN à entrelacement temporel exploitant la mise en forme du bruit, car ils sont déjà limités en bande passante. De plus, cela ne limite pas le nombre de SCAN. Des simulations comportementales vérifient la méthode proposée avec MATLAB/Simulink. La moyenne de la plage dynamique sans parasites (SFDR) est respectivement améliorée de 11.64 dB et 17.72 dB pour les zones basse fréquence

et haute fréquence.

Il est à noter que les techniques proposées, dans cette thèse, sont validées par diverses simulations utilisant MATLAB/Simulink et Xilinx Vivado Design Suite. Les méthodes proposées sont également implémentées sur un réseau de portes programmables par l'utilisateur (FPGA) pour évaluer l'efficacité des méthodes proposé pour différentes largeurs de mots. Nous avons validé la possibilité de synthétiser le modèle Simulink à virgule fixe, Ceci a permis d'évaluer le coût matériel pour différentes largeurs de mots.

ABSTRACT

The backbone of current and emerging wire-line and optical communication systems critically relies on analog-to-digital converters (ADCs) with ultra-high sampling rates exceeding 20 GS/s. Utilizing ADCs enables the processing of signals and data in the digital domain via digital signal processing (DSP) approaches. The main advantage of DSP schemes is their robustness to process, voltage, and temperature (PVT) variations. Since the power dissipation of ADCs linearly increases with the sampling rate up to a point and exponentially grows beyond that, time-interleaving is introduced to address the need for higher rates while keeping the power consumption in the linear zone. Time-interleaved ADCs (TI-ADCs) are nominally identical sub-ADCs (SADCs) simultaneously operating in parallel. TI-ADCs also use a special clocking pattern for SADCs to sequentially and repeatedly sample the input signal. TI-ADCs are known to be vulnerable to mismatches among their SADCs.

Imperfections among the SADCs, including of *offset*-, *gain*-, and *timing skew* mismatches, degrade the desired effective resolution. This necessitates the use of calibration methods to obtain the desired effective resolution. Timing skew calibration methods generally need means for estimating and compensating the timing skew mismatch to retrieve the target effective resolution. Mixed-signal and fully digital approaches are the two main timing skew mismatch calibration classes. The fully digital approach appears to be a sensible choice for high-resolution targets. On the other hand, mixed-signal techniques are the best option for high-speed applications.

This dissertation contributes to both fully digital and mixed-signal methods to compensate for the timing skew mismatch in TI-ADCs and overcome the limitations of current comparative techniques. First, this dissertation proposes the concept of time shift to desensitize the timing-skew estimation mechanism to the input signal's autocorrelation. The proposed method operates without additional SADC(s) or the TI-ADC's design manipulation. The signal-to-noise-and-distortion ratio (SNDR) of a 10-bit TI-ADC in a specific benchmark was improved from 37.44 dB to more than 56.64 dB when the timing-skew has a standard deviation of 10% of the TI-ADC's sampling interval.

Then, the source separation approaches and the Hilbert transform are adapted to recognize and remove the error raised from the timing skew, as a main contribution. The source separation approach desensitizes the proposed method to the frequency variation of the input signal and avoids introducing any delay by using two finite impulse response (FIR) filters. With this technique, the SNDR is enhanced from 23.06 dB to more than 66.82 dB in an

example 12-bit TI-ADC when the standard deviation of timing skew mismatches is 10% of the TI-ADC's sampling interval.

This dissertation then proposes a source separation scheme by adapting a polyphase decomposition approach and a modulation mechanism as a main contribution to relieve its speed requirement. The adaptive FIR filters remove errors arising from the timing-skew mismatch in the TI-ADC's digital output. The proposed source separation-based approaches operate without the need for any additional SADC(s) and without any manipulation of the TI-ADC's structure. With this technique, the SNDR enhances from 24.29 dB to more than 60.14 dB in a 12-bit TI-ADC when the standard deviation of timing-skew is 10% of the TI-ADC's sampling period.

In addition, this dissertation contributes to fully digital approach by utilizing adaptive filters and a modulation matrix. The polyphase decomposition also realizes the proposed mechanism approaches to relieve the speed requirement of the proposed technique. This method performs its compensation task without needing additional SADC(s) and manipulating the TI-ADC's design. This technique enhances the SNDR from 22.97 dB to 68.6 dB in a 12-bit TI-ADC when the standard deviation of timing-skew is set to 10% of the sampling period of the TI-ADC.

Finally, this dissertation uses oversampling and noise-shaping mechanisms, as a main contribution, to mitigate the effects of the errors resulting from enlarging the minimum step size of variable delay lines (VDLs) while avoiding utilizing complex clock routing methods. The proposed method drives the error (introduced by increasing the delay steps) outside the operating frequencies. This technique is more suitable for noise-shaping time-interleaved ADCs since they are already band-limited. Also, it does not restrict the number of SADCs. Behavioral simulations verify the proposed method with MATLAB/Simulink. The mean of the spurious-free dynamic range (SFDR) is respectively enhanced by 11.64 dB and 17.72 dB for the low-frequency and high-frequency zones.

Notably, the proposed techniques in this dissertation are validated by various simulations using MATLAB/Simulink and Xilinx Vivado Design Suite. The proposed methods are also implemented on field-programmable gate arrays (FPGAs) to evaluate their effectiveness for various word widths, validate the ability to synthesize the fixed-point Simulink model, and evaluate the hardware cost for various word widths.

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LIST OF SYMBOLS AND ABBREVIATIONS

ADC	Analog to Digital Converter
TI-ADC	Time-Interleaved ADC
SADC	Sub-ADC
IC	Integrated Circuit
PVT	Process Voltage Temperature
DSP	Digital Signal Processing
VDL	Variable Delay Line
CMOS	Complimentary-Metal-Oxide-Semiconductor
SNR	Signal-to-Noise Ratio
SNDR	Signal-to-Noise and Distortion Ratio
SFDR	Spurious Free Dynamic Range
ENOB	Effective Number of Bits
SAR	Successive Approximation Register
n	Discrete-Time Index Associate with TI-ADC
m	Discrete-Time Index Associate with SADCs
PN	Pseudo-Random Number
M	Number of SADCs
F_s	Overall Sampling Rate of TI-ADC
T_s	Sampling Time of TI-ADC
τ	Timing Skew
RC	Resistor–Capacitor
LMS	Least Mean Squares
μ	Loop Gain Factor
v	Correction Vector in Time Domain
V	Correction Vector in Frequency Domain
LUT	Lookup Table
FIR	Finite Impulse Response
AFIR	Adaptive Finite Impulse Response
LPF	Low Pass Filter
HPF	High Pass Filter
MA	Moving Average
HDL	Hardware Description Language
FPGA	Field Programmable Gate Arrays

ASIC	Application-Specific Integrated Circuit
$c(\cdot)$	Auto-Correlation Operator/Cross-Correlation Operator
NS	Noise Shaping
OSR	Over-Sampling Ratio

CHAPTER 1 INTRODUCTION

1.1 Motivation

Current and emerging data centers and long-haul telecommunication systems critically depend on high-speed optical links. Information transmitted as modulation to high-speed carriers over these optical links is recovered using medium-resolution, around 10 bits, analog-to-digital converters (ADCs). These ADCs typically operate at ultra-high sampling rates exceeding 20 GS/s [10–15].

Utilizing ADCs enables the processing of signals and data in the digital domain via digital signal processing (DSP) methods. The main advantage of DSP mechanisms is their robustness to process, voltage, and temperature (PVT) variations [7, 15]. Since the power dissipation of ADCs linearly increases with the sampling rate up to a point, and beyond that, it exponentially grows [2, 16], time-interleaving was introduced to address the need for higher sampling rates while keeping the power consumption in the linear zone [16, 17]. Figure 1.1 shows the typical structure of time-interleaved ADCs (TI-ADCs) consisting of a set of nominally identical sub-ADCs (SADCs) simultaneously operating in parallel [8, 15, 17–19].

TI-ADCs also use a particular clocking pattern for SADCs to sequentially and repeatedly sample the input signal. This parallel sampling approach proportionally increases the equivalent sampling rate of TI-ADCs to the number of SADCs, M [4, 7, 18, 20]. Nonetheless, TI-ADCs' performances suffer from mismatches among their embedded SADCs. Known types of SADC imperfections causing mismatches include DC offset o_k , gain g_k , and timing skew τ_k , where $k = 0, \dots, M - 1$. These mismatches are notably due to process voltage and temperature (PVT) variations [4, 7, 18, 21–23]. Mismatches among the SADCs lead to the degradation in the desired effective resolution of TI-ADCs. Mitigating these mismatches necessitates calibration or compensation methods to retrieve the effective target resolution. It is worth mentioning that the frequency dependency of the error arising from the timing-skew mismatches further degrades the resolution of TI-ADCs. This makes measurement and cancellation of mismatches more challenging [8, 9, 24].

1.2 Problem Formulation and Research Question

Timing skew calibration methods generally need means for estimating and compensating the timing skew mismatch to retrieve the target effective resolution. Figure 1.2 depicts two main classes of calibration methods: (a) mixed-signal and (b) fully digital. The calibra-

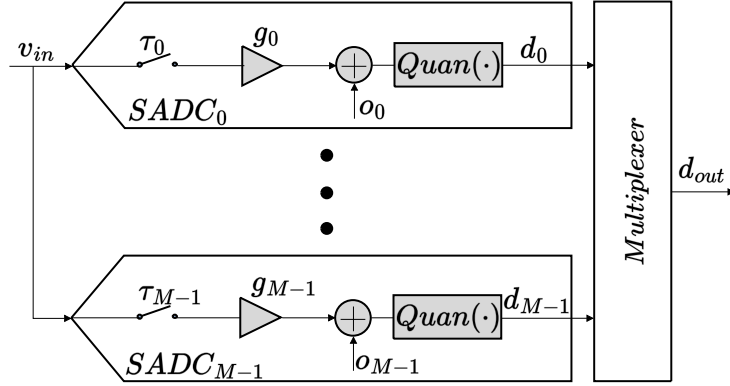


Figure 1.1 Architecture of a typical time-interleaved ADC (TI-ADC).

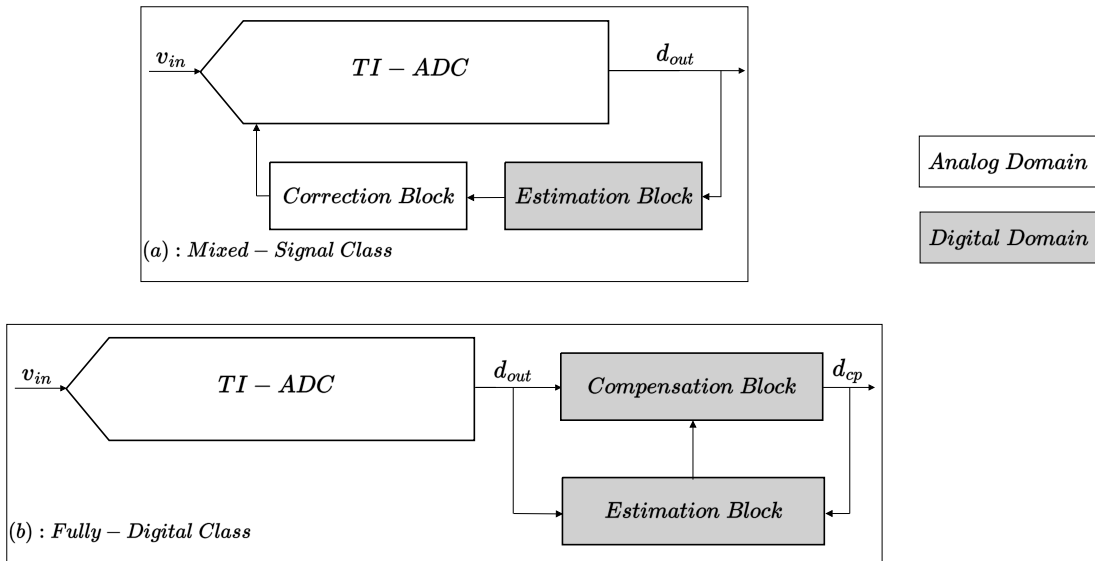


Figure 1.2 Calibration classes. (a): Mixed-signal class. (b): Fully digital class.

tion techniques are often decomposed into 2 functionalities: 1—estimation and 2—correction (or compensation). Most estimation mechanisms are realized in the digital domain to benefit from its immunity to PVT variations [1, 2, 4, 5, 15–17, 21, 22, 25–28]. Nonetheless, the compensation part is realized in the digital or analog domains according to the specified requirements.

The fully digital approach benefits from the mass integration of advanced complementary-metal-oxide-semiconductor (CMOS) technologies and fast portability from one technology to the next more advanced one [7, 15]. Despite all the advantages of present mixed-signal and fully digital approaches, both have drawbacks. On the one hand, mixed-signal approaches require additional analog circuits such as variable delay lines (VDLs), modifying the TI-ADC,

and extra SADC(s). Also, sensitivity to PVT variations [7, 27] is an additional disadvantage of analog circuits. In turn, VDLs impose more limitations on the achievable target effective resolution. On the other hand, fully digital schemes can impose additional power dissipation, which can be unacceptable. Also, fully digital mechanisms restrict the usable input bandwidth or limit the number of SADC channels [3, 6]. In general, any development in the mixed-signal approach should thus consider

- Avoiding any extra SADC(s),
- Avoiding any manipulation of the TI-ADC's architecture.

Similarly, any development in the fully digital approach should consider

- Avoid imposing any limit on the useful input bandwidth,
- Avoid restricting the number of channels.

The mixed-signal estimation mechanism proposed in [1, 19] tries to maximize the auto-correlation function to remove the timing skew mismatch at the cost of extra SADC and manipulation of the clock pattern. The estimation mechanism in [17, 29] (and its variants [16, 30]) tries to eliminate the requirement for extra SADC(s) and manipulation of the TI-ADC by evaluating the two cross-correlations. However, this mechanism is sensitive to the cross-correlation distribution and values at $\pm 1/F_s$ where F_s denoted the TI-ADC's sampling rate. The technique reported in [10] tried to mitigate this sensitivity by introducing a time shift at the cost of an extra SADC. Therefore, any alternative improved mechanism in the mixed signal class must consider

- Avoiding extra SADC(s),
- Avoiding manipulations of the TI-ADC's architecture,
- Mitigating the sensitivity to the auto-correlation.

Traditionally, a first-order Taylor approximation of the error raised by timing-skew mismatches has been utilized to make the power/area consumption efficient [5, 7–9, 21]. Nonetheless, the finite impulse response (FIR) filter's response accuracy for realizing the derivative filter drops as the input frequency approaches the Nyquist frequency [26]. The methods reported in [5, 6] restrict the input signal due to the oversampling mechanism used. The techniques introduced in [4, 6, 25] limit the channel number to two and four. The method

reported in [7] restricts the number of channels to specific numbers (i.e., 2, 4, 8, ...) [9, 31]. The approaches in [27, 28] need extra SADC(s) for calibration. In addition, these fully digital methods introduce a delay in the compensated signal due to the use of FIR filter(s) in the feedforward path(s), which can be unacceptable in applications with feedback mechanisms. In summary, any enhanced fully digital mechanism must deal with the following considerations:

- Avoid imposing any limit on the useful input bandwidth,
- Avoiding introducing a delay in the compensated digital output,
- Avoid manipulating the architecture of TI-ADC,
- Avoid restricting the number of channels,

Any method that could relieve the current limits would be beneficial.

In practice, realizing the required minimum step size of the VDLs can be challenging in high-resolution and ultra-high-speeds. As mentioned above, randomization, oversampling, and noise shaping can be utilized [32–34] to mitigate the need for VDLs. Although this approach eliminates the need for VDLs, the effective resolution remains unchanged. Also, it needs complicated clock routing. Moreover, a calibration approach is still needed to enhance the signal-to-noise and distortion ratio (SNDR). In addition, the over-sampling and noise-shaping mechanisms are employed in the reported methods in [35, 36] to avoid using calibration. Nevertheless, a calibration scheme is essential if the number of channels exceeds the over-sampling ratio. Any developing approach must consider the following terms

- Avoid complicating the clocking routes,
- Avoid limiting the number of channels.

Any developed method that could minimize these limits could also be promising.

1.3 Research Objective

Following the disadvantages and drawbacks of the current calibration methods mentioned in Section 1.2, this dissertation proposes and validates mechanisms and approaches to overcome (and improve) the current unsolved issues. For this reason, the main objectives of this dissertation are as follows:

1. Propose and validate a desensitizing method to the autocorrelation of the input signal

The first research objective aims to propose and validate an approach to desensitizing the current correlation-based techniques to the input signal's auto-correlation function. The target technique should avoid utilizing any extra SADC(s), and it should prevent modifications to the analog circuit of the TI-ADC. Moreover, it should mitigate the sensitivity to the input signal's auto-correlation function. The proposed technique aims to make the estimation part suitable for high-speed applications. Finally, this method will be validated by evaluating its suitability for practical input signals and its robustness to various input frequencies.

2. Propose and validate fully digital timing-mismatch compensation techniques exploiting adaptive algorithms

This part aims to propose and validate fully digital methods to mitigate (or minimize) the sensitivity of the current fully digital techniques to high-frequency regions. It must also improve the quality of the compensation done with state-of-the-art techniques. The target techniques will avoid restricting the usable input bandwidth and introducing any delay in the compensated signal. The target methods will not require any extra SADC(s). The developed techniques will make the compensation methods suitable for high-speed applications. Finally, the proposed method will be validated by evaluating its suitability for practical input signals and its robustness to various input frequencies.

3. Propose and validate the use of a noise-shaping mechanism to relieve constraints associated with the implementation of variable delay lines

This last objective will attempt to use oversampling and noise-shaping mechanisms to mitigate the effects of the errors resulting from enlarging the minimum step size of VDLs. This approach will avoid complex clock routing methods. Since this method will be the first attempt to apply noise-shaping to reduce the impact of VDL quantization errors, behavioral simulations will first evaluate its capabilities and limitations. If simulations yield good results, we will attempt to obtain a theoretical explanation supported by analytic models.

Due to funding limitations of the project supporting this research, the TI-ADCs, and the proposed methods are developed, verified, and evaluated with realistic models in MATLAB/Simulink instead of being implemented and measured from fabricated custom chips. However, all digital parts of the developed methods will be programmed on FPGA from HDL codes derived from the Simulink models; these HDL models operate with fixed-point

precision to evaluate and verify them in a realistic environment with various word widths and to estimate their potential for high-speed operation and for meeting stringent power dissipation constraints.

1.4 Research Contributions

Based on the research objectives mentioned above, the following main contributions of this dissertation, along with their related articles, are presented as

1. Desensitizing the estimation methods to the autocorrelation of the input signal

Chapter 3 proposes the concept of time shift to desensitize the estimation mechanism to the autocorrelation of the input signal. One finite impulse response (FIR) filter generates the required time shifts, which the polyphase decomposition mechanism implements to relieve the proposed method's speed requirement. The proposed fully digital estimation method operates without additional SADC(s) and without manipulating the TI-ADC's architecture, making it suitable for fully digital calibration mechanisms. The following articles are related to the first contribution:

- Hamidreza Mafi, Mohammad Honarparvar, Mohamed Ali, Naim Ben-Hamida, and Yvon Savaria, “*Background Calibration of Time-Interleaved ADCs with Polyphase Filters*,” 2023 IEEE 21st Interregional NEWCAS Conference (NEWCAS), Edinburgh, United Kingdom, 2023, pp. 1-5.
- Hamidreza Mafi, Mohammad Honarparvar, Mohamed Ali, Naim Ben-Hamida, and Yvon Savaria, “*Digital Background Estimation of Timing-Skew Mismatches in Time-Interleaved ADCs*,” Submitted to IEEE Transactions on VLSI Systems, 2024.

2. Using source separation algorithm along with the Hilbert transform for fully digital compensation

The proposed method, in Chapter 4, benefits from the source separation algorithm, which mainly contributes to removing the errors arising from the timing-skew mismatch in the TI-ADC's digital output. This chapter proposes the Hilbert transform, together with down-sampling and up-sampling, to be used as the required second input. The proposed technique compensates without additional SADC(s) or manipulating the TI-ADC structure. It can also operate in almost all the Nyquist range. In addition, this

fully digital method avoids introducing any delay in the compensated signal by using filters in the feedback paths. The following article is related to this contribution:

- Hamidreza Mafi, Naim Ben-Hamida, Sadok Aouini, and Yvon Savaria, “*Digital Compensation of Timing Skew Mismatches in Time-Interleaved ADCs by Source Separation*,” IEEE Transactions on Instrumentation and Measurement, vol. 73, 2024.

3. Using polyphase source separation algorithm along with the modulation operation for fully digital compensation

Chapter 5 benefits from the polyphase realization of the source separation algorithm, which, as a main contribution, removes the errors arising from the timing-skew mismatch in the digital output of the TI-ADC. The polyphase decomposition realizes the source separation algorithm approaches to relieve the speed requirement of the proposed method. For this phase, the Hadamard transform is used as a modulation operation to generate the second set of inputs to the source separation algorithm. The proposed method can operate in almost all the Nyquist range. It also performs its compensation task without the need for additional SADC(s) and without manipulating the TI-ADC’s structure. In addition, this fully digital technique avoids introducing any delay in the compensated signal by using filters in the feedback paths. The following articles are related to the third contribution:

- Hamidreza Mafi, Naim Ben-Hamida, Sadok Aouini, and Yvon Savaria, “*Digital Compensation of Timing-Skew Mismatch in TI-ADCs by Polyphase Source Separation*,” Accepted in 2024 IEEE 22nd Interregional NEWCAS Conference (NEW-CAS), Sherbrooke, QC, Canada, 2024, pp. 1-5.
- Hamidreza Mafi, Naim Ben-Hamida, Sadok Aouini, and Yvon Savaria, “*Digital Compensation of Timing-Skew Mismatch in TI-ADCs by Polyphase Source Separation*,” IEEE Transactions on Circuits and Systems I: Regular Papers, 2024.

4. Using polyphase adaptive filters for fully digital compensation

In Chapter 6, this phase uses the adaptive FIR filters in feedback loops as a main contribution to remove the errors arising from the timing-skew mismatch in the digital output of the TI-ADC. Also, the proposed mechanism is realized by the polyphase decomposition approaches to relieve the speed requirement of the proposed technique. Moreover, the proposed approach uses a modulation operation to detect errors. The proposed method performs its compensation task without the need for any additional

SADC(s) and without manipulating the TI-ADC's structure. Moreover, it can operate in almost all the Nyquist range. Also, this fully digital technique prevents introducing any delay in the compensated signal by using filters in the feedback path. The following article is related to the fourth contribution:

- Hamidreza Mafi, Sadok Aouini, Naim Ben-Hamida, and Yvon Savaria, “*Digital Compensation of Timing-Skew Mismatches in TI-ADCs with Adaptive Polyphase Filters*,” Submitted to IEEE Transactions on Signal Processing, 2024.

5. Using a noise-shaping technique to relieve limitations of variable delay lines

As a main contribution, Chapter 7 attempts to use oversampling and noise-shaping mechanisms to mitigate the effects of the errors resulting from enlarging the minimum step size of VDLs, while avoiding utilizing complex clock routing methods. The proposed method drives the error (raised by increasing the delay steps) outside the operating frequencies. This technique is more effective for noise-shaping TI-ADCs since they are already band-limited. Furthermore, it does not restrict the number of SADCs. As a result of using this method, the spurious-free dynamic range (SFDR) is significantly enhanced. The following article is related to this objective:

- Hamidreza Mafi, Mohammad Honarparvar, Mohamed Ali, Naim Ben-Hamida, and Yvon Savaria, “*Background Calibration of Time-Interleaved ADCs with Polyphase Filters*,” Accepted in 2024 IEEE International Symposium on Circuits and Systems (ISCAS), 2024.

According to the objective of this research, the methods in Chapter 3-6 are evaluated and verified in a realistic environment with various word widths by being programmed on FPGA using HDL codes obtained from fixed-point precision Simulink models.

1.5 Structure of the Thesis

The remainder of this dissertation is structured as follows: Chapter 2 explains the structure of TI-ADC, reviews the advantages and drawbacks of the pioneer and state-of-the-art calibration methods, and formulates the drawbacks and disadvantages of the present calibration techniques. Chapter 3 presents the proposed mixed-signal method based on the time-shift concept.

Chapter 4 proposes the source-separation-based method for compensating for the error introduced by the timing-skew mismatch. Chapter 5 presents the polyphase extension of the

source-separation-based method to relieve the operation speed requirement of the proposed method in Chapter 4. Chapter 6 proposes using adaptive polyphase filters in the feedback loops to compensate for the error introduced by the timing-skew mismatch.

Chapter 7 proposes the noise-shaping approach to relieving the VDLs requirements. Chapter 8 provides the general discussion of this dissertation. Finally, Chapter 9 concludes this dissertation.

CHAPTER 2 FUNDAMENTALS AND RESEARCH CONTRIBUTION ON CALIBRATION OF MULTICHANNEL ADCS

This chapter briefly explains the TI-ADC's architecture, its impact on imperfection, and the classification of mismatch errors. Then, current significant timing skew mismatch calibration approaches in the analog and digital domains and mechanisms are reviewed.

2.1 Fundamentals of Multichannel ADCs

TI-ADCs were first proposed by Black and Hodges [15,37] as a means to increase the effective sample rate of ADCs [19]. In this architecture, a set of M nominally identical SADCs operate in parallel, as depicted in Figure 2.1. The SADCs can have the architecture of Flash [1] and SAR ADCs [11, 12] or noise-shaping delta-sigma modulators [35,36]. The resolution of the SADCs must be identical. In this case, TI-ADCs hold the resolution of the SADCs. The sampling time of SADCs is uniformly spaced by the sampling time, $T_s = 1/F_s$, where F_s is the equivalent sampling rate of TI-ADC [20,25]. The pattern of the delay in the k^{th} SADC is defined as kT_s for $k = 0, \dots, M - 1$. Accordingly, the input signal, v_{in} , is sampled every T_s seconds resulting in the overall sampling frequency of F_s in TI-ADC structure. However, the TI-ADC is sensitive to imperfections among its SADC channels that can severely degrade the target resolution in the TI-ADC.

As mentioned in Chapter 1, the SADCs manifest inherent *offset*, *gain*, and *sampling-time skew* mismatches due to random PVT variations in the SADCs [4,18,38]. Since these mismatches severely degrade the effective resolution of the TI-ADC, almost all TI-ADCs need to include means to restore the target resolution by estimating and compensating these mismatches [38]. In the following, the effect of mismatches is presented. As seen from Figure 2.1, the sampled input signal in the k^{th} SADC can be expressed as follows

$$v_{s,k}(m) = o_k + (1 + g_k)v_{in}([mM - k]T_s) + \tau_k, \quad k = 0, \dots, M - 1, \quad (2.1)$$

where m denotes the discrete-time index (associated with the sampling rate of SADCs), and also, o_k , g_k , and τ_k respectively stand for the offset, gain, and timing skew, in the k^{th} SADC. It is obvious from the first-order approximation of the Taylor series that [15,21,22], the sampled input signal in the k^{th} SADC can be roughly expressed as

$$v_{s,k}(m) \approx o_k + (1 + g_k)v_{in}([mM - k]T_s) + \tau_k \frac{dv_{in}([mM - k]T_s)}{dt}. \quad (2.2)$$

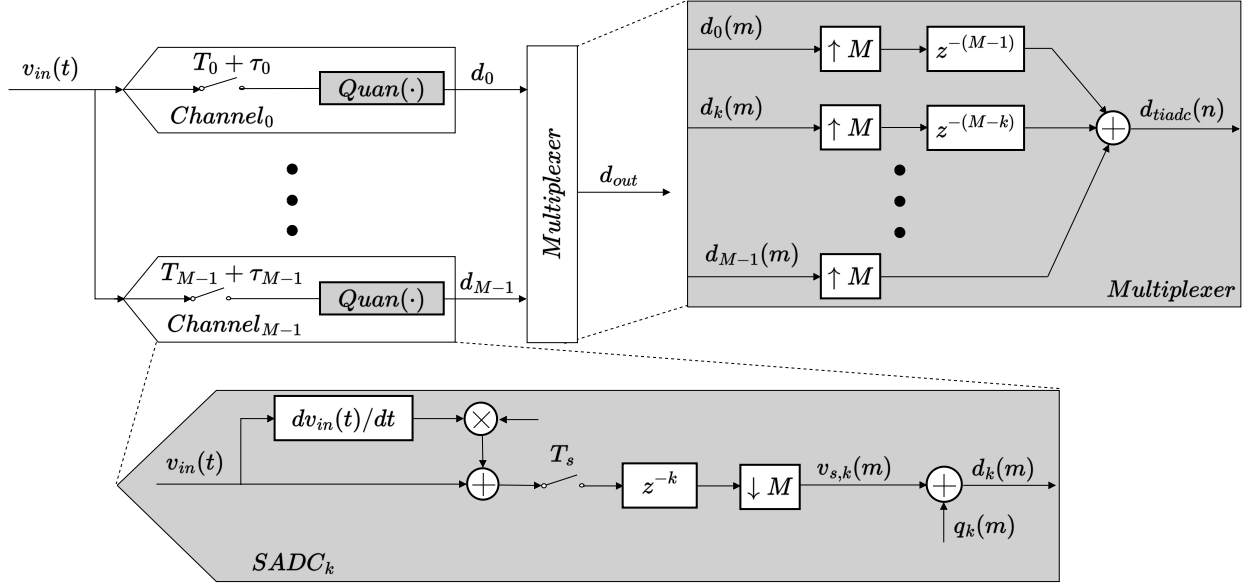


Figure 2.1 Architecture of a typical time-interleaved ADC (TI-ADC).

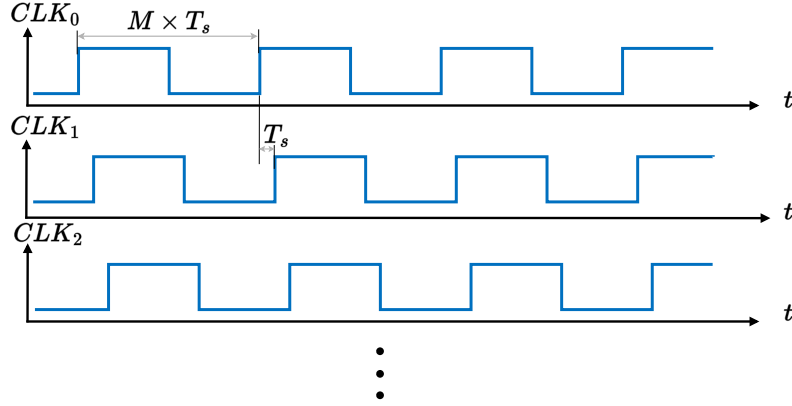


Figure 2.2 Typical clock pattern of TI-ADC with M SADCs.

This expression assumes that $\tau_k \ll T_s$ for $k = 0, \dots, M - 1$, which restricts the maximum timing skews. Ideally, the outputs of the SADCs, d_k , are the digital format of their inputs plus an injected error term as the result of the quantization process. In this dissertation, the quantization error is omitted to concentrate on the proposed methods for calibration (or compensation) of timing-skew mismatches [5, 23].

In this dissertation, the frequency representation of variables and signals is denoted with

capital letters. In the frequency domain, the digital output of the k^{th} SADC is expressed as

$$\begin{aligned}
D_k(e^{j\omega}) = & \frac{1}{M} \sum_{i=0}^{M-1} e^{-jk(\frac{\omega}{M} - \frac{2\pi i}{M})} V_{in}(e^{j(\frac{\omega}{M} - \frac{2\pi i}{M})}) \\
& + o_k \frac{1}{M} \sum_{i=0}^{M-1} e^{-jk(\frac{\omega}{M} - \frac{2\pi i}{M})} \\
& + g_k \left\{ \frac{1}{M} \sum_{i=0}^{M-1} e^{-jk(\frac{\omega}{M} - \frac{2\pi i}{M})} V_{in}(e^{j(\frac{\omega}{M} - \frac{2\pi i}{M})}) \right\} \\
& + \tau_k \left\{ \frac{1}{M} \sum_{i=0}^{M-1} e^{-jk(\frac{\omega}{M} - \frac{2\pi i}{M})} V_{in}(e^{j(\frac{\omega}{M} - \frac{2\pi i}{M})}) j \left(\frac{\omega}{M} - \frac{2\pi i}{M} \right) \right\}, \quad k = 0, \dots, M-1.
\end{aligned} \tag{2.3}$$

Afterward, the digital output of the TI-ADC is obtained by multiplexing the outputs of the SADCs [5, 23]. In the frequency domain, the multiplexing operation is represented by up-sampling the outputs of the SADCs by a factor M and then applying the effect of the $M-k$ time delays in the frequency domain (i.e., $= e^{-j(M-k)\omega}$). This can be expressed as

$$\begin{aligned}
D_{us,k}(e^{j\omega}) = & \frac{e^{-jM\omega}}{M} \left\{ \sum_{i=0}^{M-1} e^{-jk\frac{2\pi i}{M}} V_{in}(e^{j(\omega - \frac{2\pi i}{M})}) \right. \\
& + o_k \sum_{i=0}^{M-1} e^{-jk\frac{2\pi i}{M}} \\
& + g_k \sum_{i=0}^{M-1} e^{-jk\frac{2\pi i}{M}} V_{in}(e^{j(\omega - \frac{2\pi i}{M})}) \\
& \left. + \tau_k \sum_{i=0}^{M-1} e^{-jk\frac{2\pi i}{M}} V_{in}(e^{j(\omega - \frac{2\pi i}{M})}) j \left(\omega - \frac{2\pi i}{M} \right) \right\}, \quad k = 0, \dots, M-1.
\end{aligned} \tag{2.4}$$

The digital output of the TI-ADC is the sum of all the upsampled signals, $d_{us,k}$ for $k = 0, \dots, M-1$ [5, 23]. In the frequency domain, the digital output of TI-ADC is thus represented as

$$D_{out}(e^{j\omega}) = D_{id}(e^{j\omega}) + E_{off}(e^{j\omega}) + E_{gn}(e^{j\omega}) + E_{tm}(e^{j\omega}) \tag{2.5}$$

where $D_{id}(e^{j\omega})$, $E_{off}(e^{j\omega})$, $E_{gn}(e^{j\omega})$, and $E_{tm}(e^{j\omega})$ respectively denote the ideal part (i.e., the digital format of the input signal), *offset*, *gain*, and *timing skew* mismatch errors, expressed

as follows

$$\begin{aligned}
D_{id}(e^{j\omega}) &= \frac{e^{-jM\omega}}{M} \sum_{i=0}^{M-1} V_{in}(e^{j(\omega - \frac{2\pi i}{M})}) \sum_{k=0}^{M-1} e^{-jk\frac{2\pi i}{M}}, \\
E_{off}(e^{j\omega}) &= \frac{e^{-jM\omega}}{M} \sum_{i=0}^{M-1} OC_i, \\
E_{gn}(e^{j\omega}) &= \frac{e^{-jM\omega}}{M} \sum_{i=0}^{M-1} GC_i V_{in}(e^{j(\omega - \frac{2\pi i}{M})}), \\
E_{tm}(e^{j\omega}) &= \frac{e^{-jM\omega}}{M} \sum_{i=0}^{M-1} TC_i V_{in}(e^{j(\omega - \frac{2\pi i}{M})}) j(\omega - \frac{2\pi i}{M})
\end{aligned} \tag{2.6}$$

where the gain and timing skew mismatch complex coefficients, OC_i , GC_i , and TC_i are, respectively, expressed as

$$\begin{aligned}
OC_i &= \sum_{k=0}^{M-1} o_k e^{-jk\frac{2\pi i}{M}}, \\
GC_i &= \sum_{k=0}^{M-1} g_k e^{-jk\frac{2\pi i}{M}}, \\
TC_i &= \sum_{k=0}^{M-1} \tau_k e^{-jk\frac{2\pi i}{M}}.
\end{aligned} \tag{2.7}$$

It can also be shown [39] that

$$\sum_{k=0}^{M-1} e^{-jk\frac{2\pi i}{M}} = \frac{1 - e^{-jk2\pi i}}{1 - e^{-jk\frac{2\pi i}{M}}} = \begin{cases} M, & i = 0, \\ 0, & i \neq 0. \end{cases} \tag{2.8}$$

Accordingly, from (2.6) and (2.8), it is straightforward to show that the ideal part, $D_{id}(e^{j\omega})$, of the TI-ADC output is given by

$$D_{id}(e^{j\omega}) = e^{-jM\omega} V_{in}(e^{j\omega}). \tag{2.9}$$

In the above equation, all the images except for the input signal itself vanished in the ideal element, $D_{id}(e^{j\omega})$ [5, 23]. It must be noted that the term $e^{-jM\omega}$ in (2.9) translates to the delay of M . However, the same is not *valid for the error terms* for OC_i , GC_i , TC_i since the mismatches are randomly distributed, and they differ from each other. The error due to the offset mismatch, $E_{off}(e^{j\omega})$, is worth mentioning as it is independent of the input signal. Nevertheless, the gain and timing skew mismatch errors, $E_{gn}(e^{j\omega})$ and $E_{tm}(e^{j\omega})$ appear as the modulated input signal and the modulated derivative of the input signal, respectively [15, 18, 38]. Moreover, the timing skew mismatch error $E_{tm}(e^{j\omega})$ appears as a

frequency-dependent variable, unlike the gain mismatch error $E_{gn}(e^{j\omega})$ [5, 23].

To mitigate the error terms in (2.6), calibration means are required to estimate and correct (or compensate) these terms. Since the focus of this dissertation is eliminating the impact of timing skew mismatches, the remainder of this chapter reviews and compares the most significant and pioneering approaches for correcting timing skew mismatch errors.

2.2 State-Of-The-Art Contributions to the Calibration of Multichannel ADCs

As mentioned in Chapter 1, calibration techniques consist of two parts: 1- *estimation* and 2- *correction* (or *compensation*). Due to continuous operation speed enhancement and digital integration augmentation, the estimation is often carried out in the digital domain. However, the correction (or compensation) mechanism must be realized in either analog or digital domain according to the specific application [7, 15–17, 28, 31].

Calibration approaches of timing skew mismatch can also be divided into *mixed-signal* and *fully-digital* classes [7, 15, 31]. In the fully digital calibration approach, both the estimation and correction are performed in the digital domain. In contrast, the mixed-signal methods exploit variable delay lines (VDLs) to correct timing skew mismatch. In addition, the mixed signal approaches may need extra SADC(s) [1, 2, 16].

The mixed-signal approach is unavoidable for ultra-high-speed targets since the VDLs can operate without restricting the target operational rate of TI-ADCs. However, VDLs often limit the effective resolution of TI-ADC to less than 8 bits due to PVT variations and added jitter to the sampling clock paths. In contrast, high-resolution applications utilize DSP methods due to their insensitivity to PVT variations, but they do so at the expense of the restricted operational frequency. As a consequence, all-digital DSP-based approaches are suitable for high-resolution applications in cases where the operation rate of the implementation of the DSP algorithms does not appear to be a limiting factor to the overall sampling rate of TI-ADC.

2.2.1 Mixed-Signal Calibration Techniques

The calibration methods are categorized as mixed-signal in case the correction (and/or estimation) are fully (or partly) realized in the analog domain via additional analog circuits and/or extra SADC(s). This class of calibration methods is often suitable for applications with low-to-mid resolutions and ultra-high sampling rates. In the following, the most influential mixed-signal calibration approaches are reviewed.

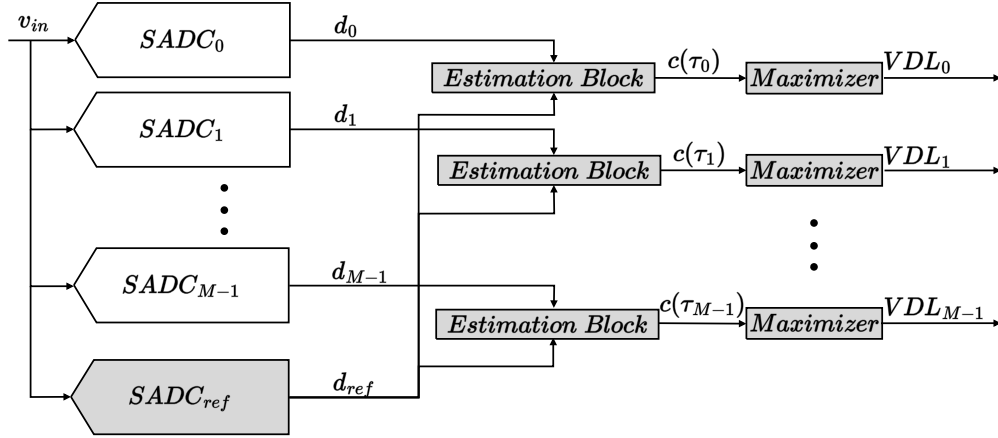


Figure 2.3 Architecture of the TI-ADC used in [1].

Correlation-Based Techniques

This approach exploits the cross-correlation mechanism for estimating timing-skew mismatches and corrects them by VDLs. This mixed-signal approach was first introduced in [18] and later developed in [17] and [10]. In the following, these methods are briefly reviewed.

The reported technique in [18] (and its variants, e.g., [19, 40]) evaluates and maximizes the cross-correlation function. This approach uses an extra SADC as the reference SADC, as shown in Figure 2.3. The SADCs and reference SADC sample the input signal at the frequencies of F_s/M and F_s/N , respectively, where F_s is the equivalent sampling rate of the TI-ADC, as mentioned earlier. The greatest common divisor of M and N is set to one [1, 15]. In that case, the sampling instance of the reference SADC periodically and sequentially coincides with the sampling edges of all the SADCs [15]. Figure 2.4 shows the case of the clocking pattern with $M = 3$ and $N = 4$. All the digital output of the SADCs and the reference SADC can be sequentially compared to perform the estimation.

For calibration of the k^{th} SADC, $k = 0, \dots, M - 1$, the cross-correlation between the input signal's samples acquired by the reference SADC and the k^{th} SADC, $c(\tau_k)$, is evaluated for the estimation process of the timing-skew, τ_k . From basics of probability and random processes, it is straightforward to show that the cross-correlation function $c(\tau_k)$ manifests its peak at the origin (i.e., $\tau_k = 0$) [18, 41]; in other words, the peak of the k^{th} cross-correlation function, $c(\tau_k)$, denotes the perfect coincidence in the sampling edge of the reference SADC and the k^{th} SADC. This estimation method uses cross-multiplications as the instant noisy estimate of the cross-correlation function $c(\tau_k)$, $k = 0, \dots, M - 1$, and moving-average (MA) filters to

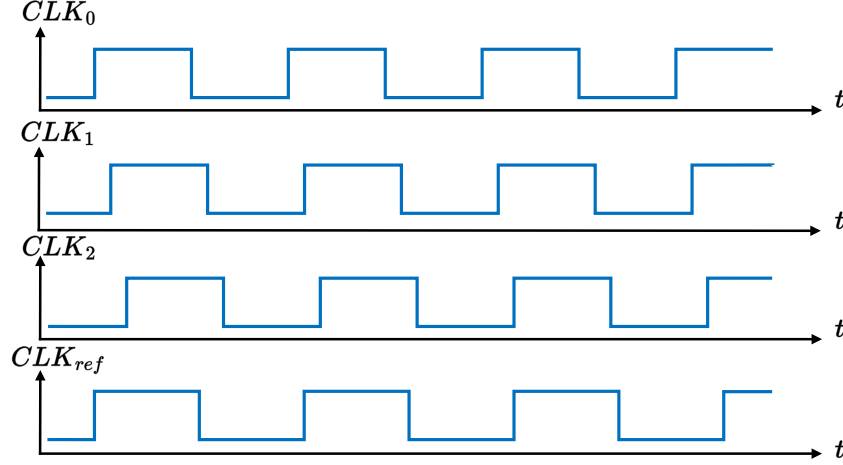


Figure 2.4 Clocking pattern used in [1].

reduce the noise and to estimate the functions $c(\tau_k)$, for $k = 0, \dots, M - 1$, as

$$c(\tau_k) \approx \frac{1}{L} \sum_{m=(r-1)L}^{rL-1} d_{ref}(m) \times d_k(m) \quad (2.10)$$

where L denotes the number of samples being averaged, while r and m respectively represent the update index of the MA filter and the discrete-time index of the SADCs corresponding to the sampling rate of F_s/M . It is shown in [15, 18] that the signal-to-noise (SNR) is related to the cross-correlations as

$$SNR = \frac{M^2 P^2}{M^2 P^2 - \sum_{k=0}^{M-1} c(\tau_k)}. \quad (2.11)$$

This equation indicates that maximizing the cross-correlation function denotes maximization of the SNR. This method uses a simple all-digital approach to gradually find the peak of the cross-correlation function by tuning the correction variables in the analog domain by VDLs. The main drawback of this method is the need for a reference SADC (in addition to utilizing VDLs).

The technique reported in [17] (and its variants [16, 30, 42]) is built upon the technique reported in [1]. This method uses the cross-correlation between the outputs of the SADCs instead of additional reference SADC. It thus operates without additional circuits in the analog domain. This method estimates the timing skews by evaluating the cross-correlation between the k^{th} SADC and its two neighbor SADCs the $(k + 1)$ th and $(k - 1)$ th, respectively. These cross-correlations are, in fact, identical to the auto-correlation function at $\pm T_s$,

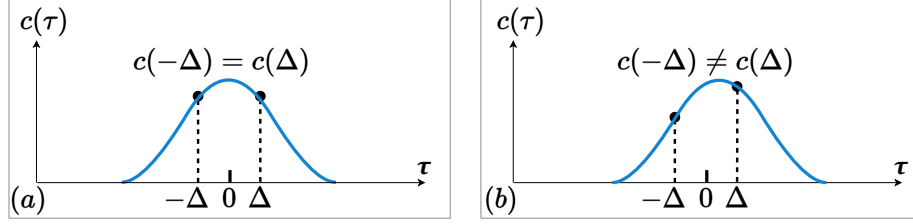


Figure 2.5 Auto-correlation function comparison. (a): the ideal case. (b): in the presence of timing-skew.

$c_k(\pm T_s)$, where T_s is the sampling time (i.e., $= 1/F_s$).

In practice, the cross-correlation function is symmetric to the origin [18]. Figure 2.5 shows an example cross-correlation function. Figure 2.5(a) shows that the cross-correlations values at T_s are identical in the ideal case with no timing skews. In contrast, these values are different in the presence of timing skew as shown in Figure 2.5(b). For this reason, this technique defines the errors as

$$e_k = c_k(T_s) - c_k(-T_s), k = 0, \dots, M - 1. \quad (2.12)$$

The errors, $e_k, k = 0, \dots, M - 1$, are proportional to their respective timing skews. For estimation of the timing skews, this technique uses cross-multiplications to obtain the instant noisy estimate of the cross-correlations $c_k(T_s)$ and $c_k(-T_s)$. This method uses a set of separate negative feedback loops containing integrators, whose outputs adjust the VDLs to eliminate the noise and to drive the cross-correlations by gradually adjusting the correction variables, VDL_k . The sensitivity to the auto-correlation of the input signal at $\pm T_s$ is the main disadvantage of this method.

The method reported in [10] is based on [17]. It performs estimation of the timing skews by evaluating and comparing the cross-correlation function at two points, like the reported method in [17]. However, it can evaluate the cross-correlation at various points, Δ , unlike the technique reported in [17], to reduce the sensitivity to the auto-correlation of the input signal at the cost of using an additional reference SADC. In this method, the reference SADC operates at $F_s/(M + 1)$, similar to the timing pattern proposed in [1]. For this reason, the sampling time of the reference SADC sequentially coincides with one of the SADCs at each sampling time. For calibration of the k^{th} SADC, the sampling edge of the reference SADC alters by $\pm \Delta$ according to a two-level pseudo-random noise (PN) signal. These two states have an equal probability of 0.5. In this mechanism, the absolute value of the difference between the SADCs and the reference SADC is obtained and multiplied with the pseudo-random noise sequence. Due to the alternation of the sampling edge of the reference SADC,

these absolute values can be approximated as

$$e_k(\tau_k) \approx (|\tau_k + \Delta| - |\tau_k - \Delta|) \times \left| \frac{dv_{in}}{dt} \right| \quad (2.13)$$

where e_k denotes the k^{th} estimated timing skew. It is shown that the cross-correlations are ideally identical to zero and proportional to the timing skews τ_k , $k = 0, \dots, M - 1$. The errors are applied to separate discrete-time integrators operating in negative feedback loops to adjust the VDLs and mitigate the timing skews. The main drawback of this method is the need for extra reference SADC and manipulation of the TI-ADC (in addition to using VDLs).

Derivative-Based Calibration Techniques

As mentioned earlier, the error introduced by the timing-skew error can be represented by the first-order approximation of the Taylor series, which requires a derivative operation. The derivative-based approach thus exploits derivation operation in the analog domain to estimate the error raised by timing-skew mismatches. It also corrects the timing skews by VDLs. This mixed-signal approach was introduced in [2] and later developed in [43, 44].

This scheme uses two additional reference SADCs to create reference samples and their associated derivatives, as shown in Figure 2.3. Both reference SADCs operate at the sampling frequency of $F_s/(M + 1)$ with a similar clocking pattern as the one in [1, 15]. Thus, similar to the mechanism in [1], the sampling instances of the reference SADCs repeatedly and sequentially coincide with the sampling instances of the SADCs [15].

For the estimation of the timing-skew in the k^{th} SADC, the error is defined as the difference between the output samples of the reference SADC and the k^{th} SADC, which is approximately proportional to the input signal's derivative as

$$us_k = d_{ref} - d_k \approx \tau_k \times \frac{dV_{in}}{dt}. \quad (2.14)$$

In this approach, the errors us_k , $k = 0, \dots, M - 1$, are compared to the second reference SADC, $SADC_{der}$, to estimate the timing-skews. The second reference SADC samples the derivative of the input signal, obtained by two RC circuits with different bandwidths, as shown in Figure 2.7. It can be shown that the cross-correlation of the second reference SADC and the errors us_k is proportional to the k^{th} timing skew, τ_k . For estimation of the timing skews, this

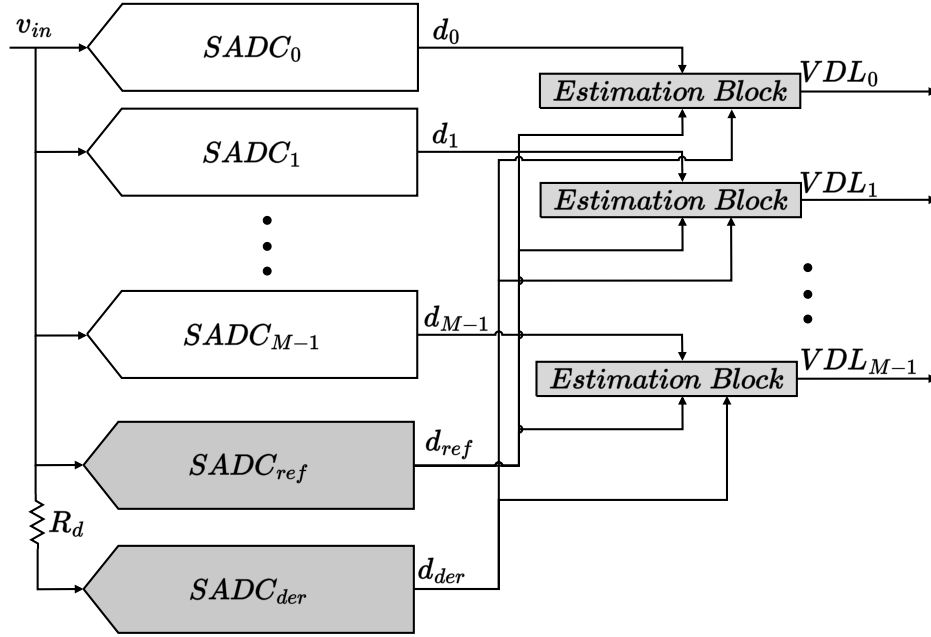


Figure 2.6 Mechanism used for estimation of timing skew in [2].

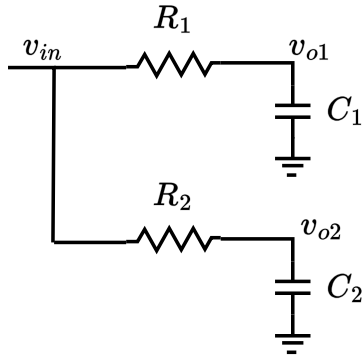


Figure 2.7 RC circuits.

method uses simple products to obtain the instant noisy estimate of the timing skews as

$$c_k(\tau) = us_k \times \frac{dV_{in}}{dt}, k = 0, \dots, M - 1 \quad (2.15)$$

The discrete-time integrators also remove the noise and drive the cross-correlations by gradually adjusting the correction variables, VDL_k . The least squares mean (LMS) algorithm mitigates the errors us_k for $k = 0, \dots, M - 1$. The update expressions in the w^{th} iteration are given by

$$VDL_k(w) = VDL_k(w - 1) + \mu \times c_k(\tau, w - 1), k = 0, \dots, M - 1 \quad (2.16)$$

where μ denotes the loop gain, while VDL_k is the correction variable to the k^{th} variable delay line. The main disadvantage of this mixed-signal technique is the need for two reference SADCs and additional analog circuits (in addition to using VDLs).

Calibration Technique by Injection of Dither Signal

The method in proposed [3] injects a dithered ramp signal as the calibration signal into the input signal for the estimation of the error raised by timing-skew mismatches, as shown in Figure 2.8. It also corrects the timing skews by VDLs.

This injected signal has a ramp shape, modulated with a PN signal, as depicted in Figure 2.9. Thus, the injected signal rises or falls depending on the dither PN signal. The injected ramp signal has a frequency of F_s , beginning sooner at $t_{0,k}$ than the sampling edges of the SADCs at $t_{sm,k}$. Ideally, the value of this signal at the ideal sampling instance, $t_{id,k}$, is $\pm V_{id}$. For this reason, the digital equivalent of $\pm V_{id}$ is subtracted from the digital output of the TI-ADC to cancel out the resolution degradation effect of the injection of the calibration signal. Nevertheless, the timing skews change the sampling edges. Consequently, the value of the ramp signal at the sampling edges alters proportionally to the timing skews and the

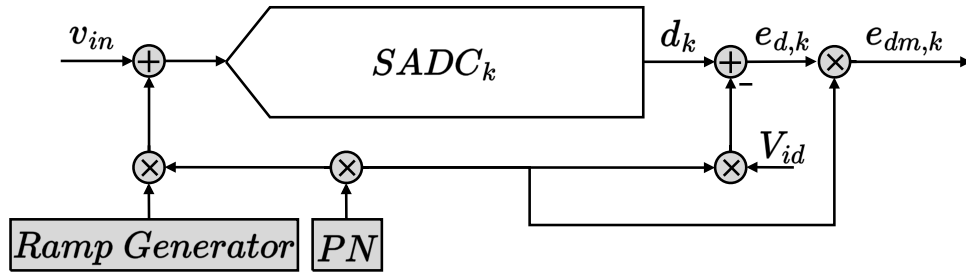


Figure 2.8 Calibration structure in [3].

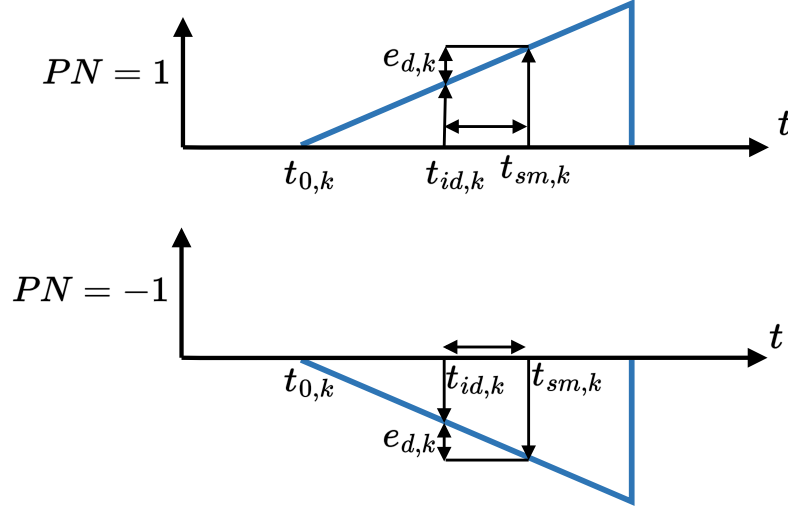


Figure 2.9 Dithered ramp calibration signal used in [3].

pseudo-random signal $\pm V_{id}$ [3]. In this case, the digital output of the TI-ADC conveys the remainder of the injected signal, defined as the timing skew error, as

$$e_{d,k}(\tau_k, m) \approx PN(m) \times V_{id}(m) - d_k(m). \quad (2.17)$$

The error signals, $e_{d,k}$, $k = 0, \dots, M - 1$ conveys the input signal samples and are also proportional to the signal PN . Thus, the error signals must first be demodulated by PN to generate the demodulated signal. The demodulated signal can be expressed as

$$e_{dm,k}(\tau_k, m) \approx e_k(M) - PN(m) \times v_{in}(m) \quad (2.18)$$

where m denotes the discrete-time index of SADCs. The demodulated error signals, $e_{dm,k}$, $k = 0, \dots, M - 1$, are, in the mean, proportional to the errors introduced by the timing skews since the samples of the input signal multiplied with the signal PN having a zero mean. The demodulated error signals can be given to separate negative feedback loops of discrete-time integrators to adjust the VDLs and mitigate the timing skews. This technique is insensitive to the input signal and operates without any reference SADC(s); nevertheless, it calls for additional analog circuits to inject the dithered ramp signal.

2.2.2 Fully Digital Calibration Techniques

Methods that realize the correction and estimation processes in the digital domain are classified as fully digital (or all-digital). This calibration class is suitable for high-resolution

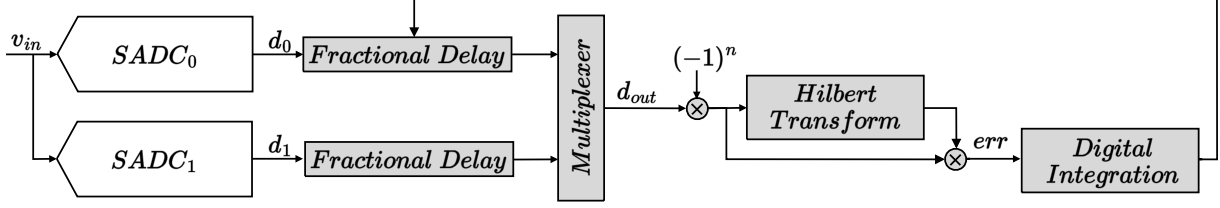


Figure 2.10 Calibration method used in [4].

applications due to its insensitivity to PVT variations. In the following, the most influential methods in this class are reviewed.

Compensation by Using Adjustable FIR Filter

The technique reported in [4] uses adjustable FIR filters for the realization of the fractional delays required to compensate for the timing skew in TI-ADCs consisting of two channels, as shown in Figure 2.10. The coefficients of the tunable FIR filter, associated with each of the required fractional delays, are precomputed. This method needs a lookup table (LUT) to store the set of the required fractional delays along with their associated coefficients [15]. The estimation task aims to remove the timing skew by properly tuning the adjustable FIR filters through the LUT block. It is worth noting that the reported techniques in [25, 45] can be viewed as the improved and extended version of [4] that can be used for calibration of TI-ADC with more SADCs.

The digital estimation part reconstructs the error introduced by the timing-skew mismatch between the two SADC channels. Since the timing-skew mismatch produces an image orthogonal to the input signal at the frequency of $F_s/2 - F_{in}$, where F_{in} denotes the frequency of the input signal, the estimation part thus reconstructs the image by using a chopper to transfer the input signal to the frequency of $F_s/2 - F_{in}$ and a Hilbert transform to make it orthogonal to the input signal [15]. The result of cross-correlation between the image and the reconstructed image indicates the amount of the timing skew error. In this method, the product of the reconstructed image and the digital output of the TI-ADC is alternatively used as a noisy version of the timing-skew error, err . The estimated error signal, err , is applied to a negative feedback loop, consisting of an integrator with an update step, μ , for iteratively driving the error to zero by tuning the adjustable FIR filter.

This approach only applies to two-channel TI-ADC. Also, the need for the variable coefficients in the tunable FIR filter leads to complex hardware.

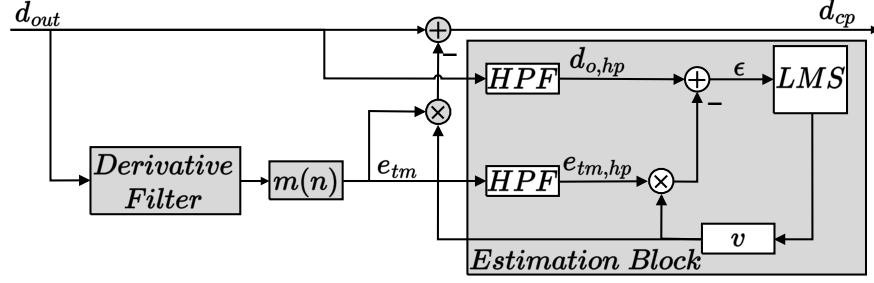


Figure 2.11 Calibration method used in [5].

Compensation Approaches Based on Over-Sampling

A compensation approach based on over-sampling was first introduced in [5]. In this approach, a high band of frequencies is generally dedicated to the estimation process. For this reason, the operational band of frequencies for the input signal is less than the Nyquist frequency.

The technique reported in [5] compensates for the timing skew mismatches by reconstructing the timing-skew error and subtracting the reconstructed signal from the digital output of the TI-ADC, based on over-sampling. For reconstructing the error, this method assumes that the amount of the timing skew is limited such that a first-order approximation of the Taylor series of the error raised by timing-skew mismatches is sufficient (as mentioned in Section 2.1). It estimates and compensates for the timing-skew error without limiting the number of SADCs. This technique also eliminates the need for the bank of adjustable FIR filters at the cost of assuming limited variations in timing skews. The reconstruction procedure uses an FIR filter, $h_d(n)$, realizing the derivative operation, and a modulation matrix, $\mathbf{m}(n)$, whose components are expressed as

$$\mathbf{m}(n) = \begin{bmatrix} 2\cos(1\frac{2\pi}{M}n), -2\sin(1\frac{2\pi}{M}n) \\ 2\cos(k\frac{2\pi}{M}n), -2\sin(k\frac{2\pi}{M}n) \\ 2\cos((\frac{M}{2} - 1)\frac{2\pi}{M}n), -2\sin((\frac{M}{2} - 1)\frac{2\pi}{M}n) \end{bmatrix}. \quad (2.19)$$

The modulation matrix generates the $M - 1$ frequency shifts to reconstruct the required $M - 1$ image components. As seen from Figure 2.11, this matrix is multiplied with the complex correction variables, v_k , $k = 0, \dots, M - 1$, to reconstruct the error components, $e_{tm,k}$, $k = 0, \dots, M - 1$, and then, these errors are subtracted from the digital output of the TI-ADC, d_{out} , for mitigation of the errors due to timing skew mismatches from the corrected digital output, d_{cp} [15].

For the digital estimation part, this approach reuses the reconstructed timing-skew error components, $e_{tm,k}$, $k = 0, \dots, M - 1$, as shown in Figure 2.11. This method thus assigns a band of high frequencies for the estimation procedure of the timing skews since, in the presence of timing skew mismatch, this band of high frequencies must be wide enough to convey information about the timing-mismatch error. As shown in Figure 2.11, high-pass filters (HPFs) are used to filter the TI-ADC digital output, d_{out} , and the error components, $e_{tm,k}$, $k = 0, \dots, M - 1$. The high-pass filtered errors, $e_{tm,hp,k}$, $k = 0, \dots, M - 1$, are compared with the filtered signal $d_{o,hp}$, which conveys the timing skew errors, as following

$$\epsilon_k(n) = d_{o,hp}(n) - e_{tm,hp,k}(n) \times v_k(n), \quad k = 0, \dots, M - 1. \quad (2.20)$$

Then, the LMS algorithm gradually drives the cost functions, defined as $\epsilon_k^2/2$, $k = 0, \dots, M - 1$, to zero by adjusting the correction variables in the correction vector, $\mathbf{v}$, as

$$v_k(n + 1) = v_k(n) + \mu \times e_{tm,hp,k}(n) \times \epsilon_k(n), \quad k = 0, \dots, M - 1. \quad (2.21)$$

Also, the correction variables, v_k , $k = 0, \dots, M - 1$, are respectively multiplied with the reconstructed error components, $e_{tm,k}$, $k = 0, \dots, M - 1$, to reconstruct the timing-skew error. The compensated digital output, d_{cp} , is generated by subtracting the reconstructed error components from the digital output, d_{out} .

As mentioned earlier, this technique restricts the maximum range of timing skews. Also, this technique's performance significantly drops as the input signal's frequency approaches the Nyquist Frequency due to using the derivative operator realized by an FIR filter.

The technique reported in [6] also uses oversampling to estimate timing skew mismatch similar to [5]. This method separates the low-frequency zone for the input signal and the high-frequency band for timing skew mismatch estimation by low-pass filters (LPF) and high-pass FIR filters (HPFs), respectively, as shown in Figure 2.12. In contrast to [5], it eliminates the need for derivative operation by using the error component in the high-frequency band for both the compensation and estimation processes. In the reconstruction approach, the HPF block, along with the modulation blocks M_2 and M_4 , reconstructs the timing skew errors.

In the digital compensation part, the reconstructed error, e_{tm} , is first de-multiplexed as $[e_{tm,0}, e_{tm,1}, e_{tm,2}]$ and multiplied with the correction variables, $\mathbf{v} = [v_0, v_1, v_2]$, and then, the results are subtracted from the de-multiplexed high-passed digital outputs, $\mathbf{d}_{hp} = [d_{hp,0}, d_{hp,1}, d_{hp,2}]$, to create the compensated signals, $\{d_{cp,0}, d_{cp,1}, d_{cp,2}\}$. Finally, the compensated signals, $\{d_{cp,0}, d_{cp,1}, d_{cp,2}\}$, are multiplexed to generate the compensated signal d_{cp} .

The estimation block compares the high-frequency band in the compensated digital output

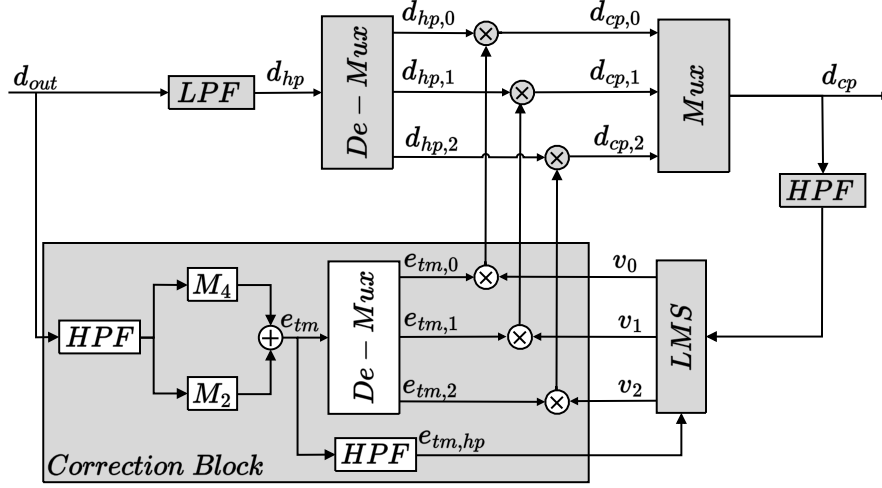


Figure 2.12 Method used in [6].

with the reconstructed error, e_{tm} , by defining the estimation error as

$$\epsilon(n) = h_{hp} * z(n) = h_{hp}(n) * \{\mathbf{d}_{hp}^T(n) - \mathbf{v}(n) \cdot \mathbf{e}_{tm}(n)\}. \quad (2.22)$$

where $h_{hp}(n)$ represents the impulse response of the HPF filters, while $(.)^T$ denotes the transpose operation. The LMS algorithm aims at minimizing the cost function, defined as $\epsilon^2(n)$, to eliminate the timing-mismatch errors in the compensated signal d_{cp} . Minimizing the cost function denotes mitigating timing skew mismatch errors in the compensated digital output. The update expression of the LMS algorithm is given by

$$\mathbf{v}(n) = \mathbf{v}(n-1) + \mu \frac{\partial(\epsilon^2(n))}{\partial \mathbf{v}} \quad (2.23)$$

where

$$\frac{\partial(\epsilon^2(n))}{\partial \mathbf{v}} = 2 \times \epsilon(n) \times HPF * d_{out}(n). \quad (2.24)$$

The advantage of this method over the reported method in [5] is eliminating the need for the FIR filter to approximate the derivative operator [3]. However, it restricts a high-frequency zone due to using an over-sampling mechanism.

Compensation Approaches Based on Pseudo-Aliasing Generation

The technique reported in [7] uses the derivative operator, the same as the method proposed in [5], as depicted in Figure 2.13. Unlike the technique in [5], it exploits the Hadamard transform as the modulation matrix for the estimation part to significantly reduce the implementation

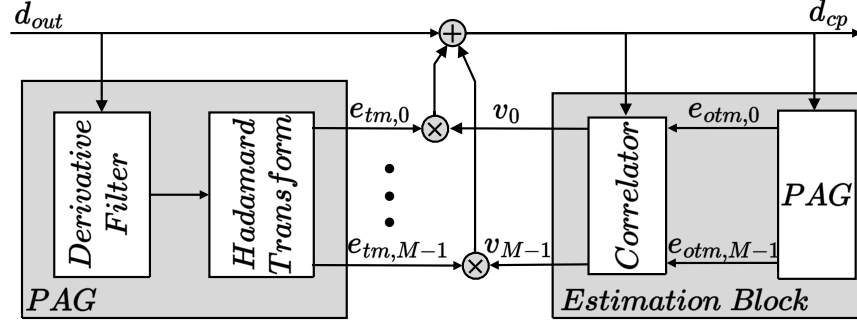


Figure 2.13 Calibration method used in [7].

complexity since the elements of the Hadamard transform are ± 1 [8, 15]. In this method, the combination of the derivative operator and the Hadamard transform is called the pseudo-aliasing generator (PAG). The PAG generates the pseudo-aliasing components, $e_{tm,k}$, $k = 0, \dots, M - 1$. The pseudo-aliased components are multiplied with their associated correction variables, v_k , $k = 0, \dots, M - 1$, to generate the error components in the digital output of TI-ADC, d_{out} , as shown in Figure 2.13.

For the correction part, this approach also uses a replica of the PAG to generate the pseudo-aliasing components, $e_{otm,k}$, $k = 0, \dots, M - 1$, from the compensated digital output, d_{cp} . In the correction part, the correlator block extracts the estimates of the cross-correlation of the pseudo-aliased components and the compensated digital output, d_{cp} . The cross-multiplications followed by MA filters realize the cross-correlation mechanism in the correlator block. In [7], it is shown that the timing skew errors can be detected by cross-multiplication between the pseudo-aliased components of the digital output, $\mathbf{e}_{otm}$, and the compensated output, d_{cp} , expressed as

$$\epsilon = c(\mathbf{e}_{otm} \cdot d_{cp}) \quad (2.25)$$

where $c(\cdot)$ denotes the cross-correlation operator. It is notable that the vector ϵ is proportional to

$$\epsilon \propto \mathbf{c}_{tm} - \mathbf{e}_{tm} \quad (2.26)$$

where the elements of the vector $\mathbf{c}_{tm}$ stand for the timing-skew error components in the digital output of TI-ADC [15]. The cross-correlation vector, ϵ , is estimated by multiplications followed by MA filters. The elements of the vector ϵ are separately applied to a set of negative feedback loops consisting of integrators to drive all the elements of ϵ to zero by properly tuning

the correction variables $\mathbf{v}$.

Similar to the reported method in [5], this technique restricts the maximum range of timing skews. Moreover, its performance degrades as the input signal frequency approaches the Nyquist Frequency. Finally, this technique limits the number of SADC channels to 2, 4, 8, ...

Compensation Approaches Based on Polyphase Decomposition

In this approach, the polyphase decomposition is utilized to relieve the speed requirement in the estimation and compensation parts by directly operating on the digital outputs of SADCs, instead of the digital output of TI-ADC. This scheme is first introduced in [46] and later enhanced in [8, 9]. These techniques are briefly reviewed in the following.

The method reported in [8] uses polyphase decomposition to reconstruct the error introduced by timing-skew mismatches. As mentioned above, this method directly operates on the SADC's outputs instead of the TI-ADC's digital output. Also, it operates with an arbitrary number of SADC channels. The method uses the polyphase derivative operation proposed in [46] to reconstruct the timings-skew mismatch error. The compensated output is obtained by subtracting the reconstructed error from the digital output of the SADCs. The estimation part of this method is similar to the method reported in [7]. Nevertheless, the PAG is replaced with the polyphase derivative operation.

First, the polyphase realization approach introduced in [46] is briefly reviewed. In this approach for the correction part, the outputs of the SADCs are expressed as

$$\begin{aligned} \mathbf{D}(z) &= \mathbf{Q}(z) \mathbf{DL}(z) V_{in}(z), \\ \mathbf{D}(z) &= [D_0(z) \ D_1(z) \ \cdots \ D_{M-1}(z)]^T, \\ \mathbf{DL}(z) &= [z^{-M+1} \ \cdots \ z^0]^T. \end{aligned} \tag{2.27}$$

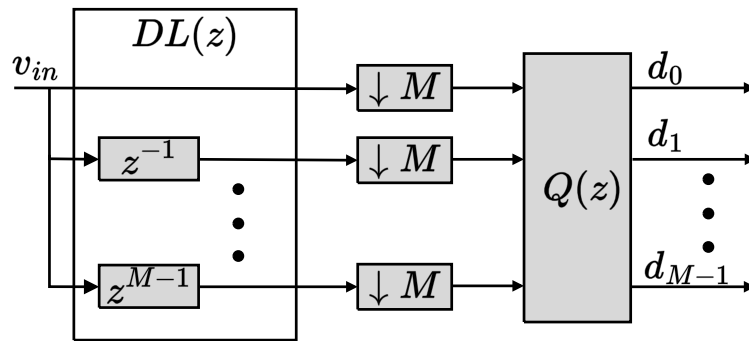


Figure 2.14 Polyphase structure of M -channel TI-ADC.

where $\mathbf{Q}$ and $\mathbf{DL}$ respectively denote the polynomial analysis bank and the delays of sampling time in the SADCs, as shown in Figure 2.14. The elements of the analysis bank represent the timing skews as

$$\mathbf{Q}(e^{j\omega}) = \text{diag}\{e^{j\omega\tau_0}, \dots, e^{j\omega\tau_{M-1}}\}. \quad (2.28)$$

The analysis bank can be represented by its first-order approximation of the Taylor series as

$$Q_k(e^{j\omega}) = e^{j\omega\tau_k} \approx 1 + \delta_k H_D(e^{j\omega}) \quad (2.29)$$

where $H_D(e^{j\omega})$ stands for the derivative operation, expressed as

$$H_D(e^{j\omega}) = j\omega. \quad (2.30)$$

As a consequence, the analysis filter bank can be expressed as

$$\mathbf{Q}(z) \approx \mathbf{I} + \tau \mathbf{P}(z), \quad (2.31)$$

$$\tau = \text{diag}\{\tau_0 \dots \tau_{M-1}\} \quad (2.32)$$

where $\mathbf{I}$ denotes $M \times M$ identity matrix, and also, $\mathbf{P}(z)$ represents the derivative operation, $H_D(z)$, realized by the polynomial decomposition as

$$\mathbf{P}(z) = \begin{bmatrix} P_0(z) & z^{-1}P_{M-1}(z) & \cdots & z^{-1}P_1(z) \\ P_1(z) & P_0(z) & \cdots & z^{-1}P_2(z) \\ \vdots & \vdots & \ddots & \vdots \\ P_{M-1}(z) & P_{M-2}(z) & \cdots & P_0(z) \end{bmatrix}. \quad (2.33)$$

In [46], it is shown that a *near-perfect* reconstruction can be achieved by the first-order inverse function, expressed as

$$\mathbf{R}(z) = \mathbf{I} - \mathbf{V}(z)\mathbf{P}(z) \quad (2.34)$$

where $\mathbf{V}(z)$ denotes $M \times M$, a correction matrix whose elements are ideally identical to their associated elements in the timing-skew vector τ . Therefore, the correction part of the reported method in [8] generates the compensated digital outputs as

$$\begin{aligned} \mathbf{D}_{cp}(z) &= (\mathbf{I} - \mathbf{V}(z)\mathbf{P}(z))\mathbf{D}(z), \\ \mathbf{D}_{cp}(z) &= [D_{cp,2}(z) \ D_{cp,1}(z) \cdots D_{cp,M-1}(z)]^T. \end{aligned} \quad (2.35)$$

The digital estimation block of this method is shown in Figure 2.15. In [8], it is proved that

the following cross-correlation vector

$$\mathbf{E}(z) = c(\mathbf{D}_{cp}(z) \cdot \mathbf{P}(z) \mathbf{D}_{cp}(z)) \quad (2.36)$$

is proportional to $\tau - \mathbf{V}(z)$, where $c(\cdot)$ denotes the correlation operator. For this reason, the cross-multiplications are used to extract the instant values of cross-correlations, and a set of M integrators are utilized in negative feedback loops to derive the mean of the cross-multiplications to zero by adjusting the correction vector $\mathbf{V}$ as

$$\mathbf{V}(z) = z^{-1} \mathbf{V}(z) + \mu \times \epsilon(z) \quad (2.37)$$

where μ is the loop gain, determining the stability and convergence rate in this method.

As mentioned earlier, this technique can be applied to TI-ADCs with an arbitrary number of SADC channels since the need for Hadamard transform is alleviated by exploiting polyphase implementation of derivative filter in [7]. However, this approach limits the maximum timing-skew span, similar to [5, 7]. Also, this technique's performance significantly declines as the input signal's frequency approaches the Nyquist Frequency due to utilizing the derivative operator realized by the polyphase FIR filter.

The reported technique in [9] (and its recent version [24]) uses the same structure as [8, 46] to cancel out the timing skew mismatch in the correction part. Nevertheless, it shares the polyphase derivative filter, $\mathbf{P}(z)$, for performing both correction and estimation parts, as shown in Figure 2.16. The following briefly explains the procedure for estimating the correction variables.

The reported method in [9] shows that the expectation of the difference between the SADC

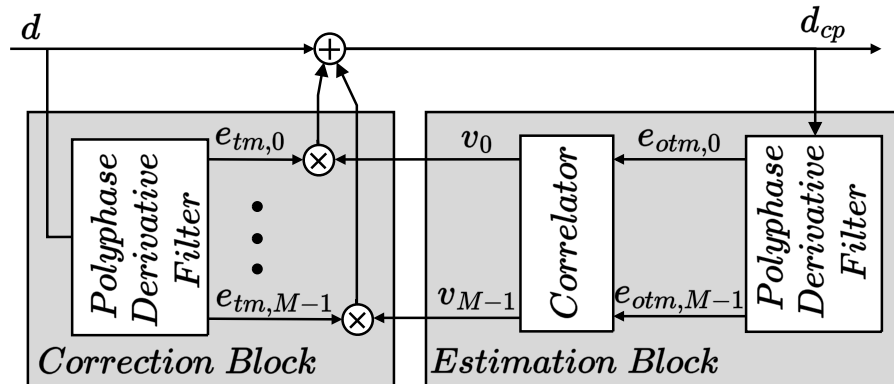


Figure 2.15 Estimation part of the method used in [8].

is proportional to the derivative of the SADCs' outputs as

$$\Delta d_k = d_{k+1} - d_k \approx (T + \tau_{k+1} - \tau_k) \nabla d_k \quad (2.38)$$

where Δ represents the difference between the two neighbor SADCs' outputs, while ∇ is the derivative operation. Also, the difference between two neighbor timing skews is estimated as

$$b_k = (E|\Delta d_k| - \bar{\Delta}d) / \bar{\nabla}d, \quad (2.39)$$

$$b_k = \tau_{k+1} - \tau_k, \quad k = 0, 1, \dots, M-2 \quad (2.40)$$

where the mean of Δd_k and ∇d_k , $k = 0, \dots, M-2$, are respectively expressed as

$$\bar{\nabla}d = \frac{1}{M} \sum_{k=0}^{M-1} E\{|\nabla d_k|\}, \quad (2.41)$$

$$\bar{\Delta}d = \frac{1}{M} \sum_{k=0}^{M-1} E\{|\Delta d_k|\} \approx T_s \cdot \bar{\nabla}d \quad (2.42)$$

where $E|\cdot|$ denotes the expectation operation, practically realized by an MA filter as

$$E|x| \approx \frac{1}{L} \sum_{n=(r-1)L}^{rL-1} x(n) \quad (2.43)$$

where L represents the number of averaged samples, while r represents the update index of the MA filter. The timing skews can be separated by using the matrix $\mathbf{B}$ as

$$\tau = \mathbf{B}\mathbf{b} \quad (2.44)$$

where the matrix $\mathbf{B}$ is defined as

$$\mathbf{B} = \frac{1}{4} \begin{bmatrix} -3 & -2 & -1 & 1 \\ 1 & -2 & 1 & 1 \\ 1 & 2 & -1 & 1 \\ 1 & 2 & 3 & 1 \end{bmatrix}. \quad (2.45)$$

The estimation method in the reported method in [9] needs less hardware than its previous relevant methods [8, 46] since it does not require any FIR filter for the estimation part. Like the methods reported in [5, 7, 8, 46], this technique also suffers from restrictions on the maximum range of timing skews. In addition, its performance significantly drops as the input signal frequency approaches the Nyquist Frequency because of using the derivative operator

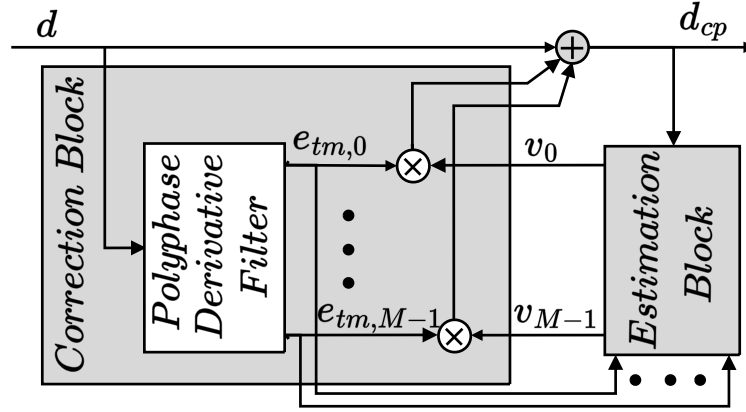


Figure 2.16 Method used in [9].

realized by the polyphase FIR filter.

CHAPTER 3 ARTICLE 1 : DIGITAL BACKGROUND ESTIMATION OF TIMING-SKEW MISMATCHES IN TIME-INTERLEAVED ADCS

The article entitled "*Digital Background Estimation of Timing-Skew Mismatches in Time-Interleaved ADCs*" will be presented in this chapter. The brief conference version of this article has been published in "*Background Calibration of Time-Interleaved ADCs with Polyphase Filters*" and the current version of this article has been submitted to "IEEE Transactions on Very Large Scale Integration (VLSI) Systems". This chapter proposes the concept of time shift as a main contribution to desensitizing the estimation mechanism to the input signal's autocorrelation. One finite impulse response (FIR) filter also generates the required time shifts. Moreover, the FIR filter is implemented by the polyphase decomposition mechanism to relieve the proposed method's speed requirement. This proposed fully digital estimation method operates without additional SADC(s) and without manipulating the TI-ADC architecture, making it suitable for all digital calibration mechanisms.

Digital Background Estimation of Timing-Skew Mismatches in Time-Interleaved ADCs

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3.1 Abstract

This paper proposes using the novel concept of time shifts realized with a polyphase finite impulse response (FIR) filter to estimate timing-skew mismatches in time-interleaved ADCs (TI-ADCs). For the first time, time shifts are used to estimate the cross-correlation at various points, desensitizing the estimation of the auto-correlation distribution of the input signal. The required time shifts are generated by a widely used polyphase FIR filter approach, which can better deal with the functional speed requirement than conventional filters. Comparisons of the output cross-correlation of the sub-ADCs are used to estimate the timing skew mismatches. The proposed all-digital estimation method is a sensible choice when the input signal's auto-correlation has zero value or discontinuity. This method eliminates the need for

additional reference sub-ADC(s) for timing mismatch calibration. The proposed calibration technique was implemented and simulated with MATLAB/Simulink, Xilinx Vivado Design Suite, and field-programmable gate array (FPGA). In one of the best-reported experiments, the signal-to-noise-and-distortion ratio (SNDR) of a specific benchmark was enhanced from 37.44 dB to more than 56.64 dB in a 10-bit TI-ADC when the timing-skew has a standard deviation of 10 % of the TI-ADC's sampling interval.

3.2 Introduction

Among them, the most interesting class of estimation mechanisms is based on the input signal's cross-correlation function.

This paper proposes a fully digital scheme for background estimation of timing skew mismatches in the context of the cross-correlation function concept. Our proposed architecture uses the novel concept of time shifts to assess and compare the cross-correlation function at two symmetric points by a polyphase finite impulse response (FIR) filter. The proposed technique aims at desensitizing the estimation to the auto-correlation of the input signal. Consequently, our all-digital estimation approach is a reasonable choice when the input signal's autocorrelation has zero value or discontinuity (e.g., at T_s). For decades, the multi-rate approach has been widely used to improve the speed of operation in various fields [47]. The polyphase decomposition approach has been widely used to realize *derivative operation* and *Hilbert transform* [8, 46]. Nevertheless, our paper uses the polyphase mechanism to implement FIR filter generating the *time-shift operation*. Other beneficial aspects of the proposed estimation approach are pure digital realization without the need for any modification of the TI-ADC and/or the exploitation of extra sub-ADC(s), unlike the methods reported in [1, 10, 19].

The remainder of the paper is structured as follows. Section 3.3 presents the proposed method, and Section 3.4 reports simulation results characterizing its performance. Then, a discussion and a comparison of our work with previously reported methods are presented in Section 3.5. Finally, Section 3.6 concludes the main findings of the paper.

3.3 Proposed Calibration Method

A set of M identical sub-ADCs constitute a typical TI-ADC as shown in Fig. 3.1. It is worth mentioning that sub-ADCs sample their input signals based on a clocking pattern. The sub-ADCs sequentially and repeatedly sample the input signal every $1/F_s$ seconds according to this clocking pattern, which makes the overall sampling rate of the TI-ADC, F_s ,

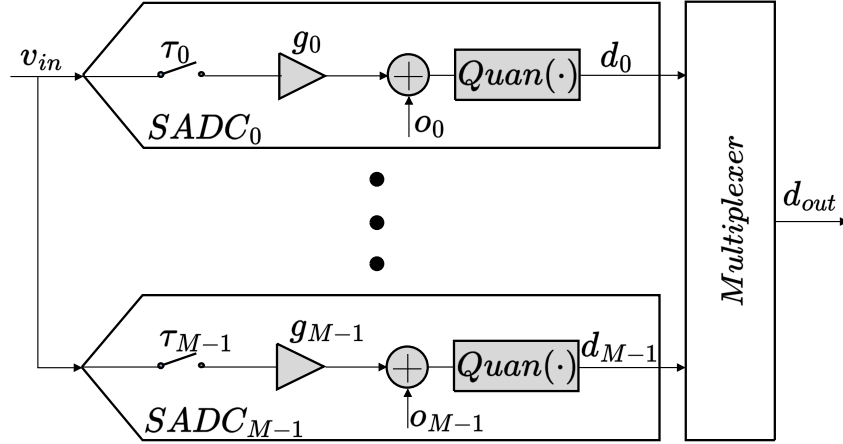


Figure 3.1 The architecture of a typical time-interleaved ADC (TI-ADC).

M times faster than the sampling rate of each sub-ADC [6, 18]. Nevertheless, additional calibration means must be exploited to retrieve the desired effective resolution by estimating and compensating for the mismatches (including offset, gain, and timing skew). Without loss of generality, the offset and gain mismatches are considered compensated before applying our technique in the remainder of the paper. Methods to do so are reported in [20, 28, 48–50].

TI-ADCs typically multiplex the outputs of sub-ADCs to create the digital output, d_{out} , which can be mathematically expressed as

$$d_{out}(n) = \sum_{k=0}^{M-1} d_k(\lfloor n/M \rfloor) \times \delta_k(n) \quad (3.1)$$

where n denotes the discrete-time index associated with the rate of F_s , while $\delta_k(n)$ is $\delta(n \bmod M - k)$ and $\lfloor \cdot \rfloor$ represents the floor function [18, 20].

3.3.1 Theoretical Framework

The cross-correlation function exhibits symmetry around the origin without the timing skew [18, 20]. Fig. 3.2(a) depicts the cross-correlation function values at $\pm\Delta$, $c(\pm\Delta)$, which would be ideally identical. The cross-correlation function manifests its peak at the origin ($\tau = 0$) and symmetrically decreases towards both positive and negative sides [18, 41]. Nonetheless, the cross-correlation function is shifted from the origin along the time axis proportionally to the timing skew, which causes the cross-correlation values $c(\pm\Delta)$ to vary in the presence of timing skew, as depicted in Fig. 3.2(b). The proposed method views the difference between the cross-correlation function at these two points $\pm\Delta$ (i.e., $c(+\Delta) - c(-\Delta)$) as the timing

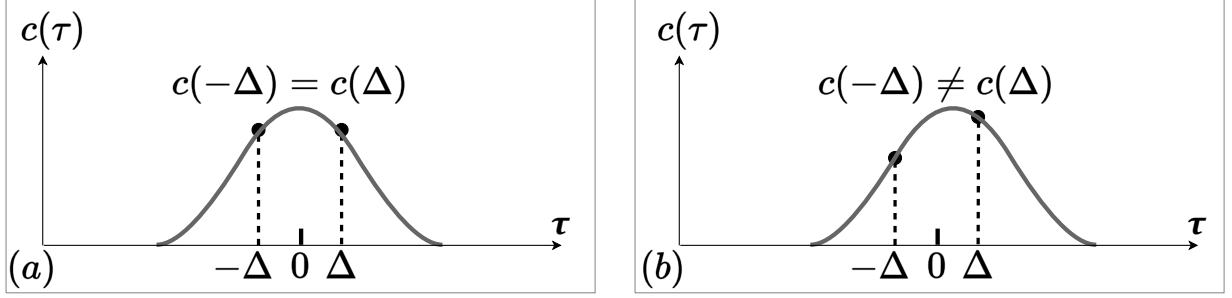


Figure 3.2 Cross-correlation function at $\pm\Delta$ (a) Without any timing skew and (b) With timing skew.

skew error [10, 41]. This error signal reveals the path to the timing skew mismatch that needs to be mitigated. Our calibration method performs on the digital version of the input signal, d_{out} (i.e., the digital output); consequently, two time-shifted versions of d_{out} at $\pm\Delta$, $d_{out,\pm\Delta}$ can be generated by two separate fractional-delay FIR filters. The outputs of the FIR filters with $2L + 1$ taps are given by

$$d_{out,\pm\Delta}(n) = \sum_{i=-L}^L d_{out}(n-i) \times h_{\pm\Delta}(i) \quad (3.2)$$

where $h_{\pm\Delta}(i)$ stands for the coefficients that are equal to $\text{sinc}(i \pm \Delta)$ [39, 41]. As evident from (3.2), the principle of this time shift generation filter is based on a reconstruction filter with a sampling rate of one [39, 41]. Ideally, the length, L , would be infinite; nevertheless, this is practically limited and selected according to the specifications of the input signal.

Estimating the cross-correlation function's values at $\pm\Delta$ is worth noting, as these values are not directly available in practice and must be estimated through digital circuits. For this reason, the outputs of the two FIR filters, mentioned above, are first multiplied by the output d_{out} . Afterward, the two multiplications are applied to two *moving average* (MA) filters to estimate the cross-correlation function at $\pm\Delta$. The estimated cross-correlation values at $\pm\Delta$ can be given by

$$\hat{c}(\pm\Delta) = \frac{1}{K+1} \sum_{i=n-K}^n d_{out}(i) \times d_{out,\pm\Delta}(i) \quad (3.3)$$

where K represents the number of samples being averaged.

3.3.2 Timing Skew Estimation of Sub-ADCs

This paper has established the required theoretical framework thus far. The following presents a feasible means of properly exploiting this concept. As mentioned earlier, each sub-ADC

generally has its own *random-in-essence* timing skew that must be separately extracted and compensated for. At this point, it would be insightful to consider the time-shifted signals, $d_{out,\pm\Delta}$ as the output of two *abstract* TI-ADCs, and also, following (3.1), the time-shifted versions of the digital output can be equivalently expressed as

$$d_{out,\pm\Delta}(n) = \sum_{k=0}^{M-1} d_{\pm\Delta,k}(\lfloor n/M \rfloor) \times \delta_k(n) \quad (3.4)$$

where $d_{\pm\Delta,k}$ can thus be considered the output of the k^{th} sub-ADC from the two separate abstract TI-ADCs. Corresponding to the k^{th} sub-ADC, $k = 1, \dots, M$, the cross-correlation function's values at $\pm\Delta$, $\hat{c}_k(+\Delta)$ and $\hat{c}_k(-\Delta)$ can be estimated by *MA* filters as

$$\hat{c}_k(\pm\Delta) = \frac{1}{K+1} \sum_{i=m-K}^m d_k(i) \times d_{\pm\Delta,k}(i) \quad (3.5)$$

where m denotes the discrete-time index associated with the rate of F_s/M . Following the framework mentioned above, it is convenient to define the timing skew associated with the k^{th} sub-ADC as the difference between $\hat{c}_k(+\Delta)$ and $\hat{c}_k(-\Delta)$ as

$$err_k = \hat{c}_k(+\Delta) - \hat{c}_k(-\Delta) \quad (3.6)$$

where $k = 1, \dots, M$. The k^{th} observed error, err_k , is proportional to the k^{th} timing skew. In addition, the ideal case would be $err_k = 0$ for $k = 1, \dots, M$. Therefore, these observed error signals can be used to gradually tune VDLs as required to decrease and possibly mitigate the timing skew mismatches in all the sub-ADCs. A bank of M discrete-time integrators embedded in separate negative feedback loops can be employed to eliminate these errors.

3.3.3 Complexity Reduction

The method mentioned above requires two FIR filters, $2M$ multipliers, and $2M$ *MA* filters for the cross-correlation estimation. It is straightforward to show that the following expression

$$err_k = \frac{1}{K+1} \sum_{i=m-K}^m d_k(i) \times d_{mg,k}(i), \quad (3.7)$$

with the k^{th} merged signal $d_{mg,k}(m)$, identical to $d_{\Delta,k}(m) - d_{-\Delta,k}(m)$, is equivalent to the expression (3.6). Since the same input is used to generate $d_{k,\Delta}(m)$ and $d_{k,-\Delta}(m)$ by two

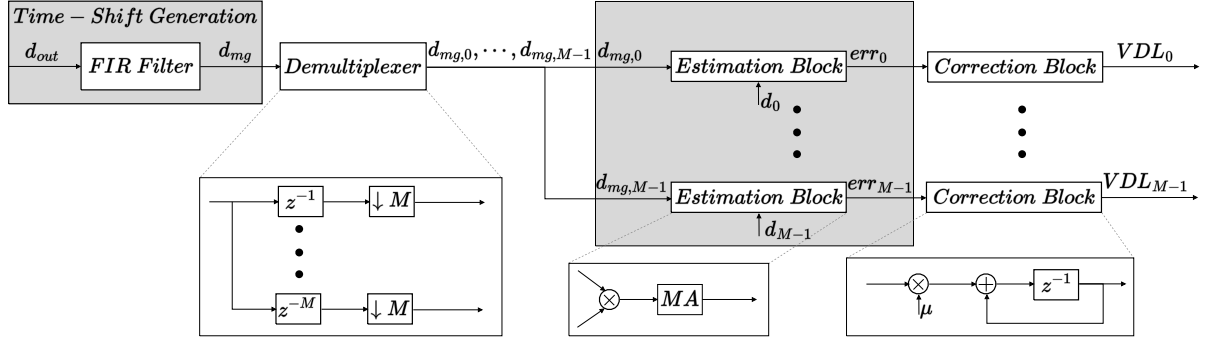


Figure 3.3 Architecture of the proposed calibration method.

separate FIR filters. It is possible to use a single merged filter as following

$$d_{mg}(n) = \sum_{i=-L}^L d_{out}(n-i) \times h_{mg}(i), \quad (3.8)$$

with $h_{mg}(i)$ denoting the i^{th} coefficient of the merged filter expressed as

$$h_{mg}(i) = h_{\Delta}(i) - h_{-\Delta}(i). \quad (3.9)$$

After these modifications, the proposed method needs a single FIR filter, M multipliers, and M moving average filters to extract the error signals. This reduces the hardware implementation cost by a factor of two. Fig. 3.3 shows the structure of the proposed method after the above-mentioned modifications. The error signals are applied to a set of M discrete-time integrators in M separate negative feedback loops. The update equations that adjust VDLs can be expressed as

$$VDL_k(w+1) = VDL_k(w) + \mu \times err_k(w) \quad (3.10)$$

where w represents the discrete-time index associated with the rate of $F_s/(M \times K)$, while μ denotes the loop gain determining the convergence rate and fluctuation amount of the VDLs. The discrete-time integrators in the feedback loops provide *infinite* DC gain [51] to iteratively drive the mean values of the error signals to zero.

3.3.4 Polyphase Implementation

If the TI-ADCs sampling rate is higher than the rate at which the FIR filter can function, using a polyphase implementation of the FIR filter becomes rational [8,39]. In this interesting trade-off, a faster functional speed can be compromised for a higher hardware cost. For instance, the FIR filter can operate at a reduced rate of F_s/M at the cost of increasing M

times the chip area. In this polyphase implementation, the coefficients of the polyphase FIR filter are obtained by finding the polyphase components [8, 39, 46, 52] as following

$$H_{mg}(z) = \sum_{i=0}^{M-1} z^{-i} H_i(z^M) \quad (3.11)$$

where $H_{mg}(z)$ stands for the z-domain representation of the filter $h_{mg}(\cdot)$, while $H_i(\cdot)$ denotes the i^{th} polyphase component. The polyphase FIR filter is then expressed as

$$\mathbf{H}_{mg}(z) = \begin{bmatrix} H_0(z) & z^{-1}H_{M-1} & \dots & z^{-1}H_1(z) \\ H_1(z) & H_0(z) & \dots & z^{-1}H_2(z) \\ \vdots & \vdots & \ddots & \vdots \\ H_{M-1}(z) & H_{M-2}(z) & \dots & H_0(z) \end{bmatrix}. \quad (3.12)$$

The outputs of the polyphase FIR filter are given by

$$\begin{bmatrix} D_{mg,0}(z) \\ \vdots \\ D_{mg,M-1}(z) \end{bmatrix} = \mathbf{H}_{mg}(z) \times \begin{bmatrix} D_0(z) \\ \vdots \\ D_{M-1}(z) \end{bmatrix} \quad (3.13)$$

where $D_k(z)$ and $D_{mg,k}(z)$ respectively denote the frequency representations of the digital output of the k^{th} sub-ADC and the k^{th} merged signal $d_{mg,k}$. In this polyphase implementation, the outputs of the sub-ADCs are directly applied to the polyphase FIR filter as depicted in Fig. 3.4. For this reason, the processing speed of this polyphase implementation is the same as the sub-ADCs. In turn, the polyphase implementation does not increase the power dissipation compared to the single-rate implementation since the polyphase FIR filter operates at $1/M$ th of the single-rate FIR filter [41].

In the polyphase version of the proposed technique, the errors err_k , $k = 1, \dots, M$, are estimated by a set of M multipliers and M moving average filters as shown in Fig. 3.4. The polyphase architecture also uses (3.10) to adjust VDLs. As mentioned earlier, the discrete-time integrators in the feedback loops offer infinite DC gain [51] causing the mean values of the error signals, err_k , $k = 1, \dots, M$, to be iteratively driven to zero. The loop gain, μ , determines the convergence rate and fluctuation amount of the VDLs. As the number of samples used in the MA filter increases, a more precise estimate of the cross-correlation values can be obtained at the cost of a slower convergence rate. Consequently, it should be chosen suitably according to the requirements of a specific application. The parameter μ must be chosen judiciously to guarantee stability as the convergence rate directly depends on it [20, 51].

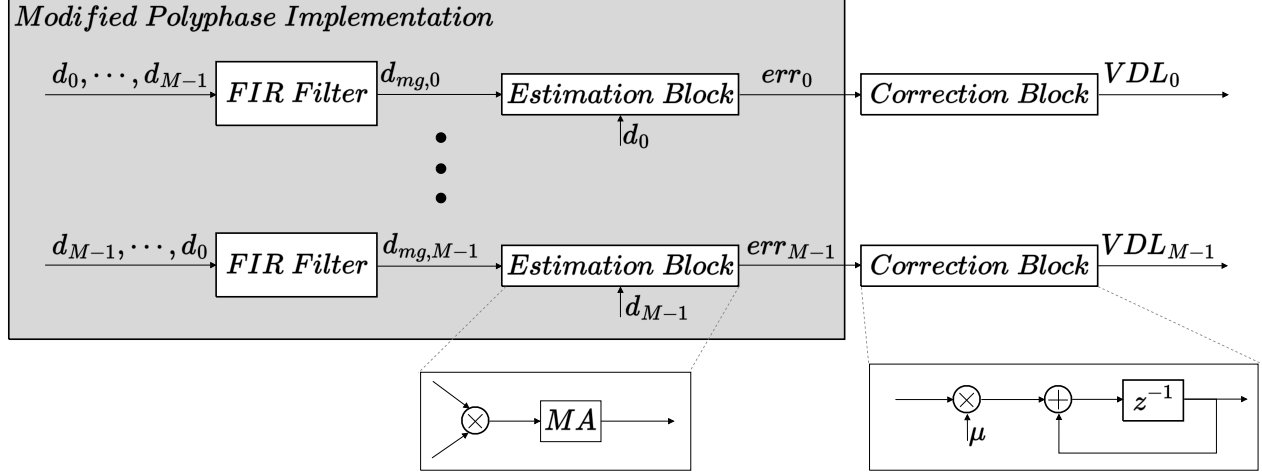


Figure 3.4 Multirate implementation of the proposed method.

3.4 Simulation Results

MATLAB/Simulink, the Vivado Design Suite, and field-programmable-gate-array (FPGA) are used to verify our proposed method, where a TI-ADC consisting of a set of 4 identical sub-ADCs (i.e., $M = 4$) was constructed. This TI-ADC, subjected to timing skews and thermal noise, is modeled in Simulink with floating point precision for all the following simulations. This section aims to verify the effectiveness of the proposed estimation method, validate the synthesizability of the Simulink model implementing the proposed method with fixed-point precision, and evaluate the hardware and power costs of the proposed method with various word widths. For simplicity, the constructed TI-ADC's sampling rate is set to 1 Hz. In our simulations, the effective resolution of the sub-ADCs, B , is set to 10 bits (using quantizers and thermal noise). In these simulations, the timing skew of each channel is generated randomly and independently with Gaussian distribution, and the standard deviation of the timing skew was assumed to be 10 % of the TI-ADC's sampling interval. In addition, the following simulations ensure the proper convergence of the calibration method by setting the parameter μ to 2^{-4} and selecting the number of samples averaged by MA filter, K , 256. Also, Δ is set to 0.4.

The following uses fast Fourier Transforms (FFTs) of the length N_{fft} to evaluate the performance of our method. Additionally, special tones with a length of N_{fft} are applied to prevent any leakage in all the following simulations. Since the bin's index in the FFT, I_{bin} , is related to the frequency of the input tones as $F_{in} = F_s \times I_{bin} / N_{fft}$, this paper alternatively refers to I_{bin} instead of the frequency of input tones. The parameter N_{fft} is set to $2^{(B+1)}$ (i.e., 2^{11}). Moreover, prime numbers in the range of $\{1, \dots, N_{fft}/2\}$ are selected for I_{bin} to

prevent repetitive patterns in the input tone(s) [53, 54].

To begin with, the proposed estimation method is modeled with floating point precision. Table 3.1 shows the impact of the VDL bit width on the signal-to-noise-and-distortion ratio (SNDR) when the maximum timing skew correction range of VDLs is considered 0.6 of the sampling interval. Additionally, all the results correspond to the same single-tone sine wave with its associated bin's index, I_{bin} , of 381, and the length L of 20. As seen in Table 3.1, 9-bit VDLs are required to reach the SNDR of 56.86 dB.

The following simulations target implementing the proposed technique on FPGA and evaluating the impact of word width on performance. For this reason, all the prime values are used for the bin index I_{bin} to extract the mean of the SNDRs observed for each word width. This part uses a single-tone sine wave with its associated bin's index, I_{bin} . In each run, I_{bin} is sequentially selected as a prime number from the interval $\{1, \dots, N_{fft}/2\}$, and a total number of 171 runs are performed for each word width. The length L is set to 20. In all simulations, the results correspond to the same set of timing-skew. Table 3.2 shows the impact of the word width on the SNDR. Although the SNDR improves as the word width increases from 8 to 10 bits, it remains almost constant beyond 10 bits.

The MATLAB/Simulink HDL Coder and the FPGA-in-the-Loop (FIL) Wizard are used to implement the proposed method as a Simulink model with fixed-point precision on an FPGA and evaluate the hardware and power consumption costs. In this case, the Simulink model is first converted to the Verilog HDL language. Then, the FIL Wizard synthesizes the Verilog code and programs the FPGA using the Xilinx Vivado Design Suite [55]. The implementation diagram is also depicted in Fig. 3.5. For our purpose, the Xilinx Virtex-7 VX690T, implemented with 28 nm FPGA technology, is employed. The VX690T series of Xilinx Virtex-7 consists of 2800 digital signal processing (DSP) slices and 485 logic cells. The communication rate of the FPGA was set to 25 MHz.

Table 3.3 corresponds to the results of the FPGA implementation of the proposed calibration method with different word widths and the polyphase FIR filter with the length $L = 20$. The hardware and its associated power consumption increase as the word width increases. According to Tables 3.2 and 3.3, the best choice is to select a word width of 10, and increasing the word width beyond 10 bits just leads to more power consumption without meaningful SNDR improvement.

In all the following simulations, VDLs with 9-bit resolution are used. In this case, the time step of the VDLs is equal to 1.16×10^{-3} . The following simulations also correspond to the FPGA implementation of the proposed technique with a word width of 10 bits and a length L of 20. For reliable verification, different separate sets of simulations are also performed

Table 3.1 Impact of VDL Resolution on SNDR

Resolution (bits)	7	8	9	10	11
$Mean_{SNDR}$ (dB)	51.15	54.07	56.86	58.02	58.31
σ_{SNDR} (dB)	3.68	2.39	1.77	2.1	2.29

Table 3.2 Impact of Word-width on SNDR

Word Width (bits)	8	9	10	11	12
$Mean_{SNDR}$ (dB)	39.73	42.98	57.47	57.47	57.45
σ_{SNDR} (dB)	17.82	18.7	2.88	2.94	2.9

as single-run simulations and stability analyses by the FPGA implementation of the digital parts.

Firstly, a single-run simulation is utilized to examine both the convergence of the VDLs during calibration and the power spectrum density (PSD) of the digital output with single- and 6-tone sine-wave inputs before and after calibration. For the case of the single-tone sine-wave with its associated bin's index $I_{bin} = 781$, Figs. 3.6 and 3.7 show the PSD of d_{out} in the presence of timing skew mismatches when applying the proposed calibration technique and when it is not applied, respectively. Our calibration method removes almost all harmonics. This technique increases the SNDR from 37.44 dB to more than 56.64 dB. Moreover, Figs. 3.8 and 3.9 depict the convergence of the VDLs and the SNDR during calibration. As seen, this calibration method converges before 1×10^5 samples.

For the case of the 6-tone sine-wave input with its associated bins' indexes of $I_{bin} = \{67, 243, 419, 596, 772, 949\}$, Figs. 3.10 and 3.11 depict the power spectral density (PSD) of d_{out} in the presence of timing skew mismatches before and after calibration, respectively. These figures show that almost all harmonics are significantly attenuated after calibration. Moreover, Fig. 3.12 shows the convergence of the VDLs during calibration.

Additionally, a stability analysis was performed using Monte Carlo simulations to depict this method's capability to operate with different input frequencies. The results of 500 separate simulations are gathered for this step of verification. In each run, the bin number, I_{bin} , is a randomly generated prime number from the interval $\{1, \dots, N_{fft}/2\}$. Moreover, the timing skew of the sub-ADCs is generated independently and randomly in each one. Again, the digital parts are implemented on the FPGA using the abovementioned method. Figs. 3.13, 3.14, and 3.15 illustrate the result of stability analysis before calibration, after calibration, and the improvement by calibration, respectively. The presented calibration technique increases the mean of the simulated SNDRs from 20.7 dB to 49.06 dB, as depicted in these figures. After

Table 3.3 Power Consumption and Hardware Cost with $L = 20$

Word-Width (bits)	8	9	10	11	12
Lookup Tables (%)	2.2	2.83	3.16	1.10	1.22
Flip Flops (%)	0.30	0.32	0.34	0.18	0.18
DSP Slices (%)	0.11	0.22	0.22	4.67	4.67
Signal Power (mW)	13	20	29	20	23
Logic Power (mW)	15	22	29	16	18
DSP Power (mW)	1	2	2	30	30
Total Power (mW)	29	44	60	66	71

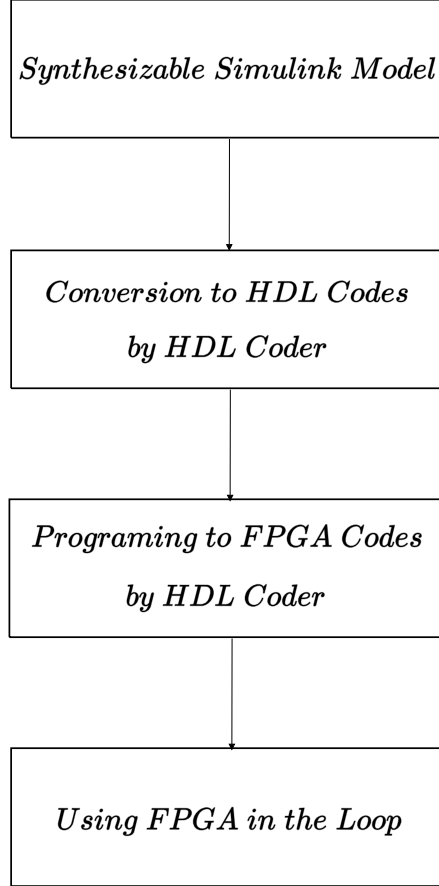


Figure 3.5 Implementation diagram on the FPGA.

using our proposed method, 64.4 % of the SNDRs are above the SNDR mean after calibration (i.e., 49.06 dB) and just 3.4 % of the SNDRs are less than the SNDR mean before calibration (i.e., 20.7 dB). As mentioned and reported in [56], all the estimation mechanisms that use the correlation approach (e.g., [17, 30]), including our proposed method fail to converge with some specific frequencies. This failure rate is not specific to our proposed method.

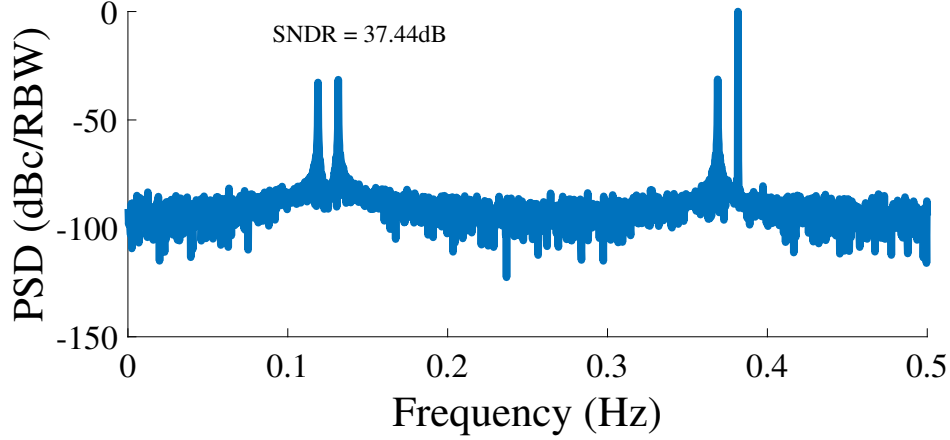


Figure 3.6 Output PSD before calibration corresponds to a single-tone sine wave when the TI-ADC, modeled in Simulink, is subject to timing skews with a standard deviation of 0.1 (10 % of the sampling interval).

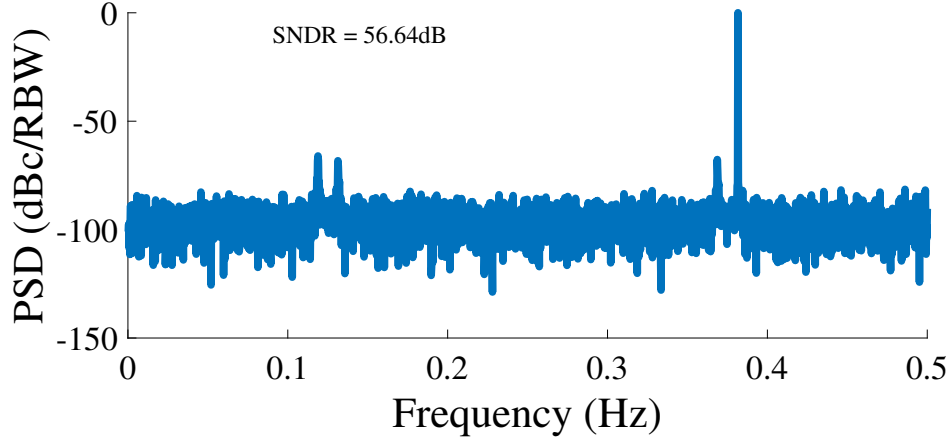


Figure 3.7 Output PSD after calibration corresponding to a single-tone sine-wave when the TI-ADC, modeled in Simulink, is subject to timing skews with a standard deviation of 0.1 (10 % of the sampling interval) and the proposed method is implemented on the FPGA.

At this point, the method's performance is evaluated in terms of the length L and Δ . For this evaluation, all the parameters and variables remain the same apart from the length L and Δ . For each value of the length L and Δ , the SNDRs before and after calibration of the TI-ADC, converting a single-tone input signal with an identical set of the bin numbers, I_{bin} , in the range $\{1, \dots, N_{fft}/2\}$, are collected. Also, the success rate is defined as the percentage of SNDRs greater after calibration than their counterpart before calibration. Fig. 3.16 depicts the simulation results of the success rate. As the figure shows, the success rate significantly improves as the length L increases to 20 and remains almost the same beyond 20. Since the hardware cost and power consumption for a length of 20 are much less than those of 30, the

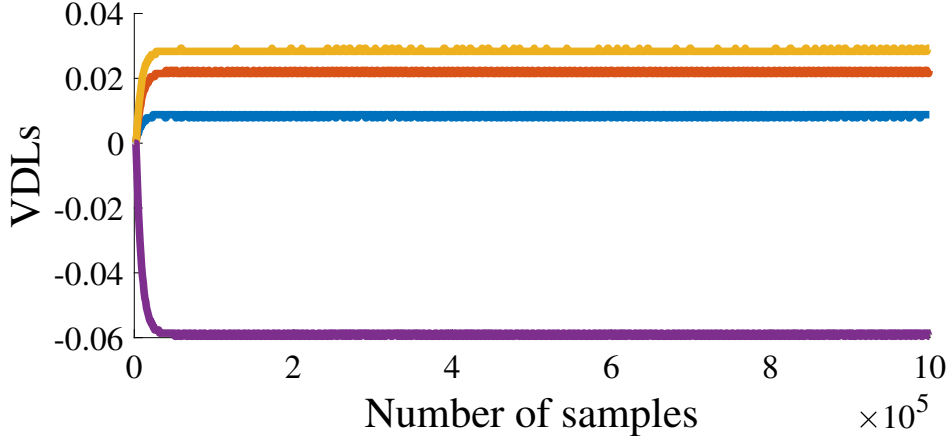


Figure 3.8 Convergence of VDLs corresponding to a single-tone input signal.

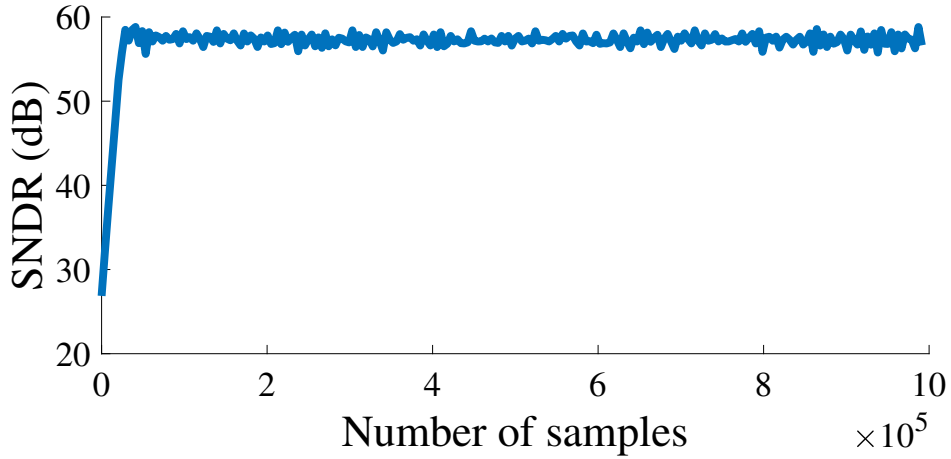


Figure 3.9 Convergence of SNDR corresponding to a single-tone sine-wave.

simulations used a length of 20.

3.5 Discussion and Comparison

As mentioned earlier, the proposed estimation concept is established based on time shift generation to desensitize the estimation to the auto-correlation of the input signal. A polyphase FIR filter generates the required time shifts. The main advantage of the estimation technique presented in this paper is that it provides a degree of freedom to select the time shifts, $\pm\Delta$, according to the application's requirements. This makes our approach highly insensitive to the cross-correlation function, unlike previous methods reported in [16, 17, 30], at the cost of using an FIR filter to generate the time shifts. The proposed method does not impose any restriction on the number of channels, and it operates with single-tone sine-wave, multi-

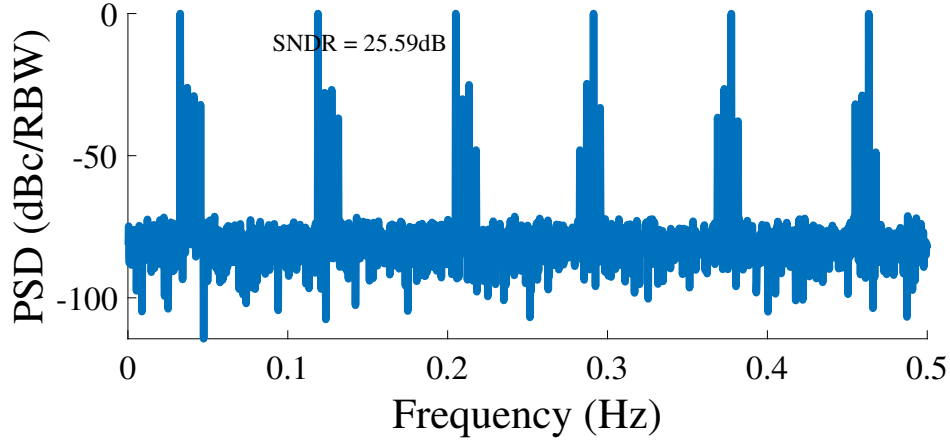


Figure 3.10 Output PSD before calibration corresponding to a 6-tone input signal when the TI-ADC, modeled in Simulink, is subject to timing skews with a standard deviation of 0.1 (10 % of the sampling interval).

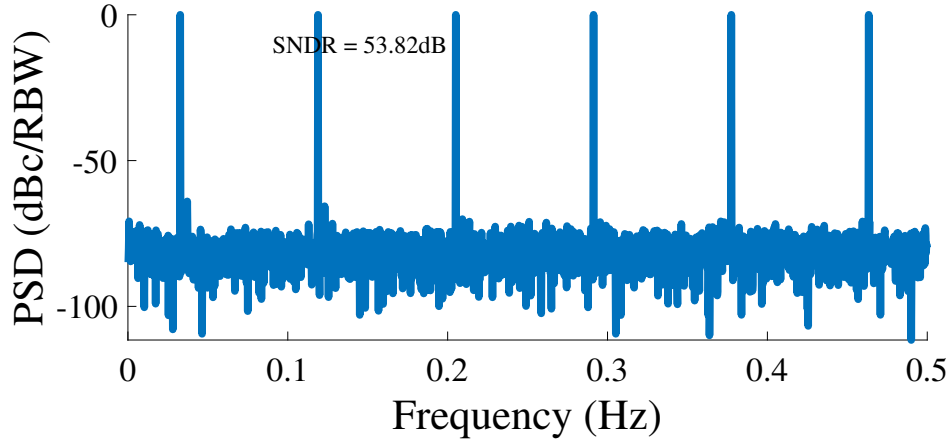


Figure 3.11 Output PSD after calibration corresponding to a 6-tone input signal when the TI-ADC, modeled in Simulink, is subject to timing skews with a standard deviation of 0.1 (10 % of the sampling interval) and the proposed method is implemented on the FPGA.

tone sine-wave, and band-limited input signals during normal operation of TI-ADC similar to [1, 10, 16, 17, 20, 30]. The merged FIR filter can be disabled to reduce power consumption, as mentioned in Section 3.5-E.

Moreover, our estimation approach is fully digital, so it does not need to modify the analog circuits and eliminates the need for any extra sub-ADC(s), unlike [10]. The widely used multi-rate approach has been utilized for decades to improve the speed of operation in various fields [47]. Notably, the polyphase mechanism has also been used to realize *derivative operation* and *Hilbert transform* for compensation of timing-skew mismatch [8, 46]. Nevertheless, our

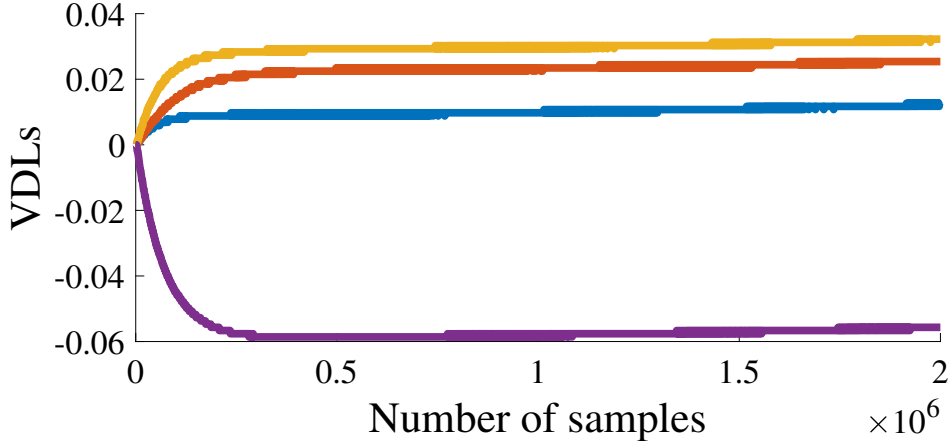


Figure 3.12 Convergence of VDLs corresponding to a 6-tone input signal.

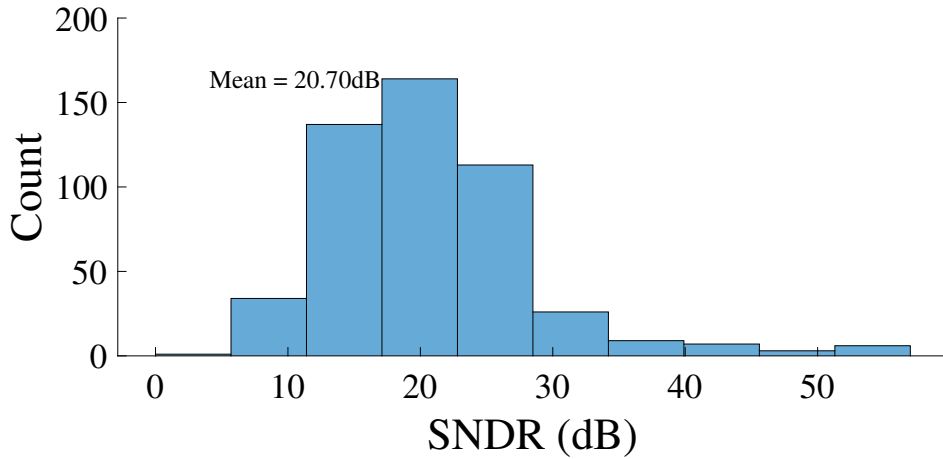


Figure 3.13 Monte Carlo simulations of the SNDR before calibration.

paper uses the polyphase mechanism to implement the FIR filter, which generates the *time-shift operation*. An important advantage of the method proposed in the present paper over our previously published method [41] is that it requires only one merged FIR filter instead of two FIR filters for all values of Δ . The reported technique in [41] needs two FIR filters except for the case $\Delta = T_s$.

More importantly, this paper implemented the proposed method with fixed-point precision in Simulink and then programmed it on the FPGA to evaluate and verify the proposed method in a realistic environment with various word widths, unlike our previous paper [41]. Although this paper has exploited timing skew correction ahead of the sub-ADCs (i.e., VDLs in the analog domain), our technique can integrate and operate with digital correction mechanisms based on derivative FIR filters (e.g., the reported correction mechanism in [46]). Our all-

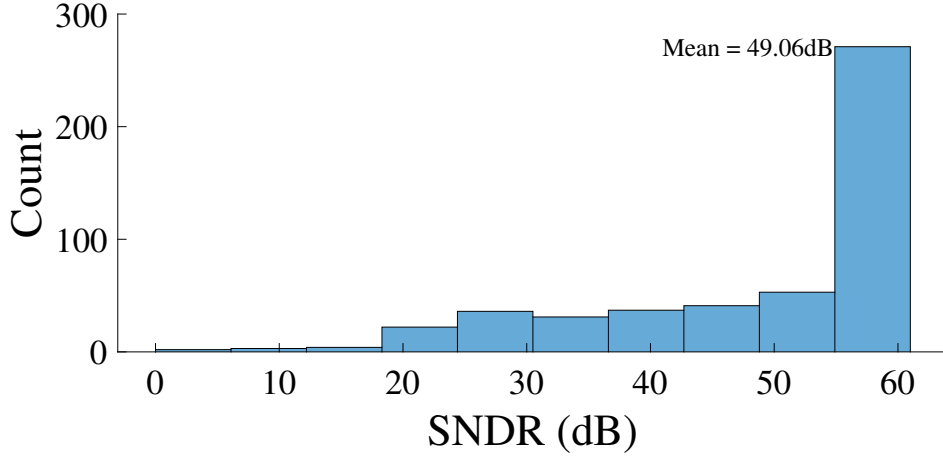


Figure 3.14 Monte Carlo simulations of the SNDR after calibration.

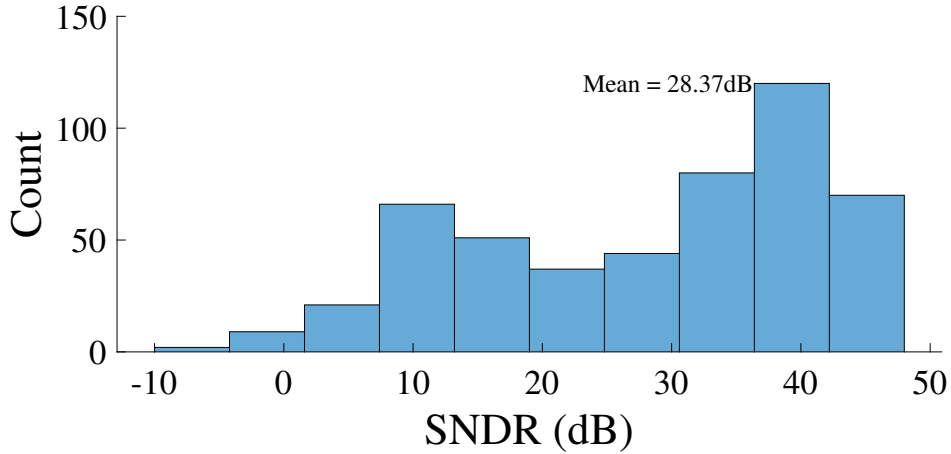


Figure 3.15 Monte Carlo simulations of the SNDR improvement by calibration.

digital estimation method is a reasonable option in case the input signal's auto-correlation has a discontinuity or zero value (e.g., at T_s). Since the proposed estimation method is fully digital and independent of any analog circuits and the design of TI-ADC, our simulation results and the FPGA implementation are considered reliable. As shown in Figs. 3.14 and 3.15, the SNDR obtained with the proposed method degrades after calibration. These results show the sensitivity of the proposed method to special frequencies similar to the methods reported in [17,30]. This sensitivity is investigated in [56]. All the estimation mechanisms that use the correlation approach (e.g., [17,30]), including our proposed method, fail to converge with some specific frequencies. This failure rate is not specific to our proposed method. As mentioned earlier, the techniques presented in [1,10,19] do not exhibit restriction over input frequencies; nonetheless, this benefit comes at the cost of extra sub-ADC(s). These points

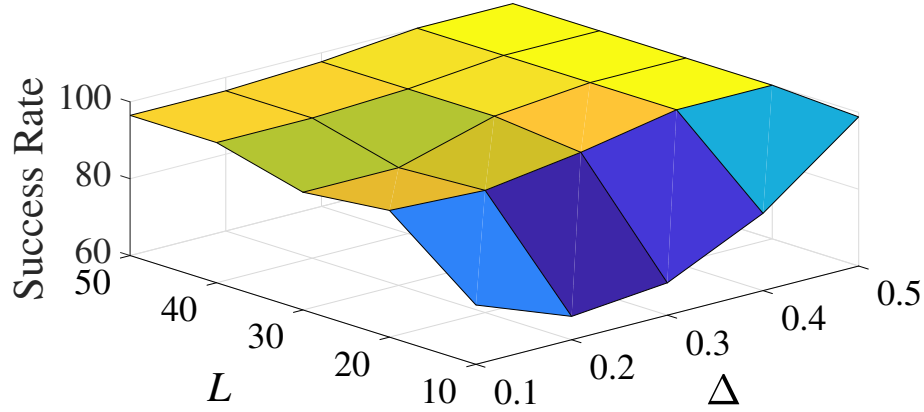


Figure 3.16 Mean of SNDRs as a function of the length L and Δ .

are highlighted in Table 4.4.

3.5.1 Merged FIR Filter

The merged FIR filter is then realized by the renowned polyphase approach [39, 46]. The FIR filter (and its polyphase realization) in previous competitive techniques generally realizes derivative operation or filtering (i.e., high-pass low-pass filtering) [5–8, 46]. In the proposed method, the functionality of the merged FIR filter (and its polyphase realization) is notable as this FIR filter realizes *time-shift operation* in contrast to [5–8, 46].

Although this method needs a polyphase FIR filter, the number of taps of this filter set could be minimized to even two; in this degenerate case, the polyphase version of the presented method simplifies the mechanism reported in [17] (and its improved variants [29, 30]). From the basics of digital signal processing, FIR filters with more taps manifest time shifts with higher precision, and their performance drops slower as the input frequency approaches the Nyquist frequency. Increasing the number of taps can reduce the sensitivity of the FIR filters to input frequencies. Accordingly, the performance of the proposed method depends on the input frequency and highly depends on the polyphase FIR filter length. The number of taps in the polyphase FIR filter should be optimized based on the specific application requirements and the input signal characteristics.

3.5.2 PVT Variations

In well-designed TI-ADCs, PVT appears as thermal noise and offset, gain, and timing-skew mismatches. Notably, offset, gain, and timing-skew mismatches vary over time, calling for background calibration mechanisms. This paper models only the impact of PVT leading to sampling time skews, neglecting the other impacts (i.e., offset and gain mismatches) to focus on compensation for the timing-skew mismatches. It is important to note that the gain and offset mismatch are introduced by inherent random internal mismatches among sub-ADCs, unlike the timing skew raised by clocking circuits and paths. Consequently, offset and gain mismatches are treated independently of the timing skew mismatch and must be calibrated before using timing skew compensating mechanisms [28, 48, 49]. Additionally, as mentioned earlier, the method presented in this paper is vulnerable to offset and gain mismatches among the sub-ADCs, similar to most of the previously reported calibration methods; nonetheless, these terms can be calibrated before utilizing the timing skew mismatch calibration method like in [20, 28, 48, 49].

3.5.3 Hardware Implementation

This paper aims to verify and evaluate the proposed method's performance with various word widths and its hardware and power consumption with these widths. Since it is instrumental for fast prototyping to demonstrate the proposed method's potential on an FPGA, this paper realized the proposed method with fixed-point precision in Simulink, and converted the Simulink model to its equivalent HDL codes, programmed the FPGA by the codes to evaluate and verify the proposed method in a realistic environment with various word widths. It is worth mentioning that the proposed method fails to operate when the word width is less than 8 bits, and the SNDR improvement by the proposed method remains almost the same beyond 10 bits. This paper showed that the best word-width is 10 bits for the target 10-bit TI-ADC resolution.

3.5.4 Operating Speed

The rate at which the hardware engine of the proposed estimation technique operates can be as high as with any other competing technique. Although the TI-ADC's sampling rate was set to 1 Hz in our Simulink models for simplicity, the operating rate of the hardware implementation depends on the CMOS technology being used. Based on the timing report of the Xilinx Vivado Design Suite [55], the proposed estimation technique can operate at a maximum frequency of 73 MHz when the Xilinx Virtex-7 VX690T FPGA implemented with 28 nm CMOS technology is used. It is important to note that FPGA realization by the HDL

codes obtained with the fixed-point Simulink model does not represent the actual operation of the proposed technique. For high-speed targets, the polyphase FIR filter must use a transposed structure that limits its maximum operating speed to the chain of a multiplier (with a constant coefficient), an adder, and a delay. However, the estimation block consisting of multipliers (with two variable inputs) appears to be the main limiting factor in the maximum operation rate. The maximum operating speed depends on the word width and the specific target technology. For this reason, the proposed method would operate much faster if our estimation engine was embedded in a modern ASIC implemented in a state-of-the-art technology (such as the TSMC 3 nm FinFET process) [57].

3.5.5 Power Consumption

It is worth mentioning that the polyphase implementation does not augment the dynamic power dissipation when compared with its single-rate counterpart, since the polyphase FIR filter operates at the $1/M$ th rate of the single-rate FIR filter. However, the polyphase FIR filter consumes M times more hardware and implementation area. Also, static power consumption increases with M . An efficient power optimization mechanism would reduce power dissipation by using both single-rate and polyphase approaches over a time-usage percentage, TP . In the polyphase approach, only one FIR filter could be employed at any time to reduce power consumption by a factor of M . Moreover, most digital calibration methods lose their *true background operation* advantage over their foreground counterparts in ultra-high-speed applications. However, the *pseudo-background* calibration approach remains attractive for benefiting from *interruption avoidance* of normal conversion operation. In this regard, the pseudo-background mechanism can periodically process the gathered data of the digital output to estimate the timing skew on FPGAs or even on a personal computer (PC) and then enter an *inactive mode* for collecting the next set of data. Consequently, power consumption can drop significantly; nevertheless, the "*operation speed challenge*" only remains for the data collection as in [10, 12, 58]. The main concern relating to the presented method is the power and implementation hardware expense. These points are highlighted in Table 3.5. In this table, each case's power and hardware requirements are normalized to those of the single-rate implementation.

3.6 Conclusions

In this paper, the use of time shift generation realized by an FIR filter realized by the multirate approach for fully digital background estimation of timing skew mismatches in TI-ADCs has been presented. For the first time, the novel concept of time shifts have been

Table 3.4 Performance summary and comparison of the proposed calibration approach

	Resolution (bits)	SNDR (dB)	Number of channels	Convergence $\times 10^3$ (Number of samples)	Extra sub-ADC(s) requirement	Digital hardware complexity	Sensitivity to auto-correlation
This work	10	56.6	4	100	no	filter & multiplier	no
[1]	5	25.1	8	500	yes	adders	yes
[10]	6	35	16	-	yes	adders	yes
[17]	10	52.9	2	56	no	multiplier	yes
[28]	10	54.2	8	80	yes	milter & multiplier	yes
[29]	12	68.6	4	800	no	multiplier	yes
[16]	8	44.4	4	160	no	adders	yes
[19]	13	60.3	8	840	yes	adders	yes

Table 3.5 Power Consumption and Hardware Optimization

Implementation	Normalized power Consummation	Normalized Hardware Requirement
Single-Rate	1	1
Periodic Usage (TP %) of Single-Rate	$TP/100$	1
Multi-Rate	1	M
Periodic Usage (TP %) of Multi-Rate	$TP/100$	M
Sequential Usage of FIR Filters in the Bank	$1/M$	M

used to estimate the cross-correlation at various points to desensitize the estimation to auto-correlation distribution of the input signal. Therefore, our all-digital estimation approach is a reasonable choice when the auto-correlation of the input signal has zero value or discontinuity. Comparisons of the output cross-correlation of the sub-ADCs have been used to extract the timing skew mismatch. The proposed estimation method's main cost is the requirement of a polyphase FIR filter for the time shift generation. Our proposed estimation technique is all-digital, so it does not require any modification of analog circuits and/or extra sub-ADC(s). Our technique's functionality and performance have been verified via extensive simulations. The proposed calibration method enhances the SNDR from 37.44 dB to more than 56.64 dB in one of the best cases with single-tone sine wave input.

Acknowledgments

The authors thank the Ciena Corporation and the Mathematics of Information Technology and Complex Systems (MITACS) granting agency for their financial support.

CHAPTER 4 ARTICLE 2 : DIGITAL COMPENSATION OF TIMING SKEW MISMATCHES IN TIME-INTERLEAVED ADCS BY SOURCE SEPARATION

The proposed method, in this chapter, entitled "*Digital Compensation of Timing Skew Mismatches in Time-Interleaved ADCs by Source Separation*" has been published in *IEEE Transactions on Instrumentation and Measurement*. This method's main contribution is the source separation algorithm, which removes the errors arising from the timing-skew mismatch in the TI-ADC's digital output. The Hilbert transform, together with down-sampling and up-sampling, is used for the required second input. The proposed technique performs compensation without additional SADC(s) or manipulating the TI-ADC structure. It can also operate in almost all the Nyquist range. The proposed technique avoids introducing any delay.

Digital Compensation of Timing Skew Mismatches in Time-Interleaved ADCs by Source Separation

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4.1 Abstract

This paper proposes an adaptive all-digital background compensation of timing skew mismatches in time-interleaved analog-to-digital converters (TI-ADCs). The proposed approach uses the orthogonality between the desired component representing ideal samples of the TI-ADC input signal and the timing skew mismatch errors. Our technique is the first attempt to use a source separation mechanism to recover the desired component in the digital output of TI-ADC. A finite impulse response (FIR) filter implementing the Hilbert transform and two separate adaptive FIR (A-FIR) filters are exploited to implement this recovery process. The proposed technique works at frequencies close to the full admissible Nyquist frequency range, and its operation does not depend on the number of sub-ADCs (SADCs). This method operates without any extra SADC. The main cost introduced by the proposed compensation technique is the requirement of two adjustable FIR filters. This cost is pro-

portional to the number of taps in these FIR filters that can be optimized according to the specific application. This technique is validated through various behavioral simulations and a field-programmable-gate-array (FPGA) implementation. With the proposed method, the signal-to-noise and distortion ratio (SNDR) is enhanced from 23.06 dB to more than 66.82 dB in a 12-bit TI-ADC when the standard deviation of timing skew mismatches is 10% of the TI-ADC's sampling interval.

4.2 Introduction

This paper proposes an adaptive all-digital mechanism for separating the desired component representing ideal samples of the input signal from the error element caused by the timing skew mismatch. In the proposed approach, an error component reflecting the errors due to timing skew mismatches that are orthogonal to the ideal samples of the input signal, along with the Hilbert transform, is exploited to compensate for these mismatches. Our method is the first attempt to use a source separation mechanism to recover the desired component in the digital output of TI-ADCs. It is of interest, however, that the concept of source separation was previously applied in transceivers to compensate for in-phase/quadrature-phase (I/Q) imbalances [59–62].

In the present paper, a symmetric source separation scheme with feedback realization is utilized [63]. The method proposed in the present paper is fully implementable in the digital domain, and consequently, any modification of the TI-ADC architecture and addition of extra SADC(s) is unnecessary in contrast to [22, 27, 28]. Unlike [25, 45, 64], our approach does not need any bank of FIR filters. Instead, two adaptive FIR (A-FIR) filters and a Hilbert transform (which is also implemented via an FIR filter) are utilized. This technique tunes the coefficients of the two A-FIR filters for the proposed compensation process. The proposed approach allows to use almost the entire Nyquist frequency range of the TI-ADC, in contrast to [5, 6], and it operates independently of the number of SADCs, as opposed to [4, 6, 7, 25]. This background compensation mechanism operates during regular data conversion operations of the TI-ADC.

The paper is structured as follows. Section 4.3 presents the proposed technique. Section 4.4 provides simulation results and related discussions. Section 4.5 compares the proposed method with the present techniques. Section 4.6 concludes the paper.

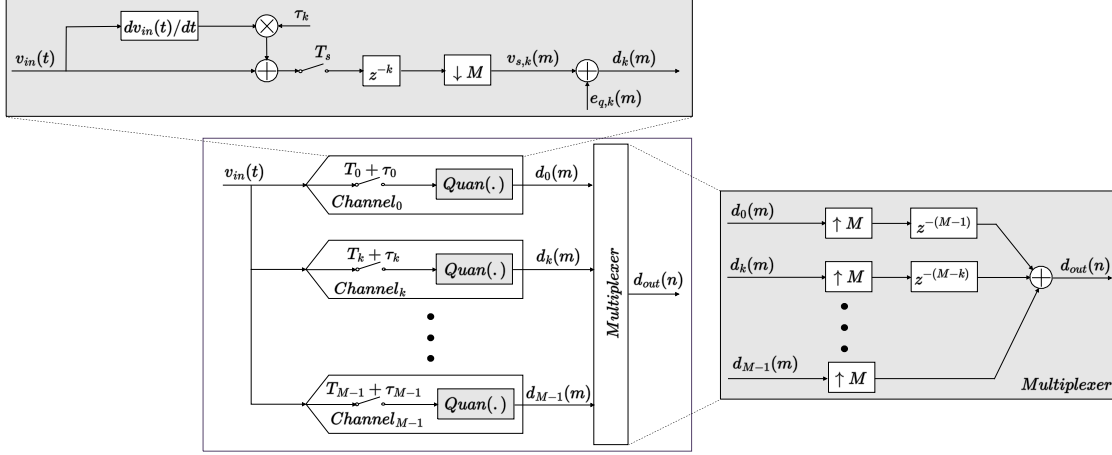


Figure 4.1 Architecture of a typical time-interleaved ADC (TI-ADC).

4.3 Proposed Source Separation-Based Method

This section presents the impact of timing skew mismatch on the performance of TI-ADCs. Subsequently, the theoretical background and implementation of the proposed recovery approach are provided. As depicted in Fig. 4.1, multiple SADCs comprise a TI-ADC. These SADCs are nominally identical ADCs with the same effective resolution, B , and the same sampling rate of F_s/M , where F_s is the overall sampling rate of the TI-ADC. The TI-ADC achieves this sampling rate by the pattern of the shifted sampling edges as kT_s in k th SADC for $k = 0, \dots, M-1$, where T_s denotes the sampling time of the TI-ADC, identical to $1/F_s$ [65, 66]. The input signal, v_{in} , is sampled at intervals of T_s seconds. Then, the TI-ADC multiplexes the outputs of the SADCs to create its own digital output, d_{out} [41].

As mentioned above, SADCs exhibit inherent *offset*, *gain*, and *sampling time skew* mismatches due to random PVT variations. Since these mismatches seriously degrade the effective resolution of the TI-ADC, mechanisms to enhance the resolution by estimating and correcting these mismatches are required. Similar to previous methods, the proposed technique also focuses on timing skew mismatch and assumes that the offset and gain mismatches have already been compensated by separate other means.

In the following, the effect of skew mismatch is presented. As seen from Fig. 4.1, the sampled input signal in the k th SADC is represented as follows

$$v_{s,k}(m) = v_{in}(m \times MT_s - kT_s + \tau_k), \quad (4.1)$$

where $k = 0, \dots, M-1$, and also, m and τ_k denote the discrete-time index (corresponding to

the rate of F_s/M) and k th skew in the sampling time [18,41,67]. It is obvious from the Taylor series approximation that [8,22,68], the k th sampled input signal can be roughly expressed as

$$v_{s,k}(m) \approx v_{in}(mMT_s - kT_s) + \tau_k \frac{dv_{in}(mMT_s - kT_s)}{dt} \quad (4.2)$$

where $k = 0, \dots, M-1$. Ideally, the outputs of the SADCs, d_k , are the sum of their inputs and injected error terms resulting from the quantization process. In the following, the quantization error is neglected in order to concentrate on the proposed method.

For the following frequency domain presentation, capital letters are utilized to represent their respective time-domain signals. In the frequency domain, the k th digital output is expressed as

$$D_k(e^{j\omega}) = \frac{1}{M} \sum_{i=0}^{M-1} e^{-jk(\frac{\omega}{M} - \frac{2\pi i}{M})} V_{in}(e^{j(\frac{\omega}{M} - \frac{2\pi i}{M})}) \times (1 + j\tau_k(\frac{\omega}{M} - \frac{2\pi i}{M})) \quad (4.3)$$

where $k = 0, \dots, M-1$. The above expression shows that the output D_k consists of the input signal and its derivative and their respective $M-1$ images. Figs. 4.2(a) and 4.2(b) show the power spectrum density (PSD) of the k th digital output without and with sampling time skew, respectively. As seen, the derivative and its images are orthogonal to the input signal and its images. The digital output of the TI-ADC is obtained by multiplexing the outputs of the SADCs. In the frequency domain, this operation is represented by up-sampling of the outputs of the SADCs by M and then applying the delays of $M-k$ (equivalently $= e^{-j(M-k)\omega}$ in the frequency domain) as

$$D_{us,k}(e^{j\omega}) = \frac{e^{-j(M-k)\omega}}{M} \sum_{i=0}^{M-1} e^{-jk(\omega - \frac{2\pi i}{M})} V_{in}(e^{j(\omega - \frac{2\pi i}{M})}) \times (1 + j\tau_k(\omega - \frac{2\pi i}{M})) \quad (4.4)$$

where $k = 0, \dots, M-1$. The digital output of the TI-ADC is the sum of all the signals $D_{us,k}$ for $k = 0, \dots, M-1$. In the frequency domain, the digital output is thus represented as

$$D_{out}(e^{j\omega}) = D_{ds}(e^{j\omega}) + E_{ts}(e^{j\omega}) \quad (4.5)$$

where D_{ds} and E_{ts} denote the desired component (i.e., the ideal samples of the input signal) and the error element resulting from the timing skew mismatches, respectively. D_{ds} and E_{ts}

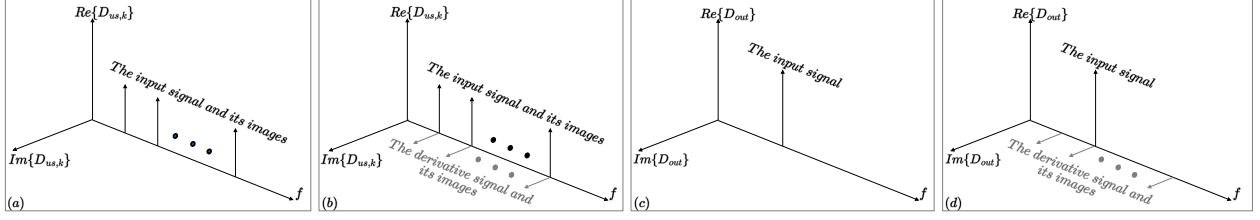


Figure 4.2 PSDs of the digital output of SADCs after being up-sampled and TI-ADC. (a): up-sampled k th output without timing skew, (b): up-sampled k th output with timing skew, (c): the ideal element of the digital output of the TI-ADC, (d): the digital output of the TI-ADC in the presence of timing skews.

can be expressed as follows

$$\begin{aligned}
 D_{ds}(e^{j\omega}) &= \frac{e^{-jM\omega}}{M} \sum_{i=0}^{M-1} \left\{ \sum_{k=0}^{M-1} e^{-jk\frac{2\pi i}{M}} \right\} V_{in}(e^{j(\omega - \frac{2\pi i}{M})}), \\
 E_{ts}(e^{j\omega}) &= \frac{e^{-jM\omega}}{M} \sum_{i=0}^{M-1} E_{ts,i}(e^{j\omega}) V_{in}(e^{j(\omega - \frac{2\pi i}{M})}) \\
 &\quad j(\omega - \frac{2\pi i}{M})
 \end{aligned} \tag{4.6}$$

where $E_{ts,i}$ also stands for the error resulting from the i^{th} image of the input signal as

$$E_{ts,i}(e^{j\omega}) = \sum_{k=0}^{M-1} \tau_k e^{-jk\frac{2\pi i}{M}} \tag{4.7}$$

where $i = 0, \dots, M-1$. It can also be shown [39] that

$$\sum_{k=0}^{M-1} e^{-jk\frac{2\pi i}{M}} = \frac{1 - e^{-jk\frac{2\pi i}{M}}}{1 - e^{-jk\frac{2\pi i}{M}}} = \begin{cases} M, & i = 0, \\ 0, & i \neq 0. \end{cases} \tag{4.8}$$

Accordingly, the desired component in the digital output of the TI-ADC is given by

$$D_{ds}(e^{j\omega}) = e^{-jM\omega} V_{in}(e^{j\omega}). \tag{4.9}$$

In the above equation, all the images except for the input signal itself vanished. However, the same is not *valid for the images*, $E_{ts,i}$ since the timing skews are randomly distributed and they differ from each other. It should be noted that the term $e^{-jM\omega}$ in (4.9) translates into the delay of M in the digital output. Figs. 4.2(c) and 4.2(d) respectively depict the digital output without and with the timing skew mismatch. Ideally, the digital output consists of only the component D_{ds} and the timing skew mismatch injects the images $E_{ts,i}$ to the digital

output. The proposed separation aims to recover the desired element D_{ds} from D_{out} .

4.3.1 Proposed Separation Method for TI-ADCs

In this paper, a symmetric source separation scheme with feedback realization is utilized [63]. The main requirement in adapting this mechanism for timing skew mismatch compensation is the orthogonality between the components d_{ds} and e_{ts} . Also, the source separation algorithm requires two different combinations of the components d_{ds} and e_{ts} as its two inputs [60, 63]. In case, these requirements are satisfied, the source separation algorithm can classify the components d_{ds} and e_{ts} by a decorrelation mechanism and route these two components to its two outputs. In the following, the orthogonality between the elements d_{ds} and e_{ts} is first shown, and then, the approach for adapting the source separation algorithm is proposed.

As stated earlier, it is shown that the input signal, sampled in the presence of the sampling time skew of τ can be represented as follows

$$v_s(n) = v_{in}(nT_s) + \tau \times \frac{dv_{in}(nT_s)}{dt}. \quad (4.10)$$

In the frequency domain, the derivative term translates to $j\omega\tau V_{in}(\omega)$ denoting the orthogonality between the input signal and its derivative. In addition, the correlation of a band-limited wide-sense-stationary (WSS) random input signal and its derivative over the period of T is given by

$$r_{v_{in}, dv_{in}/dt} = \lim_{T \rightarrow \infty} \frac{1}{T} \int_{-T/2}^{+T/2} v_{in}(t) \frac{dv_{in}}{dt} dt \quad (4.11)$$

which is asymptotically equal to zero if the input signal is bounded in amplitude [17]. This equation proves the orthogonality between the components d_{ds} and e_{ts} as the first requirement of the source separation method. However, the only available combination of the elements d_{ds} and e_{ts} is the TI-ADC digital output. For this reason, the proposed method creates a second combination so as to recover the desired component, d_{ds} , by the source separation algorithm.

The proposed method creates the required second combination from the TI-ADC digital output by a Hilbert transform followed by up-sampling and down-sampling. The proposed method utilizes a Hilbert transform to generate the orthogonal version as the required second input. The Hilbert transform has the form of a finite impulse response (FIR) filter that can be expressed as follows

$$h_{hil}(n) = \begin{cases} \frac{2}{\pi} \frac{\sin^2(\pi n/2)}{n}, & n \neq 0, \\ 0, & n = 0, \end{cases} \quad (4.12)$$

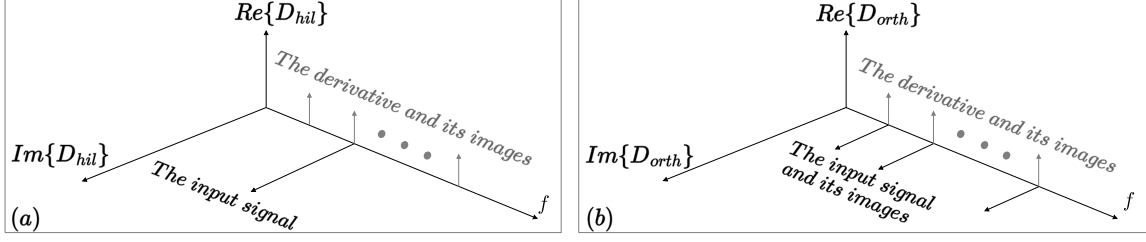


Figure 4.3 The PSDs of the Hilbert transform before and after down-sampling and up-sampling by M .

for $-DHT \leq n \leq DHT$ where n and DHT respectively denote the discrete-time index (corresponding to the rate of F_s) and the delay introduced by Hilbert transform. As shown in Fig. 4.3(a), the components e_{ts} and d_{ds} respectively appear as the real and imaginary parts of the signal d_{hil} . Since the error element in d_{out} consists of the main derivative of the input signal and its $M - 1$ images, the second combination must also comprise the orthogonal $M - 1$ images in addition to the imaginary version of the input signal. In turn, a mechanism needs to be considered to create the required image from the output of the Hilbert transform. From discrete-time signal processing basics, the down-sampling operation creates M images of the input signal as

$$D_{hil,d}(e^{j\omega}) = \sum_{i=0}^{M-1} D_{out}(e^{(\omega/M - 2\pi i/M)}). \quad (4.13)$$

Up-sampling of (4.13) by the factor M results in

$$D_{orth}(e^{j\omega}) = D_{hil,d}(e^{jM\omega}). \quad (4.14)$$

By substituting (4.13) into (4.14), the output signal after up-sampling is given by

$$D_{orth}(e^{j\omega}) = \sum_{i=0}^{M-1} D_{hil}(e^{(\omega - 2\pi i/M)}). \quad (4.15)$$

As seen from the above equation, down-sampling followed by up-sampling results in the creation of the required $M - 1$ images from the output of the Hilbert transform. As shown in Fig. 4.3(b), the second combination, d_{orth} , consists of the real version of the element e_{ts} and the input signal's orthogonal version with its images. The source separation algorithm can now operate on the signals d_{out} and d_{orth} as its inputs. Then, this algorithm, after convergence, makes its two outputs orthogonal as

$$E(d_{rcv} \times d_{err}) = 0 \quad (4.16)$$

where d_{rcv} and d_{err} respectively denote the recovered output (conveying the desired component, d_{ds}) and the error output (carrying the error component, e_{ts}).

The adaptive source separation algorithm that can be used to recover the input signal from its images can now be presented. The structure of the source separation machine is depicted in Fig. 4.4. The source separation section consists of two A-FIR filters. The filter $A-FIR_{rcv}$ aims at purifying d_{rcv} from the error component, e_{ts} , and the filter $A-FIR_{err}$ targets removing the desired component, d_{ds} , from d_{err} as follows

$$d_{rcv}(n) = d_{out}(n) - (filt_{err} * d_{err})(n), \quad (4.17)$$

$$d_{err}(n) = d_{orth}(n) - (filt_{rcv} * d_{rcv})(n) \quad (4.18)$$

where $filt_{rcv}$ and $filt_{err}$ represent the impulse response of the filters $A-FIR_{rcv}$ and $A-FIR_{err}$, respectively. The presence (i.e., leakage) of the error component, e_{ts} , in the recovered output, d_{rcv} , and the desired component, d_{ds} , in the error output, d_{err} , are considered as the adjustment process errors of the A-FIR filters. It can be shown that, the minimization of both energy signals

$$\begin{aligned} \xi_{rcv} &= E(d_{rcv}^2), \\ \xi_{err} &= E(d_{err}^2), \end{aligned} \quad (4.19)$$

allows removing the two leakages mentioned above [63]. The separation mechanism minimizes the energy of the two outputs d_{rcv} and d_{err} separately by iteratively tuning the coefficients of the filters $A-FIR_{rcv}$ and $A-FIR_{err}$, respectively, by least-mean-squares (LMS) algorithm. The LMS mechanism exploits the derivative of the energy signals as a compass to find the direction to the minimum of the energy signals. These derivatives, which are called the update steps, are expressed as

$$\begin{aligned} \delta w_{rcv,j} &= \frac{d\xi_{rcv}}{dw_{rcv,j}}, \\ \delta w_{err,j} &= \frac{d\xi_{err}}{dw_{err,j}} \end{aligned} \quad (4.20)$$

where $j = 1, \dots, FL$. The parameter FL denotes the number of taps of these A-FIR filters. By substituting (4.18) and (4.17) into (4.20), the update-steps can be expressed by

$$\begin{aligned} \delta w_{rcv,j}(n) &= d_{rcv}(n) \times d_{err}(n - j), \\ \delta w_{err,j}(n) &= d_{err}(n) \times d_{rcv}(n - j). \end{aligned} \quad (4.21)$$

The LMS algorithm utilizes them as part of update steps to tune the coefficients at each

iteration. The update expressions in the LMS machine are expressed as

$$\begin{aligned} w_{rcv,j}(n+1) &= w_{rcv,j}(n) + \mu \times \delta w_{rcv,j}(n), \\ w_{err,j}(n+1) &= w_{err,j}(n) + \mu \times \delta w_{err,j}(n) \end{aligned} \quad (4.22)$$

where $j = 1, \dots, FL$, and also, $w_{rcv,j}$ and $w_{err,j}$ are the weights of the filters $A\text{-}FIR_{rcv}$ and $A\text{-}FIR_{err}$, respectively. In the above update expressions, the parameter μ represents the update rate which controls the stability of the two A-FIR filters [41]. The convergence of the coefficients in (4.22) shows that the update steps converge to zero, and it equivalently confirms the orthogonality between d_{rcv} and d_{err} . The value of the parameter μ must be selected properly according to the length of A-FIR filters and the required convergence rate. A suitable adjustment of μ is necessary to ensure the stability of the A-FIR filters. As μ is reduced, the stability margin increases at the cost of a reduced convergence rate of the A-FIR filters [51]. The selection of the length of A-FIR filters and Hilbert transform is a significant design decision as when the number of SADCs and/or the number of tones in the input signal increases, the lengths of filters must be expanded. Therefore, the number of taps for the A-FIR filters should be chosen according to the requirements of the specific application and the number of SADCs to limit power consumption.

4.4 Simulation Results

To begin with, parameters and values that will be used in the sequel are defined. For simplicity, in the following simulations, input tones are applied to the system that needs compensation. Indeed, the performance of the proposed compensation method depends on the number of tones and their respective frequencies. The performance of the system will be characterized by performing fast Fourier transforms (FFTs) analyses of the various signals at key points of the system. Injected input tones have respective frequencies that can be expressed as floating point values. These input tones of frequency, F_{in} , will be mapped to their corresponding index of the bin(s), I_{bin} , by the FFT analysis. The index of the bin(s), I_{bin} , has(ve) integer value(s), with no dimension, that can be expressed as $N_{fft} \times F_{in} / F_s$, where N_{fft} is the total number of indexes in the FFT. It is notable that N_{fft} needs to be selected as multiples of 2^B , with B being the desired effective resolution of the TI-ADC expressed as a number of bits, and I_{bin} must be a prime number in the range of $\{1, \dots, N_{fft}/2\}$ to avoid spectral leakage and repetitive patterns in the input-tone (i.e., to make the quantization noise spectrum uniformly distributed) [53, 54]. For instance, N_{fft} is set to 2^{B+1} ($= 2^{13}$) in the following simulations, and a prime number is used from the 563 distinct prime values in the range $\{2, \dots, 2^{12}\}$ for I_{bin} .

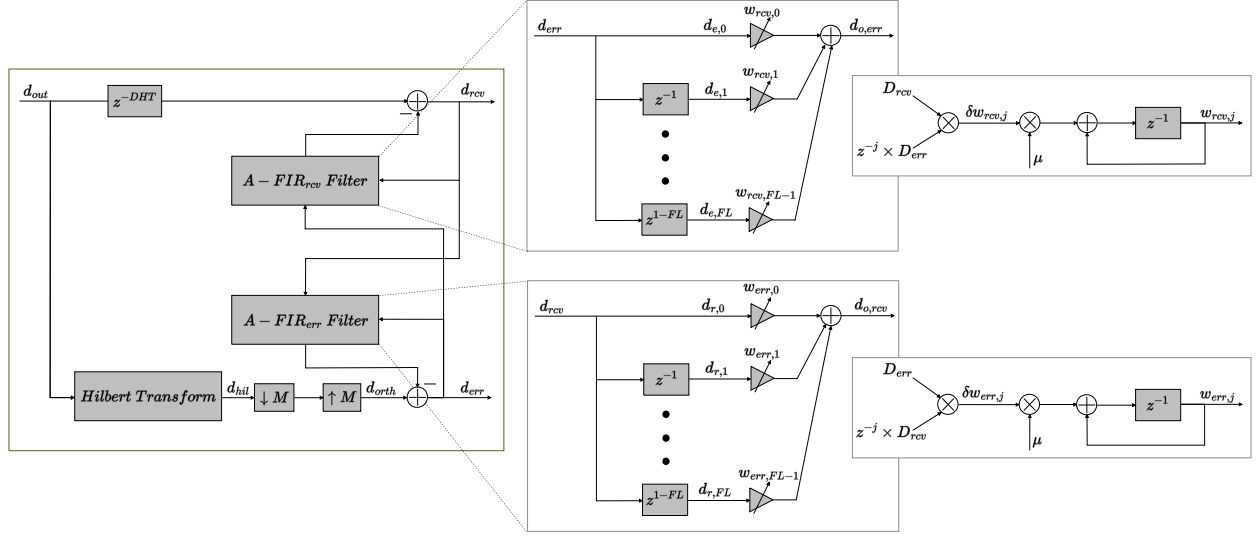


Figure 4.4 Architecture of a module implementing the symmetrical adaptive source separation method.

To validate and characterize the performance of the proposed separation and recovery scheme used for compensation, behavioral simulations were performed with MATLAB/Simulink. In these simulations, the TI-ADC modeled in Simulink comprises four identical 12-bit SADCs. In turn, the quantization errors of the SADCs restrict the effective resolution of the TI-ADC, B , to 12 bits. The sampling rate of the TI-ADC, F_s , is normalized to 1 Hz for simplicity. Moreover, the standard deviation of the timing skew mismatch is set to 0.1 (i.e., 10% of the TI-ADC's sampling clock period). The proposed method is modeled by both its fixed point Simulink model and by field-programmable-gate-array (FPGA) implementations. The fixed point Simulink model is used to evaluate the effectiveness of the proposed method for various word widths, and the FPGA implementation is used to validate the synthesizability of the fixed point Simulink model and to evaluate the hardware cost for various word widths. For proper convergence of the compensation technique, the update step factor, μ , is set to 2^{-12} . The length of the A-FIR filters, FL , and the Hilbert transform filter, DHT , are set to 30 and 60, respectively (see Section 4.5).

It is of interest that the word width with which the proposed method is implemented impacts the hardware cost, but it also impacts the effectiveness of our method (i.e., the resolution of the recovered digital output, d_{rcv}). Therefore, various input frequencies (i.e., various bin indexes, I_{bin}) are used to estimate the mean of the signal-to-noise-and-distortion ratios (SNDRs) obtained with each selected word width. In each run, a prime number in the range $\{2, \dots, 2^{12}\}$ is selected for the bin index I_{bin} . The simulations are repeated (563 times) to cover all these primes. Then, the results of all the simulation runs are gathered as a

function of the selected word width. The timing skew values remained the same in all the simulations to only evaluate the impact of the word width and various input frequencies on the performance. The mean of the obtained SNDRs (563 instances), each SNDR requiring a simulation run, are reported in Table 4.1 corresponding to different word widths. The observed standard deviations are also reported in that table. The obtained SNDR after mismatch compensation improves significantly as the word width grows from 14 to 16 bits, but it increases only a little from 16 to 17 bits and it remains almost constant beyond 17 bits. It is notable that the proposed method fails to converge for word widths smaller than 14 bits.

Additionally, the synthesizability of the proposed method's fixed-point Simulink model and the hardware cost of the proposed compensation method corresponding to each word width are evaluated on FPGA. For this part, the equivalent Verilog HDL of the behavioral Simulink model of the proposed method is generated by the Simulink HDL Coder [55]. The MATLAB FIL Wizard then synthesizes the resulting Verilog codes and the Vivado Design Suite finally programs the FPGA. To obtain the results reported below, the Xilinx Virtex-7 VX690T implemented with a 28nm FPGA CMOS technology is targeted. The data is generated by the behavioral model of the TI-ADC on Simulink and transferred to the FPGA, supporting the implementation of the proposed method, via the JTAG protocol [55]. The communication rate between the FPGA and Simulink was set to 12.5 MHz in agreement with the JTAG protocol. Notably, the VX690T series of Virtex-7 comprises 2800 digital signal processing (DSP) slices and 485 k logic cells. Table 4.2 shows the implementation results of the proposed method corresponding to various word widths. As reported, the hardware consumption grows as the word width increases. Note that, remarkably, when the word width went up from 17 to 18 bits, the number of lookup tables (LUTs) went down (from 3.41% to 2.27%) but the number of DSP modules went up (from 5% to 6.72%) which is consistent with the fact that DSP modules are optimized to handle 18-bit operands. A good choice of word width that offers a good compromise between the SNDR and the power consumption is 16 bits. Indeed, increasing the word width beyond 16 bits improves the SNDR only slightly at the cost of consuming significantly more hardware resources with a corresponding higher power consumption.

The quality of the timing skew mismatch compensation obtained with the proposed method was characterized by numerous simulations. In the following simulations, the PSD of the digital output, d_{out} , the recovered desired signal, d_{rcv} , and the error signal, d_{err} , were obtained to evaluate the effectiveness of the proposed method with

1. Single run simulations by applying a single sine wave and a 6-tone sine wave,

Table 4.1 Impact of Word Width on the SNDR

Word Width (bits)	14	15	16	17	18
$Mean_{SNDR}$ (dB)	66.8	69.5	70.7	71.02	71.1
σ_{SNDR} (dB)	5.9	6.2	6.4	6.6	6.6

Table 4.2 Hardware Cost

Word-width (bits)	14	15	16	17	18
LUTs (%)	2.33	2.56	2.83	3.41	2.27
Flip Flops (%)	0.4	0.52	0.54	0.57	0.59
DSP Slices (%)	4.83	4.89	4.89	5	6.72

2. Monte Carlo simulations with 500 simulation runs by applying a single sine with various randomly generated bin indexes.

It is notable that a Simulink model is used as the TI-ADC, and both the fixed-point Simulink model and the FPGA implementation of the proposed method are used in parallel in the first part of the following simulations. However, the FPGA implementation of the proposed method is just utilized for the second part (Monte Carlo simulations). Moreover, the FIL Wizard transfers data between the Simulink model and FPGA.

For the case of a single-tone input signal with its associated bin's index $I_{bin} = 2781$, the PSD of d_{out} , d_{rcv} , and d_{err} are respectively reported in Figs. 4.5, 4.6, and 4.7. For this case, the SNDR is enhanced from 22.57 dB to more than 71.96 dB by the proposed approach and almost all harmonics of d_{out} are obviously attenuated in d_{rcv} (for both the FPGA implementation and the Simulink model). Furthermore, the convergence of SNDR, $A-FIR_{rcv}$ and $A-FIR_{err}$ are depicted in Figs. 4.8, 4.9, and 4.10, respectively. As depicted in these figures, this method needs fewer than 1×10^5 samples to converge while remaining stable after convergence. These figures depict that the results of both the FPGA implementation and the Simulink model coincide entirely.

Additionally, for the case of the 6-tone sine wave input signal with its associated bins' indexes $I_{bin} = \{512, 1126, 1741, 2355, 2969, 3584\}$, the simulated PSD of the digital output is reported in Fig. 4.11. Also, Figs. 4.12 and 4.13 depict the PSDs of the recovered desired signal and of the error signal, respectively, after convergence for both the FPGA implementation and the Simulink model of the proposed method. As seen from these figures, the results of both the FPGA implementation and the Simulink model completely coincide, and all harmonics of d_{out} are again significantly attenuated in d_{rcv} . In addition, Figs. 4.14, 4.15, and 4.16 show the convergence of SNDR, $A-FIR_{rcv}$, and $A-FIR_{err}$, respectively. As seen from these

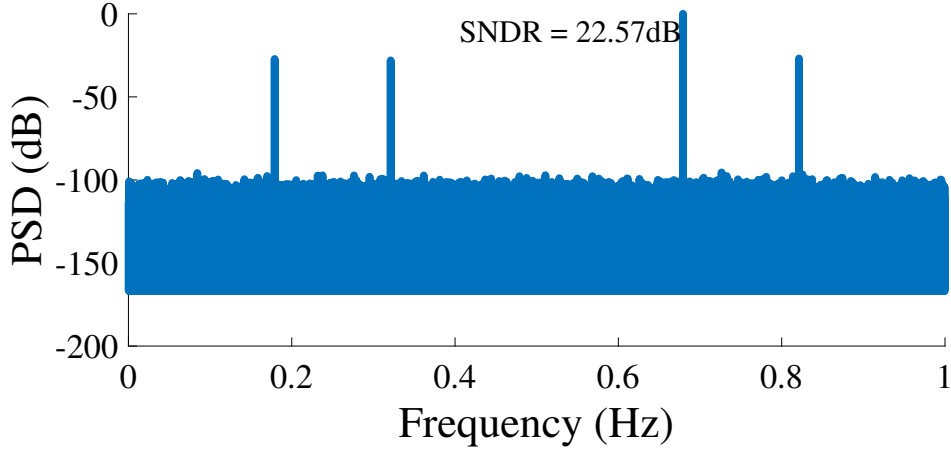


Figure 4.5 Output PSD of d_{out} corresponding to a single-tone sine wave and the TI-ADC, modeled in Simulink, with the timing skews' standard deviation of 0.1 (10% of the TI-ADC's sampling period).

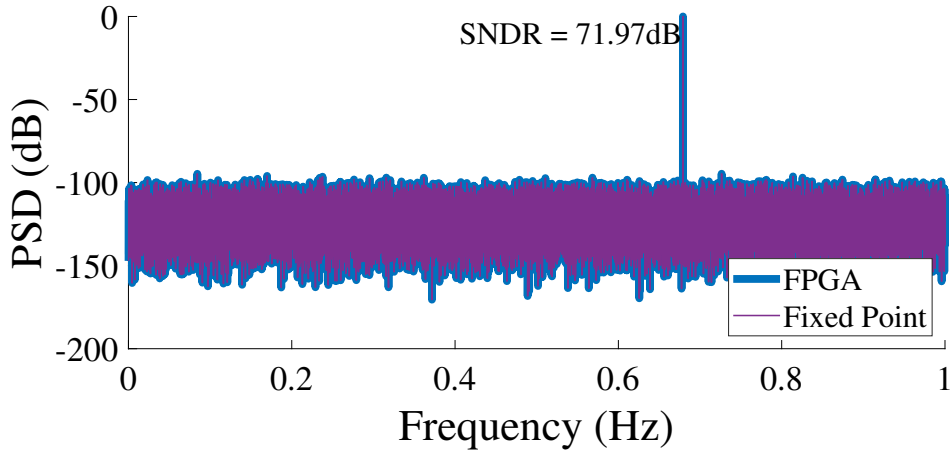


Figure 4.6 Output PSD of d_{rev} corresponding to a single-tone sine wave and the TI-ADC, modeled in Simulink, when both the FPGA implementation and fixed-point Simulink model of the proposed method are used simultaneously.

figures, the source separation method proposed in the present paper converges after utilizing approximately 2×10^6 samples, and the SNDR is enhanced from 23.84 dB to 65.84 dB by using our method.

For the second part of the simulations to evaluate the effectiveness of our method, a set of 500 Monte Carlo simulations was performed with the FPGA implementation to evaluate the stability of the proposed technique to the variation of input frequencies and random timing skews, and their results are reported here. Furthermore, the index of the bin, I_{bin} , is a *randomly generated prime number* from the interval $\{2, \dots, 2^{12}\}$ for each separate simulation.

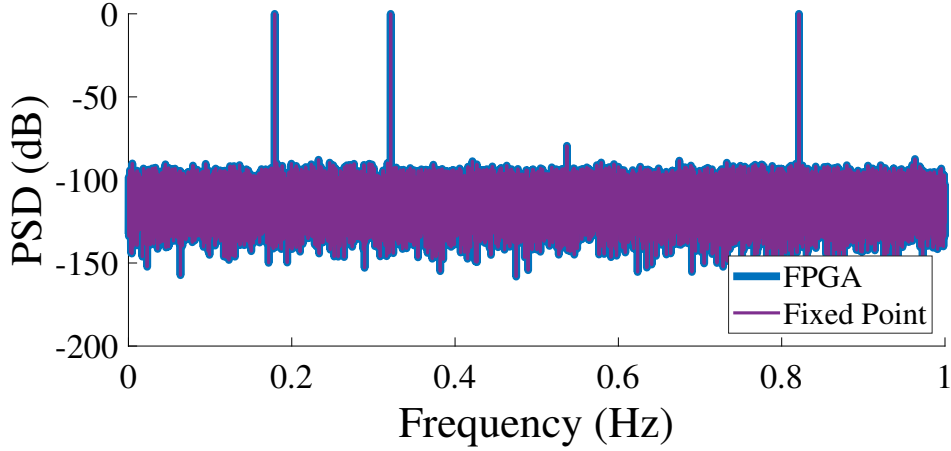


Figure 4.7 Output PSD of d_{err} corresponding to a single-tone sine wave and the TI-ADC, modeled in Simulink, when both the FPGA implementation and fixed-point Simulink model of the proposed method are used simultaneously.

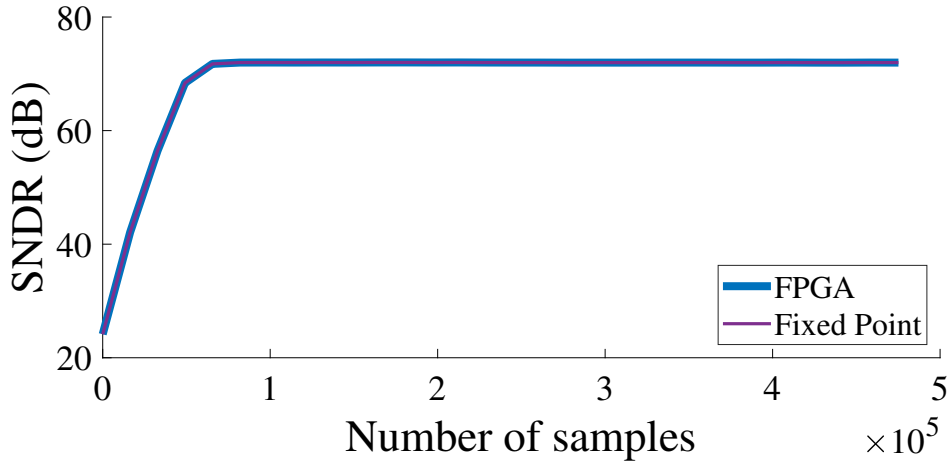


Figure 4.8 Convergence of SNDR corresponding to a single-tone sine wave with both the FPGA implementation and the fixed-point Simulink model of the proposed method running simultaneously.

The timing skews of the SADCs are also *independently and randomly generated* in each simulation run. The set of 500 Monte Carlo simulations are repeated for four different cases. In the first three cases, the same timing skew standard deviation of 10% was used; however, the lengths of the A-FIR and Hilbert transform filters were respectively set to $\{15, 30\}$, $\{30, 60\}$, and $\{60, 120\}$. The last case has the timing skew standard deviation of 5% and the lengths of the filters are set to $\{30, 60\}$. It is worth mentioning that the Monte Carlo simulations for each case reported above consumed about one day on an Intel® Xeon® E5-2637 processor.

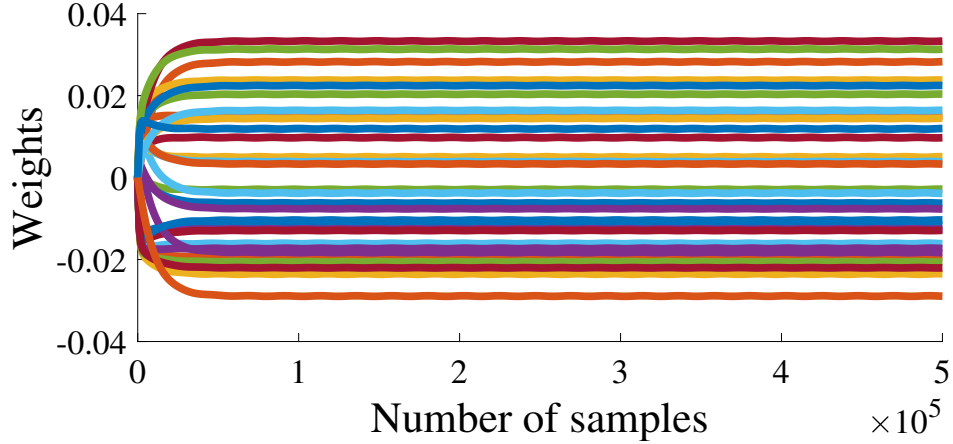


Figure 4.9 Convergence of $A\text{-}FIR_{rev}$'s coefficients corresponding to a single-tone sine wave with the fixed-point Simulink model of the proposed method.

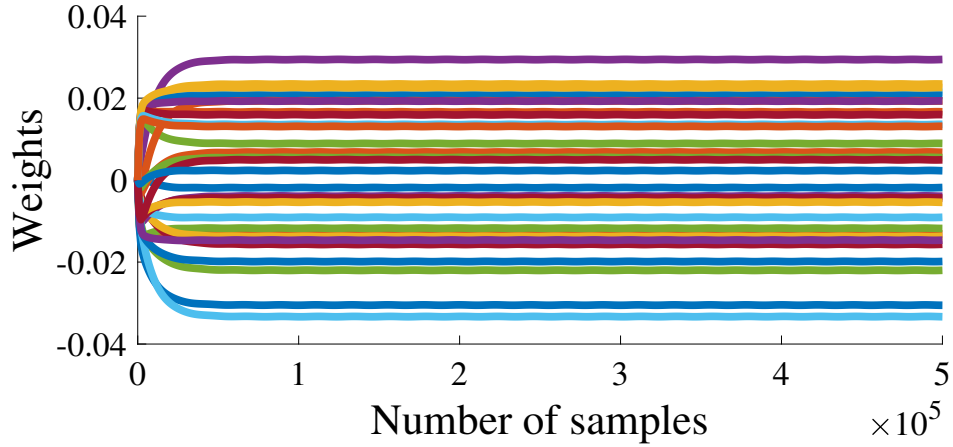


Figure 4.10 Convergence of $A\text{-}FIR_{err}$'s coefficients corresponding to a single-tone sine wave with the fixed-point Simulink model of the proposed method.

The stability analysis results report the mean of SNDRs on the TI-ADC digital output ($SNDR\ Mean_{dout}$) and the mean of SNDRs on the recovered signal ($SNDR\ Mean_{drcv}$). Also, the SNDR mean improvement is defined as $SNDR\ Mean_{drcv} - SNDR\ Mean_{dout}$. Table 4.3 summarizes these results. The results of the stability analysis are also illustrated in Figs. 4.17, 4.18, and 4.19. The second case is notable as its associated parameters are used for all the simulations reported in the rest of the paper. For this case, the SNDR mean of the TI-ADC, $Mean\ SNDR_{dout}$, is enhanced from 23.06 dB to 66.82 dB with an SNDR mean improvement of 43.81 dB. It is worth noting that the variations in the SNDR mean in the digital output before applying our method, $Mean\ SNDR_{dout}$, (third column of Table 4.3) are due to the random nature of Monte Carlo simulations, and these fluctuations for cases 1 to

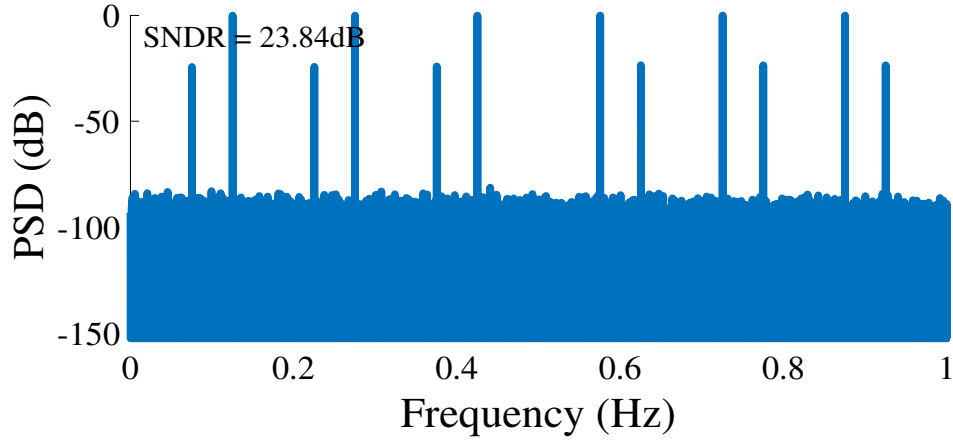


Figure 4.11 Output PSD of d_{out} corresponding to a 6-tone sine wave and the TI-ADC, modeled in Simulink, with the timing skews' standard deviation of 0.1 (10% of the TI-ADC's sampling period).

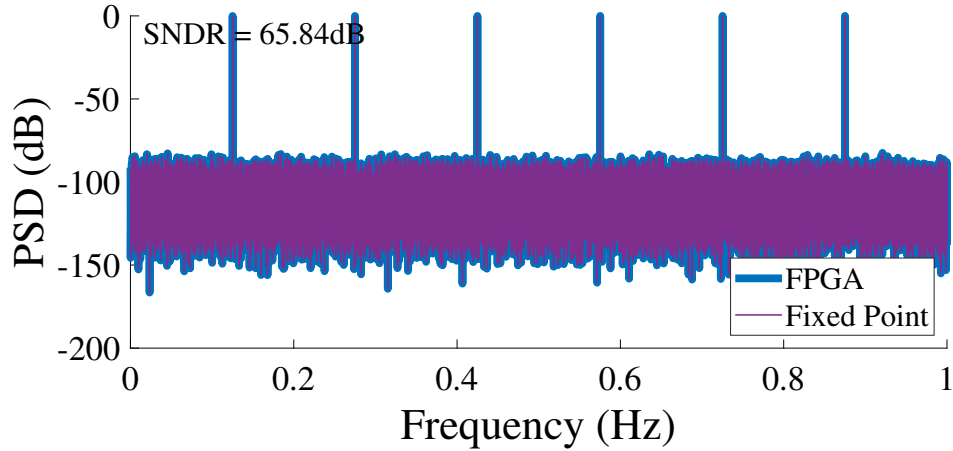


Figure 4.12 Output PSD of d_{rcv} corresponding to a 6-tone sine wave and the TI-ADC, modeled in Simulink, when both the FPGA implementation and fixed-point Simulink model of the proposed method are used simultaneously.

3, with having the same timing skew standard deviation of 10%, are less than 0.32 dB. These fluctuations, corresponding to less than 5.34% of one effective bit, are not significant.

In Table 4.3, obtained SNDRs in our distinct Monte Carlo simulations were greater/less than the SNDR mean of the recovered signal defined as best/worst cases. Also, the number of runs that led to divergence of the proposed method is indicated as a failure. As reported in Table 4.3, the SNDR mean of d_{rcv} , the SNDR improvement, and the rate of best cases improved with the lengths of the filter, and at the same time, the failure rate decreased. It is of interest that the SNDR mean of the recovered signal and the SNDR improvement are respectively

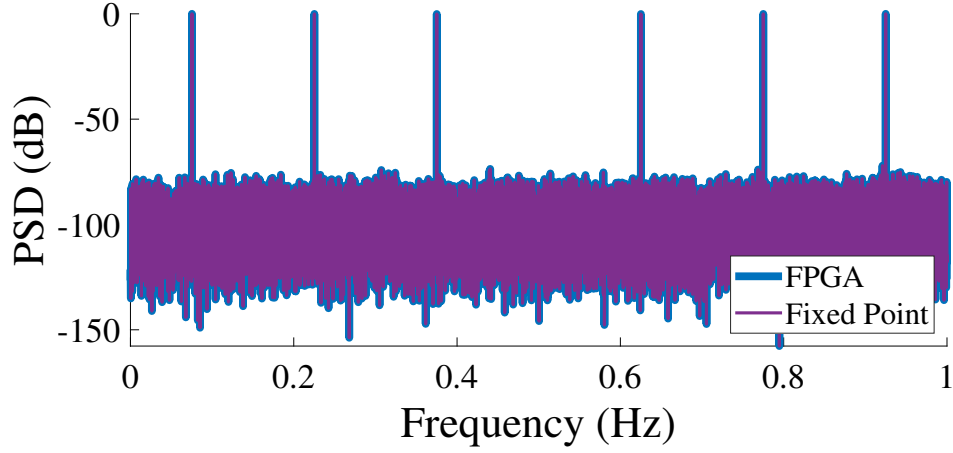


Figure 4.13 Output PSD of d_{err} corresponding to a 6-tone sine wave and the TI-ADC, modeled in Simulink, when both the FPGA implementation and fixed-point Simulink model of the proposed method are used simultaneously.

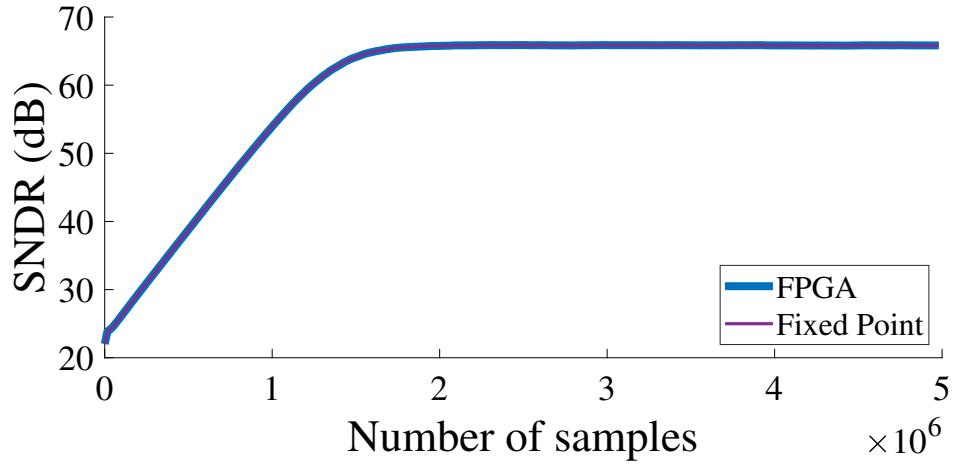


Figure 4.14 Convergence of SNDR corresponding to a 6-tone sine wave and the TI-ADC, modeled in Simulink, when both the FPGA implementation and fixed-point Simulink model of the proposed method are used simultaneously.

enhanced by 4.93 dB and 4.97 dB with quadrupling the filter sizes (from $\{15, 30\}$ to $\{60, 120\}$), while the failure rate decreased from 1.6% to 0.6%. Another comparison of interest is the one between the last case and the second case that shows the effect of reducing the timing skew standard deviation from 10% to 5%. In these experiments, the SNDR mean of d_{rev} improved from 66.82 dB to 69.51 dB (2.69 dB improvement) and the rate of best cases from 87.4% to 92.11% when the timing skew was reduced from 10% to 5%.

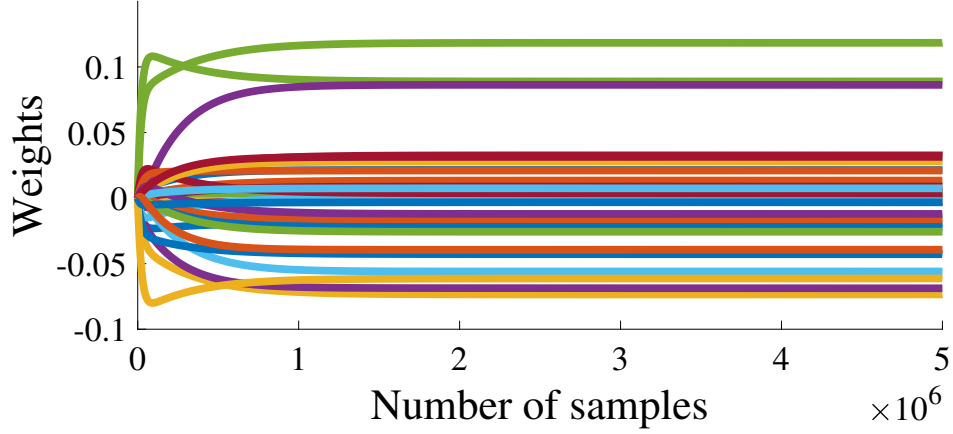


Figure 4.15 Convergence of $A\text{-}FIR_{rcv}$'s coefficients corresponding to a 6-tone sine wave with the fixed-point Simulink model of the proposed method.

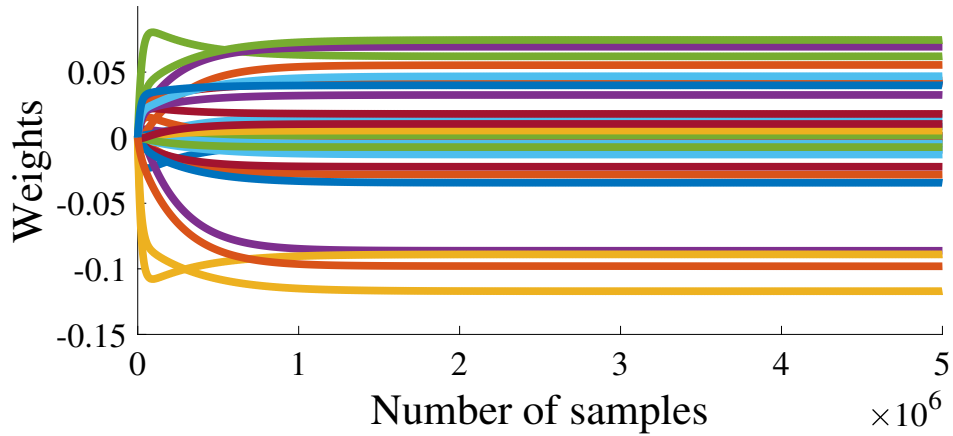


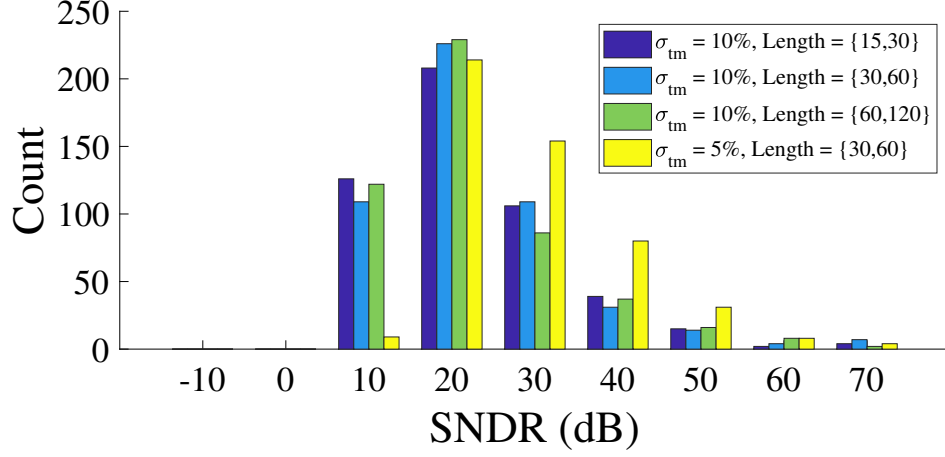
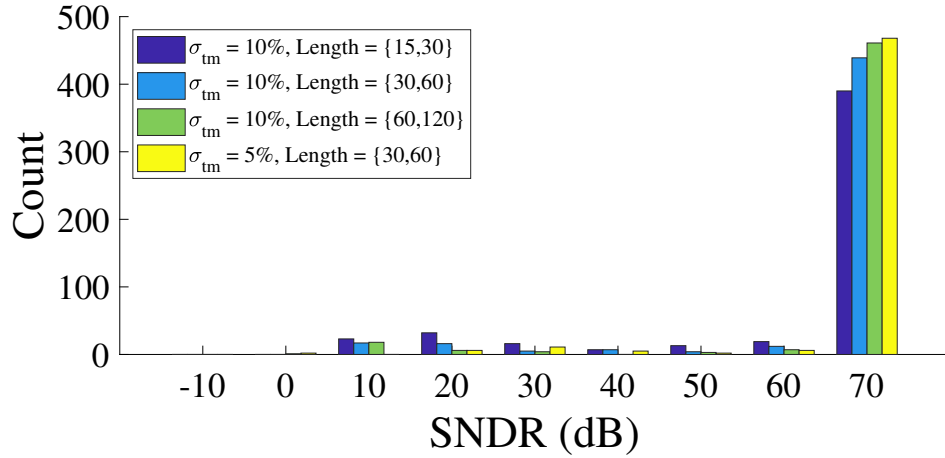
Figure 4.16 Convergence of $A\text{-}FIR_{err}$'s coefficients corresponding to a 6-tone sine wave with the fixed-point Simulink model of the proposed method.

4.5 Comparisons and Discussions

This paper aims to extend the applications of source separation algorithms to compensate for the timing skew mismatch in the TI-ADC for the first time. Creating a second input (d_{orth}) that captures the effect of the timing skew mismatches is a main contribution of this paper. As mentioned earlier, to obtain d_{orth} the Hilbert transform is used followed by down-sampling and up-sampling operations. This paper utilizes a symmetric source separation algorithm with feedback realization [63]. This algorithm needs two A-FIR filters in feedback loops for the separation and recovery of the desired element in the TI-ADC digital output. Unlike present all-digital and mixed-signal methods which estimate the amount of timing skews and then compensate them in the analog or digital domain, our method removes the errors in

Table 4.3 Stability Analysis Results

	Timing-mismatch, Lengths	SNDR $Mean_{d_{out}}$ (dB)	SNDR $Mean_{d_{rcv}}$ (dB)	SNDR Mean Improvement (dB)	Best Case (%)	Worst Case (%)	Failure (%)
Case 1	$\sigma_{tm} = 10\%$, Length = {15, 30}	22.78	62.93	40.14	79.01	9.6	1.6
Case 2	$\sigma_{tm} = 10\%$, Length = {30, 60}	23.06	66.82	43.81	87.4	6.2	1.2
Case 3	$\sigma_{tm} = 10\%$, Length = {60, 120}	22.74	67.86	45.11	91.2	5.09	0.6
Case 4	$\sigma_{tm} = 5\%$, Length = {30, 60}	29.05	69.51	40.45	92.11	3.4	1.4

Figure 4.17 Stability analysis: frequency of various SNDR of the digital output, d_{out} .Figure 4.18 Stability analysis: frequency of various SNDR at the recovered output, d_{rcv} .

the compensated digital output, d_{rcv} , by tuning the two adaptive FIR filters. It is of interest that in almost all digital calibration methods (e.g., [7, 8, 64]), sine-waves (single-tone and multi-tone) are used to validate the reported calibration mechanisms. Thus, single-tone and multi-tone sine waves are adapted to characterize and compare our method with competitive methods. In our simulations, the length of the A-FIR filters and Hilbert transform filter are selected according to the 6-tone input signal and the target resolution. These lengths could be reduced as a function of 1- the desired resolution, 2- the number of channels, and 3- the

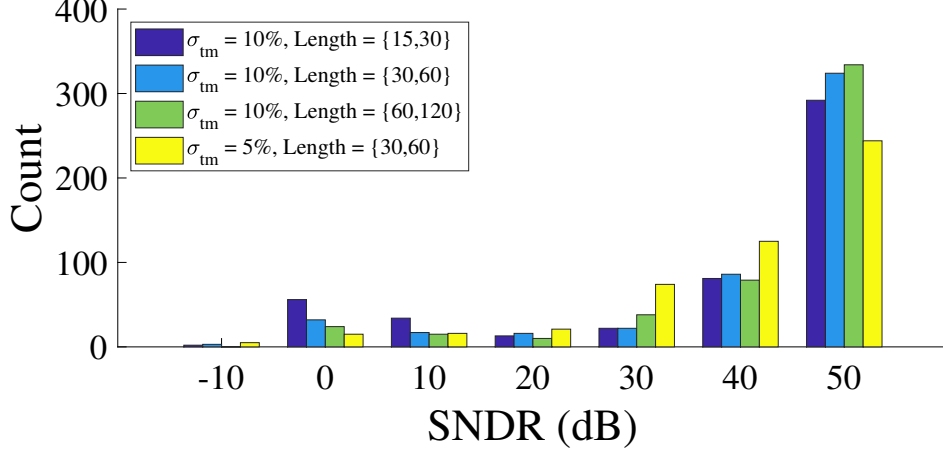


Figure 4.19 Stability analysis: frequency of observed improvements.

number of tones. As shown by Monte Carlo simulations, the rate of best cases and the mean of SNDRs at the output of our method improve at the expense of more complexity (growing the filter lengths). Therefore, the lengths should be optimized based on the target resolution. For instance, the length set of $\{15, 30\}$ is sufficient for an effective resolution of 10 bits.

In reference to Table 4.4, our all-digital method does not manipulate analog circuits and it does not require extra SADC(s) in contrast to [22, 28]. Unlike [5, 6, 46], our proposed technique can operate with input frequencies close to the Nyquist rate of the TI-ADC. Also, the presented mechanism can operate with any number of SADCs in contrast to [4, 6, 7, 25]. According to Table 4.4, the proposed method also exhibits better average SNDRs (66.82 dB for Case 2 and 69.51 dB for Case 4) than previously reported techniques, except for the method reported in [22]. Nonetheless, this technique achieves an SNDR mean of 72 dB at the cost of using an extra SADC, while the proposed method uses none. It is worth stressing that our paper opens other research avenues that can make the proposed method suitable for wider applications and/or to optimize its hardware and power consumption costs. The possible development could consider adapting other source separation algorithms and/or creating new combinations as the second input, d_{orth} .

In well-designed TI-ADCs, parametric variations appear only as thermal noise in the sample and hold stage of SADCs as well as offset, gain, and timing-skew mismatches among SADCs. In our TI-ADC Simulink model used for simulations, the thermal noise at the sample and hold stage and random sampling time skews in SADCs introduced by parametric variations are modeled in the simulations, and their other impacts (i.e., offset and gain mismatches) are neglected (assumed to be mitigated by some other means) to concentrate only on the compensation of the timing-skew mismatches similar to [6–8, 22, 64]. Since the TI-ADC model

in Simulink is used for the simulations, parametric variations have no additional impact on the measurement. Similar to previous schemes, our technique is also sensitive to offset and gain mismatches among the SADCs. In turn, prior to using the proposed mechanism, these mismatch terms must be estimated and compensated for. It is worth mentioning that since this technique just operates on the digital output of the TI-ADC, the behavioral simulations are reliable enough for verification of the performance and applicability of this method without the requirement for considering the analog circuit architecture of TI-ADC. By contrast, mixed-signal calibration methods must consider the TI-ADC and its analog circuits for verification. Although the sampling rate of the TI-ADC was set to 1 Hz for simplicity in our Simulink models, the rate at which the hardware operates with the proposed method can be as high as with any other competing methods, and it mainly depends on the technology being used. In the reported FPGA implementation (performed to validate the compatibility of the proposed method with hardware), the compensation engine can operate at a maximum rate of 147 MHz when the design targets the Xilinx384 Virtex-7 VX690T FPGA implemented with a 28 nm CMOS technology according to the timing report of the Xilinx Vivado Design Suite [55]. Clearly, that architecture would operate much faster if this compensation engine was embedded in a high-speed ASIC implemented in a state-of-the-art technology such as 3 nm TSMC [57].

4.6 Conclusions

In this paper, a source separation method for the recovery of the ideal samples of the TI-ADC input signal exempt from the timing skew mismatch error has been proposed. The main cost of the presented compensation method is the requirement of the two adaptive FIR (A-FIR) filters and an additional FIR filter to implement the Hilbert transform. Nevertheless, the number of taps of these FIR filters could be optimized according to the specific application. This method appears as a preferable choice over other methods in case no restriction on the number of SADCs is permitted. The proposed technique does not need any extra SADC(s) and it does not restrict the Nyquist range. The proposed method has been verified through

Table 4.4 Comparison with Compatible Methods

	This work (Case 2/Case 4)	[7]	[4]	[6]	[28]	[8]	[25]	[64]	[22]	[5]
Target Resolution (bits)	12	10	10	10	10	11	12	12	14	–
SNDR (dB)	66.82/69.51	61.9	61.96	58.07	54.2	60	46.61	63.58	72	66
Number of Samples (Iterations)	100k	50k	30k	0.6k	80k	10k	30k	200k	1.5k	80k
Bandwidth Limitation(s)	✗	✗	✓	✓	✗	✓	✗	✓	✗	✓
M (Number of SADCs)	4	8	2	4	8	4	4	4	4	4
Extra SADC(s)	✗	✗	✗	✗	✓	✗	✗	✗	✓	✗
Limitation on Number of SADCs	✗	2,4,6,...	2	4	8	✗	4	✗	✗	✗

behavioral simulations along with field-programmable-gate-array (FPGA) implementation. The proposed technique exhibited better SNDR in comparison to the present significant techniques. In the reported best case, the proposed method enhanced the SNDR from 22.57 dB to more than 71.96 dB.

CHAPTER 5 ARTICLE 3 : DIGITAL COMPENSATION OF TIMING-SKEW MISMATCH IN TI-ADCS BY POLYPHASE SOURCE SEPARATION

This chapter will present the article "Digital Compensation of Timing-Skew Mismatch in TI-ADCs by Polyphase Source Separation." This article has been submitted to "*IEEE Transactions on Circuits and Systems I: Regular Papers*". This article's main contribution is the polyphase source separation algorithm, which removes the errors arising from the timing-skew mismatch in the TI-ADC's digital output. The polyphase decomposition realizes the source separation algorithm approaches to relieve the speed requirement of the proposed method. For this phase, the Hadamard transform is used as a modulation operation to generate the second set of inputs to the source separation algorithm. The proposed method can operate in almost all the Nyquist range. It also performs its compensation task without the need for additional SADC(s) and without manipulating the TI-ADC's structure. The proposed technique avoids introducing any delay.

Digital Compensation of Timing-Skew Mismatch in TI-ADCs by Polyphase Source Separation

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5.1 Abstract

This paper proposes a fully digital timing-skew mismatch method for time-interleaved analog-to-digital converters (TI-ADCs) based on a polyphase realization of a source separation approach. The proposed mechanism separates the ideal samples of the input signal from the error element (arising from the timing-skew mismatch) in the digital output of sub-ADCs. Our technique benefits from its polyphase realization, allowing it to operate directly on the sub-ADCs data flow. Our method utilizes two polyphase adaptive filters (PAFs) and a modulation matrix, implementing the Hadamard transform. Unlike present techniques, the proposed approach avoids introducing any delay in the compensation path. It does not restrict the Nyquist frequency range, and it functions its compensation task without extra

sub-ADC. The proposed polyphase implementation thus relieves the operating speed requirements since the two PAFs only need to operate at the speed of the embedded sub-ADCs. This technique is validated by extensive behavioral simulations using MATLAB/Simulink, Vivado, and field-programmable gate array (FPGA) implementation. In an experiment reported in the present paper, the proposed method enhances the signal-to-noise and distortion ratio (SNDR) from 24.29 dB to more than 60.14 dB in a 12-bit TI-ADC when the standard deviation of timing-skew is 10 % of the TI-ADC's sampling period. These results show that our technique exhibits a better SNDR than almost all other competitive techniques.

5.2 Introduction

The present paper proposes an all-digital scheme for recovering the ideal input signal samples separated from the error element (arising from timing-skew mismatches) in the digital output of TI-ADC. Our technique utilizes the orthogonality between the desired component and the error component. The proposed approach adapts the source separation scheme reported in [69] and implements it using a polyphase approach [39, 46, 47]. It notably implements source separation and the Hadamard transform using polyphase adaptive filters (PAFs) and a modulation matrix. The polyphase implementation operates on each sub-ADC, thus relieving the speed requirements, unlike the reported methods in [23, 69]. Unlike almost all present compensation techniques, the proposed method avoids introducing any delay in the compensation path. Our technique shows a better SNDR than others (except for the method reported in [22]). However, [22] needs extra sub-ADC imposing modifications to TI-ADCs architecture, whereas our technique does not.

Our proposed method adjusts the coefficients of the two PAFs and allows the entire Nyquist frequency range to be used, unlike the schemes presented schemes in [5, 6, 21]. Our method is fully implementable in the digital domain without modifying the TI-ADC architecture or adding extra sub-ADC(s), unlike [22, 27, 28]. Nevertheless, our approach limits the number of sub-ADC(s) to specific numbers, similar to the method reported in [7]. The proposed mechanism performs its task during regular data conversion operations of the TI-ADC.

The paper is organized as follows. Section 5.3 introduces the proposed method. Section 5.4 provides simulation results confirming the excellent performance of the proposed method. Section 5.5 presents discusses. Finally, Section 5.6 concludes the paper.

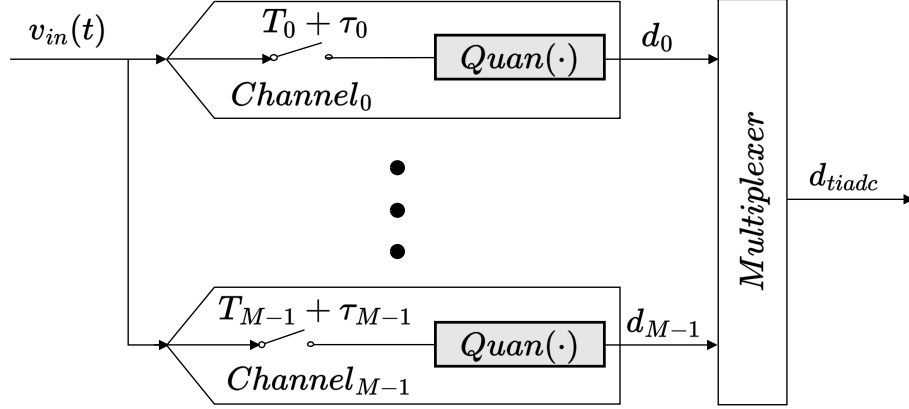


Figure 5.1 Architecture of a typical time-interleaved ADC (TI-ADC).

5.3 Proposed Polyphase Method

This section first reviews the detrimental impact of timing-skew mismatch on the performance of TI-ADCs. As depicted in Fig. 5.1, TI-ADC consists of multiple sub-ADCs. Nominally, the sub-ADCs have an identical architecture with the same effective resolution, B , and a sampling rate of F_s/M , where F_s denotes the overall sampling rate of the TI-ADC. The TI-ADC performs sampling of the input signal, v_{in} , by a clock pattern with the shifted sampling edges of kT_s in k th sub-ADC for $k = 0, \dots, M - 1$, where the sampling time, T_s , is identical to $1/F_s$ [70]. Due to this clock pattern, the input signal, v_{in} , is sampled at intervals of T_s seconds. The TI-ADC digital output is created by multiplexing the outputs of the sub-ADCs [23, 41].

As explained earlier, inherent *offset*, *gain*, and *sampling-time skew* mismatches among sub-ADCs (due to random PVT variations) severely degrade the effective resolution of TI-ADCs, calling for techniques to restore the desired resolution by estimating and correcting these mismatches. Our method only concentrates on timing-skew mismatches while assuming that the offset and gain mismatches are compensated by other means, as with previously reported techniques [4, 7, 16, 20, 28, 48, 49, 71].

To begin with, the effects of skew mismatches on the sampled input signal are presented. As seen from Fig. 5.1, the sampled input signal in the k th sub-ADC can be expressed as

$$v_{si,k}(m) = v_{in}(m \times MT_s - kT_s + \tau_k), \quad (5.1)$$

where $k = 0, \dots, M - 1$, and also, m and τ_k respectively stand for the discrete-time index (associated with the operating rate of F_s/M) and k th timing skew. From the Taylor series ap-

proximation, it is clear, [21–23,68,69], that the k th sampled input signal can be approximated as

$$v_{si,k}(m) \approx v_{in}(mMT_s - kT_s) + \tau_k \frac{dv_{in}(mMT_s - kT_s)}{dt} \quad (5.2)$$

where $k = 0, \dots, M - 1$. The outputs of the sub-ADCs, d_k , ideally represent their respective inputs plus injected error terms resulting from the quantization process [23,69]. This section neglects the quantization errors to concentrate on the proposed method. Also, this paper uses capital letters for the frequency-domain equivalents of time-domain signals.

As mentioned above, multiplexing the outputs of the sub-ADCs creates the digital output of the TI-ADC. Multiplexing in the frequency domain is equivalent to up-sampling of the outputs of the sub-ADCs by M and then passing through the delay operators of $M - k$ (in the frequency domain, $= e^{-j(M-k)\omega}$). It can be shown that [23] the digital output of the TI-ADC in the frequency domain is given by

$$D_{tiadc}(e^{j\omega}) = e^{-jM\omega} \{V_{in}(e^{j\omega}) + E_{er}(e^{j\omega})\} \quad (5.3)$$

where the element E_{er} stands for the error element (arising from the sampling-time skew mismatch), expressed as

$$E_{er}(e^{j\omega}) = \frac{1}{M} \sum_{i=0}^{M-1} E_{er,i}(e^{j\omega}) V_{in}(e^{j(\omega - \frac{2\pi i}{M})}) j(\omega - \frac{2\pi i}{M}) \quad (5.4)$$

where $E_{er,i}$ denotes the i th error term arising from the i th image of the input signal as follows

$$E_{er,i}(e^{j\omega}) = \sum_{k=0}^{M-1} \tau_k e^{-jk \frac{2\pi i}{M}}. \quad (5.5)$$

The term $e^{-jM\omega}$ in (5.3) is notable as it translates into a delay of M samples in the digital output, d_{tiadc} . The digital output, d_{tiadc} , consists of the input signal, and the timing skew mismatch manifests itself as the images $E_{er,i}$ in the digital output. However, the same is not *valid for the error terms*, $E_{er,i}$, $i = 0, \dots, M - 1$, since the timing skews have a random nature with distinct values. It can be shown that the input signal is orthogonal with the error element E_{er} [23]. For this reason, a source separation mechanism can be used to recover E_{er} from D_{tiadc} by separating them.

This paper develops the symmetrical source separation algorithm with feedback realization reported in [69] to its proposed polyphase implementation. The proposed polyphase method directly operates on the digital output of the sub-ADCs (at the rate of F_s/M), unlike the method reported in [69], which operates on the TI-ADC output at the rate of F_s . The

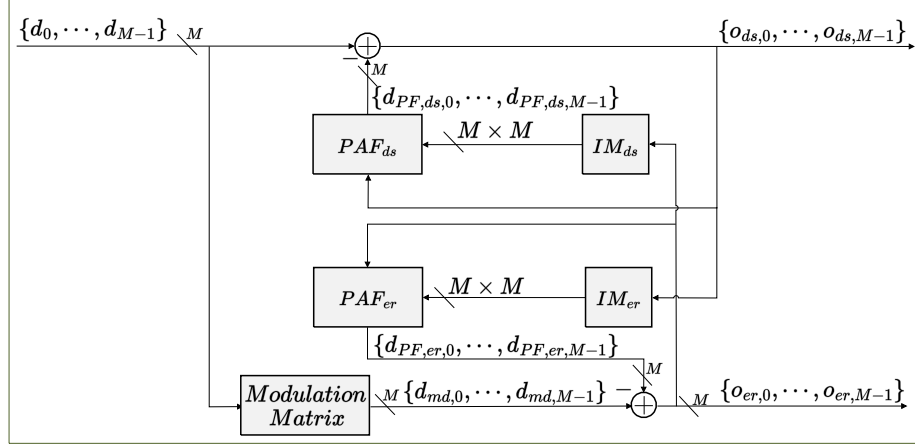


Figure 5.2 Architecture of polyphase symmetrical adaptive source separation method.

proposed polyphase source separation approach consists of two polyphase adaptive filters. The architecture and operation of the polyphase filter are briefly explained in Appendix 5.7. The proposed method uses modulation operation realized by Hadamard matrix to generate course estimate of the error element, E_{er} , as the required second input since the source separation method uses the decorrelation principle, needing at least two inputs, to recognize and categorize the ideal samples of the input signal and the error element, E_{er} , (arising from the timing-skew mismatch) in the digital output of TI-ADC [61, 63, 69].

Fig. 5.2 depicts the proposed polyphase source separation method. The proposed technique targets decorrelating its desired output vector, $\mathbf{O}_{ds}$ (including, $\{O_{ds,0}, \dots, O_{ds,M-1}\}$), and the error output vector, $\mathbf{O}_{er}$ (including, $\{O_{er,0}, \dots, O_{er}\}$). Since the error element, E_{er} , is orthogonal to the desired samples of the input signal, the proposed method routes the desired samples of the input signal to its desired output, $\mathbf{O}_{ds}$, and the error element, E_{er} , to its error output, $\mathbf{O}_{ds}$. In reference to the single-rate technique reported in [69], the modulation matrix of order M creates the modulated vector, $\mathbf{D}_{md}$, $\{D_{md,0}, \dots, D_{md,M-1}\}$, by modulating the vector $\mathbf{D}$ consisting of the outputs of sub-ADCs, $\{D_0, \dots, D_{M-1}\}$. The modulation matrix can be generally realized by the complex frequency shift mechanism introduced in [5]. Nonetheless, this paper alternatively uses the Hadamard transform to reduce the hardware complexity (see Section 5.5.4). The inputs and outputs of the two polyphase filters PAF_{ds} and PAF_{er} are worth mentioning, as both receive a vector of the size $M \times M$ from their respective input metric. While the filter PAF_{ds} acquires the error output vector $\mathbf{O}_{er}$ via its associated input matrix $\mathbf{IM}_{ds}$ to remove the error terms in the desired vector, $\mathbf{O}_{ds}$. This polyphase filter needs the error output $\mathbf{O}_{ds}$ to tune itself by evaluating and comparing the desired output with the error output $\mathbf{O}_{er}$. On the other hand, the polyphase filter PAF_{er}

receives the desired output vector $\mathbf{O}_{ds}$ through its respective input matrix $\mathbf{IM}_{er}$ to purify the error output $\mathbf{O}_{er}$ from the desired signal. This filter tunes itself by evaluating and comparing the error output with the desired output $\mathbf{O}_{ds}$. The outputs of the polyphase source separation method can be expressed as follows

$$\mathbf{O}_{ds}(z) = \mathbf{D}(z) - \mathbf{PF}_{er}(z) \times \mathbf{O}_{er}(z), \quad (5.6)$$

$$\mathbf{O}_{er}(z) = \mathbf{D}_{md}(z) - \mathbf{PF}_{ds}(z) \times \mathbf{O}_{ds}(z), \quad (5.7)$$

where $\mathbf{PF}_{ds}$ and $\mathbf{PF}_{er}$ respectively represent the filter vectors of PAF_{ds} and PAF_{er} , expressed as

$$\mathbf{PF}_{ds}(z) = \mathbf{IM}_{ds}(z) \times \mathbf{PC}_{ds}(z), \quad (5.8)$$

$$\mathbf{PF}_{er}(z) = \mathbf{IM}_{er}(z) \times \mathbf{PC}_{er}(z), \quad (5.9)$$

where $\mathbf{PC}_{ds}$ and $\mathbf{PC}_{er}$ respectively denote the polyphase component vector of filters PAF_{ds} and PAF_{er} , and also, $\mathbf{IM}_{er}$ and $\mathbf{IM}_{ds}$ respectively represent the outputs of the input metric associated with the filters PAF_{ds} and PAF_{er} , respectively (see Appendix 5.7).

5.3.1 Tuning Polyphase FIR Filters

The polyphase realization of the source separation algorithm treats the adjustments of the processing errors (when tuning the filters PAF_{ds} and PAF_{er}) as leakages of the error element in the desired output and the leakages of the desired element in the error output. The LMS algorithm tunes the coefficients of the polyphase components, $PC_{ds,j}$ and $PC_{er,j}$ $j = 0, \dots, M-1$, for both the polyphase filters. For this reason, gradual adjustment of the coefficients of $PC_{ds,j}$ and $PC_{er,j}$ needs to process all the sub-ADC outputs concurrently. Each component, $PC_{ds,j}$ and $PC_{er,j}$ $j = 0, \dots, M-1$, remains the same in all the M FIR filters PAF_{ds} and PAF_{er} even though receiving M different inputs (i.e., the outputs of the input metric).

The LMS algorithm tunes the coefficients of the PAFs by the energy signal, defined as

$$\begin{aligned} \xi_{ds,PC_j} &= \sum_{i=0}^{M-1} E(ds_{PC_j,i}^2), \\ \xi_{er,PC_j} &= \sum_{i=0}^{M-1} E(er_{PC_j,i}^2), \end{aligned} \quad (5.10)$$

where $j = 0, \dots, M-1$, and also, $ds_{PC_j,i}$ and $er_{PC_j,i}$ respectively stand for the outputs of the j th polyphase component receiving their i th inputs $im_{er,i,j}$ and $im_{ds,i,j}$ from the input metric. The minimization of the energy signals denotes the decorrelation of the desired output from the error output. According to the LMS algorithm, the update steps of the coefficients can

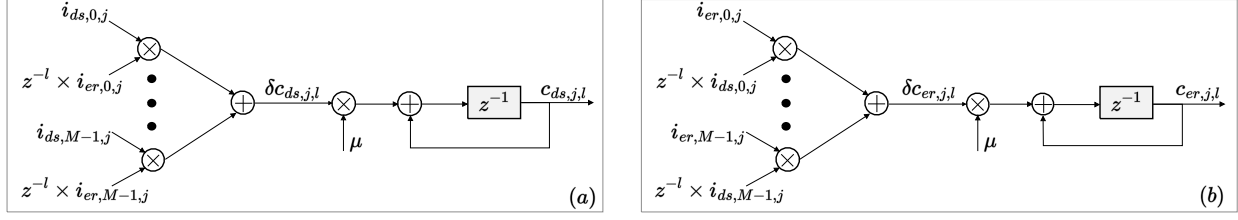


Figure 5.3 The LMS update block diagram, adjusting the l^{th} coefficient of the j^{th} polyphase component in (a): PAF_{ds} , (b): PAF_{er} .

gradually minimize the energy signal, defined as

$$\begin{aligned} \delta c_{ds,j,l}(m) &= \frac{d\xi_{ds,PC_j}}{dc_{ds,j,l}}, \\ \delta c_{er,j,l}(m) &= \frac{d\xi_{er,PC_j}}{dc_{er,j,l}}. \end{aligned} \quad (5.11)$$

From (5.10) and (5.11), it is obvious to show that the update steps can be expressed as

$$\begin{aligned} \delta c_{ds,j,l}(m) &= \sum_{i=0}^{M-1} im_{ds,i,j}(m) \times im_{er,i,j}(m-l), \\ \delta c_{er,j,l}(m) &= \sum_{i=0}^{M-1} im_{er,i,j}(m) \times im_{ds,i,j}(m-l). \end{aligned} \quad (5.12)$$

In the frequency domain, these equations can also be expressed as

$$\begin{aligned} \delta C_{ds,j,l}(z) &= \mathbf{D}_{cp}(z) \cdot z^{-l} \mathbf{IM}_{ds,j}(z), \\ \delta C_{er,j,l}(z) &= \mathbf{D}_{cp}(z) \cdot z^{-l} \mathbf{IM}_{j_{er,j}}(z) \end{aligned} \quad (5.13)$$

where $\mathbf{IM}_{ds,j}$ and $\mathbf{IM}_{j_{er,j}}$ denote the j^{th} column of the input matrices. In addition, the update equations that adjust the coefficients of the polyphase FIR filters are given by

$$\begin{aligned} c_{ds,j,l}(m+1) &= c_{ds,j,l}(m) + \mu \times \delta c_{ds,j,l}(m), \\ c_{er,j,l}(m+1) &= c_{er,j,l}(m) + \mu \times \delta c_{er,j,l}(m), \end{aligned} \quad (5.14)$$

where $j = 0, \dots, M-1$, and $l = 1, \dots, FL$. Also, the parameter μ is the update size by which the stability of the coefficients of the two polyphase filters is ensured. Fig. 5.3 depicts the update block diagram adjusting the l^{th} coefficient of the j^{th} polyphase components. The polyphase implementation, where the bank of M FIR filters operates at $1/M$ th of the single-rate FIR filter, does not increase the power dissipation compared to the single-rate implementation reported in [69].

Similar to its single-rate counterpart, the factor μ must be selected carefully to stabilize the polyphase filters. The suitable selection of the parameter μ guarantees the stability of

the AFIR filters. The stability margin improves as μ reduces at the expense of a reduced convergence rate of the proposed technique [72]. Furthermore, the impact of the number of sub-ADCs and the input signal's bandwidth on the proposed method is notable, as the filters PAF_{ds} and PAF_{er} with more taps must be used as these two parameters increase. Accordingly, the bandwidth requirements and the number of sub-ADCs determine the optimum number of taps for the PAFs.

5.4 Simulation Results and Discussions

Using MATLAB/Simulink and Vivado Design Suite, several simulations of target field-programmable gate array (FPGA) implementations were performed to verify and validate our compensation method. Moreover, this section targets verifying the proposed technique's performance for different word widths, validating its synthesizability, and evaluating its hardware cost. The following simulations use a behavioral TI-ADC model in Simulink. This model consists of four identical sub-ADCs restricted by thermal noise and quantization error to 12 bits. For simplicity, the TI-ADC's sampling rate, F_s , is normalized to *one*, and the standard deviation of the timing-skew mismatch is set to 0.1 (i.e., 10 % of the TI-ADC's sampling period). Proper convergence of the proposed compensation technique relies on a maximum of 2^{-12} for the update step factor, μ . The size of the polyphase filters, FL , was set to 15.

In these simulations, fast Fourier transforms (FFTs) of length N_{fft} are utilized to measure and evaluate the performance of our method. Also, length of signals N_{fft} are employed as the input signal of the TI-ADC to prevent spectral leakage. The frequency selected for the input tones, f_{in} , is of interest as it translates to the bin index I_{bin} in the FFT outputs with a value of $F_s \times I_{bin} / N_{fft}$. In the following simulations, the bin index I_{bin} is referred to as an alternate for the frequency of the input tones. The values selected for I_{bin} were prime numbers to make the TI-ADC quantization errors spectrum uniform (it avoids repetitive patterns in the input tone(s)) [23, 53, 54]. In our simulations, N_{fft} is set to 2^{B+1} ($= 2^{13}$).

The simulations begin by evaluating the word width impact on our method's performance to select the optimum width regarding the signal-to-noise-and-distortion ratio (SNDR) and hardware cost. A fixed-point Simulink model of the proposed method was used in this part, and a single-tone sine wave with its corresponding I_{bin} was applied as the input signal. For each word width, 563 simulation runs were performed by sequentially selecting prime numbers in the range $\{1, \dots, N_{fft}/2\}$ for the bin I_{bin} , and these SNDR outcomes are gathered to obtain the mean of SNDRs. Table 5.1 provides the results of this part of the simulation with different word widths.

Table 5.1 Impact of Word Width

Word Width (bits)	14	15	16	17	18
$Mean_{SNDR}$ (dB)	60.31	63.70	65.38	65.91	66.02
σ_{SNDR} (dB)	12.49	13.76	14.49	14.68	10.08

The proposed method's fixed-point version of the Simulink model was implemented on FPGA to validate its synthesizability and the hardware cost for each word width. The FPGA implementations target the Xilinx Virtex-7 VX690T realized on 28-nm technology. The Virtex-7 VX690T series from Xilinx comprises 2800 DSP slices and 485k logic cells. First, the Simulink fixed-point model of our method is converted to Verilog HDL codes with the Simulink HDL Coder [55]. These codes are then synthesized and implemented on FPGA by the MATLAB FIL Wizard and the Vivado Design Suite. The transfer rate via the JTAG protocol for communicating is 12.5 MHz. Table 5.2 provides the hardware cost of FPGA implementation for various word widths. This table shows that the SNDR mean enhances as the word width expands from 14 to 16 bits. Nevertheless, the improvement beyond 16 bits is negligible. The absence of results for word widths lower than 14 bits is worth mentioning in Table 5.1 as the proposed method failed to converge for such word widths. As shown in Table 5.2, the hardware and power consumption costs expand with growing word width. Thus, a 16-bit word width is the best compromise between a good SNDR and an acceptable hardware cost.

The following simulations depict the convergence of the PAFs and also the PSD of the *digital output*, d_{tiadc} , the *desired output*, o_{ds} , and the *error output*, o_{er} . Single-tone and 4-tone sine-wave inputs are applied to the TI-ADC for these simulations. This part of the simulations utilizes the TI-ADC, modeled in Simulink with floating-point precision, together with the proposed method's FPGA implementation and the fixed-point Simulink model.

First, a single-tone sine wave is applied to the TI-ADC as the input signal with its corresponding bin index $I_{bin} = 2781$. Fig. 5.4 depicts the PSD of d_{tiadc} , and also, Figs. 5.5 and 5.6 respectively show the PSD of the desired output, o_{ds} , and the error output, o_{er} , after the proposed compensation method has converged. These figures indicate that almost all harmonics of d_{tiadc} are significantly attenuated in o_{ds} . Also, the convergence of SNDR, PAF_{ds} , and PAF_{er} are respectively depicted in Figs. 5.7, 5.8, and 5.9. The proposed approach enhances the SNDR from 22.57 dB to more than 71.51 dB. Our method converges with approximately 3×10^5 samples and remains stable after convergence. As evident from Figs. 5.5, 5.6, and 5.7, the results of the fixed-point Simulink model and the FPGA implementation of the proposed method entirely match validating the synthesizability of the Simulink model with fixed point

Table 5.2 Hardware Cost

Word Width (bits)	14	15	16	17	18
Lookup Tables (%)	6.88	6.41	6.6	15.05	21.81
Flip Flops (%)	0.92	0.95	0.98	1.18	1.31
DSP Slices (%)	28.89	28.89	28.89	28.89	28.89

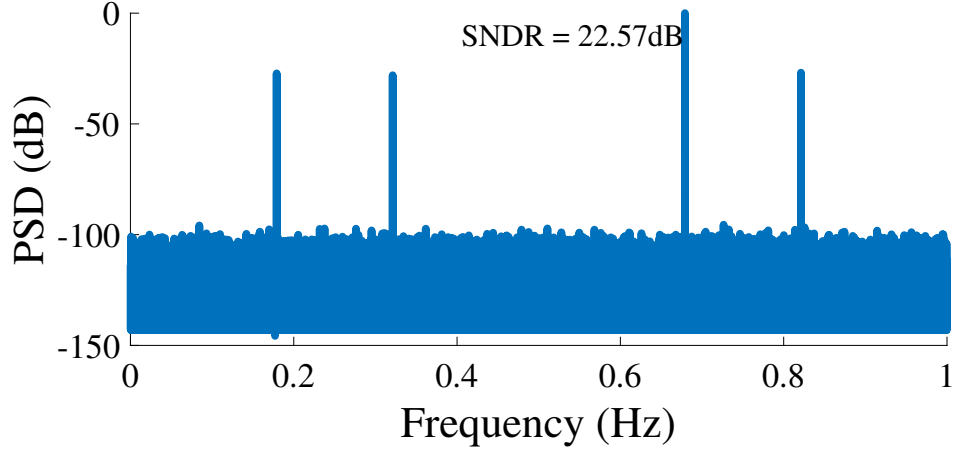


Figure 5.4 Output PSD of d_{tiadc} corresponding to a single-tone sine-wave when the TI-ADC, modeled in Simulink, is not compensated and the standard deviation of timing skews is 0.1 (10 % of the sampling clock period).

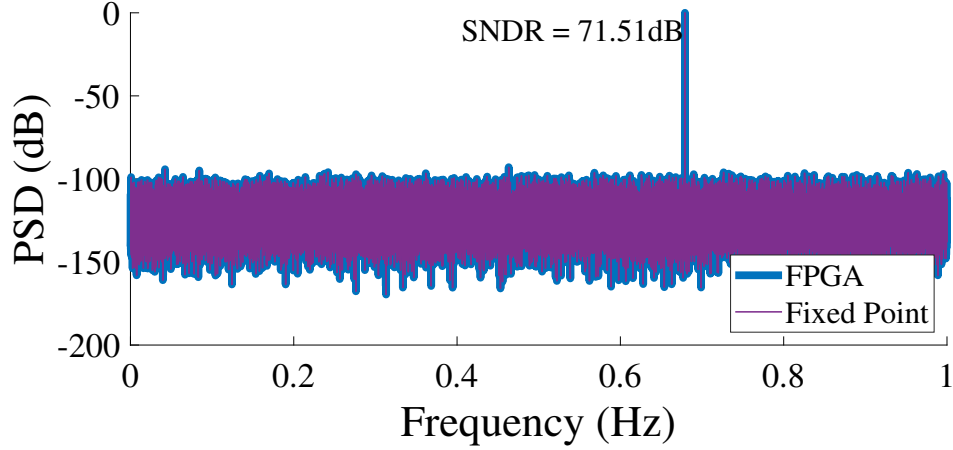


Figure 5.5 PSD of o_{ds} (the desired output) corresponding to a single-tone sine-wave when the TI-ADC, modeled in Simulink, is compensated with both the FPGA implementation and the fixed-point Simulink model.

precision.

In addition, these simulations evaluate the proposed method's performance for the 4-tone sine-wave input signal with its corresponding bins $I_{bin} = \{530, 902, 1274, 1647\}$. This part

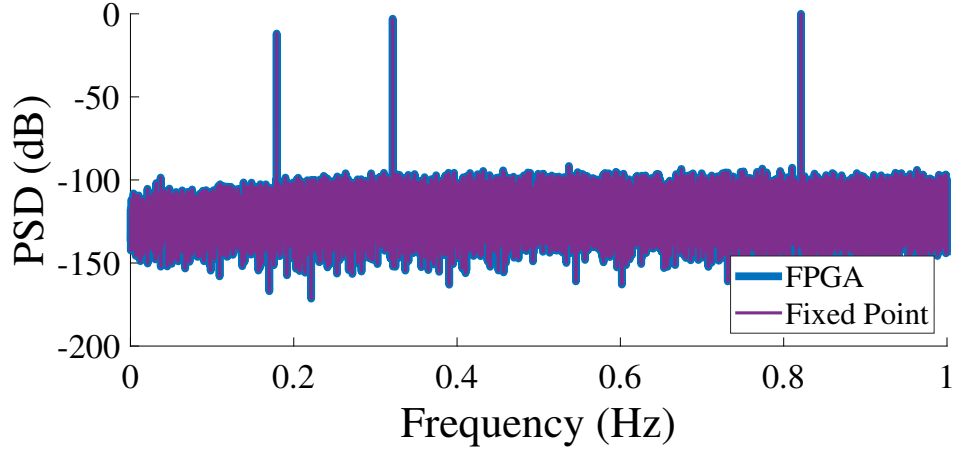


Figure 5.6 PSD of o_{er} (the error output) corresponding to a single-tone sine-wave when the TI-ADC, modeled in Simulink, is compensated with both the FPGA implementation and the fixed-point Simulink model.

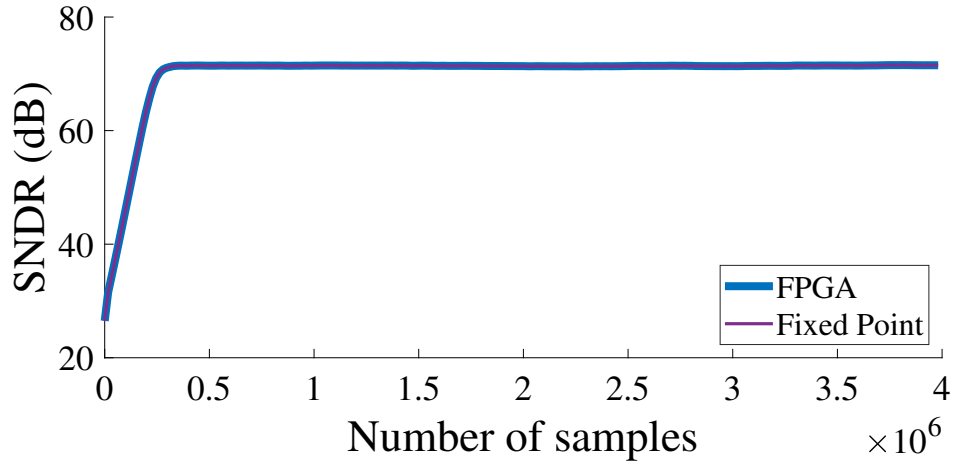


Figure 5.7 SNDR convergence observed with a single-tone sine-wave when both the proposed method's FPGA implementation and the fixed-point Simulink model are used.

of the simulations again utilizes the TI-ADC modeled in Simulink, together with the FPGA implementation and the proposed method's fixed-point Simulink model. Fig. 5.10 shows the PSD of the digital output, d_{tiadc} . Figs. 5.11 and 5.12 respectively depict the PSDs of the desired output, o_{ds} , and the error output, o_{er} after the convergence of the proposed technique. As seen from these figures, almost all harmonics of the digital output, d_{tiadc} , are extremely attenuated in the desired output, o_{ds} . Figs. 5.13, 5.14, and 5.15 also indicate the convergence of SNDR, PAF_{ds} , and PAF_{er} , respectively. As seen from these figures, this method converges after utilizing approximately 5×10^6 samples, and also, the SNDR is enhanced from 24.11 dB to 66.92 dB. As evident from Figs. 5.11, 5.12, and 5.13, the results

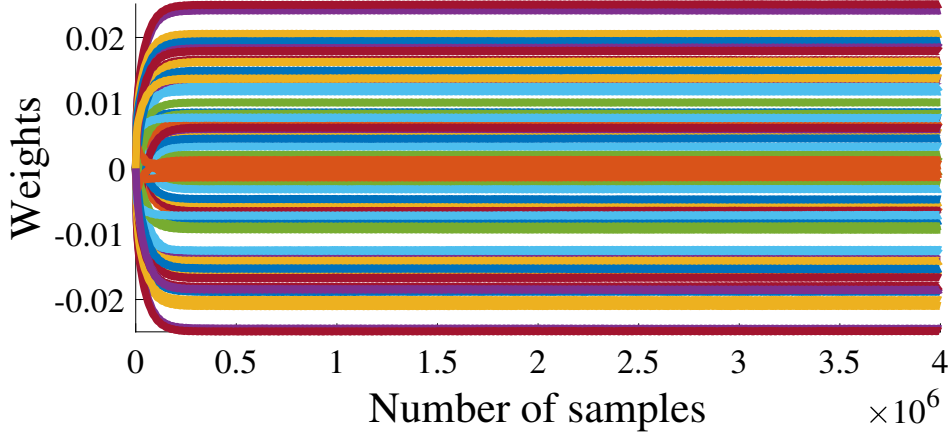


Figure 5.8 Convergence of the PAF_{ds} 's coefficients (for the desired element) observed with a single-tone sine-wave when the fixed-point Simulink model is used.

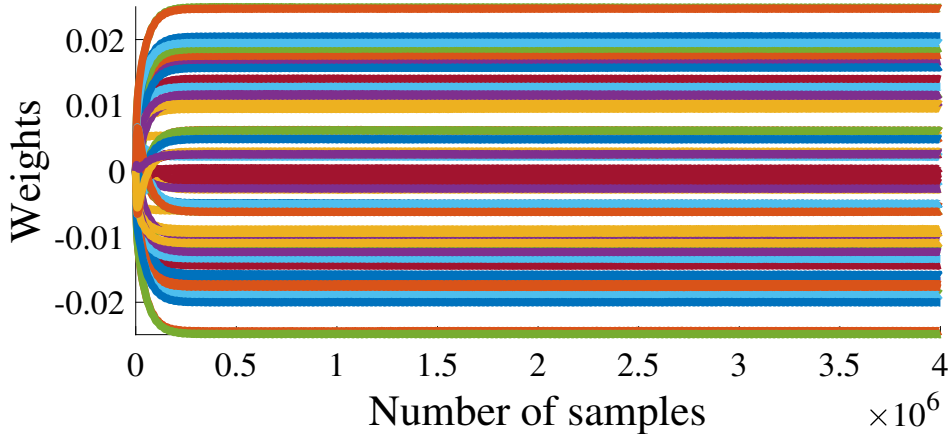


Figure 5.9 Convergence of the PAF_{er} 's coefficients (for the error element) observed with a single-tone sine-wave when the fixed-point Simulink model is used.

of the fixed-point Simulink model and the FPGA implementation of the proposed method entirely match, again validating the synthesizability of the Simulink model as a fixed point precision implementation.

Finally, Monte Carlo simulations are performed to evaluate the stability of our proposed technique under three cases of varying the frequency of the single-tone sine wave (injected as the input signal) and random timing skews. This part of the simulations utilizes the TI-ADC, modeled in Simulink, and the proposed method's FPGA implementation. For each case, a set of 500 separate simulation runs is gathered. In these three cases, the timing-skew standard deviation is selected as 10 %, 5 %, and 2.5 % of the TI-ADC's sampling rate, and the bin index, I_{bin} , is a *randomly generated prime number* for each separate simulation.

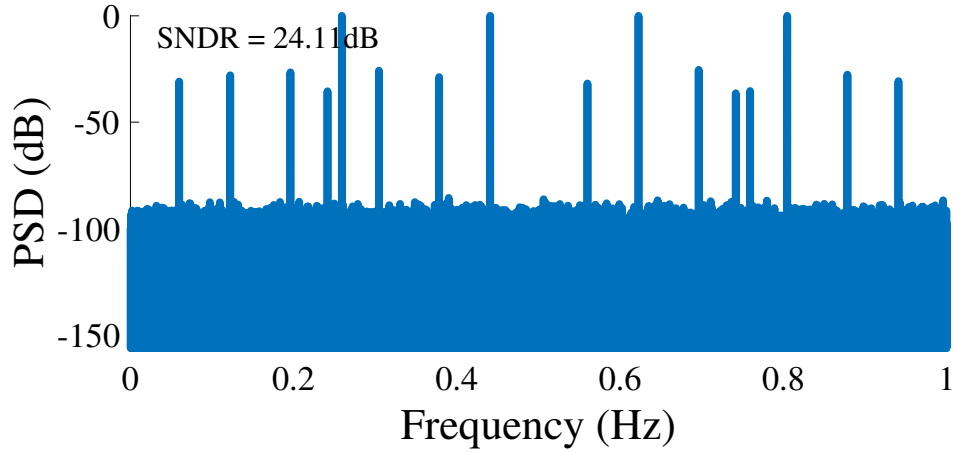


Figure 5.10 Output PSD of d_{tiadc} corresponding to a 4-tone sine-wave when the TI-ADC, modeled in Simulink, is not compensated and the standard deviation of timing skews is 0.1 (10 % of the sampling clock).

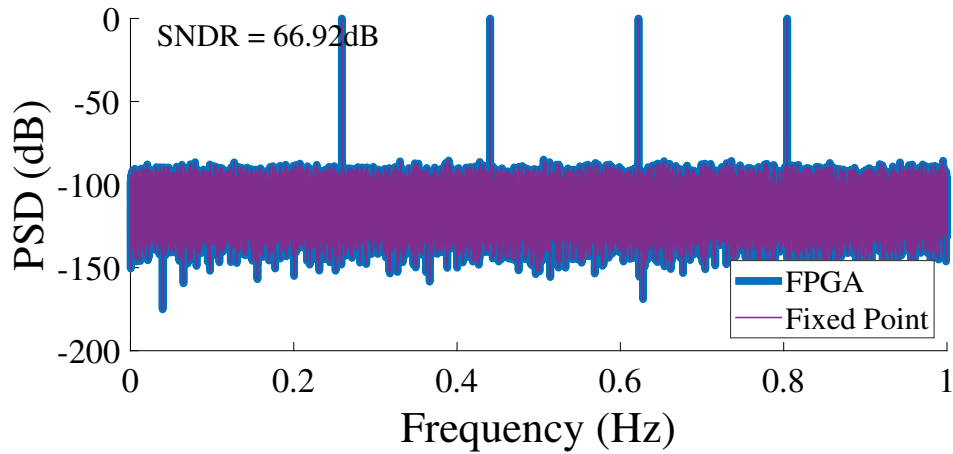


Figure 5.11 PSD of o_{ds} (the desired output) corresponding to a 4-tone sine-wave when the TI-ADC, modeled in Simulink, is compensated with both the FPGA implementation and the fixed-point Simulink model.

In each simulation run, the timing skews of the sub-ADCs are also *independently and randomly generated with Gaussian distribution*. Figs. 5.16, 5.17, and 5.18 respectively show the results of stability analysis of the TI-ADC digital output, d_{tiadc} , the desired output, o_{ds} , the improvement by the proposed technique. The improvement is notable as it is defined as the SNDR difference between the desired output and the TI-ADC's digital output (i.e., $SNDR_{improve} = SNDR_{o_{ds}} - SNDR_{d_{tiadc}}$). Furthermore, Table 5.3 provides more data on this simulation part. As shown in Table 5.3, the mean of the collected SNDRs of TI-ADC digital output is improved from 24.29 dB to 60.14 dB for Case 1, from 28.99 dB to 65.93 dB

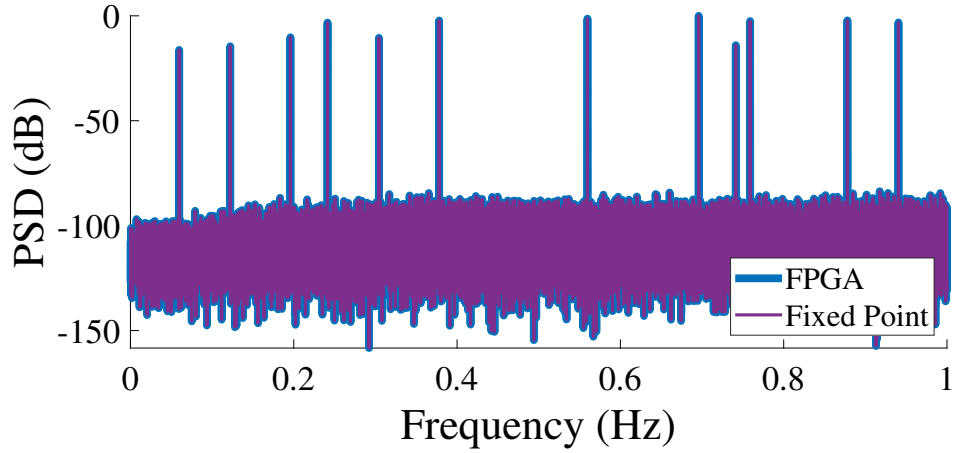


Figure 5.12 PSD of o_{er} (the error output) corresponding to a 4-tone sine-wave when the TI-ADC, modeled in Simulink, is compensated with both the FPGA implementation and the fixed-point Simulink model.

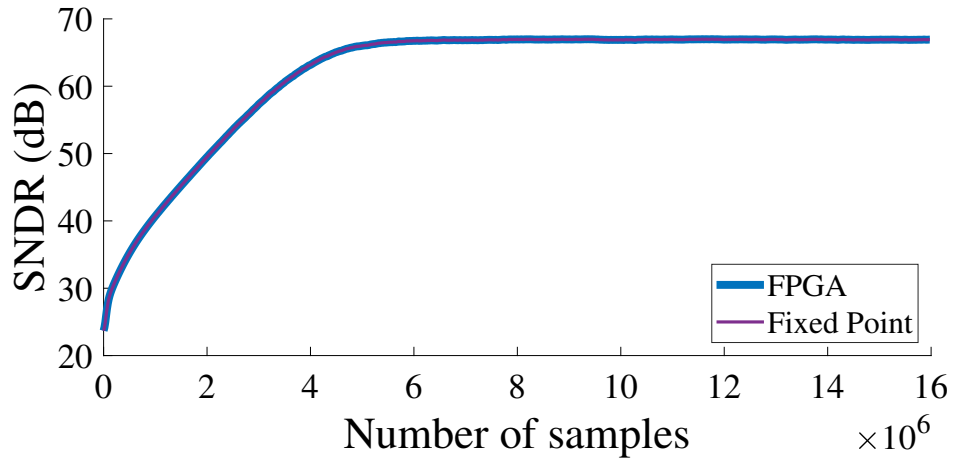


Figure 5.13 SNDR convergence observed with a 4-tone sine-wave when both the proposed method's FPGA implementation and the fixed-point Simulink model are used.

for Case 2, and from 35.19 dB to 68.14 dB for Case 3 after using the proposed compensation method. From Case 1 to Case 3, the SNDR mean of the desired output improves from 60.14 dB to 68.14 dB (i.e., by reducing the standard deviation of the timing-skew mismatch from 10 % to 2.5 %). In the table, the improved SNDR rate is defined as the occurrence frequency of the experiments for which the compensated SNDR is greater than the SNDR of the TI-ADC's digital output, and the degraded SNDR rate is defined as the rate with which the compensated SNDR is smaller than the SNDR of the TI-ADC's digital output. Failure is expressed as the rate at which the proposed technique diverges. The rate at which the SNDR is improved and degraded remains almost the same, at 99 % and 1 % for the

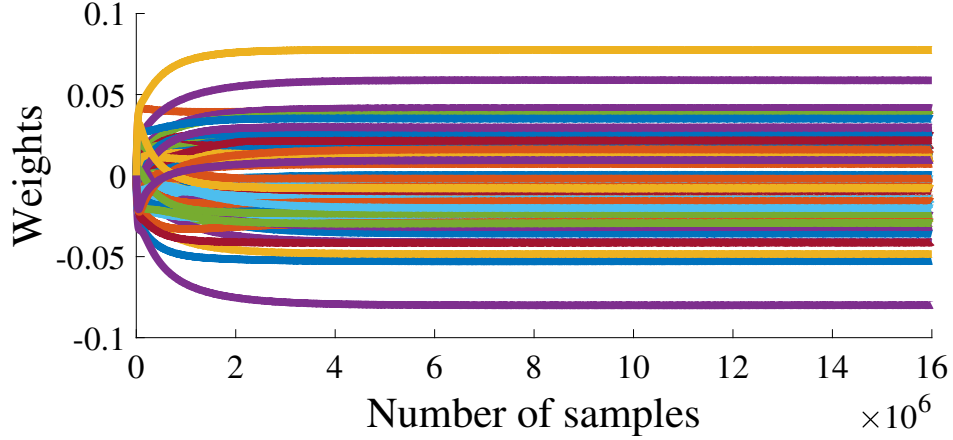


Figure 5.14 Convergence of PAF_{ds} 's coefficients (for the desired element) when a 4-tone sine-wave input and the fixed-point Simulink model are used.

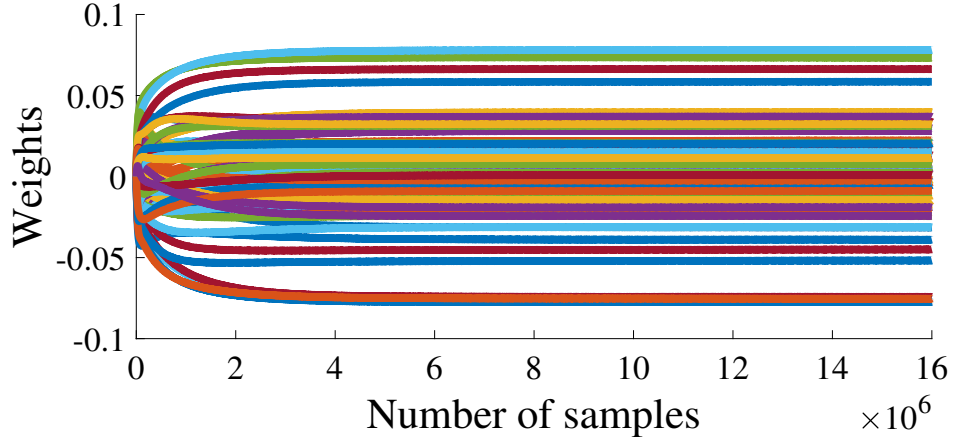


Figure 5.15 Convergence of PAF_{er} 's coefficients (for the error element) when a 4-tone sine-wave input and the fixed-point Simulink model are used.

three cases. The failure rate is also 0.2 % for the three cases. As reported in [56], all the correlation-based estimation approaches (e.g., [7–9]), including our proposed method, fail to converge with some specific frequencies [56]. This failure rate is not specific to the proposed technique.

5.5 Discussions and Comparison

As mentioned earlier, the proposed all-digital polyphase source separation mechanism separates the desired samples of the input signal from timing skew mismatch error, E_{er} . Our method adapts and develops the approach proposed in [63], and implements it with a polyphase decomposition approach to relieve the speed requirements of the filters used. The

Table 5.3 Stability Analysis Results

Case	Timing-Skew Standard Deviation (%)	SNDR $Mean_{d_{indc}}$ (dB)	SNDR $Mean_{d_{acc}}$ (dB)	Average SNDR Improvement (dB)	SNDR improved (%)	SNDR degraded (%)	Failure (%)
Case 1	$\sigma_{tm} = 10$	24.29	60.14	35.84	99.2	0.8	0.2
Case 2	$\sigma_{tm} = 5$	28.99	65.93	36.99	99.2	0.8	0.2
Case 3	$\sigma_{tm} = 2.5$	35.19	68.14	32.94	99	1	0.2

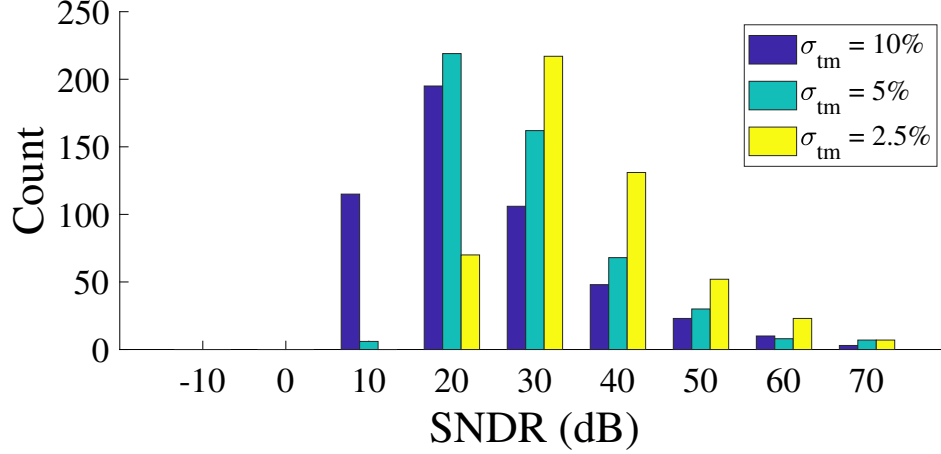


Figure 5.16 Stability analysis: the digital output of the TI-ADC.

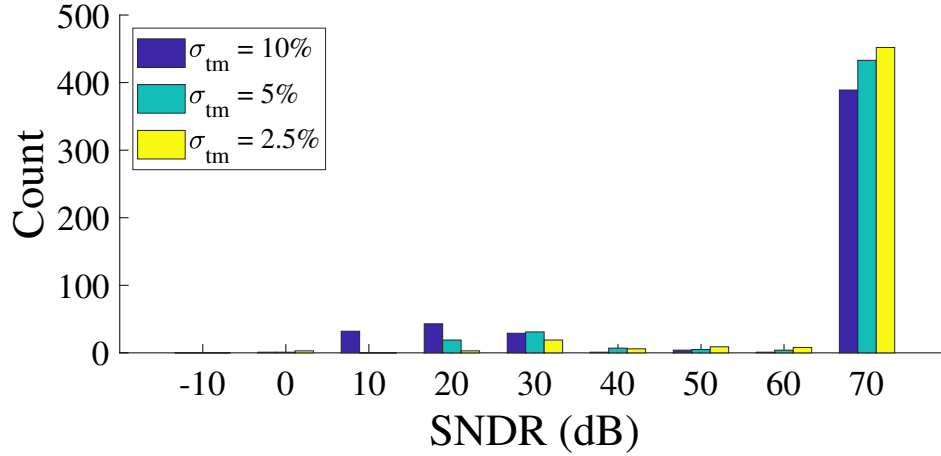


Figure 5.17 Stability analysis: Compensated output obtained with the proposed method.

proposed polyphase implementation relieves the operating speed requirements since the two PAFs only need to operate at speed on the embedded sub-ADC channels.

Table 5.4 compares the proposed technique with existing leading all-digital methods. This table shows that the proposed technique does not require extra sub-ADC(s) compared to [22, 27, 28]. Unlike the techniques reported [5, 6, 46], the entire Nyquist range of the input frequency is usable with the proposed technique. Likewise, as in the methods reported in [4, 6, 7, 25], our method is restricted to the special number of channels due to its use of the

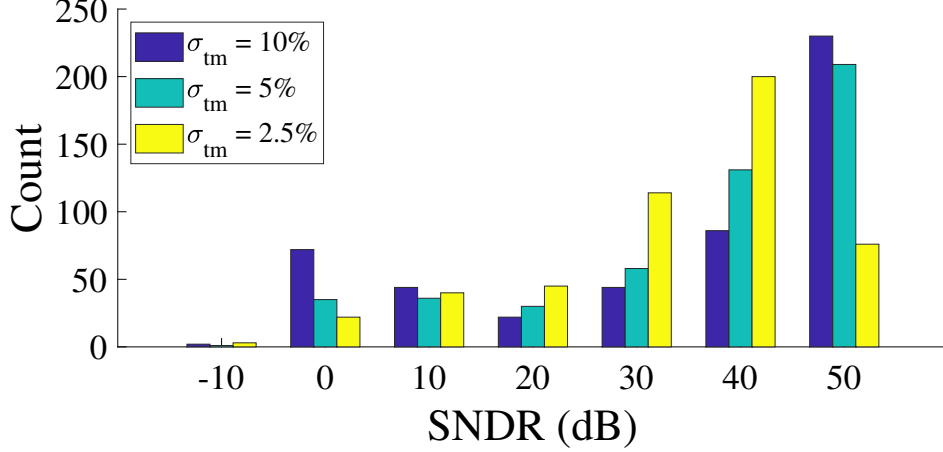


Figure 5.18 Stability analysis: improvement obtained with the proposed method.

Table 5.4 Comparison with compatible methods

	This work (Cases 1/2/3)	[7]	[4]	[6]	[28]	[8]	[25]	[64]	[22]	[5]
Target Resolution (bits)	12	10	10	10	10	11	12	12	14	–
SNDR (dB)	60.14/65.93/68.14	61.9	61.96	58.07	54.2	60	46.61	63.58	72	66
Number of Samples (Iterations)	300k	50k	30k	0.6k	80k	10k	30k	200k	1.5k	80k
Bandwidth Limitation(s)	no	no	yes	yes	no	yes	no	yes	no	yes
Extra sub-ADC(s)	no	no	no	no	yes	no	no	no	yes	no
Number of sub-ADCs	any even value	any even value	2	4	8	any value	4	any value	any value	any value

Hadamard transform. When applied to Cases 2 and 3, our technique shows a better SNDR than other techniques (except for the technique in [22]). Note that the method reported in [22] needs an extra sub-ADC that modifies TI-ADCs architecture, whereas the proposed method does not. To summarize, the proposed method is the best choice for target applications that use the whole Nyquist range. It also does not require modifying the TI-ADC architecture. All the correlation-based estimation approaches (e.g., [7–9]), including our proposed method, fail to converge with some specific frequencies as reported in [56]. This failure rate is not specific to the proposed technique.

As noted before, the proposed method needs two polyphase adaptive FIR filters (PAF_{ds} and PAF_{er}) to retrieve the input signal’s desired samples and remove the error element, E_{er} , (arising from the timing-skew mismatches). The length of the polyphase filters must be selected according to the number of tones in the input signal. In this paper, FL is set to 15 based on an applied 4-tone input signal. The proposed technique eliminates the errors in the compensated digital output by tuning the PAFs. This contrasts with previously reported all-digital and mixed-signal methods that estimate timing skews and compensate them in the analog or digital domains. Unlike competitive techniques, our technique also avoids introducing any delay in the compensation path.

5.5.1 Reliability of the Simulation Results

The proposed fully digital technique’s behavioral simulations and FPGA implementations are notable, as the proposed method is independent of the TI-ADC architecture and its analog circuits. For this reason, the results obtained in this paper are reliable enough to confirm its good performance and applicability compared to mixed-signal methods that depend on the analog TI-ADC architecture and its embedded analog circuits.

In well-designed TI-ADCs, PVT manifests as offset, gain, and timing-skew mismatches and thermal noise. Since the behavioral model of TI-ADC in Simulink is used for the simulations, only the impact of PVT leading to thermal noise and sampling time skews is modeled. The other impacts (i.e., offset and gain mismatches) are neglected to focus on compensating the timing-skew mismatches. The independence of the offset and gain mismatches from the timing-skew mismatch is notable, as the offset and gain mismatches are introduced by inherent random internal mismatches among SADCs, in contrast to the timing skews raised by clocking circuits and paths. For this reason, offset and gain mismatches must be independently calibrated ahead of using timing-skew compensating mechanisms [48, 49, 71]. Like all previously reported approaches, our approach is also susceptible to offset and gain mismatches (e.g., [4, 7, 16, 20, 28, 28, 48, 49, 71]). Accordingly, these mismatches must be estimated and compensated before using our method.

5.5.2 Implementation of the Proposed Method

It is also worth noting that even though the behavioral simulations were performed assuming an FPGA target implementation, our results easily transpose to ASIC platforms as the proposed method is fully digital and operates independently of the architecture and circuit design of TI-ADCs. As reported earlier, the proposed digital compensation method can be implemented on FPGA to operate on real-time data faster than a conventional processor could do. The resulting implementation costs were already reported in Table 5.2. In addition, since timing skews are expected to vary slowly with time (e.g., due to temperature drifts), the coefficients needed for the proposed method can be discovered using an LMS built-in Software/Firmware. Most state-of-the-art TI-ADCs have built-in memory for testing and calibration; hence, the proposed polyphase source separation method can take advantage of these memories without additional hardware costs. Furthermore, the proposed technique can be fully synthesized offline in software, where operation on real-time traffic is not necessary (e.g., test applications).

5.5.3 Operation Rate of the Proposed Method

The proposed technique's hardware implementation can operate as fast as any other competing technique, mainly relying on the CMOS technology used. The resulting operating frequency from these codes does not represent the proposed method's real operating speed potential, since obtaining HDL codes from the Simulink model is not optimal. Nevertheless, this approach is instrumental in fast prototyping and demonstrating the proposed method's potential.

As mentioned earlier, our Simulink models assumes that the TI-ADC's sampling frequency to 1 Hz for simplicity. According to the timing report of the Xilinx Vivado Design Suite [55], the compensation engine of the proposed method can operate at a maximum rate of 78 MHz when the design is programmed on the Xilinx Virtex-7 VX690T FPGA implemented with a 28 nm CMOS technology. The proposed architecture would function much faster if this compensation machine were embedded in an ASIC implemented using state-of-the-art technology (3 nm TSMC) [57].

5.5.4 Modulation Operation and the Number of Sub-ADCs

The present paper has established a basis for timing-skew compensation by exploiting polyphase source separation and the modulation mechanism. Although this paper used the Hadamard transform as the modulation mechanism due to its Hardware implementation simplicity, the modulation operation can be realized by a complex frequency shifts approach, similar to the modulation mechanism in [5], $\mathbf{m}(n)$, to remove the restriction imposed by the Hadamard transform. For the single-rate realization of the proposed approach, the required estimates of $M - 1$ images of the input signals are created by a set of $M - 1$ modulating complex-value signals, $e^{jn(i/M)}$, as follows

$$d_{md,i}(n) = d_{tiadc}(n) \times e^{jn(i/M)}, \quad i = 0, \dots, M - 1. \quad (5.15)$$

In this case, the modulated signals, $d_{md,i}(n)$, are complex values, which makes the AFIR filters operate with complex-value signals. In this case, the hardware complexity increases by a factor of two since the modulating signals, $e^{jn(i/M)}$, need to be implemented by sine and cosine operations as $\sin(n(i/M)) + j\sin(n(i/M))$ [5]. For the polyphase realization of the proposed technique, the modulation matrix of size $(M - 1) \times M$ by the modulated signals,

$d_{md,i}(n)$, are given by

$$\begin{bmatrix} e^{j/M} & e^{j2/M} & \dots & e^{j(M-1)/M} \\ e^{j2/M} & e^{j4/M} & \dots & e^{j(M-1)2/M} \\ \vdots & \vdots & \ddots & \vdots \\ e^{j(M-1)/M} & e^{j2(M-1)/M} & \dots & e^{j(M-1)(M-1)/M} \end{bmatrix}. \quad (5.16)$$

In polyphase format, the hardware complexity also increases by a factor of two.

5.5.5 Power Consumption and Hardware Complexity of Adaptive Filters

The power consumption of the multipliers in the adaptive filters is evaluated and compared with the power consumption of FIR filters with constant coefficients since the proposed source separation technique is based on adaptive filters, in contrast to most of the present techniques developed using FIR filters with constant coefficients.

As depicted in Fig. 5.19, a B -bit multiplier needs a chain of B -bit adders. In this design, the input data, $\{d_{i,msb}, \dots, d_{i,lsb}\}$, is multiplied with the weight, $\{w_{msb}, \dots, w_{lsb}\}$, to generate the B -bit output, $\{d_{o,msb}, \dots, d_{o,lsb}\}$. Since the coefficients of the adaptive filters in the proposed method depend on the input signal and the random timing skews, the bits of the coefficients, $\{w_{msb}, \dots, w_{lsb}\}$, are also random variables. For this reason, it can be assumed that the probability of the bits $w_i, i = 0, \dots, B-1$, being 0 or 1 is 0.5. Consequently, half of the bits w_i (i.e., $B/2$) are zero (and the other half are one).

In FIR filters with constant coefficients, the adders corresponding to the bits w_i being equal to one are just considered and implemented, and the other $B/2$ adders are ignored. In other words, just $B/2$ adders are required to implement B -bit multipliers. Nevertheless, adaptive FIR filters need to implement all the B adders. If their coefficients continuously vary during the convergence of the proposed method, adaptive filters consume two times more hardware and power than FIR filters. The power consumption after the proposed technique converges is an important consideration since the adders associated with the bits being equal to zero act as buffers, and their activity is restricted to one of their inputs. Therefore, these adders' power consumption is reduced by a factor of three (the carry signals inside the B -bit adders also remain inactive).

In summary, the power consumption of multipliers in adaptive filters during convergence of the proposed method consumes two times more power than their FIR counterpart during convergence, and the proposed source separation method consumes just 33% more power after its convergence. The proposed method with adaptive filters is comparable with some

state-of-the-art techniques mentioned above (e.g., [7, 71]) since the adaptive filters in the proposed method need 15 taps, compared to the reported methods in [7, 71] which uses FIR filters with 25 and 31 taps, respectively.

5.5.6 Future Research

Possible future developments and improvements include optimizing the hardware requirement, adapting the proposed method to operate with wider applications, and exploiting other source separation algorithms.

5.6 Conclusions

This paper proposed a polyphase source separation method to retrieve the desired input signal samples unaffected by the error arising from the timing-skew mismatch in the digital output of TI-ADCs. The proposed all-digital technique categorizes and separates the desired signal and the error, routing them to separate outputs through distinct polyphase adaptive filters (PAFs). The polyphase realization allows our proposed method to operate directly on the sub-ADCs. This polyphase implementation relieves the operating speed requirements, as the two PAFs only need to operate at speed on the embedded sub-ADC channels. Unlike previously reported techniques, our technique avoids introducing any delay in the compensation path. The proposed method is best if all the Nyquist zones must be functional, and it does not use any extra sub-ADC(s). Finally, several behavioral simulations and FPGA implementations are utilized to verify the applicability and performance of our method. The proposed approach enhanced the SNDR mean from 24.29 dB to more than 60.14 dB when the standard deviation of the timing skew was 10 % of the TI-ADC's sampling period.

Acknowledgments

The authors thank Ciena Corporation and the Mathematics of Information Technology and Complex Systems (MITACS) granting agency for their financial support.

5.7 Appendix A: Polyphase Filters

The coefficients of the FIR filter are divided into its polyphase components [8, 39, 46, 52] as

$$FIR(z) = \sum_{k=0}^{M-1} z^{-k} PC_k(z^M) \quad (5.17)$$

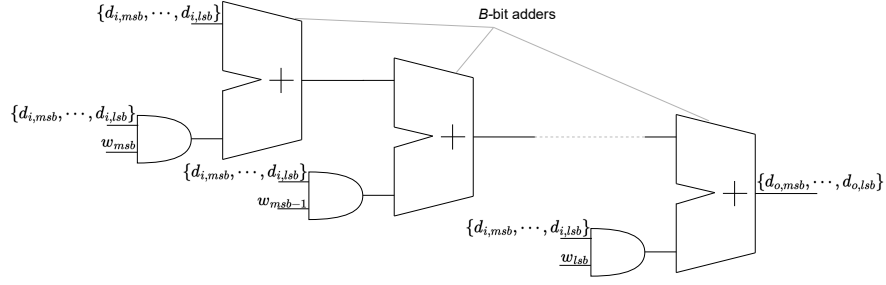


Figure 5.19 Conceptual model of a B -bit multiplier consisting of B -bit adders with B -bit inputs and output.

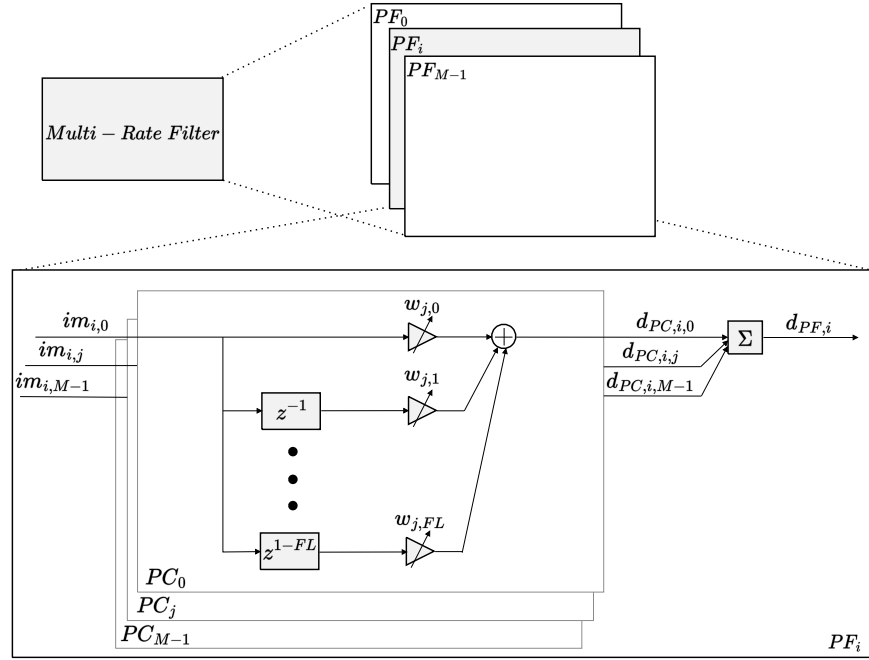


Figure 5.20 Structure of the proposed polyphase filter.

where PC_k denotes the k th polyphase component of the single-rate filter $FIR(z)$. The polyphase implementation requires the polyphase components to create M FIR filters, $\{PF_0(z), \dots, PF_{M-1}(z)\}$, that separately operate on the outputs of the sub-ADCs. The polyphase filter bank format of the single-rate FIR filter $FIR(z)$, expressed, in the vector form, as

$$\mathbf{PF}(z) = \mathbf{IM}(z) \times \mathbf{PC}(z) \quad (5.18)$$

where the vector $\mathbf{PC}(z)$ and the matrix $\mathbf{IM}(z)$ respectively represent the polyphase components and the input matrix expressed as

$$\mathbf{PC}(z) = \begin{bmatrix} PC_0(z) \\ \vdots \\ PC_{M-1}(z) \end{bmatrix}, \quad (5.19)$$

$$\mathbf{IM}(z) = \begin{bmatrix} D_{in,0} & z^{-1}D_{in,M-1} & \dots & z^{-1}D_{in,1} \\ D_{i,1} & D_{in,0} & \dots & z^{-1}D_{in,2} \\ \vdots & \vdots & \ddots & \vdots \\ D_{in,M-1} & D_{in,M-2} & \dots & D_{in,0} \end{bmatrix}. \quad (5.20)$$

The multiplication of i^{th} row of the matrix $\mathbf{IM}(z)$ and the vector $\mathbf{PC}(z)$ in (5.18) specifies the i^{th} polyphase FIR filter, $i = 0, \dots, M-1$. Each FIR filter includes all the components PC_k , but their order in each FIR filter differs. For example, the component PC_1 obtains the last input, D_{M-1} , as its input in the first FIR filter, while it receives the first input, D_0 , as its input in the second FIR filter. Fig 5.20 depicts an example of the polyphase FIR filter consisting of M filters, $\{PF_0(z), \dots, PF_{M-1}(z)\}$. The outputs of these filters are denoted as $\{d_{PF,0}(z), \dots, d_{PF,M-1}(z)\}$. The outputs of the M polyphase components $\{d_{PC,i,0}(z), \dots, d_{PC,i,M-1}(z)\}$ are added to create the output of i^{th} filter $i = 0, \dots, M-1$.

CHAPTER 6 ARTICLE 4 : DIGITAL COMPENSATION OF TIMING-SKEW MISMATCHES IN TI-ADCS WITH ADAPTIVE POLYPHASE FILTERS

In this chapter, the article entitled "*Using polyphase adaptive filters for fully digital compensation*" has been submitted to *IEEE Transactions on Signal Processing*. This chapter uses the adaptive FIR filters in feedback loops as a main contribution to remove the errors arising from the timing-skew mismatch in the digital output of the TI-ADC. Moreover, the proposed approach uses a modulation matrix to detect errors. The polyphase decomposition realizes the proposed mechanism approaches to relieve the speed requirement of the proposed technique. The proposed method performs its compensation task without the need for additional SADC(s) and without manipulating the TI-ADC's structure. Also, it can operate in almost all the Nyquist range. The proposed technique avoids introducing any delay.

Using polyphase adaptive filters for fully digital compensation

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6.1 Abstract

This paper uses polyphase adaptive FIR filters and a modulation matrix to propose a novel fully digital timing-skew mismatch compensation approach for time-interleaved analog-to-digital converters (TI-ADCs). The proposed method uses the digital compensated output vector to reconstruct the error resulting from the timing-skew mismatches with polyphase adaptive FIR filters in the feedback path together with a Hadamard transform as the modulation operation, and it subtracts the reconstructed error vector from the TI-ADC digital output to generate the compensated vector signal. Thus, our technique mitigates the timing-skew mismatch error by tuning the weights of the polyphase adaptive filters without introducing any delay between the digital output of the sub-ADCs and the compensated output vector, unlike previous competitive methods. This paper also proposes a tuning mechanism for the polyphase adaptive filters. The polyphase realization allows our method to operate directly on the sub-ADCs, resulting in an operating speed reduction by a factor of M (i.e.,

the number of sub-ADCs), thus relieving the requirements on the polyphase adaptive FIR filters. This method operates without any additional sub-ADCs and without modifying the architecture of TI-ADC, and it does not impose constraints on the Nyquist frequency range. Extensive behavioral simulations using MATLAB/Simulink, the Vivado Design Suite, and Field-Programmable Gate Array (FPGA) implementations validate the proposed method's performance. Our technique enhances the signal-to-noise and distortion ratio (SNDR) from 22.97 dB to 68.6 dB in a 12-bit TI-ADC when the standard deviation of timing-skew is set to 10 % of the sampling period of the TI-ADC. These results indicate that our method exhibits a better SNDR than almost all other competitive techniques.

6.2 Introduction

This paper proposes a novel fully digital technique for reconstructing the error (resulting from the timing-skew mismatch) and generating the compensated vector signal by subtracting the reconstructed error from the digital output of the TI-ADC. For the first time, the proposed technique uses the compensated output vector and feeds them, in the *feedback* path, to polyphase adaptive FIR (PAF) filters and a modulation operation, realized by the Hadamard transform. For this reason, the proposed method avoids introducing *any delay between* the digital output of SADCs and the compensated output vector. It must be noted that the polyphase approach has been widely used for decades [47] and used to relieve the speed requirement of filters in digital compensation of timings-skew mismatch for TI-ADCs [8, 46]. Therefore, the proposed polyphase realization permits our method to operate directly on the SADCs. This polyphase implementation relieves the operating rate requirements as the PAF filters are only required to operate at the speed of the SADC channels. In contrast to previous competitive methods, which compensate for the errors arising from the TI-ADC timing-skew mismatch by derivative operation implemented by FIR filter in the *feed-forward* path (or by VDLs in analog domains), our technique mitigates the timing-skew mismatch error by tuning the weights of the PAF filters *feedback* path. This paper also proposes a tuning mechanism for the polyphase adaptive filters. The proposed technique allows using the entire Nyquist frequency range, in contrast to the methods reported in [5, 6, 21]. Our method exhibits a better SNDR than other competitive methods (except for the method proposed in [22]). However, the technique reported in [22] needs an additional SADC calling for manipulation to TI-ADCs architecture, while our technique does not. Like the reported technique in [7], it limits the number of SADC(s) to specific numbers. The proposed mechanism operates during the regular data conversion function of the TI-ADC. Our technique is fully implementable on-chip or field-programmable-gate-array (FPGA) operating independently of TI-ADC design

and analog circuits, unlike [22, 27, 28].

The paper is structured as follows. Section 6.3 briefly explains the system model of TI-ADCs. Section 6.4 explains the proposed method. Section 6.5 provides the simulation results, which are discussed and compared in Section 6.6. Section 6.7 concludes the paper by summarizing our main contributions.

6.3 System Model Of TI-ADC

This section begins by describing the effect of timing-skew mismatch on the performance of TI-ADCs. The theoretical background and implementation of the proposed technique are then explained in Section 6.4. Fig. 6.1 shows the architecture of TI-ADC consisting of multiple SADCs as mentioned above. In the absence of PVT variation, the SADCs are identical ADCs, having the sampling rate of F_s/M , where F_s represents the overall sampling rate of the TI-ADC and the same effective resolution, B . The TI-ADC operates based on a clock pattern. According to this pattern, k^{th} SADC samples with the shifted sampling edges as kT_s , $k = 0, \dots, M-1$, where the sampling interval, T_s , is the reciprocal of the sampling rate (i.e., $1/F_s$) [23, 70]. This clock pattern causes the TI-ADC to sample the input signal, v_{in} , at intervals of T_s seconds. The outputs of the SADCs, after being multiplexed, create the TI-ADC digital output [23, 41].

Random PVT variations result in *offset*, *gain*, and *sampling-time skew* mismatches among SADCs, appearing as remarkable causes of the effective resolution degradation of TI-ADCs. To mitigate these effects, mismatch sources must be estimated and corrected. This paper supposes the offset and gain mismatches are compensated and mitigated by other means [20, 23]. Dealing with timing skew mismatches, after offset and gain mismatch are corrected, is commonly adopted in the literature [4, 7].

Firstly, the effects of timing-skew mismatch are described. As seen from Fig. 6.1, the k^{th} SADC samples the input signal as

$$v_{s,k}(m) = v_{in}(m \times MT_s - kT_s + \tau_k) \quad (6.1)$$

where $k = 0, \dots, M-1$, while τ_k and m represent k^{th} timing skew and the discrete-time index (corresponding to the operating frequency of F_s/M) [23, 73]. It is straightforward to show that [8, 21, 22, 68], the k^{th} sampled input signal, by the Taylor series, can be approximated as

$$v_{s,k}(m) \approx v_{in}(mMT_s - kT_s) + \tau_k \frac{dv_{in}(mMT_s - kT_s)}{dt}. \quad (6.2)$$

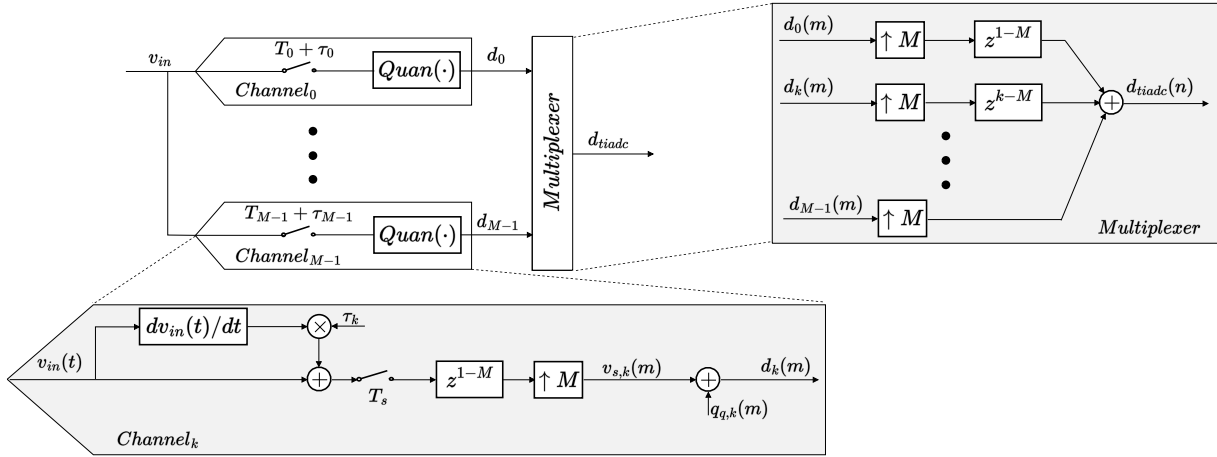


Figure 6.1 Structure of a typical time-interleaved ADC (TI-ADC).

Ideally, the outputs of the SADCs, d_k , $k = 0, \dots, M - 1$, are digital values that reflect the input signal subject to quantization errors introduced by the quantization process [23]. Notably, the quantization error is ignored in this section for presentation simplicity, but all the simulations are performed considering the quantization error in Section 6.5. However, the quantization error is ignored to focus on the proposed technique in the rest of the paper.

This paper uses capital letters for the frequency-domain equivalents of time-domain signals. The k^{th} digital output, in the frequency domain, is expressed as

$$D_k(e^{j\omega}) = \frac{1}{M} \sum_{i=0}^{M-1} e^{-jk(\frac{\omega}{M} - \frac{2\pi i}{M})} V_{in}(e^{j(\frac{\omega}{M} - \frac{2\pi i}{M})}) \times (1 + j\tau_k(\frac{\omega}{M} - \frac{2\pi i}{M})) \quad (6.3)$$

where $k = 0, \dots, M - 1$. In the above equation, the k^{th} digital output, D_k , contains the input signal and its derivative and associated $M - 1$ images. The derivative and its images appear as orthogonal terms to the input signal and its images [23]. The TI-ADC utilizes multiplexing operation to create its digital output, D_{tiadc} , from the outputs of the SADCs. Multiplexing operation in the frequency domain can be expressed as up-sampling of the SADCs' outputs by M and then delaying the results by $M - k$ (in the frequency domain, $= e^{-j(M-k)\omega}$), for $k = 0, \dots, M - 1$, as

$$D_{u,k}(e^{j\omega}) = \frac{e^{-j(M-k)\omega}}{M} \sum_{i=0}^{M-1} e^{-jk(\omega - \frac{2\pi i}{M})} \times V_{in}(e^{j(\omega - \frac{2\pi i}{M})}) (1 + j\tau_k(\omega - \frac{2\pi i}{M})) \quad (6.4)$$

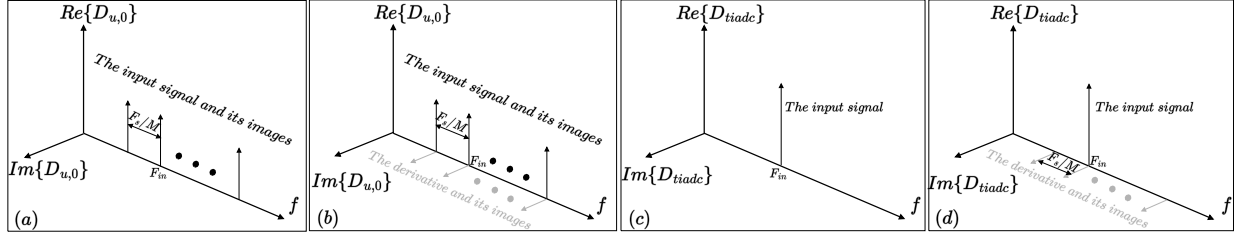


Figure 6.2 PSDs of the digital output of first SADC after being up-sampled and TI-ADC. (a): up-sampled output of first SADC without sampling time-skew, (b): up-sampled output of first SADC with sampling-time skew, (c): the ideal part of the digital output of the TI-ADC, (d): the digital output of the TI-ADC corrupted with sampling-time skews, (in this figure, the phase circulation is ignored for presentation simplicity).

where $k = 0, \dots, M - 1$. The sum of all the signals $D_{u,k}$ for $k = 0, \dots, M - 1$ provides the digital output of the TI-ADC [23]. As an example, Figs. 6.2(a) and 6.2(b) respectively depict the power spectrum density (PSD) of the first SADC digital output, after being up-sampled, without and with sampling time skew. The digital output in the frequency domain is presented as

$$D_{tiadc}(e^{j\omega}) = C_{ds}(e^{j\omega}) + C_{er}(e^{j\omega}) \quad (6.5)$$

where C_{ds} and C_{er} respectively denote the desired component (depicting the desired samples of the input signal) and the error component (introduced by the sampling-time skew mismatch) as

$$\begin{aligned} C_{ds}(e^{j\omega}) &= \frac{e^{-jM\omega}}{M} \sum_{i=0}^{M-1} \left\{ \sum_{k=0}^{M-1} e^{-jk\frac{2\pi i}{M}} \right\} V_{in}(e^{j(\omega - \frac{2\pi i}{M})}), \\ C_{er}(e^{j\omega}) &= \frac{e^{-jM\omega}}{M} \sum_{i=0}^{M-1} C_{er,i}(e^{j\omega}) V_{in}(e^{j(\omega - \frac{2\pi i}{M})}) \\ &\quad j(\omega - \frac{2\pi i}{M}) \end{aligned} \quad (6.6)$$

where $C_{er,i}$ is the i^{th} image of the input signal expressed as follows

$$C_{er,i}(e^{j\omega}) = \sum_{k=0}^{M-1} \tau_k e^{-jk\frac{2\pi i}{M}}. \quad (6.7)$$

It can be shown that [39],

$$\sum_{k=0}^{M-1} e^{-jk\frac{2\pi i}{M}} = \frac{1 - e^{-jk2\pi i}}{1 - e^{-jk\frac{2\pi i}{M}}} = \begin{cases} M, & i = 0, \\ 0, & i \neq 0. \end{cases} \quad (6.8)$$

For this reason, the desired component of the digital output of the TI-ADC can be represented as

$$C_{ds}(e^{j\omega}) = e^{-jM\omega} V_{in}(e^{j\omega}). \quad (6.9)$$

All the images disappear except for the input signal in the expression above [23]. Notably, the term $e^{-jM\omega}$ in (6.9) represents the delay of M in the digital output. Nevertheless, the same is not valid for the terms $C_{er,i}$, $i = 0, \dots, M-1$, because the timing skews are random, in essence, with different values [23]. Figs. 6.2(c) and 6.2(d) respectively depict the digital output of the TI-ADC, d_{tiadc} , without and with the presence of timing skew mismatches. In these figures, the phase circulation is ignored for presentation simplicity. The digital output, d_{tiadc} , includes the component C_{ds} , and the timing skew mismatch appears as the images $C_{er,i}$ in the digital output. As its target, the proposed method aims to reconstruct C_{er} to purify D_{tiadc} from the error.

6.4 Proposed Polyphase Adaptive Compensation

The proposed compensation technique aims to reconstruct the error component iteratively, c_{er} , (arising from the timing-skew mismatch) by a set of polyphase adaptive filters (together with modulation operation). It generates the compensated digital output, d_{cp} , by removing the reconstructed error component from the TI-ADC digital output. For simplicity, the basic concept of the proposed technique is first presented in an abstract single-rate version, as shown in Fig. 6.3 (a). Afterward, the polyphase realization of our method is explained in detail. Fig. 6.3 (a) depicts the proposed approach that uses modulation operation to generate course estimates of the error terms from the compensated signal, d_{rc} . The modulated signals, $\{d_{md,1}, \dots, d_{md,M-1}\}$, are applied to AFIR filters to reconstruct the errors introduced by the timing-skew mismatch, d_{rc} . The AFIR filters also need the compensated digital signal, d_{cp} , to evaluate the error terms and remove them by properly tuning their coefficients. As mentioned earlier, the proposed method uses adaptive FIR filters in the *feedback* path to *avoid introducing any delay* in contrast to current techniques based on FIR filters (with constant coefficients) in the *feed-forward* path, for instance, [5, 7–9].

The proposed method uses the Hadamard transform, similar to [7], for the modulation operation due to its simple hardware implementation, as following

$$D_{md,i}(z) = D_{tiadc}(z) * md_i(z) \quad (6.10)$$

where $md_i(\cdot)$ represents the i^{th} modulating signal, $i = 1, \dots, M-1$, (i.e., the i^{th} row of the Hadamard matrix of order M). The compensated digital signal, d_{cp} , is fed to the adaptive

FIR (AFIR) filter input. Modulation by the Hadamard transform results in efficient hardware implementations. The modulated signals have all the $M-1$ images. The AFIR filters $AFIR_i$, $i = 1, \dots, M-1$, respectively, acquire the modulated signals, $d_{md,i}$, $i = 1, \dots, M-1$, as shown Fig. 6.3 (a). The reconstructed error signal, targeting to estimate the error component, c_{er} , can be expressed as follows

$$D_{rc}(z) = \sum_{i=1}^{M-1} AFIR_i(z) \times D_{md,i}(z). \quad (6.11)$$

Also, the compensated signal is generated by subtracting the reconstructed error signal, $D_{rc}(z)$, from the TI-ADC digital output as

$$D_{cp}(z) = D_{tiadc}(z) - D_{rc}(z). \quad (6.12)$$

The adaptive filters $AFIR_i$, $i = 1, \dots, M-1$, must be tuned such that the compensated digital signal, d_{cp} , becomes uncorrelated to the reconstructed error signal, d_{rc} . In this case, the set of AFIR filters perfectly reconstructs the error in the digital output of TI-ADC. On the other hand, the adaptive filters $AFIR_i$, $i = 1, \dots, M-1$, aims to purify the error component, c_{er} , from the compensated signal, d_{cp} .

In our approach, the coefficients of the AFIR filters can be adjusted by the least-mean-square (LMS) algorithm to the values that minimize the energy signal defined as

$$\xi_{cp} = E(d_{cp}^2). \quad (6.13)$$

The minimization of this energy signal mitigates the error terms, $c_{er,i}$, $i = 0, \dots, M-1$, in the compensated signal, d_{cp} . It also ensures the orthogonality between the compensated signal, d_{cp} , and the error components, c_{er} . The LMS machine minimizes the energy signal by iteratively adjusting the filters $AFIR_i$, $i = 0, \dots, M-1$. In the LMS algorithm, the derivatives of the energy signal direct the AFIR filters to the minimum of the energy signal [72]. These derivatives for each coefficient, called the update steps, could be expressed as

$$\delta w_{i,l} = \frac{d\xi_{cp}}{dw_{i,l}} \quad (6.14)$$

where $l = 1, \dots, FL$, and $w_{i,l}$ denotes the weights of the i^{th} filter $AFIR_i$, while FL represents the number of taps of these AFIR filters, as shown in Fig. 6.3 (b). By substituting (6.12)

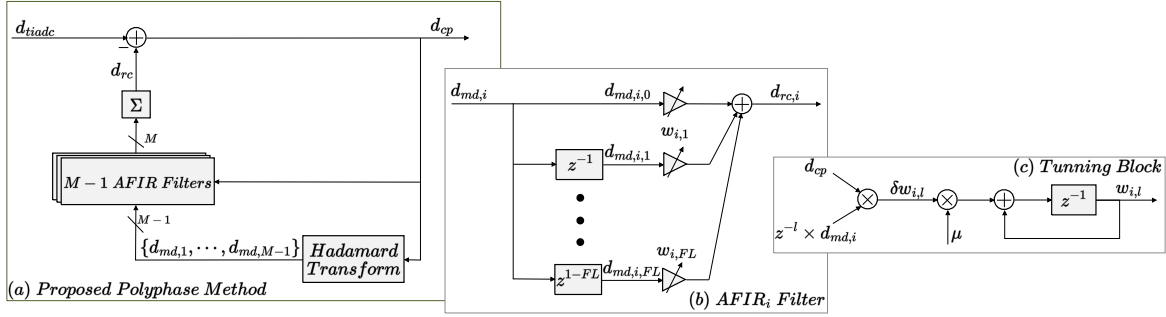


Figure 6.3 (a): The architecture of the single-rate version of the adaptive compensation method. (b): The i^{th} adaptive filter. (c): The tuning block that adjusts the weight $w_{i,l}$.

into (6.14), the update steps can be expressed as

$$\delta w_{i,l}(n) = d_{md,i}(n-l) \times d_{cp}(n) \quad (6.15)$$

where n denotes the discrete-time index (corresponding to the operating frequency of F_s). The LMS algorithm could tune these weights to steer the AFIR filters towards the minimum energy. As shown in Fig. 6.3 (c), the update expressions of the LMS algorithm could be given by

$$w_{i,l}(n+1) = w_{i,l}(n) + \mu \times \delta w_{i,l}(n) \quad (6.16)$$

where $l = 1, \dots, FL$, while the factor μ represents the update rate. The orthogonality between d_{cp} and $d_{md,i}$, $i = 0, \dots, M-1$, denotes the convergence of the coefficients in (6.16) and making the mean of the update steps zero. The proper choice of μ ensures the stability of the AFIR filters. The stability margin of the LMS machine could be enhanced by reducing μ at the expense of decreasing the convergence rate of the LMS algorithm [51, 72].

6.4.1 Polyphase Implementation of the Proposed Method

Thus far, the basis of our target proposed polyphase method is established. The main disadvantage of the approach mentioned above relies on its high operation rate requirement, as it works on the digital output of the TI-ADC at the sampling frequency of F_s . Implementing the abovementioned method by polyphase decomposition approach causes a significant reduction in the operation speed to F_s/M since the polyphase format of the proposed method directly operates on the outputs of SADCs. Fig. 6.4 shows the structure of the proposed method in its polyphase realization. Based on the single-rate format, the proposed polyphase method also uses modulation operation to reconstruct the error raised by the timings-skew mismatch from the compensated vector signal, $\mathbf{D}_{cp} = \{D_{cp,0}, \dots, D_{cp,M-1}\}$.

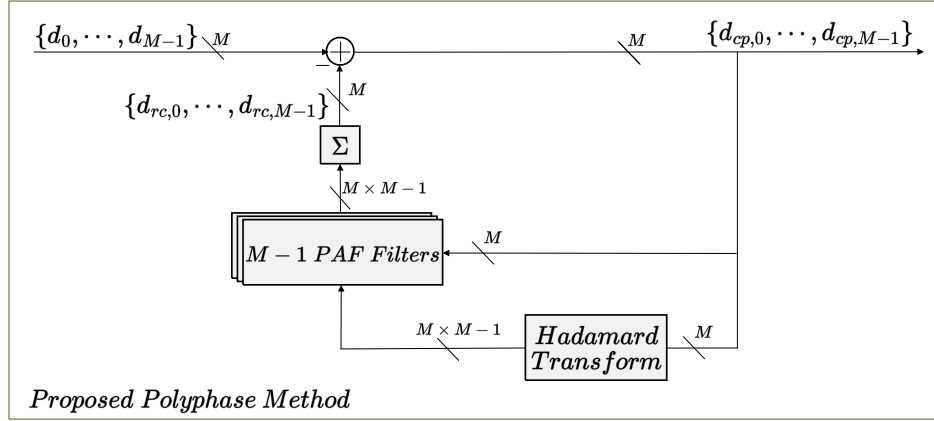


Figure 6.4 The architecture of the polyphase version of the adaptive compensation method.

The modulated vector signal, $\mathbf{D}_{\text{md},i}$, $i = 1, \dots, M-1$, are respectively applied to the set of $M-1$ PAF filters, $\mathbf{PAF}_i$, $i = 1, \dots, M-1$ to reconstruct the errors introduced by the timing-skew mismatch, $\mathbf{D}_{\text{rc}} = \{D_{\text{rc},0}, \dots, D_{\text{rc},M-1}\}$. The i^{th} modulated vector signal, $\mathbf{D}_{\text{md},i} = \{D_{\text{md},i,0}, \dots, D_{\text{md},i,M-1}\}$, is generated by the product of the compensated vector signal, $\mathbf{D}_{\text{cp}}$, with the i^{th} column of the Hadamard transform as

$$\mathbf{D}_{\text{md},i} = \mathbf{D}_{\text{cp}} \times \mathbf{HT}_i \quad (6.17)$$

where $\mathbf{HT}_i$ stands for the i^{th} column of the Hadamard transform. The PAF filters also need the compensated vector signal to evaluate the error terms and remove them by properly tuning their coefficients.

For the polyphase implementation of our technique, the basics of the polyphase realization and the concept of dividing the coefficients of an AFIR filter into its polyphase version is presented [8, 41, 46, 52] as

$$AFIR(z) = \sum_{k=0}^{M-1} z^{-j} PE_k(z^M) \quad (6.18)$$

where PE_k represents the k^{th} polyphase element of $AFIR(z)$. The polyphase realization needs these polyphase elements to assemble different M adaptive FIR filters in a PAF filter, which individually process the outputs of the SADCs. Similar to the single-rate format mentioned above, the outputs of the polyphase filter bank, representing the reconstructed error signal, are expressed as

$$\mathbf{D}_{\text{rc}}(z) = \sum_{i=1}^{M-1} \mathbf{D}_{\text{PAF},i}(z) \quad (6.19)$$

where the output vector comprises the signals $\{D_{\text{rc},0}(z), \dots, D_{\text{rc},M-1}(z)\}$, while $\mathbf{D}_{\text{PAF},i}(z)$

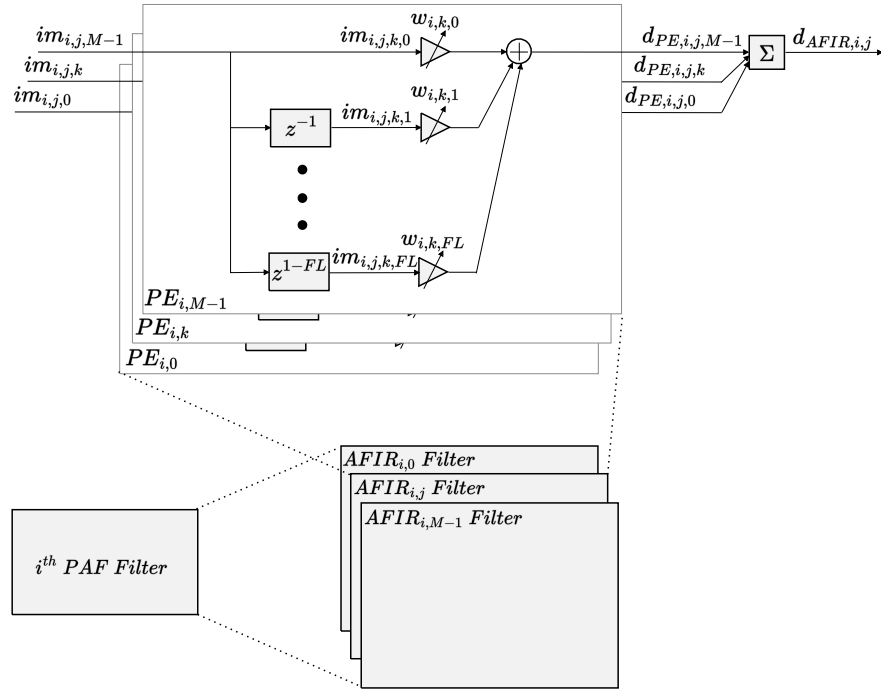


Figure 6.5 The structure of the i^{th} PAF filter, $i = 1, \dots, M - 1$.

denotes the output vector of the i^{th} PAF filter, consisting of the M outputs of its adaptive FIR filters, expressed as

$$\mathbf{D}_{\text{PAF},i}(z) = \begin{bmatrix} D_{AFIR,i,0}(z) \\ \vdots \\ D_{AFIR,i,M-1}(z) \end{bmatrix}. \quad (6.20)$$

The i^{th} PAF filter can also be represented as

$$\mathbf{D}_{\text{PAF},i}(z) = \mathbf{IM}_i(z) \times \mathbf{PE}_i(z) \quad (6.21)$$

where the vector $\mathbf{PE}_i(z)$ and the matrix $\mathbf{IM}_i(z)$ respectively denote the output vector of the i^{th} PAF filter and input matrix defined as

$$\mathbf{PE}_i(z) = \begin{bmatrix} PE_{i,0}(z) \\ \vdots \\ PE_{i,M-1}(z) \end{bmatrix}, \quad (6.22)$$

and

$$\mathbf{IM}_i(z) = \begin{bmatrix} D_{md,i,0} & z^{-1}D_{md,i,M-1} & \dots & z^{-1}D_{md,i,1} \\ D_{md,i,1} & D_{md,i,0} & \dots & z^{-1}D_{md,i,2} \\ \vdots & \vdots & \ddots & \vdots \\ D_{md,i,M-1} & D_{md,i,M-2} & \dots & D_{md,i,0} \end{bmatrix}, \quad (6.23)$$

where $D_{md,i,j}$, $i = 1, \dots, M-1$, $k = 0, \dots, M-1$, denote the modulated signals created by the modulation matrix from the outputs of SADCs. Therefore, the PAF filters receive the modulated signals through the input matrices $\mathbf{IM}_i$ of the size $M \times M$, $i = 1, \dots, M-1$, as their inputs. Multiplying each row of the input matrix, $\mathbf{IM}_i$, by the polyphase element vector, $\mathbf{PE}_i$, in (6.21) defines a unique FIR filter within a PAF filter. From (6.21), it is also clear that the j^{th} adaptive FIR filter inside the i^{th} PAF filter, $AFIR_j$ $j = 1, \dots, M-1$, is formed by multiplying the j^{th} row of the i^{th} input matrix, $\mathbf{IM}_i$, and the i^{th} polyphase component vector, $\mathbf{PE}_i$. Therefore, the output of the j^{th} adaptive FIR filter inside the i^{th} PAF filter, $j = 1, \dots, M-1$, is given by

$$D_{AFIR,i,j}(z) = \mathbf{IM}_{i,j}(z) \times \mathbf{PE}_i(z). \quad (6.24)$$

Each adaptive FIR filter, within a PAF filter, has all the elements $PE_{i,k}$, $k = 0, \dots, M-1$, but the order of the elements is determined according to (6.23). Therefore, the order of elements in each FIR filter is different. In this arrangement, the polyphase element $PE_{i,1}$ receives $D_{md,i,0}$ in the first FIR filter as its input, whereas it acquires $D_{md,i,1}$ as the input in the second FIR filter. The vector of compensated signals is expressed as follows

$$\mathbf{D}_{cp}(z) = \mathbf{D}(z) - \mathbf{D}_{rc}(z). \quad (6.25)$$

The polyphase adaptive filters aim to remove the error terms for generating the desired vector signal, $\mathbf{D}_{cp}$.

In the i^{th} PAF filter, $i = 1, \dots, M$, the LMS machine iteratively adjusts the weights of the polyphase elements, $PE_{i,k}$, $k = 0, \dots, M-1$. This paper proposes a tuning mechanism for the polyphase adaptive filters. The proposed technique individually adjusts the polyphase elements, $PE_{i,k}$. In the i^{th} PAF filter, the element $PE_{i,k}$ contributes to all the M FIR filters while acquiring M different inputs (from the matrix $\mathbf{IM}_i$). Consequently, all the M replicas of the element $PE_{i,k}$ must contribute to the gradual adjustments of its coefficients. Based on the LMS algorithm, the energy signal associated with the element $PE_{i,k}$ is thus defined

as the sum of all its associated energy signals as

$$\xi_{cp,PE_{i,k}} = \sum_{j=0}^{M-1} E(d_{PE_{i,j},k}^2), \quad k = 0, \dots, M-1 \quad (6.26)$$

where $d_{PE_{i,j},k}$ stands for the output of the element $PE_{i,k}$. The LMS algorithm defines the update steps of the weights as

$$\delta w_{i,k,l}(m) = \frac{d\xi_{cp,PE_{i,k}}}{dw_{i,k,l}}, \quad (6.27)$$

for $i = 1, \dots, M-1$, $k = 0, \dots, M-1$, and $l = 1, \dots, FL$. From (6.26) and (6.27), the update steps can be represented as

$$\delta w_{i,k,l}(m) = \sum_{j=0}^{M-1} im_{i,j,k}(m-l) \times d_{cp,k}(m) \quad (6.28)$$

for $k = 0, \dots, M-1$. This equation can be presented as

$$\delta w_{i,k,l}(m) = \mathbf{D}_{cp}(z) \cdot z^{-l} \mathbf{IM}_{i,\bar{j}}(z) \quad (6.29)$$

where $\mathbf{IM}_{i,\bar{j}}$ shows the j^{th} column of the i^{th} input matrix. Moreover, as shown in Fig. 6.6, the update equations adjusting the k^{th} polyphase element, $k = 0, \dots, M-1$, inside the i^{th} PAF filter, $k = 1, \dots, M-1$, are given by

$$w_{i,k,l}(m+1) = w_{i,k,l}(m) + \mu \times \delta w_{i,k,l}(m) \quad (6.30)$$

where μ denotes the update rate. This parameter ensures the PAF filters' stability, as with the single rate format expressed before. Thus, the operation rate of the PAF filters is $1/M$ th of the TI-ADC sampling rate (the same as the operating rate of the SADCs). Therefore, the polyphase implementation exhibits almost the same dynamic power dissipation as its single-rate format. The value of the factor μ must be determined carefully to ensure stability while providing a good convergence speed of the polyphase filters, similar to the single-rate counterpart [51, 72]. Eventually, the number of taps for the PAF filters must be specified according to the required bandwidth and the number of SADCs as is the case with the single-rate version, as discussed in Section 6.6.

6.5 Simulations

Several simulations using MATLAB/Simulink, Vivado Design Suite, and FPGA designs derived from the functional models verify and evaluate the performance and applicability of our method. The behavioral model used for the TI-ADC consists of four identical 12-bit SADCs.

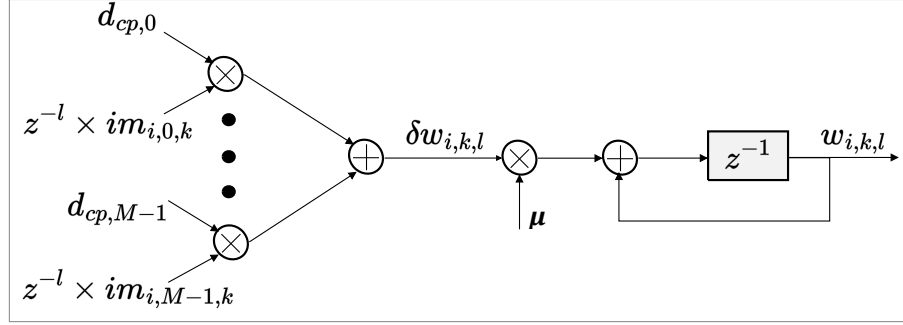


Figure 6.6 The LMS update block diagram adjusting the k^{th} polyphase element, $k = 0, \dots, M-1$, inside the i^{th} PAF filter, $i = 1, \dots, M-1$.

Notably, the effective resolution of the SADCs is restricted to 12 bits by both thermal noise and quantization error, and in this model, the sampling rate of TI-ADC, F_s , is normalized to *one*. Also, the timing skew of each channel is generated randomly and independently with Gaussian distribution. The standard deviation of the randomly generated timing-skew skews is set to 0.1 (i.e., 10 % of the TI-ADC's sampling interval). The update rate factor, μ , is set to 2^{-12} to ensure the convergence of our method. The length of the polyphase filters, FL , is set to 10.

In these simulations, Fast Fourier Transforms (FFTs) of size N_{fft} measure and evaluate the performance of the proposed technique. Input signals comprising N_{fft} samples are applied to the TI-ADC to avoid spectral leakage. The frequency of the input tones, F_{in} , is translated to the bin index of I_{bin} in FFTs as $F_s \times I_{bin}/N_{fft}$. The input tone frequency specified by I_{bin} is used in all the simulations. Notably, I_{bin} values are selected as prime numbers to avoid repetitive patterns in the input tone(s), to make the TI-ADC quantization errors spectrum uniform, and to prevent spectral leakage in the FFT bins for measurement purposes at the TI-ADC output and the compensated output [53, 54]. For all the simulations, N_{fft} is set to 2^{B+1} ($= 2^{13}$).

First, the impact of word width on the performance of the proposed technique is evaluated to select the optimum word width in terms of the signal-to-noise-and-distortion ratio (SNDR) and hardware expense. A single-tone sine wave with its associated I_{bin} is selected as the input signal. Corresponding to each word width, 563 simulation runs are performed by sequentially selecting prime numbers in the range $\{1, \dots, N_{fft}/2\}$ as I_{bin} , and the SNDRs are collected to calculate the mean of SNDRs. Table 6.1 shows the results with different word widths.

In the following simulations, our technique is implemented on an FPGA to verify the syn-

Table 6.1 Impact of Word Width

Word Width (bits)	14	15	16	17	18
$Mean_{SNDR}$ (dB)	63.93	67.01	68.69	69.27	69.45
σ_{SNDR} (dB)	3.62	4.08	4.85	4.84	4.7

thesizability of the Simulink model, evaluate the hardware requirement of the proposed technique, and compare the results from the Simulink fixed-point model and FPGA. The Xilinx Virtex-7 VX690T realized on 28-nm technology is utilized for implementations. The VX690T series of Xilinx Virtex-7 includes 2800 digital signal processing (DSP) slices and 485k logic cells. The Simulink fixed-point model of the proposed technique is first converted to Verilog HDL codes by the Simulink HDL Coder [55]. Then, the MATLAB FIL Wizard and Vivado Design Suite synthesize and implement these codes on FPGA. The transfer rate via the JTAG protocol for communicating is 12.5 MHz. Table 6.2 depicts the hardware cost of FPGA implementation corresponding to different word widths. As reported in Table 6.1, the SNDR mean improves when the word width grows from 14 to 16 bits. However, the SNDR shows negligible improvement beyond 16 bits. The hardware and power consumption expenses expand with extending word width, as depicted in Table 6.2. Therefore, a 16-bit word width is adopted to provide a good trade-off between the SNDR performance and hardware cost.

The following simulations evaluate the convergence of the PAF filters and the PSD of the digital output, d_{tiadc} , and the compensated signal, d_{cp} , with single- and 8-tone sine-wave inputs. The TI-ADC, modeled in Simulink with floating point precision, is used with both the FPGA implementation and the fixed-point Simulink model of the proposed technique for this part. First, a single-tone sine wave is used as the input signal of the TI-ADC with its associated bin index $I_{bin} = 2781$. Figs. 6.7 and 6.8 respectively depict the PSD of the TI-ADC digital output, d_{tiadc} , and the compensated signal, d_{cp} , by using the proposed method. Almost all harmonics in the TI-ADC digital output, d_{tiadc} are significantly attenuated in the compensated signal, d_{cp} . As shown in these figures, the results of the fixed-point Simulink model and its FPGA implementation of the proposed method also coincide, thus validating the synthesizability of the Simulink model. Also, Figs. 6.9 and 6.10 respectively show the convergence of the SNDR and PAF filters. Our proposed method improves the SNDR from 22.57 dB to 70.5 dB, and it also converges with $30k$ samples and remains stable after convergence.

Moreover, the TI-ADC for the case of the 8-tone sine-wave input signal with its corresponding bins $I_{bin} = \{166, 404, 642, 1117, 1355, 1592, 1830\}$ is evaluated. The TI-ADC, modeled in

Table 6.2 Hardware Cost

Word Width (bits)	14	15	16	17	18
Lookup Tables (%)	4.15	4.35	4.29	4.78	5.04
Flip Flops (%)	0.41	0.42	0.44	0.46	0.47
DSP Slices (%)	15	15	15	15	15

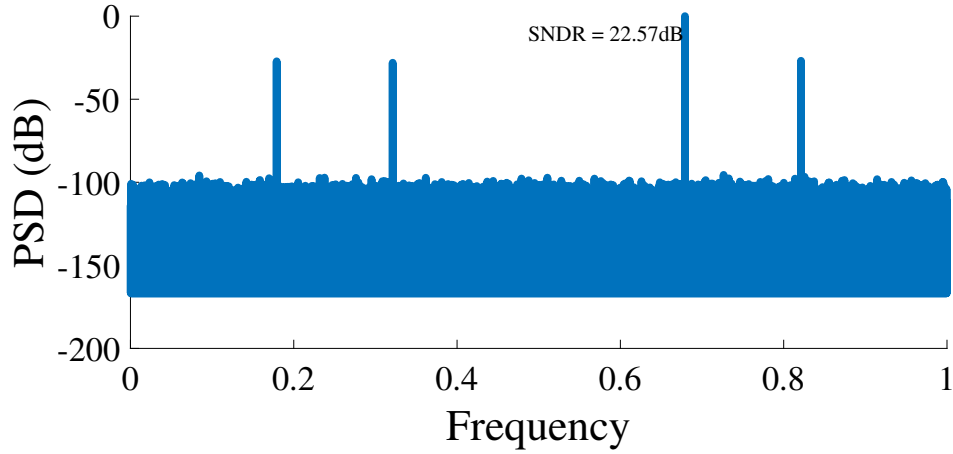


Figure 6.7 PSD of the TI-ADC output, d_{tiadc} , corresponds to a single-tone sine-wave when the digital output of TI-ADC, modeled in Simulink, is not compensated.

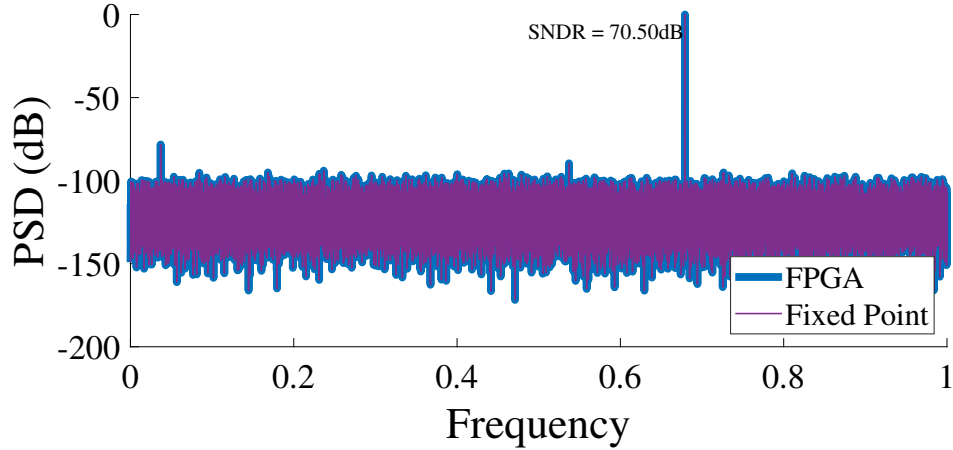


Figure 6.8 PSD of the compensated output, d_{cp} , obtained with the fixed-point Simulink model and the derived FPGA implementation when the input is a single-tone sine-wave after the convergence of the compensation method.

Simulink with floating point precision, is again utilized with the FPGA implementation and the fixed-point Simulink model of the proposed technique in this part. Figs. 6.11 and 6.12 respectively depict the PSDs of the digital output, d_{tiadc} , and the compensated signal, d_{cp} , after convergence. These figures show that almost all harmonics of d_{tiadc} are

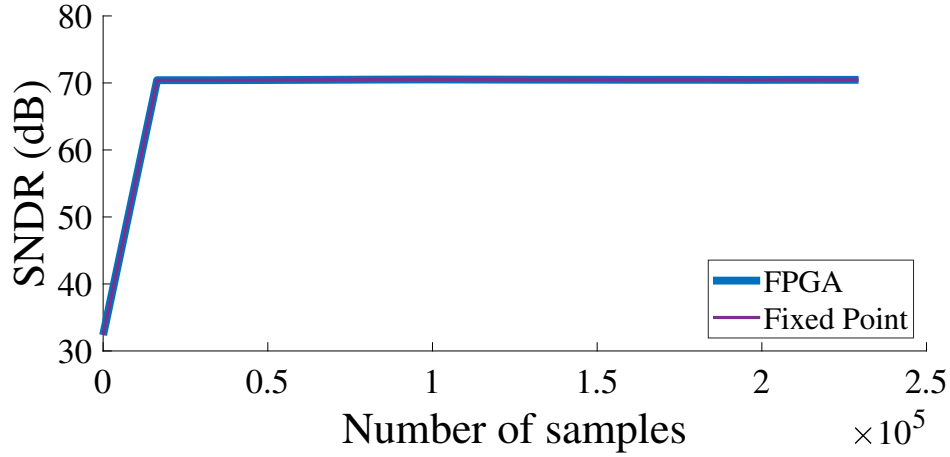


Figure 6.9 SNDR convergence when the input is a single-tone sine-wave observed with the compensated TI-ADC Simulink model and its derived FPGA implementation.

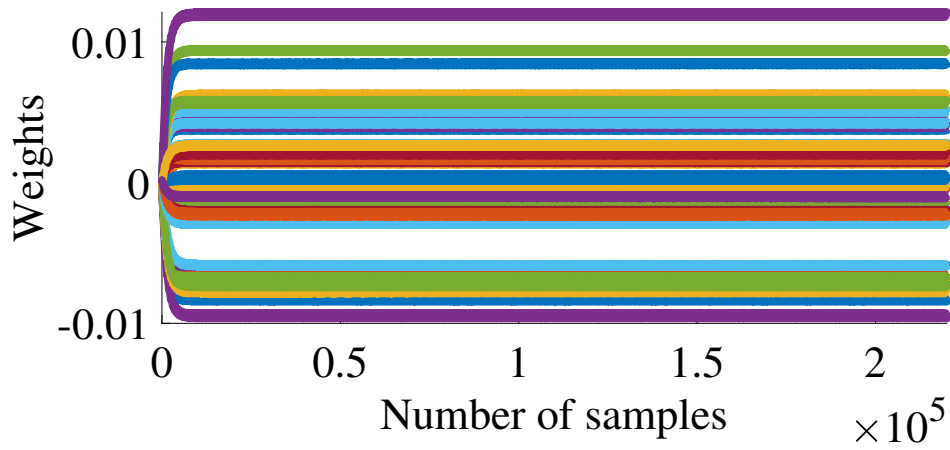


Figure 6.10 Convergence of *PAF*'s coefficients with the fixed-point Simulink model corresponding to a single-tone sine-wave.

extremely attenuated in d_{cp} . As shown in these figures, the results of the fixed-point Simulink model and its FPGA implementation of the proposed method also coincide, confirming the synthesizability of the proposed method's Simulink model. Figs. 6.13 and 6.14 indicate the convergence of the SNDR and PAF filters, respectively. These figures indicate that our technique converges after utilizing approximately 4×10^6 samples, and the SNDR is enhanced from 24.32 dB to 63.74 dB.

Finally, Monte Carlo simulations examine the proposed method's stability in three cases of frequency variation of the single-tone sine wave (as the input signal) and random timing skews. For each case, a set of 500 separate simulation runs is collected. In these cases, the timing-skew standard deviation is set to 20 %, 10 %, and 5 % of the TI-ADC's sam-

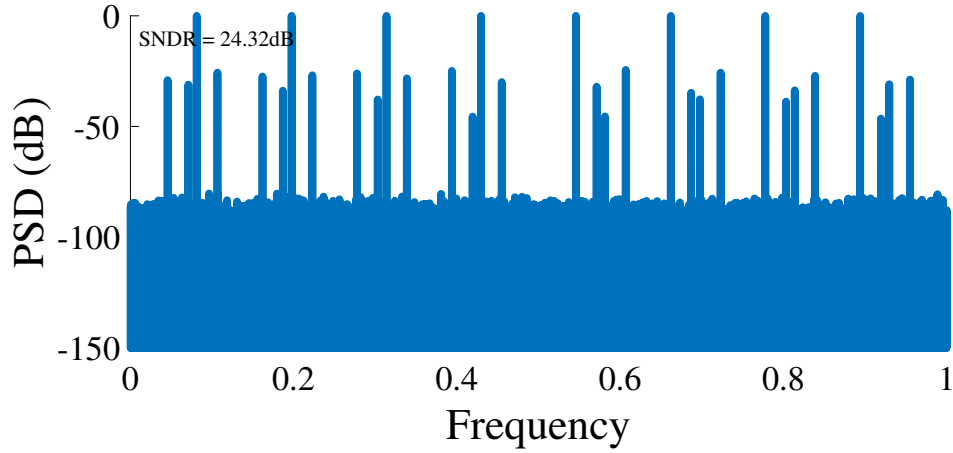


Figure 6.11 PSD of the TI-ADC output, d_{tiadc} , corresponds to an 8-tone sine-wave when the digital output of TI-ADC, modeled in Simulink, is not compensated.

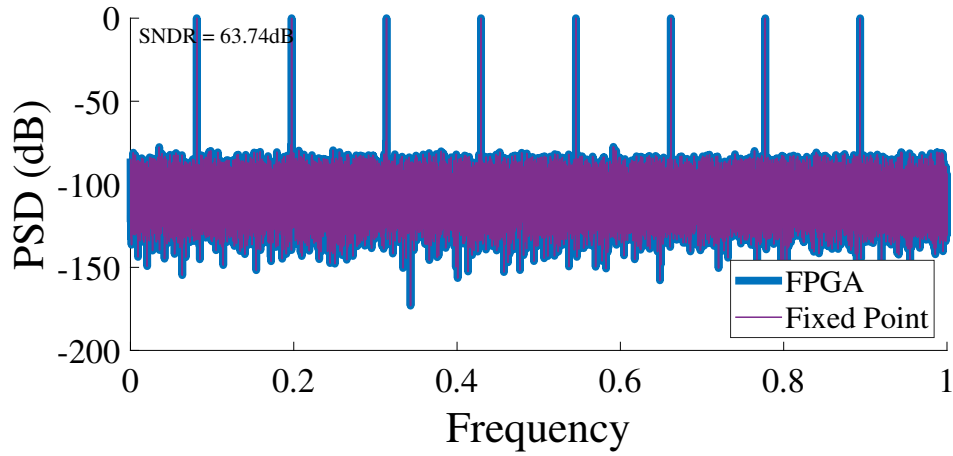


Figure 6.12 PSD of the compensated output, d_{cp} , corresponds to an 8-tone sine-wave when the TI-ADC Simulink model is compensated with both the fixed-point Simulink model and FPGA implementation.

pling interval. The bin index, I_{bin} , is a randomly generated prime number for each separate simulation run. Also, the random timing skews of the SADCs are *generated independently with Gaussian distribution*. Figs. 6.15, 6.16, and 6.17 respectively depict the outcomes of the stability analysis of the TI-ADC digital output, d_{tiadc} , the compensated signal, d_{cp} , and the improvement by our proposed method. The improvement is defined as the SNDR difference between the compensated signal and the TI-ADC's digital output (i.e., $SNDR_{improve} = SNDR_{d_{cp}} - SNDR_{d_{tiadc}}$). Moreover, Table 6.3 shows more results about this part of the simulation. In this table, the *SNDR improved* is defined as the rate at which SNDRs of the compensated signal are greater than the SNDRs of the TI-ADC digital output.

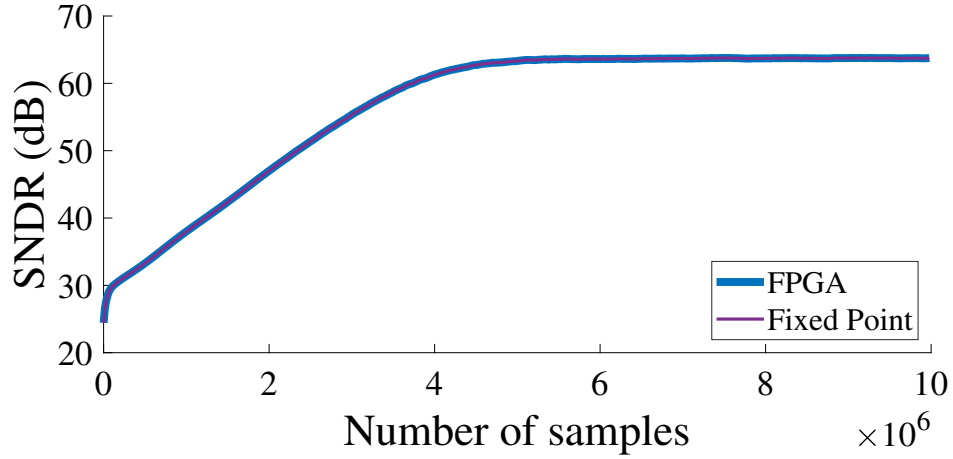


Figure 6.13 SNDR convergence corresponds to an 8-tone sine-wave when the TI-ADC Simulink model is compensated with the fixed-point Simulink model and its derived FPGA implementation.

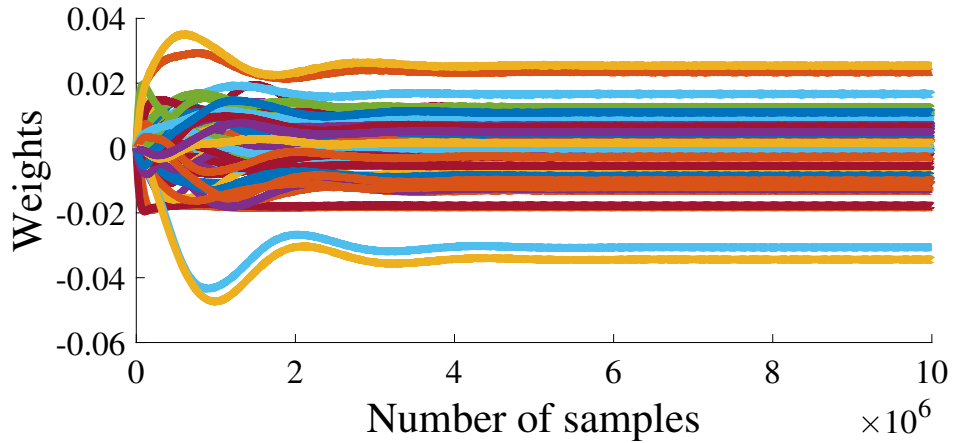


Figure 6.14 Convergence of *PAF*'s coefficients with the fixed-point Simulink model corresponding to an 8-tone sine-wave when the TI-ADC Simulink model is compensated.

The *SNDR degraded* is defined as the rate at which SNDRs of the compensated signal are smaller than the SNDRs of the TI-ADC digital output. Also, the failure rate is the divergence percentage of the proposed technique. For the three cases, the mean of the collected SNDRs is respectively enhanced from 16.98 dB to 67.98 dB, from 22.97 dB to 68.6 dB, and from 28.78 dB to 68.97 dB when the proposed compensation method is applied. The failure rate is insignificant and remains less than 0.2 % for the three cases. It is important to note that this failure rate is not specific to our method. As mentioned earlier, all the estimation mechanism that uses the correlation approach, including our proposed method (e.g., [7–9]) fail to converge with some specific frequencies [56]. This failure rate is not specific to our

proposed method.

6.6 Discussions and Comparison

The proposed all-digital polyphase method aims to alleviate the error introduced by timing skew mismatch in the digital output independent of the analog circuits and design of TI-ADCs. As mentioned earlier, the proposed method uses the compensated output vector to reconstruct the error resulting from the timing-skew mismatches with polyphase adaptive FIR filters in the *feedback* path together with a Hadamard transform as the modulation operation. It subtracts the reconstructed error vector from the digital output of SADCs to generate the compensated digital vector signal. For this reason, the proposed method avoids *introducing any delay* between the digital output of SADCs and the compensated output vector. Unlike previous competitive methods, which compensate for the errors arising from the TI-ADC timing-skew mismatch by derivative operation implemented by FIR filter in the feed-forward path (or by VDLs in analog domains), our technique mitigates the errors by tuning the weights of the PAF filters. This paper proposes a tuning mechanism for the polyphase adaptive filters. The polyphase realization allows the proposed technique to operate directly on the SADCs. Therefore, our polyphase implementation relieves the operating rate requirements of the proposed method since the PAF filters solely need to operate at the speed of the SADC channels. Also, the manipulation of analog circuits is unnecessary in the proposed approach. As mentioned earlier, all the estimation mechanism that uses correlation mechanism, including our proposed method, (e.g., [7–9]) fail to converge with some specific frequencies [56]. This failure rate is not specific to our proposed method.

Table 6.4 compares our proposed method with existing competitive, fully digital techniques. The proposed method does not need additional SADC(s) contrary to [22, 27, 28], as shown in Table 6.4. Almost the whole Nyquist input frequency range is functional in the proposed approach, unlike the methods reported in [5, 6, 46]. Likewise, in some reported methods [4, 6, 7, 25], like with our method due to using the Hadamard transform, the number of channels is restricted. The proposed method exhibits a better SNDR for all three cases than other techniques (except for the technique in [22]). The reported method in [22] needs an extra SADC, while our method does not. Therefore, our method emerges as the best

Table 6.3 Stability Analysis Results

Case	Timing-Skew Standard Deviation (%)	SNDR $Mean_{dtadc}$ (dB)	SNDR $Mean_{dop}$ (dB)	SNDR Improvement (dB)	SNDR Improved (%)	SNDR Degraded (%)	Failure (%)
Case 1	$\sigma_{tm} = 20$	16.98	67.98	51	98.8	1.2	0.2
Case 2	$\sigma_{tm} = 10$	22.97	68.6	45.62	99	1	0
Case 3	$\sigma_{tm} = 5$	28.78	68.97	40.18	97.8	2.2	0

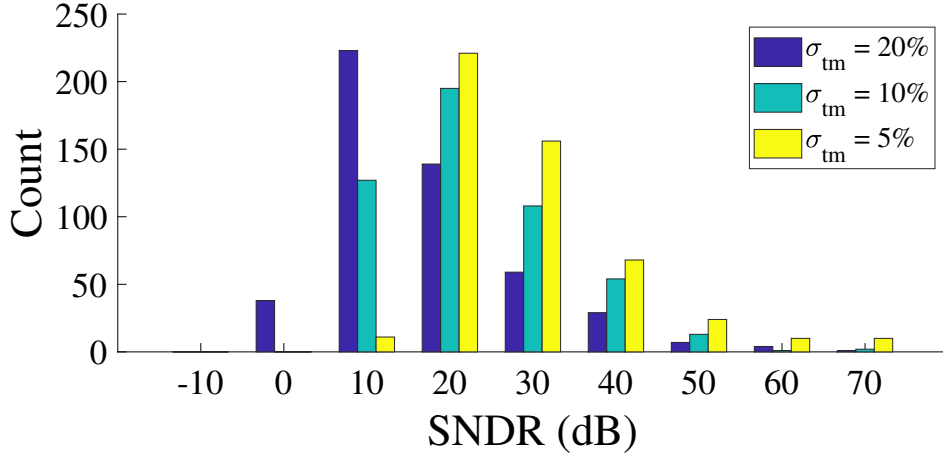


Figure 6.15 Monte Carlo simulations of the TI-ADC digital output, d_{tiadc} , without compensation.

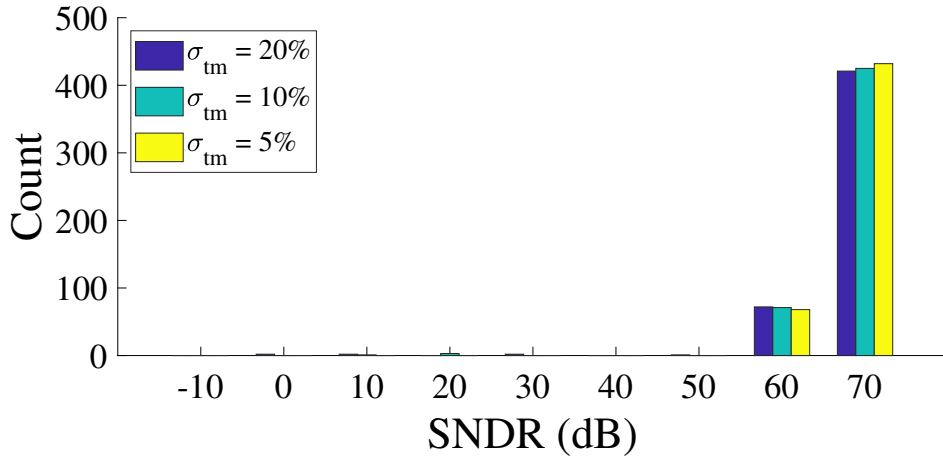


Figure 6.16 Monte Carlo simulations of the compensated digital output, d_{cp} , after convergence of the proposed method.

option for target applications when the entire Nyquist range must be utilized, and the TI-ADC architecture must not be manipulated. Although the PAF filters consume M times more chip area than their single-rate counterpart, optimizing the hardware cost by carefully determining the size of the PAF filters according to the specific application and the number of tones in the input signal is possible.

As mentioned, the proposed technique requires PAF filters to alleviate the error resulting from the timing-skew mismatches in the compensated signal. The size of these filters needs to be selected according to the number of tones in the input signal. For this reason, FL is selected as 10 based on the applied 8-tone input signal.

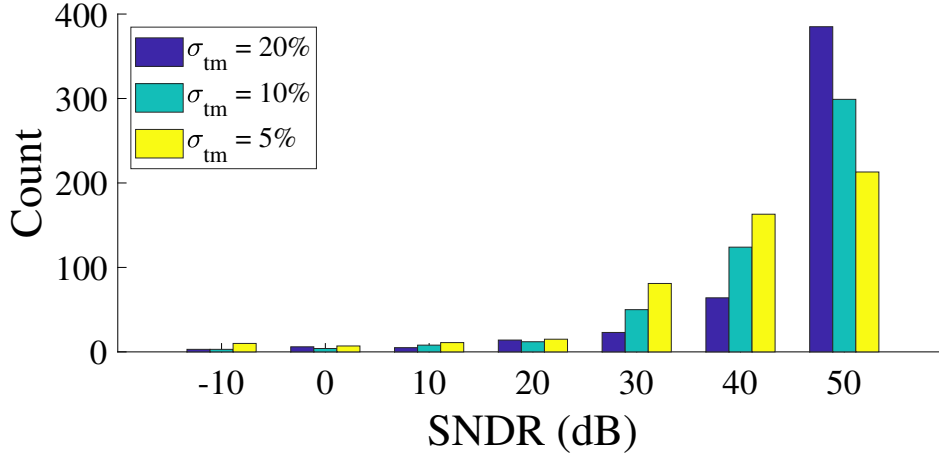


Figure 6.17 Monte Carlo simulations of improvement with the proposed compensation method.

6.6.1 Reliability of the Simulation Results

In contrast to mixed signal calibration techniques depending on the TI-ADC architecture and its analog circuits, the behavioral simulations and FPGA implementations of our fully digital method, independent of the TI-ADC architecture, are notable as these results are reliable enough to verify its performance and applicability.

In well-designed TI-ADCs, PVT manifests as thermal noise and offset, gain, and timing-skew mismatches. In the Simulink behavioral model used to model the TI-ADC, only sampling time skews introduced by PVT variations are considered, and the other impacts (i.e., offset and gain mismatches) are ignored to focus on compensation for the timing-skew mismatches. It is notable that the gain and offset mismatches are introduced by inherent random internal mismatches among SADCs, unlike the timing skews raised by clocking circuits and paths. For this reason, offset and gain mismatches are independent of the timing-skew mismatch and must be calibrated ahead of using timing-skew compensating mechanisms [48–50, 71]. The proposed technique is also sensitive to offset and gain mismatches like most existing methods [4, 7, 48–50, 71]. Therefore, these mismatches must be estimated and compensated before utilizing the proposed technique.

6.6.2 Implementation of the Proposed Method

Although this paper used behavioral simulation with FPGA implementations, the proposed

technique is easily portable to ASIC platforms since our method is fully digital and independent of the TI-ADC design and architecture. As mentioned earlier, the proposed digital compensation technique can be implemented on FPGA to process real-time data faster than a processor could, using the resources already reported in Table 6.2. Moreover, the coefficients needed for the proposed polyphase filters can be determined using an LMS built-in Software/Firmware since timing skews are expected to vary slowly with time (e.g., due to temperature drifts). Most state-of-the-art data converter systems have built-in memory for testing and calibration; hence, the proposed method can take advantage of these memories without any extra hardware cost. Also, in other applications where operating on real-time traffic (e.g., test applications) is unnecessary, the proposed technique can be fully synthesized offline in software.

6.6.3 Operating Rate of the Proposed Method

Although the TI-ADC's sampling frequency was set to 1 Hz in our Simulink models for presentation simplicity, as stated before, the frequency at which the hardware realization of our method operates can be as high as that of any other competing approaches. The maximum operating frequency relies primarily on the CMOS technology node being used. When running on FPGA, the compensation engine implementing the proposed technique can operate at a maximum rate of 78 MHz, based on the timing report of the Vivado Design Suite [55], when targeting the Xilinx Virtex-7 VX690T FPGA implemented with a 28 nm CMOS technology. Indeed, the proposed architecture would function much faster if the proposed technique targeted a modern ASIC implemented in a state-of-the-art technology (such as 3 nm TSMC) [57].

6.6.4 Power Consumption and Hardware Complexity of Adaptive Filters

The proposed method is based on adaptive filters with variable coefficients despite most current methods being developed by FIR filters with constant coefficients. The multipliers in

Table 6.4 Comparison with Similar Methods

	This work (Case 1/Case 2/Case 3)	[7]	[4]	[6]	[28]	[8]	[25]	[64]	[22]	[5]
Target Resolution (bits)	12	10	10	10	10	11	12	12	14	–
SNDR (dB)	67.98/68.6/68.97	61.9	61.96	58.07	54.2	60	46.61	63.58	72	66
Number of Samples (Iterations)	30k	50k	30k	0.6k	80k	10k	30k	200k	1.5k	80k
Bandwidth Limitation(s)	no	no	yes	yes	no	yes	no	yes	no	yes
M (Number of SADCs)	4	8	2	4	8	4	4	4	4	4
Extra SADC(s)	no	no	no	no	yes	no	no	no	yes	no
Limitation on Number of SADCs	2,4,6,...	2,4,6,...	2	4	8	no	4	no	no	no

the adaptive filters with variable coefficients are expected to be the main power consumption overhead. The LMS algorithm can be made inactive to reduce power consumption, similar to the current approaches. For this reason, the power consumption of the adaptive filters should be evaluated and compared with the power consumption of FIR filters.

Fig. 6.18, depicts a B -bit multiplier consisting of a chain of B -bit adders. In this architecture, the input data, $\{d_{i,msb}, \dots, d_{i,lsb}\}$, is multiplied with the weight (i.e., the coefficient), $\{w_{msb}, \dots, w_{lsb}\}$, to create the B -bit output, $\{d_{o,msb}, \dots, d_{o,lsb}\}$. Also, the coefficients' bits, $\{w_{msb}, \dots, w_{lsb}\}$, are random variables since the coefficients of the adaptive filter in the proposed method depend on the random timing-skews and the input signal. For this reason, it can be supposed that the bits w_i $i = 0, \dots, B - 1$ being 0 or 1 has an equal probability of 0.5. Consequently, the bits w_i (i.e., $B/2$) is identical to zero.

In FIR filters, the adders, whose associated input bits w_i are equal to one, are implemented, and the other $B/2$ adders are neglected. Thus, for the implementation of B -bit multipliers, $B/2$ adders are required. However, adaptive FIR filters require the use and implementation of all the B adders. For this reason, adaptive filters consume two times more hardware and power than FIR filters if their coefficients continuously vary during the proposed method's convergence. After the proposed method converges, it is notable that the adders corresponding to the bits w_i equal to zero behave as buffers, since their activity is restricted to one input (notably, the carry signals within the B -bit adders are inactive). In these adders, the power consumption is reduced by three.

In experiments conducted with 3 nm TSMC technology in Cadence Virtuoso to characterize the power consumption of our method, it was found that general complete multipliers consume two times more power than multipliers with constant coefficients before our method's convergence (i.e., with varying coefficients) and 33% more power after convergence (i.e., with stable coefficients). Thus, the proposed method with adaptive filters is comparable with the state-of-the-art techniques mentioned above, with more 33% power overhead.

6.6.5 Future Research

This paper concentrated on developing polyphase adaptive FIR filters with a modulation scheme to estimate and mitigate the errors from the timing-skew mismatch. For this reason, the possible future development and enhancement can be considered *the optimization of hardware resource and power consumption*, implementation on ASIC, and adapting our

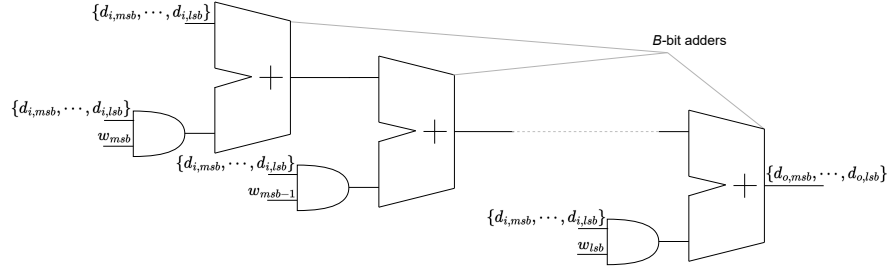


Figure 6.18 Model of a B -bit multiplier comprising of B -bit adders with B -bit inputs and output.

technique to operate with *a broader range of applications*.

6.7 Conclusions

This paper proposed a novel fully digital method using polyphase adaptive FIR (PAF) filters, fed by the compensated digital outputs in the feedback path, to reconstruct the error arising from timing-skew mismatches and to generate the compensated vector signal by subtracting the reconstructed error vector. For this reason, our technique mitigates the timing-skew mismatch error by tuning the weights of the PAF filters without introducing any delay between the digital output of the sub-ADCs (SADCs) and the compensated output vector, in contrast to current competitive techniques. This paper also proposed a tuning mechanism for the polyphase adaptive filters. Our proposed method directly operates on the SADCs by leveraging the polyphase approach. Therefore, this polyphase implementation relieves the functional speed requirement of the proposed method. The proposed approach appears as a reasonable option in case the entire Nyquist zone needs to be functional, and it does not require any extra SADC(s). Finally, various behavioral simulations and FPGA implementation have been used to verify the applicability and performance of our technique. In one of the best cases, the proposed method improved the SNDR mean from 22.57 dB to more than 70.5 dB, while the standard deviation of the timing skew was 10 % of the TI-ADC's sampling interval.

Acknowledgments

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CHAPTER 7 ARTICLE 5 : UTILIZATION OF NOISE-SHAPING IN MIXED-SIGNAL TIMING-SKEW MISMATCH CALIBRATION OF TI-ADCS

This chapter will present the article entitled "*Using a noise-shaping technique to relieve limitation of variable delay lines*" which has been accepted for publication in 2024 IEEE ISCAS. This article attempts to use oversampling and noise-shaping mechanisms to mitigate the effects of the errors resulting from enlarging the minimum step size of VDLs, while avoiding utilizing complex clock routing methods. The proposed method drives the error (raised by increasing the delay steps) outside the operating frequencies. This technique is more effective for noise-shaping TI-ADCS since they are already band-limited. Furthermore, it does not restrict the number of SADCs.

Using a noise-shaping technique to relieve limitation of variable delay lines

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7.1 Abstract

This paper proposes an approach based on oversampling and noise-shaping mechanisms to mitigate the implementation complexity of variable delay lines for mixed-signal calibration of timing-skew mismatch in time-interleaving ADCs. The proposed technique pushes the error (introduced by increasing the delay steps) outside the operating frequencies. Our method is more appropriate for noise-shaping time-interleaved ADCs since they are band-limited. However, the proposed method permits the utilization of either the high-frequency or low-frequency zones. This approach avoids utilizing complex clock routing methods. Also, it does not restrict the number of sub-ADCs. The proposed method is verified by behavioral simulations with MATLAB/Simulink. The mean of the spurious-free dynamic range (SFDR) is respectively enhanced by 11.64 dB and 17.72 dB for the low-frequency and high-frequency zones.

7.2 Introduction

Fully digital and mixed-signal techniques are the main types of calibration. On one hand, fully digital methods are suitable for high-resolution applications due to their insensitivity to PVT variations, but these techniques restrict the sampling rate of the TI-ADC. On the other hand, mixed-signal methods appear as a sensible choice in ultra-high-speed, beyond Giga-Hz, applications. However, these methods typically utilize variable delay lines (VDLs) in the analog domain which makes them sensitive to PVT variations. Consequently, mixed-signal methods are not suitable for high-resolution applications [8, 41]. In comparison with digital-to-analog converters (DACs), VDLs easily provide several delays that can be used to calibrate TI-ADCs. The maximum range of the delays and the delay step (i.e. the difference between two consecutive delays) define the resolution of a given VDL. In addition, accurately controlling many VDLs with sub-ps resolution is challenging.

Randomization approaches have been used to overcome the need for timing-skew mismatch calibration mechanisms [32–34] to mitigate the need for high-resolution VDLs. Nonetheless, these mechanisms are not able to significantly improve the ENOB. Also, randomization of the SADC activation order is challenging and typically requires high-density clock routing. Among various TI-ADC architectures, over-sampling and noise-shaping mechanisms are explored in [35, 36] as means to increase the ENOB without applying any calibration technique. However, some calibration methods are essential when the number of SADCs (channels) is greater than the over-sampling ratio (OSR).

This paper proposes an approach based on oversampling and noise-shaping methods to decrease the harmful impacts of VDLs imperfections for mixed-signal calibration of timing-skew mismatches in TI-ADC. The proposed technique moves the errors (introduced by increasing the delay steps) outside the operating frequencies range by using a finite impulse response (FIR) filter. It is worth noting that our method is more suitable for noise-shaping TI-ADCs since the band of operating frequencies is already restricted in this type of TI-ADCs. Nevertheless, the proposed method permits using either the high-frequency or the low-frequency zones. This approach avoids complex clock routing that was used in previous works [32–34]. In addition, it does not restrict the number of SADCs in contrast to [35, 36].

The paper is structured as follows. Section 7.3 presents the proposed technique. Section 7.4 provides simulation results and a related discussion. Section 7.5 concludes the paper by summarizing our main findings.

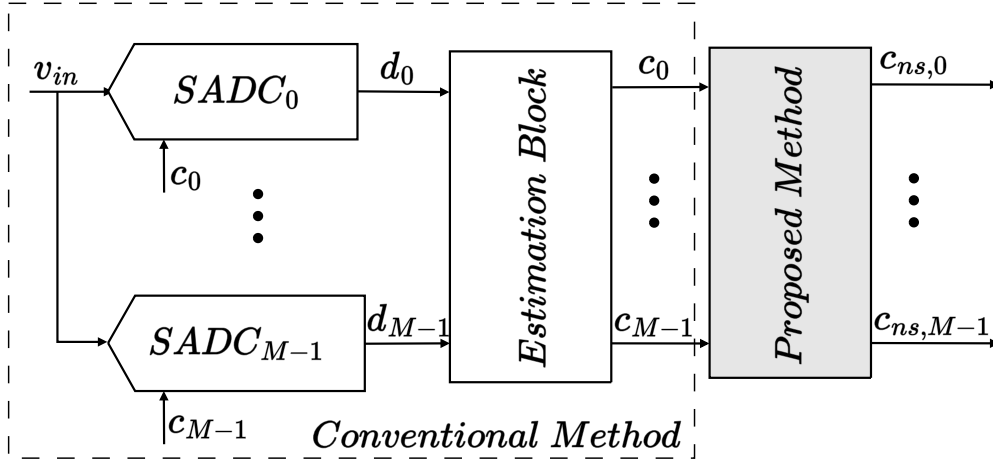


Figure 7.1 Architecture of the mixed-signal estimation mechanism (without and with the proposed method).

7.3 Proposed Method

This section begins by briefly presenting the basics of mixed-signal calibration, and then, it introduces the proposed method together with its theoretical background. Fig. 7.1 shows a model that allows estimating loop parameters applicable to the conventional mixed-signal calibration approaches. In this approach, the estimation loop acquires the digital output of the TI-ADC, d_{out} , estimates the timing-skews, τ_k , $k = 0, \dots, M - 1$, and generates the correction coefficients, c_k , $k = 0, \dots, M - 1$, with B_{vdl} -bit resolution to tune the VDLs with the same resolution. The selection of the delay step, Δ , of the VDLs is worth mentioning as it depends on the desired ENOB of the TI-ADC, B_{tiadc} . Generally, targeting a one-bit higher desired ENOB, B_{tiadc} , reduces the delay step of programmable VDLs Δ by half. The required timing correction range, CR , is also notable as it depends on the variance of the timing skews in a specific TI-ADC. The required resolution of the VDLs, and consequently of the correction coefficients, is expressed as

$$B_{vdl} = \text{ceil}(\log_2(\frac{CR}{\Delta})) \quad (7.1)$$

where $\text{ceil}(\cdot)$ denotes the ceiling operation. In a TI-ADC consisting of an M SADCs, the sampled voltages at the SADCs can be combined and represented by

$$v_s(n) \approx v_{in}(nT_s) + e_{tm}(n) \quad (7.2)$$

where n , T_s , and $e_{tm}(n)$ respectively represent the discrete-time index (corresponding to the TI-ADC's sampling rate, F_s), the sampling time of the TI-ADC (identical to $1/F_s$), and the error element (determined by timing-skew mismatches) expressed as

$$e_{tm}(n) = res_{tm}(n) \times dv_{in}(nT_s)/dt \quad (7.3)$$

where $dv_{in}(\cdot)/dt$ is the derivative of the input signal and $res_{tm}(n)$ is the residual error due to timing skews after convergence of the estimation block expressed as follows

$$res_{tm}(n) = \tau_{[n \bmod M]} - c_{[n \bmod M]} \quad (7.4)$$

where τ_k and c_k respectively denote the k^{th} timing-skew mismatch and k^{th} correction coefficient. Note that (7.3) is valid if and only if the absolute value of the error element $\|e_{tm}\| \ll T_s$. Mixed-signal calibration technique drives the residual error, $res_{tm}(n)$, to zero by estimating the timing-skews, τ_k for $k = 0, \dots, M-1$, and making the correction coefficients, c_k , equal to τ_k for $k = 0, \dots, M-1$. However, the residual error, $res_{tm}(n)$, will never be eliminated since the resolution of the correction coefficients is finite (limited to B_{vdl} -bit). Assuming that the residual $res_{tm}(n)$ is randomly distributed in the range $\{-\Delta/2, \Delta/2\}$, its standard deviation is given by $\sigma_{r-tm}^2 = \Delta/\sqrt{12}$.

Fig. 7.1 also illustrates the proposed method placed in the estimation loop of a conventional mixed-signal calibration method. Our technique obtains the correction coefficients from the estimation block, c_k , $k = 0, \dots, M-1$, and generates their respective noise-shaped format, $c_{ns,k}$, $k = 0, \dots, M-1$ with a reduced width of B_{ns} . In the same context, the noise-shaped coefficients, $c_{ns,k}$, $k = 0, \dots, M-1$, control and adjust the VDLs rather than, c_k , $k = 0, \dots, M-1$. Consequently, the resolution of the VDLs is reduced in proportion to B_{ns} and the delay step of the VDLs in our approach increases to

$$\Delta_{ns} = \frac{CR}{2^{B_{ns}}}. \quad (7.5)$$

The digital output of the TI-ADC, d_{out} , is equivalent to the digital format of the sampled input signal. In our approach, the digital output of TI-ADC after the convergence of the estimation block can be expressed as

$$d_{out}(n) \approx v_{in}(nT_s) + e_{ns}(n) \quad (7.6)$$

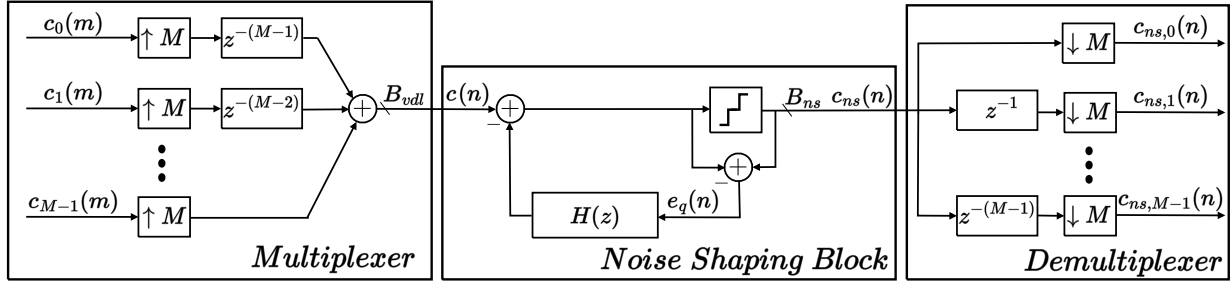


Figure 7.2 Architecture of a model depicting the proposed method.

where $e_{ns}(n)$ represents the noise-shaped error element expressed as

$$e_{ns}(n) = res_{ns}(n) \times dv_{in}(nT_s)/dt \quad (7.7)$$

where $res_{ns}(n)$ denotes the noise-shaped residual error that can be expressed as follows

$$res_{ns}(n) = \tau_{[n \bmod M]} - c_{ns}(n) \quad (7.8)$$

where $c_{ns}(n)$ is the output of the proposed noise-shaping block. The residual error can also be expressed as

$$res_{ns}(n) = ntf(n) * e_q(n) \quad (7.9)$$

where $*$, $ntf(n)$, and $e_q(n)$ respectively denote the convolution operator, the noise transfer function (NTF) of the proposed method, and the error due to the quantization process as shown in Fig. 7.2. In the spectral domain, the digital output, after convergence of the estimation block, can be represented by

$$D_{out}(\omega) \approx V_{in}(\omega) + E_{ns}(\omega) \quad (7.10)$$

where the element $E_{ns}(\omega)$ is given by

$$E_{ns}(\omega) = RES_{ns}(\omega) * j\omega V_{in}(\omega). \quad (7.11)$$

As seen in Fig. 7.2, the noise-shaped error component, $E_{ns}(\omega)$, appears as the frequency convolution between $V_{in}(\omega)$ and the residue $RES_{ns}(\omega)$. Note that we use capital letters for the frequency representation of variables. We can separate the elements $V_{in}(\omega)$ and $E_{ns}(\omega)$ with a proper noise transfer function, $NTF(\omega)$, if oversampling is permitted. In this paper, we target shifting $E_{ns}(\omega)$ over frequency to remove its overlap with the input signal with oversampling and noise-shaping.

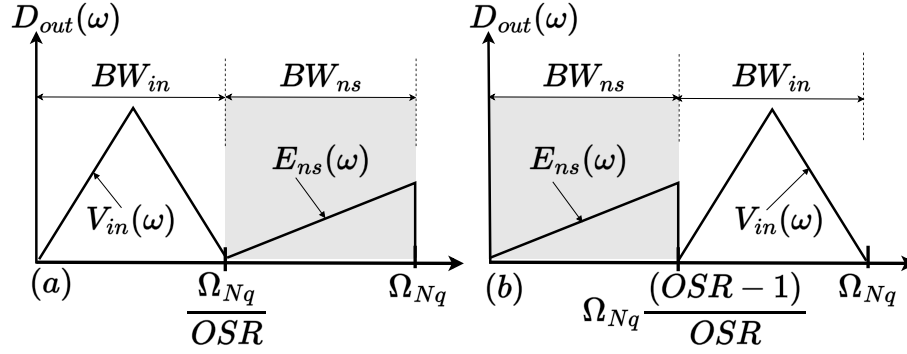


Figure 7.3 Frequency zones, (a): Low-frequency zone, (b): High-frequency zone.

The convolution in the frequency domain is notable as the bandwidth of $E_{ns}(\omega)$ (i.e., Ω_{ext}) is the sum of the bandwidths of $V_{in}(\omega)$ and $RES_{ns}(\omega)$. In turn, the band of frequencies dedicated to noise shaping is expressed as

$$BW_{ns} = \Omega_{Nq} - 2BW_{in} \quad (7.12)$$

where BW_{ns} , Ω_{Nq} , and BW_{in} respectively stand for the bandwidth of the noise-shaped residual error, $RES_{ns}(\omega)$, the Nyquist frequency of TI-ADC ($= F_s/2$), and the frequency bandwidth of the input signal, $V_{in}(\omega)$. The Nyquist zone is divided into two regions as shown in Fig. 7.3. The valid operating frequency band is limited to Ω_{Nq}/OSR , where the oversampling ratio is expressed as

$$OSR = \Omega_{Nq}/(\Omega_{Nq}/2 - BW_{in}). \quad (7.13)$$

This expression shows the first requirement. The OSR begins from 2 for a DC input signal to ∞ for a BW_{in} of $\Omega_{Nq}/2$.

Similar to the noise-shaping DAC approaches, the proposed method, depicted in Fig. 7.2, targets nullifying the frequency components in the band of operation from $E_{ns}(\omega)$. As mentioned earlier, the conventional estimation methods aim to estimate the timing skews, τ_k $k = 0, \dots, M - 1$, independently and separately from our proposed technique. First, our technique multiplexes the coefficients, $c_k(m)$ $k = 0, \dots, M - 1$, to create the combined signal $c(n)$ where m denotes the discrete-time index corresponding to the operating rate of F_s/M . The proposed method utilizes an FIR filter $H(z)$ for shaping the error element $E_{ns}(\omega)$. It can be shown [39] that the noise transfer function is as follows

$$NTF(z) = 1 - H(z). \quad (7.14)$$

Notably, the sharpness of the transition region enhances as the degree of the filter $H(z)$ (equivalently, its number of taps, N) increases. In the proposed approach, the delay step expands to the bound $\{-\Delta_{ns}/2, \Delta_{ns}/2\}$. The quantization error, $e_q(n)$, is randomly distributed by a standard deviation of $\sigma_q^2 = \Delta_{ns}/\sqrt{12}$. Therefore, the variance of the noise-shaped residual error, $RES_{ns}(\omega)$, is given by

$$\sigma_{r-ns}^2 = \sigma_q^2 \sum_{j=0}^{N-1} W_j^2 \quad (7.15)$$

where W_j^2 , $j = 0, \dots, N-1$, denotes the weight of the noise transfer function. This equation shows the second limitation of the proposed method. The NTF must be designed to keep $\sigma_{r-ns}^2 \ll 0.1 \times T_s$; otherwise, the approximation in (7.6) is not valid. Thus, a FIR filter $H(z)$ with fewer taps is preferable. Finally, the noise-shaped coefficient, $c_{ns}(n)$ is demultiplexed to the noise-shaped coefficients $c_{ns,k}(m)$, $k = 0, \dots, M-1$, to tune the VDLs.

It is worth noting that the convolution operator in (7.11) functions in the *analog domain*. Therefore, Ω_{ext} can exceed the Nyquist frequency of the TI-ADC, Ω_{Nq} . In case, the input signal and the residual error $RES_{ns}(\omega)$ are respectively limited to the frequency ranges of $\{0, \Omega_{Nq}/OSR\}$ and $\{0, \Omega_{Nq}/2\}$, as depicted in Fig. 7.4(a), the bandwidth of the noise-shaped error element is expressed as

$$\Omega_{ext} = \Omega_{Nq} \times (OSR + 2)/(2 \times OSR). \quad (7.16)$$

This equation shows that Ω_{ext} being greater than Ω_{Nq} results in an additional frequency aliasing element, $E_{ns,im}(\omega)$, which can affect the performance of this method in the high-frequency zone as depicted in Fig. 7.4(b).

7.4 Simulations

In this section, the proposed approach is validated and characterized by behavioral simulations with MATLAB/Simulink. In our simulations, we set the desired ENOB of the TI-ADC to 10 bits. For simplicity, the sampling rate of the TI-ADC is set to one (normalized to the sampling rate). The timing skews are randomly generated with Gaussian distributions. The standard deviation of the timing skews is set to 0.1. We use an FIR filter with 5 poles at the origin and 5 zeros at $\{1, 0.27 \pm 0.96i, -0.5 \pm 0.86i\}$ to realize the high-pass filter ($H(z)$). We set the delay step of the VDLs, Δ_{ns} , to 0.01, and the resolution of the VDLs, B_{ns} , is set to 6 bits.

Fig. 7.5 shows the power spectrum density (PSD) of the TI-ADC with and without the

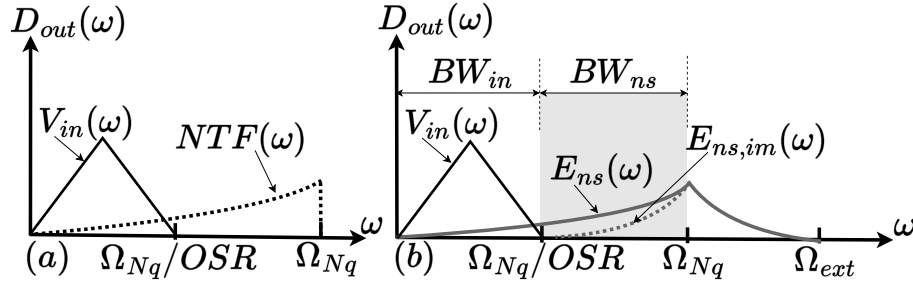


Figure 7.4 Noise shaping concept, (a): Bandwidth of $NTF(\omega)$, (b): Bandwidth of noise-shaped error

proposed noise-shaping mechanism for two zones: low-frequency and high-frequency. In these simulations, we set the number of SADCs (M) to 11. Also, we use single-tone sine waves with frequencies of 0.1 Hz and 0.4 Hz in the low-frequency and high-frequency zones, respectively. As seen in Fig. 7.5, the spurious-free dynamic range (SFDR) is improved, and the harmonics are significantly attenuated and converted to a higher noise floor. Also, the noise floor is moved away from the range of normal operating frequencies.

In addition, we evaluate the SFDR improvement (*the difference of the SFDRs obtained with and without using our proposed method*). The proposed approach is evaluated when the number of SADCs, M , varies from 4 to 20 and single-tone sine waves are sampled in the low-frequency zone (0.01Hz to 0.15Hz) and the high-frequency zone (0.35Hz to 0.49Hz). Figs. 7.6 and 7.7 respectively depict the SFDR improvement results for both the low-frequency and high-frequency zones. The SFDR is significantly improved for $M > 5$ in both zones. The SFDR is respectively improved by 11.64 dB and 17.72 dB corresponding to the low-frequency and high-frequency zones.

It is worth noting that we obtained the above-mentioned results by filtering and evaluating the frequency bands of $\{0, 0.15\}$ for the low-frequency zone and $\{0.35, 0.5\}$ for the high-frequency. For the low-frequency zone, the SFDR improvement increases, whereas the SFDR is around 20 dB for the whole high-frequency band. Although our method significantly improves the SFDR, it does not exhibit any enhancement in the signal-to-noise and distortion ratio (SNDR). It appears that the main benefit of the proposed method is to spread the energy in the spurs over the spectrum of interest.

7.5 Conclusions

This paper proposed an oversampling and noise-shaping approach to mitigate the severe degradation caused by imperfect small delay steps in VDLs' used to combat timing-skew

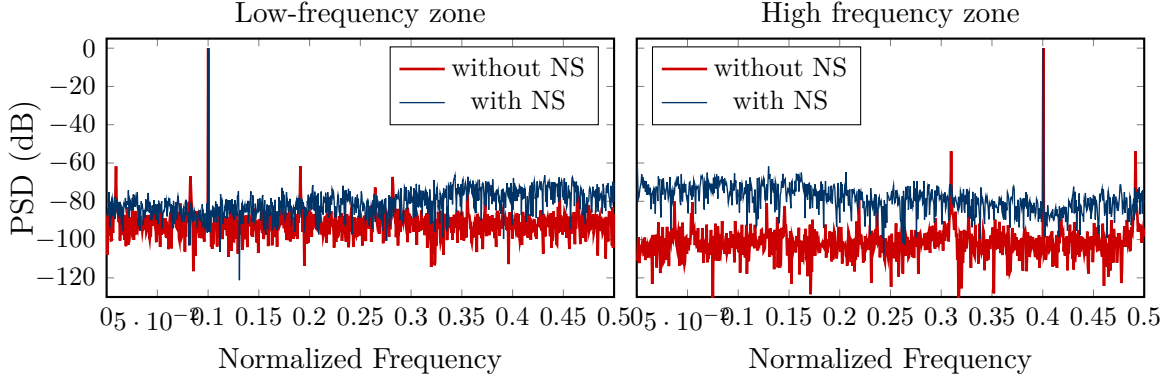


Figure 7.5 Resulting PSDs in response to a low-frequency and to a high-frequency single-tone input.

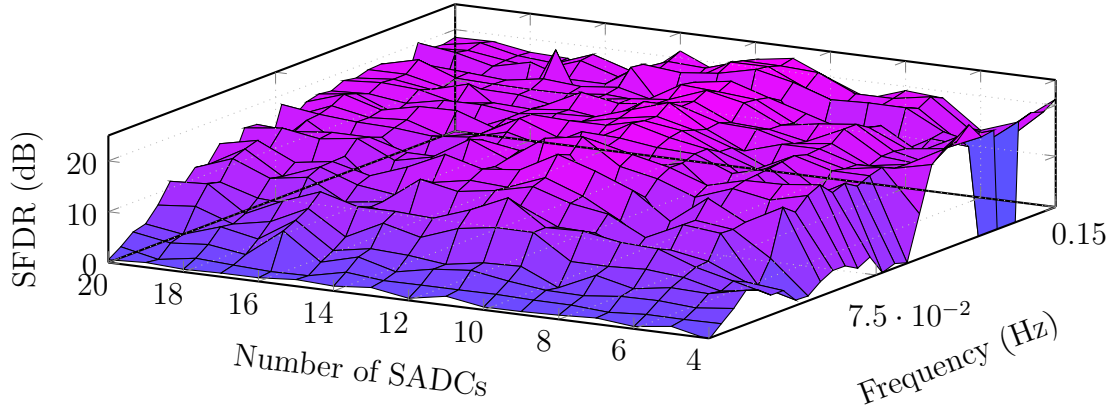


Figure 7.6 Resulting SFDR improvement of the low-frequency zone (frequencies are normalized to the sampling frequency), the mean improvement is 11.64 dB.

mismatches of mixed-signal calibrated TI-ADCs. This method limits the input signal operating bandwidth to less than half the Nyquist frequency. Our method is more suitable for noise-shaped TI-ADCs since their range of operating frequencies is already restricted. However, the proposed method permits the use of either the high-frequency or low-frequency portion of the spectrum. The proposed approach avoids complicating clock routing while limiting the number of SADCs. This method was verified by behavioral simulations with MATLAB/Simulink. In reported experiments, the mean SFDRs were respectively enhanced by 11.64 dB and 17.72 dB for low-frequency and high-frequency zones.

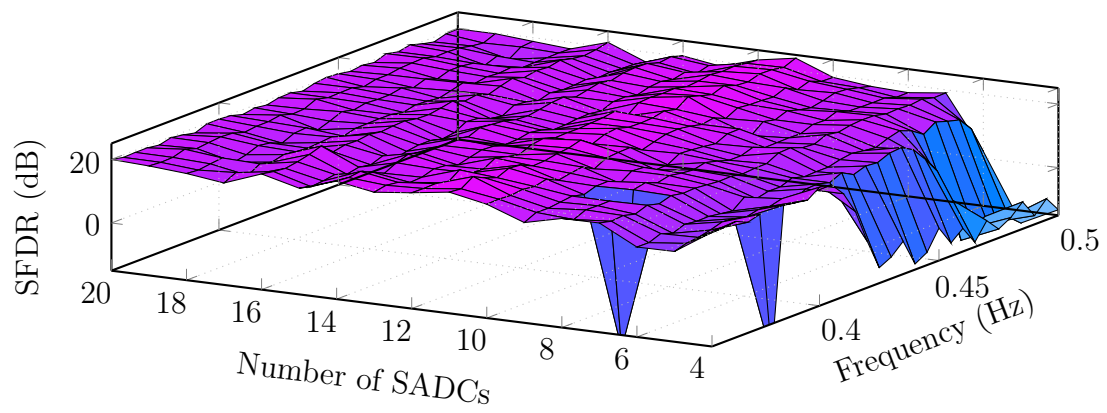


Figure 7.7 Resulting SFDR improvement of the high-frequency zone. Mean improvement is 17.72 dB.

CHAPTER 8 GENERAL DISCUSSION

The TI-ADC plays a key role in modern communication systems as mentioned in Chapter 1. Indeed, this architecture allows combining multiple sub-ADCs (SADCs) to significantly increase the rate at which analog samples can be converted to high-resolution digital representation. A TI-ADC sequentially and repeatedly activates its SADCs to sample the input signal. However, the overall effective resolution of TI-ADCs is sensitive to the mismatches among SADCs. The timing skew among different types of mismatches is more critical and more difficult to estimate and correct due to its frequency dependency. For this reason, various estimation and correction methods have been proposed in the context of two major mixed-signal and fully digital classes with their advantages and disadvantages, as mentioned in Chapter 2. This dissertation targeted to mitigate the weaknesses of the previously reported methods by proposing and validating mixed-signal and fully digital approaches, as mentioned in Chapters 3-7, according to the objectives indicated in Chapter 1.

8.1 Addressing Research Objectives

This section explains the resulting contributions of this dissertation as per their associated objectives indicated in Chapter 1.

1. Proposed Mixed-Signal Calibration Scheme

Chapter 3 contributes to the mixed-signal class that follows the target of the first objective defined in Chapter 1, proposing and validating an approach to desensitize the estimation procedure to the auto-correlation of the input signal without the need for additional SADC or manipulating the design of TI-ADC. The method proposed in Chapter 3 targets desensitizing the estimation procedure to the auto-correlation of the input signal by the time-shift concept. The proposed estimation technique provides a degree of freedom to select the time shifts without needing any extra SADC(s) or manipulating the design of TI-ADC. Although Chapter 3 has utilized timing skew correction ahead of the SADCs (i.e., VDLs in the analog domain), this technique can integrate and operate with correction methods in the digital domain, based on derivative operation using FIR filters (e.g., the correction mechanism proposed in [46]). The performance of this method is also evaluated and verified by numerous simulations.

2. Proposed Fully Digital Compensation Methods

Following the targets of the second objective defined in Chapter 1, which are to propose and validate fully digital methods, able to operate in the whole Nyquist zone without inserting additional delay and the need for additional SADC(s), Chapters 4-6 contribute to the fully digital class. Chapters 4 and 5 seek to develop the applications of the source separation approach to compensate for the timing skew mismatch in the TI-ADC. The main contribution of these two chapters is in generating a second input that extracts the impact of the timing skew mismatches in the proposed source separation approaches. The polyphase implementation of the proposed techniques in Chapters 5 and 6 are worth mentioning, as the polyphase implementation makes this method directly operate on the SADCs' output (instead of TI-ADC output). This polyphase implementation relieves the operating speed requirements of the proposed mechanisms. In addition, the methods proposed in Chapters 4-6 can operate with input signal over the whole Nyquist zone. Various simulations are performed to verify their performance. The proposed methods in Chapters 4-6 shows better performance than their competitive methods according to various simulations.

3. Proposed Noise Shaping Approach

Following the third objective defined in Chapter 1 proposing and validating a method to reduce the impacts of VDLs imperfections without the need for complex clock routing mechanism and without restricting the number of SADCs, Chapter 7 proposes a scheme based on oversampling and noise-shaping methods to reduce the detrimental effects of VDLs imperfections for mixed-signal calibration of timing-skew mismatches in TI-ADC. The proposed mechanism operates without a complex clock routing mechanism while avoiding restricting the number of SADCs. The simulation results show the significance of this method in improving the SFDR.

8.2 Interpretation of Results

This section explains the design and advantages of the methods proposed in this dissertation.

1. Proposed Mixed-Signal Calibration Scheme

Chapter 3 targets desensitizing the estimation procedure to the auto-correlation of the input signal by the time-shift concept. The proposed fully digital estimation method, based on the time-shift concept, is a sensible choice if the auto-correlation of the input signal exhibits a discontinuity or zero value (for example, at T_s). From the basics of digital signal processing, FIR filters with more taps can implement time shifts with

higher precision, and their performance drops slower as the input frequency approaches the Nyquist frequency. Accordingly, the performance of the proposed method depends on the input frequency. Also, it highly depends on the polyphase FIR filter length, and the polyphase FIR filter taps should be optimized based on the specific application requirements and the input signal characteristics. According to the simulations performed in Chapter 3, the signal-to-noise-and-distortion ratio (SNDR) of a specific benchmark was enhanced from 37.44 dB to more than 56.64 dB in a 10-bit TI-ADC with the timing-skew standard deviation of 10% of the TI-ADC's sampling period.

2. Proposed Fully Digital Compensation Methods

Chapters 4-6 proposes fully digital compensation methods by adapting the source separation approach and adaptive FIR filter in feedback. Chapters 4 and 5 are based on a symmetric source separation algorithm with feedback realization [63]. This algorithm needs two adaptive FIR (A-FIR) filters in feedback loops to separate and recover the desired element in the TI-ADC digital output. As mentioned in Chapter 4, the Hilbert transform followed by down-sampling and up-sampling operations is used as the required second input. Chapter 5 adapts and develops the source separation in [63] with a modulation mechanism and realizes it with a polyphase decomposition method to relieve the speed requirements of the filters used. Chapter 6 uses adaptive FIR filters in feedback loops with a modulation mechanism.

The polyphase realization in Chapters 5 and 6 permits the proposed method to work directly on the SADCs. Thus, the polyphase implementation relieves the operating speed requirements, as the two polyphase filters only need to work at the speed of the embedded SADCs. Unlike present mixed-signal and fully digital techniques, which estimate the timing skews and then compensate them in the analog or digital domain, the proposed techniques in Chapters 4-6 eliminate the errors in the compensated digital output by adjusting the adaptive FIR filters.

In our simulations reported in Chapters 4-6, the proposed approaches require FIR filters to mitigate the error resulting from the timing-skew mismatches in the compensated output signals. These FIR filters' length (the number of taps) must be selected according to the number of tones in the input signal and the target resolution. In these methods, the number of taps could be reduced as a function of 1- the desired resolution, 2- the number of channels, and 3- the number of tones. In contrast to most previous competitive techniques, which compensate for the errors, introduced by the TI-ADC timing-skew mismatch, by implementing derivative operations realized by FIR filters (or by VDLs in the analog domain), these techniques mitigate the error by adjusting

the taps of the FIR filters.

Extensive simulations have been performed to verify and evaluate the performance of the proposed fully digital techniques. With the proposed technique in Chapter 4, the SNDR is enhanced from 23.06 dB to more than 66.82 dB in a 12-bit TI-ADC when the standard deviation of timing skew mismatches is set to 10% of the TI-ADC's sampling period. In addition, in a reported experiment, the proposed technique in Chapter 5 enhances the SNDR from 24.29 dB to more than 60.14 dB in a 12-bit TI-ADC when the standard deviation of timing-skew is 10 % of the TI-ADC's sampling period. Moreover, the proposed technique in Chapter 6 improves the SNDR from 22.97 dB to 68.6 dB in a 12-bit TI-ADC when the standard deviation of timing-skew is set to 10% of the sampling interval of the TI-ADC.

3. Proposed Noise Shaping Approach

The proposed method in Chapter 7 pushes the errors (raised by increasing the delay steps) outside the operating frequencies zone by using an FIR filter. It is worth noting that our method is more suitable for noise-shaping TI-ADCs since the operating frequency band is already restricted in this type of TI-ADCs. This technique permits either the high-frequency or low-frequency zones be utilized. This technique avoids utilizing complex clock routing approaches. The proposed method in Chapter 7 is verified and evaluated by behavioral simulations in MATLAB/Simulink. The mean of the spurious-free dynamic range (SFDR) is respectively enhanced by 11.64 dB and 17.72 dB for the low-frequency and high-frequency zones.

8.3 Comparison to Existing Literature

In this section, the proposed methods are compared with existing competitive methods.

1. Proposed Mixed-Signal Calibration Scheme

The time shift concept proposed in Chapter 3 makes the proposed approach less sensitive to the cross-correlation function, unlike previous techniques reported in [17, 30], at the cost of using an FIR filter to generate the time shifts. The method proposed in Chapter 3 manifests dependency on the input signal, which can be reduced by selecting the number of taps. Nevertheless, as mentioned in Chapter 2, the techniques presented in [1, 10, 19] do not reveal any limitation over input frequencies at the price of extra SADC(s).

Table 8.1 Comparison of the Method Proposed in Chapters 3 with Similar Methods

	Resolution (bits)	SNDR (dB)	Number of channels	Convergence $\times 10^3$ (Number of samples)	Extra sub-ADC(s) requirement	Digital hardware complexity	Sensitivity to auto-correlation
This work	10	56.6	4	100	no	filter & multiplier	no
[1]	5	25.1	8	500	yes	adders	yes
[10]	6	35	16	-	yes	adders	yes
[17]	10	52.9	2	56	no	multiplier	yes
[28]	10	54.2	8	80	yes	filter & multiplier	yes
[29]	12	68.6	4	800	no	multiplier	yes
[16]	8	44.4	4	160	no	adders	yes
[19]	13	60.3	8	840	yes	adders	yes

The polyphase FIR filter's power consumption is notable, as it can be disabled to reduce its power consumption. Notably, the polyphase FIR filter in previous competitive techniques generally realizes derivative operation [5, 7, 8, 46]. In the proposed method, the functionality of the polyphase FIR filter is notable as this FIR filter realizes time-shift operation in contrast to [5–8, 46]. Table 8.1 compares the method proposed in Chapter 3 with competitive methods.

2. Proposed Fully Digital Compensation Methods

The proposed techniques in Chapters 4-6 show better SNDRs than other methods (except for the technique in [22]). The reported technique in [22] requires an additional SADC, while these methods do not. Consequently, the techniques in Chapters 4-6 appear as the best options for target applications when the TI-ADC architecture must not be modified, and the whole Nyquist range must be operational. The proposed fully digital methods in Chapters 4-6 do not manipulate analog circuits, and they do not need extra SADC(s) unlike [22, 28]. However, in the proposed techniques, in Chapters 5 and 6, the number of SADC channels is restricted due to using the Hadamard transform, likewise in some reported methods [4, 6, 7, 25]. The complex frequency shift (like the

Table 8.2 Comparison of the Method Proposed in Chapters 4-6 with Similar Methods

	Ch. 4	Ch. 5	Ch. 6	[7]	[4]	[6]	[28]	[8]	[25]	[64]	[22]	[5]
Target resolution	12	12	12	10	10	10	10	11	12	12	14	–
SNDR (dB)	68.8	60.1	68.6	61.9	61.96	58.07	54.2	60	46.61	63.58	72	66
Introducing delay	yes	no	no	yes	yes	yes	yes	yes	yes	yes	yes	yes
Bandwidth limitation	no	no	no	no	yes	yes	no	yes	no	yes	no	yes
Extra SADC(s)	no	no	no	no	no	no	yes	no	no	no	yes	no
Limitation on the number of SADCs	no	2,4,6,...	2,4,6,...	2,4,6,...	2	4	8	no	4	no	no	no

method reported in [5]) can be used instead of Hadamard transform to remove this restriction. Unlike [5, 6, 46], the proposed methods in Chapters 4-6 can operate with input frequencies close to the Nyquist rate of the TI-ADC. Unlike current fully digital compensation schemes, these techniques avoid introducing any delay due to using the filter(s) in the feedback path(s). Table 8.2 compares the fully digital methods proposed in Chapters 4-6 with the competitive methods.

3. Proposed Noise Shaping Approach

The method proposed in Chapter 7 is more suitable for noise-shaping TI-ADCs because the band of operating frequencies is already limited in this type of TI-ADCs. In addition, the proposed technique permits using either high-frequency or low-frequency bands. This scheme avoids complex clock routing used in previous works [32–34]. Moreover, it does not limit the number of SADCs, unlike [35, 36].

8.4 Implications and Significance

TI-ADCs play a key role as the backbone of current modern high-speed communication systems, as mentioned in Chapter 1. TI-ADCs require additional calibration (or compensation) mechanisms to eliminate the inherent random mismatches among the SADC channels. For this reason, several calibration (or compensation) methods have been developed for both mixed-signal and fully digital classes, each with its benefits and disadvantages.

This dissertation contributed to both mixed-signal and fully digital approaches and targeted to overcome the current limitations according to the objectives indicated in Chapter 1. The proposed mixed-signal and fully digital methods are realized in the digital domain, operating without extra SADC(s) and manipulating the TI-ADC architecture. This feature makes them easily portable from one technology node to the next, more advanced technology without

Table 8.3 Summary of the Proposed Methods

	Polyphase realization	Number of FIR filters	Limitation on the number of Sub-ADCs	Estimation part	Correction part
Chapter 3: Time-shift concept	yes	1	no	digital	analog
Chapter 4: Source separation approach	no	2	no	digital	digital
Chapter 5: Polyphase source separation approach	yes	2	2,4,8,...	digital	digital
Chapter 6: Adaptive filters in the loop	yes	$M - 1$	2,4,8,...	digital	digital
Chapter 7: Noise-shaping approach	no	1	no	-	-

requiring design. The proposed techniques in this dissertation mark significant advances in both the mixed-signal and fully digital classes. Chapter 3 proposed a digital method to desensitize the estimation procedure to auto-correlation of the input signal. This method offers the following advantages:

- A better SNDR in comparison to the methods that target 10-bit resolution,
- Insensitivity to the input signal's auto-correlation,
- Operation without the need to manipulate the design of TI-ADC.
- Operation without the need for extra sub-ADC or the manipulation of TI-ADC.

Chapters 4-6 proposed fully digital methods that do not introduce any delay between the outputs of the SADCs and their associated compensated outputs. These methods offer the following advantages:

- They show better SNDRs than almost all other methods,
- They avoid restricting the high-frequency band
- They avoid using extra sub-ADC(s) or manipulating the TI-ADC structure.

Finally, the technique proposed in Chapter 7 pushes the errors (introduced by increasing the delay steps) outside the operating frequencies range using an FIR filter, with the following advantages:

- It shows the complex clock routing that was used in previous works,
- It avoids restricting the number of sub-ADCs.

The mixed-signal methods proposed in Chapters 3 and 7 are suitable for low-resolution targets (less than 8 bits) as they use VDLs for correction of timing-skews, unlike the fully-digital method proposed in Chapters 4-6 targeting high-resolution applications (more than 8 bits). The methods proposed in Chapters 3, 5, and 6 are suitable for high-speed targets since they use the polyphase mechanism. In contrast to the proposed techniques in Chapters 3-5, and 7 using one filter for any number of SADCs, the method proposed in Chapter 6 needs $M - 1$ polyphase filters, making it suitable for TI-ADCs with low number of SADCs. The proposed techniques in Chapters 5 and 6 restrict the number of SADC to specific numbers (i.e., 2, 4, 8, $\dots$), unlike the proposed methods in Chapters 3, 4, 7, and 7 operating without

restricting the number of SADCs. Therefore, each of the methods proposed in this thesis offers something that none of the other offers. Table 8.3 summarizes the specifics of the methods proposed in Chapters 3-7.

8.5 Robustness of the Results

The Chapters 3-7 are not implemented on ASIC due to the financial limitations of this research project. Therefore, the TI-ADCs in these chapters are modeled in Simulink (see Section 8.6.1). In well-designed TI-ADCs, parametric variations appear only as thermal noise in the sample and hold stage of SADCs and offset, gain, and timing-skew mismatches among SADCs. In the TI-ADC Simulink models, used in this dissertation, the thermal noise at the sample and hold stage and random time skews in SADCs, introduced by parametric variations, are modeled in the simulations, and their other impacts (i.e., offset and gain mismatches) are neglected (assumed to be mitigated by some other means) to concentrate only on the compensation of the timing-skew mismatches similar to [6–8, 22, 64].

Chapters 3-6 used simulations using FPGA implementations of the HDL codes obtained from fixed-point precision models of the proposed methods to evaluate and verify the proposed methods in a realistic environment with various word widths (see Section 8.6.2). For this reason, these proposed techniques are easily portable to ASIC platforms as these methods are fully digital, operating independently of the TI-ADC architecture and design. The robustness of the methods proposed in Chapters 3-6 is worth noting as the reported techniques in these chapters either operate on the digital output of the TI-ADC or the SADCs, the behavioral simulations with fixed-point models using FPGA implementations are trustworthy enough for applicability of these techniques and verification of their performance without the need for considering the analog circuits and architecture of the TI-ADC.

It is of interest that in almost all calibration methods (e.g., [2, 4, 8, 10, 17, 28, 30, 46, 64]), sine-waves (single-tone and multi-tone) are utilized to validate and compare the reported calibration techniques. Thus, single-tone and multi-tone sine waves are used to characterize and compare the proposed methods in this dissertation with competitive techniques.

8.6 Limitations

This section discusses the limitations of the proposed methods in this dissertation.

8.6.1 Simulink Models of TI-ADC

The techniques proposed in this dissertation are sensitive to offset and gain mismatches, like most existing methods [4, 7, 20, 28, 48, 49]. Therefore, these mismatches must be calibrated before utilizing the proposed methods in Chapters 3-6. Notably, the gain and offset mismatch are introduced by inherent random internal mismatches among sub-ADCs, unlike the timing skew raised by clocking circuits and paths. Therefore, offset and gain mismatches must be treated independently of the timing skew mismatch and calibrated before using timing skew compensating mechanisms [28, 48, 49].

8.6.2 Maximum Operating Speed of Proposed Methods

Although the TI-ADC's sampling frequency was set to 1 Hz in our Simulink models for presentation simplicity, the frequency at which the hardware realization of our methods operates can be as high as that of any other competing approaches. The maximum operating frequency relies especially on the CMOS technology node being used. When running on FPGA, the compensation engines implementing the proposed techniques can operate at frequency rates from 78 to 147 MHz, based on the timing report of the Vivado Design Suite [55], when targeting the Xilinx Virtex-7 VX690T FPGA implemented with a 28 nm CMOS technology. It is important to note that FPGA realization by the HDL codes obtained with the fixed-point Simulink model does not represent the actual operation of the proposed techniques in this dissertation. For evaluating the real maximum operating rate of the proposed methods, the FIR filters, appearing as a limiting factor to the maximum operation rate, must be directly written in an HDL code and implemented in an ASIC target. For this reason, the proposed techniques would function much faster if the proposed methods targeted a modern ASIC implemented in a state-of-the-art technology (such as 3 nm TSMC) [57].

8.6.3 Power Consumption of Polyphase FIR Filter

In Chapters 3, 5, and 6, the polyphase realization permits the proposed methods to operate directly on the SADCs. Therefore, the proposed polyphase implementations relieve the operating speed requirements. Although the polyphase filters in Chapters 3, 5, and 6 consume M (i.e., the number of SADCs) times more chip area than their single-rate counterparts, their power consumption is almost the same as their single-rate counterparts since the polyphase filters operate M times lower than the single-rate filters.

8.6.4 Modulation Operation and the Number of SADCs

Although the Hadamard transform is used as the modulation operation to reduce the hardware resource in Chapters 5 and 6, a complex frequency shift approach can be used to realize the modulation operation, as introduced in [5], $\mathbf{m}(n)$, and to remove the restriction on the SADCs imposed by the Hadamard transform. For the single-rate version of our method, the estimates of $M - 1$ images are created by a set of $M - 1$ modulating complex-value signals, $e^{jn(i/M)}$, from the input signal as follows

$$d_{md,i}(n) = d_{tiadc}(n) \times e^{jn(i/M)}, \quad i = 0, \dots, M - 1. \quad (8.1)$$

In this case, the modulated signals, $d_{md,i}(n)$, are complex values, which makes the adaptive FIR filters operate with complex-value signals. The hardware complexity thus doubles since the modulating signals, $e^{jn(i/M)}$, are practically realized by sine and cosine operations as $\sin(n(i/M)) + j\sin(n(i/M))$ [5]. Moreover, the modulation matrix of size $(M - 1) \times M$ must be generated for the polyphase realization version. The modulated signals, $d_{md,i}(n)$, are expressed as follows

$$\begin{bmatrix} e^{j/M} & e^{j2/M} & \dots & e^{j(M-1)/M} \\ e^{j2/M} & e^{j4/M} & \dots & e^{j(M-1)2/M} \\ \vdots & \vdots & \ddots & \vdots \\ e^{j(M-1)/M} & e^{j2(M-1)/M} & \dots & e^{j(M-1)(M-1)/M} \end{bmatrix}. \quad (8.2)$$

In this polyphase realization case, the hardware complexity also doubles.

8.6.5 Power Consumption and Hardware Complexity of Adaptive Filters

The proposed fully digital methods in Chapters 4-6 are based on adaptive filters with variable coefficients, despite most current methods being developed with FIR filters with constant coefficients. For this reason, the power consumption of adaptive filters should be evaluated and compared with FIR filters.

Fig. 8.1 depicts a B -bit multiplier consisting of a chain of B -bit adders. In this architecture, the input data, $\{d_{i,msb}, \dots, d_{i,lsb}\}$, is multiplied with a weight (i.e., the coefficient), $\{w_{msb}, \dots, w_{lsb}\}$, to create the B -bit output, $\{d_{o,msb}, \dots, d_{o,lsb}\}$. Also, the coefficient's bits, $\{w_{msb}, \dots, w_{lsb}\}$, are random variables since the coefficients of the adaptive filter in the proposed method depend on the random timing skews and the input signal. For this reason, it can be supposed that the bits $w_i \quad i = 0, \dots, B - 1$ being 0 or 1 has an equal probability of

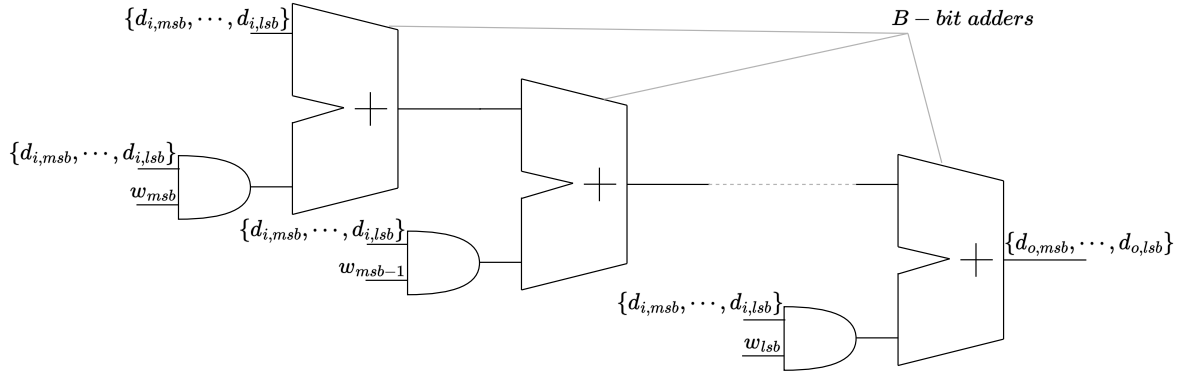


Figure 8.1 Model of a B -bit multiplier comprising of B -bit adders with B -bit inputs and output.

0.5. Consequently, the bits w_i (i.e., $B/2$) is identical to zero.

In FIR filters, the adders whose associated input bits w_i are equal to one are implemented, and the other $B/2$ adders are neglected. Thus, for the implementation of B -bit multipliers, $B/2$ adders are required. However, adaptive FIR filters require implementing all the B adders. For this reason, adaptive filters consume two times more hardware and power than FIR filters if their coefficients continuously vary during the proposed method's convergence. After the proposed method converges, it is notable that the adders corresponding to the bits w_i equal to zero behave as buffers since their activity is restricted to one input. These adders reduce power consumption by three (notably, the carry signals within the B -bit adders are inactive).

In summary, multipliers in the adaptive filter consume two times more power during convergence than their FIR counterparts, and after convergence, the proposed source separation method consumes just 33% more power. The proposed method with adaptive filters is comparable with some state-of-the-art techniques mentioned above (e.g., [7, 71]) since the adaptive filters in the proposed method need 15 taps, compared to the methods reported in [7, 71] which use FIR filters with 25 and 31 taps, respectively.

CHAPTER 9 CONCLUSION AND RECOMMENDATIONS

Time-interleaved ADCs (TI-ADCs), which achieve higher sampling rates, play a key role in today's communication systems. TI-ADCs use multiple identical parallel sub-ADCs (SADCs). The equivalent sampling frequency of TI-ADC is higher than the SADC sampling rate by the number of SADC channels due to the sequential sampling of the input signal by SADCs. However, TI-ADCs are sensitive to mismatches among their SADCs. Imperfections among the SADCs, consisting of *offset*-, *gain*-, and *timing skew* mismatches, degrading the target effective resolution and necessitating the use of calibration methods to retrieve the target effective resolution. Timing skew calibration methods generally require means for estimation and compensation of the timing skew mismatch to recover the target effective resolution. Mixed-signal and fully digital approaches are the two main timing skew mismatch calibration classes. The mixed-signal schemes are suitable for high sampling rates, whereas the fully digital approaches are sensible choices for high-resolution targets.

9.1 Research Summary

This dissertation has established a mixed-signal based on time-shift for estimating timing-skew mismatch method in Chapter 3, fully digital timing-skew mismatch compensation approaches in Chapters 4-6, and noise-shaping mechanism in Chapter 7 to relieve the VDL complexity. In Chapter 3, this dissertation first proposed the concept of time shift to desensitize for estimation mechanism of timing-skew to the autocorrelation of the input signal. The proposed method operates without additional SADC(s) and without manipulating the design of TI-ADC. In Chapter 4, the source separation approaches and the Hilbert transform are adapted to characterize and remove the error introduced by the timing skew. The source separation mechanism desensitizes the proposed technique to the frequency variation of the input signal while avoiding introducing any delay by using two finite impulse response (FIR) filters. Chapter 5 developed the source separation by a polyphase decomposition approach, together with a modulation mechanism, to relieve its speed requirement. In addition, the proposed approach utilizes the Hadamard transform as the modulation operation to detect errors. Also, the proposed mechanism is realized by the polyphase decomposition approaches to relieve the speed requirement of the proposed technique. The proposed source separation-based approaches, in Chapters 4 and 5, operate without the need for any additional SADC(s) and without any manipulation of the TI-ADC's structure. In addition, Chapter 6 used the polyphase adaptive FIR filters in feedback loops to remove the errors

arising from the timing-skew mismatch in the digital output of the TI-ADC. This method performs its compensation task without needing additional SADC(s) and manipulating the TI-ADC's design. The polyphase decomposition realizes the proposed method to relieve the speed requirement of the proposed technique. Finally, oversampling and noise-shaping mechanisms are used to mitigate the effects of errors from enlarging the minimum step size of variable delay lines (VDLs) while avoiding complex clock routing methods. The proposed method drives the error (introduced by increasing the delay steps) outside the operating frequencies. This technique is more suitable for noise-shaping TI-ADCs since they are already band-limited. Also, it does not restrict the number of SADCs.

9.2 Summary of Contributions

The main contribution of this dissertation can be summarized as

1. **Desensitizing the estimation methods to the autocorrelation of the input signal**

In Chapter 3, the concept of time shift was proposed to desensitize the estimation mechanism to the auto-correlation of the input signal. One finite impulse response (FIR) filter generates the required time shifts. Also, the FIR filter was implemented using the polyphase decomposition mechanism to relieve the speed requirement of the proposed method. This proposed fully digital estimation method operates without additional SADC(s) and without manipulating the TI-ADC's architecture, making it suitable for fully digital calibration mechanisms.

2. **Using source separation algorithm along with the Hilbert transform for fully digital compensation**

The method proposed in Chapter 4 benefited from the source separation algorithm to remove the errors arising from the timing-skew mismatch in the digital output of the TI-ADC. The Hilbert transform, down-sampling, and up-sampling were used for the required second input. The proposed technique compensates without additional SADC(s) or manipulating the TI-ADC structure. It can also operate in almost all the Nyquist range without introducing any delay in its compensated output signal.

3. **Using polyphase source separation algorithm for fully digital compensation**

Chapter 5 also benefited from the source separation algorithm to remove the errors arising from the timing-skew mismatch in the digital output of the TI-ADC. The polyphase decomposition realized the source separation algorithm approaches to relieve the speed

requirement of the proposed method. For this phase, the Hadamard transform was used as a modulation operation for the second set of inputs to the source separation algorithm. The proposed method can operate in all the Nyquist range. This technique avoids introducing any delay in its compensated output signal. In addition, it performs its compensation task without the need for any additional SADC(s) and without any manipulation of the architecture of TI-ADC.

4. Using polyphase adaptive filters for fully digital compensation

Chapter 6 proposed using polyphase adaptive FIR filters in feedback loops as a main contribution to remove the errors arising from the timing-skew mismatch in the digital output of the TI-ADC. The polyphase decomposition realized the proposed mechanism approaches to relieve the speed requirement of the proposed technique. Moreover, the proposed approach used a modulation operation to detect errors. The proposed method performs its compensation task without needing additional SADC(s) and manipulating the TI-ADC's structure. It can also operate without restricting the Nyquist range and without introducing any delay in its compensated output signal.

5. Using a noise-shaping technique to relieve limitation of variable delay lines

As a main contribution, Chapter 7 attempted to use oversampling and noise-shaping mechanisms to mitigate the effects of the errors resulting from enlarging the minimum step size of VDLs, while avoiding utilizing complex clock routing methods. The proposed method drives the error (raised by increasing the delay steps) outside the operating frequencies. This technique is more effective for noise-shaping TI-ADCs since they are already band-limited. Also, it does not restrict the number of SADCs.

9.3 Future Research

The methods reported in Chapters 3-7 are based on single-rate and polyphase FIR filters. The number of taps in Chapter 3 affects the effective resolution of the TI-ADC after being calibrated. In Chapters 4-6, the number of taps used in the proposed techniques also affects the effective resolution, and it depends on the number of SADC channels and the number of tones in the input signal. Chapter 7 introduces a noise-shaping technique that shows its performance dependency on the number of taps of the FIR filter. Optimizing the number of filter taps in these chapters remains an open subject to study. Optimizing these filters leads to minimum hardware and power consumption. Finally, the estimation of the proposed method's hardware requirement and power consumption in state-of-the-art CMOS technology remains for possible development.

Possible future developments and improvements can be considered as improving and adapting the proposed schemes in Chapters 4 and 5 to operate with wider applications by proposing new input combinations and using other source separation methods. As mentioned earlier, evaluating different modulation mechanisms (e.g., complex frequency shift operation) to improve the performance of the proposed techniques in Chapters 5 and 6 remains an open research subject. Finally, implementing the proposed noise-shaping method in Chapter 7 using polyphase decomposition can also be considered a possible future development.

9.4 Final Thoughts

The performance of the proposed method compared to the competitive techniques showed the significance of the contributions in this research. The proposed methods in this research appear to be the best choice for target applications in which the TI-ADC architecture must not be modified since all the proposed methods in this dissertation operate independently of the TI-ADC's structure and analog circuit design. The proposed estimation technique based on time-shift concept, in Chapter 3, highly desensitizes the dependency of the present correlation-based techniques to the auto-correlation of the input signal. In Chapters 4-6, the proposed techniques appear as the best options due to achieving higher SNDRs, and these techniques avoid introducing any delay in the compensated output signals. Also, the noise-shaping-based approach in Chapter 7 to relieve the VDL requirement effectively improves the SFDR. Since the proposed methods in this dissertation use FIR filter, implementation and optimization of FIR filters according to the target application and the benefit of ASIC implementation are valid subjects for future research. Moreover, the use of modulation operation (e.g., complex frequency shift operation) for the proposed methods in Chapters 5 and 6 remains a good topic for future research.

9.5 Closing Statement

This research contributes to both mixed-signal and fully digital compensation classes, as mentioned in Section 9.3. The proposed method's performance and results compared to the competitive techniques proved the significance of the contributions in this dissertation. The contributions in this thesis can be optimized and/or extended according to the recommendations in Section 9.3 to operate with broader applications.

9.6 Publications

Two articles have been published, two have been accepted, and two have been submitted as part of this research.

1. Hamidreza Mafi, Mohammad Honarparvar, Mohamed Ali, Naim Ben-Hamida, and Yvon Savaria, “*Background Calibration of Time-Interleaved ADCs with Polyphase Filters*,” 2023 IEEE 21st Interregional NEWCAS Conference (NEWCAS), Edinburgh, United Kingdom, 2023, pp. 1-5.
2. Hamidreza Mafi, Naim Ben-Hamida, Sadok Aouini, and Yvon Savaria, “*Digital Compensation of Timing Skew Mismatches in Time-Interleaved ADCs by Source Separation*,” IEEE Transactions on Instrumentation and Measurement, vol. 73, 2024.
3. Hamidreza Mafi, Mohammad Honarparvar, Mohamed Ali, Naim Ben-Hamida, and Yvon Savaria, “*Background Calibration of Time-Interleaved ADCs with Polyphase Filters*,” Accepted in 2024 IEEE International Symposium on Circuits and Systems (IS-CAS), 2024.
4. Hamidreza Mafi, Naim Ben-Hamida, Sadok Aouini, and Yvon Savaria, “*Digital Compensation of Timing-Skew Mismatch in TI-ADCs by Polyphase Source Separation*,” Accepted in 2024 IEEE 22nd Interregional NEWCAS Conference (NEWCAS), Sherbrooke, QC, Canada, 2024, pp. 1-5.
5. Hamidreza Mafi, Mohammad Honarparvar, Mohamed Ali, Naim Ben-Hamida, and Yvon Savaria, “*Digital Background Estimation of Timing-Skew Mismatches in Time-Interleaved ADCs*,” Submitted to IEEE Transactions on VLSI Systems, 2024.
6. Hamidreza Mafi, Sadok Aouini, Naim Ben-Hamida, and Yvon Savaria, “*Digital Compensation of Timing-Skew Mismatches in TI-ADCs with Adaptive Polyphase Filters*,” Submitted to IEEE Transactions on Signal Processing, 2024.
7. Hamidreza Mafi, Naim Ben-Hamida, Sadok Aouini, and Yvon Savaria, “*Digital Compensation of Timing-Skew Mismatch in TI-ADCs by Polyphase Source Separation*,” Submitted to IEEE Transactions on Circuits and Systems I: Regular Papers, 2024.

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