IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Date of publication exxxx 00, 0000, date of current version tentative xxxx 00, 0000.

Digital Object Identifier 10.1109/ACCESS.2017.DOI

Thermal Analysis of System in Package Considering Boundary Conditions for Long-Term Reliability Studies

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"This work was supported in part by Polytechnique de Montreal under Grant BS123456."

ABSTRACT This paper proposes an integrated Foster-based thermal network for a System in Package (SiP) that models thermal interaction between package layers to predict the transient temperature of junctions and interlayer compression in SiP. The critical factors contributing to impedance mismatch are detailed to ensure modeling accuracy. Important factors include the boundary conditions and the interface layer of the thermal material. With the help of the Finite Element Method (FEM) and data curve fitting, thermal parameters are derived and expressed as a function of boundary conditions. The proposed modeling method is demonstrated with 3D heterogeneous System in Package models implemented in Simulink for long-term temperature predictions. Predicted junction and interlayer temperatures show good accuracy, confirmed by reported results obtained by Finite Element Analysis (FEA). The importance of considering the boundary conditions and the materials used in the various interfaces is shown through simulation results. Neglecting one of these key factors, the predicted temperature differs by as much as 14.5 °C in the reported results. The proposed thermal network is consistent with FEA, while computing much faster and producing results that differ by no more than 0.5 °C, unlike previously reported models.

INDEX TERMS Finite Element Analysis (FEA); Finite Element Method (FEM); heat transfer and interaction; integrated Circuits (ICs); System-in-Package (SiP); thermal model.

I. INTRODUCTION

System-in-Package (SiP) enables innovative solutions for microsystems assemblies. Compared to monolithic ASICs, it can offer several advantages, such as shorter time to market and lower cost through heterogeneous integration [1]. Their features make them suitable for applications requiring small modules integrating mixed-signal circuits and passive devices. They are appealing for integrating versatile sensor and interface applications [2]. However, due to the high level of integration offered by SiP, which may imply stacking dies and layers comprising heterogeneous materials, issues may arise when the various parts of a SiP have different coefficients of thermal expansion. This may induce critical thermo-mechanical stress [3],[4]. Thermo-mechanical issues can degrade SiP reliability [5], lead to module failures, and short system lifetime in the absence of proper thermal management and reliability analysis. In addition, it was shown that fatigue and cracks can occur under thermal cycling, mostly at the interface between different layers such as bumps, Through-Silicon Vias (TSVs), and silicon substrate [6].

To tackle thermal challenges in SiPs, several methods have been suggested in the literature to characterize heat flow between chips, and heat sinks. These methods can be classified into two groups: analytical and numerical. The analytical methods are suitable for systems with simple geometry and boundary conditions. In addition, when the heat flow is uniform, exact solutions of 1D or 2D governing partial differential equations can be obtained by using Fourier-series solution [7]-[9], Green's functions [10]-[12], or Volterra's Series Expansion [13],[14]. The work presented in [15] demonstrates that the heat paths within the structure toward the heat sink have high thermal impedance. The thermal parameters R and C were computed using analytical expressions. However, it is still hard to determine an accurate

thermal profile due to the heat spread effect.

Numerical methods include Finite Elements Methods (FEMs) [16],[17], Finite Difference Methods (FDMs) [18]-[20], and Discontinuous Galerkin Time-Domain (DGTD) recently presented by [21] to conduct the transient thermal modeling for heterogeneous ICs. These models cannot consider the dependence on temperature of volumetric heat capacity and boundary conditions [12]. A weighted Laguerre polynomials finite element-based model [22],[23] is reported for transient thermal simulation of 3D-ICs. The finite element-based numerical methods can model any device geometry and yield accurate results. However, it makes them very time-consuming, and unsuitable for real long-term measurements and analysis. Modeling of thermal behavior within electronic systems provides the basis for thermal management and optimization. A key aspect of the reliability assessment model of SiPs is the need to accurately reflect the thermal behavior [24] of dies and underneath layers in the transient regime.

Many researchers in the field of thermal design combine thermal-network-based methods and Finite Element Analysis (FEA)-based methods to benefit from the advantages of these two methods [25],[26]. The combination of methods is widely used. It allows for effective prediction of the temperature distribution in complex structure geometry. In [25], the model is presented based on an analogy between heat flow driven by temperature differences and electrical current flow driven by voltage differences. Using this analogy, heat flow can be represented by a thermal equivalent RC network. This model has the advantage of offering fast computation of transient thermal profiles. However, it generally neglects temperature-dependent factors and can only be applied for simplified boundary conditions. In [26], an analytical model based on electrical network theory for 3D ICs was reported. The steady-state model that was developed assumes ideal cases. Then, by applying Kirchhoff's law, a new model was developed for 3D ICs. This model can only be used to analyze simple problems. For instance, only the vertical heat flow was considered in this model, and lateral heat effects were neglected.

In [27], a new thermal model combining the advantages of Cauer and Foster thermal networks was given. It consists of two paths for thermal flow: the first one estimates the junction temperature, and the second one estimates the case and heat sink temperatures. The disadvantage of this method is that it does not consider thermal coupling and does not permit predicting the temperature difference between the junction and the case. A review of recent research on the modeling of heat transfer in three-dimensional integrated circuits was presented in [28]. In this article, the advantages and disadvantages of existing models are given. It has also been reported that, while analytical models are accurate and easy to integrate with design tools, it is often difficult to consider complex geometries, temperature-dependent properties, and the effect of nonuniform cooling systems. On the other hand, numerical models can model complex geometries, and when used appropriately, they can provide accurate predictions of temperature profiles.

Existing models cannot predict inter-layer temperatures, only accept simplified boundary conditions, and are limited to modeling steady-state conditions. By contrast, modeling the transient heat transfer response is critical to avoid detrimental thermal peaks. Therefore, when studying reliability, a fast and accurate transient thermal model for 3D SiPs that predicts temperatures in junction and critical layers such as solder bumps and joints is required. These features are vital for thermal management and reliability analysis tools.

In [30], the transient thermal behavior of heterogeneous 3D-ICs was extracted from the COMSOL Multiphysics® package, with which thermal simulation results were saved in a data file. Unlike in our previous work [29], the step response to all boundary conditions affecting the thermal model's accuracy was also simulated with the COMSOL Multiphysics® package [30]. The data extracted from COMSOL contains temperature profiles of dies and critical layers (Bumps, Underfill, etc.). Then, the well-known analogy between the thermal and electrical systems is applied to build the thermal-network-based model for transient temperature calculations. In this respect, all layers of interest in the 3D-IC are considered node voltages (temperature), and every two adjacent layers crossed by the flows are connected by thermal impedances analogous to "electrical" ones. The Foster-type Resistance Capacitance (RC) network represents every impedance in our proposed thermal model, and every RC parameter is expressed as a function of boundary conditions. A curve-fitting algorithm can obtain the values of RC thermal parameters. The proposed model was implemented in Simulink for temperature node solving; then, a test case was applied to validate the proposed model. Moreover, the thermal analysis is performed, and the impact of different layers on the behavior of the thermal model is studied.

The main contributions of the present article can be summarized as follows: a) a method is proposed to develop SiP's thermal networks that take into account the heat transfer between layers and the boundary conditions and that accurately predicts the temperatures of all layers of interest in an acceptable time, b) the models obtained from that modeling method permit effective thermo-mechanical analysis of packages, c) a time-efficient transient analysis is proposed to detect localized stress that could arise in complex multi-layer structures. We will show that the proposed method allows for predicting a complex thermal profile in minutes, which would take several hours to obtain with finite element tools. This is demonstrated through a specific SiP that comprises multiple die stacks subject to thermal transients and complex boundary conditions. d) Later, Specific benchmarks reported demonstrate the feasibility of obtaining a transient thermo-mechanical profile of a SiP comprising multiple and stacked dies. The ability to get these transient profiles is key to reliability analysis of this class of complex systems, where failures could appear in an interface such as a solder joint due to thermal cycling. e) The paper also studies the impact of

including and removing some layers on the model's accuracy and proposes a trade-off between the model's accuracy and simulation time.

The rest of this article is structured as follows: Section II gives a brief definition of the system in the package of interest and then describes the proposed thermal model. This system model is based on detailed thermal impedance derived from the COMSOL Multiphysics® package. Section III reports the results obtained with the proposed methods and models and their validation. Finally, section IV concludes this paper by summarizing its main findings.

II. PROPOSED THERMAL MODEL

A. THERMAL MODELING METHOD

The thermal modeling method proposed in this paper is outlined in Fig. 1. To evaluate the time efficiency and prediction accuracy of the proposed thermal modeling approach, two representative SiP case studies are performed. These benchmarks allow the analysis of the effects of inevitable thermo-mechanical stress due to heat generation in SiPs. To model the short-time thermal response of this type of complex system, we combine the use of a circuit-based simulator and the Finite Element Method (FEM). The adopted FEM tool is COMSOL. Generally, FEM tools can only simulate this type of system for short-term studies, and they require excessive processing time for long-term studies, which is important for reliability studies. Without loss of generality, we focus in this section on explaining the thermal interactions and temperature predictions of an exemplary system that includes four dies and many layers. The step-by-step thermal modeling of this system is described below.

The first step of the process is to describe the geometry of the target heterogeneous 3D-SiP together with the properties of its constituting materials. Fig. 2 shows the structure of the system and the configuration of the self and cross-impedances, which change depending on the heat source. Every two consecutive layers are connected by thermal impedance, and all impedances are connected in series. In this figure, TIM stands for thermal interface material (often called Thermal Grease). Die 2 self-impedance in the first heat path includes the silicon, thermal interface material, and heat sink layers. However, Die 1 self-impedance includes, in addition to layers previously mentioned, the die 1-silicon and TSV1. The Through Silicon Via (TSV) may feature tungsten interconnections representing only a fraction of the silicon base. This results in forming a composite material with an anisotropic thermal conductivity in the TSV layer, creating a preferential conduction pathway through the tungsten connections.

This results in differences between the thermal impedance configuration as depicted in Fig. 2(a) and 2(b), and its implementation in COMSOL is depicted in Fig. 3. The dimensions and the material properties are taken from [31] and they are listed in Table 1.

The modeled system consists of two stacks, each containing two dies, one on top of the other, and several layers. Each

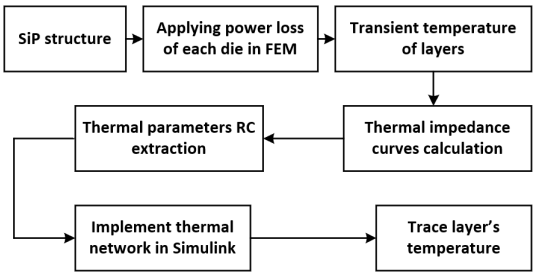

FIGURE 1. Thermal modeling process.

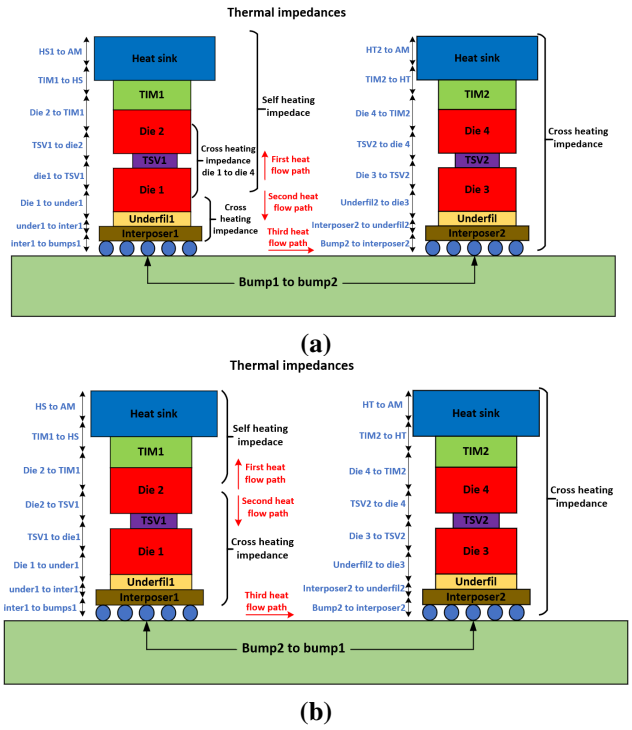

FIGURE 2. Thermal impedance configurations: (a) Die 1 heated. (b) Die 2 heated.

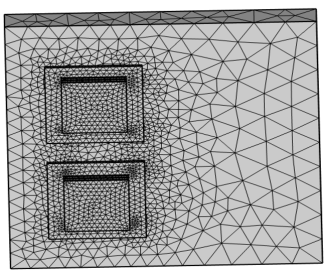

FIGURE 3. 3D model treillis (not to scale).

TABLE 1. Geometry information and equivalent thermal parameters.

Layer	Dimension (mm^3)	Material	Thermal cond (W/m.K)	Thermal cap (J/Kg.K)
TIM	5x5x0.37	epoxy	1.6	610
Die	5x5x0.75	Si	130	700
Microbump	5x5x0.125	SnAg, epoxy	0.9	1381
Interposer	10x10x0.25	Cu, Si	170	583
package	20x20x2.25	FR4	0.3	1369
TSV	2X2X0.125	Tungsten	174	133
Underfil	5X5X0.175	Epoxy resins	2.5	490

TABLE 2. List of symbols.

Ta	Ambient temperature
Tjn	Junction temperature of die n
T_{LK}	Temperature increases in layer K
Z_{Lij}	Thermal impedance between tow predefined layers i and j
$j_n p_1$	Impedance of die n due to the first heat flow path
$j_n p_2$	Impedance of die n due to the second heat flow path
$L_k p_1$	Impedance of layer K due to the first heat flow path
$L_k p_2$	Impedance of layer K due to the second heat flow path
Z^D_{self}	Total self-impedance of die D
Z^{P1}_{self-D}	Self-impedance of die D due to the first heat flow
Z^{P2}_{self-D}	Self-impedance of die D due to the second heat flow
$Z_A - Z_B$	Impedance between two consecutive layers

layer has a different CTE (coefficient of thermal expansion). Thus, cracks can occur when heat crosses these layers. Therefore, a model that can predict the temperature in these critical layers must be developed.

B. THERMAL IMPEDANCE COMPONENTS

When heat is generated on the surface of a die, and it goes through different thermal paths, the transfer of heat might occur in a vertical thermal path among layers in the same stack where heat is generated or may go to the adjacent stack through a horizontal thermal path. The heat generated in one die may affect all other dies in the system so that the junction temperature could be calculated as the sum of contributions due to the self-heating temperature, the ambient temperature, and the coupling effects due to the heat generation on other dies. Fig. 4a and b show the average bulk temperature for each layer caused by the heat generated by die 2 and die 3, respectively. Once generated, the heat propagates through the layers and raises their temperature. The layers react differently to heat and increase their temperature depending on their thermal properties, the amount of heat, and the distance from the heat source. Fig. 4a shows the temperature rise in die 2 due to self-impedance, and the temperature rises in die 1, die 3, and die 4 due to the effect of the heat flows from die 2 to die 1, die 3, and die 4. To study the thermal influence between the different dies, the transient thermal temperature in each node along the thermal path is required (see Fig. 4b). To obtain these node temperatures, FE simulation has been performed four times with the COMSOL Multiphysics®package. In every simulation, one die is active by applying expected dissipated power, and all the rest are kept inactive, during a simulation all layers' temperatures must be measured (Fig. 4b). Once the transient temperatures are extracted, results are used to compute thermal impedances produced by self and cross heating. As discussed before, the self and cross impedances depend on the active die during the simulation. Therefore, four configurations must be considered. Fig. 2a and 2b show the configuration of thermal impedances of the 3D-SiP in the case where die 1 and die 2 are heated, respectively. The thermal impedance between two layers in this work is defined as the ratio of the temperature difference between their geometric centers to the applied dissipated power (equation 1). The notation P_{loss} in equation 1 represents the thermal power dissipated between the layers, which includes the heat lost due to thermal resistance between the different layers. In other cases, it may represent the total power introduced into the matrices, including both the applied and lost power.

$$Z_{layerij}(t) = \frac{T_{layeri} - T_{layerj}}{P_{loss}} \tag{1}$$

Table 2 provides more details of the meaning of symbols used throughout the text.

C. CURVE FITTING OF THERMAL IMPEDANCES

The 3D-SiP under study contains four heat sources, namely die 1,2,3, and 4. Therefore, four FE simulations have been performed by applying a set of heat powers to the dies. These simulations produce a set of curves representing the transient temperatures of the four dies and underneath layers, as shown in Fig. 4. Transient thermal impedances between any two layers are directly derived, as shown in equation 1. The obtained curves are time-dependent quantities, and they can be emulated by a Foster equivalent network that consists of n pairs of parallel RC connected in series, as shown in Fig. 5, where P_1 through P_4 are the dissipated power in the dies and T_{LK} are the temperature increases in the K layer due to heat from the four dies. The thermal network shown in Fig.5 comprises four branches, each corresponding to heat flow caused by one of the dies. Each branch consists of thermal impedances, representing the layers of the SiP, connected in series. The mathematical model of the impedance shown in Fig. 5 is given by Equation 2. Details about the symbols in Fig.5 are given in Table.2. The analytical representation of Equation 2 is chosen as the objective function within the fitting procedure used to extract RC pair thermal parameters. In this work, the curve fitting algorithm provided by Matlab has been exploited to fit the step response of equation 2 to the simulated impedance curves.

$$Z_{thjc}(t) = \sum_{k=1}^{3} R_k(1 - e^{\frac{t}{\tau_k)}} \tag{2}$$

Where τ_k is the thermal time constant of k^th term, and equals to $R_{k^th} \times C_{k^th}$, where R_{k^th} is the equivalent thermal

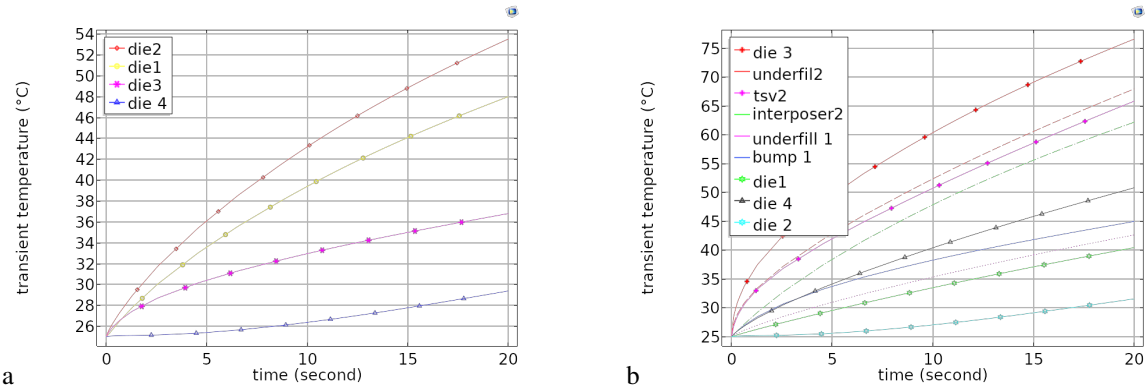

FIGURE 4. Transient temperature distribution over dies and underneath layers obtained by FE simulation: (a) Die 2 heated. (b) Die 3 heated.

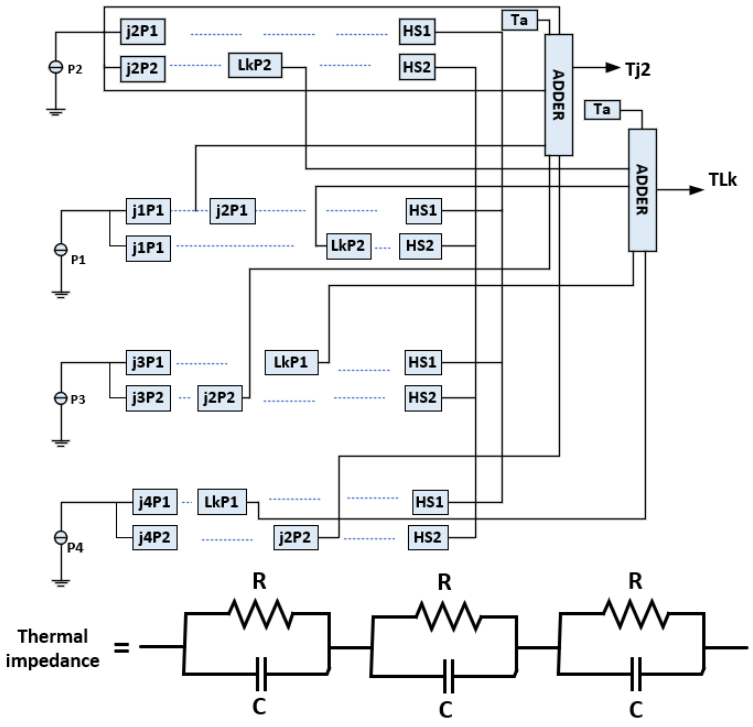

FIGURE 5. Proposed thermal network.

resistance, and C_{k^th} is the equivalent thermal capacitance and k is the number of exponential terms usually equals 3.

By doing so, the thermal parameter values are obtained and can subsequently be used in the corresponding Simulink model for temperature calculation.

D. THERMAL IMPEDANCE EQUATIONS AND ORDER REDUCTION

To reduce the order of the model and, subsequently, the calculation time, a test case under varying loss power is reported in section III. A was applied, then the transient thermal impedances between layers were computed. In this figure, the y-axis (vertical) represents impedance in (k/w), while the x-axis (horizontal) represents time in seconds (s), please refer to Table 2 for more details. The curve plotted on the graph shows how the impedance of the layers evolves. This evolution is related to changes in the system's operating conditions, such as temperature in our case. Observing these curves provides information about the evolution of the electrical properties of the layers over time, which is crucial for understanding our system's overall behavior and performance. Through transient thermal simulations reported in Fig. 6, we found that some coupling impedances are close to zero or remain unchanged when a heat source is added due to the long distance of the added heat source from the layer characterized by these impedances. Therefore, the impedance of each layer varies according to the physical property of the layer and its position relative to the source of the heat flux. In this case, the model order can be reduced by ignoring some thermally unaffected layers in the self and coupling impedance calculations. Therefore, the total impedance is considered invariant when other less significant impedances add no more than one percent of the total self-impedance and 5% of the total cross impedance in the steady state. As an illustration, Fig. 7 shows a thermal path in the case of the heated die 2, all the layer's impedances above the layer of the interposer have been removed from the model and the impedance of the latter is directly connected to the heat-sink. Where $D_1 - TSV_1, TSV_1 - D_2, D_2 - TIM_1, TIM_1 - HS_1$ represent the thermal impedance in the first heat flow path between die 1 and TSV_1, TSV_1 and die 2, die 2 and thermal material interface, thermal material interface 1 and the heat sink 1 respectively. Also $D_1 - unf_1, unf_1 - int_1, int_1 - b_1, b_1 - b_2, b_2 - int_2, int_2 - hs_2$ represent the thermal impedance in the second heat flow path between die 1 and underfill 1, underfill 1 and interposer1, interposer1 and bump 1, bump 1 and bump 2, bump 2 and interposer 2, interposer 2 and the heat sink 2 respectively

In this case, the self-thermal impedance of layer die 2 is given as follows:

$$Z_{self}^{die2} = Z_{self-die2}^{P1} + Z_{self-die2}^{P2} \tag{3}$$

Where

$$Z_{self-die2}^{P1} = Z_{die2-TIM1}^{self-die2} + Z_{TIM1-HS2}^{self-die2} \tag{4}$$

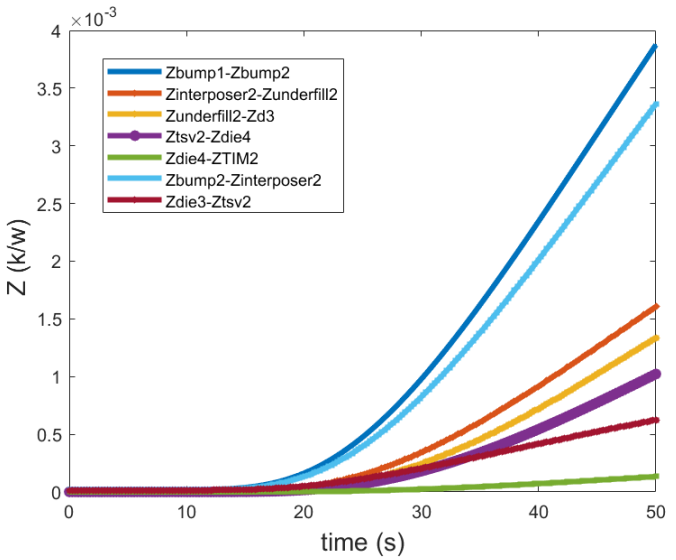

FIGURE 6. Variation of the layers' impedances.

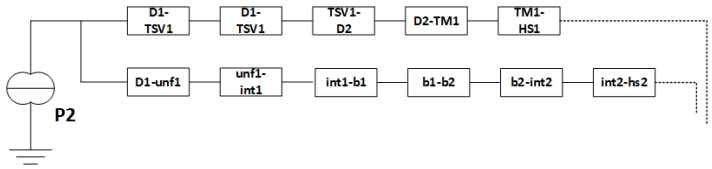

FIGURE 7. Model reduction example.

and

$$Z^{P2}_{self-die2} = Z^{self-die2}_{die2-TSV1} + Z^{self-die2}_{TSV1-die1} + ...Z^{self-die2}_{int2-hs2} \tag{5}$$

To calculate the coupling impedance between a die and any layer within the package, all the impedances between the heat flux source and the target layer must be summed. As an example, equation (6) shows the cross impedance between die 2 and die 1.

$$Z^{die2-die1}_{cross} = Z^{die1}_{die2-TSV1} + Z^{die1}_{TSV1-die1} \tag{6}$$

Equation (1) can calculate the impedances in the right of equations (4), (5), and (6). To find the temperature rise in each layer within the package, equation (7) can be used.

$$T_L(t) = \sum_{i=1}^{N} \sum_{j=1}^{j_{l,i}} Z^l_{i,j} P_i + T_{reference} \tag{7}$$

Where $T_{reference}$ represents the reference temperature of layer L, $P_i, i = 1,..4$ represent the losses powers on dies, and $Z^l_{i,j}$ is the the thermal impedance from heat flux to target layer and is the self-impedance of layer L if $i = j$.

E. CHARACTERIZATION OF THERMAL PARAMETERS IN TERMS OF BOUNDARY CONDITIONS

In real cases, SiPs experience different environmental conditions (change in ambient temperature), dynamic thermal management based on nonlinear cooling techniques, and variation of load powers on dies. All these external conditions are considered boundary conditions and have an impact on the accuracy of the thermal model as it shows more discrepancies in thermal impedances while these factors change. So far, the thermal network shown in Fig. 5 provides reliable thermal interaction between layers within SiP. Still, it does not take into account the effect of boundary conditions on prediction accuracy.

Through transient thermal simulations, we show the importance of including the boundary conditions in the thermal model. FEA is performed for each operating condition, and then the transient thermal impedance of all layers is extracted. To understand the impact of nonlinear cooling of the package on thermal impedances, the convection boundary is applied at the surface of the heat sink. Then, step responses are analyzed under varying heat transfer coefficients htc in the range of $1100 < htc < 22000 W.m^{-2}.K^{-1}$. The transient impedance between the Thermal Interface Material TIM and the heat sink, under these htc values, is shown in Fig. 8.a, and between the die 1 and the underfill is shown in Fig. 8.b. As shown in Fig. 8, not all impedances are sensitive to htc. htc has more impact on the impedance near the heatsink, as shown in Fig. 8.a, and its effect decreases as the impedances are farther from the heatsink.

In Figure 8b, we notice that the thermal impedance increases slightly as the heat transfer coefficient increases, especially during the transient time. The reason is the thermal blocking phenomena; the more the htc increases, the more heat flux is localized beneath the heat source (die 1 in this case), which causes less heat spread in the structure, especially toward the thermal grease and heat sink. This will raise the temperature near the heat source and, in return, increase the thermal impedance and, consequently, the thermal spreading resistance in the steady state. Adding spreading resistance to the existing study can provide valuable insights into how heat propagates across component surfaces. This can help better understand heat transfer phenomena and refine the model to be more representative of the real system. In practice, the layers respond to heat spreading differently depending on the thermal and electrical properties of materials and their dimensions. Using a model that does not match the specification of the validated model can affect the accuracy of the results and lead to discrepancies in the performance predicted by the model. For every thermal impedance that varies according to htc the equivalent thermal parameters are computed, then the analytical expressions of thermal parameters as a function of the htc can be obtained by fitting the computed RC values to htc. Fig. 9 shows a thermal branch in which the thermal parameters have been expressed as a function of the htc for each layer sensitive to the varying heat transfer coefficient, and that is kept constant for insensitive layers. For example, the parameter values of the thermal impedance between die 1 and TSV_1 are kept constant while the parameter values of the thermal impedance between die2 and $TIM1$, and between $TIM1$ and heat sink $hs1$ are changing in function of the htc.

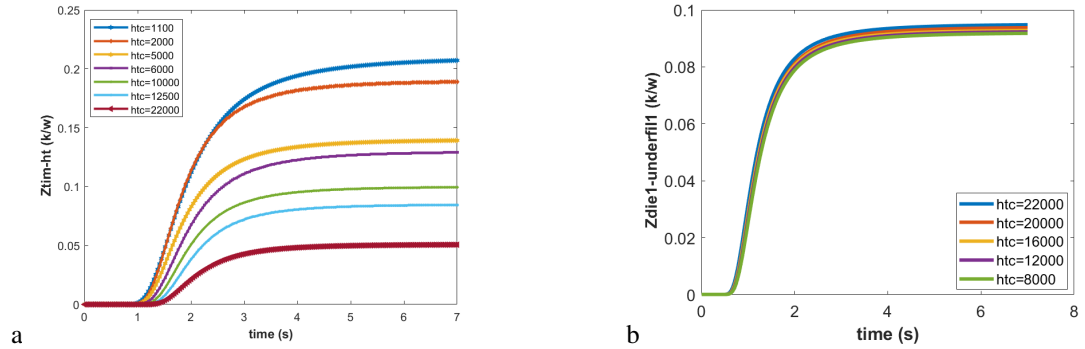

FIGURE 8. Impact of the htc on the model: (a) Transient impedance sensitivity to the htc. (b) Transient impedance insensitivity to the htc.

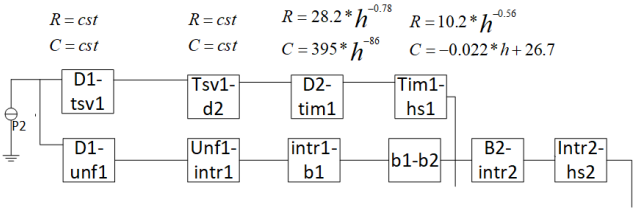

FIGURE 9. Thermal branch with htc boundary condition.

To analyze the effect of power losses from dies on thermal impedances, the ambient temperature is fixed to room temperature, htc to $1000W.m^{-2}.K^{-1}$, and dies are excited with different pulse power varies from 30 W to 180 W. The transient thermal impedance between $die1$ and $TSV1$, and between the heat sink and thermal material interface under these conditions, are shown in Fig. 10.a and Fig. 10.b, respectively. Following these figures, all thermal impedances increase with power losses, especially between die 1 and TSV1 and between TSV1 and die 2. The reason is due to the thermal properties of Silicon whose conductivity decreases as its temperature increases, which in turn affects the rest of the self and coupling impedances. However, the impedance between the heat sink and the thermal material interface is almost not affected. Finally, the impact of ambient temperature in some impedances is shown in Fig. 11.a and Fig. 11.b. All impedances are affected to different degrees, however, the impedances of the outer layers such as the heat sink show more sensitivity to changes in ambient temperature than the inner layers.

For each layer of the SiP whose impedance is affected by the boundary conditions, its RC thermal parameters have been expressed as a function of these boundary conditions and approximated as:

$$R = r_1 + r_2.T_a^2 + r_3.T_a + r_4.e^{r_5 + r_6.P_{loss}} + r_7.e^{r_8 + r_9.htc} \quad (8)$$

$$C = c_1.htc^{c_2} + c_3.T_a^2 + c_4.T_a + c_5.P_{loss}^2 + c_6.P_{loss} + c_7 \quad (9)$$

Where $r_1....r_9$, $c_1....c_7$ are fitted values; T_a, P_{loss} and htc are boundary condition's variables.

III. MODEL VALIDATION AND VERIFICATION

To validate the proposed model, two applications have been studied, which include the system shown in Fig.3 and the 3X3aFan. We applied different power losses to the entire system, and then the junction as well as underneath temperature were measured based on the method explained in the previous section.

A. VALIDATION OF THE PROPOSED MODEL WITH FE

To verify the constant thermal parameters-based model and boundary conditions dependent thermal parameters-based model, a test case under varying loss power was applied in Simulink and then results were compared to temperatures coming from FEM. The four dies are subjected to power losses modulated by pulses shown in Fig. 12.(a) and Fig. 12.(b). The carrier waves shown in Fig. 12 are designed to facilitate the performance of experiments, the test bench, and measurements. Thus, the carrier wave's amplitude varies with the amplitude of the power losses (the Pulses in Fig.12 are modulators and are used only to modulate the power losses). In the first experiment, the total applied power was 160 W modulated by a pulse shown in Fig. 12.(a), the heat transfer coefficient, htc, is fixed to $1000W.m^{-2}.K^{-1}$, the ambient temperature was set to room temperature. These boundary conditions are the same as those applied using COMSOL during the extraction of the thermal parameters. In Fig. 13.(a), we can see heat curves for the junction's temperature estimation for die 2 obtained by FE and the proposed models. It is noted that the results of the proposed models are in good agreement with those produced by FEM, with the max temperature difference being lower than 0.70 °C obtained by the model, including the boundary conditions. The good agreement obtained in this case does not take into account the boundary conditions with the variation of nearly 0.5 °C. These results were expected because the thermal parameters were derived under the same conditions applied in this first experiment. On the other hand, the model that included the boundary conditions loses some accuracy when deriving the terms of the thermal parameters for the boundary conditions.

In the second experiment, we slightly modify the boundary conditions: the total applied power was 220 W modulated by

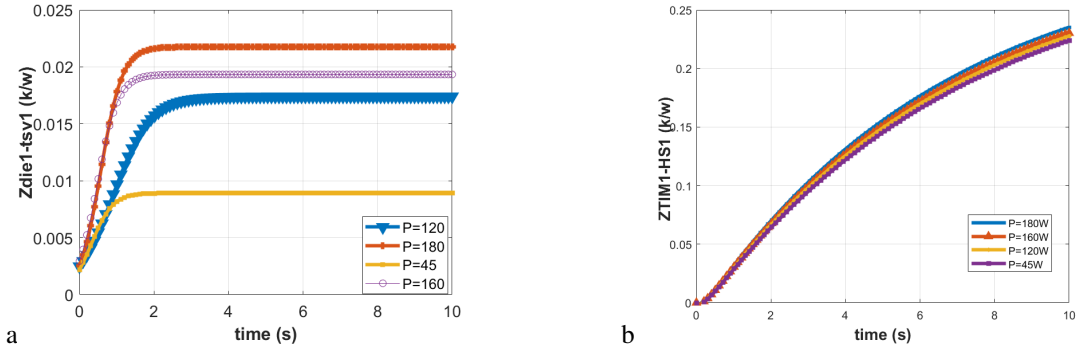

FIGURE 10. Impact of change in power loss on impedance: (a) between dies and TSVs. (b) between TIMs and HSs.

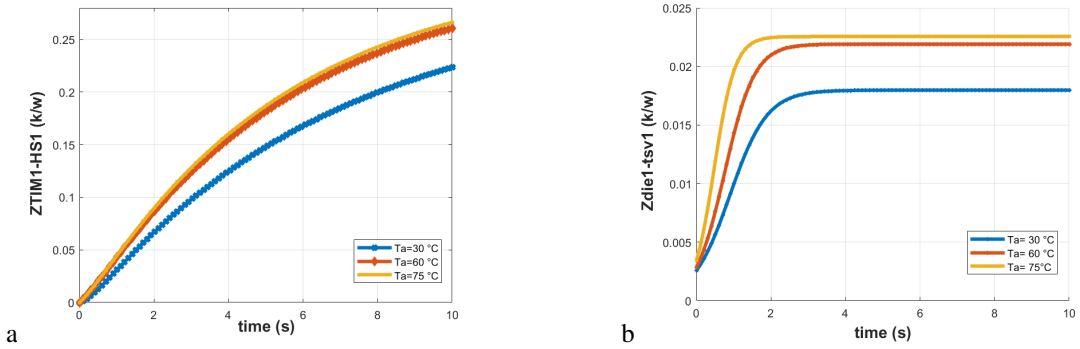

FIGURE 11. Variation of the impedance according to the ambient temperature. (a) between the TIM and the HS. (b) between the die and the TSV

a pulse shown in Fig. 12.(a), and the heat transfer coefficient htc is fixed at $2500W.m^{-2}.K^{-1}$, the ambient temperature assumed to be 45 °C. As shown in Fig. 13.(b), the transient temperature simulation obtained by the model, including the boundary conditions, is slightly different from that obtained by FE, with a maximum error of 0.6 °C. However, a large error of about 8.4 °C is obtained from the constant parameters thermal model. The reason for the dramatic discrepancy between FE and the model without boundary conditions is due to the sensitivity of thermal impedances to the change of boundary conditions, as shown in Fig. 8 to Fig. 11. It is clear that for the thermal model to predict the temperature distribution accurately and consistently, it must include boundary conditions. To further verify the accuracy of the original model with boundary conditions (BC), a superposition of three time-variable pulses (see Fig. 12) was employed as the heat source. Fig. 14 depicts the transient temperature of the solder's layer obtained by the original model and COMSOL. The results presented so far have concerned junction temperatures. To ensure the validity of our model in predicting the layer's temperature, we also show the results of the solder layer prediction and compare them to the FEA, as this is critical for solder cracking reliability studies. As it is clear in Fig. 14, our model is in good agreement with FEA. The error between our original model with BC and FEM is less than 0.5 °C. The results of Fig.14 also show the performance of the original model with BC that accurately describes the

TABLE 3. Computational efficiency comparison

	COMSOL		LBFEM		Proposed	
Package	t	er%	t	er%	t	er%
$3X3FA$	3h51 m	NA	19m 44s	1.7	9s	1.8
3D SiP	2h 37m	NA	15m 24s	2.3	4s	1.3

thermal behavior at critical layers such as the solder joints.

The accuracy of the model has been checked against the Laguerre-based finite-element $(LBFEM)$ method presented recently in [32]. In the first case, we modeled the same package $3X3afan - outwafer - levelpackagingarray$ used by the authors (not shown here for the sake of brevity), and under the same boundary conditions, we applied our thermal model to the two packages, i.e. SiP and $3X3afan - outwafer - levelpackagingarray$. In the second case, we applied the $(LBFEM)$ method under the same conditions as in the first case. In Table 3 we show the results obtained by our model and those reported in [32]. The error mentioned in Table 3 is the prediction error when compared with the full COMSOL model. In the second case, we applied the $LBFEM$ method on the 3D SiP depicted in Fig. 3, and the computational efficiency results are reported in Table 2 next to the prediction error.

It is obvious that our proposed model can be computed much faster than the $LBFEM$ and COMSOL models for almost the same accuracy. In Fig.15, the transient temperature curve estimation of die 2 for different levels of power dis-

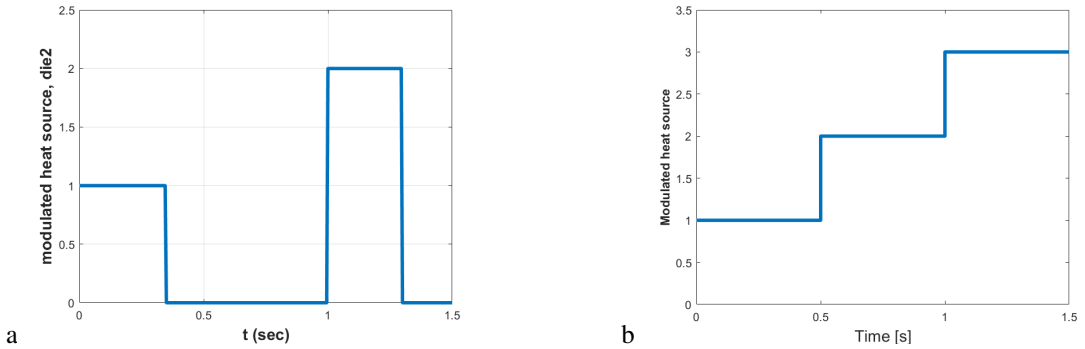

FIGURE 12. Time-varying pulse used for modeling a heat source: (a) first and second experiments, (b) third experiment.

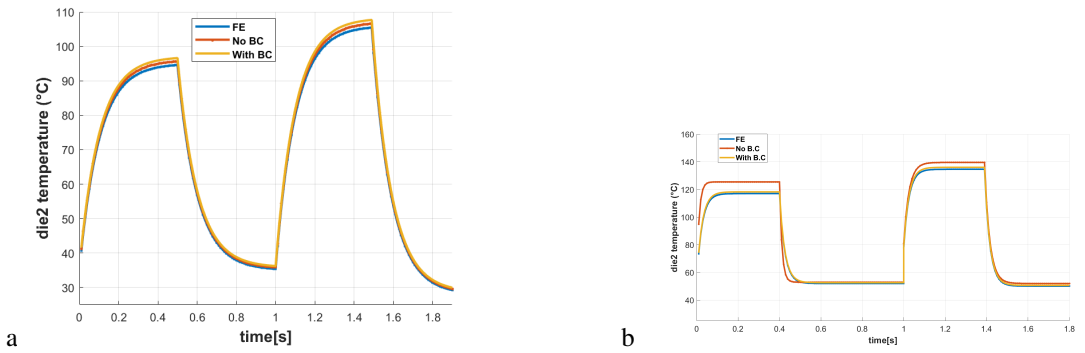

FIGURE 13. Transient temperature curves of die 2: (a) first experiment, (b) second experiment.

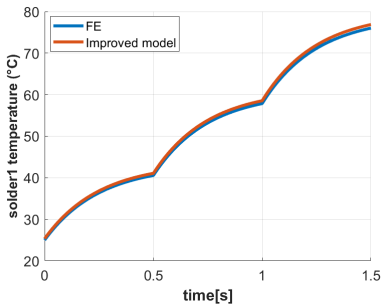

FIGURE 14. Third experiment: Transient temperature curves of solder joints.

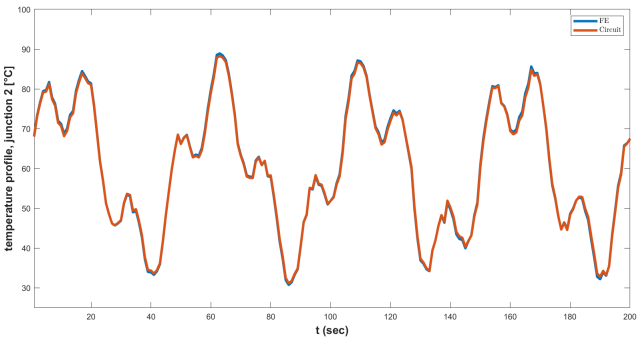

FIGURE 15. FEM validation of the proposed thermal circuit.

sipation shows a good agreement. While the Finite Element Method (FEM) simulation in COMSOL took about 3 hours to converge and requires a very large amount of memory that goes up to 3.4 GB (proportional to the simulated time that is rather short here), the proposed model took about 4 seconds to evaluate while the model consumed 2.3 MB. This gain in computing time and memory becomes very significant when a long-term prediction of the thermal behavior of a package is performed. It is not only for the intrinsic prediction speed reason, but also because the FEM may not converge. The figure also shows that the layer undergoes thermal cycling and peaking, which can lead to serious long-term reliability issues.

B. ANALYSIS OF THE EFFECT OF UNDERNEATH LAYERS ON THERMAL MODEL

In the experiment performed in the present section, we show the importance of considering thermal interface materials in the model when they are present. This is true even when we wish to perform a reliability analysis of the package, and the temperature distribution in this layer is not needed. To show the impact of the TIM, we simplified our model by neglecting these layers. Thus, in the simplified model, only thermal impedances between dies are included. The results with the full model and with the simplified model are reported in Table 4. This table shows the temperature predicted by the

TABLE 4. Impact of underneath layers on model's accuracy

model	COMSOL	original		simplified	
	temp °C	temp °C	dif °C	temp °C	dif °C
die1	77.2	77.6	0.4	68.9	8.3
die2	62.3	62.55	0.25	51.8	10.5
die3	107.55	108.1	0.55	95.95	11.6
die4	72.30	72.65	0.35	63.1	9.2

original model and the simplified model, as well as the errors in temperature prediction.

Comparing results obtained with the two models to those produced by COMSOL, the proposed thermal model with TIM provides better accuracy compared to the model without the TIM layers. Compared to the results provided by COMSOL, the original model in the worst case differs only 0,55 °C, reported in die 4, and the best case reported in die 1 with an error equal to 0.35. The temperature differs at die 1, 2, 3, and 4 by 8.3 °C, 10.5 °C, 11.6 °C, and 9.2 °C, respectively, for a simplified model.

The large discrepancy in temperature predicted by the simplified model comes from the fact that each layer has its thermal resistance and capacitance, which contributes to the thermal behavior of the entire system. The TIM material has a significant contribution in transferring the heat from the dies to the heat sink, so the large errors provided by the model without TIM layers are understandable, as they are caused by the heat blocked inside the package. From the reported results, the original model with TIM can predict the thermal behavior more accurately than the simplified model without TIM. the accuracy of the thermal model depends on taking into account the TIM layer.

IV. CONCLUSION

A new and fast transient thermal model for heterogeneous 3D-SiP mounted on a heat sink, which contains four dies and several underneath layers, has been presented. The proposed model takes into account the change in the boundary conditions that reflect the ambient temperature, the nonlinear cooling, and the power losses. The boundary conditions are transformed into thermal parameters by mathematical relations. The proposed modeling method can be applied to any geometric structure. It can predict not only junction temperatures but also the temperature of underneath layers. Moreover, it can easily be integrated into Simulink models for long-term reliability and thermo-mechanical stress analysis. The performed thermal analysis shows that the accuracy of the thermal model depends strongly on the consideration of the boundary conditions influencing the thermal impedances and on the consideration of each layer in the system under study. The validity of the proposed model has been evaluated by comparing the results obtained by the proposed model to the simulated results obtained by finite elements and by comparing its computational efficiency to that reported in the literature. The maximum difference in temperature between our model and FEA is 1 °C, and the minimum difference in temperature is 0.5 °C. Finally, a key feature of the modeling method adopted in the present paper is its capacity to predict the thermal behavior of systems in package within a time sufficiently short to enable long-term reliability studies that notably include thermal cycling.

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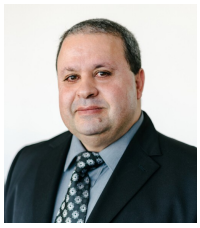

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