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SELF - ALIGNED INSULATED GATE FET TECHNOLOGY FOR InP: AN INTERFACE ENGINEERING APPROACH

par

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SELF - ALIGNED INSULATED GATE FET TECHNOLOGY FOR InP: AN INTERFACE ENGINEERING APPROACH

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Man ought to act
There is freedom only in action
-Bhagavad Gita-

To My Parents

C.R.Srinivasan and Amirtha Srinivasan

SUMMARY

The technologies based on InP and associated ternary and quaternary alloys are being pursued vigorously in the emerging areas of optoelectronics, and high frequency electronics. Fabrication of insulated gate FET structures on InP is hampered by the poor quality of the InP/insulator interface. InP does not have a stable native oxide and deposited insulators are normally used. However, the InP surface degrades during even modest thermal annealing 150-300°C, similar to that used for dielectric deposition, with the formation of surface phosphorus (V_P) vacancy traps. These traps reduce the transconductance and cause the drain current to drift with time. Thermal degradation is especially serious for self-aligned gate (SAG) structures that use a high temperature implant anneal in the fabrication process and there are no reports of a reproducible SAGFET technology for InP to date.

In this study, we present a new approach by combining a novel indirect plasma deposition technique with sulfur (S) surface passivation to engineer a low trap interface that shows good high temperature stability and a highly reproducible SAGFET technology has been developed that shows promise. The first phase of this study concentrates on the nature of S passivation of InP by PL and XPS measurements. The results clearly show thermal S passivation leads to the formation of a 30Å In_2S_3 layer that prevents P out-diffusion from the InP surface, thereby decreasing the V_P deep level emission intensity from the passivated samples. Latter a universal model for the formation of sulfide layers on InP from monolayer coverage to thick sulfide layers is proposed. Monolayer In-S coverage is explained as a photo electrochemical interaction between deposited neutral S^o atoms and acceptor-like In dangling bonds while thicker

sulfide layers are due to S reacting with the InP substrate according to the In-P-S ternary equilibrium phase diagram.

S passivated Metal/silicon nitride/InP (MIS) capacitors with near ideal C-V characteristics, negligible hysterisis and midgap interface state density in the low $10^{11} cm^{-2}.eV^{-1}$ have been fabricated for the first time. The passivated capacitors exhibit good high temperature stability upto 700°C thermal annealing and show promise for a self-aligned gate FET technology for InP. The complete process technology, viz. mesa isolation, implantations, implant activation, indirect plasma nitride, gate and contact metallization, has been developed including a novel implant annealing technique and the new indirect plasma deposition technique. A exclusive copyright test chip using 5 mask levels is designed to fabricate the SAGFETs and to evaluate their characteristics. Accumulation and inversion type passivated SAG MISFETs and InP/InGaAs/InP SAG HIGFETs are fabricated and tested. This is the first report of passivated SAGFETs in literature and the technology is extremely reproducible. The FETs exhibit excellent transistor characteristics with low output conductance (g_o = 0.05-0.38 mS/mm) and performance comparable to non-self-aligned FETs. The measured peak transconductances are 10-12 mS/mm and 30 mS/mm for MISFETs and HIGFETs respectively. The drain current drift in these devices is quite small (6%) and upward over a period of 10^4 seconds indicating the absence of V_p related traps. Device performance is mainly limited by high gate leakage due to S incorporation into the insulator and the passivation process is also found to be quite non-uniform. Suggestions are made to reduce gate leakage and a novel epitaxial interface engineering technique is proposed to improve uniformity.

The study clearly reveals the advantages of using interface engineering techniques for next generation insulated gate high speed devices for InP and is expected to inspire the development of a mature interface engineering technology for III-V semiconductors.

RÉSUMÉ

Les techniques de passivation deviennent de plus en plus populaires pour les dispositifs à base de semi-conducteurs III-V et leurs développements promet une amélioration des performances des dispositifs à grande mobilité actuels et mènera vers de nouvelles structures de dispositifs. En particulier, l'ingénierie d'interface à base de souffre (S) promet des structures à grille isolante basées sur l'InP, comme par exemple les HIGFET. Dernièrement, des études ont montré que la passivation InP/SiO_2 avec du souffre (S) donnait une faible densité d'états d'interface et que les MISFET à grille non-auto-alignée passivés ont des courants de dérive de drain négligeables . Malgré les aspects bénéfiques de la passivation à base de souffre (S) qui ont été rapportés, la nature exacte du mécanisme de passivation, sa stabilité en température et son application au procédé de grille auto-alignée ne sont pas connus. Ces importants résultats sont cruciaux pour le développement des futurs transistors à effet de champ à grille isolante (FET) sur InP.

Dans ce travail, on a étudié en détail la passivation de la surface de l'InP avec du souffre et on a expliqué comment se produit la passivation thermique avec du souffre, on a proposé un modèle universel sur la formation des couches de sulfure sur l'InP. On a réussi à appliquer le procédé de passivation pour la première fois au nitrure de silicium déposé par PECVD, utilisé comme grille isolante et ainsi démontré l'efficacité de la technique de passivation à base de souffre afin de contrôler la densité de défauts à l'interface InP/nitrure de silicium.

La surface passivée est stable jusqu'à T=700°C et la technique est appliquée pour la première fois afin de fabriquer des structures Métal-isolant-semi-conducteur (MIS) FET à grilles isolantes auto-alignées et des hétérojonctions à grilles isolantes (HIG) FET InP/InGaAs/InP. Un procédé technologique complet, convenable pour la passivation de grille métallique, incluant quelques nouvelles techniques de traitement a été développé. Un module (chip) de diagnostic a été mis au point afin d'évaluer les différents procédés, le dispositif et les paramètres du circuit. Les structures FET à grilles isolantes auto-alignées non passivées n'exhibent pas les caractéristiques d'un transistor, par contre ceux passivées au souffre possèdent une excellente caractéristique DC mais de modestes performances. Ce travail montre l'importance des techniques de passivation à l'interface pour les structures à grilles isolantes à base d'InP.

La passivation thermique de la surface de l'InP avec du souffre est étudiée en détail en utilisant des techniques analytiques telles que la photoluminescence (PL) , la spectroscopie de photo électron à rayon X (XPS) et l'XPS à résolution angulaire. À partir des mesures PL, il a été observé que la passivation réduit les lacunes de phosphore qui sont liées à l'émission des niveaux profonds dans la gamme de température 150-300°C. La dissociation du phosphore à la surface durant le recuit thermique conduit à la formation des lacunes de surface, qui sont très importantes pour les dispositifs à base d'InP. À partir des mesures XPS, on a montré que durant le recuit le souffre réagit avec le substrat d'InP selon le diagramme de phase ternaire In-P-S et forme une couche tampon In_2S_3 de 30 Å d'épaisseur. La diffusion du souffre S et la formation d'une couche de sulfure à la surface empêchent la diffusion du

phosphore P de la surface de l'InP, minimisant ainsi les niveaux profonds associés aux états vacants de P. Ayant identifié le mécanisme exacte du procédé de passivation thermique de l'InP, on a proposé un modèle universel de passivation portant sur la formation des différentes couches de sulfure, des monocouches jusqu'aux couches épaisses qui sont rapportées dans la littérature.

Le modèle proposé classifie les couches de sulfure en a) interaction photoélctrochimique de surface entre les atomes neutres de souffre S déposés à partir d'une solution et les états accepteurs associés à la surface d'atomes In conduisant à une monocouche S servant de couverture; b) réactions à l'équilibre du diagramme de phase assistées thérmiquement/plasma entre l'InP et S conduit à la formation d'une couche épaisse de sulfure. Ces dernières réactions sont divisées en régime de sulfurisation faible, intermédiaire et fort. Il a été remarqué que la passivation thermique entre 150-300°C correspond au faible régime de sulfurisation. La densité d'états d'interface à l'interface InP/nitrure est évaluée par des mesures C-V à haute fréquence sur des structures MIS passivées et non-passivées. Afin de fabriquer des capacités MIS, une nouvelle technique de dépôt du diélectrique a été développée, c'est la méthode par plasma indirect, qui est non coûteuse et évite d'endommager le substrat par le plasma. Les capacités MIS de InP/Si_3N_4, passivées exhibent à haute fréquence des caractéristiques C-V idéales avec un hystéresis négligeable (< o.1 V) et une densité d'états d'interface de $1x10^{11}$ $cm^{-2}.eV^{-1}$ et une densité égale à $8x10^{10}$ $cm^{-2}.eV^{-1}$ au milieu de la bande interdite. Par contre, les courbes C-V correspondant aux échantillons non-

passivés montrent de large hystéresis ainsi qu'une augmentation de la densité d'états d'interface à 0.15 eV en dessous de l'extrémité la bande de conduction.

Une étude préliminaire par spectroscopie transitoire des niveaux profonds (DLTS) a été effectuée pour évaluer l'énergie d'activation et la section efficace de capture des pièges d'interface à l'interface passivée au souffre. La passivation d'interface utilisant le souffre S montre une bonne stabilité thermique car les structures MIS conservent leurs caractéristiques C-V idéales même après un recuit allant jusqu'à 700°C. La passivation avec du souffre apparaît comme étant un bon candidat pour réaliser des structures à grilles auto-alignées sur InP.

Pour fabriquer les SAGFET passivés, on a développé un procédé technologique complet, comprenant l'évaluation du substrat, le nettoyage de la gaufre, l'isolation mésa, le dépôt par plasma indirect de la couche isolante Si_3N_4, l'implantation, son activation et la métallisation grille/contact. Les techniques rapportées dans la littérature ont été modifiées et de nouveaux procédés ont été développés. En particulier, une nouvelle méthode de recuit à lampe, à rampe lente (SRLA) et une nouvelle technique de déposition par plasma indirect. Une variété d'instruments de caractérisation sont utilisés pour optimiser ces procédures. un module de diagnostic avec des structures de test spéciales est crée pour vérifier la compatibilité de l'intégration des séquences du nouveau procédé,les différents matériaux, le procédé et les paramètres du dispositif. L'ensemble de test intégré utilise 5 niveaux de masques dont la dimension minimale d'un motif est de 1μm.

En utilisant les procédés de fabrication mentionnés et l'ensemble de masques, les premiers SAG MISFET et HIGFET passivés ont été fabriqués. Le

test des dispositifs a montré des caractéristiques de transistors bien définies, exhibant une faible conductance de sortie (g_o=0.05-0.38 mS/mm) et des performances modestes. Les MISFET du type accumulation et inversion ont exhibé une transconductance maximale (g_{mo}) de 10-12 mS/mm et 2-3 mS/mm respectivement tandis que pour les HIGFET la valeur maximale était de 30 mS/mm. Par contre, les FET non passivés mais fabriqués en utilisant le même procédé n'ont montré aucune propriété de transitor; ce qui implique que l'ingénierie d'interface à base de S est l'étape qui a permis d'obtenir des SAGFET et cela indique l'importance d'utilisation de ces techniques pour la fabrication de dispositifs à base d'InP. De plus, les MISFET à accumulation montrent un faible courant de dérive de drain (<6%) positif (DCD) sur une période de 10^4 secondes, comparable au courant de dérive négatif qui est associé à l'interface et aux pièges vacants de phosphore P. L'augmentation du courant de drain dans les expériences de (DCD) indique que la passivation contrôle la formation des sites vacants de P à l'interface.

Le recuit après fabrication a un impact important sur le procédé et les caractéristiques du dispositif. Un recuit à 400°C durant 30 minutes améliore les caractéristiques électriques des MISFET de type accumulation par contre cela dégrade les performances de ceux en mode d'inversion. À partir des mesures de lignes de transmission (TLM) on a pu estimer des valeurs minimales de résistivité de contact de 15 $\mu\Omega.cm^2$ pour les MISFET et HIGFET et des résistances de couches implantées correspondantes de 2-5 kΩ/¬ et 40 Ω/¬ respectivement.

Le problème majeure est l'incorporation du souffre S dans la grille isolante durant le traitement à haute température, causant un courant de fuite

de grille élevé, ce qui limite les performances des FET. De plus, le traitement de passivation chimique utilisé dans cette étude est assez non-uniforme et l'interface passivée présente des rugosités ce qui cause la réduction de la mobilité dans le canal. En utilisant un diélectrique plus dense et une autre couche épitaxiale servant d'interface, par exemple une couche sous contrainte de GaP, à large bande interdite, qui remplace la couche protectrice de sulfure d'indium, on pourra résoudre les problèmes de fuite et de non-uniformité et améliorer ainsi les performances du transistor. Néanmoins, l'étude révèle l'importance des techniques d'interface pour les prochaines générations de dispositifs à grilles isolantes et à grande vitesse. Il est attendu à ce que ce travail contribue à de sérieux travaux scientifiques et conduit au développement de techniques d'interfaces pour les semi-conducteurs III-V.

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TABLE OF CONTENTS

DEDICATION iv

SUMMARY v

RESUMÉ viii

ACKNOWLEDGMENTS xiv

TABLE OF CONTENTS xvi

LIST OF FIGURES xxi

LIST OF TABLES xxviii

OTHER ILLUSTRATIONS xxix

LIST OF ANNEXES xxx

INTRODUCTION 1

CHAPTER 1 - SURFACE PASSIVATION

1.1 Introduction 13

1.2 Thermal S passivation of InP 15

1.2.1 The passivation procedure 14

1.2.2 Photoluminescence experiments 17

1.2.3 X-ray photoelectron spectroscopy 25

1.2.3.1 Chemical nature of the surface 28

1.2.3.2 Thickness of the sulfide layer 34

1.2.3 The Passivation mechanism 36

1.3 A universal model for the formation of sulfide layers on InP 39

1.3.1 Surface interactions 40

1.3.2 Bulk interactions 48

1.3.3 Conclusions 49

CHAPTER 2 - FABRICATION TECHNOLOGY FOR SAG FETS

2.1 Introduction 52

2.2 Wafer characterization 53

2.3 Chemical cleaning and etching 60

2.3.1 The cleaning cycle 60

2.3.2 Iodic acid 61

2.3.2.1 Etch rate with concentration 62

2.3.2.2 Etch rate with temperature 63

2.3.2.3 Surface and profile 66

2.3.3 The phosphoric-peroxide mixture 69

2.4 The gate insulator 72

2.4.1 Limitations and solutions 72

2.4.2 Indirect plasma nitride 74

2.4.2.1 The indirect plasma system 74

2.4.2.2 Conditions for nitride deposition 75

2.4.2.3 The Si/nitride interface 76

2.4.2.4 Stoichiometry of the nitride 77

2.5 Ion Implantation 80

2.5.1 General considerations 80

2.5.2 TRIM simulations 81

2.5.3 Polaron measurements 82

2.5.4 Rapid thermal activation 83

2.5.5 Slow Ramp Lamp Anneal (SRLA) 84

2.5.5.1 Polaron profiles 85

2.6 Contacts 87

2.6.1 Transmission line model 89

2.6.2 Contact resistivity measurements 92

CHAPTER 3 - INTERFACE ENGINEERED MIS DIODES

3.1 Introduction 94

3.2 Fabrication of Interface engineered MIS capacitors 95

3.3 The dielectric on S treated InP 97

3.4 Dielectric leakage 97

3.4.1 I-V characteristics 97

3.5 The InP/nitride interface 99

3.5.1 C-V characteristics 99

3.5.2 Experimental results 102

3.5.3 Surface state density 104

3.6 Interface trap characteristics 107

3.6.1 Deep level transient spectroscopy 107

3.6.2 Experimental results 109

3.7 Temperature stability of the passivated capacitors 113

CHAPTER 4 - MASK SET DESIGN

4.1 Introduction 118

4.2 Criteria for diagnostic chip design 118

4.3 Design considerations 121

4.4 Test structures 122

CHAPTER 5 - DEVICE FABRICATION

5.1 Introduction 125

5.2 Samples 125

5.3 Chemical cleaning 125

5.4 Device isolation 129
5.5 Passivation 130
5.6 Gate dielectric deposition 131
5.7 Gate metal lift-off 131
5.8 Post metallization anneal 133
5.9 Implantation 133
5.10 Implant activation 134
5.11 Contact metallization 135

CHAPTER 6 - DC ELECTRICAL PERFORMANCE

6.1 Introduction 140
6.2 Performance of MISFETs 140
6.2.1 Accumulation type MISFETs 140
6.2.1.1 Current- Voltage characteristics 140
6.2.1.2 Gate leakage 141
6.2.1.3 Effect of annealing 143
6.2.1.4 Channel mobility 144
6.2.1.5 Uniformity 145
6.2.1.6 Drain current drift 147
6.2.2 Inversion Type MISFETs 148
6.2.2. Figure of merit 149
6.2.3 Unpassivated MISFETs 151
6.2.4 Conclusions 152
6.3 HIGFETS 153

CONCLUSIONS AND RECOMMENDATIONS 157

REFERENCES 163

ANNEXES 177

THE TEST CHIP

LIST OF FIGURES

Figure 1 Cross-section of a non-self-aligned MISFET. Note the overlap of the gate with the source / drain regions. 3

Figure 2 Cross-section of a conventional non-self-aligned HIGFET with gate/source and gate/drain overlap. 2DEG refers to the two dimensional electron gas channel that is formed at the heterojunction interface. 5

Figure 3 Cross-section of a self-aligned gate MISFET. Note that the source / drain regions are perfectly aligned to gate and the gate does not overlap these regions..... 8

Figure 1.1 8K PL spectrum from unsulfurized InP:Zn annealed at 250°C 18

Figure 1.2 A selective representative PL spectra of the deep level emission from (a) as-received InP:Zn and unsulfurized InP:Zn and annealed at temperatures of (b) 150, (c) 250 and (d) 300°C..... 20

Figure 1.3 PL spectra from (a) as-received InP:Zn and sulfurized InP:Zn annealed at temperatures of (b) 150, (c) 250 and (d) 300°C..... 21

Figure 1.4 PL spectra of (a) as-received InP and from untreated and S passivated InP:Zn samples that are annealed at temperatures of (b) 150, (c) 250 and (d) 300°C, and etched to remove the top 20Å surface layers 23

Figure 1.5 Representative curve fitted S_{2p} line from a sulfurized sample annealed at 250°C for 30 minutes. 29

Figure 1.6 Sulfur peak positions for standards and sulfurized samples. 30

Figure 1.7 The curve fitted P_{2p} line from a sulfurized sample annealed at 250°C for 30 minutes. 32

Figure 1.8 Comparison of the S_{2p} spectra from sulfurized samples annealed at 150, 250, and 300°C. 33

Figure 1.9 The semiconductor-electrolyte junction depicting the distribution of charge and electric potential. 41

Figure 1.10 A perspective view of the (100) InP surface with In and P dangling bonds giving rise to acceptor and donor states in the band gap. 42

Figure 1.11 Schematic of a) the energy band diagram of the electrolyte - n InP interface with partly filled acceptor surface states and b) creation of S° states at the interface following S deposition and the formation of In-S bonds due to charge sharing between filled acceptor states and the S° states. 44

Figure 1.12 Schematic diagram showing the formation of improved In-S coverage under high intensity above bandgap illumination. E_{Fn} and E_{Fp} represent the quasi-Fermi levels for electrons and holes respectively. 46

Figure 1.13 The In-P-S ternary phase diagram showing the various compounds that are formed for T < 408°C 48

Figure 2.1 Measured mismatch in parts per million (ppm) over the entire wafer. 55

Figure 2.2 High resolution X-ray diffraction fringe pattern of the epitaxial wafer. 56

Figure 2.3a 7K band edge PL spectrum of the InGaAs channel layer lattice matched to InP. 58

Figure 2.3b Scanning PL measurement to estimate uniformity of the epitaxial layers over the 2" heterostructure wafer 59

Figure 2.4 Variation of etch rate with wt. % concentration (C). 63

Figure 2.5a. Photomicrograph of the surface quality of a p-InP sample etched in 5 wt.% HIO_3. 64

Figure 2.5b. Photomicrograph of the p-InP surface quality following a etch in 30% HIO_3 64

Figure 2.6 Variation of etch rate with temperature for different wt % of HIO_3. 65

Figure 2.7a. SEM profile of the (100) p-InP sample etched in 20 wt.% HIO_3 along the [0 1 1] direction. 68

Figure 2.7b. SEM profile of the (100) p-InP sample etched in 20 wt% HIO_3 along the [0 1 $\bar{1}$] direction. 68

Figure 2.8. Variation of etch rate with relative concentration of H_3PO_4 70

Figure 2.9. Variation of etch rate with dilution for a 1:1:H_3PO_4:H_2O_2 solution 71

Figure 2.10. Variation of etch rate with temperature for a 1:1:H_3PO_4:H_2O_2 solution 71

Figure 2.11. Schematic drawing of the floating potential indirect plasma PECVD deposition apparatus used in the study. 74

Figure 2.12. Capacitance-voltage curves of Al/ Silicon nitride/ p-Si direct and Indirect plasma MIS structures. 77

Figure 2.13. ERD depth profile of indirect plasma nitride on Si substrate. 78

Figure 2.14 Polaron dopant depth profile of the 1x1014/ cm^2, 80 keV Si implantation activated by a 800°C RTA. 83

Figure 2.15 The 700°C SRLA anneal sequence used for implant activation. 84

Figure 2.16 Polaron dopant depth profile of the 1x1014/ cm^2, 80 keV Si implantation activated by a 800°C RTA. 86

Figure 2.17 Plot of total resistance (RT) with contact length. 89

Figure 2.18. a) Potential variation with separation of the unloaded contact and b) potential variation within a contact. 91

Figure 2.19 I-V characteristics of the Au-Ge-Ni contacts to a Si implanted and mesa isolated region arranged in a TLM structure with different contact separations. 92

Figure 3.1 ERD depth profile of indirect plasma silicon nitride on InP. 96

Figure 3.2. Leakage current Vs voltage characteristics of a) mildly sulfurized (S1) and b) strongly sulfurized (S2) Au/Ti/Silicon Nitride/undoped InP MIS diodes. 98

Figure 3.3. High frequency (100 KHz) C-V curves of sulfur passivated and unpassivated Ti/Au/Si3N4/undoped InP MIS capacitors. 102

Figure 3.4 The high frequency capacitance-voltage curves before

and after the 300°C anneal in forming gas 103

Figure 3.5. Variation of interface state density with energy in the InP bandgap calculated by the high frequency C-V (Terman) method for a sulfur passivated MIS diode. 104

Figure 3.6. Sulfur passivated MIS capacitor exhibiting small frequency dispersion and hysterisis in its C(f) - V characteristics..... 106

Figure 3.7. Sulfur passivated MIS capacitor exhibiting frequency dispersion due to extra parasitic resistance R_S 106

Figure 3.8. Typical DLTS spectrum of a S interface engineered MIS diode for two different rate windows.. 110

Figure 3.9 Leakage characteristics of S passivated MIS diode following a 700°C SRLA anneal. 114

Figure 3.10 High frequency C-V characteristics of a passivated MIS diode subjected to a 700°C SRLA anneal. 115

Figure 3.11 Frequency dispersion of passivated MIS diode (S2) after SRLA anneal. 115

Figure 4.1. Layout of the 4 level mask..... 120

Figure 5.1. Flow chart of the device fabrication sequence for SAGFETs..... 126

Figure 5.2. Schematic view of the wafer cross-section during different stages of processing..... 128

Figure 5.3. Photomicrograph of the amorphised silicon nitride regions and the gate metal following implantation. 136

Figure 5.4 A 1μm gate and the implanted silicon nitride regions following activation a 700°C SRLA anneal 136

Figure 5.5 Photomicrograph of the S out-diffusion near the edge of a 3 μm gate on a post implant annealed sample. 137

Figure 5.6 Photomicrograph of the completed HIGFET showing the gate and source/drain metallizations. 137

Figure 5.7 SEM photograph of the completed HIGFET showing the gate, source/drain and contact metallizations. 138

Figure 6.1 Drain I-V characteristics of a 5x200 μm^2 accumulation MISFET after annealing. 141

Figure 6.2. Gate leakage characteristics of the MISFETs. 142

Figure 6.3. Effect of annealing on MISFET transconductance 143

Figure 6.4. The $\sqrt{I_{DS}}$ Vs V_G plot to estimate channel mobility and threshold voltage. 144

Figure 6.5. Drain current drift of the accumulation type MISFET annealed at 400°C for 30 minutes. 147

Figure 6.6. Drain current-voltage curves of an as-fabricated 3x200 μm^2 inversion type MISFET showing excellent linear and saturation regions. 149

Figure 6.7. I_{DS} Vs V_G curve of the as-fabricated inversion MISFET. The curve indicates that leakage sets in before strong inversion is achieved. 150

Figure 6.8. The $\sqrt{I_{DS}}$ Vs V_G plot to estimate channel mobility and threshold voltage. 150

Figure 6.9. Drain current-voltage characteristics of an unpassivated MISFET. The characteristics do not change with gate voltage (V_G) 151

Figure 6.10. Drain I-V characteristics of an as-fabricated 2x200μm^2 HIGFET 153

Figure 6.11. Variation of transconductance with gate voltage of as-fabricated HIGFET. 154

Figure 6.12. The $\sqrt{I_{DS}}$ Vs V_G plot to estimate channel mobility and threshold voltage. 154

The Test Chip

LIST OF TABLES

Table 1.1 Ratio of the integrated intensity of the deep level emission in treated InP 20

Table 1.2. Parameters used for fitting the XPS peaks. 29

Table 1.3 Measured and calculated values of R and overlayer thickness for different temperatures. 35

Table 2.1 Bulk wafer specifications of manufacturer. 54

Table 2.2 Manufacturer supplied material specifications for heterostructure wafer. 54

Table 2.3a Peak positions of the P_{2p} and $In_{3d5/2}$ spectra. 66

Table 2.3b Atomic ratios of the etched surface. 66

Table 2.4 TRIM simulated range and straggle values for different material combinations for ion energies used in this study 81

Table 3.1 Position of DLTS peaks for different rate windows and gate bias 112

Table 3.2 Measured activation energies and capture cross-sections of interface states in the InP band gap for a S passivated MIS capacitor 112

Table 5.1 Parameters used for electron beam metal evaporation 132

Table 6.1 Transconductance (G_m), sheet resistance (R_{sh}) of implanted regions and contact resistivity (ρ_c) values of enhancement and inversion type, as-fabricated and thermally annealed, FETs monitored on sample dies 146

OTHER ILLUSTRATIONS

The test chip xxxviii

LIST OF ANNEXES

ANNEXE I: Single overlayer model xxxi

ANNEXE II: Capacitance - Voltage relationships for an ideal MIS capacitor xxxiii

ANNEXE III: Small pulse MIS DLTS analysis xxxv

INTRODUCTION

In order to understand the motivation for a work like this, we have to look beyond this narrow effort at the larger perspective. The one that defines the basic nature of human beings: the need to evolve. Evolution is a fundamental property of human beings. Except for periods of lethargy in history, we are constantly attempting to speed up this process in a systematic fashion. To what end - nobody knows, but let's hope it stays coherent and under control. The evolutionary process like any other in nature has matured in character from an urge to survive to a desire to understand the properties and order of the universe and engineer them to our advantage. Such comprehension and management requires effective communication coupled to information gathering and processing. As a result we have witnessed a steady increase in speed and volume in these areas. The modern day communication and information systems have a strong under-pinning in electronics and opto-electronics technologies that are semiconductor based. It is therefore natural for us to seek newer and faster semiconductor technologies.

III-V semiconductors such as Gallium Arsenide (GaAs), Indium Phosphide (InP) and their alloys are especially attractive since carrier transport is faster in these materials with higher peak electron velocities and mobilities than Silicon (Si). In addition, most of the III-V materials of interest possess a direct bandgap with the alluring possibility of assembling electronic and optical components on the same chip. The initial attempts to develop a bulk III-V technology by applying the techniques used in Si technology did not succeed for various reasons like material degradation during high temperature processing, difficulty to control

dopant diffusion, lack of a stable native oxide, surface Fermi level pinning etc. [1]. It became obvious that new technological strategies have to be adopted to address these issues. Such adaptations led to the development and maturity of the GaAs based MEtal Semiconductor Field Effect Transistor (MESFET) technology. The advent of advanced epitaxial techniques such as molecular beam epitaxy offered a new impetus to the III-V area by allowing lattice matched or strained growth of different binary, ternary and quaternary crystalline layers on a bulk single crystal substrate. A multitude of new exotic heterostructure devices immediately followed. Devices with tunable band gaps, strain layer superlattices, hot electron transistors, quantum well structures, wave guides and optical modulators based on refractive index variations, heterostructure lasers etc. The list is quite long and we are just exploring the tip of the iceberg. Although the immediate impact in terms of application is quite limited, these developments are expected to revolutionize the area of opto-electronics. This trend also saw the emergence of InP based heterostucture lasers and detectors that operate in the low loss 1.2-1.3 μm wavelength range suitable for optical communications. It was therefore highly desirable to develop a InP based FET technology to provide some amount of on-chip electronic circuitry with the optoelectronic components.

The major problem hindering a suitable MESFET technology was the low Schottky barrier height (≈0.2-0.3V) on n-type InP. One solution is to deposit/ grow a thin (≈50 -100 Å) tunnel oxide that increases the barrier height [2]. The most promising approach is to grow a epitaxial layer of a material that has a large Schottky barrier over the high mobility channel layer. Depletion type Metal Insulator Doped channel (MID)FETs fabricated using this approach show great potential and were first demonstrated by S.Bahl and J.Del Alamo of MIT [3,4].

However, leakage is still a problem and limits this approach for applications that demand a large dynamical voltage range and for low noise, low power requirements. For these purposes we need a Metal-Insulator-Semiconductor (MIS) type Insulated gate FET technology on InP.

As mentioned earlier, InP does not have a stable native oxide and attempts to grow one have failed miserably (1). Deposited insulators are used instead, but the InP/insulator interface is quite rough with a large concentration of

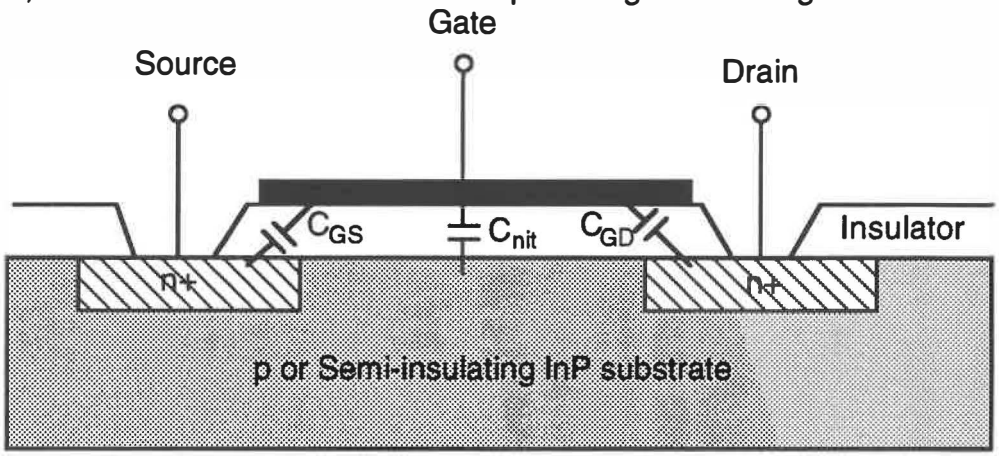


Figure 1 Cross-section of a non-self-aligned MISFET. Note the overlap of the gate with the source / drain regions.

interface states (> 10^{13} cm^{-3}) that reduce the channel carrier mobility [1]. Thus the advantages of using a high mobility material is lost. Another important consideration is the poor stability of InP to thermal anneals and plasma exposure. InP surface degrades quite easily even at moderate processing temperatures with the formation of Phosphorus (P) vacancies [1,5,6]. In fact, we show in chapter 1.2.2 that formation of P vacancies is inescapable during insulator deposition. In addition, high temperature processing causes the InP/insulator interface to degrade and become unusable. The first reports on InP MISFETs therefore used a non-self- aligned gate approach, shown in figure 1, that

deliberately avoids subjecting the interface to high temperature process cycles [6-8]. Although some groups reported impressive performance, slow traps at the interface cause the drain current to drift as high as 80% and the long term reliability of these devices is in question [9,10]. This drawback has been addressed and solved by R.Iyer and D.L.Lile [6,11]. Prompted by the success of Sulfur (S) passivation techniques that dramatically reduced the surface recombination velocity in GaAs [12], they applied this technique to achieve InP/SiO_2 interface with low surface state density and effectively suppress drift in non-self-aligned FETs without loss of performance. The mechanism responsible for this improvement is presumed by Wilmsen et. al. to be due to S filling up the surface P vacancies [13]. We study the passivation mechanism in detail and offer direct evidence in chapter 1 that S treatment reduces surface P vacancies. We show that passivation is due to the formation of a cap indium sulfide layer that suppresses P out-diffusion from the near surface regions of InP. However, it is generally believed that the S treated interface is quite rough and there are no reports of mobility enhancement in passivated surface channel devices to date and the uniformity of the passivation process is poor [6,11].

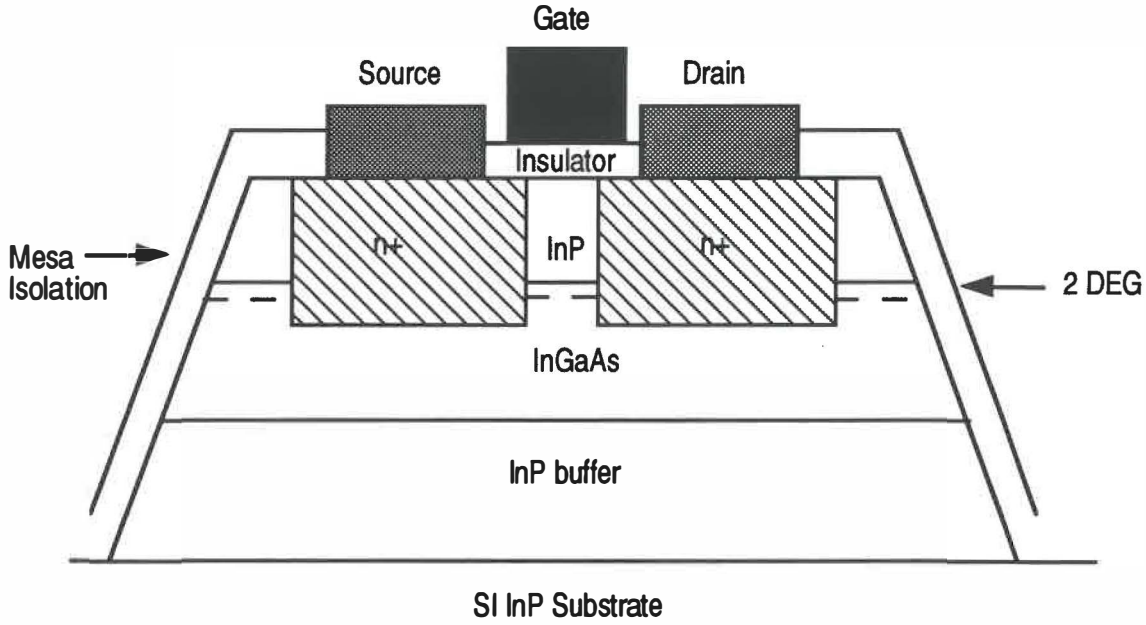


Figure 2. Cross-section of a conventional non-self-aligned HIGFET with gate/source and gate/drain overlap. 2DEG refers to the two dimensional electron gas channel that is formed at the heterojunction interface.

A parallel trend in III-V FETs has therefore been the development of Heterojunction Insulated Gate Field Effect Transistors (HIGFETs), where electron transport occurs at a high mobility heterojunction interface and the channel is physically separated from the low mobility insulator/semiconductor interface [14,15]. The cross-section of the HIGFET is shown in figure 2. The state-of-the-art technology is to use epitaxial insulators such as InAlAs that possess a larger band gap than the channel material, e.g. InGaAs [16,17]. The main requirements of epitaxial dielectrics are a large conduction band discontinuity (ΔE_c) and high resistivity. The lattice matched InAlAs technology offers a ΔE_c of 0.51 eV that restricts the maximum gate source voltage typically to 1.0-1.25 volts. In comparison, the barrier height of a conventional insulator is about 5-7 eV. The lower barrier heights of epitaxial insulators also restrict the high temperature operation and reduce the maximum charge holding capacity of CCD type

structures. The ideal solution is to epitaxially grow a lattice matched or strained layer of a high resistivity, large band gap insulator like BN or diamond like carbon etc. This is a technological challenge and has not been adequately realized yet. Lacking such a epitaxial insulator technology, use of conventional dielectrics for HIGFETs is still of interest. Recently, Martin et. al. demonstrated a non-self-aligned buried channel InP/InGaAs (ΔE_c = 0.3 eV) HIGFET using SiO_2 as the gate insulator [14]. Charge confinement in these devices is determined by the large insulator barrier while the confinement of the carriers in the channel is decided by the ΔE_c barrier. These devices show large transconductance due to carrier transport at the high mobility heterojunction interface and a large allowable (> ± 5V) input voltage swing. However a 20% Drain Current Drift (DCD) over 10^4 seconds at 300°K and considerable hysterisis in the C-V characteristics indicate a significant amount of traps at the insulator/InP interface. Lowering the interface state density at the top semiconductor/ insulator will lower DCD and result in better modulation of the channel charge and increase the small signal response [18,19].

The other aspect to this picture is that if compound semiconductor technologies have to become a viable alternative, they have to out-perform the ever shrinking Si electronics which increases in speed on a daily basis [20]. The pressure is even greater with the emergence of newer technologies such as Multi-Chip Modules (MCMs) that mount chips of different technologies close to each other eliminating parasitics that the different circuits appear to be part of the same Integrated Circuit (IC), for e.g. a MCM with a Si IC driving a III-V laser diode for all purposes is similar to a silicon IC with a on-chip laser diode. It is important to stress that these trends will effectively terminate interest in III-V

FETs if they don't catch-up. However, in favor of compound semiconductors we find that the electron mobility at the hetero-interface is much larger than the channel mobility at the Si/SiO_2 interface and III-V technologies such as HEMTs, HIGFETs etc., dominate Si in high frequency response [18,21]. The major advantage of Si MOSFETs is that the gate is aligned to the drain and source regions with minimum overlap and therefore minimum parasitic capacitance. Please refer to figure 3 for the cross-section of a self-aligned gate FET. So a decrease in channel length with other parameters unchanged will lead to a increase in speed and a larger cut-off frequency (f_t) given by [5]

$$f_t = \frac{g_m}{2\pi(C_{nit} + C_{GS} + C_{GD})} \qquad (1)$$

where g_m represents the transconductance, C_{nit} the insulator capacitance, C_{GS} the gate to source parasitic capacitance and C_{GD} the gate to drain parasitic capacitance. C_{GS} and C_{GD} are negligible for a self-aligned gate FET.

In contrast, since surface degradation of InP is a major concern, almost all InP based III-V devices reported in the available literature follow the non-self-aligned approach that avoids high temperature anneal cycles once the gate dielectric is deposited [6,7,10,14,22,23]. In non-self-aligned FETs the gate metallization has a minimum overlap of about 1 micron over the drain and source regions for alignment purposes as shown in figure 1. This overlap causes the parasitic capacitances C_{GS} and C_{GD} to dominate when device geometry shrinks to a micron or below and offsets any gain in performance. In addition, there are many associated process problems in fabricating non-self-aligned short channel

FETs and realization of self-aligned FETs would be essential for the future development of this technology [5].

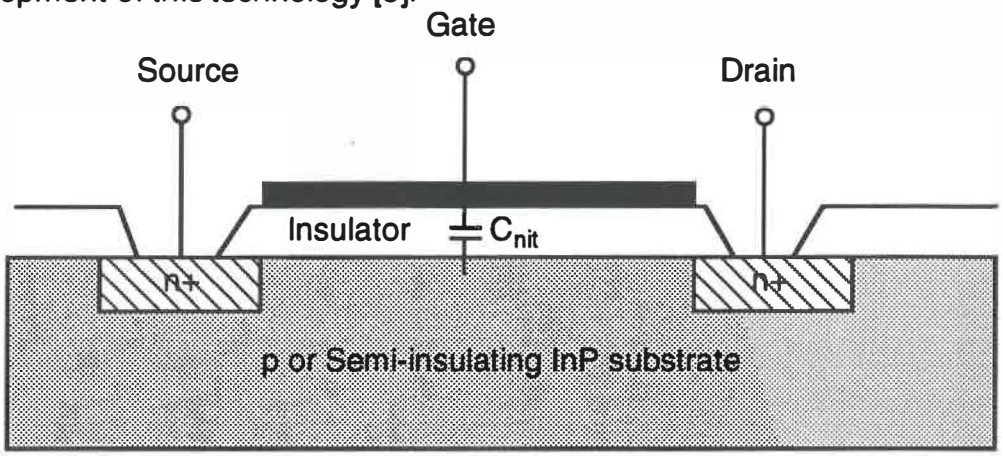


Figure 3. Cross-section of a self-aligned gate MISFET. Note that the source / drain regions are perfectly aligned to gate and the gate does not overlap these regions.

Very little work has been done to date to fabricate self-aligned structures on InP. There are only two reports in the available literature on self-aligned FETs on InP [24,25]. Both follow an approach very similar to the Si MOSFET technology with metal gates. The first report is by D.C.Cameron et. al. in 1982 [24]. They use a SiO_2 gate insulator and a Mo gate which also serves as the implant mask. They report impressive FET characteristics with channel mobilities of 1700-2400 $cm^2V^{-1}s^{-1}$. The second report is by K.Oigawa et. al. in 1987, who use a similar approach with W gates and silicon nitride as the gate insulator [25]. The 10μm gate length devices exhibit large transconductances of 55 mS/mm but show non-linear I-V characteristics. As pointed out in a review article by J.F.Wager et. al., these efforts could not be reproduced by other groups [5]. They mention that interfacial considerations have to be taken into account and observe that a high temperature anneal increases the InP/insulator interface density to an unacceptably large value and results in a large negative shift in the flatband

voltage. As seen in chapters 4&7, our own work shows that the Fermi level is pinned at the interface for such unpassivated self-aligned devices, probably due to an increase in interface state density associated with P vacancies. There are no reports to date on the fabrication of a InP/InGaAs Self-Aligned Gate (SAG) FET presumably due to such interfacial problems.

It is clearly obvious, that the next generation self-aligned gate HIGFET requires a technology strategy that should allow high temperature processing while maintaining a low defect density insulator/InP interface and a high mobility heterojunction interface [5,18]. In this report we propose, for the first time, that interface engineering based fabrication schemes are essential for this purpose and that such techniques open the door to self-aligned gate HIGFETs using conventional dielectrics. The term "interface engineering" refers to any fabricational procedure that conditions the interface to modify or ameliorate its electrical, thermal, microstructural, mechanical and optical properties. The III-V epitaxial technology abounds with such techniques. Some common examples are, buffer layers to stop substrate dislocations and provide a smooth interface [14], superlattices (SLS) to relieve interfacial stress [26] and trap carriers and large bandgap tunnel layers to increase Schottky barrier heights [2]. We would like to point out that interface passivation that usually alters the electrical or chemical nature of the surface is a subset of interface engineering [27]. As mentioned before, we are chiefly concerned about engineering a low trap density interface and increase its high temperature stability. The idea is motivated by our initial work to investigate the S passivation mechanism of InP, an enigma at that time [28,29]. The study identified that crucial to the passivation technique is the formation of a thin In_2S_3 layer that effectively checks P out-diffusion from the

substrate, especially at higher temperatures. In_2S_3 is a large bandgap material with better high temperature stability than InP. Our experiments show that this layer can stabilize the InP surface from degradation at temperatures as high as 300°C. It is quite possible that by depositing an insulator on top of the cap layer we should be able to protect the cap indium sulfide layer and the InP/insulator interface from thermal degradation at even higher temperatures. This logically translates into potential high temperature operation and a SAG process. We therefore proceeded to develop a SAG technology based on S interface engineering of the InP surface.

In the following chapters, we present our original detailed study of the S passivation process that elucidates the exact thermal S passivation mechanism. We show that S reacts with the InP substrate according to In-P-S equilibrium phase diagram forming a 25-30Å cap In_2S_3 layer that prevents P out-diffusion from the substrate. We also propose a universal model that describes the photo electrochemical and thermal kinetics involved in the formation of sulfide layers on InP, from monolayer coverage to thick sulfide layers. We extend the S passivation process formerly used with Plasma Enhanced Chemical Vapor Deposition (PECVD) Si_xO_y to PECVD Si_xN_y that has better thermal stability than the oxide. The interface state density at the InP/silicon nitride interface has been drastically reduced by the passivation process and the Fermi level is easily scanned over the entire bandgap. The passivated MIS diodes exhibit low mid-gap trap density in the $8x10^{10}$ $cm^{-2}.eV^{-1}$ range that is comparable to the best values obtained for silicon oxide. The MIS capacitors that use our passivation procedure are shown to retain their capacitance-voltage characteristics after thermal annealing upto 700°C, providing first evidence that interface engineering

techniques can control defect formation even at high temperatures. The associated III-V fabrication technology is modified for compatibility with a self-aligned interface engineered metal gate process. This includes developing a novel indirect plasma deposition technique and a new slow ramp lamp annealing sequence to activate the source/drain implantations. An exclusive diagnostic chip is designed with special structures catering to the self-aligned insulated gate process development, device fabrication and evaluation. Finally, interface engineered SAG FETs are fabricated for the first time. The devices that are subjected to a peak process temperature of 700°C show transistor action with excellent linear and saturation regions in their drain current-voltage characteristics, a low (6%) upward DCD over 10^4 seconds and modest performance. The measured peak transconductances (g_m) are 12 and 30 mS/mm for MISFETs and HIGFETs respectively [30]. Although these values are much lower than the g_m values reported for non-self-aligned FETs, they show for the first time that interface engineering is essential to realize a mature self-aligned insulated gate technology based on InP and other similar III-V semi-conductors. It is worthwhile to note that SAGFETs not incorporating the passivation step did not show any transistor action. The major problems associated with the chosen S passivation technique are degradation of insulator integrity leading to gate leakage, uniformity and mobility degradation owing to the rough nature of the passivated interface. We propose a novel epitaxial passivation strategy using GaP as a possible solution.

The interested reader should keep in mind that this work is aimed at the demonstration of an idea, namely the use of interface engineering techniques for a InP based SAGFET process, and at no time any serious effort is made to

improve or optimize device performance. With this prologue, you are invited to take a step into the world of interface engineered SAGFETs.

In chapter 1, the S passivation process is examined in detail and an alternate passivation mechanism is proposed. chapter 2 deals with the various processing aspects of the SAG technology. In chapter 3 we study the electrical properties of passivated MIS capacitors and use of the high frequency capacitance to assess the passivation process, the InP/nitride interface and its high temperature stability. This chapter also contains some preliminary Deep Level Transient Spectroscopy (DLTS) measurements to characterize the interface trap properties. Details of the developmental test chip used to fabricate and evaluate the SAG MISFETs and HIGFETs are outlined in chapter 4. The fabricational aspects of the interface engineered SAGFETs are covered in chapter 5 and their DC characteristics are presented in chapter 6. We conclude this report with a critical review of the merits and demerits of the chosen procedure and indicate a novel alternative interface engineering technique with suggestions for further effort in this direction.

CHAPTER 1
SURFACE PASSIVATION

1.1 INTRODUCTION

The term passivation as applied to semiconductors is the process which reduces the electrical and/or the chemical reactivity of a particular interface or surface [27]. Passivation thereby attempts to minimize material related interference of the charge transport and storage processes in semiconductor devices. Surface and interface passivation techniques have been extremely important in the development of the semiconductor technology. Indeed, it was only when the oxide/Si interface was under control that the MOS technology became widespread. These techniques have been widely used to reduce surface recombination velocity, to provide barrier layers and lower interface state density.

Here, we are mainly concerned about suppressing P vacancy (V_p) formation in the near surface regions, which occurs when InP is subjected to modest heating cycles. A large concentration of V_p related deep levels increases the surface state density and pins the Fermi level at the interface. When present in relatively smaller concentrations they act as scattering centers which reduce the channel mobility and transconductance (g_m) in MISFETs [5,9]. In addition, V_p formation is also largely responsible for the Drain Current Drift (DCD) phenomenon associated with InP MISFETs [9]. Van Vechten has proposed a mechanism by which the anion vacancy (V_p) hopping induced by the presence of an accumulated or inverted surface results in electron capture and leads to DCD in n-channel MISFETs [31]. It is therefore essential to suppress V_p formation at the InP surface during typical high temperature

process cycles. Various approaches have been tried that include using a P or P_2O_5 interface layer or maintaining a P over pressure during the dielectric deposition process [11,32,33]. Although, these techniques have been shown to improve the surface quality considerably there are associated problems of chemical stability in the case of a P_2O_5 interface and P over pressure leads to high gate insulator leakage.

Lile and Iyer were the first to demonstrate that chemical sulfur passivation of InP by $(NH_4)_2S$ at 60°C and subsequent SiO_2 deposition at about 250°C would result in a near ideal interface with low trap densities as observed by C-V measurements of MIS structures [6]. Their work was prompted by the considerable improvement of surface properties reported on sulfur passivated GaAs. It is interesting to note that the size of the sulfur atom is close to that of the P atom and S readily bonds to indium. Thus sulfur can easily replace a P vacancy without straining the InP lattice. In an effort to understand the passivation mechanism Wilmsen et. al. carried out XPS investigation of the InP surface, chemically treated by ammonium sulfide solution at 60°C and annealed at 250°C on a hot plate in an atmosphere of N_2 [13]. They observed the formation of In-S bonds and the absence of P-S bonds in the near surface regions of the InP sample and concluded that sulfur replaces the surface phosphorus resulting in the formation of a indium sulfide surface layer. Although they did not directly measure the surface V_p concentrations, they speculated that sulfur replaces the surface P vacancies. An earlier study by Gendry et. al. on the thermal sulfurization of InP by sulfur vapor identified the formation of In_2S_3 or In_2S_3 + $InPS_4$ complexes depending on the partial pressure of water vapor [34].

We have addressed the thermal sulfur passivation process in the temperature range which is normally used for dielectric deposition, viz. 150-300°C. PL measurements of the passivated and annealed InP surface conclusively prove the reduction of V_P related complexes by sulfur treatment [29]. We have performed angle resolved XPS measurements to determine the chemical state of the passivated surface and the extent of sulfur penetration into the substrate [28]. These results provide a good overall picture of the passivation process and we propose a passivation mechanism based on these results. Following this, we propose a universal model for the formation of sulfide layers on InP to explain the formation of the various sulfide layers.

1.2 THERMAL S PASSIVATION OF INP

1.2.1 THE PASSIVATION PROCEDURE

Liquid-encapsulated Czochralski grown (100) oriented bulk InP samples from Crystacomm, a California based company, are used in this study. The samples are degreased in organic solvents and subjected to the following chemical cleaning procedure: 1) 3 min. dip in a $1HF:1HCl:4H_2O$ solution to remove the native oxide, 2) 3 min. etch in a 10 wt.% HIO_3 to etch about 2000Å of the InP surface to remove any surface damage, 3) 3 min. polishing etch in a $1H_3PO_4:1H_2O_2$ solution to form a smooth surface and finally 4) a 2 min. dip in the solution of step 1 to remove the oxides formed during steps 2 and 3. The samples are dipped in flowing de-ionized (DI) water for 5 minutes after each cleaning step. The passivation process involves depositing a thin layer of elemental sulfur on the InP surface. This is done by immersing the InP sample in 15 ml of a 20wt.% $(NH_4)_2S$ solution in water maintained around 60-65°C for

30 minutes. Care is taken to not expose the semiconductor surface to air between the final cleaning and sulfurization steps. Ammonium sulfide dissolves in water according to the following reaction

$$(NH_4)_2S + 2H_2O \text{ -------> } 2NH_4OH + H_2S\uparrow \quad (1.1)$$

$$H_2S + H_2O \text{ -------> } HS^- + 2H^+ + OH^- \quad (1.2)$$

$$HS^- \text{ -------> } S\downarrow + H^+ + 2e^- \quad (1.3)$$

leading to evolution of H_2S gas (upward arrow) which can be identified by its pungent odor. The dissolved H_2S forms HS^- ions in the solution which dissociate and precipitate as elemental sulfur 'S' (downward arrow) out of the solution and deposits on the sample surface as a clearly visible coating. We thermally anneal the sulfur deposited samples in flowing ultrahigh pure N_2 at 150, 250 and 300°C for a constant time of 30 minutes. The temperature 150°C and 300°C represent the lower and upper limits that are normally used for dielectric deposition, while 250°C is the temperature often reported in the literature [6,35].

It should be noted that the S is present in its elemental form in the as-passivated sample surface and can be washed away by prolonged immersion in running DI water. This procedure has been studied in detail by Tao and Yelon [36]. They show that S provides a single monolayer coverage on a washed surface and forms a bridge bond between surface In atoms. As will be shown later in this chapter, such surface interactions can be explained in terms of photo electrochemical interactions.

1.2.2 PHOTOLUMINESCENCE EXPERIMENTS

Photoluminescence is a well proven non-destructive technique for detecting radiative levels associated with impurities and defect states in semiconductors [37]. This technique has been widely used to study a variety of surface related properties including surface state density and surface degradation via thermally induced defect formation [37,38,39]. In particular, this technique has been used to identify V_p complexes in InP in the 0.9 - 1.25 eV range. If S treatment does alter the V_p density, it should be observed in the photoluminescence spectra.

We prepared four series of samples from a p-type Zn doped wafer for these experiments aimed at comparing the emission spectra of defect states from untreated and S treated InP surfaces. The samples of series 1 and 3 are S treated and annealed at 150, 250 and 300°C. The samples of series 2 and 4 are etched but are not S treated and underwent the same annealing treatment. Finally, to ascertain that S passivation affects only the near surface regions and investigate its influence on the substrate defect density, we etched about 20Å of the top surface layers of the series 3 (S treated) and series 4 (untreated) samples in a $1H_3PO_4:1H_2O_2:10H_2O$ solution for 20 seconds. A detailed characterization of this etchant is given in chapter 3.

The PL is excited using the 514.5 nm line of an Ar^+ laser. The signal is dispersed by a 1 m spectrometer and detected by a liquid-nitrogen-cooled Ge *p-i-n* photo diode using conventional lock-in techniques. The sample temperature is maintained at 8K in a continuous flow helium cryostat. The excitation power density is held at 0.5 W cm^{-2}. The spectra are corrected for the system response.

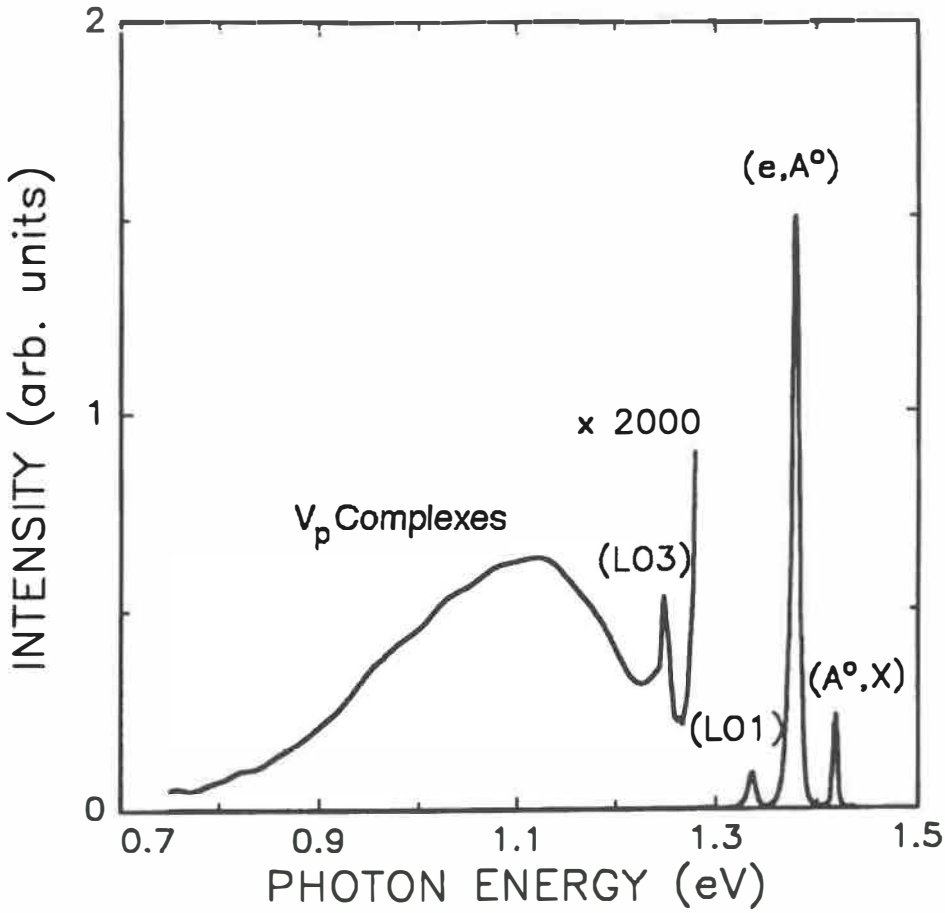


Figure 1.1. 8K PL spectrum from unsulfurized InP:Zn annealed at 250°C. The low energy curve is multiplied by a factor of 2000. Three peaks (A°,X), (e,A°) and (V_p) and two phonon replicas (LO1,LO3) are identified. Please refer to text for a more complete discussion.

Figure 1.1 shows the PL spectrum from an unsulfurized sample annealed at 250°C. The band edge emission in the range 1.25-1.42 eV is similar for all samples investigated. It consists of a bound exciton (A°,X) peak at 1.418 eV, a free-to-bound (e,A°) transition at 1.378 eV and several phonon replicas (LO1,LO3) of the latter. This emission is the same for all the samples investigated with negligible variations in intensity and we will not discuss the spectra in this energy range anymore. The lower energy curve marked "V_p complexes" between 0.75 and 1.25 eV is multiplied by a factor of 2000 and

represents emission from radiative deep traps in the InP bandgap. It is this region of the PL spectra that is of interest to us since phosphorus vacancy related deep levels are observed in this range as a band centered at 1.08 eV [38]. Significant differences in the PL spectra (b-d) were observed in this region for the untreated and annealed samples of series 2 as shown in figure 1.2. The spectrum (a) from the as-received sample is shown for comparison. We observe that low temperature annealing around 150°C leads to the creation of a broad peak centered at 1.14 eV. The absolute intensity of this peak grows with increasing temperature and the position of the maximum shifts to a lower energy value of about 1.08 eV. It is generally accepted that the 1.14 eV luminescence is related to Mn impurities in the InP lattice while the 1.08 eV luminescence is tentatively associated to a complex involving V_p [39]. It has been shown by Banerjee et. al. [40] that the broad luminescence feature at 1.14 eV is due to the combination of these emissions, and while the 1.08 eV peak grows considerably with thermal treatments in the range 500-550°C, the 1.14 eV peak does not show any significant change. We observe in our unpassivated samples a similar growth in intensity of the deep level PL signature and its displacement to a lower energy with annealing. Our results strongly corroborate the V_p peak assignment at 1.08 eV of the earlier studies [37,39,40]. We estimate the increase in magnitude of this band with temperature by comparing the integrated intensity with the as-grown sample. The values are tabulated under series 2 in table 1.1. For example, the deep level emission intensity from the 250°C annealed sample is about 12 times that of as-grown InP.

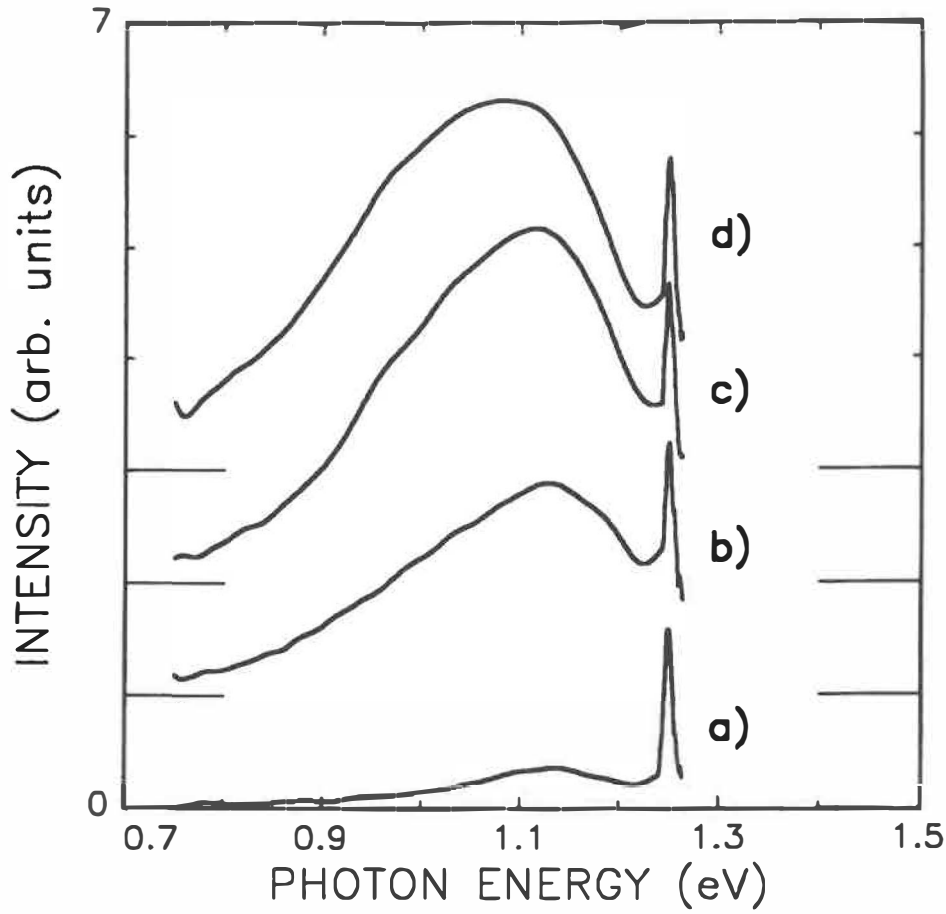


Figure 1.2 A selective representative PL spectra of the deep level emission from (a) as-received InP:Zn and unsulfurized InP:Zn (series 2) annealed at temperatures of (b) 150, (c) 250, and (d) 300°C.

Table 1.1 Ratio of the integrated intensity of the deep level emission in treated InP:Zn relative to as-grown InP:Zn.

Temperature(°C)	Series 1	Series 2	Series 3	Series 4
150	6.9	7.1	2.3	3.2
250	11	12	3.4	4.6
300	6.6	15	1.8	2.8

We conclude from this study, that P vacancy formation occurs when InP is annealed in the temperature range 150-300°C and its concentration increases with temperature. This work is the first to present direct evidence that V_P formation occurs at 150-300°C for 1/2 hour annealing, a temperature range and time frame commonly used in InP technology. From the stand point of insulated gate structures this essentially means that for untreated InP, formation of surface P vacancies is inevitable during insulator deposition at 250°C, the temperature popularly reported in literature.

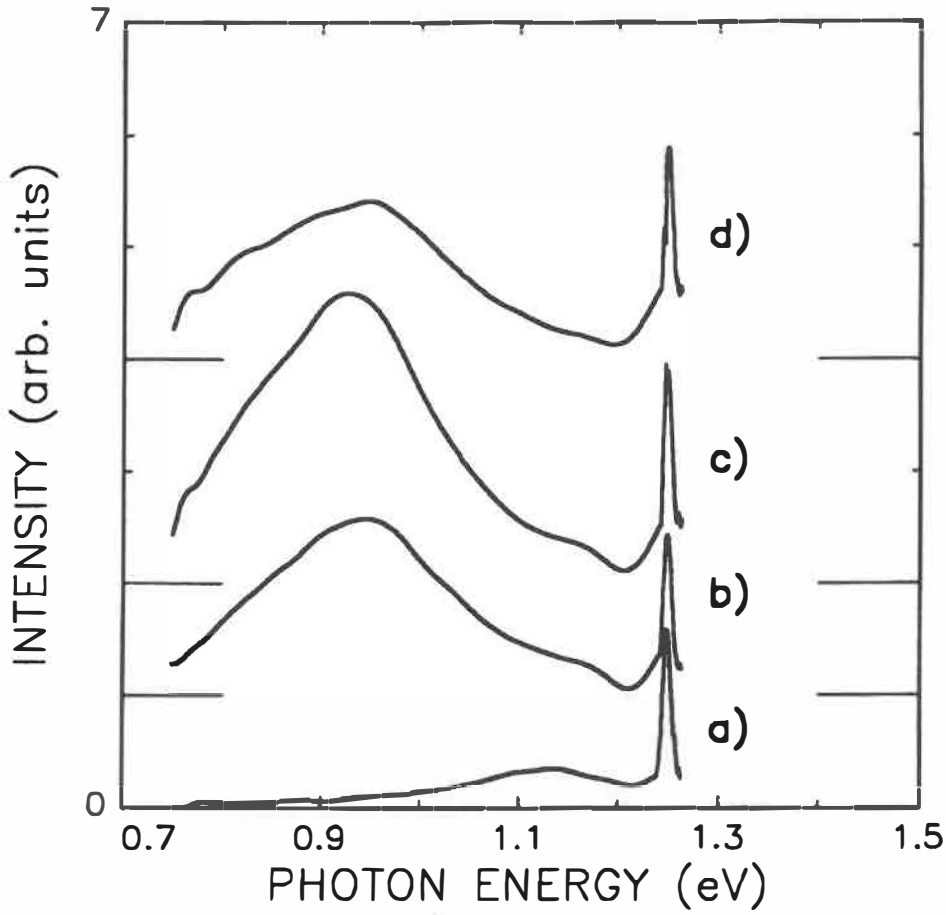


Figure 1.3 PL spectra from (a) as-received InP:Zn and sulfurized InP:Zn (series1) annealed at temperatures of (b) 150, (c) 250, and (d) 300°C.

We now turn our attention to the effect of S treatment on the PL spectra. figure 1.3 shows the spectra from the sulfur treated and annealed samples of series 1. Only the lower energy PL spectra between 0.75 eV to 1.25 eV is shown. The near bandgap emission is the same as figure 1.1. The essential features of these spectra are the appearance of a broad curve, centered at 0.93 eV. Unlike the spectra of unpassivated samples, this curve is neither displaced nor its intensity increases appreciably with annealing temperature. In fact, the measured intensity is least for the 300°C annealed sample. The intensity of the 1.08 eV ,V_p, band is considerably reduced and is now observed as a weak shoulder to the main 0.93 eV band . It therefore appears that sulfur treatment reduces the V_p concentration at the surface probably by sulfur filling up the phosphorus vacancies. In our original publication we attribute the 0.93 eV band to a S atom occupying a P vacancy in the InP lattice or in other words a S_P complex related deep center. We however show latter in this section and from our XPS results that this radiative center is associated with a cap indium sulfide layer that is formed when S reacts with the InP substrate and this layer is responsible for minimizing P vacancy formation at the surface. The marked reduction in the V_p (1.08 eV) luminescence intensity from the underlying InP substrate for the S passivated samples indicates reduced surface V_p formation. This work again is the first report in the literature that conclusively shows that S treatment of the InP surface prevents the formation of surface P vacancies. For insulated gate FET structures, this translates to a new technique to control P vacancy formation at the InP/insulator interface. On a wider perspective we can now think in terms of applying such interfacial techniques to control defect formation at any semiconductor interface.

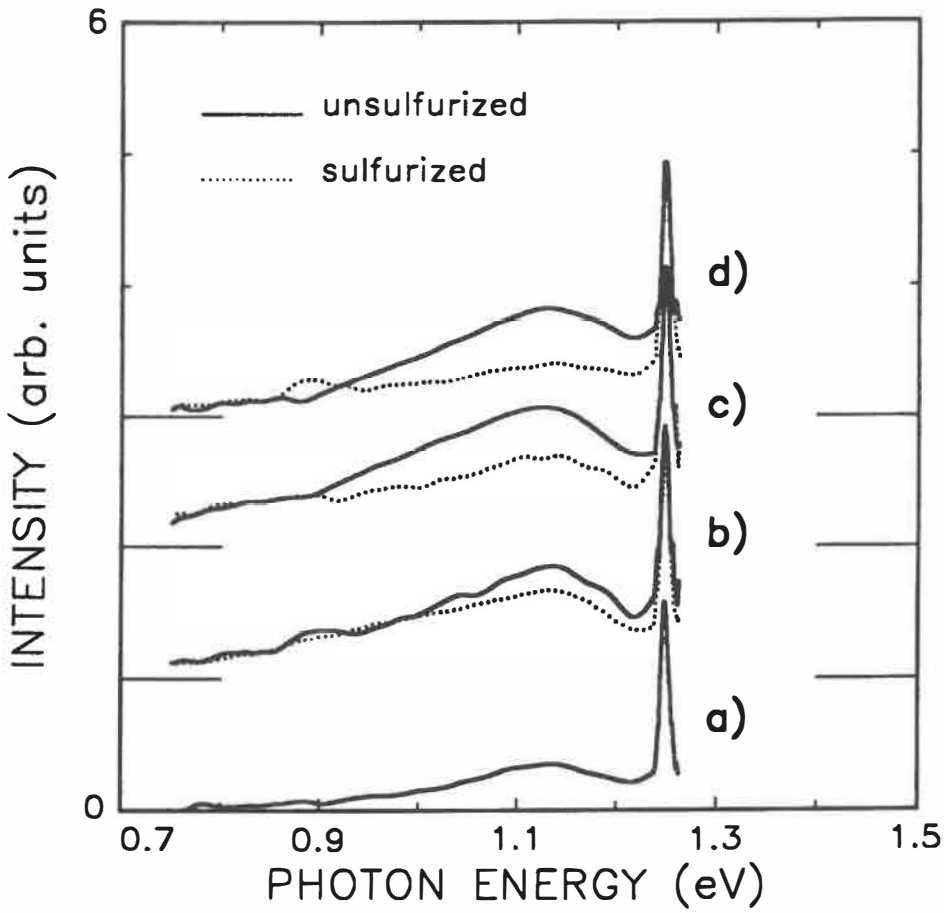


Figure 1.4. PL spectra of (a) as-received InP:Zn and from untreated (series 4) and S passivated (series 3) InP:Zn samples that are annealed at temperatures of (b) 150, (c) 250, and (d) 300°C, and etched to remove the top 20Å surface layers.

During the course of this discussion we have implicitly assumed that the effects we have observed are from the surface regions. Since the absorption length of InP at 514.5 nm is roughly 100 nm, the PL information is obtained from a depth equal to this absorption length plus the diffusion length of the minority carriers [37]. It is therefore possible that the observations made so-far are not surface but bulk related. To ascertain that these effects are from the semiconductor surface, we etched the top 20Å surface layers of the passivated (series 3) and unpassivated (series 4) InP samples that are annealed in the

temperature range 150-300°C. The results are shown in figure 1.4. The 0.94 eV band has now completely vanished for the passivated series 3 samples indicating that these deep states are associated to a cap layer that is completely etched away. We show in the following section from XPS measurements that a thin indium sulfide layer is formed during annealing. On the other hand, the 1.08 eV and 1.14 eV bands are related to the InP substrate as they can still be observed in the unpassivated samples of series 4 after etching. Interestingly, the series 3 (sulfur treated and etched) deep level emission intensities are systematically smaller than the untreated and etched samples of series 4. As seen from table 1.1 the integrated intensity of passivated series 3 samples is about 30-40% smaller than the untreated series 4 samples and about 3 to 7 times smaller than the unetched, unsulfurized samples of series 2. We can conclude from the marked reduction in PL intensity following a 20Å etch, that both the 0.94 eV and 1.08 eV bands originate from recombination centers located within the first few atomic layers of the samples. The former from a thin cap sulfide layer and the latter from the near surface regions of the InP substrate. Assuming that both unpassivated (series 4) and passivated (series 3) samples are etched to the same depth, reduction in the V_p complex intensity signifies that the cap sulfide layer is able to prevent degradation of the underlying InP substrate. Although S replacing P vacancies is a possibility, we did not observe any S_p related band in our experiments as such emissions would persist even after the cap sulfide layer is etched away. However, there is no report of S_p emission from InP and it may be that the states associated with S_p are not formed in the energy range investigated in the PL experiments. Surprisingly, the post-etch deep level luminescence intensity is least for the

passivated sample annealed at 300°C sample. As seen from the next section, this can be explained if a denser sulfide layer is formed at higher temperatures.

In conclusion, we show that the InP surface degrades with the formation of P vacancies when annealed in the temperature range 150 - 300°C. Our results corroborate the earlier V_p assignment of the 1.08 eV luminescence. We provide the first direct evidence that sulfur treatment reduces V_p formation in the near surface regions in the temperature range 150 - 300°C. Sulfur treatment appears to form a surface layer that gives rise to a deep level emission at 0.94 eV. The cap layer suppresses V_p formation in the underlying InP substrate by reducing the phosphorus escape rate. Both cap layer and V_p formations are limited to a few surface monolayers. The passivation is effective up to 300°C, the maximum temperature used in these studies.

As mentioned earlier, the passivation process can be used to control defect formation at the InP/insulator interface and its high temperature effectiveness can be advantageously used in a SAGFET process.

1.2.3 X-RAY PHOTOELECTRON SPECTROSCOPY

In the previous section, PL experiments provided the initial evidence for the formation of a surface layer containing S. We have used X-ray photoelectron spectroscopy (XPS) measurements to investigate the chemical nature and thickness of this surface layer. In the XPS technique the sample is irradiated with high energy X-ray photons that cause core orbital electrons of the substrate elements to be ejected from the surface regions of the sample. The kinetic energy of the photoelectrons depends on their binding energy to the particular atomic orbital which in turn is related to the chemical environment of

the particular element. By analyzing the energy of the emitted photoelectrons and comparing the spectra of the XPS peaks with those of standard samples we can identify the chemical nature of the surface [41]. The energy position of the peak shifts due to surface charging and is usually corrected by fixing the position of the carbon (C_{1s}) reference peak. The information depth is determined by the mean free path (λ) of the photoelectrons for the particular substrate [41]. For normal detection, i.e.. for a photoelectron take-off angle Θ = 90° measured with respect to the substrate, the photoelectrons that are usually within 3λ of the surface are collected and we obtain a maximum probing depth of 3λ. The value of λ is normally a few tens of Angstroms and this technique is therefore very sensitive to the chemical nature of the surface. By decreasing Θ we decrease the probing depth according to $3\lambda * \mathrm{Cos}(90-\Theta)$. For InP, λ is approximately 27Å and 3λ is about 81Å [42]. This is much larger than the depth of approximately 20Å we are interested in. We have therefore adapted the XPS technique to focus on the surface layer in more detail by measuring the photoelectron spectra at smaller values of Θ. In these experiments Θ was varied between 30 and 90° in steps of 20°. To change Θ, we tilt the sample's orientation with respect to the photoelectron analyzer.

Angle-resolved XPS technique also offers a nondestructive way to determine the thickness d of thin overlayers that are a few tens of Angstroms thick [43]. In this method, we measure the area of the XPS peak of interest for different take-off angles Θ. The XPS peak area is proportional to the number of photoelectrons emitted by the particular element. The photoelectron count is proportional to the illuminating area of the X-ray beam on the sample surface. For large Θ, this area can be much larger than the sample area and the number

of photoelectrons detected becomes proportional to the surface area *A* of the sample. Since the surface areas vary for each sample, we calculate the ratio *R* of the XPS peak areas (e.g. S/In, P/In etc.) of the elements. For thin over layers ($d < 3\lambda$), *R* of the element (e.g. S) that forms the overlayer changes with Θ. For $\Theta = 90°$ the contribution from the bulk InP is larger relative to the surface layer and for smaller Θ the signal from the surface is enhanced. We therefore monitor the Θ variation of the S/In area ratios. Indium is chosen as it forms a compound with S and its concentration in the surface regions does not change unlike P which disassociates from the surface. The measured S/In ratios for different Θ are then compared with those calculated from a single overlayer model, the fitting parameter being the thickness *d* of the overlayer. The actual thickness of the layer is then that value of *d* that gives reasonably close *R* values to those obtained experimentally. The precision of the fit is ± 2Å. The calculations for a single overlayer model are reproduced in Annexe I.

We performed XPS measurements in a VG system using a Mg Kα X-ray source. The angle-resolved XPS spectra are obtained by varying the photoelectron take-off angle (Θ), measured with respect to the substrate, between 30° and 90° in steps of 20°. To properly identify the chemical nature of the sulfurized surface, standard spectra of 99.999% pure S and In_2S_3 powder standards are also taken. The carbon reference peak is fixed at 285.5 eV for the analysis. Sensitivity factors of 3.9 and 0.54 are used for the In_{3d} and $S2_p$ lines respectively.

In the next section, we present the measured photoelectron emission spectra from the 2p orbitals of S and P. The 2p emission produces the prominent peak in the XPS spectra of these elements. Photoemission from p

electronic states with non-zero orbital angular momentum gives rise to a doublet (two peaks) in the XPS spectra corresponding to spin-orbital splitting of the 2p states into $2p_{1/2}$ and $2p_{3/2}$ states. The XPS peak area ratios of the $2p_{1/2}$ to $2p_{3/2}$ lines is 1:2. The energy separation of the peaks depends on the particular element but is a constant for a given compound/element. In addition the full-width half maximum (FWHM) is the same for both peaks. Therefore only the more intense, lower binding energy $2p_{3/2}$ line is considered for analysis and is referred to as the 2p peak in the following section. The In $3d_{5/2}$ spectrum from the passivated samples does not show any appreciable binding energy shift and was not useful for chemical analysis. However, the In peaks areas are used in the angle resolved XPS experiments to measure the thickness of the cap layer.

1.2.3.1 CHEMICAL NATURE OF THE SURFACE

The curve fitted S_{2p} high resolution XPS spectrum measured at a take-off angle of $\Theta = 30°$ for the sulfur treated sample annealed at 250°C is shown in figure 1.5. The reason for choosing the $\Theta = 30°$ spectrum is discussed later. From the fit we observe the presence of two sets of peaks. For the curve-fit, we have used the parameters of the In_2S_3 standard for the prominent lower binding energy 2p peaks marked "In_2S_3" and those of the elemental S standard for the secondary higher energy peaks marked "S". These values are listed in table 1.2 and provide a good fit to the measured data. The $2p_{3/2}$ spectra of the dominant peaks is centered at 161.9 eV and that of the secondary peaks at 164.12 eV. To determine if the S had reacted with the substrate and to identify the surface

chemical composition we compare the S_{2p} peak positions of the sulfurized sample with those of the In_2S_3 and S standards as seen in figure 1.6.

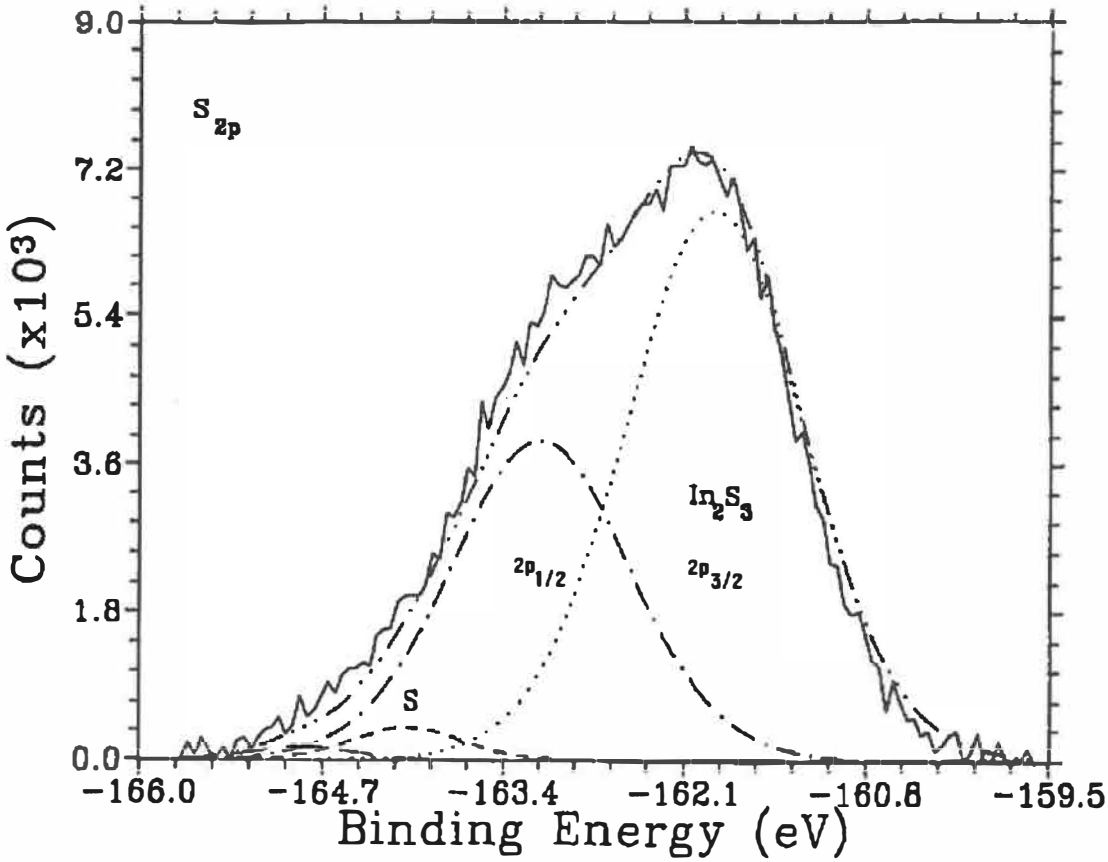
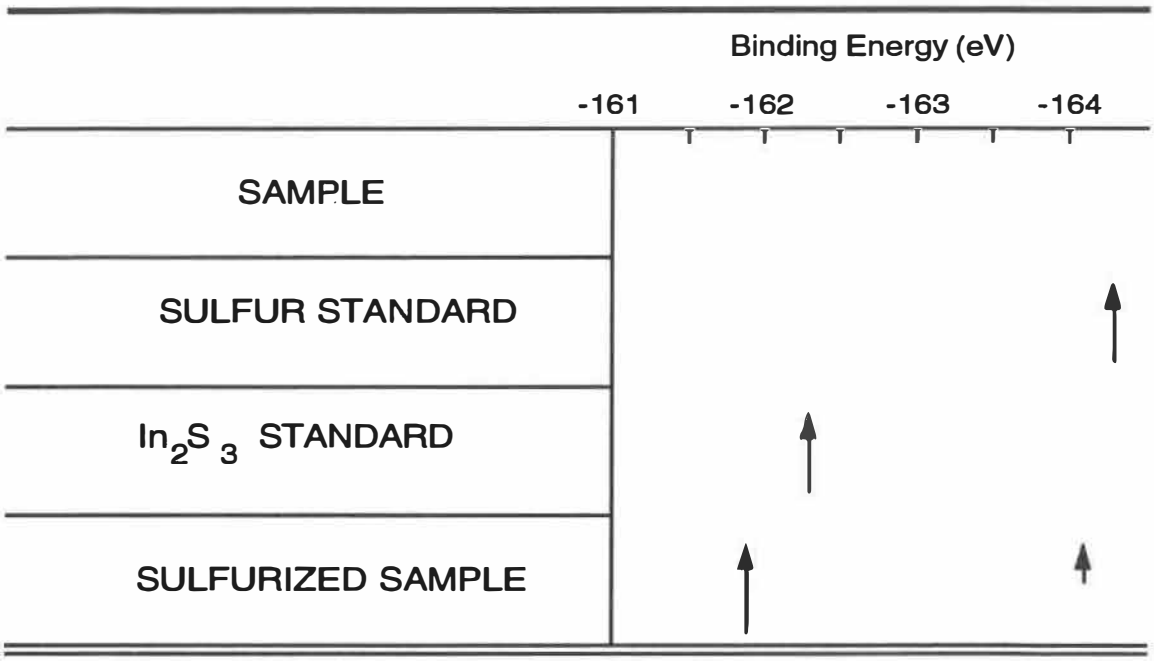


Figure 1.5. Representative curve fitted S_{2p} line from a sulfurized sample annealed at 250°C for 30 minutes. The take-off angle Θ is 30°. The solid line is the experimental data. The (. . . . .) and the (_ . _ . _) lines represent the $2p_{3/2}$ and the $2p_{1/2}$ peaks for In_2S_3 and the (_ _ _ _) lines represent the corresponding peaks for S. The (_ ... _ ...) line is the envelope of all the peaks.

Table 1.2. Parameters used for fitting the XPS peaks.

Sample	Element	FWHM (eV)	2p Peak Separation (eV)
In_2S_3	S	1.5	1.25
S	S	0.9	0.75
InP	P	0.75	0.83
P_2O_5	P	1.3	0.9



NOTE: C 1s reference at 285.5 eV

Figure 1.6. Sulfur peak positions for standards and sulfurized samples.

The bigger arrow for the sulfurized sample indicates the dominant S_{2p} peak and the smaller the weak secondary peak. We find that the position of the main peak (161.9 eV) from the sulfur-treated sample is shifted away from the elemental S standard and lies close to the S_{2p} line position of the In_2S_3 standard (162.3 eV). The energy difference of 0.4 eV from the standard is within the instrumental error (0.7 eV). This indicates that the S has bonded with indium to form either a In-S or a In-P-S compound. We shall show in the next part of this discussion that P-S bonds are absent in the sample surface and S in fact, reacts with InP during annealing to form In_2S_3. The secondary peak (smaller arrow) of the sulfurized sample is closer to the peak from the elemental S standard at 164.35 eV. This weak peak is detected only for the $\Theta = 30°$ spectra

and indicates the presence of some unreacted or unevaporated elemental sulfur on the sample surface.

From the S_{2p} spectra we conclude that S reacts with the InP substrate at 250°C to form a compound containing indium-sulfide bonds and a minuscule amount of elemental S is present on the sample surface.

According to the In-P-S ternary phase diagram that is shown later in this chapter, the equilibrium products when S reacts with InP are In_2S_3 and elemental P [34]. The earlier XPS reports of the S passivated and thermally annealed InP surface detected the formation of In_2S_3 but there was no evidence of elemental P. It was believed that the high volatility of P would lead to its absence in the sulfide layer after the thermal annealing [13,45]. As a result the conclusion that In_2S_3 was formed was based solely on position of the S_{2p} peak position and the absence of P-S compounds. Such an inference is ambiguous since the S_{2p} peak position measured on InP surfaces with a monolayer S coverage and an apparent stoichiometry of InS is the same as In_2S_3 [36]. The same is true for two dimensional In-S compounds [46]. These reactions do not proceed according to the equilibrium phase diagram and monolayer S coverage bonded to the top In layer of InP occurs even at room temperature [47]. If however elemental P is detected and P-S compounds are absent at the sample surface , we can be certain that the reaction follows the equilibrium phase diagram with formation of In_2S_3. As mentioned earlier in this section the top surface layer is probed in more detail by performing the XPS measurements at smaller values of Θ. We have used a Θ value of 50° to analyze the presence of phosphorus. At this angle we probe the top surface layers to a depth of 60Å.

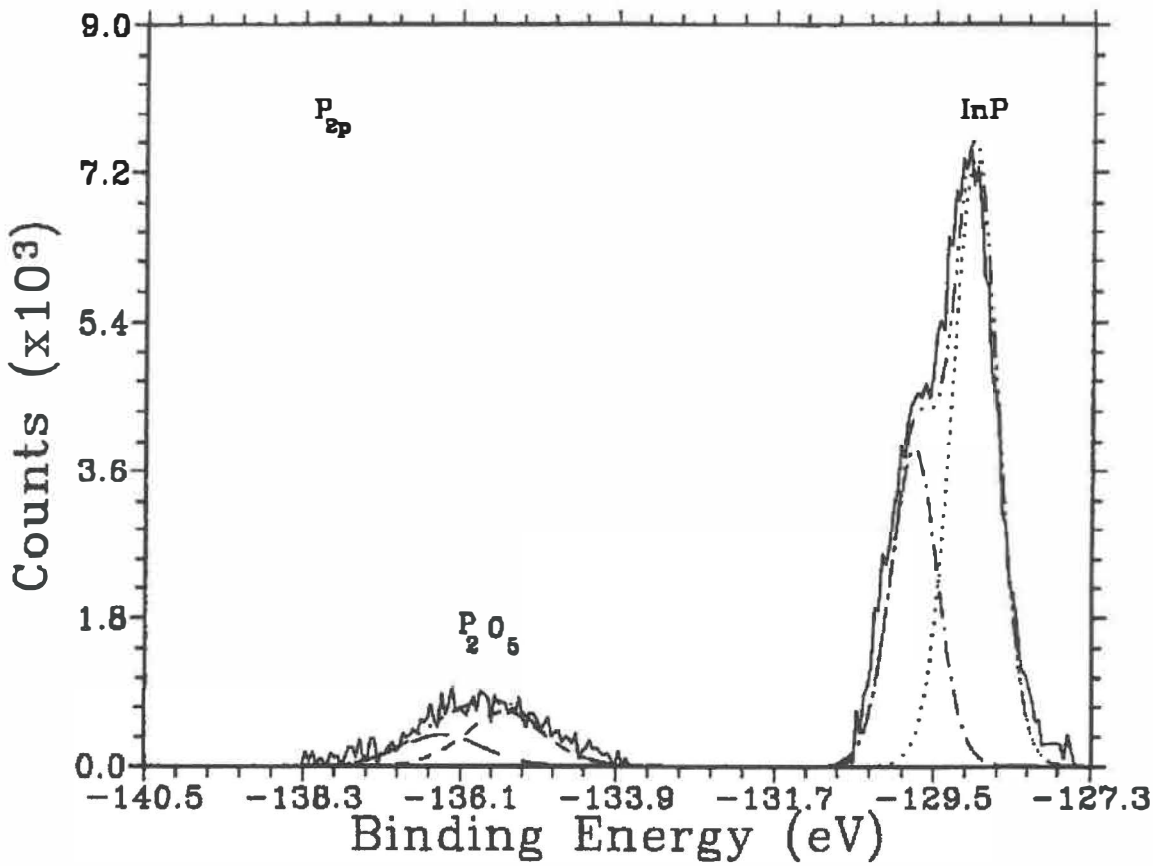


Figure 1.7. The curve fitted P_{2p} line from a sulfurized sample annealed at 250°C for 30 minutes. The take-off angle Θ is 50°. The solid line is the experimental data. The (. . . . .) and the (_ . _ . _) lines represent the $2p_{3/2}$ and the $2p_{1/2}$ peaks for InP and the (_ _ _ _) lines represent the corresponding peaks for P_2O_5. The (_ ... _ ...) line is the envelope of all the peaks.

Figure 1.7 shows a typical P_{2p} spectrum measured for the sulfurized sample annealed at 250°C. The strong InP substrate peak is present at 128.97 eV while a second peak is seen at 135.5 eV. The position of the latter peak corresponds to the oxide P_2O_5 [48]. This is rather intriguing since P_2O_5 is not a native oxide of InP and is definitely not formed during the passivation process. In fact, the ammonium sulfide solution dissolves the native oxides of InP and P_2O_5 is highly soluble in water. The only possible explanation for the presence

of P_2O_5 on the sample surface is that the elemental P that is formed when S reacts with InP during the thermal anneal, oxidizes on exposure to air. The intensity of this peak is quite small suggesting that part of the elemental P does indeed evaporate from the sample surface. It should be noted that this peak is barely observable for larger values of Θ and is usually lost when the background is subtracted before the curve fit. Since there are no other peaks present in the energy range 133.1-133.5 eV, we also conclude that P—S compounds which are formed for plasma sulfurization and $InPO_4$, the stable oxide of InP, are absent [48,49]. These results clearly indicate that thermal sulfurization of InP in the temperature range 150-300°C proceeds according to the equilibrium phase diagram with the formation of In_2S_3 + P. The elemental P that is formed in this reaction oxidizes to form P_2O_5 on exposure to air.

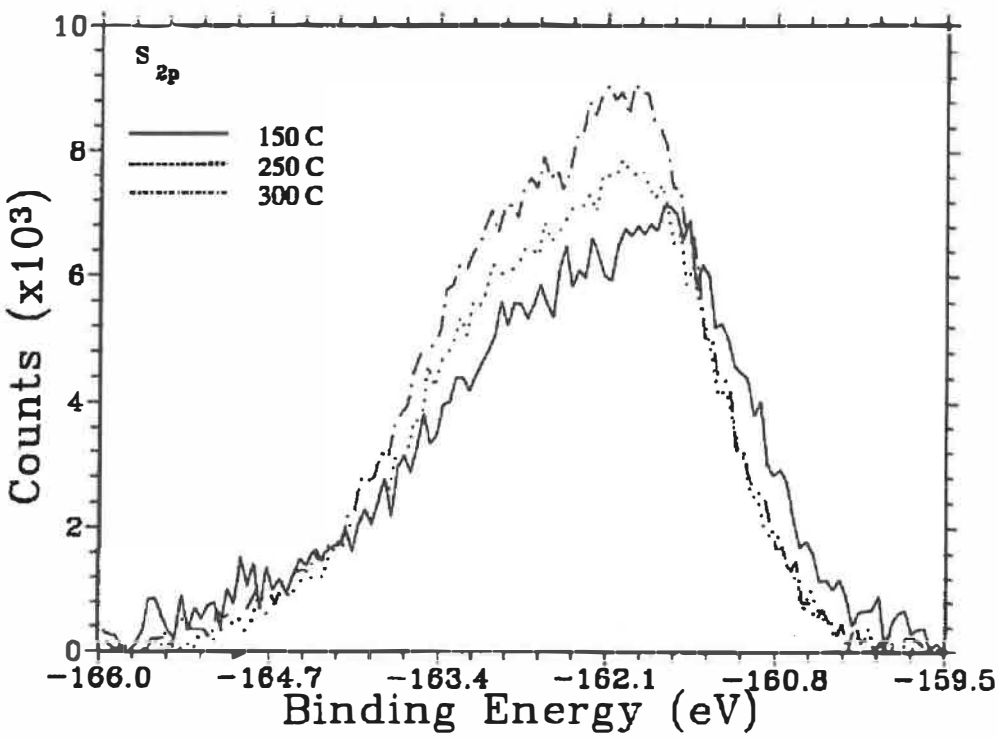


Figure 1.8. Comparison of the S_{2p} spectra from sulfurized samples annealed at 150, 250, and 300°C.

We find that the thermal sulfur treatment always results in the formation of In_2S_3 in the temperature range 150-300°C, as seen from figure 1.8 that compares the S_{2p} spectra of the samples annealed at 150, 250 and 300°C. The P_{2p} lines are also similar in this temperature range. Thermal sulfurization of InP between 150-300°C, therefore proceeds according to the equilibrium In-P-S phase diagram with sulfur reacting with the InP substrate forming a layer of In_2S_3 that contains a small amount of P_2O_5.

1.2.3.2 THICKNESS OF THE SULFIDE LAYER

In_2S_3 is a semiconductor with a band gap of 2.1 eV that is larger than InP. Formation of a higher band gap cap layer will have important consequences in MIS characteristics and MISFET operation depending on its thickness. It is therefore essential to measure the thickness of the top sulfide layer. We have used the angle resolved XPS method described earlier in this chapter for this purpose. The detailed calculation for overlayer thickness measurement is given in Annexe I.

For the calculation, a thin abrupt layer of In_2S_3 is assumed to be present. The area under the curve A(Θ) for any element is given as a summation over depth

$$A(\Theta) = C\int_0^{\infty} n(x)\exp\left(\frac{-x}{\lambda\cos\Theta}\right)dx \qquad (1.4)$$

where *n(x)* is the atomic concentration of the element and λ the mean free path of the photoelectrons.

From this equation, it can be easily shown that for a single layer model (see Annexe I)

$$R_{meas} = \frac{A(\Theta)_{[S]}}{A(\Theta)_{[In]}} = \left[\frac{N_{L(In)}}{N_{L(S)}} + \frac{N_{S(In)}}{N_{L(In)}} \frac{1}{\left[\exp\left(\frac{d}{\lambda \cos \Theta}\right) - 1\right]}\right]^{-1} \qquad (1.5)$$

where $N_L(In)$ and $N_S(In)$ are the indium concentrations in the sulfide layer and the InP substrate respectively, and $N_L(S)$ is the sulfur concentration in the In_2S_3 layer.

Table 1.3 Measured and calculated values of R and overlayer thickness for different temperatures.

Temp.	Ratio	Θ				Thickness
(°C)	S/In	90	70	50	30	*d* (Å)
150	$R_{meas.}$	0.45	0.55	0.68	0.92	27
	$R_{calc.}$	0.46	0.50	0.70	0.96	
250	$R_{meas.}$	0.55	0.52	0.64	0.74	29
	$R_{calc.}$	0.52	0.56	0.70	1.05	
300	$R_{meas.}$	0.57	0.55	0.58	0.67	31
	$R_{calc.}$	0.54	0.58	0.72	1.07	

Comparison of the experimental values $R_{meas.}$ with those calculated $R_{calc.}$ (table 1.3) indicate that the thickness of the In_2S_3 layer is around 30±2Å. The thickness increases very slightly in the temperature range 150 to 300°C. $R_{meas.}$ deviates appreciably from $R_{calc.}$ for large Θ values at higher temperatures. This deviation probably represents S loss by evaporation from the cap layer during the thermal anneal.

In this study we have conclusively shown for the first time that thermal sulfurization of InP is similar to thermal oxidation and follows the equilibrium phase diagram with the formation of a 30Å In_2S_3 layer. The elusive elemental P that is formed in the reaction has been finally detected in the sulfide layer in the form of P_2O_5. The cap layer however appears to degrade during annealing. Presence of an in-diffusing species like S forming a cap layer would inhibit P out-diffusion and is a key factor in understanding the exact passivation mechanism.

1.2.3 THE PASSIVATION MECHANISM

Let us first recap our results before describing the passivation mechanism. The PL results show that formation of P vacancies is inevitable when InP is annealed in the temperature range 150-300°C and the intensity of the V_p luminescence at 1.08 eV increases with temperature. S treatment of the InP surface leads to a dramatic reduction in the substrate V_p complex intensity at all temperatures. The thermal sulfur treatment also appears to form a surface layer that gives rise to a deep level emission at 0.94 eV which vanishes when the near surface regions are etched. Comparing the PL spectra after etching the top 20Å surface layers of passivated and unpassivated samples shows that the passivation suppresses V_p formation in the underlying substrate. From the XPS measurements, we find that thermal sulfurisation is very similar to oxidation and proceeds according to the equilibrium In-P-S phase diagram. The reaction between the elemental S and the InP substrate in the temperature range 150-300°C forms In_2S_3 +P. The elemental P oxidizes to form P_2O_5. The In_2S_3 layer is estimated to be approximately 30Å thick.

From these results we can conclude that formation of the cap In_2S_3 layer leads to a reduction in the V_P defect density in the underlying substrate. Although these results are in general agreement with those of Wilmsen et. al. who propose that the passivation mechanism is due to sulfur replacing P vacancies and forming an In_2S_3 - InP heterojunction, our conclusions are different and we present an alternative passivation mechanism [13,29]. From our results it is quite obvious that In_2S_3 is formed by the equilibrium reaction of InP+S as predicted by the In-P-S phase diagram. The energy necessary for this reaction is supplied in these experiments by thermal annealing. Since sulfurisation is similar to oxidation, presence of an in-diffusing species like S will prevent the out-diffusion of a substrate element like P with reduced vacancy formation in the underlying substrate. Moreover, once the cap layer is formed, its presence will reduce the phosphorus escape rate from the substrate. The reduced V_P intensity at 300°C is probably related to the cap layer formation. Similar to dry oxidation processes, at higher temperatures, a denser sulfide is formed preventing more efficiently phosphorus loss from the substrate. Due to its size similarity with P, the in-diffusing S can also replace any P vacancies at the In_2S_3 / InP although we do not have any direct evidence for S_P formation.

It is interesting to note that deliberately deposited capping layers are commonly used in III-V technology to prevent the group-V-element loss from the substrate during high temperature processing. In the case of sulfurized InP, the In_2S_3 layer acts as a natural cap that prevents V_P formation in the underlying InP substrate during the thermal anneal and during subsequent high temperature processing steps. This technique is able to control defect formation at the InP/sulfide interface up to 300°C. The cap sulfide layer however appears

to degrade during annealing. By depositing an insulator on the cap layer, this degradation can be prevented and the passivation mechanism can be effective at even higher temperatures. We shall show in chapter 4 that by depositing silicon nitride on the passivated InP surface we are able to preserve the C-V characteristics of MIS structures at temperatures as high as 700°C. The high temperature passivation scheme is extremely attractive for a SAGFET process and we demonstrate the feasibility of passivated SAG MISFETs and HIGFETs that use a 700°C implant anneal in their fabrication.

As mentioned in chapter 1 and observed later in chapter 7, the nature of the solution deposition method, makes an uniform S coverage and therefore a uniform sulfide layer over the sample surface hardly possible. Moreover, reproducibility is a problem since the available commercial solutions are known to vary in chemical composition. As seen in chapter 7 interfacial roughness is another problem of concern and greatly reduces channel mobility. As a result, we suggest the use of a novel, inherently uniform epitaxial interface engineering techniques that duplicate the function of the sulfide cap layer. One such would be the growth of a thin (≈ 30Å) strained epitaxial GaP layer on the InP substrate. GaP has a larger band gap (2.26 eV) than InP (1.35 eV) and has a larger thermal stability (T_{mp}= 1738°K) and does not dissociate at the temperatures used for insulator deposition. The cap GaP layer is expected to efficiently suppress P vacancy formation in the underlying InP substrate. Moreover, the epitaxial layer can be grown very uniform and the epitaxial InP/GaP heterojunction interface is expected to be very smooth and support high mobility.

1.3 A UNIVERSAL MODEL FOR THE FORMATION OF SULFIDE LAYERS ON INP

During the course of this discussion we have shown that sulfur passivation of the InP surface between 150-300°C was in the equilibrium reaction regime with the formation of In_2S_3 + P. However, the recent literature is full of different solution [6,28,36,47,50] gas [51] and plasma [52,53] sulfur treatments and each technique produces distinct sulfide layers with diverse surface properties. The confusion is compounded as some research groups propose monolayer or sub-monolayer coverage of S atoms on the surface [36,47,54], while others report formation of thin [13,8] and thick sulfide layers [52,53]. Surely, monolayer and sub-monolayer S coverage do not follow the equilibrium phase diagram and a different mechanism is responsible for the formation of these sulfide layers. Confronted with such a plethora of information, it is often not clear which method would be appropriate to passivate the InP surface. We present for the first time the common link between these seemingly diverse techniques. In particular, we concentrate on the solution techniques using $(NH_4)_2S$. It is shown that all passivation schemes operate in one of the two regimes of sulfide formation, namely 1) photo electrochemical charge transfer interactions at the InP/electrolyte (NH_4S_x) interface leading to monolayer or sub monolayer S coverage of the InP surface and 2) chemical reactions between deposited S and InP that follow the In-P-S equilibrium phase diagram and result in thicker sulfide layers. We show that our passivation procedure is in a mild sulfurisation regime predicted by equilibrium thermodynamics.

1.3.1 SURFACE INTERACTIONS

Here surface interactions are referred to those processes that lead to monolayer or sub-monolayer S coverage of the InP surface. Tao et. al. have shown that illumination and heating are necessary to achieve complete monolayer S coverage of the InP surface [36]. Although not explicitly stated in the article, their results suggest that a photochemical reaction might be involved in the formation of surface S bonds.

Recently, Bessolov et. al. have proposed a model that explains the formation of S-B^V (B^V atoms in this case refers to P atoms) bonds in III-V semiconductors as a photo electrochemical reaction involving charge exchange between H^+ and S^{2-} ions in the solution and the III-V substrate [55]. The 2-step charge exchange model considers only the donor-like states associated with B^V atoms at the surface and does not explain formation of S-A^{III} (In) bonds that are the only bonds normally observed for solution treatments. In fact, P-S bonds are not observed in solution treated InP samples and are assumed to be soluble in the alkaline $(NH_4)_2S$ solution. Moreover in the pH range of the commercial solutions, HS^- ions and not S^{2-} ions are dominant in the electrolyte. The model therefore falls short of completion and does not pertain to solution treated InP.

In the following sections we examine a photo electrochemical pathway that bonds S atoms to the surface In atom. It is shown that the neutral S atoms deposited from the sulfide solution can share electrons with acceptor states related to surface In atoms and form In-S bonds. Above band gap illumination is shown to improve the coverage and heating enhances S precipitation. This

work extends the recent report and provides a complete mechanism for monolayer S coverage of the InP surface.

When an electrolyte is in contact with a semiconductor at room temperature, the chemical potential of the solution and the Fermi level of the semiconductor should align by charge exchange at the solid/liquid interface. The Fermi energy describes the chemical potential of a semiconductor. This interaction creates a space charge region with a built-in potential as shown in figure 1.9 [56]. The space charge regions can be depletion or accumulation regions in the semiconductor and a Helmholtz double layer ion distribution in the electrolyte.

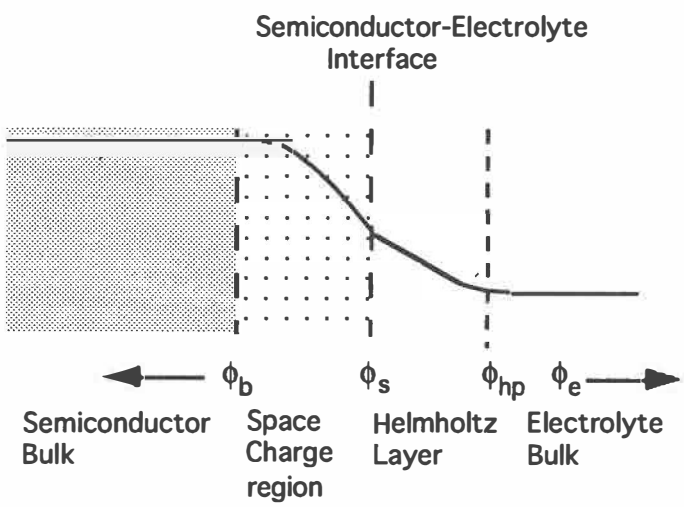


Figure 1.9 The semiconductor-electrolyte junction depicting the distribution of charge and electric potential.

As an example, we consider the case of n-InP in contact with the electrolyte $(NH_4)_2S$. Electrochemical alignment will result in the formation of a depletion layer of positive donor ions and a Helmholtz double layer with negative ions near the interface. The charged regions will create a built-in field

that will maintain the ion concentrations in the near surface regions. In the case of a semiconductor and a concentrated electrolyte (>0.1M) this junction behaves like a Schottky barrier with a constant potential drop across the Helmholtz layer and a larger potential is dropped across the depletion region of the semiconductor [57]. Under room illumination conditions, the potential drop is still present and removes any excited electrons in the semiconductor from the near interface region towards the semiconductor bulk. In addition, the field also dictates the concentration of anions and cations at the interface.

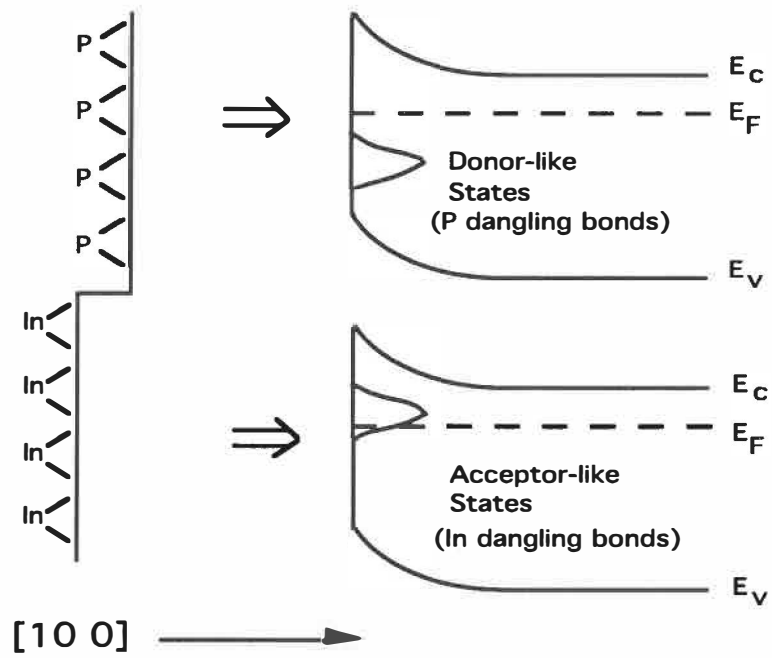


Figure 1.10 A perspective view of the (100) InP surface with In and P dangling bonds giving rise to acceptor and donor states in the band gap. The atomic surface diagram on the left is a conceptual representation showing In or P terminated (100) planes.

It is known that the alkaline sulfide solution dissolves the native oxides of InP. This results in a (100) surface with atomic planes having P or In dangling bonds as shown in figure 1.10. These dangling bonds usually form states that

are either donor-like or acceptor-like [1]. Donor-type states are neutral when occupied while acceptor-like states are neutral when empty. In the absence of surface relaxation, tight-binding and self-consistent pseudo potential calculations predict that these surface states are formed inside the band gap of InP. Acceptor-like In dangling bonds are estimated to be close to the conduction band edge and occupied donor-like P dangling bonds have been measured close to the valence band edge [1]. In the case of GaAs, Ga dangling bonds have been experimentally determined to form acceptor-like states close to the conduction band edge and occupied donor-like As dangling bonds are postulated to be about 1eV below the valence band edge [58,59]. In the presence of surface states, the semiconductor surface would be neutral if the donor-like states lie below the Fermi level and acceptor-like states above the Fermi level. If however a portion of these states are empty or filled the surface would be charged accordingly and the band bending and the built-in potential altered [60].

Figure 1.11a shows the initial condition of the electrolyte-semiconductor (n-InP) junction at room temperature and illumination. The positive H^+ ions in the solution form unoccupied electron states centered at E_{ox} while the negative ions give rise to the occupied states about E_{red}. The E_{redox} level defines the chemical potential of the electrolyte. The semiconductor Fermi level is aligned to the E_{redox} level resulting in a depletion layer inside the semiconductor. Depending on the position of the bulk Fermi-level a part of the In related acceptor-like dangling bonds are occupied.

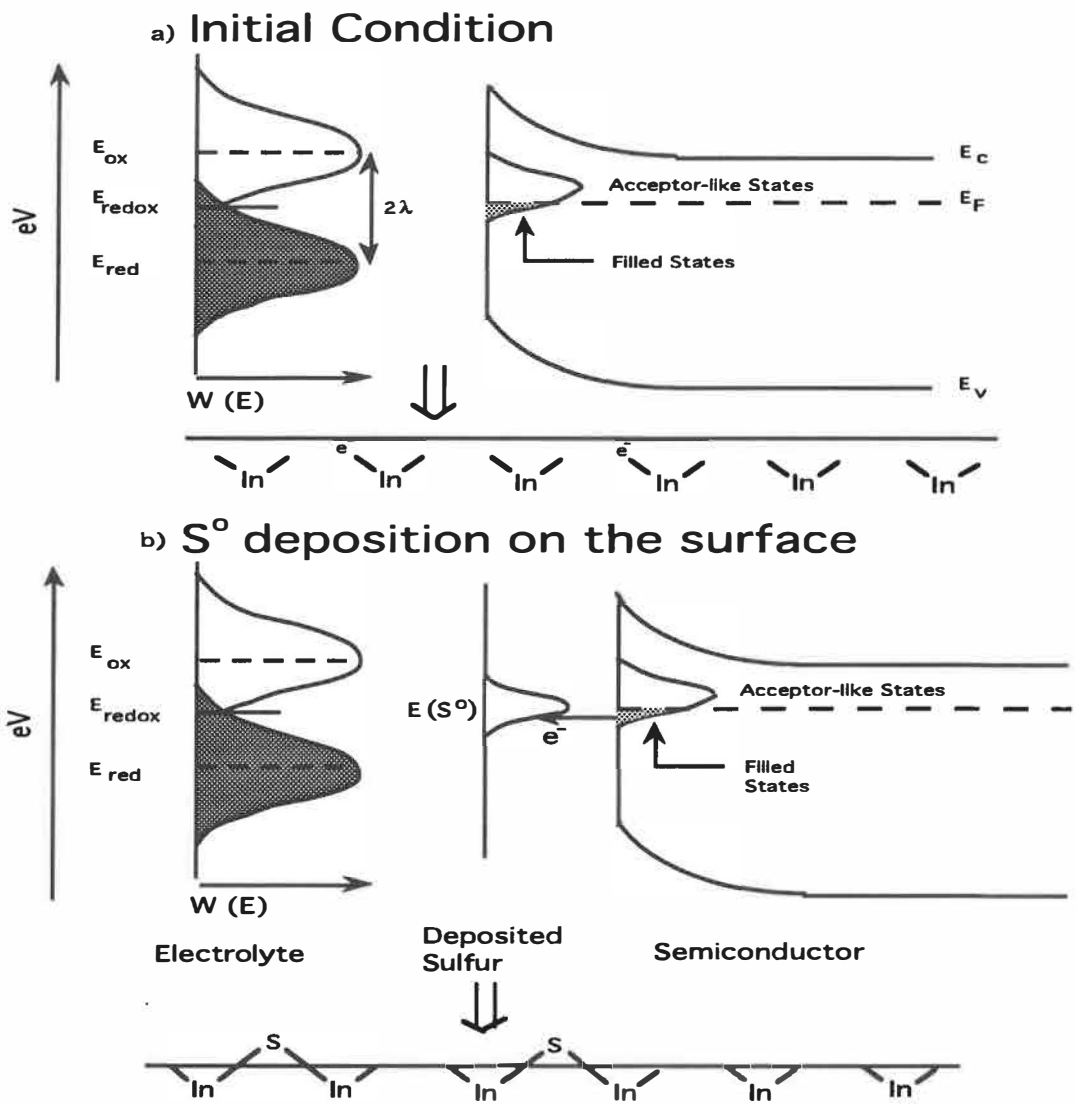


Figure 1.11 Schematic of a) the energy band diagram of the electrolyte - n InP interface with partly filled acceptor surface states and b) creation of S° states at the interface following S deposition and the formation of In-S bonds due to charge sharing between filled acceptor states and the S° states. The atomic surface diagrams at the bottom of each figure are drawn conceptually to indicate filled acceptor states and In-S bond formation. The states labeled E(S°) are drawn in perspective to indicate that the S atom can share two electrons to complete its valance orbital.

As described earlier in this chapter S is precipitated from the $(NH_4)_2S$ solution and deposited on the sample surface during treatment. It is interesting

to note that in most techniques sulfur/polysulfide precipitation is aided by adding excess sulfur/polysulfide or by adding a few drops of an acid to the solution [47,50,54,61]. In our previous experiments [28], we have observed S precipitation to be enhanced by heating similar to others [6,13,36].

Figure 1.11b describes the situation when the precipitated S° atoms are adsorbed to the InP surface. In drawing figure 1.11b it has been implicitly assumed that the neutral S° coverage of the surface does not affect the band bending [57]. The filled valence states of the S atoms will coincide with the Fermi level of the semiconductor and overlap the filled acceptor-like states. The states labeled $E(S^{\circ})$ are drawn in perspective to indicate that the S atom can share two electrons to complete its valence orbital. Charge sharing with acceptor states of the same energy results in the S atoms being bonded to the surface In atoms. Formation of a In-S bond will move the acceptor state from the bandgap to the valence band of the semiconductor. By this we do not imply complete removal of surface states as the surface S atoms will now give rise to another distribution of surface states [51,62]. However, we note under room temperature illumination only a portion of the of the surface acceptor states are filled leading to sub-monolayer S coverage. When the surface is exposed to high intensity above bandgap illumination, optical electron-hole-pair generation at the near surface regions splits the Fermi level into quasi Fermi levels, E_{Fn} and E_{Fp}, for electrons and holes respectively as depicted in figure 1.12. The large surface carrier density will tend to flatten the bands and increase the occupational probability of an acceptor state [57]. This will enhance the reaction rate and lead to a more complete S coverage.

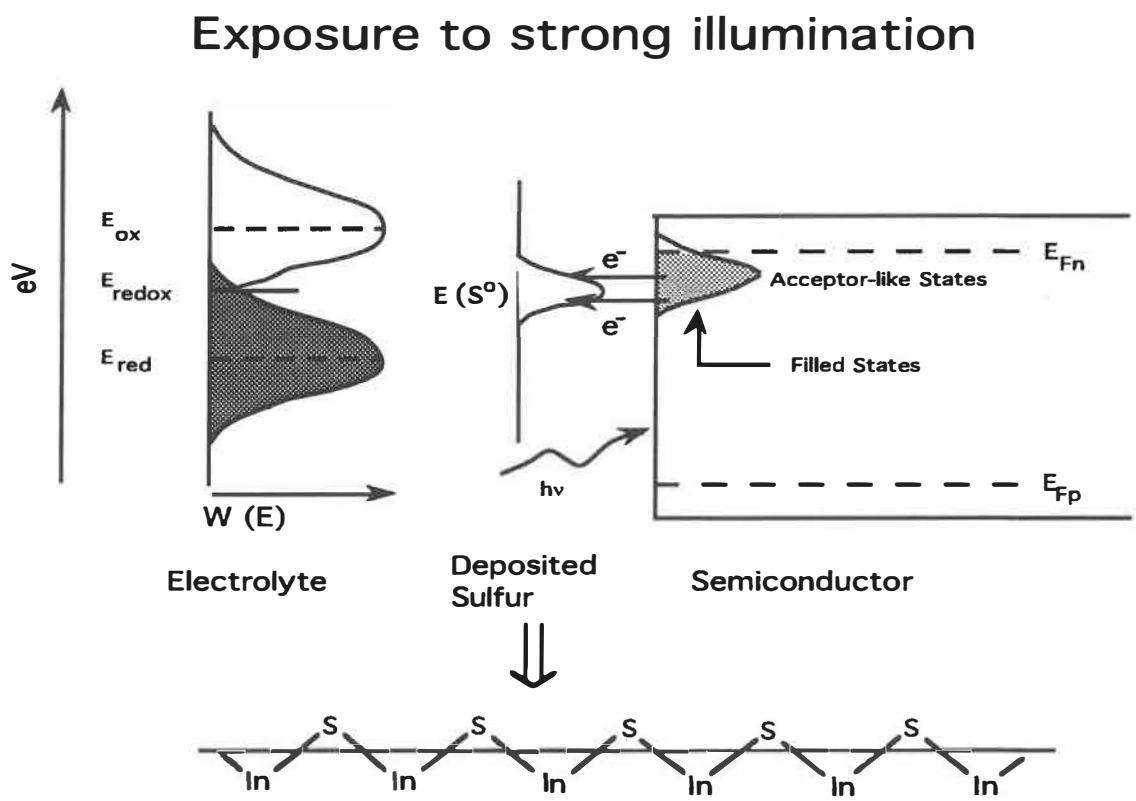


Figure 1.12. Schematic diagram showing the formation of improved In-S coverage under high intensity above bandgap illumination. E_{Fn} and E_{Fp} represent the quasi Fermi levels for electrons and holes respectively. The atomic surface diagrams at the bottom of the figure are a conceptual representation to indicate charge sharing between filled acceptor states and adsorbed S atoms with the formation of In-S bonds.

Surface P-S bonds are formed in a similar fashion, when the reduced S^{2-} states share charge with empty positive donor states. This mechanism requires the removal of an electron from the donor state associated with P dangling bonds and is described in detail in the recent article by Bessolov et. al. However, P-S compounds are highly soluble in the aqueous sulfide solution [36,63,64] and it has been conclusively proved in many XPS studies that S forms bonds only with In and P-S bond formation is not observed when InP is treated with $(NH_4)_2S$. P-S bonds have however been observed when p-InP is treated to hydrogen sulfide vapor [51].

Needless to say the formation of In-S or P-S bonds under room temperature and illumination are dependent on the position of the bulk Fermi level and the band bending. The passivation process therefore depends on the doping type and doping level of the semiconductor. However, under conditions of strong above bandgap illumination and high temperature, the surface carrier concentration and therefore the passivation mechanism should be relatively insensitive to the material related parameters such as doping. The unbonded excess S in these experiments is usually washed away in DI water or sublimated in vacuum [36,47]. However, as seen in the following section, if not removed this excess S reacts with InP at higher temperatures according to the equilibrium phase diagram [13,28,61].

From the proposed model, it is seen that filled acceptor states are essential for the electrochemical interaction leading to In-S bonds. It therefore follows that instead of using above bandgap illumination to satisfy this condition, one should obtain complete monolayer coverage in the dark by forward biasing the n-InP/electrolyte junction. In addition, the model also suggests that monolayer coverage can also be obtained with the other group VIB elements such as Se.

The model presented here therefore complements the work of Bessolov et. al. and describes a possible photo electrochemical pathway leading to In-S bond formation and provides for the first time a complete picture of monolayer S coverage on InP substrates.

1.3.2 BULK INTERACTIONS

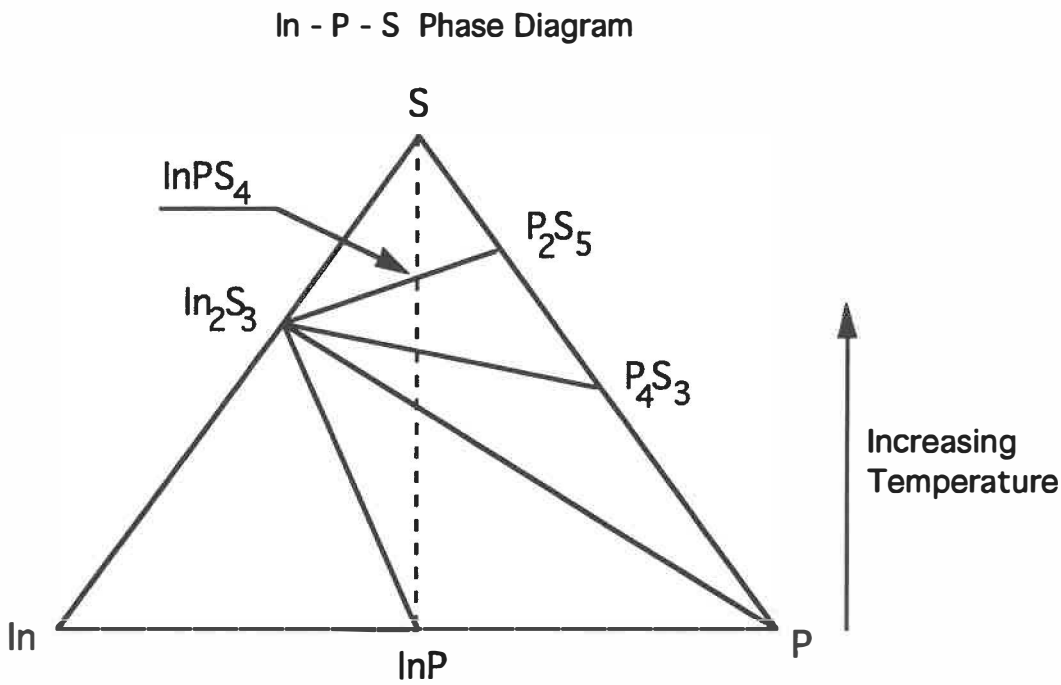


Figure 1.13. The In-P-S ternary phase diagram showing the various compounds that are formed for T < 408°C (after ref. 34). The intersection of the dotted line with the tie lines with increasing temperature results in the compounds at each end of the tie line.

In contrast to monolayer S coverage, bulk interactions occur when InP samples containing excess deposited S are annealed at high temperatures (>100°C). The deposited S reacts with the InP substrate according to the In-P-S equilibrium phase diagram [34] shown in figure 1.13. For these reactions chemical and diffusion barriers need to be overcome and the elevated temperature normally provides the necessary energy for this reaction to begin and proceed. Referring to the phase diagram as we proceed from InP to S we see the dotted line cuts the tie lines resulting in the following possibilities 1) mild sulfurisation with the formation of In_2S_3 + P, 2) intermediate sulfurisation resulting in the formation In_2S_3 + P_4S_3 and 3) strong sulfurisation producing

layers of $InPS_4$. The compound P_4S_3 is not stable and is reduced by the InP substrate to In_2S_3 + P [45].

As shown in section 1.2.3 of this chapter, thermal sulfurisation of InP proceeds according to the equilibrium phase diagram with the formation of 30Å In_2S_3 + P layer in the temperature range 150 - 300°C and refers to the case of mild sulfurisation. The P oxidizes on exposure to air to form P_2O_5. Formation of a In_2S_3 layer at 250°C has also been reported by Wilmsen et. al. [13]. It has been recently observed that sulfurisation of InP in $(NH_4)_2S$ at 90°C under illumination results in a In_2S_3 surface layer [65] and reaction around 350°C leads to the formation of $InPS_x$ [54]. In addition, Gendry et. al. have shown that plasma sulfurisation can form $InPS_4$ [45]. Thus there is evidence for intermediate and strong sulfurisations to occur at high T and in plasma reactions. In plasma reactions in addition to the equilibrium phase diagram reactions, the chemical potential of the S species changes gradually leading to sub-sulfide layers.

1.3.3 CONCLUSIONS

A universal model for the formation of sulfide layers on InP is presented for the first time. The model explains the formation of surface In-S bonds as due to charge interaction between deposited neutral S atoms and the filled acceptor states associated with surface indium atoms. Above band gap illumination is shown to increase the filled acceptor concentration and result in much better S coverage. This work complements the recent model (55) that explains P-S bond formation and provides a more complete picture of the passivating mechanism. Monolayer In-S coverage occurs from room temperature to about 65°C. At

higher temperatures, the deposited S reacts with the InP substrate according to the In-P-S phase diagram resulting in sulfide layers that are a few monolayers thick. In essence, all the sulfur passivation techniques can be classified into either photo electrochemical surface reactions that produce monolayer S coverage or thermally assisted bulk reactions that proceed according to the In-P-S phase diagram. This work is expected to improve our understanding of the nature of the S passivated InP surface.

It should however be emphasized that the model presented here offers a simple-minded view of the sulfur coverage of the surface. The model predicts charge transfer between the solution and that the semiconductor bands participate in this charge transfer process leading to monolayer S coverage of the InP surface. However HS^- ion adsorption due to acid-base type surface chemical interactions can also lead to surface S coverage at the surface. These reactions contribute to an ionic double layer at the surface that control the flat band potential of the semiconductor/electrolyte interface. Since the semiconductor bands do not participate in such adsorption processes, above band gap illumination does not influence these interactions contrary to the observations of [36]. In addition, formation of S bridge bonds are observed in these experiments, HS^- ion adsorption will not result in bridge bonds since presence of the proton will tend to stabilize the electron at the site (57). Adsorption of elemental S° as explained here will result in bridge bond formation as seen in figure 1.12. Thus there is enough evidence to support the photo electrochemical pathway presented here and detailed flat band measurements will throw more light in this direction. A rigorous treatment

should also consider quantum electrochemical aspects to quantitatively explain the charge exchange processes.

CHAPTER 2

FABRICATION TECHNOLOGY FOR SAG FETS

2.1 INTRODUCTION

We have seen in the earlier chapter that S passivation of the InP substrate reduces defect formation and can be advantageously used to fabricate InP based insulated gate devices. In particular, we attempt here to develop the complete fabrication technology for SAGFETs that require a high temperature implant activation anneal in the process sequence. Other devices such as MIS structures and non-self-aligned FETs can be readily fabricated using the same procedure.

Realization of any semiconductor device involves the integration of various process steps. Choice of each process sequence has to be made judiciously bearing in mind the fabricational aspects involved in the succeeding steps and its effect on the performance of other processes. For example, a long contact anneal increases the sheet resistance of the implanted regions. Needless to say, the final transistor behavior depends critically on the chosen fabrication procedure. Therefore, demonstration of a novel technique without loss of performance requires a delicate balancing act on the part of the device engineer. In our case, decision making is often complicated due to InP surface degradation during high temperature processing and the fledgling nature of InP technology. Although, characterization and optimization of individual process steps are considered in the available literature on InP, most of these reports attempt to find the optimal conditions for the particular process in question while ignoring other limiting factors during device fabrication. For example, an RTA anneal at 800°C will give the best implant activation but will also "fry" the metal

gates in a self-aligned process such as ours. As a rule of the thumb, these reports are to be used as a guide line and each process has to fine tuned depending on the type of device being attempted. We therefore turned to the available literature to locate the known and proven methods and used some as reported while modifying others to suit our purpose. During the course of this effort, we have developed a few new processes tailored for our interface engineered metal gate SAG technology and also characterized processes or particular areas that are found lacking in literature.

This chapter begins with wafer characterization and goes on to describe wet chemical cleaning and device isolation procedures, a novel and inexpensive indirect-plasma dielectric deposition method, gate metallizations, implantation conditions, a new slow ramp lamp annealing (SRLA) activation sequence, and contact formation. We discuss the various issues involved in choosing appropriate process sequences for the self-aligned device in question.

2.2 WAFER CHARACTERIZATION

Using starting materials of known properties is crucial to the success of any fabrication procedure. Device fabrication is no exception and we try to keep the uncertainties of the InP substrate to a minimum. For Czochralski grown bulk InP wafers, the important wafer specifications are orientation, dopant concentration, resistivity, carrier mobility, etch pit density (EPD), thickness and surface finish. These specifications, supplied by the manufacturers are listed in Table 2.1. We verified the carrier concentration, mobility and resistivity values of some samples by Hall and four point probe methods and found good agreement with Table 2.1. EPD values are representative of the surface defect

density and a value of $4x10^4$ /cm^2 is acceptable for bulk InP. Usually wafer slice specifications vary with the particular application. For MIS capacitor structures, we use undoped InP substrates with residual n doping to obtain large capacitance changes. For n-channel MISFETs moderately doped p^- and Fe-doped semi-insulating substrates are used to fabricate inversion and enhancement type devices. Moderate doping levels ensure high channel mobility, large reverse breakdown p-n junction voltages and low parasitic capacitances. Interface roughness which affects mobility can be greatly reduced by using polished wafers.

Table 2.1 Bulk wafer specifications of manufacturer.

Dopant	Fe	None	Zn
Carrier Density (/ cm^3)	-	$5.6x10^{15}$	$8.5x10^{15}$
Mobility (cm^2 / V.sec.)	-	4420	140
Resistivity (Ohm-cm)	$1x10^7$	0.268	5.46
Etch Pit Density (/ cm^2)	$4x10^4$	$4x10^4$	$4x10^4$

Table 2.2 Manufacturer supplied material specifications for heterostructure wafer.

Layer & Purpose	Material	Thickness (µm)	Doping Level (cm^{-3})	Type
1: Cap	InP	0.04	$<1x10^{15}$	n
2: Channel	$In_{0.47}Ga_{0.53}As$	0.15	$<1x10^{14}$	n
3: Buffer	InP	0.15	$<1x10^{15}$	n

Note: Substrate is semi-insulating Fe doped InP.

Undoped InP/InGaAs/InP MOCVD epi-layers grown on semi-insulating substrates are used for HIGFET fabrication. The specifications supplied by the manufacturer are given in Table 2.2. The semi-insulating substrate results in low parasitic capacitance, the first InP buffer layer stops substrate dislocations from creeping into the channel region. The middle InGaAs layer is the active channel layer and the top InP cap layer provides the ΔE_C barrier that results in carrier confinement and buried channel transport. Characterizing heterostructure wafers like growing them is more of an art and involves using sophisticated techniques. In addition to the above mentioned properties, we are also interested in knowing the lattice mismatch, epitaxial layer thickness, quality of the active InGaAs channel region and the uniformity at the wafer scale.

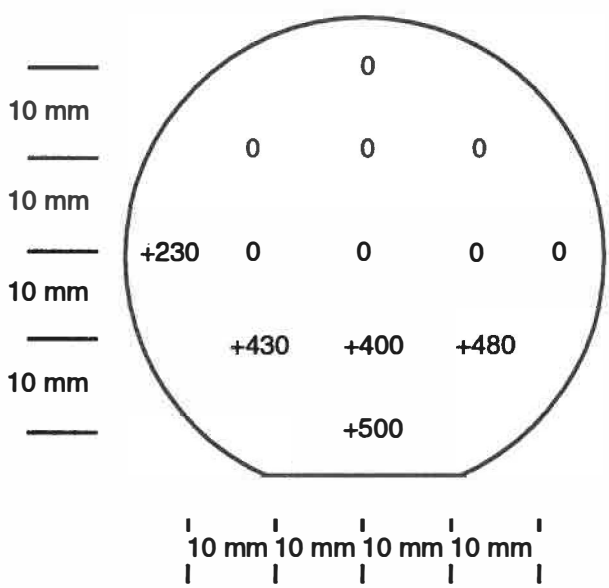


Figure 2.1 Measured mismatch in parts per million (ppm) over the entire wafer.

A large lattice mismatch ,f, ($f = \frac{a_s - a_o}{a_s} = \frac{\Delta a}{a_s}$) of the InGaAs layer leads to the creation of dislocations if the layer thickness exceeds the critical thickness [66].

In the formula for f, a_s represents the lattice constant of the substrate and a_o that of the overlayer. In the case of a small mismatch ($f \leq 0.5\%$), the tensile or compressive stress due to the strain layer might relax during high temperature annealing leading to dislocations. It is therefore essential for the active layer to be lattice matched to InP. HXRD diffraction patterns are used to measure the lattice mismatch over the wafer surface. The results shown in figure 2.1 indicate that the majority of points are on match with the maximum measured mismatch being 500 parts per million (ppm). The region close to the wafer flat is under slight tensile stress.

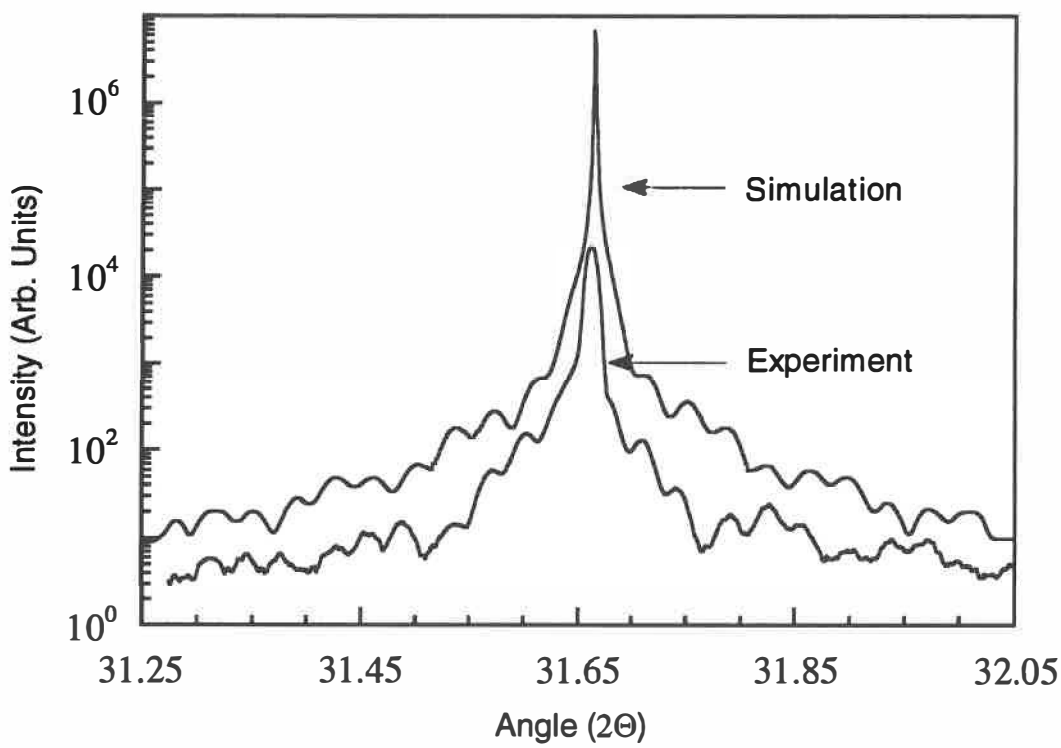


Figure 2.2. High resolution X-ray diffraction fringe pattern of the epitaxial wafer. The bottom is the experimental curve and the top is the curve obtained using a commercial dynamical simulation software.

The other important aspect is to control the epi-layer thickness within specifications. As discussed in chapter 7, a relatively thick InP cap layer

encourages parallel transport in the InP cap degrading performance. Similarly, changes in the active layer thickness will affect the channel pinch-off voltage. We use experimental and computed HXRD interference fringe patterns to accurately determine the epi-layer thicknesses. The computed curve is a dynamical simulation obtained using a commercial software [67]. The presence of thin epitaxial layers gives rise to an interference fringe pattern on both sides of the main HXRD peak [68]. The thickness of the active and cap layers affect the position and periodicity of these fringes. By comparing the experimental curve with the simulation curve, we are able to measure the epi-layer thicknesses to a precision of ± 5Å. The results are shown in figure 2.2. We obtain a close fit for an active InGaAs layer of 970Å and a InP cap layer of 450Å. These values when compared with those of table 2.2 supplied by the manufacturer indicate a lack of thickness control in the growth process. The thickness variation however should not affect demonstration of SAG HIGFETs.

The quality of the InGaAs layer is determined by obtaining a PL scan at 7K as shown in figure 2.3a. PL measurements are sensitive to material quality and any nonhomogenity will broaden the band edge PL spectrum [69]. The Full Width at Half Maximum, FWHM, of the PL peak is therefore indicative of layer quality. We estimate a FWHM of 4.2 meV which represents a good quality InGaAs channel layer.

The uniformity at the wafer scale is studied by performing scanning PL measurements at room temperature. In this method, the emission intensity is mapped over the entire wafer at the peak wavelength (1630 nm) of the PL spectrum. The results are displayed in figure 2.3b as a color code that reflects the intensity measured at the particular point on the wafer. The intensity

values recorded over most of the wafer is close to the average value of 780 calibration (Cal.) units to within a 10% variation. The mismatched regions near the wafer flat deviate above this value by about 70 Cal. units. These results indicate acceptable uniformity over the wafer. The scanning PL study is performed at Bell Northern Research, Ottawa with the kind assistance of Dr.Carla Miner.

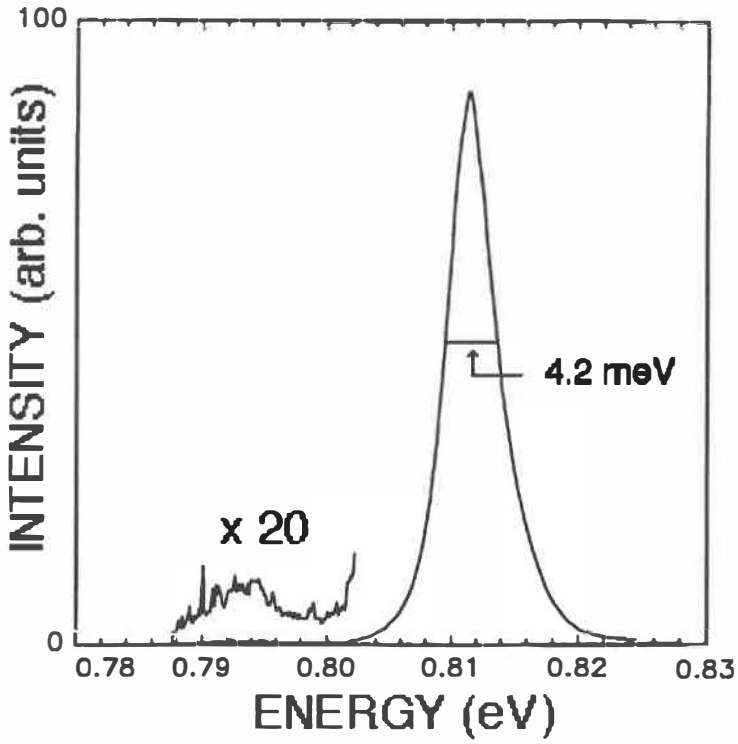


Figure 2.3a 7K band edge PL spectrum of the InGaAs channel layer lattice matched to InP.

Mobility values are a measure of the device worthiness of the epitaxial sample. However these values have to be treated with caution when measured on thin overgrowths of low doping since depletion effects in multi-layered structures can lead to an underestimation of the actual values [70]. We measure on the as-received samples Hall mobilities of 5500 $cm^2/V.sec$ at RT and 54,000 $cm^2/V.sec$ at 77K.

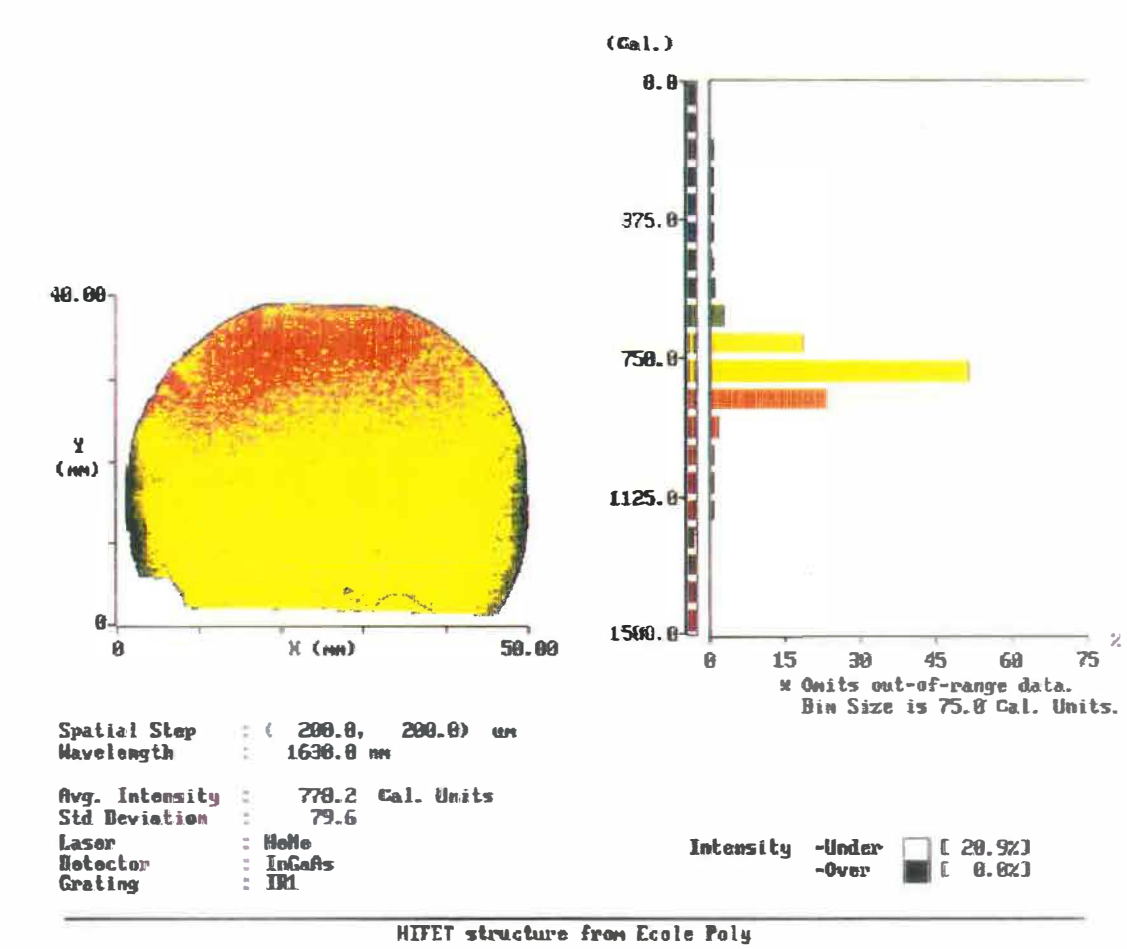


Figure 2.3b Scanning PL measurement to estimate uniformity of the epitaxial layers over the 2" heterostructure wafer. Emission intensity values are shown as a color code on the wafer. The graph on the right shows a histogram of intensity Vs % of sample area.

The corresponding resistivities at these temperatures are 60 and 7.6 mΩ/cm. The Hall experiments indicate residual donor concentrations of 1-2x10^{16}/cm^3. These doping values are an order of magnitude higher than the specifications provided by the manufacturer (table 2.2) and agree with Polaron depletion profiles of the wafer. This may be related to carrier transfer from the InP cap and buffer layers into the InGaAs channel resulting in an apparent increase in the residual concentration or could again indicate lack of control of the growth process.

Having characterized the starting wafers we now turn our attention to the fabrication procedures for SAGFETs.

2.3 CHEMICAL CLEANING AND ETCHING

Chemical etching plays an important role in the fabrication of electronic devices and is used for a variety of applications. Sample cleaning, mesa device isolation, selective material removal etc. are some of the common processes which involve a chemical etching step. Here we are mainly concerned about selecting an appropriate cleaning cycle for InP and a fast etchant that delineates higher order crystal planes with gentler slopes for device isolation.

2.3.1 THE CLEANING CYCLE

A number of cleaning recipes are reported in the literature for InP, with solutions based on HBr and HIO_3 the most popular [10,11,71]. Any sample cleaning cycle must meet the following requirements: A degreasing step to remove organic contaminants, a native oxide strip followed by an etch that eliminates any surface damage and metallic contaminations and a final polishing etch that leaves a smooth surface. For our experiments, we use a

slightly modified version of the cleaning cycle reported by Iyer et. al. [11]. The cycle is as follows

1) Degreasing in heated solutions of Tri-Choloro-Ethylene (TCE), acetone and propanol for 5 minutes each.
2) A 3 minute etch in a 1HCl:1HF:4H_2O solution to remove the native oxide.
3) A 3 minute etch in 10% HIO_3 to remove approximately 2000Å of the top InP surface and any metallic contaminants.
4) A 3 minute polishing etch in a solution of 1H_3PO_4:1H_2O_2.
5) A final etch in the solution used in step 2 to remove any surface oxides formed in steps 3 and 4.

In the sequence described above we use in step 4 a mixture that is normally used for GaAs [72]. We find that this solution acts as a soft etchant for InP. On the other hand, the fast etchant HIO_3 although increasingly used in InP processing is found lacking in literature. Technologically, it is important to use well characterized etchants rather than particular etchant formulas. Etchants with known properties markedly improve the confidence level of the process and provide flexibility in device fabrication. We therefore proceed to characterize both these etchants in detail in terms of etch rate, etch profile and post etch physical and chemical state of the surface [73,74].

2.3.2 IODIC ACID

Cadmium doped p type, $N_A=8x10^{18}$ cm^{-3}, (100) oriented samples are used in this study. The samples are coated with Shipley S1400-23 positive photoresist that serves as the etch mask. The etch pattern consists of straight lines with widths ranging from 1-10 microns. Etching is carried out in weight

percentage (wt.%) solutions prepared prior to etch, by dissolving 99.5% HIO_3 crystals in 18 Mohm de-ionized water. The solutions are continuously stirred during etching to ensure homogeneity. The temperature is maintained to within ±1°C throughout these experiments. The typical etching time is 10 minutes. For concentrations greater than 40% and temperatures above 30°C, the time is reduced to avoid severe photoresist attack. The etch rates are determined based on the total etch depth measurements made using a Sloan Dektak. The total depth is usually measured over multiple points on more than one sample to minimize the error associated with the etch rate to less than ±10Å. XPS measurements are performed on post etched and as-received InP samples to identify the chemical composition of the surface. The carbon C_{1s} reference is taken at 285.5eV for XPS analysis. The crystallographic planes exposed by the etchant are observed by SEM and the quality of the etched surface by an optical microscope.

2.3.2.1 ETCH RATE WITH CONCENTRATION

The etch rate variation with wt.% concentration (C) is shown in figure 2.4. The rate exhibits a linear increase at low HIO_3 concentrations and tends to saturate around 850 Å/min. above 30wt.% concentration. The quality of the etched surface depends critically on the concentration. The etch results in a mirror quality surface up to 20wt.% concentration. Above this critical value, we observe the formation of "cigar" shaped hillocks which increase in density with concentration. Due to the rough nature of the surface we conclude that concentrations greater than 20wt.% will not be suitable for InP processing. Another negative side is the severe photoresist attack at high concentrations

(C>40wt.%). The nature of the post etch surface for concentrations above and below 20 wt.% are shown in figures 2.5a&b.

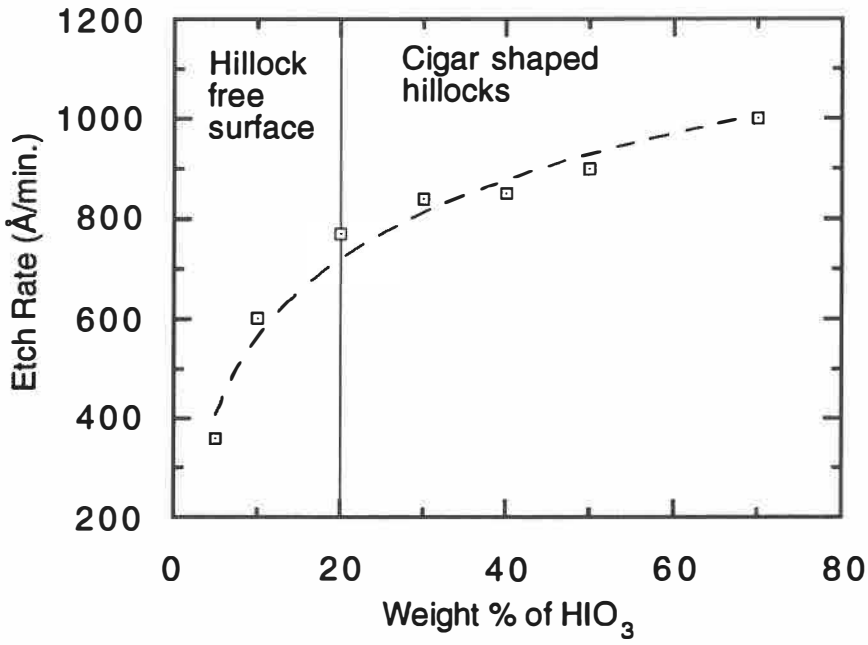


Figure 2.4 Variation of etch rate with wt. % concentration (C). The dashed line is a logarithmic fit of the data points. The features of the post etched surface are shown in the micro graphs of figure 2.5.

2.3.2.2 ETCH RATE WITH TEMPERATURE

The variation of etch rate with temperature is studied to determine the activation energy of the etching process. The temperature dependent etch rate, r (T), can be written as follows

$$r(T) = r_0 \exp\{E_a/kT\} \qquad (2.1)$$

where E_a is the activation energy, k the Boltzmann constant and T the temperature of the solution. The slope of the line ln(r) Vs $\frac{1000}{T}$ is then proportional to the activation energy.

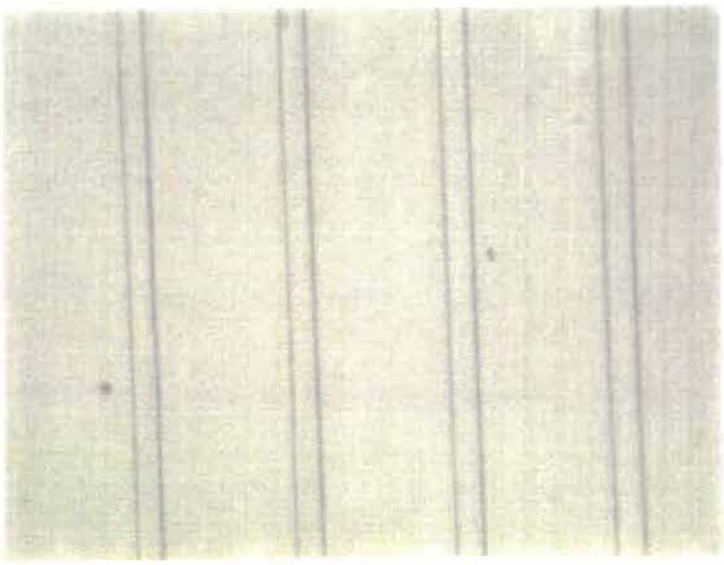


Figure 2.5a. Photomicrograph of the surface quality of a p-InP sample etched in 5 wt% HIO_3. The surface has a mirror quality.

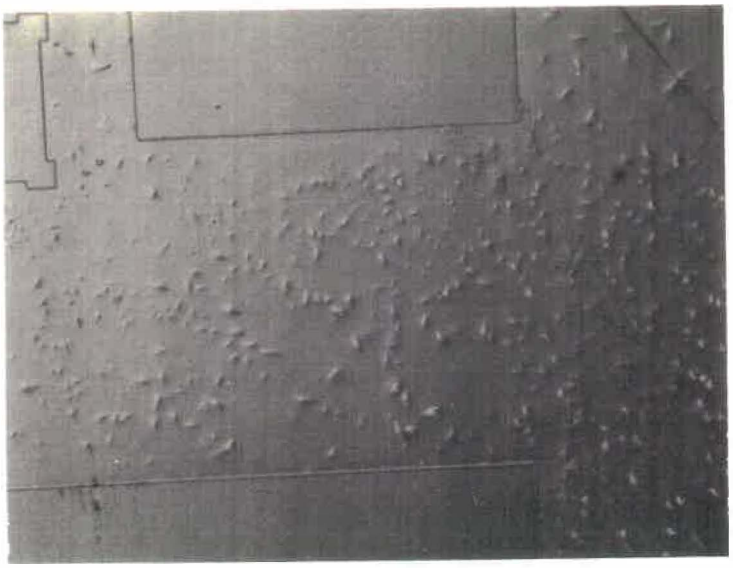


Figure 2.5b. Photomicrograph of the p-InP surface quality following a etch in 30 wt% HIO_3. Note the 'cigar' type features on the wafer surface.

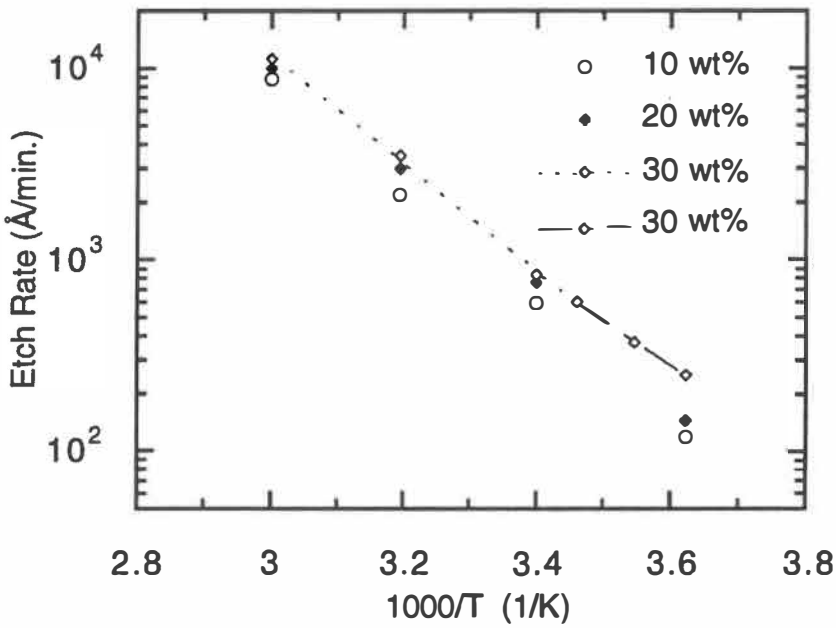


Figure 2.6 Variation of etch rate with temperature for different concentration. The deduced activation energy by a linear fit is between 12.5-13.5 Kcal./mole for the 10 and 20 wt.% solutions and above room temperature (RT) for the 30 wt.% solution. The values indicate a reaction rate limited process. The activation energy drops to a diffusion limited value of 10.8 Kcal./mole for the 30 wt.% solution below RT. The different activation energies above and below RT for the 30 wt.% solution are indicated by the dashed and dotted linear fits to the measured data. The standard deviation of these measurements is less than ±0.35 Kcal/mole.

The variation of rate with temperature is studied for three different concentrations and the results are plotted in figure 2.6. These solutions exhibit activation energies between 12.5-13.5 Kcal/mole, with the value decreasing with increasing concentration. The standard deviation for these measurements is less than ±0.35 Kcal/mole. In addition, the 30wt.% solution exhibits a different slope at lower temperatures which corresponds to an activation energy of 10.8 Kcal/mole. It is well known that etching processes are limited by either the chemical reaction rate or by the transport of etchant molecules by diffusion [71].

Diffusion limited processes are relatively insensitive to temperature with lower activation energies and are usually encountered at high concentrations [75]. Our results on the 30wt.% solution are consistent with this observation. Moreover, it is reasonable to expect the transition from reaction rate limited to diffusion limited etching to manifest initially at low temperatures where transport of etchant molecules is much lower. The higher E_a values for the 10-20wt.% solutions therefore correspond to reaction rate limited etching while for the 30wt.% solution, the process is diffusion limited up to room temperature above which it becomes reaction rate limited.

Table 2.3a Peak positions of the P_{2p} and $In_{3d5/2}$ spectra.

	P	P(o)	In	In(o)
Binding Energy (eV)	128.9	133.5	444.58	445.75

Table 2.3b Atomic ratios of the etched surface.

	P/In	In(o)/In	P(o)/P	P(o)/In(o)
Atomic Ratios	0.83	0.192	0.26	1.12

(o) -- oxidized state

2.3.2.3 SURFACE AND PROFILE

As discussed earlier the physical state of the surface depends critically on the concentration. In order to study the chemical state of the etched surface, XPS analysis is performed on the 10wt.% solution etched sample. HIO_3 is a strong oxidizer and is expected to leave the surface in an oxidized state. The

$In_{3d5/2}$ line exhibits a higher binding energy tail due to a small peak at 445.75eV apart from the main line at 444.58eV for InP. The higher energy component may be due to the formation of either $InPO_4$ or In_2O_3 [49]. However, the oxides and phosphates of indium do not show any appreciable binding energy shifts and one generally identifies the oxidation state by analyzing the P_{2p} spectrum. The P_{2p} line shows two peaks, one at 128.9eV which is from the InP substrate and the other at 133.5eV due to the phosphate [48,49]. The peak positions and the binding energy differences (Table 2.3a) between the oxidized and unoxidized states of In and P correspond to the phosphate $InPO_4 . xH_2O$ with $x>2$. The spectra are curve-fitted and the atomic ratios of the various constituents on the surface are calculated from the areas under the different curves (Table 2.3b). Sensitivity factors of 0.39 and 3.9 are used for the P_{2p} and the $In_{3d5/2}$ lines respectively [44]. The etch reduces the P/In ratio to 0.83 from 0.95 for the unetched sample. This is consistent with the formation of a slightly phosphorus rich phosphate (Table 2.3b).

SEM profiles of the 20wt.% etched sample are shown in Figures 2.7a&b. The etchant exposes the $\{2\ 1\ \bar{1}\}$ and $\{2\ 1\ 1\}$ planes in the $[0\ 1\ 1]$ and the $[0\ 1\ \bar{1}]$ directions respectively. These planes make a low angle of 35° in both directions with the (1 0 0) plane. This is an important result from a technological view point, since low angles are ideally suited for mesa device isolation and ensure proper metal coverage over the mesa side wall. The 10 wt.% solution exhibits similar profiles.

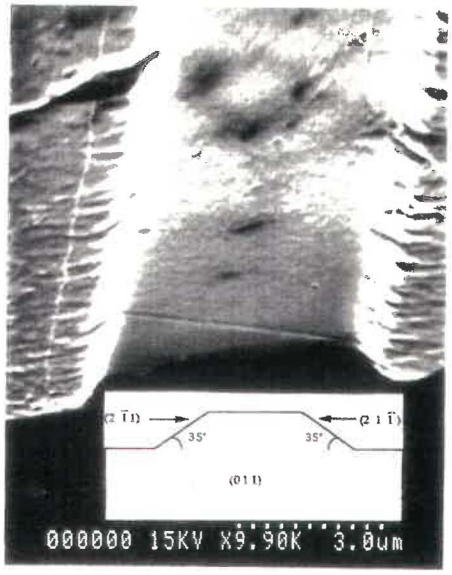


Figure 2.7a. SEM profile of the (100) p-InP sample etched in 20 wt.% HIO_3 along the [0 1 1] direction. The exposed {2 1 1} planes make an angle of 35° with the (100) surface. Note that the side wall roughness.

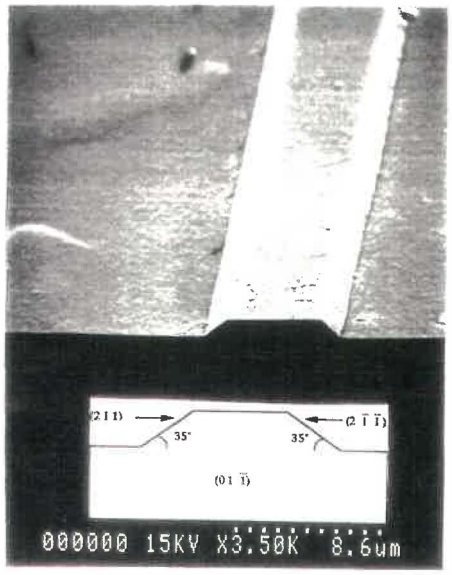


Figure 2.7b. SEM profile of the (100) p-InP sample etched in 20 wt.% HIO_3 along the [0 1 $\bar{1}$] direction. The exposed {2 1 1} planes make an angle of 35° with the (100) surface. Note that the side wall smoothness.

The side wall roughness varies with direction and is more rough for the (0 1 1) direction. In compound semiconductors etching always occurs by dissolution of double layers and leads to termination of a particular plane. It is well known that plane A (Indium) termination leads to rough surfaces while exposure of B (P) planes forms smooth side walls [76]. It therefore appears that the etch exposes A planes in the (0 1 1) direction and B planes in the $(0\ 1\ \overline{1})$ direction. This roughness aspect is taken into account during mask design as seen in chapter 4. This is particularly important for short HIGFET gates that should run over the mesa without breaking. Inserting a lattice matched InGaAs layer between two InP layers fortunately does not affect the etch profile and the 10% solution is successfully used for mesa isolation of HIGFETs.

This etchant attacks metals like Au, Au-Ge-Ni which are used in device fabrication and should be used with care.

2.3.3 THE PHOSPHORIC-PEROXIDE MIXTURE

A similar study with p-type, Cd doped, InP samples is conducted to characterize the phosphoric-peroxide mixture that is used as a soft etchant for InP. These results are briefly described below. A more detailed account of this study can be found elsewhere [74].

Since the etch rate varied with the relative volume concentrations of H_3PO_4 and H_2O_2 in addition to dilution, our initial study is on the etch rate variation for different relative concentrations of H_3PO_4 (x) and H_2O_2 (1-x) for two degrees of dilution in H20 (y), $y = \frac{10}{x}$. As observed in figure 2.8, the rate is

maximum for solutions with equal volumes of H_3PO_4 and H_2O_2 i.e.. x=0.5.

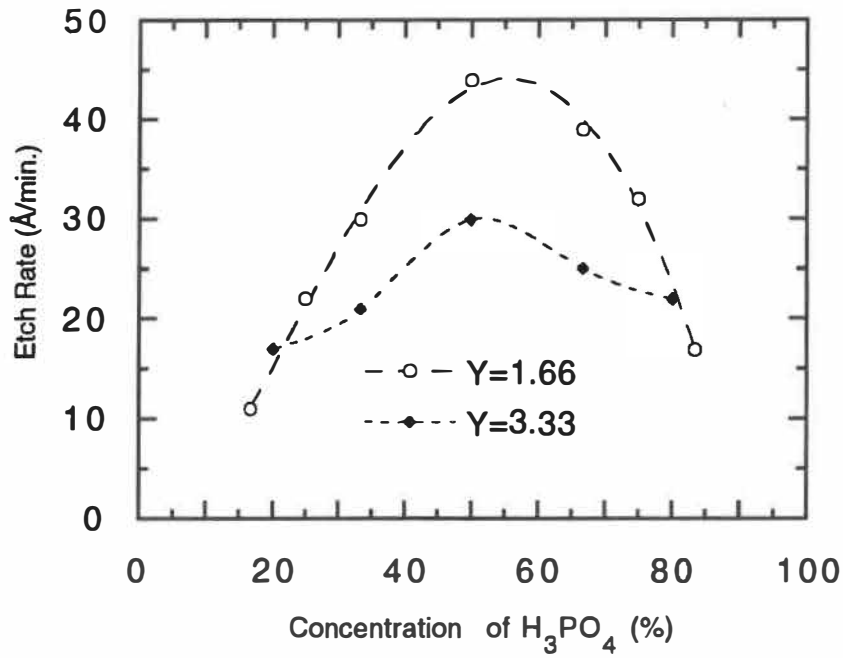


Figure 2.8. Variation of etch rate with relative concentration of H_3PO_4.

The variation of etch rate with dilution is shown in figure 2.9. The rate drops from 70Å/min. for the undiluted solution to about 15Å/min. for the 1:1:10 solution. At large dilutions the etch rate is small and these solutions can be used as very precise or soft etchants for InP. We use the 1:1:10 solution in the sulfur passivation PL experiments of chapter 2 to remove about 20Å of the top surface. We estimate an activation energy of 16.3 ± 0.2 Kcal/mol for the undiluted 1:1 solution from the etch rate Vs $\frac{1000}{T}$ plot of figure 2.10. As discussed previously this value of activation energy indicates a reaction rate limited process.

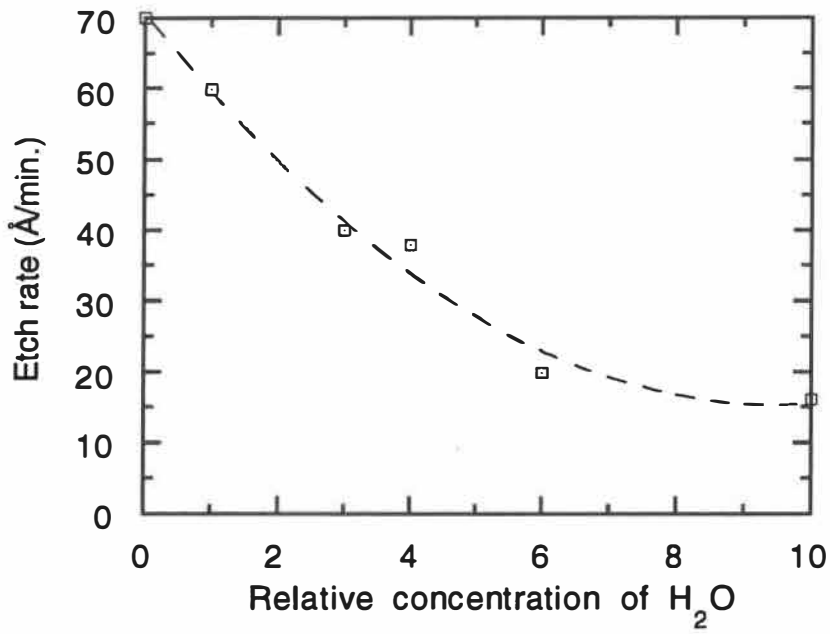


Figure 2.9. Variation of etch rate with dilution for a 1:1 : H_3PO_4:H_2O_2 solution.

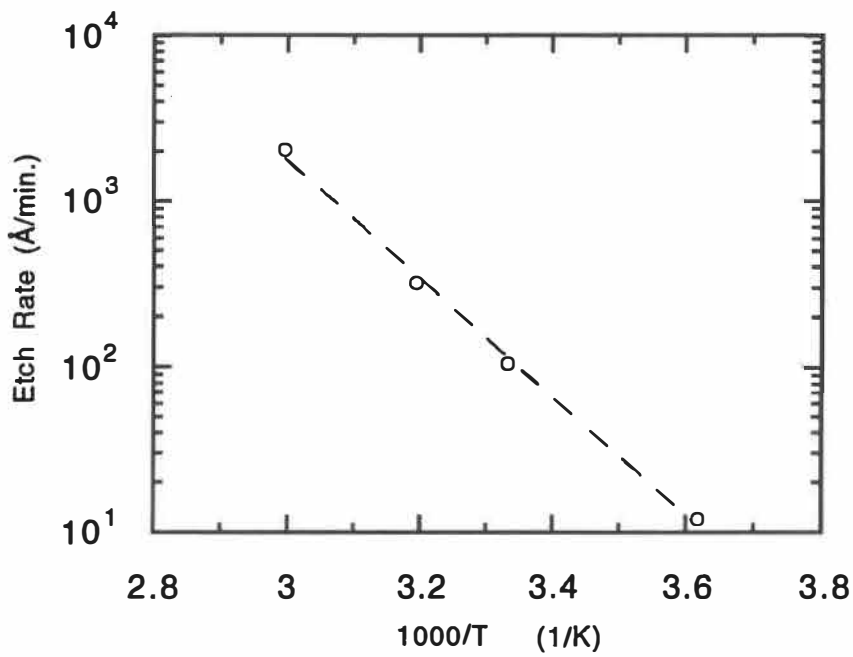


Figure 2.10. Variation of etch rate with temperature for a 1:1:H_3PO_4:H_2O_2 solution. From the linear fit we deduce an activation energy of 16.3±0.2 Kcal/mole indicative of a reaction rate limited process.

It is observed that the post-etch surface always remains smooth with absence of etch pits for all concentrations and temperatures used in these experiments. We therefore use this etchant in the final step of our cleaning process to get a very smooth surface.

XPS analysis indicates that the etch leaves the surface in a oxidized state with the formation of $InPO_4.xH_2O$. The etchant exposes the $(4\ \bar{1}\ \bar{1})$ and $(1\ 1\ \bar{1})$ planes in the $(0\ 1\ \bar{1})$ and $(0\ 1\ 1)$ directions respectively. These planes make angles of 21° and 55° respectively with the (100) surface.

In addition to the above mentioned etchants we also use a 10% HF solution to etch the PECVD silicon nitride that is used as the gate dielectric and a 10% HCl solution to remove any native oxide before contact deposition.

2.4 THE GATE INSULATOR

2.4.1 LIMITATIONS AND SOLUTIONS

Compound semiconductors do not have a stable native oxide and this has been the major limiting factor in the development of insulated gate structures based on these materials [1]. The alternative is to use a deposited insulator or an epitaxially grown larger band gap semiconductor which serves as the dielectric layer. Epitaxial dielectrics are very attractive since it is possible to grow clean hetero-structures with negligible interface state densities. The important requirements are a small lattice-mismatch, a large conduction band / valence band discontinuity and high resistivity layers. The requirement of lattice match restricts the number of available materials. Although sufficiently large conduction band discontinuities ($\Delta E_C \approx 0.3$-0.5 eV) result in electron confinement at the interface, these barriers are still much smaller compared to those of

conventional insulators and appreciable carrier emission over the barrier restricts the dynamic voltage range and high temperature operation. From a technological stand point, it is a challenge to grow high resistivity large band-gap epi-layers. The epitaxial insulator technology is currently under intense investigation [3,4,16,17].

Lacking a mature epitaxial insulator technology, the alternative is to use Plasma Enhanced Chemical Vapor Deposition (PECVD) techniques to deposit the dielectric layer [35]. A whole range of dielectrics are used for compound semiconductors including exotic ones like $InPO_x$, $InPS_4$ and $P_xN_yCl_z$ with silicon oxide and silicon nitride the most popular [52,77,78]. In the popular PECVD technique, a low pressure plasma discharge of the input gases creates excited species that react to form the insulator on a substrate usually maintained at 200-300°C. It is preferable to load the sample face down to avoid incorporating silica dust in the layer. In a conventional parallel plate system, the substrate is placed on the grounded electrode and a Radio Frequency, RF, signal is applied to the power electrode. In this arrangement, the samples are directly exposed to the plasma which consists of a non-thermal distribution of electrons, ionized atoms and molecules and high energetic photons that create trapping centers within 10nm of the exposed surface. This damage is not completely removed by annealing up to 400°C and can adversely affect the electrical properties of the interface and the final device, especially for III-V materials [79]. To overcome this problem, a remote plasma technique has been developed by L.G.Meiners in 1982 [79]. The samples are subjected to gentler environments by separating the plasma chamber from the deposition chamber. In a modified indirect plasma version described in [8], the samples are placed

on a pedestal that does not face the plasma. Although remote/indirect plasma techniques have been widely used for gate dielectric deposition on III-V, there are also reports of direct plasma depositions used successfully on passivated InP surfaces [33].

2.4.2 INDIRECT PLASMA NITRIDE

2.4.2.1 THE INDIRECT PLASMA SYSTEM

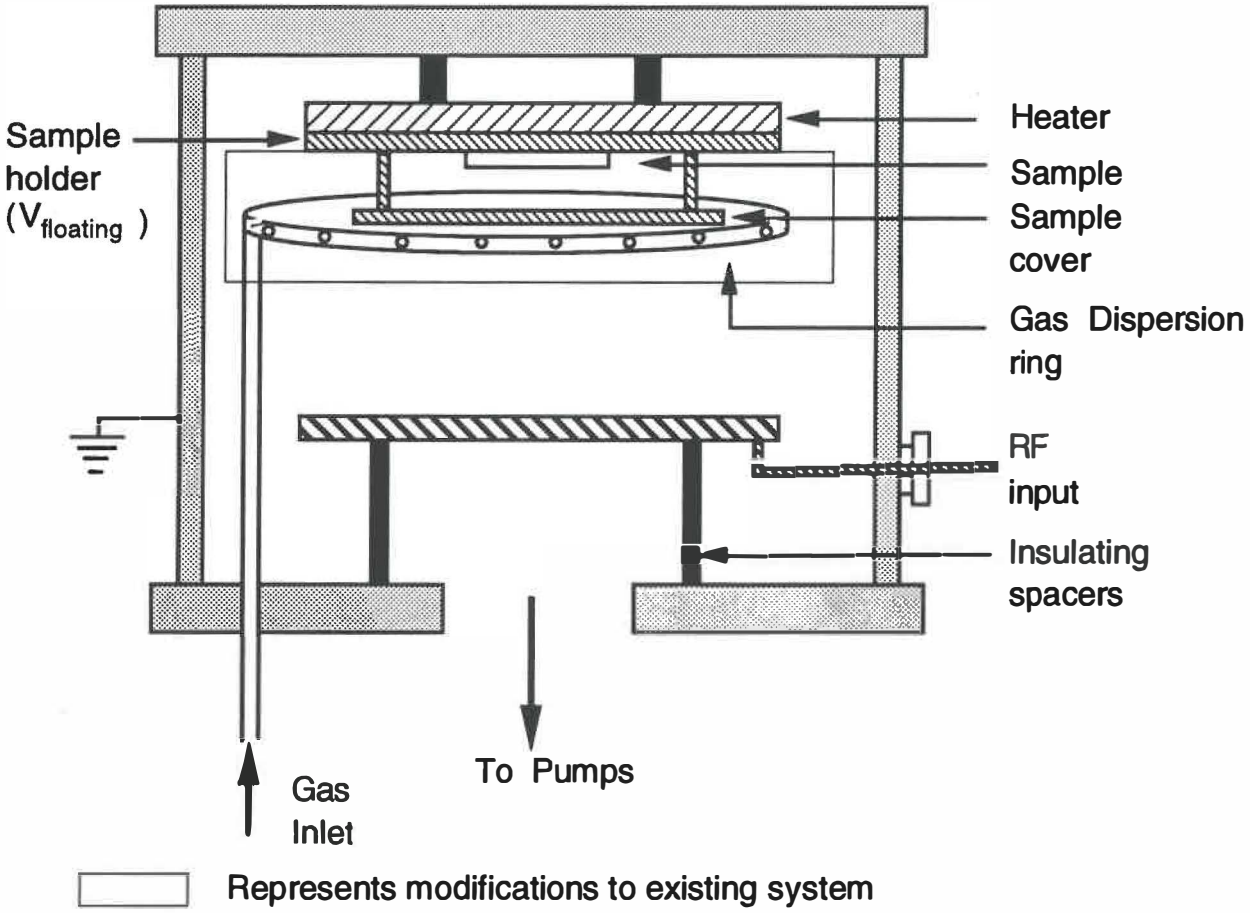


Figure 2.11. Schematic drawing of the floating potential indirect plasma PECVD deposition apparatus used in the study.

We have directed considerable effort to develop an indirect plasma deposition technique from the existing conventional plasma system in our laboratory shown in figure 2.11. An estimate shows that building a separate remote plasma system is quite expensive and time consuming and we are forced to look for simpler solutions. It appears that the most reasonable approach is to mount the sample on the top side of the upper plate, marked heater in figure 2.11, that does not face the plasma similar to that described in [8]. This attempt is unsuccessful due to poor uniformity and deposition of silica dust on the sample surface. We have deliberated several modifications of the system and decided that the easiest would be to use a metal cover close to the sample and shield it from ion and photon damage as shown in the modifications region of figure 2.11. This set-up has not been attempted before and if successful would permit an inexpensive and rapid modification of existing direct plasma systems to perform indirect plasma deposition. A 2" diameter steel cover, indicated as "Sample cover" in figure 2.11, is spaced 5 mm from the sample's surface and the substrate holder ,"Sample holder", is left at floating potential to further reduce any stray ion damage.

2.4.2.2 CONDITIONS FOR NITRIDE DEPOSITION

The modified indirect plasma PECVD system shown in figure 2.11 consists of a parallel plate capacitive configuration. The wafers are loaded on the top plate that is heated by a resistive element. This plate is left electrically floating. The 100 KHz RF signal is applied to the bottom electrode and the walls of the chamber are grounded. The reactant gases, SiH_4 and NH_3, are introduced into the chamber through a gas distribution ring. The chamber is

pumped to a base pressure of 2-3x10^{-6} Torr before deposition begins. An initial NH_3 discharge is used to clean any residual oxygen from the chamber. The ratio of SiH_4 : NH_3 flow rate is maintained at 1:10 and the deposition pressure at 200 mT. The layers are normally grown at temperatures between 250-300°C. Presence of the metal cover lowers the deposition rate by a third to approximately 10Å/min. This rate can be increased by increasing the pressure during growth. The thickness of the sample is determined by an optical interference fringe method. For our devices we use a gate nitride thickness of approximately 500Å.

2.4.2.3 THE Si/NITRIDE INTERFACE

The initial feasibility study is performed on 6-8.5 Ohm-cm resistivity p-type silicon substrates by depositing approximately 500Å of silicon nitride and fabricating Al/nitride/p-Si MIS capacitors. The thickness uniformity of the indirect plasma nitride is about 15% over a 1cm diameter circle. By using the gas distribution ring and careful sample positioning, we are able to improve the uniformity to 5-10% over 1.5 cm x 1.5 cm sample areas. Figure 2.12 shows a comparison of the 100 KHz C-V curves of the MIS devices fabricated from samples positioned inside and outside the metal cover. The unprotected sample shows a large negative voltage shift that is indicative of a large amount of fixed charges at the interface but more importantly the C-V curve appears to be similar to a low frequency curve as the capacitance increases in inversion. This tendency is due the formation of a permanent inversion layer at the sample interface that communicates with the charge under the gate [80]. This we believe is due to surface damage caused by ion bombardment. The sample that

is covered on the other hand shows typical HF characteristics with more positive threshold voltage and low hysterisis. The technique therefore appears to be effective in reducing ion bombardment and preserving surface integrity for Si substrates. As will be seen in chapter 5, we are able to reproduce these results on S passivated InP surface. The important consideration for dielectric deposition on InP is to keep the time required to reach the final deposition temperature to a minimum since the semiconductor surface degrades if annealed for long durations.

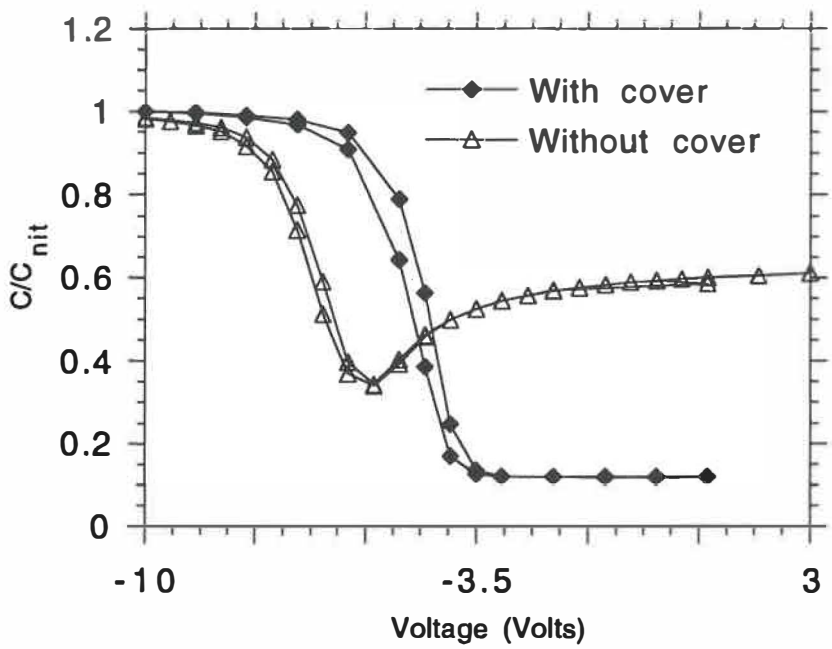


Figure 2.12. Capacitance-voltage curves of Al/ Silicon nitride/ p-Si direct and indirect plasma MIS structures.

2.4.2.4 STOICHIOMETRY OF THE NITRIDE

The stoichiometric depth profile of the indirect silicon nitride films is obtained by the Elastic Recoil Detection (ERD) technique. Here, the sample is bombarded by energetic chlorine ions at glancing angle and the ejected recoil

atoms as well as the ions scattered in the forward direction are detected [81]. The measured energy spectra of the recoiled atoms can be related to their concentration profiles. The technique has a mass resolution of 0.7 amu, 0.01 atomic % detection limit and 0.1 atomic % depth resolution. Figure 2.13 shows the ERD profile of the silicon nitride on Si. The atomic ratios of the various elements in the silicon nitride film are plotted with respect to Si. The X-axis provides the depth in $\mu g/cm^2$. The $\mu g/cm^2$ values can be converted to depth in angstroms by dividing the number by the density (ρ) of the film in gm/cm^3 and multiplying by 100. For example, $40\mu g/cm^2$ of Si (ρ = 2.3 gm/cm^3) corresponds to a depth of 1724Å.

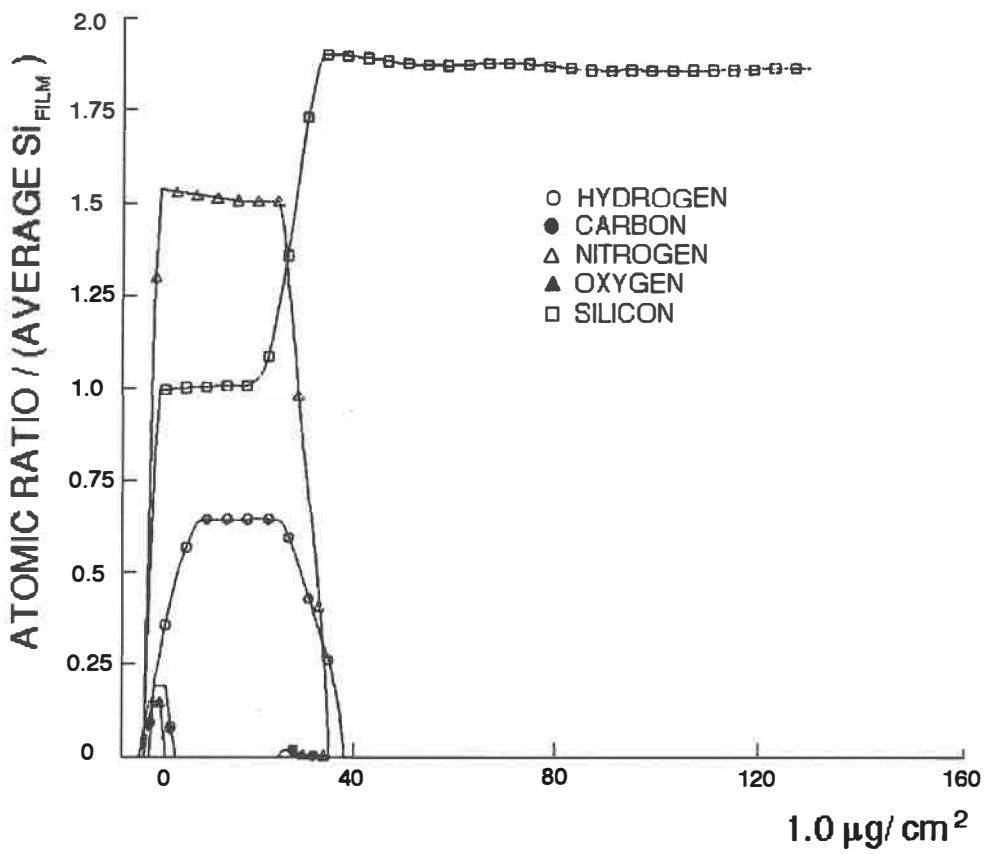


Figure 2.13. ERD depth profile of indirect plasma nitride on Si substrate.

The interested reader is referred to the article by Gujrathi et. al. that discusses the principles of this technique in detail [82]. The experimentally obtained film stoichiometry is $SiN_{1.5}$ and the film density is about 2.5 gm/cm^3 which are comparable to reported values of PECVD nitride. There is negligible carbon or oxygen contamination of the films. The H content in the films is estimated by Time of flight (TOF) experiments [83]. These measurements are done with an extended ERD system. We observe considerable hydrogen incorporation in the film up to a H to Si ratio of 0.5. The H concentration peaks near the interface resulting in a H rich insulator/semiconductor interface. We believe that this is due hydrogen ions produced in the initial NH_3 plasma discharge getting adsorbed to the semiconductor surface. H is known to passivate dangling bonds and defects and an anneal in forming gas (N_2+10%H_2) is widely used to improve the electrical characteristics of MIS, implanted regions and contacts. H incorporation will also relieve stress in the dielectric films. Preparing a H rich interface is therefore quite interesting from a technological stand-point and we intend to investigate this in the future for device applications.

The breakdown voltage for a 500Å thick nitride layer is about 10-12V that corresponds to a breakdown field of $2x10^6$V/cm which is slightly lower than the value of $6x10^6$V/cm reported for low pressure direct plasma PECVD nitride. On S passivated InP surfaces the nitride tends to leak under electron accumulation conditions, probably due to S incorporation into the nitride. It is not possible to evaluate the S concentration in the nitride by ERD since the sulfur peak is completely submerged by the tail portion of the incident Cl beam.

2.5 ION IMPLANTATION

2.5.1 GENERAL CONSIDERATIONS

MISFET fabrication requires the formation of selected regions that are heavily doped and act as a source or drain for carriers. The preferred way of introducing dopants into a III-V crystal lattice is by implanting the appropriate species at several keV [76]. The as-implanted dopant profile is a Gaussian and the peak concentration coincides with the ion range for the chosen energy. It is therefore possible to position the peak value at the desired depth simply by varying the implant energy. This feature offers considerable flexibility in device processing. The implantation process however damages the crystal lattice and the as-implanted atoms do not occupy substitutional lattice sites. Implantation is therefore followed by a high temperature anneal that repairs crystal damage and activates the dopant atoms. Conventional long time furnace annealing that is well suited for Si technology when applied to III-V semiconductors results in severe surface degradation unless proper measures are taken to suppress group V element out-diffusion, such as dielectric capping layers [84]. As an alternative, lamp and graphite strip annealing techniques that use fast ramps have been developed. The attractive features of these rapid thermal annealing (RTA) techniques are that extremely short anneal times (≈10-25 secs) at moderate temperatures (750 - 800°C) are sufficient to activate the dopant atoms and restore crystallinity and the anneals can be performed using close contact methods without the necessity of dielectric capping layers. Dopant redistribution is also minimal if the time-temperature cycle is carefully chosen. In general for InP, donors (e.g. Si and Se) exhibit better activation with minimal redistribution than acceptors (e.g. Zn and Be) [85].

Si is the most popular n type dopant used for InP based technology. Although Si is an amphoteric dopant in InP, like most dopants it predominantly occupies the In site and acts as a donor. We have used Si implantation to form the source and drain regions of the n channel FETs. The important parameters that characterize an implantation are the position and magnitude of the peak dopant concentration, the activation percentage, dopant redistribution, surface degradation during high temperature activation and post anneal residual implant damage. It is important to keep the peak position close to the interface for surface channel devices like MISFETs and near the heterojunction interface for buried channel HIGFETs.

Table 2.4. TRIM simulated range and straggle values for different material combinations for ion energies used in this study.

Material System	Density (gm/cm^3)	Energy (KeV)	Range (Å)	Straggle (Å)
Si_3N_4/InP	2.5/4.78	60	813	336
Si_3N_4/InP	2.5/4.78	80	1041	412
Si_3N_4/InP	2.5/4.78	100	1252	486
Au/Si_3N_4	19.3/2.5	80	423	217
Au/Si_3N_4	19.3/2.5	100	460	266

2.5.2 TRIM SIMULATIONS

The range of the implanted ions gives the position of the peak dopant concentration and is determined apriori using a software package that simulates the TRansport of Ions through Matter (TRIM), in other words, implantations. The values obtained from these simulations are tabulated in table 2.4 that lists the range for the Si_3N_4/InP combination and for Au, the gate

metal that acts as a mask to stop ions from reaching the channel region. The implantations are performed through the silicon nitride gate dielectric layer that also serves as a cap during the subsequent implant activation.

2.5.3 POLARON MEASUREMENTS

The post activation dopant profile is determined with the Polaron PN-4300 electrochemical profiler. This technique uses an electrolyte in contact with the semiconductor in a Schottky configuration to perform standard C-V measurements that yield dopant depth profiles. The maximum depth information in the case of a Schottky contact is limited by the reverse breakdown voltage. This drawback is overcome by using an electrolyte that dissolves the semiconductor in a slow and controlled manner. When a suitable voltage is applied accumulation of holes at the semiconductor surface causes electrochemical etching. n-type samples are illuminated with above band gap photons during etching to generate the holes. By performing C-V measurements at different depths, the complete dopant profile is obtained. For InP, 1M HCl solution is used as the electrolyte and the etch steps varies between 0.001-0.005μm [86].

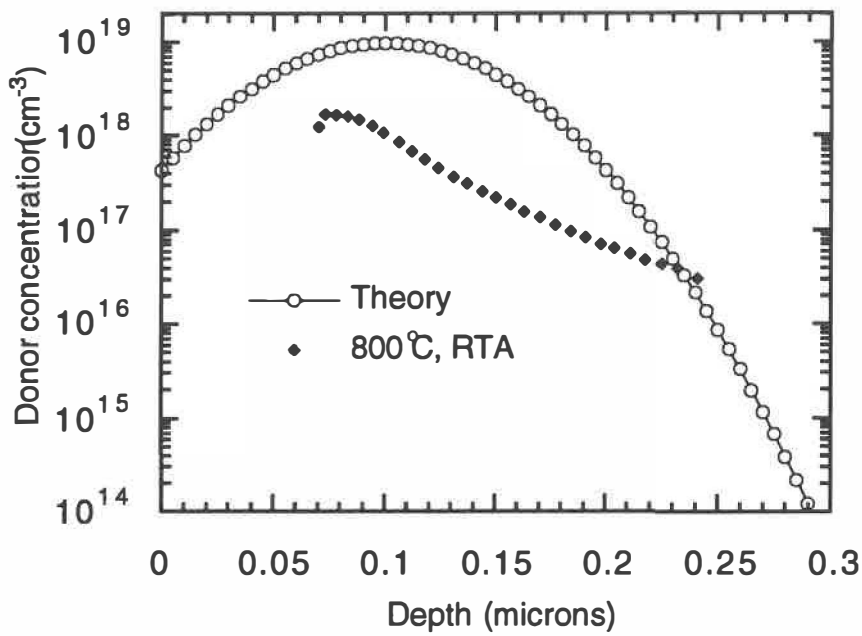


Figure 2.14 Polaron dopant depth profile of the $1x10^{14}/cm^2$, 80 keV Si implantation activated by a 800°C RTA. The theoretical Gaussian is shown for comparison.

2.5.4 RAPID THERMAL ACTIVATION

The initial experiments are performed on Fe doped semi-insulating InP substrates with a 550Å cap silicon nitride layer. The samples are implanted at room temperature (RT) with $^{28}Si^+$ ions at a dose of $1x10^{14}$ ions/cm^2 at 80 keV. Following implantation, we use a 800°C, 10 seconds rapid thermal activation anneal (RTA) that is reported to give optimal results for silicon implants. This anneal uses a fast ramp of 125°C/second and the sample is in contact with a silicon wafer during the anneal to prevent group V element loss. The post activation doping profile is determined using the Polaron electro-chemical profiler and is shown in figure 2.14 , the theoretical Gaussian is shown for comparison. Values of 0.1μm and 0.04μm for the ion Range (R_p) and lateral

Straggle (ΔR_p) are used to plot the theoretical curve. The experimental peak dopant concentration is $1.67 \times 10^{18}/\ cm^3$ and corresponds to an activation of 17%. The close contact anneal yields smooth surfaces with no visible degradation. However, indium balling-up on the surface restricts this method to temperatures below 900°C.

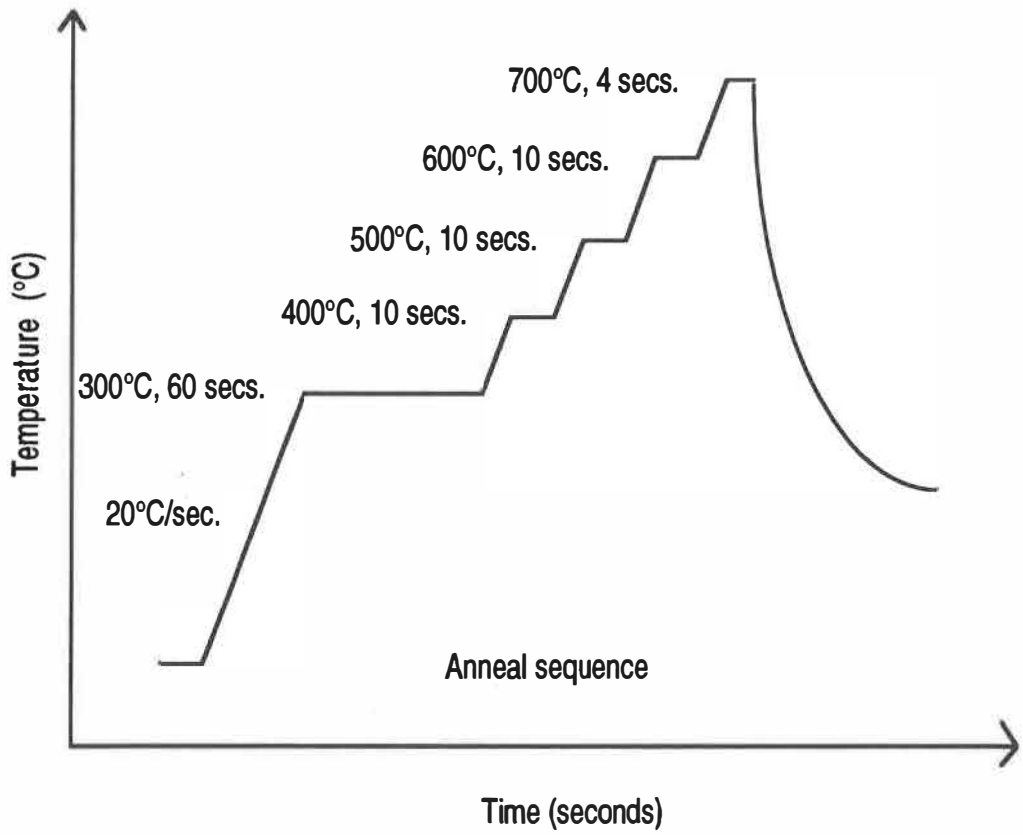


Figure 2.15 The 700°C SRLA anneal sequence used for implant activation.

2.5.5 SLOW RAMP LAMP ANNEAL (SRLA)

As seen later in chapter 6, RTA anneals using fast ramps (≈ 100°C/sec.) are not compatible with the metal gate technology and we discover that in lieu a multi-step Slow Ramp Lamp Anneal (SRLA), shown in figure 2.15 can be used

that preserves gate metal and insulator integrity. When fast ramps are used the top gate metal peels off completely due to the large difference in thermal expansion co-efficients between the metal and the substrate. Cracking and flaking-off of the nitride is also observed that renders the sample unusable. When the ramp up rate is reduced, sufficient time is allowed for thermal equilibrium to be reached and sample integrity is preserved. The term 'SRLA' is coined by us to describe our unique annealing procedure. The first temperature step is 300°C and is chosen close to the deposition temperature of the nitride. This 60 seconds anneal repairs the implantation damage to the nitride and completely eliminates nitride peeling-off at the implanted regions. The subsequent steps are spaced at 100°C until the final activation temperature of 700°C is reached. The samples are slowly ramped-up at 20°C/second between steps. The time of 10 seconds is sufficiently long to attain thermal equilibrium as evidenced by the excellent metal pattern integrity on the annealed samples.

2.5.5.1 POLARON PROFILES

Figure 2.16 shows the experimental polaron depth profile of a sample implanted at 80 keV for a dose of $1x10^{14}$ through 550Å Si_xN_y and activated using SRLAs with peak temperatures at 700°C and 800°C for 4 seconds. The first temperature step in the profile is chosen close to the insulator deposition temperature and the subsequent steps are spaced at 100°C. The peak dopant concentration for the 700°C and 800°C anneal are $1.72x10^{18}/cm^3$ and $2.78x10^{18}/cm^3$ and the corresponding activations are 18% and 28% respectively. The interesting thing to note is that the 700°C- 4 seconds SRLA cycle gives higher dopant activation than the 800°C-10 seconds RTA anneal.

Similarly, the 800°C SRLA results in higher activation when compared to a 775°C-25 seconds RTA that yields 26% activation for comparable doses [87]. It has been observed that activation usually saturates at around 20 - 30 % for Si RT implants and the values reported here are close to saturation. Apart from the activation, other issues of concern are that the implant damage may not be completely annealed out due to the shorter resident time at the peak temperature and the longer total anneal time might lead to broader profiles. We find that the RTA and SRLA anneals result in profiles of comparable width, and the absence of a twin peak in the SRLA polaron profiles signifies the absence of appreciable post anneal residual damage [87].

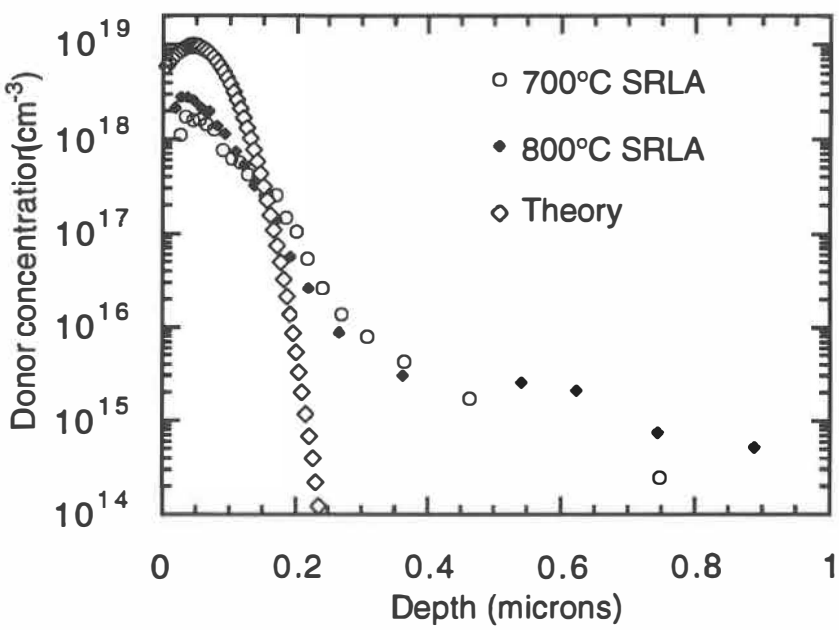


Figure 2.16 Polaron dopant depth profile of the $1x10^{14}/cm^2$, 80 keV Si implantation activated by a 800°C RTA. The theoretical curve is shown for comparison.

We use the lower temperature 700°C SRLA anneal for device fabrication since for the peak donor concentration of $1.72x10^{18}/cm^3$ the Fermi level is

inside the conduction band and these regions are sufficiently n^+ in nature to act as source and drain regions for the FETs.

Higher activation values can be obtained by performing elevated temperature (150 - 200°C) Si and P co-implantation and by annealing at slightly higher temperatures and for longer times, e.g. 800°C - 8-10 seconds SRLA [88]. Phosphorus (P) co-implantation is also used to combat anomalous in-diffusion of dopants into the substrate. The in-diffusion results in long tails or humps in the dopant profile and is caused by surface stoichiometric disturbances that occur for high dose implantations or during thermal annealing [89]. We have already performed a similar study on the characteristics of low dose ($1x10^{11}$ -$1x10^{12}$ ions/cm^2) heated (200°C) Zn implantations in InP and activated by RTA [89]. We find that heated implantations result in 90+ % activation with minimal dopant redistribution. This work can be easily extended to the case of heated Si implants.

2.6 CONTACTS

Stable, low resistivity contact formation is a crucial step in device fabrication. It has been observed that for high speed devices with low channel resistances the ultimate performance is limited by the parasitic source/drain contact resistances [90]. Non-linearity of I-V characteristics is another cause for concern that has to be overcome to obtain reliable high frequency performance [91]. There has been considerable effort in recent years to realize extremely low resistive and reliable ohmic contacts to III-V materials and their alloys that are used in high speed device technology. There are a number of detailed reports in the recent literature on ohmic contacts to n-InP [90,91,94].

Au-Ge-Ni metallization is the most attractive technique to contact n-type InP with good uniformity, low contact resistivity and high linearity. This contacting procedure is so popular that almost every report in the current literature on InP based devices uses Au-Ge-Ni to contact n-type regions. Au-Ge-Ni contacts are usually highly ohmic with low contact resistivities of a few $\mu\Omega/cm^2$. In this scheme, Ge acts as a n type dopant while Au decreases the overall contact resistance and Ni is used to improve the adhesion of the metallic film to the semiconductor surface. These contacts are normally RTA annealed in the temperature range 375-450°C in forming gas (N_2+ 10%H_2) for times varying from a few seconds to several minutes. The surface morphology of the contact is an important consideration and it is necessary to produce smooth a morphology without Ge or Au cluster formation. We have not attempted to optimize this contact scheme but rather use the available literature to establish our conditions [91].

In this study, use a Au-Ge+10 wt % Ni mixture that is e-beam evaporated to form the contacts. The thickness of the contact usually varies from 500-1000Å. The contacts are annealed at 420°C for 10 seconds in a forming gas atmosphere. The contact resistivity and the sheet resistance of implanted regions are monitored by the standard Transmission Line Model (TLM) structures [92].

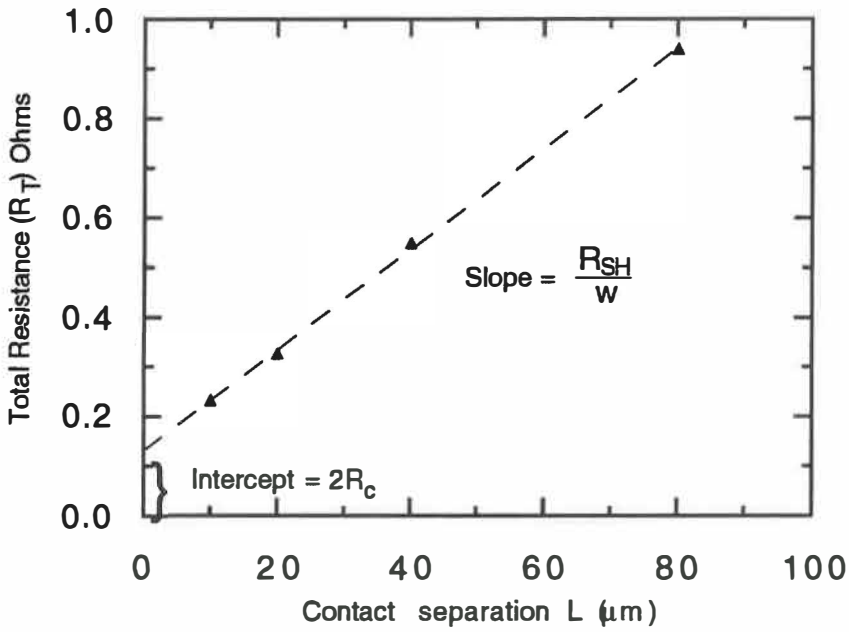


Figure 2.17 Plot of total resistance (R_T) with contact length. The slope gives the implantation sheet resistance R_{SH} and the intercept the contact resistance R_C. w refers to the width of the contact.

2.6.1 TRANSMISSION LINE MODEL

The TLM structure used for planar contact resistance measurements is a series of ohmic contacts of identical areas spaced at varying intervals l_1, l_2, l_3, l_4. The total resistance (R_T) between 2 adjacent contacts is measured and plotted as a function of contact separation as shown in figure 2.17. R_T varies linearly with distance and can be written as the sum of two components.

$$R_T = 2R_C + R_{SH}\frac{l}{w} \qquad (2.2)$$

where R_C is the resistance of a single contact, R_{SH} is the sheet resistance of the implanted layer, l the contact separation and w the width of the region between contacts. In the absence of current spreading/crowding, as in our case, w is equal to the width of the contacts. Thus the intercept is equal to $2R_C$ and the

slope equals R_{SH}/w. To find an analytical solution, the contacts are modeled as a transmission line and the contact resistance given by [93]

$$R_c = \frac{\sqrt{R_{SH} \cdot \rho_c}}{w} \mathrm{Coth}(\alpha.d) \qquad (2.3)$$

Where ρ_C is the contact resistivity and w is the width of the contact, d the length of the contact and α denotes the transfer length or the current injecting / collecting portion of the contacts. For electrically long contacts $\alpha d >> 2$ and coth $(\alpha d) = 1$. This condition is always met when the contact length $d \geq 80\ \mu m$ [94].

The resistivity ρ_C is then

$$\rho_c = \frac{w^2.R_C}{R_S} \qquad (2.4)$$

where R_S is the sheet resistance of the layer immediately beneath the contact and is different from R_{SH}. In order to determine R_S, Harrison and Reeves perform an end resistance (R_E) measurement as shown in figure 2.18 [95]. The end resistance, R_E, is the extra resistance that is present when the contact is included in the measurement and is related to the contact resistivity. This type of measurement assumes that the semiconductor potential further from the contact is equal to the value at its edge.

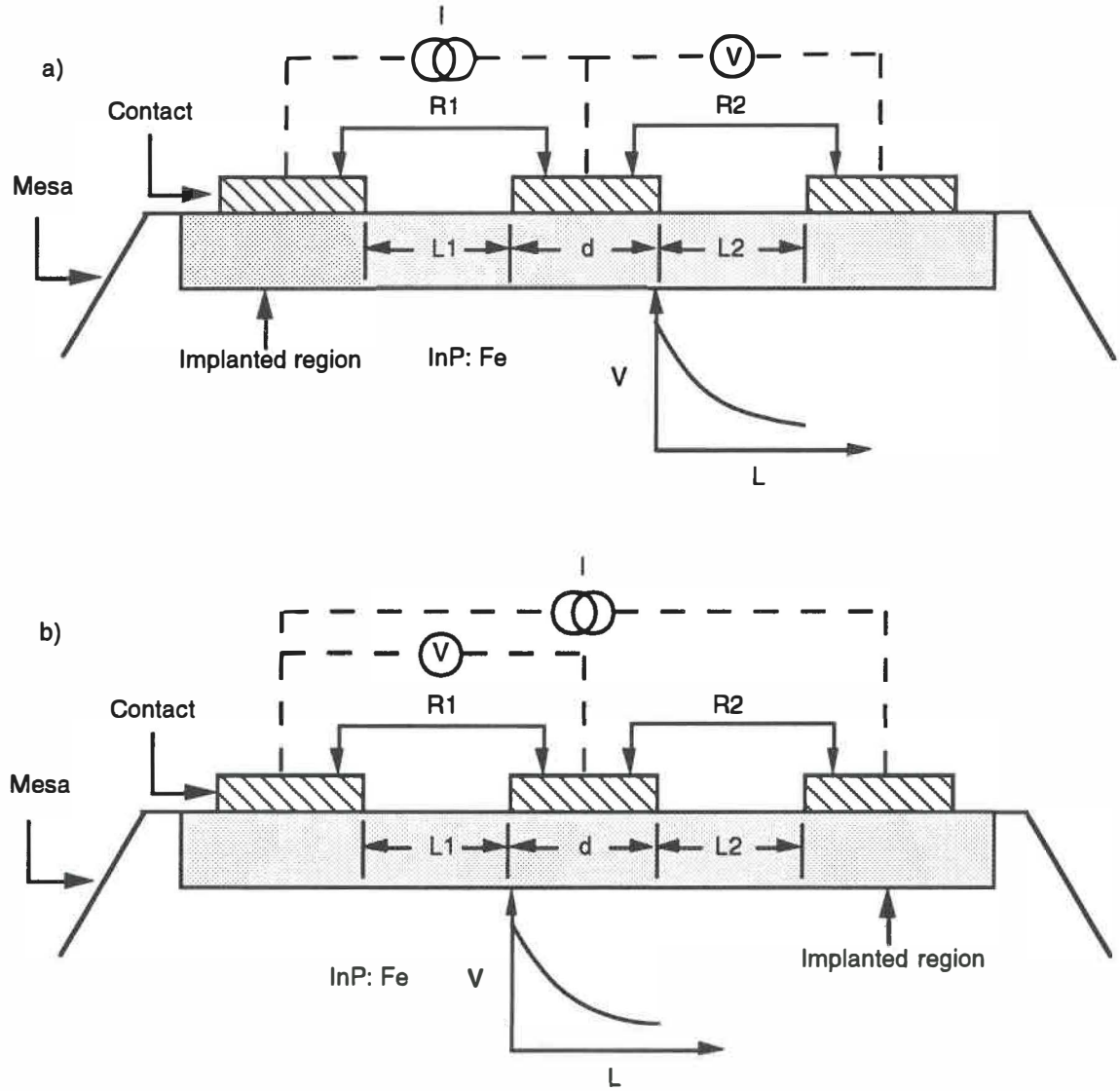


Figure 2.18. a) Potential variation with separation of the unloaded contact and b) potential variation within a contact.

This is not a valid assumption since our experiments show that there is a potential variation with the distance of the unloaded contact as shown in figure 2.18. In fact, it has been shown that the potential falls-off exponentially even within the contact [96]. This drop is large when measurements are made on regions with large sheet resistance values. The end resistance or floating gate measurements therefore show a strong R_E variation depending where the

probe is located. More work is required to correctly clarify the situation. We therefore assume that $R_S = R_{SH}$ for our measurements.

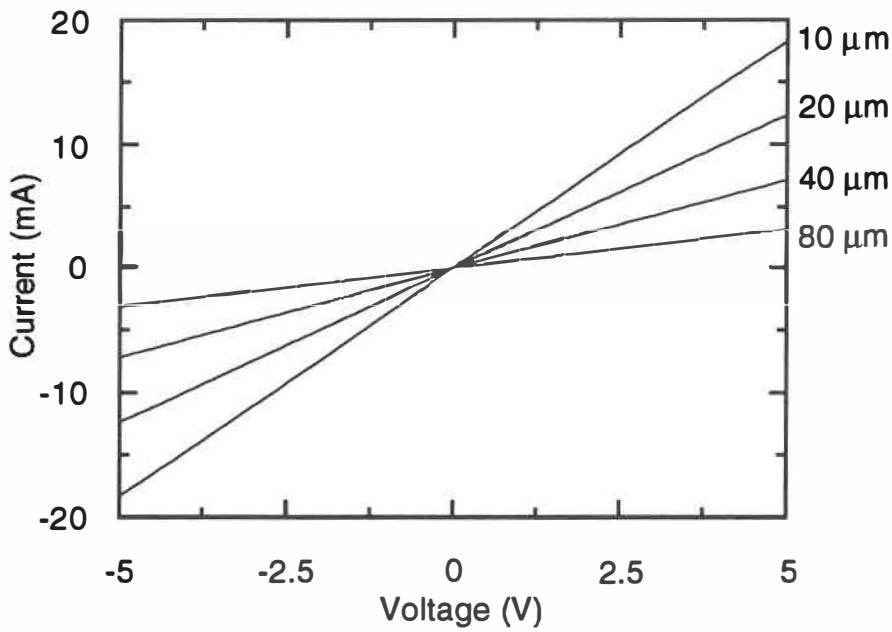


Figure 2.19 I-V characteristics of the Au-Ge-Ni contacts to a Si implanted and mesa isolated region arranged in a TLM structure with different contact separations.

2.6.2 CONTACT RESISTIVITY MEASUREMENTS

Electrical measurements to evaluate the contacts are performed on TLM structures with contact separations of 10, 20,40 and 80 µms. The as-annealed contacts exhibit smooth surfaces with contact resistivities in the of 1-2 $m\Omega/cm^2$ range. A subsequent anneal at 400°C for 30 minutes reduces the contact resistivity to a minimum value of 15 $\mu\Omega/cm^2$. Further anneal again increases resistivity values to the 80-100 $\mu\Omega/cm^2$ range. We find that the contact resistivities and implanted sheet resistances depend strongly on the sample type. Au-Ge-Ni contacts to Fe doped SI samples always exhibit highly linear ohmic I-V behavior. Figure 2.19 show the I-V characteristics of the TLM structure

for different contact spacings for an implanted SI sample and figure 2.17 shows the variation of the total resistance R_T with the contact separation L. Further we find the sulfur passivation process used in this study affects the contact resistivity as regions that are strongly sulfurized usually showed larger resistivities than those that are mildly sulfurized. This problem is addressed in more detail in chapter 6.

In conclusion, we have developed the technology base to fabricate insulated gate devices on InP, particularly suitable for SAGFETs. The existing technologies for InP are reviewed and some are adopted as is while others are fine tuned or characterized in detail according to the need. In particular we present a complete set of experiments to characterize heterostructure wafers for FET applications and the first detailed characterization of the iodic acid system that is extensively used in InP processing. A few new processes have resulted from this effort, the first is a H_3PO_4 based soft etchant for InP, a simple indirect plasma dielectric deposition technique and a slow ramp lamp anneal sequence specially suited for the SAGFET technology. The other fabrication areas have been characterized on a need basis. In the next chapter, we apply the indirect plasma technique to fabricate MIS structures and to study and characterize the passivated interface.

CHAPTER 3
INTERFACE ENGINEERED MIS DIODES

3.1 INTRODUCTION

The first step in implementing an insulated gate SAG process is to fabricate MIS diodes with low interface state densities. We have seen in chapters 1 and 2 that the S passivation process is effective in reducing P out-diffusion and the states associated with P vacancies and the indirect plasma deposition scheme eliminates/lowers plasma damage of Si substrates resulting in good high frequency (100 KHz) C-V characteristics. It now remains to be seen if these independent techniques can be combined to produce InP/silicon nitride interfaces with low trap densities. A large number of interface states (> 10^{13}/ cm^2.eV) pin the Fermi level at the interface and while present in slightly lower magnitudes ($\approx 10^{12}$ - 10^{13}/ cm^2.eV) require large changes in gate voltage to bring about small changes in the surface potential. Changes in gate voltage, therefore serve to modify the occupancy of the interface states and modulation of the channel charge is negligible or minimal. As a result varying the gate voltage brings about small changes in drain current and result in poor FET performance. It is therefore imperative to obtain interfaces state densities in the 10^{10} - 10^{11}/cm^2.eV range for an insulated gate FET technology to be viable [80].

We are encouraged by the work of Iyer and Lile, who fabricated MIS structures on InP with low trap densities using the sulfur passivation technique. They deposited silicon oxide gate dielectric on S passivated InP surfaces in a specially built indirect plasma system. O_2 is pre-ionized and made to react with

SiH_4 in the deposition chamber thereby completely eliminating plasma damage [97]. As mentioned before in chapter 2, such systems are quite expensive to build [97,50] and we have adopted the simpler strategy of protecting the sample with a metal cover in a conventional direct plasma system. Although this set-up works fine with Si, as seen in chapter 2, it needs to be proven for InP which is more susceptible to plasma damage. The other uncertainties are the compatibility of the passivation process with silicon nitride and its high temperature stability.

The principal issues are insulator leakage, the nature of the MIS C-V characteristics, the magnitude and distribution of interface states in the InP band gap and the thermal stability of the MIS diodes. A preliminary DLTS study that provides an estimate of the activation energy and capture cross-sections of the interface traps at the S passivated InP/nitride insulator is also presented.

3.2 FABRICATION OF INTERFACE ENGINEERED MIS CAPACITORS

The undoped InP substrates, with residual n doping in the $1\text{-}5\times10^{15}/\ cm^3$ range, used in these studies are subjected to the standard cleaning cycle. They are then immersed into a 20% solution of $(NH_4)_2S_x$ in water that is maintained at approximately 60-65°C for about 30 minutes. Care is taken to not expose the sample to air during transfer. The process deposits a thin layer of elemental sulfur on the sample surface. In some cases the passivation is performed under illumination to enhance the surface reaction. The results in both cases are quite similar. One set of samples are not S treated to compare the effect of the passivation process. The samples are then transported under vacuum and

loaded immediately into the modified indirect plasma system described in chapter 3 and a 500Å silicon nitride layer is grown at 250-300°C. It is important to keep the ramp-up time as short as possible to avoid InP surface degradation. The typical time required for our system which has a large thermal load is about 20 minutes. Following the PECVD process, Ti/Au/Ti gates of 1mm diameter are sequentially e-beam deposited without breaking vacuum and Au/Ge/10%Ni is evaporated on the back side of the samples. A final anneal in forming gas at 350°C for 5 minutes, serves the dual purpose of forming the ohmic contacts and H passivating the interface.

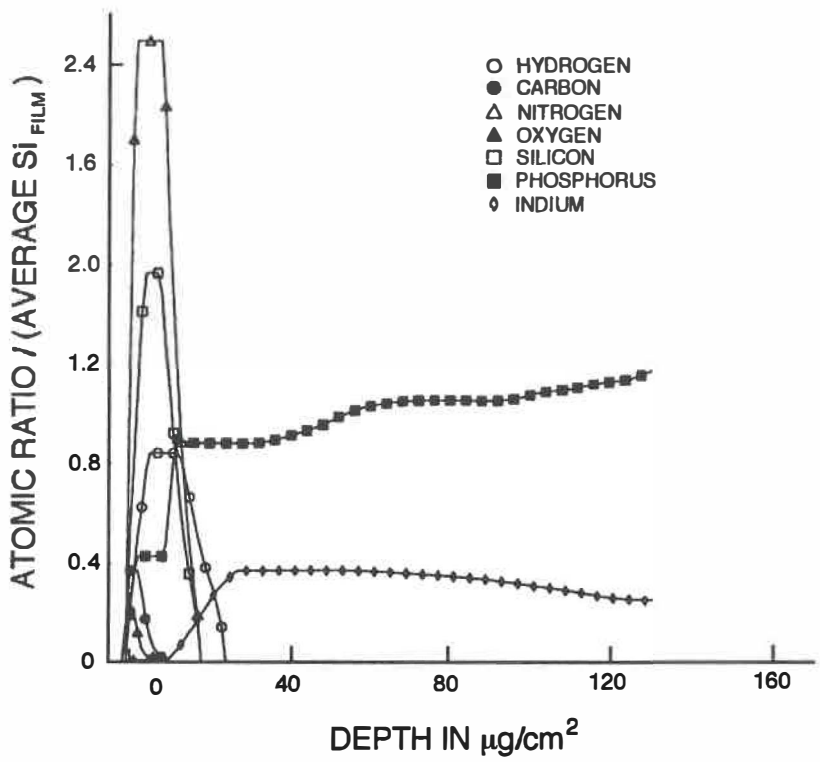


Figure 3.1 ERD depth profile of indirect plasma silicon nitride on InP.

3.3 THE DIELECTRIC ON S TREATED INP

The ERD depth profile of the nitride deposited on InP passivated for 30 minutes in $(NH_4)_2S$ under illumination is shown in figure 3.1. The profile is similar to that presented in chapter 3 on Si substrates, however the film thickness is about half that of the layer measured on Si. The film stoichiometry is approximately $SiN_{1.6}:H_{0.5}$. As mentioned earlier, we are not able to estimate the amount of S incorporation in the films due to limitations imposed by the probe beam. The incident chlorine beam is mass separated from S by only 1 amu and gives rise to a strong, broad peak that completely submerges the S signal. However, it may be possible to use a different probe, such as a sodium beam, with a large mass separation to detect S. The variation of P/In ratio of the substrate from 1.0 is related to the contribution from the tail part of the chlorine signal to the P line and probably a larger phosphorus scattering in the forward direction.

3.4 DIELECTRIC LEAKAGE

3.4.1 I-V CHARACTERISTICS

The inclusion of S in the films can be indirectly observed by studying the leakage characteristics of the MIS diodes. It has been previously observed that P incorporation in SiO_2 leads to leakage and S should have a similar effect on the nitride. We perform I-V measurements on two samples, one mildly passivated (S1) for 10 minutes and the other (S2) strongly for 45 minutes. Passivation is referred to as mild when the deposited S is visible only under a microscope. On the other hand, a passivation cycle is considered strong if it leaves a layer of sulfur on the sample surface clearly visible to the naked eye.

The results are shown in figure 3.2, CAP 1-4 denote different MIS diodes on sample S2.

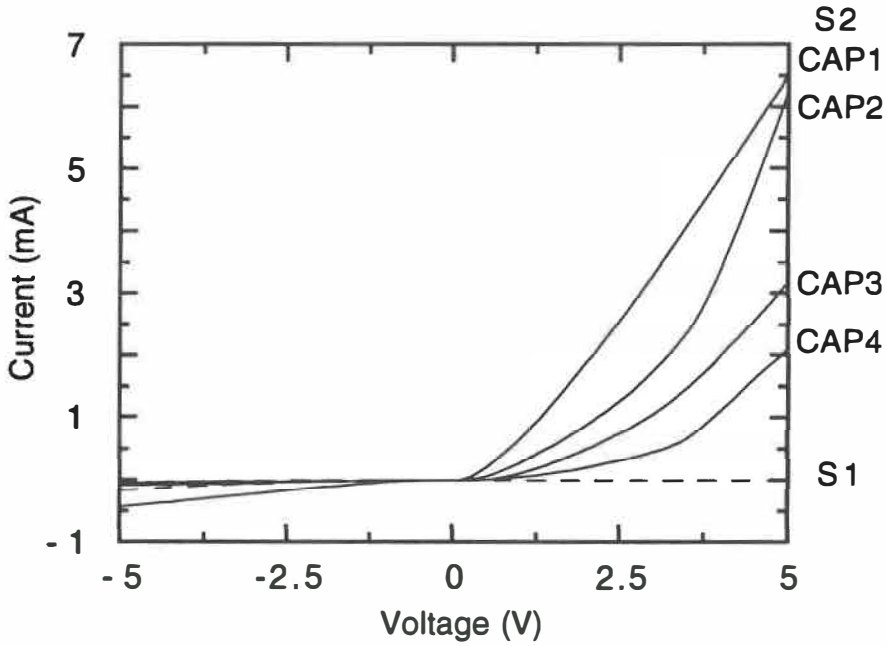


Figure 3.2. Leakage current Vs voltage characteristics of a) mildly sulfurized (S1) and b) strongly sulfurized (S2) Au/Ti/Silicon Nitride/undoped InP MIS diodes.

Sample (S2), that is strongly sulfurized exhibits large leakage under accumulation conditions and the I-V resembles a Schottky diode. On the other hand, milder S treatment results in low leakage in inversion. It therefore appears that prolonged passivation results in S incorporation in the dielectric leading to poor leakage characteristics. As seen later in chapter 7 leakage (> 1mA) degrades the performance of the SAGFETs and it is imperative to completely suppress current leakage through the dielectric. The other striking factor is the non-uniformity in the I-V measurements as seen for MIS diodes CAP 1-4. Non-uniformity is a major cause of concern and results in large variations in transistor characteristics. Such uniformity problems stem from the

chemical nature of the passivation process and rapid aging of the $(NH_4)_2S$ solution with time [98].

3.5 THE INP/NITRIDE INTERFACE

3.5.1 C-V CHARACTERISTICS

Applying appropriate voltages to the MIS capacitor gate alters the semiconductor surface potential and the interface Fermi level is scanned in the band gap from the conduction to valence bands of the semiconductor leading to accumulation and inversion conditions. Presence of interface states in the band gap act as a source of "friction" and affect the Fermi level movement inside the band gap. When the Fermi level encounters a group of states at a particular energy, changes in gate voltage will now have to change the occupancy of these states in addition to the depletion region charge and the Fermi level movement with voltage will be retarded. Depending on the interface trap concentration this movement can be uninhibited, slowed down or completely stopped. The first case refers to concentrations of $1x10^{10}$ - $5x10^{11}$ states/cm^2 and above these values the motion is lethargic and at concentrations of $1x10^{13}$ states/cm^2 the movement will be stopped. Thus by studying the energy movement of the Fermi level with gate voltage in the band gap, one can determine the magnitude and spread of the interface trap states. The question now is how does one determine the energy motion of the Fermi level. The answer is rather simple since variations in surface potential that accompany the Fermi level movement alter the band bending and the depletion capacitance and therefore the measured capacitance. Thus by studying the capacitance variation with gate voltage we can estimate the extent of band bending and

therefore the Fermi level position in the band gap. When the Fermi level is swept slowly due to the presence of traps the measured capacitance varies slowly with applied voltage stretching the C-V curve along the voltage axis. In contrast mobile charges in the oxide and fixed charges at the interface shift the C-V curve along the voltage axis without altering the shape. Shape distortion is caused by states at or close to the surface and an interface trap with a pronounced structure would give rise to a specific shape distortion. The C-V characteristics are therefore representative of the quality of the interface. In particular high frequency characteristics are popular as they avoid the ac capacitance contribution of the surface states in their measurements [80].

To measure capacitance as a function of bias in steady state, a small ac voltage is superimposed on the gate bias and the differential capacitance defined as $C \equiv dQ_T/dV_G$ is measured. The amplitude range should be within the small signal range viz. linear response of ac current to ac voltage and the frequency should be high enough that surface states do not respond to the ac signal. The interface states therefore do not contribute to the high frequency capacitance. However since trap states follow the gate bias, they affect the static capacitance $C_{stat} \equiv Q_T/V_G$ that is related to the band bending. In this work we have used the high frequency (HF) C-V measurements as a tool to determine the quality of the interface and the efficiency of the passivation process.

By comparing the measured C-V with the theoretical C-V curve for the ideal MIS without surface states, one can estimate the position and concentration of surface states in the band gap. The HF method, originally proposed by Terman is used extensively in the literature to determine interface trap concentration in MIS structures [99]. The elegance of this method lies in the

simple concept that regardless of the trap density at the interface, the measured capacitance C_{HF} normalized to the value of the insulator capacitance C_{nit} will be identical to the ideal capacitance value expected for the same amount of band bending (Ψ_s). Thus by comparing the measured C_{HF}/C_{nit} versus V_G values with the computed C_{HF}/C_{nit} versus Ψ_s curve for an ideal MIS capacitor with zero interface states we construct a plot of Ψ_s versus V_G viz. variation of band bending with gate voltage that essentially determines the shape of the C-V curve. The capacitance associated with the interface state density (C_{it}) is then calculated by taking the derivative of this curve and using the formula (99,100)

$$C_{it}(\Psi_s) = C_{nit}\left[\left(\frac{d\Psi_s}{dV_G}\right)^{-1} - 1\right] - C_s(\Psi_s) \qquad (3.1)$$

Where C_s is the semiconductor surface capacitance per unit area. Knowing C_{it} we determine the interface trap density (D_{it}) from

$$C_{it}(\Psi_s) = qD_{it}(\phi_s) \qquad (3.2)$$

Where ϕ_s is the interface or semiconductor surface potential. Each value of Ψ_s corresponds to a position in the band gap. Thus D_{it} values can be determined from the CB edge to the VB edge. The exact position in the band gap for n type samples is determined by the equation.

$$E_C - E_T = \frac{E_g}{2} - \phi_b - \Psi_s \qquad (3.3)$$

where E_T is the energy of the trap, E_g the band gap of InP and ϕ_b the semiconductor bulk potential.

3.5.2 EXPERIMENTAL RESULTS

Figure 3.3 shows the experimental high frequency C-V curves for the sulfur passivated and unpassivated Ti/Au/Si_3N_4/undoped InP MIS capacitors.

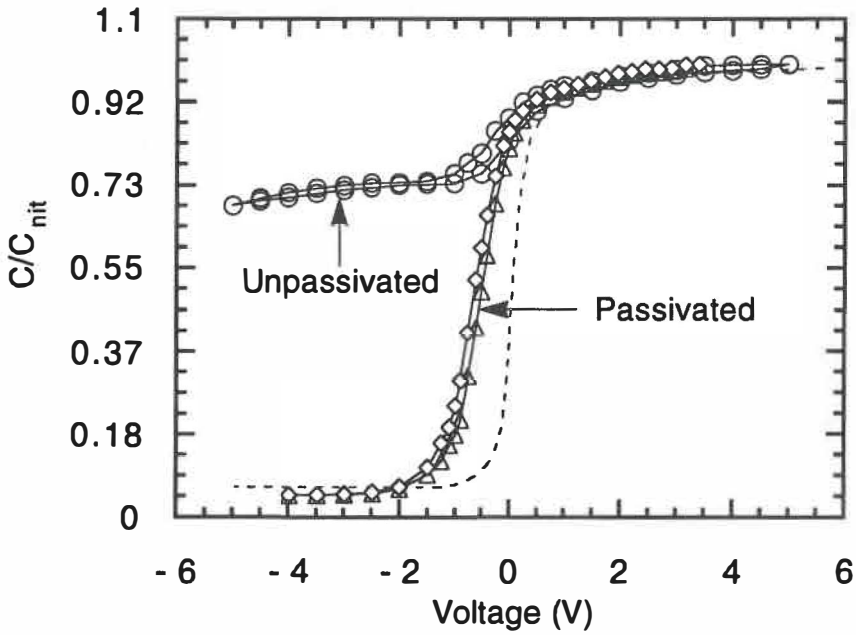


Figure 3.3. High frequency (100 KHz) C-V curves of sulfur passivated and unpassivated Ti/Au/Si_3N_4/undoped InP MIS capacitors. The theoretical curve in dotted line is shown for comparison.

The theoretical C-V curve for N_D= $1x10^{15}$/ cm^3 and t_{nit} = 550Å is drawn in dashed line and shown for comparison. The equations used for drawing this curve are given in Annexe II [100]. For the untreated sample the curve tends to flatten out at a $C/C_{nitride}$ value of 0.72. As explained earlier, this corresponds to a large density of interface states at around 0.15 eV below the conduction band edge. This is consistent with the photoluminescence results of chapter 2, that indicate a broad level due to P vacancy related complexes at approximately the same energy value. As a result, in unpassivated device structures the semiconductor surface is always under accumulation and cannot be driven into inversion. As will be seen later in chapter 7 the drain current in unpassivated

MISFETs cannot be modulated. Annealing in forming gas does not affect the characteristics of these MIS diodes. This anneal however has a dramatic effect on the S passivated samples. S passivation followed by an anneal in forming gas results in C-V characteristics similar to the theoretical curve with negligible (< 0.1V) hysterisis. As observed from figure 3.4 the N_2/H_2 anneal cycle is important to obtain good C-V characteristics. Referring to the results of chapter 2, the passivation mechanism is due to S reacting with the InP substrate and reducing P loss from the surface by forming a 30Å thick cap layer of In_2S_3. However, this leads to the creation of trap states centered at 0.94 eV in the band gap, which are mainly present in the cap layer. Interestingly, it appears that these states unlike the P vacancies can be H passivated by annealing in N_2/H_2. Interface passivation in sulfur treated MIS structures therefore proceeds in two steps - a) S filling up P vacancies and reducing surface P loss by forming a thin 30Å cap layer of In_2S_3 and b) H passivation of the states present mainly in the cap layer.

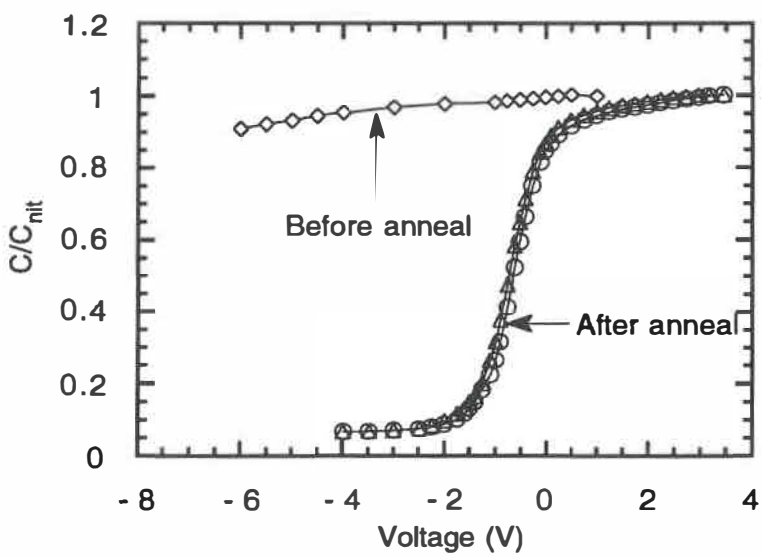


Figure 3.4 The high frequency capacitance-voltage curves before and after the 300°C anneal in forming gas.

3.5.3 SURFACE STATE DENSITY

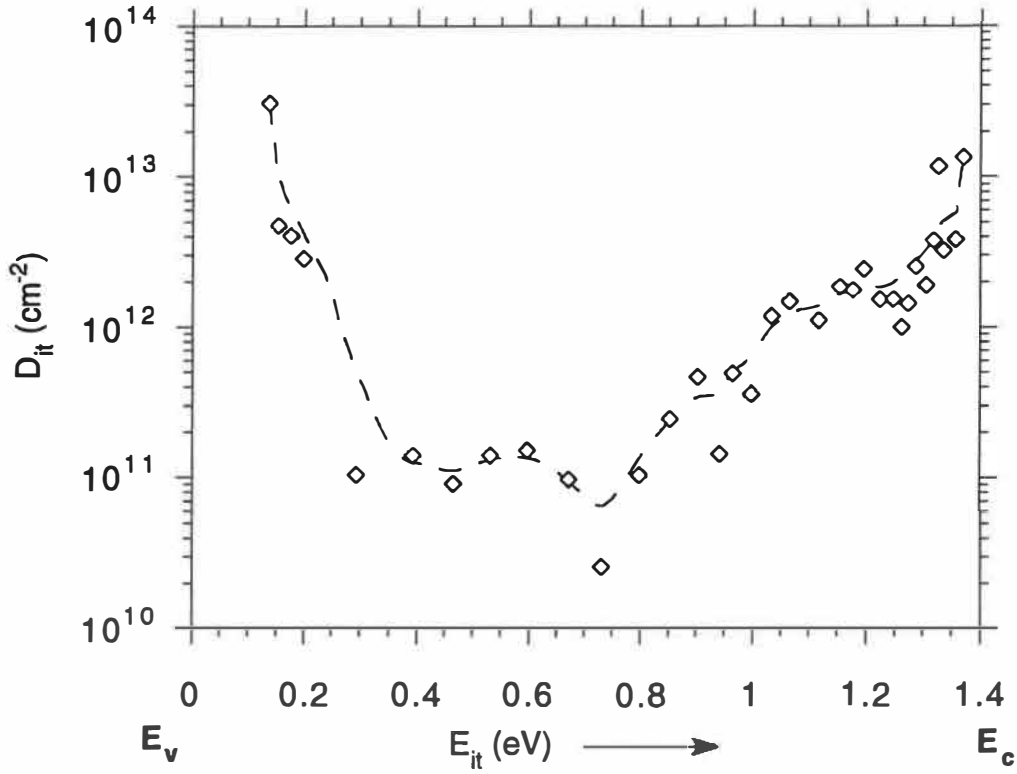


Figure 3.5. Variation of interface state density with energy in the InP bandgap calculated by the high frequency C-V (Terman) method for a sulfur passivated MIS diode. The dotted line is the curve fit to the experimental data. Note the minimum value at midgap of $8x10^{10}/cm^2.eV$ is the lowest value reported for S passivated MIS structures using silicon nitride.

By comparing the experimental curve with the theoretical curve for $N_D = 1x10^{15}/cm^3$ and t_{nit} = 550Å, we estimate the variation of interface state density in the band gap. The results are shown in figure 3.5. The minimum value of interface states is about $8x10^{10}$ $cm^{-2}.eV^{-1}$ and occurs approximately at the mid-gap position. It is interesting to note that this is the first report on the application of the S passivation process to silicon nitride with low interface state densities and excellent C-V characteristics. This is important since SiN_X is popularly used

as a passivation layer and as an encapsulant, something not readily achievable with SiO_x because of its greater porosity. Recently, another group has reported similar results on polysulfide treated InP using a ECR plasma nitride [50]. This value is comparable to those obtained with SiO_2 as the gate insulator. The next section describes a method to determine the interface state characteristics by Deep Level Transient Spectroscopy (DLTS).

The frequency dispersion of the C-V curves for two sulfur passivated capacitors are shown in figures 3.6 & 3.7. In the first case, the dispersion is minimal while we observe considerable dispersion in the second case, especially at high frequencies. This frequency dispersion is due to the extra parasitic series resistance (R_S) in the equivalent circuit in accumulation as shown in the inset of figure 3.7. This series resistance can be due to the low doped substrate or due to the back ohmic contact. For some MIS diodes, the low frequency capacitance increases linearly in accumulation. This is probably due to traps in the nitride near the metal electrode that respond to the applied frequency. This would result in an apparent decrease of the insulator thickness and the measured capacitance would be higher. Since the drop across the oxide varies linearly in accumulation, we expect a linear variation in capacitance too.

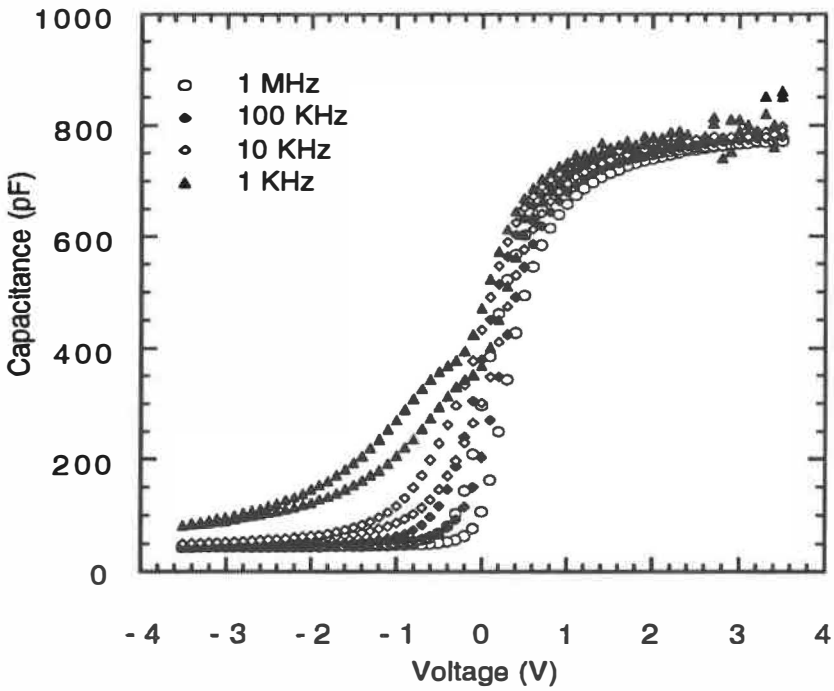


Figure 3.6. Sulfur passivated MIS capacitor exhibiting small frequency dispersion and hysterisis in its C(f) - V characteristics.

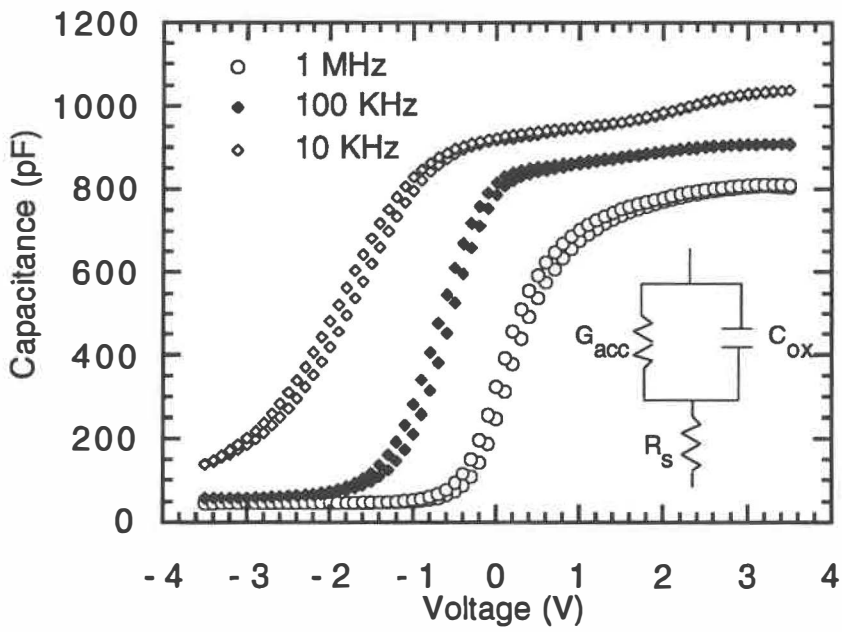


Figure 3.7. Sulfur passivated MIS capacitor exhibiting frequency dispersion due to extra parasitic resistance R_S shown in the equivalent circuit for the MIS capacitor in accumulation.

3.6 INTERFACE TRAP CHARACTERISTICS

3.6.1 DEEP LEVEL TRANSIENT SPECTROSCOPY

Deep Level Transient Spectroscopy (DLTS) offers a relatively simple yet powerful way to determine the trap parameters of bulk and interface states. DLTS is originally developed by D.V.Lang to characterize the discrete trap states in the bulk and use a Schottky configuration [101]. In DLTS, the device is reverse biased with the formation of a space charge region. A zero/forward bias filling pulse is applied that reduces the space charge region and fills the traps with majority carriers in the region where the space charge is collapsed. When the filling pulse is removed the traps start emptying with their natural emission time constant (τ) resulting in an exponential capacitance transient. The capacitance change (ΔC) is sampled at two points in time (t_1 and t_2) and $\Delta t = t_1 - t_2$ is called the rate window. This would result in a specific value of ΔC for the given rate window at the particular value of temperature T. If T is changed, the shape of the capacitance transient changes and results in a different value of ΔC. ΔC therefore varies with temperature and exhibits a peak value for that temperature "T" when the emission time constant (τ_n) matches the system time constant, i.e..

$$\tau_n = \frac{t_2 - t_1}{\ln\left(\frac{t_2}{t_1}\right)} \tag{3.4}$$

Traps with different characteristics produce peaks at different T. By measuring the capacitance transients as a function of T for different rate windows important trap parameters such as the capture cross-section (σ_o), the activation energy (E_A), the energy position and concentration are obtained.

In our case, we are dealing with interface traps which are distributed in a continuous fashion in the band gap with different capture cross-sections and different activation energies. The situation is more complicated since the trap parameters are both temperature and energy dependent [102]. The large pulse method that works well for discrete bulk traps cannot be directly applied to interface traps. When a large filling pulse is applied emission from a multitude of traps with different activation energies would give rise to a broad spectrum and information from traps at particular energy values would be lost or difficult to extract [103]. A modified small signal version of DLTS is therefore used to obtain the interface state properties of MIS structures and is described below [102,103].

An appropriate bias to the gate electrode is applied and the interface Fermi-level is fixed at a particular energy value. Now by applying a small filling voltage pulse we change the occupancy of the states in a narrow energy region (ΔE_F) near the Fermi level. When the pulse is removed, the Fermi level will return to its original value with emission of carriers from the traps resulting in a capacitance transient and an interface state signal peak with temperature. The DLTS peaks associated with interface states will shift with bias unlike the DLTS peaks from bulk states and interface traps can be easily identified and studied as a function of position in the band gap. The exact energy position is determined as described earlier by measuring the C-V characteristics for the temperature at which the peak occurs.

The theoretical treatment we have followed is detailed in ref.102 and is reproduced in Annexe III. We can write the emission time constant (τ_n) in the form

$$\tau_n = \left[v_{th}.N_d.\sigma_o(E_t).e^{\left\{\frac{-\Delta E_\sigma (E_T) + qV_s - \frac{1}{2}\Delta E_F}{kT}\right\}} \right]^{-1} \qquad (3.5)$$

Where v_{th} is the thermal velocity of the carriers, N_d the doping density, $\sigma_o(E_t)$ the capture cross-section of the interface state at the energy E_t, ΔE_σ is a constant related to the variation of the capture cross-section with energy, V_s is the semiconductor surface potential and ΔE_F is the fluctuation of the Fermi-level due to the small filling pulse.

By measuring the variation of the peak position with T for different rate windows, we get an Arrhenius plot of $\ln(\tau)$ vs T^{-1}. The slope of this plot gives the apparent activation energy ($E_A = \Delta E_\sigma(E_t) + qV_S - 1/2\Delta E_F$) and the intersection yields $v_{th}N_D\sigma_o(E_t)$.

3.6.2 EXPERIMENTAL RESULTS

The DLTS experiments are performed using the Polaron apparatus at the EE department at the University of Sherbrooke with the kind assistance of Dr. Çetin Aktik. We measure the DLTS spectra for S treated MIS diodes in the gate voltage (V_G) range 0.6-2.0V for four different rate windows. The filling pulse height is 0.15V. Figure 3.8 shows a typical DLTS spectrum for a gate bias of 0.8V. Apart from the peak around 215 K the shoulder of a higher T peak is also seen. For gate biases below 0.6V the lower T peak is not observed. We did not measure the trap properties related to the high T peaks.

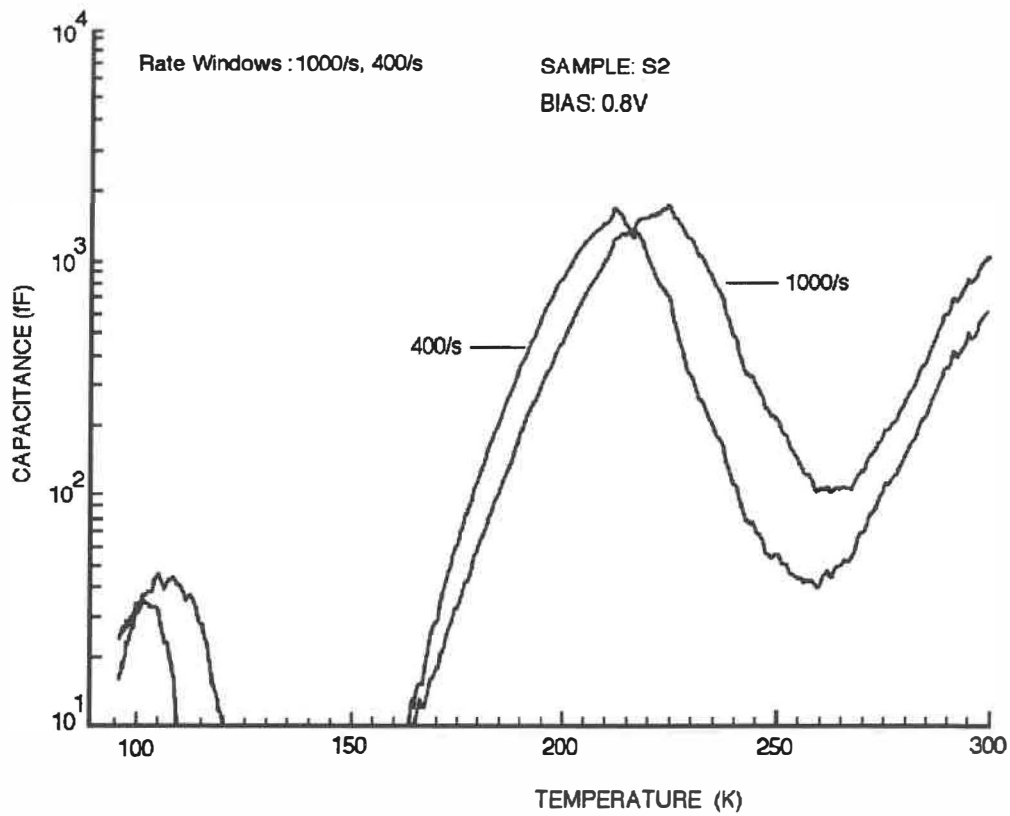


Figure 3.8. Typical DLTS spectrum of a S interface engineered MIS diode for two different rate windows. The gate bias is 0.8V.

The results of the DLTS experiments are tabulated in tables 3.1 and 3.2. It is important to note that only those values when the semiconductor surface is under accumulation or weak depletion are valid i.e.. for V_G = -0.6 - 0.9 V. DLTS for n-type MIS structures provides reliable information only for traps located in the upper half of the band gap. For large positive V_G values, the Fermi level is in the bottom half of the bandgap and the semiconductor surface is under inversion. The number of available majority carriers (electrons) in inversion is quite small and only a portion of the traps will be filled when the filling pulse is applied. Presence of minority carriers at the interface will also affect the trap

emission rates. Even in the case of mild or strong accumulation, the electron concentration at the interface will affect the emission characteristics, but is normally neglected. In depletion/inversion, apart from the capacitance transient due to the traps, the space charge width and the measured capacitance changes due to carrier generation within the space charge region and we might be measuring the minority carrier generation rate instead. Usually, for good quality semiconductors, this is not a problem since the generation rates are in the order of seconds. The DLTS technique is ideally suited to measure emission rates in the order of a few milliseconds and is not particularly useful to measure extremely fast (< 1ns) or slow (> .1 sec) traps. This is important since presence of slow traps at the unpassivated InP/insulator interface is the major cause for drain current drift with time in InP based MISFETs. As seen later in Chapter 7 the measured drain current drift for passivated SAGFETs is quite small indicating the absence of a significant number of slow traps at the interface.

Table 3.1. Position of DLTS peaks for different rate windows and gate bias.

V applied (Volts)	Peak Temperatures for Rate Windows (/ second)			
	1000	400	200	80
-1.5	241.5	231.5	225	214.5
-1.4	240	229	224	216
-1.2	235	224.5	217.5	208
-1.1	233	225	215	205
-1.0	225.5	215.5	212	203.5
-0.9	225	216.5	210.5	202.5
-0.8	222	212	206	196.5
-0.7	220	210	203.5	194.5
-0.6	214	205	200	192

Table 3.2. Measured activation energies and capture cross-sections of interface states in the InP band gap for a S passivated MIS capacitor.

V applied (Volts)	E_C-E_T (eV)	Activation Energy E_A (eV)	Capture Cross-section σ_o (cm^2)
-0.6	0.6145	0.4106	1.01×10^{-10}
-0.7	0.7185	0.3668	5.40×10^{-12}
-0.8	0.8225	0.3753	7.02×10^{-12}
-0.9	0.9005	0.4414	1.63×10^{-10}
-1.0	0.9655	0.4620	4.70×10^{-10}
-1.1	1.0498	0.3596	1.14×10^{-12}
-1.2	1.1059	0.3953	6.14×10^{-12}
-1.4	1.1501	0.4749	2.14×10^{-10}
-1.5	1.2125	0.4198	1.18×10^{-11}

As mentioned earlier the major drawback with the DLTS measurements on n-type MIS structures is lack of electrons at the interface in inversion restricts this method to states in the upper half of the band gap and charge storage at the interface affects the emission properties [104]. One way to eliminate both problems is to include an appropriate charge supplying or draining region in contact with the semiconductor and placed close to the MIS interface and biased appropriately [105]. This can be accomplished by using an implanted region in contact with the semiconductor. It needs to be emphasized that the results presented here are preliminary but quite interesting. We observe that the traps at the S passivated InP/nitride interface are electron traps with large capture cross-section (table 3.2) and two sets of traps appear to be present. We have done a preliminary characterization of the lower temperature traps and more work needs to be done to characterize the S passivated InP/nitride interface trap states in detail.

3.7 TEMPERATURE STABILITY OF THE PASSIVATED CAPACITORS

One of the most critical considerations of the passivation process is its temperature stability. This factor alone determines if S interface engineering is a viable technique for SAG FETs, since interface integrity should be maintained during the high temperature implant anneal. It is quite possible that the anneal creates a large number of interface states rendering the passivation process ineffective. We therefore study the electrical performance of passivated MIS capacitors that are subjected to a 700°C, 4 seconds SRLA anneal described in Chapter 3. The I-V and C-V results are shown in figures 3.9 & 3.10 . The curves

of figure 3.9 represent the characteristics of the MIS diodes CAP 1-4 of sample S2. In figure 3.10, S2 represents the C-V curves for diode CAP1. The C-V characteristics of the other diodes exhibit a similar behavior.

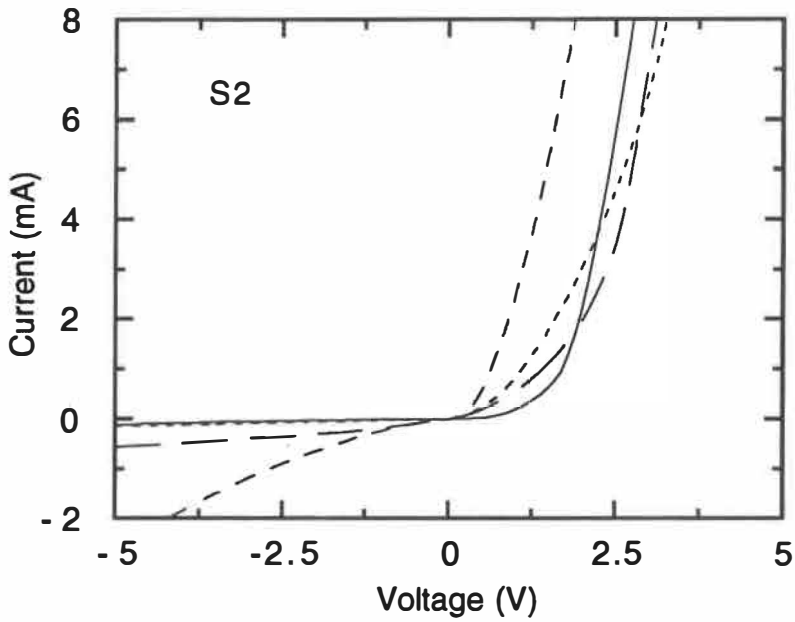


Figure 3.9. Leakage characteristics of S passivated MIS diode following a 700°C SRLA anneal. The profile is shown on figure 3.15.

Clearly the gate leakage is much larger compared to figure 3.2. This is due to S incorporation into the film from the interface. The leakage in accumulation is so large that the I-V is similar to a diode. Figure 3.10 compares the 100 KHz, C-V characteristics of the capacitor just before and after anneal. As explained earlier in this chapter the important aspects that need to be considered are the magnitude of change of the C-V characteristics and stretch-out. We find that difference between C_{min} and C_{max} is similar to that of the unannealed sample with minimal stretch-out and hysterisis.

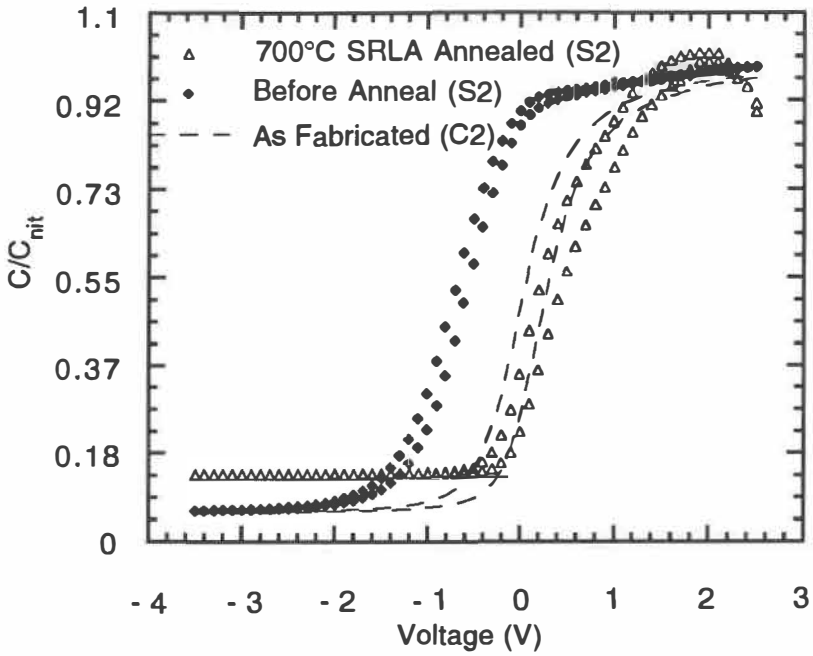


Figure 3.10 High frequency C-V characteristics of a passivated MIS diode subjected to a 700°C SRLA anneal. The C-V curves before anneal and of a sample (C2) immediately after fabrication are shown for comparison.

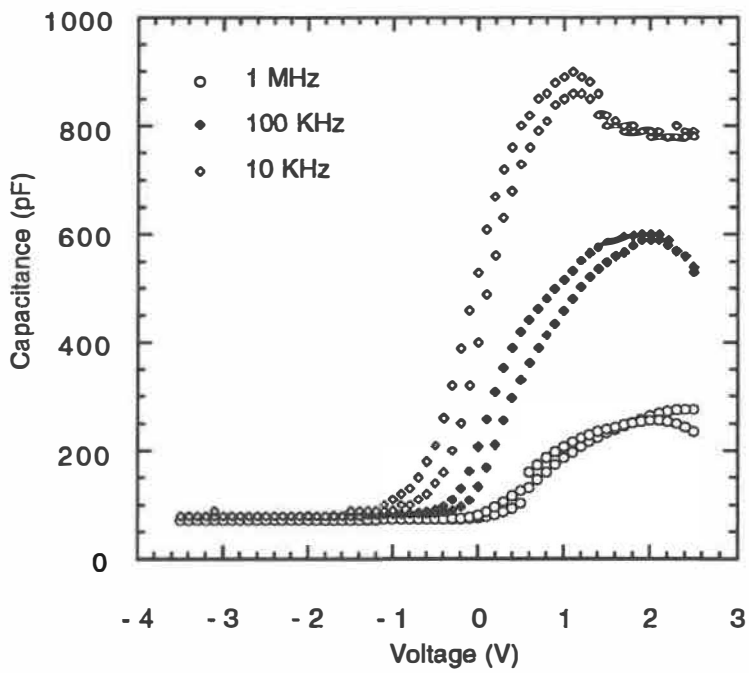


Figure 3.11. Frequency dispersion of passivated MIS diode (S2) after SRLA anneal.

The surface potential of the annealed sample therefore varies from accumulation to inversion. The anneal however results in a negative shift of the C-V curve along the x axis possibly due to creation of fixed charges at the interface or mobile charge in the nitride due to S incorporation. Such a shift would result in a negative threshold voltage and normally-ON FETs as seen in chapter 7. The curve for an as-fabricated sample (C2) is also compared to show that the shift is not large and is within the deviation normally observed in these experiments. The bottom line is the passivation process is still intact and SAGFETs are a definite possibility. The decrease in capacitance in accumulation is due to leakage through the nitride. We also observe a large dispersion of the C-V curves with frequency in the samples subjected to the SRLA anneal. This dispersion is shown in figure 3.11 and is also related to leakage through the nitride.

In conclusion, we show that S passivation of InP translates to low interface state densities with excellent, near ideal C-V characteristics. We have fabricated the first S passivated InP MIS devices, that use silicon nitride as the gate insulator, with midgap D_{it} values in the range of $8x10^{10}/cm^2$. As expected and mentioned in Chapter 2, the passivated interface is stable when capped by an insulating layer and subjected to an implant anneal cycle. We find that S incorporation in the dielectric under certain conditions poses a serious leakage problem through the nitride. In addition, the chemical nature of the passivation results in non-uniform I-V characteristics that needs to be remedied. However, the C-V curves exhibit minimal strechout and hysterisis. This again is the first report on the high temperature stability of the passivated interface. These

results bolster our original claim that interface engineering techniques should be used in the realization of SAGFETs.

CHAPTER 4
MASK SET DESIGN

4.1 INTRODUCTION

With the various process steps characterized and optimized, our next goal is to integrate them to realize self-aligned insulated gate MISFETs and a InGaAs/InP HIGFET. Integration involves the use of a suitable mask set for fabricating appropriate FET structures. Since material and process parameters strongly influence device performance, one usually adds specially designed test structures into the mask set, for the particular process sequence, that can aid in identifing the cause of any anomalous device behavior. These structures are an invaluable aid for device development and optimization, and are usually a part of any IC manufacturing process. Although some test structures are common for different technologies, it is important to stress that the nature of the test structure set should reflect the chosen technology and is unique for the particular process sequence. There are only a few reports in the literature that deal with a complete diagnostic chip for FET development on GaAs and to our knowledge none for passivated HIGFET and MISFET structures based on InP. Therefore a chip incorporating various test and FET structures is designed and used to evaluate the self-aligned gate technology. The chip contains some test structures suggested by the Rockwell group [106] and National Research Council (NRC) of Canada for GaAs FETs [107].

4.2 CRITERIA FOR DIAGNOSTIC CHIP DESIGN

The design methodology attempts to address the following issues

- Basic material properties

- Process parameters
- Device characteristics
- Basic circuit aspects

The material properties we are interested in are

1. Resistivity
2. Mobility
3. Carrier concentration / doping
4. Interface trap concentration and their properties
5. Conduction band discontinuity (ΔE_c) for heterostucture layers
6. Interface recombination velocity and carrier life time (τ)

The important process parameters are

1. Specific contact resistivity (ρ_c), transfer length (L_T) and the contact resistance (R_C) of the ohmic contacts
2. Sheet resistance (R_{SH}) of the implantation
3. Thickness of the nitride and its quality
4. Mesa depth and device isolation.
5. Sheet resistances and thickness of the gate and contact metallizations
6. Gate metal step coverage

The device characteristics include

1. C-V and I-V of MIS structures
2. Frequency dispersion of C-V characteristics
3. FET I_{DS} - V_{DS} characteristics and transconductance (G_m)
4. Threshold voltage (V_T)
5. Variation of channel mobility with gate voltage

6. Charge concentration (n_s) and resistivity variation in the channel region with gate voltage
7. Short channel effects
8. Source contact resistivity
9. Microwave performance
10. Drain current drift with time

and the basic circuit aspects cover

1. Inverter characteristics with different pull-up resistors, V_T and noise margin
2. Ring oscillators

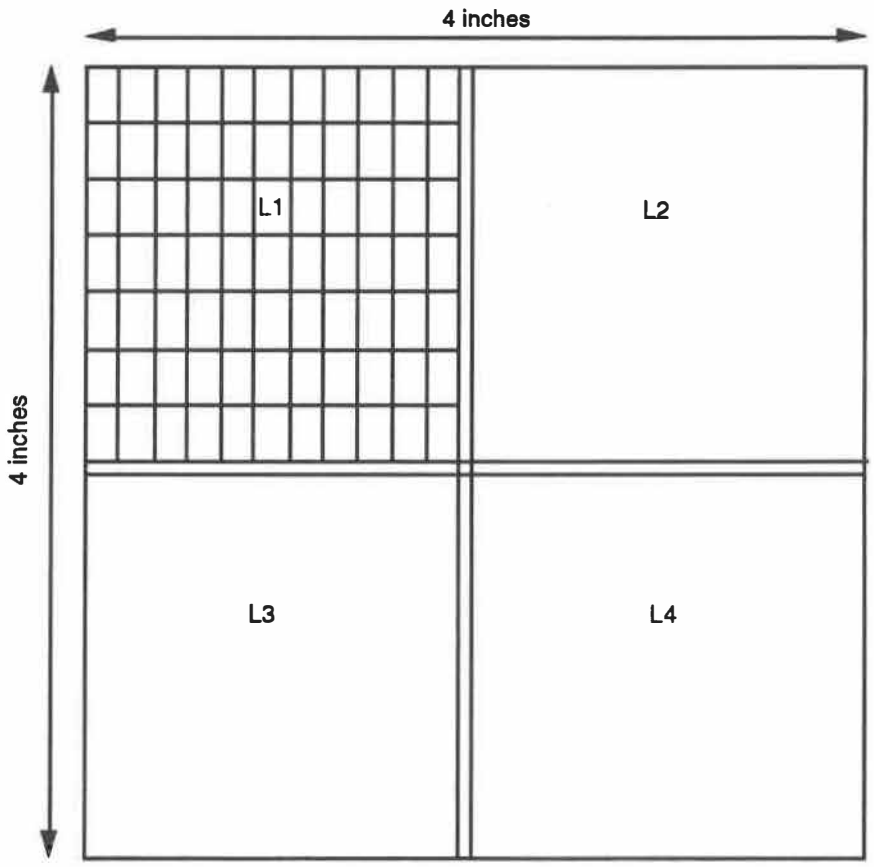


Figure 4.1. Layout of the 4 level mask.

4.3 DESIGN CONSIDERATIONS

The diagnostic chip, MODFAB HIFET1, addresses all the above mentioned issues. We use 5 mask levels to fabricate the chip. The e-beam direct write mask set ordered from Precision Photo Mask has a minimum feature size of 1μm. Each mask costs $1200 and is 4x4 inches in dimension and consists of 4 masking levels. A single mask level contains up to 110 individual chips of dimension 4.25 x 3.75 mm^2. Figure 4.1 shows the layout of one such mask. Since our maximum sample size is 1.5x1.5 cm^2, the masking levels are sufficiently large for fabrication and we are able to keep our costs to a minimum. The masking levels and their attributes are

L1.	Mesa isolation mask	- light field	-	Chemical etch
L2.	Gate mask	- dark field	-	Metal lift-off
L3.	Implant mask	- dark field	-	Selective Implantation
L4.	Contact mask	- dark field	-	Metal lift-off
L5.	Pad mask	- dark field	-	Metal lift-off

All the structures except the microwave FETs can be fabricated with just 4 masking levels. L5 provides an extra metal lift-off step for bonding purposes. Figure 4.2 shows the layout of the test chip and the design rules used in the layout are listed below

1.	Mesa to mesa separation	50 μm
2.	Implant to mesa separation	2 μm
3.	Gate to mesa overlap (Pad side)	20 μm
4.	Gate to mesa overlap (opposite side)	10 μm
5.	Contact to gate separation	2 μm
6.	Contact to implant separation	2 μm

7.	Pad metal to contact separation	5 μm
8.	Metal line to metal line separation	20 μm
9.	Pad sizes	200x200 μm^2
10.	Pad to pad separation	25 μm
11.	Pad to pad separation (microwave FETs)	50 μm

4.4 TEST STRUCTURES

We shall now examine the mask set in detail and dwell on the traits of each test structure and their utility. For the nomenclature, please refer to the mask layout entitled "The Test Chip" listed under other illustrations and provided at the end of this embodiment .

The alignment keys are placed at each corner of every individual chip. We have used both point and cross alignment structures in the mask set. The latter is more useful in performing fine alignments.

The Hall structures H1,H2 and H3 are used to measure mobility (μ), resistivity (ρ) and carrier concentration (n). H1 is used to measure these values for the substrate, H2 for the implanted regions and H3 with a gate can be used to study the variation of n and μ for different gate voltages.

The National Bureau of Standards, NBS structure is used to accurately measure implant sheet resistance and the lateral spread of the dopant profile after implant activation [108].

The step coverage structure SC1 is used to evaluate the mesa step coverage of metal gates. The mesa sidewall roughness, in different [011] directions, is taken into account by running 1 and 5 μm lines over both sidewalls. The gate metal lines are also run over multiple mesas spaced close

to each other. The set of six mesas at the center of the chip are used to measure the mesa depth in both the $[0\ 1\ \bar{1}]$ and $[0\ 1\ 1]$ crystallographic directions.

The Transmission Line Measurement (TLM) arrangement is used to measure the specific contact resistivity (ρ_c), the transfer length (L_T) and the total contact resistance (R_C) of the Au-Ge/10% Ni ohmic contacts and the sheet resistance (R_{SH}) of the implanted regions.

The long metal lines GATE RES and CONTACT RES determine the sheet resistance, thickness and resistivity of the gate and contact metallization.

FATFET is a FET with a gate length of 50 μm and width of 200 μm and measures the drift mobility of the active channel layer using the technique described in [109] and the drain current drift with time due to slow traps at the insulator semiconductor interface.

The devices under the name FETs consist of 22 FETs with different L/W ratios. The gate lengths are 1,2,3,5,10 & 20 μm and the widths are 100, 150 and 200 μm. The FET design takes the mesa sidewall roughness into account and studies the DC performance with the channel oriented in both directions. These devices allow experimental determination of important device parameters such as threshold voltage (V_{th}), transconductance (G_m), etc. More importantly, they provide an estimate of the statistical deviation of these parameters and address uniformity and reproducibility. These structures can also be used to measure the source contact resistance [90,110].

The MSTRUCTURES are FETs specially designed for microwave evaluation. The pad spacing allows the direct probing of these structures by cascade type probes.

CAP is a MIS capacitor with an implanted doped region placed in contact with the interface. The structure can be used to evaluate the quality of the nitride, quasi-static C-V and I-V characteristics, frequency dispersion of C-V characteristics, carrier lifetime from conductance measurements, distribution of interface traps in the band gap, their concentration, activation energies and capture cross-section and the surface recombination velocity. The presence of the doped region that acts as a supply of majority carriers allows interface states in both the lower and upper half of the band gap to be probed by DLTS. By avoiding the nitride deposition and implantation steps, this structure can also be used to fabricate an n-N heterojunction diode and determine the magnitude of the conduction band discontinuity from C-V measurements [111].

The last structure termed INV consist of 4 FETs of width 50 μm and lengths 1,2,3 and 5 μm. The source of the 1 and 5 μm FETs are connected to an implanted region that acts as a pull-up resistor. The implanted region has three taps that allows the value of the pull-up resistor to be varied. The FET in conjunction with the pull-up resistor acts as an inverter. By connecting three such inverters in sequence one can realize a ring oscillator.

In conclusion, we have designed and fabricated a complete test mask set, the first of its kind, for SAGFETs .This work now puts us within one step of fabricating interface engineered insulated SAG devices and evaluating its process compatibility.

CHAPTER 5
DEVICE FABRICATION

5.1 INTRODUCTION

Our goal is to demonstrate that interface engineering is essential to realize SAGFETs on InP. We now have all the necessary technological ingredients for this purpose - the characterized interface engineering step, the fine tuned complete process technology and a complete set of masks - and proceed to fabricate the self-aligned FET structures. The flow chart of figure 5.1 details the process sequence. A schematic view of the process for the HIGFETs is shown in figure 5.2. The process sequence is the same for MISFETs except the mesa isolation step is not required. Apart from the interface engineered devices, unpassivated FETs are also fabricated for comparison purposes. We go through the fabrication process in a step by step fashion, problem areas are pointed out and discussed.

5.2 SAMPLES

Fe doped SI and Zn doped p^- InP substrates are used for fabricating enhancement and inversion type MISFETs respectively and the HIGFETs are conceived on the 450ÅInP/970Å$In_{0.53}Ga_{0.47}As$/1500ÅInP/semi-insulating InP heterostructure sample.

5.3 CHEMICAL CLEANING

Fabrication begins with a chemical cleaning cycle that removes any surface organic and metallic contaminants. The cleaning procedure is described

in chapter 2. For the heterostructure samples the iodic acid etch is limited to 10 seconds since the cap InP layer is only 450Å thick.

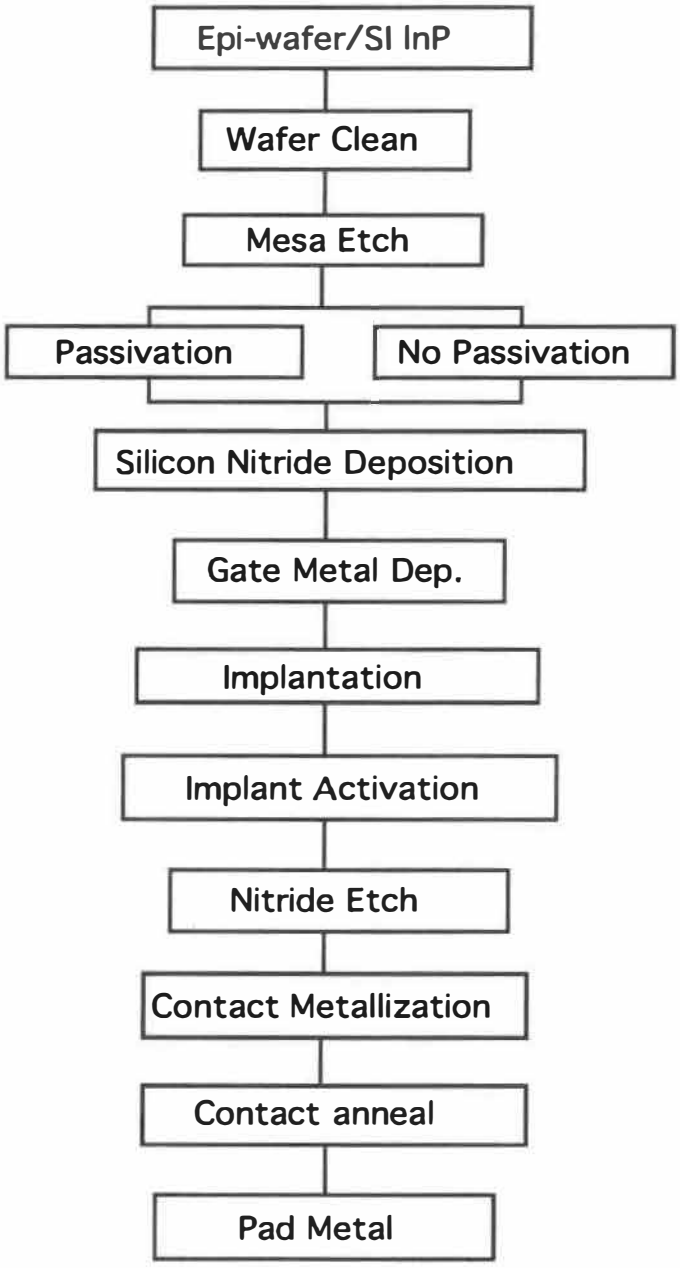
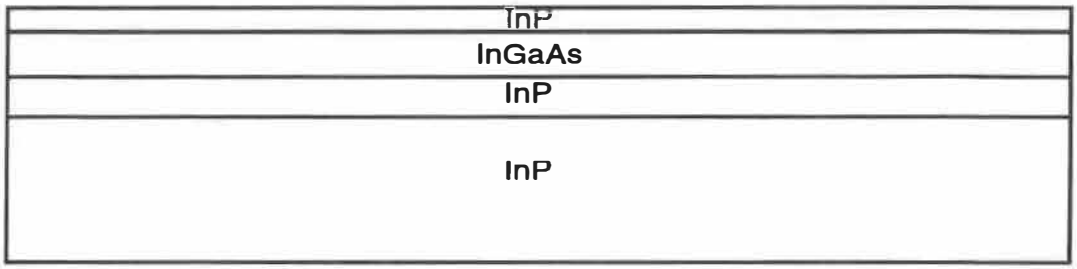
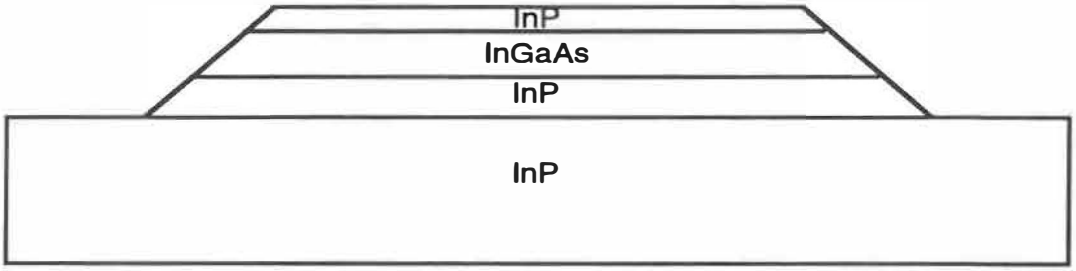


Figure 5.1. Flow chart of the device fabrication sequence for SAGFETs.

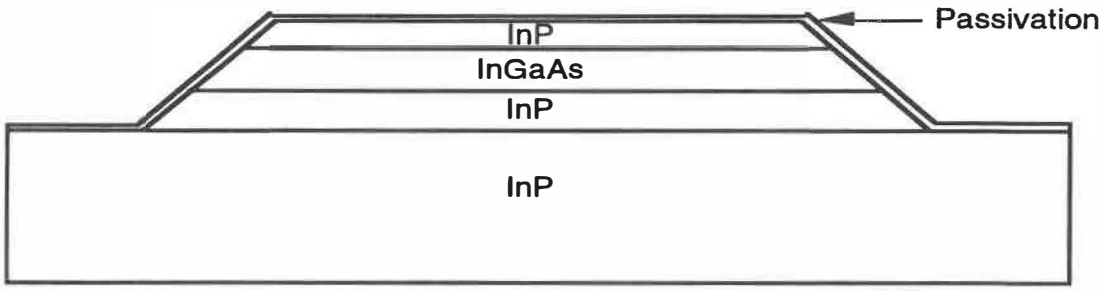


- Wafer Clean

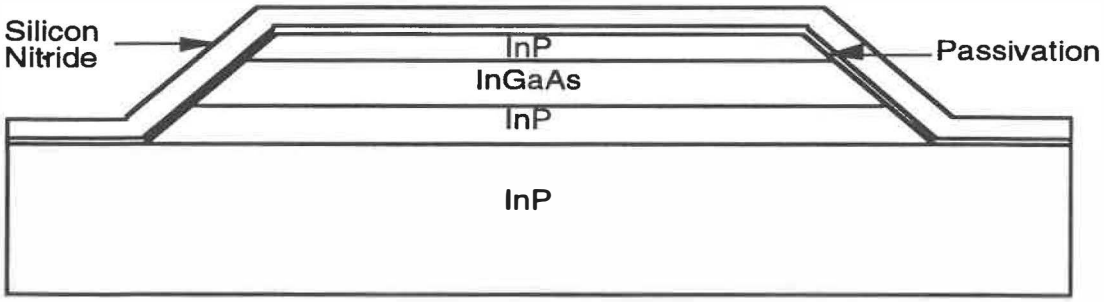


- Mesa device Isolation etch

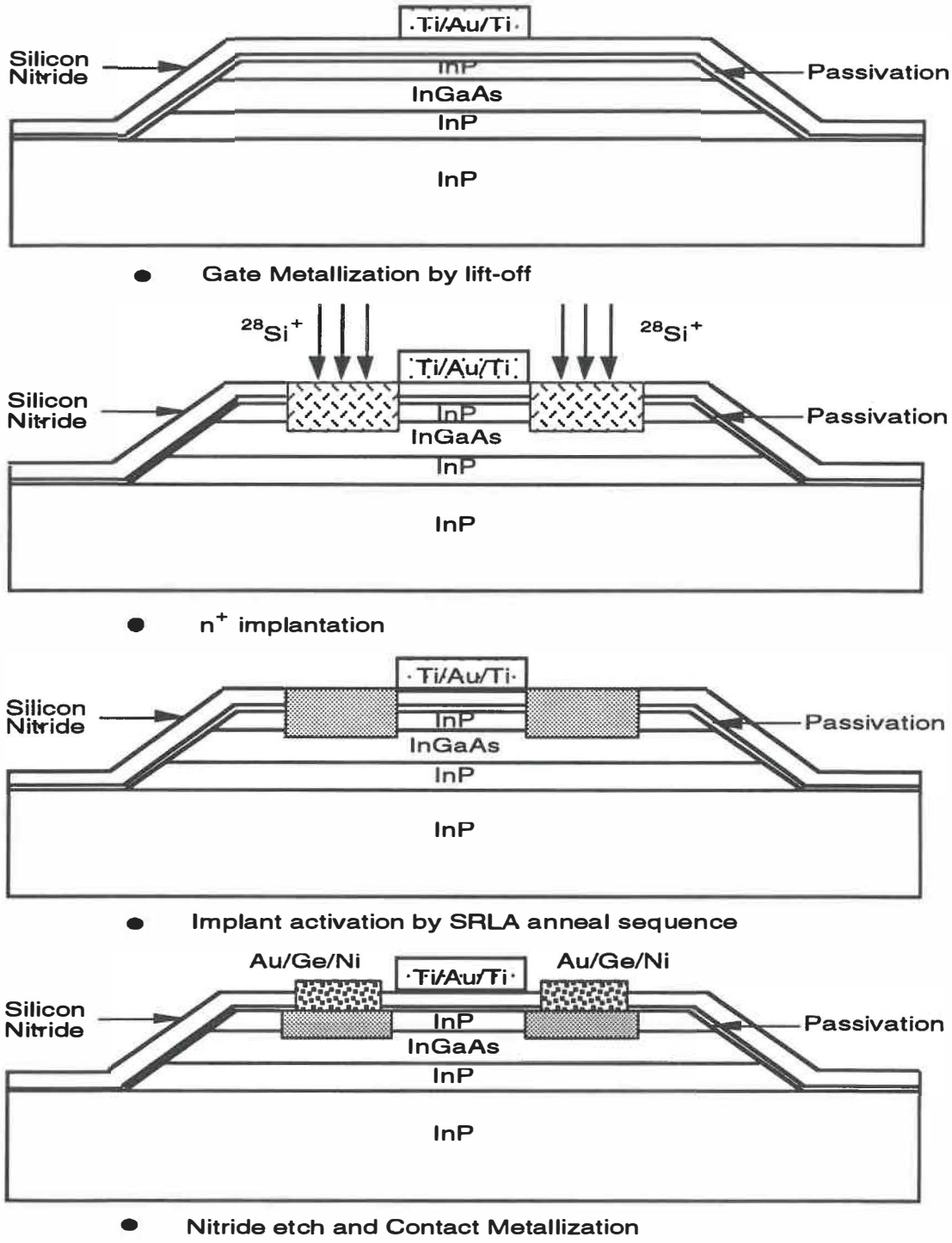
Note: Isolation etch not performed for MISFETs



- S passivation



- Indirect plasma nitride deposition



Note: MISFETs are fabricated on InP substrates without epi-layers

Figure 5.2. Schematic view of the wafer cross-section during different stages of processing.

5.4 DEVICE ISOLATION

It is essential to isolate the individual devices and their active regions from one another. Isolation is not a problem for MISFETs as the high resistivity SI substrate and the p^--n^+ junction formed on p substrates naturally isolate devices. For the heterostructure samples it is essential to define the active regions as there is a possibility of lateral current spreading in the low doped channel region. The popular method to isolate III-V heterojunction devices is by using a mesa [112]. The technique consists of etching away the material from the intermediate regions while protecting the active regions by a photoresist mask. The sample after etch therefore consists of a number of mesa type structures that define the active regions with air as the intermediate dielectric. The technique is quite simple and easy to realize. The disadvantage is that we lose planarity and the metal gates must now run over the mesa without breaking. This imposes the restriction that the mesa must have low equi-angle side walls that are not rough. Therefore the etch has to be anisotropic and reveal the higher order crystallographic planes. Wet chemical etchants meet this requirement but these etchants are highly material sensitive and they normally expose different crystallographic planes in the $[0\ 1\ \bar{1}]$ and $[0\ 1\ 1]$ directions. In addition, the etch rate may not be the same for the InGaAs and InP layers and could produce notches or ridges at the sidewalls. Choice of the etchant therefore becomes highly critical. The 10% iodic acid etchant used in this study produces 35° angle slopes in both directions without any abnormal sidewall features. The sidewall roughness in the $[0\ 1\ 1]$ direction did not affect the gate metal step coverage. The important consideration is that the etch must completely remove the epitaxial

layers and expose the SI substrate. In our case this translates to a mesa depth of atleast 5000Å.

Lithography is done using the mask level L1. The conditions for lithography are listed below.

Photoresist	1400-17 (Positive)
Coat	3000 rpm, 30 seconds
Prebake	90°C, 30 minutes
Exposure	7 seconds
Developer	154 (undiluted)
Develop	20 seconds
Postbake	120°C, 30 minutes
Etch	12 minutes in 10% HIO_3

The etch results in a 5500Å deep mesa which conforms to the specifications and provides adequate isolation.

Isolation can also be performed by a high dose proton implantation to maintain sample planarity.

5.5 PASSIVATION

S passivation of the samples is done by immersing them in the $(NH_4)_2S$ solution at 60-70°C for half hour under illumination. Prior to passivation the samples are given a 10 second dip in a 1HF:1HCl:4H_2O solution to remove any surface native oxide.

5.6 GATE DIELECTRIC DEPOSITION

Following sulfurisation the samples are immediately loaded into the indirect plasma PECVD deposition chamber. The unit is pumped to a base vacuum of $\approx$ 3-4 x 10^{-6} torr and the silicon nitride is deposited at 270°C for 1 hour at 15 Watt input power. All other procedures and parameters are as described in chapter 2. The nitride thickness varies from 600-700Å on the bulk InP samples and is around 550Å for the heterojunction sample. Visual observation under a microscope shows no sign of S out-diffusion from the sample interface.

5.7 GATE METAL LIFT-OFF

Complying with the process sequence, the Ti/Au/Ti gates are formed next by the lift-off technique [113]. The photoresist is patterned to expose the gate regions with an overhang near the edges. The overhang is created by treating the photoresist surface with chlorobenzene which forms a surface layer that dissolves slowly in the developer. The untreated underlying resist dissolves faster than this surface layer resulting in the overhang. The metal is e-beam deposited on the sample through these windows. Metal deposition does not occur under the overhang as these regions are shielded from the line of sight of the evaporating atoms by the photoresist overhang. After deposition the sample is immersed in a solvent such as acetone. With a proper overhang, the solvent lifts-off the double layer of resist and metal by dissolving the underlying untreated resist and leaves the required gate metal geometry on the sample.

The important considerations are the duration of the chlorobenzene treatment that forms the surface layer, the development time that creates the overhang and determines the line width and lastly the deposited metal thickness.

Prolonged treatment in chlorobenzene causes the PR surface to become spotty. Under-treatment ,naturally, does not result in a sufficiently thick and hard surface layer. Over development will cause the overhang to collapse while insufficient development time will not form a good resist overhang. Similarly, from our experiments we find that the total thickness of the gate metal layer can be at most one-third the resist thickness to get a good lift-off. We have optimized these conditions and the optimum parameters are listed below.

Photoresist	1400-17 (Positive)
Coat	3000 rpm, 30 seconds
Prebake	95°C, 30 minutes
Chlorobenzene	3 minutes
Exposure	7 seconds
Developer	354 (undiluted)
Develop	45 seconds

Table 5.1 Parameters used for electron beam metal evaporation.

Element	Voltage (kV)	Current (mA)	Rate (Å/sec.)
Ti	5.0	150	20
Au	4.4	60	10
Au/Ge/10%Ni	4.2	50	10

Since the resist thickness is about 5500Å, the maximum gate metal thickness that can be reliably lifted-off is around 1800Å. For our process, we deposited a 200Å Ti/ 1200Å Au/ 100Å Ti gate layer for a total thickness of 1500Å.

The base vacuum before deposition is about 1.5×10^{-6} torr and the deposition rate varied with the particular metal. The details are given in table 5.1. The lift-off is performed by dipping the samples in hot acetone for about 15 minutes. Using the procedure described above, we are able to easily delineate the fine 1μm geometry gate structures.

5.8 POST METALLIZATION ANNEAL

A post metallization RTA anneal of the samples is performed at 350°C for 10 minutes in forming gas to H passivate the interface. We observed on some samples out-diffusion of the excess sulfur from the interface through the silicon nitride. The sulfur out-diffusion is stopped by the gate metal resulting in the formation of bubbles at the center and sulfur rings near the edge of the gates.

5.9 IMPLANTATION

Selective implantation is performed following lithography to form the source and drain regions. The L3 mask is used for this purpose. The conditions for lithography are similar to the mesa etch except that the post-bake step is left out. The samples are transported to the implant site and a Varian DF300 medium current implanter is used to implant 100 keV, $^{28}Si^{+}$ ions at a dose of 1×10^{14} ions/cm^2. The implantation is done at room temperature (RT) with the samples oriented 7° off the [100] direction [84]. The implant hardened photoresist is removed using the commercially available photoresist stripper Shipley 1165 maintained at 80°C. Usually a double bath approach is followed and the samples are immersed in two baths sequentially. The remover slowly etches the silicon

nitride and the strip time should be less than 15 minutes. In our case the total time is about 5 minutes.

Observation under a microscope shows that the implanted regions appear to be amorphised by the implantation as seen from figure 5.3.

5.10 IMPLANT ACTIVATION

The initial attempts to activate the implantation using conventional rapid thermal treatments (RTA) are not successful due to the presence of the metal gates. The metal gates and the nitride peeled-off completely when the wafers are subjected to a 800°C RTA anneal and the samples are destroyed. We therefore adopted the SRLA strategy described in chapter 2 that maintains gate metal integrity while resulting in acceptable activation. Figure 5.4 shows a sample following a SRLA implant activation at 700°C as described in chapter 2. As seen clearly these results are quite acceptable. The anneal also repairs nitride damage. However, the high temperature step results in considerable S out-diffusion on all samples as seen in figure 5.5. As seen later in chapter 6, the out-diffusion lowers the breakdown voltage of the nitride layer and affects transistor characteristics.

The integrity of the gate metallization during the high temperature activation can be preserved by using materials such as W or WSi_x with better high temperature stability [16]. S out-diffusion can be minimized by resorting to milder passivation of the InP surface. Using a thin GaP layer, as mentioned in chapter 1 instead of S can also prevent insulator degradation.

5.11 CONTACT METALLIZATION

Au/Ge+10%Ni metallization is formed by lift-off using mask L4. The conditions for lithography is similar to the gate metallization. The silicon nitride is etched-off by dipping in 10% HF for 15 seconds and about 1000Å of the contact metal alloy is e-beam evaporated. The conditions for e-beam evaporation are listed in table 5.1 . The contacts are then defined by lift-off and annealed at 400°C for 10 seconds in a forming gas atmosphere. The final device with the gate and source/drain contact metallization is shown in figure 5.6 and the SEM photograph of figure 5.7. The bonding pad mask L5 is not used in the fabrication as the devices are directly probed for DC characterization.

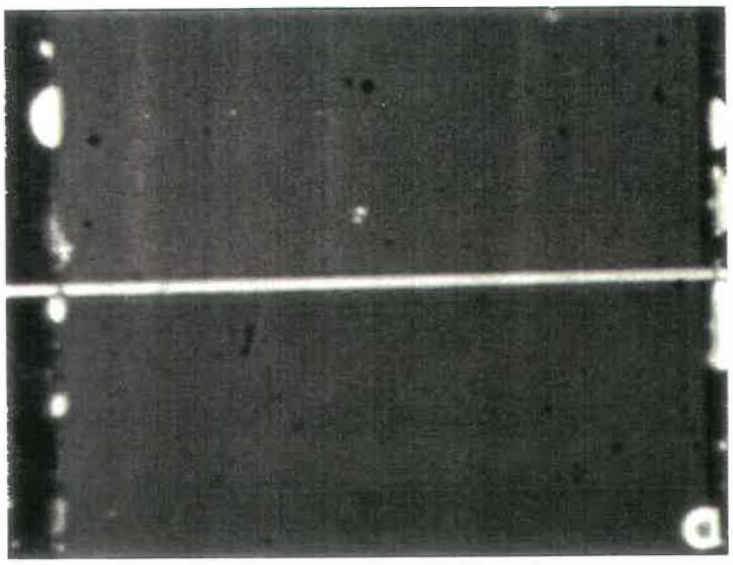


Figure 5.3. Photomicrograph of the amorphised silicon nitride regions and the gate metal following implantation. The gate stops the ions from reaching the channel region.

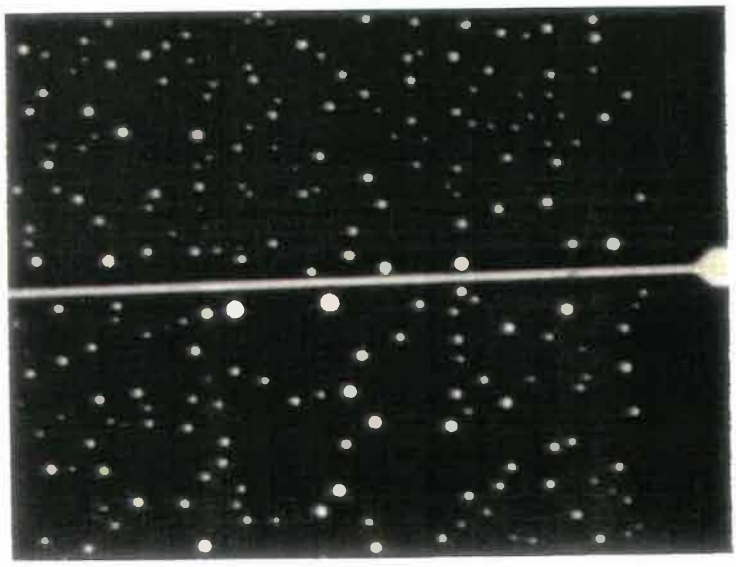


Figure 5.4. A 1μm gate and the implanted silicon nitride regions following activation a 700°C SRLA anneal. Note that the anneal repairs the damage to the nitride cap and preserves excellent gate integrity.

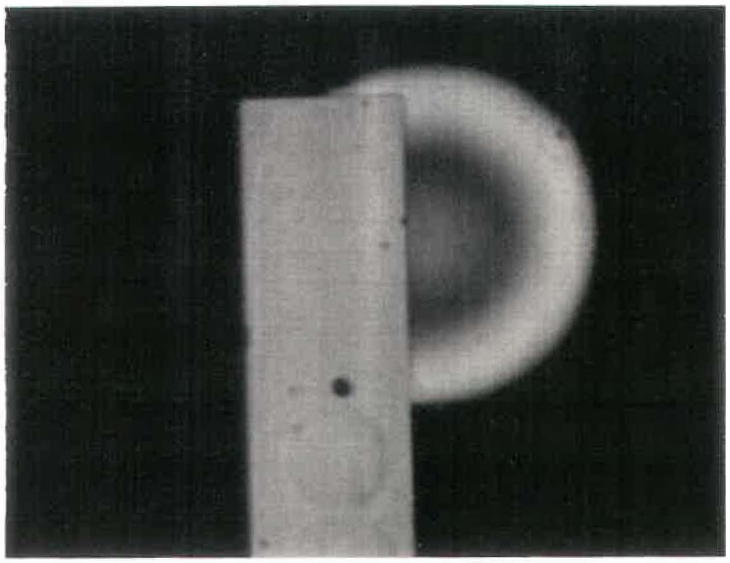


Figure 5.5. Photomicrograph of the S out-diffusion near the edge of a 3 μm gate on a post implant annealed sample.

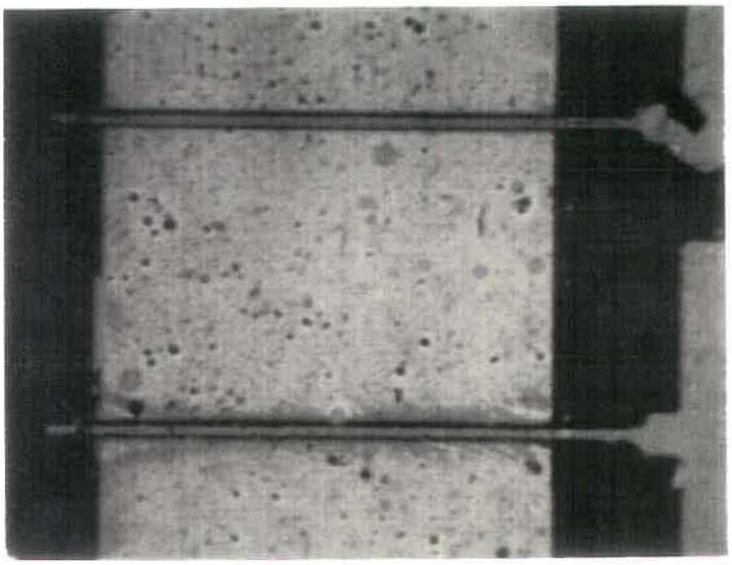


Figure 5.6. Photomicrograph of the completed HIGFET showing the gate and source/drain metallizations. The gate runs over the faint mesa edge. A part of the probe pads are also seen.

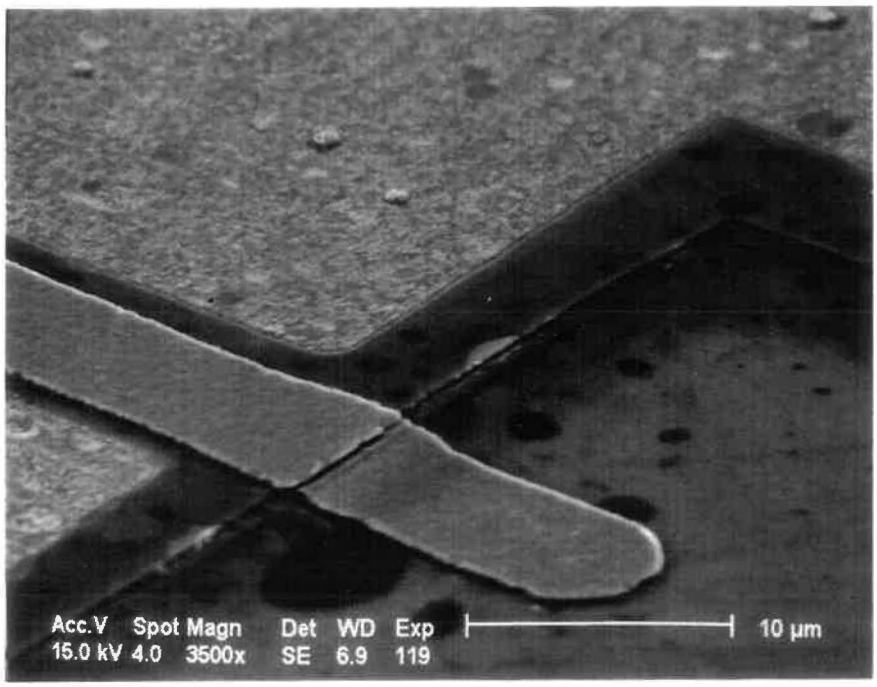


Figure 5.7. SEM photograph of the completed HIGFET showing the gate, source/drain and contact metallizations.

This completes the device fabrication of the SAGFETs. Compatibility of implant activation with S passivation is a crucial consideration during fabrication. These individual steps should be tailored to prevent S out-diffusion from the interface. In spite of the S out-diffusion problem it is shown that by incorporating the interface engineering technique we are able to fabricate SAGFETs exhibiting acceptable transistor action with modest performance. The DC electrical characteristics of the interface engineered SAGFETs are considered in the next chapter.

CHAPTER 6

DC ELECTRICAL PERFORMANCE

6.1 INTRODUCTION

The ultimate test of any new technology is the electrical performance of the final devices. Electrical characteristics can easily expose weak links in a new process and more importantly would help make any major changes in direction and finally assess if the approach is worth pursuing at all. In addition, as discussed in Chapter 5, electrical measurements provide a valuable estimate of the various important device and process parameters such as transconductance (g_m), output conductance (g_o), threshold voltage (V_T), channel mobility (μ_{ch}), cut-off frequencies (f_t), contact resistivity (ρ_c) and sheet resistance (R_{SH}) of the implanted regions. We shall dwell on these issues and try to deduce conclusions and directives for further effort in this direction.

6.2 PERFORMANCE OF MISFETS

6.2.1 ACCUMULATION TYPE MISFETS

6.2.1.1 CURRENT - VOLTAGE CHARACTERISTICS

Electrical evaluation of the fabricated devices is carried out by direct probing using a Wentworth prober. The current-voltage curves of the FETs are measured with a HP4145A parametric analyzer. The typical drain current-voltage curves (I_{DS} Vs V_{DS}) of an accumulation type passivated self-aligned MISFET is shown in figure 6.1. The nominal gate length is 5 μm and the width 200 μm. The as-fabricated device exhibits well-defined linear and saturation regions at low and high V_{DS} respectively unlike the self-aligned FETs reported by K.Oigawa et al. [25] that are highly non-linear. We believe that this result will encourage the

realization of a more mature interface engineering self-aligned gate FET technology on InP. Maximum transconductance (g_m) values about 3 mS/mm at a gate voltage of 0.7 volts are measured for the as-fabricated device.

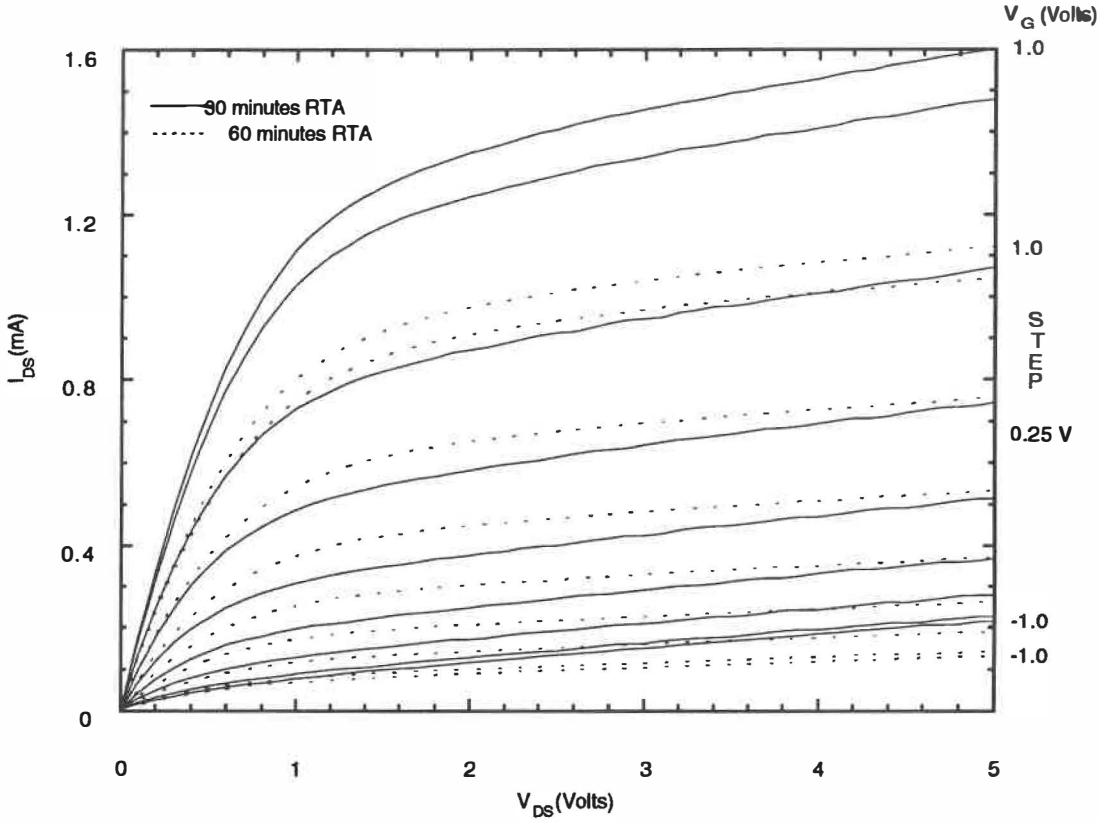


Figure 6.1. Drain I-V characteristics of a 5x200 μm^2 accumulation MISFET after annealing.

6.2.1.2 GATE LEAKAGE

It is observed from both I_{DS} Vs V_{DS} and I_{DS} Vs V_{GS}measurements that the drain current does not vary when the gate voltage exceeds ± 0.75 - 1.0 volts. This is due to leakage through the gate dielectric as seen in figure 6.2. Diffusion of sulfur into the nitride during the high temperature implant annealing step degrades the breakdown voltage of the insulator from about 10-11 volts to about 0.7 volts that corresponds to a breakdown field of 1.2×10^5 V/cm and results in

excessive gate current above this value and the gate loses control above this voltage value. As a result, the devices are normally-ON and cannot be turned-OFF.

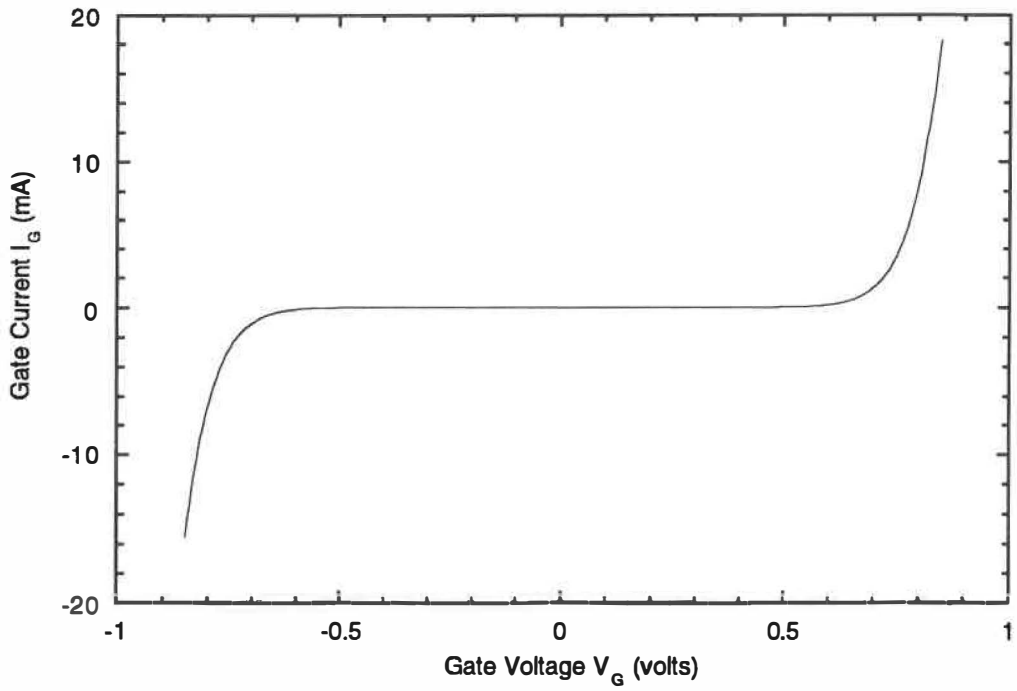


Figure 6.2. Gate leakage characteristics of the MISFETs.

The sulfur diffusion problem, discussed earlier in Chapters 3&5, mainly arises due to the strong passivation process employed in the FET fabrication. Strong passivation usually refers to a passivation cycle that leaves a clearly visible layer of sulfur on the sample surface. As observed in chapter 1, this sort of passivation results in excess unbonded elemental S on the sample surface even after annealing at 300°C for 30 minutes. We believe that this excess sulfur at the interface diffuses into the nitride during implant activation. The sulfur out-diffusion from the interface can be easily minimized by performing a mild passivation and washing off any excess sulfur. Another approach would be to duplicate the function of the cap In_2S_3 layer by growing a thin strained layer (≈ 20-30Å) of GaP

on top of InP. Over layers containing phosphorus have been successfully used as passivating layers and have shown excellent thermal stability. The logical extension to this line of thought is to use a high bandgap epitaxially grown phosphorus compound with good high temperature stability. GaP is a large band material with a gap of 2.1eV and has better high temperature stability than InP and can be grown epitaxially with good uniformity. This layer is expected to be more resilient to surface degradation during the insulator deposition process and any high temperature process steps and can serve as a cap layer to prevent P vacancies in the underlying InP substrate. The reader is reminded that cap layers prevent P out-diffusion from the InP substrate.

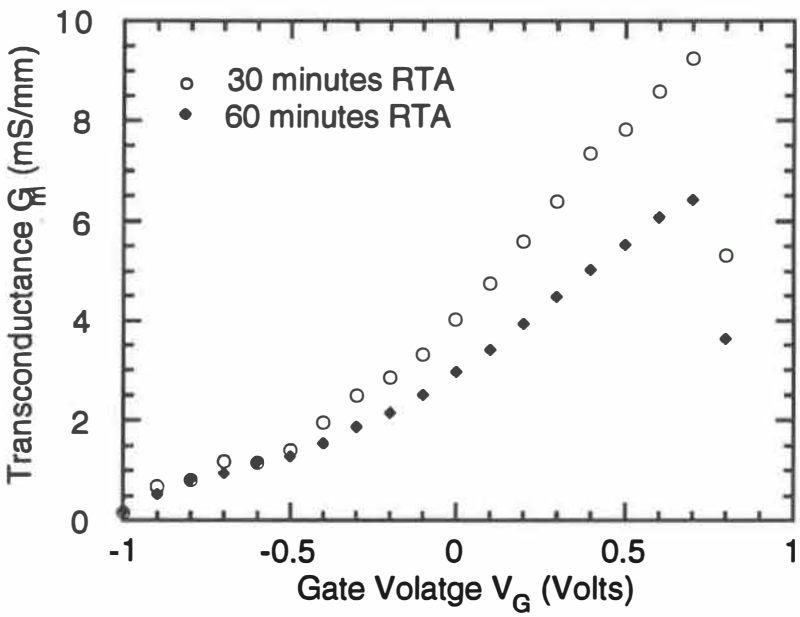


Figure 6.3. Effect of annealing on MISFET transconductance.

6.2.1.3 EFFECT OF ANNEALING

It has been shown in [23] and [33] that the performance of FETs using a P_2O_5 interface improves considerably by thermal annealing at 400°C, mainly due

to changes at the interface. We subjected our devices to thermal anneals at 400°C for times up to 1 hour in steps of 30 minutes. By annealing for 30 minutes we are able to increase the maximum transconductance of these devices to 10-12 mS/mm (V_G = 0.7V). Figures 6.1 & 6.3 show the drain I-V characteristics and the variation of G_m with gate voltage (V_G) for the 30 minutes annealed sample. The 400°C anneal does not change the gate leakage characteristics, as expected, since low temperatures should have little effect on the sulfur diffusion mechanism. The g_m values are comparable to those of the non-self-aligned S passivated FETs [6]. As seen from figures 6.1 & 6.3, further annealing degrades the current drive and the transconductance.

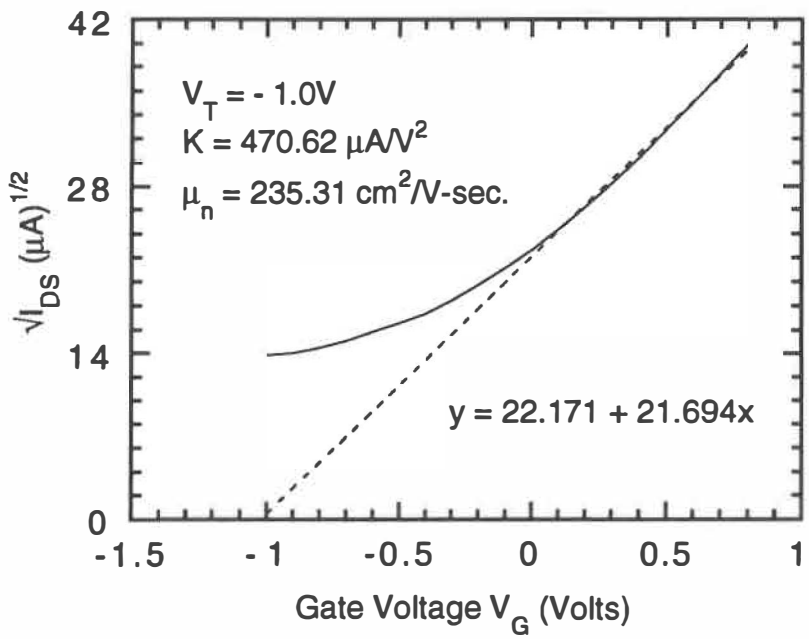


Figure 6.4. The $\sqrt{I_{DS}}$ Vs V_G plot to estimate channel mobility and threshold voltage.

6.2.1.4 CHANNEL MOBILITY

The equation of $\sqrt{I_{DS}}$ Vs V_G for a MISFET in the saturation regime represents a straight line and can be written as [114]

$$\sqrt{I_{DS(sat)}} = \sqrt{\frac{Z}{2L}\mu_n C_{nit}}\,(V_G - V_T) \qquad (6.1)$$

By extrapolating the straight line to the x-axis (i.e.. zero drain current) we can determine the threshold voltage V_T of the transistor. Figure 6.4 shows the plot of $\sqrt{I_{DS}}$ Vs V_G for the transistor of figure 6.1 that is annealed for 30 minutes. The inferred V_T for this transistor is -1.0 volts. The slope gives the K value defined as [15]

$$K = \frac{Z}{2L}\mu_n C_{nit} \qquad (6.2)$$

The K value for this transistor is 470.62 $\mu A/V^2$. Knowing C_{nit} the capacitance per unit area of the insulator, L the channel length and W the channel width, we can estimate the channel mobility (μ_n) of the electrons. For a C_{nit} value of 10^{-7}F/cm^2, μ_n is 235 cm^2/V-sec. The low mobility value is attributed to the rough nature of the interface. It is normally believed that S passivation increases the interface roughness in MISFETs. The passivation techniques described earlier in this chapter are expected to result in smoother interfaces. The mobility value calculated from the peak transconductance value of 12 mS/mm is 352 cm^2/V-sec.

6.2.1.5 UNIFORMITY

Apart from g_m, we also monitored the impact of the anneal on important process parameters that are thermal history sensitive, namely contact resistivity (ρ_c) and the implant sheet resistance (R_{SH}). The TLM structure of the test chip is used for this purpose. Table 6.1 lists the g_m ,R_{SH} and ρ_c values of the MISFETs, as-fabricated and after thermal treatments. The main issue of concern is that the passivation process is quite non-uniform and we observe variations in device performance from die to die.

Table 6.1 Transconductance (G_m), sheet resistance (R_{sh}) of implanted regions and contact resistivity (ρ_c) values of enhancement and inversion type, as-fabricated and thermally annealed, FETs monitored on sample dies.

	As Fabricated			400°C Anneal 30 min.			400°C Anneal 60 min.		
	G_m mS/mm	R_{sh} kΩ/sq	ρ_c mΩ.cm^2	G_m mS/mm	R_{sh} kΩ/sq	ρ_c mΩ.cm^2	G_m mS/mm	R_{sh} kΩ/sq	ρ_c mΩ.cm^2
Enhancement FETs	2-3	4.0	0.150 (L)	10-12	2.1	0.08 (L)	5-6	3.0	0.015
Inversion FETs	1-2	5.0	1.0 (L)	0.6	18	72 (NL)	_	_	_

L : TLM exhibits linear I-V characteristics.
NL: TLM exhibits non-linear I-V characteristics.

The measured standard deviation of I_{DS}(sat) at V_{GS} =1V over 12 devices is 0.487mA and provides an estimate of this non-uniformity. The non-uniformity has a strong impact on the contact resistivity of the samples and shows up as a variation from 15 $\mu\Omega$-cm^2 when sulfurization is mild to 1.0 mΩ-cm^2 in regions that are strongly sulfurized. This problem can in principle be solved by etching the surface passivation layer and a few Angstroms of the InP surface before metal deposition for contacts. The favorable aspect is that inherently more uniform passivation techniques are already available.

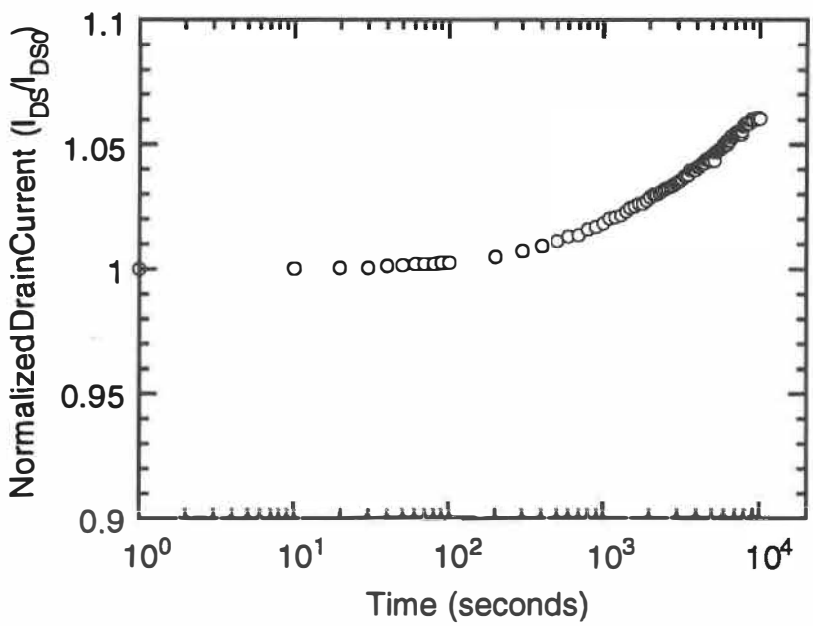


Figure 6.5. Drain current drift of the accumulation type MISFET annealed at 400°C for 30 minutes.

6.2.1.6 DRAIN CURRENT DRIFT

As observed previously in the introduction, P vacancies lead to the formation of slow traps at the interface that cause the drain current to drift with time, sometimes as high as 30-80% to its original value [9]. The drift usually shows up as a decrease in current and is indicative of the presence of slow traps

at the interface. Figure 6.5. shows the drain current of the accumulation type MISFET annealed at 400°C for 30 minutes. The current drift is measured over a period of 10^4 seconds at a gate bias, V_{GS} , of 0V. The significant details are, the drift is small (≈ 6%) and is upward compared to the usual downward drift that is normally observed in InP MISFETs. The downward drift is believed to be due to interface traps related to P vacancies [11]. The upward drift is an encouraging result as it indicates the absence of P vacancy traps at the interface of the SAGFETs. There is no obvious explanation for the upward drift and this phenomenon needs to be studied in detail. The drain current drift is comparable to that reported for non-self-aligned FETs [6].

6.2.2 INVERSION TYPE MISFETS

The I_{DS} Vs V_{DS} curves of the inversion type MISFETs fabricated on p substrates are shown in figure 6.6. The device shows excellent linear and saturation regions. The I_{DS} Vs V_{GS} and $\sqrt{I_{DS}}$ Vs V_{GS} plots are shown in figures 6.7 and 6.8. The latter provides a V_T of -0.65V and the former indicates that gate leakage sets in before strong inversion is achieved [114]. The as-fabricated FETs show slightly lower g_m values of 1-2 mS/mm with sheet resistances of 4-7 KΩ/sq. and contact resistivity of 1 mΩ-cm^2. Annealing decreases g_m to about 0.6 mS/mm with associated increases in R_{SH} and ρ_c values (table 6.1). In general, the inversion type MISFETs show better saturation characteristics than accumulation type devices and lower output conductances ,g_o, as discussed below.

6.2.2.1 FIGURE OF MERIT

A common figure of merit to assess transistor performance is the ratio of g_m/g_o, that is also equal to the equivalent circuit voltage gain for large loads. Here g_o represents the output conductance and is defined as [115]

$$g_o = \left.\frac{\partial I_D}{\partial V_D}\right|_{V_{GS}} \tag{6.3}$$

in the saturation regime. g_o manifests as a finite slope in the drain current-voltage characteristics, for an ideal transistor g_o is zero. It is important that g_o be low for large gain and high linearity. The measured g_o value for the accumulation type MISFET (30 minutes RTA) of figure 6.1 is 0.381 mS/mm and the ratio of g_m/g_o is approximately 25. Since the inversion type MISFETs show near ideal saturation characteristics, we measure smaller g_o values of 0.0515 mS/mm and the value of g_m/g_o is about 35. The figure of merits, g_m/g_o, of these devices are larger than the reported value (g_m/g_o = 14) for unpassivated InP/InGaAs HIGFETs (g_o =18 mS/mm) [116].

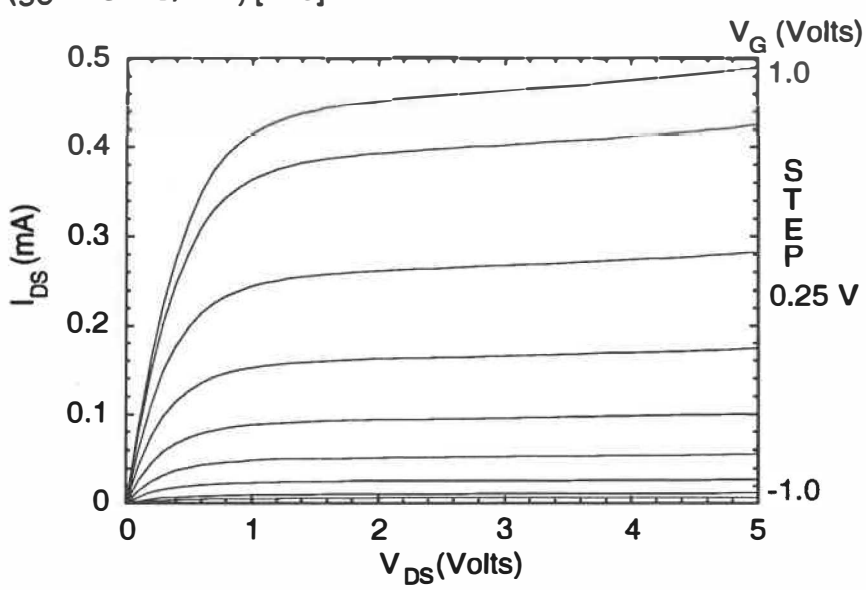


Figure 6.6. Drain current-voltage curves of an as-fabricated 3x200 μm^2 inversion type MISFET showing excellent linear and saturation regions.

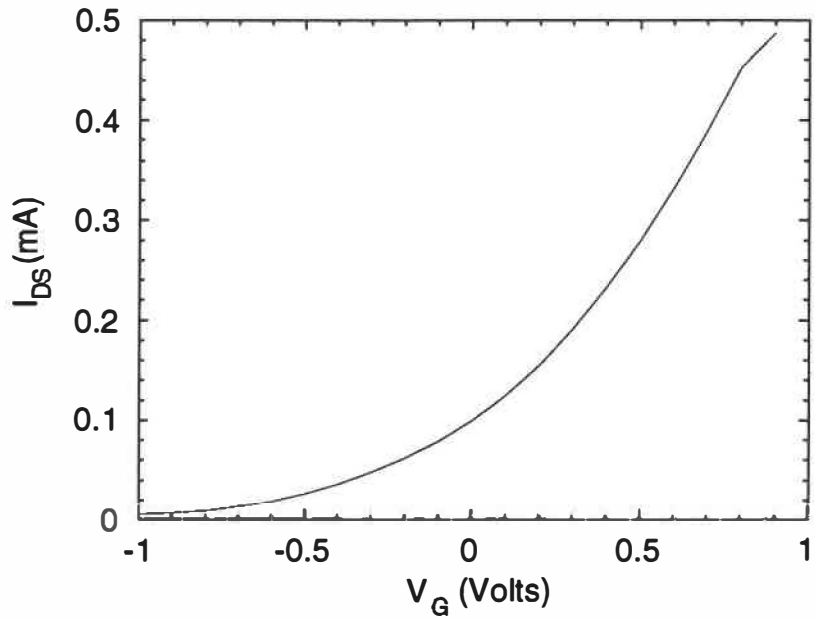


Figure 6.7. I_{DS} Vs V_G curve of the as-fabricated inversion MISFET. The curve indicates that leakage sets in before strong inversion is achieved.

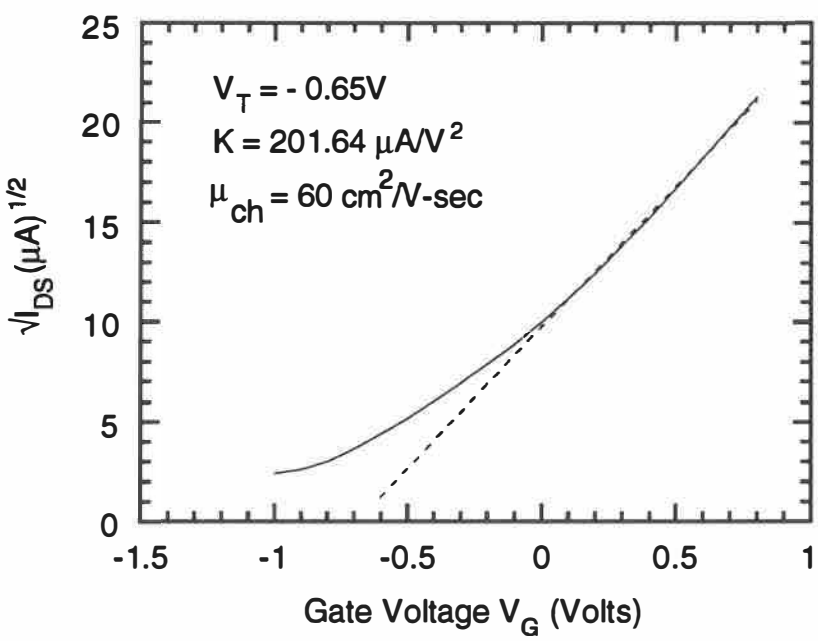


Figure 6.8. The $\sqrt{I_{DS}}$ Vs V_G plot to estimate channel mobility and threshold voltage.

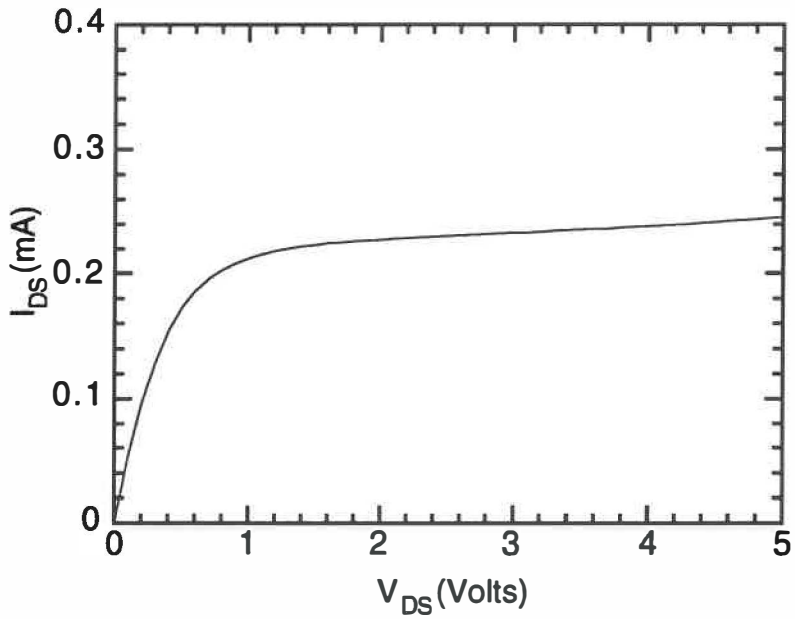


Figure 6.9. Drain current-voltage characteristics of an unpassivated MISFET. The characteristics do not change with gate voltage (V_G).

6.2.3 UNPASSIVATED MISFETS

It is important to note that the unpassivated accumulation and inversion type SAG MISFETs fabricated in parallel using the same process do not show any transistor action proving that interface passivation is responsible for achieving transistor action. The drain current voltage characteristic of an unpassivated FET is shown in figure 6.9. The gate voltage does not have any effect on the drain current and instead of the usual family of curves we measure only a single curve that does not vary with V_G. The Fermi level at the nitride/InP interface is therefore pinned in these samples and the interface appears to be either accumulated or inverted as the particular case might be. We have shown in chapter 1 that when the untreated InP surface is subjected to a thermal anneal above 150°C, a large concentration of surface P vacancies are formed with the

creation of a broad continuum of deep levels about 0.15 eV below the conduction band edge. It is seen in chapter 3 that these levels pin the Fermi level at the interface and result in poor C-V characteristics. Presence of these interface states causes negligible variation in surface potential and the drain current when a gate voltage is applied.

6.2.4 CONCLUSIONS

From these results it is quite obvious that interface engineering is effective in minimizing InP surface degradation by controlling P vacancy formation during high temperature thermal processing resulting in the observed transistor action in MISFET structures. This is the first report in the literature on the fabrication of self-aligned gate MISFETs using an interface engineering technique. This is also the first report on the high temperature stability of S passivated MISFETs. With the successful fabrication of the passivated SAG MISFETs we have accomplished our primary objectives i.e. to control defect formation at the InP/insulator interface and its degradation at high temperatures. The passivated MISFETs show promise with excellent I_{DS} - V_{DS} characteristics and high g_m/g_o values. By eliminating gate leakage we expect to improve device performance. These results indicate the importance of interface engineering techniques for insulated gate devices and these schemes are expected to play a predominant role is the realization of high performance self-aligned-gate FETs and devices based on InP.

The DC characteristics of the passivated SAG HIGFETs is discussed below.

6.3 HIGFETS

We have applied the S passivation process to fabricate for the first time a self-aligned InP/InGaAs/InP HIGFET. The drain I-V characteristics of the as-fabricated 2μm gate length device is shown in figure 6.10.

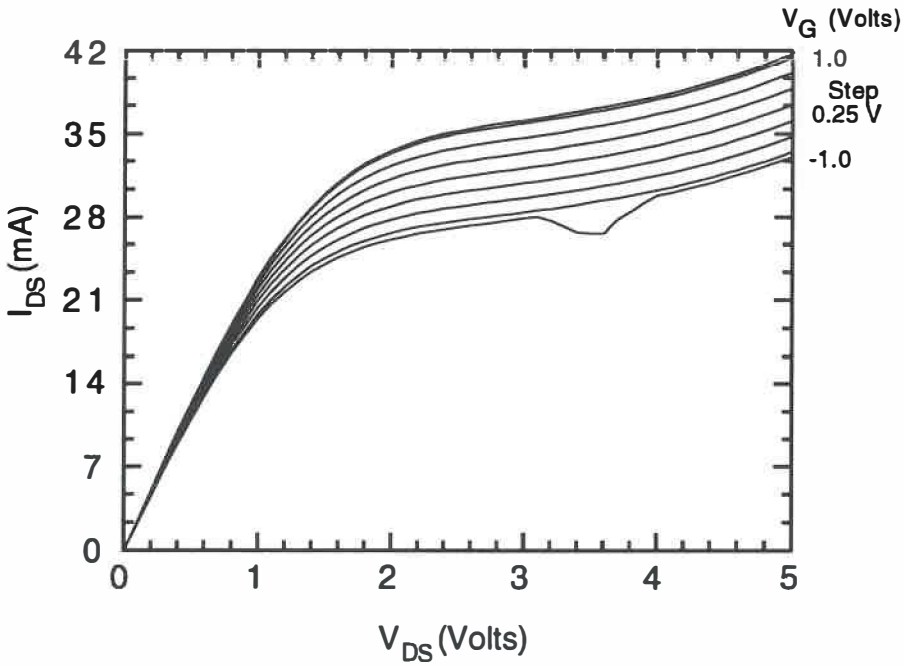


Figure 6.10. Drain I-V characteristics of an as-fabricated 2x200μm^2 HIGFET.

These devices, again exhibit excellent linear and saturation characteristics with a large current drive, $I_{DS} \approx 35$ mA for a gate voltage of V_G =0.25 V and V_{DS} = 5V, as compared to about 1.0 mA for a MISFET of similar dimensions under identical bias conditions. Kinks are observed in the drain I-V characteristics, as seen in figure 6.10, for reasons that are not yet quite clear. The gate leakage characteristics are very similar to figure 6.2. The variation of transconductance with gate voltage is shown in figure 6.11. The device exhibits a leakage limited transconductance of 30 mS/mm. Unlike the MISFETs that show an increase in g_m with voltage, the HIGFET transconductance is almost constant for this gate voltage range.

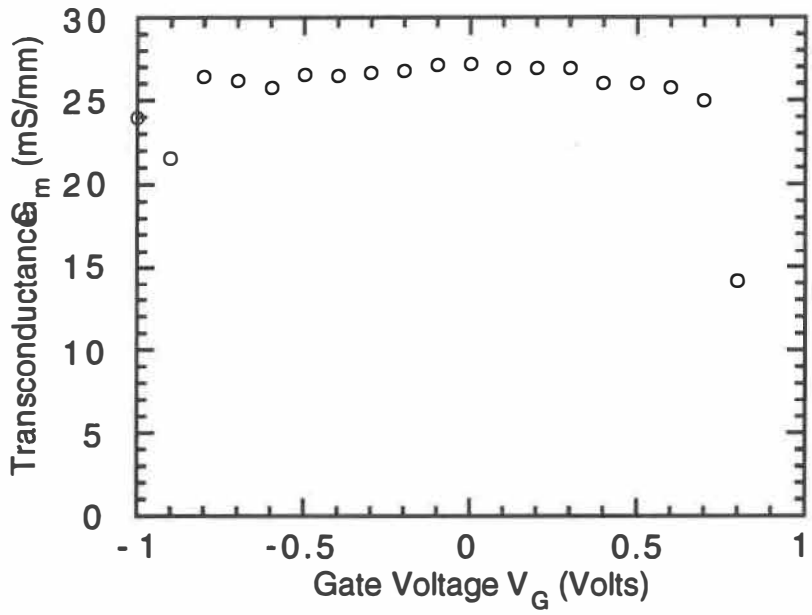


Figure 6.11. Variation of transconductance with gate voltage of as-fabricated HIGFET.

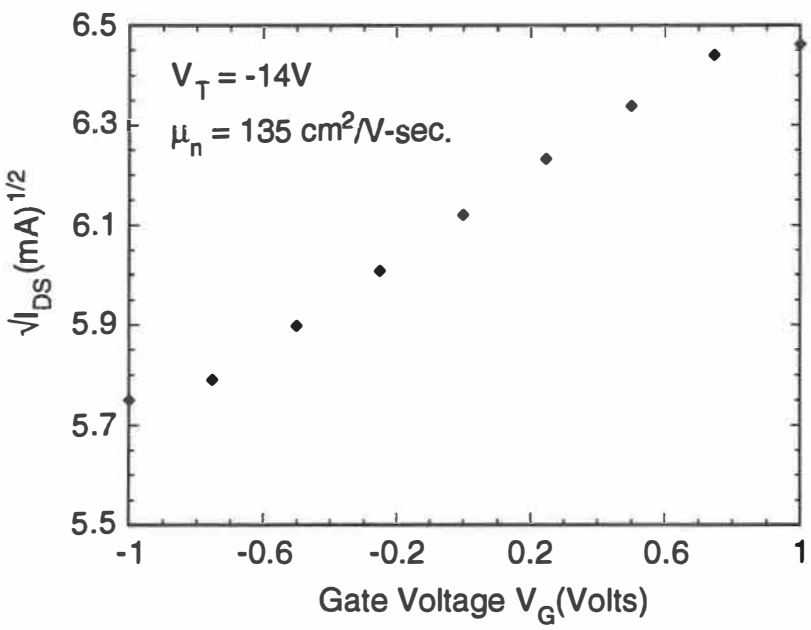


Figure 6.12. The $\sqrt{I_{DS}}$ Vs V_G plot to estimate channel mobility and threshold voltage.

This can be explained due to parallel conduction through the buffer InP layer resulting in bulk carrier transport and the device operates similar to a MESFET. Since the buffer layer is quite thick a significant amount of current may flow through the buffer layer and small gate voltage steps, as in our case, cause only minor changes in the electron charge density in the channel and buffer regions and G_m is therefore fairly constant. A V_T value of -14V estimated from the $\sqrt{I_{DS}}$ Vs V_{GS} plot of figure 6.12 supports this theory. The large current drive is partly due to this mode of operation. At a sufficiently high positive gate voltage 2DEG operation will be preferred. Reducing the buffer layer thickness or eliminating it will reduce the drive but is expected to increase the transconductance. The measured g_o value of 9.04 mS/mm for this device is one-half the value reported for the unpassivated InP/InGaAs HIGFET using a SiO_2 gate insulator [116].

The sheet resistance of the implanted region is about 40Ω/square and the contact resistivity is 15 $\mu\Omega.cm^2$. Apart from insulator leakage and transport through the buffer, parallel conduction in the InP cap also limits the performance of these FETs. Parallel conduction through the cap InP layer of 450Å is a definite possibility in our structure. By reducing gate leakage and the thickness of the buffer and cap layers we expect to realize state-of-the-art HIGFET performance. It is encouraging to note that the leakage limited transconductance of these devices is still comparable to that of unpassivated non-self-aligned HIGFETs with similar epi-layer thicknesses [116].

In conclusion, we have successfully demonstrated the fabrication of the first passivated SAG MISFETs and HIGFETs on InP. It is shown that the S interface engineering scheme controls defect density at the InP/insulator

interface and maintains its integrity during high temperature processing and opens the door for self-aligned structures on InP. If optimized such interface engineering schemes are expected to enhance the performance of HIGFETs that show great promise for high speed and high frequency applications and would be crucial in developing a future self-aligned gate HIGFET technology. In essence, we have shown from this work that interface engineering techniques should be implemented to control the electrical, thermal and optical properties of any critical semiconductor device interface.

CONCLUSIONS AND RECOMMENDATIONS

Development of a mature interface passivation/engineering technology is vital for future high speed Heterojunction insulated gate FETs, currently under intensive research. This thesis represents the first step in that direction. In this dissertation, we have demonstrated the effectiveness of interface engineering techniques in controlling the InP/insulator interface and their importance in the realization of InP based self-aligned gate FETs. The objective is to achieve an interface with low trap densities and good thermal stability. A case study is presented for the S passivation process, that is characterized in detail to understand the exact nature of the, hereto unknown, passivating mechanism. The essential requirements to be fulfilled by any potential high temperature interface engineering technique for InP have been identified. Our investigation of the S passivation mechanism has also led to the proposal of a universal model that explains the formation of various sulfide layers on InP. The model provides the first glimpse of the passivating behavior of S layers on InP. The complete InP/InGaAs fabrication technology suitable for SAGFETs has been developed. A copyright exclusive diagnostic mask set for insulated gate FET fabrication has been designed. The S passivation technique has been successfully and reproducibly applied to fabricate for the first time interface engineered accumulation and inversion type SAG MISFETs and a InGaAs/InP accumulation mode SAG HIGFET. This is the first time an extremely reproducible SAG technology is proposed for InP based insulated gate FETs. We demonstrate in this work that interface engineering can control the properties of any critical interface of a semiconductor device.

S passivation of the InP surface is studied by PL, XPS and angle resolved XPS techniques. P vacancy related deep levels at the interface are suppressed in the temperature range 150 - 300°C by S reacting with the InP substrate to form a 30Å cap In_2S_3 layer that reduces P out-diffusion from the surface. The proposed universal model provides the common link between the various S layer formation techniques found in literature and classifies them into either a) photo electrochemical surface interactions that lead to monolayer S coverage of the surface or b) equilibrium phase diagram reactions between InP and S that result in thicker sulfide layers. The latter reactions are further divided into mild, intermediate and strong sulfurisation regimes. It is shown that annealing between 150-300°C corresponds to the case of mild sulfurisation.

The effectiveness of the passivation process is tested by studying the high frequency C-V characteristics of MIS structures. A novel and inexpensive indirect plasma CVD dielectric deposition technique has been developed that effectively and inexpensively avoids plasma damage of the substrate. S passivated InP/Si_3N_4 MIS capacitors show excellent near ideal high frequency C-V characteristics with negligible (< 0.1V) hysterisis. The surface potential of these devices is easily varied to scan the Fermi level between the conduction and valence bands. Using Terman analysis, we estimate low interface densities in the range of $1x10^{11}$ $cm^{-2}.eV^{-1}$ with a midgap value of $8x10^{10}$ $c\,m^{-2}.eV^{-1}$. A preliminary MIS DLTS study is performed to evaluate the activation energy and the capture cross-section of the interface traps. The MIS capacitors exhibit good thermal stability and preserve their C-V characteristics after a high temperature implant activation step at 700°C. The chemical passivation process is quite non-

uniform and there is considerable leakage through the nitride under certain conditions.

The diagnostic chip with 5 mask levels and a minimum feature size of 1μm is designed to fabricate the SAG MISFETs and HIGFETs. The layout includes special test structures to evaluate the various material, process and device parameters. Apart from the interface passivation technique, we propose a complete technology package that includes substrate evaluation, wafer cleaning, mesa isolation, indirect plasma deposition of silicon nitride, implant conditions, a slow ramp implant activation, gate and contact metallization from the point of view of an interface engineered metal gate SAG technology. The existing process technologies have been used as-is or suitably modified to integrate the various fabrication steps. In particular we propose a new slow ramp lamp anneal (SRLA) that preserves metal gate integrity during implant activation for a self-aligned process. Various characterization techniques like XPS, PL, HXRD, ERD etc. have been used to arrive at the conditions necessary for fabrication.

The passivated SAG MISFETs and HIGFETs show well-defined transistor characteristics with low output conductance and modest performance. The accumulation and inversion type MISFETs exhibit peak transconductance of 10-12 mS/mm and 2-3 mS/mm respectively and the maximum value for HIGFETs is 30mS/mm. In contrast, unpassivated FETs fabricated using the same process sequence do not show any transistor action implying that interface passivation is responsible for realizing the SAGFETs. Post fabrication anneal has a strong effect on the final device and process characteristics, while annealing at 400°C for 30 minutes improves the characteristics of accumulation type MISFETs, it degrades the performance of inversion mode MISFETs. The minimum contact

resistivity is 15μm.cm^2 for both MISFETs and HIGFETs. The sheet resistance is about 2-5 kΩ/sq. for InP substrates and approximately 40Ω/sq. for the hetero-junction wafers. FET performance is limited by gate leakage due to S incorporation into the insulator. In addition, the passivated interface is rough leading to low channel mobilities. Finally, uniformity and stress related issues have to be addressed. Nevertheless, these results indicate the importance of interface engineering techniques for high temperature stability of InP based insulated gate structures and this work is expected to lead to a more mature self-aligned technology.

In this thesis, we have proposed and successfully demonstrated a novel approach to fabricate next generation, high speed self-aligned insulated gate FETs based on InP or other compound semiconductors. We proposed that an additional interface engineering step in the process would control degradation of the InP/insulator interface. We have demonstrated this idea by fabricating self-aligned insulated gate InP MISFETs and InP/InGaAs HIGFETs that use a S interface engineering step. Study of the passivation process resulted in elucidation of the passivation mechanism and the kinetics of sulfide layer formation on InP. Although the first passivated SAGFETs show excellent current-voltage characteristics their performance is much inferior compared to state-of-art devices. The fabrication process is extremely reproducible but uniformity is poor and has to be improved. Other problems of concern are high gate leakage and low channel mobility . It needs to be stressed that until these important issues are solved and state-of-art performance is achieved, interface engineering may not be a viable technology. To this end we propose two independent interface engineering steps or their combination as possible solutions. The first is

a variation of the current procedure that leaves just one monolayer of S bonded to In with no elemental residues and the second is to epitaxially grow a strained GaP layer on InP.

FUTURE WORK

As mentioned repeatedly during the course of this presentation, the current work should be viewed only as the first demonstration on the feasibility of using interface engineering techniques in a SAG process. A good deal of effort on all fronts from material, process to device characterization and development is required before the eventual realization of a mature SAG technology for InP. The following is a list (not by any means complete) of suggestions for further effort in this direction

- A suitable , uniform epitaxial passivation technique with good thermal stability should be developed .
- Strategies to reduce gate leakage must be developed.
- The channel mobility should be increased and the variation of mobility with annealing should be investigated.
- A better heterostructure device design with low parallel conduction should be used to achieve state-of-art device performance.
- Strategies to control the threshold voltage.
- PL should be extended for practical MIS structures.
- Lower stress silicon-oxy-nitride layers can be used as gate insulator.
- Changes in H content and stress of the insulating dielectric layer due to thermal processing need to be studied.

- Gate metallizations with better thermal stability should be incorporated in the process.
- A more complete understanding of interface trap properties and their high frequency response is required.
- Window re-growth epitaxial techniques can be used to realize SAG FETs without high temperature processing.
- Microwave characterization of the devices.

REFERENCES

1. WILMSEN, C.W., Editor, "Physics and Chemistry of III-V compound semiconductor interfaces", Plenum Press, (1985).

2. ILIADIS, A.A., LEE, W. and AINA, O.A., "N-Channel depletion-mode InP FET with enhanced barrier height gates", IEEE Electron Device Letters, 10, pp. 370-372, (1989).

3. BAHL, S.R. and DEL ALAMO, J.A., "Breakdown voltage enhancement from channel quantization in InAlAs/n^+-InGaAs HFET's", IEEE Electron Device Letters, 13, pp. 123-125, (1992).

4. GREENBERG, D.R., DEL ALAMO, J.A. and BHAT, R., "A Recessed gate InAlAs/n^+-InP HFET with InP etch-stop layer", IEEE Electron Device Letter, 13, pp. 137-139, (1992).

5. WAGER, J.F., OWEN, S.J.T. and PRASAD, S.J., "InP MISFET technology - interface considerations", J.Electrochem.Soc., 134, pp. 160-165, (1987).

6. IYER, R., CHANG, R.R., and LILE, D.L., "Sulfur as a surface passivation for InP", Appl.Phys.Lett., 53, pp. 134-136, (1988).

7. PANDE, K.P. and NAIR, V.K.R., "High mobility n-channel metal-oxide-semiconductor field effect transistors based on SiO_2-InP interface", J.Appl.Phys., 55, pp. 3109 - 3114, (1984).

8. PANDE, K.P., NAIR, V.K.R., and GUTIERREZ, D., "Plasma enhanced metal-organic chemical vapor deposition of aluminium oxide dielectric film for device applications", J.Appl.Phys., 54, pp. 5436-5438, (1983).

9. LILE, D.L. and TAYLOR, M.J., "The effect of interfacial traps on the stability of insulated gate devices on InP", J.Appl.Phys., 54, pp. 260-267, (1983).

10. LEE, P.Z., CHANG, H.L., and MEINERS, L.G., "Substrate-affected instability in accumulation-mode InP metal-insulator-semiconductor field-effect transistor", J.Appl.Phys., 63, pp. 5694-5698, (1988).

11. IYER, R., CHANG, R.R., DUBEY, A. and LILE, D.L., "The effect of phophorous and sulfur treatment on the surface properties of InP", J.Vac.Sci.Technol.B.,6, pp. 1174-1179, (1988).

12. NEUDECK, P.G., CARPENTER, M.S., MELLOCH, M.R. and COOPER, J.A., Jr., "Significant long-term reduction in n-channel MESFET subthreshold leakage using ammoniun-sulfide surface treated gates", IEEE Electron Device Letters, 12, pp. 553-555, (1991).

13. WILMSEN, C.W., GEIB, K.M., SHIN, J., IYER, R. and LILE, D.L., "The sulfurized InP surface", J.Vac.Sci.Technol., 7, pp. 851-853, (1989).

14. MARTIN, E.A., AINA, O.A., ILIADIS, A.A., MATTINGLY, M.R. and STECKER, L.H., "Undoped InP/InGaAs heterostructure insulated-gate FET's grown by OMVPE with PECVD-deposited SiO_2 as gate insulator", IEEE Electron Device Letter, 9, pp.500-502, (1988).

15. DEL ALAMO, J.A. and MIZUTANI, T., "A self-aligned enhancement-mode AlGaAs/InP MISFET", IEEE Electron Device Letter, 8, pp. 220-222, (1987).

16. FEUER, M.N., HE, Y., SHUNK, S.C., HUANG, J.H., VANG, T.A., BROWN-GOEBELER, K.F. and CHANG, T., "Direct-coupled FET logic circuits on InP", IEEE Electron Device Letters, 12, pp. 98-100, (1991).

17. HARRANG, J.P., DANIELS, R.R., FUJI, H.S., GRIEM, H.T. and RAY, S., "High performance $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ HFET compatible with optical-dectector integration", IEEE Electron Device Letters, 12, pp. 206-209, (1991).

18. MARTIN, E.A., AINA, O.A., ILIADIS, A.A., MATTINGLY, M.R. and HEMPFLING, E., "Highly stable microwave performance of InP/InGaAs HIGFET's", IEEE Transactions on Electron Devices, 37, pp. 1916-1917, (1990).

19. DICKMANN, J., HASPEKLO, H., GEYER, A., DAEMBKES, H., NICKEL,H. and LOSCH, R., "High performance fully passivated InAlAs/InGaAs/InP HFET", Electronic Letters, 28, pp. 647-648, (1992).

20. IWASE, M., MIZUNO, T., TAKAHASHI, M., NIIYAMA, H., FUKUMOTO, M., ISHIDA, K., INABA, S., TAKIGAMI, Y., SANDA, A., TORIUMI, A., and YOSHIMI, M., "High-performance 0.10 μm CMOS devices operating at room temperature", IEEE Electron Device Letters, 14, pp.51-53, (1993).

21. NGUYEN, L.D., BROWN, A.S., THOMPSON, M.A., JELLOIAN, L.M., LARSON, L..E. and MATLOUBIAN, M., "650Å Self-aligned-gate pseudomorphic $Al_{0.48}In_{0.52}As/Ga_{0.20}In_{0.80}As$ high electron mobility transistors", IEEE Electron Device Letters, 13, pp. 143-145, (1992).

22. TSENG, W.F., BARK, M.L., DIETRICH, H.B., CHRISTOU, A., HENRY, R.L., SCHMIDT, W.A. and SAKS, N.S., "A virtual self-aligned process for n-channel InP IGFET's (or MISFET's)", IEEE Electron Device Letters, 11, pp.299-301, (1981).

23. BIEDENBENDER, M.D. and KAPOOR, V.J., "Chemical nature of silicon nitride-indium phosphide interface and rapid thermal annealing for InP MISFETs", J.Electrochem.Soc., 137, pp. 1537-1547, (1990).

24. CAMERON, D.C., IRVING, L.D., WHITEHOUSE, C.R., and WOODWARD, J, "Planar self-aligned ion-implanted InP MOSFET", Electronics Letters, 18, pp. 534-535, (1982).

25. OIGAWA, K., UEKUSA, S., SUGIYAMA, Y. and TACANO, M., "Self-aligned inversion-mode InP MISFET", Japan's Journal of Applied Physics, 26, pp. 1719-1721, (1987).

26. LAI, R., BHATTACHARYA, P.K., ALTEROVITZ, S.A., DOWNEY, A.N. and CHOREY, C., "Low-temperature microwave characteristics of pseudomorphic $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ modulation-doped field-effect transistors", IEEE Electron Device Letters, 11, pp. 564-566, (1990).

27. VAN VECHTEN, J.A., "A simple man's view of the passivation of semiconductors", Corrosion Science, 31, pp. 39-52, (1990).

28. SUNDARARAMAN, C.S., POULIN, S., CURRIE, J.F. and LEONELLI, R., "The sulfur-passivated InP surface", Can,J, Phys., 69, pp. 329-332, (1991).

29. LEONELLI, R., SUNDARARAMAN, C.S., and CURRIE, J.F., "Photoluminescence study of sulfide layers on *p*-type InP", Appl.Phys,Lett., 57, pp. 2678-2679, (1990).

30. SUNDARARAMAN, C.S. and CURRIE, J.F., "Fabrication of novel self-aligned MISFETS on InP by a S interface engineering technique", Can.J.Phys., 70, pp. 1035-1038 (1992).

31. VAN VECHTEN, J.A., WAGNER, J.F., "Consequences of anion vacancy nearest-neighbor hopping in III-V compound semi-conductors: drift in InP metal-insulator-semiconductor field effect transistors", J.Appl.Phys., 57, pp. 1956-1960 (1985).

32. SCHACHTER, R., OLEGO, D.J., BAUMANN, J.A., BUNZ, L.A., RACCAH, P.M., and SPICER, W.E., "Interfacial properties of InP and phosphorus deposited at low temperature", Appl.Phys.Lett., 47, pp. 272-274, (1985).

33. YOUNG, P.G. and KAPOOR, V.J., In Proceedings of the symposium on dielectric films on compound semiconductors, The Electrochemical Society, 88-15, pp. 151-179, (1988).

34. GENDRY, M., DURAND, J., VILLENEUVE, M. and COT, L., "Etude du diagramme des phases condensées du système In-P-S", Thin Solid FIlms, 139, pp. 53-59, (1986).

35. HELIX, M.J., VAIDYANATHAN, K.V., STREETMAN, B.G., DIETRICH, H.B. and CHATTERJEE, P.K., "R.F. plasma deposition of silicon nitride layers", Thin Solid Films, 55, pp. 143-148, (1978).

36. TAO, Y., YELON, A., SACHER, E., LU, Z.H. and GRAHAM, M.J., "S-passivated InP (100)-(1 X 1) surface prepared by a wet chemical process", Appl.Phys. Lett., 60, pp. 2669-2671, (1992).

37. RAO, M.V., AINA, O.A., FATHIMULLA, A. and THOMPSON, P.E., "Deep radiative levels in as-grown and implanted rapid thermal annealed InP", J.Appl.Phys., 64, pp. 2426-2433, (1988).

38. CHANG, R.R., IYER, R. AND LILE, D.L., "Surface characterization of InP using photoluminescence", J.Appl. Phys., 61, pp. 1995-2004, (1987).

40. BANERJEE, S., SRIVASTAVA, K. and ARORA, B.M., "Thermal degradation of InP in open tube processing: deep-level photoluminescence", J.Appl.Phys., 68, pp. 2234-2330, (1990). and BANERJEE, S., "Comment on 'Photoluminescence study of sulfide layers on *p*-type InP' ", Appl.Phys.Lett., 59, pp.1796-1797, (1991).

39. TEMKIN, H., and DUTT, B.V., in Mat. Res. Soc. Symp. Proc., 14, p. 253, (1983).

41. WAGNER, C.D., RIGGS, W.M., DAVIS, L.E. and MOULDER, J.F., Handbook of X-ray photoelectron spectrocopy, edited by G.G. Muilenberg, (Perkin-Elmer, N.Y.), (1989).

42. KLASSON, M., BERNATSSON, A., HEDMAN, J., NILSSON, R. and NORDLING, C., J. Electron Spectroscopy, 3 , p. 427, (1974).

43. YIH, R.S. and RATNER, B.D., "A comparison of two angular dependent ESCA algorithms useful for constructing depth profiles of surfaces", Journal of Electron Spectroscopy and Related Phenomena, 43, pp. 61-82, (1987).

44. BRIGGS, D. and SEAH, M.P., editors, Practical Surface Analysis, John Wiley and sons, (1983).

45. GENDRY, M., DURAND, J. and COT, L.., "Utilisation du diagramme des phases condensées du système In-P-S pour l'analyse de la composition des couches de sulfures natifs formées sur InP", Thin Solid Films, 150, pp. 347-356, (1987).

46. BARBOUTH, N., BERTHIER, Y., OUDAR, J., MOISON, J.M. and BENSOUSSON, M., " The first steps of the sulfurization of III-V compounds", J. Electrochem. Soc., 133, pp. 1663-1670, (1986).

47. OIGAWA, H., FAN, J., NANNICHI, Y., SUGAHARA, H. and OSHIMA, M., "Universal passivation effect of $(NH_4)_2S_x$ treatment on the surface of III-V compound semiconductors", Japanese Journal of Applied Physics, 30, pp. L322-L325, (1991).

48. HOLLINGER, G., ESTRADA, C., DURAND, J. and GENDRY, M., "Spectroscope XPS d'oxydes et de sulfures d'InP: composes etalons et couches de passivation", J.Microsc.Spectrosc.Electron., 13, pp. 31-48, (1988).

49. CLARK, D.T. and FOK, T., "An investigation by electron spectroscopy for chemical analysis of chemical treatments of the (100) surface of n-type InP epitaxial layers for langmuir film disposition", Thin Solid Films, 70, pp. 261-283, (1980).

50. KAPILA, A. and MALHOTRA, V., "Passivation of the InP surface using polysulfide and silicon nitride overlayer", Appl. Phys. Lett., 62, pp.1009-1011, (1993).

51. LAU, W.M. and KWOK, R.W.M., "Controlling surface band-bending of InP with polysulfide treatments", Surf. Science, 271, pp. 579-586, (1992).

52. KLOPFENSTEIN, P., BASTIDE, G., ROUZEYRE, M., GENDRY, M. and DURAND, J., "Interface studies and electrical properties of plasma sulfide layers on *n*-type InP", J. Appl.Phys., 63, pp. 150-158, (1988).

53. GENDRY, M., DURAND, J., ERMAN, M., THEETEN, J.B., NEVOT, L. and PARDO, B., "Chemical and structural analysis by ellipsometry and X-ray reflectometry of thin sulfide layers grown on InP", Appl.Surf.Science, 44, pp. 309-320, (1990).

54. GALLET, D. and HOLLINGER, G., "Chemical, structural, and electronic properties of sulfur-passivated InP(001) (2X1) surface treated with $(NH_4)_2S_x$", Appl.Phys.Lett., 62, pp. 982-984, (1993).

55. BESSOLOV, V.N., LEBEDEV, M.V., NOVIKOV, E.B. and TSARENKOV, B.V., "Sulfide passivation of III-V semiconductors: Kinetics of the photoelectrochemical reaction", J.Vac.Sci.Technol., 11, pp. 10-14, (1993).

56. VIJH, A.K., Electrochemistry of metals and semiconductors, Marcel Dekker, New York, (1973).

57. MORRISON, S.R., Electrochemistry at semiconductor and oxidized metal electrodes, Plenum Press, New York, (1980).

58. LUDEKE, R. and ESAKI, L., "Electron energy-loss spectroscopy of GaAs and Ge surfaces", Phys.Rev. Lett., 33, pp. 653-656, (1974).

59. MASSIES, J., ETIENNE, P., DEZALY, F. and LINH, N.T. , "Stoichiometry effects on surface properties of GaAs {100} grown in situ by MBE", Surf. Sci., 99, pp. 121-131, (1980).

60. YABLONOVITCH, E., SKROMME, B.J., BHAT, R., HARBISON, J.P. and GMITTER, T.J., "Band bending, fermi level pinning and surface fixed charge on chemically prepared GaAs surfaces", Appl. Phys.Lett., 54, pp. 555-557, (1989).

61. PETITJEAN, M., PROUST, N., CHAPEAUBLANC, J.F. and PERRIN, J., "Optimization of the InP/SiO_2 interface treatment by $(NH_4)_2 S_x$ for the InP MISFET fabrication technology", Sensors and Actuators A, 33, pp. 33-38, (1992).

62. SPICER, W.E., NEWMAN, N., SPINDT, C.J., LILIENTAL-WEBER, Z. and WEBER, E.R.," 'Pinning' and Fermi level movement at GaAs surfaces and interfaces", J.Vac.Sci.Technol., 8, pp. 2084-2089, (1990).

63. LAU, W.M., JIN, S., WU, X-W. and INGREY, S., "Studies on type-inversion of sulfide-treated p-InP", J.Vac. Sci. Technol.A, 9, pp. 994-997 (1991).

64. SKROMME, B.J., SANDROFF, C.J., YABLONOVITCH, E. and GMITTER, T.J., "Effects of passivating ionic films on the photoluminescence properties of GaAs", Appl.Phys. Lett., 51, pp. 2022-2024, (1987).

65. TAO, Y., YELON, A. and LEONELLI, R., "Electronic properties of $(NH_4)_2S$ passivated InP(100) surfaces" Can.J.Phys., 70, (1992).

66. MATHEWS, J.W. and BLAKESLEE, A.E., "Defects in epitaxial multilayers: I. Misfit dislocations", Journal of Crystal Growth, 27, pp. 118-125, (1974).

67. HXRD commercial software, written by P.Fewster, Philips.

68. WIE, C.R., CHEN, J.C., KIM, H.M., LIU, P.L., CHOI,Y. and HWANG, D.M., "X-ray interference measurement of ultrathin semiconductor layers", Appl. Phys. Lett., 55, pp. 1174-1776, (1989).

69. RAZEGHI, M., in Semiconductors and semimetals, 31, "Indium phosphide crystal growth and characterization", eds. R.K.W. Willardson, and A.C. Beer, p.327.

70. AINA, L., MATTINGLY, M., FATHIMULLA, A., MARTIN, E.A., LOUGHRAN, T. and STECKER, L., "OMVPE growth of AlInAs and device quality AlInAs-based heterostructures", Journal of Crystal Growth, 93, pp. 911-918 (1988).

71. ADACHI, S., "Chemical etching of InP and InGaAsP/InP", J. Electrochem. Soc., 129, pp. 609-613, (1982).

72. RAMAM, A., KAPOOR, S., PRABHAKAR, S., GULATI, R. and CHANDRA, I., "Study of mesa undercuts produced in GaAs with H_3PO_4-based etchants", J. Electrochem.Soc., 136, pp. 2405-2410, (1989).

73. C.S.SUNDARARAMAN, A.MOUTON and J.F.CURRIE, Chemical Etching of InP, in Proceedings of the 2nd International Conference on InP and related materials, Denver, Colorado, April 23-25,1990, pp.224-227. The Institute of Electrical and Electronic Engineers, New York, 1990.

74. MOUTON, A., SUNDARARAMAN, C.S., LAFONTAINE, H., POULIN, S. and CURRIE, J.F., "Etching of InP by H_3PO_4, H_2O_2 solutions", Japanese Journal of Appl.Phys., 29, pp. 1912-1913, (1990).

75. LIDA, S. and ITO, K., "Selective etching of gallium arsenide crystals in H_2SO_4- H_2O_2- H_2O system", J. Electrochem Soc., 118, pp. 768-770, (1971).

76. GHANDHI, S., in VLSI Fabrication Principles, Silicon and Gallium Arsenide, (John Wiley, New York) (1983).

77. CHANG, H.L., MEINERS, L.G. and SA, C.J., "Preparation and electrical properties of InP_xO_y gate insulators on InP", Appl.Phys.Lett., 48, pp. 375-377, (1986).

78. ASITO, A., FOUCARAN, A., BASTIDE, G., ROUZEYRE, M., LECLERCQ, J.L. and DURAND, J., "Preparation electrical properties and interface studies of plasma nitride layers on *n*-type InP", J. Appl. Phys., 70, pp. 2584-2588, (1991).

79. MEINERS, L.G., "Indirect plasma deposition of silicon dioxide[a)]", J.Vac.Sci.Technol., 21, pp. 655-658, (1982).

80. NICOLLIAN, E.H. and BREWS, J.R., in MOS (Metal Oxide Semiconductors), Physics and Tech., John Wiley, p.150, (1982).

81. GUJRATHI, S.C., AUBRY, P., LEMAY, L. and MARTIN, J.P., "Nondestructive surface analysis by nuclear scattering techniques", Can.J.Phys., 65, pp. 950-955, (1987).

82. GUJRATHI, S.C., in ACS Symp., Series no. 440, Metalization in Polymers, eds. E. Sacher, J. Pireaux and S.T. Rowalczyk, 6, pp. 88-109, (1990).

83. GUJRATHI, S.C. and BULTENA, S., "Depth profiling of hydrogen using the high efficiency ERD-TOF technique", Nuclear Instruments and Methods in Physics Research, 64, pp. 789-795, (1992).

84. SHARMA, B.L., "Implantation in InP technology", Solid State Technology, pp. 113-117, (1989).

85. RAO, M.V. and THOMPSON, P.E., "Two-step rapid thermal annealing of Si-implanted InP:Fe", Appl.Phys.Lett., 50, pp. 1444-1446, (1987).

86. AMBRIDGE, T. and ASHEN, D.J., "Automatic electrochemical profiling of carrier concentration in InP", Electronic Letters, 15, pp. 647-648, (1979).

87. TELL, B., BROWN-GOEBELER, K.F. and CHENG, C.L., "Rapid thermal annealing of elevated-temperature silicon implants in InP", Appl.Phys.Lett., 52, pp. 299-301, (1988).

88. WANG, K.W., "Formation of a shallow p^+layer on InP using P/Be co-implant", Appl. Phys. Lett., 25, pp. 2127-2129, (1987).

89. SUNDARARAMAN, C.S., POULIN, S., MASUT, R.A. and CURRIE, J.F., "Rapid thermal annealed ohmic contacts to high temperature Zn implanted InP", in Proceedings on Emerging Optoelectronic Technologies, SPIE, Tata McGraw Hill, pp. 68-72, (1991).

90. DEL ALAMO, J.A. and AZZAM, W.J., "A floating-gate transmission-line model technique for measuring source resistance in heterostructure field-effect transistors", IEEE Transaction of Electron Devices, 36, pp. 2386-2393, (1989).

91. PANDE, K.P., MARTIN, E., GUTIERREZ, D. and AINA, O., "An optimal annealing technique for ohmic contacts to ion-implanted *n*-layers in semi-insulating indium phosphide", Solid-State Electronics, 30, pp. 253-258, (1987).

92. BERGER, H.H., "Contact resistance and contact resistivity", J.Electrochem.Soc., 119, pp. 507-514, (1972).

93. BERGER, H.H., "Models for contacts to planar devices", Solid-State Electron., 15, pp.145-158, (1972).

94. YAMAGUCHI, E., NISHIOKA, T. and OHMACHI, Y., "Ohmic contacts to Si-implanted InP", Solid-State Electronics, 24, pp. 263-265, (1981).

95. REEVES, G.K. and HARRISON, H.B., "Obtaining the specific contact resistance from transmission line model measurements", IEEE Electron Device Letters, 3, pp. 111-113, (1982).

96. TING, C. and CHEN, C.Y., "A study of the contacts of a difused resistor", Solid-State Electronics, 14, pp. 433-438, (1971).

97. IYER, R., CHANG, R.R. and LILE, D.L., "The growth and in-situ characterization of chemical vapor deposited SiO_2", Journal of Crystal Growth, 83, pp. 290-296, (1987).

98. IYER, R. and LILE, D.L., "The role of polysulfides in the passivation of the InP surface", - private communication.

99. TERMAN, L.M., "An investigation of surface states at a Silicon/silicon oxide interface employing Metal-oxide-Silicon diodes", Solid State Electron., 5, pp. 285-299, (1962).

100. PIERRET, R.F., in Field effect devices, Vol. IV, Modular series on solid state devices, Addison-Wesley publishing company, Reading, (1990).

101. LANG, D.V., "Deep-level transient spectroscopy: A new method to characterize traps in semiconductors", J. Appl. Phys., 45, pp. 3023-3032, (1974).

102. KATSUBE, T., KAKIMOTO, K. and IKOMA, T., "Temperature and energy dependences of capture cross sections at surface states in Si metal-oxide semiconductors diodes measured by deep level transient spectroscopy", J. Appl. Phys., 52, pp. 3504-3508, (1981).

103. MURRAY, F., CARIN, R. and BOGDANSKI, P., "Determination of high-density interface state parameters in metal-insulator-semiconductor structures

by deep-level transient spectroscopy", J. Appl. Phys., 60, pp. 3592-3598, (1986).

104. YAMASAKI, K., YOSHIDA, M. and SUGANO, T., "Deep level transient spectroscopy of bulk traps and interface states in Si MOS diodes", Japanese Journal of Appl. Phys., 18, pp. 113-122, (1979).

105. WANG, K.L. and EVWARAYE, A.O., "Determination of interface and bulk-trap states of IGFET's using deep-level transient spectroscopy", J. Appl. Phys., 47, pp. 4574-4577, (1976).

106. IMMORLICA, A.A. JR., DECKER, D.R. and HILL, W.A., "A diagnostic pattern for GaAs FET material development and process monitoring", IEEE Transactions on Electron Devices, 27, pp.2285-2291, (1980).

107. National Research Council, Ottawa, Canada, CGAS mask set, Private communication.

108. DAVID, J.M. and BUEHLER, M.G., "A numerical analysis of various cross sheet resistor test structures", Solid State Electron., 20, pp. 539-543, (1977).

109 PUCEL, R.A. and KRUMM. C.F., Elec. Lett., 12 , pp. 539-543, (1977).

110. POUVIL, P., ZEMOUR, B., PASQUET, D. and GAUBERT, J., "Determination of source and drain parasitic resistances of HEMTs", Electronics Letters, 28, pp. 618-619, (1992).

111. KROEMER, H., CHIEN, W., HARRIS, J.S. JR. and EDWALL, D.D., "Measurement of isotype heterojunction barriers by *C-V* profiling[a)]", Appl.Phys.Lett., 36, pp. 295-297, (1980).

112. CHAN, Y-J., PAVLIDIS, D. and NG, G-I., "The influence of gate-feeder/mesa-edge contacting on sidegating effects in

$In_{0.52}Al_{0.48}As/In_{0.53}GA_{0.47}As$ heterostructure FET's", IEEE Electron Device Letters, 12, pp. 360-362, (1991).

113. OREN, M. and CHOUDHURY, A.N.M.M., "Interconnect metallization technique for GaAs digital ICs", J. Electrochem. Soc., 134, pp. 750-752, (1987).

114. SZE, S.M., in Physics Of Semiconductors Devices, Wiley Eastern, (1981).

115. GRAY, P.E. and SEARLE, C., in Electronic Principles, Physics, Models, and Circuits., John Wiley & Sons, Inc., p. 36, (1969).

116. MARTIN, E.A., "High-performance undoped indium phosphide/indium gallium arsenide heterojunction insulated-gate field-effect transistors", Ph.D Thesis, University of Maryland, (1989).

ANNEXE I

SINGLE OVERLAYER MODEL

The theoretical calculation for the single overlayer model of chapter 2 is presented in this appendix. The model is used to calculate the thickness d of the cap sulfide overlayer by angle resolved XPS measurements. For the calculation, a thin abrupt layer of In_2S_3 is assumed to be present over the InP substrate. The area "A(Θ)" under the XPS peak for any element for any Θ is given as a summation over depth

$$A(\Theta) = C\int_0^{\infty} n(x)\, e^{\left(\frac{-x}{\lambda \cos \Theta}\right)} dx \qquad (1)$$

where, n(x) is the number of atoms of the element per unit volume (cm^{-3}) as a function of depth "x", λ is the mean free path of the photoelectrons in the material, Θ is the photoelectron take-off angle measured with respect to the substrate and "C" the constant of integration.

For Indium, this area can be written as

$$A(\Theta)_{[In]} = C\int_0^{d} N_{L(In)}\, e^{\left(\frac{-x}{\lambda \cos \Theta}\right)} dx + \int_0^{\infty} N_{S(In)}\, e^{\left(\frac{-x}{\lambda \cos \Theta}\right)} dx \qquad (2)$$

where, $N_{L(In)}$ and $N_{S(In)}$ are the number of In atoms/cm^3 in In_2S_3 and InP respectively and d is the thickness of the overlayer. Integrating over the limits, we have

$$= C\left[N_{L(In)}\, \lambda \cos \Theta \left[1 - e^{\left(\frac{-d}{\lambda \cos \Theta}\right)}\right] + N_{S(In)}\, \lambda \cos \Theta\, e^{\left(\frac{-d}{\lambda \cos \Theta}\right)}\right] \qquad (3)$$

Similarly for S we have

$$A(\Theta)_{[S]} = C\int_0^{d} N_{L(S)}\, e^{\left(\frac{-x}{\lambda \cos \Theta}\right)} dx \qquad (4)$$

where and $N_{L(S)}$ corresponds to the number of S atoms/cm^3 in In_2S_3.

Integrating, we have

$$= C\ N_{L(S)}\ \lambda\cos\Theta\left[1 - e\left(\frac{-d}{\lambda\cos\Theta}\right)\right] \qquad (5)$$

and the variation of S to In concentrations with depth is given as the ratio ($R_{calc.}$) of the peak area of S with respect to In and is given by

$$\frac{A(\Theta)[S]}{A(\Theta)[In]} = \frac{N_{L(S)}\ \lambda\cos\Theta\left[1 - e\left(\frac{-d}{\lambda\cos\Theta}\right)\right]}{N_{L(In)}\ \lambda\cos\Theta\left[1 - e\left(\frac{-d}{\lambda\cos\Theta}\right)\right] + N_S\ \lambda\cos\Theta\ e\left(\frac{-d}{\lambda\cos\Theta}\right)} \qquad (6)$$

$$R_{calc.} = \frac{A(\Theta)[S]}{A(\Theta)[In]} = \left[\frac{N_{L(In)}}{N_{L(S)}} + \frac{N_{S(In)}}{N_{L(In)}}\frac{1}{\left[e\left(\frac{d}{\lambda\cos\Theta}\right) - 1\right]}\right]^{-1} \qquad (7)$$

The theoretical $R_{calc.}$ values are fitted to those measured experimentally for different "Θ", the fitting parameter being the thickness d of the overlayer.

ANNEXE II

CAPACITANCE-VOLTAGE RELATIONSHIPS FOR AN IDEAL MIS CAPACITOR

Analysis based on exact charge distribution in an ideal MIS capacitor yields the following equations. The capacitance of the MIS structure is given by

$$C = \frac{C_{nit}}{1+\left(\frac{\varepsilon_0 W_{eff}}{\varepsilon_s x_0}\right)} \qquad (1)$$

where, C is the equivalent capacitance of the MIS structure at any bias V_G, C_{nit} the insulator (nitride) capacitance, ε_o and ε_s are the dielectric constants of the insulator and the semiconductor, x_o the insulator thickness and W_{eff} is the effective width of the semiconductor in units of the Debye length L_D that contributes to the silicon surface capacitance and W_{eff} for accumulation, flat band and depletion/inversion is given by

$$W_{eff} = \begin{cases} \hat{U}_s L_D \left[\dfrac{2F(U_S,U_F)}{e^{U_F}(1-e^{-U_S}) + e^{-U_F}(e^{U_S}-1)}\right] & \text{---- accumulation} \\ \dfrac{\sqrt{2}L_D}{(e^{U_F}+e^{-U_F})^{1/2}} & \text{---- flat band} \\ \hat{U}_s L_D \left[\dfrac{2F(U_S,U_F)}{e^{U_F}(1-e^{-U_S}) + \dfrac{e^{-U_F}(e^{U_S}-1)}{(1+\Delta)}}\right] & \text{---- depletion/inversion} \end{cases} \qquad (2)$$

$$\hat{U} = \begin{cases} +1 & \text{if } U_S>0 \\ -1 & \text{if } U_S<0 \end{cases} \quad \text{and} \quad L_D = \left[\frac{\varepsilon_S \varepsilon_0 kT}{2q^2 n_i}\right]^{1/2}$$

where, $\hat{U}_s$ gives the sign of the equation, L_D the Debye length, U_S and U_F are the surface potential (ϕ_S) and bulk potentials (ϕ_b) normalized to kT/q, n_i the intrinsic

carrier concentration, $F(U_S,U_F)$ is the dimensionless field at the semiconductor surface and Δ represents the ac fluctuation of the inversion charge in response to the applied signal. Δ for the high frequency limit is given by

$$\Delta = \frac{\dfrac{(e^{U_S}-U_S-1)}{F(U_S,U_F)}}{\displaystyle\int_{0^+}^{U_S} \frac{e^{U_F}(1-e^{-U})(e^{U}-U-1)}{2F^3(U,U_F)}du} \qquad (3)$$

where $F(U,U_F)$ is the dimensionless field at any potential U in the semiconductor is given by

$$F(U,U_F) = \left[e^{U_F}(e^{-U} + U - 1) + e^{-U_F}(e^{U} - U - 1)\right]^{1/2} \qquad (4)$$

and the field at the surface is given by

$$F(U_S,U_F) = F(U = U_S,U_F) \qquad (5)$$

and the variation of the surface potential U_S with gate voltage V_G is given by

$$V_G = \frac{kT}{q}\left[U_S + \hat{U}_S \frac{\varepsilon_S x_0}{\varepsilon_0 L_D} F(U_S,U_F)\right] \qquad (6)$$

The theoretical C-V curve is plotted by varying U_S and calculating C and the corresponding V_G. The equations are valid only for p-type semiconductor, n-type characteristics can be obtained by simply changing the sign of the computed V_G values.

ANNEXE III

SMALL PULSE MIS DLTS ANALYSIS

The small signal MIS DLTS analysis is presented here. Determination of the properties of interface traps that are distributed in a continuous fashion in the band gap with different capture cross-sections and activation energies is more complicated than discrete bulk traps [102]. A modified small pulse version is therefore used. The MIS diode is biased at a constant surface potential V_S under depletion conditions and a small signal injection pulse is applied to fill the interface states in a narrow energy range ΔE_F with majority carriers. When the pulse is removed, the Fermi level returns to its original value with the emission of trapped carriers from the interface states resulting in a capacitance transient.

The capacitance difference ΔC between two gating times, t_1 and t_2 which is the DLTS signal is given by

$$\Delta C = A \int_{E_v}^{E_c} N_s(E)\left[\exp\left(-\frac{t_1}{\tau_n}\right) - \exp\left(-\frac{t_2}{\tau_n}\right)\right] x\,[f_0(E) - f_1(E)]\, dE \qquad (1)$$

where $N_s(E)$ is the surface state density at energy E, τ_n is the emission time constant of electrons, f_0 and f_1 are the electron occupation probability of the surface states when the surface potential is V_S and V_S-$\Delta E_F/q$ respectively and are given by

$$f_0(E) = \left[1 + \exp\left(\frac{E - E_F}{kT}\right)\right]^{-1} \qquad (2)$$

$$f_1(E) = \left[1 + \exp\left(\frac{E - E_F + \Delta E_F}{kT}\right)\right]^{-1} \qquad (3)$$

When the pulse height is small, $f_1(E) - f_0(E)$ can be regarded as a δ function $\delta(E-E_t)$ and the trap energy is $E_t = E_F + \frac{1}{2}\Delta E_F$ and the equation for ΔC reduces to

$$\Delta C = AN_S(E_t)\left[\exp\left(-\frac{t_1}{\tau_n(E_t)}\right) - \exp\left(-\frac{t_2}{\tau_n(E_t)}\right)\right] \quad (4)$$

The expression now resembles that of a discrete trap level. Thus the conventional analysis ia applied [101]. The DLTS spectrum has a peak at

$$\tau_n = \frac{t_2 - t_1}{\ln(t_2/t_1)} \quad (5)$$

The emission time constant τ_n is given by

$$\tau_n = [v_{th}N_c\sigma_n \exp(-\Delta E_t/kT)]^{-1} \quad (6)$$

where v_{th} is the thermal velocity of electrons, N_c the effective density of states in the states in the conduction band, σ_n the capture cross section for electrons and ΔE_t is the activation energy given by

$$\Delta E_t \equiv E_c - E_t = qV_s + qV_F - \tfrac{1}{2}\Delta E_F \quad (7)$$

where V_F is the bulk potential of the semiconductor and V_s is the surface potential that can be measured from capacitance - voltage experiments for a given temperature. The capture cross-section σ_n can be expressed as

$$\sigma_n = \sigma_0 \exp(-\Delta E_\sigma/kT) \quad (8)$$

Where σ_0 and ΔE_σ are constants inherent to the level. Since different interface states at different energies have different σ_0 and ΔE_σ

$$\sigma_n(E_t,T) = \sigma_0(E_t) \exp(-\Delta E_\sigma(E_t)/kT) \quad (9)$$

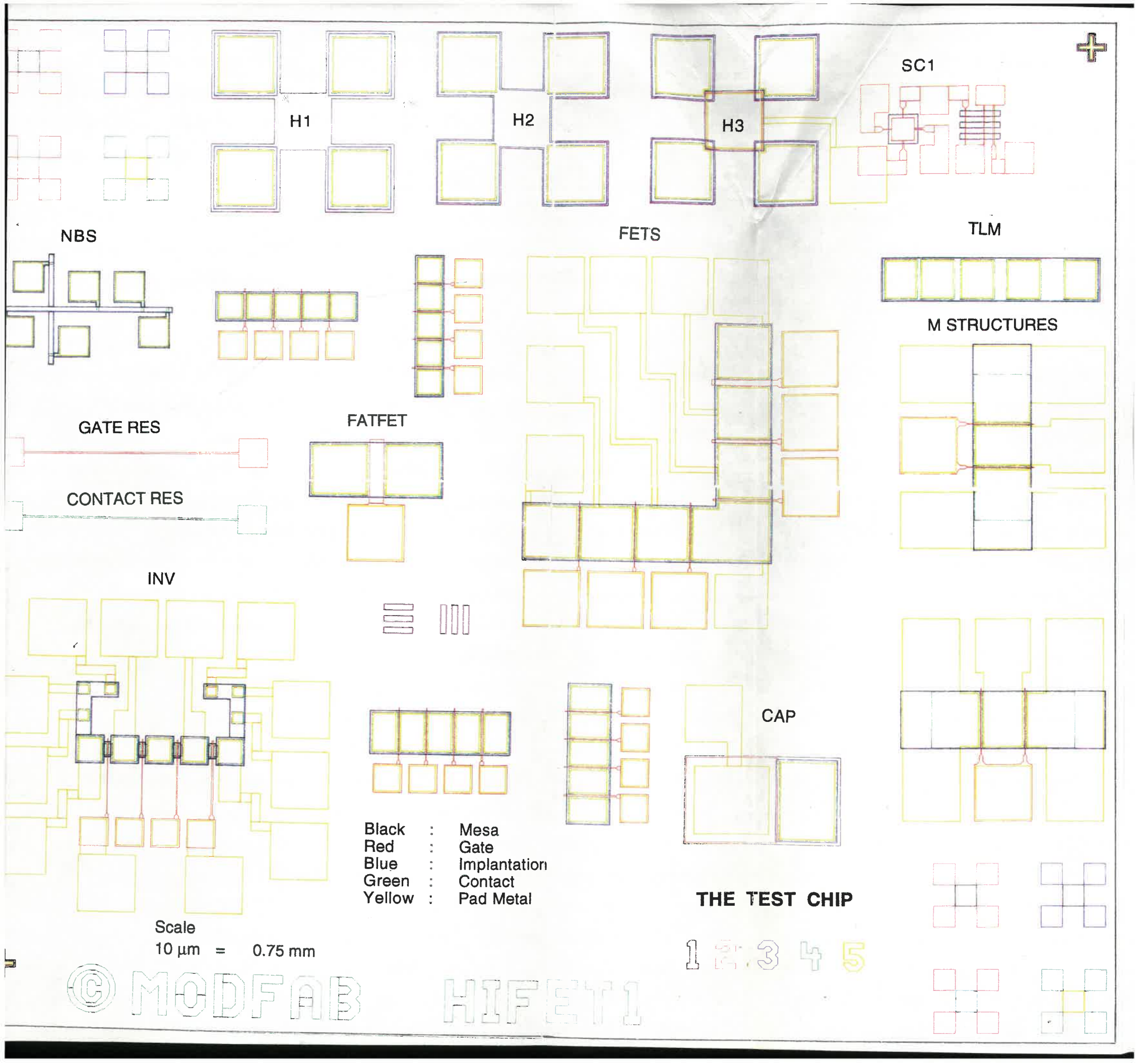
When shallow impurities are dominant in the bulk, N_c is given by

$$N_c = N_D \exp(qV_F/kT) \quad (10)$$

Substituting eqs.(7),(9)& (10) into eq. (6) yeilds

$$\tau_n = (v_{th} N_D \sigma_0(E_t) \exp\{-[\Delta E_0(E_t) + qV_s - \tfrac{1}{2}\Delta E_F]/kT\})^{-1} \quad (11)$$

Thus the slope of the Arrhenius plot, ln τ_n vs T^{-1}, gives the term in the exponent , the apparent activation energy. To determine $\Delta E_\sigma(E_t)$, we deduce the surface potential V_s from C-V measurements at different temperatures. The intercept gives the capture cross-section $\sigma_0(E_t)$.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