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UNIVERSITE DE MONTREAL

TRANSIENT FREE SWITCHING OF CAPACITOR BANKS

par

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ECOLE POLYTECHNIQUE

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Ce rapport de projet intitulé

TRANSIENT FREE SWITCHING OF CAPACITOR BANKS

présenté par: Gordon P. MACK

en vue de l'obtention du grade de: M. Ing.

a été dûment accepté par le jury d'examen constitué de:

M. Georges-Emile April, M. Sc.

M. Guy Olivier, Ph.D., directeur de projet

SOMMAIRE

Le but de cette étude est de démontrer qu'il est possible de commuter des banques de condensateurs sans transitoires. Six topologies différentes de commutateur triphasés à thyristor ont été analysées au moyen de la transformé de Laplace. Par la suite quatre de ces six topologies ont été mises à l'essai au laboratoire avec une charge de 7 kvar. Dans chaque cas, la banque de condensateur a été commutée avec succès sans aucune transitoire de courant. La conclusion le plus importante de cette étude est la suivante: les thyristors, qui constituent les éléments principaux des commutateurs, doivent être amorcés seulement quand la tension à leurs bornes est nulle. De plus, il a été démontré que des banques de condensateurs peuvent être commutées sans transitoires à l'aide d'un commutateur constitué de seulement trois thyristors.

ABSTRACT

The purpose of this study was to demonstrate that it is possible to switch banks of capacitors without transients. Six different configurations of three phase thyristor switches were analyzed using Laplace Transforms. Subsequently, four of the six configurations were tested in the laboratory, with a 7 kvar load. In each case the capacitor bank was successfully switched without inrush currents. The most important conclusion of this study is this: the thyristors, of which the thyristor switch is composed, should only be fired when the voltage across them is zero. Furthermore, it was demonstrated that transient free switching could be achieved with a thyristor switch made with only three thyristors.

ACKNOWLEDGEMENTS

There are many people who have encouraged and supported me throughout these last ten months. I would now like to thank them publicly.

Guy Olivier has surpassed all my expectations of what a supervisor could be. I began my masters with the notion that supervisors were often the modern day equivalent of slave drivers, Guy has been anything but. He has been a good friend and an excellent teacher, so much so that many things that I had "learned" in the past finally started making sense after I began working with Guy. His manner with students is exemplary if not remarkable; how Guy manages to service so many interrupts without losing synchronism or his sense of humour baffles me - maybe he operates at a higher clock rate than the rest of us.

I am really thankful that the project required me to work in the lab, for it is there that I got to know Stephane Poulin and Daniel Lefebvre. Apart from giving me timely technical advice, they were a tremendous moral support, sympathizing with me when my circuits and software were plagued with bugs and celebrating with me when things worked. They both are quick with a joke, and although it meant that I always had to beware of booby traps, it made for a great work atmosphere.

Other members of the Polytechnique family that deserve special recognition are Rosaire Deslierres and Jean-Luc Sheink, who do much to cultivate good relations within the section (even with anglophones), and my fellow graduate students Ngandui Eloi and Mohand Ouhrouche who have taken an interest in me and my work.

My own family's support should not go unmentioned. For years now they have given me much love and encouragement, which in turn has given me the confidence to take on new challenges. My parents deserve a special thanks for they have been loving mentors; the fact that I am an engineer is due in large part to my desire emulate my father.

This masters has required a fair amount of sacrifice. Unfortunately I have not been the one who has had to bear most of the sacrifice. That lot fell on my fiancé Anne. She has come to realize that when people refer to me as her "futur", it is because I can't be her "present" because I have to go off and work in the lab. Certainly, I do regret that this project has taken longer than I expected, because it has often meant that I have not been able to do what I enjoy most, spend time with Anne.

Finally, it is exciting to realize that I have learned a tremendous amount here at Polytechnique and that I can now embark on new ventures a little "moins niaiseux" than when I came.

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INTRODUCTION

Switching banks of capacitors in and out of power systems is becoming increasingly common, largely because there is a growing interest in reactive power control. High energy prices coupled with the difficulties in extending transmission networks due to high interest rates and the occasional problems in obtaining right of way oblige utilities to look for ways to operate existing power systems more efficiently. Reactive power control is one such scheme that enables the system to operate at or very near unity power factor.

Reactive power control is based on the fact that when the reactive power demanded by the load is supplied locally the generating source need only produce the real power demanded. Consequently losses can be reduced by minimizing the total flow of reactive power.

However most industries constitute inductive loads and as result operate at lagging power factor. Because of the high cost of supplying reactive power most utilities penalize customers if their power factor falls below a fixed value. The purpose of penalty tariffs for low power factor is to encourage industry to share the power utility's

enthusiasm for reactive power control, or as it is more commonly referred to, power factor correction.

There are different ways that the vars can be supplied at the load. Synchronous condensers were common in the past but increasingly power capacitors are becoming the preferred choice. The demise of PCBs during the 1970's resulted in a considerable amount of research into capacitor technology and subsequently several important advances. As a result, it is now possible to install large, reliable and highly efficient banks of capacitors in a relatively small space and at a modest price.

Power capacitors connected in shunt are usually installed in one of three ways: as fixed capacitance connected directly across the load; in banks of capacitors which can be switched into or out of a particular system or as part of a continuously controlled static compensator usually called a TSC (Thyristor Switched Capacitor).

Whether the capacitors are installed in a fixed, switched or continuously controlled configuration will depend mostly on the type of compensation involved. In load compensation the objectives [4] are such that one can afford a slower response, so either fixed or switched capacitance will normally be sufficient. However, in transmission compensation the speed of response is critical so switched or preferably continuously controlled capacitors are used.

Capacitors have traditionally been switched using mechanical contactors. The most serious problem which results is that of switching transients, otherwise known as in-rush currents. The transients occur whenever there is a potential difference between the load and the source voltages at the moment that the switch is closed. Because contactors, by their very construction, are closed in a random fashion one cannot predict the magnitude of the transient that will result. Frequently they can exceed 10 pu. [3] and the resulting wear is such that the switching life of the contactor is quite limited.

The second drawback of mechanical contactors is that they are slow. The fastest available mechanical switches [4] take 2 cycles to close or open whereas the more conventional capacitor switches can take anywhere between six and thirty cycles.

Replacing conventional mechanical contactors with three phase thyristor switches would solve both these problems. The fact that thyristors can be "turned on" almost instantaneously (0.9 μsec) means that the response would be less than 2 cycles and better still, it means that the capacitor bank could be switched in without transients. Appendix A explores in greater detail the subject of reactive power control and the use of thyristor switched capacitors.

The objectives of this project are two-fold:

1) Demonstrate that it is possible to switch banks of capacitors without transients using thyristors.

2) Conduct a preliminary characterization study of suitable three phase thyristor switches.

The research was pursued through three different stages. The first was a review of currently available literature. This was carried out primarily at CISTI (Canadian Institute for Scientific and Technical Information) in Ottawa. The second stage was that of the theoretical analysis. The different thyristor configurations were analyzed using Laplace transforms. The final stage was one of experimentation in the laboratory to ensure that our calculations were correct.

The report is divided into nine chapters. Chapter one provides preliminary information helpful in understanding the work that follows. Chapters two through eight present the six different three phase thyristor switches as well as the single phase thyristor switch. Chapter nine is a discussion of the results and a comparison of the different configurations.

CHAPTER ONE

PRELIMINARY INFORMATION

1.1 - Literature Review

There is very little published information on the use of ac controllers in switching banks of capacitors since most of the literature concerning ac controllers focuses on ways to control R-L loads (i.e. induction motors, heaters etc.). Of the dozen or so publications concerning thyristor-switched capacitors, most approach the problem from the utility's perspective, namely: how can one improve the power system's performance? To our knowledge there are two publications [1], [2] which approach the problem of switching banks of capacitors from an industrial perspective, namely: what is the most economical solution? However, while these texts give a very comprehensive treatment of the capacitor aspects of the problem, they tend to give only a cursory treatment of the power electronic aspects.

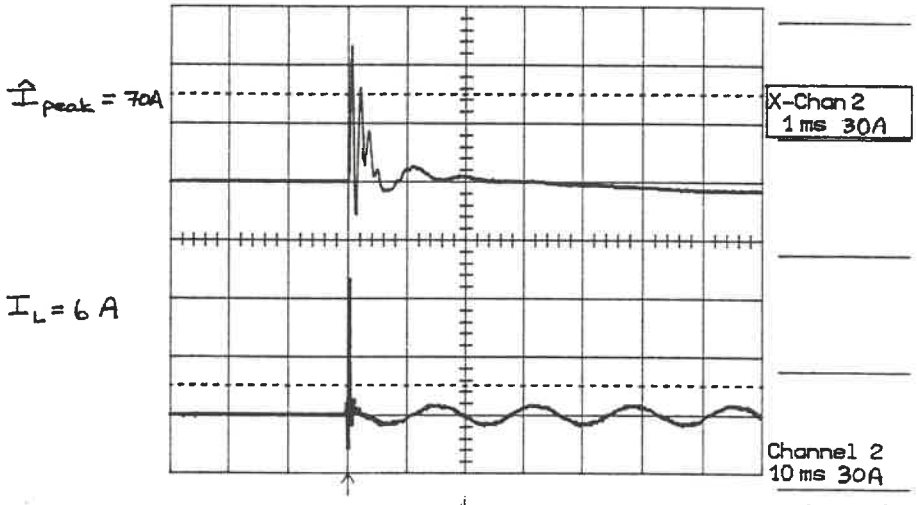
When actual thyristor configurations are presented in the literature the accompanying analysis usually only describes the single phase controller or at best the three-phase controller in delta, which is simply three single phase controllers joined together. To my knowledge there is no publication which details how capacitor banks

can be switched with less than six thyristors. One can, nonetheless, glean some information from the literature.

Generally it is agreed that the ideal instant for transient-free switching is when $dv_s/dt = 0$ and $V_{Ca} = v_s(0)$. This implies that the capacitors are charged to the peak voltage and that the thyristors are only gated when the source voltage peaks. Consequently the thyristors begin conducting at the instant that the current passes through zero. However, if the thyristors are fired at any instant other than when the source voltage equals the load voltage, switching transients will result. It is therefore critical to monitor the voltage across the thyristor switch and to only fire the thyristors when the voltage across the thyristors passes through zero. This switching condition is derived in chapter two.

In order to quantifiy the seriousness of the problem we decided to reproduce switching transients in the single phase case. This was accomplished by delaying the thyristor firing signal. Plot 1.1 shows the in-rush currents, in excess of 11 p.u., which occurred when the thyristors were fired 30 electrical degrees after the voltage across the thyristors passed through zero. The switching transients got worse as this delay was increased. In the event that the capacitors were discharged the most serious transients would occur if the thyristors were fired when the source

voltage was at its peak. However, even worse transients could be expected if the capacitors were left fully charged to the negative peak voltage and the thyristors were then fired when the source was at its positive peak voltage. With conventional switch gear it is possible that this situation could occur periodically.



Plot 1.1 In-rush currents in a single phase circuit; load = 130μF, thyristors are fired 30° after zero-crossing

Switching transients can shorten the life of both the capacitor bank and the switching apparatus. In the case of thyristor switches the thyristors can be destroyed if the di/dt of the in-rush currents exceed the thyristor ratings. Traditionally there have been two solutions to the problem of switching transients. The first solution, a pre-charger, is rather elaborate and requires that the capacitors be pre-charged to their peak value of the source voltage. In a sense, this method attempts to create the ideal conditions for switching since the resulting current will

be zero if the thyristors are fired when the source voltage passes through its peak. However, this solution is both costly and slow. The second solution consists of adding an inductance in series. The inductance is rated so that in the worst case the di/dt will still be less than what the thyristor is rated for. While simpler than the pre-charger solution, it would be better if the series inductance could be eliminated completely: this would be the case if the inherent inductance of the circuit could safely limit the di/dt.

Given the lack of information on ways in which thyristors can be used to switch capacitors, we felt it would be worthwhile to conduct a practical study examining different configurations of thyristors that could be used to switch banks of capacitors without transients. The questions we wanted to address included: 1) Is it possible to switch capacitors without transients? 2) Can the traditionally included series inductors and pre-chargers be eliminated? 3) What is the minimum number of thyristors that can be used to switch a three-phase capacitor bank?

1.2 - Description of Test Setup

Upon completion of the literature review the analysis stage began. The various results of the analysis stage are presented in chapters two through ten, so we will not dis-

cuss them here but rather jump ahead to look at how each configuration was tested in the laboratory.

The wiring diagrams for each of the tested configurations are given below (see Fig. 1.1). Each configuration has been named and coded. The names are slightly modified versions of the names that Shepherd gave to these configurations of ac controllers [3]. The codes, however, conform to the IEEE Standard P428/D2 entitled "Standard Definition and Requirements for Thyristor AC Controllers".[6] Relevant sections of this standard are included in Appendix C.

Note that W33AY and W33AD were not tested as they behave the same as W32AY and W32AD respectively.

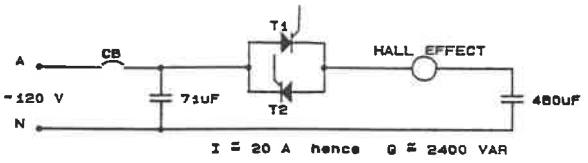


Fig. 1.1a The Single Phase AC Controller

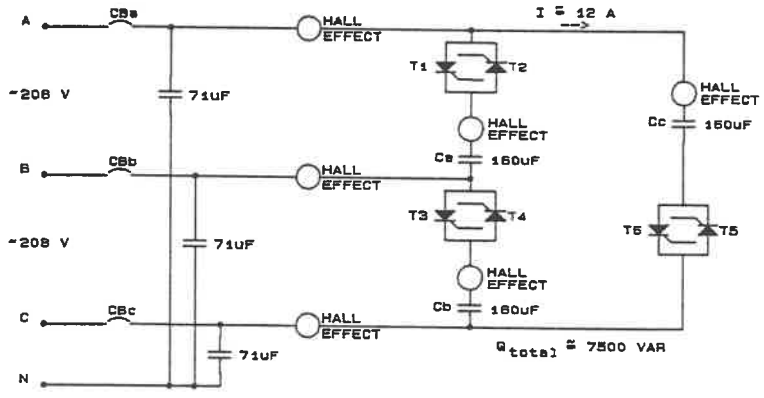


Fig. 1.1b The Three-Wire Branch-Controller with Delta-Connected Load, W33AA

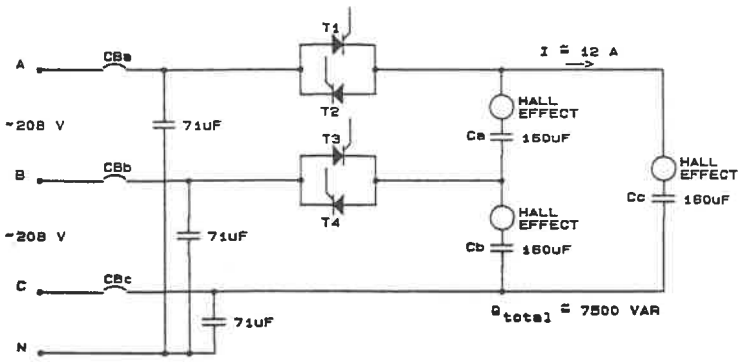


Fig. 1.1c The Three-Wire Asymmetrical Line-Controller with Delta-Connected Load, W32AD

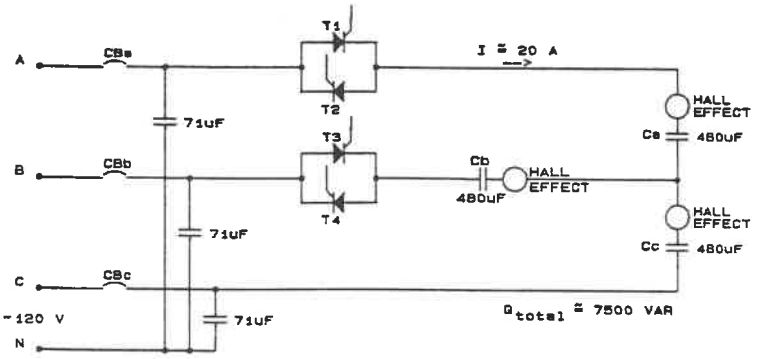


Fig. 1.1d The Three-Wire Asymmetrical Line-Controller with Wye-Connected Load, W32AY

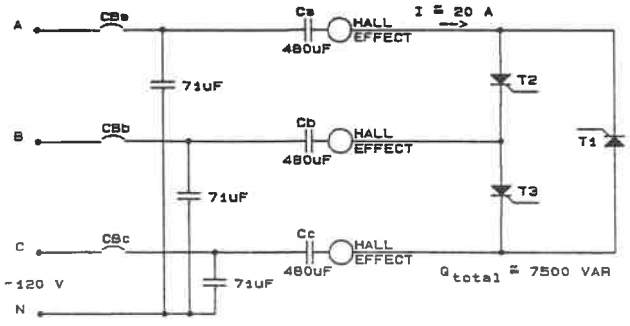


Fig. 1.1e The Three-Wire Neutral Point-Controller with Wye-Connected Load, U33DA

A few explanations will help clarify why we chose these particular test setups.

1) The 71uF connected across the source was meant to ensure that if there were any transients, we would see them as this source capacitance would try to transfer any excess charge instantaneously to the load capacitance. We chose 71uF because that was the largest capacitance we could connect across each phase with the material we had available.

2) The thyristors used in the experiment are International Rectifier, 50RIA Series, 80 A rms. Each thyristor was mounted on its own heatsink and has its own snubber (R=15 Ω, C=1uF). The thyristor specifications are given in Appendix E.

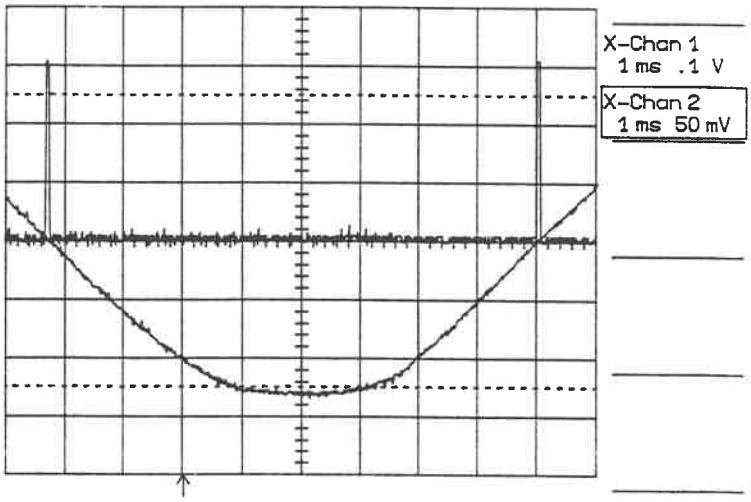
3) The thyristors are fired by means of a fibre optic gate amplifier circuit developed by Ecole Polytechnique. The signal to gate the thyristor is basically the output of a two input AND gate where INPUT 1 is the 'Turn-on' signal and INPUT 2 is the output of the zero crossing detector circuit (see Plot 1.2). The circuit diagram for the logic circuits is given in Appendix F.

4) The use of fibre optic triggered gate amplifiers was necessary since the opto-thyristors, which we initially used to fire the thyristors, introduced delay thus causing switching transients.

5) The current is monitored by means of Hall Effect current sensors.

6) The source voltage is governed by the ac controller configuration (i.e. W33AD requires V_{LL} whereas W33AY requires V_{LN}).

7) The load varies according to the line current. As the circuit breaker was rated for 20 A, the load would either be 480uF or 160uF so as to ensure the maximum line current.



Plot 1.2 Output from the zero-crossing detector

CHAPTER TWO

THE SINGLE PHASE AC CONTROLLER USED AS A SWITCH:

2.1 - Introduction

Having completed a review of published literature, the analysis stage began. It consisted of analyzing, by means of Laplace Transforms, the various equivalent circuits for each configuration. The analysis of the single phase case is very helpful in understanding subsequent analyses of three phase circuits since many of the results found in the single phase case can be applied directly.

It is worth noting that the experimental results for the single phase case are presented later in this chapter. It was felt that for the sake of clarity the experimental results of each configuration should be presented in the same chapter as the configuration's analysis.

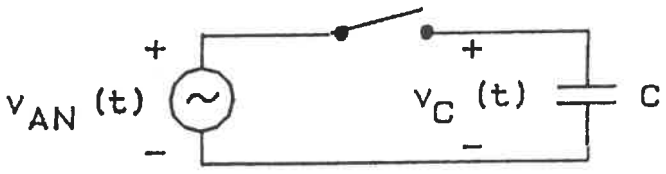


Fig. 2.1 An equivalent circuit for a Single Phase AC Controller with a capacitive load.

2.2 - Analysis of a Single Phase AC Controller

Given that the sinusoidal ac supply voltage is:

$$V_s = V_{max}\sin(\omega_o t + \alpha)$$

The corresponding Laplace transform is (see Appendix D for derivation):

$$L\{V_s\} = V_{max}\left(\frac{s\cdot\sin\alpha + \omega_o\cdot\cos\alpha}{s^2 + \omega_o^2}\right)$$

Using the circuit of Fig. 2.1, we see that after the switch has been closed, Kirchhoff's voltage law requires that:

$$V_s = \frac{1}{C}\int_0^t i\ dt + v_c(0^-)$$

Transforming this equation into the s-domain and solving for I(s) yields:

$$I(s) = C\left[V_{max}\left(\frac{s^2\cdot\sin\alpha + \omega_o s\cdot\cos\alpha}{s^2 + \omega_o^2}\right) - v_c(0^-)\right]$$

[eq. 2.1]

After ensuring that all factors of the equation are expressed as proper rational polynomials (i.e. the denominator is of a higher order than the numerator) we can find the Inverse Laplace Transform:

$$i(t) = L^{-1}\{I(s)\}$$

$$= C\{\ V_{max}\sin\alpha - v_c(0^-)\ \}\ \delta(t) + C\omega_o V_{max}\cos(\omega_o t + \alpha)$$ [eq. 2.2]

This equation shows that the optimal moment for firing the thyristors is when the voltage across the thyristor switch is zero, namely when $V_{max}\sin\alpha = v_c(0^-)$. It is possible to switch the capacitor in without transients at this instant because the impulse component of the current expression is zero.

With an understanding of how thyristor switches open, one can predict the final conditions of the system. The thyristors block after the gate triggering signals have been removed, and the current flowing through their anode declines to zero. Since the current in a capacitor leads the voltage by 90°, the current passes through zero when the voltage is at its peak value V_{max}. In other words, whenever the switch is opened the capacitor is left charged to its maximum value.

2.3 - Predictions of Circuit Behavior:

With this information we can predict how the circuit will perform in the stages of operation that interest us: 1) switching in a discharged capacitor; 2) switching out the capacitor; 3) switching in the charged capacitor.

1) SWITCHING IN A DISCHARGED CAPACITOR:

Thyristors should be gated at $V_c = v_s(0^-) = 0$

(i.e. when the voltage across the thyristors is zero)

Corresponding current $i(t) = C\omega_o V_{max} \cos(\omega_o t + \alpha)$

2) SWITCHING OUT THE CAPACITOR:

Thyristor stops conducting at $i_c(t) = 0$

resulting capacitor voltage $V_c = \pm V_{max}$

3) SWITCHING IN CHARGED CAPACITOR:

Thyristors should be gated at $V_c = v_s(0^-) = V_{max}$

(i.e. when the voltage across the thyristors is zero)

Corresponding current at $i(0^+) = 0$

2.4 - Computer Plots of Expected Circuit Behavior:

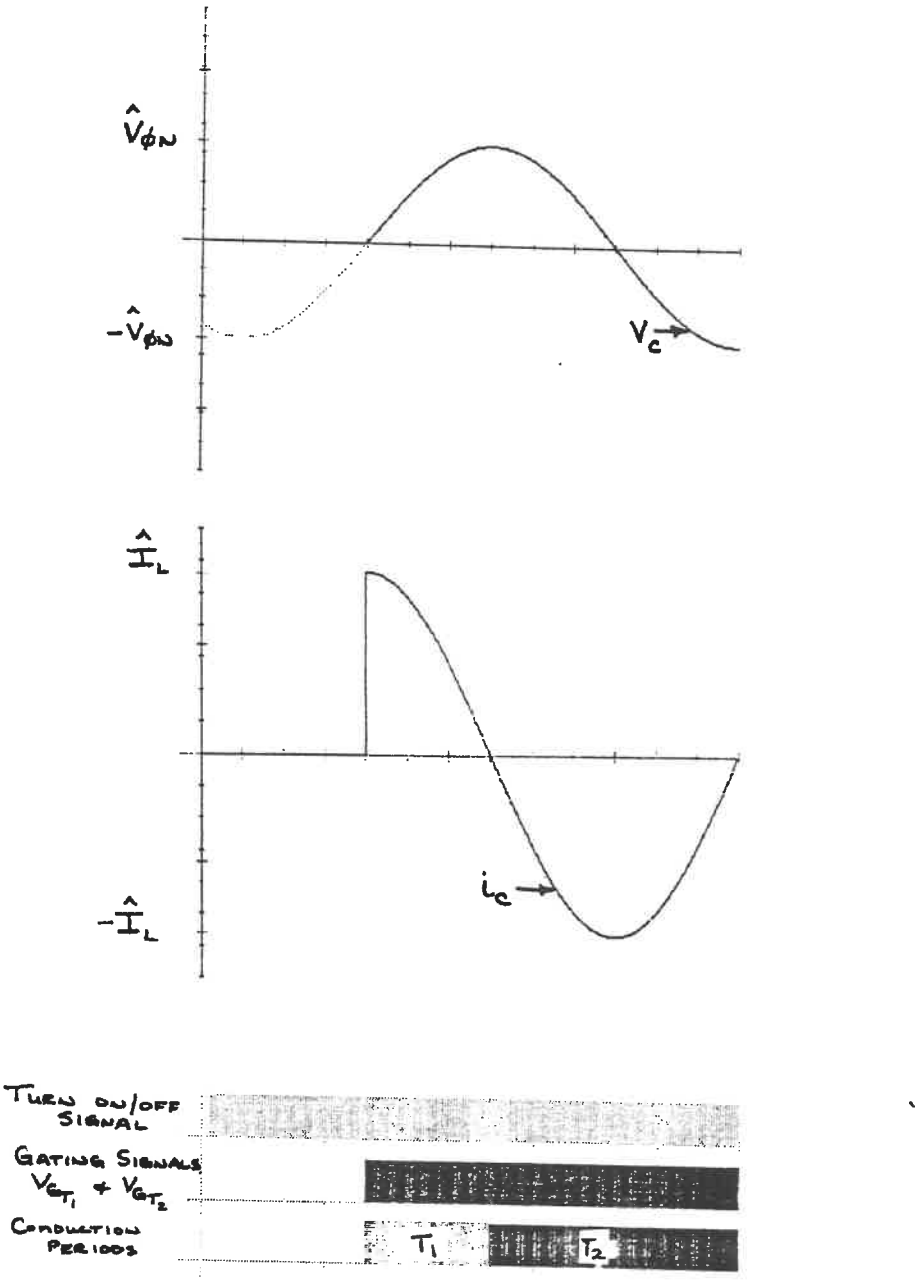


Fig. 2.2 Switching in the Single Phase AC Controller with the capacitor discharged

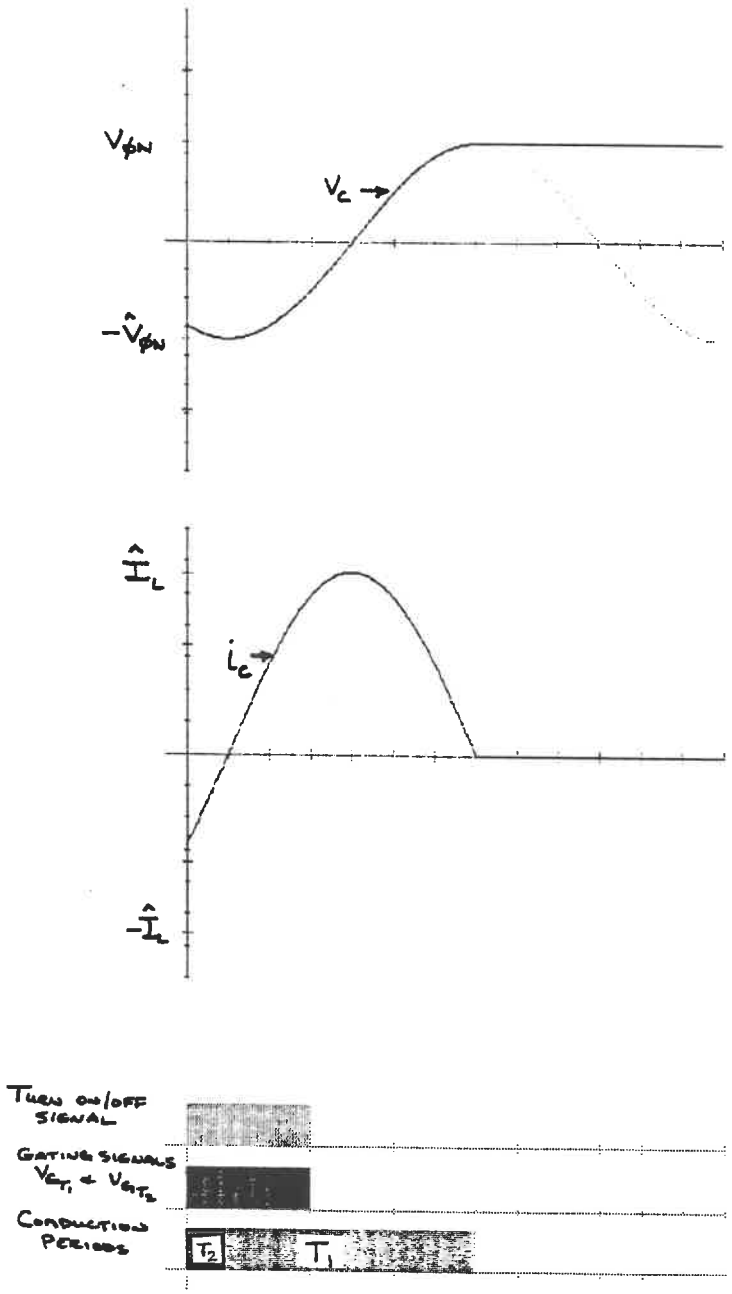


Fig. 2.3 Switching out the Single Phase AC Controller

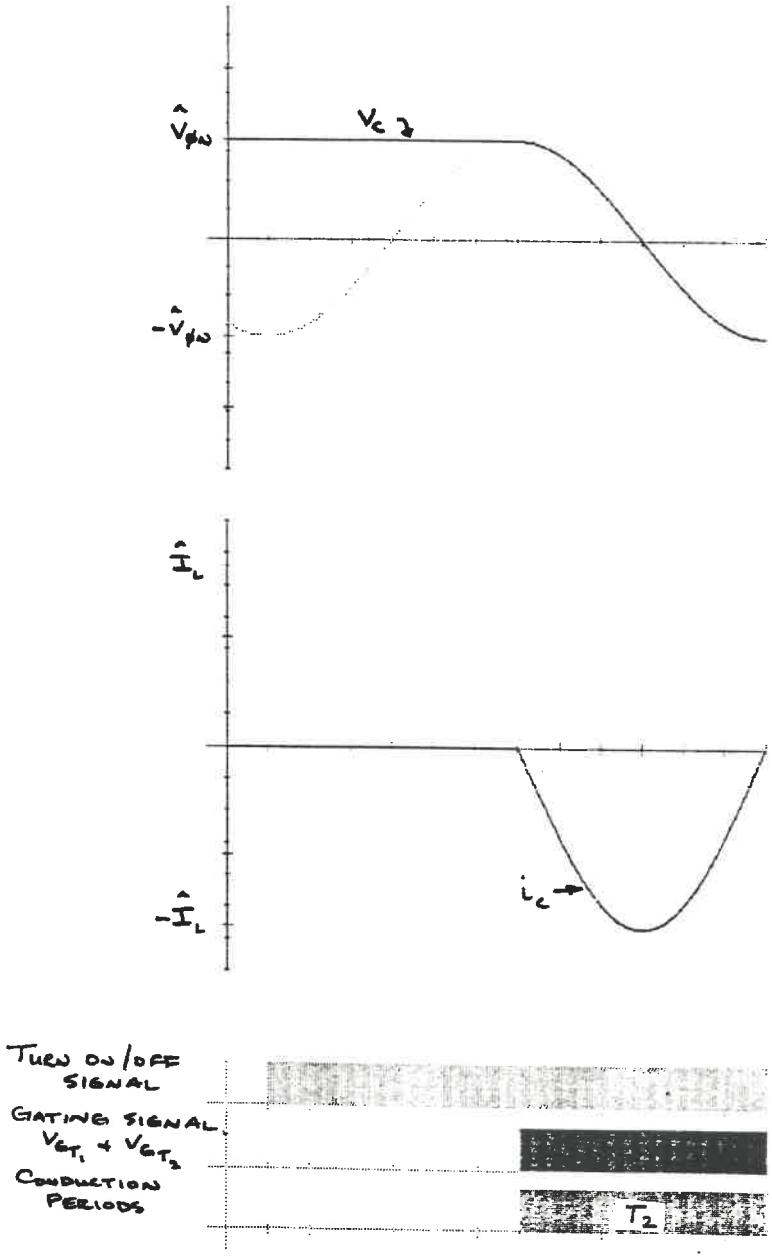
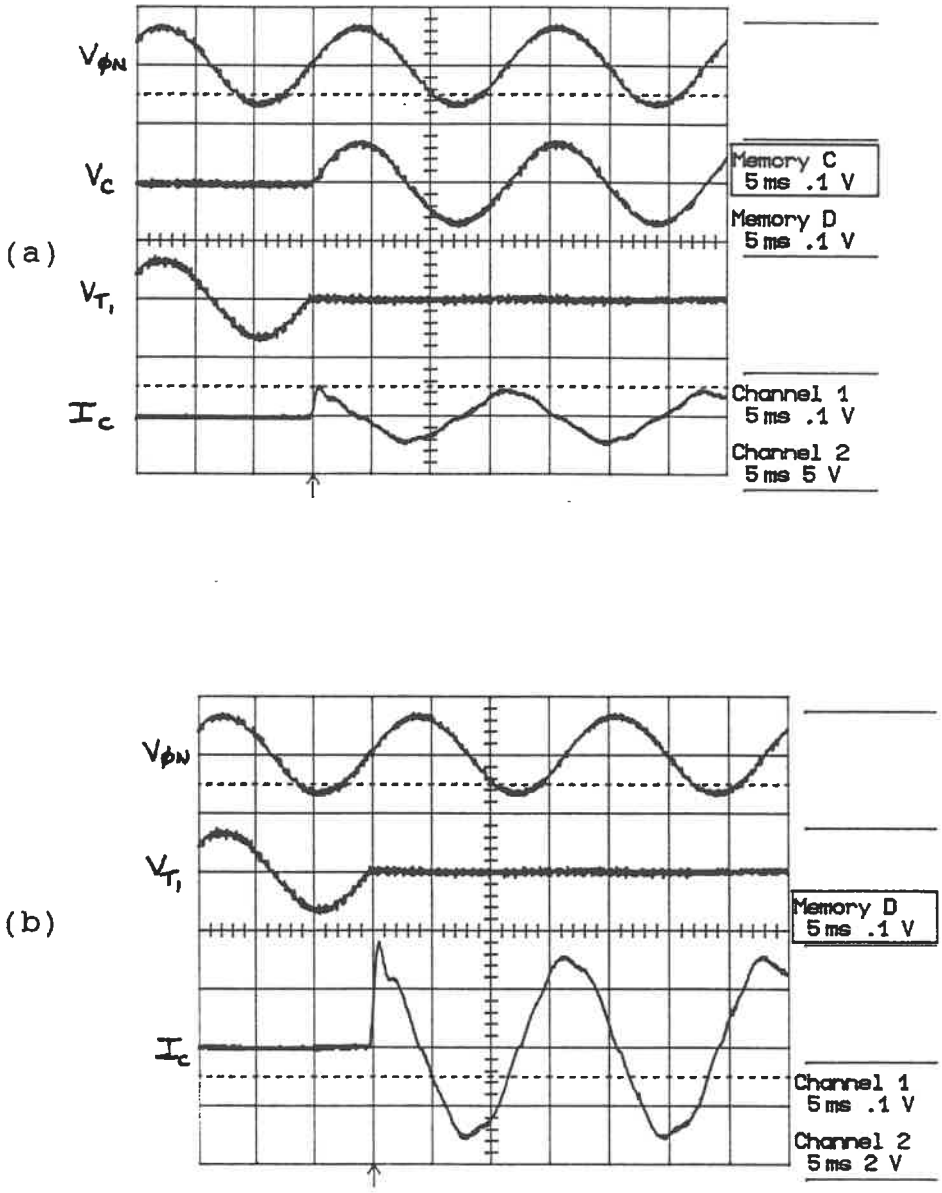
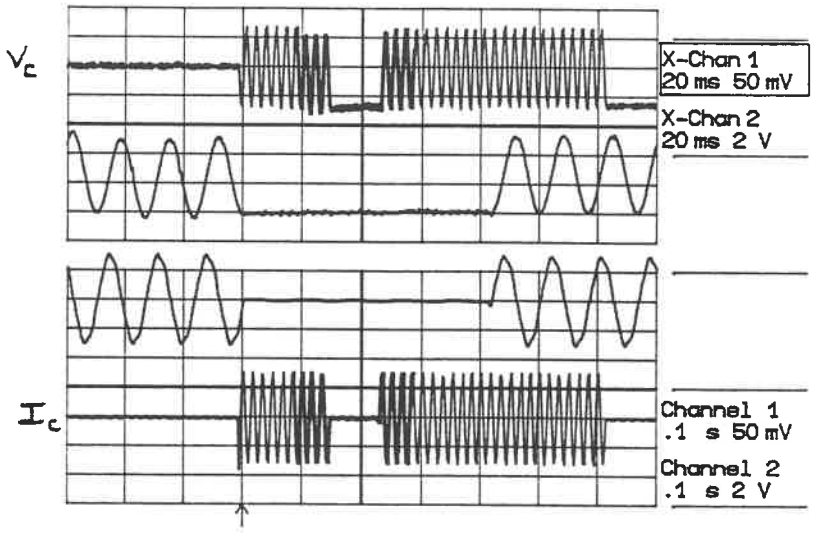


Fig. 2.4 Switching in again the Single Phase AC Controller with capacitor fully charged

2.5 - Experimental Results:



Plot 2.1 Switching in the Single Phase AC Controller with the capacitor is discharged. (a) Oscillogram including the voltage across the thyristors; (b) Oscillogram showing a magnified current waveform.
$V_{\Phi N}$=120V, I_C=21A



Plot 2.2 Switching in, out and in again the Single Phase AC Controller. The two centre traces are the magnification of the highlighted portions of V_c and I_c.
$V_{\Phi N}$=120V, I_C=21A

CHAPTER THREE

THREE-WIRE BRANCH-CONTROLLER WITH DELTA-CONNECTED LOAD:

3.1 - Introduction:

In this configuration, three separate switches must be closed before the capacitive load is fully connected to the source. Hence we have three different cases to analyse in order to determine how this configuration behaves.

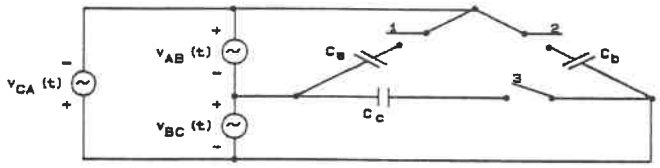


Fig. 3.1 Circuit diagram of a Three-Wire Branch-Controller with a Delta-Connected Load

3.2 - Analysis:

Case a: Close switch 1

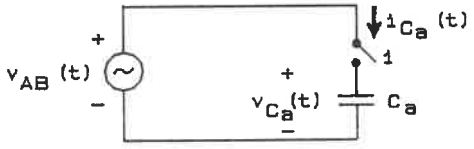


Fig. 3.2 Equivalent circuit of case a where switch 1 is closed

The equivalent circuit of this case is shown in Fig. 3.2. By analogy with the single phase circuit we can write directly:

$$i_{AB}(t) = C_a\{V_{ABmax}\sin\theta_{AB} - v_{Ca}(0^-)\}\delta(t) + C_a\omega_o V_{ABmax}\cos(\omega_o t + \theta_{AB})$$

where $V_{ABmax} = \sqrt{3}V_{ANmax}$ and $\theta_{AB} = \alpha_A + 30°$

hence

$$i_{AB}(t) = C_a\{\sqrt{3}\cdot V_{ANmax}\sin(\alpha_A + 30°) - v_{Ca}(0^-)\}\delta(t) + C_a\omega_o\sqrt{3}\cdot V_{ANmax}\cos(\omega_o t + \alpha_A + 30°)$$

Condition to switch without transients:

$$V_{ABmax}\sin\theta_{AB} = v_{Ca}(0^-)$$

This shows that switch 1 should be closed when the voltage across it is zero.

Case b: Close switch 2

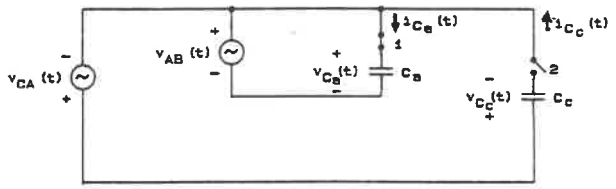


Fig. 3.3 Equivalent circuit of case b where switch 2 is closed while switch 1 remains closed

The equivalent circuit of this case is shown in Fig. 3.3. As both loops are independent, this case can be viewed as two independent single phase ac circuits.

The current in the inner loop remains unchanged from the steady state current of case a. Hence

$$i_{AB}(t)=C_a\omega_o V_{ABmax}\cos(\omega_o t+\theta_{AB})$$

The current in the outer loop can be written directly by analogy with the single phase circuit:

$$i_{CA}(t) = C_c\{V_{CAmax}\sin\theta_{CA}-v_{Cc}(0^-)\}\delta(t) + C_c\omega_o V_{CAmax}\cos(\omega_o t + \theta_{CA})$$

where $V_{CAmax}=\sqrt{3}V_{Cmax}$ and $\theta_{CA}=\alpha_C+30°$

Condition to switch without transients:

$$V_{CAmax}\sin\theta_{CA} = v_{Cc}(0^-)$$

This shows that switch 2 should be closed when the voltage across it is zero.

Case c: Close switch 3

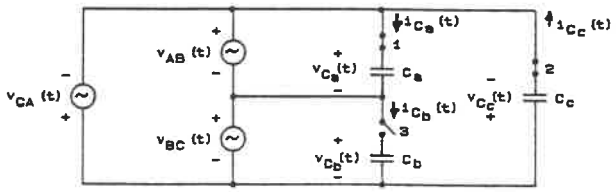


Fig. 3.4 Equivalent circuit of case c where switch 3 is closed while switches 1 & 2 remain closed

The equivalent circuit of this case is shown in Fig. 3.4. The parameter of interest to us is $i_{BC}(t)$ when switch 3 is closed. This can be found by writing the differential equation for the current flowing through C_b.

$$i_{BC}(t)=C_b\,dV_{BC}(t)/dt$$

where $V_{bc}(t)=V_{BCmax}\sin(\omega_o t+\theta_{BC})$

Transforming this equation into the s-domain yields:

$$I_{BC}(s)=C\left[V_{max}\left(\frac{s^2\cdot\sin\alpha\ +\ \omega_o s\cdot\cos\alpha}{s^2\ +\ \omega_o{}^2}\right)-v_c(0^-)\right]$$

As this is of the same form as eq. 2.1, we know that the time domain solution will be in the same form as eq. 2.2. Hence:

$$i_{BC}(t)\ =\ C_b\{V_{BCmax}\sin\theta_{BC}-v_{Cb}(0^-)\}\delta(t)$$
$$+\ C_b\omega_o V_{BCmax}\cos(\omega_o t\ +\ \theta_{BC})$$

where $V_{BCmax}=\sqrt{3}V_{BCmax}$ and $\theta_{BC}=\alpha_b+30°$

Condition to switch without transients:

$$V_{BCmax}\sin\theta_{BC}\ =\ v_{Cb}(0^-)$$

This shows that switch 3 should be closed when the voltage across it is zero.

3.3 - Predictions of Circuit Behavior:

With this information, we can predict how the circuit will perform in the stages of operation that interest us: 1) switching in a discharged capacitor; 2) switching out the capacitor; 3) switching in the charged capacitor.

1) SWITCHING IN A DISCHARGED CAPACITOR:

Thyristors should be gated when the voltage across them is zero.

Corresponding current $i(t)=\pm i_{max}$.

2) SWITCHING OUT THE CAPACITOR:

Thyristor stops conducting at $i_{\phi}(t)=0$.

Resulting capacitor voltages:

$V_{Ca} = \pm V_{ABmax} = \pm 294$ V

$V_{Cb} = \pm V_{BCmax} = \pm 294$ V

$V_{Cc} = \pm V_{CAmax} = \pm 294$ V

3) SWITCHING IN CHARGED CAPACITOR:

Thyristors should be gated when the voltage across them is zero.

Corresponding current: $i(0^{-})=0$.

3.4 - Computer Plots of Expected Circuit Behavior:

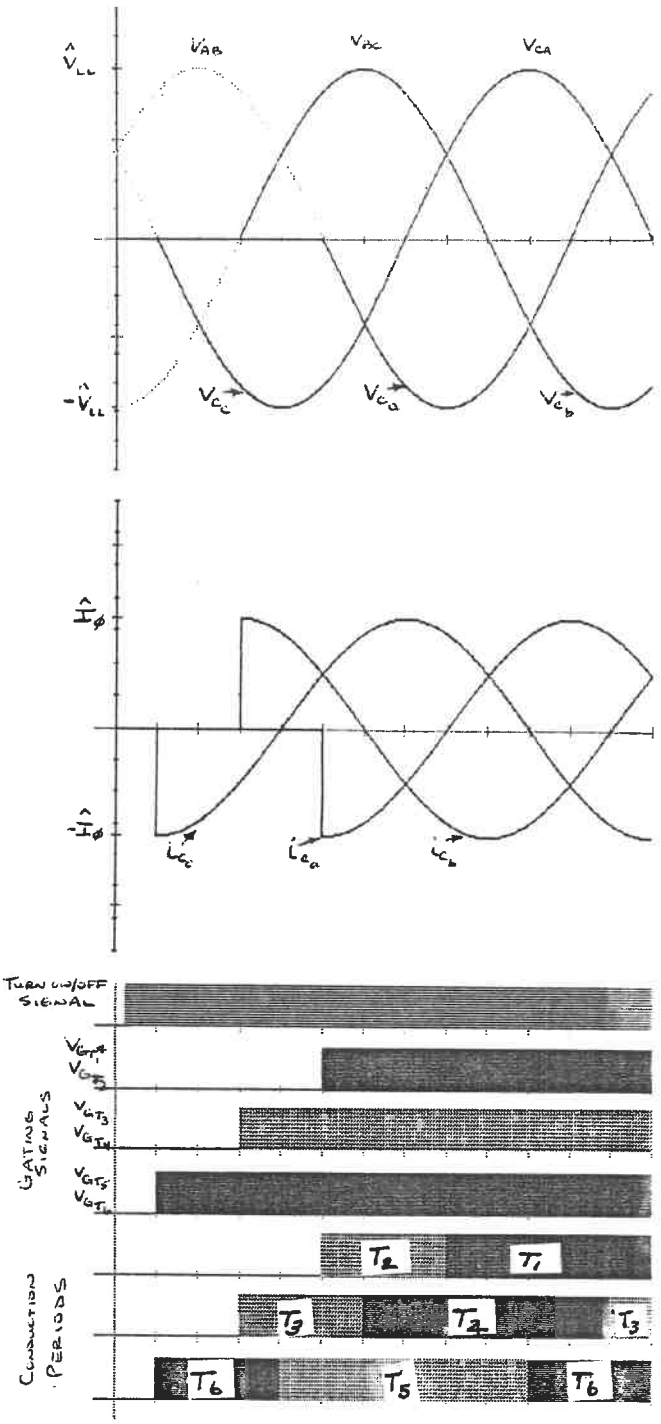


Fig. 3.5 Switching in a Three-Wire Branch-Controller with a Delta-Connected Load; the capacitors are discharged

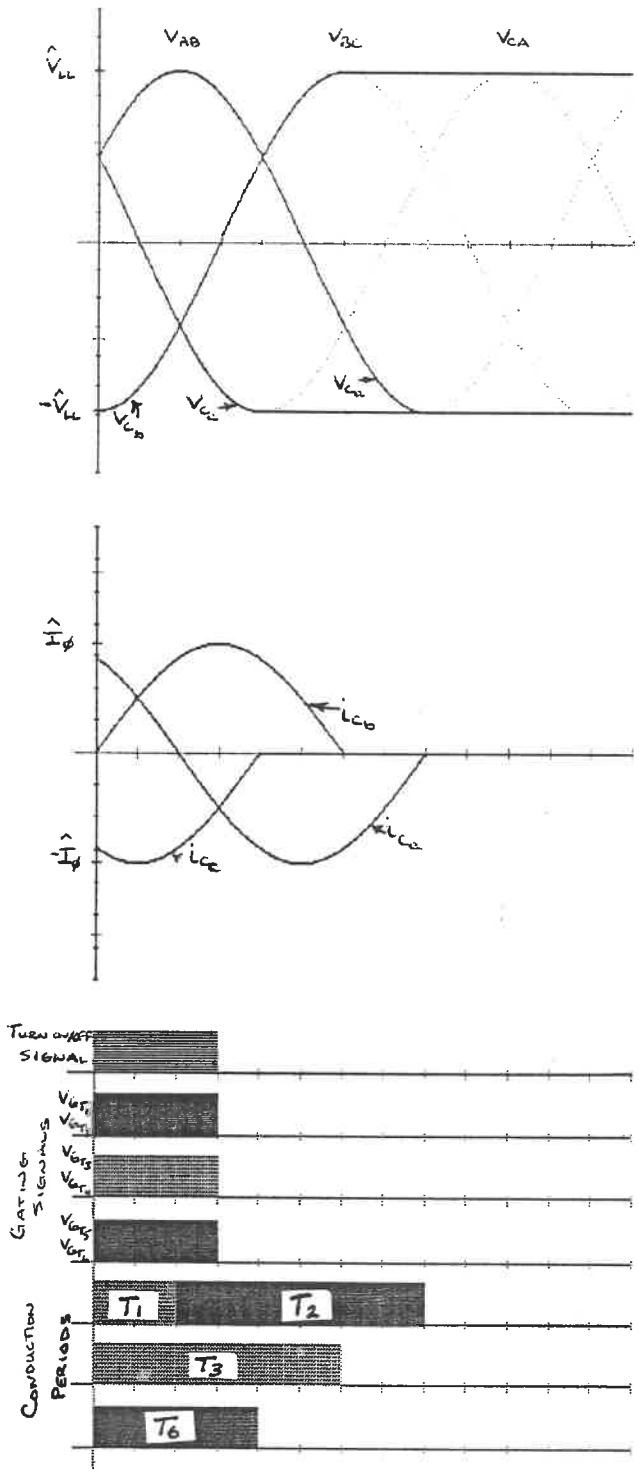


Fig. 3.6 Switching out a Three-Wire Branch-Controller with a Delta-Connected Load

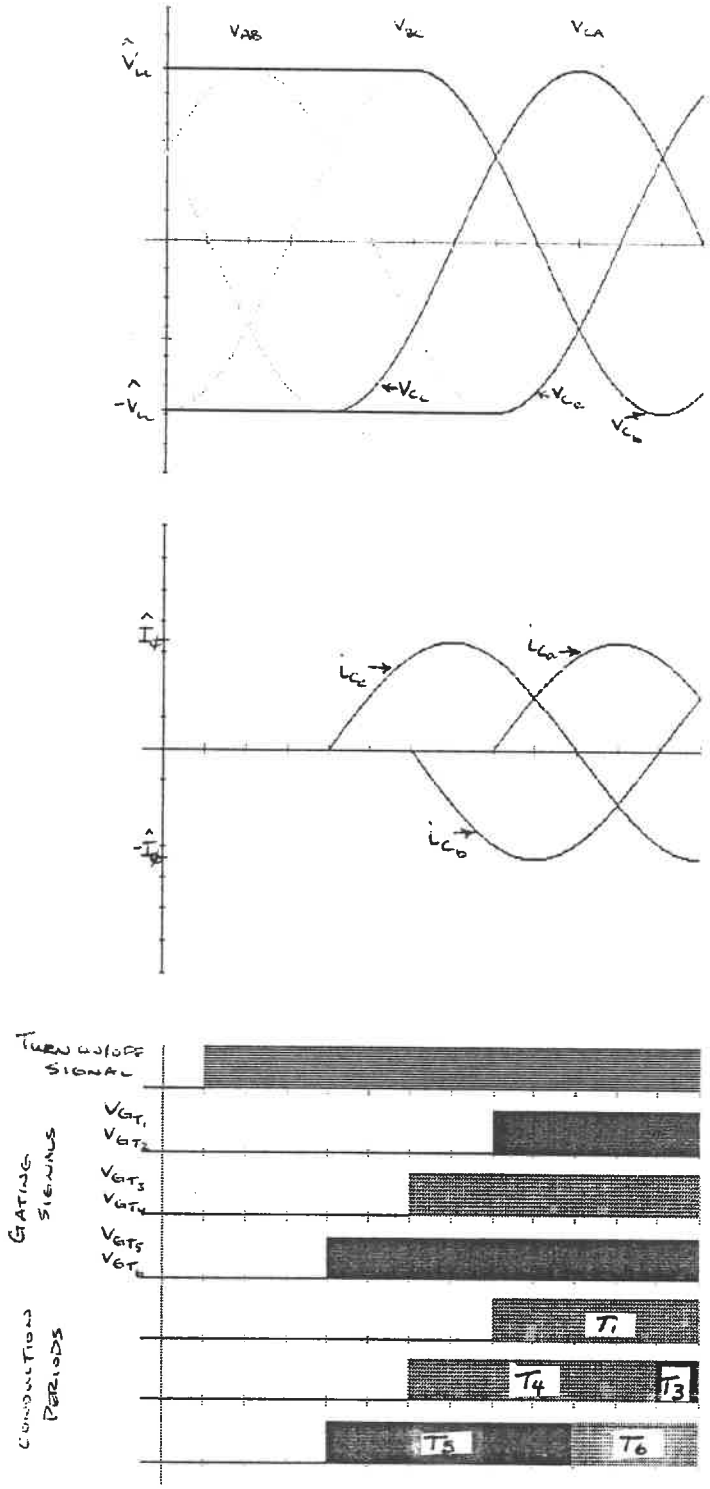
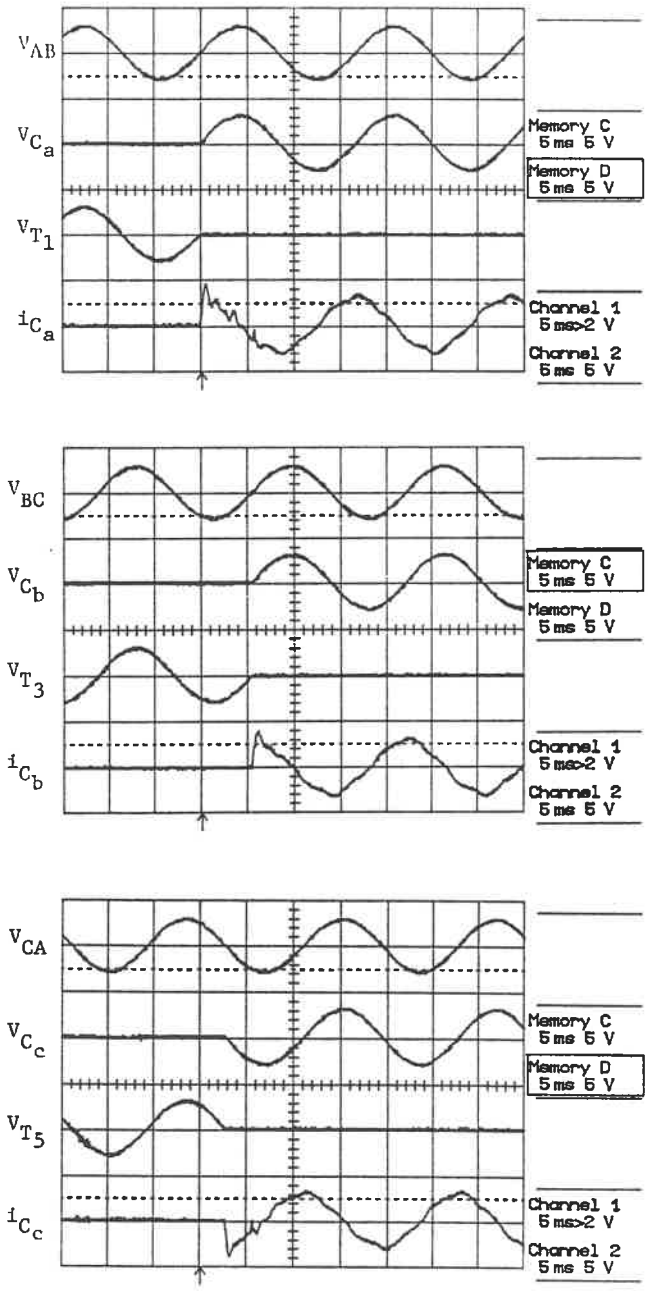


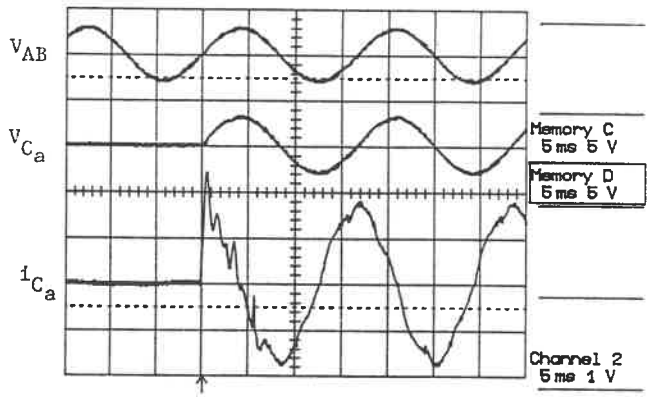
Fig. 3.7 Switching in again a Three-Wire Branch-Controller with a Delta-Connected Load

3.5 - Experimental Results:

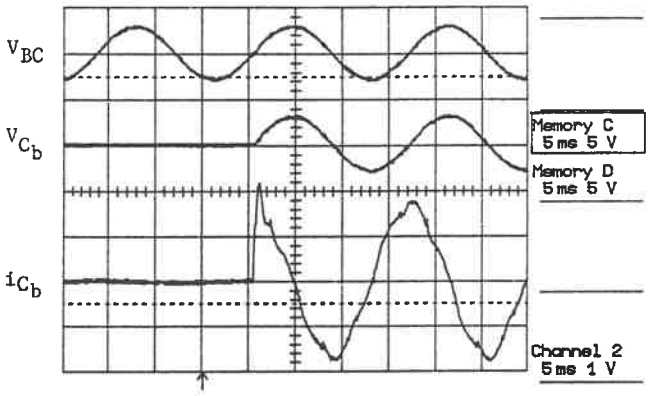


Plot 3.1 Switching in a Three-Wire Branch-Controller with a Delta-Connected Load; the capacitors are discharged (a) Phase A; (b) Phase B; (c) Phase C.
V_{LL}=208V, I_{Ca}=11.5A

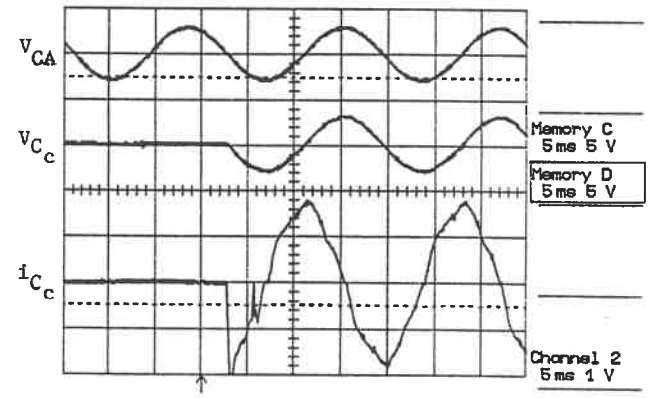
(a)



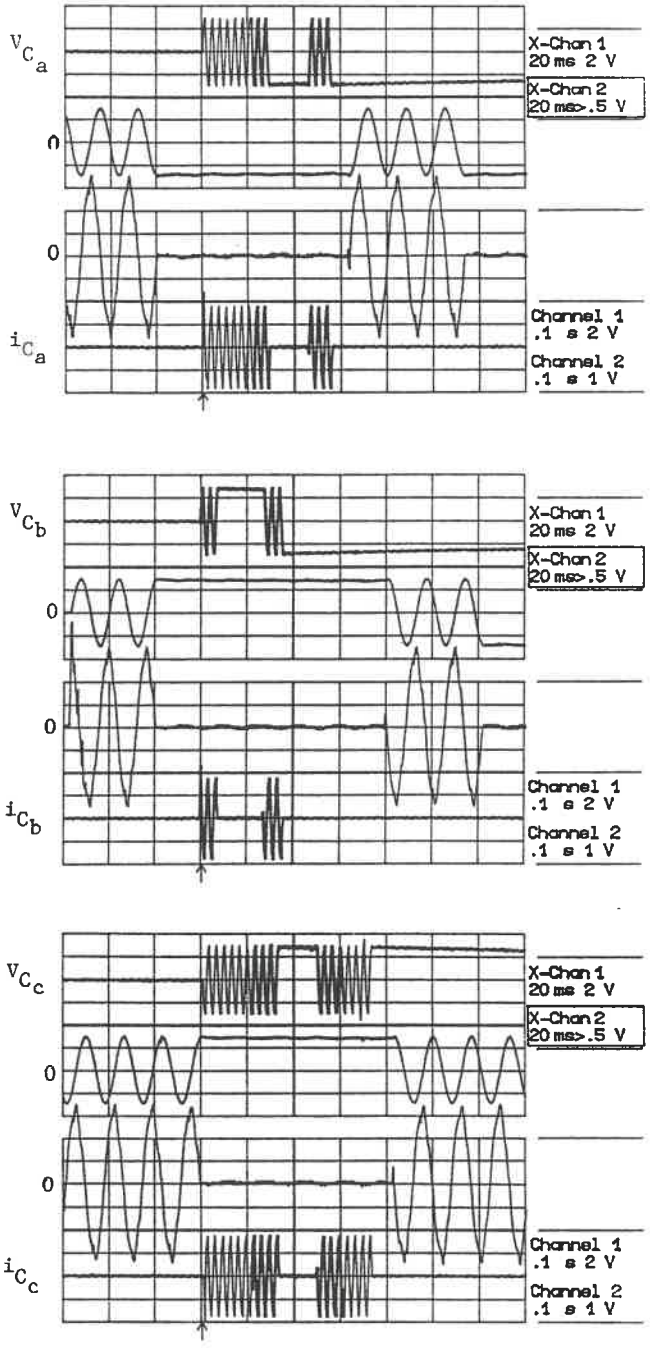
(b)



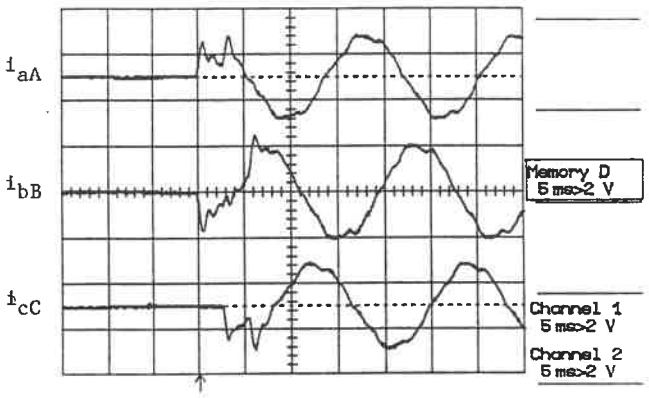
(c)



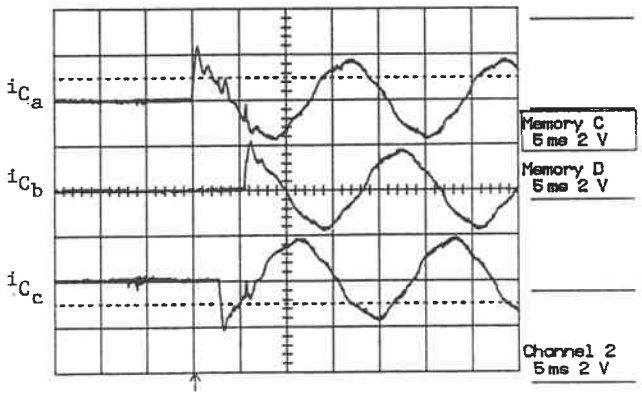
Plot 3.2 The capacitor currents when switching in a Three-Wire Branch-Controller with a Delta-Connected Load; the capacitors are discharged;
(a) Phase A; (b) Phase B; (c) Phase C.
V_{LL}=208V, I_{Ca}=11.5A



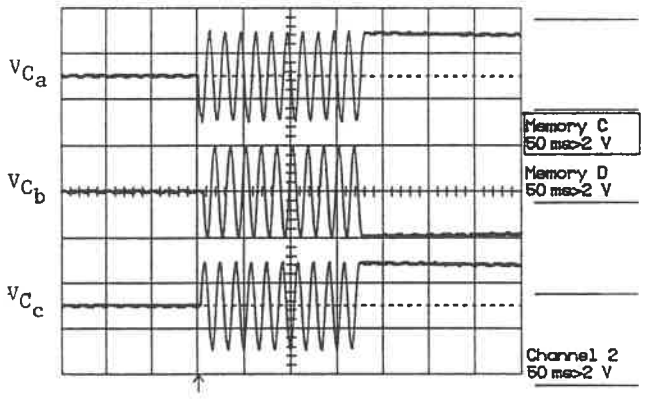
Plot 3.3 Switching in, out, and in again a Three-Wire Branch-Controller with a Delta-Connected Load; the capacitors are charged
(a) Phase A; (b) Phase B; (c) Phase C.
V_{LL}=208V, I_{Ca}=11.5A



Plot 3.4 Line currents when switching in a Three-Wire Branch-Controller with a Delta-Connected Load; V_{LL}=208V, I_{Ca}=11.5A



Plot 3.5 Phase currents when switching in a Three-Wire Branch-Controller with a Delta-Connected Load; V_{LL}=208V, I_{Ca}=11.5A



Plot 3.6 Capacitor voltages when switching a Three-Wire Branch-Controller with a Delta-Connected Load; V_{LL}=208V, I_{C_a}=11.5A

CHAPTER FOUR

THREE-WIRE LINE-CONTROLLER WITH DELTA-CONNECTED LOAD

4.1 - Introduction:

In this configuration three switches must be closed before the capacitive load is fully connected to the source. However, closing the first switch does not cause any current to flow, although it does connect one of the phases of the load to the source. Current only begins to flow when the second thyristor switch is closed, and a path for the current is created. As a result, this configuration behaves the same way as the Three-Wire Asymmetrical Line-Controller with a Delta-Connected Load. For the analysis of the circuit's behavior refer to chapter five.

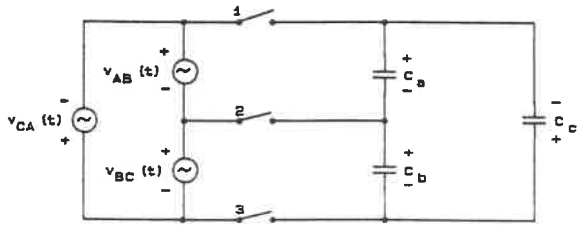


Fig. 4.1 Circuit diagram of a Three-Wire Line-Controller with a Delta-Connected Load

4.2 - Predictions of Circuit Behavior:

Using the information found in the analyses of Chapter Five, we can predict how the circuit will perform in the stages of operation that interest us: 1) switching in a discharged capacitor; 2) switching out the capacitor; 3) switching in the charged capacitor.

1) SWITCHING IN A DISCHARGED CAPACITOR:

Thyristors should be gated when the voltage across them is zero.

The magnitude and direction of the current in the different phases depends on which switch is closed first and the polarity of the source voltage when the switch is closed. Nonetheless the magnitude of the largest current in the thyristors will not exceed: $\pm i_{Lmax}$.

2) SWITCHING OUT THE CAPACITOR:

Thyristors stop conducting when the corresponding line current $i_L(t)=0$.

There are only four possible states that the capacitor bank could adopt after being switched off (this is because we have choosen to operate the W33AD as a W32AD by ensuring that switch 3 is always the last switch to turn off and the first switch to turn on).

To understand how these final states are arrived at it is useful to remember that after one of the three

switches has been opened we no longer have a three phase source, but rather a single phase source. In addition, opening a switch causes one of the capacitors to be connected in parallel with the two other capacitors. Consequently, as the capacitor which is connected directly across the source is charged to its peak value, the two other capacitors see their voltage decrease. (For a more detailed discussion of the turn off process see chapter five.)

The four possible final states are:

	A	B	C	D
V_{Ca}	107.6V	-401.6V	-107.6V	401.6V
V_{Cb}	294.0V	107.6V	-294.0V	-107.6V
V_{Cc}	-401.6V	294.0V	401.6V	-294.0V

3) SWITCHING IN CHARGED CAPACITOR:

Thyristors should be gated when the voltage across them is zero.

Corresponding current: $i(0^-)=0$.

4.3 - Computer Plots of Expected Circuit Behavior:

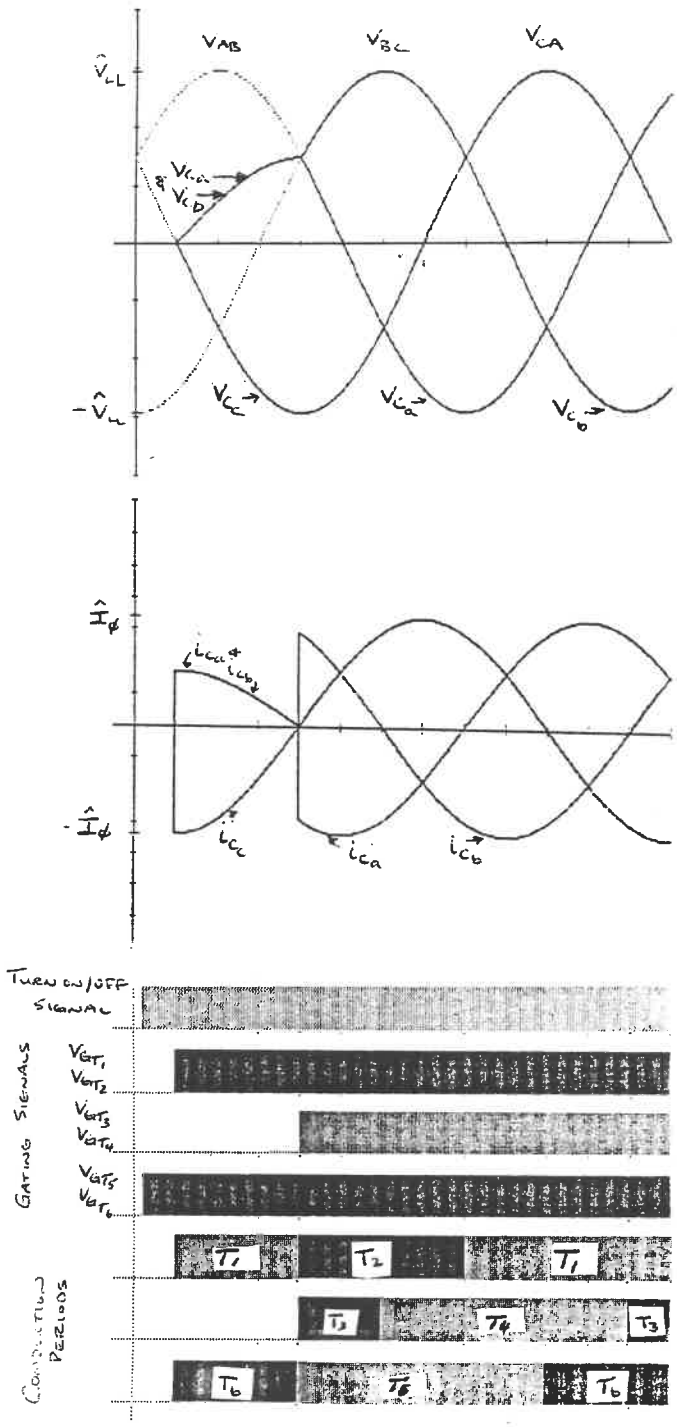


Fig. 4.2 Switching in a Three-Wire Line-Controller with a Delta-Connected Load; the capacitors are discharged

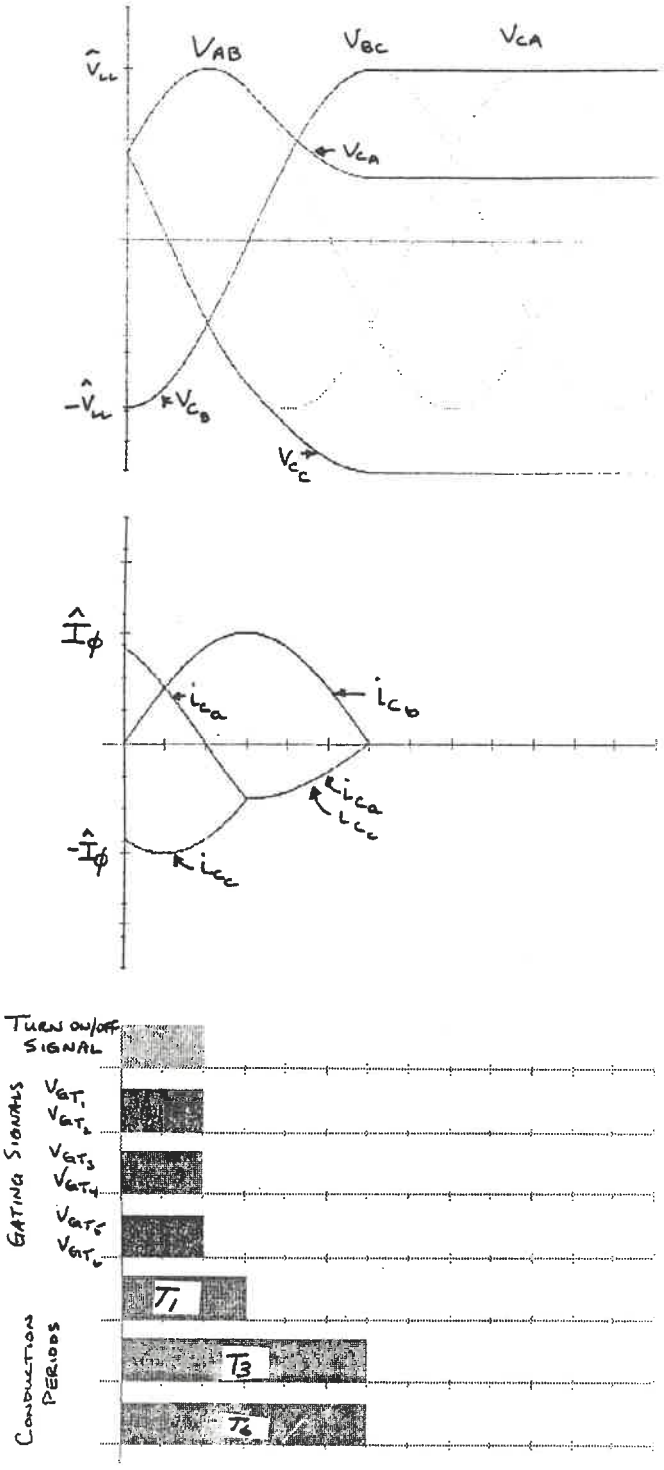


Fig. 4.3 Switching out a Three-Wire Line-Controller with a Delta-Connected Load

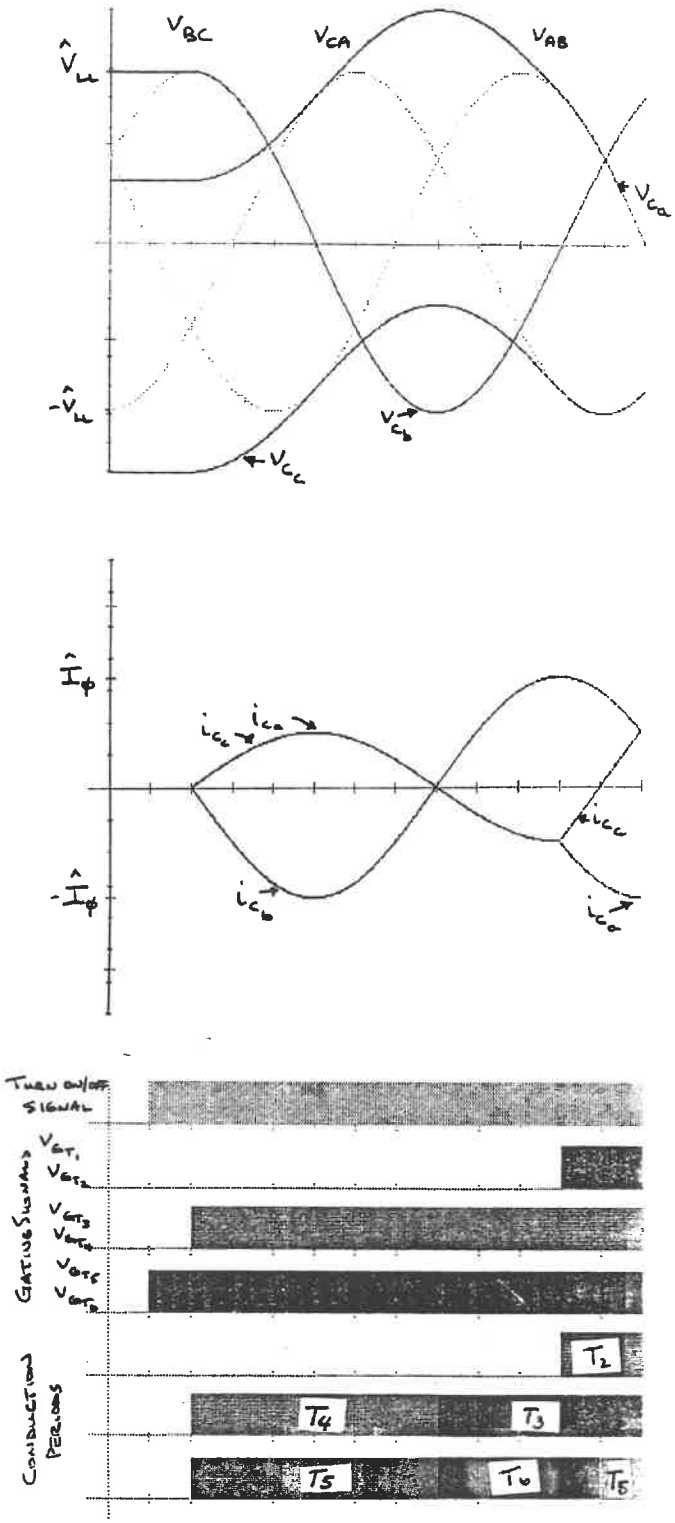


Fig. 4.4 Switching in again a Three-Wire Line-Controller with a Delta-Connected Load

CHAPTER FIVE

THREE-WIRE ASYMMETRICAL LINE-CONTROLLER WITH DELTA-CONNECTED LOAD

5.1 - Introduction:

In this configuration, two switches must be closed before the capacitive load is fully connected to the source. Hence we have two different cases to analyze, in order to understand how this configuration behaves.

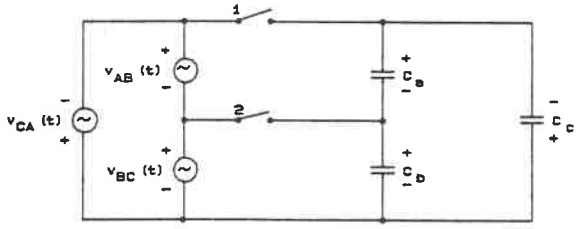


Fig. 5.1 Circuit diagram of a Three-Wire Assymmetrical Line-Controller with a Delta-Connected Load

5.2 - Analysis:

Case a: close switch 1

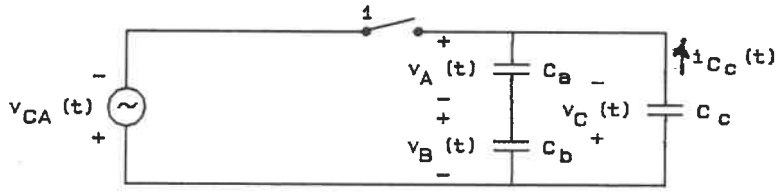


Fig. 5.2 Equivalent circuit of case a where switch 1 is closed

Using the circuit of Fig. 5.2 we see that after the switch has been closed, Kirchhoff's voltage law requires that:

$$v_{CA}(t)= \frac{1}{C_a}\int_0^t i_{Ca}\cdot dt + v_{Ca}(0^-) + \frac{1}{C_b}\int_0^t i_{Cb}\cdot dt + v_{Cb}(0^-)$$

note that $i_{Ca} = i_{Cb}$

After transforming, solving for $I_{Ca}(s)$, and then finding the inverse transform we see that:

$$i_{Ca}(t)= \frac{C_a \cdot C_b}{C_a + C_b}\left[V_{CAmax}\sin\theta_{CA} - v_{Ca}(0^-) - v_{Cb}(0^-)\right]\delta(t)$$
$$+ \frac{C_a \cdot C_b}{C_a + C_b}\,\omega_0 V_{Camax}\cos(\omega_0 t+\theta_{Ca})$$

In like manner we can show that:

$$i_{Ca}(t)=C_c\left[V_{CA}\sin\theta_{CA} - v_{Cc}(0^-)\right]\delta(t)$$
$$+ C_c\omega_0 V_{CAmax}\cos(\omega_0 t+\theta_{CA})$$

Conditions for switching without transients are:

$$V_{CAmax}\sin\theta_{CA}=v_{Ca}(0^-)=v_{Cc}(0^-)$$

This shows that switch 1 should be closed when the voltage across it is zero.

Case b: close switch 2 with switch 1 remaining closed

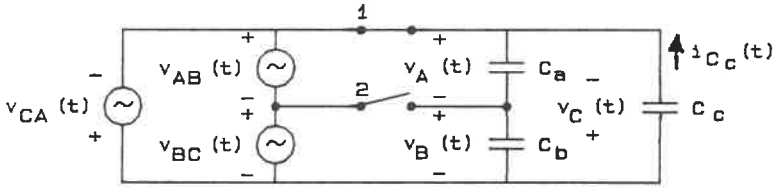


Fig. 5.3 Equivalent circuit of case b where switch 2 is closed while switch 1 remains closed

The equivalent circuit is shown in Fig. 5.3. By Kirchhoff's voltage law we can show that:

$$v_{AB} = \frac{1}{C_a}\int_0^t i_{Ca}\,dt + v_{Ca}(0^-)$$

Transforming, solving for $I_{Ca}(s)$ and then finding the inverse transform yields:

$$i_{Ca}(t) = C_a[V_{ABmax}\sin(\theta_{AB}) - v_{Ca}(0^-)] + \delta(t)$$
$$+ C_a\omega_0 V_{ABmax}\cos(\omega_0 t + \theta_{AB})$$

In the same way we can show that:

$$i_{Cb}(t) = C_b[V_{BCmax}\sin\theta_{BC} - v_{Cb}(0^-)]\,\delta(t)$$
$$+ C_b\omega_0 V_{BCmax}\cos(\omega_0 t + \theta_{BC})$$

Conditions for switching without transients are:

$$V_{ABmax}\sin\theta_{AB} = v_{Ca}(0^-)$$
$$\text{and } V_{BCmax}\sin\theta_{BC} = v_{Cb}(0^-)$$

This shows that switch 2 should be closed when the voltage across it is zero.

Turn Off:

It is important to remember that these equations can be used to determine the optimal moment for switching in a capacitor bank regardless of the capacitor voltage. Consequently, whether the capacitors are fully charged or fully discharged makes no difference; the optimal moment for switching in the capacitors is when the voltage across the thyristor switch is zero.

We will now exam the turning off process. Upon receiving the command to turn off the thyristors, the gate signal to each thyristor is removed. However, this does not mean that the thyristors are turned off. A thyristor only turns off when the current flowing through it decreases to zero. In this particular configuration it is the line current which must decline to zero before the thyristors will stop conducting. If we examine the same case that is depicted in Fig. 5.5, we note that when the line current is zero (i.e. $i_{aA} = 0$), the corresponding capacitor voltages are: $V_{Ca} = 0.866 \cdot V_{AB}$, $V_{Cb} = 0$, $V_{Cc} = -0.866 \cdot V_{CA}$. (Remember that the line current lags the phase current by 30°.) Consequently, these are the conditions that exist immediately after switch 1 is opened.

As soon as switch 1 is opened the circuit topology changes; we no longer have a three phase source, but rather a single phase source connected directly across one capaci-

tor C_b, and across the series connection of C_a and C_c. We note that at the instant that switch 1 is opened that the new source voltage V_{BC} equals the load voltage $V_{Cb} = V_{Ca} + V_{Cc}$, which equals zero. Kirchhoff tells us the sum of the load voltages must always equal zero. Therefore, as V_{Cb} is being charged to the peak line voltage, V_{Ca} has to decrease at the rate of half the source voltage V_{BC}. Likewise, V_{Cc} has to decrease at the same rate. If this does not happen the load voltages will not be balanced.

At the instant that V_{Cb} is charged to the peak line voltage, the corresponding line current i_{bB} will decline to zero. It is at this moment that we can consider the capacitor bank disconnected from the source. We note that the final voltages are: $V_{Ca} = (0.866-0.5)\cdot V_{LLmax} = 107.6V$; $V_{Cb} = V_{LLmax} = 294.0V$; $V_{Cc} = (-0.866-0.5)\cdot V_{LLmax} = -401.6V$.

5.3 - Predictions of Circuit Behavior:

With this information we can predict how the circuit will perform in the stages of operation that interest us: 1) switching in a discharged capacitor; 2) switching out the capacitor; 3) switching in the charged capacitor.

1) SWITCHING IN A DISCHARGED CAPACITOR:

Thyristors should be gated when the voltage across them is zero.

The magnitude and direction of the current in the different phases depends on which switch is closed first and the polarity of the source voltage when the switch is closed. Nonetheless the magnitude of the largest current in the thyristors will not exceed: $\pm i_{Lmax}$.

2) SWITCHING OUT THE CAPACITOR:

Thyristors stop conducting when the corresponding line current $i_L(t)=0$.

There are only four possible states that the capacitor bank could adopt after being switched off. The four possible final states are:

	A	B	C	D
V_{Ca}	107.6V	-401.6V	-107.6V	401.6V
V_{Cb}	294.0V	107.6V	-294.0V	-107.6V
V_{Cc}	-401.6V	294.0V	401.6V	-294.0V

3) SWITCHING IN CHARGED CAPACITOR:

Thyristors should be gated when the voltage across them is zero.

Corresponding current: $i(0^-)=0$.

5.4 - Computer Plots of Expected Circuit Behavior:

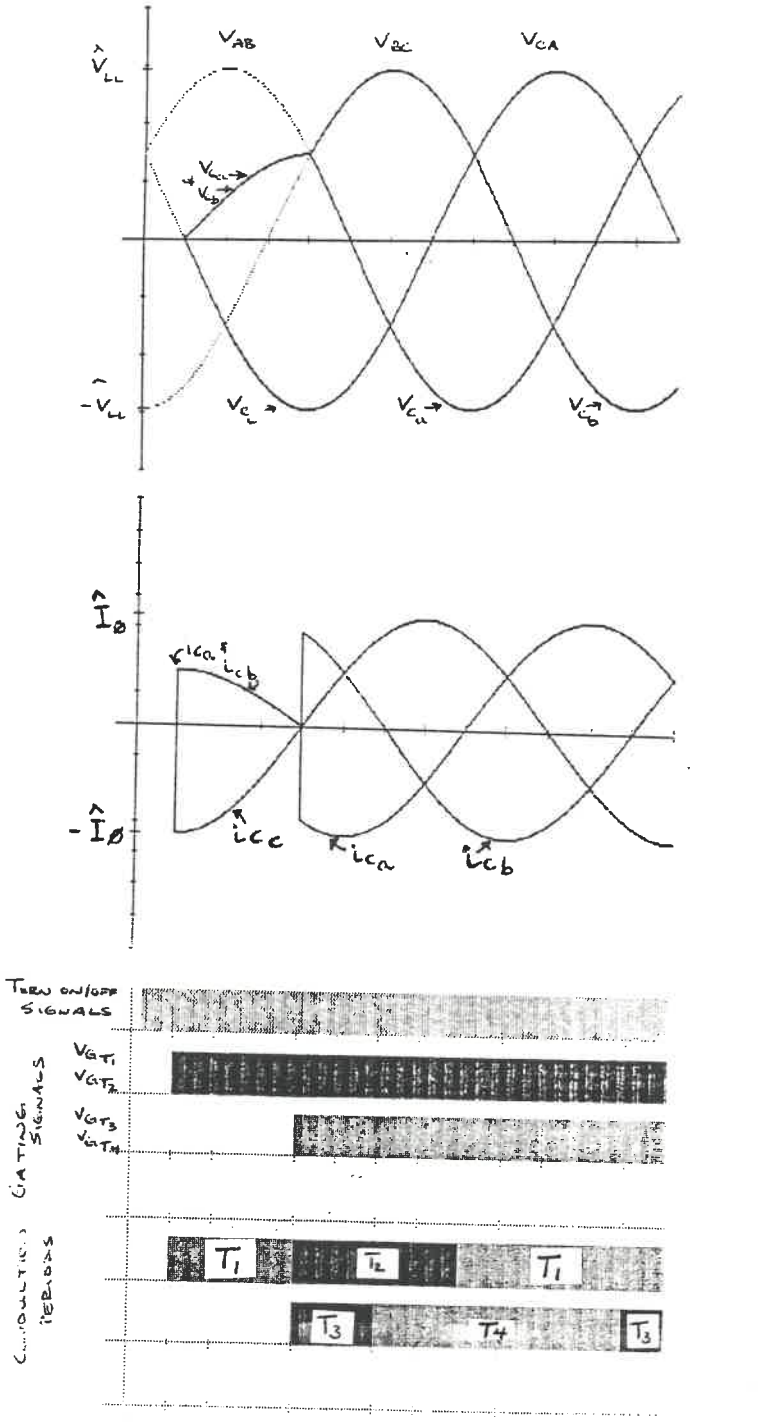


Fig. 5.4 Switching in a Three-Wire Assymetrical Line-Controller with a Delta-Connected Load; the capacitors are discharged

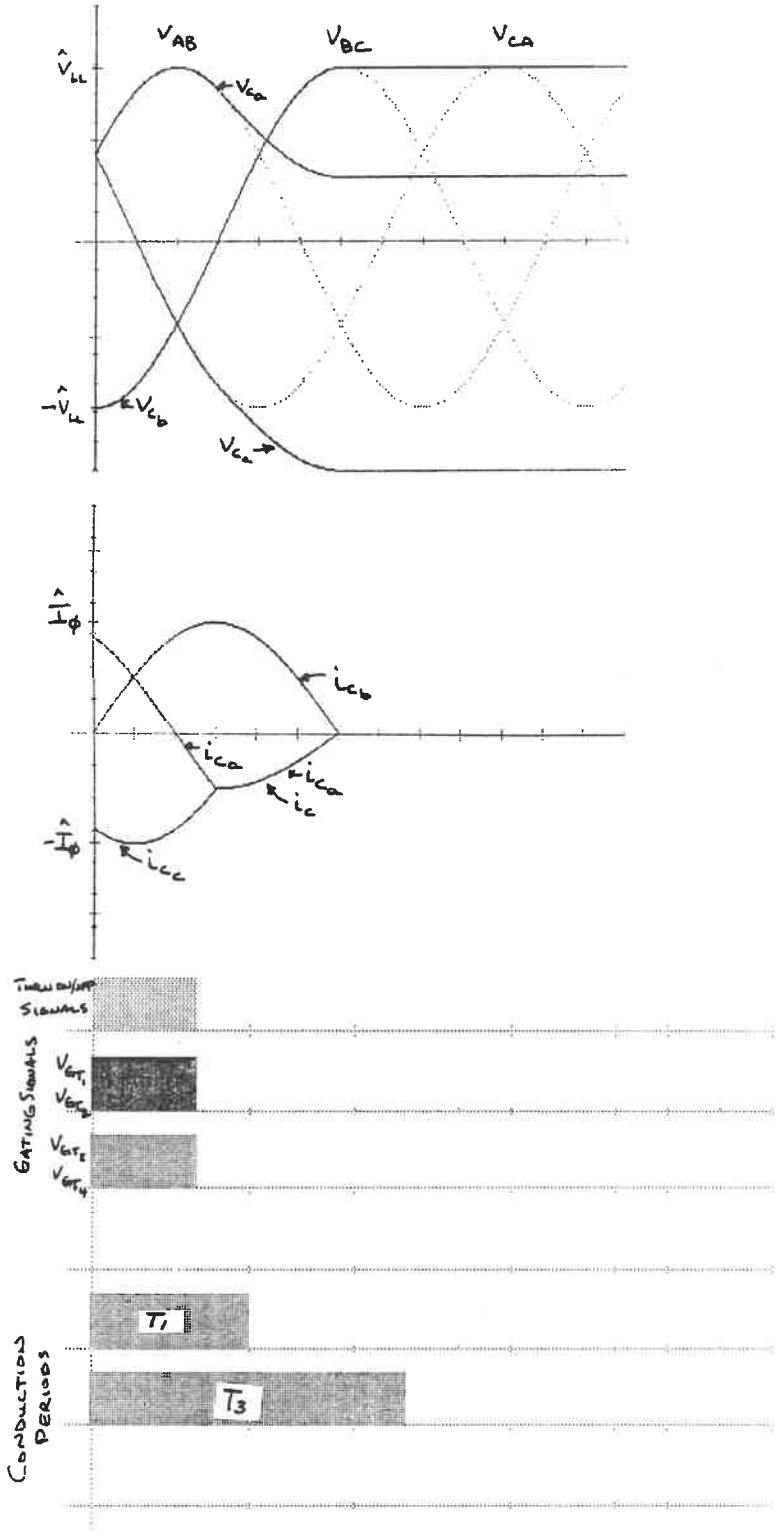


Fig. 5.5 Switching out a Three-Wire Assymetrical Line-Controller with a Delta-Connected Load

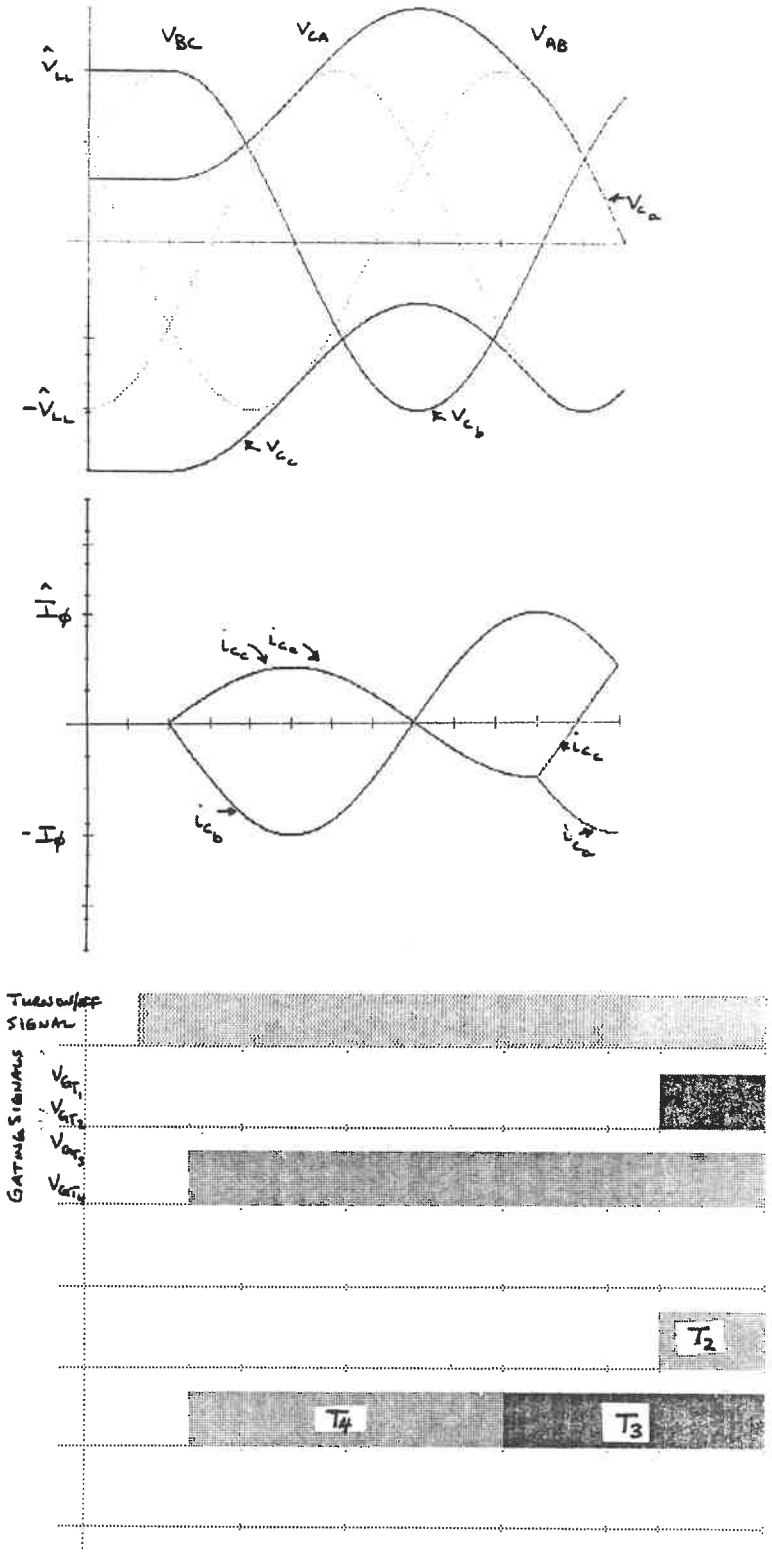
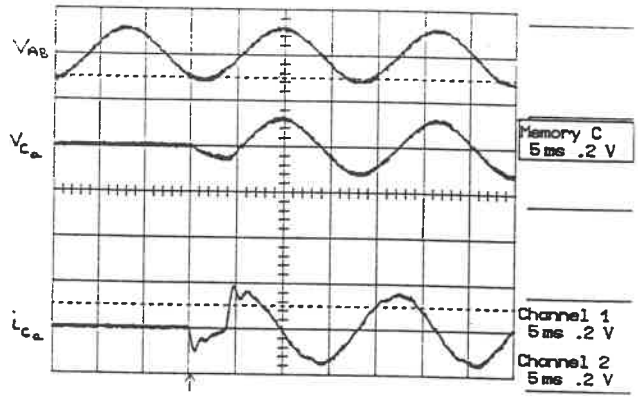


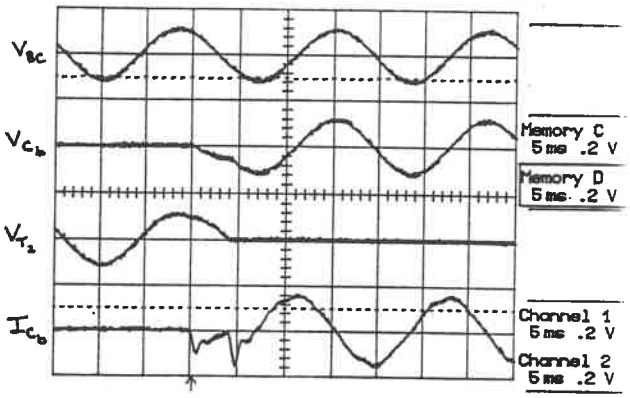
Fig. 5.6 Switching in again a Three-Wire Assymetrical Line-Controller with a Delta-Connected Load

5.5 - Experimental Results:

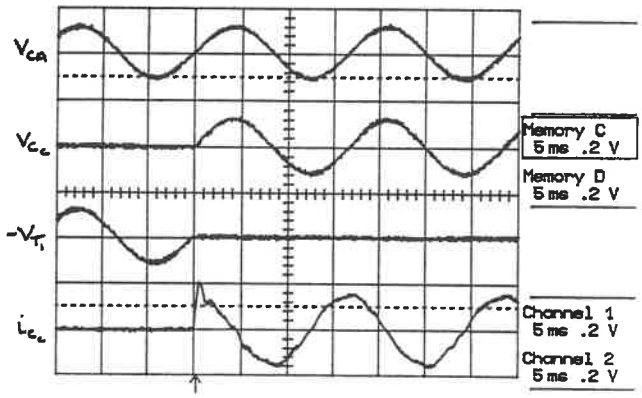
(a)



(b)



(c)

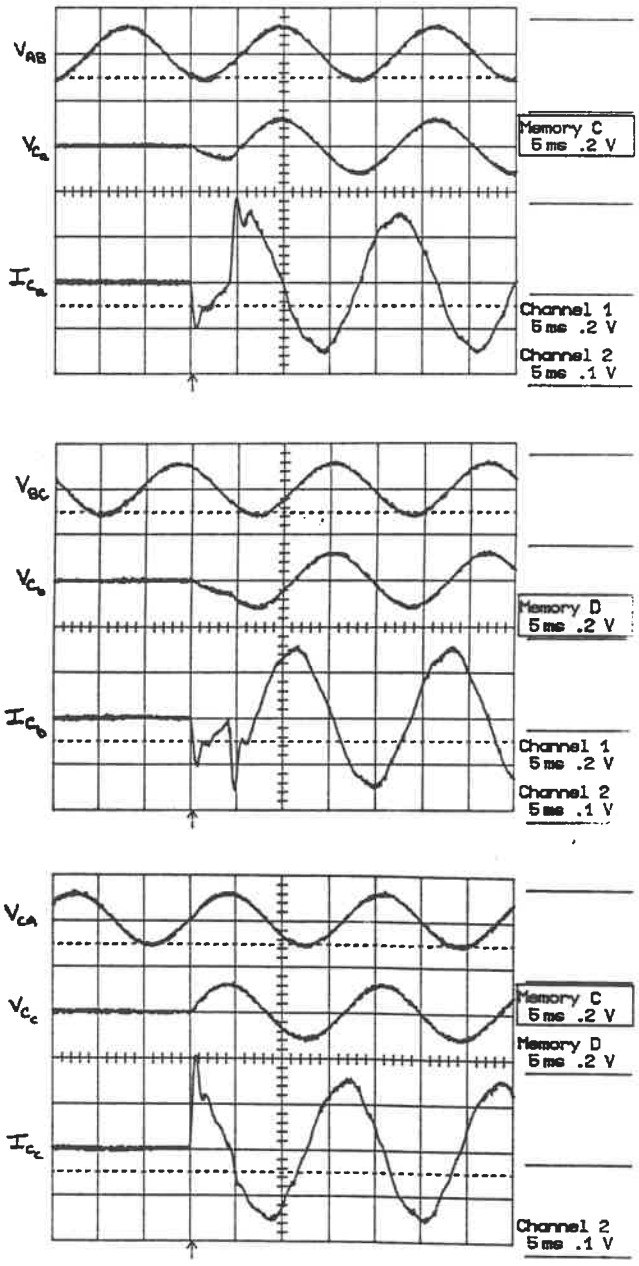


Plot 5.1 Switching in a Three-Wire Assymetrical Line-Controller with a Delta-Connected Load; the capacitors are discharged. (a) Phase A; (b) Phase B; (c) Phase C. V_{LL}=208V, I_{Ca}=11.5A

(a)

(b)

(c)

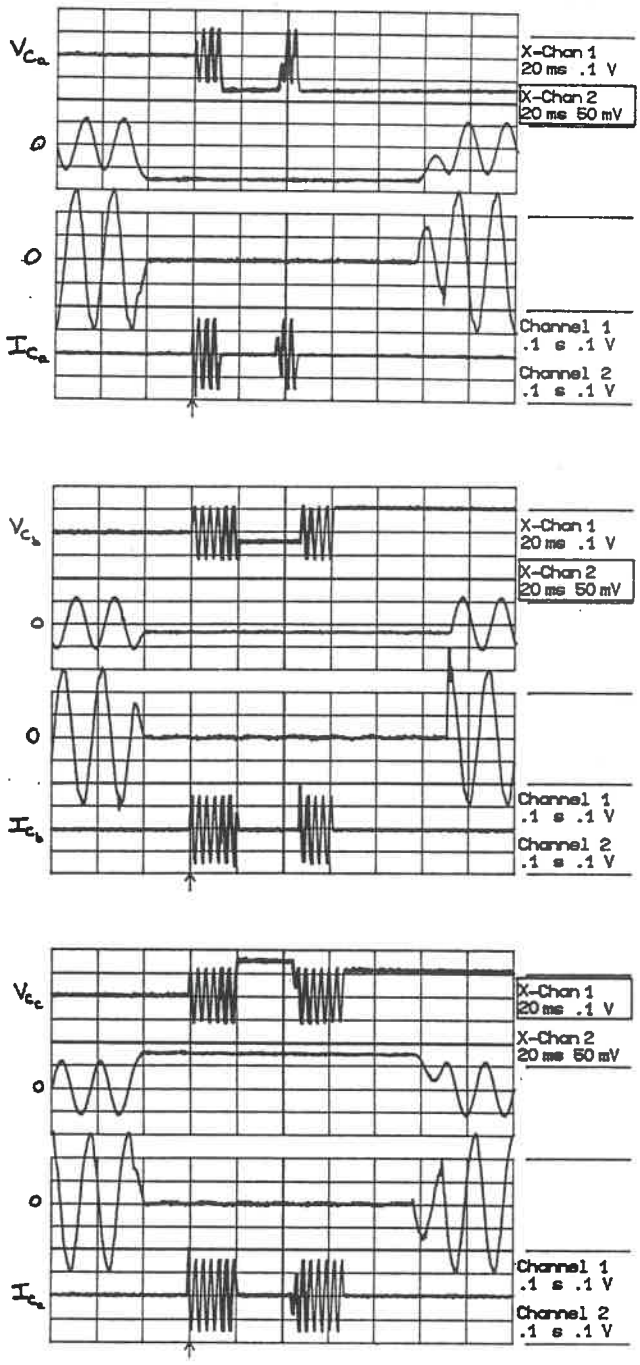


Plot 5.2 The capacitor currents when switching in a Three-Wire Assymetrical Line-Controller with a Delta-Connected Load; the capacitors are discharged; (a) Phase A; (b) Phase B; (c) Phase C. V_{LL}=208V, I_{Ca}=11.5A

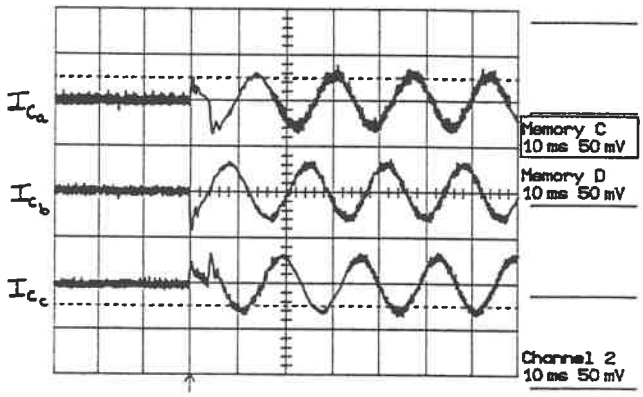
(a)

(b)

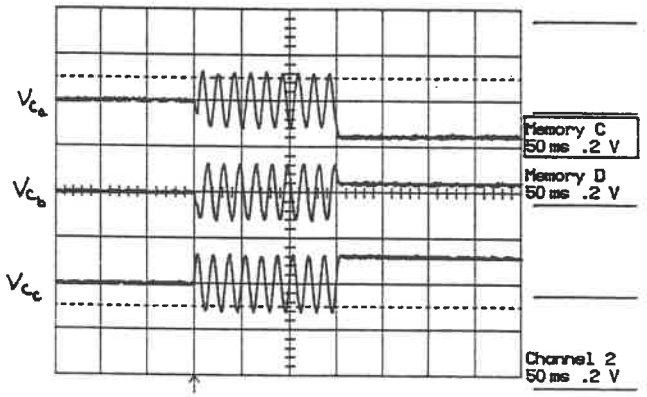
(c)



Plot 5.3 Switching in, out and in again a Three-Wire Assymetrical Line-Controller with a Delta-Connected Load; the capacitors are discharged.
(a) Phase A; (b) Phase B; (c) Phase C.
V_{LL}=208V, I_{Ca}=11.5A



Plot 5.4 Phase currents when switching in a Three-Wire Assymetrical Line-Controller with a Delta-Connected Load.
V_{LL}=208V, I_{Ca}=11.5A



Plot 5.5 Capacitor voltages when switching a Three-Wire Assymetrical Line-Controller with a Delta-Connected Load.
V_{LL}=208V, I_{Ca}=11.5A

CHAPTER SIX

THREE-WIRE LINE-CONTROLLER WITH WYE-CONNECTED LOAD

6.1 - Introduction:

In this configuration three switches must be closed before the capacitive load is fully connected to the source. However, closing the first switch does not cause any current to flow, although it does connect one of the phases of the load to the source. Current only begins to flow when the second thyristor switch is closed, and a path for the current is created. As a result, this configuration behaves the same way as the Three-Wire Asymmetrical Line-Controller with a Wye-Connected Load. For the analysis of the circuit's behavior refer to chapter seven.

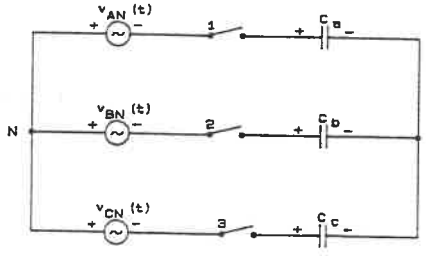


Fig. 6.1 Circuit diagram of a Three-Wire Line-Controller with a Wye-Connected Load

6.2 - Predictions of Circuit Behavior:

With this information we can predict how the circuit will perform in the stages of operation that interest us: 1) switching in a discharged capacitor; 2) switching out the capacitor; 3) switching in the charged capacitor.

1) SWITCHING IN A DISCHARGED CAPACITOR:

Thyristors should be gated when the voltage across them is zero.

The magnitude and direction of the current in the different phases depends on which switch is closed first and the polarity of the source voltage when the switch is closed. Nonetheless the magnitude of the largest current flowing through the thyristors will not exceed: $\pm i_{\Phi max}$.

2) SWITCHING OUT THE CAPACITOR:

Thyristors stop conducting when the corresponding line current $i_{\Phi}(t)=0$.

There are only four possible states that the capacitor bank could adopt after being switched off (this is because we have choosen to operate the W33AY as a W32AY by ensuring that switch 3 is always the last switch to turn off and the first switch to turn on).

To understand how these final states are arrived at it is useful to remember that after one of the three switches has been opened we no longer have a three

phase source, but rather a single phase source. In addition, opening a switch causes one of the capacitors to be disconnected while leaving the two other capacitors connected in series across the source. Consequently, the disconnected capacitor is left fully charged; the two other capacitors, while orginally charged to the same voltage, now see their voltage increase and decrease respectively as the source voltage climbs to its peak and the phase current declines to zero. (For a more detailed discussion of the turn off process see chapter seven.)

The four possible final states are:

	A	B	C	D
V_{Ca}	170.0V	-232.2V	-170.0V	232.2V
V_{Cb}	62.2V	170.0V	-62.2V	-170.0V
V_{Cc}	-232.2V	62.2V	232.2V	-62.2V

3) SWITCHING IN CHARGED CAPACITOR:

Thyristors should be gated when the voltage across them is zero.

Corresponding current: $i(0^-)=0$.

6.3 - Computer Plots of Expected Circuit Behavior:

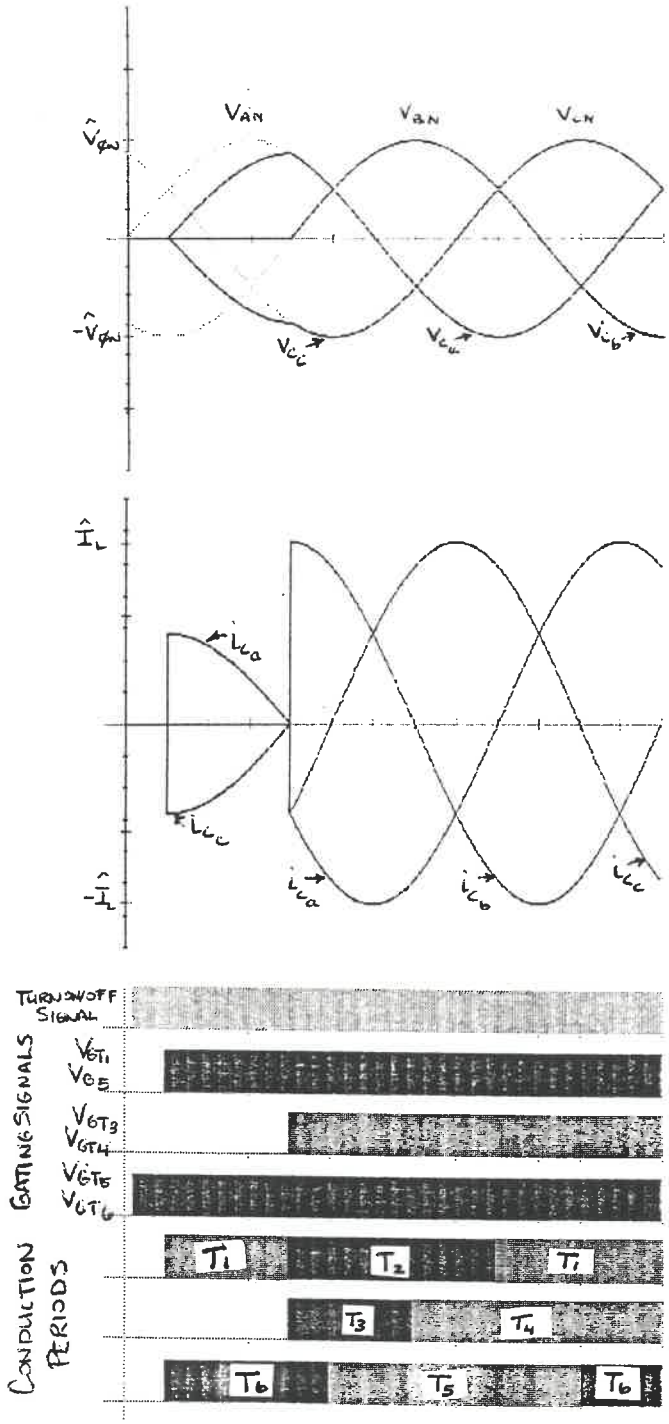


Fig. 6.2 Switching in a Three-Wire Line-Controller with a Wye-Connected Load; the capacitors are discharged

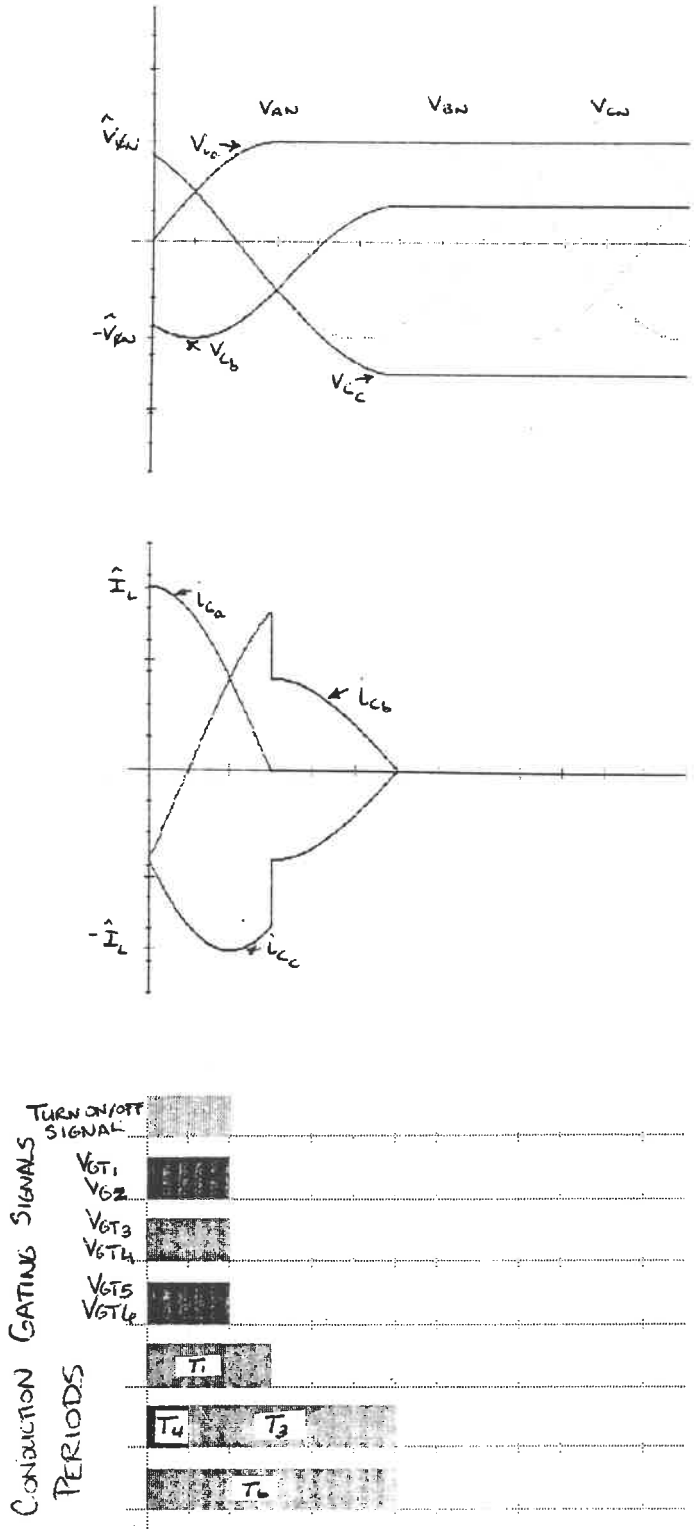


Fig. 6.3 Switching out a Three-Wire Line-Controller with a Wye-Connected Load

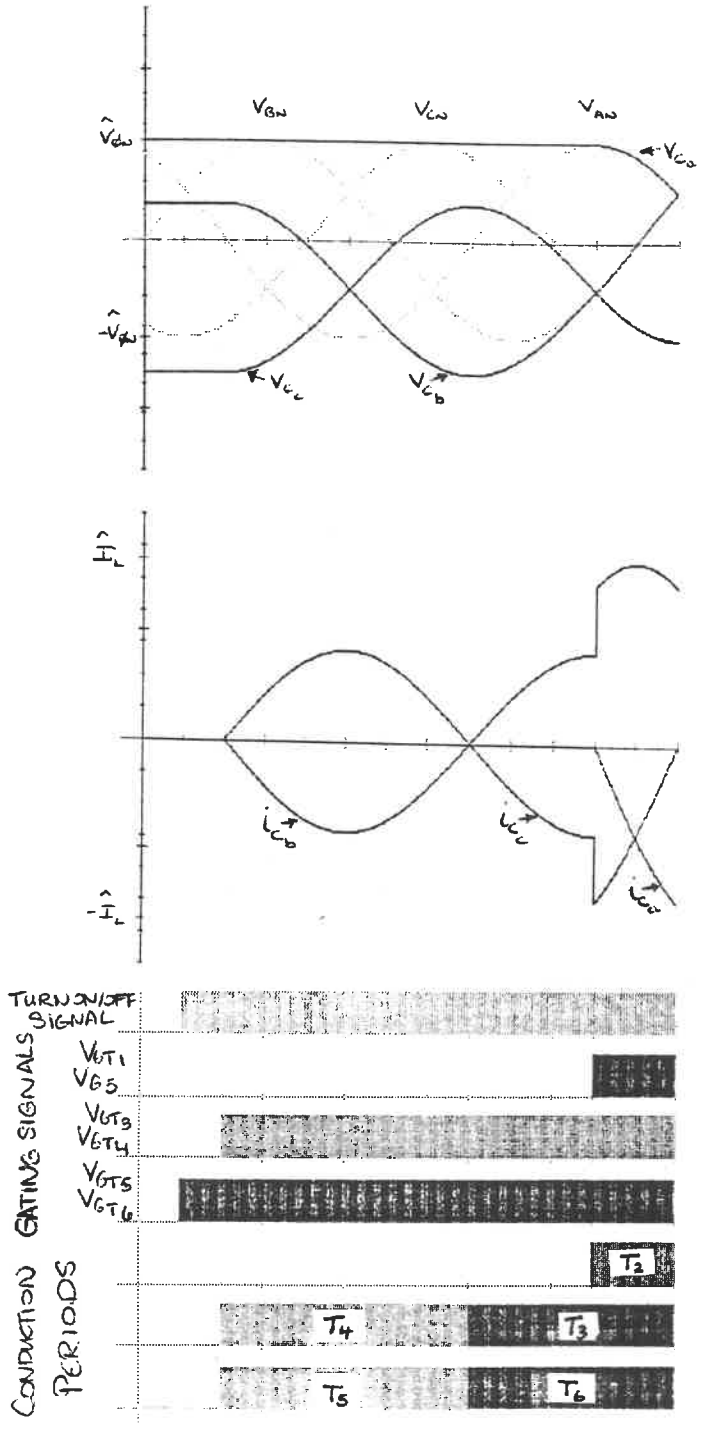


Fig. 6.4 Switching in again a Three-Wire Line-Controller with a Wye-Connected Load

CHAPTER SEVEN

THREE-WIRE ASYMMETRICAL LINE-CONTROLLER WITH WYE-CONNECTED LOAD

7.1 - Introduction:

In this configuration, two switches must be closed before the capacitive load is fully connected to the source. Hence we have two different cases to analyze, in order to understand how this configuration behaves.

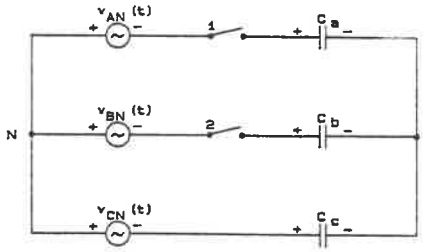


Fig. 7.1 Circuit diagram of a Three-Wire Asymmetrical Line-Controller with a Wye-Connected Load

7.2 - Analysis:

Case a: close switch 1

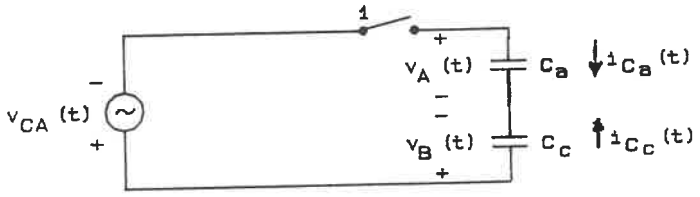


Fig. 7.2 Equivalent circuit of case a where switch 1 is closed

Using the circuit of Fig. 7.2 we see that after the switch has been closed, Kirchhoff's voltage law requires that:

$$v_{CA}(t)= \frac{1}{C_a}\int_0^t i_{Ca}\cdot dt + v_{Ca}(0^-) + \frac{1}{C_c}\int_0^t i_{Cc}\cdot dt + v_{Cc}(0^-)$$

note that $i_{Cc} = -i_{Ca}$

After transforming, solving for $I_{Cc}(s)$, and then finding the inverse transform we see that:

$$i_{Cc}(t)= \frac{C_a \cdot C_c}{C_a + C_c}\left[V_{CAmax}\sin\theta_{CA} - v_{Cc}(0^-) + v_{Ca}(0^-)\right]\delta(t)$$

$$+ \frac{C_a \cdot C_c}{C_a + C_c}\,\omega_0 V_{CAmax}\cos(\omega_0 t+\theta_{CA})$$

Conditions for switching without transients are:

$$V_{CAmax}\sin\theta_{CA} = v_{Cc}(0^-) - v_{Ca}(0^-)$$

This shows that switch 1 should be closed when the voltage across it is zero.

Case b: close switch 2 with switch 1 remaining closed

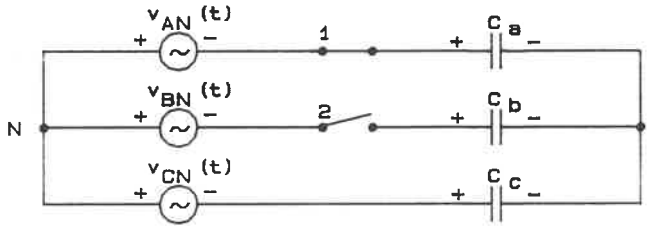


Fig. 7.3 Equivalent circuit of case b where switch 2 is closed while switch 1 remains closed

The equivalent circuit is shown in Fig. 7.3. By Kirchhoff's current law we can show that:

$$I_{aA}+I_{bB}+I_{cC}=0$$

where:
$$I_{aA}=sC_a(v_{AN}-v_0)-C_a v_{AN}(0^-)$$
$$I_{bB}=sC_b(v_{BN}-v_0)-C_b v_{BN}(0^-)$$
$$I_{cC}=sC_c(v_{CN}-v_0)-C_c v_{CN}(0^-)$$

solving for v_0 yields:

$$V_0=\frac{1}{3}\left[\left(v_{AN}-\frac{v_{Ca}(0^-)}{s}\right)+\left(v_{BN}-\frac{v_{Cb}(0^-)}{s}\right)+\left(v_{CN}-\frac{v_{Cc}(0^-)}{s}\right)\right]$$

since $C_a=C_b=C_c$

Transforming, solving for $I_{Cb}(s)$ and then finding the inverse transform yields:

$$i_{Cb} = (C/3)\cdot\{ (V_{BCmax}\cdot\sin\theta_{BC} - V_{Cb}(0^-) + V_{Cc}(0^-) - V_{ABmax}\cdot\sin\theta_{AB} - V_{Cb}(0^-) + V_{ca}(0^-) \}\cdot\delta(t) + (C/3)\cdot\{ V_{BC}\omega_o\cos(\omega t+\theta_{BC}) - V_{AB}\omega_o\cos(\omega t+\theta_{AB}) \}$$

Conditions for switching without transients are:

$$V_{BNmax}\cdot\sin\theta_{BN}=V_{Cc}(0^-) + V_{Ca}(0^-) - 2\cdot V_{Cb}(0^-)$$

This shows that switch 2 should be closed when the voltage across it is zero.

Turn Off: It is important to remember that these equations can be used to determine the optimal moment for switching in a capacitor bank regardless of the capacitor voltage. Consequently, whether the capacitors are fully charged or fully discharged makes no difference; the optimal moment for switching in the capacitors is when the voltage across the thyristor switch is zero.

We will now exam the turning off process. Upon receiving the command to turn off the thyristors, the gate signal to each thyristor is removed. However, this does not mean that the thyristors are turned off. A thyristor only turns off when the current flowing through it decreases to zero. In this particular configuration it is the line current which must decline to zero before the thyristors will stop conducting. If we examine the same case that is depicted in Fig. 7.5, we note that when the line current is zero (i.e. $i_{aA} = 0$), the corresponding capacitor voltages are: $V_{Ca} = V_{AN}$, $V_{Cb} = -0.5 \cdot V_{BN}$, $V_{Cc} = -0.5 \cdot V_{CN}$. Consequently, these are the conditions that exist immediately after switch 1 is opened.

As soon as switch 1 is opened the circuit topology changes; we no longer have a three phase source, but rather a single phase source connected directly across the series connection of C_b and C_c. We note that at the instant

switch 1 is opened that the new source voltage V_{BC} equals the load voltage $V_{Cb} - V_{Cc}$, which equals zero. Kirchhoff tells us the sum of the load voltages must always equal zero. Therefore, as V_{BC} rises to the peak line voltage, V_{Cb} has to increase at the rate of half the source voltage. Likewise, V_{Cc} has to decrease at the same rate. If this does not happen the load voltages will not be balanced.

At the instant that V_{Cb} is charged to the peak line voltage, the corresponding line current i_{bB} will decline to zero. It is at this moment that we can consider the capacitor bank disconnected from the source. We note that the final voltages are:

$$V_{Ca} = V_{LNmax} = 170.0V \text{ (as before);}$$

$$V_{Cb} = (-0.5+0.866) \cdot V_{LNmax} = 62.2V;$$

$$V_{Cc} = (-0.5-0.866) \cdot V_{LNmax} = -232.2V.$$

7.3 - Predictions of Circuit Behavior:

With this information we can predict how the circuit will perform in the stages of operation that interest us: 1) switching in a discharged capacitor; 2) switching out the capacitor; 3) switching in the charged capacitor.

1) SWITCHING IN A DISCHARGED CAPACITOR:

Thyristors should be gated when the voltage across them is zero.

The magnitude and direction of the current in the different phases depends on which switch is closed first and the polarity of the source voltage when the switch is closed. Nonetheless the magnitude of the largest current flowing through the thyristors will not exceed: $\pm i_{\Phi max}$.

2) SWITCHING OUT THE CAPACITOR:

Thyristors stop conducting when the corresponding line current $i_{\Phi}(t)=0$.

There are only four possible states that the capacitor bank could adopt after being switched off. The four possible final states are:

	A	B	C	D
V_{Ca}	170.0V	-232.2V	-170.0V	232.2V
V_{Cb}	62.2V	170.0V	-62.2V	-170.0V
V_{Cc}	-232.2V	62.2V	232.2V	-62.2V

3) SWITCHING IN CHARGED CAPACITOR:

Thyristors should be gated when the voltage across them is zero.

Corresponding current: $i(0^-)=0$.

7.4 - Computer Plots of Expected Circuit Behavior:

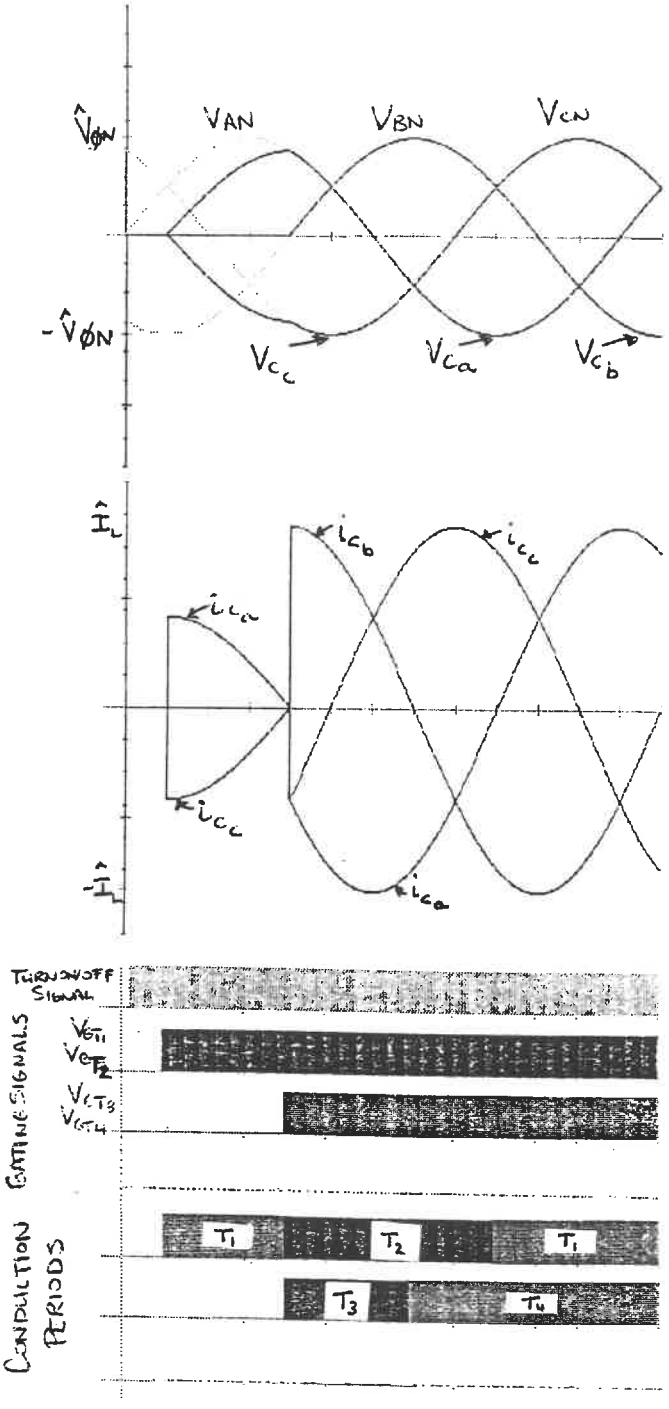


Fig. 7.4 Switching in a Three-Wire Line-Controller with a Wye-Connected Load; the capacitors are discharged

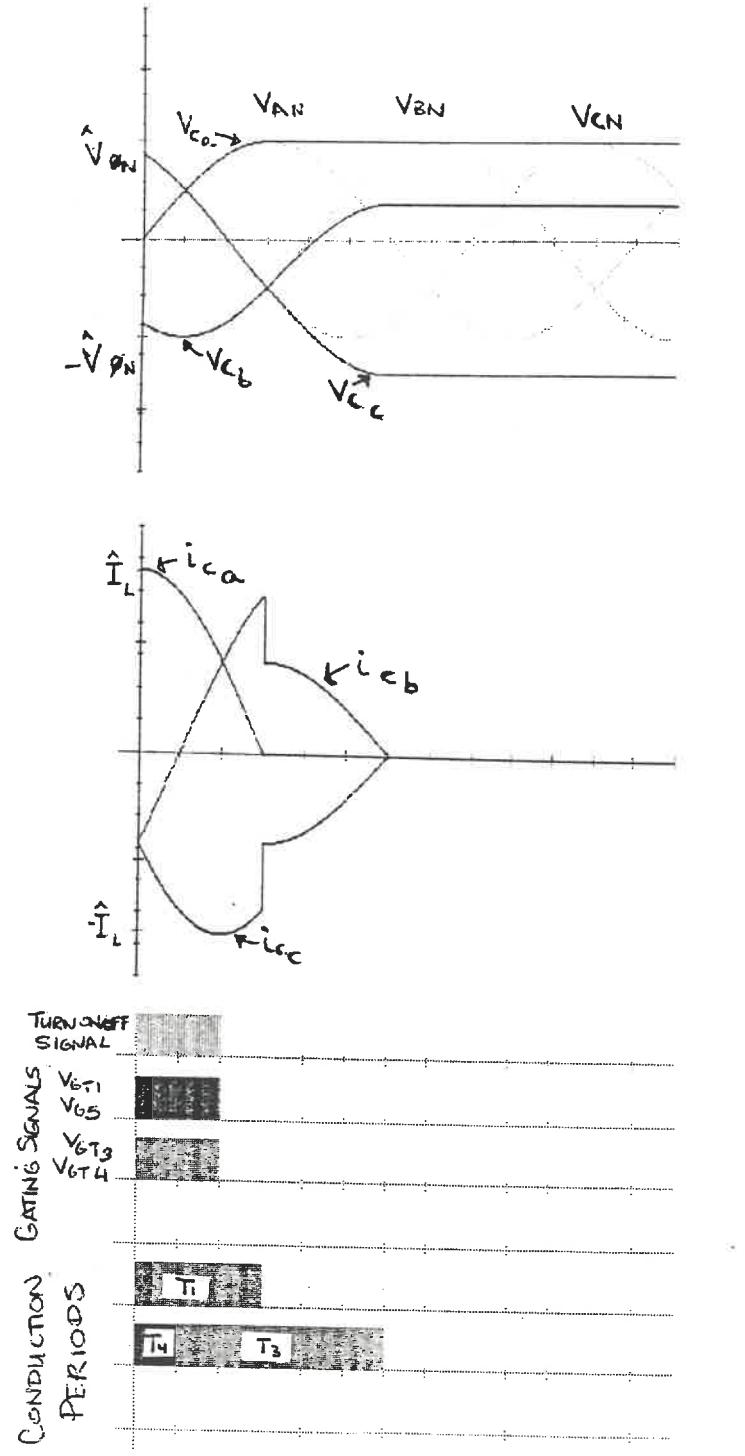


Fig. 7.5 Switching out a Three-Wire Line-Controller with a Wye-Connected Load

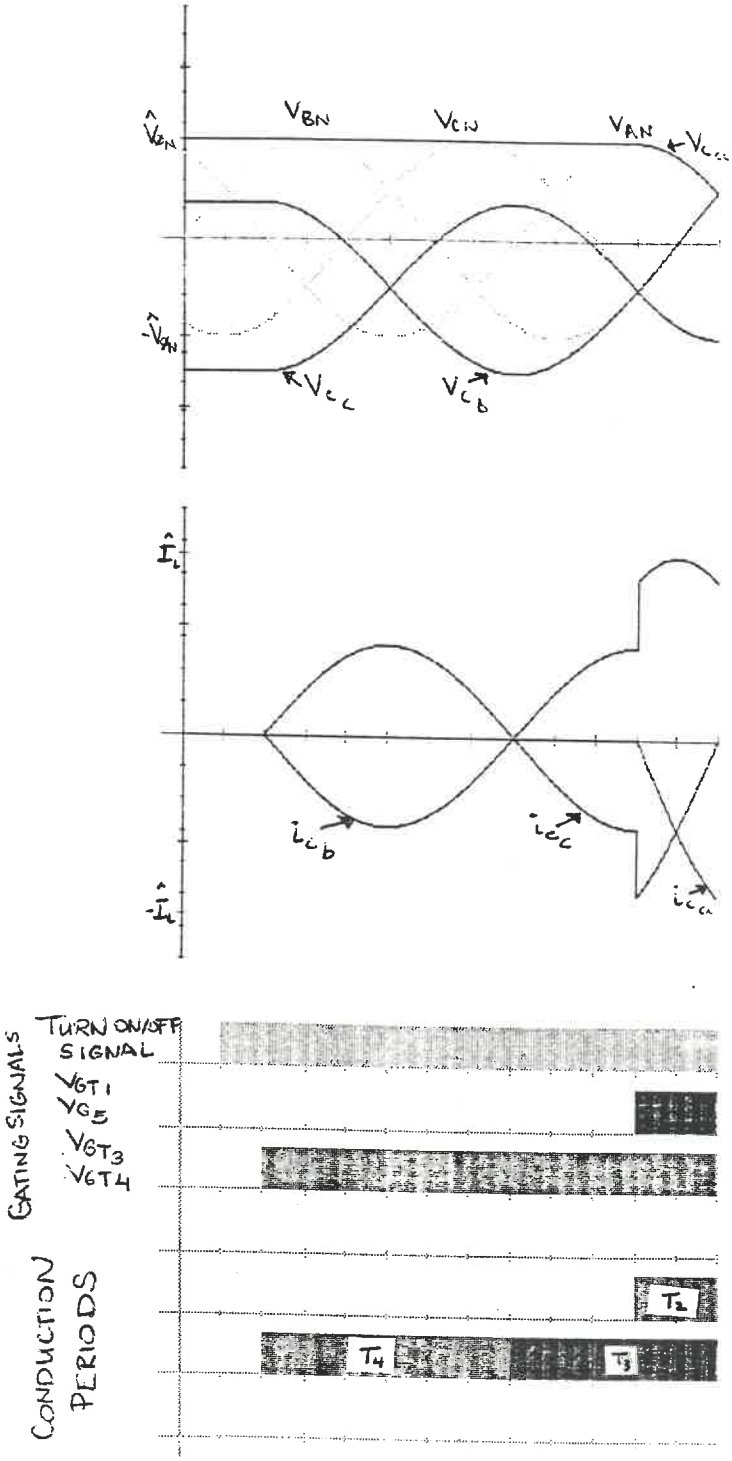
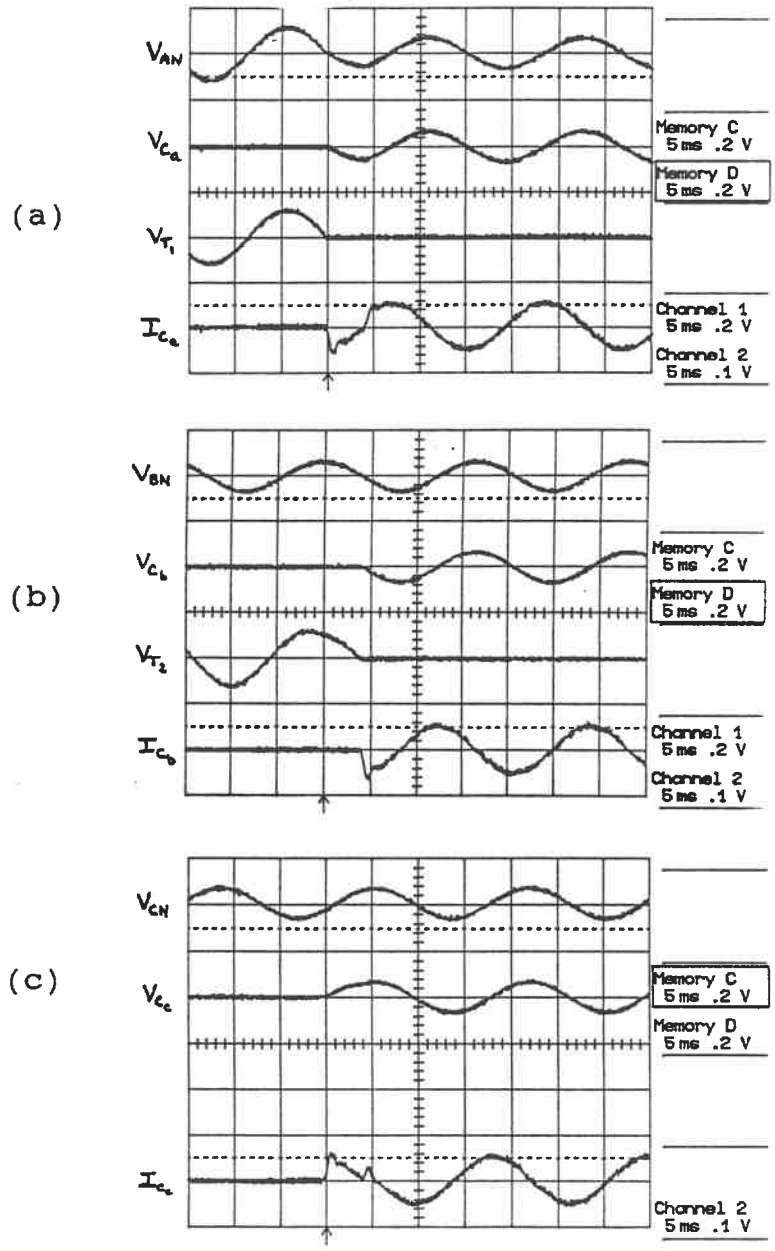


Fig. 7.6 Switching in again a Three-Wire Line-Controller with a Wye-Connected Load

7.6 - Experimental Results:

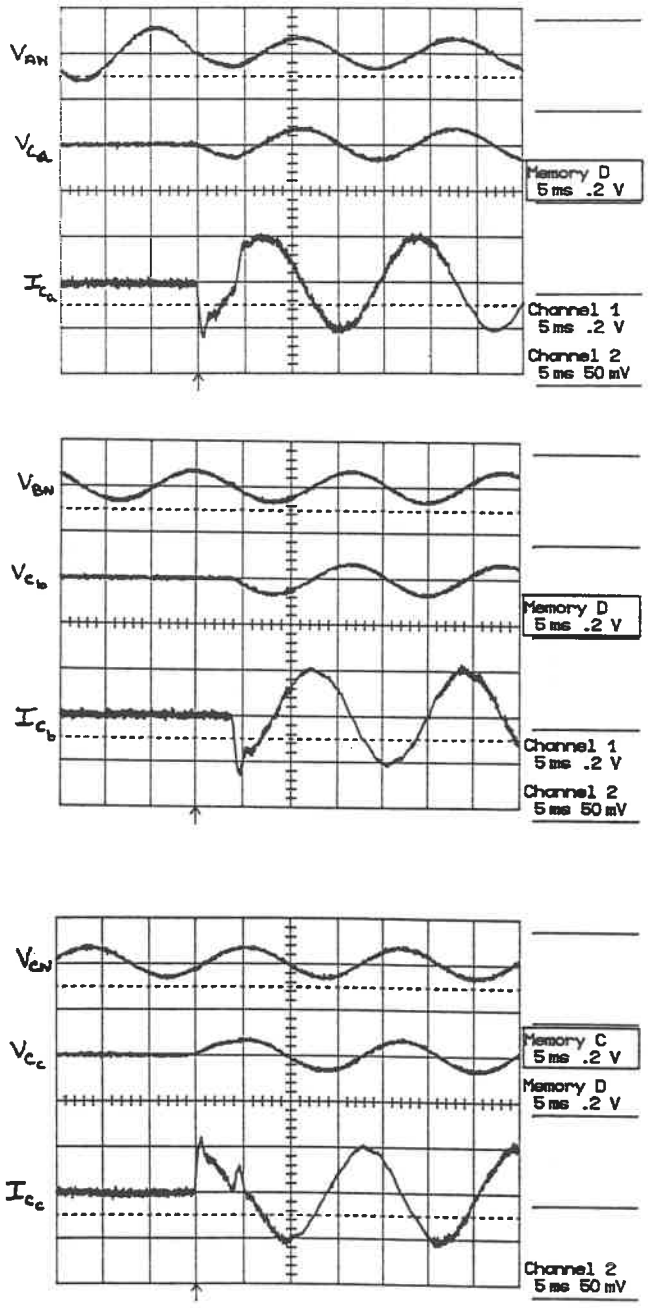


Plot 7.1 Switching in a Three-Wire Asymmetrical Line-Controller with a Wye-Connected Load; the capacitors are discharged. (a) Phase A; (b) Phase B; (c) Phase C. $V_{\Phi N}$=120V, $I_{C a}$=21.5A

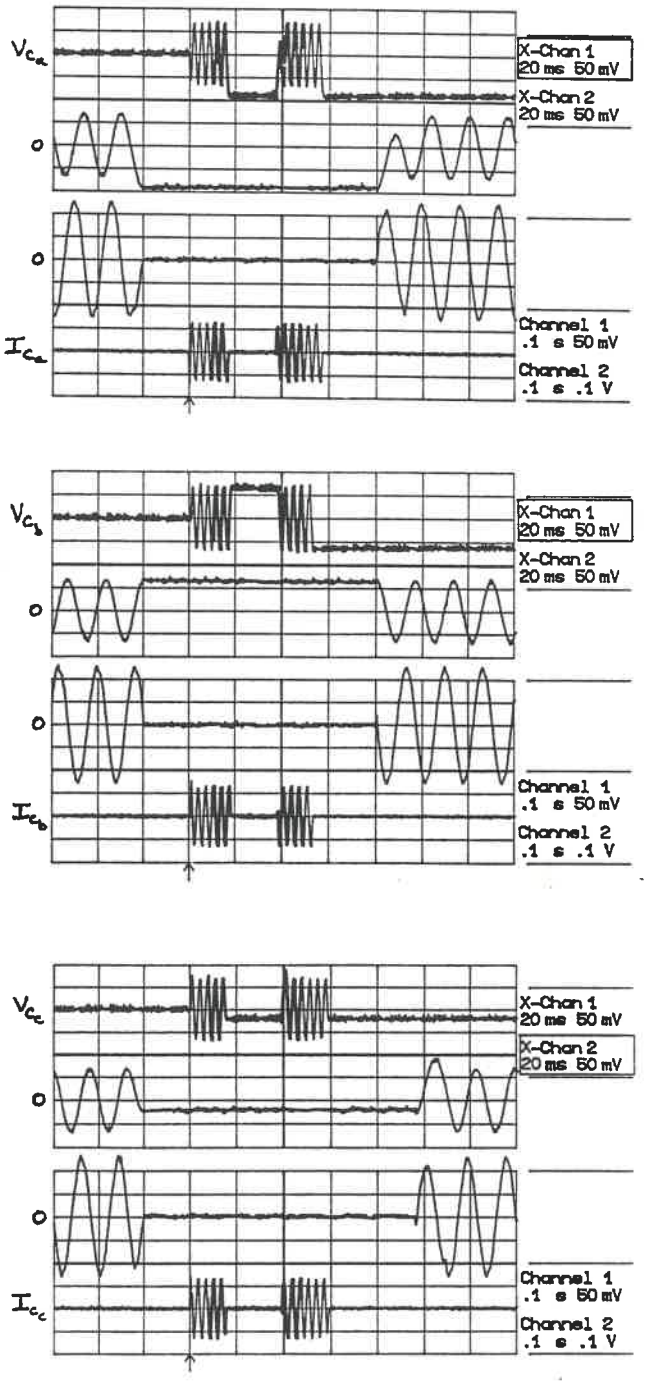
(a)

(b)

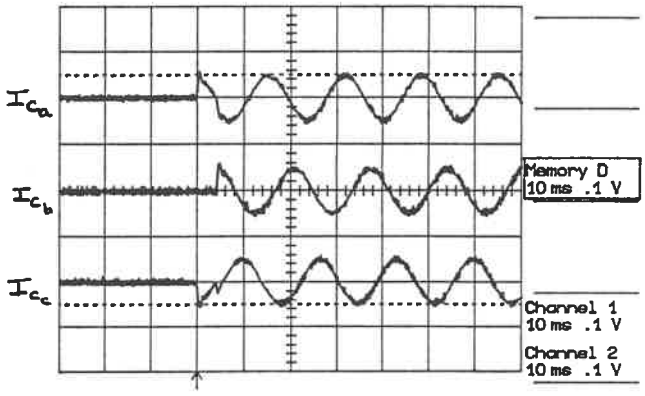
(c)



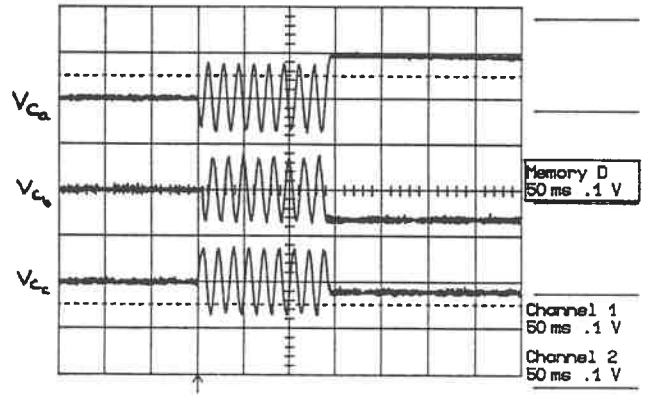
Plot 7.2 Capacitor currents in a Three-Wire Asymmetrical Line-Controller with a Wye-Connected Load.
(a) Phase A; (b) Phase B; (c) Phase C.
$V_{\Phi N}$=120V, I_{Ca}=21.5A



Plot 7.3 Switching in, out and in again a Three-Wire Branch-Controller with a Wye-connected Load
(a) Phase A; (b) Phase B; (c) Phase C
$V_{\Phi N}$=120V, $I_{C a}$=21.5A



Plot 7.4 Phase currents when switching in a Three-Wire Branch-Controller with a Wye-Connected Load
$V_{\Phi N}$=120V, $I_{C a}$=21.5A



Plot 7.5 Capacitor voltages when switching a Three-Wire Branch-Controller with a Wye-Connected Load
$V_{\Phi N}$=120V, $I_{C a}$=21.5A

CHAPTER EIGHT

THREE-WIRE NEUTRAL POINT-CONTROLLER WITH WYE-CONNECTED LOAD

8.1 - Introduction:

In this configuration, three thyristors must be fired before the capacitive load will be fully connected to the source. Two general cases present themselves:

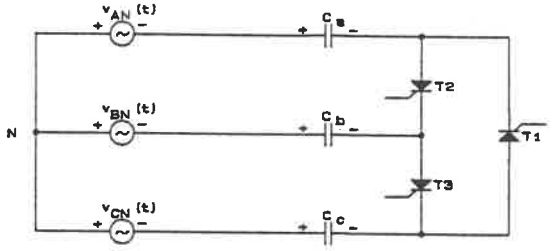


Fig. 8.1 Circuit diagram of a Three-Wire Neutral Point-Controller with a Wye-Connected Load

8.2 - Analysis:

Case a: fire T1

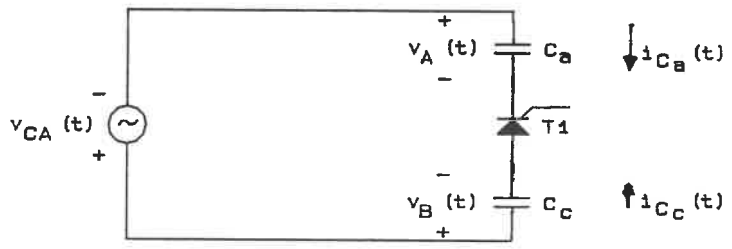


Fig. 8.2 Equivalent circuit of case a where T1 is fired

So long as $i_{Cc} > 0$, we know that Kirchhoff's voltage law requires that:

$$v_{Ca}(t) = \frac{1}{C_A}\int_0^t i_{Cc}\,dt + v_{Ca}(0^-) + \frac{1}{C_c}\int_0^t i_{Cc}\,dt + v_{Cc}(0^-)$$

note that $i_{Cc} = -i_{Ca}$

After transforming, solving for $I_{Cc}(s)$, and then finding the inverse transform we see that:

$$i_{Cc}(t) = \frac{C_a \cdot C_b}{C_a + C_b}\left[(V_{CAmax}\sin\theta_{CA} + v_{Ca}(0^-) - v_{Cc}(0^-)\right]\cdot\delta(t)$$

$$+ \quad \frac{C_a \cdot C_b}{C_a + C_b}\left[\, V_{CAmax}\omega_o\cos(\omega t + \theta_{CA})\right]$$

N.B.: this is only true so long as T1 is conducting

i.e. $t \leq (\pi/2 - \theta_{CA})/\omega$

for $t > (\pi/2 - \theta_{CA})/\omega$ $\quad i_{Cc} = 0$

Consequently the conditions for switching without transients are:

$$V_{CA}\sin\theta_{CA} = V_{Cc}(0^-) - V_{CA}(0^-)$$

This shows that thyristor 1 should be fired when the voltage across T1 is zero.

Case b: fire thyristors T2 and T3 while T1 continues to be triggered.

This case is quite a bit more complex. We want to determine when T2 and T3 should be fired. It should be noted that while T1 is still being triggered, it may not be conducting. This would occur if the sum of the voltages stored across C_a and C_c is equal to the magnitude of the line voltage.

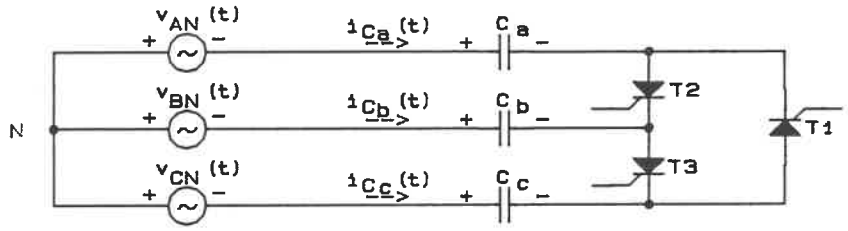


Fig. 8.3 Equivalent circuit of case b where T2 and T3 are fired while T1 continues to conduct

The equivalent circuit of case b is shown in Fig. 8.3. The question to be answered is: when can the various neutral points (currently separated by thyristors) be joined together without transients occurring?

We know that under balanced conditions:

$$I_{aA}+I_{bB}+I_{cC}=0$$

where:
$$I_{aA}=sC_a(V_{AN}-V_0)-C_a v_{AN}(0^-)$$
$$I_{bB}=sC_b(V_{BN}-V_0)-C_b v_{BN}(0^-)$$
$$I_{cC}=sC_c(V_{CN}-V_0)-C_c v_{CN}(0^-)$$

solving for v_0 yields:

$$V_0 = \frac{1}{3}\left[\left(v_{AN} - \frac{v_{Ca}(0^-)}{s}\right) + \left(v_{BN} - \frac{v_{Cb}(0^-)}{s}\right) + \left(v_{CN} - \frac{v_{Cc}(0^-)}{s}\right)\right]$$

since $C_a = C_b = C_c$

Transforming, solving for $I_{Cb}(s)$ and then finding the inverse transform yields:

$$\begin{aligned} i_{Cb} = {} & (C_b/3)\cdot\{ (V_{BCmax}\cdot\sin\theta_{BC} - V_{Cb}(0^-) + V_{Cc}(0^-) \\ & - V_{ABmax}\cdot\sin\theta_{AB} - V_{Cb}(0^-) + V_{Ca}(0^-) \} \cdot \delta(t) \\ & + (C_b/3)\cdot\{ V_{BC}\omega_o\cos(\omega t+\theta_{BC}) - V_{AB}\omega_o\cos(\omega t+\theta_{AB}) \} \end{aligned}$$

In like manner we find that:

$$\begin{aligned} i_{Ca} = {} & (C_a/3)\cdot\{ (V_{ABmax}\cdot\sin\theta_{AB} - V_{Ca}(0^-) + V_{Cb}(0^-) \\ & - V_{CAmax}\cdot\sin\theta_{CA} - V_{Cc}(0^-) + V_{Ca}(0^-) \} \cdot \delta(t) \\ & + (C_a/3)\cdot\{ V_{BC}\omega_o\cos(\omega t+\theta_{BC}) - V_{AB}\omega_o\cos(\omega t+\theta_{AB}) \} \end{aligned}$$

$$\begin{aligned} i_{Cb} = {} & (C_c/3)\cdot\{ (V_{CAmax}\cdot\sin\theta_{CA} - V_{Cc}(0^-) + V_{Ca}(0^-) \\ & - V_{BCmax}\cdot\sin\theta_{BC} - V_{Cb}(0^-) + V_{Cc}(0^-) \} \cdot \delta(t) \\ & + (C_c/3)\cdot\{ V_{CA}\omega_o\cos(\omega t+\theta_{CA}) - V_{BC}\omega_o\cos(\omega t+\theta_{BC}) \} \end{aligned}$$

Hence the conditions for switching without transients are:

$V_{BCmax}\cdot\sin\theta_{BC} = V_{Cb}(0^-) - V_{Cc}(0^-)$

$V_{ABmax}\cdot\sin\theta_{AB} = V_{Ca}(0^-) - V_{Cb}(0^-)$ and

$V_{CAmax}\cdot\sin\theta_{CA} = V_{Cc}(0^-) - V_{Ca}(0^-)$

It is important to note that when these conditions are satisfied, the voltages across T2 and T3 are zero. Consequently, this shows that T2 and T3 should be fired when the voltages across each of them are zero.

Turn Off:

We will now examine the turning off process. Upon receiving the command to turn off the thyristors, the gate signal to each thyristor is removed. However, this does not mean that the thyristors are turned off. A thyristor only turns off when the current flowing through it decreases to zero. In this particular configuration it is the line current which must decline to zero before the thyristors will stop conducting. If we examine the same case that is depicted in Fig. 8.5, we note that when the line current is zero (i.e. $i_{aA} = 0$), the corresponding capacitor voltages are: $V_{Ca} = V_{AN}$, $V_{Cb} = -0.5 \cdot V_{BN}$, $V_{Cc} = -0.5 \cdot V_{CN}$. Consequently, these are the conditions that exist immediately after thyristor 2 stops conducting.

As soon as T2 stops conducting the circuit topology changes; we no longer have a three phase source, but rather a single phase source connected directly across the series connection of C_b and C_c. We note that at the instant T2 stops conducting the new source voltage V_{BC} equals the load voltage $V_{Cb} - V_{Cc}$, which equals zero. Kirchhoff tells us the sum of the load voltages must always equal zero. Therefore, as V_{BC} rises to the peak line voltage, V_{Cb} has to increase at the rate of half the source voltage. Likewise, V_{Cc} has to decrease at the same rate. If this does not happen the load voltages will not be balanced.

At the instant that V_{Cb} is charged to the peak line voltage, the corresponding line current i_{bB} will decline to zero. It is at this moment that we can consider the capacitor bank disconnected from the source. We note that the final voltages are:

$$V_{Ca} = V_{LNmax} = 170.0V \text{ (as before);}$$

$$V_{Cb} = (-0.5+0.866) \cdot V_{LNmax} = 62.2V;$$

$$V_{Cc} = (-0.5-0.866) \cdot V_{LNmax} = -232.2V.$$

Turning On Again:

It is not possible to rapidly switch a Three-Wire Neutral Point-Controller with a Wye-Connected Load. What one has to do is to wait for the voltages across the phase capacitors to decay. In the lab we noticed that while the capacitors did not need to be fully discharged, the voltages across all capacitors had to be less that 170V.

If one attempts to rapidly switch the system on, off and on again, which is what we show in Fig. 8.6 and Plot 8.3, the system will respond by charging two capacitors to the peak voltages and completely discharging the third capacitor. The net result is that the delay is even longer than if one had initially waited. As a result, in any practical realization of this configuration some sort of "fixed delay" would need to be installed to ensure that the system will not try to turn on again until the capacitors have discharged sufficiently. Some of the information that would be needed to calculate this "fixed delay" would be the amount of resistance in parallel with each capacitor (apparently the C.S.A. requires that all banks of capacitors have resistance connected in parallel across them to ensure that they will not remain fully charged) and the theoretical result indicating the earliest possible time that capacitors, with voltages decaying from their final values, can be switched in again.

8.3 - Predictions of Circuit Behavior:

With this information we can predict how the circuit will perform in the stages of operation that interest us: 1) switching in a discharged capacitor; 2) switching out the capacitor; 3) switching in the charged capacitor.

1) SWITCHING IN A DISCHARGED CAPACITOR:

Thyristors should be gated when the voltage across them is zero.

The magnitude and direction of the current in the different phases depends on which thyristor is fired first and the polarity of the source voltage when the switch is closed. Nonetheless the magnitude of the largest current flowing through the thyristors will not exceed: $\pm i_{\Phi max}$.

2) SWITCHING OUT THE CAPACITOR:

Thyristors stop conducting when the corresponding line current $i_{\Phi}(t)=0$.

There are only three possible states that the capacitor bank could adopt after being switched off. The three possible final states are:

	A	B	C
V_{Ca}	170.0V	-232.2V	-232.2V
V_{Cb}	62.2V	170.0V	62.2V
V_{Cc}	-232.2V	62.2V	170.0V

3) SWITCHING IN CHARGED CAPACITOR:

Thyristors should be gated when the voltage across them is zero. However, it is important to wait until the voltages across all the capacitors have decayed to voltages below 170V, before one fires any of the thyristors. If one does not wait the required time before sending the turn on signal, two of the thyristors will be able to conduct but the third be blocked indefinitely. This is the situation simulated in Fig. 8.6 and shown in Plot 8.3. We note that since only two thyristors can conduct the capacitor bank becomes charges to a new final state: $V_{Ca} = -294V$; $V_{Cb} = 294V$; $V_{Cc} = 0V$. In practise it is still possible to eventually reconnect the capacitor bank to the source, however the delay will be longer than the orginal delay.

8.4 - Computer Plots of Expected Circuit Behavior:

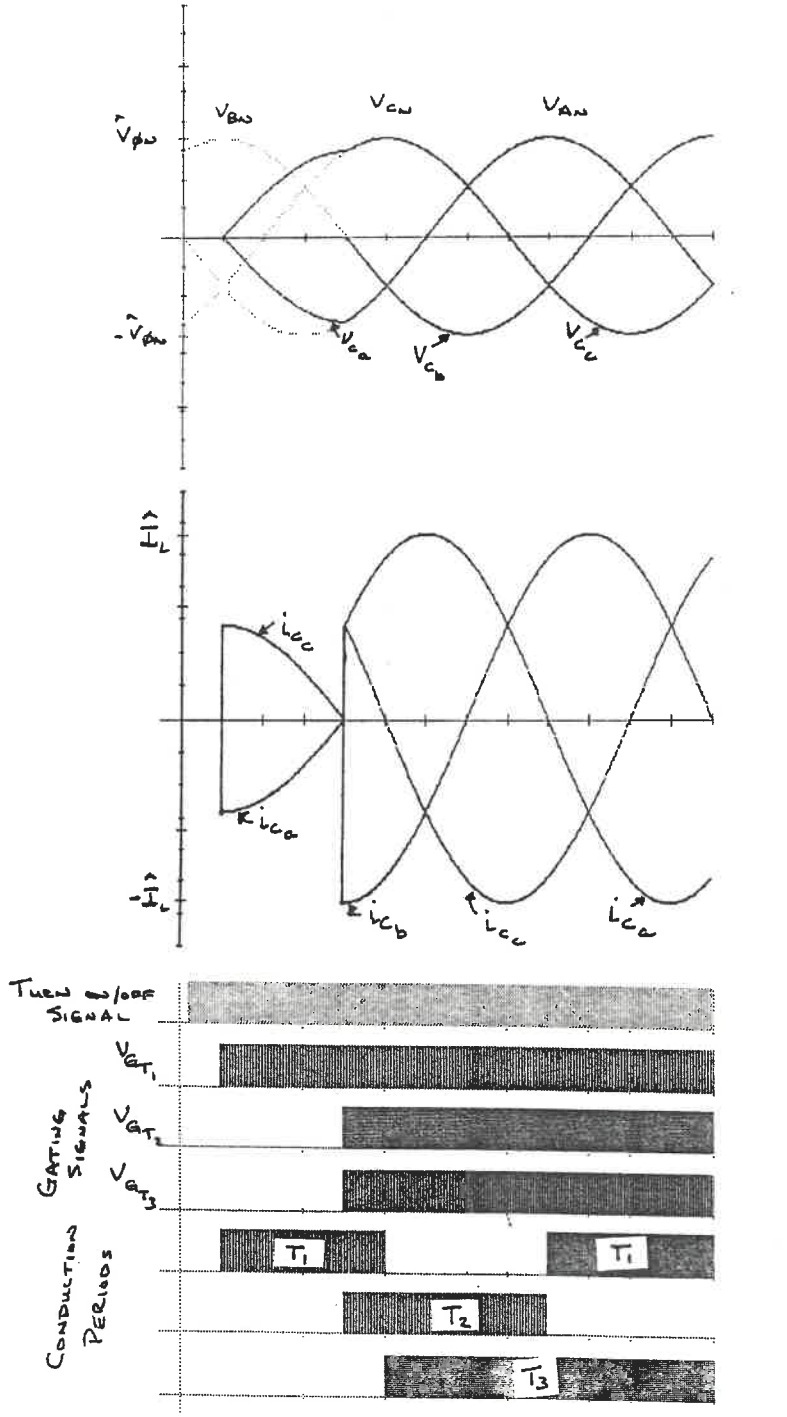


Fig. 8.4 Switching in a Three-Wire Neutral Point-Controller with a Wye-Connected Load; the capacitors are discharged

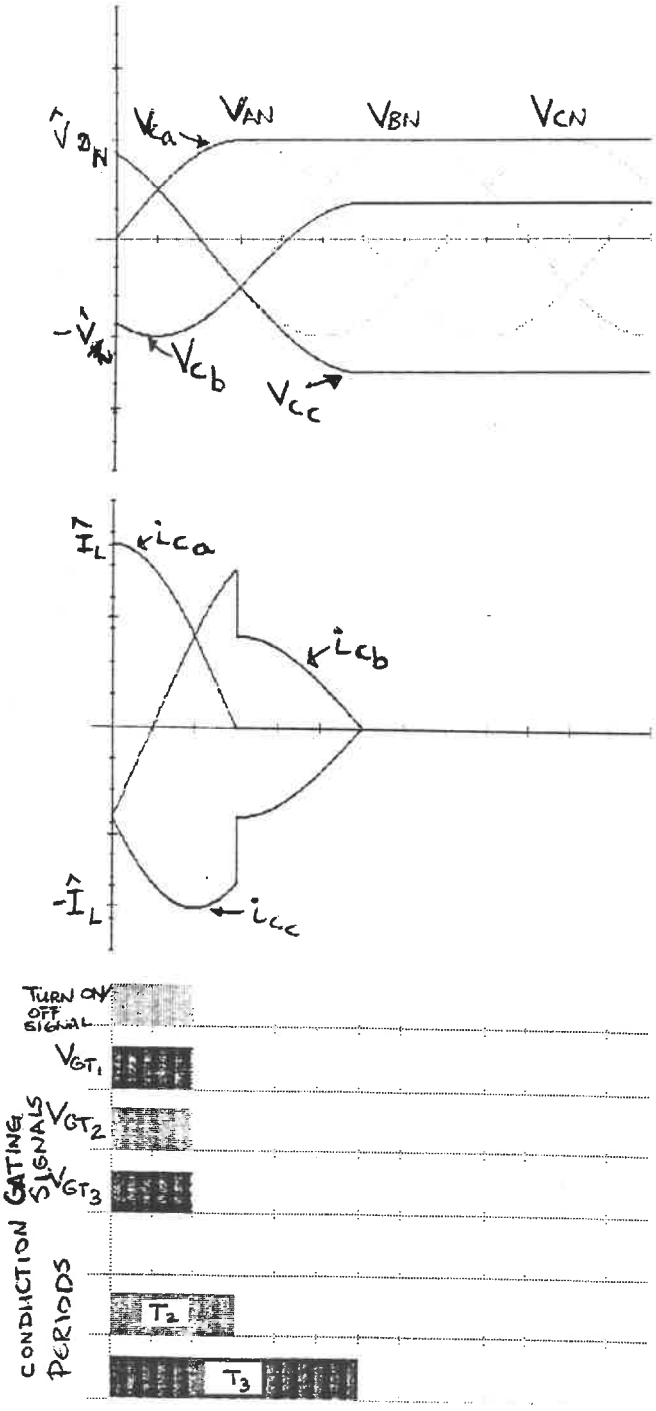


Fig. 8.5 Switching out a Three-Wire Neutral Point-Controller with a Wye-Connected Load

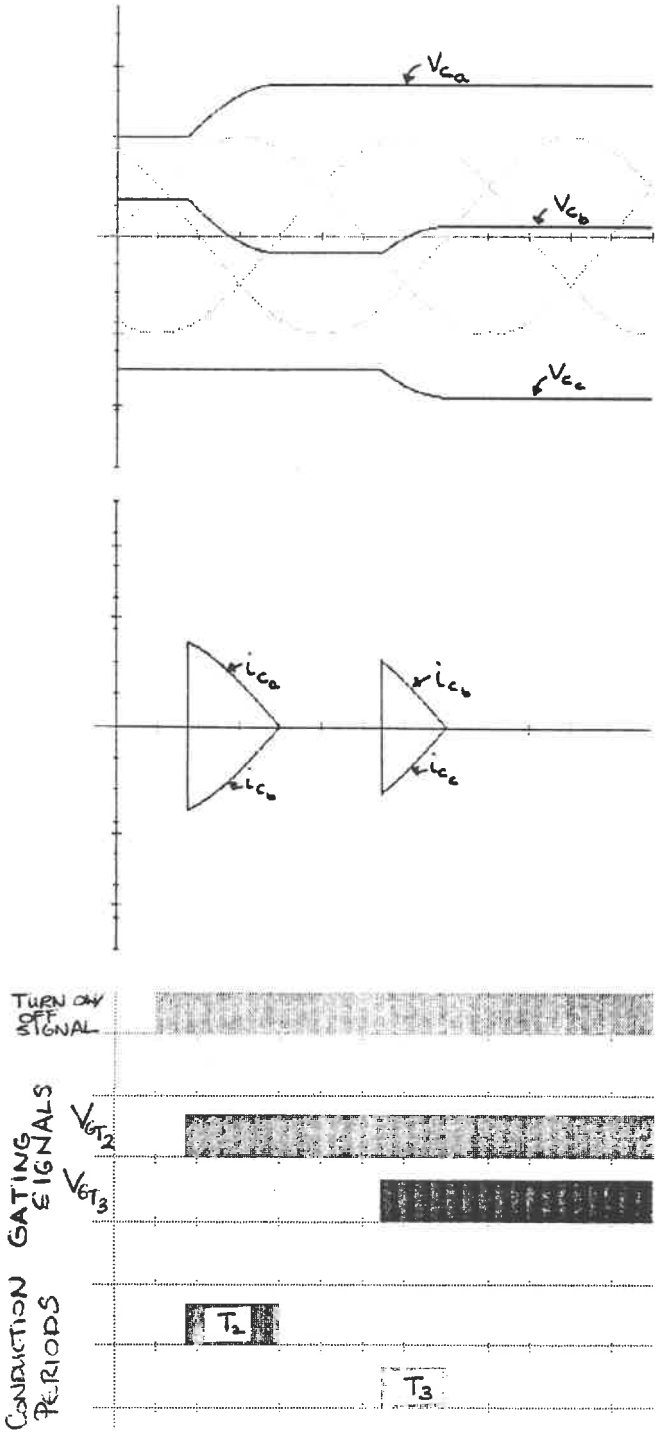


Fig. 8.6 Switching in again a Three-Wire Neutral Point-Controller with a Wye-Connected Load

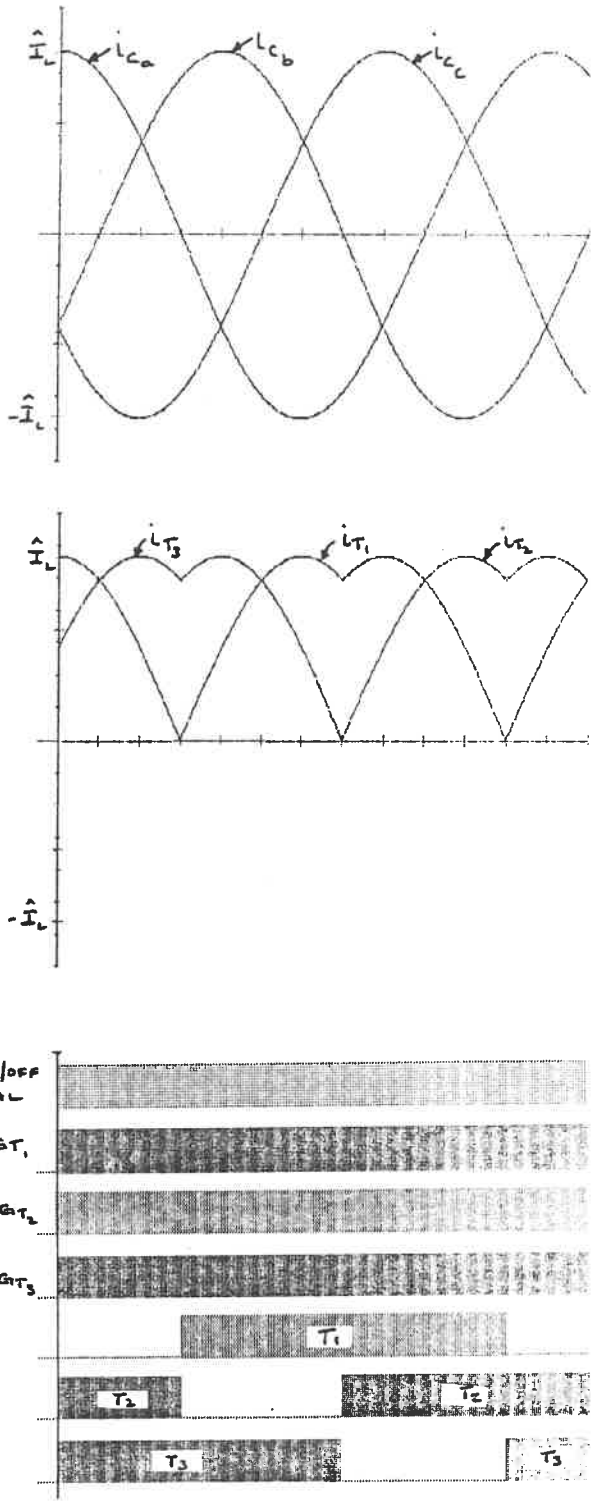
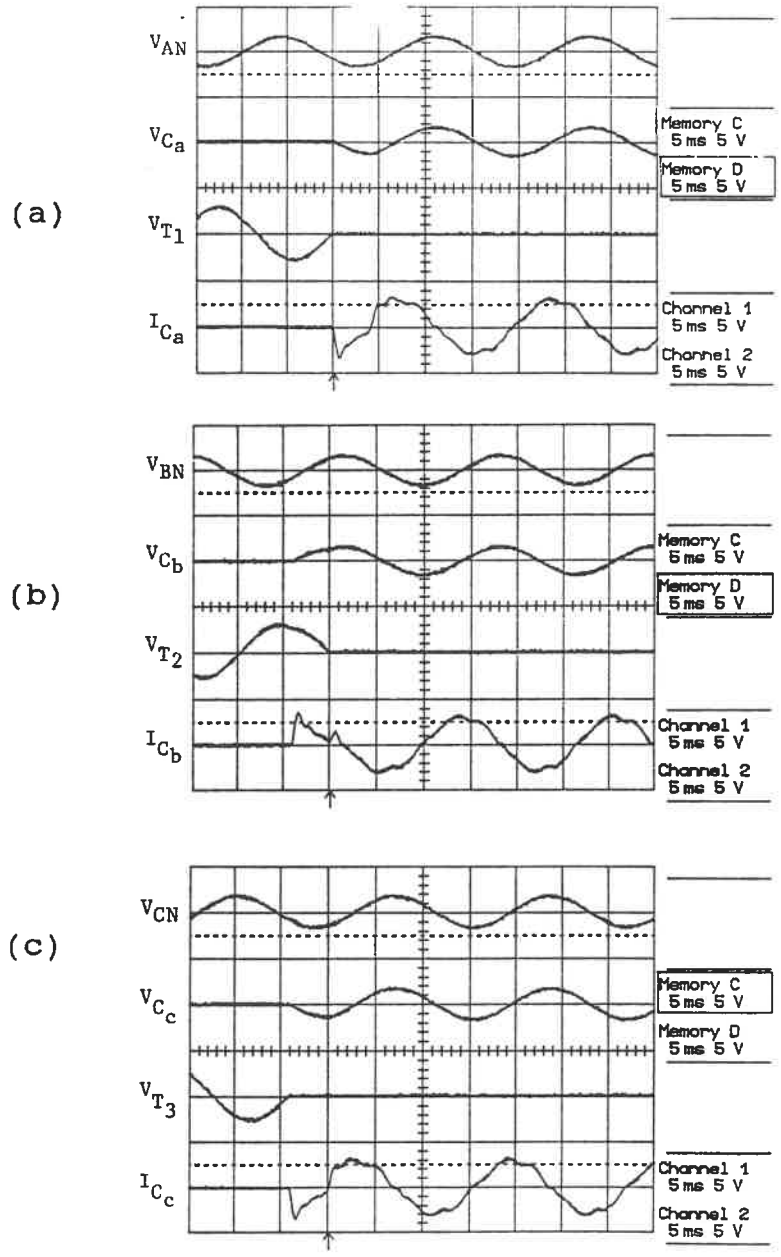


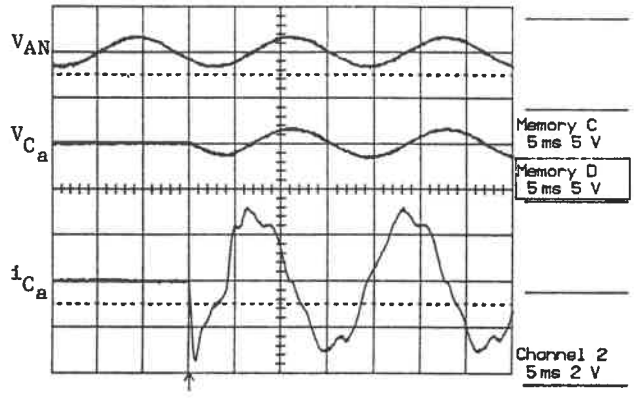
Fig. 8.7 Currents flowing in a Three-Wire Neutral Point-Controller with a Wye-Connected Load

8.5 - Experimental Results:

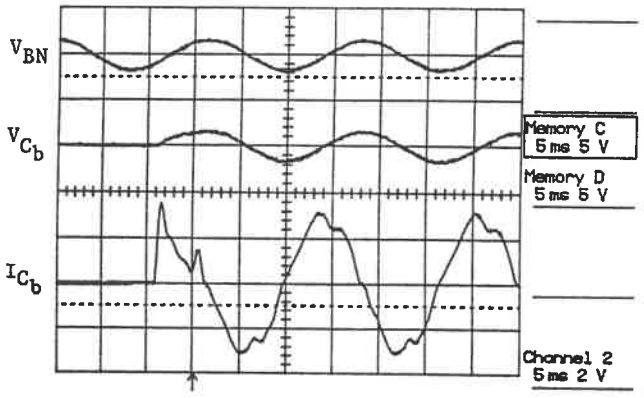


Plot 8.1 Switching in a Three-Wire Neutral Point-Controller with a Wye-Connected Load; the capacitors are discharged. (a) Phase A; (b) Phase B; (c) Phase C. $V_{\Phi N}$=120V, $I_{C a}$=21.5A

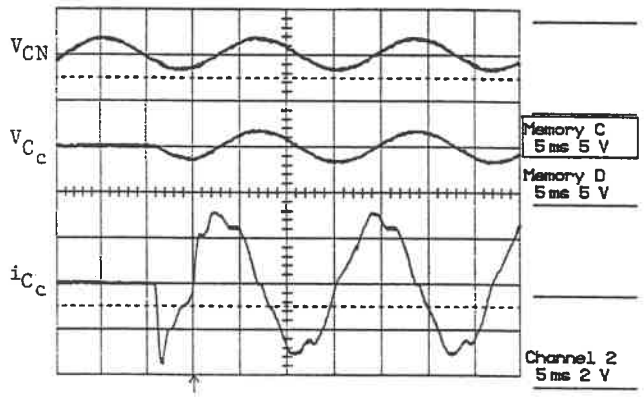
(a)



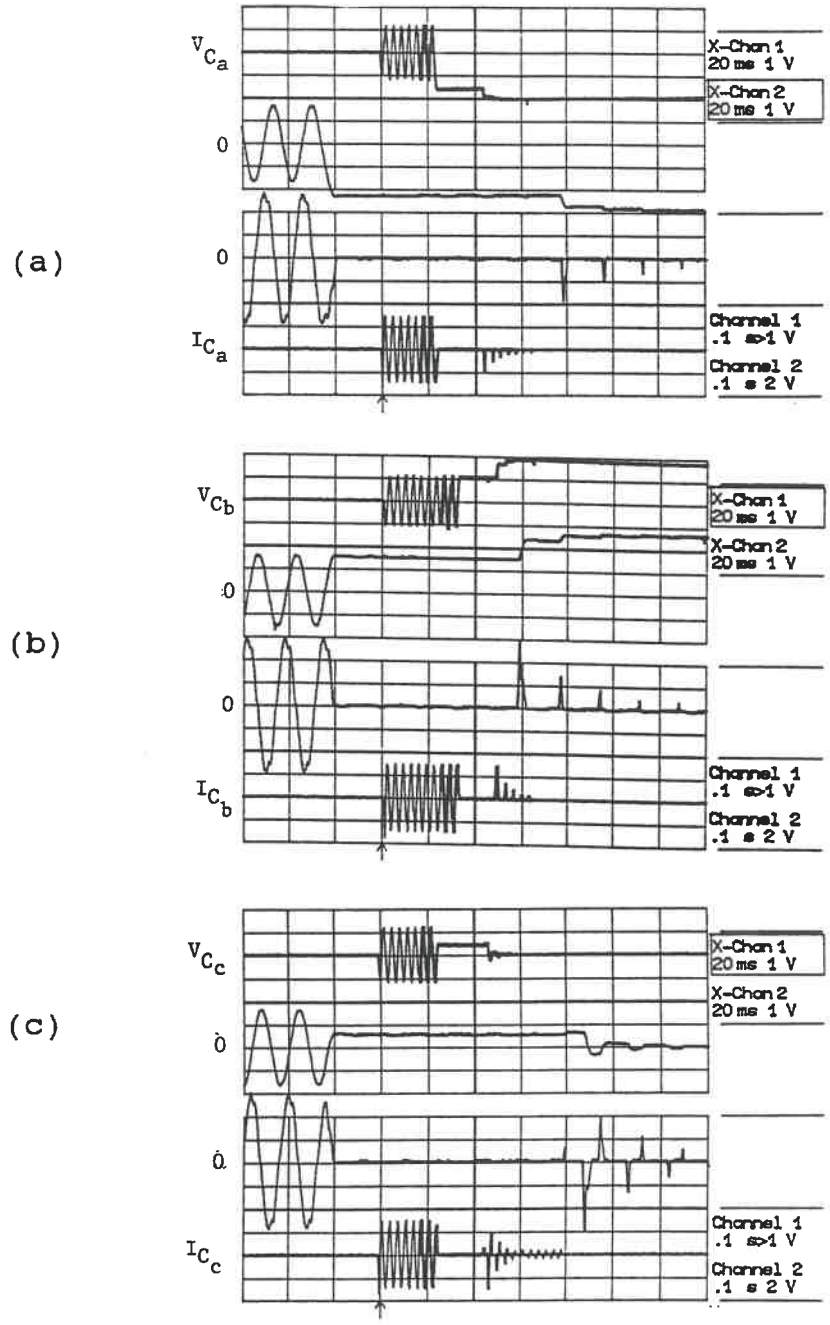
(b)



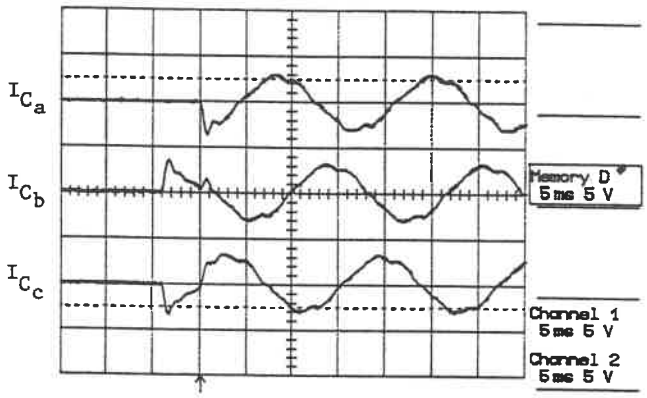
(c)



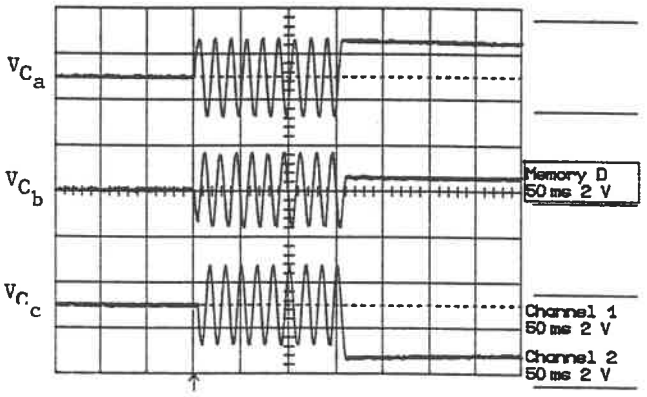
Plot 8.2 Capacitor currents in a Three-Wire Neutral Point-Controller with a Wye-Connected Load.
(a) Phase A; (b) Phase B; (c) Phase C.
$V_{\Phi N}$=120V, $I_{C a}$=21.5A



Plot 8.3 Switching in, out and in again a Three-Wire Neutral Point-Controller with a Wye-connected Load
(a) Phase A; (b) Phase B; (c) Phase C
$V_{\Phi N}$=120V, $I_{C a}$=21.5A



Plot 8.4 Phase currents when switching in a Three-Wire Neutral Point-Controller with a Wye-Connected Load
$V_{\Phi N}$=120V, $I_{C a}$=21.5A



Plot 8.5 Capacitor voltages when switching a Three-Wire Neutral Point-Controller with a Wye-Connected Load
$V_{\Phi N}$=120V, $I_{C a}$=21.5A

CHAPTER NINE

DISCUSSION

9.1 - Introduction:

Having presented the six different three phase "thyristor switches" in the preceding chapters, we will compare them in this chapter. Following the comparison, we will briefly detail some of the more difficult problems encountered during this research and suggest ways that they may be overcome in future work.

9.2 - Comparison of the "Thyristor Switches":

Three-Wire Branch-Controller with Delta-Connected Load

ADVANTAGES:
- Ease of control
- Switching phase current
- Rapid response
- Each phase is independent

DISADVANTAGES:
- Six thyristors
- Thyristors must block line voltage

Three-Wire Line-Controller with Delta-Connected Load

ADVANTAGES:
- Complete isolation of load when switch is open

DISADVANTAGES:
- Six thyristors
- Thyristors must block line voltage
- Slower response
- Switching line current

Three-Wire Asymmetrical Line-Controller with Delta-Connected Load

ADVANTAGES:
- Four thyristors

DISADVANTAGES:
- Thyristors must block line voltage
- Slower response
- Switching line current

Three-Wire Line-Controller with Wye-Connected Load

ADVANTAGES:
- Complete isolation of load when switch is open
- Thyristors block phase voltage

DISADVANTAGES:
- Six thyristors
- Slower response

Three-Wire Asymmetrical Line-Controller with Wye-Connected Load

ADVANTAGES:
- Four thyristors
- Thyristors block phase voltage

DISADVANTAGES:
- Slower response

Three-Wire Neutral Point-Controller with Wye-Connected Load

ADVANTAGES:
- Three thyristors

DISADVANTAGES:
- Thyristors must block line voltage
- Thyristors conduct for 2*T/3 & not T/2
- Switching line current
- Slower response
- Cannot be retriggered before all capacitor voltages have decayed below 170V

9.3 - Common Evaluation:

A common evaluation of the six thyristor switches is presented in Table 9.1. It would therefore be helpful to examine the different criterion used in this evaluation.

Criterion 1: Number of Thyristors

This criterion is self evident.

Criterion 2: Repetitive Peak Voltage across capacitors

This is the maximum voltage to which any one of the phases of the capacitor bank can be charged:

W33AA can be charged to maximum of $\sqrt{2}\cdot V_{LL}$ (see pg. 26)

W33AD & W32AD can be charged to a maximum of

$(\sqrt{3}/2 + 0.5)\cdot\sqrt{2}\cdot V_{LL} = 1.932\cdot V_{LL}$ (see pg. 44)

W33AY & W32AY can be charged to a maximum of

$(0.5 + \sqrt{3}/2)\cdot\sqrt{2}\cdot V_{LN} = 1.115\cdot V_{LL}$ (see pg. 64)

U33DA can be charged to a maximum of

$(0.5 + \sqrt{3}/2)\cdot\sqrt{2}\cdot V_{LN} = 1.115\cdot V_{LL}$ (see pg. 79)

Criterion 3: Repetitive Peak Voltage across thyristors

This is the maximum steady state voltage which the thyristors would have to block:

W33AA must be able to block the voltage resulting from a fully charged capacitor and the source voltage reaching the peak line voltage i.e. $\sqrt{2}\cdot V_{LL} + \sqrt{2}\cdot V_{LL} = 2.828\cdot V_{LL}$

W33AD & W32AD must be able to block the voltage resulting from a fully charged capacitor and the source voltage reaching the peak line voltage

i.e. $1.932\cdot V_{LL} + \sqrt{2}\cdot V_{LL} = 3.346\cdot V_{LL}$

W33AY & W32AY must be able to block the voltage resulting from two fully charged capacitors and the source voltage reaching the peak line voltage. A worst case scenario for V_{T1} would exist with $V_{Ca} = 170V$, $V_{Cc} = -232.2V$, and $V_{CA} = -294V$ i.e. $0.817\cdot V_{LL} + 1.115\cdot V_{LL} + \sqrt{2}\cdot V_{LL} = 3.346\cdot V_{LL}$

U33DA must be able to block the voltage resulting from two fully charged capacitors and the source voltage reaching the peak line voltage. A worst case scenario for V_{T1} would exist with $V_{Ca} = 170V$, $V_{Cc} = -232.2V$, and $V_{CA} = -294V$ i.e. $0.817\cdot V_{LL} + 1.115\cdot V_{LL} + \sqrt{2}\cdot V_{LL} = 3.346\cdot V_{LL}$

Criterion 4: RMS On-state Current (In one thyristor)

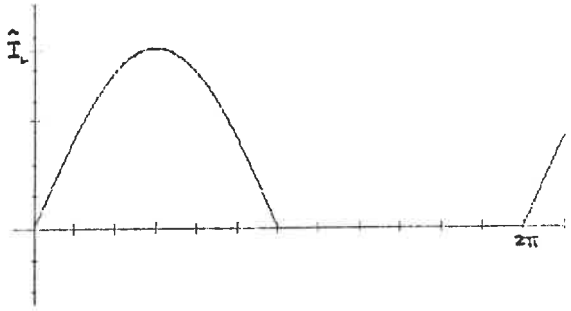


Fig. 9.1 A half-wave rectified sinusoidal current

The rms value of the half-wave rectified sinusoidal current shown in Fig. 9.2 is: $I_{rms} = I_{max}/2$. This will be useful in calculating the rms currents flowing through the thyristors, since in all but the last configuration each thyristor carries only half of the available current.

W33AA has a peak current of $I_{max} = \sqrt{2} \cdot I_\Phi = \sqrt{2} \cdot I_L / \sqrt{3}$ hence the rms current flowing in each thyristor is

$$I_{rms} = (0.5 \cdot \sqrt{2} \cdot I_L)/\sqrt{3} = 0.408\ I_L$$

W33AD & W32AD have peak currents of $I_{max} = I_L$ hence the rms current flowing in each thyristor is $I_{rms} = 0.707 \cdot I_L$

W33AY & W32AY have peak currents of $I_{max} = I_L$ hence the rms current flowing in each thyristor is $I_{rms} = 0.707 \cdot I_L$

U33DA is a special case. The current flowing through the thyristors is made up of different segments of the sinusoidal line currents; the current flowing through T1 is shown below in Fig. 2. The resulting rms current is:

$I_{rms} = 0.577 \cdot I_{max} = 0.577 \cdot \sqrt{2} \cdot I_L = 0.816 I_L$

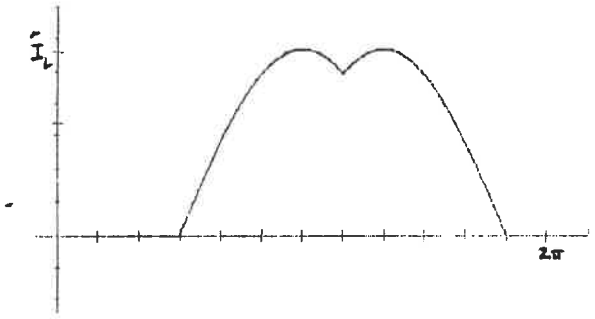


Fig. 9.2 Thyristor current in a Neutral Point-Controller with a Wye-Connected Load

Criterion 5: Switching Times

All of the switching times were calculated on a worst case basis. That is to say that it was assumed that the signal to change state would be received just after the system could have responded (i.e. in the case of turn on, we assumed that the command signal would arrive just after the voltage across the thyristors passed through zero). As a result the maximum delay was added to the system's response time. This sum is fair representation of the worst case switching times.

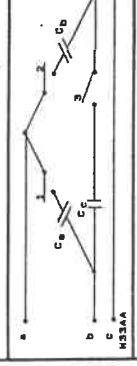
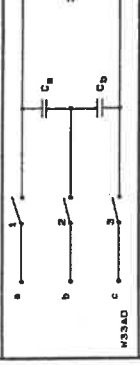
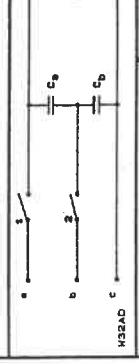
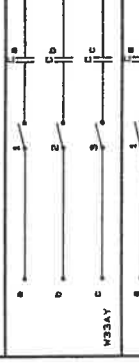
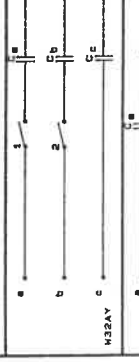
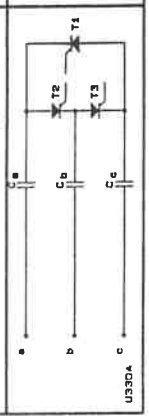
NOTE: =	Number of Thyristors	Repetitive Peak Voltage seen by the capacitors	Repetitive Peak Forward Volt. ...as seen by the thyristors	RMS On-state Current (In one thyristor)	Switching Times	
					t_{on} (max) with cap. bank discharged (cycles)	t_{off} (max) (cycles)	t_{on} (max) with cap. bank charged (cycles)
 M33AA	6	$1.414*V_{LL}$	$2.828*V_{LL}$	$0.408*I_L$	$\frac{6}{12}$	$\frac{6}{12}$	$\frac{12}{12}$
 M33AD	6	$1.932*V_{LL}$	$3.346*V_{LL}$	$0.707*I_L$	$\frac{5}{12}$	$\frac{4}{12}$	$\frac{20}{12}$
 M32AD	4	$1.932*V_{LL}$	$3.346*V_{LL}$	$0.707*I_L$	$\frac{7}{12}$	$\frac{6}{12}$	$\frac{20}{12}$
 M33AY	6	$1.115*V_{LL}$	$3.346*V_{LL}$	$0.707*I_L$	$\frac{5}{12}$	$\frac{5}{12}$	$\frac{21}{12}$
 M32AY	4	$1.115*V_{LL}$	$3.346*V_{LL}$	$0.707*I_L$	$\frac{7}{12}$	$\frac{7}{12}$	$\frac{21}{12}$
 U33DA	3	$1.115*V_{LL}$	$3.346*V_{LL}$	$0.816*I_L$	$\frac{7}{12}$	$\frac{7}{12}$	variable (depends on the size of cap. bank & discharge resistance)

Table 9.1 Common evaluation of the six three phase thyristor switches

9.4 - Problems and Suggested Solutions:

The most serious problem, which plagued me through out the research, was noise! The problem was aggravated by the fact that my control circuitry was mounted on bread boards. Often I had very impressive transients because external noise had caused a thyristor to be fired at the wrong moment. By way of example I include Fig. 9.1, which shows a current spike caused by noise generated by a relay. All control circuits needed a common on/off signal. This I provided by means of a three pole relay. The problem in this particular case was that the noise generated when I tried to rapidly switch the relay on and off caused the third thyristor in the Three-Wire Neutral Point-Controller with a Wye-Connected Load to be triggered thus releasing a lot of energy.

The principal suggestions I have as regards to noise is to mount the control circuits on their own Printed Circuit Boards; and secondly to use capacitors extensively in the control circuits.

The second annoying problem encountered throughout the research was the lack of a programmable master switch. It would have been very nice to have had a switch that could be, for instance, 1) turned on, 2) turned off for exactly three cycles and then 3) turned on again. Such a master switch would have greatly simplified the data collection in

addition to giving greater correlation between the different phases. If these thyristor switches are examined again it would certainly be worthwhile spending the time to design the aforementioned master switch.

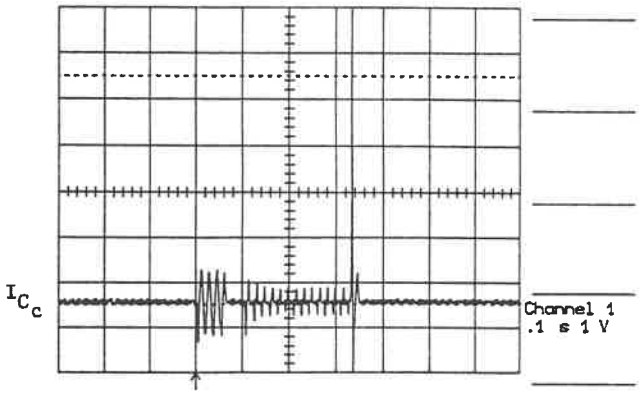


Fig. 9.3 Current spike caused by noise
I_{ϕ}=21.5A, I_{peak}>600A

CONCLUSION

It is possible to switch banks of capacitors with thyristor switches without transients. In demonstrating this fact, both theoretically and experimentally for six different configurations of three phase thyristor switches, we have accomplished the principal objective of our research.

Our secondary objective was to carry out a preliminary characterization of the six different configurations. This was accomplished and is presented with the aid of over one hundred and fifty oscillograms and computer plots. Together they present a comprehensive picture of what is actually going on within the controllers.

The application of thyristors in switching banks of capacitors has a very promising future in a world that is looking to use its energy resources more efficiently.

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APPENDIX A

REACTIVE POWER CONTROL AND THE USE OF THYRISTOR SWITCHED CAPACITORS

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ECOLE POLYTECHNIQUE DE MONTREAL

November 30, 1989

INTRODUCTION:

Interest in reactive power control continues to grow as the need for a more efficient and more reliable electric supply increases. Compensators are devices that can compensate for the reactive power generated or absorbed by the load and thereby control the reactive power seen by the source. There are many different types of compensators which can be used for compensation in the electrical systems but this paper focuses on the use of static capacitors connected in parallel.

The paper is divided into two parts. The first part is a literature study on reactive power control. Beginning with a very broad focus, namely giving reasons for the current interest in reactive power control, the study gradually narrows its focus onto ways in which shunt capacitors have traditionally be used in compensation schemes. As such part 1 gives the frame work, in a sense the "raison d'être", for the subsequent analysis. Part 2 is an analysis detailing ways in which capacitors can be used more effectively in compensation schemes when switched with thyristor ac power controllers.

PART I

The Interest in Reactive Power Control:

The efficient use of energy resources is presently a major concern for our society. Part of this concern stems from a greater awareness that the cost of the manufactured goods we buy is directly related to the cost of the energy used in production. But perhaps the greater part of the concern stems from the realization that our energy resources are not infinite and that we must therefore, manage them wisely. The importance of wise management in order to optimize efficiency has long been appreciated by the electric industry. Reactive power control has been one of the ways they have employed to manage our energy resources more efficiently.

Interest is reactive power control has grown in recent years for several reasons. These include:

1) the need for a more efficient operation of power systems resulting from the increasing price of fuels;

2) the need to transmit as much power as possible on existing transmission networks because high interest rates and occasional difficulties in obtaining right of way have curtailed in general the extension of existing networks.;

3) the problems of stability and voltage control in long distance transmission;

4) the need for a high quality of supply because of the increasing use of electronic equipment (especially computers and colour television receivers) and because of the growth of continuous process industries;

5) the need for reactive power control on the ac side of converters involved in dc transmission schemes. (1)

Reactive power control can 'go a long way' in resolving these problems and needs. As examples consider that for a given distribution of power the losses can be reduced by minimizing the total flow of reactive power. Similarly for a given transmission line with a fixed capacity, the amount of power sent can be increased if the flow of reactive power is minimized. Also the quality of a supply, most often measured by its stability and its voltage regulation, depends on reactive power control. But why control reactive power rather than just eliminate it?

Reactive power is consumed by most of the network elements as well as most of the consumer loads so it has to be supplied somewhere. It could be supplied by the electric authority, but this would mean that much more current is generated than is theoretically needed. As was indicated earlier this would cause increased I^2R and I^2X losses. It would also impose a physical constraint on the amount of real power supplied since the generators have to withstand the rated voltage and current regardless of the power

delivered.

As reactive power is not easily transmitted it is usually preferable to generate it where it is needed. In fact power systems are usually sized according to the maximum demand and the reactive power demand is met with compensators and other equipment which can be deployed more flexibly than generating units and which make no contribution to fault levels.

Power Factor - a measure of reactive power:

Frequently the demand for reactive power is quantified in terms of the power factor (a low power factor corresponds to a high demand for reactive power). By universal definition the power factor is 'the factor by which the apparent power must be multiplied to obtain the average power.' (2)

Power factor = average power/apparent power

Unity power factor is achieved when the average power P_s equals the apparent power S_s. In that instance the reactive power as seen from the source is zero: $Q = S^2_s - P^2_s = 0$. From the supply authorities point of view this is the ideal operating condition.

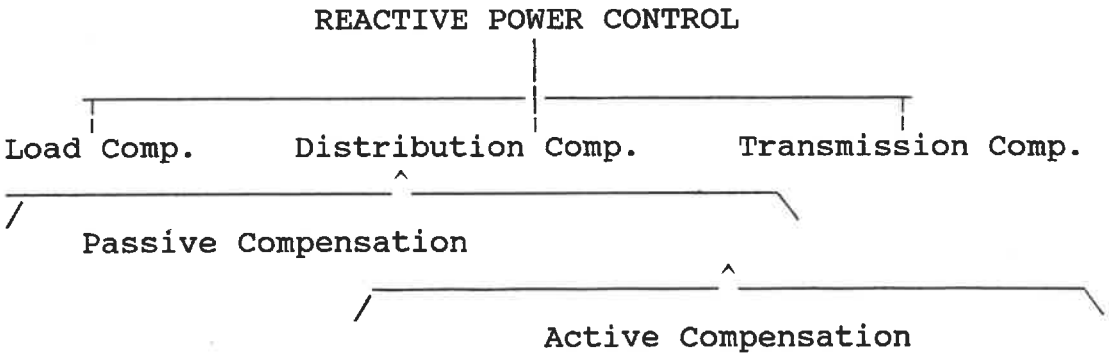
For most industries, however, the difference between the ideal of unity power factor and the actual power factor is quite substantial. As a result either the consumer or the supply authority has to compensate for the reactive power consumed or absorbed by the load. In actual fact both compensate but it is worth noting that the complex tariff structure set by the supply authority is meant to encourage consumers to improve their power factor and to penalize those who do not.

TYPICAL POWER FACTORS ENCOUNTERED IN INDUSTRY:

Textile	0.65/0.75	Steel works	0.6/0.85
Chemical	0.75/0.85	Plastic moulding	0.6/0.75
Machine shops	0.4/0.65	Printing	0.55/0.7
Breweries	0.75/0.8	Quarries	0.5/0.7
Coreless ind. furnaces	0.15/0.4	Rolling mills (thyristor drives)	0.3/0.75 (3)

There are several types of compensation; each type draws its name from its location in the electrical system. Hence there is load compensation, distribution compensation and transmission compensation. Naturally the amount of reactive power controlled increases as one moves from local level compensation to system compensation. There are also two general groups of compensator: 1) passive compensators - devices which may be either permanently connected or switched but which generally are incapable of continuous (i.e. stepless) variation; 2) active compensators - usually

shunt-connected devices which tend to maintain almost constant voltage at their terminals, this they do by rapidly and continuously absorbing or generating the exact amount of reactive power resulting from small variations in voltage at their point of connection. Illustrated below are the various groups and types of compensation.



The Objectives of Compensation:

The objectives for all groups of compensation are essentially the same. What varies is the importance attributed to each objective, and this varies according to where in the electric system compensation is taking place. For instance, power factor correction is the most important objective for the consumer, hence it is the primary objective in load compensation. Whereas voltage regulation and improvement of power system stability are the key objectives for the utility therefore they are the primary objectives in transmission compensation. Tables shown below summarize the objectives for load and transmission compensation. The priorities for distribution compensation would depend to a large extent on whether it was owned by the consumer or the utility.

OBJECTIVES IN TRANSMISSION COMPENSATION:
1) Maintain voltage at or near a constant level
- under slowly varying condition due to load changes
- to correct voltage changes due to unexpected events (e.g. load rejections, generator and line outages)
- to reduce voltage flicker caused by rapidly fluctuating loads (e.g. arc furnaces)
2) Improve power system stability
- by supporting the voltage at key points (e.g. the mid-points of a long line)
- by helping improve voltage swing
3) Improve power factor
4) Correct phase unbalance

OBJECTIVES IN LOAD COMPENSATION:
1) Power factor correction
2) Improvement of voltage regulation
3) Load balancing

(1)

An ideal compensator, capable of meeting all objectives for any type of compensation, would satisfy three key specifications.

It would: 1) Provide a controllable and variable amount of reactive power precisely according to the requirements of the load, and without delay
2) Present a constant-voltage characteristic at its terminals
3) Be capable of operating independently in the three phases. (1)

But as we live is a less than ideal world there are economical and technical factors which must be taken into account. Points which must be considered when evaluating any proposed compensator include:

1) Reliability of the equipment to be installed
2) Probable life
3) Capital cost
4) Maintenance cost
5) Running cost
6) Space required and ease of installation (3)

There is a variety of equipment that can supply or absorb reactive power. These include synchronous condensers, shunt reactors, series capacitors or shunt capacitors. This project focuses specifically on ways in which parallel static capacitors can be used in various compensation schemes.

Shunt capacitors are widely used in compensation schemes. This is due in large part to the fact that most electrical loads are inductive and hence require capacitive compensation. But there are also several advantages in

using capacitors. These include: 1) low initial cost; 2) minimal upkeep costs; 3) compact size; 4) reliability; 5) high efficiency and 6) ease of installation. (3)

Capacitors are usually installed in one of three ways: as fixed capacitance connected directly across the load; in banks of capacitors which can be switched into or out of a particular system or as part of a continuously controlled static compensator usually called a TSC (Thyristor Switched Capacitor).

FIXED CAPACITANCE:

This is the most rudimentary form of compensation. An example of where it could successfully be applied would be in a machine shop where there are a large number of similar motor loads. In that context capacitors could be connected across the individual loads - hence they would supply a fixed amount of reactive power whenever the motor was in operation.

Generally it is not advisable to have a fixed capacitance connected to a plant's main distribution bus unless the plant is engaged in continuous process work. Longland cites several reasons why large blocks of capacitors cannot be left connected to their distribution systems at light loads:

1) Increases in system voltage normally associated with light-load conditions will be amplified by the presence of capacitive loads and may well reach values which are unacceptable to voltage-sensitive devices which may, of necessity, be connected to the supply permanently (e.g. tungsten and fluorescent lighting, solid state devices, computers)
2) Increased copper losses
3) Possibility of instability of generating plant and system operation generally
4) Increase in voltage regulation may cause oversaturation of the transformer cores resulting in the generation of harmonic currents and hence the possibility of harmonic resonance
5) Possibility of undesirable interaction between domestic and industrial loads
6) Depending on tariff structure it could incur financial loss. (3)

An improvement in the compensator's performance can be attained if the banks of capacitors can be switched in and out of the system.

SWITCHED CAPACITORS:

Traditionally capacitors have been switched automatically using a suitable contactor unit which is connected to the supply. Reactive current relays sense the amount of reactive component and then cause the segments of capacitor banks to be switched in or out as required. This allows for discrete changes in the compensating reactive power. This system of compensation has the advantage of being simple in principle and construction. The disadvantages are the presence of switching transients when segments of the bank are connected to the system and the fact that as a result of the discrete steps in compensating current the

control is usually quite coarse.

Smoother control could be achieved by operating the bank on a binary basis. In such a scheme a four segment capacitor bank could supply 2^4 or 16 different amounts of reactive power. But such a scheme would be difficult to implement reliably with mechanical contactors; it really would be preferable to use electronic switches. The main drawback to using thyristor switches is the cost. However, the price of power thyristors will likely continue to fall to the point where even the cost is one of the advantages of thyristor switches as compared with mechanical switches.

Thyristor switches (see Appendix B) switch capacitors better than mechanical switches. They are faster:

Thyristor switch:	1 cycle
Fastest available mechanical switch	2 cycles
Conventional capacitor switch	6-30 cycles

(1)

Thyristor switches are also more robust - they virtually have an unlimited switching life. Whereas the rapid accumulation of switching operations may cause mechanical problems in circuit breakers. Another very significant advantage of thyristor switches it the fact that they can be closed at precise instants in each phase thus eliminating transients when a capacitor bank is switched on line.

CONTINUOUSLY CONTROLLED STATIC COMPENSATORS - TSC:

The principle of Thyristor-Switched Capacitors is similar to the basic switched capacitor except emphasis is placed on the speed of commutation and the ability to continuously control the reactive power supplied. This is achieved by adjusting the susceptance through controlling the number of parallel capacitors in conduction. As there is always the problem of discrete steps an "interpolating reactor" is often used in parallel to smooth out these steps. The rapid and continuous response of TSCs enables them to enhance the system's stability and to dampen any oscillation that may occur.

One can easily understand that performance of the compensators is directly related to the complexity of control and the final cost of the system. Hence a TSC is far closer to the ideal compensator as defined earlier than a fixed capacitance scheme. However, the task of the engineer in this field of compensation is to determine the most economic combination of fixed, switched and continuously variable capacitance.

APPENDIX B

ELECTRONIC SWITCHES:

As the current and blocking voltage ratings of thyristors increase, so do the number of application where mechanical switches can be replaced with electronic switches.

In its simplest form an electronic switch is an arrangement of two inverse-parallel-connected thyristors. Such an arrangement is shown below.

Operation of an electronic switch is quite simple. When one wants to close the electronic switch, one simply sends triggering pulses to the gates of both thyristors. The thyristor which is forward biased will conduct so long as it has been triggered. To open the switch simply stop sending triggering pulses to the gates of both thyristors. The thyristor which was conducting at the moment when the triggering pulses ceased will continue to conduct until the current it is carrying goes to zero. From that moment on both thyristors will block the forward voltages unless triggered again.

An electronic switch, otherwise known as an ac static switch has several advantages:

1) has no contacts and is therefore not subject to wear
2) requires very little maintenance
3) simple starting procedure
4) available for use with minimum of delay

APPENDIX C

WORKING DOCUMENT FOR THE REVISION OF

Standard Definitions and Requirements for Thyristor AC Power Controllers

Prepared by

Static Power Converter Committee of the
IEEE Industry Applications Society

3.8.7 Latching Current (Thyristor). The minimum principal current required to maintain the thyristor in the ON-state immediately after switching from the OFF-state to the ON-state has occured and the triggering signal has been removed.

3.8.8 Principal Voltage. The voltage between the main terminals.

NOTE: (1) In the case of reverse blocking and reverse conducting thyristors, the principal voltage is called positive when the anode potential is higher than the cathode potential, and called negative when the anode potential is lower than the cathode potential.
(2) For bi-directional thyristors, the principal voltage is called positive when the potential of main terminal 2 is higher than the potential of main terminal 1.

3.8.9 Principal Current. A generic term for the current through the anode junction.

NOTE: It is the current through both main terminals.

4. Classification Code

Basic Control Element

Number of Line Phases

Number of Basic Control Elements

Controller Connection

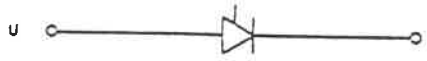
Load Connection

U	1	1	A	A
V	3	2	D	D
W	·	3	Y	Y
	·	·	N	N
	·	·		X
		·		

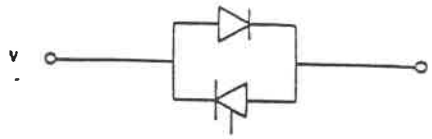
For circuit examples, see Appendix A.

4.1 Basic Control Elements Used in the Classification Code

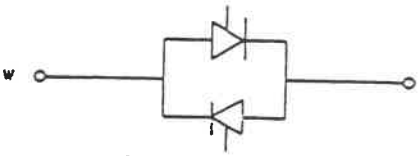
4.1.1 Unidirectional Control — Reverse Blocking. A configuration which permits control only in one direction of current flow and block in the opposite direction.



4.1.2 Unidirectional Control — Reverse Conducting. A configuration which permits control only in one direction and conducts uncontrolled in the reverse direction.



4.1.3 Bidirectional Control. A configuration which permits control in both directions of current flow. The control may be either symmetrical or asymmetrical.



NOTE: It is possible to obtain the same control characteristics as in U, V, W by other thyristor or thyristor/diode connections, or both.

4.2 Controller Connections. The following controller connections are used in the classification code:

A = open (neither D, Y, or N)
D = delta
Y = star
N = star with neutral connected

4.3 Load Connections. The following load connections are used in the classification code:

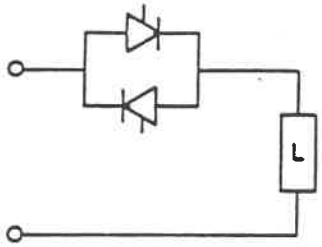
A = open (neither D, Y, or N)
D = delta
Y = star
N = star with neutral connected
X = optional (either A, D, Y, or N)

5. Service Conditions

Service conditions are all external factors (ambient temperature, air humidity, character of load, character of ac source, etc) which may have an influence on the performance of an ac power controller.

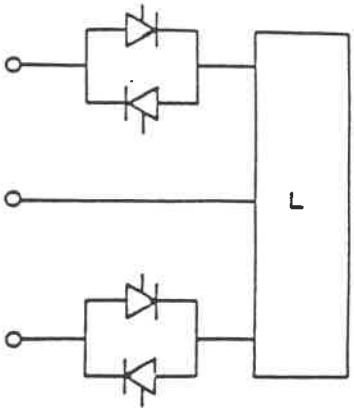
Appendix A[4]

Examples for Using the Classification Code



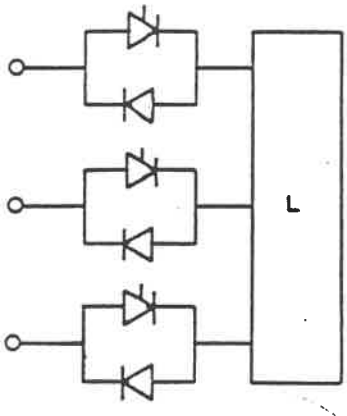
W11AA

Fig A1
Bidirectional Control, Single Phase



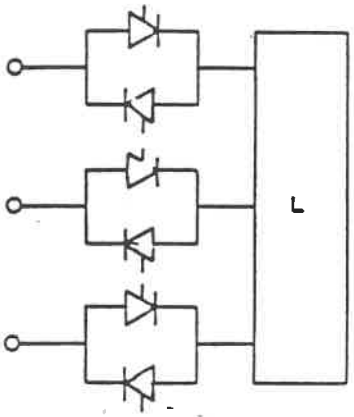
W32AX

Fig A3
Bidirectional Control,
Three Phase, Two-Line Control



W33AX

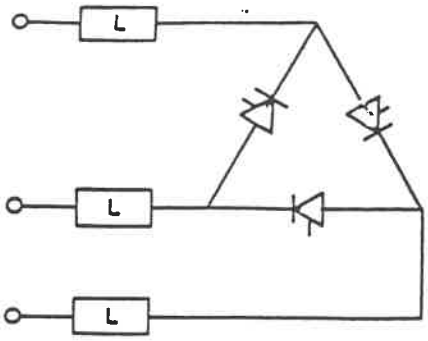
Fig A2
Bidirectional Control, Three Phase



V33AX

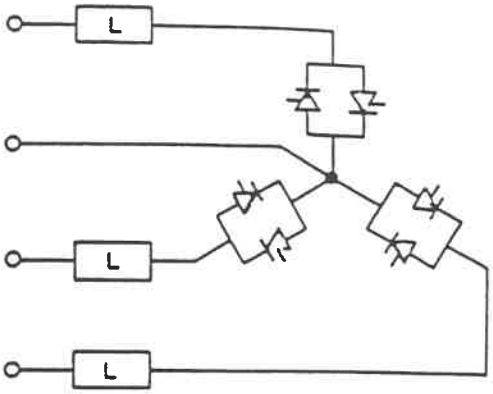
Fig A4
Unidirectional Control,
Reverse Conducting, Three Phase

[4] NOTE: Neutral connected circuits shown may generate extremely high 3rd harmonic currents in the phase control mode. Unless the supply transformer is much greater in rating than the controller, it must have a Δ primary or tertiary to balance the 3rd harmonic currents of the secondary, which may have an amplitude as great as the load current. With no balancing ampere-turns in the primary, the resulting 3rd harmonic air flux can destroy the transformer by extreme overheating of the core-clamps and other structural steel parts.



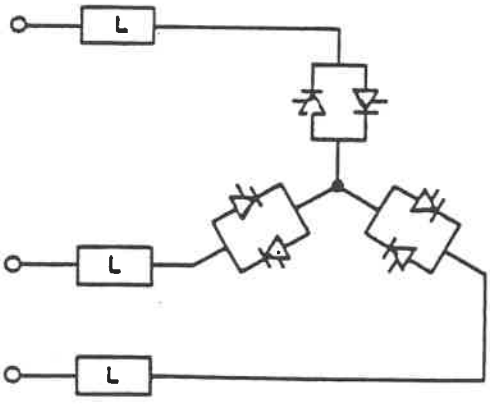
U33DA

Fig A5
Three Phase,
Polygon Connection



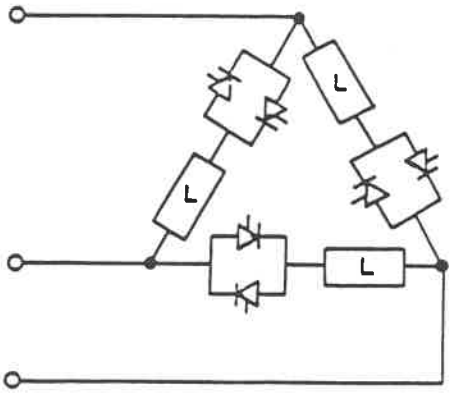
W33NA

Fig A7
Bidirectional Control, Three Phase,
Neutral Connected, Tie Control



W33YA

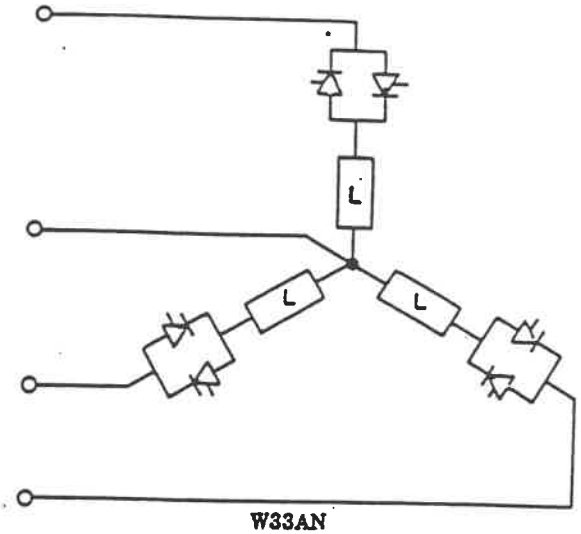
Fig A6
Bidirectional Control,
Three Phase, Tie Control



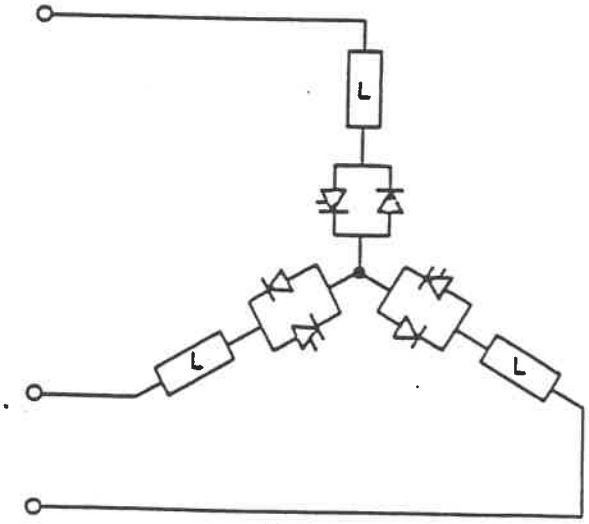
W33AA

Fig A8
Bidirectional Control, Three Phase,
Delta (Control Element and Load)

P428/D2



W33AN
Fig A9
Bidirectional Control, Three Phase, Neutral Connected



V33YA
Fig A10
Unidirectional Control, Reverse Conducting, Three Phase

APPENDIX D:

Derivation of the Laplace Transform for a sinusoidal voltage source

Given that $V_s(t) = V_{max} \sin(\omega_o t + \alpha)$ the easiest way to find the corresponding Laplace transform is to express this function in exponential terms using Euler's identity where by

$\sin\theta = (e^{j\theta} - e^{-j\theta})/2j$ and $\cos\theta = (e^{j\theta} - e^{-j\theta})/2$

hence

$$V_s(t) = (V_{max}/2j)\cdot(e^{j(\omega t+a} - e^{-j(\omega t+\alpha)})$$

This is useful in determining the Laplace transform since by definition:

$$L\{V_s(t)\} = \int_0^\infty V_s(t)\cdot e^{-st}\,dt$$

$$= \frac{V}{2j}\left[\int_0^\infty e^{j\alpha}\cdot e^{(-s+j\omega)t}\,dt - \int_0^\infty e^{-j\alpha}\cdot e^{(-s-j\omega)t}\,dt\right]$$

$$= \frac{V}{2j}\left[\frac{e^{j\alpha}}{s-j\omega} - \frac{e^{-j\alpha}}{s+j\omega}\right]$$

$$= V\left[\frac{s\cdot\sin\alpha + \omega\cdot\cos\alpha}{s^2+\omega^2}\right]$$

APPENDIX E

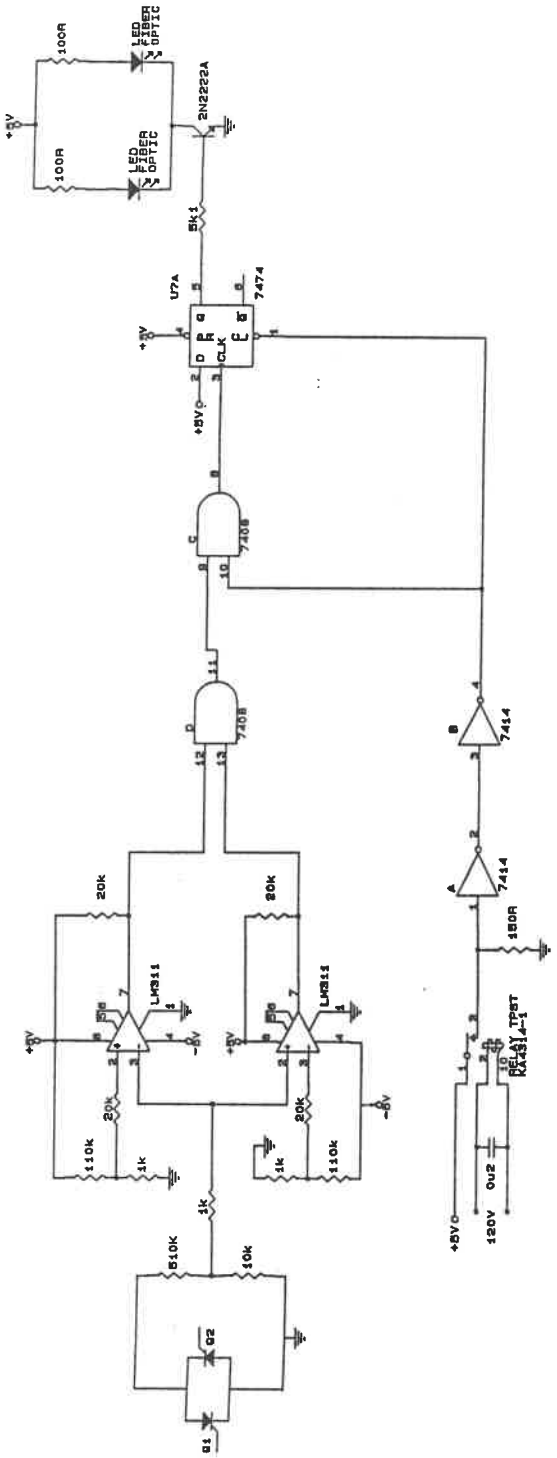
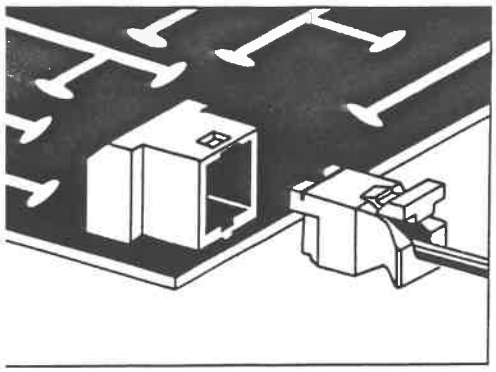
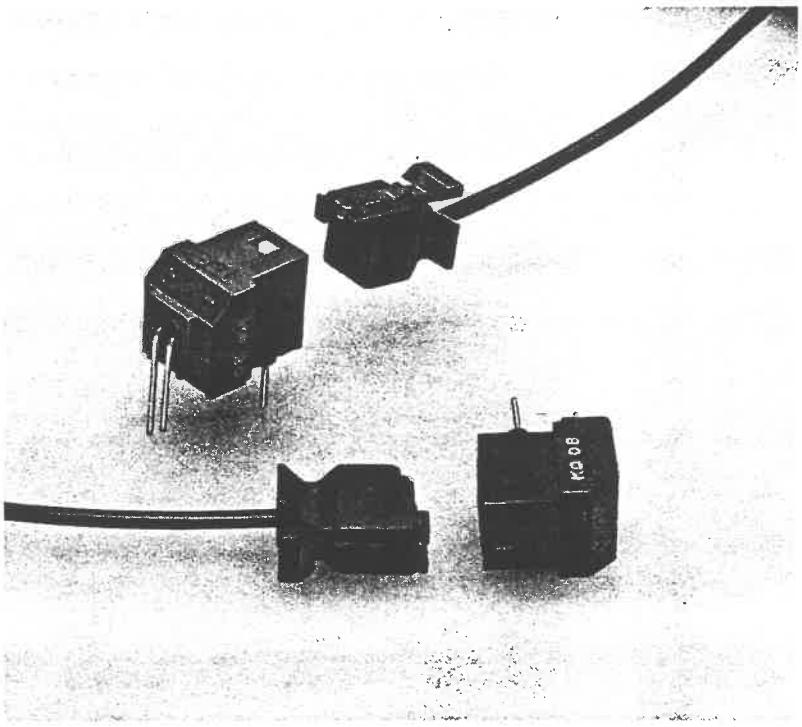


Fig. E.1 Zero Crossing and Gating Logic Circuit



FIBER OPTIC PCB DATA LINK

Self-terminating optical-electronic interface



escription/Application

B's Fiber Optic PCB Data Link combines the efits of fiber optic signaling with the convenience plug-in PCB electrical termination. It is designed permit fast, reliable, self-termination of single chan- plastic optical fiber... without the need for spe- l tools, adhesives, or polishing.

The Data Link consists of a PCB-mounted re- otacle with an integral emitter or detector opto- vice; and a mating, self-terminating cable con- tor plug featuring a quick-release tab. The re- otacle is wave solderable and color-coded for y transmitter and receiver identification. It mates h the polarized cable connector plug with positive ents to achieve a high performance, cost-ef- tive link.

T&B's PCB data link is ideal where EMI/RFI im- inity, ground loop isolation, extended distance ds, and spark-free data transmission are required.

esign Considerations

Compatible with 1mm diameter, simplex plastic tical fiber with an OD of 2.25mm

Terminates fiber optic cable in seconds without ls, adhesives, or polishing

Suitable for terminating data transmission links up to 60 meters (200 feet) at signal rates of b/s (NRZ)

Opto-electrical interface includes a TTL compati- receiver and LED driver (30ma)

Polarized connector plug provides positive, snap ention with quick-release tab

Optional color-coded (red) cable connector plug mits easy identification of transmission or re- ver end of cable assembly

TERFACE	PC BOARD
ER TYPE	1mm PLASTIC SIMPLEX
BLE TYPE	POLYETHYLENE JACKET
STANCE	60 METERS
TA RATE	3Mb/SEC
ERATING TEMPERATURE	0°C to 70°C

Standard Product Options

The information below provides a general overview of this product family. For complete ordering information, please consult specification page.

PCB-Mounted Receptacle

92915 – T – DD

Receptacle Function (Color)
T-DD *– Transmitter (Red)*
R-HS *– Receiver (Black)*

Self-Terminating Cable-Connector Plug

92910 – R

With red fiber clamp (For black fiber clamp, leave blank).

Plastic Polyethylene-Jacketed Simplex Fiber

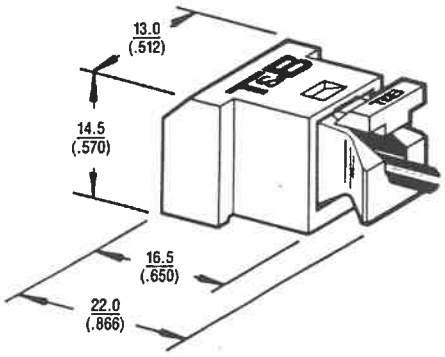
93902 – 100

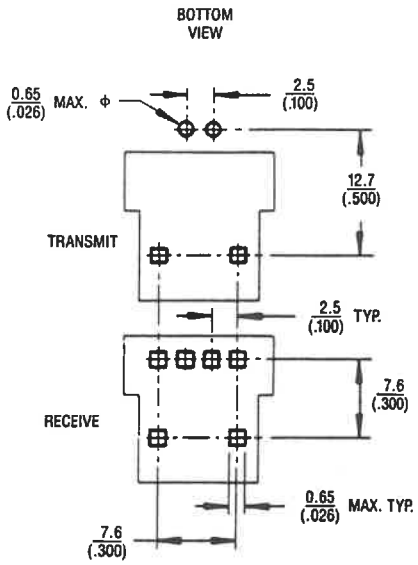
Length of Roll
100 *– 100 Feet*
500 *– 500 Feet*

92910KT
Designer Kit
Contains transmitter, receiver, 2 connector plugs, 10 feet of cable, application notes and data sheet.

FIBER OPTIC PCB DATA LINK SPECIFICATIONS

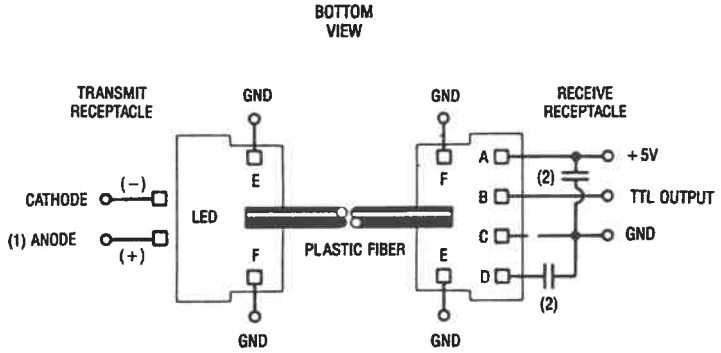
ensional Specifications





ONS ARE SHOWN IN mm/(inches)

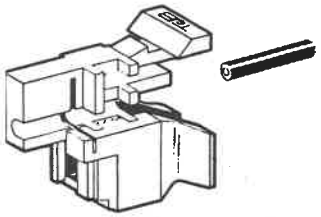
Assignment



Proper operation of this product requires observance of certain design considerations. Refer to T&B publication No. OPD-AN100. "Performance specification and application notes."

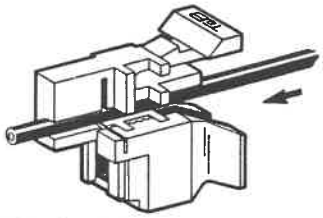
NOTES: 1. LED DRIVE CURRENT 30mA
2. CONNECT A 0.1μF BY-PASS CAPACITOR (VOLTAGE RATING 25V OR MORE)

llation Procedure



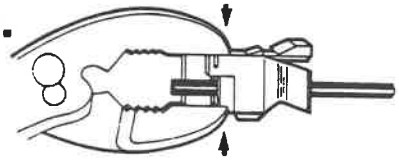
connector plug is packaged ready
se. No fiber preparation is necessary.

2.



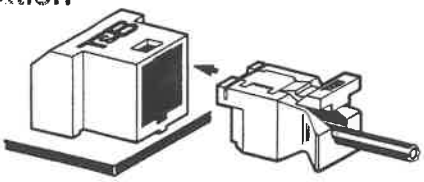
Insert the fiber in the connector as shown. The fiber should protrude through the housing by a minimum of 1 cm.

3.



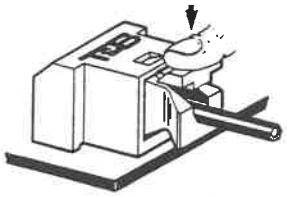
Using pliers as shown, press down on the fiber clamp until it is fully bottomed in the housing. The termination is then complete. Discard unused fiber.

Operation



Insert the polarized positive-snap retention plug into the color-coded receptacle.

2.



To remove, depress the quick-release tab and slide the plug out of the receptacle.

INTERNATIONAL RECTIFIER IOR

50RIA SERIES

80 Amp RMS SCRs

Major Ratings and Characteristics

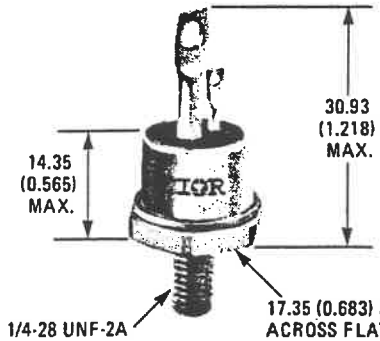
		50RIA . . .	Units
$I_{T(RMS)}$		80	A
$I_{T(AV)}$		50	A
@ Max. T_C		94	°C
I_{TSM}	@ 50 Hz	1200	A
	@ 60 Hz	1255	
I^2t	@ 50 Hz	7200	A^2s
	@ 60 Hz	6560	
I_{GT}		100	mA
dv/dt		200	V/µs
di/dt		200	A/µs
t_q (typ.)		110	µs
T_J		-40 to 125	°C
V_{RRM}		50 to 1200	V

Description/Features

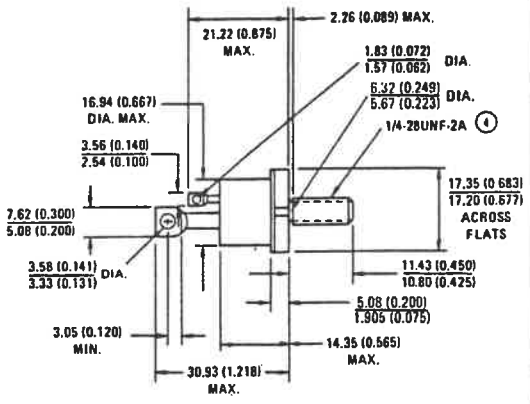
This series of medium power thyristors is intended for general purpose phase control applications in converters, lighting circuits, battery chargers, regulated power supplies and temperature and speed control circuits.

- High current rating.
- Excellent dynamic characteristics.
- For general purpose applications.
- Superior surge capabilities.
- Standard package.
- Metric thread version available.
- Types up to 1200V V_{RRM}, V_{DRM}.
- Can be supplied to meet stringent military, aerospace and other high-reliability requirements.

CASE STYLE AND DIMENSIONS



ACTUAL SIZE



Conforms to JEDEC : TO-208AC (TO-65)
IEC 191 : A14U, A14M (4)
BS 3934 : SO-28
DIN 41892 : 202 C 3

All Dimensions in Millimeters and (Inches)

VOLTAGE RATINGS (Applied gate voltage zero or negative.)

Part Number ④	V_{RRM}, V_{DRM} – Max. Repetitive Peak Reverse or Off-State Voltage (V) ①②	V_{RSM} – Max. Non-Repetitive Peak Reverse Voltage (V) ①	I_{RM}, I_{DM} – Max. Peak Reverse and Off-State Current at Rated V_{RRM} and V_{DRM} Zero Gate Bias Voltage, Gate Open Circuited (mA)
	T_J = -40°C to 125°C	T_J = 25°C to 125°C	T_J = 125°C
50RIA5	50	100	15
50RIA10	100	150	15
50RIA20	200	300	15
50RIA40	400	500	15
50RIA60	600	720	15
50RIA80	800	960	15
50RIA100	1000	1200	15
50RIA110	1100	1320	15
50RIA120	1200	1440	15

ELECTRICAL SPECIFICATIONS

			Units	Conditions
	ON-STATE			
$I_{T(RMS)}$	Max. RMS on-state current	80	A	
$I_{T(AV)}$	Max. average on-state current	50	A	T_C = 85°C and 94°C max., 180° sinusoidal conduction.
I_{TSM}	Max. peak one cycle, non-repetitive surge current	1200	A	50 Hz half cycle sine wave or 6 ms rectangular pulse — Following any rated load condition, and with rated V_{RRM} applied, SCR turned fully on.
		1255		60 Hz half cycle sine wave or 5 ms rectangular pulse
		1430		50 Hz half cycle sine wave or 6 ms rectangular pulse — Following any rated load condition, and with V_{RRM} following surge = 0.
		1490		60 Hz half cycle sine wave or 5 ms rectangular pulse
I^2t	Max. I^2t capability, for fusing	7200	A^2s	t = 10 ms — Rated V_{RRM} applied following surge, initial T_J = 125°C.
		6560		t = 8.3 ms
I^2t	Max. I^2t capability, for individual device fusing	10180	A^2s	t = 10 ms — V_{RRM} following surge = 0, initial T_J = 125°C.
		9300		t = 8.3 ms
$I^2\sqrt{t}$	Max. $I^2\sqrt{t}$ capability, for individual device fusing ③	101,800	$A^2\sqrt{s}$	t = 0.1 to 10 ms, V_{RRM} following surge = 0, initial T_J = 125°C.
V_{TM}	Max. peak on-state voltage	1.6	V	T_J = 25°C, $I_{T(AV)}$ = 50A (157A peak)
I_H	Max. holding current	200	mA	T_C = 25°C, anode supply = 22V.
	BLOCKING			
dv/dt	Min. critical rate-of-rise of off-state voltage	200	V/μs	T_J = 125°C. Exponential to 100% rated V_{DRM} — Zero gate bias voltage, gate open circuited.
		500		T_J = 125°C. Exponential to 67% rated V_{DRM}

① For voltage pulses with $t_p \leq 5$ ms.

② Units may be broken over non-repetitively in the off-state direction without damage, if di/dt does not exceed 20 A/μs.

③ I^2t for time $t_x = I^2\sqrt{t} \cdot \sqrt{t_x}$

④ For M6 threads add "M" to code, e.g., 50R1A60M.

ELECTRICAL SPECIFICATIONS (Continued)

			Units	Conditions
	SWITCHING			
t_d	Typical delay time	0.9	μs	T_C = 25°C, V_{DM} = rated V_{DRM}, I_{TM} = 10A dc resistive circuit, Gate pulse: 10V, 15Ω source, t_p = 20 μs.
di/dt	Max. non-repetitive rate of rise of turned-on current			T_C = 125°C, V_{DM} = rated V_{DRM}, I_{TM} = 2 x rated di/dt, Gate pulse: 20V, 15Ω, t_p = 6 μs, t_r = 0.1 μs max. Per JEDEC standard RS-397, 5.2.7.6.
	V_{RRM} = 50 to 600V	200	A/μs	
	= 700 to 1200V	100		
t_q	Typical turn-off time	110	μs	T_C = 125°C, I_{TM} = 50A, di/dt = -10 A/μs, V_R during turn-off interval = 50V min. reapplied, dv/dt = 20 V/μs linear to rated V_{DRM}. Gate bias: 0V, 100Ω.
	TRIGGERING			
P_{GM}	Max. peak gate power	10	W	$t_p \leq$ 10 ms
$P_{G(AV)}$	Max. average gate power	2	W	
I_{GM}	Max. peak positive gate current	2.5	A	
$+V_{GM}$	Max. peak positive gate voltage	20	V	
$-V_{GM}$	Max. peak negative gate voltage	5	V	
I_{GT}	Max. required DC gate current to trigger ⑤	250	mA	T_C = -65°C
		100		T_C = 25°C
		50		T_C = 125°C
V_{GT}	Max. required DC gate voltage to trigger ⑤	5	V	T_C = -65°C
		2.5		T_C = 25°C
V_{GD}	Max. DC gate voltage not to trigger ⑥	0.2	V	T_C = 125°C

THERMAL-MECHANICAL SPECIFICATIONS

T_J	Operating junction temperature range	-40 to 125	°C	
T_{stg}	Storage temperature range	-40 to 125	°C	
R_{thJC}	Max. internal thermal resistance, junction to case	0.35	deg. C/W	DC operation
R_{thCS}	Thermal resistance, case to sink	0.25	deg. C/W	Mounting surface smooth, flat and greased.
T	Mounting torque			
	Min.	2.8 (25)	N • m (lbf-in)	Non-lubricated threads
	Max.	3.4 (30)		
wt	Approximate weight	28 (1.0)	g (oz.)	
	Case Style	TO-208AC (TO-65)		

⑤ Max. required gate trigger current (or voltage) is the lowest value which will trigger all units with +6 volts anode-to-cathode.

⑥ Max. gate current or voltage not to trigger is the maximum value which will not trigger any unit with rated V_{DRM} anode-to-cathode.

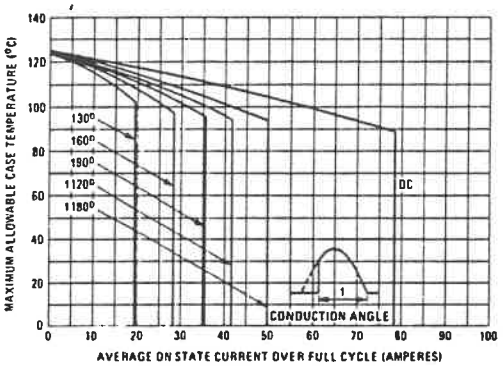


Fig. 1 — On-State Current Vs. Case Temperature (Sinusoidal Current Waveform, 50 to 400 Hz)

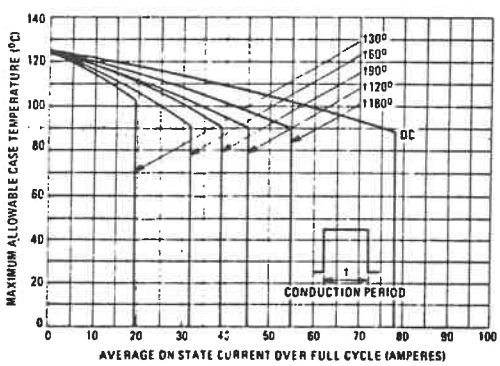


Fig. 2 — On-State Current Vs. Case Temperature (Rectangular Current Waveform, 50 to 400 Hz)

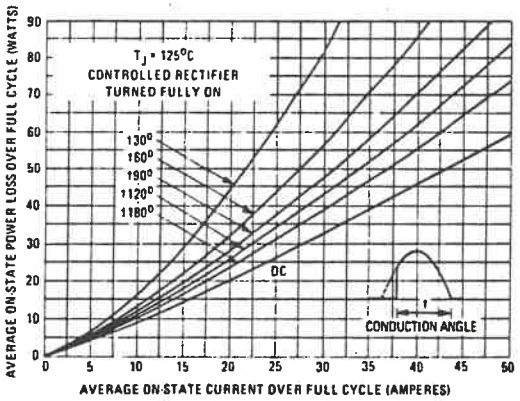


Fig. 3 — Maximum Low-Level On-State Power Loss Vs. Current (Sinusoidal Current Waveform)

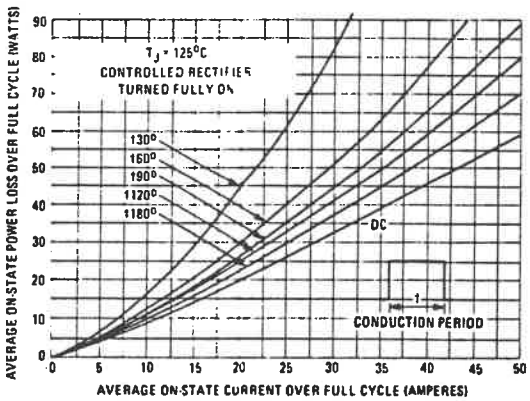


Fig. 4 — Maximum Low-Level On-State Power Loss Vs. Current (Rectangular Current Waveform)

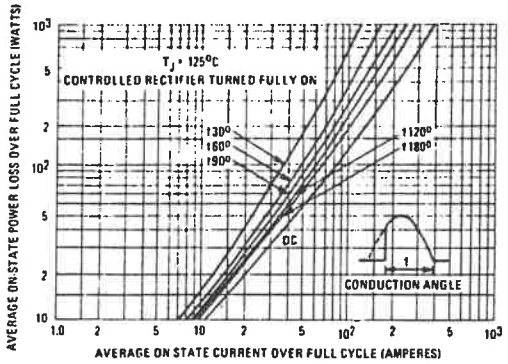


Fig. 5 — Maximum High-Level On-State Power Loss Vs. Current (Sinusoidal Current Waveform)

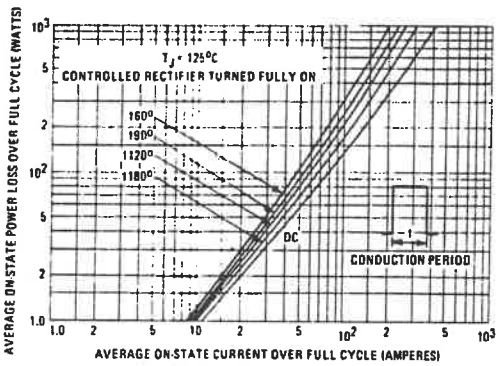


Fig. 6 — Maximum High-Level On-State Power Loss Vs. Current (Rectangular Current Waveform)

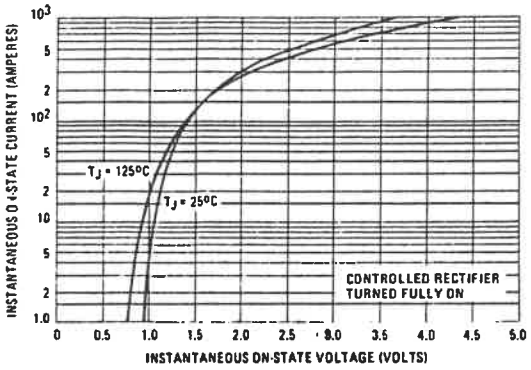


Fig. 7 — Maximum On-State Voltage Vs . Current

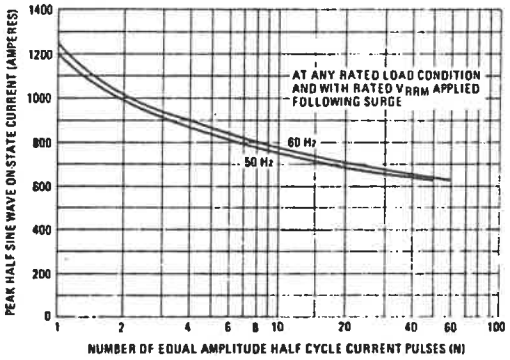


Fig. 8 — Maximum Non-Repetitive Surge Current Vs. Number of Current Pulses

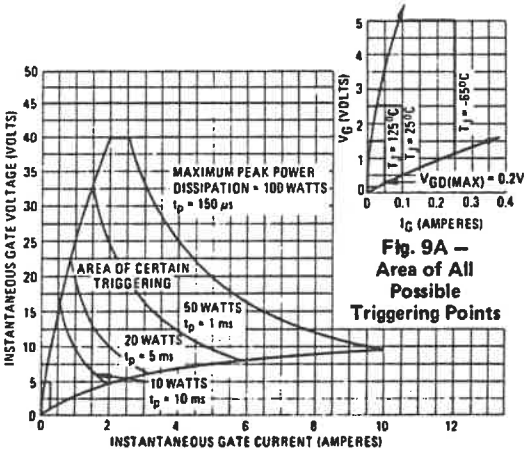


Fig. 9A — Area of All Possible Triggering Points

Fig. 9 — Gate Characteristics

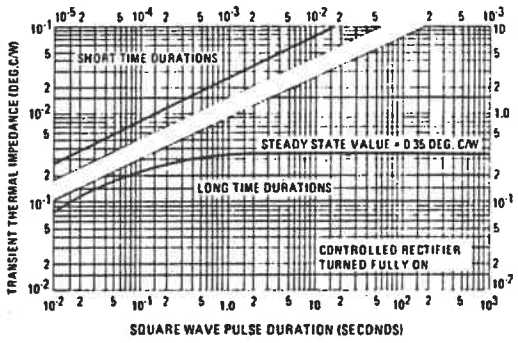


Fig. 10 — Maximum Transient Thermal Impedance, Junction-To-Case Vs. Square Wave Pulse Duration

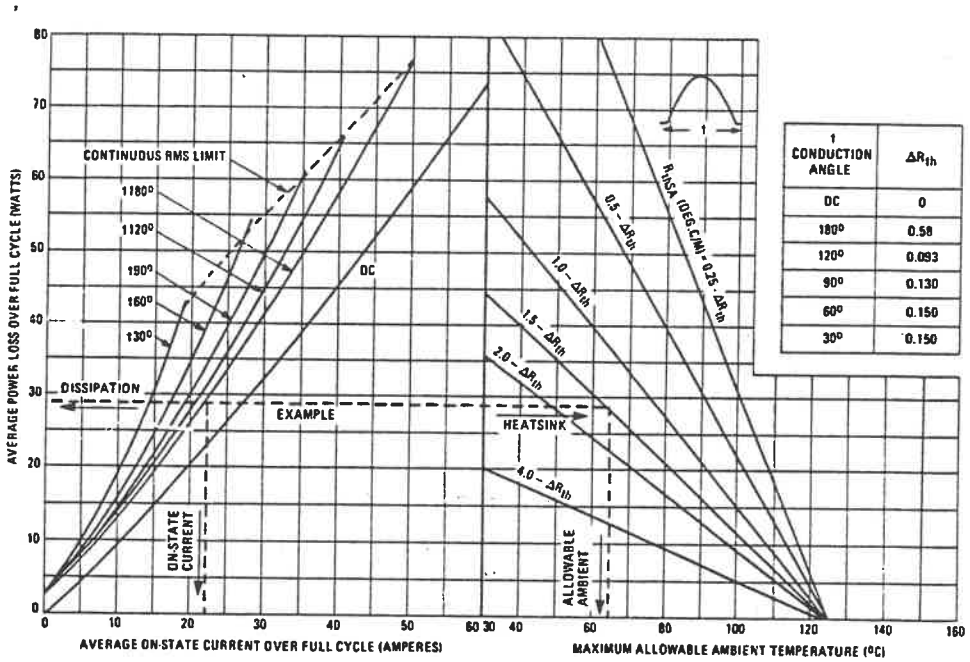


Fig. 11 – Thermal Nomogram (Sinusoidal Current Waveform, 40 to 400 Hz)

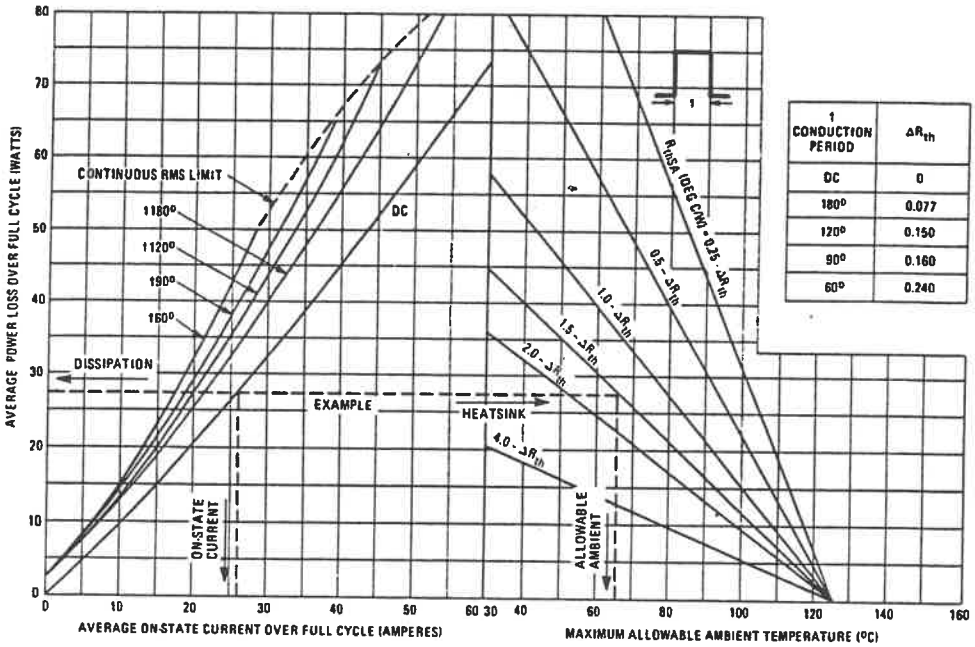


Fig. 12 – Thermal Nomogram (Rectangular Current Waveform, 40 to 400 Hz)

Notes: A. Maximum allowable heatsink thermal resistance, R_{thSA}, equals the graph value minus the ΔR_{th} factor which allows for instantaneous T_J excursion.

B. Caution. Data assumes that the controlled rectifier is mounted with thermally conductive grease to achieve R_{thCS} = 0.25 deg.C/W.