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Unified circuit-antenna integration for next generation wireless systems

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Thèse présentée en vue de l'obtention du diplôme de *Philosophiæ Doctor*

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Cette thèse intitulée :

Unified circuit-antenna integration for next generation wireless systems

présentée par **Srinaga Nikhil NALLANDHIGAL**

en vue de l'obtention du diplôme de *Philosophiæ Doctor*

a été dûment acceptée par le jury d'examen constitué de :

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RÉSUMÉ

Les technologies sans fil ont évolué rapidement au fil du temps, tant en termes de fréquences d'opération que de gammes d'applications. De nos jours, une myriade de systèmes sans fil bon marché opérant a moins de 6 GHz sont disponibles, et ils sont devenus une partie intégrante de la vie des gens. Due à un spectre à basse fréquence saturé et une demande grandissante du marché pour des débits de données plus élevés, les futures technologies sans fil se développent dans le spectre fréquence des ondes millimétriques (mmW) et des terahertz (THz). Les caractéristiques inhérentes de l'utilisation de plus hautes fréquences et d'une bande passante plus élevée sontdes antennes de plus petites dimenaions et de meilleures résolutions, ce qui les rendent attrayantes pour les applications pour la 5G, l'imagerie, les radars automobiles, l'identification, la spectroscopie, etc. qui présentent des avantages incontournables. De nombreuses technologies ont été étudiées et déployées à l'appui des développements des émetteurs-récepteurs intégrés pour les applications dans les MHz jusqu'aux THz. Parmi eux, bien que les implémentations basées sur l'utilisation des lignes microrubans promettent des caractéristiques intéressantes en termes de coût, de poids, et d'encombrement, leurs performances électriques sont limitées lorsque les antennes sont intégrées aux émetteurs-récepteurs par des approches d'antennes intégrées conventionnelles ou actives. En effet, les pertes dans les lignes de transmission et les pertes par radiation des éléments des circuits inhérents sont des inconvénients notables dans la réalisation de ces solutions à des fréquences mmW et au-delà.

En conséquence, il a été nécessaire de développer des techniques d'intégration avancées en mettant l'accent sur l'élimination ou la fusion des composants qui composent les circuits Ceci a été largement étudié au cours des dernières années. En outre, pour faire face à l'atténuation en mode grand signal et atteindre des plages de fonctionnement souhaitables, la transmission à haute puissance est souvent une nécessité qui peut être réalisée par des amplificateurs de puissance et / ou des réseaux d'antennes. Motivés par toutes ces exigences, nous avons proposé et développé une architecture nouvelle appelée antenne de circuit unifiée et intégrée (unified and integrated circuit antenna-UNICA). Ici, les antennes sont conçues pour effectuer les multiples tâches des composants de circuits en plus du patron de rayonnement et sont directement intégrées aux dispositifs actifs pour réaliser des fonctions simultanées de circuiterie et de rayonnement à travers un espace unifié de conception et d'intégration. Cet objectif de cette recherche est d'explorer les moyens potentiels

de les intégrer pour réaliser des solutions de circuiterie-radiation, à faible coût, efficaces et compactes.

Dans un premier temps, l'intégration des éléments actifs entre les réseaux d'antennes multifonctionnelles a été proposée. Ces éléments de réseaux fonctionnent simultanément comme des adaptations d'impédances et des éléments rayonnants, tandis que les transistors intégrés entre eux sont réglés pour amplifier le signal et aussi interconnecter les éléments du réseau. Un prototype de réseau d'antenne-amplificateur 1×2 avec des patchs rectangulaires et des transistors commerciaux HJ-FET a été mesuré expérimentalement pour prouver le concept. Ce prototype de PCB est adapté à la fréquence de conception de 5 GHz et a montré un gain de 11,5 dBi avec un faisceau de rayonnement dirigé à $+30^0$. En outre, les fonctions de circuiterie d 'oscillation, d'amplification à large bande et d'amplification à faible bruit sont également réalisées en adoptant cette approche et sont discutées en détail.

Par la suite, l'intégration de plusieurs dispositifs actifs directement dans les fentes gravées à l'intérieur d'une antenne patch est proposée pour réaliser les fonctions simultanées d'amplification parallèle et de rayonnement. L'antenne-amplificateur parallèle est développé à 146 GHz en technologie CMOS pour optimiser l'efficacité et l'intégration des dispositifs actifs et des modules d'antenne sur puce. Ce prototype élimine tous les diviseurs/combineurs de puissance, les réseaux d'adaptation et les différentes interconnexions, ce qui les rend extrêmement compacts et efficaces. La mono cellule antenne amplificateur développée a montré une amélioration de l'EIRP de 3,4 dB par rapport à la configuration conventionnelle. En outre, l'auto-distribution de ces cellules unitaires pour former un prototype de réseau d'antennes d'amplification de 2x2 sans lignes d'alimentation et de réseaux d'adaptation a également été mesuré expérimentalement. Ce dernier présente une amélioration de 6 dB de l'EIRP et le rayonnement de compensation par rapport aux solutions conventionnelles.

Bien que les deux prototypes précédents aient permis le contrôle du gain pour l'ensemble des dispositifs actifs, le contrôle de la phase n'est pas abordé, c'est pour cette raison que le faisceau est dirigé. À cet égard, le contrôle de la phase à travers le dispositif actif ainsi que le gain sont analysés et discutés en détails. Ainsi, deux prototypes amplification-réseau d'antennes 1×5 sont développés pour réaliser un patron de réseau de Chebyshev avec -20 dB niveau de lobe secondaire et un patron de rayonnement de faisceau plat- de -10^0 à 30^0. L'amplitude souhaitée et l'excitation de phase de

chaque élément du réseau sont directement réalisées par l'intégration des éléments actifs entre les éléments du réseau et les lignes d'alimentation, éliminant ainsi les réseaux d'adaptations généralement requis des d'amplificateurs et des circuits déphaseurs.

Ensuite, la configuration planaire 2D amplification-réseau d'antennes échelonnable est proposée et démontrée à travers un prototype de 8x8. Les éléments actifs sont directement intégrés entre les lignes d'alimentation conçues de manière appropriée et les bords non rayonnants-des éléments du réseau RPA pour réaliser une amplification souhaitée, et ce, sans utiliser de réseaux d'adaptation. Une nouvelle approche d'intégration de ces éléments de réseau avec la configuration d'alimentation série-parallèle est développée pour réduire à la fois le niveau dépolarisation croisée et un certain nombre de lignes d'alimentation, ce qui facilite également la réalisation de l'ensemble du système sur une seule couche, en incluant les lignes DC. En outre, la configuration parallèle du prototype développé le rend attrayant pour des applications a haute puissance.

Dans les développements actuels de l'UNICA, la co-conception et l'analyse des antennes et des circuits inhérents sont effectuées dans différentes plates-formes de simulation en exportant et en important les données pertinentes, ce qui est un processus qui prend beaucoup de temps. Dans ce contexte, nous proposons un modèle de réseau-maillage équivalent généralisé pour l'antenne patch, qui permet les co-simulations et analyses initiales dans la plate-forme schématique, accélérant ainsi le processus de conception. Le modèle correspondant est réalisé en divisant le layout du RPA en plusieurs sections et en les intégrant de manière appropriée. En outre, la capacité du modèle proposé à prendre en considération les fentes gravées les vias, en multimode et les variations d'alimentation sont également discutés en détail.

Toutes les analyses théoriques nécessaires, les procédures générales de modélisation, les co-simulations, les développements des prototypes et les démonstrations expérimentales pour chaque technique proposée sont largement discutées dans cette thèse. Le contenu de ce travail est publié dans des brevets et des revues et conférences internationales réputées. Finalement, nous croyons que ce travail ouvre des perspectives au chercheur pour la manipulation des circuits et des antennes en tant qu'entités indépendantes pour les fusionner et développer des solutions innovantes, efficaces et compactes, qui ont le potentiel de transformer les déploiements de systèmes sans fil des prochaines générations.

ABSTRACT

Wireless technologies have been evolving rapidly over time, both in terms of operating frequencies and range of applications. As of today, a myriad of inexpensive wireless systems operating below 6 GHz are available, which have become an integral part of the present-days human life. Triggered by such overcrowded low-frequency spectrums and persistent market demand for higher data rates, the future wireless technologies are expanding into the millimeter-wave (mmW) and terahertz (THz) range spectrums. The inherent features of higher bandwidth, smaller antennas, and improved resolutions among others make them attractive for the intended applications of 5G, imaging, automotive radar, identification, spectroscopy, and so on, which enable great conveniences. Numerous hardware technologies have been studied and deployed in support of integrated frontend developments for MHz through THz applications. Among them, although the microstrip implementations promise the features of low-cost, lightweight, and compactness, the electrical performances of corresponding hardware solutions are limited when the frontend circuits and antennas are integrated through either conventional or active integrated antenna approaches. In particular, the significant transmission line losses and radiation disturbances from the inherent circuitry elements are notable drawbacks in realizing these solutions at mmW frequencies and beyond.

As a result, it is a high time to develop advanced integration techniques with focus on eliminating or merging the circuitry components, which are being widely researched in the recent years. Furthermore, to cope up with the large signal attenuation and achieve desirable operating ranges, high power transmission is often a necessity that can be achieved through frontend power amplifiers and/or array antennas. Motivated by all these requirements, we have proposed and developed a novel architecture called the unified and integrated circuit antenna (UNICA). Here, the antennas are designed to perform the multiple tasks of circuitry components in addition to their radiation and are directly integrated with the active devices to realize simultaneous circuit and radiation functions through a unified space of design and integration. And, the objective of this research is to explore the potential ways of integrating them to realize low-cost, efficient, and compact joint circuiting-radiating solutions.

In the first instance, the integration of active devices between the subsequent multifunctional antennas arranged in a series array configuration has been proposed. These array elements operate simultaneously as matching networks and radiators, while the transistors integrated between them are set to amplify the signal and also interconnect the array elements. A 1×2 amplifier-array antenna prototype with rectangular patches and off-the-shell HJ-FET has been experimentally demonstrated to prove the concept. This PCB prototype is matched at the design frequency of 5 GHz and exhibited an amplifying gain of 11.5 dB with a beam steered radiation at $+30^0$. Besides, the circuitry functions of oscillation, wideband amplification, and low noise amplification are also realized by adopting this approach and they are discussed in detail.

Subsequently, the deep integration of multiple active devices directly within the slots etched inside a rectangular patch antenna is proposed for realizing simultaneous paralleled amplification and radiation functions. The corresponding paralleled amplifier-antenna developed at 146 GHz in CMOS facilitates the efficient design and optimal integration of both the active devices and on-chip antenna modules. This prototype eliminates all the typically required dedicated power dividers/combiners, matching networks, and corresponding interconnections, thus making them extremely compact and efficient. The developed single paralleled amplifier-antenna cell verified an EIRP improvement of 3.4 dB compared to the conventional configuration. Furthermore, the self-distribution of these unit cells to form a 2x2 amplifying-antenna array prototype without feed lines and matching networks has also been experimentally demonstrated, which exhibits a 6 dB EIRP improvement and offset radiation compared to passive counterparts.

Although the previous two demonstrations have discussed the control of gain across the active devices, the corresponding phase component control is not addressed which is the reason for beam steered radiation in them. In this regard, the control on the phase component across the active device along with the gain are extensively analyzed and discussed. With this knowledge, two 1×5 amplifying-array antenna prototypes are developed to realize a Chebyshev radiation pattern with -20 dB sidelobe level and a flat-top beam radiation pattern from -10^0 to 30^0. The desired magnitude and phase excitation of each array element are directly realized through active devices integrated between array elements and feed lines, thereby eliminating the typically required dedicated matching networks of amplifier and phase shifting circuitry.

Then, the scalable and planar two-dimensional amplifying-array antenna configuration is proposed and demonstrated through an 8x8 prototype. The active devices are directly integrated between appropriately designed feed lines and non-radiating edge-fed RPA array elements to realize a desired amplification, without utilizing any matching networks. Moreover, a novel approach of integrating these array elements with series-parallel feed configuration is developed to reduce both the cross-polarization and a number of feed lines, which also facilitates the realization of the entire system on a single layer including the DC lines. Furthermore, the paralleled configuration of the developed prototype makes them attractive even for high-power applications.

In the present-day UNICA developments, the co-design and analysis of inherent antennas and circuits are carried out in different simulation platforms by exporting and importing the relevant data, which is a time-consuming process. In this context, we propose a generalized mesh-network equivalent model for rectangular patch antenna, which enables the initial co-simulations and analyses in the schematic platform, thereby speeding up the design process. The corresponding model is realized by dividing the RPA layout into several sections and appropriately integrating them. Besides, the ability of the proposed model to support the slots etched in it, with vias, in multimode, and feed variations are also discussed in detail.

All the necessary theoretical analyses, general modeling procedures, co-simulations, prototype developments, and experimental demonstrations of each proposed technique are extensively discussed in this dissertation. The content of this work is published in patents, and also in reputed international journals and conferences. Eventually, we believe that this work opens up the researcher’s perspective from handling the circuits and antennas as independent entities to fuse them and develop innovative, efficient, and compact solutions that have the potential to transform the next generation wireless system deployments.

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LIST OF SYMBOLS AND ABBREVIATIONS

2.5D	2.5 dimensional
3D	Three dimensional
5G	Fifth generation
AC	Alternating current
ACA	Amplifier circuit antenna
ACRPA	Active compact rectangular patch antenna
ADS	Advance design system
AIA	Active integrated antenna
Aoc	Antenna-on-chip
Aip	Antenna-in-package
AUT	Antenna under test
BW	Bandwidth
CMOS	Complementary metal oxide semiconductor
CPW	Coplanar waveguide
CRPA	Compact rectangular patch antenna
CST-MWS	Computer simulation technology-microwave studio
DAR	Distributed active radiator
DC	Direct current
DUT	Device under test
EIRP	Equivalent isotropically radiated power
FEKO	Feldberechnung für körper mit beliebiger oberfläche
FET	Field effect transistor

GaAs	Gallium arsenide
GCPW	Grounded coplanar waveguide
GHz	Gigahertz
GSG	Ground signal ground
HFSS	High frequency structural simulator
HJ-FET	Hetero junction field effect transistor
IC	Integrated circuit
IF	Intermediate frequency
IIP3	Third-order intercept point
IMN	Input matching network
LO	Local oscillation
LTCC	Low temperature co-fired ceramic
MHz	Megahertz
MIMO	Multi input multi output
MMIC	Monolithic microwave integrated circuit
MmW	Millimeter-wave
NF	Noise figure
OCA	Oscillator circuit antenna
OMN	Output matching network
PA	Power amplifier
PAE	Power added efficiency
PCB	Printed circuit board
R&D	Research and development
RF	Radio frequency

RFID	Radio frequency identification
RPA	Rectangular patch antenna
Rx	Receiver
SiGe	Silicon germanium
SIW	Substrate integrated waveguide
SLL	Side lobe level
SOM	Self oscillating mixer
TE	Transverse electric
THz	Terahertz
TL	Transmission line
TM	Transverse magnetic
Tx	Transmitter
TV	Television
UN-ACA	Unified amplifier circuit antenna
UNICA	Unified and integrated circuit antenna
VNA	Vector network analyzer
WLAN	Wireless local area network
WPN	Wilkinson power divider

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CHAPTER 1 INTRODUCTION

Wireless technologies have come a long way since the pioneering demonstration of transatlantic transmission by Marconi in 1901 [1]. Over the years, these technological implementations have been spurred by a fast-changing landscape of radio frequency (RF) and microwave applications, that had gradually evolved from the bulky setups at megahertz (MHz) frequencies to portable systems in gigahertz (GHz) frequency range [2]. Especially, the last two decades or so have witnessed a vibrant growth in the range of wireless applications, which eventually became an integral part of our life in the smart world. And today, a myriad of inexpensive devices are available for the present-day commercial, military, and space applications typically operating below 6 GHz frequencies, resulting in the congestion of this spectrum.

Triggered by such overcrowded legacy RF spectrum allocations and to meet the persistent market demand for higher data rates, finer resolutions, compactness, enhanced integration, and so on; millimeter-wave (mmW) and terahertz (THz) range frequencies have become the emerging focal points of wireless research and development (R&D) projects [3-5]. The targeted applications include automotive radar, electromagnetic imaging, 5G, short-range communication, space exploration, and spectroscopy, to name a few [6-8]. However, their operating ranges are typically low, because of the high atmospheric attenuation at these bands [9, 10]. Nevertheless, the operating range can be improved through two potential techniques;

1. by boosting the transmission power through high power amplifiers integrated with antennas [11, 12]. The typical amplifier circuit consists of matching networks, harmonic attenuation networks (depending on the class of amplifier), and corresponding interconnections. In addition, power dividers and combiners are required in case of a paralleled power amplifier circuits design.
2. deploying phased array antennas, where the array gain compensates the losses and the desired angular coverage is achieved through beam steering [13-16]. Correspondingly, the phase shifters, feed lines, and interconnections are vital building blocks of these systems.

All these reported components are indispensable in conventional architectural implementations, wherein the circuits and antennas are designed independently at a reference impedance and are

interconnected through transmission lines [17], as shown in Fig. 1.1. The microstrip line technologies are promising for compact, cost-effective, and efficient implementation of these systems as they can be manufactured with high precision and can facilitate an easier integration of the relevant components. However, the high losses caused from passive networks, signal feeders, and line interconnections are some of the well-known bottleneck issues [15, 18]. In addition, the parasitic radiations from them are omnipresent in all RF and microwave systems, which can significantly deteriorate the system performances.

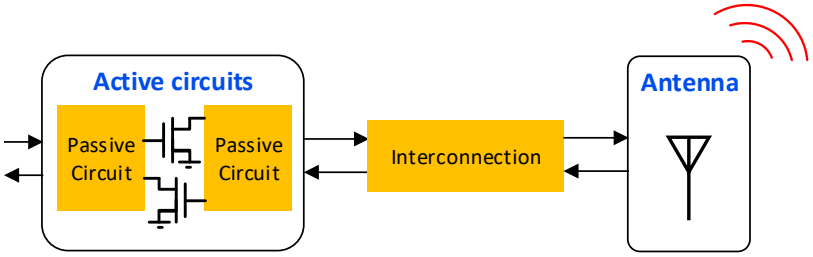


Figure 1.1: Block diagram of conventional configuration.

To alleviate these effects, different approaches are being thought which usually requires additional steps and burden the design process and complexity in manufacturing. For example, the transmission losses and radiation effects can be reduced through wave-guide based solutions. However, they are relatively bulky, expensive, and even difficult to integrate the active devices directly with them. While, an alternative solution to mitigate the radiation effects is to install all the circuits and their interconnections along with the feed networks at the backside or on a separate layer in an attempt to isolate them from the radiating structure. However, the realization of multilayer integrations and vertical alignments is a tedious and costly process at higher frequencies. Also, the well-documented common disadvantage of both the single and multiple layer circuit configurations is the loss resulted from circuits, feeders and interconnects.

As a result, the existing schemes are not able to resolve the fundamental problems in connection with the relationship between circuits and antennas as they handle those two blocks in a separate and independent manner. Therefore, an improved architectural solution is required to deal with this fundamental hurdle in the preparation of a circuit-antenna integration for the development of next generation wireless systems.

1.1 Active integrated antenna

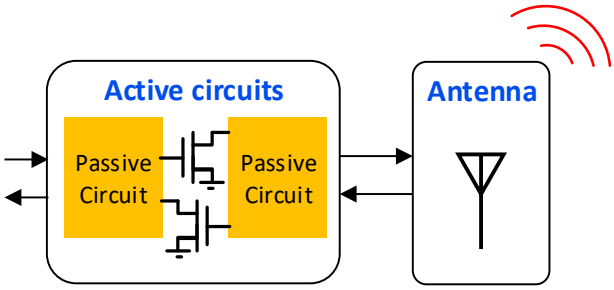


Figure 1.2: Block diagram of active integrated antenna configuration

In this regard, the active integrated antennas (AIAs) systems have emerged as an architectural development to tackle a few of these bottleneck issues. AIAs involve the co-design of frontend active circuitry and antennas close to each other on the same board, as shown in Fig. 1.2, reducing or eliminating a number of passive components [19, 20]. The first demonstration of this idea can be traced back to as early as 1928, comprising of tubes and wire antenna [21]. Subsequently, diodes have replaced tubes, and eventually the availability of high frequency transistors in the 1970's has triggered an extensive research in these solutions [22]. Although, the present day AIAs are realized by integrating either diode or transistors based active circuitry with antenna, we limit the discussion to the AIA solutions that involve transistors, which is of interest in this work.

Generally, in AIAs, active circuits and antennas can still be separately designed and interfaced through certain pre-defined impedance conditions. While in special cases, they are mutually related via electromagnetic coupling and have to be co-designed, and a re-normalization of the S-parameters is recommended to appropriately evaluate the coupling between circuits and antennas [23]. In any case, AIAs are developed through multifunctional modules and presents notable advantages of compactness, lower loss, high power handling, and reduced power consumption [24-26]. Acknowledging these features, they are proposed for deployment in the present-day applications including wireless power transfer, RFID, radar, cubesats and so on [27-29]. Also, they are being considered for the next generation mobile connectivity solutions [30, 31].

However, the passive circuitry components and corresponding interconnections are still existent, which induces significant transmission and radiation losses in mmW range applications. The

transmission loss is dissipated as heat, thereby limiting the power handling capabilities of such solutions and demanding additional cooling equipment. Besides, the radiation losses from the passive circuitry components influences the antenna's performances [32], especially when they are placed in the proximity of the radiating structures. It is also worthwhile noting that at mmW and THz bands, the antenna size shrinks and becomes comparable to the feed lines affecting each others' performances [33-35]. These drawbacks limit AIA implementations in the mmW/THz range systems and demand the research for further improved architectural solutions.

1.2 Motivation

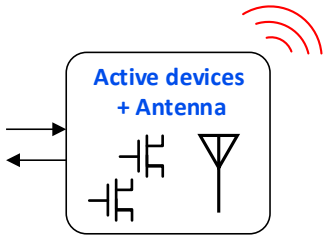


Figure 1.3: Proposed unified and integrated circuit antenna (UNICA)

An ideal solution, therefore, will be the one that can provide simultaneous active circuitry and radiation functions by integrating only active devices with antennas as shown in Fig. 1.3. This eliminates all the typically required passive circuitry components and corresponding awful effects.

A typical active circuit comprises of input and output circuitry along with the core functional elements such as diodes or transistors. The corresponding passive circuitry can be considered as providing certain functionality (for example, matching, power division, power combining, harmonic control, and so on) with an impedance looking into it. If such circuitry functions can be absorbed into the antenna and still present the desired impedances over a frequency range of interest, the circuit antenna can be unified for in-situ integration. In fact, antennas are capable of providing these additional functions in addition to radiation. Subsequently, the antenna in conjunction with the active device can realize simultaneous circuitry and radiation functions. Motivated by all these requirements of mmW and THz range applications and assessing the feasibility, we have proposed and patented the deep integration of circuits and antennas and referred it as unified and integrated circuit antenna (UNICA).

Furthermore, the technological advancements facilitate an easier design and integration of active devices and antennas. Especially, the silicon-based technologies such as CMOS, SiGe, GaAs, and so on offer extreme flexibility in designing such UNICA solutions at a lower cost [36]. As a result, there is a great potential window for developing the highly integrated UNICA solutions with circuitry functions along with radiation through a unified space.

1.3 Objective

The primary objective of this work is to develop such novel UNICA solutions that are efficient, compact, inexpensive, and easy to manufacture. Moreover, they should be able to radiate amplified powers to compensate the high path losses of mmW and THz frequencies and achieve desirable operating ranges. In this regard, this research work focusses to;

1. completely eliminate the dedicated matching networks and corresponding interconnections involved in the active circuits.
2. eliminate or reduce the number of feed lines utilized in the typical array antenna developments and,
3. constructively utilize the spacing and mutual coupling between array elements to design highly integrated circuit-antenna frontends.

Moreover, the research interest is also to perform the necessary analyses, develop theory wherever necessary, present generalized modeling procedures, and experimentally demonstrate the prototyping circuitry and radiation functions along with their characterization.

1.4 Organization

Chapter 1 discusses the background, motivation, and objectives of this research work.

Chapter 2 reviews the different frontend circuit-antenna integration approaches proposed earlier, which are organized based on the integration level, followed by the contribution of this work.

Chapter 3 introduces a unified circuit-antenna approach, presents a comprehensive analysis on microstrip rectangular patch antennas to demonstrate its abilities to operate as circuit in addition to radiation, and justify its choice in the design of unified circuit-antenna solutions. Following it, the general design process for active device integration between array elements in series has been

discussed and experimental prototypes are demonstrated for amplifying-circuit antenna operations. Moreover, the novel ways of characterising the parameters of the developed prototypes are also explained in detail.

Chapter 4 demonstrates the deep integration of multiple active devices directly within the rectangular patch antennas by etching appropriate slots within it, to realize simultaneous paralleled power amplification and radiation functions. All the relevant analyses, modelling procedures, comparisons, simulations, designs, and characterization are extensively presented. Furthermore, the potential integration of these unified modules to form an array configuration has also been proposed and experimentally verified.

Chapter 5 starts with a theoretical analysis on the signal coupled across any two-port network and discussion on the port impedances that influence it. Subsequently, the derivation for closed-form equation is presented, which can evaluate the impedance for a predefined magnitude and phase combination of the signal coupled across it. Following it, the procedure to load the active devices directly with antennas to realize an amplified radiation with a specified beam pattern is presented, and verified through two design examples.

Chapter 6 introduces the scalable and planar two-dimensional active-array antenna configurations that are intended for high-power applications. A novel arrangement of the relevant components including array elements, feed lines, and DC lines is proposed that supports the realization of the targeted UNICA solutions. The corresponding analysis and prototype development are discussed.

Chapter 7 delivers the generalized mesh-network equivalent model of rectangular patch antenna, that facilities a rapid design of UNICA solutions in schematic platform. Moreover, the applicability of the proposed model for different modifications inside the RPA has been evaluated and presented.

Chapter 8 presents a general discussion of this research.

Chapter 9 concludes the entire research work and gives an insight into the potential future research solutions adopting this approach.

In appendix, the realization of oscillation, wideband amplification, and low noise amplification functions are demonstrated through integrating transistor between array elements. All the corresponding analysis and design methodologies are included in the appendix.

CHAPTER 2 LITERATURE REVIEW AND CONTRIBUTIONS

To meet the requirements of evolving mmW and THz range applications, the research towards the unification of frontend active circuits with antennas has begun, which are capable of realizing compact, efficient, and low-cost solutions. Since the independent design of active circuits [37, 38] and antennas [39-41] at a reference impedance and their integration is well matured, we restrict the content of this chapter to demonstrate their integration techniques beyond the conventional approach. These developments are often referred to as active integrated antennas, active antennas, and deep integration of circuits and antennas in the literature. Till date, a significant number of the relevant research articles are available in the literature, covering a wide range of frontend circuitry functions along with radiation, and distinct integration approaches. In fact, some of these developments have been documented in relevant books [42-45] and literature review papers [19, 46-48], for reference. Nevertheless, few interesting and recent developments in this direction are presented here, which are divided based on their integration level. Moreover, different frontend active circuit configurations are discussed in each of these developments.

2.1 With input and output circuitry

Traditionally, the frontend active circuits consists of active devices along with the input and output circuits. Subsequently, the research towards reducing a number of lossy output circuitry elements by realizing them through the integrated antennas has begun, which are discussed in this section.

2.1.1 Oscillator

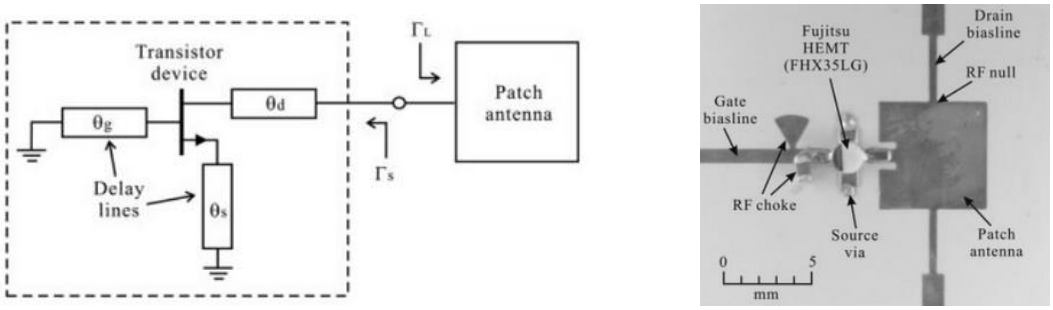


Figure 2.1: Negative resistance oscillator circuit integrated with patch antenna [49].

The delay lines at the gate and source terminal of the transistor are optimized to realize a negative resistance at its drain terminal. Subsequently, the delay line and patch antenna integrated at the drain terminal are tuned to satisfy the oscillation conditions. Different oscillator-antenna prototypes are thereby reported operating in C and X-bands with a phase noise around -70 dBc/Hz [49].

2.1.2 Amplifier

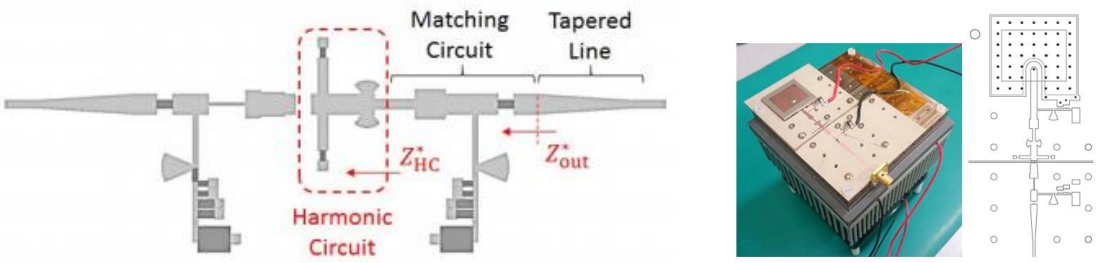


Figure 2.2: Amplifier circuit with input, output matching networks, and harmonic suppression circuitry integrated with rectangular patch antenna [50].

In [50], the class AB amplifier is designed at 5.8 GHz with input and output matching networks, along with an additional network to handle the second harmonic of 11.6 GHz. Subsequently, the designed amplifier is integrated with the patch antenna, which is designed to have an input-impedance that decreases the complexity of amplifier output matching network. The resultant prototype exhibited a PAE of 59.93% and EIRP of 44.61 dBm.

(a) (b)

Figure 2.3: Amplifier-antenna with input and output matching networks, while harmonic suppression is achieved through (a) diagonal slots etched in rectangular patch antenna [51] and (b) circular sectoral antenna with 120^0 cut [52].

Subsequently, the antennas are designed to handle the non-linear amplifier harmonics in addition to radiation, thereby absorbing the relevant circuitry within them. The introduction of diagonal slits inside a rectangular patch antenna has been reported in [51] which improved the PAE of the realized class-B amplifier-antenna integration by 4-5% at 2.37 GHz. Similarly, a circular sector antenna with 120^0 cut out is proposed in [52] for harmonic control. The corresponding prototype designed at 7.25 GHz demonstrated a PAE of 42 %. In both these designs, the output-matching network is designed to directly transform the non-linear power amplifiers impedance to the integrated antennas impedance.

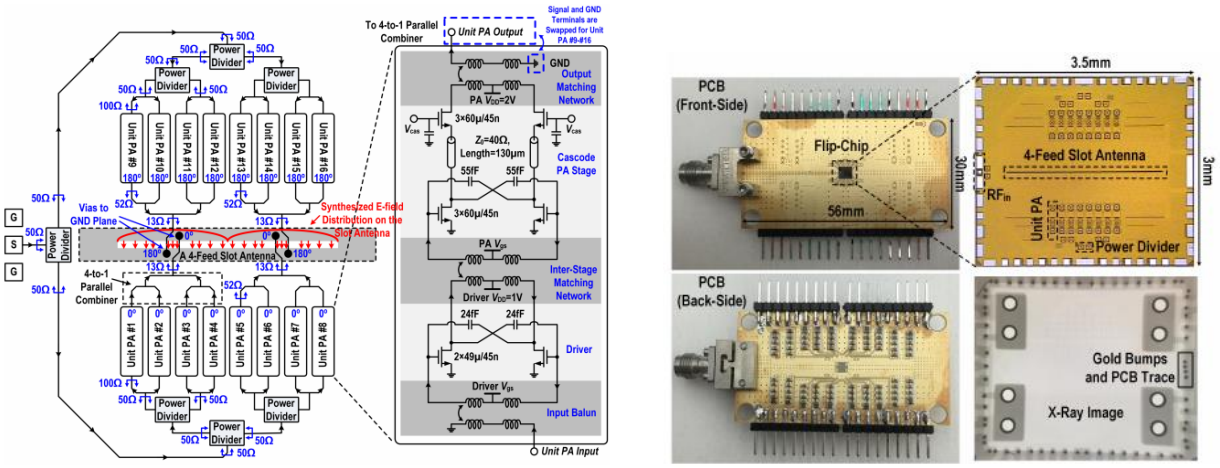


Figure 2.4: Paralleled amplifier circuitry with input circuitry of power dividers, matching networks and output matching network and low complex power combiner directly integrated with multiport slot antenna [53].

On the other hand, a paralleled power amplifier (PA) integration with the slot antenna is reported in [53], where each unit PA comprises of class B and class AB amplifier stages. While the power amplifiers involves the input and output circuitries, the complexity of output power combiner is reduced by directly integrating its multiple outputs with the slot antenna [at appropriate impedance locations as shown in Fig. 2.4]. The realized prototype exhibited a PAE of 23.4 % and EIRP of 27.9 dBm at 59 GHz.

2.1.3 Self oscillating mixer

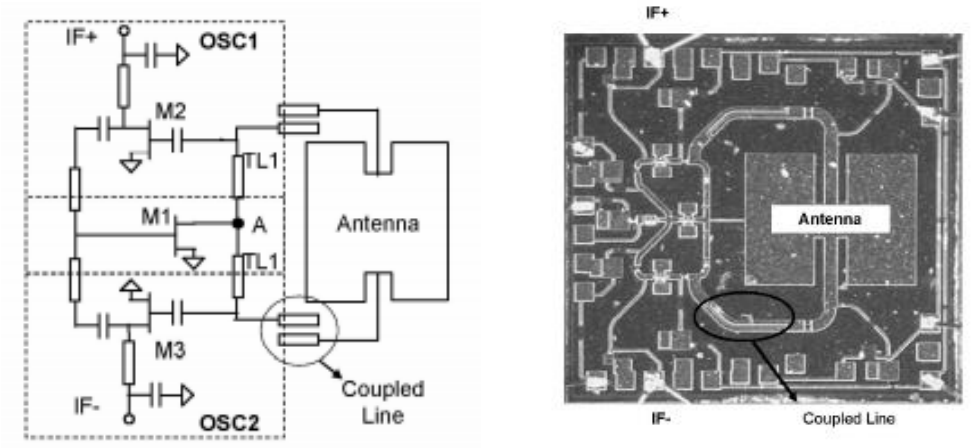


Figure 2.5: Balanced self-oscillating mixer circuit integrated with the differential excitation of rectangular patch antenna [54].

A self-oscillating balanced mixer configuration integrated directly with the differential excitation of the rectangular patch antenna is proposed in [54]. This prototype is designed for the receiver end with input mmW signal of 60 GHz and LO of 58.46 GHz. Correspondingly, the measurements demonstrated a -18.9 dB effective isotropic conversion gain at 1.54 GHz IF. However, the couplers, feedback oscillator circuitry, and other components are still present along with the antenna.

2.1.4 Frequnecy multiplier

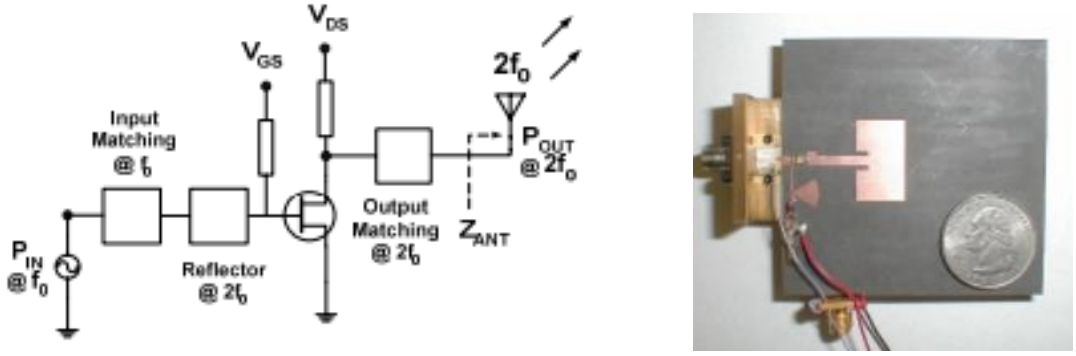


Figure 2.6: Frequency multiplier circuit with input and output matching network integrated with rectangular patch antenna [55].

The frontend frequency doubler circuit integration with a rectangular patch antenna that is designed at second harmonic is demonstrated in [55]. Here, the fundamental frequency suppression at the output has been achieved directly through the designed antenna. Moreover, the output-matching network is designed to directly match with the antennas impedance. The realized 4 GHz to 8 GHz prototype demonstrated a conversion gain of 5 dB and an output power of 25 dBm.

All these demonstrated prototypes including spatial power combining oscillator-array antenna [56], dual frequency self-oscillating dual frequency radiator [57], broadband class-E power amplifier-antenna [25], power amplifier-antenna [58] and so on have reported enhanced performances and are compact compared to the conventional counterparts, due to a relatively lower number of output circuitry components. However, the output circuitry still induces losses and influences the antennas performance. For reference, the influence of output matching networks has been extensively analyzed and reported in [59]. In fact, these drawbacks have forced the researchers to develop even more compact and efficient solutions.

2.2 With only input circuitry

As a result, the absorption of entire output circuitry within the antenna has been studied to reduce their awful effects, and further improve the integration and efficiency. This section presents such solutions where a dedicated output circuitry is eliminated, while the input circuitry is still present.

2.2.1 Oscillator

Figure 2.7: Co-design of negative resistance oscillator circuit with microstrip patch antenna [60].

The terminating network at the gate terminal of transistor is designed to generate a negative resistance at its drain terminal at the design frequency. Then the patch antenna is designed to satisfy

the oscillation conditions, thereby eliminating the dedicated matching circuitry at drain terminal. The realized prototype [Fig. 2.7] oscillates at 1.512 GHz with an EIRP of 18.2 dBm [60].

2.2.2 Amplifier

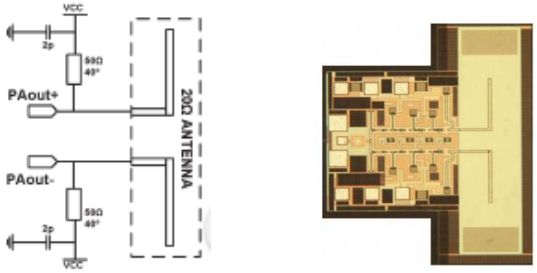
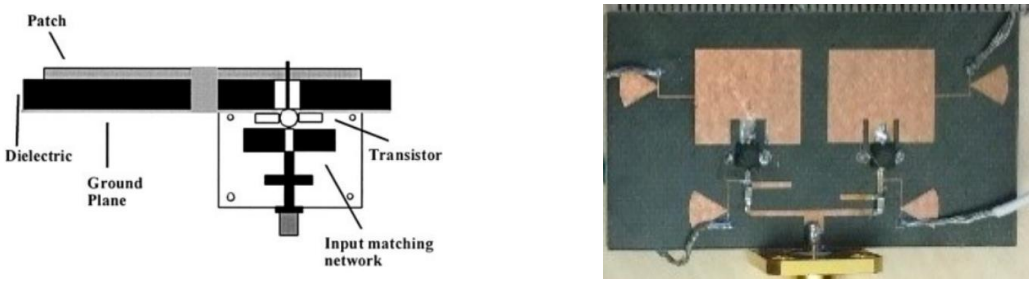


Figure 2.8: Co-design of power amplifier with dipole antenna [61]



(a) (b)

Figure 2.9: Amplifier-antenna configuration with input circuitry and transistor output directly integrated with (a) a single RPA [62] and (b) each RPA in a 1x2 array [63].

In [61-63], the output matching networks of amplifier are absorbed by antenna, by designing it to have an input impedance defined by the preceding active device output. A differential PA integration with dipole antenna is shown in Fig. 2.8, which exhibited an EIRP of 8.5 dBm at 77 GHz, where the dipole impedance is controlled by varying its line width. Stacked patch antenna integration with transistor for wideband amplification is shown in Fig. 2.9(a), which is matched between 1650 MHz and 2300 MHz and exhibits an 11-12 dB EIRP improvement compared to passive counterpart. A 1 x 2 class-A amplifier-antenna array operation achieved through direct active device integration with appropriately designed RPAs is shown in Fig. 2.9(b). The antenna

dimensions and feed positions are tuned for impedance modification of RPA. The demonstrated prototype at 10 GHz reported a 12 dB amplification gain and beam steered radiation.

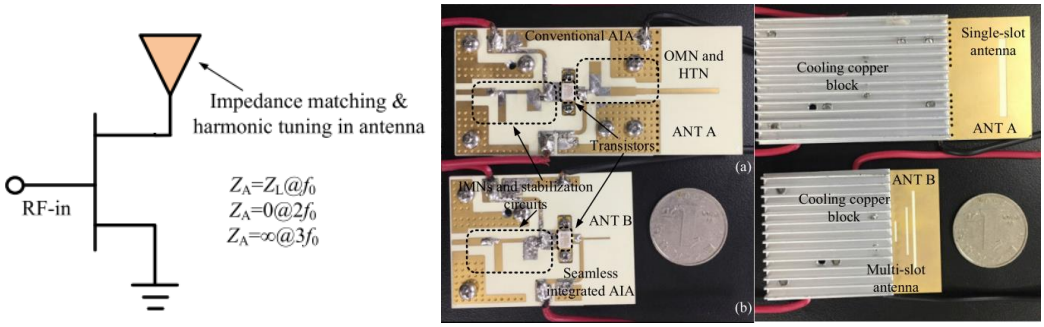


Figure 2.10: Co-design of class-F amplifier with slot antenna by avoiding output circuitry elements [64].

As shown in Fig. 2.10, the matching network and harmonic tuning circuitry required at the output of a Class-F power amplifier are absorbed into the slot antenna [64]. Additional slots are etched and optimized in this case to control the impedances at harmonics. The demonstrated prototype realized over PAE of 52% between 3.4 GHz and 3.6 GHz, which is 14.2% more than the conventional configuration.

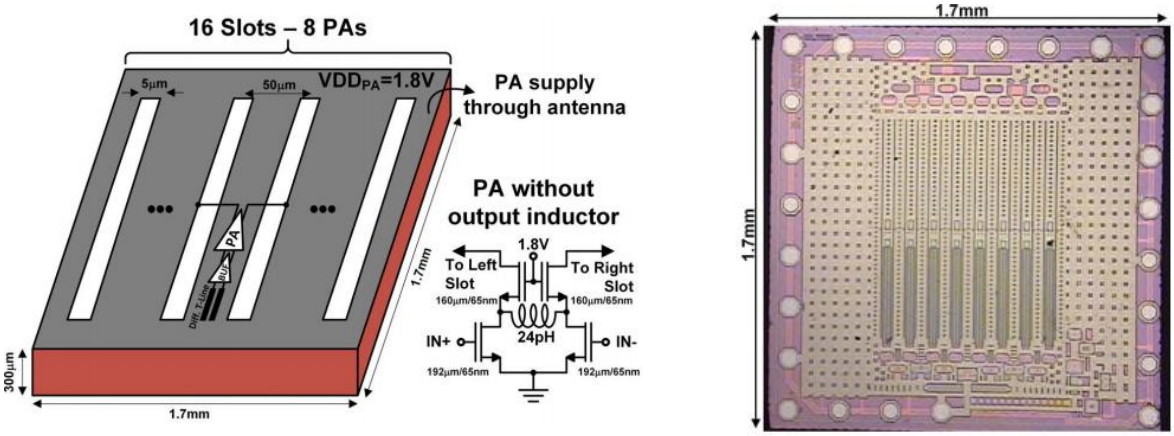


Figure 2.11: Multiple power amplifiers integrated with multiport slot antenna [65].

A 16 element slot array antenna integration with 8 pseudo differential PAs is proposed in [65], as show in Fig. 2.11. Here, the slot antenna dimensions are tuned to realize the desired impedances

and directly match with the output of active elements in PAs. The prototype designed between 69-79 GHz in CMOS exhibited an EIRP of 35.7 dBm and PAE of 30.8 %.

2.2.3 Self oscillating mixer

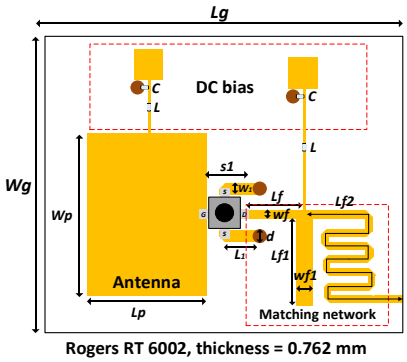


Figure 2.12: Self-oscillating mixer-antenna with rectangular patch antenna directly connected with active devices for receiving frontend solutions [66].

A SOM-antenna is proposed in [66], where the antenna is designed to simultaneously satisfy the impedance requirements at RF and LO and achieve a lower noise frequency conversion, by tuning its length. This eliminated the typically required dedicated multiband matching networks and interconnections between antenna and active device, along with the oscillator circuitry. The prototype is designed for receiver system, and the experiments demonstrated that the received RF signal of 10 GHz is mixed with a LO of 10.8 GHz and exhibits a 10 dB maximum conversion gain at 0.8 GHz IF.

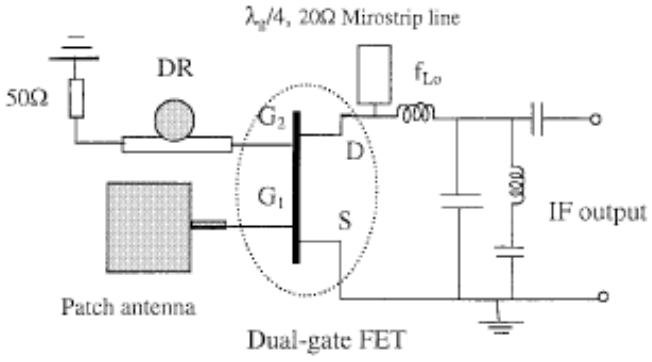


Figure 2.13: Integration of dual gate FET with receiving rectangular patch antenna and circuitry for oscillator to realize self-oscillating mixer operation [67].

Alternatively, a SOM-antenna configuration with dual gate FET has been reported in [67], which improves the isolation between RF and LO signals. One of the FET's gate terminal is directly integrated with the patch antenna for receiving the RF signal, while the oscillator circuitry is present at the other gate terminal. The demonstrated prototype oscillates at 4.045 GHz and mixes with input RF signal from 3.145 to 4.045 GHz to realize IF from 0 to 900 MHz, with maximum IF at 440 MHz which is the antenna resonance.

2.2.4 Frequency multiplier

Figure 2.14: Unified frequency doubler-antenna prototype demonstration with appropriately designed multiport rectangular patch antenna suitable for high power applications [68].

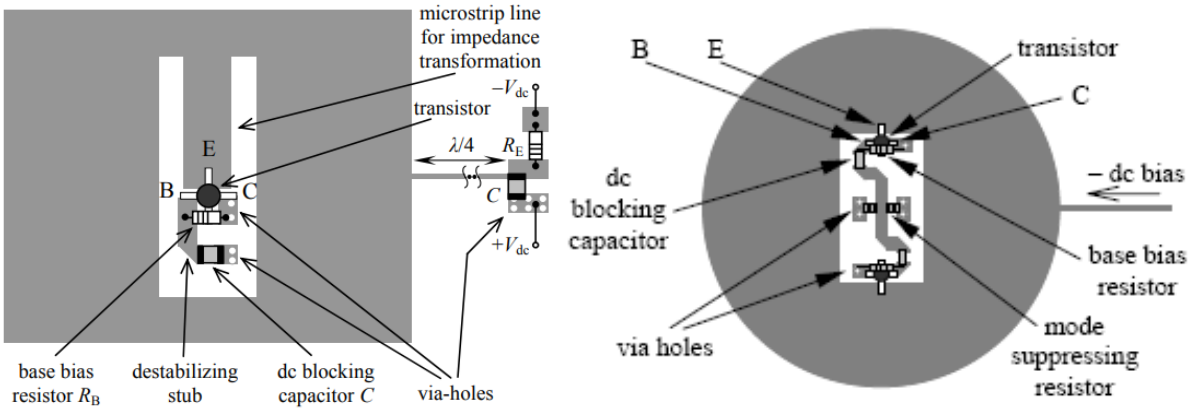
A high-power-oriented frequency doubler integration with a rectangular patch antenna designed at second harmonic is demonstrated in [68]. The antenna length is tuned to directly realize the impedance defined by the active device at second harmonic. Also, the fundamental frequency suppression and multiport excitation features are reported. As a result, all the output power circuitry is absorbed by the antenna, and the demonstrated 14 GHz to 28 GHz prototype achieved a conversion gain and fundamental suppression of 9 dB and 14 dB, respectively.

All these solutions along with oscillator-array antenna [69], amplifier-antenna [70] are physically more compact, and eliminates the losses and radiation effects of the output passive circuitry components. However, the above-described integrations do not benefit completely from the inherent circuitry behaviour of the antennas in the development. Moreover, the losses and radiation effects from the input circuitry are still prevalent.

2.3 Circuit inside antenna

Nevertheless, a few works have also proposed the integration of all the active circuitry within the antennas. Such developments realize an extremely compact solution and are reported here.

2.3.1 Oscillator



(a) (b)

Figure 2.15: AIA with oscillator circuitry integrated within properly etched slots in (a) rectangular patch antenna [71] and (b) circular patch antenna [72].

In [71, 72], the entire negative resistance oscillator circuitry is directly integrated within the slots etched inside the rectangular patch and circular patch antennas. These slots are devised to have minimal influence on the antennas performances, and all the circuitry components are soldered on the same layer. The developed prototype as shown in Fig. 2.15(a) operates at 2.3 GHz and achieved an EIRP of 19.4 dBm, while the prototype shown in Fig. 2.15(b) exhibited an EIRP of 25.3 dBm around 2.1 GHz. They both reported the tuning of antenna dimensions to realize the desired impedances and also demonstrated frequency tuning with bias.

2.3.2 Amplifier

The direct integration of the small signal amplifier and switching circuits within the diamond shaped ring patch antenna on the same layer, is reported in [73]. This approach realizes a compact

solution that occupies 57 % less that the conventional prototype. In addition to the amplified radiation, the realized prototype also enables switching between the circular polarization of radiated signal.

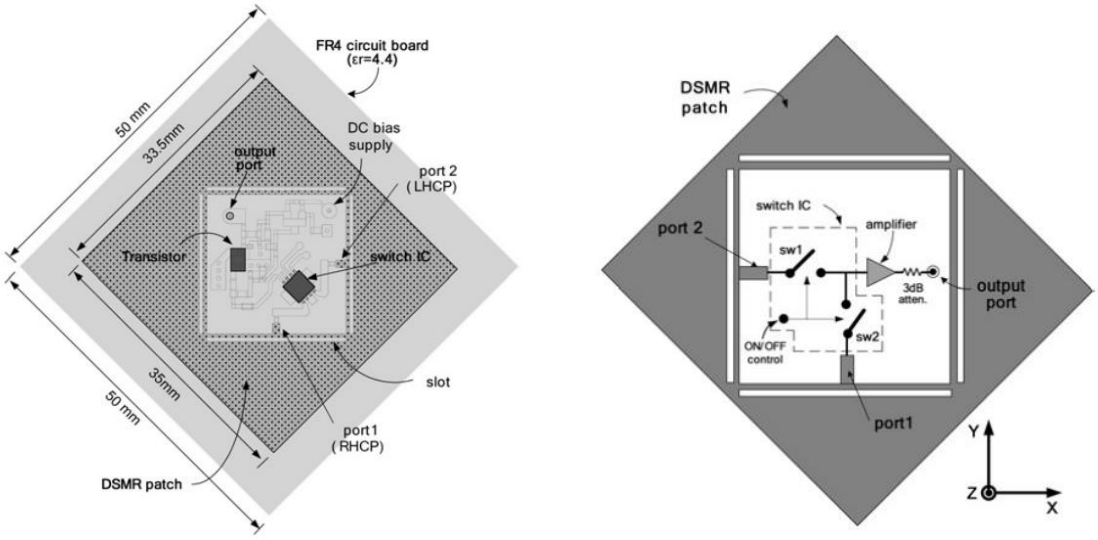


Figure 2.16: Amplifier-antenna with reconfigurable circular polarization diversity[73].

2.3.3 Self oscillating mixer

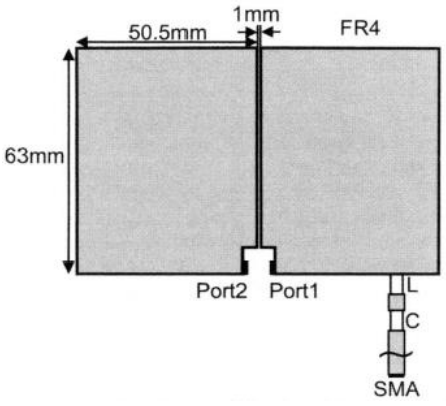


Figure 2.17: SOM-antenna demonstration with amplifier integrated within dual patch radiators [74]

The work in [74] demonstrates a direct amplifier circuit integration between port 1 and port 2 to realize simultaneous oscillation and radiation at 1.2 GHz. Furthermore, the receiving RF signal will mix with the generated oscillation signal, resulting in a self-oscillation mixing operation and

receiving the IF signal. A conversion gain of -5.4 dB to 5.54 dB is thereby reported, which is varied with biasing and chosen IF.

2.3.4 Transceiver

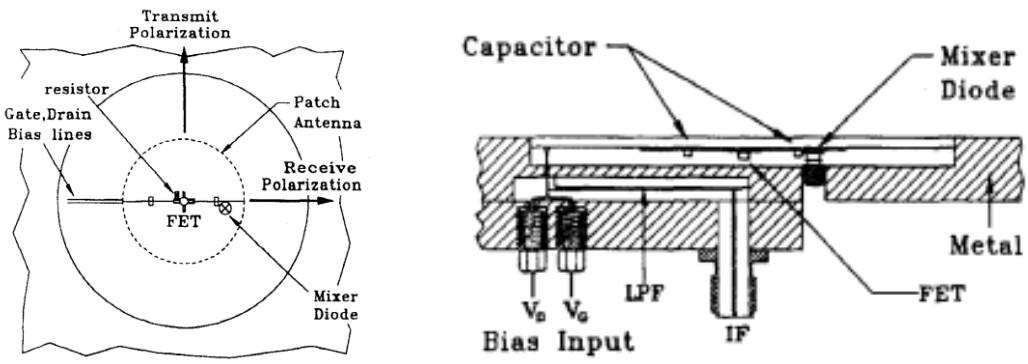


Figure 2.18: Transceiver functions realized through corresponding circuitry integrated within circular patch antenna [75].

The FET is integrated inside the circular patch antenna to simultaneously oscillate and transmit the signal. A part of this transmitted signal is received by the mixer diode, which performs the mixing operation and results in the IF signal in conjunction with the received RF signal in orthogonal plane All the necessary components are intelligently placed inside the antenna [75]. A 5.5 conversion loss is thereby reported through this prototype operating at 6 GHz RF and 0.2 GHz IF.

In addition, amplifier and filter integrated inside a hollow dielectric resonator is proposed in [76]. Nevertheless, these solutions are still lossy and impact antennas performances even though they are compact. Furthermore, this configuration is not practically realizable for mmW applications where the antennas size is very small and comparable to the circuitry elements.

2.4 Active devices only with antenna

Finally, the absorption of all the input and output passive circuitry present in an active circuit by the antenna has been proposed. The corresponding intelligent solutions involve only the active devices and antennas, which are appropriately designed and interconnected. These are the deeply unified compact and efficient solutions, where the dedicated components are eliminated and

antenna acts as circuit and vice versa. The corresponding demonstrations are presented here, covering different frontend circuitry functions.

2.4.1 Oscillator

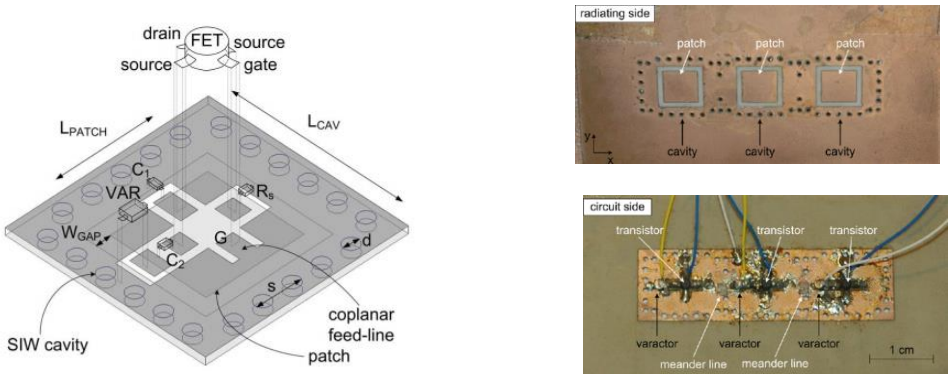
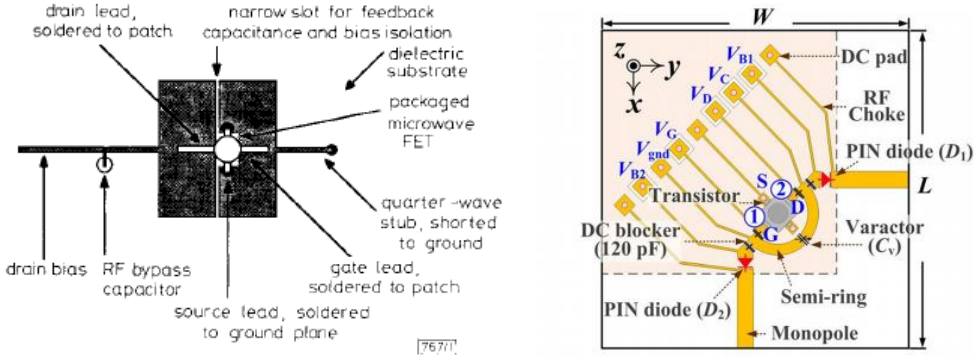


Figure 2.19: Active device integration with SIW cavity backed rectangular patch antenna for oscillation and radiation functions, and demonstration of beam scanning [77]

The active device only integration with an SIW cavity backed patch antennas for oscillation-radiation at 10.55 GHz is proposed in [77]. Here, the impedances required at both the terminals of transistor are satisfied by integrating them at appropriate locations of the same antenna. Furthermore, the arrangement of these elements in an array configuration to realize beam steering functions without phase shifters is also reported.

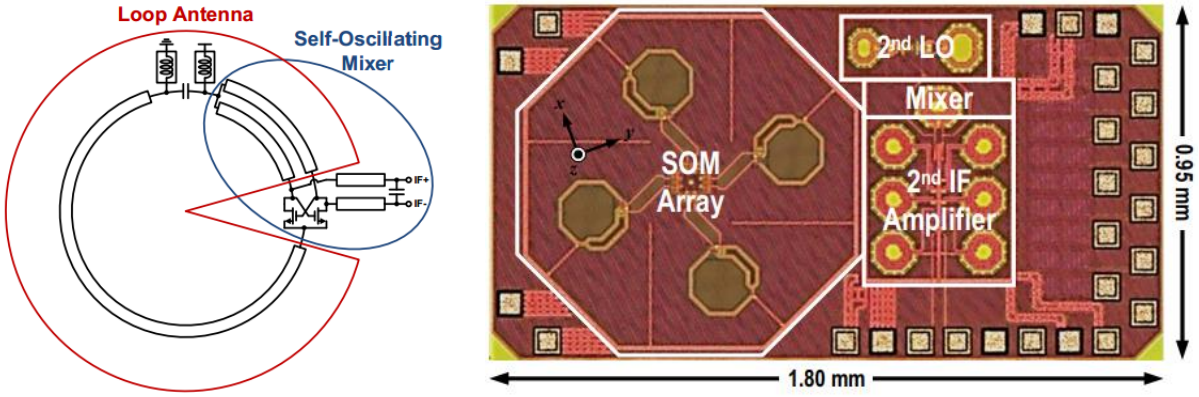


(a) (b)

Figure 2.20: Oscillating-antenna with active device integrated within (a) rectangular patch antenna [78] (b) semi ring and monopole antennas for pattern reconfigurable features [79].

In addition, a planar oscillation-radiation configuration where the active device co-exists with the antenna on the same layer are also reported. The corresponding oscillator design reported in [78] and shown in Fig. 2.20 (a) has exhibited a 6 mW output power at design frequency of 8.2 GHz. On the other hand, the oscillation functions along with reconfigurable radiation pattern features are proposed in [79], by using additional switching diodes as shown in Fig. 2.20 (b). The corresponding demonstration has EIRP varying from 5.4 to 9.3 dBm from 4.27 GHz to 4.94 GHz, along with a phase noise better than -102.7 dBc/Hz.

2.4.2 Self oscillating mixer



(a) (b)

Figure 2.21: (a) Harmonic self-oscillating mixer unification with loop antenna and (b) corresponding receiver system [80]

In [80], the third harmonic self-oscillating mixer and loop antenna are smartly merged to realize a receiver frontend within a compact space as shown in Fig. 2.21(a). As a result, this configuration incorporates the functionality of multiple devices including a band-selected antenna, a local oscillator, multiplier circuit, and a mixer. The receiving array thereby demonstrated in CMOS with additional LO, mixer, and amplifier [as shown in Fig. 2.21(b)] exhibited a conversion loss of 19 dB for a received mmW signal of 312 GHz to 1.7 GHz IF signal.

2.4.3 Frequency multiplier

On the other hand, an intelligent co-design of active devices and loop radiator has been demonstrated in [81] [as shown in Fig. 2.22]. This unified module performs the functions of signal generation, multiplication, filtering, and radiation through a single active electromagnetically coupled structure. The 2x2 array thereby realized at 291 GHz measures an output power of 80 μW and net EIRP of -1 dBm.

Figure 2.22: Co-existing multiple active devices with loop antenna for frequency multiplied signal radiation [81].

In addition, oscillator-radiator [82] and frequency reconfigurable oscillator-radiator [83] are also reported through eliminating the dedicated passive circuitry elements. These solutions are extremely compact with minimum circuitry losses and reduced radiation influences, which are desirable for mmW applications and beyond. As a result, the present research is oriented in this direction. Subsequently, the proposed integration approaches in this research work also fall in this category.

2.5 Discussion and contributions

The comparison of circuit-antenna integration status and the corresponding performances of all the discussed prototypes or demonstrators are further tabulated for reference in this work. As a part of it, Table 2.1 compares the oscillation-radiation prototypes, Table 2.2 compares the amplifier-antenna prototypes, Table 2.3 compares the mixer-antenna prototypes, and Table 2.4 compares the frequency multiplier-antenna prototypes.

Table 2.1: Comparison of oscillator-antenna performances.

Reference	***Passive circuitry***		***Antenna (Active device)***	***Operating freq. (GHz)***	***EIRP (dBm)***	***Phase noise (dBc/Hz)***
	Input	***Output***				
[49]	Yes	Yes	RPA (Fujitsu FHX35LG)	9	10	-85
[56]	Yes	Yes	RPA (Avantek ATF 26884)	10	15.6	-
[57]	Yes	Yes	SIW self duplexing (NEC NE3210S01)	7.97 8.9	5.3 6.41	-90
[60]	Yes	No	RPA (Cree CGH40010)	1.512	18.2	-
[69]	Yes	No	Series RPA array (NEC 71083)	10	-	-
[71]	Yes	No	RPA (HP AT-41485)	2.3	19.4	-
[72]	Yes	No	CPA (HP AT-41485)	2.1	25.3	-
[77]	No	No	SIW cavity backed RPA (NEC NE3210S01)	10.55	15	-
[78]	No	No	RPA (Fujitsu FSX03)	8.2	16	-
[79]	No	No	Semi-ring, monopole (NEC NE3512S02)	4.27-4.94	5.4-9.3	-102.7
[82]	No	No	Monopole (NEC NE3514S02)	5.05	-	-
[83]	No	No	Ring (NEC NE3512S02)	3.45 5.25	-1.2 4.3	-96.5 -84.6

Table 2.2: Comparison of amplifier-antenna performances.

Reference	*Passive circuitry*		*Antenna (Active device)*	*Amplifier class*	*Operating freq. (GHz)*	*BW (%)*	*Amplifier Gain (dB)*	*PAE (%)*	*EIRP (dBm)*
	Input	*Output*							
[25]	Yes	Yes	Cross slot coupled RPA (Agilent ATF34143)	E	1.78-2.06	14.6	-	50	-
[50]	Yes	Yes	RPA (Sumitomo SG0601C)	AB	5.8	-	-	60	44.6
[51]	Yes	Yes	RPA (CEL NESG2031M16)	B	2.37	-	-	68	-
[52]	Yes	Yes	Circular sectoral (ALGaN/GaN)	-	7.25	-	8	41	-
[53]	Yes	Yes	Slot (CMOS)	B and AB	60	-	17.4	23.4	27.9
[58]	Yes	Yes	RPA (Amplifier MGA 31689)	-	2.45	1.5	8	-	-
[61]	Yes	No	Dipole (SiGe BiCMOS)	Differential	79	7.5	19	-	8.5
[62]	Yes	No	RPA (Agilent ATF-35143)	-	1.65-2.3	33	11	-	-
[63]	Yes	No	RPA (CEL CE3512K2)	A	10	-	12	-	-
[64]	Yes	No	Slot (Cree CGH40010F)	F	3.5	5.7	12	66	42
[65]	Yes	No	Slot (CMOS)	Differential	69-79	13	-	30.8	35.7
[70]	Yes	No	Slot (Qorvo TGF2942)	-	20	-	9	34.8	30.7
[73]	Yes	Yes	Ring patch (Agilent ATF-55143)	-	1.575	5.3	17	-	-
[76]	Yes	Yes	Dielectric resonator (Amplifier TQP369181)	-	2.38-2.52	5.7	9	-	-

Table 2.3: Comparison of self-oscillating mixer-antenna performances.

References	*Passive circuitry*		*Antenna (Active device)*	*Operating freq. (GHz)*	*Conversion Gain (dB)*
	Input	*Output*			
[54]	Yes	Yes	RPA (GaAs)	f_{mmW}=60 f_{LO}=58.46	-18.9
[66]	No	Yes	RPA (CEL CE3512K2)	f_{RF}=10 f_{LO}=10.8	10
[67]	No	Yes	RPA (Dual gate FET)	f_{RF}=3.145-4.045 f_{LO}=4.045	-
[74]	Yes	Yes	RPA (Amplifier ERA-2SM)	f_{RF}=1.2 f_{LO}=1.18	4.6
[80]	No	No	Loop (CMOS)	f_{mmW}=312 f_{IF}=1.7	-19

Table 2.4: Comparison of frequency multiplier-antenna performances.

Reference	*Passive circuitry*		*Antenna (Active device)*	*Operating freq. (GHz)*	*Conv. Gain (dB)*	*Fundamental suppression (dBm)*
	Input	*Output*				
[55]	Yes	Yes	RPA (AlGaN/GaN HEMT)	4 to 8	5	11
[68]	Yes	No	RPA (CEL CE3512K2)	14 to 28	9	14
[81]	No	No	Loop (CMOS)	150 to 300	-	-

The presence of passive components (of an active circuit), antenna types, active devices/circuits, and the relevant parameters of all different circuit-antenna solutions are presented in Table 2.1-2.4. The PCB implementations are often utilized with commercial active devices integrated with antennas of choice, while the on-chip solutions are developed with their own active elements along with antenna structures.

Regardless of circuitry functions being realized, the RPA has been a widely popular antenna configuration that facilitates efficient integration with active device, and realizes simultaneous circuitry functions along with efficient radiation. However, a comprehensive analysis and a general description on the utilization of RPA as a passive circuitry and corresponding drawbacks have not

been addressed, which should be studied and understood. In addition, the accessibility to an equivalent schematic model of RPA that supports different geometric modifications in it will help speed up the UNICA designs, which has not been developed so far.

A majority of the previously proposed circuit-antenna solutions are limited to a single antenna integrated with active devices. In rare demonstrations, these joint circuiting-radiating modules are interconnected through traditional feed networks to realize array configurations. As these bring up losses, there is a necessity to develop alternative and smart ways to reduce a large number of dedicated passive components along with the feed lines even in the array developments.

Moreover, phase shifting control across the active devices has not been discussed in the past, which is worthwhile understanding to develop more intelligent solutions.

Table 2.5: An overview of the state-of-art works available in the literature.

Frontend circuit	***Oscillator***	***Amplifier***	***Mixer***	***Frequency Multiplier***
With input and output circuitry	[49], [56], [57]	[25], [50]-[53], [58]	[54]	[55]
With only input circuitry	[60], [69]	[61]-[65], [70]	[66], [67]	[68]
Circuit within antenna	[71], [72]	[73], [76]	[74]	[75]
Active devices only with antenna	[77]-[79], [82]-[83]	-	[80]	[81]

On the other hand, an overview of all the reported integration techniques along with different front-end circuit configurations is further described in Table 2.5. This illustrates that the amplifier circuit configurations with active devices integrated only with antennas have not been explored in the past. Besides, they cannot be ignored anymore, which form one of the most important frontend circuit blocks and should be investigated.

In this regard, this research work targets are set to propose distinct and innovative active-device and antenna integration approaches that achieve amplified radiation. Consequently, we intend to demonstrate solutions at both sub-10 GHz and mmW bands, and develop prototypes on PCB and

on-chip as well. Moreover, single, one-dimensional, and two-dimensional circuit-antenna array configurations are also involved and studied. In fact, the proposed solutions are more attractive for all the present-day and emerging applications.

The specific contributions of this research work are described as follows:

- A comprehensive analysis on the microstrip rectangular patch antenna (RPA) is presented to demonstrate its abilities to operate as the passive circuitry in addition to a good radiator. Additionally, the minimum spacing required between two RPAs arranged in an array, and the mutual coupling at non-resonating dimensions are also discussed.
- A general modelling approach and the design of 1 x 2 series array layout with active device integrated between array elements is proposed, to realize simultaneous amplification and radiation functions through a unified space. Moreover, these features have been experimentally verified through a prototype, which is free from matching networks and array feed lines.
- Developed novel methods to extract the characteristic parameters of these unified circuit-antenna solutions, as they cannot be measured in a traditional approach.
- Proposed and verified the deep integration of multiple active devices within RPA to realize simultaneous paralleled power amplification and radiation. An approach to self distributing them is demonstrated through a 2x2 amplifying-array antenna prototype which is experimentally verified. All the relevant analyses and design procedures are further presented.
- The impact of complex port impedances on the signal coupled across a two-port network is theoretically analyzed and presented. The derivation of an equation that evaluates the impedances corresponding to a predefined signal coupling across active devices is described. The meaning of the corresponding outcomes is analyzed, and explained in detail.
- Proposed general modelling procedures towards the design of amplifying-array antenna prototypes for beam synthesis applications, and experimentally demonstrated the 1x5 configurations. Here, only the active devices are utilized to simultaneously control the magnitude and phase of the signal exciting the array elements.

- A scalable and planar integration technique to realize two-dimensional amplifying-array antenna configuration is proposed, and verified through an 8 x 8 prototype design. The realized model is free from matching networks, and utilizes a reduced number of feed lines.
- A novel mesh-network equivalent model is developed for rectangular patch antenna that is capable of supporting different modifications in the RPA, and has been verified. This enables the initial co-simulations to be carried out in the schematic platform for a rapid design of unified circuit-antenna structures.
- The realization of simultaneous oscillation and radiation functions by integrating active device between the array elements is proposed and verified.
- Suggested a method to improve the stability of amplifier circuits without utilizing any additional components. Moreover, the introduction of wideband RPA as the input matching circuit to enhance the matching bandwidth of the amplifier-antenna designs is proposed and validated through a prototype design.
- A novel noise reduction technique is explored on the receiver front-end, and presented in detail. The necessary theoretical analysis, general modelling procedure and prototype demonstration are further presented.

CHAPTER 3 ARTICLE 1: UNIFIED AND INTEGRATED CIRCUIT-ANTENNA IN FRONT-END - A PROOF OF CONCEPT

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A concept of seamlessly co-located and co-integrated antennas and front-end chain circuits in the form of a unified and integrated design space is proposed, studied, and demonstrated in this work, which strives to create future joint circuiting-radiating front-end analog functional blocks. To show the proposed concept, the building elements involving dual-function amplifier-antenna are highlighted as an example and arranged in a series-connected array, each acting simultaneously as a matching circuit and transmitting antenna. In other words, a single geometrical space serves as both circuits and antennas, meaning a space overlap in which the circuit is an antenna and the antenna is a circuit. This reflects both the harmony and harmonious relationship of the circuit-antenna. In this research, the spacing between two neighboring array elements is utilized to accommodate active devices, such as transistors, in this example. As the first theoretical and experimental demonstration, this work involves the design of patch antennas, the analysis of mutual coupling and the placement of amplifying transistors in different operation modes. The modelling procedure for a 1×N amplifier-antenna system is presented. The proposed concept is experimentally validated by prototyping a 1×2 amplifier-antenna array at 5 GHz with rectangular patches and off-the-shell HJ-FET. An equivalent circuit network is established for the proposed dual function block. Measured results show that the experimental block has -10 dB matching bandwidth of 125 MHz at the steering angle of $+30^0$ with an amplifying gain of 11.5 dB. It is also experimentally illustrated that frequency tuning and beam steering can easily be enabled by varying the dc bias. The design of 1×4 amplifier-antenna array at 5 GHz is also discussed to generalize the proposed theory and guide the design of higher order amplifier arrays.

3.1 Introduction

Wireless technology has been evolving rapidly over time since the advent of radiofrequency (RF) transmitters and receivers. This phenomenon has been spurred by a fast-changing landscape of RF and microwave technologies and applications, in particular, front-end integration solutions and system architecture developments together with countless and diversified antenna techniques. Indeed, the last decades or so witnessed a vibrant growth and today, a myriad of inexpensive front-end devices and circuits are available for all types of applications like WLAN, cellular mobile, TV broadcast, etc., operating at frequencies below 6 GHz. Triggered by such overcrowded legacy RF spectrum allocations and persistent market demand for higher data rates, millimetre-wave (mmW) frequencies have become the emerging focus points of wireless research and development (R&D) projects [84, 85], which are related to much-publicized applications such as electromagnetic imaging [86, 87], automotive radar [88], short-range communication [89], space exploration [90], 5G and future wireless systems [16]. The advantages of mmW include high speed, better resolution, frequency reuse, increased integration, compact antenna etc. [3]. On the other hand, large free space path loss, line-of-sight propagation, in particular, parasitic radiations from circuits nearby antennas and high losses caused by signal feeders and line interconnections are some of the well-known bottleneck issues. Such parasitic radiations from proximity circuits are omnipresent in all RF and microwave systems, which can significantly deteriorate system performances. All the remedies usually require additional steps and measures through cumbersome electrical or mechanical techniques, which generally augment the burden and complexity of design cycle and fabrication process. Certain smart techniques have been proposed and studied to overcome those issues such as active integrated antennas (AiA), antenna-in-package (AiP), antenna-on-chip (AoC) and related solutions of integration, which will be briefly discussed in the following sections to highlight the particularity of our proposed technique. It is worthwhile mentioning that those existing schemes are not able to resolve the fundamental problems in connection with the relationship between circuits and antennas as they handle those two blocks in a separate and independent manner. Therefore, a disruptive solution is required to deal with this fundamental hurdle in the preparation of a circuit-antenna integration for the development of future front-ends.

To avoid any potential confusion with reference to terminology and substance in our discussions throughout this paper, signal feeders are referred to as all the circuitry that are part of antenna in this work, for example, RF circuits used to excite each element in an array. Similarly, interconnections are referred to as all the connecting parts among different modules in a front end, for example, interconnects between amplifier and antenna in this work.

An approach to coping with severe free space path loss without boosting circuit input power is to increase the radiation gain by deploying an antenna array. Nevertheless, this inevitably results in reducing the angular coverage because of a narrow beam width. This can be improved by a number of phased array techniques through a beam steering achieved by varying input signal phases and amplitudes fed into array elements in a well-synchronized manner. For the design platform of antenna arrays involving feed lines and phase shifters on the same layer as radiators [91, 92], the overall radiation performance is usually influenced by those comparably sized building components, which presents a serious issue for parasitic radiations and mutual couplings. To mitigate this awful effect, the feeding network and circuits are placed at the back side or on a separate layer in an attempt to isolate them from the radiating structure [93, 94]. However, the realization of multilayer integrations and vertical alignments is a tedious and costly process at higher frequencies. Also, the well-documented common disadvantage of both these single and multiple layer feeding configurations is an excessive loss resulted from feeders and interconnects.

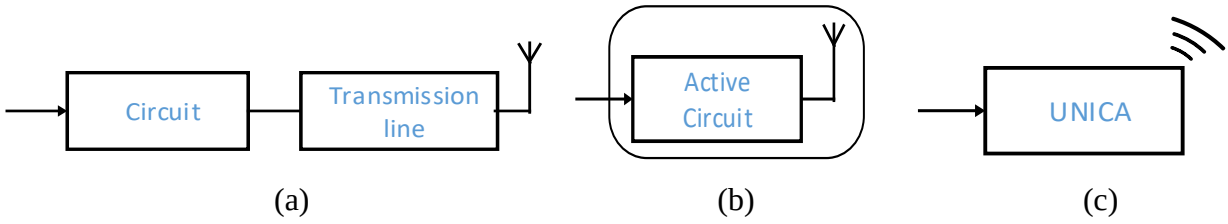


Figure 3.1: Block diagram of (a) conventional architecture (b) AIA approach and (c) proposed unified and integrated circuit antenna (UNICA) configuration

In order to reduce or remove the loss associated with feeders and interconnects involved in conventional configurations (as shown in Fig. 3.1(a)), the scheme of AiA [19, 46, 47] was proposed and developed, where active circuit and antenna are integrated on the same board close to each other as shown in Fig. 3.1(b). Generally, they are separately designed and interfaced through certain

pre-defined impedance ports. In special cases, active circuits and antennas are mutually related via electromagnetic coupling or connection through co-design approaches [95]. Although this scheme presents the advantages of compactness, low excessive loss, minimum power consumption and multi-functionality, which is attractive for high-frequency and mmW system developments, the presence of active circuits in the periphery of antenna is still existent for parasitic effects and the feeder loss in array architectures cannot be ignored.

On the other hand, emerging technologies such as AiP [96, 97] and AoC [98, 99] have been exploited for high-density and high-frequency integration-based wireless systems, which have already gained a significant popularity over the range of mmW and THz. Both schemes can provide better system reliability, functionality, and repeatability thanks to their robust processing techniques. AiP involves a set of process-dependent multi-chip modules packaged together with antenna (LTCC, e.g.) while AoC is generally based on a wafer-scaled integration of circuits and antennas (CMOS, e.g.). In some cases, AoC may also resort to multiple processing schemes that separately handle ICs and antennas. Nevertheless, those design platforms are still limited to the classical platforms in which circuits and antennas are designed separately and they are integrated via proximity electromagnetic couplings or short low-loss physical contacts and connectors (lines, balls, and other means).

3.2 Unified and Integrated Circuit-antenna (UNICA)

The above discussions suggest that existing approaches and configurations are not well suited for the antenna-circuit integration, in particular at mmW frequencies and beyond. In this regard, we propose a unification of circuit and antenna as a potential solution of all-in-one integration for future RF and mmW systems and refer it as “UNified and Integrated Circuit Antenna (UNICA)”. The fundamental driving thread behind this development is that in any RF/mmW front-end circuit, active circuit in particular, can be simply regarded as a core functional element such as diode or transistor surrounded by impedance matching networks. If such impedance matching networks can be absorbed by or embedded into antennas or radiators over a frequency range of interest, the circuit-antenna can be unified for in-situ integration. In this work, antennas are referred to as all types of radiating elements and structures. In this vision, a particular space or spot designed and arranged in a singlet or array operates simultaneously as antenna and circuit as shown in Fig. 3.1(c),

removing the necessity of additional circuitry such as matching network. In this way, the circuit elements can fully be distributed in the configuration of an array or vice-versa, depending on underlying design requirements and accomplished functionalities. The spacing along those functional pairs is utilized to accommodate active devices such as diodes or transistors, which also acts as feeding connectors of the array elements.

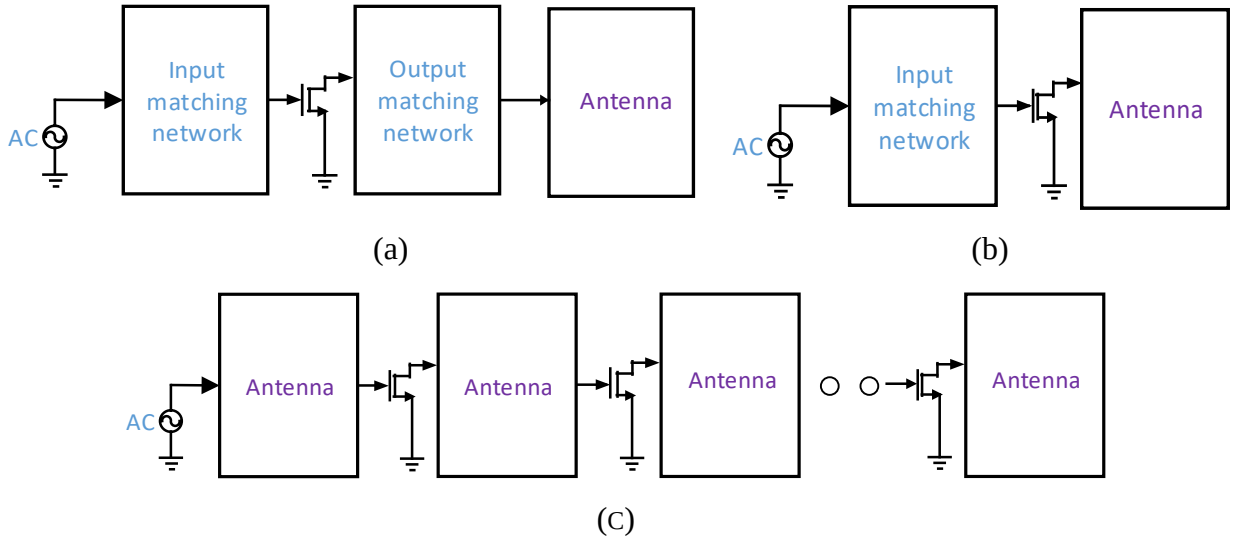


Figure 3.2: Block diagram of (a) AiA with input and output matching networks of amplifier interconnected to antenna (b) AiA with input matching network of amplifier and output matching load provided by antenna impedance and (c) proposed unification and integration

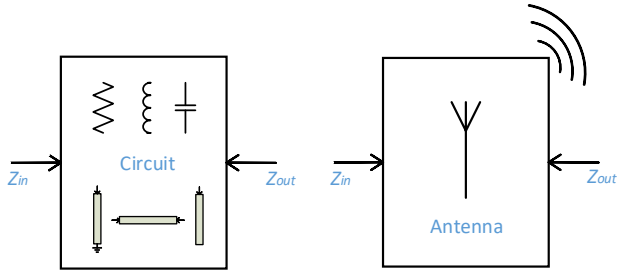
Since the circuits are realized by antennas, the impedance seen by active device should be related to the fields emitted by antenna rather than voltage and current. As a matter of fact, the proposed configuration has multiple features and functions, which may be summarized as follows; 1) an array that increases the gain to cope with a large free space path loss; 2) a steerable beam with varying dc bias of active device free from phase shifters for angular coverage; 3) no additional circuitry that affects radiation performance; 4) removal of lossy feeding lines replaced with active devices; 5) absence of lossy interconnections since antenna acts as circuit and circuit as antenna and; 6) increased integration density through the use of all space and mutual coupling between array elements.

Since, this unified circuit-antenna configuration effectively avoids the feed lines, interconnections and additional circuitry, we should be able to develop planar structured systems that are cost effective, light weight, compact size, and energy efficient. This concept may lead to the development of various unified and integrated circuit-antenna modules and systems in which the circuits may be made in the form of an amplifier, oscillator, self-oscillating mixer, transmitter, receiver, retrodirective array, reconfigurable array and so forth.

In this paper, we present the proposed concept through concrete example as well as design details and demonstrate the unification and integration of amplifier circuit and antenna (ACA) array as a proof of concept for the proposed design platform. To justify the uniqueness of our proposed ACA as a part of the demonstrative work, we compare it with the existing amplifier type of AiAs [100]. To the best of authors' knowledge, all the amplifier-based AiAs published so far have generally involved the straightforward design of two different building schemes, namely (i) amplifier circuit with input and output matching networks and interconnected to antenna, which acts as a load [50, 51, 101], as shown in Fig. 3.2(a), and/or (ii) amplifier circuit with only input matching network and antenna acting as both output matching network and load [102, 103] as shown in Fig. 3.2(b). The block diagram of the proposed ACA is sketched in Fig. 3.2(c) which comprises only antenna elements and active devices, simultaneously operating as amplifier circuit and antenna. This exemplified all-in-one design achieves array gain, amplifier gain, matching network, frequency tuning, and beam steering simultaneously within the same unified design space.

In the following sections, this new paradigm shift of future front-end design is illustrated through the realization of circuit functionalities by planar patch antennas. To this end, analysis of spacing, mutual coupling, placement of active device and also the modelling procedure for a general $1\times N$ ACA are presented. Subsequently, a 1×2 ACA operating in the dominant mode is designed with rectangular patches and commercial HJ-FET at 5 GHz for featuring simultaneous amplifier and antenna operations followed by an equivalent circuit model. Subsequently, the fabricated prototype is presented to validate the proposed concept through both simulation and measurement results along with discussions. Finally, the design of 1×4 ACA is presented along with simulation results, as an example to demonstrate the larger array realization of this unified configuration followed by concluding remarks.

3.3 Theory



(a) (b)

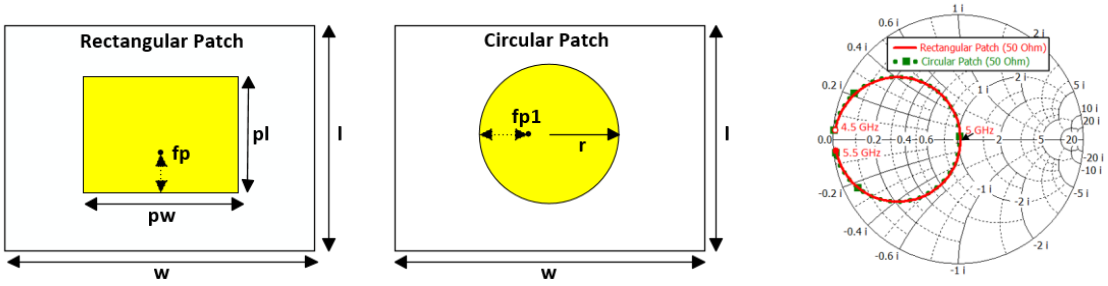
Figure 3.3: Block diagram showing (a) impedance looking into ports of circuit and (b) equivalent circuit impedance and radiation achieved by antenna design.

A RF and mmW front-end circuit, regardless of its inbuilt components (for example, lumped or distributed elements or transmission lines) can be considered as a black box with impedances Z_{in} and Z_{out} at input and output ports as shown in Fig. 3.3(a). The soul of our proposed concept lies in the ability to realize these circuit impedances Z_{in} and Z_{out} by antenna which also radiate as briefed in Fig. 3.3(b), thus replacing the circuit by antenna. This is the case of a circuit driven by antenna. Interestingly, this viewpoint can be also applied to the case of an antenna driven by circuit. This conceptual reciprocity can be easily understood as the circuit becomes an antenna and vice-versa.

In the following, the microstrip patch antenna and the circuit are used to showcase and reveal a typical scenario of a unified and integrated circuit-antenna pair for the development of front-end amplifying radiating blocks and arrays.

3.3.1 Antenna

Let us begin with the antenna that forms a primary building block of ACA and should be carefully identified. It is necessary that the antenna of interest should be; 1) capable of providing an appropriate impedance interface to achieve a desired circuit behavior such as “virtual matching network”, 2) flexible and agile to use different feed locations and topologies to achieve a wide range of impedance dynamics; 3) cost effective and low-loss; and 4) radiating efficiently with targeted patterns and polarization. In this case, carefully crafted circuit-antenna co-design techniques become a fundamental issue in this work.



(a) (b)

Figure 3.4: (a) Rectangular and circular patch antenna design in CST-MWS, *pw*= 22.6 mm, *pl*=16.5 mm, *fp*= 5 mm, *l*=40 mm, *w*=40 mm, *r*= 9.64 mm and *fp1* = 7 mm on substrate of $\varepsilon_r = 3$ with thickness of 0.508 mm, and (b) rectangular and circular patch input impedance performance in the Smith chart.

Table 3.1: Rectangular and circular patch radiation performance.

Parameters	Rectangular patch	Circular patch
Gain (dBi)	6.4	6.1
Radiation efficiency (%)	74	72
HPBW (deg.)	74.4	77.6

Planar microstrip patch presents the most widely used low-cost antenna solution owing to its straightforward integration and compatibility with planar circuits, leading to a preferred all-in-one UNICA design platform. Although various shapes are possible depending on design specifications, rectangular and circular geometries are likely considered at first. In this work, the impedance and radiation performances of these two antenna topologies are examined so as to pick up the best possible solution for our case-study. CST-MWS is utilized to design these two antenna topologies at the same resonance frequency of 5 GHz and under the same design conditions as depicted in Fig. 3.4(a). Excitation port impedances of both the structures are plotted in Fig. 3.4(b), suggesting a good overlap in the Smith chart. Similar radiation performances are also observed for both the antennas as shown in Table 3.1. Since, there is no visible and considerable difference between them in impedance performance and acceptable difference in radiation performance, our further analysis is limited to the geometry of rectangular patches. The outcomes can directly be applied to circular and other patch antenna structures as the fundamental principles essentially remain the same. It should be noticed that we are not concerned with any bandwidth issues for this work.

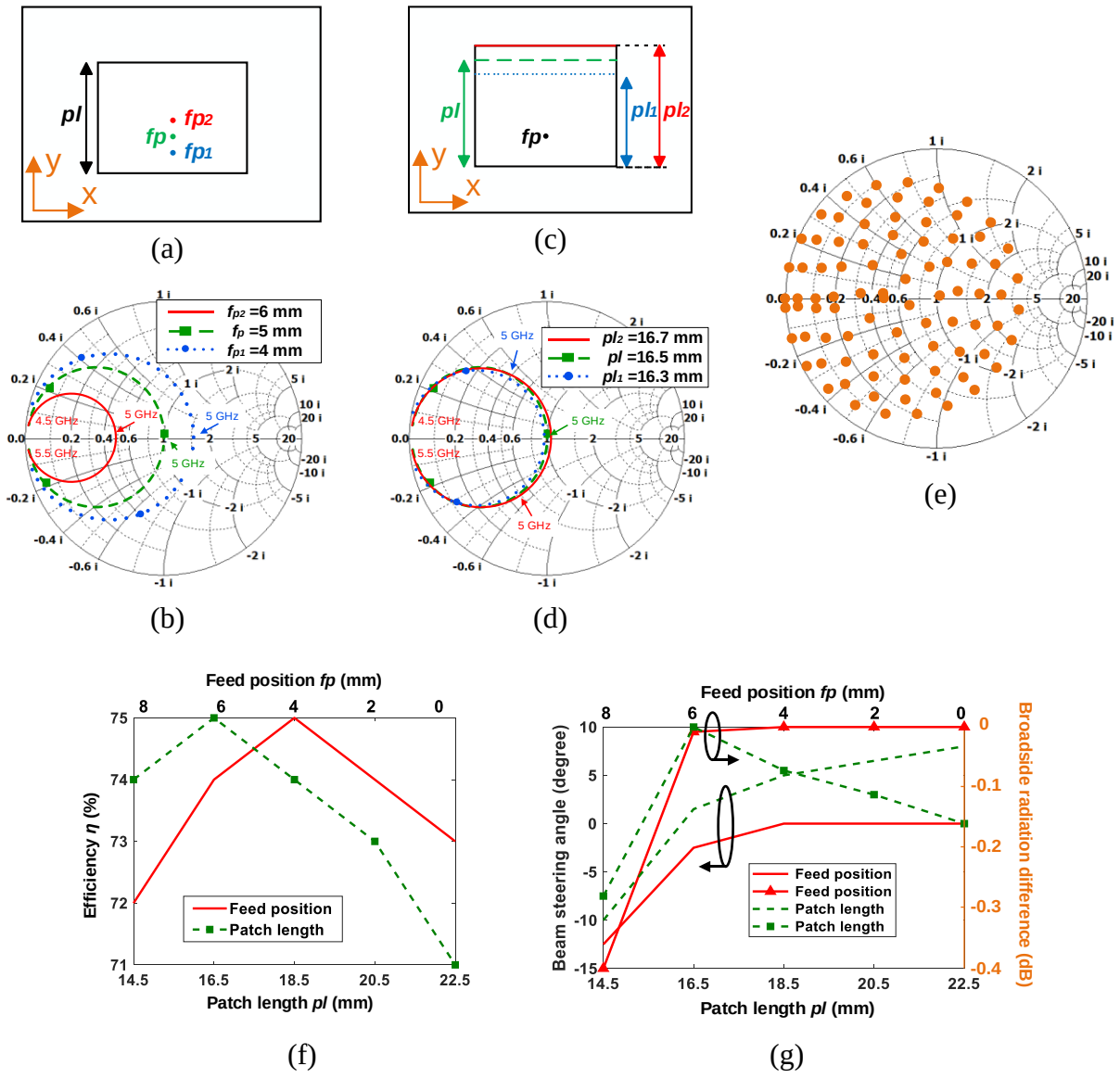


Figure 3.5: Rectangular patch antenna (a) showing feed locations - *fp1*, *fp* and *fp2* (b) impedance variation in the Smith chart for different feed positions (c) depicting patch length variation - *pl1*, *pl* and *pl2* (d) Rectangular patch antenna (a) showing feed locations - *fp1*, *fp* and *fp2* (b) impedance variation in the Smith chart for different feed positions (c) depicting patch length variation - *pl1*, *pl* and *pl2* (d) impedance variation in the Smith chart for different patch lengths (e) all the impedances realizable by varying length and feed position plotted in the Smith chart (f) radiation efficiency variation along with feed position and feed length change and (g) beam steering in E-Plane and radiation power difference of broadside with respect to maximum beam steering angle for various feed points and feed locations.

The inherent capability of a rectangular patch antenna to realize different impedance points is studied by designing it at frequency 'f_r = 5 GHz' with a coaxial feed. Fig. 3.4(b) shows the impedance behaviour of a matched antenna, which contains only a real term of 50 Ω at design frequency f_r. A direct way of varying this real part of impedance at f_r is to change the feed position along the center as shown in Fig. 3.5(a), and the result obtained for feed locations *fp2* = 6 mm, *fp* = 5 mm, and *fp1* = 4 mm are shown in Fig. 3.5(b). However, a slight tune of antenna length is necessary to achieve this real impedance at f_r. Additionally, the imaginary part of impedance can be modified by varying the patch length from its design frequency length *pl* = 16.5 mm as shown in Fig. 3.5(c). We can generate a capacitive behaviour by increasing the patch length, for example at *pl2* = 16.7 mm and an inductive behaviour by decreasing the patch length, for example at *pl1* = 16.3 mm (with *fp* = 5 mm being fixed for both cases) as shown in Fig. 3.5(d).

Subsequently, varying *fp* from 0 mm to 8 mm and pl from 14.5 mm to 22.5 mm will cover a majority of impedance points in the Smith chart as shown in Fig. 3.5(e) and shows a very good radiation efficiency of above 71 % in all the cases as presented in Fig. 3.5(f), which is close to 74 % achieved by the matched antenna. Although a beam steering is observed both for varying patch length (at fixed *fp*=5 mm) and feed position (at constant *pl*=16.5 mm), it is dominant only at the extremities as shown in Fig. 3.5(g). Even in the case of beam steering, the amount of power radiated in the broad side is never less than -0.29 dB for patch length variation and never below -0.4 dB for feed position variation relative to power radiated in the maximum direction for all cases. We can therefore conclude that the radiation performance is reasonably stable at f_r. for a variation in feed location and patch length. Thus, a rectangular patch antenna is able to provide the required dynamics of impedance similar to a normal circuit, in addition to its radiation performance.

In fact, the rectangular patch antenna is also flexible in the choice of its shape or feed type to achieve the uncovered impedance points. Thus, all the possible modifications may be simultaneously performed to achieve a specific impedance behavior mimicking a specific circuit, along with a targeted radiation performance. So, the rectangular patch antenna acts as a good replacement to circuits and is therefore utilized for the demonstration of ACA in this paper. Although, only the resonant patch antennas are discussed in this work, the proposed concept is not limited and can be extended to other resonant and non-resonating antennas provided there is a required impedance behavior with a desired radiation performance.

3.3.2 Mutual coupling and minimum spacing

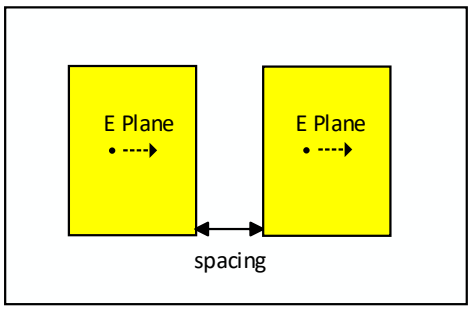
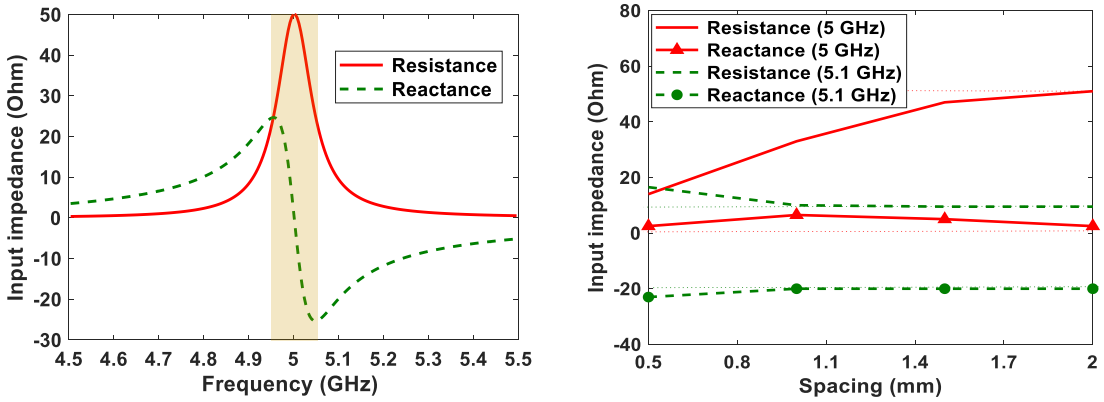


Figure 3.6: Visualization of E-plane and spacing in a series fed configuration.



(a) (b)

Figure 3.7: Input impedance of patch antenna (a) in isolated environment and (b) in array configuration varying spacing at 5 GHz and 5.1 GHz.

With the above-discussed scenarios and techniques, the proposed ACA structure can be realized by rectangular patch antennas, by arranging them in a serially connected configuration with active devices embedded in between. In this case, they are coupled in E-plane and the spacing between elements is determined by mutual coupling and active device size. Here, spacing is defined as the distance between edges of consecutively connected patch elements coupled in the E-plane as shown in Fig. 3.6.

In our design consideration, the development of ACA is generally focused on a higher-density integration on electrically thin substrate, which results in a near field coupling. This near field coupling decreases at rate of 12 dB when the distance is doubled due to the terms $1/r^2$ or 18 dB

when the distance is doubled due to the terms of $1/r^3$ [104]. So, even a slight increment of spacing can achieve a drastic decline in mutual coupling. Interestingly, for the spacing below a half wavelength in this near field region, the mutual coupling along the E-plane is small compared to the H-plane, which was also observed from measurements and discussed in [105]. This typically happens due to a dielectric substrate which influences E-field while ignoring H-field. This is an additional benefit of closely-spaced array elements in a serially fed configuration compared to its corporate feeding counterpart.

Traditionally, antenna is designed for 50 Ω input impedance to match the front end circuitry and achieving it in an isolated environment is practical. However, this is not feasible in an array environment because of the mutual coupling involved. Impedance characteristics of a typical rectangular patch antenna designed at 5 GHz (with dimensions as in Fig. 3.4(a)) in the isolated environment is shown in Fig. 3.7(a). It can be observed that resistance and reactance vary rapidly near the resonant frequency as highlighted in Fig. 3.7(a), which is also a typical behaviour of resonating structures. This rapid variation is the reason for a poor impedance performance of resonant antennas in an array environment, demanding for the analysis of mutual coupling and its reduction techniques for achieving a better control on individual array elements. Relaxing the 50 Ω input impedance concept has an advantage of loading the antenna in the non-highlighted region where the variation of resistance and reactance is rather smooth. This results in a relatively minimum mutual coupling effect on antennas input impedance even in an array environment and is discussed below.

Consider the same patch antenna design of Fig. 3.4(a) arranged in a 1×2 array configuration coupled in E-Plane as shown in Fig. 3.6, to study the impedance variation with spacing at resonant frequency of 5 GHz and an offset frequency of 5.1 GHz. Input impedance of the designed isolated antenna at 5 GHz is 50+j0 Ω and at 5.1 GHz is 10-j20 Ω. Variation of input impedance with increasing spacing between edges of array elements is shown in Fig. 3.7(b). It can be observed that input impedance at 5 GHz in the array environment matches closely with the isolated impedance at around 2 mm spacing with a large deviation observable at lower spacing. On the other hand, at 5.1 GHz, the impedance match of array antenna with the isolated one is achievable at minimum spacing of 1 mm, and offset observed in impedance even when closely spaced is very low. This confirms that designing antenna at offset frequency of its resonance length has a better impedance

performance in the array environment even at a small spacing realizing a high-density integration by still maintaining the radiation performance. In our demonstration, transistors that are commercially available in market are utilized and they directly accommodate in this spacing. In addition, this spacing falls into the near field region where the E-field coupling is less compared to that in H-plane.

3.3.3 Placement of FET

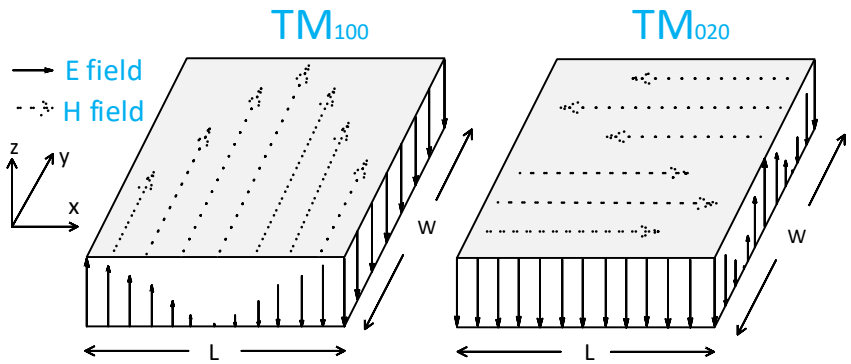


Figure 3.8: E-field and H-field distribution of patch for TM_{100} and TM_{020} modes.

Active device placed in between the antennas sees an impedance based on the fields governed by each antenna. So, its location (i.e. at center or at edge) depends on the field distribution, which is in turn related to the operation mode of antenna. For the dominant mode (TM_{100}) operation of patch antenna, E-field and H-field are constant along the width of patch as shown in Fig. 3.8 and therefore, the impedance remains nearly constant except at edges. Although, the transistor can be placed at any point along the width, it is placed at center to preserve the symmetry.

Considering the operation of a higher-order mode (TM_{020}, e.g.) as shown in Fig. 3.8, E-field and H-field vary along the width of patch and hence, the impedance varies in this case. As such, the location of transistor should be selected on the basis of a required impedance. In both the operating modes, multiple active devices can be placed at equal impedance points along the width, acting as a paralleled amplifier configuration. We can further extend this concept to develop other higher-order and multimode ACA models through the deployment of multiple transistors.

3.4 ACA mutual coupling analysis and general modelling steps

3.4.1 ACA mutual coupling analysis

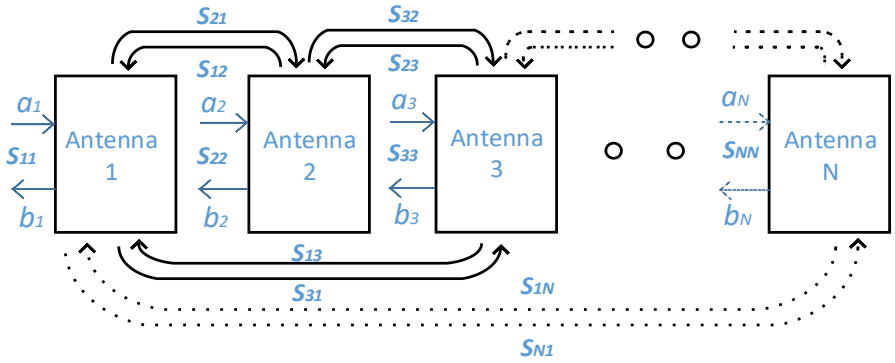


Figure 3.9: Block diagram showing S-parameter components of 1×N ACA.

Let us consider N antennas of a series feeding configuration, be individually fed with their respective signal as shown in Fig. 3.9, for the mutual coupling analysis of ACA. The whole system can therefore be described by a simple N-port S-parameter model as

$$\begin{aligned} b_1 &= S_{11}a_1 + S_{12}a_2 + S_{13}a_3 + \cdots\ S_{1N}a_N\,, \\ b_2 &= S_{21}a_1 + S_{22}a_2 + S_{23}a_3 + \cdots\ S_{2N}a_N, \\ &\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \\ b_N &= S_{N1}a_1 + S_{N2}a_2 + S_{N3}a_3 + \cdots\ S_{NN}a_N \end{aligned} \tag{3.1}$$

where $S_{ii\ (i\,=\,1,2..N)}$ is the reflection coefficient of corresponding antenna, $S_{ij\ (\,i\,=\,1,2..N,\ j\,=\,1,2..N,\ I\neq j\,)}$ is due to a mutual coupling between array elements. The mutual coupling results in a change of input impedance $(^{b_i}/_{a_i}, i = 1,2 \ldots N)$ looking into each antenna as described by

$$\begin{aligned} \frac{b_1}{a_1} &= S_{11} + S_{12}\frac{a_2}{a_1} + S_{13}\frac{a_3}{a_1} + \cdots\ S_{1N}\frac{a_N}{a_1} \\ \frac{b_2}{a_2} &= S_{22} + S_{21}\frac{a_1}{a_2} + S_{23}\frac{a_3}{a_2} + \cdots\ S_{2N}\frac{a_N}{a_2}, \\ &\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \\ \frac{b_N}{a_N} &= S_{NN} + S_{N1}\frac{a_1}{a_N} + S_{N2}\frac{a_2}{a_N} + \ldots S_{NN-1}\frac{a_{N-1}}{a_N} \end{aligned} \tag{3.2}$$

Since it is an ACA, the subsequent antenna *n+1* (*n*=1,2,3…*N*-1) is fed with an amplified signal ($a_{n+1(n=1,2,3\ldots N-1)}$) compared to the present antenna *n* (*n*=1,2,3…*N*-1) feeding signal $a_{n(n=1,2,3\ldots N-1)}$. Considering the case of an equal amplification for all the stages, let $\frac{a_2}{a_1} = \frac{a_3}{a_2} = \ldots = \frac{a_N}{a_{N-1}} = k$ ($k > 1$), where *k* is the amplification gain for which the ACA is designed. Substituting *k* in (3.2) results in (3.3)

$$\begin{aligned}
\frac{b_1}{a_1} &= S_{11} + S_{12}k + S_{13}k^2 + \cdots \; S_{1N}k^{N-1} \\
\frac{b_2}{a_2} &= S_{22} + S_{21}\frac{1}{k} + S_{23}k + \cdots \; S_{2N}k^{N-2}, \\
&\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \\
\frac{b_N}{a_N} &= S_{NN} + S_{N1}\frac{1}{k^{N-1}} + S_{N2}\frac{1}{k^{N-2}} + \cdots S_{NN-1}\frac{1}{k}
\end{aligned} \tag{3.3}$$

For higher amplification gain *k*, the antenna *n* (*n*=2, 3…*N*-1) input impedance is affected by the amplified signal radiated from the antennas *l* (*l*>*n*) next to it and not affected due to a low mutual coupling from antennas *m* (*m*<*n*) in front of it. For example, antenna *N-1* impedance is affected by only antenna *N* and not affected by antennas *N-2* to 1 in the front. So, the best way of designing an ACA is to start with N^{th} antenna and move on to 1^{st}, which is similar to the design of amplifiers in the operating power gain method, and is implemented here.

3.4.2 General modelling steps

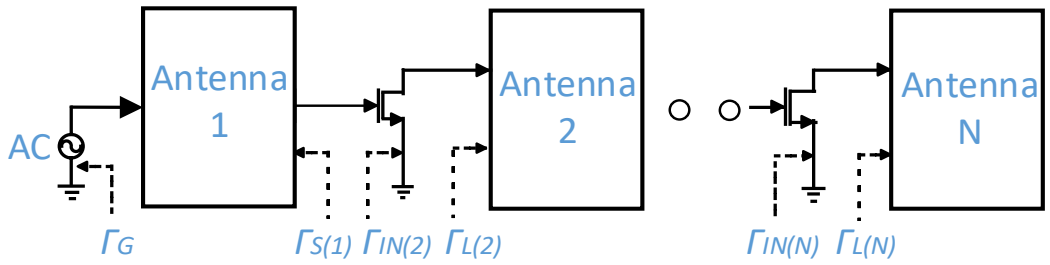


Figure 3.10: Block diagram showing reflection impedance components of a 1×N ACA.

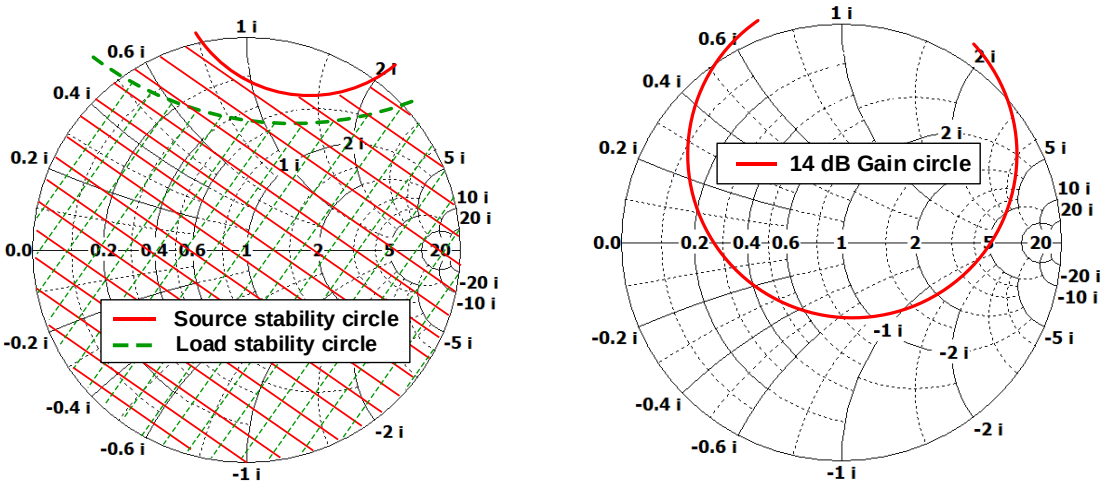
The key steps for designing an amplifier available in [37] are extended to include the design of amplifier circuits with antennas i.e ACA, and are described below (with definitions utilized as shown in Fig. 3.10.)

1. For the transistor chosen, stability analysis is performed first. If the transistor is potentially unstable which is generally the case, stability circles of source and load are drawn to identify the stable regions in the Smith chart. The desired operating power gain circle G_P is then drawn to choose the load impedance/reflection point on the gain circle located in the stable region and preferably far from the stability circle.
2. Chosen $\Gamma_{L(N)}$ is achieved by a proper design of antenna *N*, which also radiates. Then $\Gamma_{IN(N)}$ at the transistor gate terminal is calculated with the designed antenna *N* connected to the drain terminal.
3. Antenna *N*-1 is then designed to transfer conjugate of $\Gamma_{IN(N)}$ to $\Gamma_{L(N-1)}$, along with radiation.
4. If antenna *N*-1 has to be designed for the same gain as antenna *N*, $\Gamma_{L(N-1)} = \Gamma_{L(N)}$ is chosen or else step 1 is repeated again for the necessary gain to choose $\Gamma_{L(N-1)}$.
5. Then $\Gamma_{IN(N-1)}$ at the transistor gate terminal is calculated with antenna *N-1* connected to the drain terminal (which is already connected to transistor and antenna *N* on the other edge).
6. The design procedure for antenna *N-2* is similar to that of antenna *N-1* and the same procedure is followed up to antenna 2. (Since, the antennas *N*-1 to 2 perform similar operation.)
7. However, antenna *1* is designed for $\Gamma_{S(1)} = \Gamma_{IN(2)}^{*}$ at one end and conjugate of generator impedance Γ_G on the other end, in addition to radiation.
8. In case of a non-feasible impedance to be realized at any point, because of either the impedance close to stability circle or the limitation of antenna design, another point should be selected that provides the necessary matching and amplifier gain.

3.5 ACA demonstration

To prove the proposed concept, 1×2 ACA is demonstrated at 5 GHz. The substrate used in this case has a relative permittivity of 3 and thickness of 0.508 mm.

3.5.1 Active device analysis



(a) (b)

Figure 3.11: Smith chart showing (a) source and load stability circles along with stable regions highlighted and (b) 14 dB gain circle.

Active device - NE3512S02 (N-Channel HJ-FET) transistor is selected as it provides good amplification gain and low noise at the design frequency. Initially, stability analysis of the transistor (along with source degenerating via connecting source terminal and ground to include its effect) is performed in ADS. Stability factor K = 0.537 < 1 and stability measure B = 1.064 > 0 of the transistor are calculated from ADS, thereby suggesting that the transistor is potentially unstable and there is a necessity to identify its stable regions.

Source and load stability circles for the transistor are then drawn through ADS, and are shown in Fig. 3.11(a). Stable region includes the center of Smith chart as $|S_{11}|$ = 0.818 <1 and $|S_{22}|$ = 0.547 < 1, and stable regions are highlighted along with stability circles in Fig. 3.11(a). Maximum amplification gain of 18 dB can be realized by this transistor. However, for maximum stability of the design, an amplification gain of 14 dB is considered and its gain circle presented in Fig. 3.11(b) is drawn to choose the load impedance. The stability and gain circles shown here are only for the design frequency of 5 GHz.

3.5.2 Output load antenna

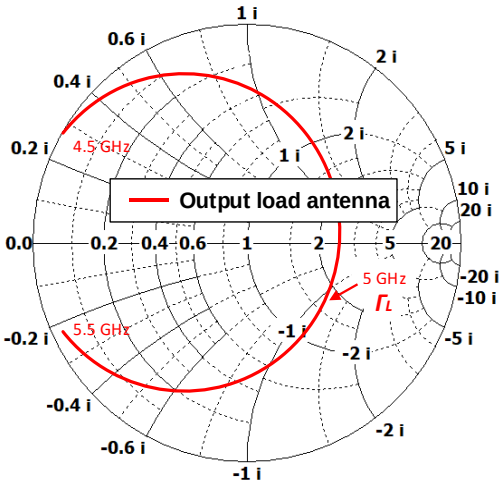


Figure 3.12: Smith chart showing input impedance variation of designed output load antenna.

Load reflection point (impedance) Γ_L= 0.47 ∠-33.12^0 (Z_L=90 – j60 Ω) is chosen from the amplification gain circle of 14 dB, in the stable region. The dimensions of the output load antenna are initially designed for the frequency of interest, and then the length and width are slightly tuned to achieve Γ_L at 5 GHz. The final antenna designed has a width of 22.6 mm and length of 16.78 mm. Impedance behavior of the output load antenna designed along with impedance marked at 5 GHz in the Smith chart is presented in Fig. 3.12. Also, it has a radiation efficiency of 73% and radiation gain of 6.3 dBi from simulations.

Then, Γ_{IN} is calculated with the output load antenna connected at the drain terminal of transistor, and the value of Γ_{IN} = 0.70 ∠-70.12^0 (Z_{IN} = 25 – j65 Ω) is obtained. However, the conjugate of this point is close to the source stability circle and so, another point Γ_S = 0.62 ∠92.64^0 (Z_S = 22 + j43 Ω) is chosen for a good matching with approximately 1 dB reduction in amplification gain.

3.5.3 Input matching circuit antenna

Design of input matching circuit with antenna is the most critical part since this antenna (a) must provide an impedance matching from Γ_S = 0.61 ∠92.22^0 (Z_S = 22 + j43 Ω) to Γ_G=1 (Z_G = 50 Ω) (b) should radiate a considerable amount of power and (c) must handle a strong mutual coupling from the load antenna.

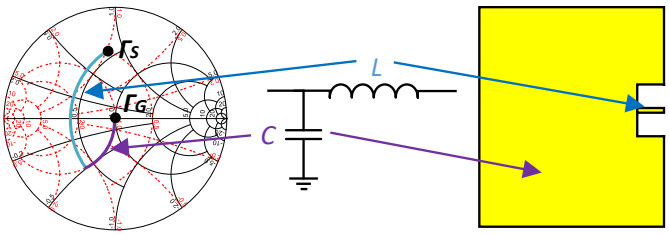


Figure 3.13: Matching circuit and equivalent input matching circuit rectangular patch antenna model

From the knowledge of matching circuits using lumped elements, we do know that a shunt capacitor and series inductor are necessary for matching Γ_S to Γ_G. The lumped component values of corresponding L matching network can be calculated from standard equations [38], which come out to be C= 0.72 pF and L=2.2 nH. This matching circuit acts as reference to design an equivalent input matching patch antenna. As shown in Fig. 3.13, the shunt capacitance is realized by increasing the resonant length of patch antenna and the series inductance is realized by modelling a narrow microstrip line in series.

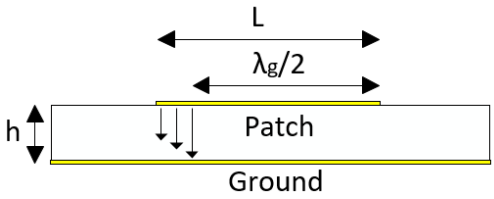


Figure 3.14: E-field distribution of patch for length above $\lambda_g/2$.

We can approximately calculate the length of patch L required from the known capacitance value C. It is to be noted that radiation loss, mutual coupling and other losses are not included in analysis, for the sake of simplicity. Considering a co-sinusoidal E-field distribution of the patch, reactance is zero for $\lambda_g/2$ length at resonant frequency. Increasing the patch length over that resonant length helps in achieving a capacitive behavior. Therefore, for E-field above that resonant length as shown in Fig. 3.14, traditional parallel plate capacitance formula cannot be utilized. So, parallel plate capacitance formula is modified by multiplying with effective electric field under the patch for the length more than resonant length (L-$\lambda_g/2$). Equation (3.4) can be used to approximately calculate

the length L of input patch antenna, which comes out to be 18.1 mm. (λ_g and β_g involved in equation are calculated for relative permittivity ε_r).

$$\left(L - \frac{\lambda_g}{2}\right) Sin(\beta_g L) = \frac{Ch\beta_g}{\varepsilon_0 \varepsilon_r W} \tag{3.4}$$

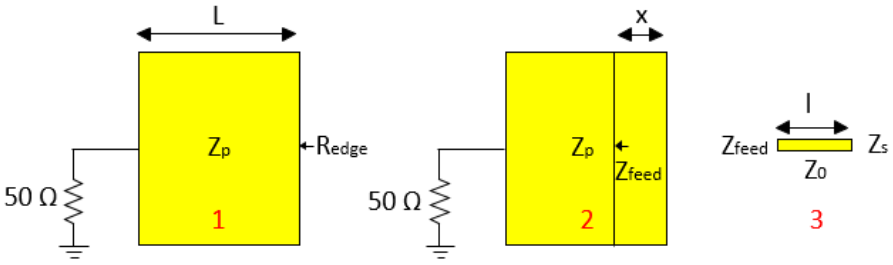
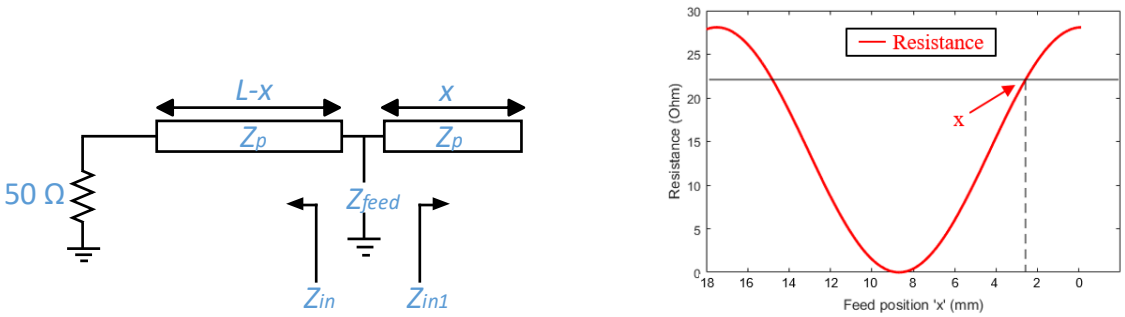


Figure 3.15: Input patch antenna design stages with all necessary variables.

The next part is to realize the inductance by adding a microstrip line of minimum possible width for fabrication (i.e 0.2 mm with our facility) at one edge, with the other edge of patch connected to 50 Ω load (because of excitation). This is achieved in three steps and are (1) to calculate the edge resistance of patch antenna of length L = 18.1 mm, (2) to locate the feed position x inside the patch antenna where feed resistance is the same as the source resistance and (2) integrating the inductance line of necessary length l to match the source impedance. All the necessary definitions and the steps involved are visually presented in Fig. 3.15, and are discussed below.



(a) (b)

Figure 3.16: (a) Equivalent transmission line model of rectangular patch antenna with all the losses ignored and (b) Resistance variation with respect to feed position of patch antenna.

As a part of the first step, the edge resistance of patch antenna is calculated from (3.5), with x=0, resulting in length L obtained from previous calculation. Z_p =4.75 Ω is the characteristic impedance of patch antenna (with width of 22.6 mm, kept the same as the output load antenna) and loaded with Z_G =50 Ω on the other edge. The edge resistance R_{edge} = 28 Ω is calculated from (3.5).

Subsequently, the feed position is to be calculated where feed resistance matches with source resistance of R_S = 22 Ω. An equivalent transmission line model of the patch is utilized to locate the same and is shown in Fig. 3.16(a) (radiation is not considered). As observed, one edge of patch is open and the other edge is loaded with Z_G =50 Ω impedance, x is the feed distance from the open edge. Equation (3.5) calculates the input impedance Z_{in} of loaded edge at feed and (3.6) (except at x=0) calculates the input impedance Z_{in1} from the open end at feed. From these two input impedances which are in parallel at the feed, effective feed impedance Z_{feed} is calculated from (3.7). The variation of feed resistance calculated by changing feed position x from 0.1 mm to 18.1 mm is plotted in Fig. 3.16(b) for reference. This shows that there exists two points to choose source resistance of R_S = 22 Ω, as expected. However, x = 2.5 mm, obtained from Fig. 3.16(b), is chosen to integrate the inductance line within the antenna close to open edge.

$$Z_{in} = Z_p \frac{Z_G + jZ_p(tan(\beta_g(L-x))}{Z_p + jZ_G(tan(\beta_g(L-x))} \tag{3.5}$$

$$Z_{in1} = -\mathrm{j}\, Z_p \, cot\, \beta_g x \tag{3.6}$$

$$Z_{feed} = \frac{Z_{in}Z_{in1}}{Z_{in}+Z_{in1}} \tag{3.7}$$

Once the x value is known, Z_{feed} = 22-j20 Ω is calculated at x =2.5 mm from (3.7). The final step is to approximately calculate the length of microstrip line l with characteristic impedance Z_0= 117 Ω to achieve the inductance necessary to transform Z_{feed} = 22-j20 Ω to Z_S = 22+j43 Ω. This is calculated from (3.8), which is the modified input impedance equation of transmission line with arbitrary load. The length of inductance line l is calculated to be 2 mm. Notably, all the parameters have to be optimized in a full-wave electromagnetic simulation software package for determining accurate dimensions and to include all the losses.

$$l \cong \left|\frac{1}{\beta_g}\tan^{-1}\left(\frac{Z_0(Z_{feed}-Z_S)}{j(Z_0^2-Z_{feed}Z_S)}\right)\right| \tag{3.8}$$

As specified, the patch antenna width is fixed at 22.6 mm similar to that of the output load antenna and the microstrip line providing inductance has a width of 0.2 mm. This antenna is designed in the presence of desired amplification power fed to the output load antenna, to include the mutual coupling effects. This mutual coupling can also be considered as the external feedback path for the transistor, modifying its properties. Therefore, it is an important parameter to include in the design for realizing the stable amplification and desired performance. The final dimensions obtained after full-wave simulations are L = 17.66 mm, x = 2.88 mm and l = 2.2 mm, which are close to the calculated values. The finally achieved source impedance for the designed input matching circuit antenna is shown in Fig. 3.17. Radiation efficiency of 67 % and radiation gain of 6.13 dBi are realized by this antenna.

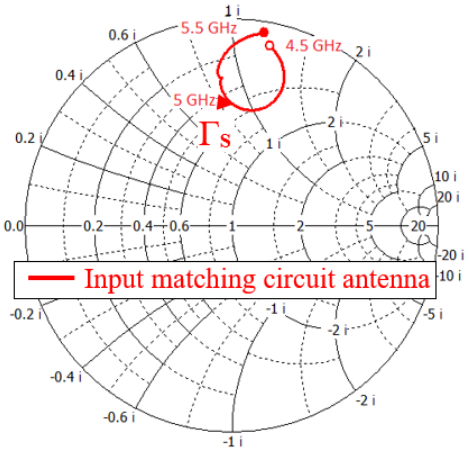


Figure 3.17: Smith chart showing impedance variation of input matching circuit antenna.

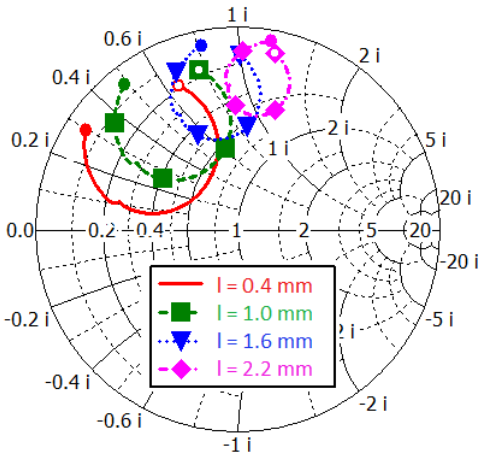


Figure 3.18: Parametric plot showing variation of input matching circuit antenna impedance by varying '*l*'.

In addition to providing a match, the series inductance line also opposes the flow of RF/mmW signal through it forcing it to radiate. However, this inductance is stemmed from the source impedance Γ_S, which actually defines the amount of power radiated by the input matching circuit antenna. The only limitation is that once Γ_S and Γ_{IN} are fixed, one cannot have control on the amount

of power radiated from the input matching circuit antenna. However, an improvement in radiated power is observed with increase in source inductance (i.e realized by increasing *l*) as observed from simulations. Alternate source impedances can also be chosen for a defined amount of power radiated through the input matching circuit antenna and improve the matching, however at the expense of amplification gain. In this design, approximately 40 % of the input power is radiated by the input matching circuit antenna for the Γ_S chosen, and the rest is fed to the gate of transistor for amplification. (note that there is a limitation for the prototyped ACA discussed in this paper as the entire design of ACA is only limited to antenna modelling because of the commercial transistor being utilized. Adding the design flexibility in some application specific transistors in addition to antenna designs results in most promising solutions.)

As reactance is directly proportional to frequency for a series inductor, the parametric plotting as shown in Fig. 3.18 shows a similar trend for varying length *l* of the inductance line. Thus, all the impedance points are shifted to nearby Γ_S for inductance line length of 2.2 mm. Hence, the matching does not get effected badly even in the case of a frequency shift caused by a high mutual coupling from the output load antenna. Therefore, the use of a series inductance also exhibits a robust design.

3.5.4 1×2 ACA prototype

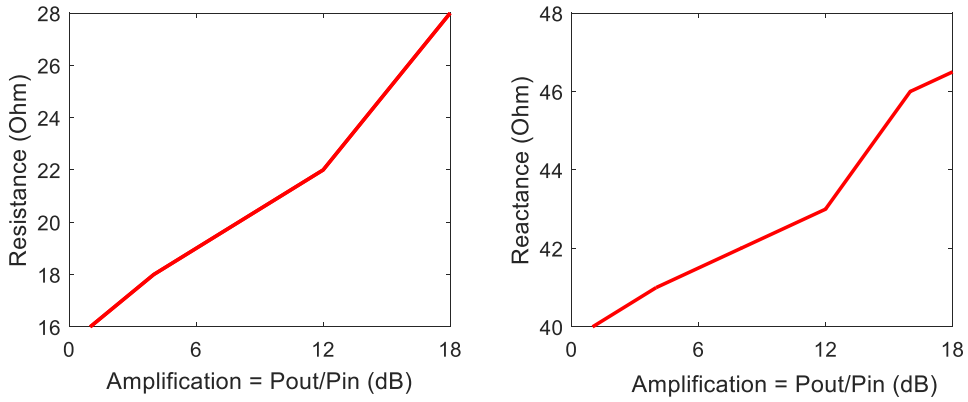


Figure 3.19: Source resistance and reactance variation with ratio of power radiated though output load antenna over that of input matching circuit antenna.

Once the output load antenna and input matching circuit antenna are designed in an array environment, the stability of integrated transistor is ensured for a possible amplification deviation in the measurements compared to simulations (The amplification term utilized here is defined as the ratio of the power radiated through the output load antenna Pout over the power radiated through the input matching circuit antenna Pin). The actual transistor properties might differ from its S-parameter model, thus resulting in mismatch of amplification and mutual coupling. Subsequently, the impedance at the antenna feed terminals is modified.

Therefore, the impedance variation of both the antennas designed is analyzed varying amplification power. Output load antenna impedance Z_L remains constant with variation in amplification power from CST-MWS simulations, which is expected from the general modelling steps discussed. However, the input matching circuit antenna impedance Z_S (= R_S + jX_S) varies with amplification. R_S and X_S vary as shown in Fig. 3.19 from simulations, with respect to amplification. All these impedance points at different amplification levels still remain in the stable region, guaranteeing the stability of ACA for possible non ideal situations.

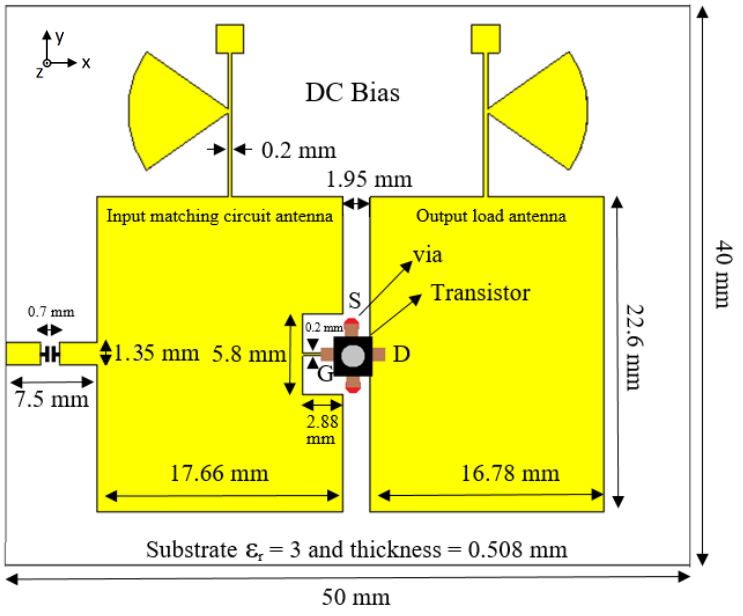
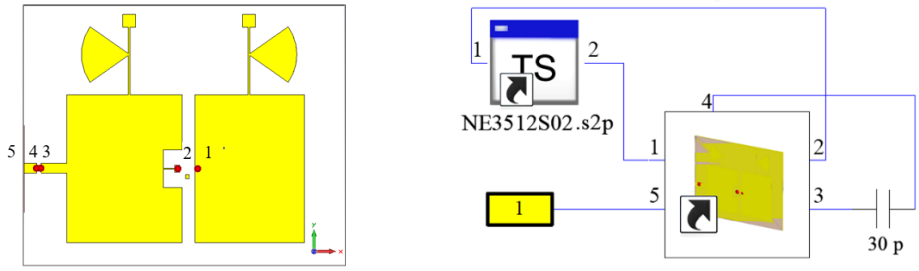


Figure 3.20: Designed ACA with all the dimensions marked.



(a) (b)

Figure 3.21: (a) Antenna designed in CST-MWS and (b) co-simulation with S-parameter model of NE3512S02.

The final ACA prototype with all the dimensions marked is presented in Fig. 3.20. DC biasing circuit is designed based on paper [106], and class-A amplifier is realized. A gap of 0.7 mm is introduced at the center of microstrip feed line to mount the dc blocking capacitor of 30 pF, to isolate the excitation. The designed antenna layout with port numbers and co-simulation with S-parameter model of the transistor through CST-MWS are shown in Fig. 3.21.

3.5.5 Equivalent circuit

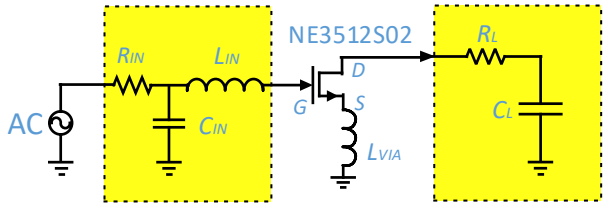
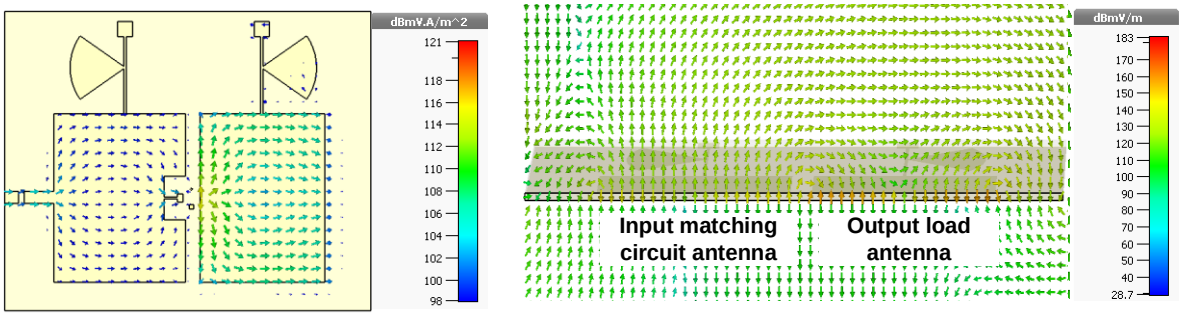


Figure 3.22: Equivalent circuit of ACA.

An equivalent circuit of the proposed ACA is presented here with circuitry realized by antennas. The load antenna behaves similar to resistor R_L and capacitor C_L in series, and radiates all the power fed to it. This load antenna is connected to the drain of the transistor with the source connected to inductor L_{via}, resulted from a via connection from the source to the ground. The input antenna equivalent circuit is already discussed in the previous analysis, and acts as series inductor L_{IN} and

parallel capacitor C_{IN} while series radiation resistance R_{IN} is added to characterize the radiation from the input antenna. The final equivalent circuit is shown in Fig. 3.22. In this approach, the antenna can effectively be formulated as a circuit.

3.6 Results and discussions

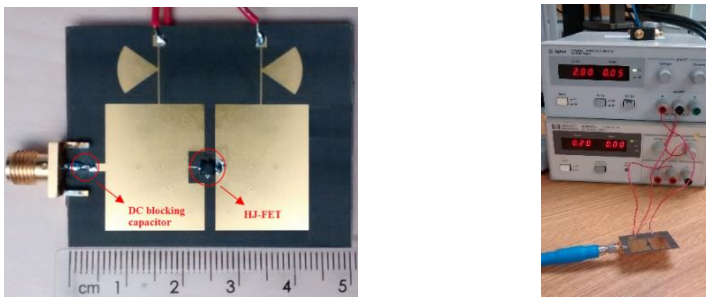


(a) (b)

Figure 3.23: Simulation results of (a) power flow in ACA and (b) E-field distribution under both the patches of ACA

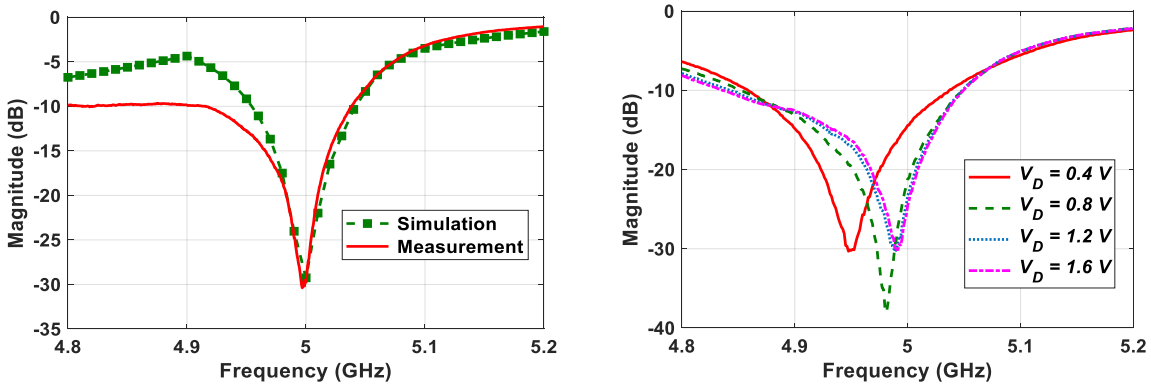
The power flow of ACA obtained through CST co-simulation is shown in Fig. 3.23(a), showing that the power on the output load antenna is amplified compared to the power on the input matching circuit antenna. E-field distribution under the antennas in ACA shown in Fig. 3.23(b), also represents a similar performance of the amplification.

3.6.1 Matching analysis



(a) (b)

Figure 3.24: (a) Fabricated prototype ACA and (b) dc bias setup.



(a) (b)

Figure 3.25: (a) Comparison of measured and simulated reflection coefficients and (b) frequency tuning measured by varying bias voltage.

Our prototyped antenna and dc bias setup for experiments are shown in Fig. 3.24(a) and Fig. 3.24(b). Gate and drain bias voltages of -0.2 V and 2 V are chosen for class-A operation of ACA. Fig. 3.25(a) shows the comparison of simulated and measured reflection coefficients which are in a very good agreement and the measurement shows a bandwidth of approximately 125 MHz. An observed difference in the measured and simulated results is due to uncertainty of the transistor model available for both simulations and experiments. A slight frequency tuning is also observed from the measurements by varying the bias as shown in Fig. 3.25(b).

3.6.2 Amplifier behavior

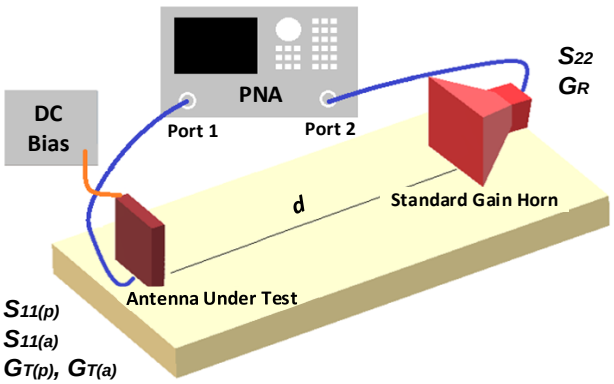


Figure 3.26: Block diagram of the experimental setup to measure amplification.

The amplifier behavior of our proposed ACA is analyzed by utilizing an experimental setup as shown in Fig. 3.26, which is similar to the proposed framework in [107]. Antenna under test or AUT (i.e rectangular patch antenna/ACA) fed to port 1 acts as a transmitting antenna (rotatable) and reference antenna (a standard gain horn antenna) acting as receiver (fixed) is fed to port 2. We can divide the procedure into two cases, one being the passive case and the other active case. Reference antenna is fixed for both the cases, while switching the AUT. The input power P_{IN} for both the cases is fixed at -20 dBm. Also, the same experimental setup is utilized to measure the linearity of ACA.

3.6.2.1 **Passive case**

AUT for this case is an isolated rectangular patch antenna designed on the same substrate and at the same frequency as ACA. The amount of power radiated by this antenna is measured by a reference antenna placed in the maximum radiation direction of AUT and in the far field. The Friis equation corresponding to it is given in (3.9)

$$\left|S_{21(p)}\right|^2 = P_{IN}\, G_{T(p)} G_R \left(1 - \left|S_{11(p)}\right|^2\right)\left(1 - |S_{22}|^2\right)\left(\frac{\lambda}{4\pi d}\right)^2 \tag{3.9}$$

where all the parameters have their original meaning and suffix *p* is added to differentiate the AUT similar parameters from the active case.

Since the comparison has to be made with ACA which is an array, let us assume the scenario where a series 1×2 array of the patch designed (equivalent to ACA without amplification) is fed with input power P_{IN}. When this input power is shared equally by the array elements, each antenna radiates only 50 % of the input power (It is an approximation of passive ACA which radiates 40 % by input matching antenna and 60 % through load antenna in ideal conditions). It is known that for uniform excitation of closely spaced in-phase array elements in a 1×2 array configuration, maximum ideal increase in radiation gain is two times compared to the isolated antenna gain in linear terms. Subsequently, the amount of power received is approximately equal to the isolated antenna transmission power as shown in (3.10). So, (3.9) still holds true for the case of 1×2 array antenna and can be utilized to compare with active case ACA array.

$$\left|S_{21(p)}\right|^2 \approx \frac{P_{IN}}{2}(2\, G_{T(p)}) G_R \left(1 - \left|S_{11(p)}\right|^2\right)\left(1 - |S_{22}|^2\right)\left(\frac{\lambda}{4\pi d}\right)^2 \tag{3.10}$$

3.6.2.2 **Active case**

AUT for this case is the designed ACA. The amount of power radiated by ACA is measured by the same reference antenna in maximum radiating direction, placed at the same distance as in passive case. Friis equation for this case is shown in (3.11), with added suffix *a* for the parameters which are different.

$$\left|S_{21(a)}\right|^2 = P_{IN} G_{T(a)} G_R \left(1 - \left|S_{11(a)}\right|^2\right)(1 - |S_{22}|^2)\left(\frac{\lambda}{4\pi d}\right)^2 \tag{3.11}$$

In the active case, the gain of ACA comprises of two parts i.e the gain of antenna and the gain of amplifier, which is shown in equation (3.12)

$$G_{T(a)} \approx G_{T(p)} G_{amplifier} \tag{3.12}$$

$$G_{amplifier} \approx \frac{\left|S_{21(a)}\right|^2}{\left|S_{21(p)}\right|^2} \frac{\left(1-\left|S_{11(p)}\right|^2\right)}{\left(1-\left|S_{11(a)}\right|^2\right)} \tag{3.13}$$

Taking the ratio of equations obtained from these two cases ((3.11)/(3.9)), and substituting (3.12), we obtain the approximate amplifier gain as in (3.13). In the scenario considered, the approximate gain of amplifier is computed as 11.5 dB, and the difference from the desired amplification gain of 13 dB (targeted for 14 dB, but 1 dB is sacrificed for choosing source impedance far from stability circle) is possibly due to the difference in the transistor model and also the fabrication tolerance. In any case, this has confirmed the amplification behavior of our proposed ACA.

Measurements are performed manually by locating the maximum gain position. It is observed that the maximum gain direction for the active case is not perpendicular because of the phase difference in signal fed to both the array elements, thus causing a beam steering. This beam steering clearly proves that both antennas radiate as an array in the proposed ACA pair, with a phase shift between them.

3.6.2.3 **Linearity**

Linearity of the amplifier inbuilt is also measured using the same experimental setup. DC biasing conditions are fixed at V_G = -0.2 V and V_D = 2 V, and input power is increased gradually to calculate the 1 dB compression point. Input power fed to ACA is varied from -30 dBm to -6 dBm and received power readings are noted along with matching. From these results, input power 1dB

compression point is observed to be around -11 dBm which is close to simulated value of -10 dBm as shown in Fig. 3.27 (-9 dBm for an ideal amplifier). In simulations, 1 dB compression point is calculated between the source and input of load antenna. However, measurement values are picked from input and received power in the maximum radiation direction. Also, input IIP3 of 7 dBm is obtained from simulations.

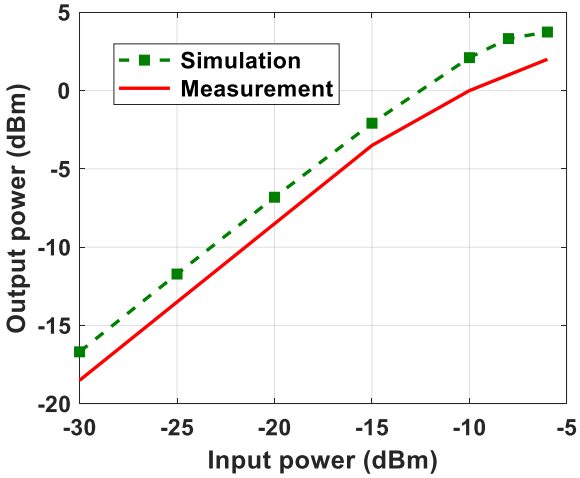


Figure 3.27: Comparison of simulated and measured 1dB compression point.

3.6.2.4 **Power Added Efficiency (PAE)**

$$PAE = \eta\left(1 - \frac{1}{G}\right) \tag{3.14}$$

Maximum drain efficiency of η=50 %, and amplification gain of G=11.5 dB, results in maximum PAE of 46.98 % (3.14), that could be realized for the class-A amplifier integrated in prototyped ACA [31]. Maximum PAE of 19 % is measured for an input power of -12 dBm and at the drain voltage of V_D=0.8 V (where ACA is matched and has a measured amplification gain of 11 dB at this dc bias point). This result is close to the simulated value of 21 % with same input parameters. It should be acknowledged that the ACA is not designed for achieving a maximum PAE. However, PAE can be improved by increasing the amplification gain, choosing the optimum load impedance and other classes of amplifiers.

3.6.3 Noise performance

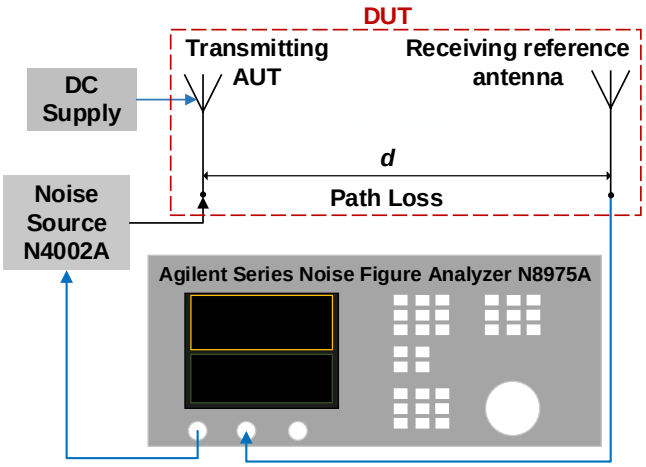


Figure 3.28: Experimental setup to measure the NF of ACA.

The prototyped ACA with the radiating input matching circuit antenna resulted in a noise figure (NF) of 2.93 dB from simulations. This NF value includes the radiation losses of input matching circuit antenna as noise, in addition to the noise of transistor. However, this radiation loss should not be reflected as noise in measurements and the significant contribution should be from transistor. Alternatively, the NF of ACA with ideal lumped components to match the ACA source impedance and 50 Ω feed is 0.92 dB, which is the NF related to only transistor. The NF simulations performed in Keysight-ADS platform does not include the noise from output load antenna, which is modelled as the second port.

The conventional NF measurement using series noise figure analyzer N8975A and noise source N4002A requires the system to be calibrated in the first instance. This resets both the gain and NF to 0 dB. Subsequently, the two port device under test (DUT) is placed in between the noise source and NF analyzer to measure the NF and gain of DUT. We can also describe this as the NF measurement for a black box existing in-between the noise source and NF analyzer.

The NF measurement of ACA cannot be performed in the conventional approach as the prototype is one port transmitting device. The experimental setup therefore utilized in this work is as shown in Fig. 3.28, and NF is measured with reference to a passive antenna. The noise source is connected

to the NF analyzer on one end and to the transmitting AUT on the other end. The reference antenna placed in the far field receives and feeds the NF analyzer, which measures and displays the NF and gain at the frequency of interest (5 GHz). The measured values are for the DUT, which comprises both the antennas and free space. Here, calibration is performed till the edge of cables where the antennas are connected, and hence the noise contribution from these cables in the results can be ignored.

In the first step, AUT and reference antenna are chosen to be identical passive rectangular patch radiators, and we refer them as passive case. The resultant noise factor F_p and gain G_p obtained are for the cascade system with components of transmitting (Tx) antenna, receiving (Rx) antenna and the environment (envir) between the antennas. This environment includes the path loss between antennas and external noise sources, if any. The effective noise factor of the cascaded system can therefore be expressed as (3.15) and effective gain as (3.16), while the noise factor and gain of individual components remain unknown.

$$F_p = F_{Tx\ Ant} + \frac{(F_{envir} - 1)}{G_{Tx\ Ant}} + \frac{(F_{Rx\ Ant} - 1)}{G_{Tx\ Ant}\ G_{envir}} \tag{3.15}$$

$$G_p = G_{Tx\ Ant}\, G_{envir}\, G_{Rx\ Ant} \tag{3.16}$$

The next step is to replace the AUT with ACA and measure the noise factor of DUT, in the same environment and with the same receiving antenna as the passive case. This result however, constitutes an additional noise because of the amplification transistor involved. Similar to the passive case, noise factor F_a (3.17) and effective gain G_a (3.18) for the active case are measured. This F_a can be decomposed as the measurement of two components in cascade connection: (1) input matching circuit antenna (input Ant) and transistor (tr) as in F_{ACA} (3.19) and (2) output load antenna, environment and receiving antenna, as in F_P (3.15). After straightforward simplification, we could realize F_a in terms of F_{ACA} and F_P as in (3.21) using the gain ratio (3.20), for this cascade system. Subsequently, the noise factor/noise figure of ACA is computed from (3.22) as 1.6/2.04 dB, where all the parameters are measured. Since, the measurements fluctuated slightly with time, we took an average of 20 readings to analyze all these results. Additional noise in active case compared to the passive case can also be calculated from the measured parameters after simple math from basic NF definitions, which comes out to be 0.48 dB.

$$F_a = F_{input\ Ant} + \frac{(F_{tr}-1)}{G_{input\ Ant}} + \frac{(F_{Tx\ Ant}-1)}{G_{input\ Ant}\,G_{tr}} + \frac{(F_{envir}-1)}{G_{input\ Ant}\,G_{tr}\,G_{Tx\ Ant}} + \frac{(F_{Rx\ Ant}-1)}{G_{input\ Ant}\,G_{tr}\,G_{Tx\ Ant}\,G_{envir}} \quad (3.17)$$

$$G_a = G_{input\ Ant}\,G_{tr}\,G_{Tx\ Ant}\,G_{envir}\,G_{Rx\ Ant} \quad (3.18)$$

$$F_{ACA} = F_{input\ Ant} + \frac{(F_{tr}-1)}{G_{input\ Ant}} \quad (3.19)$$

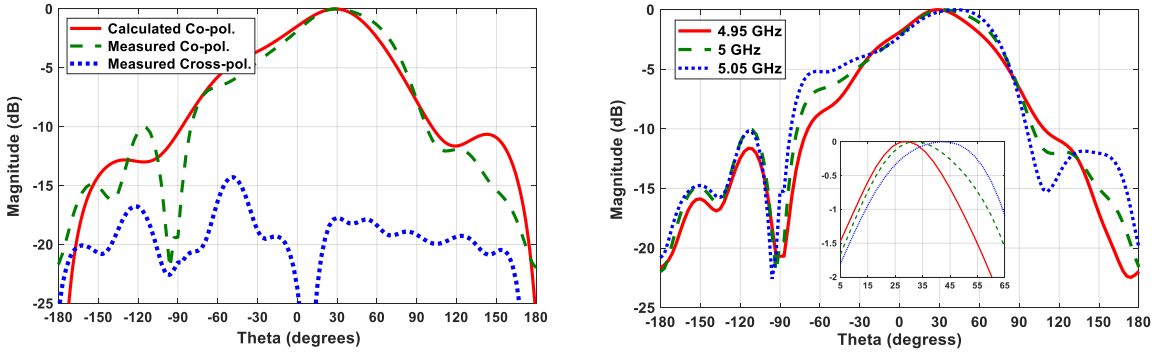
$$G_{input\ Ant}\,G_{tr} = \frac{G_a}{G_p} \quad (3.20)$$

$$F_a = F_{ACA} + \frac{(F_p-1)}{(G_a/G_p)} \quad (3.21)$$

$$F_{ACA} = F_a - \frac{(F_p-1)}{(G_a/G_p)} \quad (3.22)$$

Measured NF value is less than the simulated value of 2.93 dB for ACA and also greater than the NF with lumped element input matching circuit. The transistor characteristics are deviated from its S-parameter model utilized in simulations, as already observed in the gain measurements. This variation could be the reason for an increase in NF compared to NF from lumped matching circuit case. Therefore, the radiating input matching circuit antenna is not deteriorating the noise performance of overall system. Transistor is the main component injecting noise and the noise performance of proposed ACA is not degraded compared to the conventional configurations.

3.6.4 Radiation performance



(a) (b)

Figure 3.29: Radiation pattern in E-plane of (a) measured co and cross polarization along with calculated co-polarization result and (b) co-polarization at different frequencies.

The radiation pattern is measured using our SATIMO Starlab setup. A beam steering is observed as expected and at $+30^0$. The maximum cross pol in the E-plane is nearly 14 dB lower than the co-pol and the side lobe is at the back of antenna, which is almost 10 dB less than the main lobe as shown in Fig. 3.29(a).

The radiation pattern of demonstrated ACA is also calculated mathematically using an active element pattern method to for verification. This particular method is effective to calculate the radiation pattern of the entire array in a more practical scenario [108], that is in the presence of all couplings. In this analysis, signal is fed into one array element with all the others loaded with corresponding impedances, and the radiation pattern $g^n(\theta,\emptyset)$ is calculated. In a similar procedure, radiation pattern of all the other elements is computed. This radiation pattern of each array element is multiplied with its excitation $I_n\, e^{j\Psi_n}$ and combined to yield the total radiation pattern $F(\theta, \phi)$ as shown in (3.23) [40].

$$F(\theta,\emptyset) = \sum_{n=1}^{N} g^n\,(\theta,\emptyset)\; I_n\; e^{j\Psi_n} \tag{3.23}$$

$$\Psi_n = \beta d \sin(\theta) + \varphi \tag{3.24}$$

To calculate ACA radiation pattern $F(\theta,\phi)$, we consider the two antennas of ACA as an array N = 2 with center to center spacing d = 19.17 mm and propagation constant β = 0.17 rad/mm. Amplification factor $I_2 \approx 3.5I_1$ is obtained from the amplifier analysis. Radiation patterns of each antenna and signal phase values at the input of each antenna in the ACA structure are generated from simulations. It is observed that the load antenna signal is delayed by a phase of φ = -120^0 compared to the signal at the feeding edge of input matching antenna, as predicted. This phase difference is also close to the calculated value from the transmission line analysis.

The final calculated active element radiation pattern $F(\theta, \phi)$ and measured co-polarization radiation pattern are compared in Fig. 3.29(a), which closely agree with each other. In this unification, we can exploit the biasing parameter to impact the transistor properties. This enables the tuning of phase and amplitude fed to the output load antenna and correspondingly realize the beam steering. Subsequently, beam shift to $+26^0$ is observed by changing the gate bias to -0.3 V. Similarly, a slight beam steering is also verified by varying the drain bias. This minor beam steering observed in both the cases is due to the commercial transistor being utilized, whose characteristics barely alter with gate and drain bias variations. However, we could realize a significant beam steering if the

transistor would have been designed to vary its characteristics rapidly with minor variation in bias voltage. The co-polarization E-field radiation patterns are also plotted for 4.95 GHz, 5 GHz and 5.05 GHz in Fig. 3.29(b), suggesting that the increase in frequency steers the beam to a larger angle.

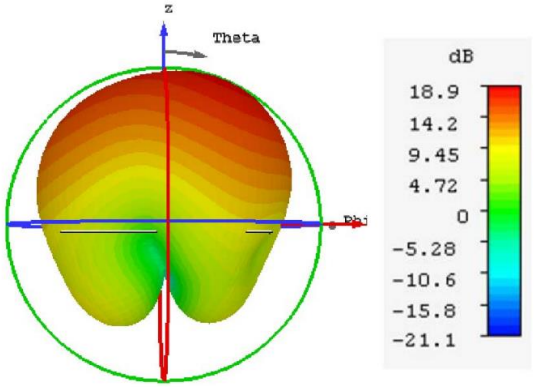


Figure 3.30: 3-D radiation pattern of ACA.

Table 3.2: Comparison of proposed ACA with the state of art.

	[23]	**[24]**	**[25]**	**THIS WORK**
Frequency (GHz)	2.37	2.45	5.8	**5**
Input matching network	Yes	Yes	Yes	**No**
Output matching network	Yes	Yes	Yes	**No**
Amplifier class	B	-	AB	**A**
Amplification Gain (dB)	17	12	16	**11.5**
Size in λ_0 (L x W)	1.2 X 0.18	0.54 X 0.4	-	**0.83 X 0. 66**
Array size	1	1	1	**1×2**
Maximum radiation	Broadside	Broadside	Broadside	**+30^0 w.r.t broadside**

The 3D radiation pattern result from CST-MWS co-simulation is shown in Fig. 3.30. It demonstrates the beam-steered radiation performance as discussed and has a maximum realized gain (which includes mismatch losses and amplification gain) of 18.9 dBi from co-simulation. The realized radiation gain of passive 1×2 array is simulated to be 6 dBi. Therefore, an amplification

of 12.9 dB is observed, which is close to the measured value of 11.5 dB. Radiation efficiency of the antennas in ACA without amplification is 72%, similar to the passive counterpart. Low radiation efficiency of the antennas is mainly attributed to the thin dielectric substrate used in this demonstration.

The comparison of our proposed ACA with the state of art designs in terms of architecture and basic parameters is presented in Table 3.2. Proposed ACA definitely removes all the matching circuitry nearby radiator, and operates as both an amplifier and antenna. It is also an array realizing the beam steering functionalities in a confined space, compared to the state of art designs with single antenna and fixed beam.

3.7 1 × 4 ACA

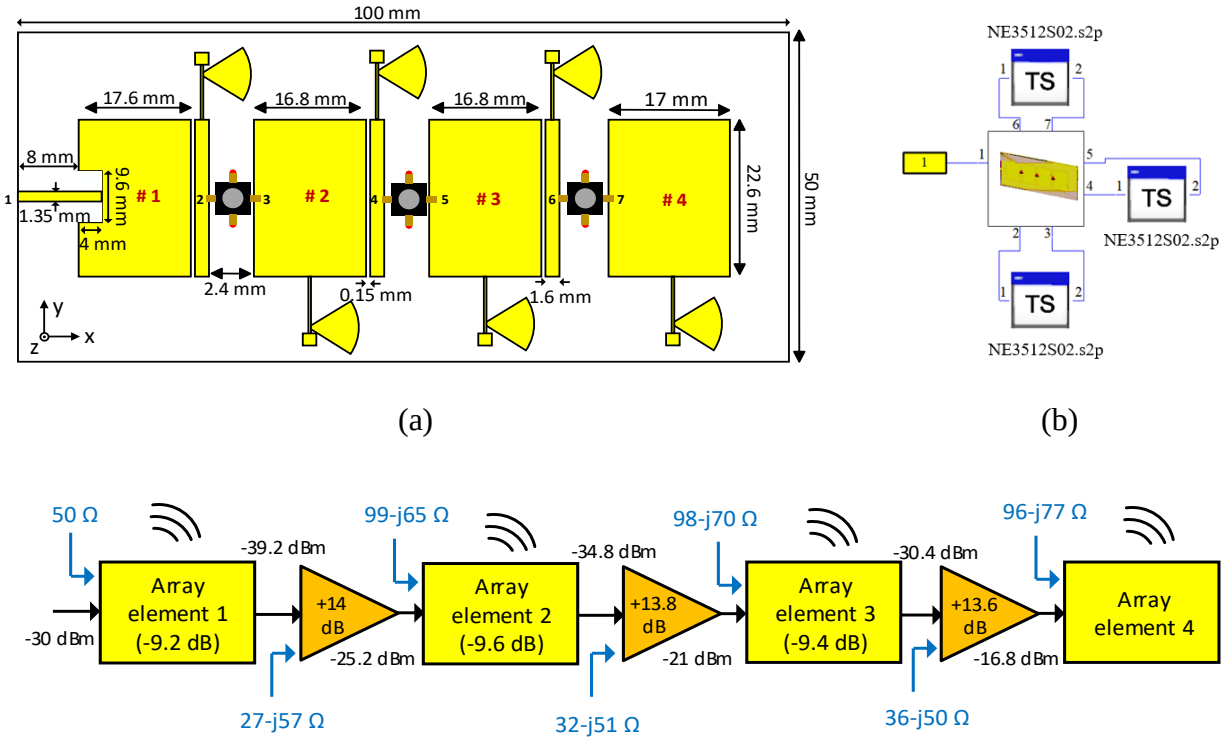


Figure 3.31: (a) 1×4 ACA model with all the dimensions marked (b) co-simulation of S-parameter model of antenna with transistor S-parameter model and (c) block diagram showing the amplification, impedances and radiation across 1×4 ACA.

1×4 ACA is designed utilizing NE3512S02-transistors and rectangular patch antennas on substrate of relative permittivity ε_r = 3 and thickness of 0.508 mm. All the drain terminals of transistors are loaded with impedances on 14 dB amplification gain circle, for an equal amplification of 14 dB through each transistor.

The procedure described in the general modelling steps is followed for the development of ACA starting from array element 4. Array element 4 acts as the output load antenna and is designed first in an isolated environment. Array element 3 and 2 act as inter stage matching networks and the array element 1 acts as the input matching network to source, in addition to radiation through all of them. Array elements 3 to 1 are designed in the presence of other elements to include the mutual coupling effects. Slots along the width are etched in all the array patch elements except array element 4, to isolate the gate and drain dc bias. Slot width along with source impedance helps in controlling the amount of power radiated through each array element and the power coupled to the other port, in contrast to the inductance line used in 1×2 ACA prototype. The final design of this 1×4 ACA with all the dimensions marked is shown in Fig. 3.31(a).

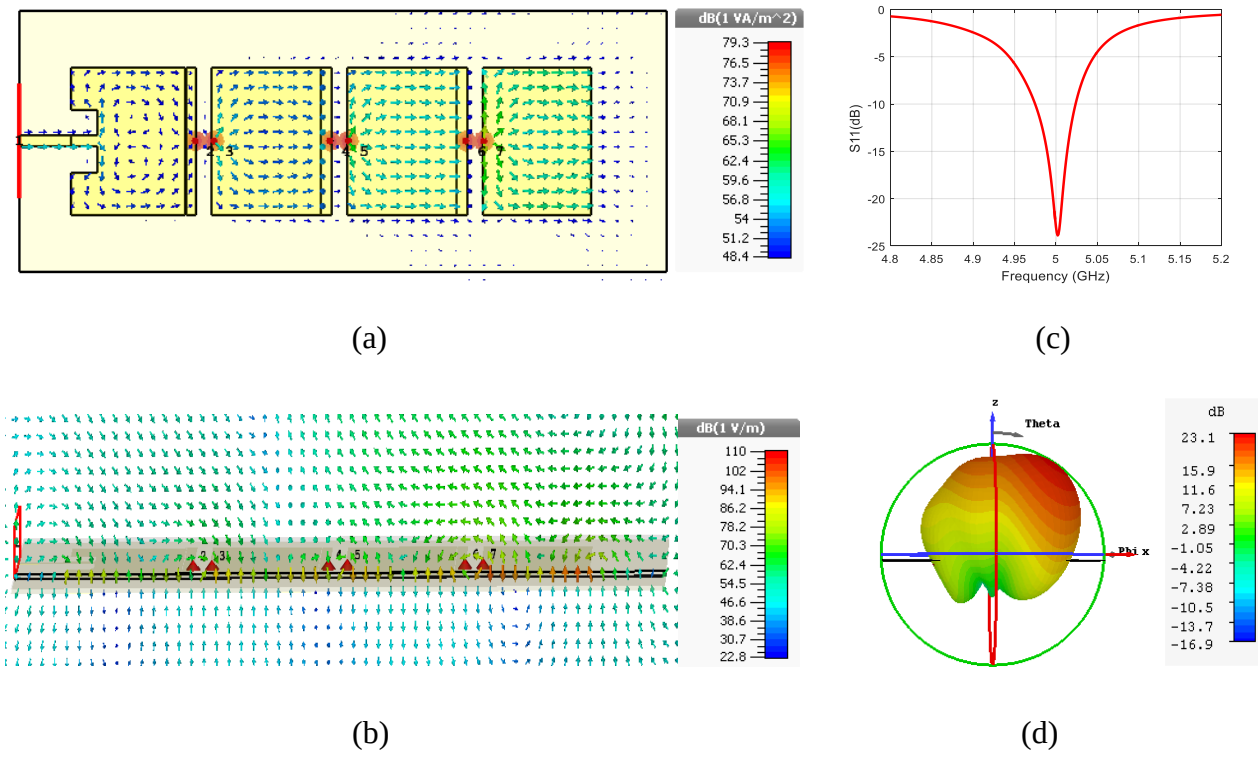


Figure 3.32: 1×4 ACA (a) power distribution (b) E- Field distribution (c) matching and (d) 3-D radiation pattern.

The input matching and radiation performance of 1×4 ACA is analyzed through co-simulation of array antenna S-parameter model and transistor S-parameter model in CST-schematic (Fig. 3.31(b)). Whereas Keysight-ADS is utilized for analyzing the power and impedance at each node throughout the ACA and the results are shown in Fig. 3.31(c) (amplifying transistors are depicted as amplifier blocks for an easy understanding). Amplification gain and antenna impedances alter slightly from the desired value because of the difference in array environment seen by each array element.

The power and E-field at each array element is shown in Fig. 3.32(a) and 3.32(b). It can be observed that there is an amplification of signal along the series array through transistors and the signal is radiated through all the array elements. The designed 1×4 ACA is matched as shown in Fig. 3.32(c). The radiation pattern of this 1×4 ACA is also beam steered to 34^0, similar to 1×2 ACA because of the phase shift induced by transistors and array elements (Fig 3.32(d)). Realized gain of 23.1 dBi from simulations shows the improvement in gain by approximately 14 dB compared to the passive counterpart, thus demonstrating the amplification of signal and radiation through the designed 1×4 ACA. ACA array elements have radiation efficiency of 73%, similar to the passive antenna, excluding the amplifier gain. In a similar approach, a larger array can be designed with the general modelling steps discussed earlier.

3.8 Conclusion

This paper has proposed, studied and demonstrated the unification and integration of a circuit and antenna (UNICA), in particular, amplifier circuit antenna (ACA) modules. This unified body of circuit-antenna may present a paradigm shift in the development of high-density all-in-one integrated front-ends for future RF, mmW and THz wireless systems. The realization of circuit performances by the antenna, the mutual coupling analysis, the placement of active device in different operation modes and the modelling procedure for the 1×N ACA array are presented and discussed. The proposed procedure is utilized to demonstrate the design of the 1×2 array in the dominant mode through the use of rectangular patches and commercial HJ-FET. A set of handful equivalent circuits are presented for the ACA topology. The proposed ACA structure is fabricated and good results are obtained through simulations and measurements. The modelled and prototyped ACA has a very good matching condition at the design frequency, radiating the amplified signal

and exhibiting a slight beam steering and frequency tuning through dc bias variations. The noise performance is not degraded and the amplifier parameters remain preserved in the integration. In addition, the design and analysis of 1×4 ACA is discussed to show the potentiality of unification for large-scaled higher order arrays. The proposed configuration is particularly attractive for mmW and THz IC systems with the following advantages, namely minimum interconnection losses, constructive radiation conditions, cost effective, light weight, functional re-configurability etc. Eventually, it is also possible to achieve phased array ICs without the use of actual phase shifters through this scheme. This unification promises even better solutions when there is a flexibility in design of both antennas and circuits (active devices). We believe that future front-ends might be replaced by this UNICA approach as the boundary between circuit and antenna can be completely removed one day.

CHAPTER 4 ARTICLE 2: DEEP INTEGRATION AND TOPOLOGICAL COHABITATION OF ACTIVE CIRCUITS AND ANTENNAS FOR POWER AMPLIFICATION AND RADIATION IN STANDARD CMOS

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In this paper, a densely-integrated and unified paralleled amplifier and antenna architecture is proposed, and demonstrated for next-generation millimeter-wave (mmW) and terahertz (THz) front-end modules. It makes use of topologically paralleled transistors cohabitated within a compact rectangular patch antenna as a unified cell. This design simultaneously amplifies and radiates power without resorting to any power divider, input and output matching networks, or power combiner whatsoever, therefore greatly reducing front-end loss, size and complexity. Then, the unified unit cell is self-consistently distributed to form a unified planar array with active elements between array elements as power feeders. In this demonstration, the input power is sequentially amplified, radiated through each array element, and spatially added up, resulting in a low on-board circuit losses and efficient radiation. In this paper, we investigate and present challenges and early results of implementing this unification concept of active circuitry and antenna at mmW frequencies. Using a standard 65-nm CMOS process, a set of chips were designed, fabricated, and tested under different amplifier biasing conditions at 146 GHz for experimental demonstration. The realized low-loss, matched and compact unified prototypes have demonstrated an amplified radiation, with power enhancement of 3.4 dB through single element and 6 dB through 2 x 2 layout compared to their respective passive counterparts. Moreover, frequency tuning is observed varying drain bias, and self-matching is improved with increasing gate bias. Therefore, the feasibility of a unique feature in the architectural implementation of low-loss, compact, and densely-integrated and topologically cohabitated mmW and THz front-end modules is confirmed.

4.1 Introduction

Driven by the ever-increasing needs of our rapidly-evolving information society, such as higher data rate, smarter connectivity, more accurate location and identification, etc., wireless technology has entered into the millimeter-wave (mmW) era, and gradually expanding into the terahertz (THz) territory. This has recently attracted much attention within research and development communities from both academia and industry, where mmW bands are emerging as the future spots of wireless communication and sensing technology. This advancement is exemplified in numerous and highly-anticipated applications, such as, but not limited to imaging [109], short distance high data rate communication [89], identification [110], automotive radar [111], as well as the upcoming and highly-publicized 5G technology portfolios [112] and beyond. However, as opposed to the overcrowded low frequency spectrum (below 6 GHz), new approaches tackling underlying technical challenges at mmW and THz bands need to emerge. Creative minds need to develop novel and innovative architectural solutions. One challenge that researchers are facing is the development of mmW and THz front-end modules in a fully integrated manner with high efficiency. In this connection, large free-space path loss, line-of-sight propagation, parasitic radiation from circuits in the proximity of antennas, and high losses associated with signal feeders and line interconnects are all critical issues for future wireless communication and sensing technology developments.

There have been reported works on front-end modules where instead of designing antenna and front-end circuitry as two independent components, their co-design methodology and side-by-side integration are demonstrated as a potential solution to these issues [46, 47, 61, 63, 113-115]. Unlike its conventional counterpart, this integration, often referred to as active integrated antenna (AIA), has the advantages of compactness, low loss, and so forth [46, 47]. However, the whole system accommodates the antenna as only a radiating structure or a part of passive circuitry in addition to radiation [61, 63, 113-115]. Furthermore, the proximity of still existent front-end circuitry close to the radiating structure (antenna) increases mutual coupling between passives, and the inherent losses degrades the overall performance of system. In this perspective, unification and integration of circuits and antennas (UNICA) has been recently proposed for simultaneous front-end circuitry and radiation functions by eliminating the passive networks including matching networks, inter-

connections and so on [116]. Henceforth, the corresponding losses and its effects on radiation performance are removed. Eventually, this approach presents an adequate candidate for low-loss, fully integrated architectural solutions for all the front-end circuitry functions. In works [116-118], amplifier/oscillator functions along with radiation have been demonstrated by replacing the input and output matching networks of active circuit by antennas, resulting in a 1x2 linear array with commercial transistor integrated between them. However, these PCB prototype models operate around or lower than 10 GHz.

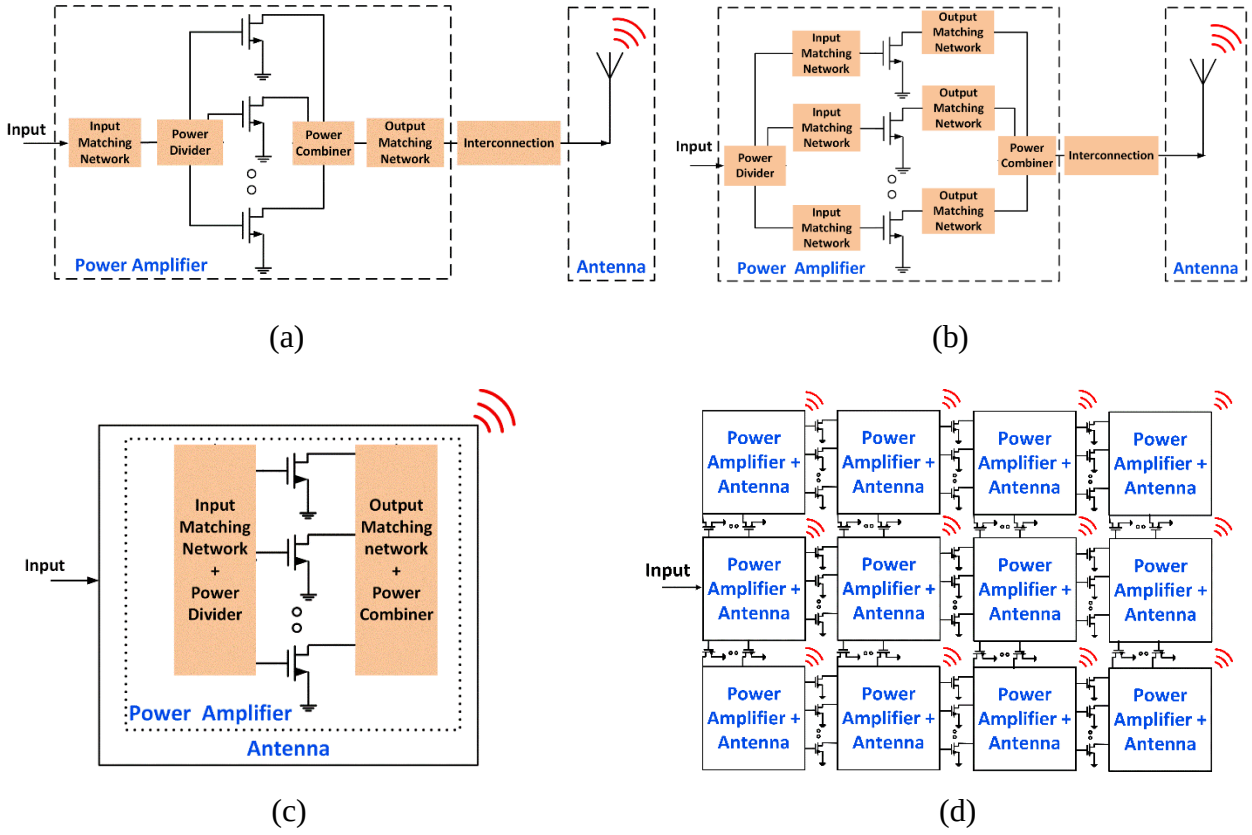


Figure 4.1: Conventional paralleled amplifier configuration with power divider/combiner and (a) common input/output matching network interconnected with antenna, (b) matching networks in each paralleled path interconnected with antenna, (c) proposed unified unit cell of paralleled power amplifier integrated within antenna, and (d) proposed planar array configuration with multiple unified unit cells and amplifying transistors between array elements.

Besides, over mmW and THz frequency bands, an effective wavelength is in the order of millimeters, and hence close to a typical semiconductor (CMOS) die size. Therefore, mmW and THz along with CMOS enable a true unification of active devices within the antenna to realize a complete front-end module (circuitry and antenna) in a single unified design space. Although different circuitry functions can be realized along with radiation through this unification, further discussion of this work is limited to the unification of multiple active devices within antenna for simultaneous amplification and radiation.

Due to a low breakdown voltage of transistors in submicron CMOS technologies, a paralleled amplification configuration is preferred to both relax transistor circuit complexity and handle high power scenarios. The input power is divided into paralleled transistors, and each of them handles lower power, therefore enhancing the amplifier's linearity, which is directly proportional to the number of transistors. The prior-art paralleled amplifier circuit configurations for integration with the antenna are mostly limited to;

1. an input matching network common to all parallel paths, followed by a power divider to partition the power into N equal parts for amplification, a power combiner to regroup the amplified signals, which are then delivered through matching network to a load [119],[120], [as illustrated in Fig. 4.1(a)]. However, this configuration suffers from losses, load sharing issues, and network dependency on all the transistors [37];
2. a power divider, N transistors paths in parallel with input and output matching networks in each path, and a power combiner [121-124] [as demonstrated in Fig. 4.1(b)]. However, synchronizing all the paths and the losses associated with increased circuitry are the major drawbacks of this configuration especially at mmW and THz bands.

Nevertheless, paralleled power amplifier and antenna integration with reduced (or removed) output power combiners realized through multiport antenna excitation [53] or multiple antennas [124] [125] have been studied. However, the still existent input circuitry, part of output circuitry, and interconnects induce critical losses and occupies a significant area making them expensive.

Henceforth, a deep integration and topological cohabitation of on-chip antenna and circuit structures need to be developed to efficiently use the allocated chip space, therefore ensuring a high-density integration of active circuits within and around the large and lossy antenna. This forms

highly-unified compact modules and improves the overall efficiency, reliability and repeatability of front-ends.

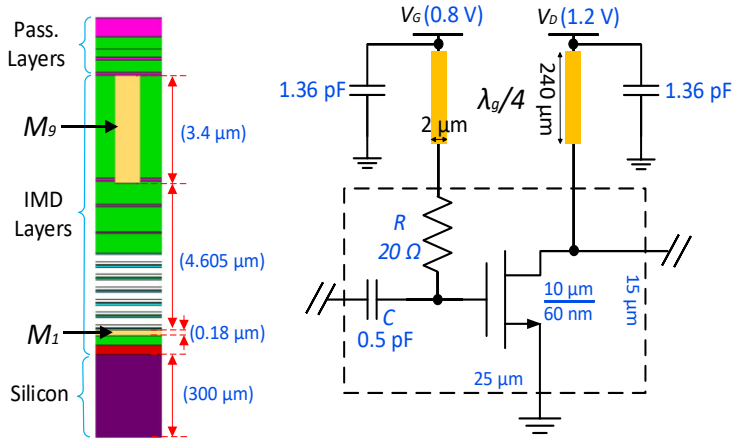
In this paper, a D-band unified and deeply integrated circuit antenna front-end, operating at around 146 GHz is successfully demonstrated on a commercially low-cost 65-nm bulk CMOS process. As illustrated in Fig. 4.1(c), the paralleled amplifier is successfully implemented by integrating active elements within the antenna with no additional passive circuits, namely input and output matching networks or a power combiner/divider. The structure simultaneously acts as a circuit (amplifying) and an antenna (radiating) through unification and cohabitation. In fact, a careful placement of the active device within the antenna is defined by the impedance, which is further related to the field distribution of the antenna. In this case, the circuit and antenna are concertedly defined and fabricated over the same space.

As conceptually illustrated in Fig. 4.1(d), the demonstrated unified cell can be distributed self-consistently to implement a planar array. As a matter of fact, we have analyzed in this paper a 1×2 amplifying-antenna array through simulations, implemented and experimentally demonstrated a 2×2 amplifying-antenna array in which paralleled amplifying transistors are used as feeding connectors of the array elements. The input power is sequentially amplified, radiated through each array element, and added up spatially to enhance the radiation power and increase the integration density through the use of entire space, leading to a cost-effective, compact-size, and energy-efficient design platform for space-power combining. The array configuration demonstrates both the antenna gain and amplification gain resulting in a much higher radiated power.

In this work, the paralleled amplifier circuit and patch antenna are individually discussed first in the context of a CMOS process, followed by their unification into a single entity, and its extension to a larger unified array. To this end, the evolution of paralleled amplifier circuit starting from a CMOS technology model is presented with a detailed discussion on biasing circuitry, stability, gain, and paralleled configuration followed by a detailed discussion on passive antenna configuration. Subsequently, the circuit-antenna unification is demonstrated with all the necessary analyses and result comparisons with the conventional counterparts. Furthermore, linear and planar unifying arrays are also presented. Finally, experimental setup details, measured results of the fabricated prototypes and analysis for amplification gain extraction are discussed, followed by concluding remarks.

4.2 Paralleled amplifier

This section describes the evolution of a paralleled amplifier circuit at design frequency of 146 GHz starting from the CMOS technology model. The supporting simulations are performed in Keysight ADS platform.

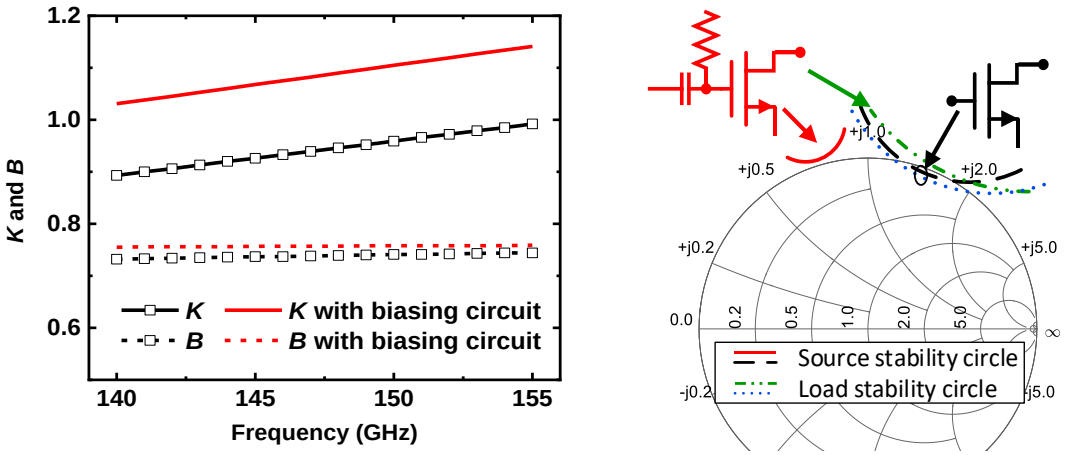


(a) (b)

Figure 4.2: (a) Demonstration of TSMC 65-nm CMOS process (Pass.: passivation, IMD: inter-metal dielectric) and (b) biasing circuit along with transistor.

The adopted TSMC 65-nm CMOS technology layout along with metal layers M_9 (patch) and M_1 (ground) utilized for patch antenna design are illustrated in the Fig. 4.2(a). As illustrated in Fig. 4.2(b), nMOS transistor is designed with a gate length of 60 nm, 1 µm unit finger width and 10 fingers, and biased at V_G = 0.8 V and V_D = 1.2 V for maximum transistor's transconductance (*gm*). The transistor sizing, as well as the number of fingers are optimized to provide maximum power gain in the context of paralleled amplifiers (power combining) at the design frequency. The circuitry to bias the nMOS transistor designed is shown in Fig. 4.2(b). Here, resistor *R* assists in removing the odd modes and potential oscillations, while the series capacitor *C* isolates the gate and drain bias for the transistor integrated within the antenna. The input and output impedances are 15.6 – j46.27 Ω and 64.98 – j111.2 Ω, respectively.

4.2.1 Stability



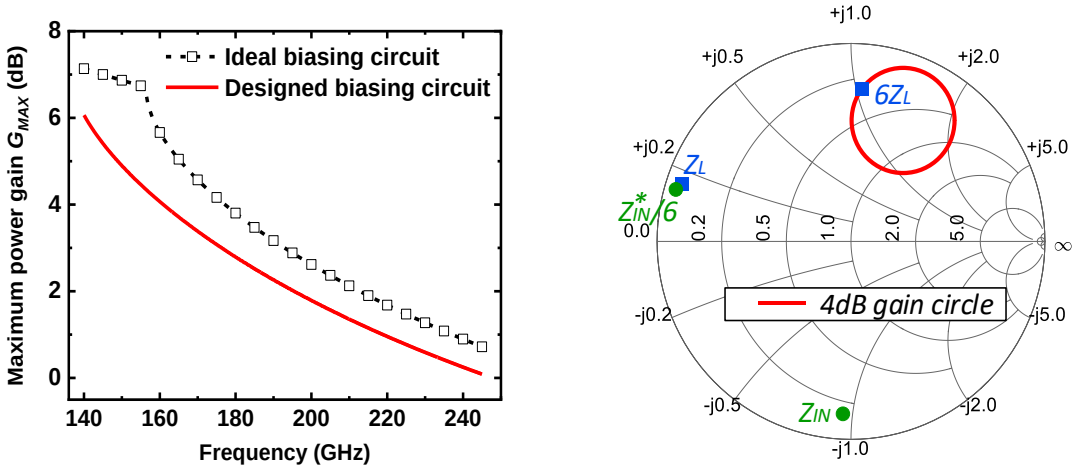
(a) (b)

Figure 4.3: Comparison of modelled transistor performance with ideal and designed biasing network for (a) stability factor *K* and stability measure *B* and (b) stability circles at the design frequency of 146 GHz.

The variation of stability factor *K* and stability measure *B* across the frequency range of interest (140 GHz to 155 GHz) are shown in Fig. 4.3(a). The transistor alone with ideal biasing network is potentially unstable as $K < 1$. Henceforth, source and load stability circles are drawn at 146 GHz to identify the stable region in the Smith chart Fig. 4.3(b). Maximum resistance on the source stability circle is thereby calculated as 2 Ω.

The on-chip biasing circuit capacitor integrated at the gate terminal of transistor has an inherent series resistance of 2.5 Ω. This resistance stabilizes the transistor (activated through designed biasing circuit) throughout the operating range, without any additional stabilizing circuit. The resultant $K > 1$ and $B > 0$ (Fig. 4.3(a)) confirms the unconditional stability of the transistor. The stable region includes entire Smith chart at 146 GHz, as $|S_{11}| = 0.84 < 0$ and $|S_{22}| = 0.72 < 0$ at the center. Source and load stability circles are further presented in Fig. 4.3(b) to highlight the difference from ideal biasing network case.

4.2.2 Gain circle



(a) (b)

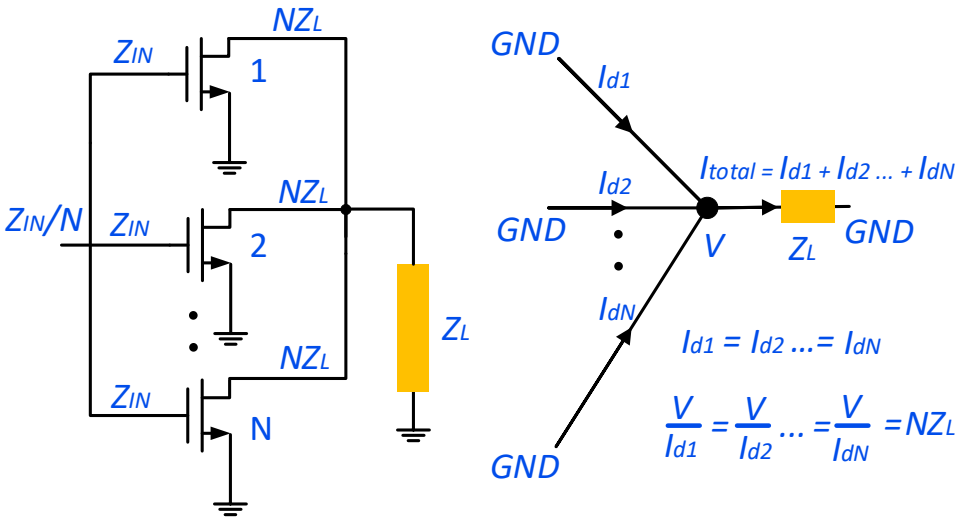
Figure 4.4: (a) Maximum gain comparison of transistor with ideal and designed biasing network and (b) Smith chart representing the 4 dB gain circle at 146 GHz and highlighting the impedances in paralleled amplifier design.

The maximum gain performance of designed transistor is studied with ideal and designed biasing network [as shown in Fig. 4.4(a)]. The lower gain observed for transistor activated through designed biasing network is due to the input power loss from the built-in resistance of biasing circuitry capacitance at gate terminal. Maximum power gain realizable by one stage transistor with designed biasing circuit is G_{MAX} = 5.3 dB at 146 GHz. However, power gain G = 4 dB is chosen as an example for demonstration in this work, and the corresponding gain circle drawn in the Smith chart is shown in Fig. 4.4(b).

4.2.3 Paralleled configuration

Let us consider an equal power division of the input signal into N identical transistors and an equal power combining at the output with a common load impedance Z_L, as shown in Fig. 4.5(a). Since all the parallel paths are simultaneously excited with equal signals, we can evaluate the effective impedances along each path based on the even mode decomposition theory [38]. For example, this decomposition results in a load impedance Z_L multiplied by N times as seen by the drain terminal

of each transistor [shown in Fig. 4.5(a)]. This behavior can also be explained from the fundamental circuit theory. The corresponding AC equivalent circuit and analysis of this paralleled amplifier load section, starting from the drain terminal towards the load is shown in Fig. 4.5(b). Through a similar approach, the inverse behavior at gate terminal results in a reduction of input impedance by a factor of N seen before the power divider $Z_{FEED}= Z_{IN}/N$ as shown in Fig 4.5(a); where Z_{IN} is the impedance looking into gate terminal of each loaded transistor.



(a) (b)

Figure 4.5: (a) Paralleled configuration-demonstrating impedances at various points when loaded with common load impedance Z_L and (b) AC equivalent circuit of paralleled amplifier load section.

4.2.4 Paralleled amplifier

An amplification gain of 4 dB realized through N = 6 transistors in parallel is designed as an example. The drain terminal of each transistor is loaded by $6Z_L$=12+j52 Ω, lying on the desired gain circle G = 4 dB, as shown in Fig. 4.4(b). From this, we can calculate the common load impedance necessary as Z_L= 2+j8.67 Ω. Eventually, the input impedance at gate terminal of each transistor is calculated as Z_{IN} = 6-j48 Ω (with drain terminal loaded). An inverse behavior at the gate terminal results in the impedance at feed as $Z_{IN}/6$ = 1-j8 Ω. The two ways of realizing paralleled amplifier design are by utilizing;

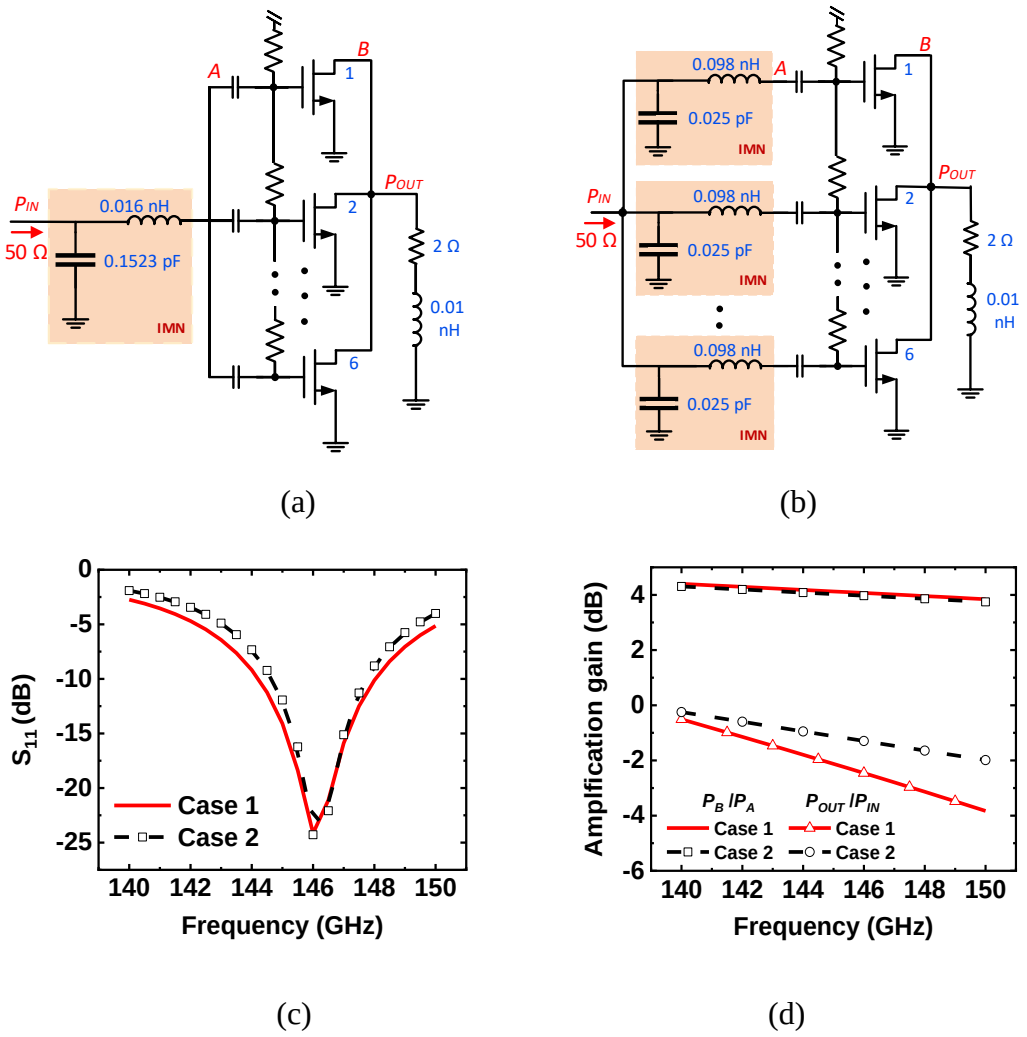
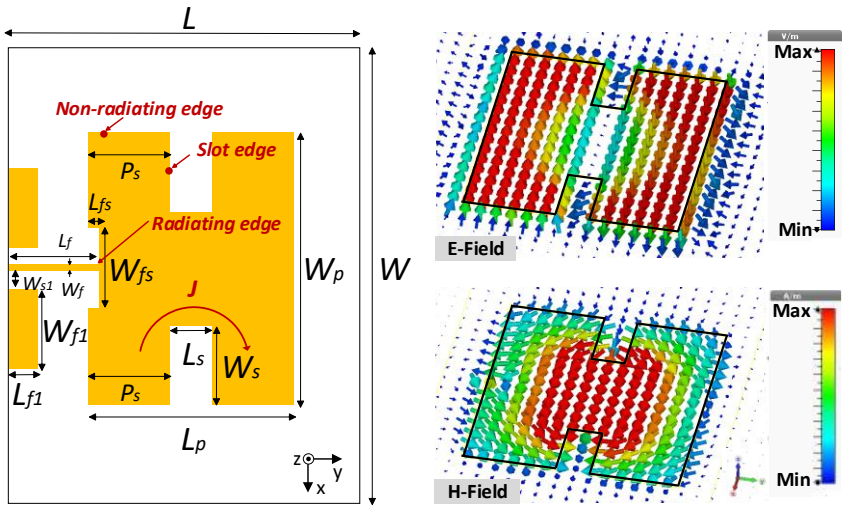


Figure 4.6: Paralleled amplifier design with a (a) single input matching network common to all the transistors(case 1), (b) individual input matching networks at each transistor (case 2). (IMN: Input-Matching Network) and; simulation results of case 1 and case 2 (c) input matching and (d) amplification gain. (Note: ideal power dividers and combiners are utilized in the design of paralleled amplifiers configurations discussed here).

1. Case 1: a single input matching circuit before the power divider to transform impedance $Z_{IN}^*/6$ to $Z_G = 50\ \Omega$ feed impedance [as shown in Fig. 4.6(a)] and
2. Case 2: separate input matching network in each parallel path to transform Z_{IN}^* to 300 Ω ($Z_G = 50\ \Omega$ feed impedance × 6 parallel paths), so that the impedance before power divider is equal to feed impedance Z_G [as shown in Fig. 4.6(b)].

For demonstration, paralleled amplifiers discussed in case 1 and case 2 are designed. Here, the input matching networks are designed with the passive circuitry elements in the same process. From simulations, the realized circuitry are matched as shown in Fig. 4.6(c). However, the loss of around 5 dB from matching circuitry resulted in the effective power delivered from source to load as $P_{OUT}/P_{IN} < 0$ dB, although there exists an amplification gain of P_B/P_A=4 dB across the biased transistor as per design [as shown in Fig. 4.6(d)]. This demonstrates the immense loss of passive elements involved, and envisions the necessity in eliminating all of these lossy passive components in the active circuits designed in this process.

4.3 Compact rectangular patch antenna



(a) (b)

Figure 4.7: Demonstration of (a) CRPA : L= 500 µm, W= 750 µm, Lp= 364 µm, Wp= 400 µm, Ls=55 µm, Ws=100 µm, Ps = 154.5 µm, L_f= 130 µm, L_{fs} = 30 µm, W_{fs}= 40 µm, W_f= 6 µm, L_{f1}=40 µm, W_{f1}=100 µm, W_{s1}= 20 µm and (b) its field distribution.

Out of many ways to realize compact rectangular patch antenna (CRPA) reported in [126], this work utilizes the technique of etching rectangular slots on the non-radiating edges of CRPA at the center along length [127], as shown in Fig. 4.7(a). These slots force the current J to traverse across the bends, thereby increasing the length of current path resulting in the reduction of size. Here,

CRPA is excited through microstrip inset feed line, which is interconnected to a grounded coplanar waveguide (GCPW) for standard ground signal ground (GSG) probe measurements; all at 50 Ω reference impedance. The ground pads on M_9 are shorted to the M_1 layer through vias. The corresponding field distribution is illustrated in Fig. 4.7(b), where the fields vary along the CRPA length, and also across its width because of the slots etched at center.

4.3.1 Impedance behaviour

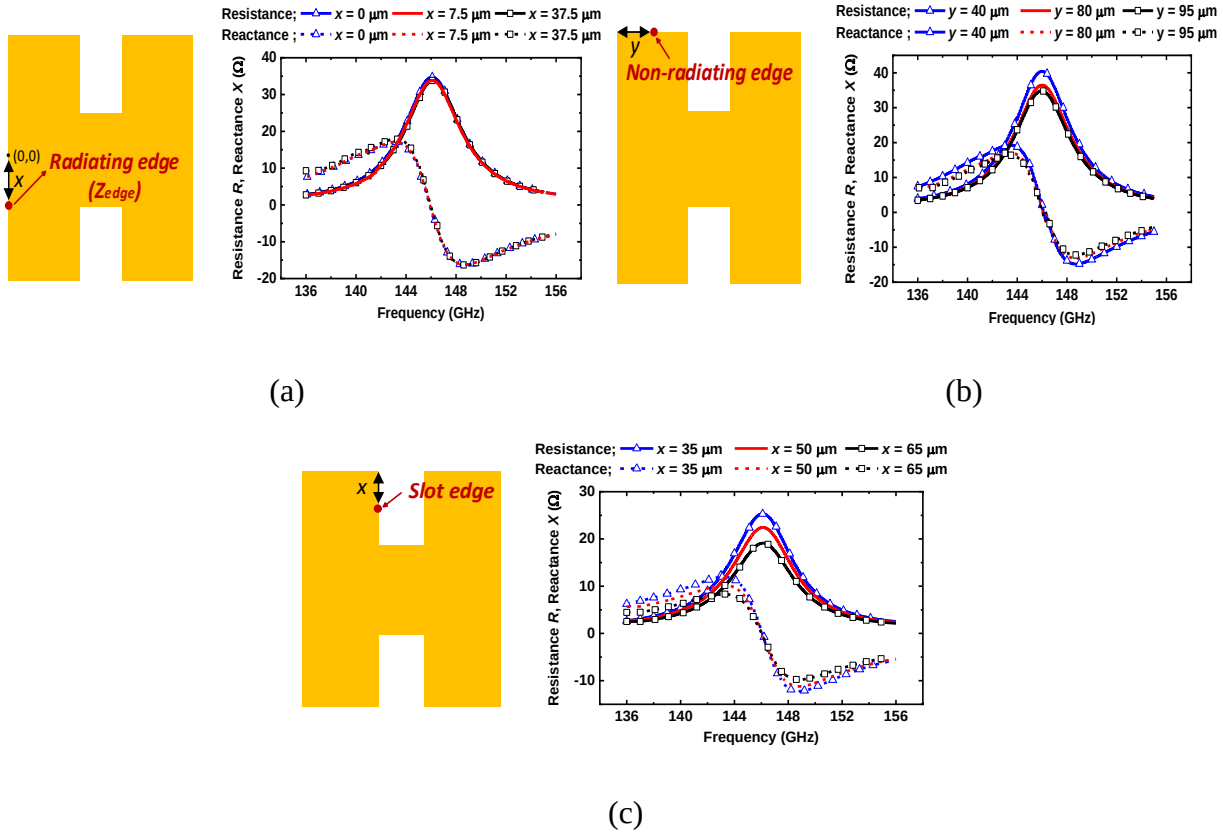


Figure 4.8: Impedance analysis of CRPA excited on (a) radiating edge (b) non-radiating edge and (c) slot edge; which are the intended locations for transistors integration.

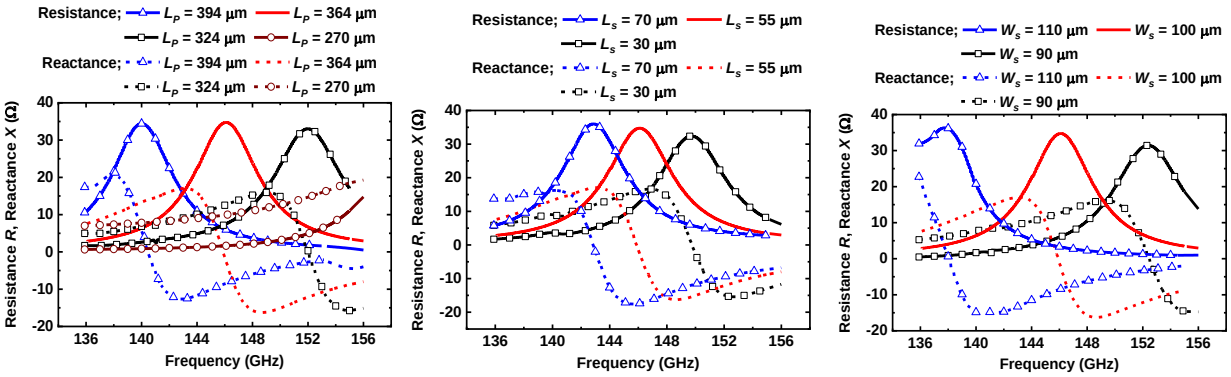
Initially, the impedance at various locations of CRPA which are intended for transistors integration has been analyzed, with fixed geometry. Subsequently, the impedance response with geometry variation has been studied and discussed.

4.3.1.1 **At various locations with fixed geometry**

The impedance response of CRPA excited on radiating edge, non-radiating edge and slot edge are analyzed independently and the corresponding results are shown in Fig. 4.8(a), 4.8(b) and 4.8(c) respectively. These impedance responses comply with the field distribution observed in Fig. 4.7(b), and conclude that the;

1. impedance remains approximately constant across the width of CRPA for radiating edge feed.
2. impedance keeps decreasing with the variation of non-radiating edge feed position towards the center of CRPA along length and
3. impedance on the slot edge decreases with feed position approaching close to the center of CRPA width.

4.3.1.2 **Varying geometry**



(a) (b) (c)

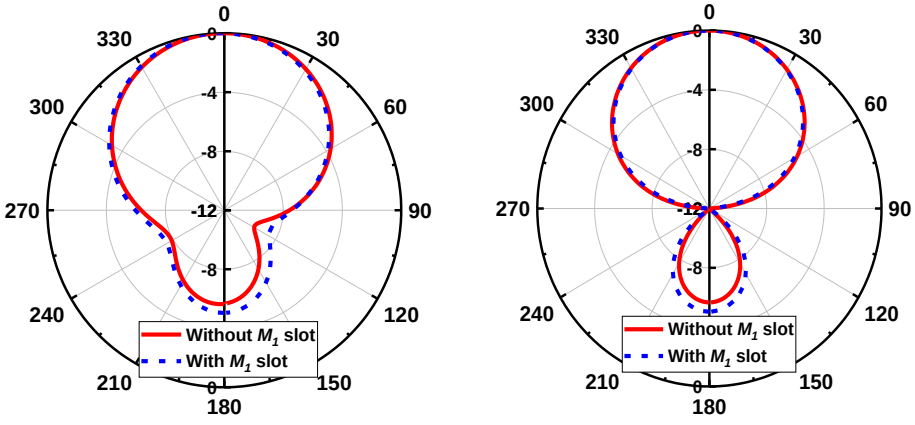
Figure 4.9: Input impedance variation of CRPA design in Fig. 4.7 varying only; (a) CRPA length *Lp* (b) slot length L_S and (c) slot width *Ws*.

For radiating edge feed of CRPA, Z_{edge} becomes purely resistive R_{edge} at the design frequency of 146 GHz when CRPA length is resonant at L_p=364 µm, as shown in Fig 4.9(a). Decreasing the CRPA length below the resonant dimension will result in an additional inductive term in impedance $Z_{edge} = R_{edge}+jX_{edge}$ at the design frequency (for example, L_p=324 µm and L_p=270 µm). On the other hand, increasing the CRPA length over resonant dimension will induce a capacitance term resulting

in $Z_{edge} = R_{edge}$-jX_{edge} at the design frequency (for example, L_p=394 µm). Similarly, the slot-length L_S and/or slot-width W_S can be reduced to realize the inductive reactance, while they can be increased to realize capacitive reactance at the design frequency as demonstrated in Fig. 4.9(b) and Fig. 4.9(c) respectively, in addition to resistance.

Furthermore, the impedance response has been analyzed at all of the locations intended for transistors integration with these geometry variations. It is thereby observed that the impedance response at all of these locations behave similarly to the discussed radiating edge feed results, although the absolute values are different. For example, the decrease in CRPA length has resulted in an inductive reactance in addition to resistance on the radiating edge $Z_{edge} = R_{edge}$+jX_{edge}. Similarly, the impedance at all other locations inside CRPA will also have an inductive reactance and resistance with decrease in CRPA length, however at a different magnitude. Subsequently, the radiating edge analysis holds valid at all the impedance locations with other geometrical variations. Henceforth, we can realize any kind of reactance (in addition to resistance) at the design frequency and at all locations by varying either the CRPA length or slot dimensions, with a slight compromise in radiation efficiency. However, the width of CRPA is kept constant throughout the analysis as its variation demonstrated a relatively smaller impact on the impedance response.

4.3.2 Radiation performance with slots in ground plane



(a) (b)

Figure 4.10: Comparison of CRPA normalized radiation performance without and with slot in M_1 along (a) E-plane and (b) H-plane.

Slots have to be etched at appropriate locations inside the ground plane (M_1) of CRPA for direct integration of patch with the transistors designed in the silicon layer of same chip. These ground plane slots are modelled to be smaller than the patch layer M_9 slots, to reduce the negative effects of M_1 slot on field distribution. Fortunately, these slots are located at the non-radiating region of CRPA and are expected to have minimum effect on overall radiation performance, as the CRPA radiates from the edges along length. From simulations, it is observed that these slots have minimum disturbance on the overall radiation pattern as shown in Fig. 4.10. However, there is a slight decrease in the front to back ratio by 0.4 dB because of the slots.

Eventually, this fundamental understanding of the impedances at appropriate locations inside CRPA and impedance tuning with geometry variation assists in the design, while the good radiation performance observed even with slots in ground plane ensures the efficient integration of transistors within antenna.

4.4 Unification of transistor and CRPA

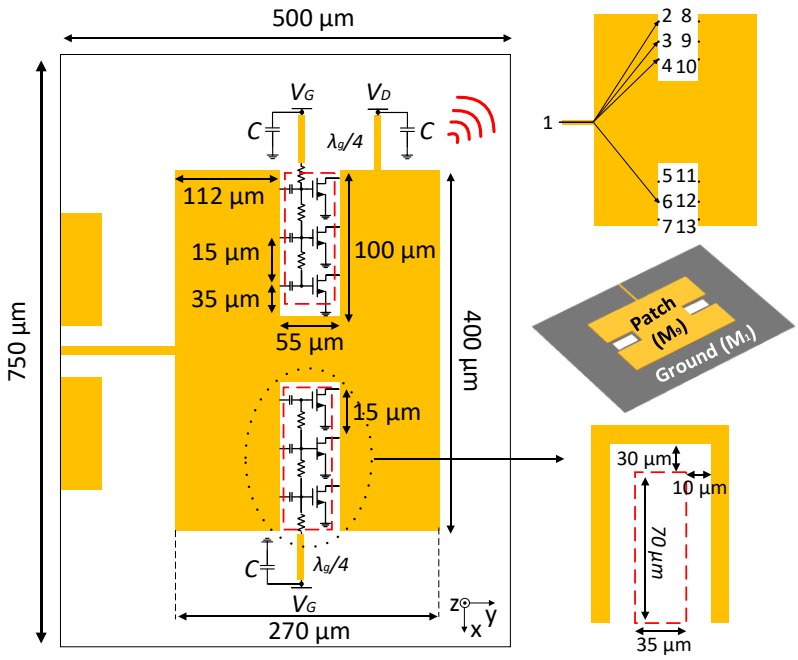


Figure 4.11: Demonstration of ACRPA (where '- - - -' represents the slots in the ground plane) and visualization of all the ports utilized for simulation. (Note: The transistors integrated within ACRPA are enlarged and not to the scale, for a better visualization).

The CRPA is diligently modelled to operate as the passive counterpart of paralleled amplifier, in addition to its inherent property of radiation. With its dimensions marked in Fig. 4.11 (feed dimensions are the same as in a CRPA), this unified prototype referred to as 'active compact rectangular patch antenna' (ACRPA) has the advantages of

1. removing the passive components of paralleled amplifier circuitry, thereby reducing the corresponding losses and its effects on the radiation performance;
2. eliminating the amplifier and antenna interconnections;
3. being a highly integrated miniaturized design and;
4. a cost-effective solution.

4.4.1 General modelling steps

The guiding steps for realizing such a unification are described as follows;

1. To begin with, the transistor is designed for maximum gain, and the stability of it is analyzed through the stability factor K and stability measure B. If the transistor is potentially unstable, the load and source stability circles are drawn in the Smith chart to identify the stable region.
2. The maximum power gain G_{MAX} is calculated for transistor, and the desired operating power gain G circle for $G < G_{MAX}$ is drawn in the Smith chart.
3. The antenna is then designed to realize an impedance Z_L (within it), such that for N transistors in parallel (directly integrated with Z_L) the effective drain terminal impedance NZ_L (seen by each transistor) must lie on the desired gain G circle, and as such in the stable region.
4. Next, the input impedance Z_{IN} corresponding to Γ_{IN} is calculated at the gate terminal of each transistor with all the N transistors drain terminal connected to the antenna.
5. The appropriate conjugate impedance point $Z_S = Z_{IN}^*/N$ on the same antenna is identified for concurrently matching the gate terminal of N integrated transistors and transforming Z_S to Z_G=50 Ω feed impedance (necessary for measurements but not mandatory).

6. An approach to improve the isolation between drain and gate terminals is to etch slots between these terminals integrated within the antenna. In addition, slots on the antenna can help to reduce its size, while the slots in the ground plane enable via connection to the co-designed transistors in the silicon layer.
7. Furthermore, the slot dimensions and its location, along with antenna dimensions are co-optimized with transistors integrated within it to accommodate all the parasitic effects including feedback path, and loading. In addition, transistor stability has to be reanalyzed to ensure stable operation in the presence of feedback path.
8. The drain terminal of each transistor is directly biased through the quarter wavelength short-circuited microstrip line connected to the radiator. However, the gate terminal of transistor(s) is (are) biased through separate quarter wavelength short circuited microstrip line biasing networks. In addition, DC blocking capacitor are utilized to isolate the gate and drain bias.

4.4.2 Design example

The transistor design and corresponding analysis have been discussed in Section. 4.2. Subsequently, load impedance Z_L=2+j8.67 Ω and N=6 transistors in parallel; same as the paralleled amplifier design are selected for demonstration. These 6 transistors in parallel are divided into two subgroups of 3 transistors and are integrated within each slot of the CRPA. Since, the CRPA slot dimensions could accommodate three transistors as required; they are kept unchanged throughout the analysis.

4.4.2.1 **Design procedure**

Table 4.1: Impedance at Z_9 varying length of CRPA and slot fixed at center of CRPA.

***CRPA length L_p* (µm)**	***260***	***270***	***280***
Resistance R (Ω)	1.8	1.9	2.1
Reactance X (Ω)	10.2	11	12.4

The primary parameter supporting this unification is the ability to simultaneously realize impedances Z_L and Z_{IN}*/6 on either side of the CRPA slot edges. Fortunately, these two impedances have inductive reactance as shown in the Smith chart Fig. 4.4(b). Henceforth, they can be simultaneous realized by decreasing the CRPA length as understood from Section. 4.3.1. Subsequently, the CRPA length L_P is decreased (with slot fixed at the center) to be around 270 μm, where the impedances on slot edge are approximately equal to the desired impedance for transistor integration. A parametric analysis of impedance on slot edge [at port 9 as shown in Fig. 4.11] modifying the CRPA length around L_P = 270 μm is shown in Table 4.1 for reference. The table format is chosen to accurately provide the result values as they vary slightly as per design. It should be noted that unless specified, the impedance terms described here are considered with all the other ports open, similar to the *Z*-parameter calculation.

Table 4.2: Impedance at Z_9 varying slot position on CRPA while its length is fixed at L_P = 270 μm.

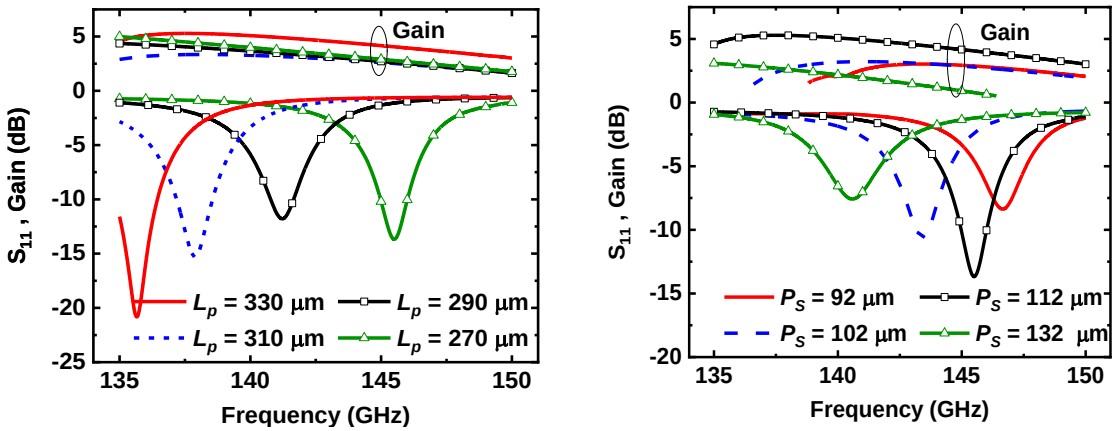
***Impedance Z*(P_s)**	**Z_9(P_s = 112 μm)**	**Z_9(P_s = 122 μm)**	**Z_9(P_s = 132 μm)**
Resistance R (Ω)	2	2.2	2.5
Reactance X (Ω)	13	13.5	15

Table 4.3: CRPA slot edge impedances at L_p = 270 μm and P_s = 112 μm.

***Impedance Z*(Ω)**	**Resistance *R*(Ω)**	**Reactance *X*(Ω)**
$Z_8 \approx Z_{13}$	2.17	14.7
$Z_9 \approx Z_{12}$	2	13
$Z_{10} \approx Z_{11}$	1.81	12.3
$Z_2 \approx Z_7$	1.39	10.1
$Z_3 \approx Z_6$	1.23	9.3
$Z_4 \approx Z_5$	1.14	8.7

Following it, impedance at the edge of slot [at port 9 as shown in Fig. 4.11] varying slot position P_S along the length of CRPA is displayed in Table 4.2. It varies from a maximum near the patch

edge (P_S = 132 μm) to a minimum as it approaches the center (P_S = 112 μm), which follows the typical impedance behavior of the CRPA. To realize a relatively lower impedance required at the gate terminals than drain terminal for conjugate matching, the slot is positioned slightly offset from the center at P_S = 112 μm. This will result in a gate side slot edge closer to the center, leading to a lower impedance on this edge relative to the higher impedance at the drain slot edge. The gate side slot edge has ports 2-7, and the drain side slot edge has ports 8-13, as demonstrated in Fig. 4.11. Subsequently, the impedance at all these feed locations is shown in Table 4.3. It is thereby observed that at the chosen CRPA length, corresponding impedance variation at the slot edge is also limited.

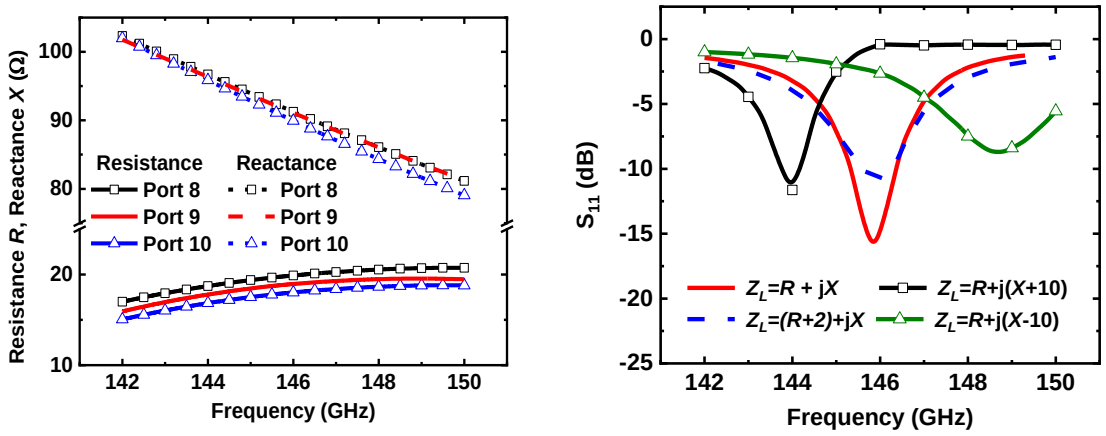


(a) (b)

Figure 4.12: Matching and amplification gain variation of ACRPA with (a) length L_P (at P_S = 112 μm) and (b) slot position P_S (at fixed L_P = 270 μm).

However, the integration of transistors at these ports in CRPA will induce parasitic and feedback effects, which alters the port impedances and thereby ACRPA operation. In this regard, ACRPA is further co-optimized for better matching and desired amplification gain with transistors integrated within it. A parametric analysis of the ACRPA response is evaluated by tuning the ACRPA length with slot fixed at P_S =112 μm, and the corresponding matching and amplification gain response are shown in Fig. 4.12(a). This demonstrates that the increase in ACRPA length will decrease the matching frequency, while the amplification gain across transistor increases at lower frequency as defined by the corresponding gain circles and loading impedances. In addition, the effect of slot position on the overall matching and amplification gain of ACRPA (with length fixed at L_p = 270

μm) has also been analyzed and illustrated in Fig. 4.12(b) for reference. It can be analyzed that the ACRPA is well matched and realizes maximum amplification gain when the slot position is slightly offset from the center at P_S =112 μm. This further envisions that the matching freqeuncy and amplification gain can be precisely controlled through both ACRPA length and slot position tuning.



(a) (b)

Figure 4.13: (a) Impedance at the drain terminal 8,9,10 in ACRPA and (b) variation of ACRPA impedance matching with load impedance tuning, where R= 3 Ω and X = 15 Ω.

After a final co-optimization for the ACRPA operation at design frequency of 146 GHz, the impedance seen by the drain terminal of each transistor is approximately equal to $NZ_L \approx 6(3+j15)$ Ω calculated from the corresponding terminal voltage over current ratio (with all the transistors integrated as in the real scenario). Subsequently, the input impedance at all the gate terminals calculated with this load impedance is modified to be around $Z_{IN} = 6(1.6-j11)$ Ω, and the optimized source impedance of antenna thereby realized is around Z_s = 1.5+j13 Ω. The load and source impedances calculated at all the corresponding ports remain close as they are fed with same bias and approximately equal amount of signal. For example, the impedance seen by the drain terminals of three transistors integrated in one slot is shown in Fig. 4.13(a) for reference. Moreover, the impact of varying load impedance connected to all the drain terminals on optimized ACRPA matching is presented in Fig. 4.13(b). Increase in resistance has demonstrated a mismatch of ACRPA, while change in reactance tunes the resonant frequency in addition to mismatch. In the cases studied, the amplification gain across transistors has varied by less than 10%.

4.4.2.2 **Signal difference**

Table 4.4: Amplitude and phase difference between ports.

Ports	***21***	***31***	***41***
Amplitude diff. (dB)	-8.2	-8.1	-8.2
Phase diff. (degree)	-149	-147	-146

Signal at all the gate ports is evaluated relative to the input feed signal, with all the transistors integrated. In fact, the resultant amplitude variation of 0.1 dB and maximum phase deviation of 30 are in an acceptable range, and the absolute values of signals realized are presented in Table 4.4. In addition, the symmetrical field distribution on the other slot comes up with a similar result. It is therefore imperative from the co-simulation that the transistors operate under both equal biasing and signal to efficiently combine and radiate the amplified signals.

4.4.2.3 **Isolation**

Table 4.5: Isolation between ports.

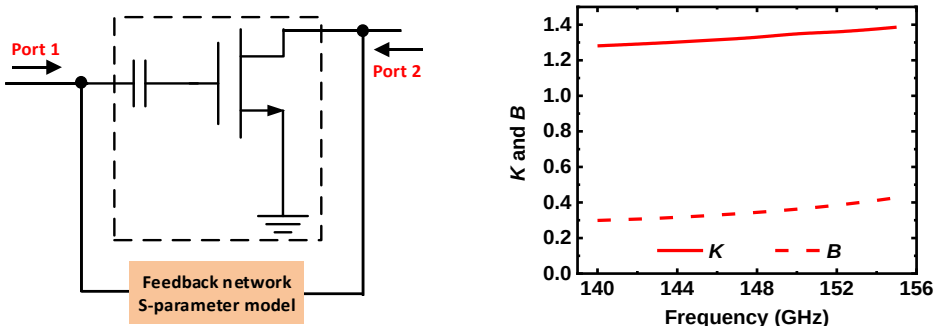
Port	**2 / 4**	**8 / 9 / 10**	**11 / 12 / 13**	**5 / 6 / 7**
3	12 dB	10 dB	17 dB	9 dB

From the actual impedances terminating all the ports known after optimization, the S-parameters are calculated with the modified reference impedance at each port, which is equal to the terminating impedance of corresponding port. This is calculated initially by transforming the $[S]_{50\,\Omega}$ to [Z], and then to $[S]_{Zl\,\Omega}$ for modified impedance. The resultant isolation calculated across different ports (with actual impedances as in the real scenario) with respect to port 3 are presented in Table 4.5. The isolation between ports on the same side of slot is more than 12 dB, and from drain to gate terminal of transistor is approximately 10 dB.

In the operation of ACRPA with approximately equal signal at the transistor integration ports as analyzed in Table 4.4, significant coupling is mainly between the gate and drain terminal integration ports of the slot edges. Since the amplified power is present at the drain terminal, the

influence of coupling from these ports on the gate terminal ports is larger, compared to the opposite way. In this regard, it is recommended to initiate the design and co-optimize starting from the drain terminal. Eventually, this design strategy assists in a faster realization of the desired matching and amplification gain at the design frequency even with a lower isolation between the ports.

4.4.2.4 **Stability**



(a) (b)

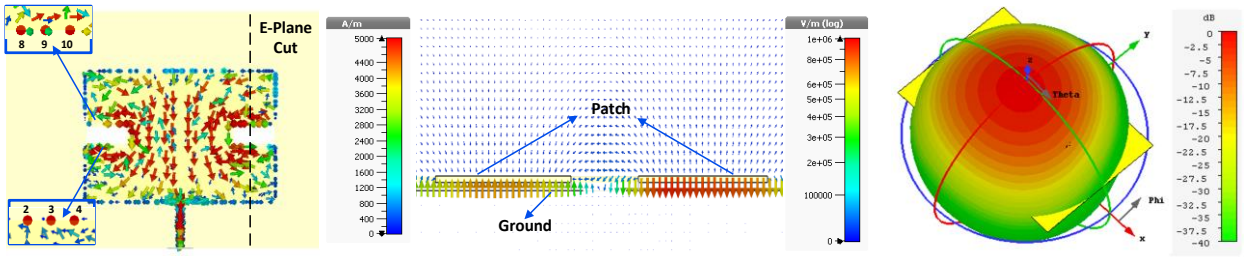
Figure 4.14: (a) Transistor with feedback network and (b) corresponding *K* and *B*.

The stability of transistors is re-analyzed by including the feedback network calculated from modified S-parameters. Although the stability parameters *K* and *B* values are varied as a result of the feedback network, they are still stable. As an example, the lowest isolation gate-to-drain terminal ports (4-to-10 or 5-to-11 *S*-parameters with modified impedance) are chosen, and the effect of this feedback path on the overall stability is studied from the circuit illustrated in Fig. 4.14(a). The corresponding results in Fig. 4.14(b) confirm that the transistor is stable even with the feedback network.

4.4.2.5 **Co-simulation**

Antenna is modelled in the CST-MWS platform with discrete ports at the locations where transistor's gate and drain terminals have to be integrated and cohabited. The *S*-parameter model thereby obtained is exported to Keysight ADS platform for amplification and matching analysis of the unified structure with transistors. On the other hand, radiation performance analysis and field/current distribution calculation of the unified module are performed through AC co-simulation in the CST-MWS schematic with transistor *S*-parameter model.

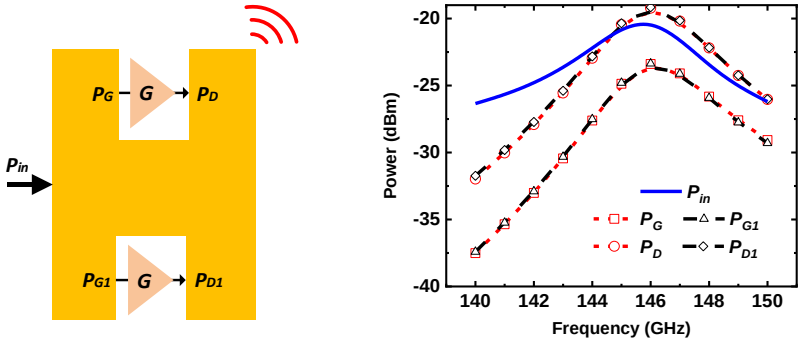
4.4.2.6 **Results**



(a) (b) (c)

Figure 4.15: Co-simulated results of ACRPA at 146 GHz (a) surface current distribution (b) E-field and (c) normalized 3-D radiation performance. (layers other than M_9 and M_1 are hidden)

Surface current distribution of the unified ACRPA is shown in Fig. 4.15(a). The enlarged view of surface current at slot edges demonstrates the amplified signal at drain terminal ports 8, 9, 10, compared to the signal at gate terminal ports 2, 3, 4. Similar amplification is also observed on the other slot. In fact, the effective current on ACRPA is the superposition of feed current and amplified current. The E-field distribution of ACRPA realized is displayed in Fig. 4.15(b) [at the cut shown in Fig. 4.15(a)], which also visualizes the amplified field after the drain edge. These results confirm the dominant mode operation of ACRPA with amplified signal at the drain terminal. Normalized 3-D radiation performance of ACRPA is shown in Fig. 4.15(c) which demonstrates the nearly broadside radiation.



(a) (b)

Figure 4.16: (a) Illustration of power variables defined at different ports and (b) simulated powers in the frequency range of interest.

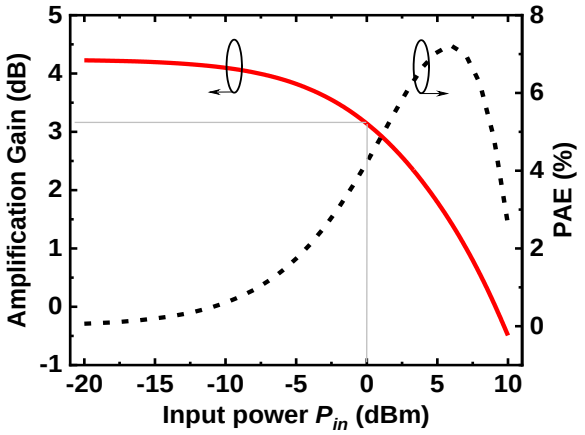


Figure 4.17: Simulated input power 1 dB compression point and PAE.

Table 4.6: Amplification gain across each transistor.

Ports	**2-8**	**3-9**	**4-10**	**5-11**	**6-12**	**7-13**
Amplification (dB)	4.2	4.1	4	4	4.1	4.2

The amplification gain across each of the biased transistor is calculated, and presented in Table 4.6. The minimal amplification deviation from the desired value of 4 dB across each transistor is due to slight impedance difference at the integration ports. In addition, input power Pin, average of power coupled to the three gate terminals on each slot edge P_G and P_{G1}, and average power of three drain terminals on corresponding slot edges P_D and P_{D1} [as illustrated in Fig. 4.16(a)] across the frequency range are shown in Fig. 4.16(b), for reference.

Furthermore, the input power 1 dB compression point of ACRPA is evaluated as 0 dBm from the harmonic balance simulation in Keysight-ADS platform, and the corresponding result is demonstrated in Fig. 4.17. For this analysis, the input power P_{in} is the power fed to the gate terminals $P_G + P_{G1}$ of transistors in ACRPA, and output power $P_{out} = P_D + P_{D1}$ 1is the total power present at drain terminals of all the transistors integrated within the ACRPA.

In addition, the power added efficiency (PAE) is calculated from

$$PAE\ (\%) = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_D + P_{D1} - (P_G + P_{G1})}{V_D I_D} \tag{4.1}$$

where drain voltage of circuit V_D = 1.2 V, and the effective DC drain bias current I_D =30 mA (5 mA of each transistor× 6 transistors in parallel) will calculate the DC power P_{DC}, in addition to simulated P_{out} and P_{in}. The variation in PAE with the input power is demonstrated in Fig. 4.17, and the maximum PAE is 7.2 % from simulations. It is worthwhile noting that the ACRPA performance is mainly limited by the 65nm CMOS technology utilized for demonstration in this work. However, the implementation of such designs in a technology with higher f_t/f_{max} such as SiGe will significantly enhance the overall performance.

4.4.2.7 **Comparison**

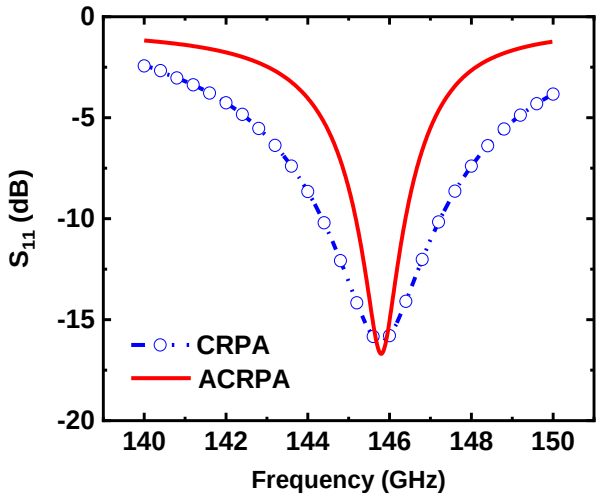


Figure 4.18: Matching performances of CRPA and ACRPA

Designed CRPA and ACRPA matching performances are compared in Fig. 4.18, which demonstrates that they are matched at 146 GHz. Although, the matching bandwidth of ACRPA is lower than the passive counterpart, this bandwidth can be improved by using broadband radiators

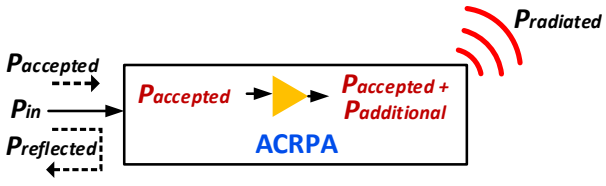


Figure 4.19: Illustration of different powers in ACRPA

In CST-MWS simultaions, the radiation efficiency η_r term is defined as

$$\eta_r = \frac{P_{radiated}}{P_{accepted}+P_{additional}} \tag{4.2}$$

where $P_{radiated}$ is power radiated, $P_{accepted}$ is accepted input source power P_{in} after matching and $P_{additional}$ is the external power which is in addition to the input source power P_{in}. For example, this additional power $P_{additional}$ can be induced from the amplification of transistor. Furthermore, an additional parameter termed as system radiation efficiency η_s

$$\eta_s = \frac{P_{radiated}}{P_{accepted}} \tag{4.3}$$

is enabled during the co-simulation in CST-MWS platform [all these parameters are further illustrated in Fig. 4.19]. Both of these terms remain equal for passive antennas, where an additional power is not injected/generated ($P_{additional}$ = 0). However, these terms are different if there is an additional power (for example, amplified power in this work).

Table 4.7: Simulated/co-simulated results comparison of active antenna (paralleled amplifiers designed in section-4.2.4 integrated with CRPA in section 4.3) and ACRPA at 146 GHz.

	Parameters	Paralleled amplifier (Case 1[a]) + CRPA	Paralleled amplifier (Case 2[a]) + CRPA	Proposed ACRPA
Antenna	*Directivity D (dBi)*	5.54	5.54	5.46
	Rad. efficiency η_r (%)	1.5	1.5	1.3
	Max. gain[b] (dBi)	-12.7	-12.7	-13.4
Paralleled Amplifier	*System rad. efficiency η_s (%)*	0.86	1.11	3.4
	Max. realized gain[c] (dBi)	-15.1	-14	-9.2
Integrated Antenna	*Loss*	Maximum	Average	Minimum
	Size and Cost	Average	Maximum	Minimum

[a]*Paralleled amplifier configurations designed in Section 4.2.4*

[b]*Max. Gain = $\eta_r D$*

[c]*Max. realized gain = $\eta_s D$*

From Table 4.7, the antenna parameters of directivity D, radiation efficiency η_r and corresponding gain of ACRPA (without transistors integrated within it) are lower than that of CRPA, as these parameters decrease typically with reduction in patch size. However, active antenna parameters of system radiation efficiency η_s and realized gain are greater in ACRPA than the conventional counterparts (with paralleled amplifiers discussed in Section. 4.2.4 integrated with CRPA designed in Section-4.3), thanks to the amplified power radiated and low losses of ACRPA. The corresponding results are shown in Table 4.7, and confirms the simultaneous amplification and radiation through ACRPA. On the other hand, integration of the independently designed paralleled amplifier circuit and CRPA occupies a significant area making it expensive, and does not even realize higher amplified radiation because of the network losses. In this way, the proposed unified-module promises superior performances in comparison to the conventional counterparts, in addition to the architectural advantages of smaller footprint, low-loss, lower cost and so on. Notably, the low radiation efficiency η_r observed for the demonstrated antennas is because of the thin dielectric and high conductor loss of the process [128-130].

4.5 Array ACRPA

4.5.1 1 × 2 ACRPA

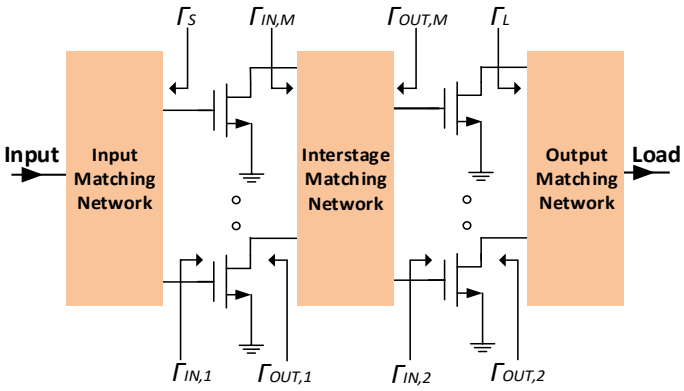


Figure 4.20: Block diagram representation of conventional cascaded paralleled amplifier.

Confirming the simultaneous matching, amplification and radiation through the highly integrated ACRPA, we extend it to a densely integrated and compact linear array with ACRPA elements.

Instead of interconnecting array elements with only lossy transmission lines [131], amplifying transistors have been utilized. In this manner, this array configuration offers unique advantages (particularly at mmW and THz) of; 1) utilizing the spacing and mutual coupling between array elements and; 2) reducing/removing the feed interconnection losses between array elements and increasing efficiency.

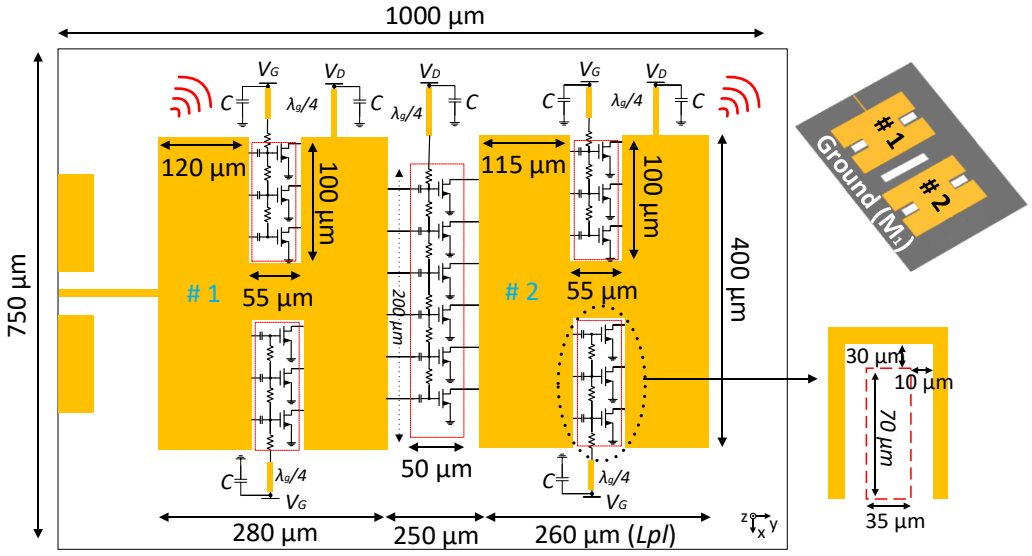
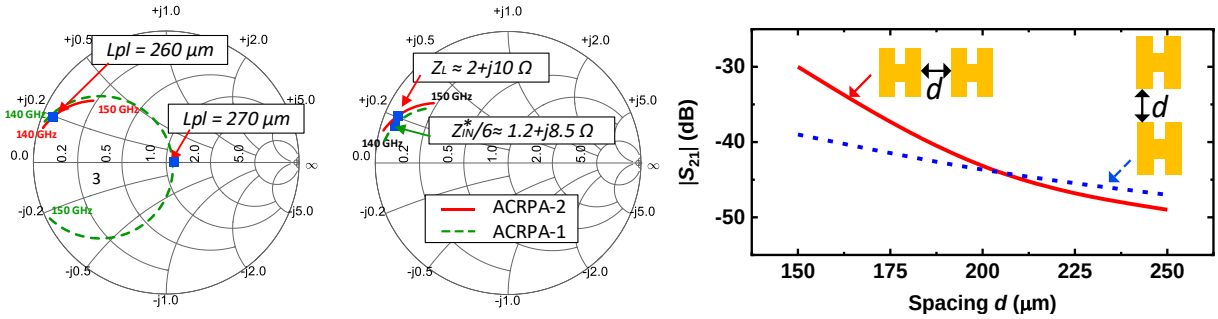


Figure 4.21: Demonstration of 1 × 2 ACRPA (- - - - demonstrate the slots etched in the ground plane).



(a) (b) (c)

Figure 4.22: (a) Impedance variation with ACRPA-2 length (b) impedance realized at the radiating edge of ACRPA-2 for drain terminals integration and ACRPA-1 for gate terminals integration along with design frequency highlighted (c) mutual coupling variation with spacing along E-plane and H-plane.

The proposed unified array configuration is also attractive in dividing the power handled by each stage and combining power spatially. This reduces the heat accumulation and thus corresponding losses generally observed in the pre-loading stage of a cascade amplifier configuration [as shown in Fig. 4.20]. Subsequently, the high power handling conditions specified in [37] for cascade amplifier have been adapted for a linear 1 × 2 ACRPA design and are formulated in (4.4) [the corresponding parameters are demonstrated in Fig. 4.20].

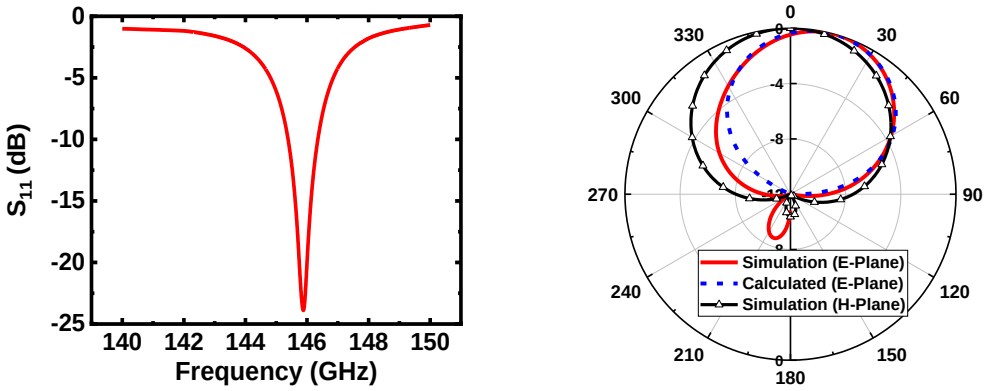
$$\Gamma_s = \Gamma_{IN,1}{}^*,\ \Gamma_{IN,M} = \Gamma_L,\ \Gamma_{OUT,M} = \Gamma_{IN,2}{}^* \tag{4.4}$$

The final integrated 1 × 2 ACRPA with all the dimensions marked is shown in Fig. 4.21, except the feed dimensions which remain similar to that of CRPA. The ACRPA forms array elements 1 and 2 with an approximate amplification gain of 4 dB each. The transistors integrated between array elements are also loaded to achieve the same amplification gain of 4 dB with N=6 transistors in parallel. Since, the load impedance Z_L required is in the inductive region with low impedance, the ACRPA length is decreased to have an input edge impedance of Z_{edge}= Z_L. The high Q of ACRPA resulted in realizing this impedance at a slight decrease in its length. The corresponding array element is termed as ACRPA-2 and its impedance response with variation in length L_{pl} is shown in Smith chart Fig. 4.22(a). The fundamental mode operation enables an approximately equal impedance along the radiating edge as also analyzed in Section. 4.3.1, facilitating the integration of multiple transistors with the same load impedance. Even mode decomposition results in the impedance 6 Z_L, as seen by the drain terminal of each transistors in parallel between array elements as desired.

Subsequently, the input impedance Z_{IN} at the gate terminal of each transistor is calculated with all the drain terminals connected to the edge of ACRPA-2. ACRPA-1 is then designed to conjugate match impedance Z_{IN} */6 on one edge and transform to 50 Ω feed impedance on the other end for measurements. Moreover, a slot is introduced over the ground plane at the center between array elements to enable transistors integration. In fact, the mutual coupling variation with spacing between array elements in the presence of center slot has been analyzed, and the result is shown in Fig. 4.22(c). The low mutual coupling observed at smaller spacing is attributed to the low radiation efficiency of antennas and electrically thin substrates utilized in demonstration [132]. Eventually, the spacing between array elements is chosen to be d=250 μm as a compromise between the

intended high-density integration, lower mutual coupling and negligible impact on the individual array elements performance because of slot. ACRPA-1 is then designed by connecting the 50 Ω impedance on the feeding edge, and in the presence of ACRPA-2 to include any existing mutual coupling. Finally, all the dimensions of both ACRPA-1 and 2 have been further co-optimized in an array environment to achieve the desired performance. Subsequently, the final impedance realized on the radiating edge of ACRPA-1 and ACRPA-2 where the inter-element transistors gate and drain terminals are integrated respectively is shown in Fig. 4.22(b). [116] provides further theory and analysis for realizing the amplification and matching utilizing transistor in-between array elements.

In operation, the input signal fed to the 1 × 2 ACRPA is initially amplified through the transistors within ACRPA-1 and a part of this signal is radiated. The remaining signal is coupled with the transistors integrated in between the array elements. This signal is further amplified through them and is fed to the ACRPA-2. This signal is again amplified by the ACRPA-2 and radiates the whole signal.

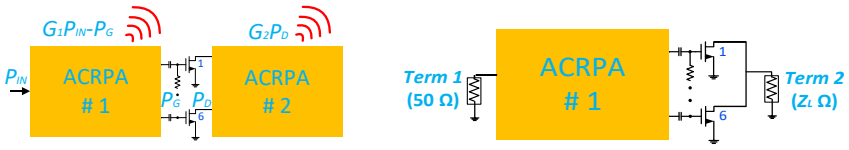


(a) (b)

Figure 4.23: Co-simulation results of 1x2 ACRPA (a) impedance matching and (b) normalized radiation performance.

The simulation procedure is similar to ACRPA discussion, and the corresponding results are discussed here. The prototype demonstrates a good matching at the design frequency of 146 GHz (Fig. 4.23(a)). The ADS co-simulation confirms the average amplification gain of around 4 dB within the ACRPA-2, 4.1-dB in ACRPA-1 and 3.8 dB through the transistors between array

elements. It has a realized gain of -7 dBi (-13.4 dBi in antenna gain+6.4 dB in amplification and array gain), 90^0 half power beamwidth, and a front-to-back ratio of 4 dB. The co-simulated normalized radiation performance of the proposed 1 × 2 ACRPA is shown in Fig. 4.23(b). The maximum radiation realized along $+17^0$ with respect to normal in E-plane is further analyzed through the well-known array pattern calculation [39]



(a) (b)

Figure 4.24: Schematic utilized for the evaluation of (a) amplitude and (b) phase difference between array elements.

$$Array\ pattern = Array\ Factor\ (AF_E) \times\ element\ pattern \tag{4.5}$$

$$where, AF_E = \left(1 + a_E e^{j\psi_E}\right), \psi_E = kd_E \sin\theta_E + \varphi_E \tag{4.6}$$

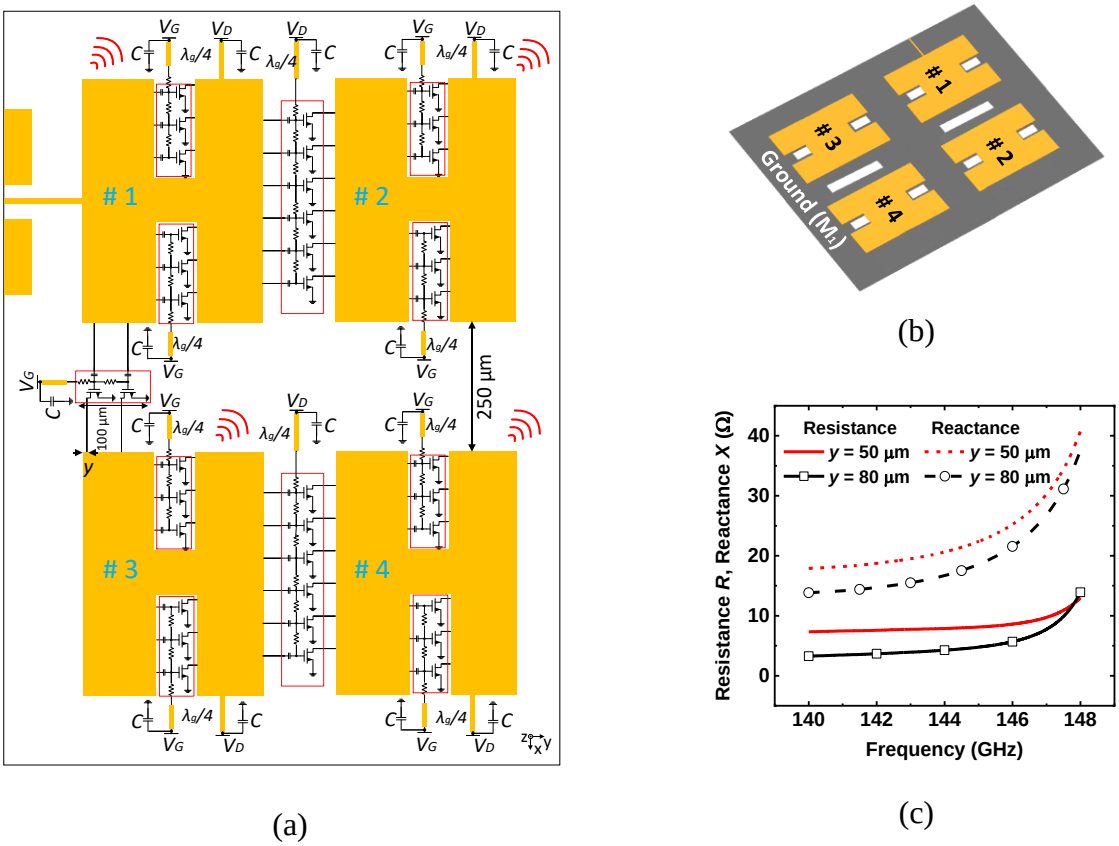
$$element\ pattern = \cos\theta_E \tag{4.7}$$

where k =3.0578 rad/mm is the phase constant, a_E and φ_E are the amplitude and phase of signal radiating through ACRPA- 2 with respect to ACRPA-1, and d_E= 520 µm is the center to center spacing between them. From the absolute power and gain values known at various locations of 1 × 2 ACRPA through the schematic shown in Fig. 4.24(a), a_E can be evaluated as 1.3 from

$$a_E \approx \sqrt{\frac{G_2 P_D}{G_1 P_{IN} - P_G}} \tag{4.8}$$

where G_1 and G_2 are the amplification gains within ACRPA-1 and ACRPA-2 respectively, P_G and P_D is the effective total power (sum of the powers from each individual transistor) present at the gate and drain terminals of inter-element transistors, and $_{PIN}$ is the input source power. On the other hand, the relative phase of signal between array elements is estimated to be φ_E= -70^0 through the schematic shown in Fig. 4.24(b). Here, the phase shift induced is attributed to both the ACRPA-1 and the impedances loading the transistors [63]. From this information, the resultant calculated array pattern response along E-plane matches well with the simulated response as shown in Fig. 4.23(b)

4.5.2 2 × 2 ACRPA



(a) (b) (c)

Figure 4.25: (a) Demonstration of 2 × 2 ACRPA model. (- - - - demonstrate the slots etched in the ground plane) (b) layout of 2 × 2 ACRPA and (c) impedance variation on the non-radiating edge position of 1 × 2 ACRPA consisting of array elements #3 and #4.

The 2 × 2 ACRPA layout [as in Fig. 4.25(a) and Fig. 4.25(b)] constitutes two sections of the designed 1× 2 ACRPA integrated in parallel with the gate, drain impedance, and the number of amplifying transistors unchanged. In order to remove the lossy interconnections even between the two parallel 1× 2 ACRPA sections, amplifying transistors are utilized. The excitation and operation of array elements 1 and 2 are similar to the discussion in the 1× 2 ACRPA. However, array element 3 (in the parallel linear path) is excited at the non-radiating edge from the amplified signal coupled through the non-radiating edge of array element 1. Such an interconnection also excites the fundamental mode as required [133-135] and follows the impedance behaviour discussed in

Section 4.3.1. Therefore, the feed point can be moved towards the center (along the length) to decrease the impedance or move towards the edge (along the length) to increase the impedance as required. Moreover, the mutual coupling variation along H-plane with spacing is analyzed and the corresponding result is illustrated in Fig. 4.22(c). The spacing along H-plane is chosen again as a compromise between intended high-density integration, lower mutual coupling and negligible impact on the individual array elements performance in the presence of slot in H-plane. As the amount of power coupled with the non-radiating edge port is lower than -15 dB from array element 1, we have reduced the number of transistors integrated between these linear paths, thus lowering the corresponding losses and unnecessary additional parallel paths. Although the coupled power from non-radiating edge of array element 1 to 3 is low, this can be enhanced by utilizing a cascaded amplifier configuration. On the other hand, this low coupling will be interesting for array antenna applications with minimum side lobe level requirement in radiation pattern. Two transistors are thereby utilized to integrate the two paralleled sections and realize the same amplification gain of 4 dB. Subsequently, the drain terminal should be loaded with impedance $2Z_L$=12+j52 Ω, resulting in the non-radiating edge impedance requirement of Z_L = 6+j26 Ω. From Fig. 4.25(c), the corresponding impedance can be realized around y=50 μm which is more towards the radiating edge of ACRPA-3 as expected. The realized prototype exhibits an average amplification of around 4 dB at each of the slots located within all array elements, and it is around 3.8 dB through the transistors integrated between array elements. The simulation procedure is similar to the previous cases discussed, and the results are presented in the following experimental results section.

4.6 Experimental results

CRPA, ACRPA and 2 × 2 ACRPA prototypes are fabricated on a single CMOS die of 1.5 mm × 1.5 mm in size including pads. Two PCBs, with ground plane removed to eliminate its negative influence on antennas performance, are designed with DC and GND lines to individually bias ACRPA and 2 × 2 planar ACRPA. The die is glued at the center of the PCB and wire-bonded for DC biasing. Although, the biasing could be integrated on the same chip; multiple DC sources are utilized to individually characterize the prototype performances. The biasing cables and bonding wires are deliberately aligned along the non–radiating edge to ensure that they do not influence the antenna performance. Furthermore, this negligible effect is also verified by including the wire

bonding cables in simulations. Periodical slots of 5 µm × 2 µm in dimension, with edge to edge spacing of 11 µm, are etched throughout all the metal layers to pass the design rule check (DRC) test, as defined by the fabrication process. These slots are inserted in parallel to the current flow to reduce its influence on the desired performance. It should be noted that the simulations are performed without these slots as they would increase the complexity of mesh and correspondingly the simulation time. Therefore, the introduced discontinuities over the mmW and THz frequency range might modify the measured results from simulations.

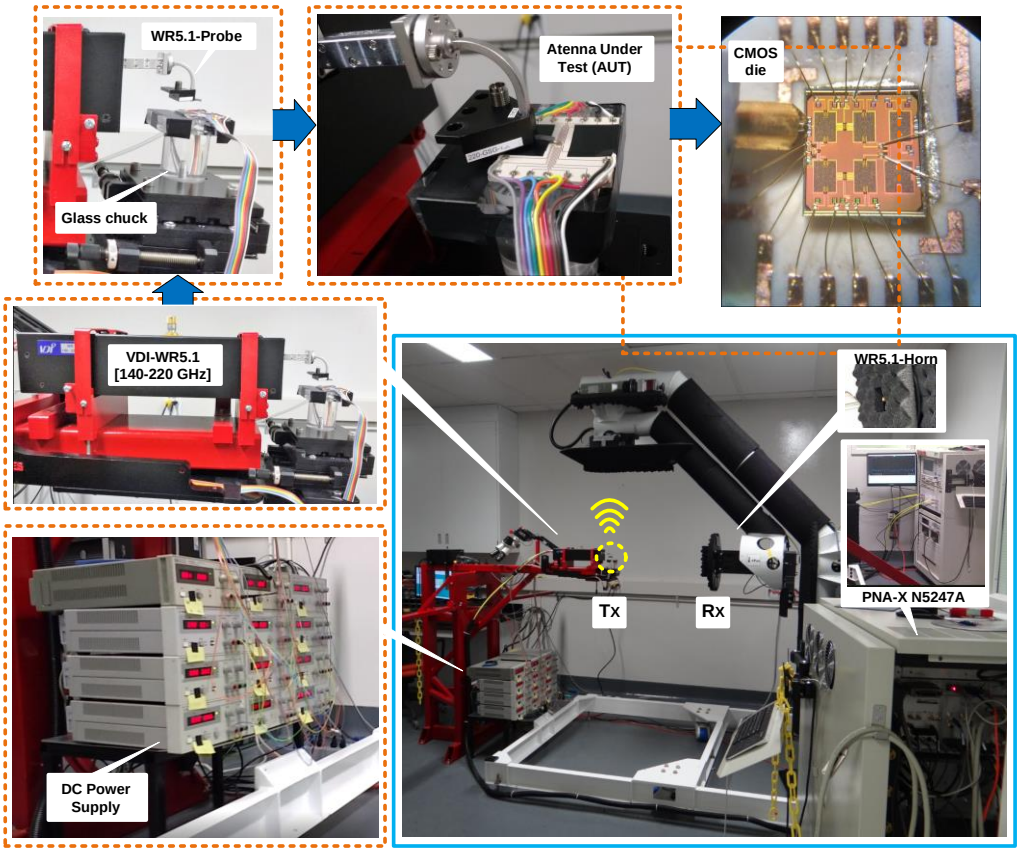


Figure 4.26: On-chip circuit-antenna experimental setup demonstrating the robotized NSI-far field measurements along with component description.

Measurements were carried out on wafer, comprising the Keysight N5247A PNA-X vector network analyzer, N5261A mmW extension controller, VDI WR-5.1 mmW/THz guide extension head (140 GHz to 220 GHz) and robotized NSI far field setup. Port 1 and port 2 of the VNA are

connected to the extension heads, which are cabled through RF, LO and IF and activated by 10 dBm input power.

In NSI farfield setup as shown in Fig. 4.26, the transmitting section head remains stationary and is interconnected with a waveguide to CPW transition for GSG probing of the antenna under test (AUT). A low dielectric glass platform supports the AUT far from the metal bottom to reduce the corresponding reflections. The whole platform can be tuned in position through *X*, *Y*, *Z* axes and tilt knobs. The final accuracy thereby realized after default setup calibration and tuning is $+1^0$. The receiving section is comprised of an extension head directly connected to a WR5.1 standard gain horn antenna, as a single module placed at a fixed distance of d = 70 cm from the transmitting AUT. This module is integrated in a movable robotic arm to enable the measurement in 3D space in any specified path fixed at fixed distance d [136].

The radiation performance is measured with a resolution of 1^0 for a limited range in both the E-plane and H-plane because of the restriction in equipment's free rotation within our lab environment—0^0 being the broadside. The probe station also blocks the signal in E-plane below -20^0 as it interferes with the line of sight path. Furthermore, multiple samples are measured to confirm the consistent performance of the proposed prototypes. The die micrograph with the CRPA, ACRPA and 2 × 2 ACRPA probed for measurements along with wire bonding and its biasing circuitry cables is also illustrated in Fig. 4.26.

4.6.1 CRPA

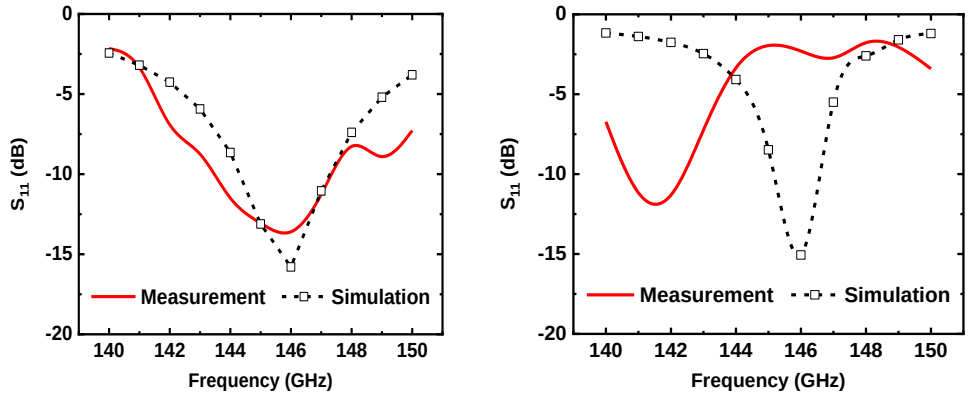
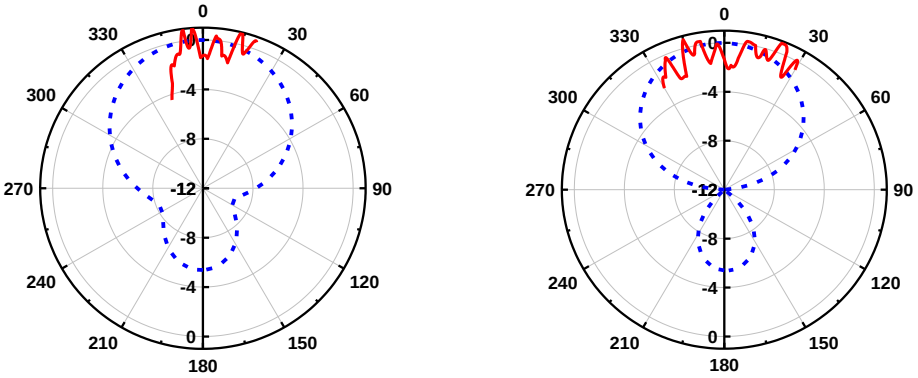


Figure 4.27: Impedance matching comparison of (a) CRPA and (b) ACRPA.



(a) (b)

Figure 4.28: Comparison of simulated (- - - -) and measured (——) normalized co-polarized radiation pattern of CRPA at 146 GHz in (a) E-plane and (b) H-plane.

The fabricated CRPA demonstrated a good impedance matching with the simulated result as shown in Fig. 4.27(a) and has a measured -10 dB bandwidth of 3.8 GHz (143.4 GHz -147.2 GHz). Subsequently, the simulated and measured normalized radiation performance in the E-plane and H-plane are compared in Fig. 4.28(a) and 4.28(b), respectively. Ripples of approximately 2 dB have been observed in the measured radiation pattern due to the signal scattering from nearby feeding setup [137], and are expected when the received power is less than -60 dB [138](which is the case here). Maximum radiation is along broadside, and the amount of signal received at port 2 with respect to input signal at port 1 can be calculated from

$$\left|S_{21(AUT)}\right|^2 = G_{T(AUT)} G_R \left(1 - \left|S_{11(AUT)}\right|^2\right) \left(1 - |S_{22}|^2\right) \left(\frac{\lambda}{4\pi d}\right)^2 \quad (4.9)$$

where AUT is CRPA here; $S_{21(AUT)}$ is the ratio of the output signal received at port 2 to the input signal from port 1; $G_{T(AUT)}$ and G_R are the antenna gain of CRPA and reference horn antenna respectively; $S_{11(AUT)}$ and S_{22} are the reflection coefficients of CRPA and reference antenna respectively; and d is the spacing between the two antennas.

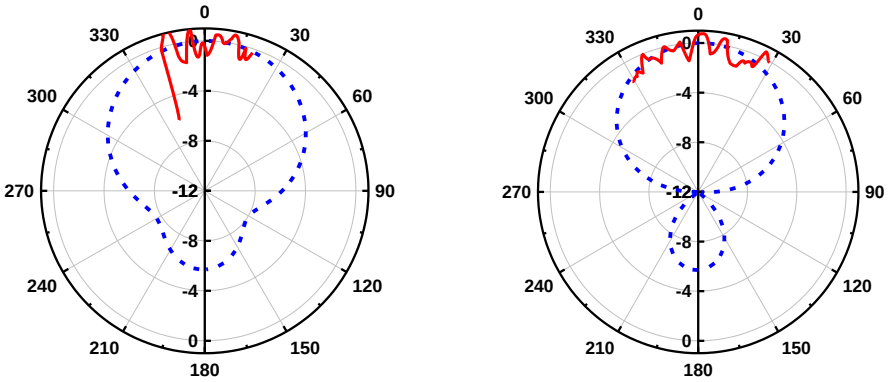
Equivalent isotopically radiated power (EIRP) can be calculated from the measured received power $P_R \approx$ -69.7 dBm, at the designed frequency of 146 GHz and along maximum radiation direction (the broadside). The path loss between the transmitting DUT and receiving standard gain horn antenna (of gain G_R = 22 dB) is L = 72.69 dB calculated from

$$L = 20\log\left(\frac{4\pi d}{\lambda}\right) \tag{4.10}$$

These terms can be utilized to calculate the EIRP = -19 dBm of CRPA from

$$EIRP = P_T + G_T = P_R + L - G_R \tag{4.11}$$

4.6.2 ACRPA



(a) (b)

Figure 4.29: Comparison of simulated (- - - -) and measured (———) normalized co-polarized radiation pattern of ACRPA at 142 GHz in (a) E-plane and (b) H-plane.

All the transistors are simultaneously biased with V_G=0.8 V and V_D=1.2 V respectively in addition to the input power. The impedance matching performance of ACRPA thereby obtained is presented in Fig. 4.27(b). Although, there is a frequency shift in the measured matching performance, the -10 dB bandwidth from simulations and measurements (140.7 GHz - 142.3 GHz) remain equal to 1.6 GHz. The normalized co-polarized radiation performance comparison in the E-plane and H-plane is compared in Fig. 4.29(a) and 4.29(b), respectively. ACRPA maximum radiation is also nearly broadside, and the power received in this case can be calculated from (4.9), where AUT is ACRPA. This result is compared with the measured passive counterpart CRPA result designed on the same board. Although this is not the ideal comparison, it provides the approximate information of amplification. Therefore, the realized gain of ACRPA can be described as

$$G_{T(ACRPA)} \approx G_{T(CRPA)} G_{amplifier} \tag{4.12}$$

which constitutes the gain of the CRPA (antenna gain) and the amplification gain (from transistors integrated within). Substituting (4.12) in (4.9) where AUT is ACRPA, and evaluating the result of

(4.9) where AUT is ACRPA upon (4.9) where AUT is CRPA, and rearranging them gives the amplification gain from

$$G_{amplifier} \approx \frac{|S_{21(ACRPA)}|^2}{|S_{21(CRPA)}|^2} \frac{\left(1-|S_{11(CRPA)}|^2\right)}{\left(1-|S_{11(ACRPA)}|^2\right)} \tag{4.13}$$

The receiving reference antenna parameters and the spacing d remain unchanged from the CRPA measurements, and therefore they cancel out. From all the measured parameters already known, we can calculate the increase in overall power radiation, which comes out to be 3.4 dB, which is close the simulated value of 3.5 dB from Table 4.7. Although there is a slight deviation from the simulation results, this confirms the matching of the ACRPA and amplification through the transistors integrated within. The EIRP is also calculated as -15.6 dBm from the measured received power $P_R \approx$ -66.3 dBm. The loss L remains constant as the spacing between antennas is unchanged.

The effects of varying the bias parameters on overall performance of the ACRPA have been measured in a limited range. Although, the ACRPA did not demonstrate a significant frequency tuning with drain bias variation, it has demonstrated an improvement in matching performance with increase in gate bias from 0.7 V to 0.9 V (at fixed V_D=1.2 V). The radiation performance also remained unchanged except for a slight change in the magnitude level with bias variation.

4.6.3 2×2 ACRPA

The entire transistors within the prototype are simultaneously biased with V_G=0.8 V and V_D=1.2 V, respectively. The matching performance of the proposed 2 × 2 ACRPA agrees closely with that of the simulation result as shown in Fig. 4.30(a), except a slight frequency shift, and has a measured -10 dB bandwidth of 4.6 GHz (145.2 GHz - 149.8 GHz). Frequency tuning range of 10 GHz is verified by varying V_D from 1 V to 1.4 V (at fixed V_G = 0.8 V), as in Fig. 4.30(b). Drain bias variation modifies the impedance seen into the input of array element 2 because of the transistors integrated within it. This results in the impedance variation seen by the transistor between array elements and its own characteristics, modifying the overall impedance at the gate terminals. This scenario runs simultaneously through the entire prototype, resulting in the overall frequency tuning observed. On the other hand, matching is improved with an increase in V_G from 0.7 V to 0.9 V, (at fixed V_D = 1.2 V) as shown in Fig. 4.30(c). This is realized because of tuning gate capacitance with gate bias.

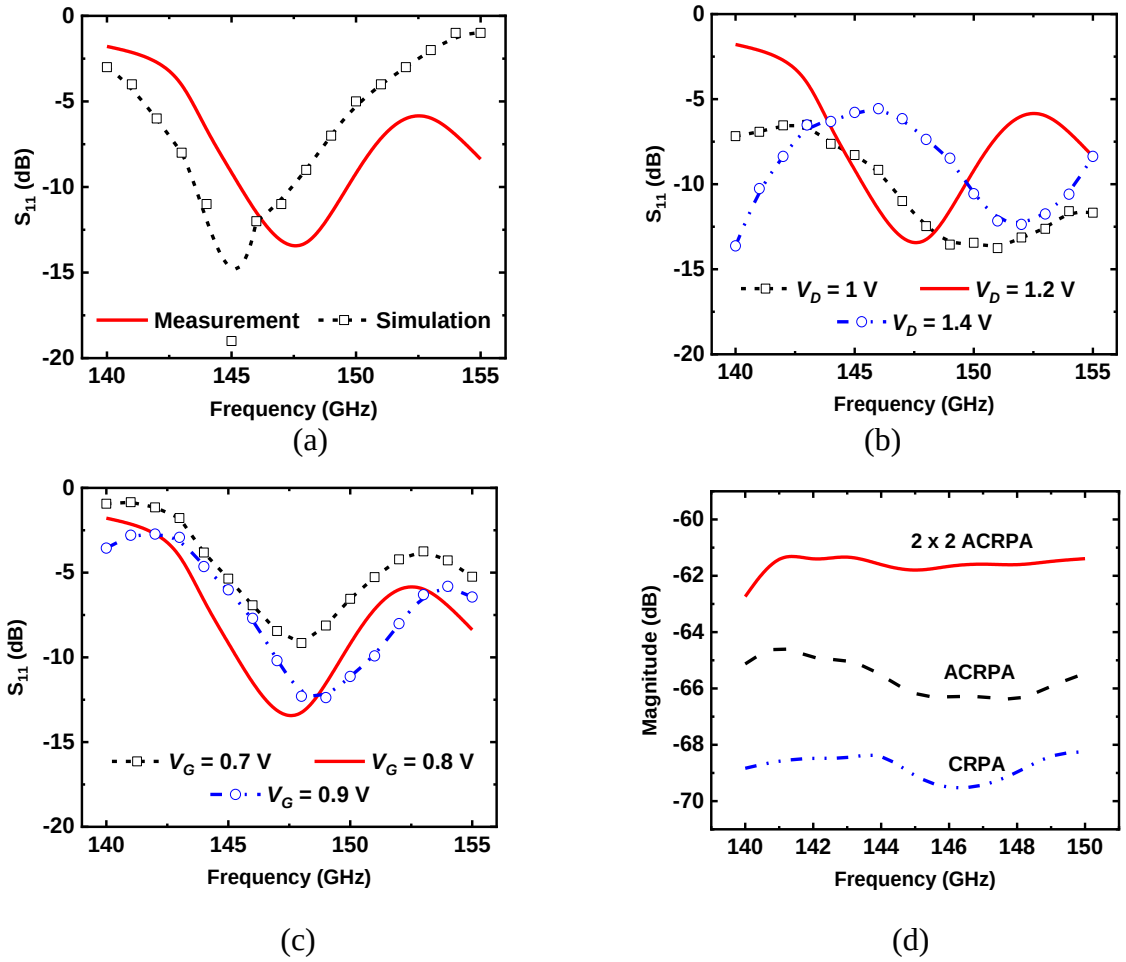


Figure 4.30: 2 × 2 ACRPA (a) impedance matching comparison (b) tuning of frequency varying drain bias (at V_G = 0.8 V) (c) tuning of frequency varying gate bias (at V_D = 1.2 V) and (d) absolute magnitude of received signal with respect to input signal for CRPA, ACRPA.

The performance of 2 × 2 ACRPA is compared with the modified passive CRPA result to extract the amplification gain. For an input power P_{IN} fed to the CRPA, the received power is calculated from (4.9) where AUT is CRPA. Assuming the same power P_{IN} is fed into an equivalent 2 × 2 CRPA (hypothetical array defined with same spacing and layout area as the 2 × 2 ACRPA, and utilized only for calculation) and array elements radiate this power in the same amplitude and phase ratio as the 2 × 2 ACRPA, we evaluate the array gain of 2 × 2 CRPA. Subsequently, this information is utilized to extract the amplification gain of 2 × 2 ACRPA. In this regard, the signal exciting these array elements has been estimated following the procedure described in Section. 4.5.1. The resultant array pattern evaluated has the maximum planar array gain enhancement by

approximately 2 dB compared to the measured signal of CRPA, and the radiation pattern is along -5^0 along the H-plane in addition to the $+16^0$ in E-plane. The effective antenna gain improvement of 2 × 2 CRPA compared to the CRPA is thereby calculated as

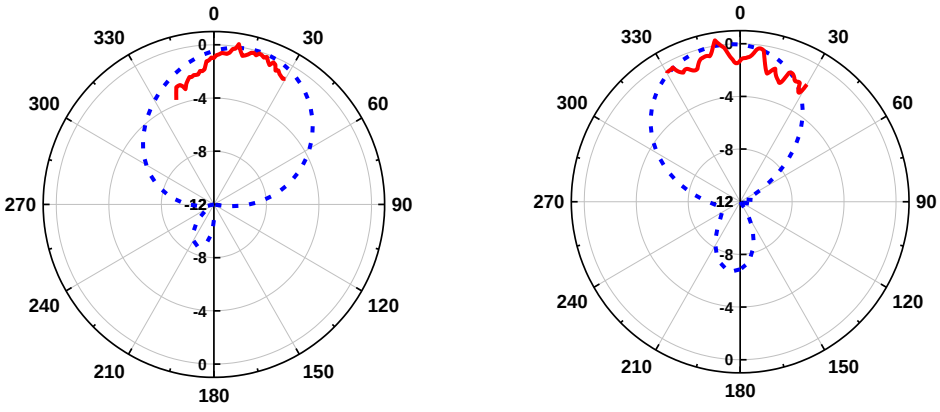
$$G_{T(2\times 2\ \mathrm{CRPA})} \approx 1.58 G_{T(CRPA)} \tag{4.14}$$

Subsequently, the 2 × 2 CRPA result is compared with the fabricated and measured 2 × 2 ACRPA result to estimate the overall amplification through the transistors integrated within the prototype. The received power measured for this case can be calculated from (4.9), where AUT is 2 × 2 ACRPA. The 2 × 2 ACRPA gain consists of passive array antenna gain as in (4.14) and amplification gain through transistors $G_{amplifier}$ as in

$$G_{T(2\times 2\ \mathrm{ACRPA})} \approx 1.58 G_{T(CRPA)} G_{amplifier} \tag{4.15}$$

Similar to the ACRPA analysis, substituting (4.15) in (4.9) where AUT is 2 × 2 ACRPA, and taking ratio of (4.9) where AUT is 2 × 2 ACRPA, upon (4.9) where AUT is CRPA gives the amplification gain from

$$G_{amplifier} \approx \frac{|S_{21(2\times 2\ ACRPA)}|^2}{1.58|S_{21(CRPA)}|^2} \frac{\left(1-|S_{11(CRPA)}|^2\right)}{\left(1-|S_{11(2\times 2\ ACRPA)}|^2\right)} \tag{4.16}$$



(a) (b)

Figure 4.31: 2 × 2 ACRPA normalized radiation pattern at 146 GHz in (a) E-plane and (b) H-plane (simulated (- - - -) and measured (———)).

The effective amplification gain through the transistors is thereby calculated to be around 6 dB, and corresponding EIRP is evaluated to be around -10.8 dBm. The comparison of simulated and

measured radiation pattern is compared in Fig. 4.31 and they agree well with each other. Furthermore, the beam steering and shift clearly proves that all the array elements radiate as an array in the proposed planar ACRPA. Even the ripples start decreasing as the amount of power received in this case is higher compared to the other prototypes. In addition, the comparison of absolute power calculated from the measured received power removing the matching, for designed prototypes is shown in Fig. 4.30(d), across the desired frequency range. Although, power handling capabilities can not be measured through our facility, this proposal demonstrates the unique way to realize a high power configuration which acts as a reference for future designers.

4.7 Conclusions

In this paper, we have successfully proposed, studied, and demonstrated a densely-integrated and topologically cohabited circuit-antenna at 146 GHz in a standard CMOS process. The proposed ACRPA has a size reduction of 26 % compared to its passive counterpart CRPA. It also exhibits amplification and radiation with paralleled transistors integrated within the antenna, without any additional circuitry such as input/output matching networks, power dividers or power combiners. Subsequently, the design and analysis of a linear 1 × 2 ACRPA is presented; where the transistors are utilized to connect array elements, thereby removing the commonly-used lossy feeding network. This reduces the associated losses and further amplifies the signal between array elements. Then, a planar 2 × 2 ACRPA is demonstrated with simulation and measurement results. Array elements are interconnected through the parallel amplifying transistors integrated in between them, and exhibit an overall amplification and array radiation. An EIRP improvement of 3.4 dB through ACRPA and around 6 dB through the 2 x 2 layout have been realized through the demonstrated prototypes with respect to their passive counterparts. Indeed, the presented prototypes have supported and demonstrated a much higher-density integration and unification of circuit-antenna beyond conventional front-end architectures. Such a self-consistently integrated circuit-antenna with topological cohabitation suggests that a nonlinear unified circuit-antenna could be developed for mmW and THz applications. This paper can pave the way for a very unconventional cohabitation and unification of active circuitry and antenna structures and can/could expect to have an impact in the near future.

CHAPTER 5 ARTICLE 3: ANALYSIS AND IMPACT OF PORT IMPEDANCES ON TWO-PORT NETWORKS AND ITS APPLICATION IN ACTIVE ARRAY ANTENNA DEVELOPMENTS

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In this paper, we present a comprehensive analysis of port impedance effects on a signal coupled across two-port networks, derive an equation to evaluate the impedances for a specified coupling, and demonstrate two prototypes of beam-shaping active array antenna to validate the theory. In this context, the generalized S-parameters are utilized, and the port impedance effects are theoretically studied and highlighted through an example. Subsequently, a closed-form equation is derived to accurately evaluate the port impedances that enable the achievement of a desired magnitude and phase of the signal coupling across the two-port network. The meaningfulness of all the potential results are discussed. Moreover, additional capabilities of the derived equation are presented through an example using a commercial transistor. With this understanding, a general modelling procedure is formulated to achieve the simultaneous amplification and phase shifting through only the active devices integrated directly between the antenna and feed line, without any additional circuitry. For verification, two 1x5 active array antenna prototypes are developed: one for broadside radiation with a -20 dB side lobe level requirement, and the other for flat-top radiation beam between -10^0 to 30^0. Rectangular patch antennas are chosen as the array elements in this demonstration, along with the commercial transistor CE3512K2. Furthermore, a 1x5 Wilkinson power divider is designed and integrated with the active array antenna prototypes for radiation pattern measurements. All these models are fabricated and measured. Their experimental results agree well with its simulated counterparts and theory, thereby proving the developed concept. Such solutions demonstrate the inherent advantages of being low-loss, compact, and efficient, which are essential for the next generation of wireless systems.

5.1 Introduction

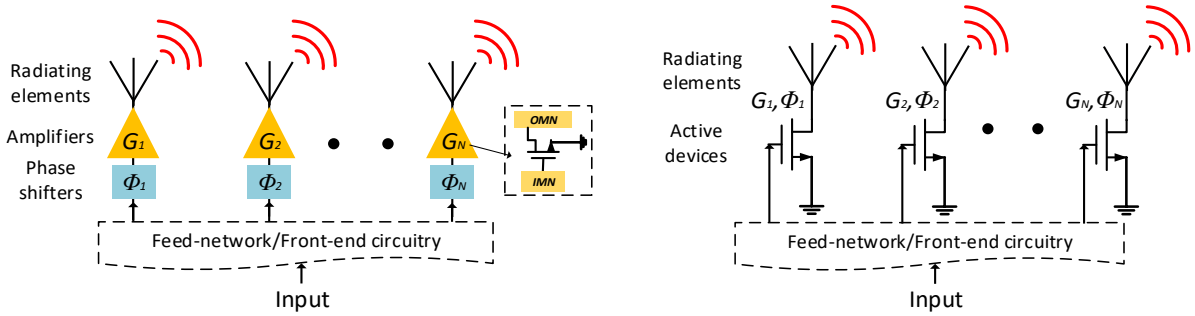


Figure 5.1: (a) Front-end amplifier and phase shifter circuits integration with antenna in a conventional approach (IMN: input matching network and OMN: output matching network) and (b) proposed unified circuit-antenna approach.

Array antennas have been a crucial part of present-day radar, sensing and communication applications operating in the lower GHz spectrum. Their significance further escalates in the emerging millimeter wave (mmW) applications, which include 5G [139], automotive radar [88], and so on, to cope up with high signal attenuation over these frequency bands. Moreover, they are sought for implementation in the next generation of terahertz (THz) applications in communications [140], imaging [141, 142], and spectroscopy [143].

In addition to the higher gain achieved through array antenna configurations, the flexibility in both the choice of array elements and their physical arrangement, along with the freedom in defining array element excitations are notable advantages. Indeed, these features facilitate an efficient control of its radiation pattern. For example, only a beam scanning is necessary for certain applications, which is predominantly realized by varying the phase of array elements. Meanwhile, another set of applications demand a pre-defined radiation pattern with constraints on its shape, direction, side lobe levels, and nulls. To fulfill such beam synthesis requirements, it is essential to control both the magnitude and phase of signals exciting the array elements, which will be demonstrated in this work. And, these beam-shaped patterns are desirable by a wide range of applications such as radar [144], satellite systems [145], wireless power transfer [146], communications [147], and so on.

To date, a large number of numerical and analytical approaches are available in the literature to evaluate the excitations that result in a specified radiation pattern [39, 41, 148-154]. However, an effective realization of such practical solutions has not progressed substantially away from its conventional configurations. In a purely passive implementation, unequal power dividers and delay lines are typically utilized for magnitude control and phase realization, respectively [155-158]. While, to achieve a higher EIRP, appropriately designed amplifiers are integrated at each array element along with the phase shifting circuitry [159-161], as illustrated in Fig. 5.1(a). In fact, such a configuration possesses the dedicated circuits that enable an independent control of magnitudes and phases. However, these circuits and even antennas are designed independently at 50 Ω reference impedance and then interconnected, making matching networks an indispensable part of these systems. As a result, the overall losses, weight, space occupied, and cost of these solutions scale proportionally with the increase in number of array elements desired, thereby limiting their efficiencies.

In this regard, active integrated antennas (AIAs) emerged as a popular integration technique, wherein the frontend active circuits and antennas are co-designed and physically close to each other [19, 42, 46, 47, 162]. In certain demonstrations, the active device outputs are directly integrated with the appropriately designed antenna, thereby eliminating the requirement for output networks of a classic active circuit[64, 68]. Nevertheless, the input networks are still required at each array element in case of a typical amplifier type AIA array configurations, which induces losses and influences the nearby antennas' performances. Furthermore, their design criteria is generally limited to achieve a desired magnitude or gain of the signal. Although the reference [163] has demonstrated that the load impedances can influence the phase shift, there are no clear directives on its control. Henceforth, a dedicated phase shifting circuitry is still required in these solutions.

In an effort to completely eliminate all the lossy passive circuitry components (present in an active circuit) while still realizing the amplifier circuitry and radiation functions, the concept of a unified and integrated circuit antenna (UNICA) arrays has been recently proposed [116-118]. Here, the array elements, which are connected in series, perform the multiple functions of matching and radiation, while the active devices integrated between them performs the signal amplification. In addition to the amplification realized through this approach, a beam steered radiation is reported, which is stemmed from the difference in phase exciting these array elements. Even though their

amplification control feature has been extensively discussed, a potential control on the phase shift, which also plays a crucial role in regulating the radiation performances, has not been presented.

Therefore, the phase shift in amplifier designs is generally an ignored term, starting right from the conventional solutions to present-day advanced integration techniques of AIA and UNICA. However, it can no longer be overlooked as the interest for multifunctional modules has gained prominence for mmW and THz range applications. Also, these modules are intended to be co-designed and integrated at complex reference impedances to eliminate the commonly required lossy matching networks between them. Therefore, the effect of complex impedances on the phase shift along with the magnitude of the signal coupled across a two-port network should be discussed extensively, which holds valid even for an amplifying transistor. Subsequently, this understanding paves the way for the development of deeply integrated solutions, as shown in Fig. 5.1(b). Here, the active devices alone can be loaded with appropriate impedances so that the desired gain and phase shift can be simultaneously realized without resorting to any matching networks or phase shifters. Eventually, these solutions provide the much-anticipated advantages of being low-loss, lightweight and compact that are desired for the next generation wireless systems.

In this work, we start with a theoretical investigation on the impact of ports impedances on the magnitude and phase shift of the signal across a two-port network. This is followed by a systematic derivation towards a closed-form equation to evaluate the load or input impedances for a pre-specified magnitude and phase shift. Subsequently, possible results from these equations and their meaning are described, followed by the discussion on abilities of derived equations. The modelling procedure for novel integration of active devices and antennas is then discussed, along with the co-simulation approach and prototype specifications. Finally, the design of two example prototypes as well as a power divider are discussed to prove the concept and facilitate the measurements, respectively. This is followed by concluding remarks.

5.2 Generalized S-parameters

In the conventional approach, the frontend building blocks and antennas are designed independently at a real reference impedance value (50 Ω in general), and they are eventually integrated together to realize the wireless system. In such configurations, the desired information regarding the matching of all ports and coupling across ports is predominantly evaluated through

S-parameters. Indeed, we are familiar with the corresponding outcomes at real reference impedances.

In the development of unified and integrated solutions, however, the frontend circuits and antennas are co-designed and mostly integrated at complex reference impedances. In this context, the generalized S-parameters that support the complex reference impedances should be utilized. Moreover, the real port impedance can be considered a specific case of these parameters. They also support the formulation of networks where the characteristic impedance does not exist (like in lumped circuits). In fact, these features of the generalized S-parameters generally make them superior as well as appropriate and promising for the design of highly integrated circuit-antenna solutions.

5.2.1 Theoretical analysis

Figure 5.2: Two-port network demonstrating all the variables in connection with the generalized S-parameters.

The generalized S-parameters $[S]_p$ of a two-port network are defined in terms of power waves as

$$b_{p1} = S_{p11}a_{p1} + S_{p12}a_{p2},\ b_{p2} = S_{p21}a_{p1} + S_{p22}a_{p2} \tag{5.1}$$

where

$$a_{p1} = \frac{1}{2\sqrt{R_S}}\left(V_1 + Z_S I_1\right), a_{p2} = \frac{1}{2\sqrt{R_L}}\left(V_2 + Z_L I_2\right) \tag{5.2}$$

$$b_{p1} = \frac{1}{2\sqrt{R_S}}\left(V_1 - Z_S^* I_1\right), b_{p2} = \frac{1}{2\sqrt{R_L}}\left(V_2 - Z_L^* I_2\right) \tag{5.3}$$

and the corresponding variables can be understood in Fig. 5.2. The derivation and physical meaning of these equations are already discussed in [37, 164-166]. However, a detailed discussion on the

signal coupled from input to output ports with complex impedances is missing. As this analysis is important for this work, this has been studied and discussed here.

5.2.1.1 S_{p21} analysis

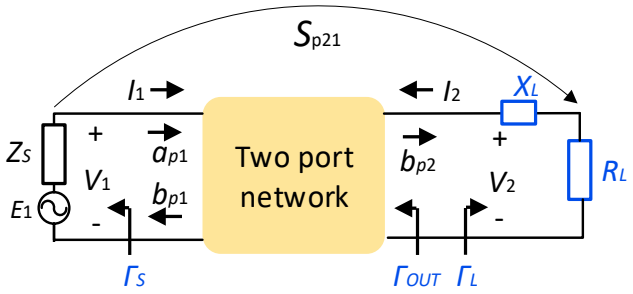


Figure 5.3: Two-port network demonstrating all the variables and illustration of S_{p21}.

Let us consider that an input source E_1 is present at port-1 with the source impedance Z_S, and load impedance Z_L is defined at port-2. In this regard, the source at port-2 is removed a_{p2}= 0, which results in

$$V_2 = -Z_L I_2 \tag{5.4}$$

Subsequently, the signal delivered from the input source at port-1 to the load at port-2 (S_{p21}) can be evaluated by substituting (5.4) in (5.1) as

$$S_{p21} = \left.\frac{b_{p2}}{a_{p1}}\right|_{a_{p2}=0} \tag{5.5}$$

Substituting (5.2) and (5.3) in (5.5), and expanding it using (5.4) results in

$$S_{p21} = \frac{2\sqrt{R_S}(V_2 - Z_L^* I_2)}{2\sqrt{R_L}(V_1 + Z_S I_1)} = \frac{I_2\sqrt{R_S}(-Z_L - Z_L^*)}{\sqrt{R_L}(V_1 + Z_S I_1)} = \frac{I_2\sqrt{R_S}(-2\,Real(Z_L))}{\sqrt{R_L}(V_1 + Z_S I_1)} = \frac{-2I_2 R_L\sqrt{R_S}}{E_1\sqrt{R_L}} \tag{5.6}$$

Following this, the magnitude component of S_{p21} can be expressed as

$$|S_{p21}| = \left|\frac{I_2\sqrt{R_L}}{\frac{E_1}{2\sqrt{R_S}}}\right| = \left|\frac{\sqrt{\frac{I_2^2 R_L}{2}}}{\sqrt{\frac{E_1^2}{8R_S}}}\right| = \left|\sqrt{\frac{P_L}{P_{AVS}}}\right| \tag{5.7}$$

which envisions that $|S_{p21}|$ estimates the square root of power delivered P_L to the load resistance R_L upon power available from the source P_{AVS}. Interestingly, the square of this component $|S_{p21}|^2$ is equivalent to the transducer power gain G_T [37]

$$|S_{p21}|^2 = \frac{P_L}{P_{AVS}} = G_T \tag{5.8}$$

On the other hand, the phase component of S_{p21} is evaluated from the source E_1 to load resistance R_L, as

$$\angle S_{p21} = \angle\left(\frac{V_{R_L}\sqrt{R_S}}{E_1\sqrt{R_L}}\right) \tag{5.9}$$

$$V_{R_L} = -2I_2R_L \tag{5.10}$$

where the phase defining parameters are the load current at port-2 I_2 and source at port-1 E_1. In conclusion, the magnitude and phase of S_{p21} are evaluated from the input source E_1 to the load resistance R_L, as shown in Fig. 5.3, and they are dependent on the source and load impedances of a two-port network. In addition, the tuning range of S_{p21} magnitude and phase components achievable by varying the port impedance's are evaluated. The corresponding discussion is included in the appendix for reference.

5.2.1.2 **Coupling between ports with complex load impedances**

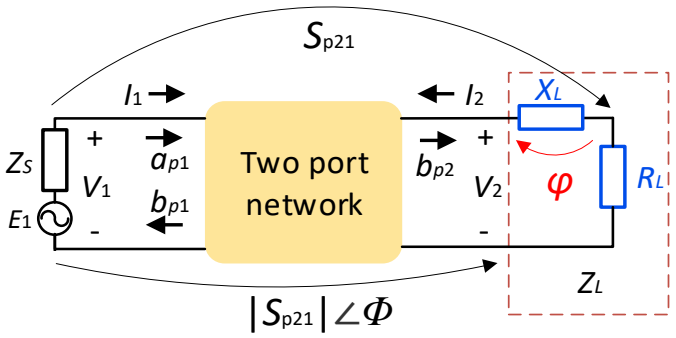


Figure 5.4: Illustration of all the variables S_{p21}, additional phase shift φ and effective phase shift Φ.

However, the signal coupled with R_L does not provide the complete information required for a direct integration at the complex reference impedance. Therefore, the signal coupled from the source to the complex load impedance Z_L=R_L+ jX_L should appropriately be evaluated.

Since, the power dissipated through the load reactance X_L is zero, the magnitude of signal coupled from source to complex load impedance Z_L still remains $|S_{p21}|$. On the other hand, the phase shift induced by the load reactance X_L should be considered to estimate the effective phase difference from the input source E_1 to the complex load impedance Z_L=R_L+ jX_L. This additional phase shift φ due to the load reactance X_L can be calculated through:

$$\varphi = \tan^{-1}\left(\frac{X_L}{R_L}\right) \tag{5.11}$$

Eventually, the effective phase shift Φ from the source E_1 at port-1 to the complex load impedance Z_L at port-2, as shown in Fig. 5.4, is equivalent to:

$$\Phi = \angle S_{p21} + \tan^{-1}\left(\frac{X_L}{R_L}\right) \tag{5.12}$$

In conventional circuitry with real load impedance R_L, the φ component is '0' as X_L is '0', and the effective phase shift across the two-port network is simply $\angle S_{p21}$. However, for the complex load impedance Z_L with non-zero reactance terms $X_L \neq 0$, the effective phase shift Φ is φ in addition to $\angle S_{p21}$.

If the load reactance is inductive, X_L is positive, and tuning it from 0 to ∞ will result in φ varying from 0^0 to $+90^0$. Similarly, X_L is negative for a capacitive load reactance and tuning it from -∞ to 0 will modify φ from -90^0 to 0^0. As a result, the effective phase shift range Φ realizable through the complex load impedance variation is 180^0.

5.2.2 Example

Indeed, a majority of the present-day commercially available simulation platforms, including Keysight ADS, CST-MWS, and ANSYS-HFSS among many others, makes use of these generalized S-parameters wave definitions [167, 168]. Since, these platforms will be eventually utilized for design and development, it is worthwhile to note that the magnitude of source defined is the signal/power available from source, while the phase value defined is the phase of source E_1.

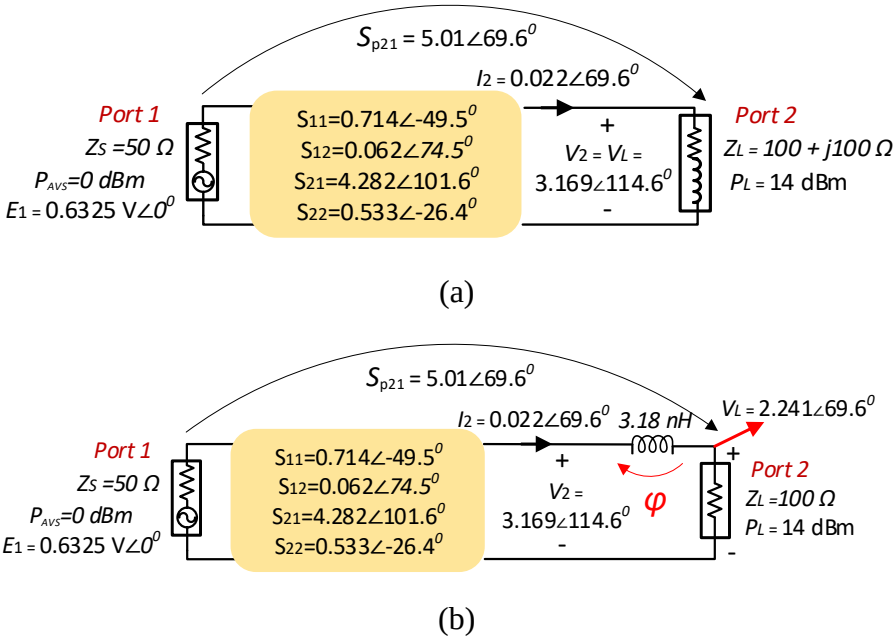


Figure 5.5: Schematic in Agilent ADS to study the power coupled from input to output of a two-port network with port-2 impedance of (a) Z_L and (b) R_L.

For example, let us consider a two-port network design in the Keysight ADS platform as shown in Fig. 5.5. The input power value of 0 dBm and phase of 0^0 entered in the source at port-1 are the power available from source and phase of the corresponding E_1, respectively. Subsequently, the influence of port-2 reactance term on S_{p21} is analyzed, while maintaining the overall load impedance at port-2 to be constant. The two cases thereby studied are described below.

1. Port-2 impedance is chosen to be the complex impedance $Z_L = R_L + jX_L$. The corresponding schematic and the results are shown in Fig. 5.5(a).
2. Port-2 impedance is the resistance R_L, while X_L is present as a separate lumped component. The respective schematic and its results are illustrated in Fig. 5.5(b).

As analyzed, the simulated S_{p21}(and power delivered to the load P_L) is the same in both cases irrespective of the port-2 reactance term. This outcome also matches well with the result calculated from (5.6). And, the respective phase of S_{p21} is equivalent to the voltage phase across the port-2 with only resistance R_L, as shown in Fig. 5.5(b). This verifies that the S_{p21} calculation doesn't involve the load reactance term even if it is present in port-2. While the magnitude of signal coupled

is unchanged due to lossless reactance, the effective phase shift before the complex impedance in this example is 69.6^0+45^0=114.6^0, which is calculated from (5.12). Also, this calculated effective phase shift result matches well with the voltage phase before the complex impedance at port-2, as shown in Fig. 5.5. This confirms that the effective phase shift from (5.12) is evaluated before the complex load impedance.

Subsequently, this fundamental understanding guides us in the characterization, analysis, and design of unified circuit-antenna solutions.

5.3 Load impedance evaluation

It is thereby evident from (5.7) and (5.12) that the complex load impedance can potentially control the magnitude and phase of a signal coupled from port-1 to port-2 in a two-port network. Henceforth, a closed-form solution to evaluate the load impedance Z_L for a predefined combination of magnitude $|S_{p21}|$ and effective phase shift Φ will be worth deriving. However, to keep the consistency and simplify the necessary derivation, $\angle S_{p21}$ and $|S_{p21}|$ are both chosen initially and analyzed in detail. The analysis of the effective phase shift Φ is an easier extension of this step and is eventually discussed.

Assuming that the two-port network parameters are known beforehand in any standard format, they can be ultimately converted into equivalent [Z] parameters. Subsequently, the magnitude of power coupled from the source to the load, which is the transducer power gain G_T of a two-port network, can be expressed in [Z] terms as

$$G_T = |S_{p21}|^2 = \left| \frac{2Z_{21}\sqrt{R_S R_L}}{(Z_{11}+Z_S)(Z_{22}+Z_L)-Z_{12}Z_{21}} \right|^2 \tag{5.13}$$

where Z_{11}, Z_{21}, Z_{12} and Z_{22} are the [Z] parameters of a two-port network; Z_S=R_S+jX_S is the source impedance at port-1; and Z_L=R_L+jX_L is the load impedance connected at port-2.

When designing the transmitting frontend, the source impedance Z_S is predefined by the circuitry integrated before it. On the other hand, Z_S has to be determined in advance to design a low-noise receiver frontend [5]. Henceforth, Z_S is assumed to be known beforehand without losing the generality, along with the [Z] parameters of a two-port network.

From (5.13), the magnitude of S_{p21} is therefore the square root of G_T. The phase of S_{p21} is estimated across the two port network, as shown in (5.9). S_{p21} can therefore be calculated from the desired gain and phase combination. Thus, (5.13) can be further expressed as

$$S_{p21} = |S_{p21}| \angle S_{p21} = \frac{2Z_{21}\sqrt{R_S R_L}}{(Z_{11}+Z_S)(Z_{22}+Z_L)-Z_{12}Z_{21}} \tag{5.14}$$

where all the parameters, except for Z_L, are known. Rearranging (5.14) and simplifying it in straightforward steps results in (5.17):

$$(Z_{11} + Z_S)(Z_{22} + Z_L) - Z_{12}Z_{21} = \frac{2Z_{21}\sqrt{R_S R_L}}{S_{p21}} \tag{5.15}$$

$$(Z_{22} + Z_L) - \frac{2Z_{21}\sqrt{R_S R_L}}{S_{p21}(Z_{11}+Z_S)} - \frac{Z_{12}Z_{21}}{(Z_{11}+Z_S)} = 0 \tag{5.16}$$

$$Z_L - \frac{2Z_{21}\sqrt{R_S R_L}}{S_{p21}(Z_{11}+Z_S)} - \frac{Z_{12}Z_{21}}{(Z_{11}+Z_S)} + Z_{22} = 0 \tag{5.17}$$

Z_L is then expanded in terms of resistance R_L and reactance X_L as

$$R_L + jX_L - \frac{2Z_{21}\sqrt{R_S R_L}}{S_{p21}(Z_{11}+Z_S)} - \left(\frac{Z_{12}Z_{21}}{(Z_{11}+Z_S)} - Z_{22}\right) = 0 \tag{5.18}$$

and these components are discretely calculated. Equating the real terms in (5.18) will result in

$$R_L - Re\left(\frac{2Z_{21}\sqrt{R_L R_S}}{S_{p21}(Z_{11}+Z_S)}\right) - Re\left(\frac{Z_{12}Z_{21}}{(Z_{11}+Z_S)} - Z_{22}\right) = 0 \tag{5.19}$$

which can be rewritten as a second-order quadratic equation with variable $\sqrt{R_L}$ as

$$\left(\sqrt{R_L}\right)^2 - \sqrt{R_L}\ \mathrm{x}\ Re\left(\frac{2Z_{21}\sqrt{R_S}}{S_{p21}(Z_{11}+Z_S)}\right) - Re\left(\frac{Z_{12}Z_{21}}{(Z_{11}+Z_S)} - Z_{22}\right) = 0 \tag{5.20}$$

The solutions of (5.20) can be obtained from the standard formula for roots extraction in a quadratic equation, and its square provides the values of R_L (5.22). Similarly, equating the imaginary terms of (5.18) results in

$$X_L - Im\left(\frac{2Z_{21}\sqrt{R_S}R_L}{S_{21Z_L}(Z_{11}+Z_S)}\right) - Im\left(\frac{Z_{12}Z_{21}}{(Z_{11}+Z_S)} - Z_{22}\right) = 0 \tag{5.21}$$

which can be rearranged to calculate the X_L term as expressed in (5.23).

$$R_L = \frac{\left(Re\left(\frac{2Z_{21}\sqrt{R_S}}{S_{p21}(Z_{11}+Z_S)}\right) \pm \sqrt{Re\left(\frac{2Z_{21}\sqrt{R_S}}{S_{p21}(Z_{11}+Z_S)}\right)^2 + 4Re\left(\frac{Z_{12}Z_{21}}{(Z_{11}+Z_S)} - Z_{22}\right)}\right)^2}{4} \quad (5.22)$$

$$X_L = \sqrt{R_L}\ \mathrm{x}\ Im\left(\frac{2Z_{21}\sqrt{R_S}}{S_{p21}(Z_{11}+Z_S)}\right) + Im\left(\frac{Z_{12}Z_{21}}{(Z_{11}+Z_S)} - Z_{22}\right) \quad (5.23)$$

Table 5.1: Possible solution outcomes.

R_{L1} , R_{L2}	X_{L1} , X_{L2}	Comments	Load impedance Z_L
Real	Real	Two solutions	$R_{L1} + jX_{L1}$ $R_{L2} + jX_{L2}$
Complex (positive real)	Complex	No solution (Gain is not realizable, while phase is realizable)	$Re\{R_{L1}\} + jRe\{X_{L1}\}$ $Re\{R_{L2}\} + jRe\{X_{L2}\}$
Complex (negative real)	Complex	No solution	-

As understood from (5.22), there could be two load resistance values R_{L1} and R_{L2} for the pre-defined S_{p21} magnitude and phase combination. Following these threads, there will be two corresponding reactance solutions, X_{L1} and X_{L2}. All the possible solution combinations from these equations are described in Table 5.1. For the defined S_{p21}, the real values of R_{L1}, R_{L2} imply that two possible solutions exist, while the complex solution of R_{L1}, R_{L2} indicates that the desired S_{p21} is not achievable. The complex solutions are further analyzed and observed. If the real part of the corresponding resistance solution is positive, Re$\{R_{L1}\}$= Re$\{R_{L2}\}$ > 0, the specified phase can be realized with the corresponding real part of the reactance, Re$\{X_{L1}\}$=Re$\{X_{L2}\}$, resulting in Z_{L1}=Re$\{R_{L1}\} + j$Re$\{X_{L1}\}$=Z_{L2}, though not the magnitude. Subsequently, if the real term of resistance solution is negative, Re$\{R_{L1}\}$=Re$\{R_{L1}\}$ < 0, then both the desired magnitude and phase are not realizable.

Once the load impedance values have been derived, the effective phase shift Φ can be easily evaluated from (5.12).

5.3.1 Source impedance

Similarly, if the load impedance Z_L and parameters of the two-port network are known in advance, the source impedance Z_S can also be calculated for the desired S_{p21} magnitude and phase combination. Starting from (5.15), the source impedance Z_S can be evaluated following the similar steps of the load impedance Z_L calculation. All the resulting combinations and further analysis are similar to that of the load impedance. As such, this discussion is not included in this paper to avoid redundancy.

5.4 Transistor results and discussion

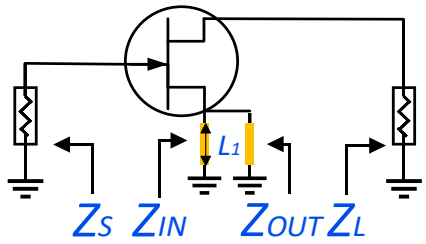


Figure 5.6: ADS schematic model with source, input and load impedance representation; L_1= 0.4 mm, W= 0.4 mm and via of diameter= 0.381 mm.

In the case of a commercial module in design, its characteristics are generally provided by the vendor, which are typically the S-parameters with a 50 Ω reference impedance $[S]_{50\ \Omega}$. Nevertheless, we can convert one form of parameters to another through the formulae defined in [169], if they are provided in any other standard format. Otherwise, the S-parameters of the two-port network $[S]_{50\ \Omega}$ can be conveniently characterized through the standard 50 Ω lab measurement setup. Once the characteristics of the network in design are known, they can be converted into equivalent [Z] parameters, from which the proposed approach can be executed and unfolded.

Although the previous analysis is generalized for applications in any two-port network, further discussion is limited in this work to the active device FET-CE3512K2 operating in a common source configuration and at design frequency of 5 GHz. The $[S]_{50\ \Omega}$ parameters of this commercial transistor have been already provided by the vendor at the desired gate and drain bias of -0.2 V and

1.2 V, respectively. Subsequently, this transistor is analyzed to be potentially unstable, restricting the impedances choice for antenna design [170]. Therefore, the stability region of the chosen transistor is primarily enhanced by introducing a shorted microstrip line at the source terminal, as shown in Fig. 5.6. The corresponding $[S]_{50\,\Omega}$ at the design frequency are

$$[S]_{50\,\Omega} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} 0.714\angle -49.5^0 & 0.062\angle 74.5^0 \\ 4.282\angle 101.6^0 & 0.533\angle -26.4^0 \end{bmatrix} \tag{5.24}$$

which are then converted into equivalent $[Z]$ parameters

$$[Z] = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} 44.8 - j32.5 & 9.3 + j5.6 \\ 393.4 + j635.6 & 83.2 + j4.6 \end{bmatrix} \Omega \tag{5.25}$$

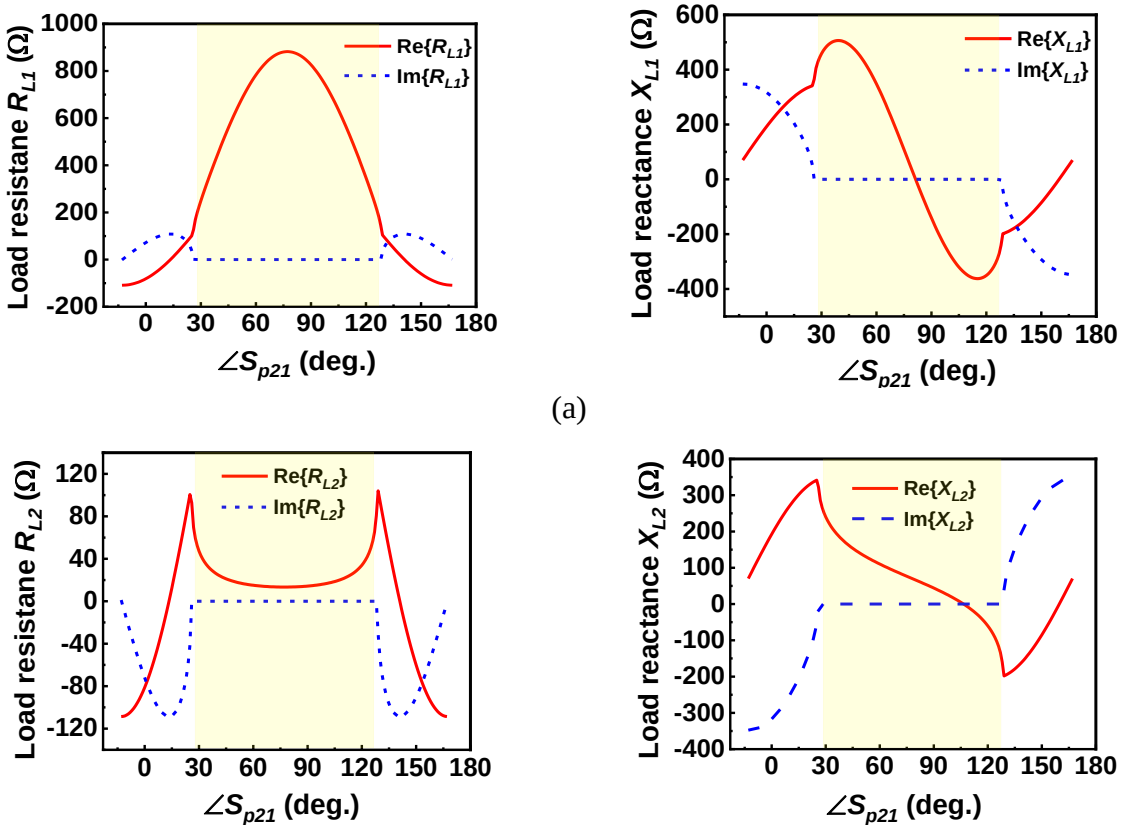


Figure 5.7: Illustration of all the load impedances calculated at constant G_T= 10 dB with (a) R_{L1} and X_{L1} and (b) R_{L2} and X_{L2} values.

From this information, the operating range of this transistor can be evaluated by following the procedure described in the appendix. For a fixed source impedance Z_S=50 Ω, Z_{OUT} corresponding to Γ_{OUT} is computed as Z_{OUT}=108.6-j71.9 Ω. Subsequently, the conjugate load impedance Z_L equals Z_{OUT}^* at the output, results in a maximum $|S_{p21}|$ of 5.060, and current phase of 77.287^0, which is the reference phase of S_{p21}. Then, the magnitude of S_{p21} can vary from 0 to 5.060, while the S_{p21} phase range is from $-90^0+77.287^0$ to $90^0+77.287^0$, which can be realized through an unrestricted load impedance variation.

In this phase range, all the load impedances corresponding to a specified transducer gain G_T ($|S_{p21}|^2$) can be instantaneously evaluated from equations (5.22) and (5.23) by varying the phase of S_{p21}. For example, the two sets of complex load impedance solutions realized at G_T =10 dB ($|S_{p21}|$=3.1623) within $\angle S_{p21}$ phase range are illustrated in Fig. 5.7(a) and 5.7(b). As discussed in Table 5.1, the evaluated load impedances where the imaginary components of both the resistance's and reactance's terms are zero can realize the desired magnitude and phase combination. Moreover, this region is highlighted in Fig. 5.7 for reference. Although, these impedances can also be plotted with respect to the effective phase shift Φ, it is recommended to plot them with respect to $\angle S_{p21}$ for better readability.

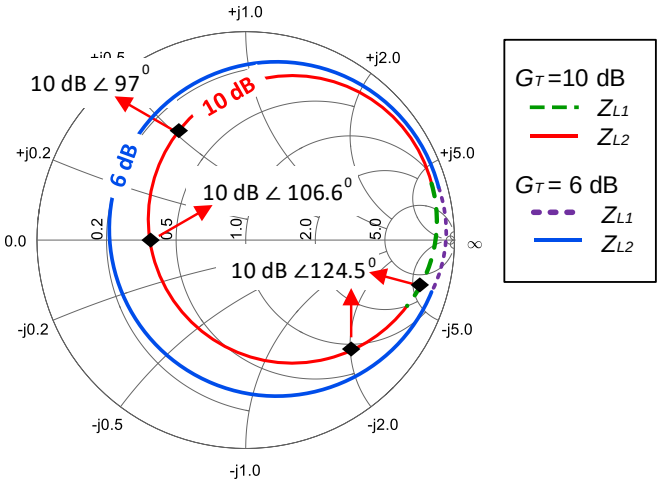


Figure 5.8: Calculated load impedances for G_T=10 dB and 6 dB

In addition, these load impedances are plotted in the Smith chart, as shown in Fig. 5.8, which are observed to form the constant transducer power gain G_T circles. Following this, the S_{p21} realized at the three distinct load impedance Z_L points on this circle are evaluated and highlighted in the Smith chart of Fig. 5.8, for reference. As expected, the magnitude of S_{p21} is constant, while the phase of S_{p21} varies with the loading impedance Z_L. In addition, an example with the two load impedance values that result in the same S_{p21} are also highlighted in this Smith chart. To further illustrate, all the load impedances related to the 6-dB gain are also evaluated and plotted in the Smith chart of Fig. 5.8, which are verified to demonstrate a similar behavior as the previous case.

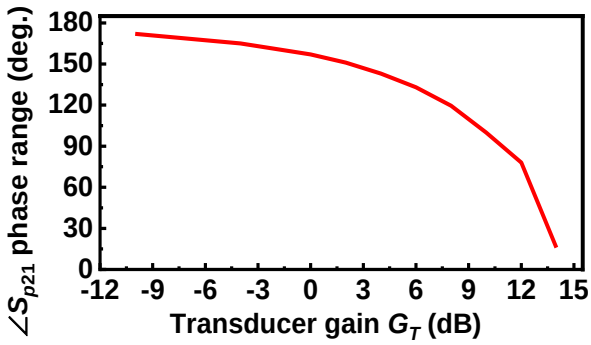


Figure 5.9: Phase shift range realizable for different gain values at fixed Z_S = 50 Ω

In addition, the S_{p21} phase range realizable at all the magnitudes of signal coupling can also be estimated, and the corresponding results are shown in Fig. 5.9. It is thereby observed that the phase range is maximum and approaching 180^0 at the lowest magnitude coupling and decreases with an increase in coupling. Furthermore, a similar response is also verified for the effective phase shift. This behaviour can also be explained by the transducer power gain circles, wherein the lower gain circle has a larger radius providing a wide range of impedance choices in comparison to the higher gain circle with smaller radius resulting in fewer impedance choices.

5.5 Modelling procedure and design process

With this prior knowledge, we are now proceeding to demonstrate its implementation in active array antenna solutions to realize the desired radiation pattern. Here, the typically required magnitude and phase combination, which excite the array elements, are directly realized by the

transistor integrated at the evaluated load impedances. The relevant general modelling approach is thereby discussed in this section, along with the co-simulation procedure and the prototype specifications.

5.5.1 Design process

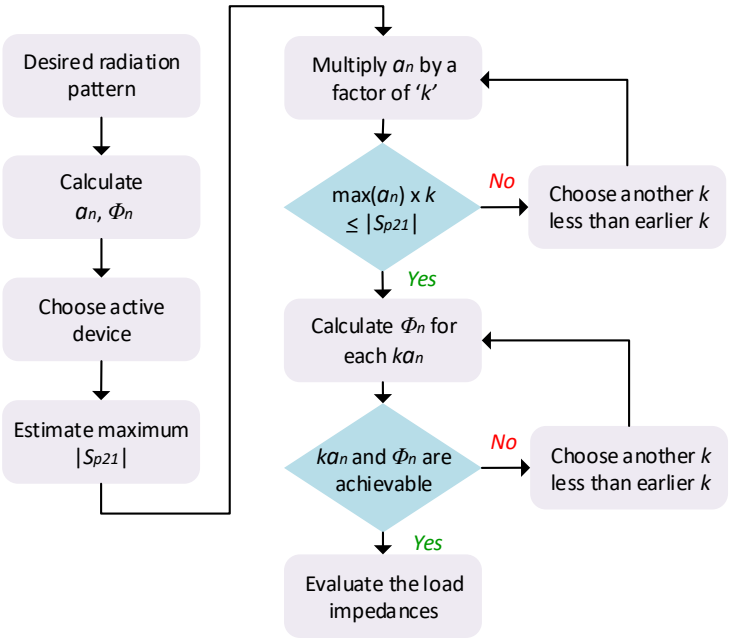


Figure 5.10: Flowchart describing the steps until the load impedances calculation for a predefined radiation pattern.

The detailed steps necessary in the evaluation of load impedances for a predefined radiation pattern are illustrated in the flowchart of Fig. 5.10, and the overall modelling procedure is discussed here in detail.

5.5.1.1 Beam synthesis

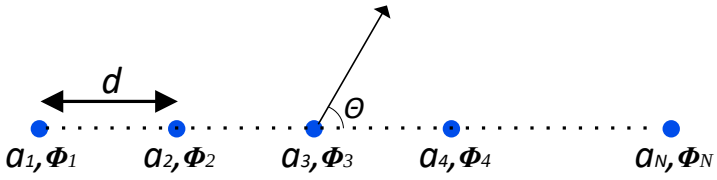


Figure 5.11: Illustration of a linear array configuration.

For a desired radiation pattern and fixed antenna layout, the excitations of each array element (amplitude $a_{n,n=1,\,2...N}$ and phase $\Phi_{n\,n,n=1,\,2...N}$ as shown in Fig. 5.11) can be evaluated from a wide range of techniques available in the literature. The accuracy of these excitations can be verified before the actual design, by plotting the corresponding radiation pattern calculated from the standard array factor approach. The relevant equations are

$$Array\ pattern = Array\ Factor\ (AF_E) \times element\ pattern \tag{5.26}$$

$$AF_E = \sum_{n=1}^{N} a_n e^{j\psi_n}, \psi_n = kd\cos\theta + \Phi_n \tag{5.27}$$

where the element pattern depends on the antenna configuration. After validation, we can proceed with the active device and antenna analyses followed by their co-design.

5.5.1.2 **Active device**

1. A commercial transistor must be initially chosen based on the requirement (or can even be designed). Then, its stability should be analyzed at the intended biasing point and design frequency.

2. If the transistor is potentially unstable, it is recommended to stabilize it for the amplifier operation. This ensures stability and increases the impedance choice, thereby relaxing the stringent requirements in antenna design with which the transistor is directly integrated.

3. The maximum $|S_{p21}|$ (square root of transducer power gain $G_{T,max}$) of this transistor can then be estimated to have a prior knowledge on the maximum achievable gain.

4. Afterwards, the desired amplitudes $a_{n,n=1,2...N}$ exciting each of the array elements can be multiplied by a common factor of k for amplified radiation. This maintains the desired amplitude ratio, and thereby the resultant radiation pattern is also preserved. Also, the multiplication factor k has to be chosen such that the corresponding maximum amplitude in $ka_{n,n=1,\,2...N}$ remains below the achievable maximum $|S_{p21,max}| = \sqrt{G_{T,max.}}$

$$\mathrm{Max}\{ka_{n,\,n=1,\,2...N}\} \leq |S_{p21,max}| \tag{5.28}$$

5. Subsequently, the effective phase shift range $\Phi_{n,n=1,\ 2...N}$ realizable at each updated amplitude $ka_{n,\,n=1,\,2...N}$ has to be estimated.

6. If the desired amplitude and phase combinations are realizable at all the array elements, we proceed to next step or the multiplication factor k must otherwise be reduced. Lowering k will increase the phase range and improve the chance of realizing the desired phase. Eventually, the achievability of the new gain and phase combinations have to be reassessed.

7. Once the desired gain and phase combinations at all the array elements are realizable, we advance to the calculation of corresponding load impedances. If multiple load impedances exist, the impedance which can be easily realized through antenna design has to be chosen.

5.5.1.3 **Array antenna**

8. Based on the evaluated impedances, an appropriate antenna configuration has to be selected that can provide the desired impedances and enables the direct active device integration. Moreover, this should be achievable without significantly degrading its radiation performance.

9. In general, the antenna dimensions can be tuned, and the feed positions can be varied in the selected resonant antenna structures to satisfy these requirements.

5.5.1.4 **Co-design**

10. When it comes to co-design, it is recommended to start with the array element which has the highest signal excitation.

11. The next maximum signal input array element is then designed in the presence of other array elements to include the coupling effects. Subsequently, the remaining array elements are designed by following this approach.

12. This approach is recommended in design as the array elements with a higher signal radiation will have a greater influence on the other array elements, and not the other way around.

13. Finally, the entire prototype is further co-optimized in an array environment to realize the desired outcome.

5.5.2 Co-simulation

The active device analysis is carried out in the ADS-schematic platform, while the necessary theoretical calculations are performed in MATLAB. Then, the array elements are designed in the CST-MWS platform. It is ensured that the desired impedance is realized at each array element, by performing simultaneous simulations in the presence of mutual coupling and with radiation pattern specific amplitudes and phases at each array element. After optimization, the array antenna S-parameter model is exported to Keysight ADS-schematic for co-simulation with the transistor to analyze the excitations at each array element and the circuitry performances. On the other hand, the active device S-parameter model is exported to CST-schematic for analyzing the co-simulated field distributions and radiation patterns.

5.5.3 Prototype specifications

The demonstrated prototypes are 1 x 5 linear active array antennas operating at the 5 GHz design frequency and with an inter-element spacing of a half wavelength of 30 mm. Microstrip rectangular patch antennas (RPA) are chosen as the array elements as they can be tuned to realize the desired impedance and can facilitate its direct integration with active devices. At the resonant length, the RPA provides real input impedance at the design frequency. Increasing this RPA length over the resonant dimension will realize a capacitive reactance, whereas decreasing this will result in an inductive reactance of RPA. In addition, the feed position can also be tuned along the RPA length to vary the impedance from maximum on the radiating edge to minimum at its center. In this way, RPA length can be tuned, and the appropriate feed position can be identified for a direct active device integration without significantly affecting its radiation performance. A detailed discussion and analysis on the impedance tuning and radiation effects of RPA are available in [116], for reference. The active device CE3512K2, which is stabilized and has been described in the Section 5.4, is chosen for integration. For activating it, the DC bias lines for gate terminals are integrated with the feed line, while the drain bias lines are integrated with the respective array elements. The input source impedance Z_S of each active device is chosen here to be 50 Ω, though it can be any other value depending on the circuitry integrated to it. Following the discussion of the modelling procedure, two prototypes have been developed on a PCB to realize different radiation pattern requirements and are presented in the following sections to prove the concept.

5.6 Chebyshev radiation pattern

The first demonstration involves the design of a 1 x 5 linear active array antenna to realize a broadside radiation with a sidelobe-level (SLL) of less than -20 dB. To realize this, the excitation of each array element is estimated from a Chebyshev array analysis [40]. The corresponding signal excitation ratio and equivalent power excitation ratio of each array element are presented in Table.5.2.

Table 5.2: Calculated and implemented signal excitations along with evaluated load impedances of each array element.

	Array Element	**# 1**	**# 2**	**# 3**	**# 4**	**# 5**
From Theory	Signal $\lvert S_{p21}\rvert$ $(\sqrt{W})$ ∠ angle Φ (deg.)	$1\angle 0^0$	$1.61\angle 0^0$	$1.93\angle 0^0$	$1.61\angle 0^0$	$1\angle 0^0$
	Power G_T (W) ∠ angle Φ (deg.)	$1\angle 0^0$	$2.59\angle 0^0$	$3.72\angle 0^0$	$2.59\angle 0^0$	$1\angle 0^0$
For Design	$\lvert S_{p21}\rvert$ $(\sqrt{W})$ ∠ S_{p21} (deg.)	$2\angle 111^0$	$3.22\angle 111^0$	$3.86\angle 111^0$	$3.22\angle 111^0$	$2\angle 111^0$
	R_L (Ω)	6.59	23.59	45.16	23.59	6.59
	X_L (Ω)	-5.4	-16.55	-31	-16.55	-5.4

5.6.1 Design

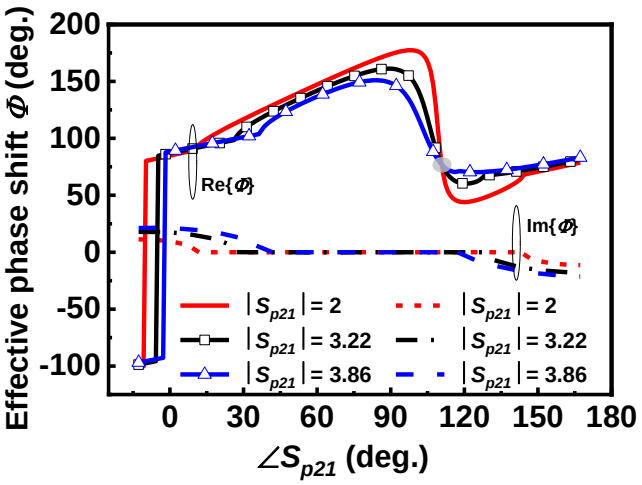
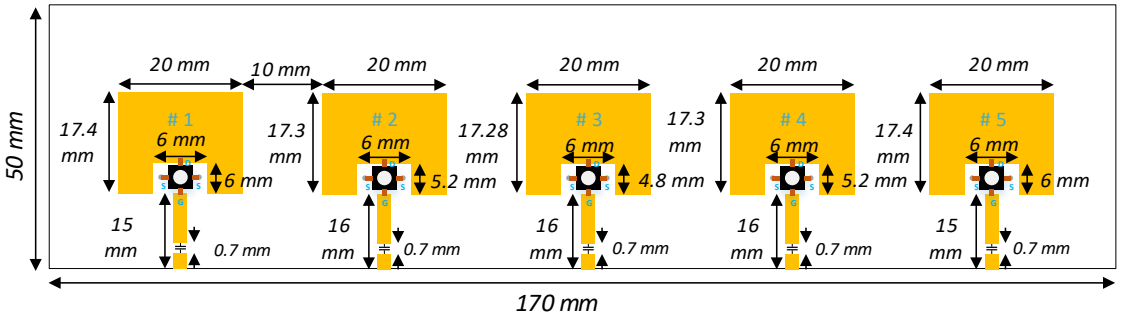


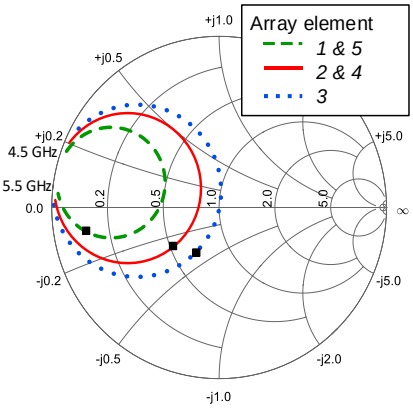
Figure 5.12: Evaluation of the phase related to the desired amplitudes.

For demonstration purposes, the amplitudes exciting each array element are doubled k=2 so that the required amplitude ratio is still maintained. The resulting highest signal level required, which

is 3.86 can be achieved as it is less than the maximum $|S_{p21,max}|$ value of 5.010. Subsequently, the entire range of effective phase shifts Φ that could be realizable by varying the load impedances at chosen signal levels are plotted in Fig. 5.12. As already highlighted in Table 5.1, the magnitude and phase combination is realizable when the evaluated load resistance and load reactance terms are real. In equivalence, this results in the effective phase shift to be real $\mathrm{Im}\{\Phi\} = 0$, when the desired magnitude and phase are realizable and, conversely, complex when they are not. Therefore, the realizable effective phase shifts Φ occur when its imaginary component is zero $\mathrm{Im}\{\Phi\} = 0$. Since the signal phases exciting all the array element should be equal, the effective phase of $\Phi = 77^0$ is chosen as the example where $\mathrm{Im}\{\Phi\} = 0$, and is also highlighted in the plot Fig. 5.12. The corresponding phase of S_{p21} is also constant for all these signal levels. As the magnitudes and phases of S_{p21} are known, the load impedances corresponding to each array element are evaluated through the equations (5.22) and (5.23) and are included in the Table 5.2.



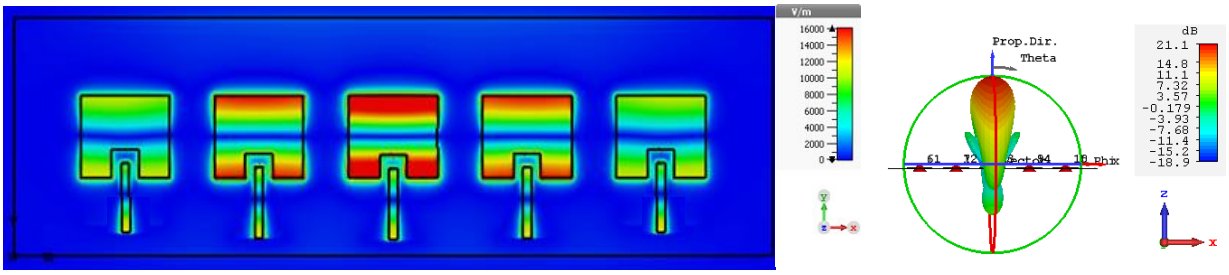
(a)



(b)

Figure 5.13: (a) Demonstration of the designed prototype and dimensions and (b) Smith chart representing the impedance response of all the array elements.

Eventually, the array element 3 is initially designed, then followed by array elements 2 and 4, and finally array elements 1 and 5. Since the desired input reactance of all the array elements is capacitive, their lengths are appropriately increased beyond the resonant length. Subsequently, the feed positions are chosen to meet the magnitude of impedances at each array elements. The impedance magnitude required for array element 3 is maximum among the array elements, which results in the corresponding feed position to be near the radiating edge. Similarly, the feed position of array elements 1 and 5 are towards the center in comparison to array elements 2 and 4, based on their impedances. To realize the planar solutions, transistors are soldered on the same layer as the patch. The array elements' edges are appropriately cut at the evaluated feed positions to accommodate the transistors and facilitate the direct integration of its drain terminal with the array elements. Subsequently, all the array elements are simultaneously excited with the desired signals and are co-optimized to realize the desired radiation pattern in the presence of mutual coupling. In this process, the feed line lengths of array elements 1 and 2 are reduced by 1 mm, compared to other array elements, to further improve the radiation pattern nulls.



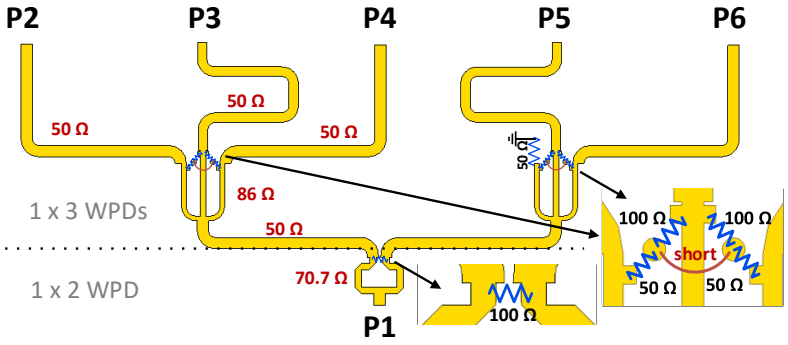
(a) (b)

Figure 5.14: Co-simulated (a) E-field distribution of the proposed prototype and (b) 3D radiation pattern of the proposed prototype.

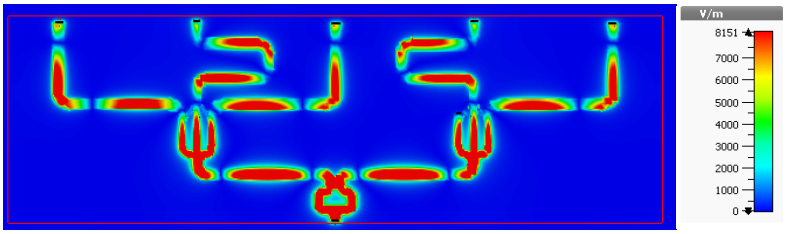
The designed prototype is thereby shown in Fig. 5.13(a), and the impedance realized at each array element is illustrated in the Smith chart as described in Fig. 5.13(b). The co-simulated E-field distribution and its 3D radiation pattern are then illustrated in Fig. 5.14(a) and 5.14(b), respectively. These results demonstrate that all the array elements are excited with equal phase as well as the desired signal amplitudes. For a constant input power excitation, an amplification gain of around 9

dB is realized through the proposed active array antenna prototype, compared to the passive counterpart. Indeed, a higher amplification and enhanced power radiation is achievable by utilizing high-power transistors.

5.6.2 Power divider



(a)



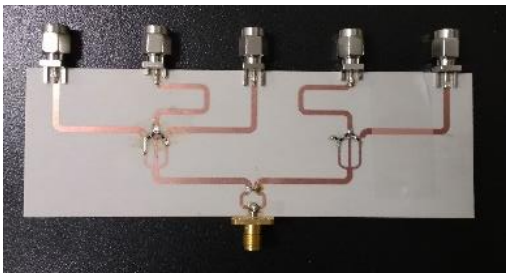
(b)

Figure 5.15: Illustration of 1 x 5 Wilkinson power divider (a) design and (b) E-field distribution.

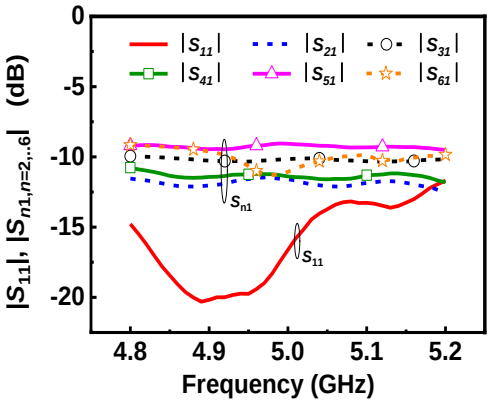
The radiation pattern of this prototype cannot be directly measured at our facility, as the multiple port excitation is not supported. Therefore, a 1x5 power divider is required to measure the prototype radiation pattern with only one input. Although different power divider configurations are available to realize this, we intend to isolate the output ports to reduce the influence of one port on another. In addition, the impedance at the output ports should be 50 Ω, which is the source impedance defined in the prototype development.

In this regard, a one input and five output (1 x 5) Wilkinson power divider (WPD) is realized by interconnecting a 1 x 2 WPD with two 1 x 3 WPDs, as shown in Fig 5.15(a). Since this integration results in a 1 x 6 power divider, one port is directly terminated with a 50 Ω load and the remaining

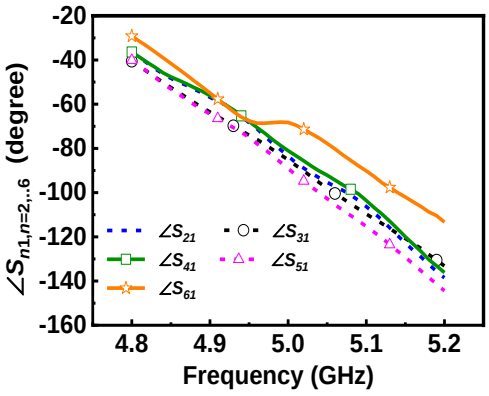
5 output ports are integrated with 50 Ω feed lines. These feed lines of equal length are organized to provide the required spacing between the output ports for direct integration with the designed active array antenna prototype. The corresponding 1 x 2 and 1 x 3 WPDs are designed by following the procedures discussed in [38] and [171], respectively. The final prototype realized and the corresponding E-field distribution are shown in Fig. 5.15(a) and Fig. 5.15(b) respectively, which demonstrate an equal magnitude and phase of the signal at its output ports.



(a)



(b)



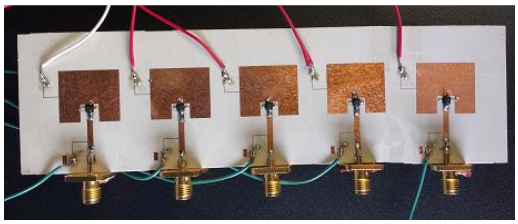
(c)

Figure 5.16: (a) Fabricated prototype, and measured (b) input matching and magnitude of power coupled from input to different ports and (c) phase of signal coupled from input to all the output ports.

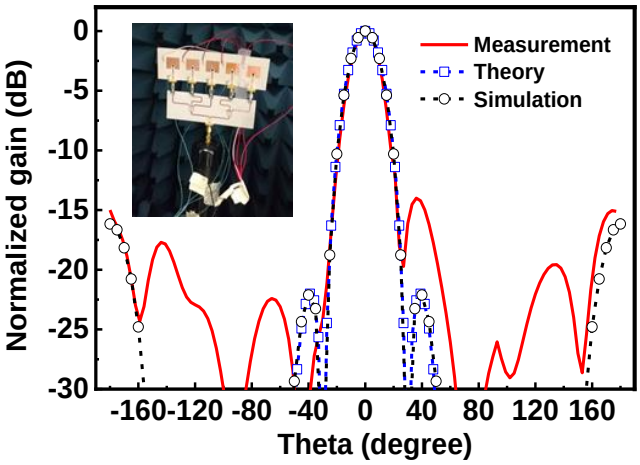
The fabricated prototype is shown in Fig. 5.16(a), where the resistors are soldered and is wire bonded for short connection in the 1 x 3 WPD. This is characterized through a multiport VNA, and the corresponding matching at the input port-1 is shown in Fig. 5.16(a). The measured magnitude and phase of signals coupled between input and output ports $S_{n1,n=2,3...6}$ of the prototype are shown in Fig. 5.16(b) and Fig. 5.16(c) respectively. Although simulations demonstrated an equal power

coupling and phase, the measurements revealed some difference in these results. This could stem from fabrications errors and/or misalignment in both soldered components and wire bonding. From the measurements, there is almost a 1.8 dB difference in the magnitude of the power coupled to the output ports, and the phase is varied by approximately 16^0.

5.6.3 Measurement



(a)



(b)

Figure 5.17: (a) Fabricated prototype and (b) comparison of normalized E-field radiation pattern results from measurements, theory and simulations.

The fabricated active array antenna prototype, as shown in Fig. 5.17(a), is integrated with the 1 x 5 WPD to measure the radiation pattern with a Satimo-starlab setup. The corresponding integrated prototype and the comparison of normalized radiation results across the H-plane are shown in Fig. 5.17(b). From measurements, the main beam and side lobe on the one side are well matched with the simulations and theoretical results, while the other side lobe is slightly dissimilar. This

difference has occurred due to the unequal signal coupled across the various ports of the 1 x 5 WPD prototype, which has been verified.

5.7 Float-top beam shifted radiation pattern

Table 5.3: Calculated and implemented signal excitations along with evaluated load impedances of each array element.

	Array Element	# 1	# 2	# 3	# 4	# 5
From Theory	Signal $\lvert S_{p21}\rvert$ $(\sqrt{W})$ ∠ angle Φ (deg.)	$1\angle 0^0$	$2.8\angle 130^0$	$4\angle 105^0$	$2.8\angle 55^0$	$1\angle -130^0$
	Power G_T (W) ∠ angle Φ (deg.)	$1\angle 0^0$	$7.84\angle 130^0$	$16\angle 105^0$	$7.84\angle 55^0$	$1\angle -130^0$
For Design	$\lvert S_{p21}\rvert$ $(\sqrt{W})\angle S_{p21}$ (deg.)	$1\angle 0^0$	$2.8\angle 105^0$	$4\angle 104^0$	$2.8\angle 117^0$	$1\angle -130^0$
	R_L (Ω)	50	13.41	39.72	20.51	50
	X_L (Ω)	0	7.62	-2.9	-39	0

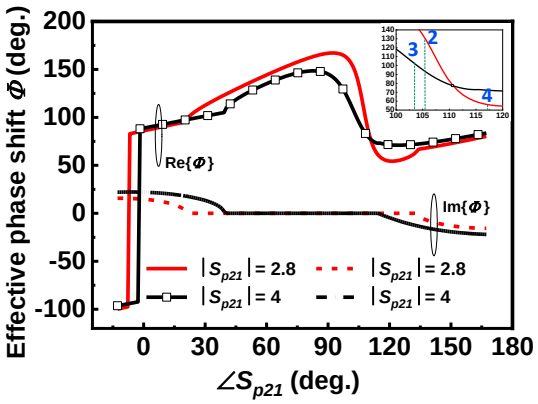


Figure 5.18: Evaluation of the phase related to the desired amplitudes.

Following a similar procedure, a 1 x 5 linear active array antenna prototype with a flat-top beam radiation from -10^0 to 30^0 is designed as another example. The targeted radiation pattern is realized by exciting each array element with the signals presented in Table 5.3. It is thereby observed that the required amplitude and phase range are large. Moreover, the desired phase range of 260^0 is not even achievable through the load impedance variation alone. In this regard, the array elements 1 and 5 (which are to be fed with the signal of magnitude 1) are directly matched and excited with the 50 Ω input source without utilizing any active device. As a result, the phase range required is

reduced to 75^0, while the amplitudes remain unchanged. The effective phase shifts realizable at the coupled signal magnitudes of 2.8 and 4 are then evaluated and plotted in Fig. 5.18. From this plot, the effective phase shifts and corresponding phases of S_{p21} can be identified at each array element. Then, the respective load impedances can be evaluated. Meanwhile, the phase shift necessary for array element 5 is achieved by extending the length of the feed line. All the relevant signal levels, phases and load impedances of array elements intended for design are presented in Table 5.3.

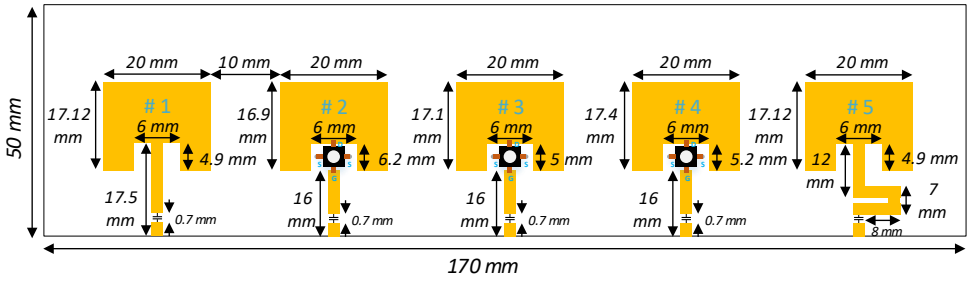
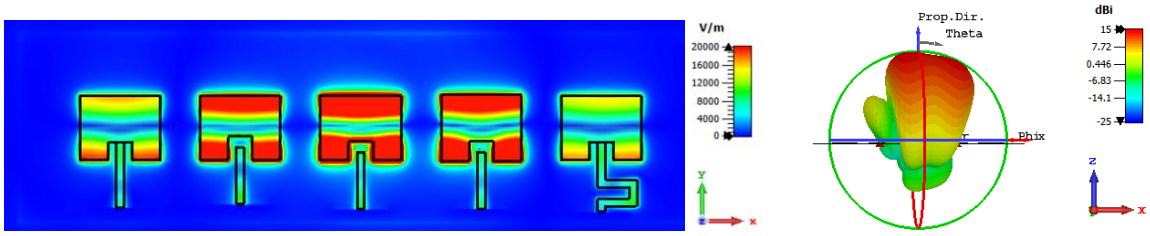


Figure 5.19: Demonstration of the prototype and dimensions.

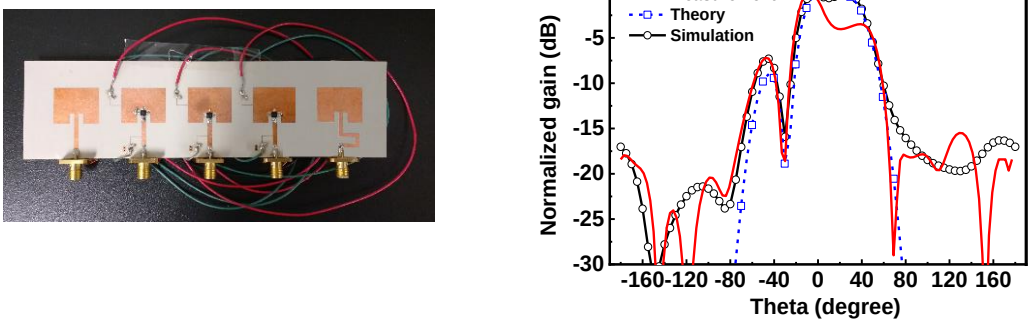


(a) (b)

Figure 5.20: Co-simulated (a) E-field distribution and (b) 3D radiation pattern of the proposed prototype.

Since the impedance desired for array elements 1 and 5 is purely resistive, their dimensions and feed positions are designed to directly match 50 Ω. The capacitive reactance required for array elements 3 and 4 necessitates them to increase their length. On the other hand, its length is decreased to realize the inductive reactance required at array element 2. From the design perspective, the array element 3 is initially designed, followed by the design of array elements 2 and 4 and finally the array elements in 1 and 5. After the initial design, all the array elements are further co-optimized to realize the desired radiation performance, and the realized prototype along with the final dimensions are shown in Fig. 5.19. The co-simulated magnitude of the E-field distribution and the corresponding radiation pattern are illustrated in Fig. 5.20(a) and Fig. 5.20(b),

respectively. This demonstrates that all the array elements are excited with the desired signals. Similar to the previous demonstration, an amplification gain of around 8 dB is realized through the proposed prototype compared to its passive counterpart.



(a) (b)

Figure 5.21: (a) Fabricated prototype and (b) comparison of normalized E-field radiation pattern results from measurements, theory and simulations.

The fabricated prototype along with the soldered components and biasing cables are shown in Fig. 5.21(a). This protoype is integrated with the 1 x 5 WPD reported in Section-5.6.2 and the radiation performance is measured. The comparision of the normalized H-plane radiation pattern from measurements, simulations, and theory is then compared in Fig. 5.21(b). Similar to the Chebyshev pattern demonstration, the right half of the radiation pattern does not match well with other results. This again originates from the differences in signal of the WPD output, which has been verified.

5.8 Conclusion

This paper provides a thorough analysis of the impact of port impedances on the magnitude and phase of the signal coupled across any two-port networks and presents an example. The closed-form equation derivation to evaluate the load impedances for a pre-defined signal coupling and the meaning of its results have been presented. Moreover, the ability of these equations to instantaneously evaluate the impedances for all phase values and phase range are also demonstrated through examples. The general modeling steps in design and interconnection of active devices with antenna are then presented for realizing beam shaping active array antennas. Following this procedure, the design and analysis of two prototypes, with one exhibiting broadside radiation with

a -20- dB side lobe level and the other with a flat-top beam shaped pattern from -10^0 to 30^0, are presented. Also, the design of a 1x5 WPD has been demonstrated, along with its measurement results. Subsequently, the integration of WPD with the active-antenna for radiation pattern measurements has been discussed. The results from these early demonstrations are satisfying and prove the concept. The derived equations and the analyses of this work become pertinent when designing efficient, compact, and low-cost unified circuit-antenna array configurations in the near future. Furthermore, two-dimensional active array antenna configurations can also be developed based on this understanding. Although, such solutions are desirable at any frequency, their implementations are most opportune in the mmW and THz frequency ranges as the losses from the matching circuitry and interconnections can be eliminated.

Appendix

The magnitude and phase range of S_{p21} can be evaluated by varying the port impedances to estimate the corresponding operating limits. For a fixed source impedance of Z_S, the output impedance looking into the port-2 is Z_{OUT} corresponding to Γ_{OUT}, as shown in Fig. 5.3. Subsequently, the maximum power transfer and equivalent maximum $|S_{p21}|$ is present when the output port is conjugate-matched with $Z_L=Z_{OUT}^*$ ($\Gamma_L=\Gamma_{OUT}^*$), whereas the minimum $|S_{p21}|$ occurs when the output is open.

When it comes to the phase component of S_{p21}, this is dependent on the current at port-2 I_2 as shown in (5.10) (when the source is fixed). The current flowing through this port is

$$-I_2 = \frac{V_{OUT}}{(Z_{OUT}+Z_L)} \tag{5.29}$$

where V_{OUT} is the signal at port-2 when $Z_L = Z_{OUT}^*$. The phase component of I_2 can then be evaluated as

$$\angle -I_2 = \angle V_{OUT} - \tan^{-1}\left(\frac{X_{OUT}+X_L}{R_{OUT}+R_L}\right) \tag{5.30}$$

Henceforth, at a fixed source impedance, the maximum phase range of S_{p21} is 180^0 by varying the load impedance, which is defined by the nature of the inverse tangent function. Furthermore, the phase center of S_{p21} is defined by the phase of V_{OUT} which remains constant for a fixed source impedance.

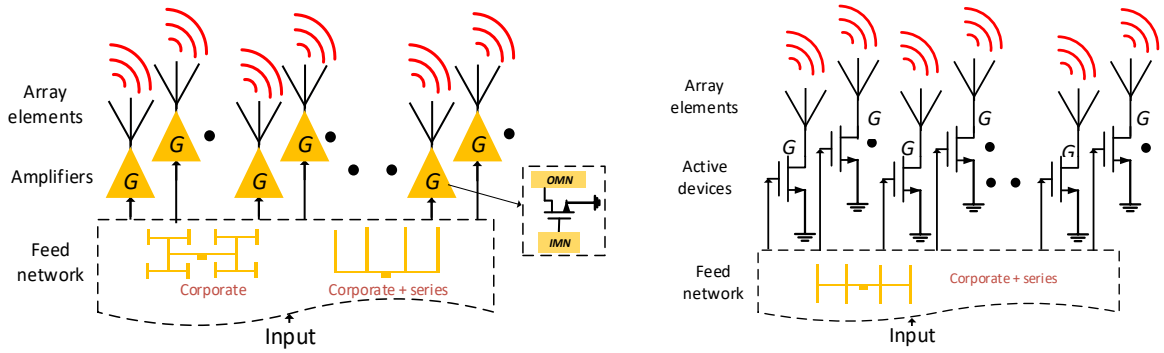
CHAPTER 6 ARTCILE 4: SCALABLE PLANAR ACTIVE ARRAY ANTENNA INTEGRATED WITH DISTRIBUTED AMPLIFYING TRANSISTORS FOR HIGH POWER APPLICATIONS

Srinaga Nikhil Nallandhigal, Nima Bayat-Makou, and Ke Wu

Submitted in the *IEEE Transactions on Microwave Theory and Techniques* on 08 Oct. 2020.

A scalable planar two-dimensional active array antenna configuration that can realize amplified radiation through co-existing active devices is proposed, studied, and demonstrated in this work. The input and output of these amplifying active devices are directly integrated with the feed network and array elements, respectively, thereby eliminating the matching networks typically required in an amplifier circuit. A comprehensive analysis of the rectangular patch antenna (RPA) performance with different feeding techniques is analyzed, and the non-radiating edge feed choice is justified not only for realizing the maximum radiation efficiency, but also for facilitating the direct active device integration. Subsequently, a physical arrangement of these array elements is devised to reduce cross-polarization. Eventually, a 4 x 2 prototype unit cell operating at 5.8 GHz is designed. Extensive analysis of active devices, optimization procedure, potential excitation signal control, and influence of faulty transistors are presented. From simulations, this active array scheme has realized a higher matching bandwidth and exhibited an amplifier gain of around 13.5 dB, compared to its passive counterpart. Subsequently, these unit cells are integrated through an equal power corporate feed network for realizing an 8 x 8 active array antenna configuration that is fabricated and measured. The measured results of the experimental prototype match reasonably well with the simulation results, thereby confirming the proposed integration technique. The resulting paralleled configuration promises the efficient handling of greater powers, making them suitable for high-power applications.

6.1 Introduction



(a) (b)

Figure 6.1: (a) Conventional/AIA frontend amplifier-array antenna integration and (b) proposed unified frontend amplifying-array antenna integration.

Millimeter wave (mmW) range deployments have the potential to meet the demands of a wide range of next-generation wireless applications that are rapidly emerging towards commercialization. The key features of higher data rates, better dimensional compactness, and increased spatial resolution of mmW frequencies along with the overcrowded lower frequency spectrum have triggered a further interest in the mmW regime[3]. On the other hand, increased path losses and significant circuitry losses are the well-known bottleneck issues over these bands [13]. In this regard, a considerable amount of research has already been instigated for realizing low-cost, compact, and efficient modules with minimum circuitry components that are capable of radiating higher power, and the antenna is no exception [172].

Although a variety of antenna configurations have been proposed for mmW applications, the planar solutions are found to be promising as they facilitate the design and integration of the entire system on the same board. In fact, mass-manufacturing techniques based on these designs are certainly possible, making them a low-cost and lightweight commercial solution. Acknowledging these capabilities, a planar arrayed antenna design is targeted in this work to increase the antenna gain, which assists in compensating the incurred free space losses to an extent[173].

In addition, a transmission of even higher power can be achieved by improving the gain of the frontend power amplifier. In a conventional approach, the power amplifier and antenna are designed independently at a reference impedance and then integrated or combined to radiate the amplified power [17, 174]. However, the effective power transmission in this case is limited due to the lower power handling capabilities of the transistors over these bands [175]. In this regard, a paralleled configuration as shown in Fig. 6.1(a), wherein the amplifiers are integrated in each array element is promising, as the input power is divided and each part is handled by a different transistor [124]. This enhances the overall power handling capabilities of the system, thereby facilitating an even greater power transmission. Furthermore, the radiated amplified power is spatially combined which is more efficient than on-board circuit power combining. And, this approach is popularly known as the spatial power combining [43, 175]. However, the increased number of passive circuitry components will result in higher circuitry losses and occupy a large area. Also, they can adversely affect the overall performances especially when they are integrated close to the radiating elements.

Therefore, it is recommended to either reduce as much as possible or to completely eliminate the maximum number of passive circuitry components, which includes matching networks, interconnections, and even feed lines. Active integrated antennas (AIAs) present an influential move in this direction, which focus on the elimination of a large number of output circuitry components, while still realizing the desired circuit and radiation functions on the same board [42, 47]. Although the AIA is rather an interesting approach, a majority of the works in literature are focused on the integration of a single independent antenna with a frontend active circuitry [51, 68, 176, 177]. Very few planar array antennas have been demonstrated by distributing individual active-antenna elements over a one-dimensional [63, 178, 179] and two-dimensional spaces [180]. However, the input circuitry is still existent in such designs which induces losses and affects the radiation performance. Recently, the complete elimination of passive circuits has been reported through a deep integration of active devices and antennas. Correspondingly, an amplifying linear series array [116, 170] and two-dimensional array configurations [181] have been demonstrated with no inter-element feed lines. Although these prototypes can be scalable, it is extremely challenging to control the amplitudes and phases of all those array elements without using feed lines.

Therefore, we intend to utilize the feed lines to have a better control over the signal exciting each array element, which can be made effortlessly scalable. Such a realization demands an unconventional feed-layout and array elements integration configuration that supports all the circuitry and bias lines on the same layer, with minimum influence on the overall performance. In fact, the widely popular feed configurations of the corporate network [40, 182] can be designed on the same layer as the antenna, though the integration of DC lines would not be feasible. Meanwhile, the hybrid feed network (with both corporate and series) [183-185] has the potential to meet the desired requirements. In utilizing the hybrid feed configuration, our interest is also to minimize the number of feed lines so to reduce their relevant losses and negative influences.

In this regard, this paper presents an approach of integrating active devices directly between the updated hybrid-feed network and array elements, which is suitable for developing two-dimensional planar and scalable active array antenna configurations[as shown in Fig. 6.1(b)]. First, the analysis of different feeding techniques of rectangular patch antenna (RPA) and the justification for non-radiation edge feed selection are discussed, followed by a proposal to reduce its inherent cross-polarization. Subsequently, the analysis of active devices and design of RPA array elements are elaborated and then integrated. Then, a 4 x 2 design example is chosen for demonstration and the corresponding feed layout is analyzed theoretically. The relevant optimization procedure, simulation results, excitation signal control, and the influence of faulty transistors are also presented. Finally, the 8x8 active array antenna design is described, along with the necessary DC biasing, fabrication challenges, and results. The concluding remarks end this paper

6.2 Rectangular patch antenna (RPA)

In this work, RPAs are chosen as the array elements of interest for demonstration, and they can be excited through different feed configurations. Among them, the co-axial probe feed and microstrip inset feed on the radiating edge are some of the well-known RPA excitation schemes, which can be realized on the same board. Nevertheless, the non-radiating edge excitation of an RPA has also been studied as an alternate feeding technique and is believed to operate like the co-axial feeding [133, 186]. However, a comprehensive analysis and comparison of the RPA performances excited through these feed configurations is still missing in the literature. And therefore, it is studied to identify an appropriate feeding technique that achieves optimum performances and also supports

the direct active device integration. For a consistent analysis, all the corresponding prototypes are designed at 5.8 GHz on Rogers 6002 of thickness 0.762 mm, and the necessary simulations are performed in the CST-MWS platform.

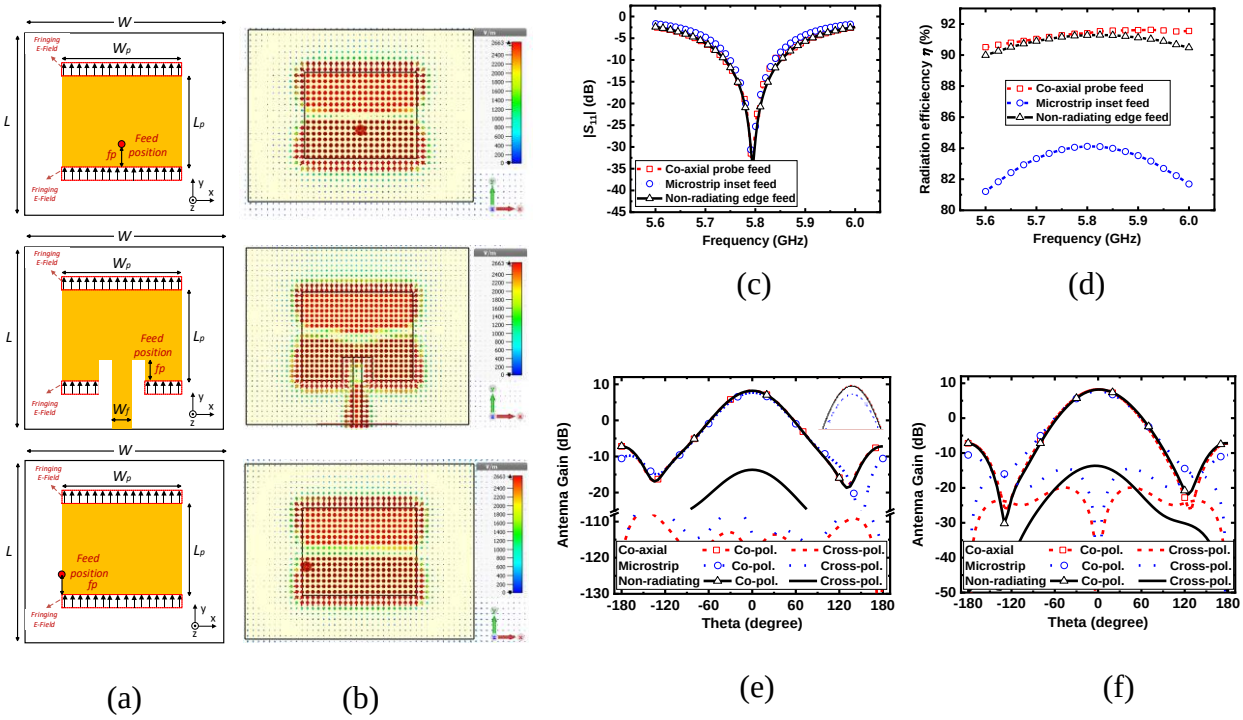


Figure 6.2: Rectangular patch antenna; L = 34.4 mm, W = 44 mm, W_p = 19.5 mm (a) co-axial feed; L_p = 14.3 mm and fp= 4.2 mm, microstrip feed L_p = 14.7 mm, fp=4.2 mm, W_f = 1.9 mm and non-radiating edge feed L_p = 14.2 mm and fp=4.2 mm; (b) illustration of corresponding E-field distributions; comparison of (c) impedance matching (d) radiation efficiency (e) E-plane radiation pattern and (f) H-plane radiation pattern.

The designed RPAs with co-axial, microstrip and non-radiating edge feeding techniques are shown in Fig. 6.2(a), and their E-field distributions are plotted in Fig. 6.2(b). Their matching responses are compared in Fig. 6.2(c), which demonstrate an approximately similar performance. However, the radiation efficiency of the microstrip inset-fed RPA is lower than the other two feeding mechanisms as shown in Fig. 6.2(d). The inset cut etched on the RPA radiating edge reduces its effective radiating area, which results in a decrease of its radiation efficiency. On the other hand, the co-axial feeding and microstrip inset feed are set to excite the pure TM_{01} mode in the RPA, thus

resulting in very low cross-polarization along the broadside in both E-plane and H-plane as shown in Fig. 6.2(e) and Fig. 6.2(f), respectively. However, the non-radiating edge-fed RPA excites the modes along the length (TM_{01}) as well as across the width (TM_{10}). This leads to a relatively higher cross-polarization for non-radiating edge-fed RPA in comparison to others, as shown in Fig. 6.2(e) and Fig. 6.2(f).

The co-axial probe excitation of RPA is not a purely planar solution, and also results in a higher input inductance when implemented on thick substrates which are typically desired for efficient antennas [187]. While, the microstrip inset feed has a lower radiation efficiency, which will worsen in the mmW range as the feed size becomes comparable to the width of RPA [34, 100]. To tackle the drawbacks of these feeding techniques and to achieve a higher radiation efficiency together with a planar solution supporting a direct active device integration, the non-radiating edge feed excitation is chosen as the appropriate feeding technique in this work.

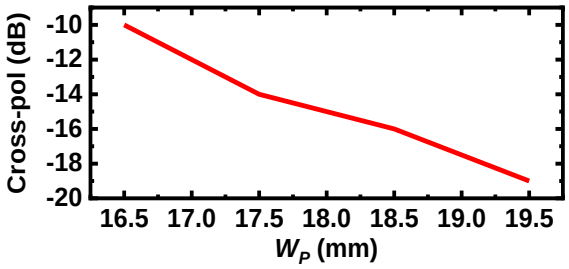


Figure 6.3: Cross-polarization variation along broadside with respect to non-radiating edge-fed RPA width W_P modification.

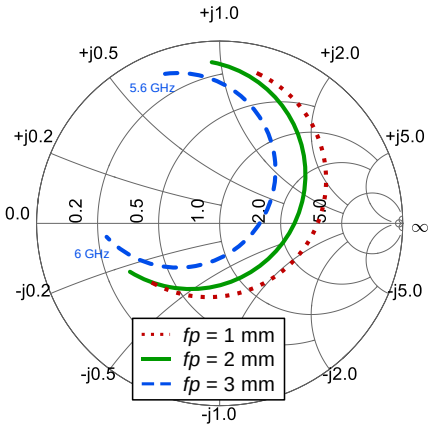


Figure 6.4: Impedance response of non-radiating edge-fed RPA with feed position *fp* variation.

In the non-radiating edge-fed RPA, the RPA width has a potential to control the cross-polarization level [188]. Therefore, this has been initially analyzed for the designed RPA, and the corresponding result is shown in Fig. 6.3. This demonstrates that an increase in RPA width will lower the cross-polarization level in the range of analysis, where the radiation efficiency varies by less than 0.5 %. From this analysis, the RPA width is chosen to be 19.5 mm, such that the cross-polarization is around -20 dB. Besides, the impedance response of the designed non-radiating edge-fed RPA with variation in feed position *fp* has been analyzed, and the corresponding result is plotted in the Smith chart as described in Fig. 6.4.

6.2.1 Cross polarization reduction technique

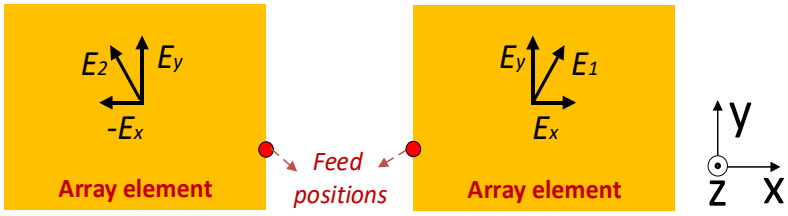


Figure 6.5: Illustration of the physical arrangement of the non-radiating edge-fed RPA array elements to reduce the cross-polarization along E-plane.

If a single non-radiating edge-fed RPA is desired for a given application, the cross-polarization level along the E-plane can be significantly reduced through a differential excitation [189]. However, the 180^0 phase shift required between the two excitations is rather difficult to realize in array configurations, considering the complexity of feed networks. In addition, the spacing between the two differential excitation ports might not be enough to directly integrate the commercial transistors in active array antenna configurations. Therefore, a simple arrangement of single-feed non-radiating edge-fed RPA array elements is proposed, as shown in Fig. 6.5, to realize a substantially lower cross-polarization without affecting other performance parameters. This behavior can be explained from the radiating E-field of these array elements as shown in Fig. 6.5. Here, the array element 1 and element 2 have the E-field distribution as $\vec{E}_1$ and $\vec{E}_2$ respectively excited by their feeds. Each of these fields can be divided into two vector components as

$$\vec{E}_1 = E_x\hat{x} + E_y\hat{y} \text{ and } \vec{E}_2 = -E_x\hat{x} + E_y\hat{y} \tag{6.1}$$

Subsequently, the effective E-field radiating due to both the array elements in phase is

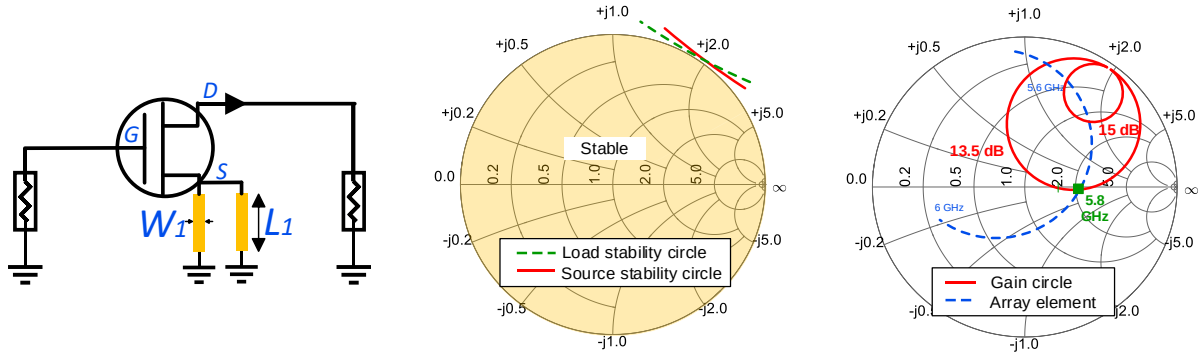
$$\vec{E}_{total} = E_1 + E_2 = 2E_y\hat{y} \tag{6.2}$$

which illustrates the complete elimination of cross-polarized component E_x along the E-plane. Henceforth, this arrangement of array elements is utilized in this work.

6.3 4 x 2 active array antenna

This section describes the development and analysis of a 4 x 2 active array antenna utilizing the cross-polarization reduction arrangement of array elements. These unit cells are eventually utilized in the design of an 8 x 8 active array antenna.

6.3.1 Transistor analysis



(a) (b) (c)

Figure 6.6: (a) Schematic utilized in ADS for transistor analysis; Smith chart representing the (b) source and load stability circles along with the stable region highlighted and (c) power gain circles of the transistor and impedance response of the non-radiating edge-fed RPA array element.

Commercially available transistors FET-CE3512K2 are chosen for this prototype demonstration and are DC-biased with a gate voltage V_{GS} = -0.2 V and a drain voltage V_{DS} = 2 V for the common source class-A amplifier operation. Indeed, it is recommended to stabilize the transistors in amplifier operations to avoid any potential instability caused by mutual coupling, fabrication errors, and soldering differences in practical implementations. Since these transistors are intended

to be soldered on the same layer as the antenna, metalized vias are utilized to ground their source terminals. Although, the diameter of these vias can be appropriately decreased to stabilize the transistor [170], our fabrication facility imposes a limit on the minimum via diameter realizable to a half of the substrate thickness. As a result, the minimum via of diameter d=0.381 mm is chosen, and the stability is then analyzed. The corresponding stability factor K=0.759 and stability measure B=1.014 demonstrate that it is still potentially unstable. Therefore, additional microstrip lines with length L_1=1.5 mm and width W_1=1 mm are utilized to unconditionally stabilize the transistor, as shown in Fig. 6.6(a). Subsequently, the stabilized transistor has a stability factor K=1.017 > 1 and a stability measure B=0.757 > 0 at the design frequency of 5.8 GHz. For reference, the resultant stability circles are drawn in the Smith chart of Fig. 6.6(b), and the stable region is highlighted, which includes the entire Smith chart as $|S_{11}| = 0.73 < 0$ and $|S_{22}| = 0.485 < 0$ at its center.

The constant power gain circles of transistors are then drawn in the Smith chart of Fig. 6.6(c) to identify the potential impedances that can achieve the desired amplification gain. Eventually, the RPA array elements are designed to realize the impedance specified on the gain circle for direct integration of the transistor drain terminal, thereby eliminating the requirement of an output matching network.

6.3.2 Array elements

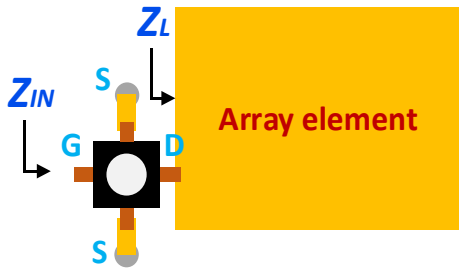


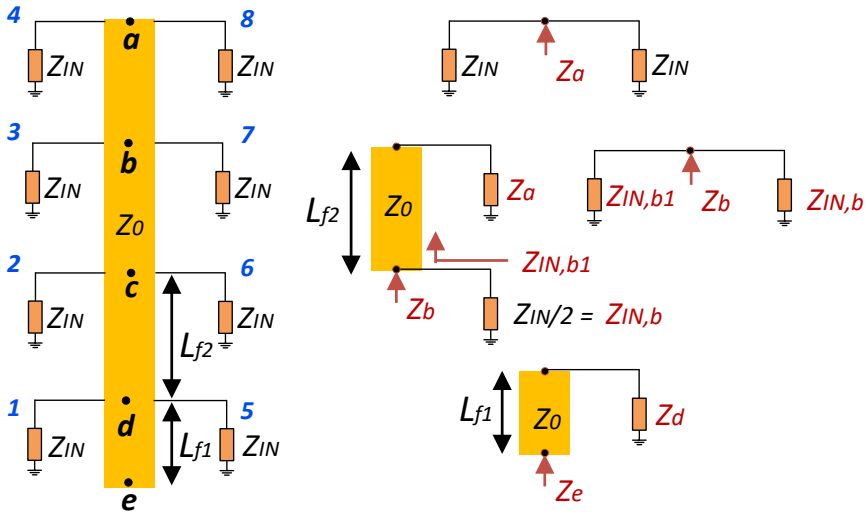
Figure 6.7: Illustration of load impedance Z_L of the antenna and input impedance Z_{IN} at the gate terminal of a loaded transistor.

The RPA offers the design flexibility in varying its dimensions and feed positions to realize a wide range of impedances, with a minimal compromise in radiation efficiency [116]. Tuning its length L_p will facilitate a control on the reactance term of the RPA input impedance, while the feed

position *fp* can be varied to modify the magnitude of input impedance. Subsequently, its length and feed position can be simultaneously adjusted to realize a number of desired impedances. For our prototype development in this work, the non-radiating edge-fed RPA dimensions are unchanged from the reported resonant values in Fig. 6.2(a) (although they can be varied for other designs). However, only the feed position *fp* is tuned to be 2 mm such that the corresponding impedance Z_L = 120 Ω at 5.8 GHz overlaps with the 13.5 dB gain circle as shown in Fig. 6.6(c), which is the targeted amplification gain for demonstration.

The drain terminal of the transistor is then directly integrated with the designed RPA at this feed position, and the input impedance Z_{IN} at the gate terminals is evaluated as Z_{IN}=47.5-j72 Ω. The array element and active device integration along with the load impedance Z_L and input impedance Z_{IN} are further illustrated in Fig. 6.7, for reference. As such, an appropriate feed network is desired to integrate these transistor-loaded RPAs in an array configuration.

6.3.3 Feed network



(a) (b)

Figure 6.8: (a) Illustration of feed network and (b) equivalent circuit of impedances calculation at various positions.

To reduce the cross-polarization signal, we intend to arrange the array elements as shown in Fig. 6.5. Correspondingly, the feed network proposed for the 4 x 2 active array antenna configuration is shown in Fig. 6.8(a). Here, the gate terminal of each transistor (loaded with an array element at its drain terminal) is integrated with the feed network. Therefore, their equivalent impedances Z_{IN} at the gate terminals represent the array elements integration positions. Since the entire array elements are intended to be designed for the same load impedance Z_L, it is assumed that the input impedance at each of the corresponding gate terminals Z_{IN} is also equal. However, this might not be the case in practical implementation because of mutual coupling.

The spacing L_{f2} between these array elements integration positions *a*, *b*, *c*, *d* is then chosen to be around λ_g to excite all of them in phase and realize broadside radiation. After this, the impedance observed at the input of feed network *d* has to be evaluated to design an appropriate impedance matching network for maximum power coupling with the circuitry integrated before it.

Indeed, an initial estimation of the impedance at node *d* can be evaluated through a theoretical approach. For this, the impedances are evaluated starting from the open edge terminal *a*, followed by nodes *b*, *c* and finally at the input terminal *d*. At position *a*, as shown in Fig. 6.8(b), the two impedances Z_{IN}, corresponding to array elements 4 and 8, operate in a paralleled configuration, resulting in the effective impedance at this node as

$$Z_a = \frac{Z_{IN}}{2} \tag{6.3}$$

Similarly, the impedance due to the only array elements 3 and 7 integrated at node *b* is also given by

$$Z_{IN,b} = \frac{Z_{IN}}{2} \tag{6.4}$$

In addition, the impedance at node *a* Z_a also loads the node *b*. The corresponding additional impedance at node *b* due to the presence of impedances at node *a* can be evaluated from the transmission line input impedance equation [38]:

$$Z_{IN,b1} = Z_0 \frac{Z_a + jZ_0(tan(\beta_g L_{f2}))}{Z_0 + jZ_a(tan(\beta_g L_{f2}))} \tag{6.5}$$

Subsequently, the effective impedance at node *b* is the parallel of these two impedances as shown in Fig.6 8(b):

$$Z_b = Z_{IN,b} || Z_{IN,b1} = \frac{Z_{IN}}{2} || \, Z_0 \frac{Z_a + jZ_0(tan(\beta_g L_{f2}))}{Z_0 + jZ_a(tan(\beta_g L_{f2}))} \tag{6.6}$$

Substituting L_{f2} as λ_g spacing in (6.6) for the intended broadside radiation, the resultant impedance at node b is evaluated as

$$Z_b = \frac{Z_{IN}}{2} || \, Z_a = \frac{Z_{IN}}{4} \tag{6.7}$$

Following a similar procedure, the impedances at node *c* and node *d* can be evaluated as

$$Z_c = \frac{Z_{IN}}{6}, Z_d = \frac{Z_{IN}}{8} \tag{6.8}$$

If the impedance at node *d* Z_d is complex, the feed line length can be extended to transform it into the real impedance R_d at node *e*. To theoretically estimate this, the equation to calculate the input impedance of a transmission line is utilized as follows:

$$Z_e = Z_0 \frac{Z_d + jZ_0(tan(\beta_g L_{f1}))}{Z_0 + jZ_d(tan(\beta_g L_{f1}))} = R_d \tag{6.9}$$

Then, it is re-arranged to evaluate the desired extension length L_{f1}:

$$L_{f1} \cong \left| \frac{1}{\beta_g} \tan^{-1} \left(\frac{R_0^2 - X_d^2 - R_d^2 \pm \sqrt{\left(R_0^2 - X_d^2 - R_d^2\right)^2 + 4R_0^2 X_d^2}}{2R_0 X_d} \right) \right| \tag{6.10}$$

This equation can instantly provide two solutions, and they are verified to be separated by a quarter wavelength. However, the lower length of transmission line extension L_{f1} is recommended to reduce the corresponding circuitry losses. Eventually, a quarter wavelength impedance transformer with dimensions L_f and W_f can transform R_d at node *e* to any other real impedance.

It should be noted that all the equations utilized and their corresponding derivations do not include any losses or coupling between various ports. As a result, the evaluated results provide only an initial estimation of the impedances and dimensions, while an overall optimization is still mandatory.

6.3.4 Co-simulation

The antenna designs were carried out in the CST-MWS 3D simulation platform, with a waveguide port integrated at the input and discrete ports at the transistor integration terminals. After the

simulations, the S-parameter model of the designed antenna is exported to the ADS-schematic platform and co-simulated with the transistor model to analyze the circuitry functions. Also, the co-simulated field distribution and radiation performance of the prototype are evaluated in the CST-schematic by utilizing the transistor model along with the designed antenna.

6.3.5 Design example

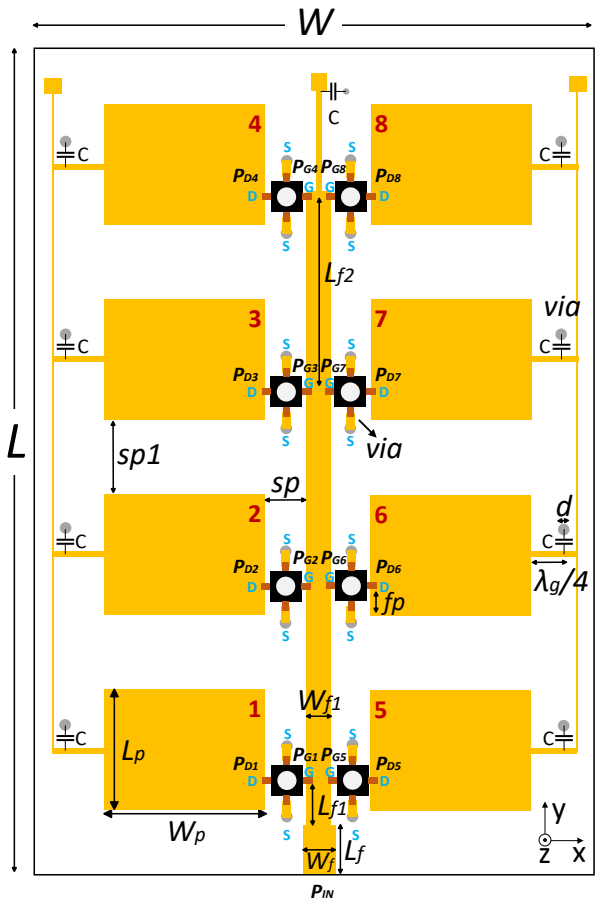


Figure 6.9: Illustration of 4 x 2 active array antenna prototype; L= 125 mm, W= 80 mm, L_p= 14.2 mm, W_p=19.5 mm, fp=2 mm, W_{f1}=1.92 mm, L_{f1}= 1.2 mm, L_{f2}=31 mm, W_f = 6 mm, L_f = 7.5 mm, d=0.762 mm, C=100 pF, sp=4 mm, $sp1$= 16.84 mm.

In our design example, the gate terminals of all array elements with an input impedance Z_{IN}=47.5-j72 Ω are appropriately integrated with the 50 Ω microstrip feed line of width W_{f1}=1.92 mm. The realized 4 x 2 active array configuration is thereby shown in Fig. 6.9, where both the feed and DC

bias lines have minimal influence on the overall performance as they are aligned along the non-radiating edge of the RPA. Furthermore, this configuration requires a less number of feedlines than in the corporate and hybrid feeding networks, and thereby the feed line losses are also reduced. At a wavelength spacing between the array elements $L_{f2}=\lambda_g$= 33 mm, the effective impedance at node *d* is Z_d = 6-j9 Ω from (6.8). Subsequently, the microstrip line extension of length L_{f1} = 0.9 mm calculated from (6.10) will transform the complex impedance at node *d* Z_d to a real impedance R_d =6 Ω at node *e*.

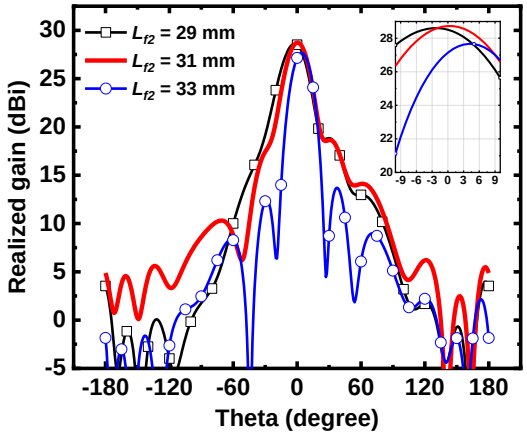


Figure 6.10: Co-polarized E-plane field distribution varying the inter-element spacing L_{f2}.

Table 6.1: Amplitude and phase exciting each array element of the prototype at various inter-element spacing L_{f2}.

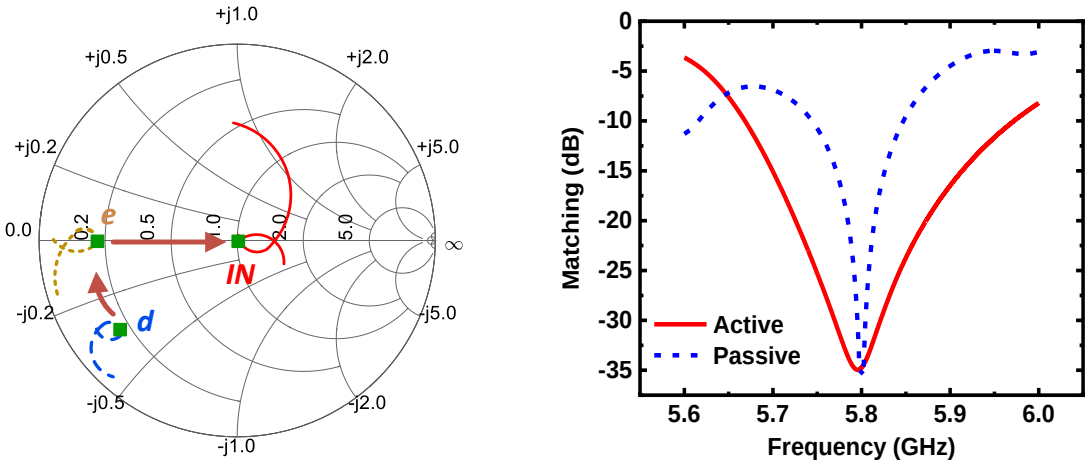
L_{f2} (mm)	Amplitude (V)				Phase (degree)			
	#1, 5	#2, 6	#3, 7	#4, 8	#1, 5	#2, 6	#3, 7	#4, 8
29	4.5	3.2	1.6	1	116^0	132^0	151^0	153^0
31	4	3	1.5	1	11^0	10^0	10^0	5^0
33	2.1	2	2	1.9	117^0	105^0	91^0	68^0

With this guided wavelength spacing λ_g between array elements, the radiation performance along the E-plane has been analyzed, and the corresponding result is shown in Fig. 6.10. The resultant offset radiation implies that the array elements are excited with a phase delay. Therefore, the spacing between array elements has to be decreased to excite them in phase. In this regard, the

radiation pattern responses are analyzed while decreasing the inter-element spacing, and these results are given in Fig. 6.10. From this analysis, it is observed that the radiation is along the broadside at the inter-element spacing of L_{f2}= 31 mm. Moreover, the absolute magnitude and phase of signal exciting each array elements are estimated from the E-field distribution, for all the cases studied. The corresponding results are shown in Table 6.1, which verifies the radiation patterns observed.

Table 6.2: Input power and power lost in prototype with variation in inter-element spacing L_{f2}.

L_{f2} (mm)	**29**	**31**	**33**
Input power P_{IN} (dBm)	0	0	0
Power lost P_{IN} - P_G (dBm)	-1.2	-0.5	-1.8



(a) (b)

Figure 6.11: (a) Smith chart representing the impedance transformation at various stages of the feed, and impedance matching at the input and (b) comparison of the simulated active array antenna and passive-array antenna matching performances.

In a typical common source amplifier circuit, the input and output matching networks are respectively designed at the gate and drain terminals of the transistor to couple the maximum power. In the proposed configuration, the output-matching network is eliminated and the desired

impedance is directly realized through the designed RPA. Similarly, we intend to absorb the input matching networks within the feed lines by integrating the gate terminal of each transistors directly at appropriate positions. Therefore, the prototype has also been optimized to couple the maximum input power P_{IN} fed into it with the gate terminals of all the transistors P_G. In this regard, the parameter analyzed is the power lost, which is defined as

$$Power\ lost = P_{IN} - P_G; where\ P_G = \sum_{n=1}^{8} P_{Gn} \tag{6.11}$$

where the corresponding variables are illustrated in Fig. 6.9. To analyze this, all the designed prototypes with variation in inter-element spacing are initially matched with the source, and the power lost through them is calculated. The relevant results shown in Table 6.2 illustrate that the power lost is minimal at the inter-element spacing when the active array radiates along the broadside. As a result, the L_{f2} spacing of 31 mm between array elements is fixed for the design of the active array antenna prototype.

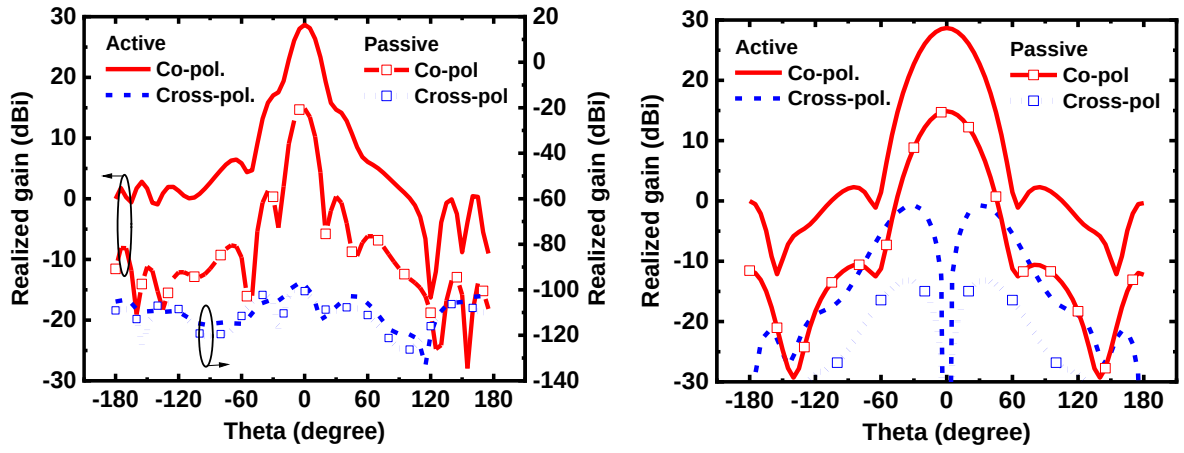
At this inter-element spacing, the impedance at node *d* from simulations is Z_d = 9-j13 Ω. And, to transform this impedance Z_d to a real impedance R_d, the microstrip line extension required is L_{f1}= 1.25 mm, which is calculated in (6.10). This is very close to the simulated value of L_{f1}= 1.2 mm. Subsequently, a quarter wavelength transmission line with a width of 6 mm and a length of 7.5 mm can match this impedance R_d =R_e = 9 Ω to 50 Ω to facilitate the measurements with the standard lab equipment. Moreover, the impedance transformation at the feed positions *d*, *e* and the input of the designed prototype are shown in the Smith chart in Fig. 6.11(a) for reference.

With this layout arrangement, the array elements in the E-Plane and H-Plane are separated by $0.58\lambda_0$ and $0.23\lambda_0$, respectively. And, the mutual coupling is evaluated to be less than -24 dB along both planes, which will help, to an extent, in the independent design of the array elements.

In operation, the input power fed into this prototype is divided into eight parts, and each part is coupled with the gate terminals of different transistors. These transistors perform the amplification and directly excites the array elements, which then radiate into space and spatially combine. As a result of the paralleled configuration, the overhead voltage problems and power dissipation of the transistors are reduced, while the efficiency, linearity, and power handling capabilities are improved [181]. Also, the spatial power combining is more efficient than the equivalent on-board circuitry. All these features are attractive for emerging mmW applications and beyond.

6.3.6 Simulated results

Besides, a passive 4 x 2 prototype has also been developed with a similar layout to compare its results with the designed active array antenna configuration. The matching responses of the developed active array antenna and passive-array antenna prototypes are compared in Fig. 6.11(b). Although these two prototypes are matched at the design frequency, the matching bandwidth achieved in the active array antenna configuration is wider than its passive counterpart.

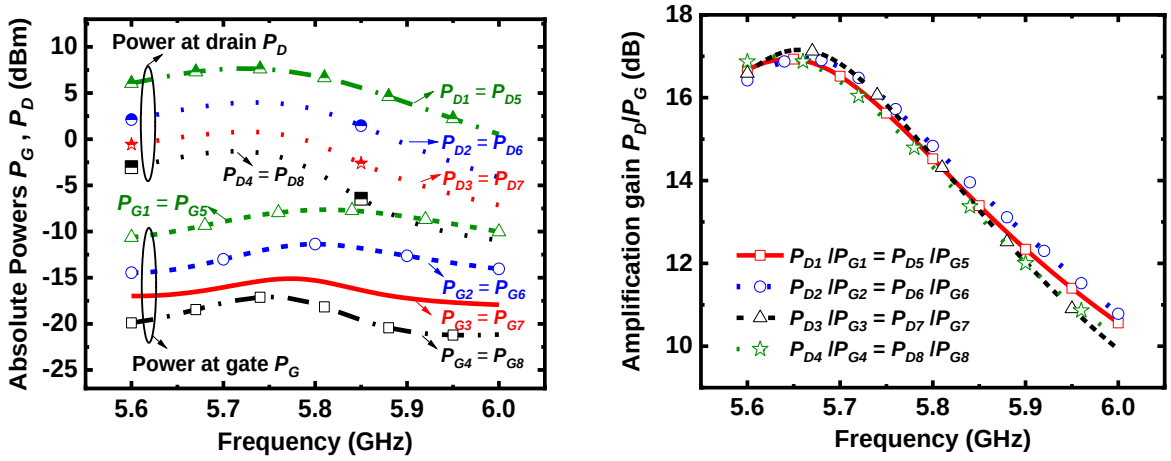


(a) (b)

Figure 6.12: Comparison of the co-simulated 4 x 2 active and passive array antennas radiation patterns along (a) E-plane and (b) H-plane.

The radiation performances along E-plane and H-plane of the co-simulated active and passive array antennas are compared in Fig. 6.12(a) and 6.12(b), respectively. As per the design, these results illustrates the broadside radiation, and the cross-polarization level along the E-plane is lower than -100 dB. The realized gain of these two prototypes is plotted in these graphs, and the difference is the amplification gain achieved through the integration of transistors. From these results, the realized gain of the active array prototype is around 28.7 dBi in comparison to the 15.1 dBi achieved in the passive counterpart. This implies that the amplification gain exhibited through the integrated transistors is around 13.6 dB, which is close to the designed amplification gain of 13.5 dB. For reference, the definition of realized gain and its ability to measure the transistor gain are discussed in [181]. If desired, the amplification gain can be further enhanced by integrating

multiple transistors in cascade or by utilizing high power transistors at each array element. Since eight transistors in parallel handle a part of the total input power, the power handling capability of this prototype is also improved. Moreover, the radiation efficiency is around 90 % in both the passive and active configurations, which is calculated as the total power radiated upon power accepted by all the array elements.



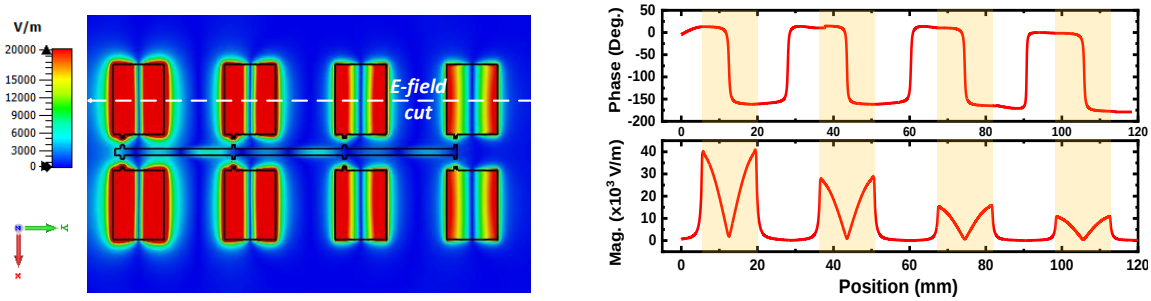
(a) (b)

Figure 6.13: Co-simulated results of 4 x 2 active array antenna (a) absolute powers at all the transistor integration ports and (b) amplification gain across each transistor.

Furthermore, the absolute powers present at all the gate and drain terminals of the transistors are analyzed and presented in Fig. 6.13(a). These results coincide with the respective signal levels reported in Table 6.1. The amplification gain across each transistor is the same as shown in Fig. 6.13(b), which is calculated as the difference in power at drain and gate terminals of the same transistor. It can also be observed that the amplification gain at 5.65 GHz is larger than the amplification gain at the design frequency, as the impedance at 5.65 GHz overlaps with a higher gain circle compared to the impedance at the design frequency of 5.8 GHz. Nevertheless, we can also decrease the RPA length so that the corresponding impedance overlaps with a higher gain circle, resulting in an improved gain at the design frequency.

Lastly, the co-simulated E-field distribution of the active array prototype is demonstrated in Fig. 6.14(a). Besides, the variation of the E-field in the substrate [at the cut shown in Fig. 6.14(a)] is

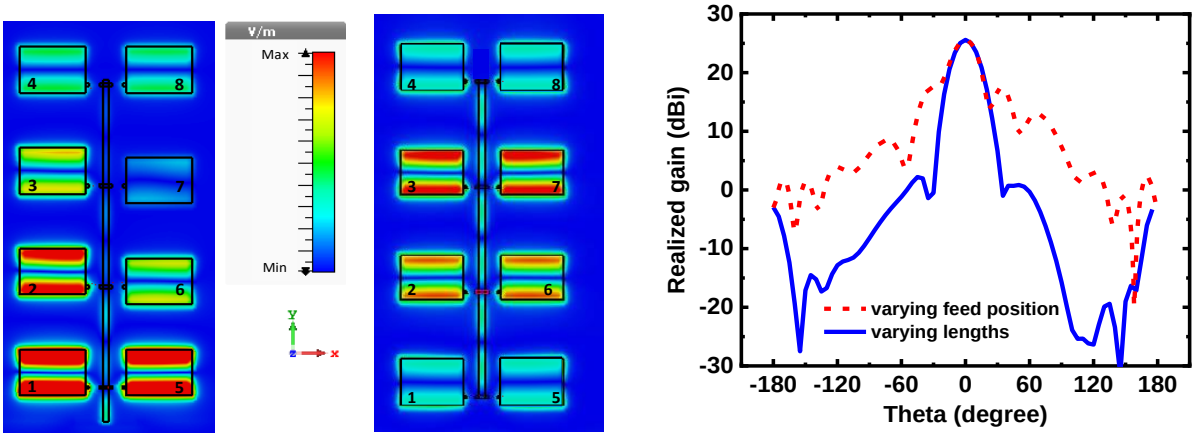
analyzed, and the corresponding phase and magnitude components are illustrated in Fig. 6.14(b). Also, the field distribution at the array element positions are highlighted. From this, we can observe that the phase distribution of the array elements is approximately equal and results in broadside radiation. However, the magnitude component of the array elements decreases as we move farther from the input excitation, which explains the unsymmetrical sidelobe levels observed in the E-plane radiation pattern.



(a) (b)

Figure 6.14: Co-simulated (a) E-field distribution of 4x2 active array antenna and (b) magnitude and phase distribution of E-field component across the cut.

6.3.7 Amplitude control



(a) (b) (c)

Figure 6.15: Co-simulated E-field distribution of proposed configuration while modifying the array elements (a) feed positions, (b) lengths and (c) corresponding radiation patterns.

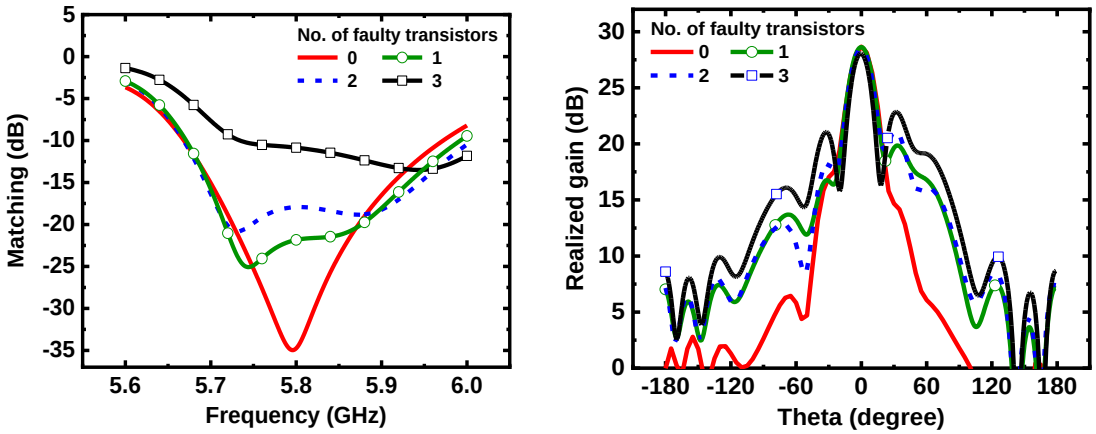
Since the input signal varies along the feed line, the magnitude and phase of the signal, which couple with the array elements also differs based on their integration positions. It is thereby evident that the array elements can be integrated at discrete locations of the feed line to vary the excitations of the array elements and potentially realize an application-specific radiation pattern.

Moreover, the transistor integration provides an additional flexibility in controlling the excitation of each array element. In this context, we can choose distinct lengths L_p and excitation positions *fp* for each array element, and, thereby, integrating transistors will result in a different amplitude and phase exciting each of them. For example, the feed positions *fp* of the array elements 6 and 7 are tuned to be closer to the center at *fp*=3 mm, which results in a lower input impedances for these RPAs. As a result, these impedances overlaps with the lower gain circle of the transistor, resulting in a reduced amplification gain realized at these array elements. The corresponding E-field distribution and radiation pattern along the E-plane are shown in Fig. 6.15(a) and Fig. 6.15(c) respectively, for reference.

Alternatively, the lengths of the array elements have been modified with the excitation positions fixed at *fp*=2 mm. For demonstration, the array elements at the center are chosen to achieve higher amplification and the outer array elements to have lower gain so that a low sidelobe level radiation performance is achieved. This is realized by increasing the length of the array elements 1 and 5 and slightly decreasing the length of array elements 3.7 and 4,8. The corresponding E-field distribution is illustrated in Fig. 6.15(b), and its radiation performance along the E-plane is shown in Fig. 6.15(c), which confirms the desired response.

6.3.8 Faulty transistors

In contrast to the identical operation of all the transistors utilized in simulations, their individual operation is generally distinct in practical implementations. This difference in operation might stem from the commercial transistor itself or from other reasons like fabrication errors and soldering mismatches. In a worst-case scenario, it is also possible that the electrostatic-sensitive transistors chosen for integration may breakdown when mishandled or even turn out to be faulty.



(a) (b)

Figure 6.16: Simulated results of 4 x 2 active array antenna by varying the number of faulty transistors (a) matching performance and (b) co-polarized E-plane radiation performance.

In this regard, the impact of faulty/malfunctioning transistors on the operation of the prototype is analyzed from simulations. To analyze this, the transistors at arbitrary locations are removed one by one, and the corresponding matching responses and radiation patterns along the E-plane are simulated and plotted in Fig. 6.16(a) and Fig. 6.16(b), respectively. From a matching point of view, this configuration can support up to 3 faulty transistors while the prototype array remains matched. On the other hand, the radiation pattern is always along the broadside. In addition, the realized gain is approximately constant in all the cases, as the array elements are excited in the paralleled configuration. However, the sidelobe level increases proportionally with the number of faulty transistors.

6.4 8 x 8 active antenna array

The designed 4 x 2 active array antenna cells are then interconnected through a one-input and eight-output corporate feed network, forming an 8 x 8 active array antenna as shown in Fig. 6.17. Since a detailed analysis of the unit cell has already been presented, this section focusses only on the corresponding corporate feeding network, DC biasing, and fabrication challenges followed by their measurement results and discussion.

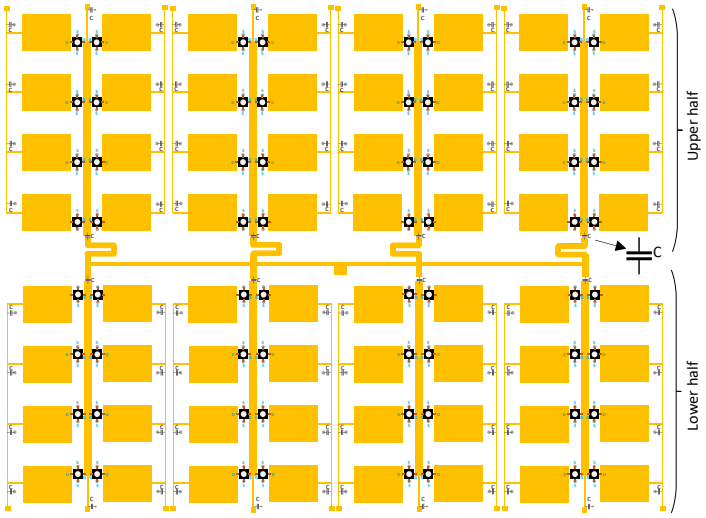
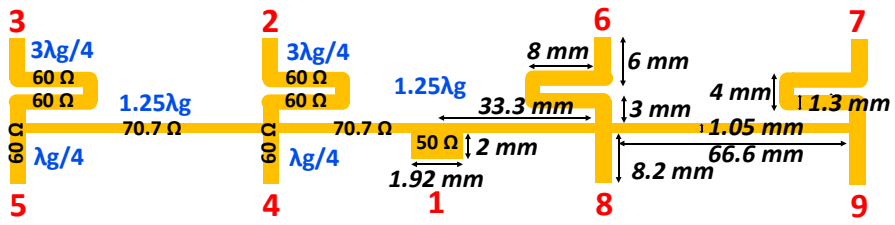
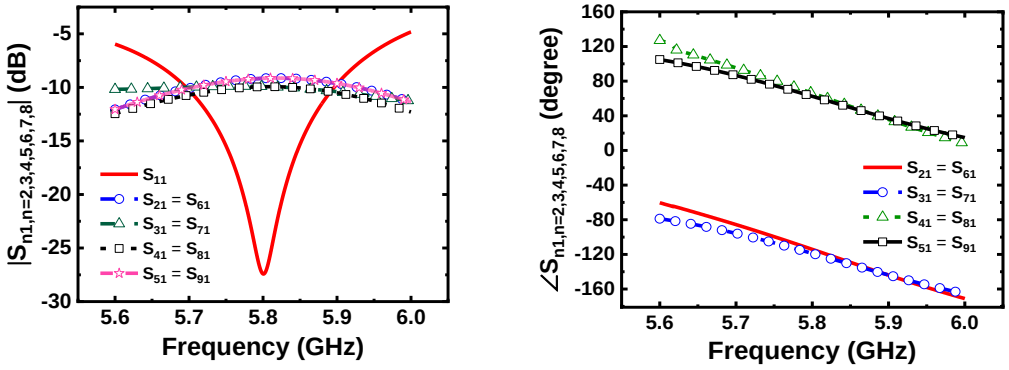


Figure 6.17: Illustration of the designed 8 x 8 amplifying active array antenna.

6.4.1 Corporate feeding network



(a)



(b) (c)

Figure 6.18: (a) Designed corporate feed layout demonstrating the microstrip line impedances and dimensions (b) input port matching and coupling magnitude at each output port in reference to input and (c) coupling phase at each output port with respect to input.

As illustrated in Fig. 6.17, the 4 x 2 unit cells integrated on the upper half and lower half of the developed prototype are mirror images. In this case, an equal phase output corporate feed network will excite the lower and upper section of the array elements in 180^0 out-of-phase, resulting in non-broadside radiation. Therefore, the introduction of the 180^0 phase difference in the corporate feed network is inevitable in either the upper half or lower half of the array to ensure broadside radiation. Keeping this in mind, the corporate feeding network is designed for equal power division as shown in Fig. 6.18(a), and the delay lines are introduced on the upper half to realize the desired phase difference. It is designed such that the input port 1 is matched with 50 Ω when the output ports 2-9 are perhaps loaded with impedance $R_e = 9$ Ω existent from the integrated 4 x 2 unit cells. All the corresponding impedances, port locations, and dimensions related to this feed network are further illustrated in Fig. 6.18(a).

The simulated results of input matching and magnitude of power coupled from input to output ports are plotted in Fig. 6.18(b), which confirm that all the array elements are excited with approximately equal power signals. And, the phase of signal coupled from input to output ports is illustrated in Fig. 6.18(c), which demonstrates the desired 180^0 out-of-phase at ports 2, 3, 6 and 7 compared to ports at 4, 5, 8 and 9. In fact, a variable phase shifter can be also be utilized instead of delay lines, which will serve the purpose and also facilities the beam steering functionalities as desired by the given application.

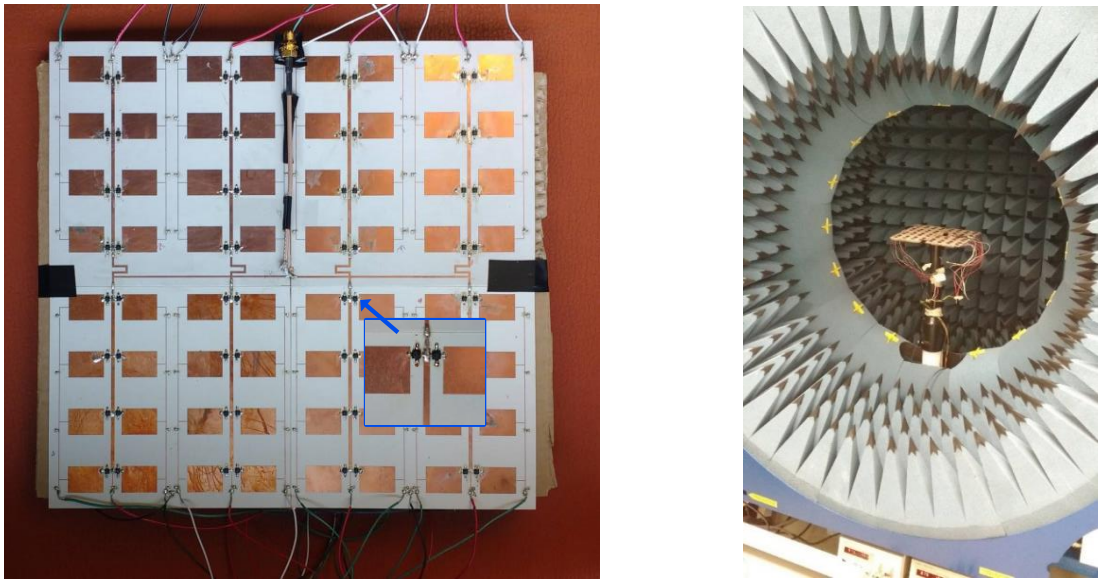
6.4.2 DC biasing

The proposed layout facilitates the installation of all DC lines on the same layer as the RPA. They are arranged between the array elements and are oriented along the non-radiating edge of the RPA, thereby minimizing its influence on the array antenna performance. Here, the quarter wavelength short-circuited microstrip lines are designed as DC bias lines. The drain bias lines are integrated at the minimum voltage location of the RPA, while the gate bias lines are integrated with the feed network.

Although each array element can be excited through independent DC biasing lines, this configuration will result in a very complex biasing circuitry. To relax this scenario, all the four array elements on one side of 4 x 2 unit cell are biased through a common drain bias line, and all the eight array elements in each cell are biased though a common gate bias line. All the 4 x 2 unit

cells are electrically connected to the corporate feed network through capacitors, making each cell independent from each other in terms of biasing.

6.4.3 Fabrication



(a) (b)

Figure 6.19: Visualization of the (a) fabricated prototype and (b) prototype installation in Satimo for radiation pattern measurement.

The dimensions of the realized 8 x 8 active array antenna prototype are around 28 cm x 28 cm and cannot be fabricated as a single board at our facility, where the maximum dimensions are limited to 15 cm x 15 cm. As a result, the prototype is appropriately divided into four parts, which are then fabricated individually. Subsequently, these four boards are manually copper taped and soldered on the bottom ground layer, while the feed lines existing on the top layer are soldered for electrical connections. The realized prototype is shown in Fig. 6.19(a) and is exited through a coaxial cable connector. In acknowledging the discrepancy between the realized prototype and the simulated design, a difference in corresponding results can be expected.

6.4.4 Results and discussion

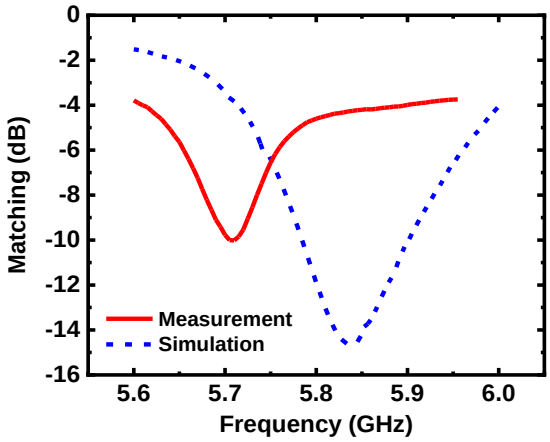
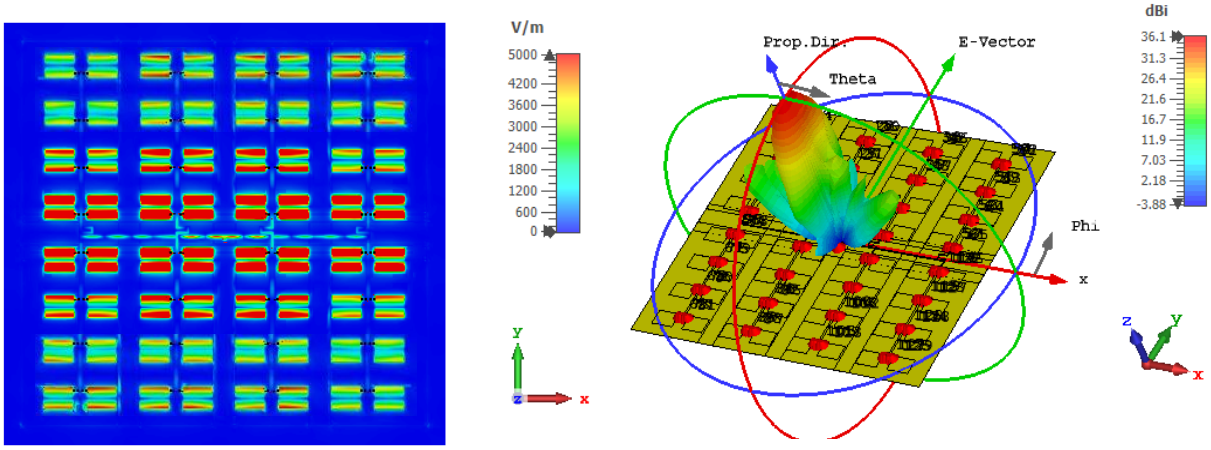


Figure 6.20: Comparison of co-simulated and measured impedance matching response of 8 x 8 active array antenna prototype.

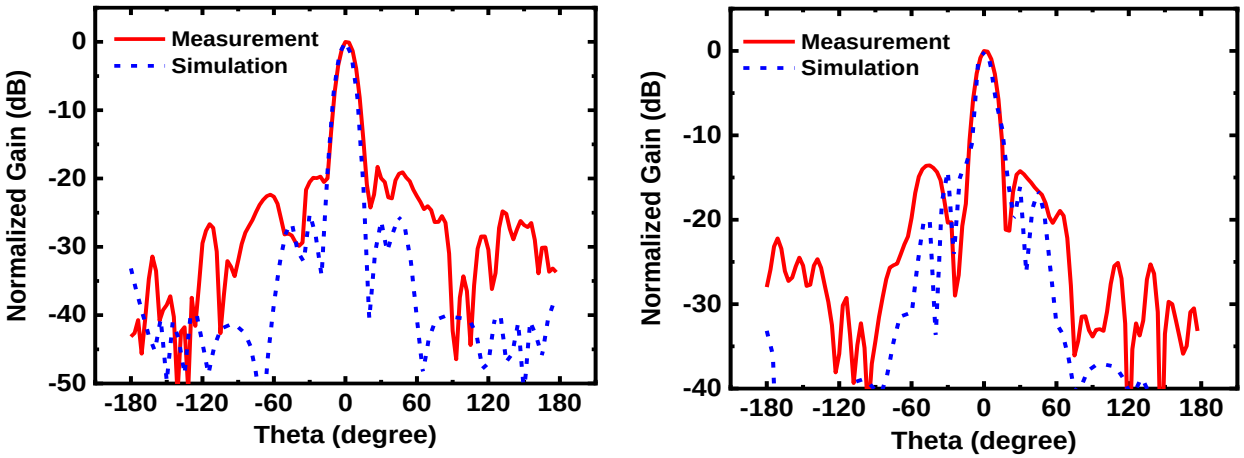


(a) (b)

Figure 6.21: Co-simulated results of 8 x 8 prototype (a) E-field distribution and (b) 3D-radiation pattern.

Initially, the matching performance is measured and the comparison of the co-simulated and measured results is shown in Fig. 6.20. Subsequently, the co-simulated E-field distribution of the prototype is analyzed and the corresponding result is shown in Fig. 6.21(a). As illustrated, the E-

field is in phase and its magnitude is maximum at the center and minimum at the edges along E-plane, which is in accordance with the unit cell design. This magnitude distribution realizes a lower side-lobe level in the radiation pattern along this plane. The magnitude is approximately constant along the H-plane due to equal power division through the designed corporate-feed network. However, an unequal power divider can also be designed to excite the center array elements with higher power compared to outer elements to achieve lower sidelobe levels even along this plane. Following this, the co-simulated 3D radiation pattern is illustrated in Fig. 6.21(b), which demonstrates the broadside radiation with a realized gain of approximately 36 dBi (23 dBi antenna gain + around 13 dB amplifier gain). While, the 8 x 8 passive counterpart exhibits a realized gain of approximately 23 dB, which demonstrates that the additional 13 dB gain realized in the active case is from the integrated transistors.



(a) (b)

Figure 6.22: Comparison of co-simulated and measured normalized radiation performance of designed 8 x 8 active array antenna prototype along (a) E-plane and (b) H-plane.

The measured radiation patterns along the E-plane and H-plane are compared with the corresponding co-simulated results in Fig. 6.22(a) and Fig. 6.22(b), respectively. This verifies the broadside radiation, and the main lobe matches well with one another. However, the sidelobe levels are different and are even higher in the E-plane from measurements. Furthermore, an analysis of

the prototype performance by varying the drain bias is also conducted. Although there is a slight variation in the overall performance, a significant difference is not observed.

In fact, the non identical/faulty transistors, fabrication errors, soldering issues, or even potential misalignment could cause the difference between all the simulated and measured results. However, this demonstration proves the concept, and we believe that this work provides substantial information that will assist the readers in the development of novel planar, low-loss and compact joint circuiting-radiating architectures.

6.5 Conclusion

In this work, we have successfully proposed and demonstrated a scalable active array antenna configuration that can realize simultaneous amplification and radiation through a unified design space. In this connection, a detailed analysis of the different feeding techniques of the RPA, appropriate array feed line layout, and DC line installation on the same layer have been presented. This result in a low-cost planar solution, with amplifying transistors soldered on it without utilizing matching networks, thus reducing losses and the overall size. An in-depth analysis and the design of 4 x 2 active array configuration have been discussed. It demonstrated a better matching and an additional gain of 13.5 dB from simulations, compared to its passive counterpart. Then, the design, fabrication challenges, and measurements of the 8 x 8 active array antenna configuration have been presented. And the measured results demonstrate a reasonable agreement with the simulations, proving the concept. Furthermore, each transistor in this configuration handles a part of the input power, thereby enhancing the overall power handling capabilities of these systems. Although the proposed configurations are suitable for implementation at all frequencies, they are more attractive in the mmW range applications and beyond.

CHAPTER 7 ARTICLE 5: MESH-NETWORK EQUIVALENT MODEL FOR UNIFIED RECTANGULAR MICROSTRIP ANTENNA ANALYSIS

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A generalized mesh-network equivalent model for a microstrip rectangular patch antenna (RPA), which is simple yet efficient is proposed, studied and demonstrated in this paper. The mesh-network equivalent model is established through the segmentation of RPA width and radiation parameters into *M* sections, as well as the segmentation of RPA length into *N* sections. A general design procedure to realize the mesh-network equivalent model is addressed and described for any number of RPA segmentations, as desired by specific applications. Subsequently, the proposed mesh-network equivalent model is used to accurately evaluate the input impedance responses at various feed positions along the length of RPA. In addition, to include the effects of a slot etched inside the RPA geometry, a generalized microstrip coupled line equivalent model is proposed, analyzed and discussed in detail. Eventually, the microstrip coupled line model in conjunction with the proposed mesh-network equivalent model can accurately estimate the input impedance response of a slotted RPA, and has been verified for RPA with center slot, edge slot and multiple slots as examples in this work. Two cases with multiport excitation of RPA are also analyzed and presented as a part of this work. For demonstration purposes, all these prototypes are designed, fabricated and measured at 28 GHz. The proposed equivalent model-based results are validated by measured and simulated counterparts. Furthermore, the extension of the proposed mesh-network model to accommodate slots of smaller size inside RPA, RPA loaded with via, inverted-F antenna, and multimode operation is demonstrated and discussed through a comparison between mesh-network modeling results and simulation results.

7.1 Introduction

Microstrip technology has been among the most popular integration techniques in the development of numerous efficient multifunctional front-end modules and antennas. The ease of integration, low-cost printed circuit board (PCB) fabrication, and compactness have secured a major spot of this technology in commercial applications, particularly for wireless systems operating below 6 GHz.

Needless to say, the world is now advancing to embrace the millimeter-wave (mmW) frequencies in response to the overcrowded low frequency spectrum, and also to meet the demand for both higher data rates and improved parametric resolution. The intended applications of 5G, imaging, automotive radar and so on have further triggered an explosive interest in this regime for both industrial and academic researchers and practitioners. However, the rise in both transmission losses and radiation issues from microstrip circuitry presents notable limitations for its applications in future mmW circuits and antennas.

Henceforth, the conventional approach of designing circuits and antenna independently at a standard reference impedance (typically 50 Ω) and interconnecting them is not a promising solution. Eventually, the active integrated antenna (AiA) has emerged as an architectural development that allows the integration of both active circuits and antennas on the same substrate within a design space close to each other. This facilitates in removing a part of interconnections and/or matching networks, and in turn their corresponding radiation effects and passive circuitry losses [19, 47]. Antennas in this case are directly referenced to an impedance defined by the circuitry in design. Still, the mandatory interconnections, feed lines, and peripheral circuits are notable drawbacks, restricting their physical implementations and electrical performances. Henceforth, the UNified and Integrated Circuit Antenna (UNICA) has been recently proposed [3]-[6], which promises the removal of interconnections, feeding lines, and matching networks. Here, the antennas operate as passive circuitry in addition to radiation, and co-exist with active devices which also function as interconnections. This eliminates the corresponding losses and radiation effects from the traditional circuitry components and feedlines, making them attractive for upcoming mmW/terahertz high-density integrated systems.

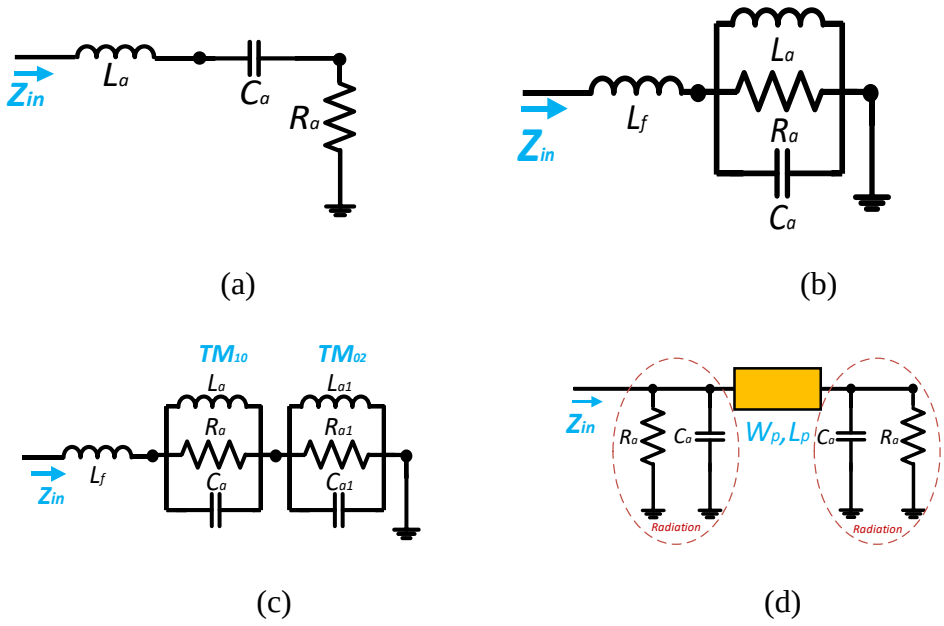


Figure 7.1: Equivalent circuit model of antenna with (a) series lumped circuit elements, (b) paralleled lumped circuit elements, (c) multiple paralleled lumped elements for simultaneous multimode realization, and (d) transmission line equivalent model with lumped and microstrip elements for rectangular patch antenna.

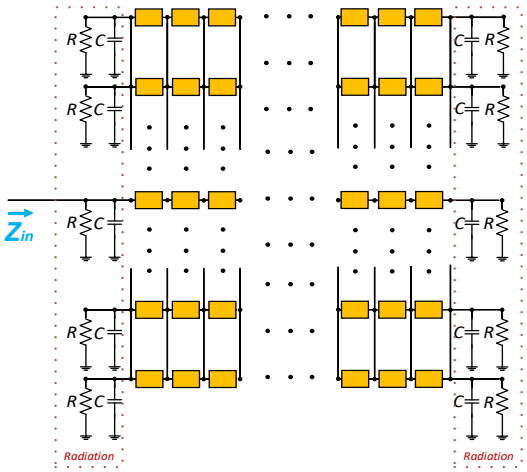


Figure 7.2: Proposed mesh-network equivalent model of microstrip rectangular patch antenna.

In the present day context, the design of corresponding front-end circuits and antennas followed by their integration may be divided into the following two major steps which eventually make use

of microstrip line technology (even though other technologies such as substrate integrated waveguide (SIW) may also be considered):

1. microstrip antenna design and analysis in a 3D field simulation platform (CST-MWS, HFSS, and FEKO, for example) or 2.5D field platform (Keysight ADS-momentum, Sonnet and IE3D, for example), and
2. active circuit design and characterization in a circuit simulator platform (Keysight ADS and Microwave Office, for example).

Conventional architectures ensure pre-specified matching conditions between the circuits and antenna modules by default. This enables the independent design of corresponding modules in different simulation platforms and efficient interconnection of them. However, in either AiA or UNICA integration techniques aforementioned, the S-parameter models of designed microstrip antennas from one platform have to be exported to the circuit simulator platform for co-simulation and global optimization, or vice versa. This procedure may have to be further repeated for each antenna parametric or geometric variation, which immensely increases the time of each simulation and optimization. Therefore, the accessibility to an efficient equivalent circuit model of antenna has been extensively examined and studied over years, which enables a rapid co-design and analysis of circuit-antenna in the same platform.

Although the well-documented cavity model [39, 190, 191] and its extended multiport network model [187, 192-194] have been proven as efficient equivalent models for microstrip antennas, they usually require the solution of complex field equations and do not support co-simulation of circuit-antenna within the same platform. On the other hand, lumped circuit models as shown in Fig. 7.1(a)- 7.1(c) can easily be evaluated from the antenna's responses [133, 195]. They support any-level of co-simulation jobs and have been utilized for analysis of both AiA [16], [17] and UNICA developments [3]. Nevertheless, the lumped circuit equivalent model fails to explicitly provide any straightforward information on antenna development or its radiation properties and does not even support parametric variations or modifications of antenna geometry.

With regards to the analysis of rectangular patch antennas (RPA) which have been popular for circuit-antenna integration, a generalized transmission line equivalent model (TL-model) [196] as described in Fig. 7.1(d) is simple and, more importantly, it supports the co-simulation requirements

of both circuit and RPA on the same platform. Moreover, it is directly relatable to an RPA layout and allows visualizing the radiation. Therefore, this model has been adopted for the analysis of both AiA [19, 197] and UNICA [198, 199] with RPAs.

In addition, numerous equivalent models have been previously proposed to support RPAs with either slots or vias or multimode operation, etc., through modifying lumped or TL equivalent model or by combining both of them. Multiband antenna configuration [200], cross-aperture coupled patch antenna for circular polarization [201], shorting strip loaded patch for compact and broadband response [202], E-patch for multiband response [203], center slot patch antenna for size reduction [204], higher-order mode [205], SIW cavity-backed RPA [26] and stacked RPA for broadband response [27] are just a few examples for which the equivalent models have already been demonstrated to accurately estimate the impedance response. However, a majority of those demonstrated equivalent models, along with the simple lumped and TL-model are neither amenable generalized solutions nor support various slots, vias, pins, etc., in the same RPAs.

As a matter of fact, a single generalized equivalent model capable of estimating the response of RPA with the following characteristics; 1) feed position variation, 2) slots etched in it, 3) vias integrated within, 4) supporting multiport excitations, and 5) multiband operations, is definitely an interesting and desirable solution. To this end, we propose a mesh-network model shown in Fig. 7.2 as a potential analysis scheme for all the specifications highlighted above. Although such a model is attractive for every application, it is of significant interest in the UNICA development through a seamless co-design process in the schematic platform, as the antenna operates as a circuit or vice-versa. As a result, the time involved in exporting and importing models between the simulation platforms, as well as the time taken for antenna simulations in 3D/2.5D platforms are eliminated. This facilities a rapid initial design and analysis of AIA and UNICA solutions, making this approach very time efficient.

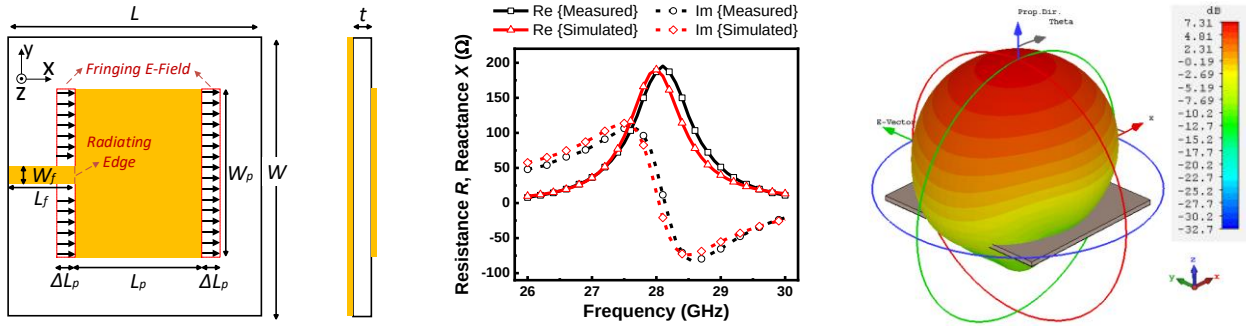
In the scope of this work, a general design procedure to realize such a mesh-network equivalent model for RPAs is initiated and discussed, followed by example demonstration and impedance matching comparison between measured, modeled, and simulated results. The impedance response with respect to varied feed positions, various slots etched in RPAs and corresponding equivalent model which include the slot effects, along with multiport analyses are also examined, measured, and compared so to demonstrate the capability of the proposed model. Furthermore, smaller slots

inclusion, via integration, and multimode performance analysis are also studied and discussed, followed by concluding remarks.

7.2 RPA and TL-model

This section starts with the design of a microstrip-fed RPA, and the demonstration of different modes emerged by exciting the designed RPA at various feed positions. Subsequently, a conventional TL-model of the RPA is detailed.

7.2.1 Rectangular patch antenna (RPA)



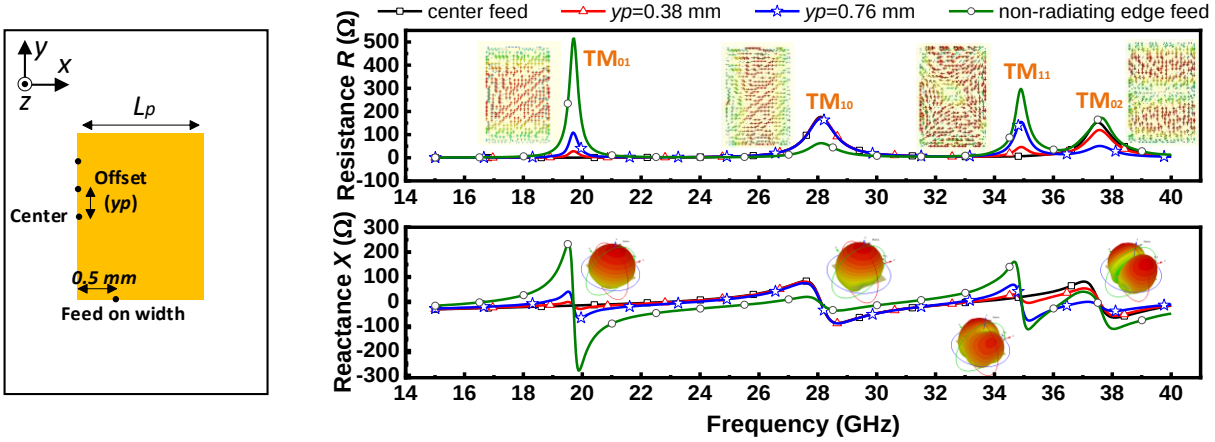
(a) (b) (c)

Figure 7.3: Rectangular patch antenna (a) top view demonstrating the fringing fields along with dimensions: L = 8.6 mm, W = 10 mm, L_p = 2.85 mm, W_p = 4.6 mm, L_f = 12 mm, W_f = 0.6 mm, and side view: t = 0.254 mm (b) comparison of measured and simulated impedance

First of all, a simple and well-matured microstrip-fed RPA is designed for our case studies at 28 GHz on a Rogers 6002 substrate with substrate thickness t = 0.254 mm, relative permittivity ε_r = 2.94, and loss tangent tan δ = 0.0012. The corresponding dimensions, along with the fringing E-field over edges in the fundamental mode (TM_{10}) of operation are illustrated in Fig. 7.3(a). The designed prototype is fabricated and the microstrip feed line length L_f is de-embedded using a through-reflect-line (TRL) calibration kit designed to accurately calculate the impedance response of the designed RPA at its radiating edge as visualized in Fig. 7.3(a). The measured impedance response compared with the simulated result is shown in Fig. 7.3(b). A slight deviation observed in this case could stem from the issue of fabrication tolerances. The designed RPA radiates along

the broadside as shown in Fig. 7.3(c), with a radiation efficiency of 84 % and gain of 7.3 dB from simulations.

7.2.2 Modal Analysis of RPA



(a) (b)

Figure 7.4: (a) Illustration of different feed positions on RPA, and (b) resulting impedance response along with corresponding surface current distribution, modes and radiation pattern visualization.

Although characteristic mode analysis provides the information of potential modes existing in RPA, this analysis is independent of excitation [28], [29]. In order to facilitate the practical designs and also to appreciate the equivalent model of this work, it is certainly important to understand the modes generated in RPA by exciting it at various positions. Subsequently, the feed positions considered in the modal analysis are described in Fig. 7.4(a), and the corresponding impedance responses are plotted in Fig. 7.4(b). For the center-fed RPA over the radiating edge [as shown in Fig. 7.4(a)], the fundamental mode (TM_{10}) and higher-order modes (e.g. TM_{02}) are excited as visualized in Fig. 7.4(b). Offset feedings over the radiating edge at yp=0.38 mm and yp=0.76 mm as marked in Fig. 7.4(a) are able to excite additional modes, namely TM_{01} and TM_{11}, compared to the center-excitation case as shown in Fig. 7.4(b). This modal phenomenon is attributed to the additional modes generated along the RPA width (y-direction) in connection with the offset feed positions. Indeed, TM_{01} mode resonance is defined by RPA width W_p, compared to the TM_{10} mode

dependency on RPA length L_p. Since $W_p > L_p$, the resonant frequency of TM_{01} mode is lower than TM_{10} mode [in Fig. 7.4(b)].

On the other hand, feeding the same RPA on the non-radiating edge as shown in Fig. 7.4(a), also excites modes similar to the offset feeding. In TM_{10} mode operation of RPA, the variation of feed position towards the center along the length (*x*-direction) results in impedance decreasing, compared to the maximum impedance point at the RPA edge. The same behavior can further be analyzed for the non-radiating edge-fed RPA [at feed position specified in Fig. 7.4(a)] through the lower impedance realized at 28 GHz, as shown in Fig. 7.4(b).

In the case of a TM_{10} mode operation of the RPA, the fields are constant along the width (*y*-direction). As a result, the RPA characteristics and impedance responses do not get significantly altered by varying the feed position along the width with regards to this mode at 28 GHz, as shown in Fig. 7.4(b). However, the other modes are affected. Therefore, we can conclude that the modal response in RPA depends on the feed position, and the frequency of modes is essentially defined by the RPA dimensions (geometry).

7.2.3 Transmission line equivalent model (TL-model)

In a TL-model [as shown in Fig. 7.1(d)], the microstrip line width and length are the designed RPA dimensions, while the radiation parameters are calculated from an equivalent radiating-slot with uniform E-field [206]. In this case, paralleled slot conductance $G_1 = 0.0018$ ℧ is evaluated from the total power radiated and corresponding excitation voltage across the slot, where

$$G_1 = \frac{1}{120\pi^2} \int_0^{\pi} \frac{\sin^2\left(\frac{k_0 W_p}{2}\cos\theta\right)}{\cos^2\theta} \sin^3\theta \; d\theta \tag{7.1}$$

Furthermore, coupling between the radiating edges of RPA is also estimated through an additional mutual conductance term $G_{12} = 0.00091$ ℧, calculated from

$$G_{12} = \frac{1}{120\pi^2} \int_0^{\pi} \frac{\sin^2\left(\frac{k_0 W_p}{2}\cos\theta\right)}{\cos^2\theta} J_0\left(k_0 L_p \sin\theta\right) \sin^3\theta \; d\theta. \tag{7.2}$$

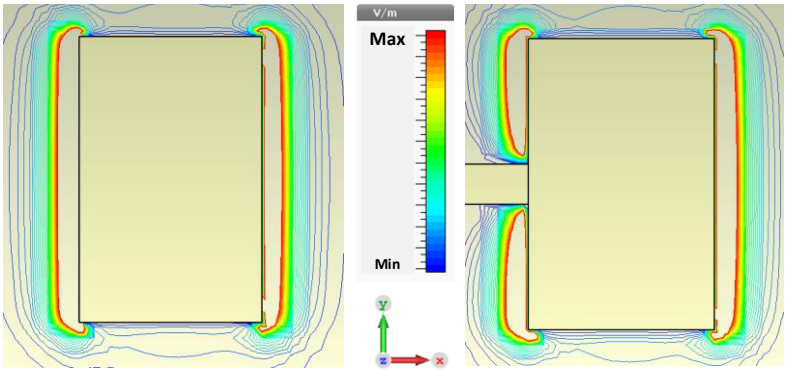
Eventually, the effective edge resistance of RPA is $R_a = 1/G_a = 370$ Ω from

$$R_a = \frac{1}{G_a} = \frac{1}{(G_1 + G_{12})} \tag{7.3}$$

while the radiating edge capacitance C_a = 0.06 pF is calculated through the equivalent microstrip open-end effect

$$\Delta L_p = 0.412\, t\, \frac{(\varepsilon_{eff}+0.3)\left({}^{W_p}/_{t}+0.264\right)}{(\varepsilon_{eff}-0.258)\left({}^{W_p}/_{t}+0.8\right)} \tag{7.4}$$

$$C_a = \varepsilon_o \varepsilon_r \frac{\Delta L_p W_p}{t}. \tag{7.5}$$



(a) (b)

Figure 7.5: Isometric E_x-field distribution of RPA with (a) co-axial/proximity/ aperture-coupled/ non-radiating edge feed and (b) microstrip inset feed.

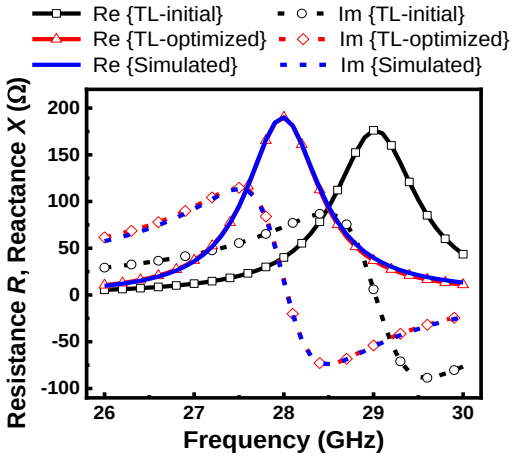


Figure 7.6: Comparison of the measured and equivalent TL-model impedance response of RPA.

For an RPA excited through coaxial feed (or) proximity-coupled (or) aperture-coupled (or) non-radiating edge feed, the fringing electric field (E_x component) isometric lines are shown in Fig.

7.5(a). This illustrates that the radiation along the edges of RPA is uniform, which is in equivalence with the models considered in the derivation of radiation parameters. However, when RPA is excited through the micorstrip line feed on the radiating edge, the radiating E-field is disturbed as shown in Fig. 7.5(b). In this case, the derived equivalence radiation parameters are no longer appropriate, and demands further optimization of them to realize an accurate TL-model. Subsequently, the optimized radiation parameters achieved for microstrip feed excitation are R_a=400 Ω and C_a=0.09 pF, after tuning. In addition, an inductor of 0.1 nH is included in series at the input to compensate the discontinuity between the feed line and RPA. For reference, the results from initial TL-model with radiation parameters from the derived equations, and TL-model with optimized radiation parameters are compared with the simulation results in Fig. 7.6.

As analyzed above, this simple one-dimensional TL-model can be considered dependent on the feed configuration, although it provides an intuition of the RPA layout and its radiation. Furthermore, this model is not a potential solution for evaluating the RPA with slots or in multimode operation or with vias and so on. For this purpose, the mesh-network equivalent model is proposed in this work as an appropriate scheme in support of this development, which is discussed in detail in Section 7.3.

7.3 Mesh-network model

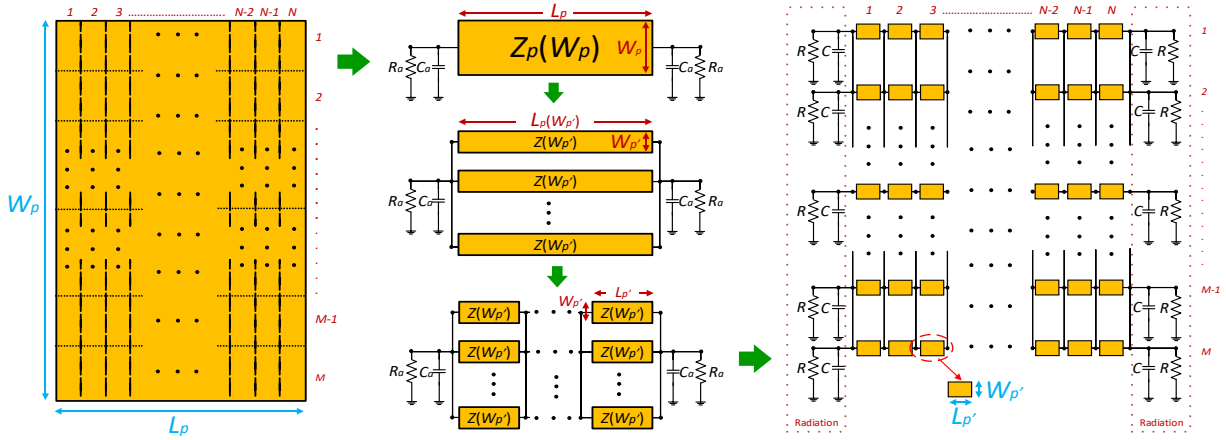


Figure 7.7: (a) Division of RPA layout into *M* sections along width and *N* sections along length, (b) modelling steps, and (c) proposed mesh-network equivalent model.

In the development of mesh-network model, RPA layout is initially divided into *M* sections along width, and *N* sections along length as shown in Fig. 7.7(a). These individual sections are then realized through equivalent microstrip lines and are properly interconnected. Furthermore, the evaluated radiation components (R_a and C_a on the edges) are also divided into *M* segments. These equivalent microstrip and lumped circuit components are readily available in any commercial microwave schematic platforms, and can be designed with high accuracy.

In a wide range of applications, RPA is operated in the fundamental mode TM_{10}, wherein the fields remain constant across its width regardless of the feed position. This behavior can be confirmed with the RPA impedance response observed by varying the feed position as described in Fig. 7.4(b). In order to preserve this behaviour in the mesh-network model, sections along the length *N* are deliberately made equal by electrically shorting after each *N*. The modelling steps to realize the proposed model are illustrated in Fig. 7.7(b), and the final mesh-network model is shown in Fig. 7.7(c), which can be directly related to the RPA.

7.3.1 Modelling procedure

In the first instance, width W_p of RPA is divided into *M* microstrip line sections. The corresponding microstrip line dimensions are defined based on the characteristic impedances instead of directly utilizing the physical RPA division values. This characteristic impedance based division approach is indispensable as the microstrip lines utilized in the mesh-network model construction have fringing fields along its length, which on the other hand doesn't exist in the inner sections of RPA.

An equal segmentation case is considered here to reduce the complexity of equivalent model's parameters extraction, but it is not mandatory. In this regard, the characteristic impedance $Z_p(W_p)$ of RPA is initially calculated from its width W_P. This impedance is then multiplied by *M* to calculate the characteristic impedance $Z(W_{p'})$ of each divided section.

$$Z(W_{p'}) = M \times Z_p(W_p) \tag{7.6}$$

This multiplication is valid as the *M* sections along the width operate similar to *M* impedances in parallel. Consequently, the width $W_{p'}$ of each divided microstrip line section can be calculated

corresponding to the characteristic impedance $Z(W_{p\prime})$. This procedure is further presented in a sequence such as

$$W_p \;\rightarrow\; Z_p(W_p) \;\rightarrow\; Z(W_{p'}) \;\rightarrow\; W_{p\prime} \tag{7.7}$$

Since the equivalent microstrip line width $W_{p'}$ of each equal section is different from the RPA width W_p on the same substrate of thickness *t*, the corresponding effective permittivity ε_{eff} is also varied, calculated from

$$\varepsilon_{eff} = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\left(1+\frac{10t}{W_{p\prime}}\right)^{-0.5} \tag{7.8}$$

This further results in the modification of guided wavelength λ_g as

$$\lambda_g = \frac{c}{f_r\sqrt{\varepsilon_{eff}}} \tag{7.9}$$

at the fixed design frequency f_r. This difference in electrical length corresponding to width should be accounted for in the division of RPA into *N* sections along length of the equivalent mesh-network model. Subsequently at width $W_{p'}$, the equivalent length $L_p(W_{p\prime})$ of microstrip line can be evaluated from

$$L_p(W_{p'}) = \frac{c}{2f_r\sqrt{\varepsilon_{eff}}} - 2\Delta L_p(W_{p'}), \tag{7.10}$$

where $\Delta L_p(W_{p\prime})$ can be evaluated by replacing W_p with $W_{p\prime}$ in (4). As width $W_{p\prime}$ decreases, both ε_{eff} and $\Delta L_p(W_{p\prime})$ decrease. However, ε_{eff} decreases at a higher rate compared to $\Delta L_p(W_{p\prime})$ resulting in an effective $L_p(W_{p\prime})$ increase from (7.10).

Eventually, the microstrip line length $L_{p\prime}$ of each section in the mesh-network model with width $W_{p\prime}$ is the division of the updated patch length $L_p(W_{p\prime})$ into *N* sections, calculated by

$$L_{p\prime} = \frac{L_p(W_{p\prime})}{N} \tag{7.11}$$

The steps for the length division are further demonstrated as

$$W_{p\prime} \;\rightarrow\; L_p(W_{p'}) \;\rightarrow\; L_{p\prime} \tag{7.12}$$

The corresponding mesh-network model development steps are further illustrated in Fig. 7.7(b). All these necessary parameters can be instantly evaluated with a calculator that is readily available in microwave design platforms like Keysight ADS, CST-MWS, etc.

Finally, the radiation parameters R_a and C_a evaluated from equations (7.3) and (7.5) of the TL-model are modified to be more relevant in the proposed mesh-network model. Since the radiation is along the width on either edges of the RPA, and the width is divided into M equal parallel sections, the radiation parameters are also divided in M parallel segments. The effective radiation resistance R of the mesh-network model is therefore the multiplication of TL-model resistance R_a by a factor of M

$$\frac{1}{R_a} = \frac{M}{R},\ R = MR_a \tag{7.13}$$

Similarly, the edge capacitance C in the mesh-network model is the division of TL-model capacitance C_a by a factor of M, considering the parallel arrangement of capacitors

$$C_a = MC,\ C = \frac{C_a}{M} \tag{7.14}$$

In fact, the radiation parameters (R and C) segmentation into M sections become important when a part of the radiating edge is removed/blocked. For example, the slot etched for an inset feeding of the RPA results in a decreasing radiation efficiency, which can be incorporated in the proposed mesh-network equivalent model by removing the corresponding radiation section.

Furthermore, the response from the proposed mesh-network model remains consistent with corresponding RPA results, even with the variation in number of sections along both width M and length N, once the design procedure is followed. The number of RPA divisions (M, N) and its equivalent-model sections can be fixed based on the minimum slot dimension to be etched, or area equal to active device dimension that is intended to be directly integrated within the antenna or number of vias and so on.

7.3.2 Demonstration

An example of the mesh-network model with M = 5 and N = 10 segmentations is realized for the designed RPA, following the above-discussed procedure. Subsequent to it, the characteristic impedance of designed RPA with W_p= 4.6 mm is initially calculated to be $Z_p(W_p)$ =10.7 Ω.

Therefore, the characteristic impedance of each section with M =5 should be $Z(W_{p'})$=10.7 x 5 = 53.5 Ω, as calculated from (7.6). Eventually, the width of each section $W_{p'}$ corresponding to $Z(W_{p'})$ can be calculated as 0.56 mm.

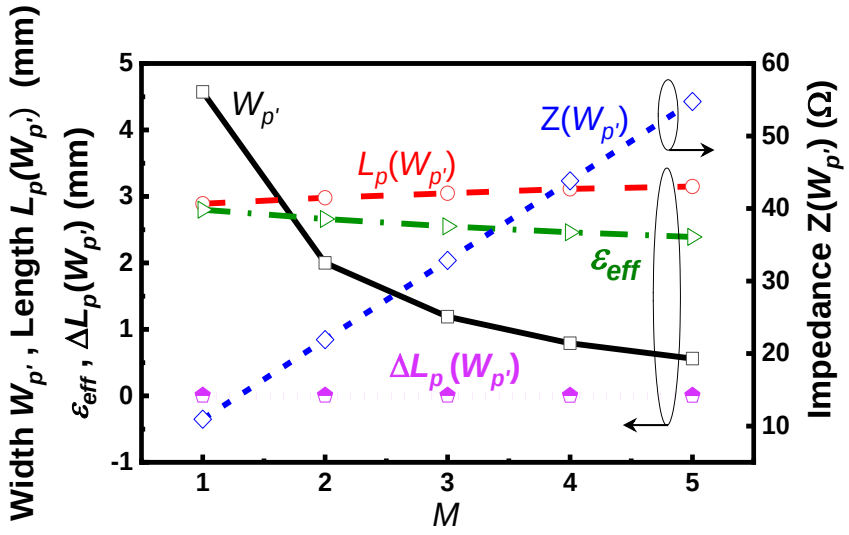
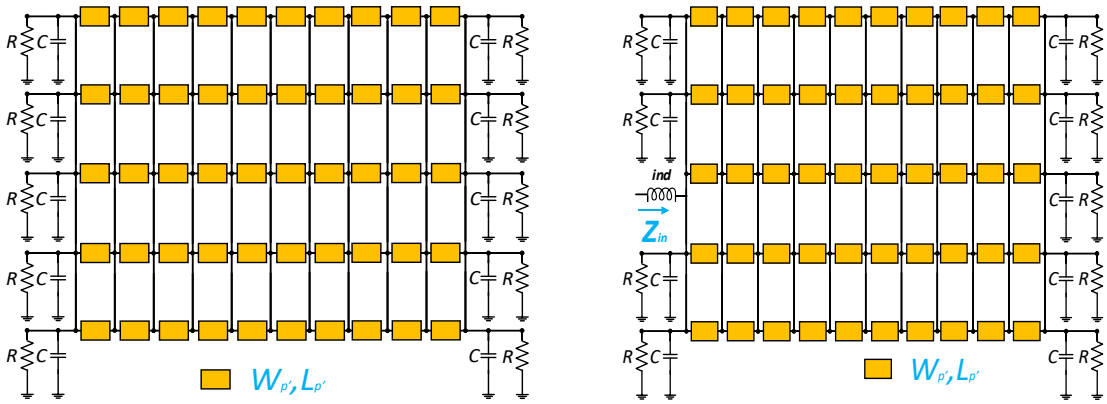


Figure 7.8: Variation of mesh-network model parameters; $W_{P'}$, $L_p(W_{P'})$, ε_{eff}, updated $\Delta L_p(W_{P'})$, and $Z(W_{P'})$ with different M.

At this width $W_{p'}$, the updated patch length $L_p(W_{p'})$ is calculated as approximately 3.246 mm. Subsequently, $L_{p'}$ of the final model is calculated by dividing the updated length $L_p(W_{p'})$ by N=10, thus $L_{p'}$ = 0.3246 mm. In addition, the variation in parameters $W_{p'}$, ε_{eff}, $Z(W_{p'})$, $\Delta L_p(W_{p'})$ and $L_p(W_{p'})$ by modifying M are included in Fig. 7.8, for reference. It can be seen that the increase in number of sections along width M results in decreasing width $W_{p'}$, effective permittivity ε_{eff} and additional length $\Delta L_p(W_{p'})$. However, the resonant patch length $L_p(W_{p'})$ increases along with the characteristic impedance $Z(W_{p'})$. While, the variation in N will only modify $L_{p'}$ in a linear function as understood from equation (11), and has no influence on other parameters.



(a) (b)

Figure 7.9: Mesh-network equivalent model of RPA with (a) co-axial/proximity/ aperture-coupled/ non-radiating edge feed and (b) microstrip inset feed.

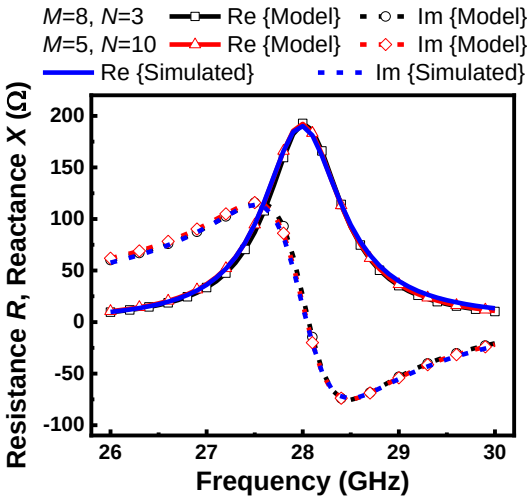


Figure 7.10: Comparison of simulated and mesh-network equivalent model impedance response of RPA with different *M* and *N* combination.

Table 7.1: Mesh-network equivalent model parameters for different *M* and *N* combination.

	$Z(W_{p'})$ Ω	$W_{p'}$ mm	$L_p(W_{p'})$ mm	$L_{p'}$ mm	R Ω	C pF
***M*=5 and *N*=10**	53.5	0.56	3.246	0.324	1850	0.012
***M*=8 and *N*=3**	85.6	0.25	3.369	1.123	2960	0.0075

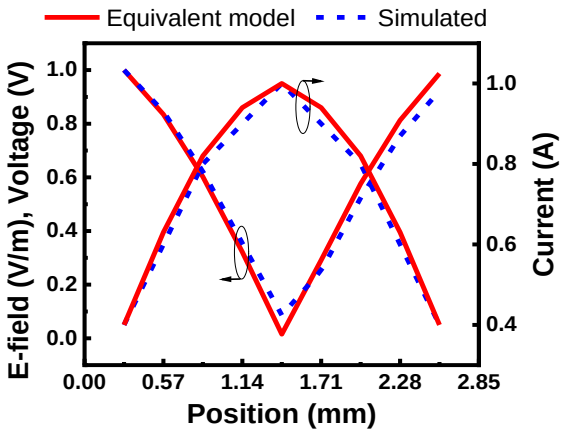


Figure 7.11: Comparison of the normalized mesh-network equivalent model voltage and simulated E-field results, along with the normalized simulated and equivalent model surface current distribution inside the RPA.

Subsequently, the radiation parameters of mesh-network equivalent model become R = 370 x 5 Ω = 1850 Ω and C = 0.06/5 pF = 0.012 pF. Indeed, the radiation parameters are evaluated from (7.1)-(7.5) considering the uniform field distribution on the radiating edges, and the corresponding equivalent mesh-network model is shown in Fig. 7.9(a). In contrast to the TL-model, the evaluated parameters remain unchanged for the proposed model even with the feed configuration that blocks the radiating field, for example through microstrip feed excitation on the radiating edge. However, the corresponding radiating section of the proposed model has to be removed as illustrated in Fig. 7.9(b), to compensate the radiation blockage through the microstrip feed line. All the evaluated parameters of this proposed equivalent model are further presented in Table 7.1, and the comparison of equivalent model [Fig. 7.9(b)] results with simulations is shown in Fig. 7.10, which agree closely. This demonstrates the fundamental advantage of the proposed model over the TL-model, wherein the evaluated parameters are directly applicable for different feed configurations and need no re-optimization. In addition, the proposed model gives a true perception of the antenna configuration along with feed information. Moreover, the comparison of normalized E-field from simulations and equivalent voltage in the proposed model, along with the normalized current distribution from both simulation and equivalent model are compared in Fig. 7.11 for reference, which demonstrate a good match.

Besides, another equivalent model of designed RPA with M=8 and N=3 sections has also been developed following the procedure described, and the corresponding parameters are presented in Table 7.1. The impedance response result of this model has also been included in Fig. 7.10, and the results agree closely with others, thus confirming the generality of the proposed design approach. The results from the equivalent-model remain accurate when the parameters of its building components are within the recommended range of usage [defined by the platform of implementation, for example ADS here].

7.4 Mesh-network model applications

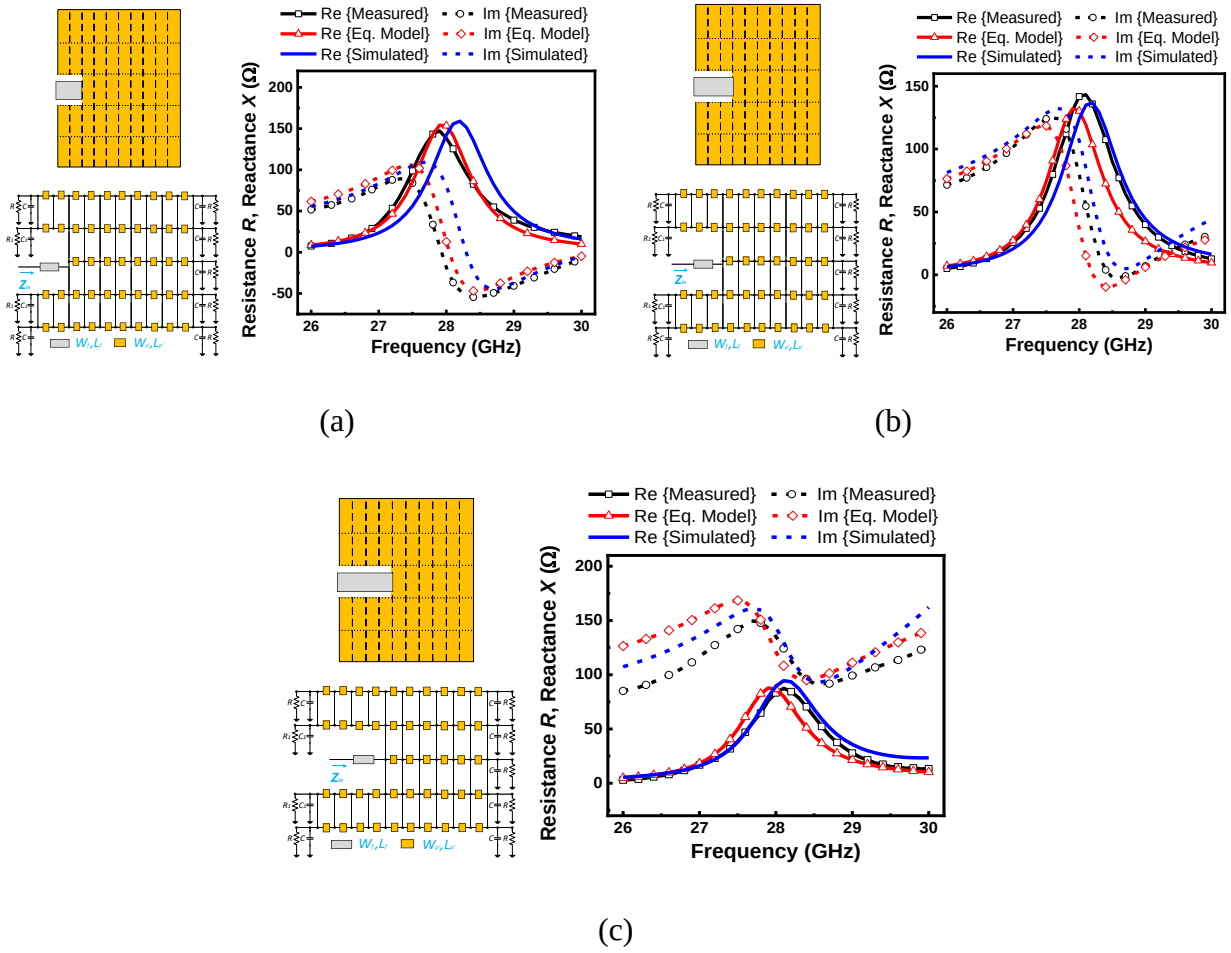


Figure 7.12: Input impedance response of RPA varying the inset feed position along its length at (a) feed position 1; L_f = 0.57 mm, (b) feed position 2; L_f = 0.86 mm and (c) feed position 3; L_f = 1.14 mm [at fixed W_f = 0.6 mm].

The proposed mesh-network equivalent model can be conveniently utilized to measure the impedance behavior of RPA; 1) at various feed positions or 2) by etching various slots inside it or 3) even with multiport excitations, which is studied and discussed in this section. All these modifications are made on the designed RPA with its own dimensions unaltered, and analyzed around the design frequency of 28 GHz. Equivalent mesh-network model with M=5 and N=10 is selected as an example for all these demonstrations.

7.4.1 Varying feed position

The three example feed locations analyzed on the designed RPA, along with the corresponding equivalent mesh-network model and results are illustrated in Fig. 7.12. This verifies that the calculated results from the equivalent mesh-network model agree closely with simulations and measurements at the analyzed feed locations. It should be noted that the results compared here are without de-embedding the additional feed line length resulted from the variation of feed position.

7.4.2 Slots

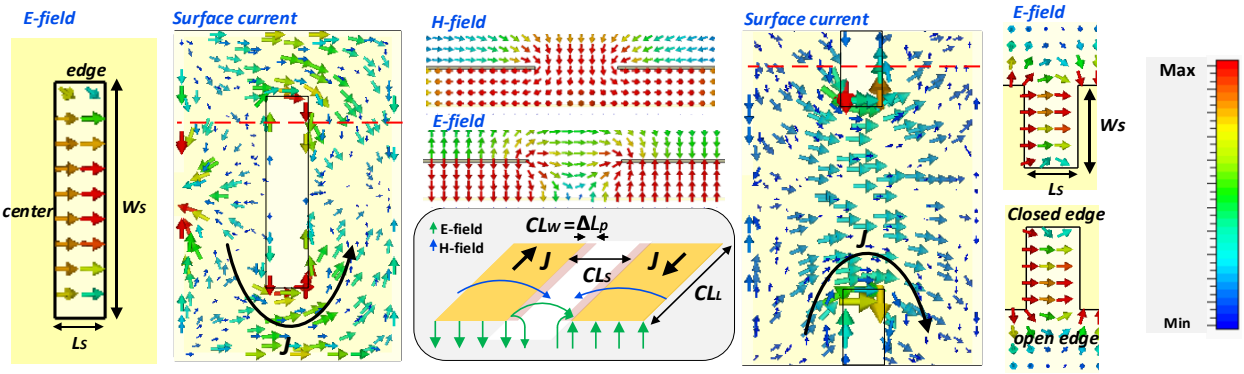


Figure 7.13: E-field distribution and surface current J variation across the center slotted and edge slotted RPA. E-field and H-field along the length of RPA at the highlighted position, along with the equivalent microstrip coupled line model demonstration.

Etching slots on the RPA has been extensively investigated to realize an improvement of one/multiple performance parameters of the RPA. Among them, the slots are etched mainly to; 1) reduce the size of antenna through center slots [207], edge slots [33] and so on and 2) enhance the

bandwidth or enable multiband operation by etching U-slot [208], E-shaped slot [209] and so on. Therefore, the application of the proposed mesh-network model to accurately estimate the impedance response of RPA with these slots is evaluated and discussed. Moreover, arbitrary slots etched in RPA is also analyzed to validate the proposed mesh-network equivalent model as a more generalized solution.

Although different equivalent models have already been proposed in the past to evaluate the impedance/matching response of slotted patches [204, 207, 210], they are valid for a specific slot and have a limited application. In this regard, we intend to develop a single equivalent model that is capable of supporting diverse slots etched inside RPA. In fact, it is evident that a slot in RPA can be equivalently implemented in the proposed mesh-network model by simply removing the corresponding sections. This approach certainly introduces the discontinuity in surface current of the equivalent model, and provides satisfying results when there is a weak coupling between the slot edges. However, the results are not appropriate when there is a considerable coupling between the slot edges, and therefore the equivalent model for slot effects becomes particularly necessary in these scenarios.

In the fundamental mode operation of RPA with slot, the current traverses around the slot and is oriented in opposite direction on either edges of the slot, regardless of the slot location and its layout. This results in the corresponding H-field to be in same direction inside the slot, and the amount of H-field coupling is determined by the magnitude of current on either edge of the slot. On the other hand, the fringing E-field is ever-present at the edge of slot, and the amount of E-field coupling is determined by the voltage on the slot edges. In fact, this distribution of currents and fields is in equivalence with the microstrip coupled lines as shown in Fig. 7.13. Henceforth, microstrip coupled lines form an appropriate equivalent model to incorporate the slot effects inside RPA, and has been analyzed. However, the possible radiation from the slot is not accounted in this development to simplify the design, which might result in a small difference in the equivalent model results compared to the real scenario.

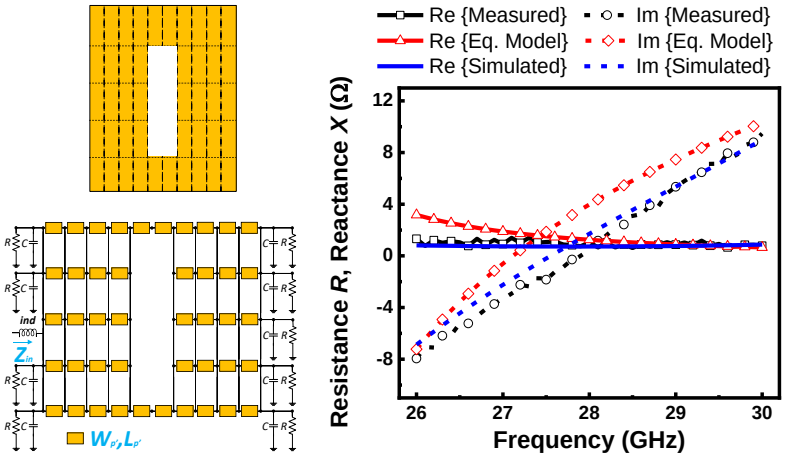
It is well known that the introduction of slots in RPA will affect its overall performance. However, the extent of its influence is dependent mainly on the type of slot, its location and dimensions;

1. All the different slots etched in RPA fall into two fundamental categories, which are a) slots etched inside RPA; and b) slots on the edge of RPA. For slots located entirely inside the RPA such as center slot, the E-field remains maximum at the center and minimum at the edges inside the slot as defined by the boundary conditions and shown in Fig. 7.13. On the other hand, for slots located on the edge of RPA as shown in Fig. 7.13, the E-field is zero on the closed edge while it is maximum and extends outside the slot at the open end.
2. The dimensions of slot also play a major role in influencing the RPA performance. The slot dimension in parallel to the current flow has a minimal influence on the RPA performance. On the other hand, the slot dimension in perpendicular to the current flow will have a significant impact on the RPA performance and even determines the amount of coupling across it.
3. Furthermore, the influence of the same type of slot (with shape and dimensions fixed) is dependent on its location inside the RPA, which is attributed to the current distribution inside RPA. For example, the current is maximum at the center of RPA in the fundamental mode of operation, and henceforth the slot etched at the center has a higher coupling than the same slot etched at an offset location inside the RPA where the current is relatively lower. Since the current distribution inside the proposed mesh-network model follows the RPA distribution as shown in Fig. 7.11, the influence of current on slot location is taken care in the equivalent model.

Considering all these scenarios, rigorous analyses have been performed to evaluate the appropriate dimensions of microstrip coupled lines which will provide the optimum results in conjunction with the proposed mesh-network equivalent model. The corresponding outcomes have been summarized in Table 7.2, and we have observed that the equivalent microstrip coupled line model utilization is slightly different based on the slot location. Nevertheless, the realized optimal dimensions are in agreement with the expected field coupling across the slot. The width of coupled line CL_W is the additional length ΔL_p resulted from the fringing E-field at the edges of slot. Whereas, the coupled line length CL_L remains the same as the width of slot W_s, and the spacing between microstrip coupled lines CL_S is evaluated to be L_s which are the absolute dimensions of the slot as shown in Fig. 7.13.

Table 7.2: Equivalent microstrip coupled line parameters for different slots etched in RPA.

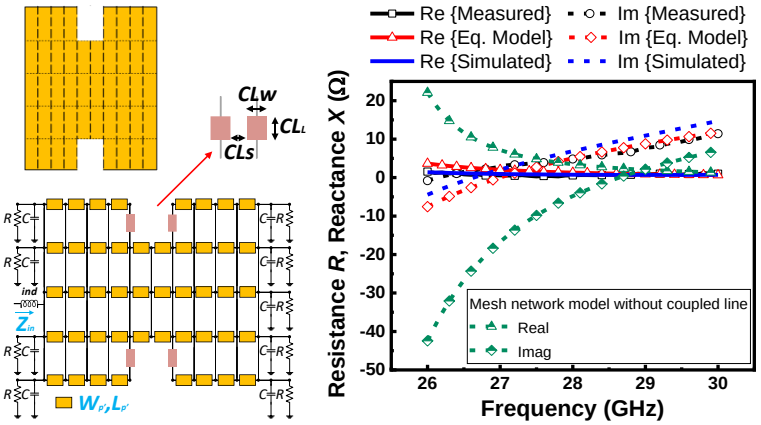
SLOT		MICROSTRIP COUPLED LINE		
LOCATION	**Dimensions**	***CL*$_W$**	***CL*$_L$**	***CL*$_S$**
INSIDE RPA	$L_s \leq 4\Delta L_p$	ΔL_p	W_s	L_s
	$L_s > 4\Delta L_p$	*Not necessary*		
EDGE OF RPA	*Any* L_s	ΔL_p	W_s	L_s



(a) (b)

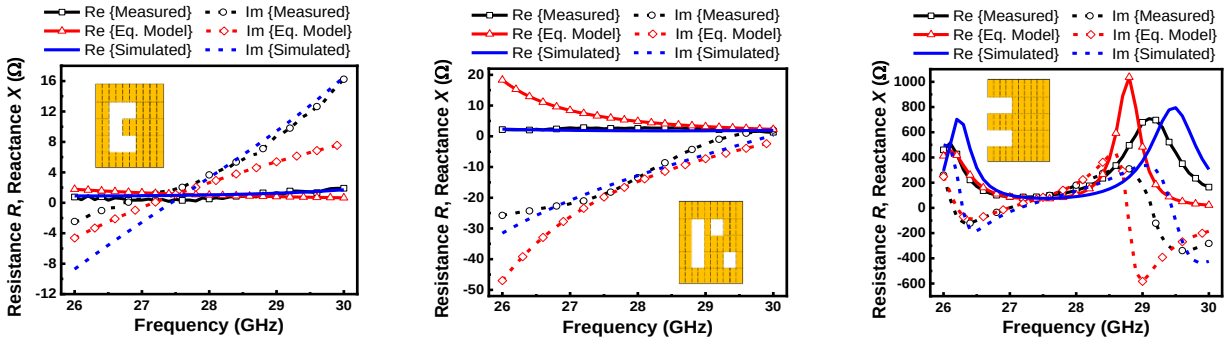
Figure 7.14: Slot etched at the center of RPA (a) with dimensions L_s = 0.57 mm and W_s = 2.76 mm, equivalent to 3 sections along width and 2 sections along length in equivalent mesh-network model, and (b) comparison of measured, equivalent mesh-network model and simulated impedance response.

For example, let's consider a slot with dimensions L_s=0.57 mm and W_s=2.76 mm that is etched at the center of designed RPA as shown in Fig. 7.14(a). Correspondingly, two sections along length and three sections along the width, with respect to the center are removed in the equivalent model as shown in Fig. 7.14(a). Since the slot is entirely inside the RPA, and the slot length L_S is larger than $4\Delta L_p$, the equivalent model for slot is not necessary as described in Table 7.2. Finally, the results from the equivalent model, measurements and simulations are all compared in Fig. 7.14(b), and agree well with one another.



(a) (b)

Figure 7.15: Slots etched on the edge of RPA (a) with dimensions L_s = 0.57 mm and W_s = 0.92 mm on each edge, equivalent to one section along width and 2 sections along length in equivalent model, and (b) comparison of measured, equivalent mesh-network model and simulated impedance response.



(a) (b) (c)

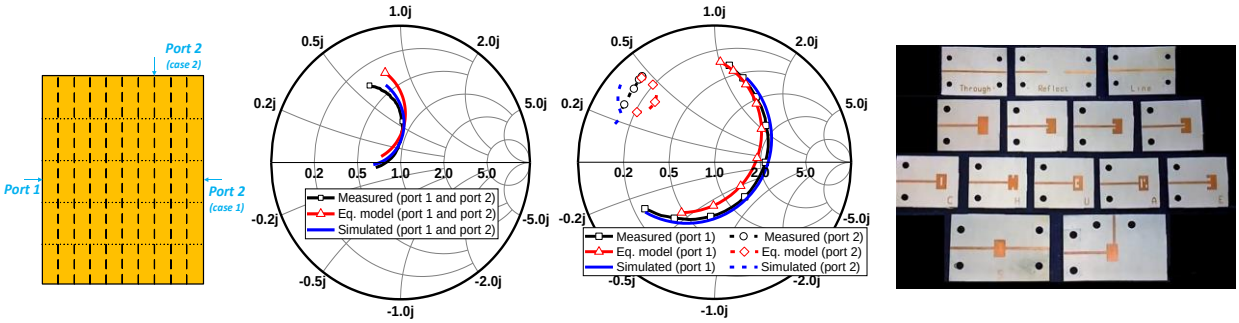
Figure 7.16: Comparison of measured, equivalent mesh-network model and simulated impedance response of RPA with (a) U-slot (b) arbitrary slot and (c) E-shape.

If slots are etched at the center but on the non-radiating edges of RPA as shown in Fig. 7.15(a), the equivalent mesh-network model sections have to be removed. Following the specified conditions in Table 7.2, the microstrip coupled lines with dimensions CL_W= 0.127 mm, CL_S= 0.57 mm and CL_L= 0.92 mm are integrated with the mesh-network model to include the slot effects, as shown in

Fig. 7.15(a). The corresponding results from the measurements, equivalent model, and simulations are all compared in Fig. 7.15(b), which match well. In addition, the results from the mesh-network model without coupled lines are included in Fig. 7.15(b) for reference.

Following this early-described procedure and understanding, the impedance responses for U-slot, arbitrary slots, and E-slot etched on the designed RPA are also analyzed from measurements, proposed mesh-network equivalent models, and simulations. The corresponding results and slot locations within the designed RPA are depicted in Fig. 7.16(a) to Fig. 7.16(c).

7.4.3 Multiple ports



(a) (b) (c) (d)

Figure 7.17: (a) Demonstration of two cases of multiport RPA excitation. (b) comparison of measured, equivalent mesh-network model and simulated results of RPA with excitation at ports 1 and 2 as shown in case 1. (c) comparison of equivalent mesh-network model, measured and simulated results of RPA with ports 1 and 2 as shown in case 2. (d) fabricated TRL calibration kit and prototypes with all of the modifications discussed.

Next, two multiport configurations have been analyzed on the designed RPA, followed by the analysis of signal coupled between the two ports on RPA.

7.4.3.1 **2 ports on opposite edges**

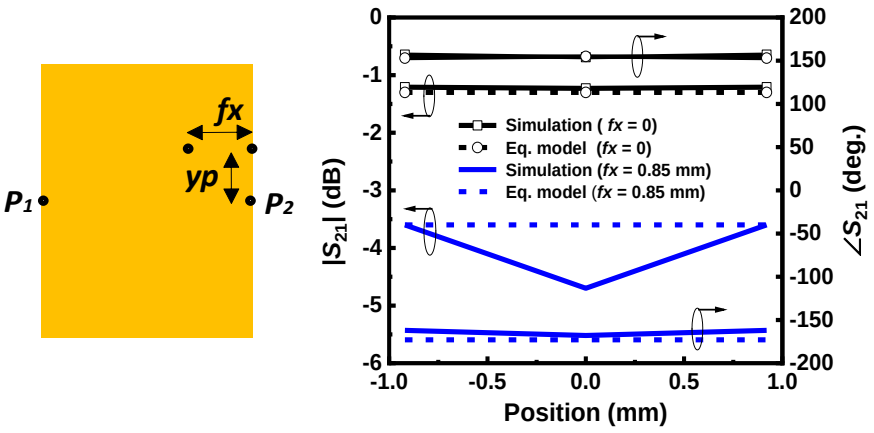
Series-fed array antennas [211], differential-feed patch antennas [212], and UNICA configurations [198] are notable applications wherein the two ports are located one on each radiating edge of RPA. The proposed mesh-network equivalent model can be utilized to estimate the impedance response

at the edge of RPA in the presence of a port on the opposite edge. Furthermore, the amount of signal coupled from one port to another, and the phase difference of the signal across ports can also be instantly evaluated from this mesh-network model. Excitation of the designed RPA with two ports on either side of the RPA is shown in Fig. 7.17(a) (case 1), which is simulated and fabricated. An equivalent mesh-network model can be realized by using two ports; one on each radiating edge of the model. The results of the equivalent model obtained here, simulation results and measurement results are compared in Smith chart as shown in Fig. 7.17(b), and they agree closely.

7.4.3.2 **2 ports on adjacent edges**

Another popular multiport excitation of RPA is through two feeds placed on the adjacent edges of RPA, for realizing circular polarization [133] and orthogonal linear polarized radiation [213]. For demonstration here, the designed RPA is excited with one port on radiating edge and the other port on non-radiating edge as shown in Fig. 7.17(a) (case 2), which is again simulated and fabricated. The equivalent mesh-network model is realized by exciting port 1 on the radiating edge of RPA, and port 2 on non-radiating edge of RPA at N=7. Finally, the impedance response of the equivalent model, simulation and measurement results are all compared in the Smith chart of Fig. 7.17(c).

7.4.3.3 **Coupling between 2 ports**



(a) (b)

Figure 7.18: (a) Illustration of dual port (P_1 and P_2) excitation of the same RPA and (b) simulated and mesh-network equivalent model results of amplitude and phase shift across the ports at various feed positions of port 2.

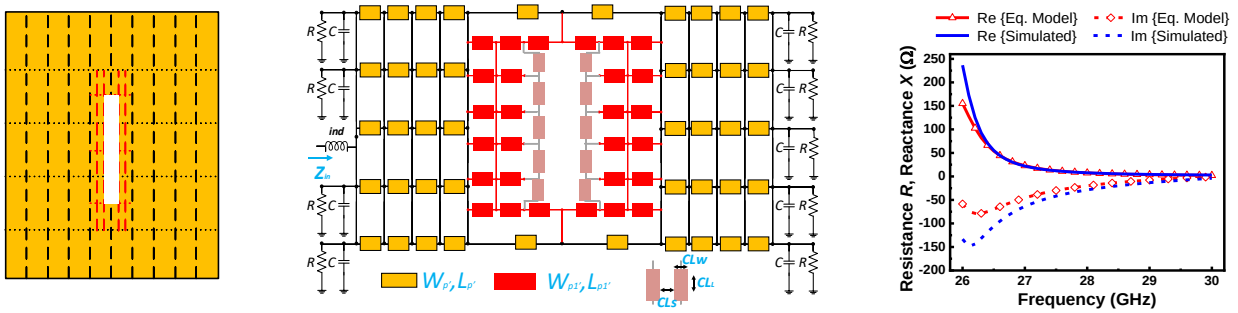
In addition, the coupling between two ports on the designed RPA has been studied and discussed. In this study, the targeted ports locations are shown in Fig. 7.18(a), where the position of port 2 P_2 is varied while port 1 P_1 is fixed in every case. The port 2 position is varied along width between -0.92 mm < yp < 0.92 mm at both fx = 0 mm which is the opposite edge of the RPA, and at fx = 0.85 mm that is inside the RPA. The amplitude and phase difference realized across these ports in each case is studied through both simulations and equivalent model, and the corresponding results are shown in Fig. 7.18(b). In the fundamental mode of RPA operation, the fields and thereby port impedances vary slightly with port 2 P_2 position along the width as shown in Fig 7.4(b), and therefore the amplitude and phase difference between the ports is expected to be minimum. As expected, a nearly equal coupling between the ports is analyzed from simulations and equivalent model for feed position variation along the width, at both fx=0 mm and fx=0.85 mm. This verifies the capability of proposed equivalent model to estimate the coupling across the multiple ports in RPA.

TRL calibration kit, microstrip fed RPA, and all the modifications in the RPA discussed in this section have been fabricated and are shown in Fig. 7.17(d) for reference. All the antennas are designed in the CST-MWS platform, while the corresponding equivalent circuits are modelled in the schematic of Keysight–ADS platform. Although PCB process is utilized for demonstration and fabrication of the prototypes to validate the proposed mesh-network model at a lower cost, this model can furthermore be validated for the RPA designed on other processes such as LTCC, CMOS, III-V MMICs, etc.

7.5 Mesh-network model extension

7.5.1 Smaller slots

In the case of smaller slots in RPA that cannot be realized by a direct removal of the equivalent model sections, we can easily carry out a subdivision only at the slot location. This sub-division can be realized by following the same design steps described earlier, while other sections can be kept unchanged. It is recommended that the subdivision is performed based on the slot dimensions to ensure the low complex equivalent model.



(a) (b) (c)

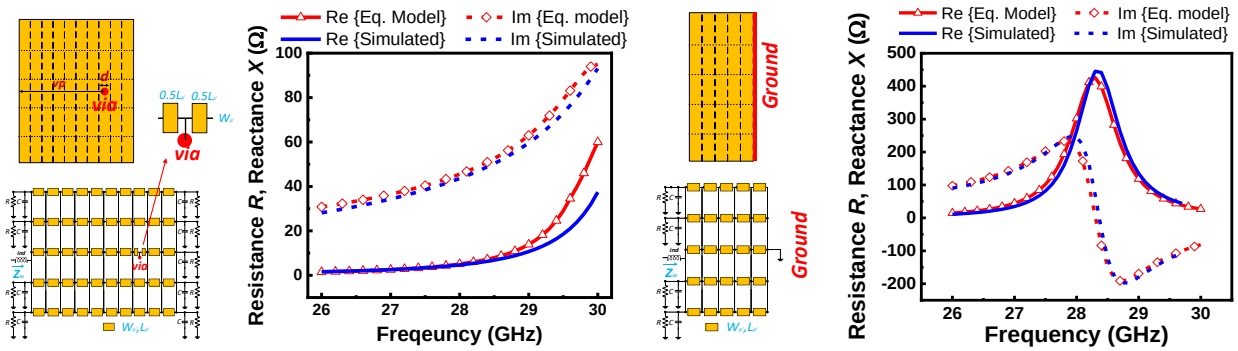
Figure 7.19: (a) Demonstration of smaller slot in RPA, (b) equivalent mesh-network model along with microstrip coupled lines and (c) comparison of equivalent mesh-network model and simulated impedance responses.

For example, let us consider the slot having absolute dimensions of L_s = 0.19 mm and W_s = 1.84 mm placed symmetrically over the center in the designed RPA as shown in Fig. 7.19(a), which is equivalent to $2L_{p'}/3$ and $2W_{p'}$ of the mesh-network model developed with M=5 and N=10. To accommodate this at the center of the already developed mesh-network model, three center sections along the width are divided into 2 subsections each followed by the division of two center sections along the length into 3 parts each. The final dimensions of mesh-network subsections are $W_{p1'}$ = 0.127 mm and $L_{p1'}$ = 0.109 mm, while the parameters of remaining sections stay unchanged as shown in Table 7.1.

Subsequently, the RPA slot sections in the updated equivalent model can be removed. In addition, appropriate microstrip coupled line dimensions from Table 7.2 are utilized (CL_W= 0.127 mm, CL_S= 0.19 mm and CL_L= 0.368 mm) in conjunction with the updated mesh-network model in order to include the coupling effects of the smaller slot in RPA. The corresponding model is shown in Fig. 7.19(b), and the results calculated from this model and simulations are compared in Fig. 7.19(c), which demonstrate a reasonable agreement between them. This confirms that the proposed equivalent mesh-network model is flexible for sub-division and supports smaller slots. Meanwhile, this demonstrates the flexibility of proposed equivalent model to start with a lower number of divisions initially, and subdivide any section based on the application.

7.5.2 Via-loaded RPA

Via loading of RPA can be utilized to control its input impedance and achieve gain enhancement, and has been investigated intensively in the recent years [214]. As a result, a possible integration of vias in the proposed mesh-network equivalent model has been analyzed and discussed.



(a) (b) (c) (d)

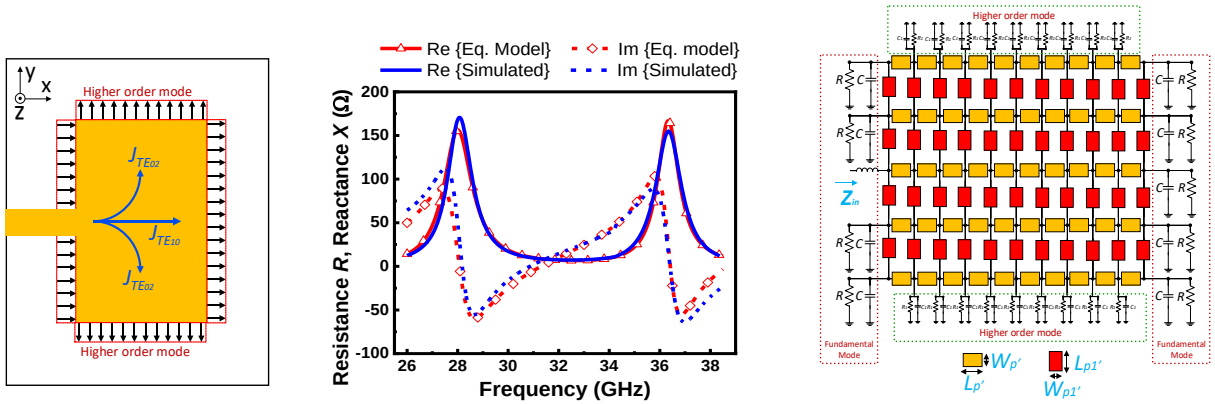
Figure 7.20: (a) Visualization of via loaded RPA, (b) comparison of equivalent mesh-network model and simulated results, (c) illustration of inverted-F antenna, and (d) comparison of equivalent mesh-network model and simulated results.

From the RPA equivalent model shown in Fig. 7.9(b), it is evident that the model is electrically shorted after each segment division along length. As a result, any via integrated at the segment division of equivalent model will be misinterpreted as via present across the patch width. Whereas, a via integrated within the length division can be accurately characterized in the equivalent model, as it is not shorted here. Therefore, it is recommended that the model be divided such that the via is within the division of RPA. For example, consider a single via of diameter d=0.3 mm is placed at the center of width and at a distance of vp=2.1375 mm from the feed edge in the RPA as shown in Fig. 7.20(a). Since this via already falls between the length divisions of developed equivalent model (with M=5 and N=10), this model can be utilized in this scenario. To accommodate this via in the equivalent model, the length section at M=3 and N=8 is divided into two equal parts with each segment of length $L_p'/2$ and W_p'. Subsequently, the via model is placed in-between them as shown in Fig. 7.20(a), and the results from the equivalent mesh-network model and simulations are

compared in Fig. 7.20(b), which agree closely. In a similar manner, multiple vias can also be integrated within the RPA, and the equivalent-model can be accurately developed.

On the other hand, the proposed equivalent model can also be applied for inverted-F antenna (IFA) impedance estimation. As an example, designed RPA is picked and the center of it is grounded as shown in Fig. 7.20(c). In equivalence, the mesh-network model components after the center of RPA model shown in Fig. 7.9(b) have been removed, and the edge has been grounded as shown in Fig. 7.20(c). The corresponding results from simulations and equivalent mesh-network model are compared in Fig. 7.20(d), and they demonstrate a good agreement. From these results, we can conclude that the proposed mesh-network equivalent model can also support integration of vias.

7.5.3 Multimode



(a) (b) (c)

Figure 7.21: (a) Demonstration of fringing fields in TM_{10} mode and TM_{02} mode of RPA, (b) comparison of equivalent mesh-network model result and simulated impedance response, and (c) equivalent mesh-network model.

The radiating edge center-fed RPA excites the fundamental mode TM_{10} and higher order mode TM_{02}, as already understood from Fig. 7.4(b). The fundamental mode radiates from the edges of the length, and the higher order mode radiates from the edges of width. As such, the corresponding fringing fields and surface current path are shown in Fig. 7.21(a). Since they are orthogonal, a multimode mesh-network model can be conveniently developed by adding the higher order mode

through microstrip lines in perpendicular to the fundamental model sections. Furthermore, the radiation from such higher order modes is included through additional radiation elements along the length. The corresponding equivalent mesh-network model for the multimode operation of RPA is visualized in Fig. 7.21(c).

In addition to the parameters already calculated for the fundamental mode operation, the higher order mode parameters should be evaluated. Initially, these parameters are calculated by following the design procedure already described in Section 7.3. Therefore, the width is divided into eleven sections, and the length is divided into four sections to fit into the already evaluated fundamental mesh-network model in Fig. 7.9(b). The RPA width for the higher order mode in this example is 2.85 mm. This width has a characteristic impedance of approximately 16 Ω. Dividing this into 11 sections multiplies the impedance to 16 x 11 = 176 Ω. The effective width $W_{p1'}$ = 0.0254 mm and the corresponding section length $L_{p1'}$ =1.19 mm are finally calculated for the higher order mode, along with the radiation parameters of R_1 = 6750 Ω and C_1 = 0.01 pF. However, slight optimization is necessary to better match the equivalent model results with the simulation results. The optimized parameters are $W_{p'}$ =0.54 mm, $L_{p'}$ =0.22 mm, $W_{p1'}$ =0.006 mm, $L_{p1'}$ =1.189 mm, R=1624 Ω, C=0.0178 pF, R_1=6750 Ω, and C_1=0.01 pF. The comparison of results between the equivalent multimode mesh-network model with optimized parameters and simulations is described in Fig. 7.21(b), which demonstrates a good agreement between them. In this way, an equivalent mesh-network model for multi-mode operation can also be evaluated and validated.

7.5.4 Equivalent model with discontinuities

Furthermore, the mesh-network equivalent model with discontunties can also be developed as shown in Fig. 7.22. The results from this equivalent network model also match very well with RPA results; with parameters $W_{p'}$ =0.54 mm, $L_{p'}$ =0.2645 mm, $W_{p1'}$ =0.103 mm, R=1845 Ω, C=0.0178 pF and ind= 0.1 nH. Although, this model is more generalized; 1) the additional discontinues here increases the complexity of mesh-network equivalent model, while offering no additional advantage in the fundamental mode of operation and 2) the discontinuities model is accurate in a very limited range, which restricts the range of segmentation. Henceforth, the mesh-network equivalent model without discontinuities is generally enough for a wide range of applications.

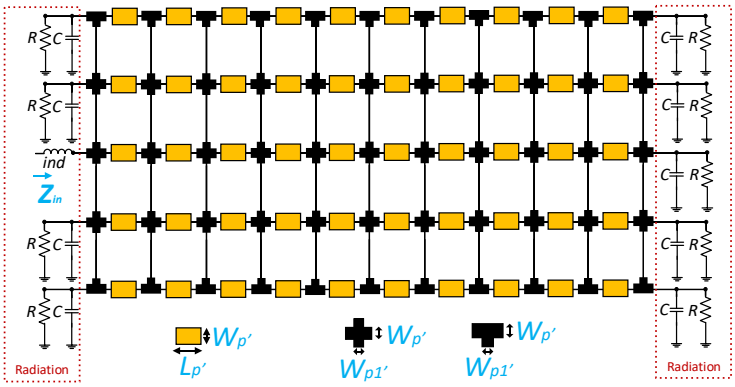


Figure 7.22: Mesh-network equivalent model with *M*=5 and *N*=10 divisions along with discontinuities.

Table 7.3: Comparison of different fundamental equivalent circuit models of RPA.

Model	LUMPED	TRANSMISSION LINE	MESH NETWORK
Components	Lumped elements	Microstrip lines and lumped elements	Microstrip lines and lumped elements
Extraction methodology	from results	from layout	from layout
Advantages	• Easy to evaluate parameters. • Supports all modifications in RPA. • Assists co-simulation.	• Easy to evaluate parameters. • Demonstrates radiation. • Supports co-simulation.	• Easy to evaluate parameters. • Generalized model supporting all modifications in RPA. • Demonstrates radiation. • Supports co-simulations. • Independent of feed configuration.
Disadvantages	• Does not provide information on antenna layout. • No information on radiation. • Each modification in RPA requires a different circuit.	• Does not support modifications. • Depends on feed configuration.	• Relatively complex model.

Modifications include slots, vias, and multimode, multiband and so on introduced in RPA.

7.5.5 Comparison

Finally, the proposed mesh-network equivalent model is compared with the other models described in the introduction and presented in Table 7.3. We have considered only the equivalent models which support co-simulations as a part of this comparison, which is the interest of this work.

7.6 Conclusion

This work has proposed, demonstrated and successfully validated a two-dimensional transmission line equivalent model (mesh-network model) of rectangular patch antenna (RPA) operating in the fundamental mode for analyzing the impedance response. A design procedure for realizing this generalized model is detailed, and successfully applied to a prototype design at 28 GHz as an example. The successful implementation of the proposed equivalent model is also verified for various feed positions and multiport excitation of the designed RPA. In addition, an equivalent model of slot through microstrip coupled lines is proposed to include slot effects inside the RPA. This microstrip coupled line in conjunction with the mesh-network model is utilized to successfully estimate the impedance response of the h-patch, u-loaded patch, arbitrary slots loaded patch, and e-patch. All the corresponding models are also fabricated, and the results generated from the proposed equivalent mesh-network model, measurements, and simulations have demonstrated a good agreement. In addition, the possibility of extending the proposed mesh-network model for the case of an RPA loaded with arbitrary slots of smaller size and via is presented along with the demonstration of multimode operation. The proposed mesh-network equivalent model provides a true and powerful intuition for RPA techniques, and can be utilized to greatly reduce the optimization and analysis time of circuit-antenna co-design scenarios. Although the work presented in this paper is limited to the cases of RPAs, the equivalent modeling idea can be extended for possible applications in other microstrip antennas and even microstrip circuits with arbitrarily shaped geometries.

CHAPTER 8 GENERAL DISCUSSION

All the above-presented research developments and innovative solutions are completely free from the lossy and influencing matching networks that are typically present in the frontend active circuits. Besides, a large number of other passive circuitry elements are either eliminated or reduced to realize efficient solutions for implementations in mmW and beyond applications.

The initial interest of this research was to estimate the feasibility of realizing unified circuit-antenna solutions. In this regard, we are intended to replicate the class-A amplifier configuration by replacing its input and output matching networks with multifunctional antennas. For inexpensive trials and demonstration, the prototype is developed at 5 GHz on PCB with commercial transistors. This prototype realized an amplified radiation in a compact space and with absolutely no passive circuit elements.

The aforementioned PCB implementation with commercial transistor has restricted the design freedom to only antennas. On the other hand, system-on-chip implementations provides the flexibility in designing both the active devices and antennas for enhanced performances and their seamless integration. Certainly, they also promise compact, reliable, and low noise solutions for applications at mmW and beyond applications. Since, the size of active devices are generally very small compared to the radiator, multiple active devices can be easily integrated within an antenna, without influencing its performances. On the contrary, the on-chip-antennas are not efficient and power handling capabilities of the active devices are typically limited. Therefore, the paralleled power amplifier-antenna prototype is proposed for high power transmission. The realized prototypes are extremely compact and demonstrated enhanced performances at the design frequency of 146 GHz in CMOS, compared to conventional paralleled amplifier-antenna integration techniques.

Now, that the antenna and active device designs and their integration is explored, the impact of impedances at which they are integrated is studied both in terms of magnitude and phase. Subsequently, this understanding is devised for realizing beam shaping functions in addition to amplified radiation that are suitable for radar, satellite, communication systems, and so on. Only the active devices are integrated with the antenna to realize these functions, thereby avoiding all the typically required amplifier matching networks and phase shifting circuitry.

Finally, a scalable and planar two-dimensional amplifying-array antenna configuration is proposed, that eliminates the dedicated matching networks required for amplifiers and can handle high powers through the paralleled configuration. The large EIRP with fixed radiation achieved through this configuration are suitable for long range line of sight solutions. Moreover, additional phase shifters can be integrated inside the prototype to add beam scanning functionalities.

Undeniably, the present-day researchers are greatly dependent on the commercial simulation platforms to analyze and design the antennas and circuits modules. Fortunately, these platforms can efficiently handle complex simulations, and in general provides accurate results within a limited time. Depending on the simulation platform, they extensively support the design and characterization of either the antenna or circuitry, while their capabilities are limited in handling the other module. As a result, the design of UNICA is carried out in separate design platforms through exporting and importing data, despite the well-developed commercial solvers available today. Although, the proposed equivalent model of antenna facilitates the co-simulation in same platform, this is effective for only initial analysis. Henceforth, there is an immediate requirement for developing the simulation platforms that supports the seamless co-designs of both the circuits and antennas. Once these software's evolve to this stage, we believe that there is a definite scope in realizing more innovative solutions with striking features, at even a much rapid pace.

On the other hand, the elimination of all the passive circuitry components may not be necessary in frequency translation circuits, as the input and output of these circuits are handling different frequency signals. In this case, the circuitry components which are handling higher frequencies can be avoided without touching the circuitry handling lower frequency signals, as the corresponding losses are lower. However, the input circuitry should be carefully placed such that they will not deteriorate the antennas performances.

Although the unified solutions are developed and demonstrated for fewer applications in this work, the idea is general and is suitable for implementation in all applications which range from sensors, smart watches, mobile phones, wireless power transfers, to satellites operating at all frequencies. While not discussed in this work, the desired joint circuiting-radiating functions can also be realized through direct integration of diodes with antennas [215]-[217].

CHAPTER 9 CONCLUSION AND FUTURE WORK

In this dissertation, we have proposed different innovative frontend circuit-antenna integration solutions that are appropriate for emerging mmW and THz range applications. The proposed diverse integration techniques diligently covers the single element, linear array, and even planar array circuit-antenna configurations. Moreover, an equivalent model of RPA is developed to speed up the relevant UNICA designs. The entire range of UNICA solutions demonstrated in this work, along with the mesh-network model developed for RPA are illustrated in Fig. 8.1 for reference and are summarized in detail.

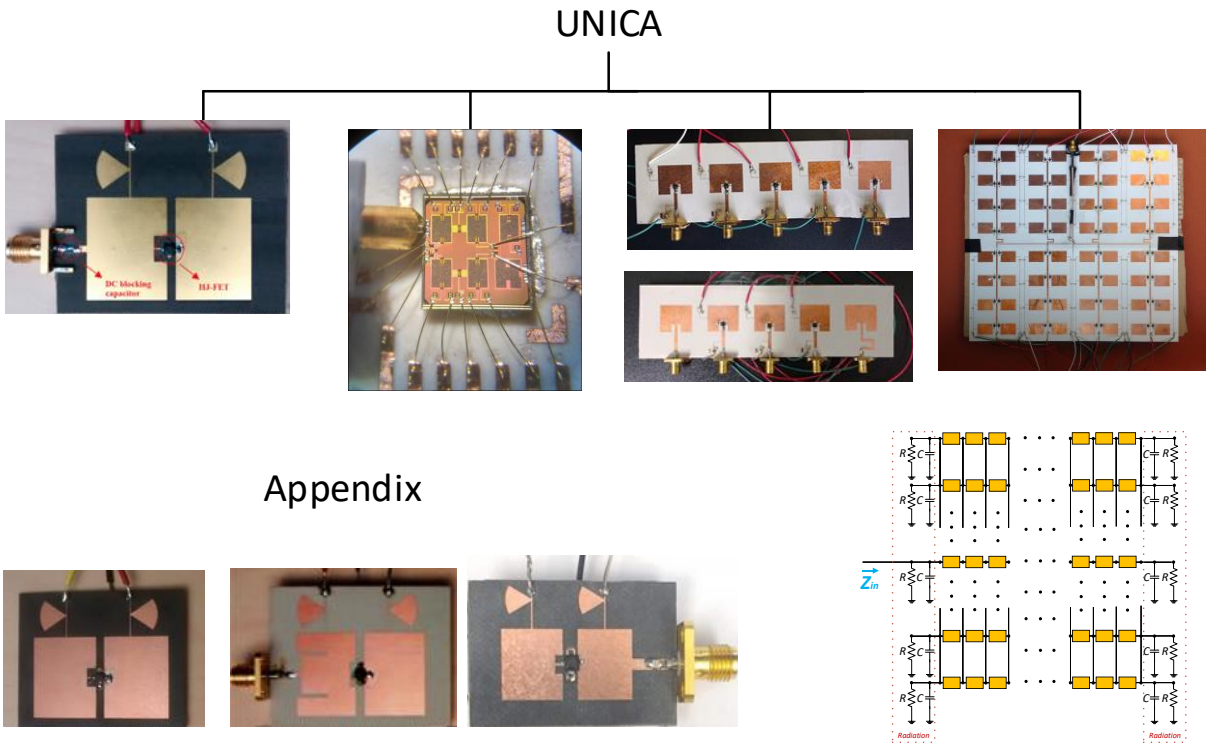


Figure 9.1: Illustration of proposed UNICA models and equivalent mesh-network model of RPA.

9.1 Summary

Chapter 1 overviews the evolution of frequencies over time and the challenges at emerging mmW and THz range frequencies. Following it, the preset day architectural implementations are briefed

and the downsides of them are highlighted. Subsequently, the research direction of this work is proposed along with the motivations, objectives, and organization of this work.

Chapter 2 extensively presents the state-of-art and interesting frontend active circuit and antenna integration techniques available in the literature. They are divided based on the integration level and the pros and cons of each technique are emphasized. Subsequently, the specific contributions of this work are highlighted.

In chapter 3, the ability of RPA to realize majority of the impedances with minimal compromise in radiation efficiency is initially verified. Also, the minimum spacing required between these RPAs arranged in a series array configuration has been presented. Subsequently, the general modelling steps for integration of active device between array elements to realize simultaneous amplification and radiation functions has been presented and verified through a PCB prototype design at 5 GHz. An 11.5 dB amplification and offset radiation beam at $+30^0$ is thereby analyzed through the 1x2 amplifier-array antenna with a commercial active device soldered on it. Moreover, the design of 1x4 amplifying-array antenna layout is also demonstrated to justify the generality of this approach. The different approaches proposed to characterize the realized solutions are also discussed in detail. Eventually, oscillation, wideband amplification and low noise amplification functions have also been realized through this architecture, and are discussed in the appendix.

The deep integration of multiple active devices directly within the antenna has been proposed in Chapter 4. The targeted implementation in CMOS facilitates the optimum design and direct integration of both the transistors and antennas which are the fundamental building blocks. In this regard, the active device design and characterization are discussed, followed by the description of paralleled configuration and losses present in conventional paralleled amplifier solutions. Then, the design approach and comprehensive analysis on multiple transistors integration within the slots etched in the rectangular patch antenna have been discussed. The self-arrangement of these unite cells to realize a 2x2 prototype has also been discussed. These are fabricated, and the measurement results along with the relevant parameters extraction approach are also described. Certainly, they are promising for compact, reliable, and low noise solutions.

A theoretical analysis on the signal coupled from the input to output of a two port network has been initially discussed through generalized S-parameters in Chapter 5. The effective phase shift and

magnitude coupling components with complex load impedances has been thereby described in detail and demonstrated through an example. Following it, the closed form equation to estimate the impedance for a specified magnitude and phase combination has been derived and the corresponding outcomes have been discussed in detail, where the real solution can realize the desired signal coupling. The application of these derived equations to instantly evaluate all the impedances and phase shifts at fixed magnitude coupling, and estimate the phase shift range at each magnitude level has been presented. Then, the general modelling steps involved in the design of amplifying-beam shaping array antenna systems have been presented. Following this, two 1x5 amplifying active array antenna prototypes are developed to realize Chebyshev and flat top beam radiation patterns to prove the concept. The desired array element excitations are directly realized through the integrated active devices alone, thereby eliminating the need for devoted matching networks, and phase shifting circuitries. These solutions are suitable for radar, satellite, communication systems and so on.

Eventually, the extension of such unified solutions to realize two-dimensional amplifying array antenna configurations is proposed in Chapter 6. Correspondingly, different feeding techniques for RPA have been analyzed and non-radiating edge feed technique choice is justified. A physical arrangement of these array elements is thereby proposed to achieve low cross polarization and its utilization in array developments is described. The design procedure, optimization, and extensive-analysis on the 4x2 prototype are then presented, which is followed by the description on its integration with corporate feed network to realize 8x8 prototype. The realized planar solution reduces the number of feed lines, and eliminates the specific matching networks required for amplifying functions. Corporate-series hybrid feeding technique has been utilized in this development, and the feed lines are integrated with the amplifying transistors at appropriate locations which are then interconnected directly with the array elements. The rectangular patch array elements are fed on the non-radiating edge and the integrated active devices are activated through DC lines on the same board. The higher EIRP with fixed radiation achieved through this configuration are appropriate for long range line of sight applications.

Chapter 7 starts with an overview of different equivalent models available for RPA in the literature and their deficiencies for implementation in UNICA solutions. A further analysis on RPA is performed to understand its behavior and is discussed. Subsequently, a mesh-network equivalent

model is proposed by dividing RPA into sections and appropriately interconnecting them, and the relevant general modelling procedure is presented. Following it, its implementation of the proposed model to evaluate the RPA performance with various slots, multiport, vias, multimode and feed positions has also been proposed. All of these solutions are further verified through comparison of simulations, equivalent model, and measurement results.

Chapter 8 presents the general discussion of this work.

Chapter 9 concludes this work and proposes the future research directions.

In conclusion, all the proposed deeply integrated circuit-antenna architectures and equivalent model of RPA have been extensively studied, and all the necessary analyses and general modeling steps are presented. All these proposed solutions are further validated through experimental measurements and demonstrated promising results.

Although the unified solutions are developed and demonstrated for fewer applications in this work, the idea is general and suitable for implementation in all applications which range from sensors, smart watches, mobile phones, wireless power transfers, to satellites operating at all frequencies. We thereby strongly believe that this research work will motivate the researcher's insights towards the co-designing of circuits and antennas as a single entity, instead of considering them as independent modules. Eventually, these solutions even have the potential to revolutionize all the future wireless systems implementations.

9.2 Future work

This emerging integration technique opens up an endless ways of developing the future unified circuit-antenna solutions, while a few are descried here that might be of interest for the readers and our future work;

- As demonstrated in this work and in the literature, the antennas can be designed to perform simultaneous matching and harmonic tuning circuitry functions in addition to radiation. As a result, there is a scope for realizing simultaneous non-linear power amplification and radiation through a unified space and achieve higher power added efficiency. The corresponding fundamental and harmonics control features will also facilitate the frequency multiplication based UNICA solutions.

- On the other hand, filtering antennas are also being developed to supress a frequency or a band of frequencies. Subsequently, the simultaneous filtering and impedance tuning through antenna, along with the feasibility to directly integrate active devices with it can enable self-oscillating mixing UNICA designs with image rejection capabilities.
- Instead of confining the active device integration with a single mode of antenna, the feasibility for its integration with the orthogonal modes of the same antenna can also be explored.
- In addition to realizing the active circuitry functions along with radiation, the potential ways of optimizing the circuitry parameters of phase noise, bandwidth and so on is worth studying. Furthermore, UNICA solutions can effortlessly be developed for reconfigurable applications and can be exploited for a large number of smart systems.
- A microstrip rectangular patch antenna that radiates along broadside is proven as a promising radiator configurations for the UNICA solutions. Nevertheless, the potential active device integration with the other antenna configurations can be explored. For example, antennas such as slot, dipole, PIFA and so on can be studied for omnidirectional radiation performance and Yagi-Uda can be analyzed for end fire radiation.
- The radiation pattern switching functionalities can be conveniently realized through UNICA based array elements that can be placed closely. Subsequently, switching on-off a certain section of the array antennas through dc bias lines would facilitate the beam switching, which can easily be established.
- The commercial active devices utilized in this work have exhibited limited phase change with bias, which has restricted the beam steering range, although such a feature is reported. Therefore, the beam steering range can be improved by designing active devices that can rapidly change phase with bias tuning. Eventually, phase shifter-less phased array antenna solutions may be developed if such active devices can be put forward, which is worth analyzing.

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APPENDIX A ARTICLE 6: A NOVEL APPROACH FOR MODELLING OSCILLATOR CIRCUIT WITH ANTENNAS

Srinaga Nikhil Nallandhigal, Ke Wu

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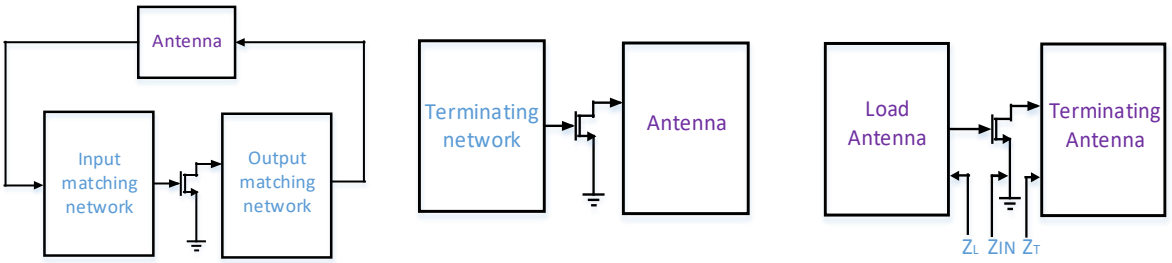
This paper presents an approach to unify oscillator circuit and antenna for future mm wave systems. Here, the passive circuitry present on both sides of transistor in an oscillator circuit are replaced by antennas. The prototype consists of two antennas arranged in a linear array with transistor placed in the spacing between them. General modelling procedure is reported followed by proof of concept demonstration at frequency of 5 GHz. Frequency tuning up to 70 MHz is aslo achieved around 5 GHz from measurements and maximum radiation is observed at beam steered angle of -20^0 with respect to broadside, from simulation. Transmission line model of the same is developed to reduce the time for initial analysis and optimization, and presented here.

Introduction



(a) (b) (c)

Figure A.1. Block diagram of (a) feedback oscillator AIA (b) negative resistance oscillator AIA and (c) proposed negative resistance oscillator circuit antenna.

Active integrated antennas (AIAs) is an eminent concept, which involves integration of active circuit and antenna on the same substrate [1]. Although, numerous innovative designs have been successfully demonstrated covering all frequencies, the concept is particularly attractive for mm wave systems as they solve the issues of, interconnection and feed losses, limited source power, efficiency, in-efficient phase shifters etc. [2, 3].

AIAs that integrate microwave oscillator circuit with radiating structures are referred as oscillator type AIAs, which are compact and light weight. The two widely adapted techniques of designing these oscillator type AIAs are (a) feedback oscillator type- wherein antenna operates as a frequency selective module in the feedback path of amplifier circuit, in addition to radiation [4, 5], as shown in Fig. A.1(a), and (b) negative resistance oscillator type - wherein antenna acts as a passive load satisfying the oscillation conditions, to the negative resistance resulted by the unstable terminating oscillator network [6, 7], as shown in Fig. A.1(b). All these models still retain a part of circuitry and interconnections nearby radiator which is not advisable at mm wave frequency, as they include huge loss and their size becomes comparable to radiator affecting the overall radiation performance.

We therefore propose the removal of circuitry and interconnections for designing efficient mm wave front ends. This is realized by utilizing two antennas to provide the necessary circuit operations in addition to radiation and connecting the transistor directly at the edge of both antennas as shown in Fig. A.1(c). This prospected model works as oscillator and antenna simultaneously, and can be referred as 'oscillator circuit antenna (OCA)'. This simple design offers additional advantages of, improvement in radiation performance, low loss, high efficiency, higher integration, fixed beam steered radiation, frequency tuning etc. compared to traditional models.

In this paper, we cover the basic theory, general modelling procedure and demonstration of working model at a low frequency of 5 GHz, to prove the concept. We also present the transmission line model of OCA which is a time effective alternative for initial analysis and optimization.

Oscillator Circuit Antenna (OCA)

The proposed OCA is guided by negative resistance oscillator theory and is briefly discussed in this section followed by general modelling procedure and design of proposed OCA.

A. Negative Resistance Oscillator

Consider a closed loop circuit with load impedance '$Z_L(\omega)$' and input impedance '$Z_{IN}(A, \omega)$' similar to Fig. A.1(c) , with current 'I' flowing through it. Applying KVL for this closed loop circuit results in equation (A1)

$$[Z_{IN}(A, \omega) + Z_L(\omega)]\, I = 0 \qquad \text{(A1)}$$

To satisfy equation (A1), either current should be zero or the sum of impedances should be zero [7]. In the case of oscillation, current cannot be zero and so, the sum of impedances is zero as given in equation (A2), at oscillation frequency 'ω_0' and amplitude 'A_0'

$$R_{IN}(A_0, \omega_0) + R_L(\omega_0) = 0 \text{ and}$$

$$X_{IN}(A_0, \omega_0) + X_L(\omega_0) = 0 \quad \text{(A2)}$$

As the oscillation amplitude increases, the input impedance varies and so, the practical value for R_L which maximizes the oscillation power and widely adapted condition for start of oscillation around design frequency is given by equation (A3) [8].

$$R_L = |R_{IN}(0, \omega)| / 3 \text{ and}$$

$$X_L(\omega_0) = -X_{IN}(\omega_0) \quad \text{(A3)}$$

B. General Modelling Procedure

The procedure for designing negative resistance oscillator circuit available in [8] is slightly modified to include antennas, and is described below.

1. The potential unstability of transistor is initially verified at design frequency. Stability circle of terminating port is then drawn to identify the unstable region in smith chart.
2. The terminating impedance is chosen in the unstable region and is achieved by terminating antenna.
3. Then, the input impedance at gate of transistor is calculated with terminating antenna connected to drain. The resulting input resistance is negative.
4. The load antenna is then designed to satisfy the start of oscillation conditions (equation (3)).
5. The spacing between array elements is chosen for minimum mutual coupling and to fit the transistor utilized.

Once the two antennas are designed individually, they are verified for consistency of impedance performance in the presence of mutual coupling and optimized, if necessary.

C. Proposed OCA

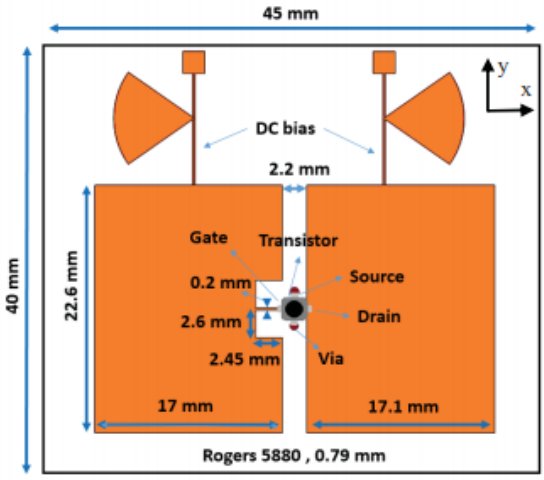
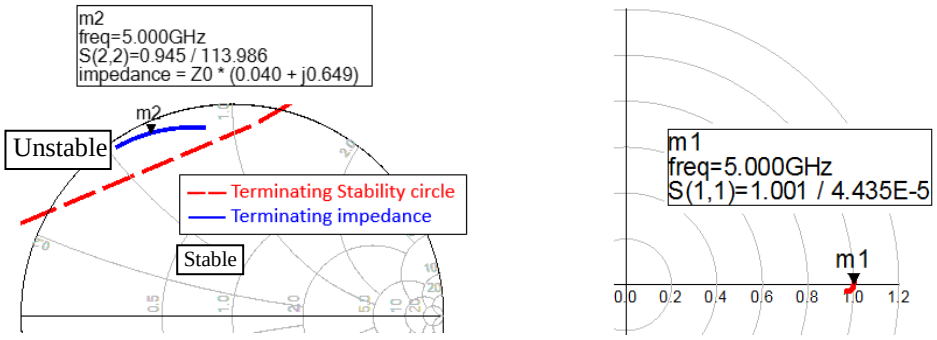


Figure A.2: Proposed OCA.

Planar radiating structures like microstrip patch antennas are easy to fabricate, flexible for design modifications to satisfy the impedance demand of oscillator circuit by still maintaining good radiation performance and also have significant applications. Therefore, rectangular patch antenna is chosen along with Rogers 5880 substrate of 0.79 mm thickness and CE3512K2 (HJ-FET) transistor to model the OCA at 5 GHz following the procedure described. The final model of designed OCA with all dimensions marked is shown in Fig. A.2.



(a) (b)

Figure A.3: (a) Smith chart showing the stability circle and impedance of the terminating antenna and (b) polar plot showing the gain and phase.

The transistor chosen has 'K = 0.759 < 1' and 'B =1.230 >0', implying that it is potentially unstable. Then, stability circle at the terminating port (at drain) of transistor is drawn in smith chart and the unstable region is identified. The antenna to be terminated is first designed at frequency of 5 GHz, where reactance is zero, and then the length is decreased to realize low resistance and inductance necessary to terminate the transistor in unstable region. Terminating impedance of 'Z_T = 2+j32.45 Ω' is realized at 5 GHz by this antenna. Terminating stability circle, stable region, unstable region and the impedance of terminating antenna (plotted from 4.8 GHz to 5.2 GHz) realized in the unstable region is shown in Fig. A.3(a).

Input impedance of 'Z_{IN} = -3.5-j88 Ω', is obtained at the gate terminal of transistor with terminating antenna connected to drain. The load impedance necessary to start the oscillation is 'Z_L = 1.16+j88'. This impedance has low resistance and high inductance, which is similar to the impedance of terminating antenna. Following the similar design procedure as terminating antenna, load antenna length is decreased to realize the impedance, but couldn't achieve it. So, a microstrip line of minimum width possible for fabrication (0.2 mm) is utilized as an inset feed to achieve low resistance and high inductance, by varying the length of it. This resulted in load antenna impedance to be 'Z_L = 1.45+j85 Ω', which is close to the required one. The width of terminating antenna and load antenna are designed for maximum radiation and are equal. Throughout the design, it is always ensured that radiation performance of both the antennas are satisfactory at design frequency.

Spacing between two antennas has to be at least two times of minimum spacing - 2 X ΔL (ΔL is due to fringing fields of patch antenna and is given in equation (4) [9]), to minimize the direct coupling between two patches in series configuration. This spacing should also perfectly fit the transistor chosen as it connects the edge of both the patch antennas.

$$\Delta L = 0.412 \frac{(\varepsilon_{reff}+0.3)\left(\frac{W}{h}+0.264\right)}{(\varepsilon_{reff}-0.258)\left(\frac{W}{h}+0.8\right)} \quad \text{(A4)}$$

Antennas involved are designed in ADS momentum, exported and co-simulated with transistor model in schematic of ADS. HB simulation is performed to characterise the OCA. Fig. A.3(b) shows the oscillator test result of designed OCA, showing the encirclement of 1+j0 point, which confirms the oscillatory behaviour at design frequency of 5 GHz.

It is also known that oscillation at one port of transistor induces oscillation on other, resulting in signal at both the ports. OCA proposed has antennas on both ports and they radiate as an array, thus achieving higher efficiency by radiating more power, constructive radiation, beam steering to a fixed angle due to phase and amplitude difference fed for both antennas, and increased integration by utilizing the space between array elements to place transistor. These are the unique features of the proposed OCA compared to all existing proposals.

Equivalent Transmission Line Model

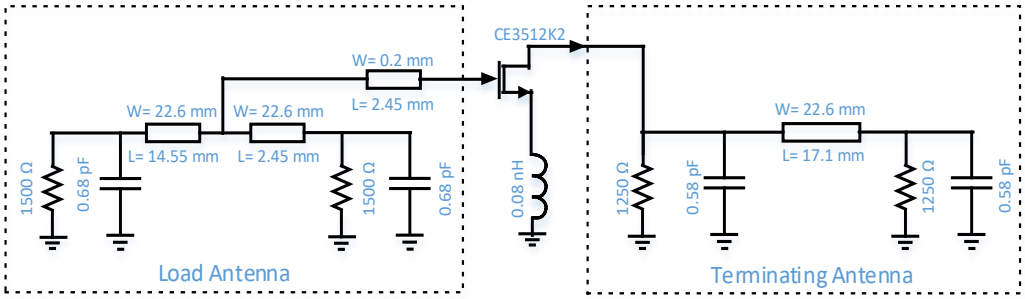


Figure A.4: Transmission line model of OCA.

The antennas involved in OCA are designed in 3D software's like CST MWS, HFSS etc. or 2.5D momentum. Then, the antenna is exported as S-parameter model to schematic of ADS and co-simulated with S-parameter model of transistor for oscillator circuit analysis. This is naturally a tedious process and optimization is laborious.

In this regard, an equivalent transmission line (TL) model of patch antenna will be of immense help, as the entire OCA can be simulated in schematic. The analysis by varying each parameter and optimization can be quickly done as a first step in schematic. Once we achieve a reasonable result, we can extract the equivalent patch antenna based on the final parameters and repeat the regular design procedure. This saves a lot of time and effort in modelling OCA.

Papers [10, 11] present very good description and necessary equations to realize the TL model for individual patch antenna. Patch antenna is considered as two slots separated by the length of patch, to calculate necessary equations. Using those equations, slot conductance, G_1 is calculated to be 0.0014 ℧ and mutual conductance between slots of patch, G_{12} is calculated as 0.000645 ℧, resulting

in final resistance of 1325 Ω. The slot capacitance is calculated to be 0.44 pF. These values are almost same for both the antennas involved, as their lengths are approximately same.

The mutual coupling between two antennas is negligibly small and no additional circuitry is necessary for mutual coupling. However, the calculated values are slightly tuned for perfect matching of TL model results with antennas at the design frequency, in the array environment. S2P file of transistor is chosen and the grounded via acting as inductive source degeneration is also included. The final TL model obtained is shown in Fig. A.4 and matching of admittances at the input of two antennas with equivalent model are shown in Fig. A.5.

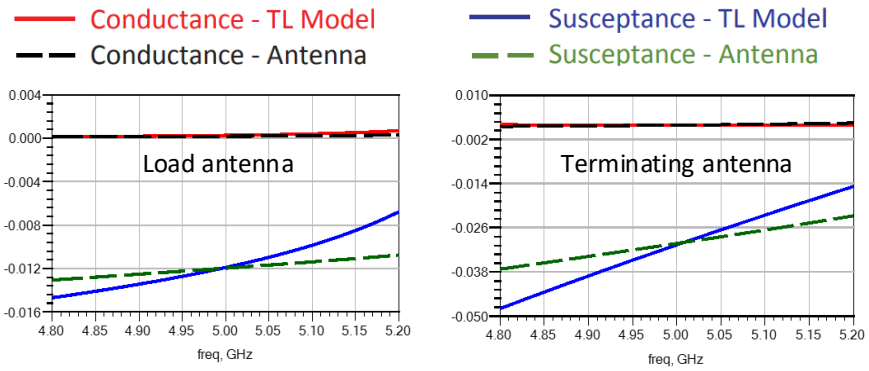
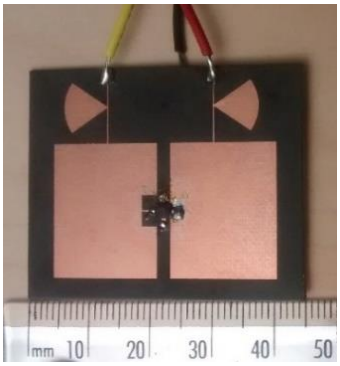


Figure A.5: Comparison of admittances for antennas designed and transmission line model developed.

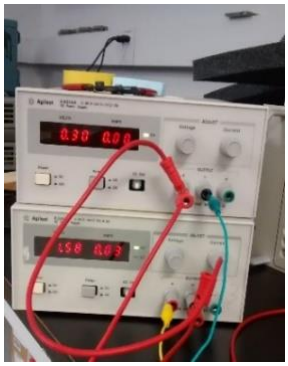
Results and Discussion

The fabricated OCA is shown in Fig. A.6(a) and DC bias for oscillation at 5 GHz is shown in Fig. A.6(b). For measurement, the OCA fabricated is fed with DC and oscillated signal radiated by it is received by a co-polarized horn antenna placed at a distance of 60 cm and connected to spectrum analyzer. Fig. A.6(c) is the output on spectrum analyzer window, showing the received signal at 5.00004 GHz with power of -48 dBm, proving the concept.

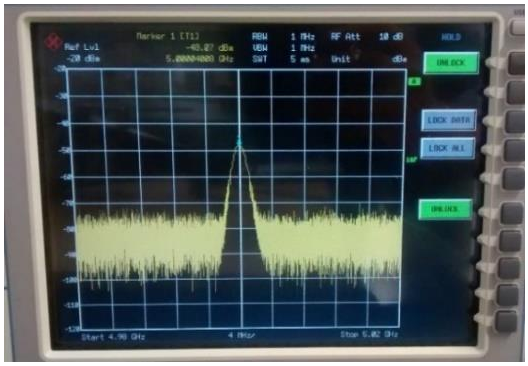
Simulated normalized radiation pattern at 5 GHz shows the beam steering at -20^0 in the E plane, as shown in Fig. A.6(d), which is attributed to phase and amplitude difference in the signal fed to both the antennas. H plane pattern is symmetrical and maximum cross-polarization (at $\Phi = 45^0$) of -16 dB is observed which are also plotted.



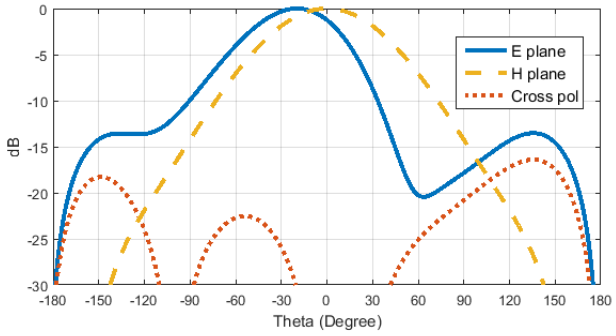
(a)



(b)



(c)



(d)

Figure A.6. (a) Fabricated OCA (b) DC bias showing the gate and drain voltage (c) received power shown in spectrum analyzer (d) simulated radiation pattern.

Freqeuncy tuning around 70 MHz is achieved by varying bias. The bias conditions and oscillation freqeuncy along with corresponding received power level are presented in Table A.1.

Table A.1: Variation of oscillation frequency with bias

V_{GS}	V_{DS}	Oscillation frequency (GHz)	Received power (dBm)
0.30	0.82	4.96	-49
0.30	1.58	5.00	-48
0.44	2.51	5.03	-48

To achieve better control on impedance of each antennas in array environment, mutual coupling can be futher decreased by adopting various techniques like EBG structures, defective ground

planes etc. However, notable disadvantge of this particular model is, minumum control on the power radiated through higher order modes and solution for it is under research.

Conclusion

This paper proves the concept of designing oscillator circuit utilizing only antennas and a transistor at 5 GHz. Antennas involved here operate as both circuit and radiator. This configuration promises additional advantages of low loss, constructive radiation, increased efficiency, and fixed beam steered radiation compared to existing models. Frequency tuning is also observed for design by varying bias. The transmission line model of the same is presented, to carry out the initial analysis, which saves time of parametric analysis and optimization. Planar array can be modelled by such OCA cells to achieve quasi optical power combining for high power transmission. Although, they can be implemented at any frequency, they are particularly attractive at mm wave frequencies.

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APPENDIX B ARTICLE 7: WIDEBAND FRONT-END INTEGRATION AND UNIFICATION OF CIRCUIT-ANTENNA FOR SIMULTANEOUS STABILIZED AMPLIFICATION AND STEERED RADIATION

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A wideband front-end integration of amplifying transistor within array antenna is proposed, analyzed and demonstrated in this paper, for simultaneous stabilized amplification and beam steered radiation, in a unified space. Source degeneration inductance realized through via is studied, from which appropriate via is utilized for stabilization. In addition, E-shaped patch antenna is used as the input matching network to enhance the impedance matching bandwidth, which also radiates. The prototype model is fabricated, and the measured results agree very well with simulated counterparts. This unified prototype has the amplification gain varying form 10 dB to 8 dB across the matching bandwidth of 13.5 %, along with beam steered radiation at $+35^0$, observed from experiments. Furthermore, frequency tuning and related radiation performance realized through varying DC bias from measurements are also presented.

Introduction

Compact, multi-functional, and low-loss front-end modules are attractive for all wireless applications including 5G, radar sensing and imaging. Active-integrated-antenna has been the focus of research and development over years for realizing these requirements, and numerous designs are readily available [1]. However, major limitations are still the losses arising from feed lines, interconnects, matching networks, as well as the proximity circuits that affect the radiation performance of antennas.

Recently, a UNified Amplifying Circuit Antenna (UN-ACA) has been proposed and demonstrated to overcome these electrical and structural limitations [2]. In this newly devised scheme, antennas operate as matching networks in addition to radiation functions, and active devices perform

amplification and other desired operations. This low cost planar configuration offers additional advantages of constructive radiation, improved efficiency, and effective use of spacing and mutual coupling between array elements. However, the stability issue has not been addressed, and the proposed UN-ACA front-end is designed at a particular frequency thereby demonstrating a narrow-band response.

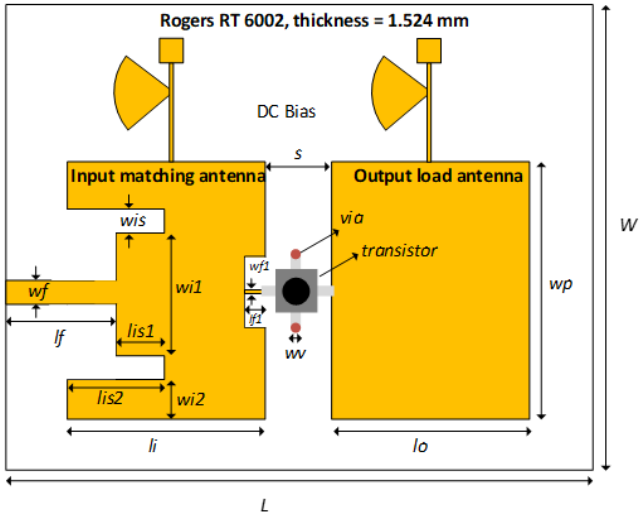


Figure B.1: E patch UN-ACA (a) top view: *L*= 50 mm, *W*= 45 mm, *lf*=8.8 mm, *wf*= 1.22 mm, *li*= 16 mm, *wis*=1 mm, *lis1*= 6.8 mm, *wi1*= 10.5 mm, *lis2*= 7.8 mm, *wi2*= 5 mm, *lf1*= 1.7 mm, *wf1*= 0.2 mm, *d*= 0.8 mm, *s*= 2.4 mm, *lo*= 16.5 mm, *wp*= 22.6 mm and *C*=30 pF, and (b) side view.

This paper presents techniques for addressing both stability and impedance matching bandwidth issues in the development of UN-ACA. The stability is improved by a proper deployment of via, and the matching bandwidth is enhanced by utilizing a planar E-shaped patch antenna [3] as far as the input matching antenna is concerned. The top view of the proposed prototype, and the side view displaying the surface mounted transistor and its via are all illustrated in Fig. B.1(a) and B.1(b), respectively. Although the E-shaped patch antenna is presented as an example, the solution is not limited to it, and other bandwidth enhanced antenna configurations can also serve the purpose. In this work, a detailed analysis for stability and bandwidth enhancement is presented, followed by a experimental prototype demonstration and comparison of simulated and measured results, along with concluding remarks.

Stability

Majority of the currently available commercial transistors are potentially unstable, thus requiring the designers to load them with a restricted set of impedances for stability. However, this restricted set of stabilizing impedances may not be realizable by radiating antennas alone (acting also as circuits) in all the cases. Henceforth, the stabilization of transistor enhances the stable impedances range, thereby providing an additional flexibility for antenna design in UN-ACA.

This work adopts a series feedback method for stabilization, which can be realized without resorting to any additional components. In this method, an inductor is included in the source path of common source circuit to generate a negative feedback and thus improve stability [4, 5], with minimal effect on source current and noise performance, and also enhancement of linearity. However, transconductance is reduced, resulting in a decrease of amplification gain.

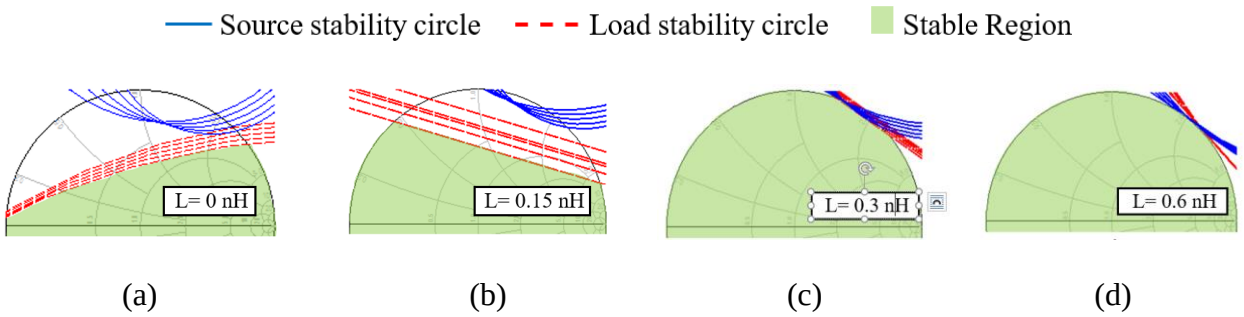


Figure B.2: Source and load stability circles with (a) no via (b) via diameter d =1.6 mm via (c) via diameter d = 0.8 mm and (d) via diameter d = 0.4 mm.

Active device, FET-CE3512K2 utilized in this work is surface-mounted on Rogers 6002 substrate of 1.524 mm thickness for the design of modified UN-ACA. Via connecting source terminal of transistor (placed on the patch layer) to the ground acts as an inductive degeneration, and is optimized for strengthening the stability. The diameter of via d is the only adjustable design parameter in this case as its length is pegged to substrate thickness. The stability circles and corresponding stable regions are highlighted on the Smith chart, as described in Fig. B.2(a) - Fig. B.2(d) for transistor without via, and with via of various diameters, along with equivalent via inductances. Such results suggest that by decreasing the via diameter, i.e. increasing the inductance, one can create a unconditionally stable transistor, thereby increasing the impedance choices for

UN-ACA design. However, our fabrication facility imposes a limitation on the achievable minimum slot diameter to 0.8 mm, and is therefore chosen which almost stabilizes the transistor.

Input Matching Circuit Antenna

An E-patch antenna operating simultaneously as input matching network and radiator is designed to resonate at both 4.9 GHz and 5.2 GHz. Dual-frequency resonance achieved by this antenna can be better explained through its surface current distribution. For a rectangular patch antenna, its surface current varies a half cycle along the length of patch, which determines the resonance frequency. Therefore, patch length l_i that gives the first resonance frequency i.e 5.2 GHz is calculated from (B1) [6].

$$l_i = 0.49\,\frac{\lambda}{\sqrt{\varepsilon_r}}\,,\; f = \frac{c}{2L\sqrt{\varepsilon_r}} \tag{B1}$$

For the E-shaped patch antenna, part of current flows along the patch length and resonates at 5.2 GHz. In addition, the slots created along the geometry forces the other part of current to flow around them resulting in an increase of the current path length, and thus the emergence of an additional resonance at a lower frequency of 4.9 GHz [7]. At lower resonant frequency, slot length has to be slightly greater than its quarter wavelength to compensate the circulation of current around it, and the guiding equation for its design is (B2) [8]

$$l_e = l + \left(\frac{0.4l}{\sqrt{\epsilon_{re}}}\right)\,,\; f = \frac{c}{4l_e\sqrt{\varepsilon_{re}}} \tag{B2}$$

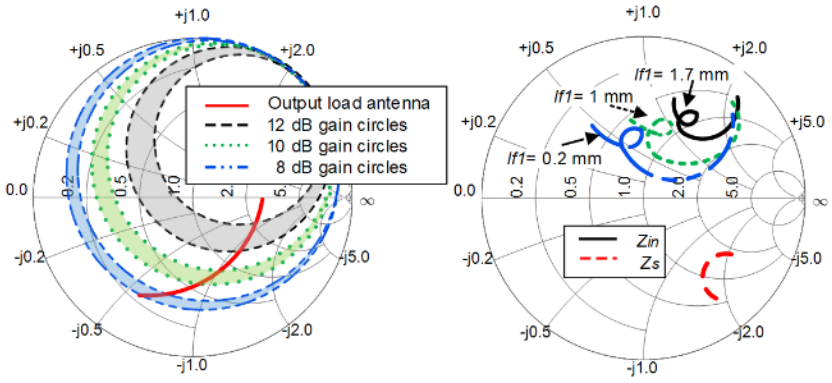
where 'ε_{re}' is calculated using averaged widths on either side of slots [3, 9]. Furthermore, microstrip inset feeding is considered for the design to realize planar structures.

Modified UN-ACA

For the stabilized CE3512K2 transistor, gain circles from 8 to 12 dB are drawn in the desired range. The gain circles for 8 dB, 10 dB, 12 dB at extreme ends of the desired range (at 4.8 GHz and 5.5 GHz) are shown in Fig. B.3(a), with the intermediate frequencies (between 4.8 GHz and 5.5 GHz) gain circles region highlighted.

The output load antenna is then designed to have the load impedance Z_L overlapping these gain circles (as shown in Fig. B.3(a)), by tuning the resonant length of the patch antenna. Subsequently,

the drain terminal of transistor is connected to the designed output load antenna, and the input impedance Z_{in} at the gate terminal of transistor is calculated, and shown in Fig. B.3(b).



(a) (b)

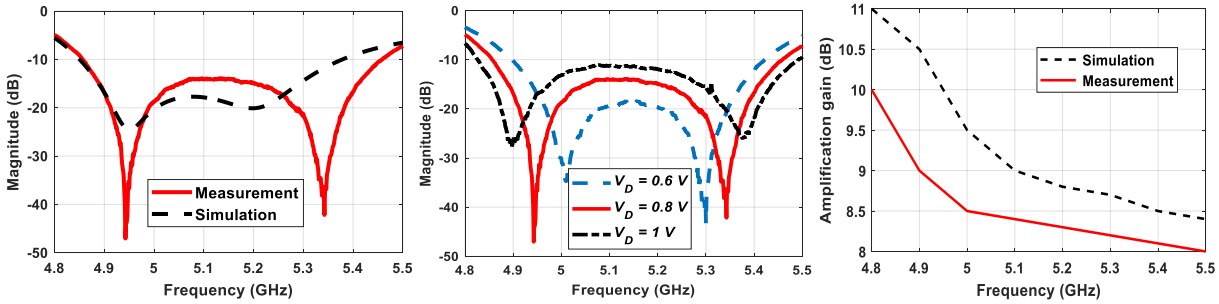
Figure B.3: Smith chart representing (a) gain circles and output load antenna impedance Z_L and (b) input Z_{in} and source Z_S impedance.

The input matching antenna is then designed in the presence of the output load antenna to conjugate-match the input impedance $Z_S = Z_{in}^*$ on one end, and transform to 50 Ω feed impedance on the other end. The E-shaped patch antenna is designed here to match the input impedance simultaneously at two nearby frequencies. The slots incorporated in the patch and the patch length offers a flexibility to control the impedances independently at these two frequencies, while maintaining the radiation performance. From simulations, it is observed that a simple E-patch antenna could not provide the necessary impedance matching and so, two additional modifications are included; (1) microstrip line of minimum width possible for fabrication is added at the gate terminal edge of E-patch to satisfy the conjugate matching, which also acts as an inductance forcing it to radiate higher power. The corresponding impedance variation modifying the micostrip line length lf_1 (with width fixed at 0.2 mm) is shown in Fig. B.3(b), and (2) a quarter-wave impedance transformer is used as the feed line for matching.

The spacing between the array elements is utilized to accommodate the transistor, resulting in increased density of integration. A slot of 0.7 mm is etched at the centre of feed line to mount capacitor C of 30 pF which blocks DC from entering the measurement system. Here, the input

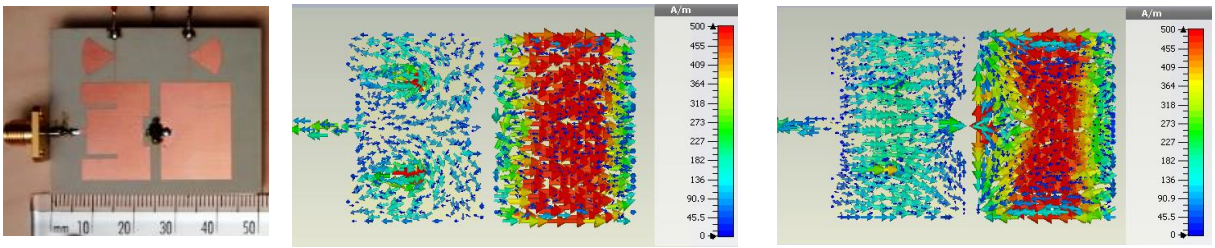
matching antenna radiates 50% of the input power, and the rest is fed to transistor for amplification. The output load antenna and the input matching E-patch antenna have a minimum radiation efficiency of 96% and 87%, respectively across the bandwidth.

Results and Discussions



(a) (b) (c)

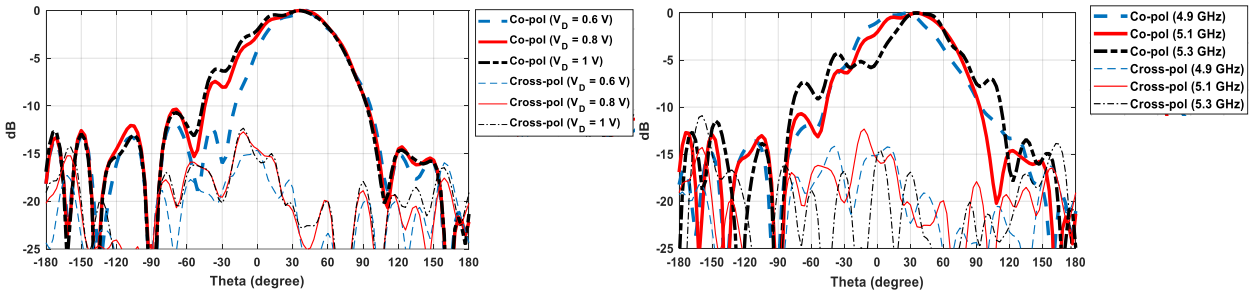
Figure B.4: (a) Comparison of matching in co-simulation and measurement (c) impedance matching varying the drain bias and (b) comparison of measured and simulated amplification gains.



(a) (b) (c)

Figure B.5: Co-simulated current distribution on modified UN-ACA at (a) 4.95 GHz and (b) 5.35 GHz.

The comparison of co-simulated and measured matching response at drain bias V_D=0.8 V and gate bias V_G=-0.2 V is shown in Fig. B.4(a). Reflection coefficient variation with V_D change is presented in Fig. B.4(b), at constant V_G=-0.2 V. Maximum bandwidth up to 13.5 % is achieved by such a configuration. Amplifier analysis is performed in ADS platform, with the exported S-parameter model of antenna designed in CST-MWS and transistor S-parameter model. Simulated amplification gains (across the input signal fed to antenna and at the drain terminal of transistor) varies from 11 dB to 8.45 dB, and measured results vary from 10 dB to 8 dB, across the band as shown in Fig. B.4(c).



(a) (b)

Figure B.6: Normalized measured E-plane radiation performance of modified UN-ACA (a) varying drain bias at 5.1 GHz. and (b) for different frequencies at fixed bias.

The fabricated prototype is shown in Fig. B.5(a). Co-simulated surface current distribution of the modified UN-ACA at the two measured resonant frequencies of 4.95 GHz and 5.35 GHz, (as shown in Fig. B.5(b) and Fig. B.5(c), respectively), visualizes an amplified signal on the load patch antenna, compared to the signal on the input matching antenna. A smaller amplification at 5.35 GHz compared to 4.95 GHz can also be observed from the current intensity. Furthermore, the current distribution visualizes the perturbed path at 4.95 GHz, and along the patch length at 5.35 GHz as expected in the input matching E-patch antenna.

Normalized measured radiation performance in the E-plane of the modified UN-ACA at different frequencies for constant V_D = 1 V and V_G = -0.2 V is plotted in Fig. B.6(a), and varying drain bias at a fixed frequency of 5.1 GHz (as an example) is shown in Fig. B.6(b). Beam steered performance (nearby $+35^0$) observed in both cases is due to difference in amplitude and phase of input signal fed to the two array elements. As frequency increases, the phase difference is increased for the same length of patch resulting in a beam steering to a larger angle as observed. On the other hand, increase in drain bias would increase amplification resulting in the removal of nulls, and nearly no phase difference (of the commercial transistor) for each bias condition results in a negligible beam steering.

Conclusion

This paper has presented a method to improve stability of the modified UN-ACA by properly choosing the via diameter which acts as inductive source degeneration, and also the use of a E-

shaped patch antenna as the input matching antenna for enhanced matching bandwidth performance. The designed modified UN-ACA has achieved a bandwidth of 13.5%, and its amplification gain varies from 10 dB to 8 dB across the band. The beam steered radiation to $+35^0$ is due to the difference in amplitude and phase of signal fed to the two antennas arranged in an array. Further beam steered radiation by varying frequency is due to the difference in phase of signal fed to the two antennas arranged in an array. However, the beam is not steered significantly by varying bias at all frequencies, as the corresponding phase shift of transistor is almost constant.

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APPENDIX C ARTICLE 8: LOW-NOISE AND SMALL-SIZED RECEIVER FRONTEND WITH UNIFIED CIRCUIT-ANTENNA INTEGRATION

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In this paper, a low-noise and small-sized receiver frontend is proposed through unified integration of transistor in between array elements. The general modelling steps in connection with this unification are described, followed by a prototype design at 10 GHz as an example. Subsequently, the noise figure formulation of both active integrated antenna (AIA) scheme and unified circuit-antenna solution are analyzed through supporting equations. The prototype is fabricated, and the measured results agree closely with simulated results. This circuit-antenna unification is able to realize 15% impedance matching bandwidth, and 11.8 dB amplification gain. It has also demonstrated a reduction in both noise figure and size by 1 dB and 45% respectively, compared to the AIA counterpart.

Introduction

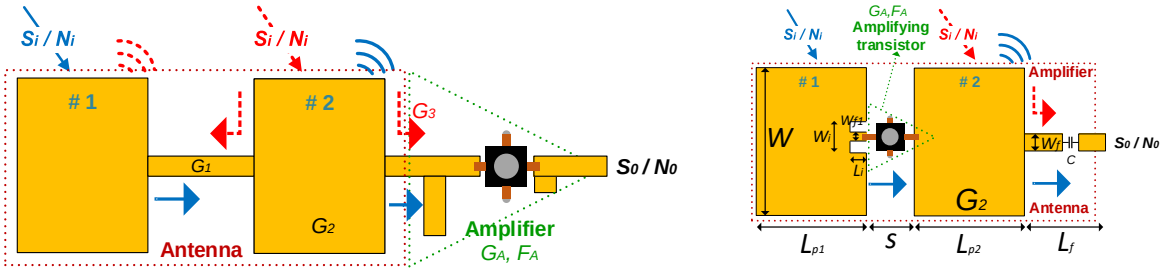


Figure C.1: (a) AIA-based low-noise receiving frontend and (b) proposed frontend unification of low noise amplifying transistor in array antenna: L_{p1} = 400 mil, L_{p2} = 360 mil, W = 450 mil, W_{f1} = 15 mil, L_i = 55 mil, W_i =120 mil, W_f = 70 mil, L_i = 300 mil, s = 100.

Compact, efficient and cost-effective wireless modules are in persistent demand for emerging applications of imaging, radar, space and 5G, all of them operating in the RF, microwave and millimetre-wave (mmW) range. Motivated by such requirements, the research and development regarding the frontend architecture underwent a structural transformation, from conventional architecture of assembling independent and discrete antennas and circuits to active integrated antennas (AIAs), where active circuits are co-designed with antennas.

Moving on to the AIA techniques in the development of receivers, work has been done in integrating a low-noise amplifier circuit (with input and output matching networks) with a single antenna [1]-[4], or an array antenna [5] (as shown in Fig. C.1(a)), through microstrip lines. Although this approach has demonstrated a well-appreciable enhanced performance, there are still significant losses from line interconnections (between antenna and amplifier), feed lines (connecting array elements) and matching networks. Such first-stage-related losses would degrade the receiving noise performances. Furthermore, radiation pattern disturbances or interferences from proximity circuits could be significant and more prevalent at mmW and in low-gain scenarios. In addition, for series AIA arrays, the signal received through intermediate array elements (for example, array element 2 in Fig. C.1(a)) is divided into two parts, with a part of the signal travelling back and radiated through array elements before it (array element 1 here), and the rest is fed to the output. This loss is more pronounced in larger arrays that are typically required in the design of mmW modules, thus demanding the development of alternative and better configurations.

The recent demonstration of unified and integrated circuit-antenna configuration seems to be a promising solution in this direction, removing line interconnections, feed lines and matching circuits as described in [6],[7]. Henceforth, this unification scheme is adopted for the design of a low-noise planar receiver frontend, as shown in Fig. C.1(b). The array elements present here serve as both radiators and matching networks, thereby resulting in a size-miniaturized, efficient and cost-effective solution. Furthermore, this architecture reduces the amount of back-coupled signal (received from array element 2 in Fig. C.1(b)) that may be radiated through the array elements (for example, array element 1 in Fig. C.1(b)) before it, thanks to the unilaterality transistor integrated between them. In addition, the introduction of amplifying transistor just after the array element 1 significantly reduces the overall noise figure (NF) of the system while still amplifying the signal.

In the scope of this work, the general modelling steps and the prototype design at 10 GHz are presented as an example. Subsequently, the NF formulation for both AIA and UNICA approaches is discussed along with the derived supporting equations. Finally, the simulated model along with reference transmitting antenna, simulation results, fabricated prototype and measured results are all presented and discussed, followed by concluding remarks.

UNICA Prototype

The demonstrative prototype consists of rectangular patch antennas as radiators, designed on Rogers 5880 substrate of 30 mil thickness, and active device FET-CE3512K2. The antenna design is performed in CST-MWS platform, and the amplifier and matching network analysis in Keysight ADS platform. In addition, co-simulation is carried out in CST schematic to study the effective radiation performance and field distribution.

General modelling steps

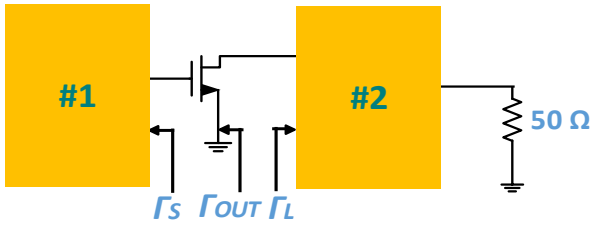


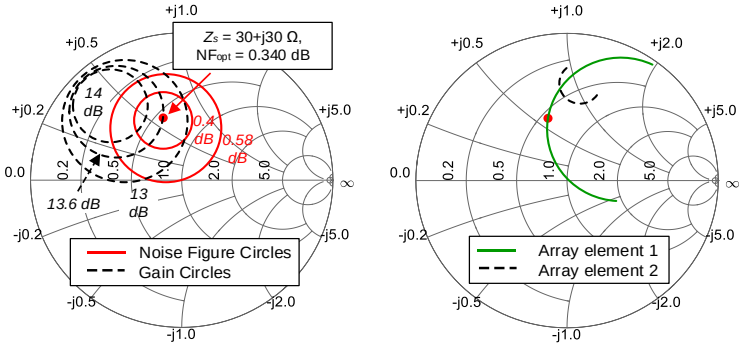
Figure C.2. Block diagram of UNICA with parameters illustration.

The general modelling steps are described here with necessary parameters that are illustrated in Fig. C.2.

1. Initially, the stability of transistor is analyzed, followed by identifying stable regions through stability circles drawn in the Smith chart.
2. NF and available power gain circles are then drawn in the Smith chart. Subsequently, the overlapping Γ_s (Z_s) on both the desired NF and gain circle is chosen in the stable region, and preferably far from the stability circle. Array element 1 is then designed to have the input impedance as specified by Γ_s.

3. Γ_{OUT} is calculated with the gate terminal of transistor connected to array element 1. Array element 2 is then designed to conjugate-match the impedance $\Gamma_L = \Gamma_{OUT}^*$ ($Z_L = Z_{OUT}^*$), and transform to 50 Ω feed impedance. Γ_L should also be chosen in the stable region.
4. Finally, the array elements are optimized in the presence of a mutual coupling.

Design



(a) (b)

Figure C.3. Smith chart representing (a) NF and available power gain circles at 10 GHz and (b) input impedance of array elements 1 and 2 from 9.5 GHz to 11.5 GHz.

Stability factor K=1.028 and stability measure B=0.801 are realized for CE3512K2 (with via connecting the source terminal of transistor placed on the top layer to ground on the bottom layer), which confirms the unconditional stability of the transistor, and therefore, the stability circles need not be drawn. The NF and gain circles drawn for the transistor, at 10 GHz design frequency is shown in the Smith chart (Fig. C.3(a)). The optimum NF, NF_{opt} = 0.34 dB overlapping with the 13.6 dB gain circle, is chosen as the source impedance Z_s for low-noise receiver design.

Array element 1 is initially designed to have the desired source impedance Z_s = 30+j30 Ω, by tuning the resonant length of patch and adding a microstrip line inset. Subsequently, the length of array element 2 is tuned to conjugate-match the output impedance $Z_{OUT}^* = Z_L$= 32+j40 Ω on one end and to 50 Ω feed impedance on the other end, in addition to the signal reception through it. This 50 Ω reference is necessary for our measurement through the standard lab equipment. However, this condition or exigence can be relaxed for direct integration with the other frontend circuitry. The inter-element spacing is chosen equal to the CE3512K2 gate to drain dimension for direct integration of the transistor, thereby utilizing the spacing between array elements and removing

related interconnections, feed lines and their corresponding losses. The two elements are further optimized in the array environment with the amplified signal fed to the array element 2 through simultaneous simulation. Thus, we include the mutual coupling effects, thereby utilizing it in a positive manner, which has generally been considered a negative aspect. The final impedance behavior realized for the two array elements is shown in Fig. C.3(b). Additionally, AIA is also designed to measure the NF difference with respect to UNICA.

Noise Figure Formulation

The signal and noise received at the load from the two array elements are calculated independently and combined to compute the effective noise factor/figure of the system from (C1).

$$F = \frac{S_i/N_i}{S_0/N_0} \ , NF = 10\log(F) \tag{C1}$$

where S_i and N_i are the effective input signal and noise received by both the array elements respectively, and S_0 and N_0 are the effective output signal and noise at the output/load respectively.

AIA configuration

The signal and noise received through array element 1 propagates through the immediate microstrip line G_1 = -0.03 dB, followed by array element 2 which radiates a half of this signal G_2 = -3 dB, and the rest is fed to the amplifier circuit.

On the other hand, signal incident on array element 2 has two parallel paths, one towards array element 1 that is radiated, and the other path to the desired output. The amount of power coupled to each path depends on impedance seen towards each path. Considering the fundamental mode operation of a typical patch antenna, the input impedance at the edge of a resonant patch antenna is real and around 200 Ω. This impedance remains unchanged even before the microstrip line of length $\lambda_g/2$, typically used in broadside radiating series array configurations. From the knowledge of this impedance and the input impedance of amplifier (for example 50 Ω), the effective signal coupled towards the output is calculated as G_3 = -1.938 dB. The gain and NF of amplifier are G_A = 13.6 dB and NF_A = 0.377 dB, respectively.

The effective signal and noise present at the output from the signal received through the entire array is (C2) and (C3) respectively, and the derived noise factor for the system is (C4). From (C4) and

by substitution of all the parameters discussed, the effective NF of the system is computed as 2.0 dB. The equivalent ADS model designed gives a NF of 2.6 dB.

$$S_0 = G_1 G_2 G_A S_i + G_3 G_A S_i \tag{C2}$$

$$N_0 = G_A N_i + G_3 G_A N_i + 2N_{Added} \tag{C3}$$

$$F = \frac{(2*F_A - 1 + G_3)}{(G_1 G_2 + G_3)} \tag{C4}$$

UNICA configuration

The signal received through array element 1 is amplified directly by the transistor, and fed to array element 2. This array element radiates a part of signal, and remaining is fed to the output. Although the amount of signal radiated through this array element can be varied, it is assumed equal to the AIA configuration G_2 = -3 dB for a fair comparison.

The effective signal and noise at the output are described in (C5) and (C6), and the derived noise factor for the system is shown by (C7). NF of the system from (C7) is computed as 0.475 dB and 0.6 dB from the equivalent ADS model. A significant improvement is that the signal received through array element 2 is directly fed to the output because of the inherent unilateral property of the transistor, and also the amplifier integrated in the front greatly reduces the overall NF of the system.

$$S_0 = G_2 G_A S_i + S_i \tag{C5}$$

$$N_0 = (G_A N_i + N_{Added}) G_2 + (1 - G_2) N_i + N_i \tag{C6}$$

$$F = \frac{(2 + F_A G_A G_2 - G_2)}{(G_2 G_A + 1)} \tag{C7}$$

Experimental Validation

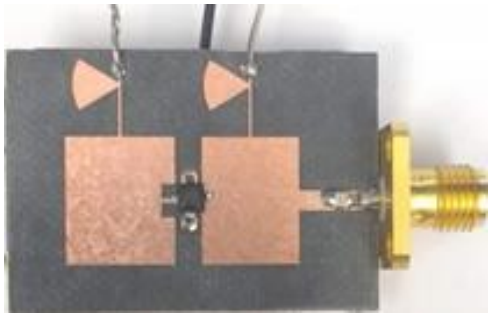


Figure C.4. Fabricated prototype.

The receiving antenna design in CST-MWS, demanded the excitation of the proposed prototype (AUT) (as shown in Fig. C.4) with the reference transmitting dipole antenna located in the far field, as shown in Fig. C.5(a). The resulting surface current distribution is demonstrated which confirms the amplified signal on array element 2, compared to the signal on array element 1. Subsequently, the E-field distribution illustrates the transformation of a dipole radiation from spherical pattern to a planar wave at the center of spacing, and the disturbance in pattern induced from AUT in its periphery, as shown in Fig. C.5(a).

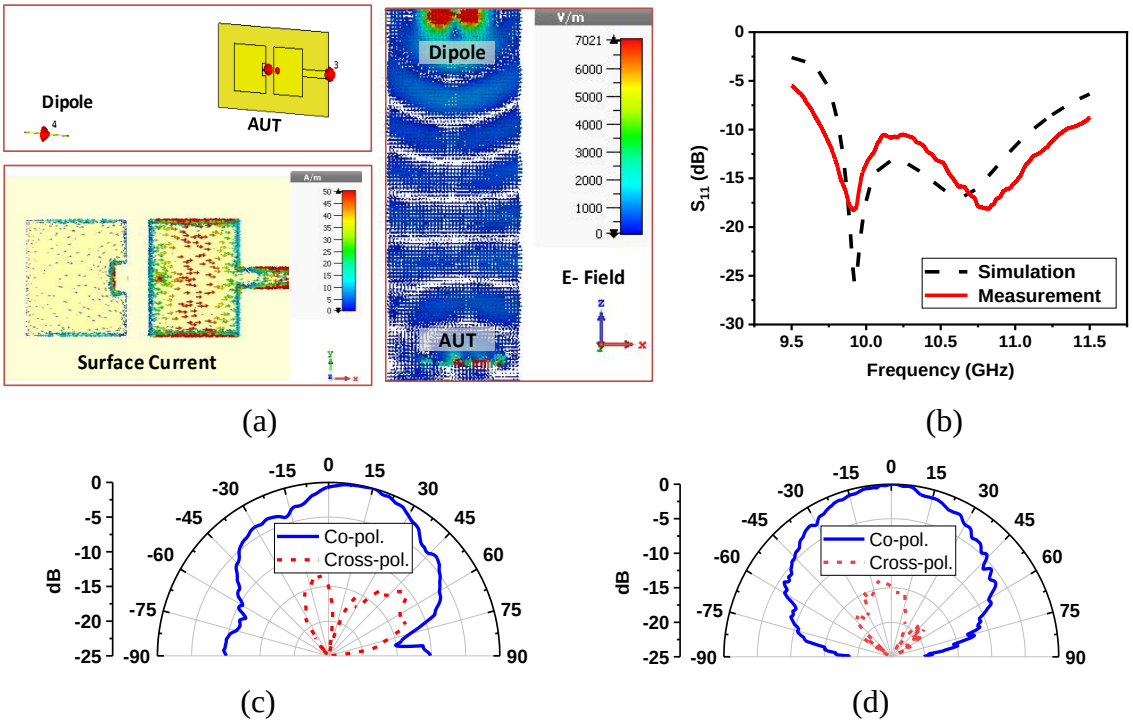


Figure C.5. (a) Simulated model with transmitting dipole antenna and receiving proposed UNICA (AUT), surface current distribution in AUT and E-field distribution (b) comparison of simulated and measured results of matching, and measured normalized radiation patterns in (c) E-plane and (d) H-plane.

The AUT is biased with gate bias V_G = - 0.2 V and drain bias current of I_D = 10 mA. The simulated and measured impedance matching performances across the frequency range are compared in Fig. C.5(b). This demonstrates a -10 dB fractional bandwidth of 15 %. The measured radiation performance in both E-plane and H plane is displayed in Fig. C.5(c) and C.5(d). The beam steered

performance to an angle of $+15^0$ from broadside in the E-plane is due to the phase shift induced by the amplifying transistor integrated between array elements. The simulated radiation efficiency is more than 90% for each array element.

The gain performance of the proposed prototype is compared with the passive series array counterpart to measure the amplification gain, following the procedure discussed in [198]. From the received signal and (C5), the estimated amplification gain is around 11.8 dB. The difference from the simulated value of 13.6 dB could be because of an error in fabrication and/or practical transistor difference from the simulated model, and a possible misalignment in our manual soldering of the transistor at the exact impedance point as in simulation.

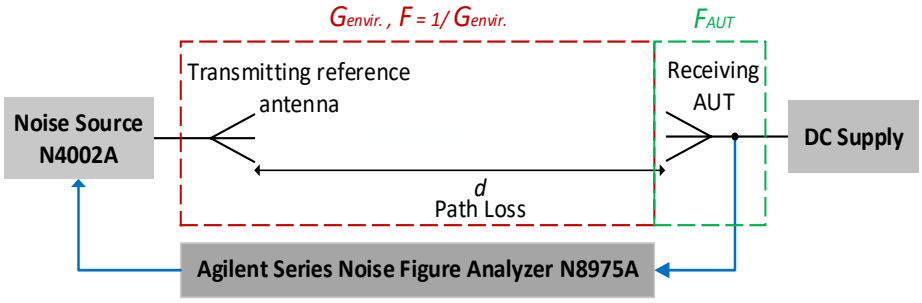


Figure C.6. Block diagram of noise figure measurement setup.

The block diagram of the NF measurement setup utilizing Agilent series NF analyzer N8975A and noise source N4002A is shown in Fig. C.6, where the transmitting reference antenna is kept fixed, and the receiving AUT is varied. After calibration, the noise factor is measured with AIA (as AUT) in the first step, and the measured result is F_{AUT1} (C8). Considering the effective gain through the path as $G_{envir.} < 1$ (gain of transmitting antenna + path loss), and noise factor of AIA as $F_{AIA,}$ the measured value of F_{AUT1} can be expressed as (C8). Similarly, the noise factor measured by replacing AUT with the proposed UNICA prototype is F_{AUT2}. $G_{envir.}$ (< 1) remains the same as the previous case, and the noise factor of prototype F_{UNICA} are related by (C9). Solving (C9)/(C8), the noise figure difference of the proposed UNICA model with respect to AIA is calculated in dB (C10). The difference thereby measured is 1 dB, which demonstrates a lower noise figure of the proposed UNICA configuration at the same amplification gain.

$$F_{AUT1} = \frac{F_{AIA}}{G_{envir.}} \tag{C8}$$

$$F_{AUT2} = \frac{F_{UNICA}}{G_{envir.}} \quad \text{(C9)}$$

$$\Delta NF = NF_{UNICA} - NF_{AIA} = NF_{AUT2} - NF_{AUT1} \quad \text{(C10)}$$

Conclusion

This paper presents a promising solution for low-noise and small-sized integrated receiver frontend for future RF and mmW modules. The proposed unified circuit-antenna architecture demonstrates a size reduction of 45 % compared to the AIA configuration and an enhanced matching bandwidth of 15 %. It also provides an amplification gain of around 11.8 dB, and the beam is steered to $+15^0$ from broadside in the E-plane. In addition, the noise figure of this proposed scheme is also reduced by 1 dB, compared to the AIA architecture. This work opens up a window in the development and design of future low-noise and compact receiver frontends.

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Patents:

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[1] **S. N. Nallandhigal** and K. Wu, "Unified and Integrated Circuit Antenna in Front End—A Proof of Concept," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 1, pp. 347-364, Jan. 2019.

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[5] **S. N. Nallandhigal** and K. Wu, " Deep Integration of Power Amplifier-on-Antenna in Standard CMOS”, (presented in APS 2020)*

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