Titre: Delay Mismatch Insensitive Dead Time Generator for High-Voltage Title: Switched-Mode Power Amplifiers
Auteurs: Ahmed Abuelnasr, Mostafa Amer, Mohamed Ali, Ahmad Hassan, Authors: Benoît Gosselin, Ahmed Ragab Anwar Ragab, \& Yvon Savaria

Date: 2023
Type: Article de revue / Article
AbueInasr, A., Amer, M., Ali, M., Hassan, A., Gosselin, B., Ragab, A. R. A., \&
Référence:
Savaria, Y. (2023). Delay Mismatch Insensitive Dead Time Generator for High-
Voltage Switched-Mode Power Amplifiers. IEEE Transactions on Circuits and
Systems I: Regular Papers, 70(4), 1555-1565.
https://doi.org/10.1109/tcsi.2022.3232074

## Document en libre accès dans PolyPublie <br> Open Access document in PolyPublie

URL de PolyPublie:
PolyPublie URL:
Version:
Version finale avant publication / Accepted version
Révisé par les pairs / Refereed
Conditions d'utilisation:
Terms of Use:
Tous droits réservés / All rights reserved

Titre de la revue: IEEE Transactions on Circuits and Systems I: Regular Papers (vol. 70, Journal Title: no. 4)
Maison d'édition:
Publisher:
IEEE
URL officiel:
Official URL:

Mention légale:
Legal notice:
https://doi.org/10.1109/tcsi.2022.3232074
© 2023 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.

# Delay Mismatch Insensitive Dead Time Generator for High-Voltage Switched-Mode Power Amplifiers 

Ahmed Abuelnasr ${ }^{\oplus}$, Mostafa Amer ${ }^{\oplus}$, Mohamed $\mathrm{Ali}^{\ominus}$, Member, IEEE , Ahmad Hassan ${ }^{\oplus}$, Member, IEEE , Benoit Gosselin ${ }^{\oplus}$, Member, IEEE, Ahmed Ragab ${ }^{\oplus}$, and Yvon Savaria ${ }^{\ominus}$, Fellow, IEEE


#### Abstract

The Design of efficient, safe, and reliable circuits is a prime objective in high-voltage (HV) electronic systems, such as switched-mode power amplifiers (PAs). One of the main causes of efficiency degradation and reliability problems, in these amplifiers, is the shoot-through current from the HV power supply to the ground. To eliminate such current, a dead time generator (DTG) is used to modify the signals propagating through the high-side and low-side gate drivers by adding a fixed dead time between them. However, any delay mismatch between these gate drivers can reduce the dead time to the point that it becomes negative. In this paper, an HV-DTG architecture is introduced. The architecture mitigates the effects of delay mismatch variations in gate drivers, which can result from parameters mismatch, fabrication process variations, and temperature variations. An HV switched-mode class-D power amplifier is used to illustrate the performance of the DTG. The amplifier is implemented in a low-cost $0.35 \mu m$ HV CMOS process. The total area of the PA is $0.5 \mathrm{~mm}^{2}$, where the DTG covers an area of $0.066 \mathrm{~mm}^{2}$. A measured system's efficiency of $\mathbf{9 5 . 1 4 \%}$ is achieved with the shortest dead time of 10.8 ns , which is 1.38 x smaller than the generated dead time in comparable state-of-the-art HV dead time generators.


Index Terms-Dead time generator, power amplifiers, switched-mode power amplifiers, class-D amplifier, highefficiency circuits, fabrication process \& temperature variations, shoot-through current.

## I. Introduction

EFFICIENCY and reliability in high-voltage (HV) electronic systems are major concerns, especially in critical applications such as those found in the automotive and aviation industries [1], [2], [3]. Recent developments in

[^0]

Fig. 1. Power amplifier block diagrams. (a) Without dead time generator. (b) With dead time generator.

HV semiconductor technologies led to the emergence of efficient and fully-integrated HV systems such as power amplifiers (PAs) and DC-DC converters [4], [5]. This helps in reducing cost, size, weight, and increase the density of power sensor interfaces and electric power distribution networks in listed applications, which improves their safety and reliability [1].

Owing to the high efficiency of the switched-mode amplifier topologies, such as class-D power amplifiers, they play a key role in many applications such as audio amplifiers, motor drivers, constant power supplies, and piezo-electric actuator drivers [1], [2], [6], [7], [8]. Even though the theoretical efficiency of switched-mode PAs can be close to $100 \%$, practically, there are several sources of power losses that degrade their efficiency. Conduction and switching losses, which are due to the finite ON-resistance and the large gate capacitance of power transistors, are the two main sources of power losses in switched-mode PAs. In addition, switched-mode PAs suffer from the shoot-through currents that happen when their high-side and low-side power transistors
are conducting at the same time. Such currents degrade their efficiency and pose safety concerns [9], [10], [11].

A typical configuration of a switched-mode PA is shown in Fig. 1(a). It consists of two complementary power MOSFETs, a high-side gate driver (HSGD) and a low-side gate driver (LSGD). This configuration has safety and reliability issues due to the possible overlapping time interval between the signals provided by the HSGD and LSGD; $V G p$ and $V G n$, respectively. During this overlapping time interval, the two power MOSFETs are ON and a shoot-through current flows from the HV power supply to the ground. This current leads to a very high power consumption and can potentially burn the circuit [6], [9], [10]. To prevent shoot-through currents, the input signal to the HSGD and LSGD can be split by a dead time generator (DTG) into two signals with a dead time between their respective active periods during which both transistors are OFF as shown in Fig. 1(b).

Even though the dead time is required to prevent the shootthrough currents, it creates other potential problems that need to be mitigated. During the dead time interval, when the two power MOSFETs of the PA are OFF, the passive filter imposes output current continuity through the internal body-diode of the low-side power MOSFET leading to unwanted power consumption and a reduction in the power efficiency [9], [12], [13]. The power consumed in the body-diode is:

$$
\begin{equation*}
P_{B D}=V_{S D} F_{S W}\left(I_{\text {out }, \text { peak }} t_{\text {dead time }}+I_{r r} t_{r r}\right) \tag{1}
\end{equation*}
$$

where $V_{S D}$ is the voltage across the diode, $F_{S W}$ is the switching frequency, $I_{\text {out,peak }}$ is the peak output current, $t_{\text {dead time }}$ is the dead time, $I_{r r}$ is the diode reverse recovery current, and $t_{r r}$ is the reverse recovery time [6]. Thus, this power consumption is directly proportional to the dead time interval. In addition, having the two power MOSFETs OFF for long time distorts the output waveform, which is highly undesirable in audio amplifiers such as class-D power amplifiers [14], [15]. Moreover, long dead times can lead to a momentary loss of control which can be problematic for amplifiers in electro-hydraulic actuators [6], [9], [13]. Consequently, the introduced dead time intervals need to be as short as possible to reduce the power consumption in the bodydiode, reduce the signal distortion, and improve the efficiency of the PA [9], [12], [13]. However, a very short fixed dead time is hard to maintain due to the possible delay mismatch between the HSGD and LSGD, and the dependence of this delay on the process, voltage, and temperature (PVT) variations as mentioned in [9].

In previous works reported in the literature, the dead time was dynamically adjusted to generate an optimal value that prevents shoot-through currents. Some designs used digital-based implementations to adjust the dead time. For example, the circuit presented in [16] adjusts the dead time using a senseFET, passive components, a flip-flop, a finite state machine, and a capacitor array. In [17], the dead time generator is integrated with a digital feedback controller to generate an optimal dead time value. Other implementations use passive components and comparators to generate the dead time [18], or use senseFETs to detect the body-diode conduction followed by comparators and digital circuits to adjust the dead time [13]. The works presented in [10]
and [19] propose an adjustable dead time generator using a structure composed of current sources and switched capacitors, while the work in [20] uses analog comparators and a digitally-controlled delay cell to adjust the dead time. Some of the reported designs use passive devices and analog components that are highly susceptible to noise. Moreover, some designs either need additional complex circuits for dead time calculations, or require calibration to offset any unwanted variations. Other designs are implemented in lowvoltage technology, and hence require scaling and adaptation to properly operate in the HV domain. The negative effects of PVT variations on the gate drivers' delay mismatch and the generated dead time were considered in previous works such as [9], [10], [18], and [19]. These effects were mitigated in such works, either by externally calibrating the dead time generator, or by accounting for them through corner simulations.

This paper validates, analyzes, and extends the work proposed in [21] on a delay mismatch insensitive DTG (DMIDTG) circuit. It notably provides a more detailed explanation of the architecture and of the design steps of the DMI-DTG, as well as of the design steps of a novel level-down shifter. The introduced DMI-DTG combines inverters, NOR gates, and HV level-down shifters to generate an always positive dead time that is proportional to the delays of the gate drivers and level-down shifters. Moreover, the insensitivity of the generated dead time to delay mismatch variations is validated through detailed analytical design equations and circuit simulations. Finally, the performance of the circuit is validated experimentally in an integrated HV power amplifier system, which is designed to drive a solenoid valve in an electro-hydraulic actuator [5], [22].
The DMI-DTG offers the following advantages:

- It generates the shortest possible dead time to ensure safe operation, while preventing cross-conduction of the halfbridge power MOSFETs, and improving the amplifier's efficiency.
- It adapts to any variations in the delays of the gate drivers that may arise due to PVT variations.
- It does not require passive components, complex digital or analog circuits, body-diode monitoring, power MOSFETs current-sensing, or other detection methods, unlike most of the previously reported methods.
- It can easily be integrated with HV switched-mode PAs as it adjusts the dead time using integrated HV level-down shifters, inverters and NOR gates.
In the remaining parts of the paper, the detailed architecture of the DMI-DTG circuit and analysis of the analytical design equations required for dead time calculations are presented in Section II. Section III presents the switched-mode PA with the integrated DMI-DTG circuit. Experimental results of the amplifier prototype, integrated with a $0.35 \mu \mathrm{~m}$ HV CMOS process, are shown in Section IV, and finally Section V concludes the paper.


## II. Dead Time Generators: Overview and Analysis

In this section, we first present the fixed DTG topology, then we introduce the modifications needed to construct the DMI-DTG.


Fig. 2. Dead time generators architecture and waveforms. (a) Fixed dead time generator (FDTG). (b) Delay mismatch insensitive dead time generator (DTG' \& level-down shifters).

## A. The Fixed Dead Time Generator

The operation and importance of the DMI-DTG can be highlighted by first explaining the fixed DTG solution. Fig. 2(a) shows the circuit diagram of a fixed DTG and the corresponding waveforms for inputs and outputs. The circuit consists of two NOR gates, inverters, and two delay elements. Its operation depends on the transition dependency of the NOR gates signals. If the input ( $I N$ ) of the upper NOR gate (NOR1) starts at 0 (low) and the input $(\overline{I N})$ of the lower NOR gate (NOR2) is 1 (high), the LSO1 (low side output) node starts at 0 and the $\mathrm{HSO} 1^{\prime}$ (high side output) node starts at 1 . HSO1 is the signal fed to the HSGD, $V G p$ is the output of HSGD and applied to the gate of the high-side power MOSFET, and $D 1$ is the delay of the HSGD. Similarly, $L S O 1$ is the signal applied to the LSGD, $V G n$ is generated from the LSGD and applied to the gate of the low-side power MOSFET, and $D 2$ is the delay of the LSGD. To simplify calculations, we assume symmetric falling-edge and rising-edge delays and negligible delays from the NOR gates and inverters. The transition of $I N$ from 0 to 1 and from 1 to 0 results in four transitions $T_{(1-4)}$ as follows:

- Transition $1\left(T_{1}\right)$ : A transition of IN from 0 to 1 results in two transitions, the transition of $\overline{I N}$ from 1 to 0 (which is instantaneous assuming the propagation delay of the inverter is negligible), and the transition of HSO1, from 1 to 0 which is delayed by the delay element $D H$.
- Transition $2\left(T_{2}\right)$ : A transition of $H S O 1^{\prime}$ from 1 to 0 makes both inputs of NOR2 (HSO1' \& $\overline{I N})$. This results in the transition of $L S O 1$ from 0 to 1 which is delayed by the delay element $D L$.
- Transition $3\left(T_{3}\right)$ : A transition of $I N$ from 1 to 0 results in two transitions, the transition of $(\overline{I N})$ from 0 to 1 (which is instantaneous assuming the propagation delay of the inverter is negligible), and the transition of $L S O 1$ from 1 to 0 with a delay $D L$.
- Transition $4\left(T_{4}\right)$ : A transition of LSO 1 from 1 to 0 makes both inputs of NOR1 (LSO1 \& IN) 0. This results in the transition of $H S O 1^{\prime}$ from 0 to 1 delayed by $D H$.
The dependency between the signals of the NOR gates and the added delay elements ( $D H \& D L$ ) results in this transition of
signals $T_{(1-4)}$ which leads to the formation of a fixed dead time between HSO1 and LSO1. In this case, the initial rising-edge dead time $\left(D T_{\text {rise }}\right)$ is equal to $D L$ and the initial falling-edge dead time $\left(D T_{\text {fall }}\right)$ is equal to $D H$. The signals generated from the dead time circuit are then applied to the power MOSFETs through the implemented gate drivers (HSGD and LSGD). The delay of the HSGD ( $D 1$ ) affects $V G p$, while the delay of the LSGD ( $D 2$ ) affects $V G n$. From the waveforms shown in Fig. 2(a), we can calculate $D T_{\text {rise }}$ and $D T_{\text {fall }}$ after propagating through the HSGD and LSGD.

$$
\begin{align*}
D T_{\text {fall }} & =D 1+D H+D L+P-(D 2+D L+P) \\
& =D H+(D 1-D 2)=D H+\Delta D T \tag{2}
\end{align*}
$$

where $\Delta D T$ is the delay mismatch between HSGD and LSGD, and $P$ is the falling-edge time of the $I N$ waveform.

$$
\begin{align*}
D T_{\text {rise }} & =D 2+D H+D L-(D 1+D H) \\
& =D L-(D 1-D 2)=D L-\Delta D T \tag{3}
\end{align*}
$$

From (2) \& (3), we can see that $D T_{\text {rise }}$ is reduced by the delay mismatch value $\Delta D T$. Accordingly, if $D L=\Delta D T$, $D T_{\text {rise }}$ will diminish while $D T_{\text {fall }}$ will increase by a value equal to $\Delta D T$. This will result in an overlap between $V G p$ and $V G n$ signals at the rising edge. Consequently, a shootthrough current will propagate from the HV power supply to the ground. Therefore, the fixed DTG configuration makes the system susceptible to the shoot-through currents, especially when there are variations in the delay mismatch $\Delta D T$.

## B. The Delay Mismatch Insensitive Dead Time Generator

To handle the issue of the delay mismatch between the HSGD and LSGD, a DMI-DTG is introduced as shown in Fig. 2(b). It consists of two NOR gates, inverters and two level-down shifters added after the HSGD and LSGD to scale down the signals provided to the NOR gates. Using this configuration, the resulting dead time will be intrinsically adjusted in accordance with the delays of the HSGD and LSGD without diminishing the rising-edge or falling-edge dead times as in the case of the fixed DTG. Following the


Fig. 3. Rising-edge dead time and falling-edge dead time variation with the delay variations of high-side and low-side gate drivers and level-down shifters. (a) High-side level-down shifter delay variation. (b) High-side gate driver delay variation. (c) Low-side level-down shifter delay variation. (d) Low-side gate driver delay variation.
waveforms depicted in Fig. 2(b), the rising-edge and fallingedge dead times are calculated as follows:

$$
\begin{align*}
D T_{\text {rise }} & =D 2+D 1+D H D S-D 1=D 2+D H D S  \tag{4}\\
D T_{\text {fall }} & =D 1+D 2+D L D S+P-(D 2+P) \\
& =D 1+D L D S \tag{5}
\end{align*}
$$

where $D 1$ and $D 2$ are the delays of HSGD and LSGD, respectively. $D H D S$ and $D L D S$ are the delays of highside level-down shifter and low-side level-down shifter, respectively. Now, $D T_{\text {rise }}$ depends only on the summation of $D H D S$ and $D 2$. Similarly, $D T_{\text {fall }}$ depends only on the summation of $D L D S$ and $D 1$. Therefore, our dead time generator is insensitive to the delay mismatch between the HSGD and LSGD.

## C. Verification of the Analytical Model

To verify the analytical design equations, the DMI-DTG architecture, shown in Fig. 2(b), was implemented and simulated using Cadence ${ }^{\circledR}$ tools [23]. In our simulations, we swept the delay of the gate drivers and that of the level-down shifters separately from 1 to 20 ns , while keeping all other delays constant, and we observed the impact on both the rising and the falling edges of the resulting dead time signals. The default delays of the various building blocks of the DMI-DTG and the gate drivers are set as follows: $D 1=8.8 \mathrm{~ns}, D 2=5.2 \mathrm{~ns}, D H D S=4.8 \mathrm{~ns}$ and $D L D S$ $=12.2 \mathrm{~ns}$. According to the formulated analytical equations $D T_{\text {rise }}=D 2+D H D S=5.2+4.8=10 \mathrm{~ns}, D T_{\text {fall }}=$ $D 1+D L D S=8.8+12.2=21 \mathrm{~ns}$. In Fig. 3(a), the delay of the HSLDS ( $D H D S$ ) is varied and, as expected from the analytical design equations, only $D T_{\text {rise }}$ varies with the variation of $D H D S$. Similarly, when varying $D 2$ in Fig. 3(d),


Fig. 4. Simulation of the variations in the gate drivers delay at different process corners and different temperatures.


Fig. 5. Simulation of the variations in the delay mismatch, rising-edge dead time and falling-edge dead times at different process corners and different temperatures if a fixed dead time generator is used.
only $D T_{\text {rise }}$ varies, while $D T_{\text {fall }}$ remains unaffected. When varying $D 1$ in Fig. 3(b) and $D L D S$ in Fig. 3(c), only $D T_{\text {fall }}$ varies, while $D T_{\text {rise }}$ remains constant in agreement with the analytical design equations.

To illustrate the significance of the DMI-DTG over the fixed DTG, variations in the delay of the HSGD and LSGD, with the process and temperature variations (through conducting corner simulations) are shown in Fig. 4. The circuit was simulated in four process corners (SS, SF, FS, FF) and under 4 different temperatures $(-40,27,100,150)^{\circ} \mathrm{C}$. Where S stands for slow, F stands for fast, the first letter is for NMOS, and the second letter is for PMOS. For example, SF27 is for slow NMOS, fast PMOS corner at $27^{\circ} \mathrm{C}$. Fig. 4 has 16 different states representing the combination between the four different corners and the four different temperatures, in addition to the nominal state which represents the typical-NMOS-typicalPMOS at room temperature. The figure illustrates the effect of the process corners and temperature variations on the delays of the gate drivers, this translates into a variation in the delay mismatch between the HSGD and LSGD. Fig. 5 illustrates the variations in the delay mismatch between the HSGD and LSGD in the 16 different states. It also shows the variations in the rising and falling edge dead times if a fixed DTG, generating a dead time of 3 ns is used. The largest variation value can be seen at the slow NMOS slow PMOS corner with a temperature of $150^{\circ} \mathrm{C}$. At this state, a 4.29 ns delay mismatch is obtained, where the nominal value (at typical-typical process corner and under room temperature) for the delay mismatch

## DMI-DTG Dead Time Variations



Corner

Fig. 6. Simulation of the variations in the rising-edge and falling-edge dead times at different process corners and different temperatures for the DMIDTG.
is equal to 1.96 ns . Accordingly, the process and temperature variations result in a $2.2 \times$ increase in the delay mismatch. As shown in Fig. 5, the rising edge dead time diminishes and becomes negative with the variation of the delay mismatch. This is due to the dependence of the rising edge dead time on the delay mismatch as illustrated in the previous section. Thus, exploiting a fixed DTG does not seem to be a good solution as the required dead time depends on the process and temperature variations, leading to possible shoot-through current problems.

Similarly, variations in rising-edge and falling-edge dead times caused by the process and temperature variations when using the DMI-DTG are shown in Fig. 6. It should be noted that in both architectures, the DMI-DTG and the fixed DTG, process variations will result in varying the delays of the gate drivers leading to a variation in the delay mismatch. This delay mismatch negatively affects the dead time generated by the fixed DTG, however, in the DMI-DTG, this delay mismatch does not affect the generated dead time, as shown in Fig. 6, positive rising-edge and falling-edge dead times are always obtained.

## III. Switched-Mode Power Amplifier With Integrated Dead Time Generator: DESIGN \& IMPLEMENTATION

The DMI-DTG is integrated and validated in the typical switched-mode PA topology shown in Fig. 7. The amplifier is integrated with a $0.35 \mu \mathrm{~m}$ HV CMOS process. It consists of five main blocks: a half-bridge, an HSGD, an LSGD, a DTG, and an off-chip passive filter. Each gate driver consists of a level-up shifter and a buffer. The DMI-DTG architecture consists of three components; a DTG' and two level-down shifters. The DTG' consists of inverters and two NOR gates, while the detailed design of the level-down shifters is highlighted in the following subsections. The off-chip filter consists of a 1 mH inductor and a 100 nF capacitor. The amplifier is supplied by two HV power supplies ( 24 V and 12 V ) and a low-voltage power supply ( 3.3 V ). The input to the amplifier is a 500 kHz pulse-width modulated (PWM) signal (0-3.3)V, while the load is (a 100 mH inductor in series with a $342.5 \Omega$ resistor), representing a solenoid valve in an electro-hydraulic actuator [22]. In the next subsections, the rest of the amplifier components will be described in detail.

## A. Half-Bridge

The half-bridge (HB) consists of two large power MOSFETs: a PMOS and an NMOS. To increase the efficiency of the PA, power losses (in the half-bridge and other circuits in the amplifier) must be reduced. There are two main sources of power loss in the half-bridge; the conduction loss and the gate-switching loss [7]. The conduction loss $\left(P_{\text {cond }}\right)$ occurs due to the flow of the output current through the finite ON-resistance of the power MOSFETs, where $P_{\text {cond }}=$ $I_{\text {out }}^{2} R_{\text {ON }}$. While gate-switching loss $\left(P_{g s w}\right)$ occurs due to the charging and discharging of the gate capacitance of the power MOSFETs when turning them ON and OFF, where $P_{g s w}=Q_{g} V F_{s w}, Q_{g}=\int_{V 1}^{V 2} C_{g} d V$ and $C_{g}$ is proportional to the gate width $(W)$ times the gate length $(L)$ of the MOSFETs. Thus, minimizing $R_{O N}$ and $C_{g}$ reduces conduction losses and switching losses, respectively.

$$
\begin{equation*}
R_{O N}=L /\left(W \mu_{n} C_{o x}\left(V_{G S}-V_{t h}-V_{D S} / 2\right)\right) \tag{6}
\end{equation*}
$$

According to (6), $R_{O N}$ is decreased by increasing the transistor gate width (W). However, increasing W increases $C_{g}$, which increases the gate-switching loss, thus, a suitable balance must be found when choosing W to reduce both conduction and gate-switching losses. Reducing L reduces both the switching and conduction losses, therefore a minimum length is selected for the transistors. For an optimum balance, $R_{O N}$ and $C_{g}$ of the implemented power transistors (at minimum gate length, L) are simulated in Fig. 8 as a function of the gate width. As W increases, $R_{O N}$ decreases rapidly at the beginning, then it decreases asymptotically, and eventually, very small changes are obtained by further increasing W. On the other hand, $C_{g}$ increases linearly with W. A Width of 5 mm is selected for the NMOS, which corresponds to an ON -resistance of $4.6 \Omega$, while a width of 8 mm is selected for the PMOS which corresponds to an ON-resistance of $8 \Omega$. Any further increase in W , for either the NMOS or the PMOS, will result in modest reductions in $R_{O N}$ and large increases in $C_{g}$ which will complicate the design of the buffer chain. At $\mathrm{W}=8 \mathrm{~mm}$, the $C_{g}$ of the PMOS is 14.8 pF , and at $\mathrm{W}=5 \mathrm{~mm}$, the $C_{g}$ of the NMOS is 10 pF (as shown in Fig. 8).

## B. Buffer Chains

Using the outputs from the level-up shifters directly to drive the large gate capacitance of the power MOSFETs will result in a large delay. Driving such a capacitance with a minimum size buffer yields propagation delays of 32 ns and 38 ns when driving the NMOS and the PMOS, respectively. To minimize this propagation delay, a tapered topology for designing the buffer is considered. In this topology, a chain of inverter stages is used with the size of each stage being k times larger than the preceding stage. The total delay of a tapered buffer driving a capacitive load can be calculated using (7) [24]:

$$
\begin{equation*}
T_{\text {tapered }}=T_{0} \frac{k}{\ln (k)} \ln (y) \tag{7}
\end{equation*}
$$

where $y=C_{\text {load }} / C_{\text {in }}, k=y^{1 / N}$ is the tapering factor, $N$ is the number of inverter stages, $C_{\text {load }}$ is the buffer load capacitance which is the gate capacitance of the NMOS or


Fig. 7. The switched-mode class-D power amplifier block diagram, with the passive off-chip components and the different types of used high-voltage transistors (shown on the right).
ON Resistance \& Gate Capacitance


(a)
(a)

(b)

Fig. 8. ON-resistance and gate capacitance of NMOS and PMOS devices versus gate width $\left(R_{O N N}\right.$ and $C_{g N}$ for NMOS), $\left(R_{O N P}\right.$ and $C_{g P}$ for PMOS).

PMOS power transistors, and $C_{i n}$ is the gate capacitance of a minimum size inverter. The minimum size inverter was implemented with a PMOS transistor with minimum length and $15 \mu \mathrm{~m}$ width, and an NMOS transistor with minimum length and $10 \mu \mathrm{~m}$ width. Using (7), and following the steps given in [24], the number of inverters in the buffer chain $(N)$ for each power MOSFET and the tapering factor $k$ were found to be 4 and 3 , respectively. The designed tapered buffer chains are shown in Fig. 7, where HSB is the high-side buffer chain and LSB is the low-side buffer chain. The HSB is designed using isolated NMOS transistors, where the body and source terminals of the device are not grounded, but connected to a floating 12 V supply. Accordingly, the transistors need to be isolated to support this floating voltage without damaging the substrate. In comparison to the minimum size buffer, using the tapered buffer reduces the propagation delay for driving the power NMOS by 6.4 times, while the propagation delay for driving the power PMOS is reduced by 6.9 times.

Fig. 9. Different configurations to illustrate the operation of level shifters: (a) and (b) are level-up and level-down shifters with resistors, while (c) and (d) are level-up and level-down shifters with diode-connected transistors.

## C. Level Shifters

To produce suitable gate drive signals for the NMOS and PMOS power transistors in the [0-12]V and [12-24]V domains, the input low-voltage PWM signal must be shifted from [0-3.3]V to the required voltage levels. This can be realized using level-up shifters. The different diagrams in Fig. 9, describe the basic operation of the level-up and level-down shifters.
The simplest way to shift a voltage signal from one level to another is to use a pulsed current source and resistors ladder. An example of this configuration is shown in Fig. 9(a), where the input signal can be shifted from [ $0-V D D 1$ ] to [ $V D D 2 / n-V D D 2$ ], where n is the number of equal-value resistors. It is always recommended to use ratioed resistors as this will minimize the effect of layout mismatch between the resistors after fabrication. Using the principle of duality, we shift the signal from a high-voltage domain to a low-voltage domain by using a PMOS, instead of an NMOS, as the current source, and connecting the resistors to the ground as shown in Fig. 9(b). Resistors are passive components that consume high power and occupy a large silicon area. Instead, diode-connected transistors are used to limit the voltage to the required level as shown


Fig. 10. Circuit diagrams of the implemented level-up shifters. (a) High-side level-up shifter. (b) Low-side level-up shifter.
in Fig. 9(c) and 9(d). The sizes of the diode-connected transistors are adjusted to clip the voltage and achieve the required output, taking into account the proper voltage ratings. The proposed circuit designs for the level-up and level-down shifters to be used in the PA system are explained in more detail below.

1) Level-Up Shifters Design: Configurations of both the high-side and low-side level-up shifters are shown in Fig. 10. A conventional Cascode Voltage Switch Logic (CVSL) configuration with identical left and right branches is utilized for the level-up shifters. The CVSL configuration ensures that once an initial state is reached on one side, an opposite state is reached quickly on the other side, while the output is kept in a quasi-static state until a change is done to the input. A slight modification to the conventional CVSL is implemented by adding extra diode-connected transistors to limit the output voltage swing between 12 V and 24 V .

The diode-connected transistors are low-voltage isolated PMOS transistors that can tolerate $V_{G S}$ of 5 V and $V_{D S}$ of 5 V with bulks isolated from the substrate. This limits the voltage drop over each transistor to 5 V , which is in the safe operating region. In our case, 12 V at the output can be obtained by using 6 transistors with a 4 V drop across each transistor. The NMOS pulsed current source transistors, one on each side, can tolerate 50 V between the drain and the source and 5 V between the gate and the source. The low-side level-up shifter shown in Fig. 10(b) is similar to the high-side level-up shifter depicted in Fig. 10(a), except that the output swing is between 0 and 12 V . Accordingly, no extra limiting transistors are required, and we can use a conventional CVSL configuration. The PMOS transistors are high-voltage transistors that can tolerate 20 V between the drain and the source and a maximum of 20 V on the gate. The NMOS transistors have thin gate-oxide that can tolerate 20 V between the drain and the source and 5 V between the gate and the source.
2) Level-Down Shifters Design: Fig. 11 presents the high-side and low-side level-down shifters. The operation of each level shifter is exactly the same as the other except that the high-side level-down shifter level shifts the signal from [12-24]V to [0-3.3]V, while the low-side level-down shifter


Fig. 11. Circuit diagrams of the implemented level-down shifters. (a) Highside level-down shifter. (b) Low-side level-down shifter.
shifts the signal from [0-12]V to [0-3.3]V. Using the principle of duality and applying it to the CVSL configuration, we can easily design the level-down shifter.

The input of the high-side level-down shifter is between [12-24]V which requires the usage of an isolated NMOS in the upper inverter, in addition, 8 isolated diode-connected NMOS transistors are utilized to scale down the 24 V signal to 3 V by introducing voltage drops of 3 V each. At the output, lowvoltage inverters are used to obtain a voltage swing between [0-3.3]V. The operation of the low-side level-down shifter is similar to the operation of the high-side level-down shifter except that only 4 isolated diode-connected transistors are utilized. Isolated transistors are adopted so that the body is isolated from the substrate, accordingly other voltages can be connected to the body other than the lowest voltage which ensures that the chip substrate is always connected to the lowest voltage.

## IV. Experimental Results and Discussion

The amplifier prototype including the DMI-DTG circuit is fabricated with a $0.35 \mu \mathrm{~m}$ HV CMOS process. The chip micrograph of the integrated amplifier as well as the layout views of the various integrated blocks are shown in Fig. 12. The amplifier occupies an area of $0.5 \mathrm{~mm}^{2}$. The chip is wire-bonded inside a pin grid array (PGA) ceramic package. The latter is soldered on a custom printed-circuit board (PCB) for characterization. Off-chip 1 mH inductor and 100 nF capacitor were used to build the low-pass filter. In addition, a 100 mH inductor was used as an inductive load in series with a purely resistive load. The amplifier test bench is depicted in Fig. 12. In this setup, a 4-channel oscilloscope was used to display the system output signals, two power supplies were used to supply the required voltage levels and one function generator was used to provide the required input PWM signal. A breakdown of the percentage of the area occupied by different blocks in the PA is shown in Fig. 13. The total percentage of the area covered by the dead time generator (DTG', HSLDS \& LSLDS) with respect to the area of the PA is $13.3 \%\left(0.066 \mathrm{~mm}^{2}\right)$. Measured input ( $V G p, V G n$ ) and output ( $H S L D S, L S L D S$ ) signals of the implemented high-side and low-side level-down shifters are depicted in Fig. 14. The rising-edge and falling-edge delays were measured and the average was taken to be the delay value. The averaged measured delay of the high-side leveldown shifter $D H D S=(5.6+4) / 2=4.8 \mathrm{~ns}$, while the averaged


Fig. 12. Experimental setup (right), fabricated chip micrograph and detailed circuit blocks of the system layout (left). a) DTG'. b) Low-side level-up shifter. c) Low-side buffer. d) Low-side level-down shifter. e) High-side level-up shifter. f) High-side buffer. g) High-side level-down shifter. h) Half-bridge.

Power Amplifier Area Breakdown


Fig. 13. Area percentage breakdown of the PA's circuit components.


Fig. 14. Rising-edge and falling-edge delays of the high-side and low-side level-down shifters.
measured delay of the low-side level-down shifter $D L D S=$ $(14.8+9.6) / 2=12.2$ ns as shown in Fig. 14.

The measured input and output waveforms of the HSGD and LSGD are shown in Fig. 15. The resulting delay from the HSGD $(D 1)=(9.2+8.4) / 2=8.8 \mathrm{~ns}$, and the delay of the $\operatorname{LSGD}(D 2)=(5.6+4.8) / 2=5.2 \mathrm{~ns}$. Using the analytical design equations derived in Section II, the actual dead time can be calculated using the measured delays for the various components as follows:

$$
\begin{gathered}
D T_{\text {rise }}=D 2+D H D S=5.2+4.8=10 \mathrm{~ns} \\
D T_{\text {fall }}=D 1+D L D S=8.8+12.2=21 \mathrm{~ns}
\end{gathered}
$$



Fig. 15. Measured rising-edge and falling-edge delays of the high-side and low-side gate drivers.


Fig. 16. Measured rising and falling-edge dead times.

The obtained delays are very close to the measured delays at the gates of the power MOSFETs shown in Fig. 16. Where $D T_{\text {rise }}=10.8 \mathrm{~ns}$ and $D T_{\text {fall }}=20 \mathrm{~ns}$. The difference between the calculated and measured delays does not exceed 1 ns , resulting in an error of less than $7.4 \%$ in $D T_{\text {rise }}$ and $5 \%$ in $D T_{\text {fall }}$. This small difference can be attributed to the fact that we are using average values for the delays, and that we ignored the delays of the logic gates (inverters and NOR gates) when we deduced the analytical design equations.

The efficiency of the implemented PA with the DMIDTG, while driving a $100 \mathrm{mH} \& 342.5 \Omega$ load at different frequencies, is shown in Fig. 17. The efficiency ( $\eta=\frac{P_{\text {load }}}{P_{\text {total }}}$ )

TABLE I
Power Amplifiers Performance Summary and Comparison

| Reference | JSSC 2012 [25] | ISSCC 2014 [26] | JSSC 2015 [27] | JSSC 2015 [7] | TPEL 2016 [9] | TCAS-I 2021 [10] | This Work |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Topology | Class-D | Class-D | Buck | Class-D | Buck | Buck | Class-D |
| Process | CMOS $0.35 \mu \mathrm{~m}$ | SOI $0.14 \mu \mathrm{~m}$ | CMOS $0.5 \mu \mathrm{~m}$ | SOI $0.14 \mu \mathrm{~m}$ | CMOS $0.35 \mu \mathrm{~m}$ | CMOS $0.35 \mu \mathrm{~m}$ | CMOS $0.35 \mu \mathrm{~m}$ |
| Power Supply (V) | 18 | 80 | 40 | 80 | 45 | 45 | 24 |
| Frequency (MHz) | 0.384 | adaptive | 0.5 | adaptive | 0.1 | 1 | 0.5 |
| Load | $8 \Omega$ | $22.5 \mu \mathrm{~F}+1.6 \Omega$ | NA | $12 \Omega$ | NA | $100 \Omega$ | $100 \mathrm{mH}+342.5 \Omega$ |
| DTG area ( $\mathrm{mm}^{2}$ ) | NA | NA | NA | NA | 0.22 | 0.0126 | 0.066 |
| Efficiency @ 0.1*Poutmax | >70\% | 80\% | >65\% | 84\% | $>87 \%$ | NA | 65\% |
| Peak Efficiency ( $\eta$ ) | 88\% | 93\% | 94.9\% | 91\% | 95\% | 82\% | 95.14\% |
| Shortest Dead Time (ns) | 15 | 100 | 25 | 100 | 15 | 35 | 10.8 |
| $\mathrm{FOM}^{*}(\mathrm{~ns} / \%)$ | 0.17 | 1.07 | 0.26 | 1.1 | 0.157 | 0.42 | 0.11 |

${ }^{*} F O M=\frac{\text { DeadTime }(n s)}{\text { Efficiency }(\eta \%)}$, NA: Not Available, Poutmax : Maximum Output Power.


Fig. 17. Measured efficiency vs power of the PA at different frequencies.
was measured by varying the duty-cycle of the input signal from 0.05 to 0.95 with a step of 0.1 and measuring the total supplied power and the power delivered to the load. $P_{\text {total }}=\sum_{i=1}^{n} I_{\text {Supply }_{i}} * V_{\text {Supply }_{i}}$, where $I_{\text {Supply }_{i}}$ and $V_{\text {Supply }}^{i}$ are the current and the supply voltage of the $i^{\text {th }}$ power supply, respectively, and $n$ is the number of power supplies used. A peak efficiency of $95.14 \%$ is achieved at 500 kHz frequency, as shown from the efficiency curves in Fig. 17. As an example, the post-layout simulation of the efficiency at 500 kHz frequency is also shown in the same figure, the simulation varies slightly from the measurements due to the difference in the parasitic capacitance which affects the switching loss especially in low-power regions [6]. Additionally, the post-layout simulation shows that the DMI-DTG consumes 16.5 mW . To examine the impact of changing the switching frequency on the amplifier's efficiency, the efficiency curves, for the same duty-cycle range, at 1 MHz and 2 MHz are measured and added to the same figure. Also, the amplifier efficiency at $50 \%$ duty-cycle is measured at 11 different frequencies up to 10 MHz as shown in Fig. 18.

The degradation in the amplifier's power efficiency is mainly due to the gate capacitance switching loss and the ON-resistance conduction loss. According to [6], the efficiency curve can be divided into three main regions depending on the main source of power dissipation. The first region is the low-power region in which the switching loss is dominant.


Fig. 18. Measured efficiency vs frequency of the PA at $50 \%$ duty cycle.

The second region is the high-power region in which the conduction loss is dominant, and the third region is the middle power region in which both sources of loss are comparable. This can be seen in Fig. 17, when the frequency increases, the switching loss is dominant in the low-power region and there is a large reduction in efficiency compared to the high-power region in which the difference is less visible. The efficiency of the PA at $50 \%$ duty cycle was measured at frequencies ranging from 500 kHz to 10 MHz as shown in Fig. 18. As we can see from the curve, the efficiency is decreasing as the frequency increases. This is because the switching power loss increases as the switching frequency increases, leading to a reduction in efficiency.

Table I presents the measured performance summary of the fabricated PA and comparable previous designs. The PA using the DMI-DTG can achieve high efficiency of $95.14 \%$ with a very short dead time of 10.8 ns , which is comparable to previous state-of-the-art PAs. In addition, a figure of merit (FOM) is used to allow a fair comparison with previous state-of-the-art. The adopted FOM shows the ability of the DTG to achieve the shortest possible dead time with high efficiency. A smaller FOM means that shorter dead time and higher efficiency are achieved. The shortest dead time achieved in previous comparable designs was 15 ns , and the highest achieved efficiency was $95 \%$, while our design achieves a smaller dead time ( 10.8 ns ) with $95.14 \%$ efficiency. In addition, compared to previous DTGs, our design
has a small area with the smallest FOM. Moreover, our DMI-DTG can adapt to process variations, while providing the shortest dead time possible, thus, improving the efficiency and reliability of the whole system.

## V. Conclusion

The design of high-voltage (HV) switched-mode power amplifiers (PAs) is centered around achieving high-efficiency, safe and reliable end solutions. Hence, very short dead times are required, while ensuring safe operation, in the amplifiers to improve their efficiency. This paper analyses, explores how to design and validates experimentally an HV delay mismatch insensitive dead time generator (DMI-DTG) that can adapt to process and temperature variations. This DTG is integrated within a switched-mode PA system and measured power efficiency of $95.14 \%$ is achieved at 500 kHz frequency with a generated dead time as small as 10.8 ns . The DMIDTG circuit consists of inverters, NOR gates, and HV leveldown shifters. The generator is implemented in a $0.35 \mu \mathrm{~m}$ HV CMOS process covering an area of $0.066 \mathrm{~mm}^{2}$ which is less than $13.3 \%$ of the total area of the PA $\left(0.5 \mathrm{~mm}^{2}\right)$. As a promising future work, the generated dead time can be further reduced by optimizing the gate drivers and the level-down shifters to make them faster, thus, reducing the body-diode conduction loss and improving the whole efficiency of the PA.

## Acknowledgment

The authors would like to thank CMC Microsystems for providing access to CAD tools and fabrication technologies.

## REFERENCES

[1] N. Swaminathan and Y. Cao, "An overview of high-conversion highvoltage DC-DC converters for electrified aviation power distribution system," IEEE Trans. Transport. Electrific., vol. 6, no. 4, pp. 1740-1754, Dec. 2020.
[2] N. Swaminathan and L. Narasamma, "Hybrid control scheme for mitigating the inherent DC-current in the transformer in buck-boost full-bridge converter for an all-electric motor drive system," IET Power Electron., vol. 11, no. 8, pp. 1452-1462, Jul. 2018.
[3] B. Sarlioglu and C. T. Morris, "More electric aircraft: Review, challenges, and opportunities for commercial transport aircraft," IEEE Trans. Transport. Electrific., vol. 1, no. 1, pp. 54-64, Jun. 2015.
[4] S. Bernet, "Recent developments of high power converters for industry and traction applications," IEEE Trans. Power Electron., vol. 15, no. 6, pp. 1102-1117, Nov. 2000.
[5] M. Ali et al., "A versatile SoC/SiP sensor interface for industrial applications: Implementation challenges," IEEE Access, vol. 10, pp. 24540-24555, 2022.
[6] A. I. Colli-Menchi and E. Sánchez-Sinencio, "A high-efficiency selfoscillating class-D amplifier for piezoelectric speakers," IEEE Trans. Power Electron., vol. 30, no. 9, pp. 5125-5135, Sep. 2015.
[7] H. Ma, R. van der Zee, and B. Nauta, "A high-voltage class-D power amplifier with switching frequency regulation for improved highefficiency output power range," IEEE J. Solid-State Circuits, vol. 50, no. 6 , pp. 1451-1462, Jun. 2015.
[8] M. Amer et al., "Fully integrated dual-channel gate driver and area efficient PID compensator for surge tolerant power sensor interface," in Proc. 18th IEEE Int. New Circuits Syst. Conf. (NEWCAS), Jun. 2020, pp. 166-169.
[9] R. Grezaud, F. Ayel, N. Rouger, and J. Crebier, "A gate driver with integrated deadtime controller," IEEE Trans. Power Electron., vol. 31, no. 12, pp. 8409-8421, Dec. 2016.
[10] M. Karimi, M. Ali, A. Hassan, M. Sawan, and B. Gosselin, "An active dead-time control circuit with timing elements for a $45-\mathrm{V}$ input $1-\mathrm{MHz}$ half-bridge converter," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 69, no. 1, pp. 30-41, Jan. 2022.
[11] S. Lee, S. Jung, C. Park, C.-T. Rim, and G.-H. Cho, "Accurate dead-time control for synchronous buck converter with fast error sensing circuits," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 60, no. 11, pp. 3080-3089, Nov. 2013.
[12] X. Jing and P. K. T. Mok, "Power loss and switching noise reduction techniques for single-inductor multiple-output regulator," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 60, no. 10, pp. 2788-2798, Oct. 2013.
[13] A. Niwa et al., "A dead-time-controlled gate driver using current-sense FET integrated in SiC MOSFET," IEEE Trans. Power Electron., vol. 33, no. 4, pp. 3258-3267, Apr. 2018.
[14] M. Mauerer, A. Tuysuz, and J. W. Kolar, "Distortion analysis of low-THD/high-bandwidth GaN/SiC class-D amplifier power stages," in Proc. IEEE Energy Convers. Congr. Expo. (ECCE), Sep. 2015, pp. 2563-2571.
[15] M. Berkhout and L. Dooper, "Class-D audio amplifiers in mobile applications," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 5, pp. 992-1002, May 2010.
[16] W. Yan, C. Pi, W. Li, and R. Liu, "Dynamic dead-time controller for synchronous buck DC-DC converters," Electron. Lett., vol. 46, no. 2, pp. 164-165, Jan. 2010.
[17] B.-T. Yeh, C.-H. Yang, K.-C. Juang, and C.-H. Tsai, "Sensorless deadtime exploration for digitally controlled switching converters," in Proc. Int. Symp. VLSI Design, Autom., Test (VLSI-DAT), Apr. 2013, pp. 1-4.
[18] L. Cong, J. Xue, and H. Lee, "A 100 V reconfigurable synchronous gate driver with comparator-based dynamic dead-time control for highvoltage high-frequency DC-DC converters," in Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC), Mar. 2015, pp. 2007-2010.
[19] M. Karimi, M. Ali, A. Aghajani, A. Hassan, M. Sawan, and B. Gosselin, "A 9.2-ns to $1-\mu \mathrm{s}$ digitally controlled multituned deadtime optimization for efficient GaN HEMT power converters," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 69, no. 11, pp. 4381-4394, Nov. 2022.
[20] C.-J. Chen, P.-K. Chiu, Y.-M. Chen, P.-Y. Wang, and Y.-C. Chang, "An integrated driver with adaptive dead-time control for GaN-based synchronous buck converter," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 69, no. 2, pp. 539-543, Feb. 2022.
[21] A. Abuelnasr et al., "Self-adjusting deadtime generator for highefficiency high-voltage switched-mode power amplifiers," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), Oct. 2020, pp. 1-5.
[22] J. H. Li, D. W. Liu, G. W. Shi, L. S. Ding, and G. Y. Zhong, "Design and simulation of solenoid valve driving circuit module for high pressure common rail diesel injector," Appl. Mech. Mater., vols. 602-605, pp. 2645-2648, Aug. 2014.
[23] Cadence, "Spectre circuit simulator reference," Cadence Des. Syst., San Jose, CA, USA, Tech. Rep., Jan. 2019.
[24] R. J. Baker, CMOS: Circuit Design, Layout, and Simulation. Hoboken, NJ, USA: Wiley, 2019.
[25] J.-M. Liu, S.-H. Chien, and T.-H. Kuo, "A 100 W 5.1-channel digital class-D audio amplifier with single-chip design," IEEE J. Solid-State Circuits, vol. 47, no. 6, pp. 1344-1354, Jun. 2012.
[26] H. Ma, R. van der Zee, and B. Nauta, "An integrated 80 V 45 W class-D power amplifier with optimal-efficiency-tracking switching frequency regulation," in Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC), Feb. 2014, pp. 286-287.
[27] Z. Liu, L. Cong, and H. Lee, "Design of on-chip gate drivers with power-efficient high-speed level shifting and dynamic timing control for high-voltage synchronous switching power converters," IEEE J. SolidState Circuits, vol. 50, no. 6, pp. 1463-1477, Jun. 2015.


Ahmed Abuelnasr received the B.Sc. degree in nanotechnology and nanoelectronics engineering from the Zewail City of Science and Technology, Egypt, in 2018. He is currently pursuing the Ph.D. degree with the Electrical Engineering Department, Polytechnique Montréal. His Ph.D. research focuses on the design of efficient high-voltage power amplifiers and developing advanced artificial intelligence (AI)-based tools for accelerating circuit design. His research interests include high voltage mixed-signal analog integrated circuits, power amplifiers, DC/DC converters, deep learning, reinforcement learning (RL), simulation-based optimization, and causality analysis.


Mostafa Amer received the B.Sc. degree in nanotechnology and nanoelectronics engineering from the Zewail City of Science and Technology, Egypt, in 2018. He is currently pursuing the Ph.D. degree with the Electrical Engineering Department, Polytechnique Montréal. His Ph.D. research focuses on the design and optimization of controllers for efficient high-voltage DC/DC converters. His research interests include high-voltage mixed-signal analog integrated circuits, switching DC/DC converters, controller design, device modeling, artificial intelligence (AI)-based generative design, and simulation-based optimization.


Mohamed Ali (Member, IEEE) received the B.Sc. degree in electronics from the Faculty of Electronics Engineering, Menoufia University, Egypt, in 2005, the M.Sc. degree in electronics and communication engineering from Ain Shams University, Egypt, in 2011, and the joint Ph.D. degree in electronics and communication engineering from Ain Shams University, jointly with Polytechnique Montréal, Québec City, Canada, in 2017, where he joined as a Research Intern from 2015 to 2017 as a part of his Ph.D. program, and he is currently a Post-Doctoral Fellow with Polytechnique Montréal. Since 2007, he has been with the Microelectronics Department, Electronics Research Institute, Giza, Egypt. His current research interests include analog, RF, mixed-signal, power management, system-on-chip (SOC), and system-in-package (SiP) designs.


Ahmad Hassan (Member, IEEE) received the Ph.D. degree in electrical engineering from Polytechnique Montréal, QC, Canada, in 2019. He is currently a Post-Doctoral Fellow with the Polystim Neurotechnologies Laboratory, École Polytechnique de Montréal, Montréal. His research interests are oriented toward emerging technologies, integrated circuits for harsh environments and photonic neuromorphic computing. He was a recipient of FRQNT Post-Doctoral Research Scholarship.


Benoit Gosselin (Member, IEEE) received the Ph.D. degree in electrical engineering from the École Polytechnique de Montréal in 2009. He was an NSERC Post-Doctoral Fellow at the Georgia Institute of Technology in 2010. He is currently a Full Professor at the Department of ECE, Université Laval, where he holds the Canada Research Chair of Smart Biomedical Microsystems. His research interests include wireless microsystems for brain-computer interfaces, analog/mixed-mode and RF integrated circuits for neural engineering, interface circuits of implantable sensors/actuators, and point-of-care diagnostic microsystems for personalized healthcare. He is an Associate Editor of the IEEE Transactions on Biomedical Circuits and Systems and he is the Chair and the Founder of the IEEE CAS/EMB Quebec Chapter (2015 Best New Chapter Award). He served on the committees of several int'l IEEE conferences, including NEWCAS, EMBC, LSC, and ISCAS. His significant contribution to biomedical microsystems research led to commercializing the first wireless electro-optic bioimplant to study the development of brain diseases in freely behaving animal models by Doric Lenses Inc. He is a fellow of the Canadian Academy of Engineering. He has received several prestigious awards, including the NSERC Brockhouse Canada Prize and the Prix Génie Innovation of the Quebec Professional Engineering Association OIQ.


Ahmed Ragab received the Ph.D. degree in industrial engineering from Polytechnique Montreal, Canada, in 2014. He is currently a Scientist in Artificial Intelligence (AI) at Natural Resources Canada (NRCan). He is also an Adjunct Professor at the Department of Mathematics and Industrial Engineering, Polytechnique Montréal. He is on leave from the Faculty of Electronic Engineering, Menoufia University, Egypt. His research interests include AI, machine learning, pattern recognition, image processing, data and decisions fusion, causality analysis, reliability modeling, operations research, discrete event systems, and process mining. At NRCan, he has worked on strategic projects funded by the Government of Canada, including forest value chain optimization (FVCO) and carbon capture, utilization and storage (CCUS). His main thematic activities focus on the practical challenges of big data and AI in several industrial applications, including abnormal events diagnosis and prognosis, predictive maintenance, supervisory control, real-time optimization, production scheduling, and systems design. He has a bunch of experience in developing advanced AI algorithms and tools in the manufacturing industry, aiming at reducing energy consumption, greenhouse gas (GHG) emissions, and operational and maintenance costs while improving operation's performance. He also teaches industrial engineering courses at graduate levels and supervises M.Sc. and Ph.D. students.


Yvon Savaria (Fellow, IEEE) received the B.Ing. and M.Sc.A. degrees in electrical engineering from the École Polytechnique Montréal in 1980 and 1982, respectively, and the Ph.D. degree in electrical engineering from McGill University in 1985. Since 1985, he has been with Polytechnique Montréal, where he is currently a Professor with the Department of Electrical Engineering. He has carried out work in several areas related to microelectronic circuits and microsystems, such as testing, verification, validation, clocking methods, defect and fault tolerance, effects of radiation on electronics, high-speed interconnects and circuit design techniques, CAD methods, reconfigurable computing and applications of microelectronics to telecommunications, aerospace, image processing, video processing, radar signal processing, and the acceleration of digital signal processing. Since June 2019, he has been the NSERC-Kaloom-Intel-Noviflow (KIN) Chair Professor. He has been working as a Consultant or was sponsored for carrying out research with Bombardier, Buspass, CNRC, Design Workshop, Dolphin, DREO, Ericsson, Genesis, Gennum, Huawei, Hyperchip, Intel, ISR, Kaloom, LTRIM, Miranda, MiroTech, Nortel, Octasic, PMC-Sierra, Space Codesign, Technocap, Thales, Tundra, and Wavelite. He is also involved in several projects related to embedded systems in aircrafts, wireless sensor networks, virtual networks, softwaredefined networks, machine learning (ML), embedded ML, and computational efficiency and application-specific architecture design. He holds 16 patents, has published 190 journal articles and 485 conference papers, and was the thesis advisor of 190 graduate students who completed their studies.
He is also a fellow of the Canadian Academy of Engineering. He was the Program Co-Chairman of NEWCAS'2018 and the General Chairman of NEWCAS'2020. He is a member of the Executive Committee of the Regroupement Stratégique en Microélectronique du Québec (RESMIQ) and a member of the Ordre des Ingénieurs du Québec (OIQ). In 2001, he was awarded the Tier 1 Canada Research Chair (www.chairs.gc.ca) on the design and architecture of advanced microelectronic systems that he held until June 2015. He also received the Synergy Award of the Natural Sciences and Engineering Research Council of Canada in 2006.


[^0]:    Manuscript received 10 September 2022; revised 5 December 2022; accepted 19 December 2022. This work was supported in part by the Natural Sciences and Engineering Research Council of Canada (NSERC) and in part by the Mathematics of Information Technology and Complex System (MITACS). This article was recommended by Associate Editor X. Zhou. (Corresponding author: Ahmed Abuelnasr.)
    Ahmed Abuelnasr, Mostafa Amer, Mohamed Ali, Ahmad Hassan, and Yvon Savaria are with the Department of Electrical Engineering, Polytechnique Montréal, Montréal, QC H3T 1J4, Canada (e-mail: ahmed.abuelnasr@polymtl.ca).
    Benoit Gosselin is with the Department of Electrical and Computer Engineering, Laval University, Québec City, QC G1V 0A6, Canada.
    Ahmed Ragab is with CanmetENERGY, Varennes, QC J3X 1P7, Canada, and also with the Department of Mathematics and Industrial Engineering, Polytechnique Montréal, Montréal, QC H3T 1J4, Canada, on leave from the Faculty of Electronic Engineering, Menoufia University, Menouf 32952, Egypt.
    Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSI.2022.3232074.

    Digital Object Identifier 10.1109/TCSI.2022.3232074

