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Delay Mismatch Insensitive Dead Time Generator for High-Voltage Switched-Mode Power Amplifiers

Ahmed Abuelnasr, Mostafa Amer, Mohamed Ali, *Member, IEEE*, Ahmad Hassan, *Member, IEEE*, Benoit Gosselin, *Member, IEEE*, Ahmed Ragab, and Yvon Savaria, *Fellow, IEEE*

***Abstract*— The Design of efficient, safe, and reliable circuits is a prime objective in high-voltage (HV) electronic systems, such as switched-mode power amplifiers (PAs). One of the main causes of efficiency degradation and reliability problems, in these amplifiers, is the shoot-through current from the HV power supply to the ground. To eliminate such current, a dead time generator (DTG) is used to modify the signals propagating through the high-side and low-side gate drivers by adding a fixed dead time between them. However, any delay mismatch between these gate drivers can reduce the dead time to the point that it becomes negative. In this paper, an HV-DTG architecture is introduced. The architecture mitigates the effects of delay mismatch variations in gate drivers, which can result from parameters mismatch, fabrication process variations, and temperature variations. An HV switched-mode class-D power amplifier is used to illustrate the performance of the DTG. The amplifier is implemented in a low-cost 0.35 μm HV CMOS process. The total area of the PA is 0.5 mm^2, where the DTG covers an area of 0.066 mm^2. A measured system's efficiency of 95.14% is achieved with the shortest dead time of 10.8 ns, which is 1.38x smaller than the generated dead time in comparable state-of-the-art HV dead time generators.**

***Index Terms*— Dead time generator, power amplifiers, switched-mode power amplifiers, class-D amplifier, high-efficiency circuits, fabrication process & temperature variations, shoot-through current.**

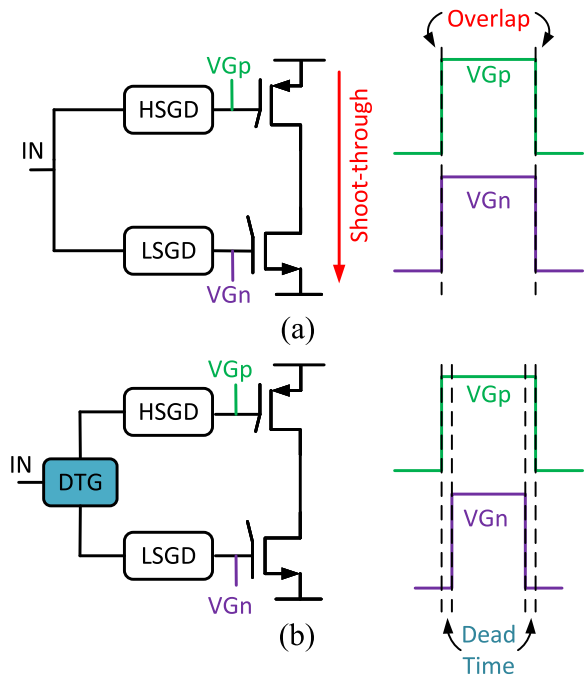

Fig. 1. Power amplifier block diagrams. (a) Without dead time generator. (b) With dead time generator.

I. Introduction

EFFICIENCY and reliability in high-voltage (HV) electronic systems are major concerns, especially in critical applications such as those found in the automotive and aviation industries [1], [2], [3]. Recent developments in HV semiconductor technologies led to the emergence of efficient and fully-integrated HV systems such as power amplifiers (PAs) and DC-DC converters [4], [5]. This helps in reducing cost, size, weight, and increase the density of power sensor interfaces and electric power distribution networks in listed applications, which improves their safety and reliability [1].

Owing to the high efficiency of the switched-mode amplifier topologies, such as class-D power amplifiers, they play a key role in many applications such as audio amplifiers, motor drivers, constant power supplies, and piezo-electric actuator drivers [1], [2], [6], [7], [8]. Even though the theoretical efficiency of switched-mode PAs can be close to 100%, practically, there are several sources of power losses that degrade their efficiency. Conduction and switching losses, which are due to the finite ON-resistance and the large gate capacitance of power transistors, are the two main sources of power losses in switched-mode PAs. In addition, switched-mode PAs suffer from the shoot-through currents that happen when their high-side and low-side power transistors

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are conducting at the same time. Such currents degrade their efficiency and pose safety concerns [9], [10], [11].

A typical configuration of a switched-mode PA is shown in Fig. 1(a). It consists of two complementary power MOSFETs, a high-side gate driver (HSGD) and a low-side gate driver (LSGD). This configuration has safety and reliability issues due to the possible overlapping time interval between the signals provided by the HSGD and LSGD; VGp and VGn, respectively. During this overlapping time interval, the two power MOSFETs are ON and a shoot-through current flows from the HV power supply to the ground. This current leads to a very high power consumption and can potentially burn the circuit [6], [9], [10]. To prevent shoot-through currents, the input signal to the HSGD and LSGD can be split by a dead time generator (DTG) into two signals with a dead time between their respective active periods during which both transistors are OFF as shown in Fig. 1(b).

Even though the dead time is required to prevent the shoot-through currents, it creates other potential problems that need to be mitigated. During the dead time interval, when the two power MOSFETs of the PA are OFF, the passive filter imposes output current continuity through the internal body-diode of the low-side power MOSFET leading to unwanted power consumption and a reduction in the power efficiency [9], [12], [13]. The power consumed in the body-diode is:

$$P_{BD} = V_{SD} F_{SW} (I_{out,peak} t_{dead\,time} + I_{rr} t_{rr}) \tag{1}$$

where V_{SD} is the voltage across the diode, F_{SW} is the switching frequency, $I_{out,peak}$ is the peak output current, $t_{dead\,time}$ is the dead time, I_{rr} is the diode reverse recovery current, and t_{rr} is the reverse recovery time [6]. Thus, this power consumption is directly proportional to the dead time interval. In addition, having the two power MOSFETs OFF for long time distorts the output waveform, which is highly undesirable in audio amplifiers such as class-D power amplifiers [14], [15]. Moreover, long dead times can lead to a momentary loss of control which can be problematic for amplifiers in electro-hydraulic actuators [6], [9], [13]. Consequently, the introduced dead time intervals need to be as short as possible to reduce the power consumption in the body-diode, reduce the signal distortion, and improve the efficiency of the PA [9], [12], [13]. However, a very short fixed dead time is hard to maintain due to the possible delay mismatch between the HSGD and LSGD, and the dependence of this delay on the process, voltage, and temperature (PVT) variations as mentioned in [9].

In previous works reported in the literature, the dead time was dynamically adjusted to generate an optimal value that prevents shoot-through currents. Some designs used digital-based implementations to adjust the dead time. For example, the circuit presented in [16] adjusts the dead time using a senseFET, passive components, a flip-flop, a finite state machine, and a capacitor array. In [17], the dead time generator is integrated with a digital feedback controller to generate an optimal dead time value. Other implementations use passive components and comparators to generate the dead time [18], or use senseFETs to detect the body-diode conduction followed by comparators and digital circuits to adjust the dead time [13]. The works presented in [10] and [19] propose an adjustable dead time generator using a structure composed of current sources and switched capacitors, while the work in [20] uses analog comparators and a digitally-controlled delay cell to adjust the dead time. Some of the reported designs use passive devices and analog components that are highly susceptible to noise. Moreover, some designs either need additional complex circuits for dead time calculations, or require calibration to offset any unwanted variations. Other designs are implemented in low-voltage technology, and hence require scaling and adaptation to properly operate in the HV domain. The negative effects of PVT variations on the gate drivers' delay mismatch and the generated dead time were considered in previous works such as [9], [10], [18], and [19]. These effects were mitigated in such works, either by externally calibrating the dead time generator, or by accounting for them through corner simulations.

This paper validates, analyzes, and extends the work proposed in [21] on a delay mismatch insensitive DTG (DMI-DTG) circuit. It notably provides a more detailed explanation of the architecture and of the design steps of the DMI-DTG, as well as of the design steps of a novel level-down shifter. The introduced DMI-DTG combines inverters, NOR gates, and HV level-down shifters to generate an always positive dead time that is proportional to the delays of the gate drivers and level-down shifters. Moreover, the insensitivity of the generated dead time to delay mismatch variations is validated through detailed analytical design equations and circuit simulations. Finally, the performance of the circuit is validated experimentally in an integrated HV power amplifier system, which is designed to drive a solenoid valve in an electro-hydraulic actuator [5], [22].

The DMI-DTG offers the following advantages:

- It generates the shortest possible dead time to ensure safe operation, while preventing cross-conduction of the half-bridge power MOSFETs, and improving the amplifier's efficiency.
- It adapts to any variations in the delays of the gate drivers that may arise due to PVT variations.
- It does not require passive components, complex digital or analog circuits, body-diode monitoring, power MOSFETs current-sensing, or other detection methods, unlike most of the previously reported methods.
- It can easily be integrated with HV switched-mode PAs as it adjusts the dead time using integrated HV level-down shifters, inverters and NOR gates.

In the remaining parts of the paper, the detailed architecture of the DMI-DTG circuit and analysis of the analytical design equations required for dead time calculations are presented in Section II. Section III presents the switched-mode PA with the integrated DMI-DTG circuit. Experimental results of the amplifier prototype, integrated with a 0.35 μm HV CMOS process, are shown in Section IV, and finally Section V concludes the paper.

II. Dead Time Generators: Overview and Analysis

In this section, we first present the fixed DTG topology, then we introduce the modifications needed to construct the DMI-DTG.

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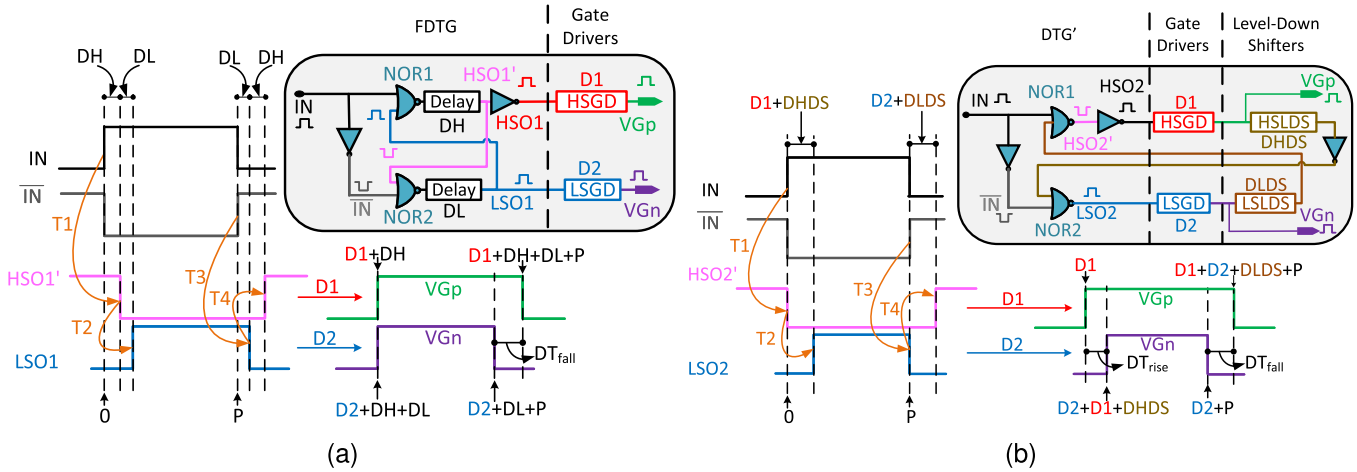

Fig. 2. Dead time generators architecture and waveforms. (a) Fixed dead time generator (FDTG). (b) Delay mismatch insensitive dead time generator (DTG' & level-down shifters).

A. The Fixed Dead Time Generator

The operation and importance of the DMI-DTG can be highlighted by first explaining the fixed DTG solution. Fig. 2(a) shows the circuit diagram of a fixed DTG and the corresponding waveforms for inputs and outputs. The circuit consists of two NOR gates, inverters, and two delay elements. Its operation depends on the transition dependency of the NOR gates signals. If the input (IN) of the upper NOR gate (NOR1) starts at 0 (low) and the input ($\overline{IN}$) of the lower NOR gate (NOR2) is 1 (high), the $LSO1$ (low side output) node starts at 0 and the $HSO1$' (high side output) node starts at 1. $HSO1$ is the signal fed to the HSGD, VGp is the output of HSGD and applied to the gate of the high-side power MOSFET, and $D1$ is the delay of the HSGD. Similarly, $LSO1$ is the signal applied to the LSGD, VGn is generated from the LSGD and applied to the gate of the low-side power MOSFET, and $D2$ is the delay of the LSGD. To simplify calculations, we assume symmetric falling-edge and rising-edge delays and negligible delays from the NOR gates and inverters. The transition of IN from 0 to 1 and from 1 to 0 results in four transitions $T_{(1-4)}$ as follows:

- Transition 1 (T_1): A transition of IN from 0 to 1 results in two transitions, the transition of $\overline{IN}$ from 1 to 0 (which is instantaneous assuming the propagation delay of the inverter is negligible), and the transition of $HSO1$' from 1 to 0 which is delayed by the delay element DH.
- Transition 2 (T_2): A transition of $HSO1$' from 1 to 0 makes both inputs of NOR2 ($HSO1$' & $\overline{IN}$) 0. This results in the transition of $LSO1$ from 0 to 1 which is delayed by the delay element DL.
- Transition 3 (T_3): A transition of IN from 1 to 0 results in two transitions, the transition of ($\overline{IN}$) from 0 to 1 (which is instantaneous assuming the propagation delay of the inverter is negligible), and the transition of $LSO1$ from 1 to 0 with a delay DL.
- Transition 4 (T_4): A transition of $LSO1$ from 1 to 0 makes both inputs of NOR1 ($LSO1$ & IN) 0. This results in the transition of $HSO1$' from 0 to 1 delayed by DH.

The dependency between the signals of the NOR gates and the added delay elements (DH & DL) results in this transition of signals $T_{(1-4)}$ which leads to the formation of a fixed dead time between HSO1 and LSO1. In this case, the initial rising-edge dead time (DT_{rise}) is equal to DL and the initial falling-edge dead time (DT_{fall}) is equal to DH. The signals generated from the dead time circuit are then applied to the power MOSFETs through the implemented gate drivers (HSGD and LSGD). The delay of the HSGD ($D1$) affects VGp, while the delay of the LSGD ($D2$) affects VGn. From the waveforms shown in Fig. 2(a), we can calculate DT_{rise} and DT_{fall} after propagating through the HSGD and LSGD.

$$\begin{aligned} DT_{fall} &= D1 + DH + DL + P - (D2 + DL + P) \\ &= DH + (D1 - D2) = DH + \Delta DT \end{aligned} \tag{2}$$

where ΔDT is the delay mismatch between HSGD and LSGD, and P is the falling-edge time of the IN waveform.

$$\begin{aligned} DT_{rise} &= D2 + DH + DL - (D1 + DH) \\ &= DL - (D1 - D2) = DL - \Delta DT \end{aligned} \tag{3}$$

From (2) & (3), we can see that DT_{rise} is reduced by the delay mismatch value ΔDT. Accordingly, if $DL = \Delta DT$, DT_{rise} will diminish while DT_{fall} will increase by a value equal to ΔDT. This will result in an overlap between VGp and VGn signals at the rising edge. Consequently, a shoot-through current will propagate from the HV power supply to the ground. Therefore, the fixed DTG configuration makes the system susceptible to the shoot-through currents, especially when there are variations in the delay mismatch ΔDT.

B. The Delay Mismatch Insensitive Dead Time Generator

To handle the issue of the delay mismatch between the HSGD and LSGD, a DMI-DTG is introduced as shown in Fig. 2(b). It consists of two NOR gates, inverters and two level-down shifters added after the HSGD and LSGD to scale down the signals provided to the NOR gates. Using this configuration, the resulting dead time will be intrinsically adjusted in accordance with the delays of the HSGD and LSGD without diminishing the rising-edge or falling-edge dead times as in the case of the fixed DTG. Following the

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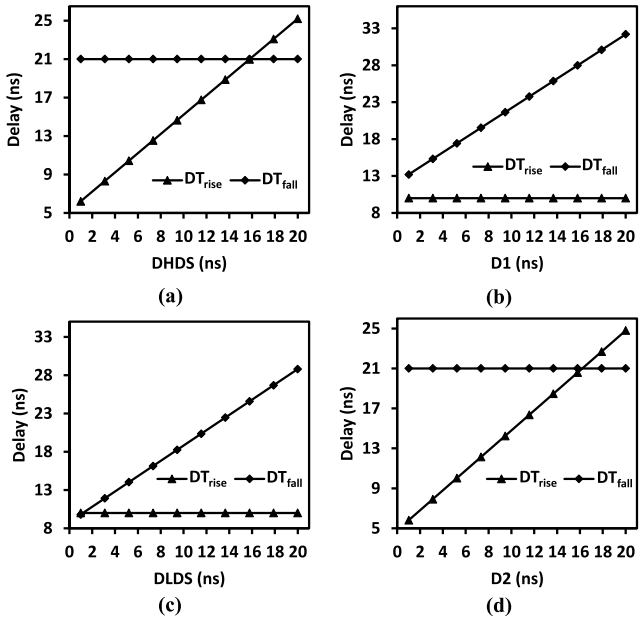

Fig. 3. Rising-edge dead time and falling-edge dead time variation with the delay variations of high-side and low-side gate drivers and level-down shifters. (a) High-side level-down shifter delay variation. (b) High-side gate driver delay variation. (c) Low-side level-down shifter delay variation. (d) Low-side gate driver delay variation.

waveforms depicted in Fig. 2(b), the rising-edge and falling-edge dead times are calculated as follows:

$$DT_{rise} = D2 + D1 + DHDS - D1 = D2 + DHDS \quad (4)$$

$$DT_{fall} = D1 + D2 + DLDS + P - (D2 + P) = D1 + DLDS \quad (5)$$

where $D1$ and $D2$ are the delays of HSGD and LSGD, respectively. $DHDS$ and $DLDS$ are the delays of high-side level-down shifter and low-side level-down shifter, respectively. Now, DT_{rise} depends only on the summation of $DHDS$ and $D2$. Similarly, DT_{fall} depends only on the summation of $DLDS$ and $D1$. Therefore, our dead time generator is insensitive to the delay mismatch between the HSGD and LSGD.

C. Verification of the Analytical Model

To verify the analytical design equations, the DMI-DTG architecture, shown in Fig. 2(b), was implemented and simulated using Cadence® tools [23]. In our simulations, we swept the delay of the gate drivers and that of the level-down shifters separately from 1 to 20 ns, while keeping all other delays constant, and we observed the impact on both the rising and the falling edges of the resulting dead time signals. The default delays of the various building blocks of the DMI-DTG and the gate drivers are set as follows: $D1 = 8.8$ ns, $D2 = 5.2$ ns, $DHDS = 4.8$ ns and $DLDS = 12.2$ ns. According to the formulated analytical equations $DT_{rise} = D2 + DHDS = 5.2 + 4.8 = 10$ ns, $DT_{fall} = D1 + DLDS = 8.8 + 12.2 = 21$ ns. In Fig. 3(a), the delay of the HSLDS ($DHDS$) is varied and, as expected from the analytical design equations, only DT_{rise} varies with the variation of $DHDS$. Similarly, when varying $D2$ in Fig. 3(d), only DT_{rise} varies, while DT_{fall} remains unaffected. When varying $D1$ in Fig. 3(b) and $DLDS$ in Fig. 3(c), only DT_{fall} varies, while DT_{rise} remains constant in agreement with the analytical design equations.

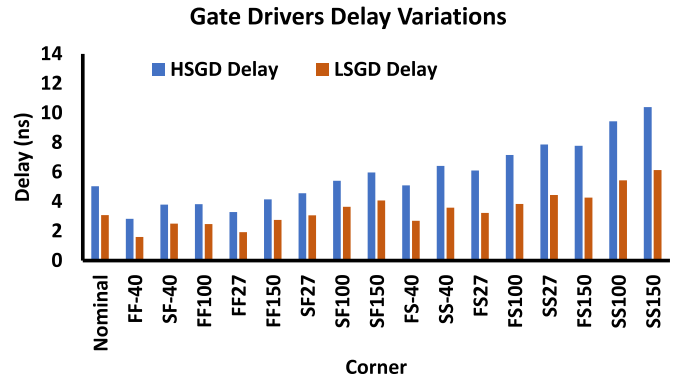

Fig. 4. Simulation of the variations in the gate drivers delay at different process corners and different temperatures.

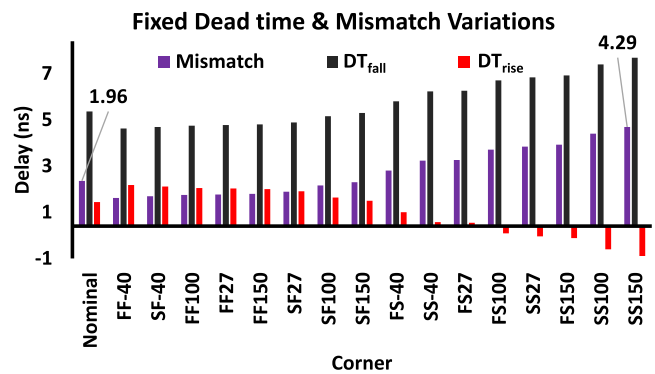

Fig. 5. Simulation of the variations in the delay mismatch, rising-edge dead time and falling-edge dead times at different process corners and different temperatures if a fixed dead time generator is used.

To illustrate the significance of the DMI-DTG over the fixed DTG, variations in the delay of the HSGD and LSGD, with the process and temperature variations (through conducting corner simulations) are shown in Fig. 4. The circuit was simulated in four process corners (SS, SF, FS, FF) and under 4 different temperatures (−40, 27,100,150) °C. Where S stands for slow, F stands for fast, the first letter is for NMOS, and the second letter is for PMOS. For example, SF27 is for slow NMOS, fast PMOS corner at 27 °C. Fig. 4 has 16 different states representing the combination between the four different corners and the four different temperatures, in addition to the nominal state which represents the typical-NMOS-typical-PMOS at room temperature. The figure illustrates the effect of the process corners and temperature variations on the delays of the gate drivers, this translates into a variation in the delay mismatch between the HSGD and LSGD. Fig. 5 illustrates the variations in the delay mismatch between the HSGD and LSGD in the 16 different states. It also shows the variations in the rising and falling edge dead times if a fixed DTG, generating a dead time of 3 ns is used. The largest variation value can be seen at the slow NMOS slow PMOS corner with a temperature of 150 ° C. At this state, a 4.29 ns delay mismatch is obtained, where the nominal value (at typical-typical process corner and under room temperature) for the delay mismatch

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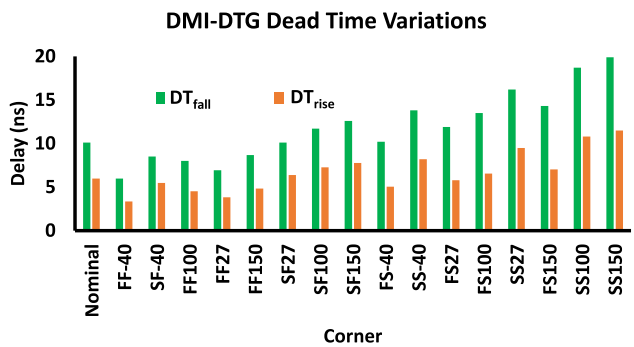

Fig. 6. Simulation of the variations in the rising-edge and falling-edge dead times at different process corners and different temperatures for the DMI-DTG.

is equal to 1.96 ns. Accordingly, the process and temperature variations result in a 2.2× increase in the delay mismatch. As shown in Fig. 5, the rising edge dead time diminishes and becomes negative with the variation of the delay mismatch. This is due to the dependence of the rising edge dead time on the delay mismatch as illustrated in the previous section. Thus, exploiting a fixed DTG does not seem to be a good solution as the required dead time depends on the process and temperature variations, leading to possible shoot-through current problems.

Similarly, variations in rising-edge and falling-edge dead times caused by the process and temperature variations when using the DMI-DTG are shown in Fig. 6. It should be noted that in both architectures, the DMI-DTG and the fixed DTG, process variations will result in varying the delays of the gate drivers leading to a variation in the delay mismatch. This delay mismatch negatively affects the dead time generated by the fixed DTG, however, in the DMI-DTG, this delay mismatch does not affect the generated dead time, as shown in Fig. 6, positive rising-edge and falling-edge dead times are always obtained.

III. Switched-Mode Power Amplifier With Integrated Dead Time Generator: Design & Implementation

The DMI-DTG is integrated and validated in the typical switched-mode PA topology shown in Fig. 7. The amplifier is integrated with a 0.35 μm HV CMOS process. It consists of five main blocks: a half-bridge, an HSGD, an LSGD, a DTG, and an off-chip passive filter. Each gate driver consists of a level-up shifter and a buffer. The DMI-DTG architecture consists of three components; a DTG' and two level-down shifters. The DTG' consists of inverters and two NOR gates, while the detailed design of the level-down shifters is highlighted in the following subsections. The off-chip filter consists of a 1 mH inductor and a 100 nF capacitor. The amplifier is supplied by two HV power supplies (24V and 12V) and a low-voltage power supply (3.3V). The input to the amplifier is a 500 kHz pulse-width modulated (PWM) signal (0-3.3)V, while the load is (a 100 mH inductor in series with a 342.5 Ω resistor), representing a solenoid valve in an electro-hydraulic actuator [22]. In the next subsections, the rest of the amplifier components will be described in detail.

A. Half-Bridge

The half-bridge (HB) consists of two large power MOSFETs: a PMOS and an NMOS. To increase the efficiency of the PA, power losses (in the half-bridge and other circuits in the amplifier) must be reduced. There are two main sources of power loss in the half-bridge; the conduction loss and the gate-switching loss [7]. The conduction loss (P_{cond}) occurs due to the flow of the output current through the finite ON-resistance of the power MOSFETs, where $P_{cond} = I_{out}^2 R_{ON}$. While gate-switching loss (P_{gsw}) occurs due to the charging and discharging of the gate capacitance of the power MOSFETs when turning them ON and OFF, where $P_{gsw} = Q_g V F_{sw}$, $Q_g = \int_{V1}^{V2} C_g \, dV$ and C_g is proportional to the gate width (W) times the gate length (L) of the MOSFETs. Thus, minimizing R_{ON} and C_g reduces conduction losses and switching losses, respectively.

$$R_{ON} = L/(W \mu_n C_{ox}(V_{GS} - V_{th} - V_{DS}/2)) \tag{6}$$

According to (6), R_{ON} is decreased by increasing the transistor gate width (W). However, increasing W increases C_g, which increases the gate-switching loss, thus, a suitable balance must be found when choosing W to reduce both conduction and gate-switching losses. Reducing L reduces both the switching and conduction losses, therefore a minimum length is selected for the transistors. For an optimum balance, R_{ON} and C_g of the implemented power transistors (at minimum gate length, L) are simulated in Fig. 8 as a function of the gate width. As W increases, R_{ON} decreases rapidly at the beginning, then it decreases asymptotically, and eventually, very small changes are obtained by further increasing W. On the other hand, C_g increases linearly with W. A Width of 5 mm is selected for the NMOS, which corresponds to an ON-resistance of 4.6 Ω, while a width of 8 mm is selected for the PMOS which corresponds to an ON-resistance of 8 Ω. Any further increase in W, for either the NMOS or the PMOS, will result in modest reductions in R_{ON} and large increases in C_g which will complicate the design of the buffer chain. At W = 8 mm, the C_g of the PMOS is 14.8 pF, and at W = 5 mm, the C_g of the NMOS is 10 pF (as shown in Fig. 8).

B. Buffer Chains

Using the outputs from the level-up shifters directly to drive the large gate capacitance of the power MOSFETs will result in a large delay. Driving such a capacitance with a minimum size buffer yields propagation delays of 32 ns and 38 ns when driving the NMOS and the PMOS, respectively. To minimize this propagation delay, a tapered topology for designing the buffer is considered. In this topology, a chain of inverter stages is used with the size of each stage being k times larger than the preceding stage. The total delay of a tapered buffer driving a capacitive load can be calculated using (7) [24]:

$$T_{tapered} = T_0 \frac{k}{ln(k)} ln(y) \tag{7}$$

where $y = C_{load}/C_{in}, k = y^{1/N}$ is the tapering factor, N is the number of inverter stages, C_{load} is the buffer load capacitance which is the gate capacitance of the NMOS or

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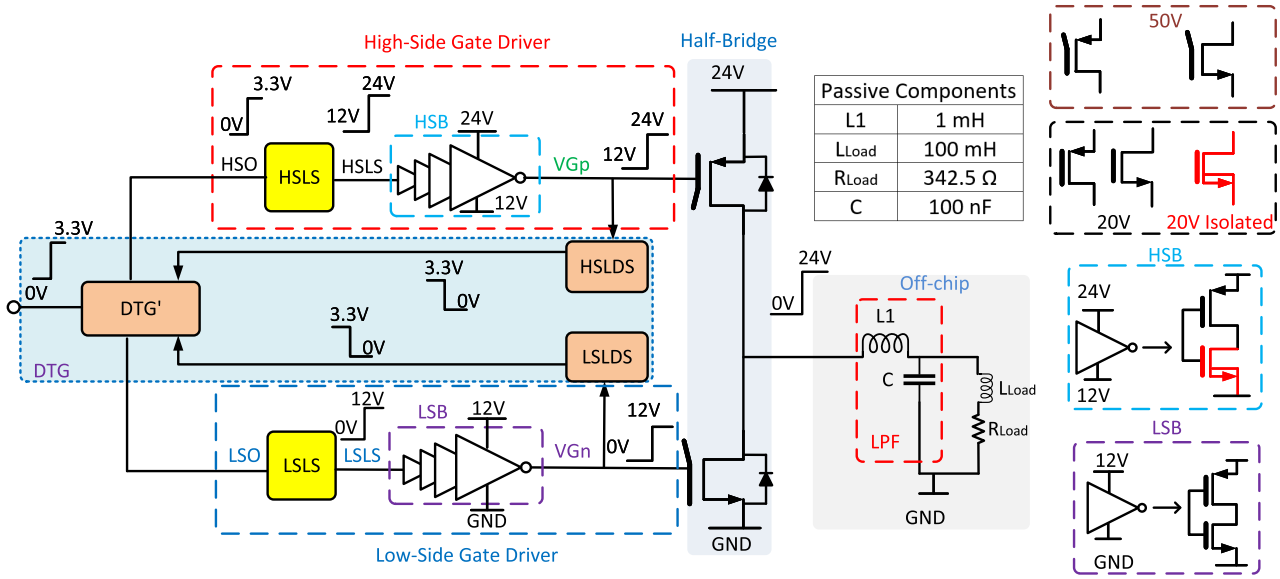

Fig. 7. The switched-mode class-D power amplifier block diagram, with the passive off-chip components and the different types of used high-voltage transistors (shown on the right).

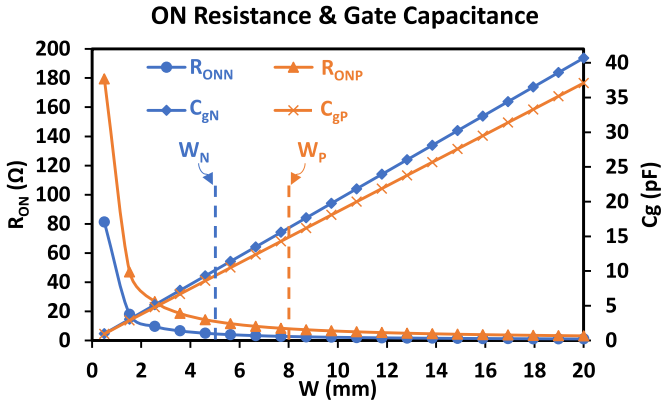

Fig. 8. ON-resistance and gate capacitance of NMOS and PMOS devices versus gate width (R_{ONN} and C_{gN} for NMOS), (R_{ONP} and C_{gP} for PMOS).

PMOS power transistors, and C_{in} is the gate capacitance of a minimum size inverter. The minimum size inverter was implemented with a PMOS transistor with minimum length and 15μm width, and an NMOS transistor with minimum length and 10μm width. Using (7), and following the steps given in [24], the number of inverters in the buffer chain (N) for each power MOSFET and the tapering factor k were found to be 4 and 3, respectively. The designed tapered buffer chains are shown in Fig. 7, where HSB is the high-side buffer chain and LSB is the low-side buffer chain. The HSB is designed using isolated NMOS transistors, where the body and source terminals of the device are not grounded, but connected to a floating 12V supply. Accordingly, the transistors need to be isolated to support this floating voltage without damaging the substrate. In comparison to the minimum size buffer, using the tapered buffer reduces the propagation delay for driving the power NMOS by 6.4 times, while the propagation delay for driving the power PMOS is reduced by 6.9 times.

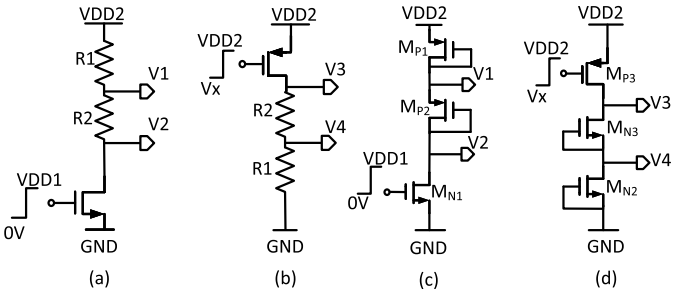

Fig. 9. Different configurations to illustrate the operation of level shifters: (a) and (b) are level-up and level-down shifters with resistors, while (c) and (d) are level-up and level-down shifters with diode-connected transistors.

C. Level Shifters

To produce suitable gate drive signals for the NMOS and PMOS power transistors in the [0-12]V and [12-24]V domains, the input low-voltage PWM signal must be shifted from [0-3.3]V to the required voltage levels. This can be realized using level-up shifters. The different diagrams in Fig. 9, describe the basic operation of the level-up and level-down shifters.

The simplest way to shift a voltage signal from one level to another is to use a pulsed current source and resistors ladder. An example of this configuration is shown in Fig. 9(a), where the input signal can be shifted from $[0 - VDD1]$ to $[VDD2/n - VDD2]$, where n is the number of equal-value resistors. It is always recommended to use ratioed resistors as this will minimize the effect of layout mismatch between the resistors after fabrication. Using the principle of duality, we shift the signal from a high-voltage domain to a low-voltage domain by using a PMOS, instead of an NMOS, as the current source, and connecting the resistors to the ground as shown in Fig. 9(b). Resistors are passive components that consume high power and occupy a large silicon area. Instead, diode-connected transistors are used to limit the voltage to the required level as shown

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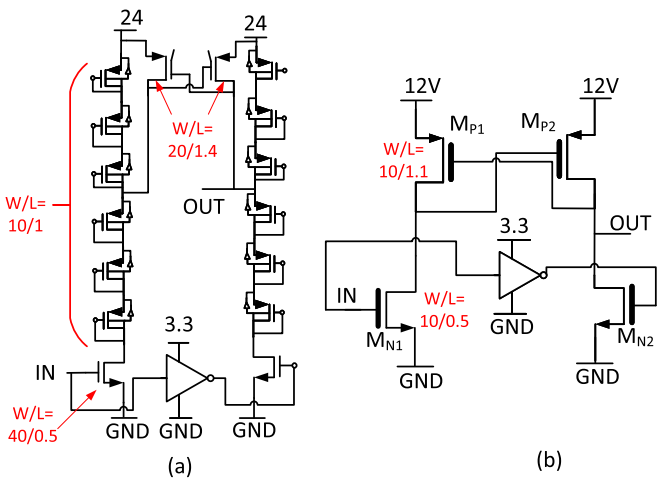

Fig. 10. Circuit diagrams of the implemented level-up shifters. (a) High-side level-up shifter. (b) Low-side level-up shifter.

in Fig. 9(c) and 9(d). The sizes of the diode-connected transistors are adjusted to clip the voltage and achieve the required output, taking into account the proper voltage ratings. The proposed circuit designs for the level-up and level-down shifters to be used in the PA system are explained in more detail below.

1) Level-Up Shifters Design: Configurations of both the high-side and low-side level-up shifters are shown in Fig. 10. A conventional Cascode Voltage Switch Logic (CVSL) configuration with identical left and right branches is utilized for the level-up shifters. The CVSL configuration ensures that once an initial state is reached on one side, an opposite state is reached quickly on the other side, while the output is kept in a quasi-static state until a change is done to the input. A slight modification to the conventional CVSL is implemented by adding extra diode-connected transistors to limit the output voltage swing between 12V and 24V.

The diode-connected transistors are low-voltage isolated PMOS transistors that can tolerate V_{GS} of 5V and V_{DS} of 5V with bulks isolated from the substrate. This limits the voltage drop over each transistor to 5V, which is in the safe operating region. In our case, 12V at the output can be obtained by using 6 transistors with a 4V drop across each transistor. The NMOS pulsed current source transistors, one on each side, can tolerate 50V between the drain and the source and 5V between the gate and the source. The low-side level-up shifter shown in Fig. 10(b) is similar to the high-side level-up shifter depicted in Fig. 10(a), except that the output swing is between 0 and 12V. Accordingly, no extra limiting transistors are required, and we can use a conventional CVSL configuration. The PMOS transistors are high-voltage transistors that can tolerate 20V between the drain and the source and a maximum of 20V on the gate. The NMOS transistors have thin gate-oxide that can tolerate 20V between the drain and the source and 5V between the gate and the source.

2) Level-Down Shifters Design: Fig. 11 presents the high-side and low-side level-down shifters. The operation of each level shifter is exactly the same as the other except that the high-side level-down shifter level shifts the signal from [12-24]V to [0-3.3]V, while the low-side level-down shifter

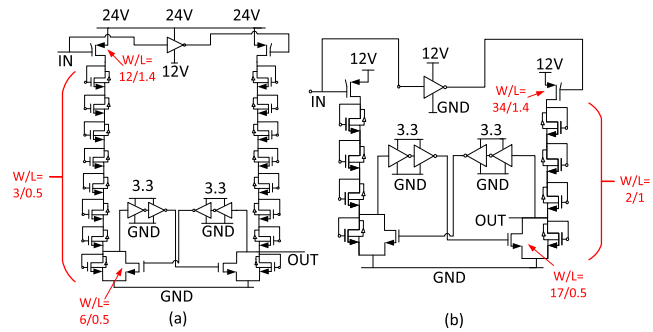

Fig. 11. Circuit diagrams of the implemented level-down shifters. (a) High-side level-down shifter. (b) Low-side level-down shifter.

shifts the signal from [0-12]V to [0-3.3]V. Using the principle of duality and applying it to the CVSL configuration, we can easily design the level-down shifter.

The input of the high-side level-down shifter is between [12-24]V which requires the usage of an isolated NMOS in the upper inverter, in addition, 8 isolated diode-connected NMOS transistors are utilized to scale down the 24V signal to 3V by introducing voltage drops of 3V each. At the output, low-voltage inverters are used to obtain a voltage swing between [0-3.3]V. The operation of the low-side level-down shifter is similar to the operation of the high-side level-down shifter except that only 4 isolated diode-connected transistors are utilized. Isolated transistors are adopted so that the body is isolated from the substrate, accordingly other voltages can be connected to the body other than the lowest voltage which ensures that the chip substrate is always connected to the lowest voltage.

IV. Experimental Results and Discussion

The amplifier prototype including the DMI-DTG circuit is fabricated with a 0.35 μm HV CMOS process. The chip micrograph of the integrated amplifier as well as the layout views of the various integrated blocks are shown in Fig. 12. The amplifier occupies an area of 0.5 mm^2. The chip is wire-bonded inside a pin grid array (PGA) ceramic package. The latter is soldered on a custom printed-circuit board (PCB) for characterization. Off-chip 1 mH inductor and 100 nF capacitor were used to build the low-pass filter. In addition, a 100 mH inductor was used as an inductive load in series with a purely resistive load. The amplifier test bench is depicted in Fig. 12. In this setup, a 4-channel oscilloscope was used to display the system output signals, two power supplies were used to supply the required voltage levels and one function generator was used to provide the required input PWM signal. A breakdown of the percentage of the area occupied by different blocks in the PA is shown in Fig. 13. The total percentage of the area covered by the dead time generator (DTG', HSLDS & LSLDS) with respect to the area of the PA is 13.3% (0.066 mm^2). Measured input (VGp, VGn) and output ($HSLDS$, $LSLDS$) signals of the implemented high-side and low-side level-down shifters are depicted in Fig. 14. The rising-edge and falling-edge delays were measured and the average was taken to be the delay value. The averaged measured delay of the high-side level-down shifter $DHDS = (5.6+4)/2 = 4.8$ ns, while the averaged

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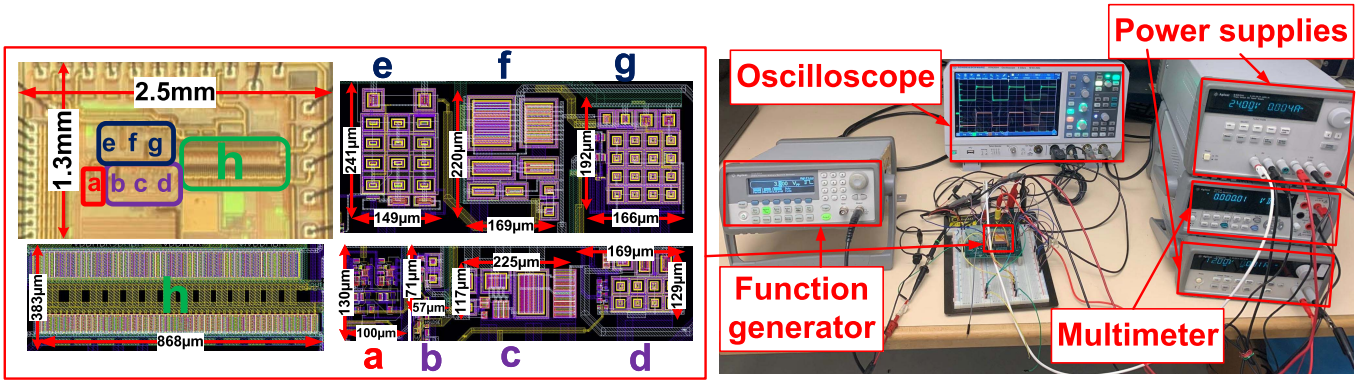

Fig. 12. Experimental setup (right), fabricated chip micrograph and detailed circuit blocks of the system layout (left). a) DTG'. b) Low-side level-up shifter. c) Low-side buffer. d) Low-side level-down shifter. e) High-side level-up shifter. f) High-side buffer. g) High-side level-down shifter. h) Half-bridge.

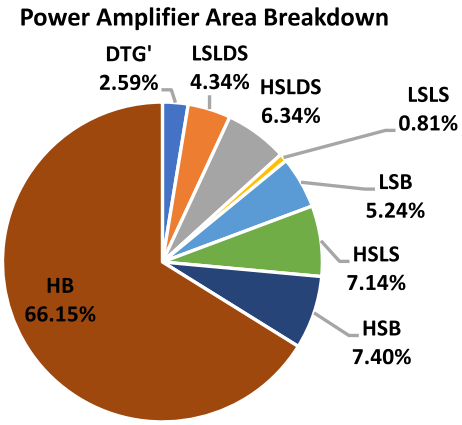

Fig. 13. Area percentage breakdown of the PA's circuit components.

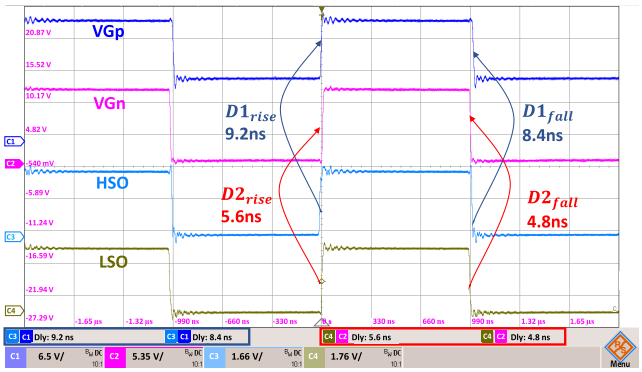

Fig. 15. Measured rising-edge and falling-edge delays of the high-side and low-side gate drivers.

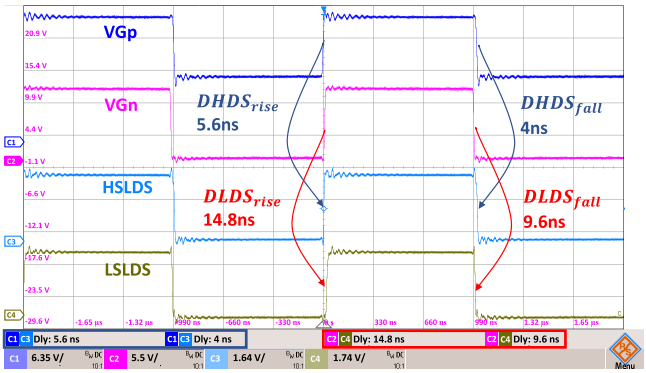

Fig. 14. Rising-edge and falling-edge delays of the high-side and low-side level-down shifters.

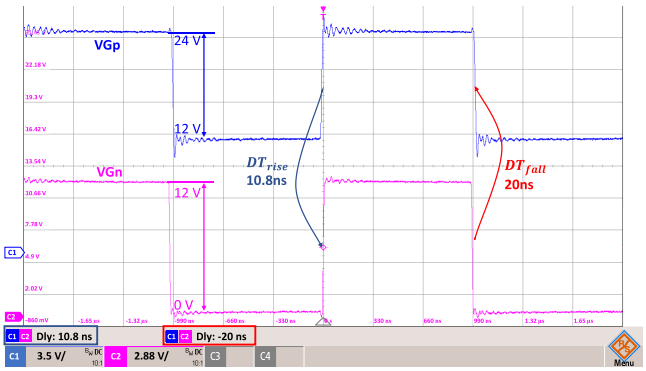

Fig. 16. Measured rising and falling-edge dead times.

measured delay of the low-side level-down shifter $DLDS = (14.8+9.6)/2 = 12.2$ ns as shown in Fig. 14.

The measured input and output waveforms of the HSGD and LSGD are shown in Fig. 15. The resulting delay from the HSGD $(D1) = (9.2+8.4)/2 = 8.8$ ns, and the delay of the LSGD $(D2) = (5.6+4.8)/2 = 5.2$ ns. Using the analytical design equations derived in Section II, the actual dead time can be calculated using the measured delays for the various components as follows:

$$DT_{rise} = D2 + DHDS = 5.2 + 4.8 = 10 \text{ ns.}$$
$$DT_{fall} = D1 + DLDS = 8.8 + 12.2 = 21 \text{ ns.}$$

The obtained delays are very close to the measured delays at the gates of the power MOSFETs shown in Fig. 16. Where $DT_{rise} = 10.8$ ns and $DT_{fall} = 20$ ns. The difference between the calculated and measured delays does not exceed 1 ns, resulting in an error of less than 7.4% in DT_{rise} and 5% in DT_{fall}. This small difference can be attributed to the fact that we are using average values for the delays, and that we ignored the delays of the logic gates (inverters and NOR gates) when we deduced the analytical design equations.

The efficiency of the implemented PA with the DMI-DTG, while driving a 100 mH & 342.5 Ω load at different frequencies, is shown in Fig. 17. The efficiency $(\eta = \frac{P_{load}}{P_{total}})$

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TABLE I
POWER AMPLIFIERS PERFORMANCE SUMMARY AND COMPARISON

Reference	JSSC 2012 [25]	ISSCC 2014 [26]	JSSC 2015 [27]	JSSC 2015 [7]	TPEL 2016 [9]	TCAS-I 2021 [10]	**This Work**
Topology	Class-D	Class-D	Buck	Class-D	Buck	Buck	**Class-D**
Process	CMOS 0.35 μm	SOI 0.14 μm	CMOS 0.5 μm	SOI 0.14 μm	CMOS 0.35 μm	CMOS 0.35 μm	**CMOS 0.35 μm**
Power Supply (V)	18	80	40	80	45	45	**24**
Frequency (MHz)	0.384	adaptive	0.5	adaptive	0.1	1	**0.5**
Load	8 Ω	22.5 μF + 1.6 Ω	NA	12 Ω	NA	100 Ω	**100 mH + 342.5 Ω**
DTG area (mm^2)	NA	NA	NA	NA	0.22	0.0126	**0.066**
Efficiency @ 0.1*P_{outmax}	>70%	80%	>65%	84%	>87%	NA	**65%**
Peak Efficiency (η)	88%	93%	94.9%	91%	95%	82%	**95.14%**
Shortest Dead Time (ns)	15	100	25	100	15	35	**10.8**
FOM* (ns/%)	0.17	1.07	0.26	1.1	0.157	0.42	**0.11**

$^*FOM = \frac{Dead\,Time\,(ns)}{Efficiency\,(\eta\%)}$, NA: Not Available, P_{outmax}: Maximum Output Power.

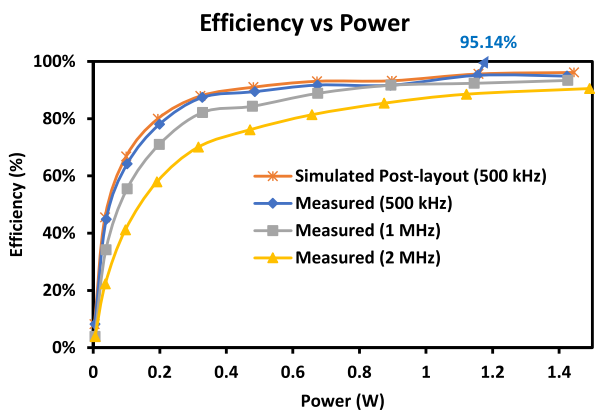

Fig. 17. Measured efficiency vs power of the PA at different frequencies.

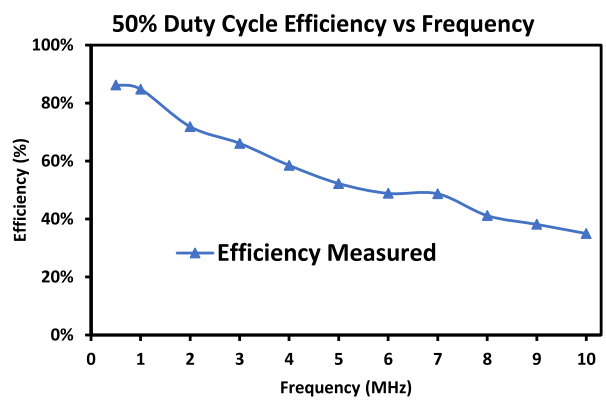

Fig. 18. Measured efficiency vs frequency of the PA at 50% duty cycle.

was measured by varying the duty-cycle of the input signal from 0.05 to 0.95 with a step of 0.1 and measuring the total supplied power and the power delivered to the load. $P_{total} = \sum_{i=1}^{n} I_{Supply_i} * V_{Supply_i}$, where I_{Supply_i} and V_{Supply_i} are the current and the supply voltage of the ith power supply, respectively, and n is the number of power supplies used. A peak efficiency of 95.14% is achieved at 500 kHz frequency, as shown from the efficiency curves in Fig. 17. As an example, the post-layout simulation of the efficiency at 500 kHz frequency is also shown in the same figure, the simulation varies slightly from the measurements due to the difference in the parasitic capacitance which affects the switching loss especially in low-power regions [6]. Additionally, the post-layout simulation shows that the DMI-DTG consumes 16.5 mW. To examine the impact of changing the switching frequency on the amplifier's efficiency, the efficiency curves, for the same duty-cycle range, at 1 MHz and 2 MHz are measured and added to the same figure. Also, the amplifier efficiency at 50% duty-cycle is measured at 11 different frequencies up to 10 MHz as shown in Fig. 18.

The degradation in the amplifier's power efficiency is mainly due to the gate capacitance switching loss and the ON-resistance conduction loss. According to [6], the efficiency curve can be divided into three main regions depending on the main source of power dissipation. The first region is the low-power region in which the switching loss is dominant. The second region is the high-power region in which the conduction loss is dominant, and the third region is the middle power region in which both sources of loss are comparable. This can be seen in Fig. 17, when the frequency increases, the switching loss is dominant in the low-power region and there is a large reduction in efficiency compared to the high-power region in which the difference is less visible. The efficiency of the PA at 50% duty cycle was measured at frequencies ranging from 500 kHz to 10 MHz as shown in Fig. 18. As we can see from the curve, the efficiency is decreasing as the frequency increases. This is because the switching power loss increases as the switching frequency increases, leading to a reduction in efficiency.

Table I presents the measured performance summary of the fabricated PA and comparable previous designs. The PA using the DMI-DTG can achieve high efficiency of 95.14% with a very short dead time of 10.8 ns, which is comparable to previous state-of-the-art PAs. In addition, a figure of merit (FOM) is used to allow a fair comparison with previous state-of-the-art. The adopted FOM shows the ability of the DTG to achieve the shortest possible dead time with high efficiency. A smaller FOM means that shorter dead time and higher efficiency are achieved. The shortest dead time achieved in previous comparable designs was 15 ns, and the highest achieved efficiency was 95%, while our design achieves a smaller dead time (10.8 ns) with 95.14% efficiency. In addition, compared to previous DTGs, our design

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has a small area with the smallest FOM. Moreover, our DMI-DTG can adapt to process variations, while providing the shortest dead time possible, thus, improving the efficiency and reliability of the whole system.

V. Conclusion

The design of high-voltage (HV) switched-mode power amplifiers (PAs) is centered around achieving high-efficiency, safe and reliable end solutions. Hence, very short dead times are required, while ensuring safe operation, in the amplifiers to improve their efficiency. This paper analyses, explores how to design and validates experimentally an HV delay mismatch insensitive dead time generator (DMI-DTG) that can adapt to process and temperature variations. This DTG is integrated within a switched-mode PA system and measured power efficiency of 95.14% is achieved at 500 kHz frequency with a generated dead time as small as 10.8 ns. The DMI-DTG circuit consists of inverters, NOR gates, and HV level-down shifters. The generator is implemented in a 0.35 μm HV CMOS process covering an area of 0.066 mm^2 which is less than 13.3% of the total area of the PA (0.5 mm^2). As a promising future work, the generated dead time can be further reduced by optimizing the gate drivers and the level-down shifters to make them faster, thus, reducing the body-diode conduction loss and improving the whole efficiency of the PA.

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