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A Reconfigurable Low-Voltage and Low-Power Millimeter-Wave Dual-Band Mixer in 65-nm CMOS

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ABSTRACT In this paper, we propose, investigate, and demonstrate a reconfigurable low-voltage and low-power millimeter-wave mixer in a 65-nm CMOS, which can be switched as either a subharmonic mixer (SHM) or a fundamental mixer (FM) for the dual-band applications. Based on a modified Gilbert mixer topology, the proposed CMOS mixer can operate at a low supply voltage and low local oscillator (LO) pumping power while providing good performance in both SHM and FM modes. To the best of our knowledge, this is the first reported Gilbert SHM based on the stacked switching quads in a low-voltage CMOS technology. Under 1-V supply voltage and −3-dBm LO pumping power, the measured conversion gain (CG) of the proposed CMOS mixer is -4.8 ± 1.5 dB from 34 to 56 GHz and -0.1 ± 1.5 dB from 17 to 43 GHz in the SHM and FM modes, respectively. The measured double-sideband (DSB) noise figure (NF) is 18.5–20 dB from 37 to 49 GHz and 12.4–14 dB from 17 to 35 GHz in the SHM and FM modes, respectively. The measured input third-order intercept point (IIP3) is 2.9 and 3.4 dBm, respectively, for the SHM and FM modes at the LO frequency of 22 GHz. In addition, the total dc power consumption of the proposed mixer including output buffers is 7 mW in both the operation modes.

INDEX TERMS CMOS, dual-band mixer, fundamental mixer (FM), Gilbert mixer, low-power, low-voltage, millimeter-wave (mmW), reconfigurable, subharmonic mixer (SHM).

I. INTRODUCTION

Research and development of multi-band and multi- standard wireless communication systems have gained significant interest in recent years [1]–[3]. Traditional design strategies have adopted separate single-band radio-frequency (RF) front-ends, which can physically be arranged in parallel for multi-band operations [1]. The drawback in this case is that the number of RF blocks involved in the system development is multiplied by the number of frequency bands of interest, hence the development cost, physical size and power consumption of the system are all increased. Alternative approach is to design a multi-band transceiver system that reuses common RF blocks as much as possible among the multiple frequency bands [2]. This approach is also appealing for millimeter-wave (mmW) transceivers on silicon to increase the versatility, save the chip area, and reduce the power consumption.

A multi-band mixer is one of the key components in a multi-band transceiver. A switched dual-band mixer was proposed in [4], where a switched inductor matching network was used to select the frequency band of interest. By using a dual-band *L-C* matching network, the mixer proposed in [5] can operate in two desired frequency bands simultaneously. The concept of composite right/left-handed transmission lines was also used to implement a dual-band mixer [6]. All these mixers, however, require multiple local oscillators (LOs) for multi-band operations. By selecting either the fundamental or 2nd order harmonic output of the oscillator as the LO through a set of complementary switches, a dual-band self-oscillating mixer was proposed in [7]. Similarly, band selection was achieved by either mixing the input signal with the fundamental or 3rd order harmonic component of the LO in [8]. A reconfigurable passive subharmonic mixer (SHM) with a multi-stage injection locked ring oscillator as LO was

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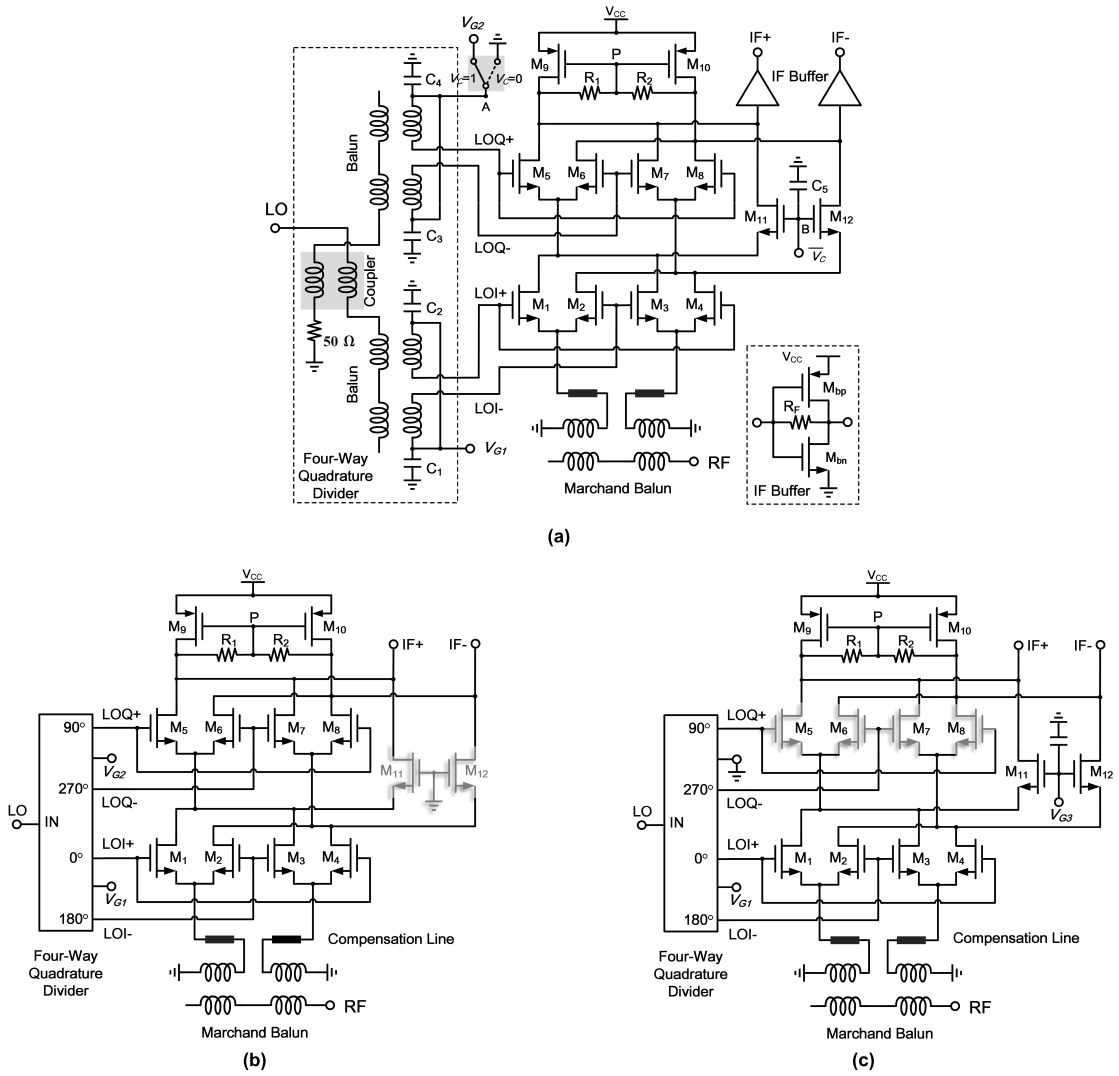

FIGURE 1. Schematic of the proposed reconfigurable dual-band CMOS mixer based on a modified Gilbert mixer topology. (a) Complete circuit. (b) Proposed mixer in SHM mode (without IF buffers). (c) Proposed mixer in FM mode (without IF buffers).

proposed in [9] for dual-band applications. The multi-stage injection locked ring oscillator was used to generate multiple LO phases. By selecting appropriate LO phases, the mixer can be reconfigured between the fundamental and subharmonic operation modes.

In this paper, a reconfigurable low-voltage and low-power mmW dual-band mixer in 65-nm CMOS is proposed, studied and demonstrated. The proposed CMOS mixer can be switched as either a SHM or a fundamental mixer (FM) for dual-band applications. By using a modified Gilbert mixer topology [10] and an active load [11], the proposed CMOS mixer can operate at 1 V supply voltage and −3 dBm LO pumping power while maintaining a good performance in both SHM and FM modes. The 1V supply voltage and −3 dBm LO power make it suitable for low-voltage and low-power applications. To the best of our knowledge, this is the first proposed Gilbert SHM based on stacked switching quads [12] in CMOS technology. The rest of this paper is organized as follows. The analysis and design of the proposed mixer in SHM and FM modes are presented in Section II (A) and (B), respectively. Section III provides the measured results and comparisons. Finally, Section IV summarizes this paper.

II. ANALYSIS AND DESIGN OF THE PROPOSED RECONFIGURABLE DUAL-BAND MIXER

As the feature size of the CMOS transistor continues to shrink, a proportional downscaling in the supply voltage is mandatory to maintain gate-oxide reliability. Therefore, low-voltage CMOS mixers are highly required, which have to force many compromises between conversion gain (CG), LO power, linearity, noise figure (NF), port-to-port isolation, power consumption, and supply voltage.

Fig. 1(a) shows the schematic of the proposed CMOS mixer based on a modified Gilbert mixer topology, where the tail current source and the RF transconductance stage in

a conversional Gilbert mixer are replaced by a Marchand-balun-based RF stage to reduce the supply voltage [10]. In addition, an active load that is composed of two PMOS transistors (M_9 and M_{10}) and two common-mode feedback resistors (R_1 and R_2) is employed to provide a high load impedance [11].

The core of the mixer is composed of two stacked switching quads (M_1-M_8) and a common-gate differential pair (M_{11}-M_{12}). The bottom switching quad is composed of transistors M_1-M_4, whose gates are biased near the threshold voltage $V_{\rm th}$. The top switching quad is composed of transistors M_5-M_8, whose gates are biased at $V_{\rm A}$. The common-gate differential pair is composed of transistors M_{11}-M_{12}, whose gates are biased at $V_{\rm B}$. As shown in Fig. 1(a), $V_{\rm A}$ and $V_{\rm B}$ represent the dc voltage at node A and node B, respectively, whose values can be selected by the control voltage $V_{\rm C}$ as

$$V_{\rm A} = \begin{cases} V_{\rm G2}, & if\ V_{\rm C} = 1 \\ 0, & if\ V_{\rm C} = 0 \end{cases} \tag{1}$$

and

$$V_{\rm B} = \overline{V_{\rm C}}. \tag{2}$$

where $V_{\rm G2}$ is the turn-on voltage of the top switching quad that is approximately equal to the sum of $V_{\rm th}$ and the drain voltage of the bottom switching quad $V_{\rm Db}$, while $\overline{V_C}$ is the complementary value of $V_{\rm C}$.

High impedance compensation lines are employed between the RF Marchand balun and the bottom switching quad, as shown in Fig. 1, to compensate the parasitic capacitances of the transistors M_1-M_4 [10]. A passive four-way quadrature divider, which is composed of a 90ř coupler and two Marchand baluns, is utilized to generate quadrature LO signals. The bottom and top switching quads are driven by the in-phase LO signal (LOI) and quadrature LO signal (LOQ), respectively. By adding four bypass capacitors (C_1-C_4) as shown in Fig. 1(a), the two LO Marchand baluns in the four-way quadrature divider could provide dc bias voltages ($V_{\rm G1}$ and $V_{\rm A}$) for the stacked switching quads without affecting the LO characteristics. Compared with a commonly used lumped poly-phase filter [12], [13], the passive four-way quadrature divider has a much lower insertion loss in the mmW range at the cost of a larger chip size. In addition, the transimpedance amplifier (TIA), which is composed of an NMOS transistor $M_{\rm bn}$, a PMOS transistor $M_{\rm bp}$ and a feedback resistor $R_{\rm F}$ (500 Ω), is utilized as an intermediate-frequency (IF) output buffer [11].

As will be discussed below, the proposed mixer can be reconfigured for operation between the subharmonic and fundamental modes simply by changing its bias, as shown in Fig. 1(b) and 1(c), where the IF buffers are removed for simplicity.

A. PROPOSED MIXER IN SUBHARMONIC MODE

A SHM allows for the use of an LO operating at a frequency that is only a fraction of the LO frequency of a FM [12]. This is very attractive in mmW frequency range, where an LO source with low phase noise and high output power is not always available [14]. The most widely used SHM topologies include the anti-parallel diode pair (APDP) based SHMs [15]–[17], the FET resistive SHMs [18]–[20], and the transconductance SHMs [14], [21]–[23]. Three distinct Gilbert SHMs [24], including the stacked-LO SHM [12], [25]–[27], the top-leveled-LO SHM [28]–[31] and the bottom-leveled-LO SHM [24], [32], have also been proposed. Among these structures, the Gilbert stacked-LO SHM achieves the highest CG and port-to-port isolation, while requiring the lowest LO pumping power [24]. However, this topology usually needs a high supply voltage, such as 3.3 V in [12] and [25] and 4 V in [26], due to the stacked structure. Thus, it is not suitable for low-voltage applications, especially in CMOS technologies. To date, all the published Gilbert stacked-LO SHMs are based on bipolar technologies. On the other hand, the top-leveled-LO SHM, the bottom-leveled-LO SHM, as well as the double balanced passive SHM [33], [34], can operate with a lower supply voltage in CMOS technologies. However, they usually require much higher LO pumping power with lower CG and worse port-to-port isolation.

To operate an active SHM at low supply voltage and low LO pumping power while providing a good CG and high port-to-port isolation, a modified Gilbert stacked-LO SHM is proposed for the first time, as shown in Fig. 1(b), where $V_{\rm A} = V_{\rm G2}$ and $V_{\rm B} = 0$ V. Which means that the transistors M_5-M_8 in the top switching quad are biased near the turn-on voltage, while the common-gate devices M_{11}-M_{12} are in off-state. During the positive excursions of LOQ, M_5 and M_8 are turned on, while M_6 and M_7 are turned off. On the contrary, during the negative excursions of LOQ, M_5 and M_8 are turned off, while M_6 and M_7 are turned on. In other words, the top switching quad is switched by LOQ. Meanwhile, the bottom switching quad is switched by LOI. The two stages of switching with 90ř phase offset provide an effective doubling of the LO frequency [12]. Therefore, a subharmonic mixing is obtained. According to the simulation, the CG of the SHM is robust to phase errors in the quadrature LO signals [34], which eases the design of the LO quadrature divider.

Compared with the conventional Gilbert stacked-LO SHM [12], [25]–[27], the balun coupling in the proposed SHM reduces two stacking stages and mitigates the voltage headroom problem. The operation of the proposed SHM is provided in the following. Assuming the LO waveform is a square wave with 50% duty cycle and the switching transistors are operating as ideal switches, the mixing function and the output voltage of the SHM can be expressed as follows [26], [34]:

$$m_h(t) = \frac{4}{\pi} \sum_{n=0}^{\infty} \frac{1}{2n+1} \sin[2(2n+1)\omega_{LO}t] \tag{3}$$

$$v_{out} = A_v v_{in}(t) m_h(t) \tag{4}$$

where $\omega_{\rm LO}$ is the angular frequency of the LO signal, $v_{\rm in}(t)$ is the input voltage of the mixer, and $A_{\rm v}$ is the nonmixing

(''amplifier-mode'') voltage gain, which is exhibited when the mixer core is configured as a simple ''cascode common-gate'' state by applying large dc bias voltages at the gates of the stacked switching quads [35]. Herein, A_v can be expressed as

$$A_v = g_m R_L \tag{5}$$

where g_m is the transconductance of the transistors M_1-M_4, and R_L is the load impedance of the mixer.

Assuming

$$v_{in}(t) = v_{RF}(t) = V_{RF}\cos(\omega_{RF}t) \tag{6}$$

where V_{RF} and ω_{RF} represent the voltage amplitude and the angular frequency of the RF input signal, respectively.

Substituting (3) and (6) into (4), we can obtain

$$\begin{aligned} v_{out}(t) &= A_v V_{RF}\cos(\omega_{RF}t)\frac{4}{\pi}\sum_{n=0}^{\infty}\frac{1}{2n+1}\sin[2(2n+1)\omega_{LO}t] \\ &= \frac{2}{\pi}A_v V_{RF}\sum_{n=0}^{\infty}\frac{1}{2n+1}\sin[\omega_{RF}t - 2(2n+1)\omega_{LO}t] \\ &\quad + \frac{2}{\pi}A_v V_{RF}\sum_{n=0}^{\infty}\frac{1}{2n+1}\sin[\omega_{RF}t + 2(2n+1)\omega_{LO}t]. \end{aligned} \tag{7}$$

As can be observed, a number of different frequency components ($\omega_{RF} \pm (4n+2)\omega_{LO}$) are obtained, but only the first term in (7) with n = 0 is the desired IF product with a frequency of $\omega_{RF} - 2\omega_{LO}$, whose amplitude can be expressed as

$$v_{IF}(t) = \frac{2}{\pi}A_v V_{RF}\sin[(\omega_{RF} - 2\omega_{LO})t]. \tag{8}$$

Therefore, the voltage conversion gain (VCG) and the power CG of the SHM can respectively be derived as

$$VCG_h = \frac{V_{IF}}{V_{RF}} = \frac{2}{\pi}A_v = \frac{2}{\pi}g_m R_L \tag{9}$$

and

$$CG_h = \frac{P_{IF}}{P_{RF}} = (VCG_h)^2\frac{R_S}{R_L} = \frac{4}{\pi^2}g_m^2 R_L R_S \tag{10}$$

where V_{IF} and P_{IF} represent the voltage amplitude and power of the IF signal, respectively, P_{RF} is the input power of the RF signal, and R_S is the source impedance.

It should be noted that, for a passive SHM [34], $A_v = 1$, and the VCG is

$$VCG_{ph} = \frac{2}{\pi}. \tag{11}$$

Therefore, the CG of the proposed SHM is higher than that of the passive SHM as long as $g_m R_L > 1$.

To obtain a high CG, a large R_L and a high g_m are required. However, a larger R_L will cause a larger dc voltage drop on the IF load and therefore aggravates the voltage headroom problem. The active load, however, can provide a very high impedance in the differential-mode for high CG but a moderate impedance in the common-mode for low dc voltage drop. By using the active load, a high CG can be obtained with a smaller dc voltage drop.

A higher g_m can also result in a higher CG. Normally, larger devices have a higher g_m. However, the larger the transistor size is, the larger the parasitic capacitances (e.g. the drain-bulk capacitance C_{DB}, and the source-bulk capacitance C_{SB}) will be, which will provide high capacitive coupling paths to the lossy substrate, especially at mmW frequency range [34]. In addition, larger devices require higher LO pumping power and higher dc power [11]. Therefore, trade-offs between CG, dc power, and LO pumping power have to be concerned during device size selection. In this design, a total gate width of 20 μm with a ten-finger transistor is selected to obtain sufficient CG with low LO power and low dc power.

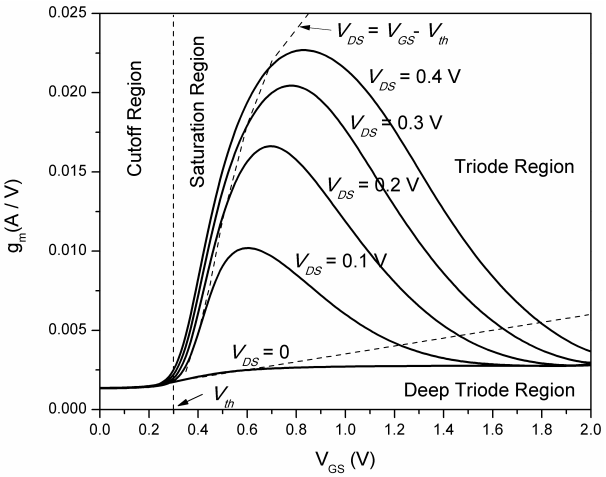

FIGURE 2. Simulated transconductance g_m of the NMOS transistor with gate width of 20 μm versus V_{GS} and V_{DS}.

Fig. 2 shows the simulated g_m of the selected NMOS transistor versus its gate-source voltage V_{GS} and drain-source voltage V_{DS}. For a given V_{GS}, g_m decreases as V_{DS} decreases. This explains why high supply voltage is normally required in the Gilbert mixer design [11], [24], [25]. It is interesting to note that, for a given V_{DS}, g_m is a convex upward function versus V_{GS}. Since V_{GS} is determined by the voltage amplitude of the LO signal (V_{LO}) in this design, the CG of the SHM will also be a convex upward function versus V_{LO}. Furthermore, if V_{LO} is large enough, the transistors will be pushed into the deep triode region, as shown in Fig. 2, and the operation of the proposed SHM will be similar to the passive SHM proposed in [34].

Fig. 3 simulates the normalized CGs of the proposed SHM, a passive SHM with optimized V_{GS} biasing [34] and a passive SHM without V_{GS} biasing, versus LO power. As can be observed, the passive SHM without V_{GS} biasing requires the highest LO power (e.g. 12 dBm) for a reasonable CG. By adding an optimized V_{GS} biasing, the CG of the passive SHM can be improved at low LO power region. The proposed SHM can further improve the CG with a lower LO power.

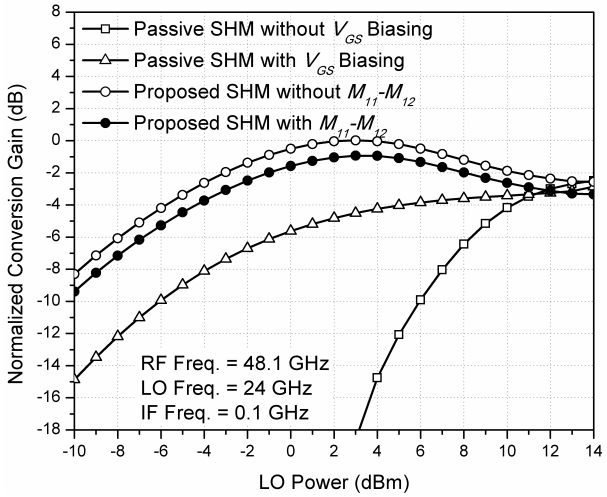

FIGURE 3. Simulated CGs of different SHMs versus LO power. The peak CG is normalized to 0 dB.

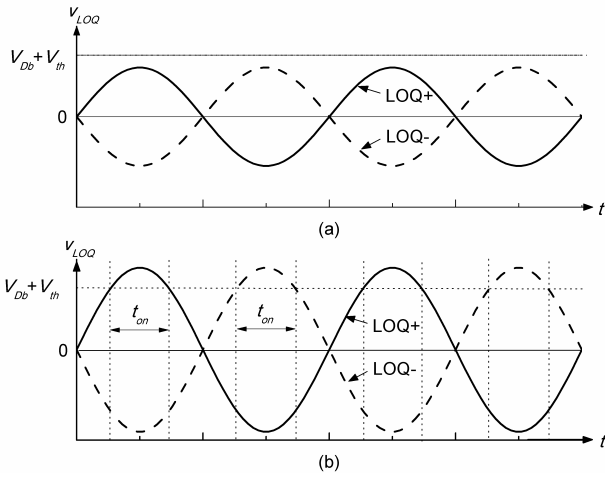

FIGURE 4. Voltages on the gates of M_5-M_8 in the FM mode. (a) $V_{LOQ} < V_{Db} + V_{th}$. (b) $V_{LOQ} > V_{Db} + V_{th}$.

For example, to achieve a −4 dB of normalized CG, the passive SHM with optimized V_{GS} biasing requires 4 dBm of LO pumping power while the proposed SHM only requires −6 dBm of LO power at the expense of 2 mW of dc power consumption. This is very attractive in the mmW frequency range, where the LO power is a valuable resource.

It should be mentioned that, the off-state transistors M_{11}-M_{12} and the IF buffers are removed in the above simulation for fair comparison. The off-state transistors M_{11}-M_{12}, however, may degrade the performance of the proposed SHM due to the parasitic loading. By adding the off-state transistors M_{11}-M_{12}, the simulated CG of the proposed SHM degrades about 1 dB, as shown in Fig. 3. Additionally, the simulated NF also degrades about 1 dB. Fortunately, the RF bandwidth and the input third order intercept point (IIP3) are hardly affected according to the simulation.

B. PROPOSED MIXER IN FUNDAMENTAL MODE

The proposed CMOS mixer can also be reconfigured as a FM by setting $V_C = 0$ V. Therefore, $V_B = 1$ V and $V_A = 0$ V, which means that the gates of the transistors M_5-M_8 in the top switching quad are biased at 0 V, while the common-gate devices M_{11}-M_{12} are activated, as shown in Fig. 1(c). If the voltage amplitude of LOQ (V_{LOQ}) is smaller than $V_{Db} + V_{th}$, as shown in Fig. 4(a), the transistors M_5-M_8 will be in off-state during both the positive and negative excursions of LOQ. In this case, the power of LOQ is wasted. Since only the bottom switching quad is switched by LOI, a mixing only happens in the bottom switching quad.

The operation of the proposed FM is provided in the following. Assuming the LO waveform is a square wave with 50% duty cycle and ideal switching, the mixing function of the FM can be expressed as

$$m_f(t) = \frac{4}{\pi}\sum_{n=0}^{\infty}\frac{1}{2n+1}\sin[(2n+1)\omega_{LO}t]. \tag{12}$$

Similarly, the output IF voltage and the CG of the FM can respectively be obtained as

$$v_{IF}(t) = \frac{2}{\pi}A_v V_{RF}\sin[(\omega_{RF} - \omega_{LO})t] \tag{13}$$

and

$$CG_f = \frac{P_{IF}}{P_{RF}} = \frac{4}{\pi^2}g_m^2 R_L R_S. \tag{14}$$

Comparing (10) and (14), it is noteworthy that the CG of the SHM is the same as that of the FM under ideal conditions. In practice, however, the CG of the SHM will be lower than that of the FM, due to a non-ideal square-wave switching and a higher parasitic capacitive coupling to the substrate at high frequencies [34].

Fig. 5 simulates the normalized CGs of the proposed FM, a passive ring mixer with an optimized V_{GS} biasing and a passive ring mixer without V_{GS} biasing, versus LO power.

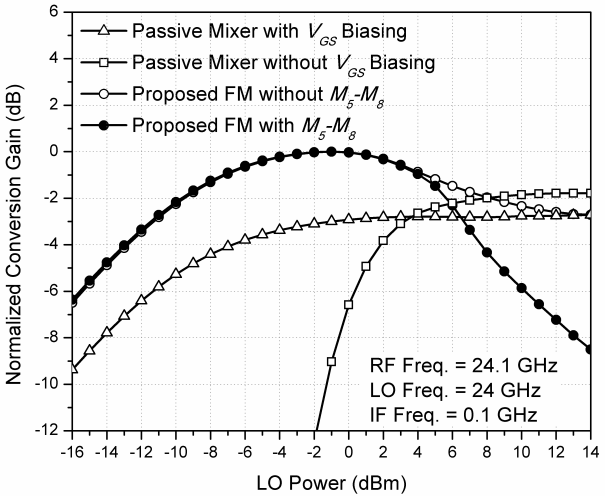

FIGURE 5. Simulated CGs of different FMs versus LO power. The peak CG is normalized to 0 dB.

Although half of the LO power is wasted by LOQ, the simulated CG of the proposed FM is still higher than that of the passive ring mixer with an optimized V_{GS} biasing at low LO power region. The simulated CG of the proposed FM equals to that of the passive ring mixer when the LO power is higher than 13 dBm, because the transistors in the proposed FM have been pushed into the deep triode region.

Similarly, the off-state transistors M_5-M_8 and the IF buffers are removed in the above simulation for fair comparison. The simulated CG of the proposed FM with M_5-M_8 is also plotted in Fig. 5, which is equal to that of the FM without M_5-M_8 when the LO power is lower than 4 dBm. However, when the LO power is higher than 4 dBm, the simulated CG of the FM with M_5-M_8 drops much faster than that of the FM without M_5-M_8. This is because the transistors M_5-M_8 will be activated during the time t_{on}, as shown in Fig. 4(b), when V_{LOQ} is larger than $V_{Db} + V_{th}$. Thus, a part of IF currents at the drain of the bottom switching quad will be routed through the top switching quad and upconverted to other frequencies. Therefore, we should make sure $P_{LO} < 4$ dBm during the operation of the fundamental mixing mode.

According to the simulation, the performances of the proposed FM, including the CG, NF, RF bandwidth and IIP3, are hardly affected by the off-state transistors M_5-M_8 when $P_{LO} < 4$ dBm. This is because the off-state transistors M_5-M_8 are connected to the IF stage, where the parasitic loading effects can be ignored.

III. MEASURED RESULTS

The proposed reconfigurable low-voltage and low-power mmW dual-band mixer is designed and fabricated in TSMC 65-nm CMOS technology. A die micrograph is shown in Fig. 6. The chip is measured via on-wafer probing. During the measurements, RF and LO signals of the mixer are provided by a vector network analyzer (Agilent N5245A) and a signal generator (Agilent E8257D), respectively, and the output spectrum is observed by a spectrum analyzer (Agilent N9030A). The complete circuit including the TIA buffers, draws 7 mA of dc current from a 1 V supply in both SHM and FM modes.

Fig. 7 shows the simulated and measured CG of the mixer in both SHM and FM modes versus the LO power. In the measurement, the LO frequency is 24 GHz and the IF frequency is 0.1 GHz. The corresponding RF frequencies are 48.1 GHz and 24.1 GHz for the SHM and FM modes, respectively. As shown in Fig. 7, the mixer in the SHM mode achieves a maximum CG of −3.3 dB at the LO power of 2 dBm, while the mixer in the FM mode achieves a maximum CG of 1.4 dB at the LO power of −3 dBm. When the LO power further increases, the measured CG of the mixer in both modes drops faster than that in Fig. 3 and Fig. 5. This is because a higher LO power reduces the dc voltage at the input port of the TIA, which drives the TIA into a low-gain operation [11]. This effect was not considered in the simulations in Section II, because the TIA buffers are removed in Fig.1(b) and (c) for fair comparison with the passive mixers. In the following measurements, an LO power of −3 dBm is used for low LO drive.

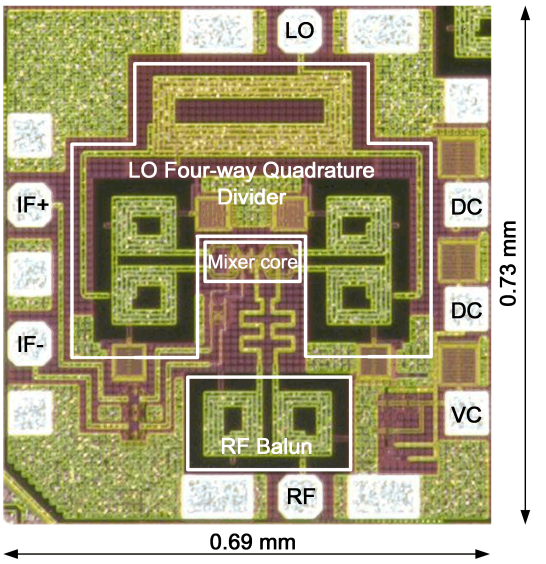

FIGURE 6. Micrograph of the proposed reconfigurable dual-band CMOS mixer.

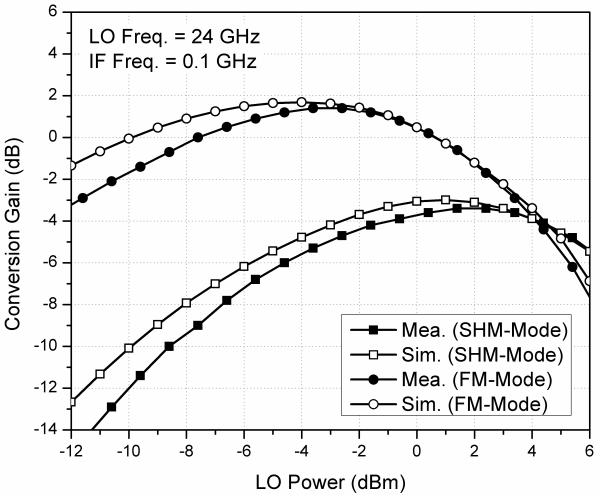

FIGURE 7. Simulated and measured CG versus the LO power for both SHM and FM modes.

Fig. 8 shows the measured CG versus the IF frequency from 10 MHz to 2.5 GHz with an LO frequency of 24 GHz for both SHM and FM modes. The proposed mixer demonstrates a 3-dB IF bandwidth of 1.7 GHz for both modes.

Fig. 9 shows the simulated and measured CG of the mixer in both modes versus the RF frequency with a fixed IF frequency of 0.1 GHz. The measured CG of the mixer is -4.8 ± 1.5 dB from 34 to 56 GHz and -0.1 ± 1.5 dB from 17 to 43 GHz for the SHM and FM modes, respectively. The measured RF return loss of the mixer is better than 10 dB from 20 to 60 GHz, which agrees well with the simulated result.

The measured LO-to-RF isolation of the mixer for both modes is better than 43 dB and the measured 2LO-to-RF isolation of the mixer in the SHM mode is better than 47 dB, as shown in Fig. 10. In the measurement of the 2LO-to-RF

TABLE 1. Comparisons of subharmonic mixers in various topologies and technologies.

Ref.	RF Freq (GHz)	CG (dB)	DSB NF (dB)	LO Power (dBm)	V_{CC} (V) & dc Power (mW)	LO-to-RF Isolation (dB)	2LO-to-RF Isolation (dB)	IIP3 (dBm)	Chip Area (mm^2)	SHM Topology	Tech.
[17]	10-40	-16.6 ± 1	n/a	8	0 & 0	> 12	> 51	n/a	0.74	APDP	0.18-μm CMOS
[20]	28-50	-10.3 ± 0.7	n/a	7	0 & 0	> 37	> 33	16	0.61	FET resistive	0.13-μm CMOS
[14]	9-31	-9 ± 1	n/a	9.7	0 & 0	> 18	> 28	3	0.9	Transconductance Source-pumped	90-nm CMOS
[22]	21-40	-11.2 ± 3	n/a	10.5	1.3 & 74.6	> 50	> 47	n/a	0.97	Transconductance Gate-pumped	0.18-μm CMOS
[12]	1-2	18.2 ± 1	7	10	3.3 & 9.2	> 30	> 67	-7.5	n/a	Gilbert Stacked-LO	Si/SiGe HBT
[24]	5.2	14.5	24	-8	3.3 & 13.2	> 50	> 75	-5	1.5	Gilbert Stacked-LO	2-μm GaInP/GaAs HBT
[24]	10	0	24	12	3.3 & 2.6	> 23	> 32	5	1	Gilbert Bottom-LO	2-μm GaInP/GaAs HBT
[24]	10	13	22	12	3.3 & 6.6	> 32	> 59	-7.5	1	Gilbert Top-LO	2-μm GaInP/GaAs HBT
[29]	35-65	-7.5 ± 1.5	14.5	5	3.3 & 45.4	> 45	> 50	6	1*	Gilbert Top-LO	90-nm CMOS
[30]	30-100	-1.5 ± 1.5	n/a	10	n/a & 58	> 47	> 47	n/a	0.35	Gilbert Top-LO	90-nm CMOS
This work	**34-56**	**-4.8 ± 1.5**	**18.5**	**-3**	**1 & 7**	**> 43**	**> 47**	**2.9**	**0.5**	**Modified Gilbert Stacked-LO**	**65-nm CMOS**

*Demodulator area

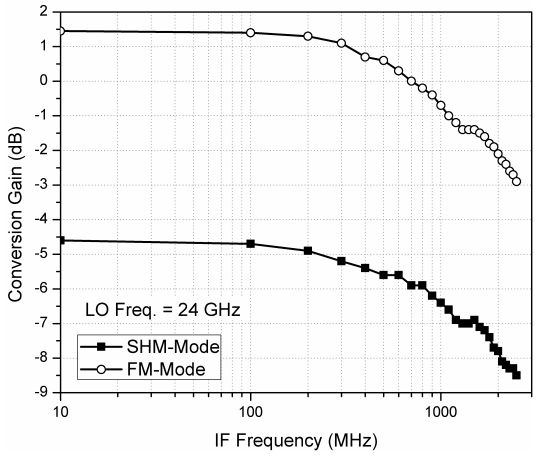

FIGURE 8. Measured CG versus the IF frequency for both SHM and FM modes.

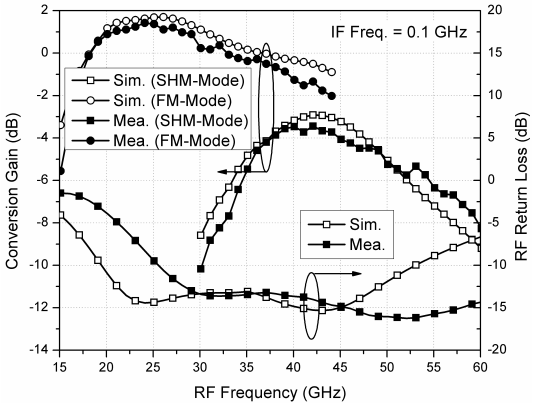

FIGURE 9. Simulated and measured CG and RF port return loss versus the RF frequency for both SHM and FM modes.

isolation, the LO frequency is only swept from 15 to 25 GHz, therefore the output 2×LO frequency range is only from 30 to 50 GHz, which is limited by the maximum frequency of the spectrum analyzer (Agilent N9030A).

For double-sideband (DSB) NF measurements, the RF source is replaced by a noise source (Keysight 346CK01). Fig. 11 shows the measured DSB NF of the proposed mixer for both modes after calibration. The lowest DSB NF is 18.5 and 12.4 dB for the SHM and FM modes, respectively.

For large signal measurements, the RF source is replaced by a vector signal generator (Agilent E8267D), which can provide a higher output power and two-tone signals up to 44 GHz. Fig. 12 shows the measured CG versus the RF input power, where the LO frequency is 22 GHz and the IF frequency is 0.1 GHz. The input 1 dB power compression point (IP_{1dB}) of the mixer is −7.6 dBm and −6.1 dBm for

TABLE 2. Comparisons of fundamental mixers in various topologies and technologies.

Ref.	RF Freq (GHz)	CG (dB)	DSB NF (dB)	LO Power (dBm)	V_{CC} (V) & dc Power (mW)	LO-to-RF Isolation (dB)	IP_{1dB} (dBm)	IIP3 (dBm)	Chip Area (mm^2)	FM Topology	Tech.
[36]	20-75	3 ± 2	n/a	6	3 & 93	> 30	2.1	11	0.3	Conventional Gilbert	90-nm CMOS
[37]	40-50	10 ± 2	n/a	15	0 & 0	> 49	4.5	15.5	0.83	Resistive Ring	45-nm SOI
[38]	30-90	-7.7 ± 1.5	n/a	2.5	1 & 0.6	> 30.2	3	n/a	0.39	Drain/Gate Pumped	90-nm CMOS
[39]	53-70	5.9 ± 1.5	13	-6	1.2 & 3	> 37	-16.6	-4	0.3	Source Pumped	90-nm CMOS
[10]	31-96	-3 ± 1.5	n/a	0	1.2 & 7.2	> 48	-4.7	n/a	0.5**	Modified Gilbert	0.13-μm CMOS
[11]	20-50	0 ± 2	13	0	1.2 & 6	> 46	-1	9.5	0.49	Modified Gilbert	90-nm CMOS
This work	**17-43**	**-0.1 ± 1.5**	**12.4**	**< -6***	**1 & 7**	**> 43**	**-7.6**	**3.4**	**0.5**	**Modified Gilbert**	**65-nm CMOS**

*The input LO power is -3 dBm, but half of the LO power (i.e. the power of LOQ) is wasted on the off-state transistors M_5-M_8. **Demodulator area.

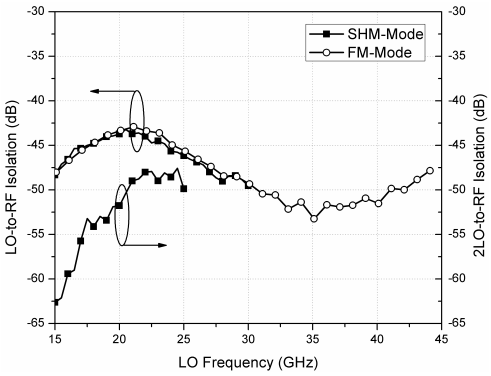

FIGURE 10. Measured isolations for both SHM and FM modes.

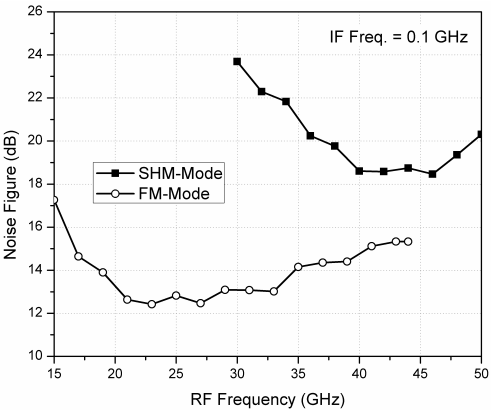

FIGURE 11. Measured DSB NF for both SHM and FM modes.

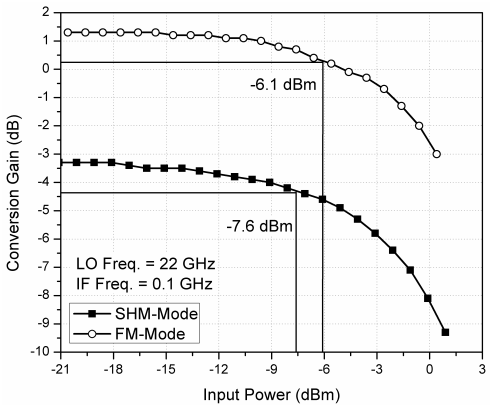

FIGURE 12. Measured CG versus the RF input power for both SHM and FM modes.

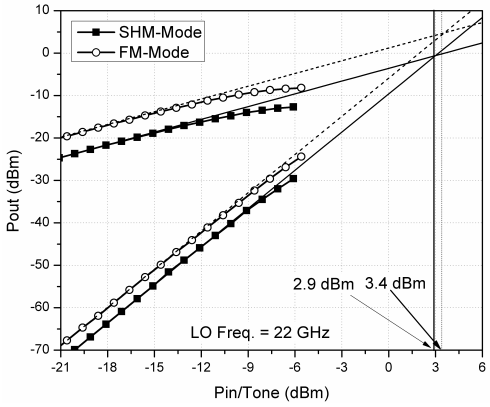

FIGURE 13. Measured IIP3 for both SHM and FM modes.

the SHM and FM modes, respectively. The measured IIP3 of the proposed mixer in the SHM mode is 2.9 dBm for RF two-tone of 43.895 GHz and 43.905 GHz, and the measured IIP3 of the mixer in the FM mode is 3.4 dBm for RF two-tone of 22.095 GHz and 22.105 GHz, as shown in Fig. 13.

Table 1 compares the proposed mixer in SHM mode with some other previously published SHMs in various topologies and technologies. The proposed CMOS mixer in the SHM mode achieves good CG, NF and linearity performance under low supply voltage, low dc power and low LO pumping power, at the expense of larger chip area due to the passive baluns and the quadrature coupler.

Table 2 compares the proposed mixer in FM mode with some other previously published FMs in various topologies and technologies [36]–[39]. The proposed CMOS mixer in the FM mode shows comparable performance with other modified Gilbert mixers, even though half of the LO power is wasted.

IV. CONCLUSION

In this paper, a reconfigurable low-voltage and low-power mmW dual-band CMOS mixer is proposed, studied and demonstrated. By changing its bias, the mixer can be reconfigured for operation between subharmonic and fundamental modes for dual-band applications. Based on a modified Gilbert mixer topology, the proposed CMOS mixer can operate at 1 V supply voltage and -3 dBm LO power while providing CG of -4.8 ± 1.5 dB from 34 to 56 GHz in the SHM mode and CG of -0.1 ± 1.5 dB from 17 to 43 in the FM mode. The measured IIP3 of the CMOS mixer is 2.9 dBm and 3.4 dBm for the SHM and FM modes, respectively, at LO frequency of 22 GHz. The total dc power consumption of the mixer is 7 mW for both states, including the output IF buffers. This circuit could be attractive in a mmW dual-band portable system where low-voltage and low-power are required.

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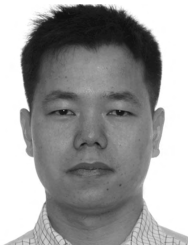

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