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A 9.2-ns to 1-μs Digitally Controlled Multituned Deadtime Optimization for Efficient GaN HEMT Power Converters

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***Abstract*— This paper presents a tunable new deadtime control circuit providing an optimal delay for power converter optimization. Our method can reduce the deadtime loss while improving the efficiency and power density of a given power converter. The circuit presents a reconfigurable delay element to generate a wide range of deadtime for different power conversion applications with varying loads and input voltages. The optimal deadtime equation for buck converters is derived, and its dependency on the input voltage and load is discussed. Experimental results show that the presented circuit can provide a wide range of deadtime delays, ranging from 9.2 ns to 1000 ns. The power consumption of the presented circuit is measured for different capacitive loads (C_L) and operating frequencies (f_s). The circuit consumed a power between 610 μW and 850 μW across the measured deadtime ranges while $C_L = 12$ pF, $V_{dd} = 3.3$ V, and $f_s = 200$ kHz. The proposed deadtime generator can operate up to 18 MHz when the minimum deadtime of 9.2 ns is selected. The presented circuit occupies an area of 150μ m × 260μm. The fabricated chip is connected to a buck converter to validate the operation of the proposed circuit. The efficiency of a typical buck converter with minimum T_{DLH} and optimal T_{DHL} at I_{Load} = 25 mA is improved by 12% compared to a converter with a fixed deadtime of $T_{DLH} = T_{DHL} = 12$ ns.**

***Index Terms*— Power converters, gate driver, GaN HEMT transistors, optimized deadtime control, efficiency, adjustable circuit, power consumption, load variation, different input voltage.**

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I. Introduction

EFFICIENT power converters are essential circuits used in System-in-Packages (SiP) modules for distributing power to the different building blocks [1]. Many high-performance applications, such as video processing [2], are particularly power-hungry. Power converters are ubiquitous in industrial and consumer electronics. They are employed in so many applications, from smartphones, tablets, and headphones [3], [4], to TV sets, car electronics, wireless power chargers for electric vehicle [5], [6], public fitness equipment [7], and wearable medical devices [8]. Power converters, such as DC–DC converters, bridges (half and full), and class-D power amplifiers, must present high efficiency and power density [9]–[12]. A thorough analysis of losses must be performed, so a power converter design can meet these key criteria [13]–[15]. Losses must be examined at the component and peripheral circuits levels to improve converter performance. Si MOS, SiC MOS, and GaN transistors are the most frequently used power switches in power converters [16]–[20]. A Figure of Merit (FoM) = $Q_{OSS}R_{ON}$ is recommended in [21] to the advantage of GaN's over Si or SiC (Q_{OSS} and R_{ON} are the output capacitor charge and the on-resistance of the power switch, respectively). Furthermore, the GaN transistor does not suffer from reverse recovery loss due to the absence of a body diode, has a lower gate charge, and a smaller output capacitance than with Si or SiC [22], [23]. The carrier mobility in the 2D electron gas (2DEG) channel is considerably faster in the GaN transistor, and the breakdown voltage is higher due to its large acute electric field [24], [25]. Hence, GaN transistors are excellent candidates for ultra-high-power density operation. Fig. 1 shows the different types of losses found in power converters. Fig. 1(a) depicts a simplified schematic of a conventional power converter. Fig. 1(b) illustrates the power converter's essential waveforms needed for the case of GaN transistors. In contrast, Fig. 1(c) shows the needed power converter's waveforms when the power switches are implemented with Si MOSFETs.

The rise and fall times (t_r and t_f) of the main curve of the power converter (V_{SW}) are shorter when GaN transistors are used, as shown in Figs. 1(b) and 1(c). In the same condition, the switching time of the GaN transistors is six times faster than for Si MOSFET [24]. Accordingly, the switching losses (P_{SW}) of the GaN transistors are minimized because the overlap of I_{DS} and V_{DS} of the high-side power switch (HSS)

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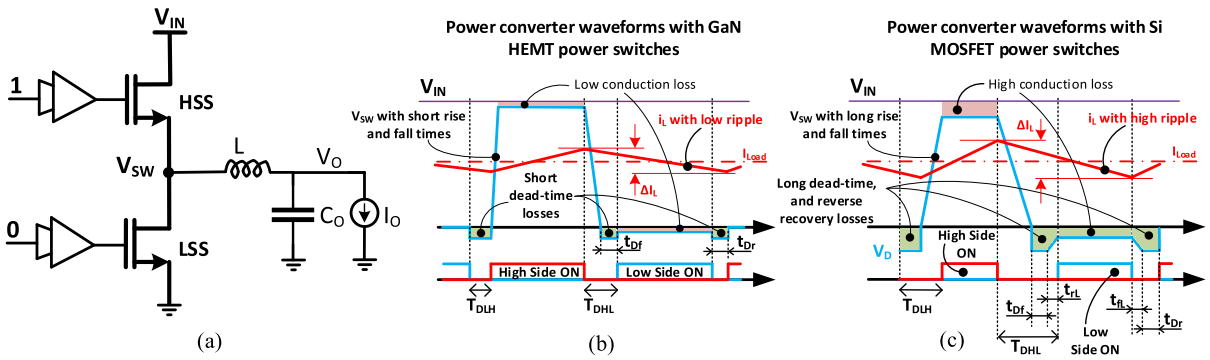

Fig. 1. Conventional power converter. (a) Simplified schematic, (b) waveforms with GaN HEMT power switches, and (c) waveforms with Si MOSFET power switches.

is minimized when the t_r and t_f of V_{SW} are shorter [24]. Figs. 1(b) and 1(c) show that the power converter using GaN transistors has a significantly lower conduction loss (P_{CON}). The P_{CON} equals the value of R_{ON} times the value of the RMS current of the power switches (see the Appendix for more details). GaN transistors achieve lower conduction loss because their R_{ON} is smaller than that of Si MOSFETs. Another type of loss in power converters is due to the reverse recovery charge (Q_{RR}) in the freewheeling of the low-side switch (LSS). This loss equals the multiplication of Q_{RR}, V_{IN}, and the operating frequency (f_S) of the converter (see the Appendix). Moreover, this loss can be significant in power converters with Si MOSFETs. However, the loss is almost zero in GaN-based converters because the GaN is a majority carrier device, and it does not have reverse recovery-based loss. This point is clarified in Figs. 1(b) and 1(c) for Si and GaN-based converters, respectively. Another factor that contributes to the switching loss is the stored energy in the output capacitance of the power switch, which is dissipated during the turn-on time. This loss (P_{CAP}) depends on the output charge of the power switch (Q_{OSS}) and equals the multiplication of Q_{OSS}, f_S, and V_{IN} (see the Appendix). GaN devices also have small output capacitances compared with Si MOSFETs. Accordingly, they exhibit a much smaller P_{CAP}. The LSS body diode in power converters can conduct during the deadtime, resulting in a power loss associated with the forward voltage of the diode. Although GaN devices have no body diode, their symmetry helps in conducting in the third quadrant with a diode-like behavior. The lateral GaN structure is comprised of a source and drain that are linked by a 2DEG channel, with the Gate controlling the conductivity of the 2DEG. Figs. 2(a) and 2(b) illustrate the cross-sectional view of the lateral structure of a GaN transistor and its behavior in the first and third quadrants, respectively. When the current flows in reverse conduction in GaN devices, the drain and source terminals can swap the termination. GaN transistors have a high third quadrant conduction (e.g., V_{SD} of 2 V at 10 A for LMG5200 compared to ~1 V for Si MOSFETs). Hence, GaN devices typically exhibit a higher power loss during deadtime (P_{DT}). This power loss can be calculated as follows:

$$P_{DT} = f_S \times V_{SD} \times I_{OUT} \times (T_{DLH} + T_{DHL}), \qquad (1)$$

where I_{OUT} is the output current of the power converter; and T_{DLH} and T_{DHL} are the required deadtimes, as shown

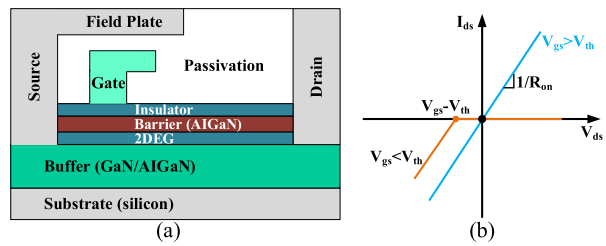

Fig. 2. GaN transistor: (a) Cross section of the lateral structure, (b) simplified behavior in 1st and 3rd quadrant.

in Figs. 1(b) and 1(c). Accordingly, an adjustable deadtime control circuit is necessary to select the optimal deadtime for different power converter applications to achieve maximum efficiency. When the optimum deadtime is tuned, the signal of V_{SW} (Fig. 1 (a)) has sufficient time to reach zero, but does not cross it. Then, the buck converter can work at its maximum operating frequency and maximum efficiency. The other power converter losses to consider include those resulting from the gate driver (P_G), output inductor DC resistance (P_{DCR}), equivalent series resistance of the output capacitance (P_{ESR}), and power switch packaging losses (see Appendix) [26]–[30].

The gate driver supply voltage (V_{DC}) is usually separated from the power switches supply (V_{IN}) in power converter implementation where two n-channel bootstrapped power switches are used as HSS and LSS (Fig. 3(a)). The V_{DC} is fixed to +5 V, while the V_{IN} is between 12 V and 200 V depending on the application. Accordingly, the same gate driver design would support different power converter applications. The amount of deadtime delay required to activate the HSS and LSS switches, which depends on the value of V_{IN}, must be set to longer values because the operation of power switches is known to be slower at higher V_{IN}. A gate driver with a reconfigurable deadtime control circuit allows to finetune and find the optimal the required deadtime for various V_{IN}. This mechanism ensures a power converter design with a sound efficiency performance for a wide range of applications with different V_{IN} values [31], [32].

The needed power converter deadtime depends on the type of load (RLC, RL, and LC) and the values of the used off-chip passive components. The primary distinction among most converter types (DC–DC, Class-D power amplifiers, and bridges, including half and full) is the kind of load. Accordingly, adopting a single implementation of a gate driver

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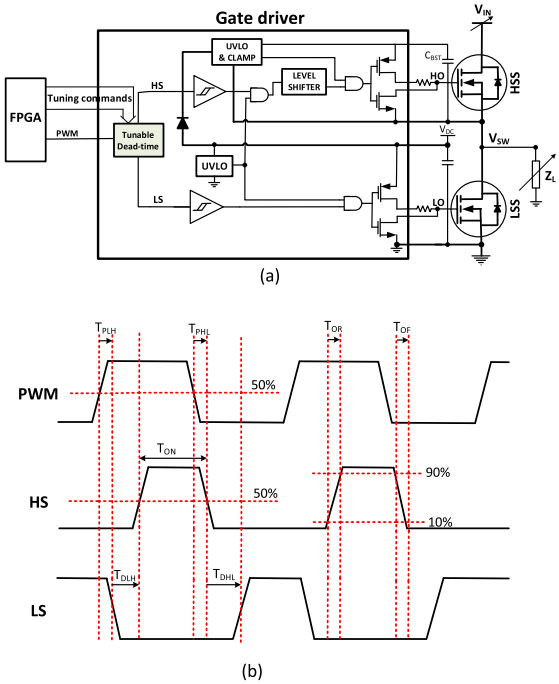

Fig. 3. (a) A power converter with a tunable dead-time generator, and (b) timing diagram of gate driver in PWM mode under no load condition.

with a tunable deadtime delay for the various power converter topologies has several benefits. Fig. 3(a) shows a power converter with variable input voltage (V_{IN}), variable load (Z_L), and reconfigurable deadtime control fulfilled with a gate driver [33]–[38]. In this configuration, a field-programmable gate array (FPGA) sends the tuning commands to the deadtime control circuit. Fig. 3(b) shows the timing diagram of the gate driver with a PWM signal under no load condition where the switching specifications are illustrated, including the turn-off delay (T_{PHL}), turn-on delay (T_{PLH}), output rise time (T_{OR}), output fall time (T_{OF}), low-to-high transition deadtime (T_{DLH}), and high-to-low transition deadtime (T_{DHL}).

The deadtime control circuit is a key circuit in gate drivers that enables high-quality switching to drive the HSS and LSS power switches [39], [40]. Fig. 3(a) presents a general building block of a power converter that includes a gate driver associated with an integrated deadtime control circuit [41]. Although the gate driver implementation frequently has a fixed deadtime, a reconfigurable gate driver with the ability to adjust the deadtime delay is desirable to provide an optimal deadtime to reduce P_{DT}, thereby increasing the efficiency and power density [42]–[45].

Several tunable deadtime control circuits were discussed in the literature. The use of a gate driver with adjustable deadtime delay used for tuning a half-bridge with a high supply voltage ($V_{IN} = +86$ V) is discussed in [36]. This gate driver configuration generates a variable deadtime delay between 4.5 ns and 58 ns for a variable load with a current ranging from 200 mA to 2 A. However, this deadtime circuit does not generate enough delays (i.e. longer delays are required) to support power converters with high V_{IN} and wider load range. A commercial gate driver integrated circuit with tunable deadtime delay is presented in [37]. It drives a half-bridge that can operate up to $V_{IN} = 200$ V and supply up to 3 A to a load. However, the deadtime control involved in this gate driver uses two off-chip resistors to allow a tunable operation. This situation increases the power dissipation of the gate driver. Moreover, the reliability of the gate driver circuit can be affected, and the resolution of the deadtime delay can be degraded.

A deadtime optimization method for GaN-based buck converters is described in [42]. In this paper, the optimization relies on mathematical analysis and the derived equations for both T_{DLH} and T_{DHL}. In [42], an efficiency improvement of up to 4.5% is achieved compared to using a fixed deadtime, but one drawback with the derived equations is a lack of accuracy. A digital deadtime correction wherein the deadtime can be tuned during a power converter operation is reported in [46]. In this technique, the deadtime circuit measures the voltages of V_{SW} and LSS gate and tunes the deadtime. An adaptive deadtime control methodology wherein a digital circuit was used to optimize the required deadtime through measuring the voltage of V_{SW} is presented in [47]. Comparator-based, dual-edge modulation deadtime optimization, and adaptive deadtime controller techniques, are presented in [48], [49], and [50], respectively. An issue with the deadtime control circuits presented in [45]–[50] is that the sensing voltage V_{SW} for estimating the required deadtime needs a few switching cycles of the power converter operation because the V_{SW} signal has the longest rise and fall times (t_r and t_f) in the power converter. This is decreasing the performance of the deadtime control circuit. The additional circuit required to measure the potential of V_{SW} can also affect the power density and increase the cost. A dynamic deadtime optimization technique for a power converter is presented in [51]. In this approach, an additional circuit was placed in parallel with the LSS, which affects the performance of LSS. Another circuit is also needed to sense the voltage of V_{IN}, which increases the overall power consumption of the converter and reduces the efficiency.

In this work, we propose a novel circuit for deadtime control that provides a wide range of delays to the power converter HS and LS by utilizing three independent reconfigurable analog modules. The tunable modules can receive digital commands from a controller to tune the required deadtime. In contrast with what is usually accepted, i.e. the values of T_{DHL} and T_{DLH} must be minimized as much as possible according to (1) to decrease the deadtime loss, we show that this applies only for T_{DLH}, while an optimal value can be reached for T_{DHL} to decrease the power converter's deadtime loss. Indeed, if the T_{DHL} is made shorter or longer than the optimal value, the deadtime loss increases degrading the converter efficiency. The remaining of this paper is arranged as follows. Section II presents the proposed building blocks, circuit implementations, and mathematical analyses. Section III presents the experimental results. Section IV discusses the performance comparison with other solutions. Section V provides the conclusion.

II. Proposed Tunable Deadtime Circuit

A. Proposed Architecture

Fig. 4 illustrates the configuration of the proposed Wide Range Multi-Tuned-Deadtime Control Circuit (WRM-TDC). Three adjustable parts (A, B, and C) are utilized to allow a wide range of deadtime delays. The controller command can be used to set up these parts (32 dedicated switches are used

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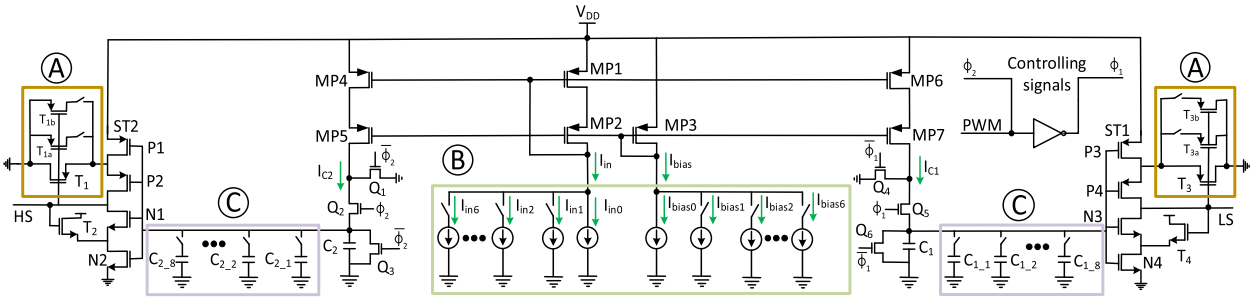

Fig. 4. Schematic of the proposed Multi-tuned-dead-time generator. Three tunable parts of A, B, and C can receive tunning commands from the FPGA to reconfigure the circuit for creating different required delays between the generated non-overlapping signals on the outputs of HS and LS [40]. All the components of the proposed circuit will be integrated as a part of gate driver for different power converter applications.

for both sides). The presented WRM-TDC uses two initial capacitors (C_1 and C_2), which are linearly charged by I_{C1} and I_{C2}, respectively, to produce two rectangular signals.

These rectangular waveforms are applied to two Schmitt Triggers (ST1 and ST2). Two pulse signals are generated at the output of ST1 and ST2 when the rectangular signals are applied because the hysteresis windows of ST_1 and ST_2 are initialized (switching thresholds of STs are set with initial values). The two pulse-shaped signals produced at the output of STs do not overlap each other due to the created deadtime between T_{DLH} and T_{DHL} thanks to the presented WRM-TDC. A wide swing current source (MP1-MP7) is employed to mirror the currents of I_{in} and I_{bias} (for producing I_{C1} and I_{C2}). In addition, the switches of Q_1-Q_6 are closed/opened with controlling signals ϕ_1 and ϕ_2 to charge/discharge C_1 and C_2. The gate driver with the adjustable deadtime receives a PWM signal from the controller and generates two waveforms for HS and LS power switches with optimal T_{DLH} and T_{DHL} to allow for high power conversion efficiency with minimized deadtime loss.

The advantages of the presented WRM-TDC are:

- Digital commands are sent to the WRM-TDC to adjust the required deadtime of the gate driver. Accordingly, off-chip components or digital-to-analog converters are not needed. Therefore, the communication between the FPGA and the gate driver is facilitated, the power consumption of the gate driver is decreased, and the reliability of power converters is increased. In addition, the strategy for generating different deadtimes is simple and fast.
- To tune the proposed deadtime control circuit, we use three different current/capacitor-based tuning circuits (A, B, and C). Hence, producing a wide range of T_{DLH} and T_{DHL} is possible. This potential procedure is essential for power converters with various loads and V_{IN}.
- The type of circuits used to design each reconfigurable part is different. Accordingly, the attained resolution from each part is different. ST has the highest resolution, while the capacitor-based parts have the lowest resolution. This situation allows the allocation of the least significant bits LSBs) of the controlling code to ST-based tuning circuit. Meanwhile, the most significant bits MSBs) are dedicated to the capacitor-based parts. Therefore, when large deadtimes is required, the proposed WRM-TDC can support power converters with a wide range of V_{IN} and load.

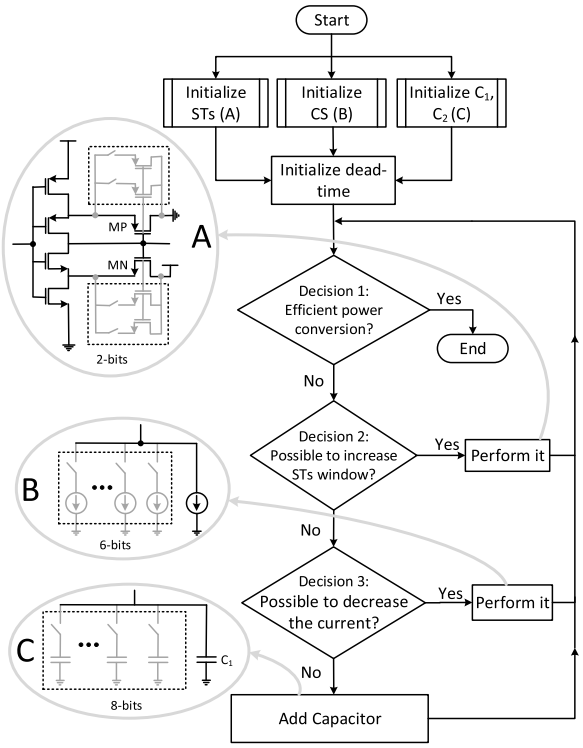

Fig. 5. Flowchart of the operation of proposed deadtime control circuit.

B. Circuit Programming and Optimization Approach

Fig. 5 clarifies the flexibility and the reconfigurability of the presented WRM-TDC. The involved parameters and the methodologies used to realize the projected objectives are illustrated. Three sections of A, B, and C must be initiated to start the deadtime. Then, the power conversion must be verified according to the decision steps of the flowchart (i.e. decision 1, decision 2, and decision 3) to achieve maximum efficiency in a given power converter. According to [17], an efficient conversion occurs when the power converter output waveform (V_{SW}) meets the following conditions: $t_{Df} = 0$, $t_{Dr} = 0$, $t_{rL} = 0$, and $t_{fL} = 0$. The power dissipation (conduction loss) of the transistor increases with V_{DS}. During "t_{Df}" and "t_{rL}" (t_{fL} and t_{Dr}) the voltage drop across the low side transistor (V_{DS}) and is larger than that when the low side transistor is ON. This increases the conduction loss of

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the low side transistor during the "t_{Df}" and "t_{rL}"(t_{fL} and t_{Dr}). Thus, by minimizing the "t_{Df}" and "t_{rL}" (t_{fL} and t_{Dr}), the conduction loss of the low-side transistor will be minimized, and the power conversion efficiency will be maximized.

If the conversion is efficient, then the configured WRM-TDC is convenient for the application. Otherwise, the first tuning part (A) must be reconfigured to achieve more delays if there is still some bit available for the reconfiguration of part A. Then, the status of the power converter must be verified again to determine if the target efficiency has been met. To reconfigure part A, 2 bits are dedicated to change the values of T_{DLH} and T_{DHL}. As shown in Fig. 5 (part A), MOSFETs are adding in parallel with MP step by step and the same for MN to change the deadtimes. Consequently, the V_{refs} of STs will be modified, resulting in a broader hysteresis window being applied to the ramp signals over the main capacitors. Finally, the deadtime is increased to reach the optimal deadtime.

If the conversion is still inefficient when both bits of part A are used, then part B must be configured, as shown in Fig. 5. Part B utilizes a tunable current source that is controlled by 6 bits. The amount of delivered current to the main capacitors must be decreased to obtain more deadtime. For this purpose, the number of paralleled current sources must be decreased step by step, with the condition of "efficient conversion" being verified at every step. If all the 6 bits of part B were used, then the third part (C), which contains a capacitive bank, must be included in the circuit. The capacitive bank is controlled with 8 bits to adjust the capacitor value and tune the adequate deadtime for the power converter based on the values of V_{IN} and the load. If all the 16 bits of parts A, B, and C were used, and the converter still needed longer deadtime, then the values of V_{IN} and the load should be fixed. Specifically, the proposed reconfigurable deadtime can be useful over specified ranges of V_{IN} and loads. Notably, cases where I_{OUT} is high, and V_{IN} is low require short deadtimes.

C. Circuit Implementation

Fig. 6 shows the circuit implementation of the reconfigurable parts (A, B, and C) of the proposed WRM-TDC. In part A, T_1 and T_3 are the key transistors to configure the hysteresis windows of ST2 and ST1, respectively. These hysteresis windows of ST1 and ST2 depend on the dimensions of T_1 and T_3, respectively. Two p-channel MOSFETs of T_{1a} and T_{1b} (T_{3a} and T_{3b}) are included in parallel with T_1 (T_3) to design an adjustable part on the STs. The hysteresis windows of the STs can be expanded if their adjusting transistors are excluded from the STs. Hence, the p-channel MOSFETs (T_{1a}, T_{3a}, T_{1b}, and T_{3b}) are enabled to achieve the shortest possible deadtime as the initial configuration. Then, this adjusting part A must be excluded from the circuit by active low switches (p-type transistors) to obtain the longer deadtime.

T_{1b} and T_{3b} which are tunable parts of ST2 and ST1, respectively, are controlled with the activating bits of b_{0L} and b_{0H} to change the values of the delays of T_{DLH} and T_{DHL} (the same for T_{1a} and T_{3a}).

The second tunable parts are I_{in} and I_{bias}. The parallel diode connected n-channel MOSFETs of MN0–MN13 are implemented to fulfill this part with real circuits. The values of the produced T_{DLH} and T_{DHL} are inversely related with currents I_{in} and I_{bias}. Accordingly, all the diodes connected must be added in the circuit to achieve the minimum T_{DLH} and T_{DHL}. Then, the MN1–MN6 and MN8–MN13 must be removed from the circuit with the active low switches (p-type transistor) to provide longer delays.

TABLE I

DIMENSIONS OF ALL COMPONENTS ADOPTED FOR REALIZING THE CIRCUIT

	Comp.	P1,2;N1,2	T2	T1	T1a	T1b
A, ST	W(μm)	0.4	0.6	0.6	0.8	1
	L(μm)	0.45	0.35	0.35	0.35	0.35
C	Comp.	C_2	$C_{2\text{-}1}$	$C_{2\text{-}2}$	$C_{2\text{-}3}$	$C_{2\text{-}4}$
	Value(fF)	10	15	30	60	120
	Comp.	$C_{2\text{-}5}$	$C_{2\text{-}6}$	$C_{2\text{-}7}$	$C_{2\text{-}8}$	
	Value(pF)	0.24	0.5	1	1.5	
B	Comp.	MN0	MN1	MN2	MN3	MN4
	W(μm)	0.4	0.6	0.8	1	1.2
	L(μm)	5	5	5	5	5
	Comp.	MN5	MN6	N/A	N/A	N/A
	W(μm)	1.4	1.4	N/A	N/A	N/A
	L(μm)	5	5	N/A	N/A	N/A
CS	Comp.	MP1, MP2	MP3	MP4-MP7	All switches	
	W(μm)	0.8	0.4	0.8	0.4	
	L(μm)	0.35	0.35	0.35	0.35	

N/A= NON-APPLICABLE; ST: SCHMITT TRIGGER; MP, P, N, T, MN: ARE TAGGED ON FIG 4,6; CS: WIDE SWING CURRENT SOURCE.

The third reconfigurable part of the proposed WRM-TDC is shown in part C. The value of the produced T_{DLH} and T_{DHL} are in direct relation with the sizes of the capacitors used. Accordingly, one capacitor is utilized in the circuit as initialization to attain the shortest T_{DLH} and T_{DHL}. Then, the integrated capacitors ($C_{1-1} - C_{1-8}$ and $C_{2-1} - C_{2-8}$ in Fig. 6) are included in the circuit to be in parallel with the main capacitors (C_1 and C_2 in Fig. 4) for creating longer T_{DLH} and T_{DHL}. The integrated switches in this part must be active high type (n-type MOSFET).

The aspect ratios of the transistors and the values of the passive components used to implement each part of the presented circuit are listed in Table I. These components are needed for implementing one side of the circuit (generating T_{DHL}). The other side of the circuit uses the same components to generate T_{DLH}. 32 bits b_{0L} to b_{15L} and b_{0H} to b_{15H} are devoted for controlling the 32 switches used to realize the tunable parts in both sides of Fig. 4. Among these 32 bits, four LSB bits of b_{0L}-b_{1L} and b_{0H}-b_{1H} are allocated to the ST-based parts (in the right and left of Fig. 4), 12 bits of $b_{2L} - b_{7L}$ and $b_{2H} - b_{7H}$ are earmarked to current source part (I_{in} and I_{bias}), and the 16 MSB bits of $b_{8L} - b_{15L}$ and $b_{8H} - b_{15H}$ are assigned to capacitor-based tunable part.

The created delays in the presented WRM-TDC depends on the amounts of currents I_{C1} and I_{C2} (Fig. 4) delivered by the current source to the integrated capacitors. Given the relation between the output current and the values of I_{in} and I_{bias}, the operation of the proposed design against mismatch and process corners should be validated. Specifically, MN0–MN13 (Fig. 6, part B), which are used to adjust the biasing current, must be made robust against process variations. The operations on both sides of the proposed WRM-TDC are the same during the production of T_{DHL} and T_{DLH} (deadtime). A different deadtime is due to the various parameter values on each

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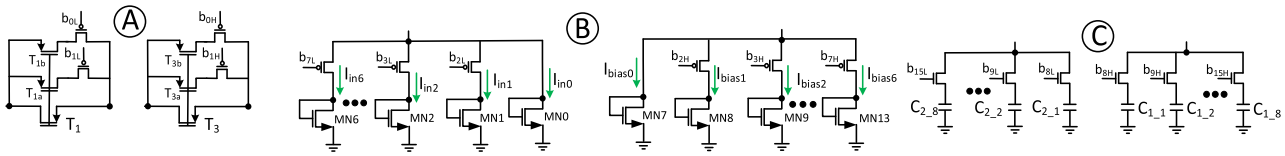

Fig. 6. Transistor level implementation of the tunable A, B, and C parts.

side of the circuit. Accordingly, the circuit is evaluated to be robust against process variations for one of the deadtimes (i.e., T_{DHL}). The simulated deadtime value T_{DHL} is 47.5 ns for the designed circuit and associated typical case corner (i.e., typical NMOS and PMOS transistors and $V_{DD} = 3.3$ V). A worst-case scenario is simulated to anticipate the effect of process variations. Using the AMS kit, "fast NMOS/fast PMOS" yields the highest power consumption or Worst power (WP), whereas "slow NMOS/slow PMOS" yields the slowest speed or Worst speed (WS). In this study, we evaluate the operation of the proposed circuit in the WP and WS cases for one of the tuning commands (i.e., 0FFF). The WP and WS are the worst operating conditions of the circuit (Fig. 6). The simulated deadtime values T_{DHL} for the WP and WS cases are 35.8 and 72.92 ns, respectively. The WS case yields the longest deadtime, while the WP has the shortest deadtime. The impact of the process variations on the performance of the proposed WRM-TDC is studied using a Monte-Carlo simulation. A supply voltage of $V_{DD} = 3.3$ V is set for the simulation. The results for T_{DHL} are shown in Fig. 7 (a). Specifically, the simulated T_{DHL} shows a log-normal distribution with a variance of 0.12. The *average delay* of T_{DHL} is 48.46 ns, and the standard deviation is 5.84 ns. To increase robustness against process variations and decrease the standard deviation, the dimensions of MN0–MN13, which are responsible for biasing the circuit, can be increased while maintaining the same aspect ratio "W/L". But, a trade-off must be made between the chip area and the sensitivity of the generated deadtime to process variations. The operation of the proposed circuit is evaluated under different programming commands (i.e., 0FFF) and temperatures (−40 °C to 80 °C). Fig. 7 (b) presents the simulated results. The value of $T_{DHL} = 50$ ns is selected by the command "0FFF", and varies from 42 to 52ns for the above temperature range.

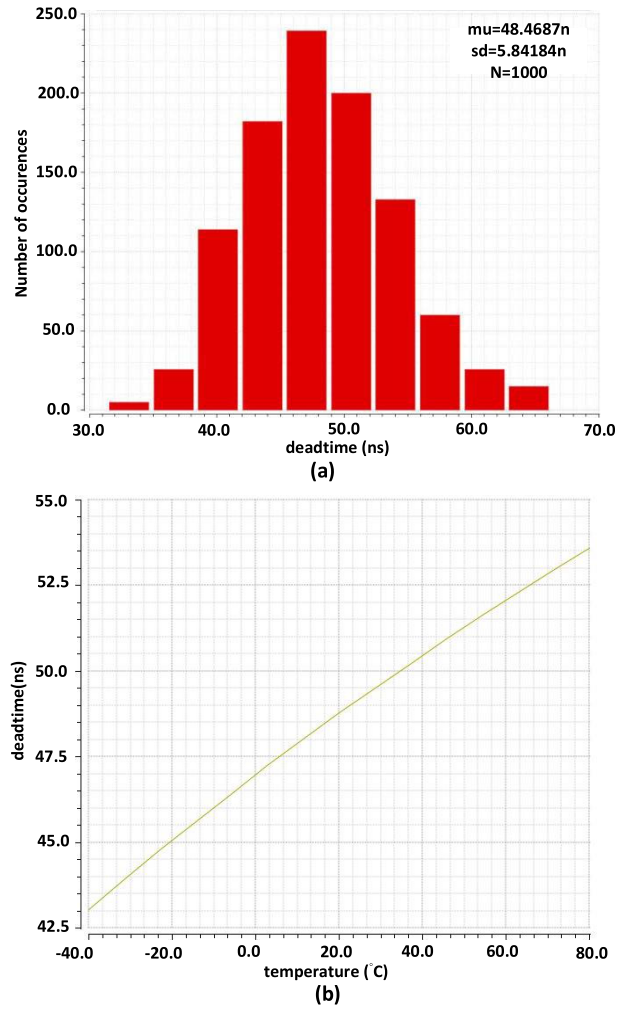

Fig. 7. (a) Evaluation of the proposed WRM-TDC operation with Monte-Carlo simulation, (b) assessment of a certain dead time value for different temperatures.

D. Optimal Deadtime Mathematical Analysis

A simplified power converter circuit is illustrated in Fig. 8 to derive the equation of the optimum required deadtime for a buck converter. Fig. 8 (a) shows the converter circuit when the HSS is turned on and the LSS is turned off. The HSS and LSS are in their 'off' states within the deadtime duration. Meanwhile, Figs. 8 (b) and (c) show the operation at the beginning of the deadtime with the effective parasitic capacitance and the equivalent circuit of the converter during the deadtime operation with the charged equivalent capacitor in node V_{SW}, respectively. Within the deadtime duration, the HSS and LSS are turned off. In this condition, the total equivalent capacitance in node V_{SW} is given by

$$C_{eq} = C_{gd-LS} + C_{ds-LS} + C_{gs-HS} + C_{ds-HS} + C_{par}, \quad (2)$$

where C_{par} is the parasitic capacitance of the power switch packaging and wire-bonding. Fig. 1 (b) shows that the deadtimes T_{DLH} and T_{DHL} are set asymmetrically to ensure a secure operation against shoot-through and provide efficient conversion of the power converter. To increase the buck converter efficiency, the T_{DHL} must be set in its optimal state, which is when the charged C_{eq} is totally discharged ($V_{Ceq}(T_{DHL}) = 0$), then the LSS must be activated. Otherwise, if T_{DHL} is set longer or shorter than the optimal time, the loss is increased, and the buck converter will not be efficiently designed. The optimal duration condition for T_{DLH} is determined to avoid shoot-through. The value of T_{DLH} can be reduced as long as shoot-through does not occur. The equivalent circuit of the buck converter is shown in Fig. 8(c)

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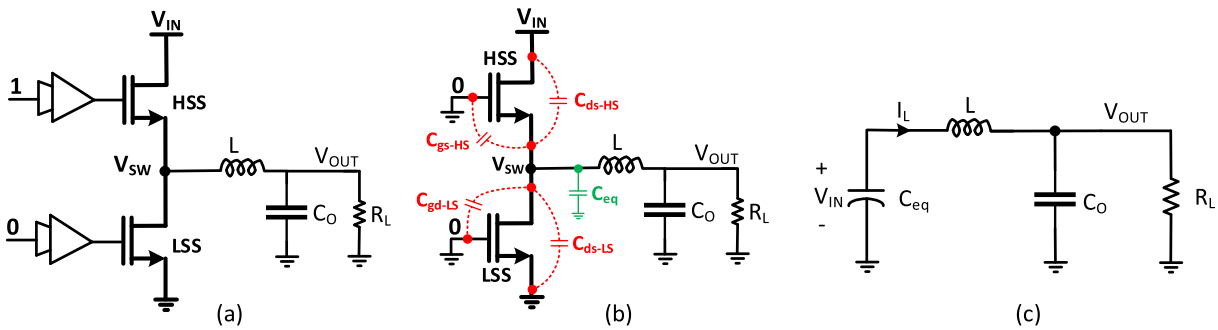

Fig. 8. Buck converter operation evaluation. (a) Simplified circuit while the HSS is turned on and the LSS is turned off, (b) operation in the beginning of deadtime with effective parasitic capacitance, and (c) equivalent circuit during deadtime operation with the charged equivalent capacitor in the node V_{SW}.

where C_{eq} is charged in advance by V_{IN} at the beginning of the deadtime. The analysis of the deadtime generation begins with:

$$V_L(t) = L\frac{dI_L(t)}{dt}, \tag{3}$$

which can be rearranged as follows when evaluated within a given time interval, ΔT:

$$V_L \Delta T = L \Delta I_L, \tag{4}$$

where V_L equals to $V_{IN} - V_{OUT}$. In this buck converter, ΔT is for the time duration of the HSS operation for one cycle of the input PWM, which is obtained by the product DT_s. Thus, in (4), ΔT must be replaced by DT_s as follows:

$$(V_{IN} - V_{OUT})\, DT_s = L \Delta I_L, \tag{5}$$

where D and T_s are the duty cycle and period of the input PWM, respectively. In the buck converter, D is equal to V_{OUT}/V_{IN}[46]. The value of ΔI_L is evaluated by substituting the V_{OUT}/V_{IN} instead of D in (5) as follows:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT})\left(\frac{V_{OUT}}{V_{IN}}\right)\frac{1}{f_s}}{L} = \frac{V_{OUT}\,(V_{IN} - V_{OUT})}{L V_{IN} f_s}. \tag{6}$$

In Fig. 1(b), the red curve shows the currents flowing into the circuit during the deadtime, in which $I_{L(peak)}$ is equal to $I_{Load} + (\Delta I_L/2)$. According to (6), $I_{L(peak)}$ can be defined by:

$$I_{L(peak)} = I_{load} + \frac{\Delta I_L}{2} = I_{load} + \frac{V_{OUT}\,(V_{IN} - V_{OUT})}{2 L V_{IN} f_s}. \tag{7}$$

After setting an optimal deadtime for the buck converter, the zero-voltage switching condition would occur [51]. In this condition, the available charge in the C_{eq} is discharged by converter's inductance before turning-on the LSS. According to the equation of the equivalent capacitance in node V_{SW} at a given time,

$$I_{Ceq} = C_{eq}\frac{dV_{Ceq}(t)}{dt} \Rightarrow I_{Ceq} = C_{eq}\frac{\Delta V_{Ceq}(t)}{\Delta t}. \tag{8}$$

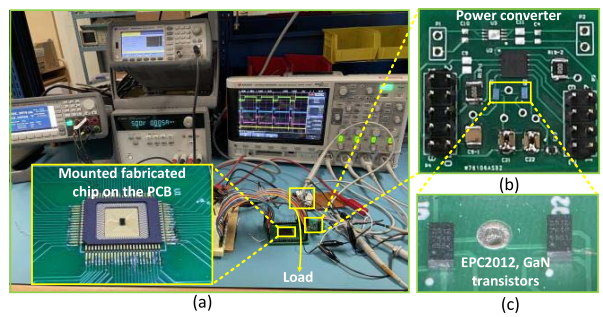

Fig. 9. Experimental setup: (a) equipment to measure the performance of fabricated WRM-TDC, (b) enlarged power converter, and (c) enlarged power GaN transistors of EPC2012.

During the discharge of the equivalent capacitance, $I_{Ceq-discharge} = I_L$. Hence,

$$\Delta t = \frac{C_{eq}\,\Delta V_{Ceq}(t)}{I_L}. \tag{9}$$

As shown in Fig. 1(b), I_L is approximately equal to I_{Lpeak} ($I_L(t) \approx I_{Lpeak}(t)$) within the deadtime duration, and $\Delta V_{Ceq}(t)$ is equal to $V_{IN} - V_{Ceq}(T_{DHL}) = V_{IN} - 0 = V_{IN}$ in the optimal deadtime conditions ($V_{Ceq}(T_{DHL}) = 0$). This condition holds for all Δt equal to T_{DHL}, specifically at its optimal value. From the equation of I_{Lpeak} in (7), the optimal deadtime is given by

$$\Delta t_{opt} = \frac{C_{eq} V_{IN}}{I_{Lpeak}} = \frac{C_{eq} V_{IN}}{I_{load} + \frac{V_{OUT}(V_{IN} - V_{OUT})}{2 L V_{IN} f_s}} = T_{DHL}, \tag{10}$$

where $I_{load} = V_{OUT}/R_L$. The deadtime T_{DLH} must be minimized as much as possible to avoid shoot-through. An efficient buck converter design must address this requirement.

III. Measured Performance

A. Experimental Results of Proposed WRM-TDC

Fig. 9 shows the experimental test bench. The experimental results of the proposed WRM-TDC are measured by soldering it on a printed circuit board (PCB) in the laboratory. Two 16-bit flat ribbon cables are utilized to send the digital commands to the proposed circuit to program the different T_{DHL} and T_{DLH} at the circuit output. A pulse-shaped signal was generated with a function generator as input signal. The deadtimes T_{DHL} and

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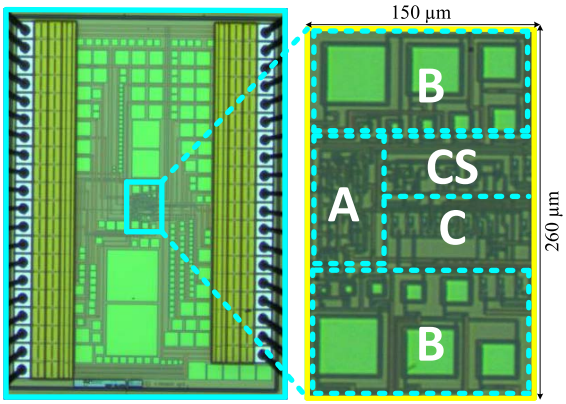

(a) (b)

Fig. 10. Chip micrograph of the proposed WRM-TDC fabricated in 0.35 μm CMOS process (a) die micrograph, (b) enlarged core including different circuit parts of A, B, C, and CS.

T_{DLH} are measured with an oscilloscope between the non-overlapping signals. Different capacitive loads of 1pF-10nF was used at each output of under test chip to measure the performance of fabricated chip.

The chip micrograph of the proposed WRM-TDC fabricated in 0.35 μm CMOS process is presented in Fig. 10. A wire-bonded die micrograph is presented in Fig. 10(a). The enlarged cores of the fabricated chip, which includes the different parts of A, B, C, and CS and occupies 150 μm$\times$260 μm of silicon area, are shown in Fig. 10(b). Fig. 11 shows the measured deadtimes generated by the WRM-TDC. The measured minimum and maximum selectable deadtimes corresponding to programing commands of 0000 and FFFF are presented in Fig. 11(a) and (b), respectively. A minimum deadtime of T_{DLH} = 9.2 ns is measured for the proposed WRM-TDC, while the circuit was supplied with V_{DD} = 5.0 V, and the operating frequency was f_s = 1 MHz. A maximum deadtime of T_{DHL} = 1 μs is measured, while the fabricated prototype was supplied with V_{DD} = 3.3 V, and the operating frequency was f_s = 200 kHz. In Fig. 11, the green waveform corresponds to the input pulse signal applied to the chip. The signals in blue and red correspond to the output of the chip, which can be used as appropriate driving signals for the HS and LS of the buck converters. The measured T_{DLH} and T_{DHL} are shown in blue and red in Fig. 12(a), respectively. The circuit is connected to V_{DD} = 5.0 V, a capacitive load C_L = 1pF was used, and the operating frequency was set to f_s = 1 MHz. The measured results are categorized based on the operation of the circuit in four different regions. In the first region, the proposed WRM-TDC is initialized to produce the shortest possible deadtime. In this configuration, parts A and B are enabled, and part C is disabled (MN0-MN13, T_{1a}, T_{1b}, T_{3a}, and T_{3b} are in the circuit, while the integrated capacitors are disabled). In this first region, the measured T_{DLH} and T_{DHL} are 9.2 and 10.8 ns, respectively. The circuit can be programed to work in the other regions to increase the deadtime. In Region 2, part A is disabled step by step by received commands, part B is enabled, and part C is disabled. The LSB b_0 is set to "1" to increase the delay whereas the other bits are kept at "0" (i.e., the command of "0001", which is the hexadecimal code corresponding to the controlling switches status, is sent to the WRM-TDC). Two bits are dedicated to Region 2. In this part, the measured deadtime resolution is 0.2 ns with 1% precision. Accordingly, the maximum achievable deadtimes for Region 2 are T_{DLH} = 9.6 ns and T_{DHL} = 11.2 ns under V_{DD} = 3.3 V and f_s = 1 MHz. The circuits of Region 3 are activated step by step by the commands to achieve longer deadtimes than what is attained in Region 2. In Region 3, parts A and C are disabled, and part B is enabled. The measured resolutions of the circuit in Region 3 for T_{DLH} and T_{DHL} are measured at approximately 0.3 and 1 ns (the difference between two measured deadtimes corresponds to two commands), respectively, while the number of bits dedicated to this region is 6 bits. Accordingly, the maximum measured T_{DLH} and T_{DHL} are 12 and 16.6 ns, respectively. Parts A and C are disabled, while part B is enabled by the commands to measure the results in Region 3. A longer deadtime can be achieved in Region 4 where the circuit is using a capacitive bank as delay element. In Region 4, eight different values of integrated capacitors (Table I) that correspond to eight controlling bits are embedded. The longest T_{DLH} = 250 ns and T_{DHL} = 300 ns are measured in Region 4 for commands of 01FF to FFFF. Parts A and B are disabled, and part C was enabled by the commands to measure the results in Region 4. The measured results in Fig. 12(b) show the performance of the circuit in various conditions. The circuit is configured by the different commands while it is connected to V_{DD} = 3.3 V, the capacitive load was changed from C_L = 1 pF to C_L = 12 pF, and the operating frequency was set to f_s = 400 kHz. In this condition, the measured T_{DLH} and T_{DHL} are 11 ns to 450 ns and 16 ns to 1000 ns, respectively, depending on the configuration, as shown in Fig. 12(b). The presented experimental results in Fig. 12 (b) demonstrate that the configured circuit can produce stable T_{DHL} and T_{DLH} for different capacitive loads at a fixed V_{dd}.

Fig. 13(a) shows that the measured power dissipation of the fabricated chip corresponds to all ranges of deadtime produced by the proposed WRM-TDC in the different programed circuit configurations. The results are measured for five different values of capacitive loads. The largest power dissipation corresponds to the "0000" command (shortest delay) because all the tunable capacitive parts of A and B are added at the load in the circuit in this condition. The power dissipation results follow a descending curve (Fig. 13 (a)) due to the removable of the tunable parts of A and B by the commands of "0001" to "00FF". The results follow an ascending curve due to inclusion of the integrated capacitors of part C at a longer deadtime. The circuit programed with command "FFFF" is tested with C_L = 10 nF at V_{dd} = 3.3 V and f_s = 200 kHz to see the performance of circuit in the case when driving big capacitive loads. The output waveforms of the chip are presented in Fig. 13(b). Fig. 13 shows that a long deadtime of T_{DHL} = 960ns with the command of "FFFF" is achieved while the circuit is driving two large capacitive loads at its outputs. For T_{DLH}, the value is set as short as possible, at the limit before shoot-through occurs. In Fig. 13(b), the red waveform (i.e. the LSS activation signal) reaches zero then the blue one (i.e. the HSS activation signal) starts to increase. Given that the waveforms have no overlap between the transition, consequently, shoot-through does not occur. In this condition, the proposed deadtime circuit consumed 41 mW, while the measured output signal slew rate (SR) was 0.62 V/ns. The circuit has two outputs, namely, LS and HS,

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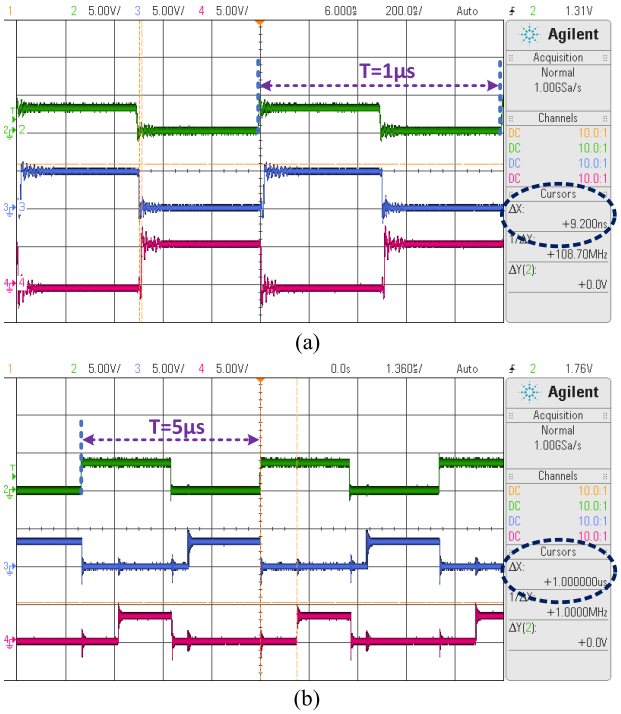

Fig. 11. Measured generated dead-times by WRM-TDC: (a) minimum produced dead-time of T_{DLH} = 9.2 ns at C_L = 1 pF, V_{dd} = 5.0 V, and f_s = 1 MHz; (b) maximum attained dead-time of T_{DHL} = 1 μs at C_L = 5 pF, Vdd = 3.3 V, and f_s = 200 kHz.

where the dynamic current is consumed to drive the capacitive loads. Therefore, to calculate the slew rate of the waveform at each output, half of the consumed dynamic current can be divided by the capacitive load (SR = $0.5 \cdot i_{dynamic}/(C_L)$ = 0.5·12.4 mA/10 nF = 0.62 V/ns), which is reasonable for typical applications. Fig. 14 illustrates the measured power consumption versus operating frequency at different tuning commands, C_L = 10 pF, and V_{DD} = 3.3 V. According to the measured results, the power consumption increases with f_s. However, the maximum f_s is limited depending on the tuning commands. At FFFF, where the circuit can produce maximum T_{DLH} and T_{DHL}, the f_s is limited to 1 MHz. The circuit programed with command 0000 to generate the minimum T_{DLH} and T_{DHL} can work properly up to 18 MHz, and the measured power consumption is presented in Fig. 14. The circuit programed with command 0000 consumed approximately 21 at f_s = 18 MHz, whereas it dissipated 0.48 mW for command FFFF at f_s = 200 MHz.

B. WRM-TDC Circuit Validation With a Buck Converter

To validate the operation of the proposed WRM-TDC, a buck converter is mounted on a PCB, as shown in Fig. 9. The fabricated chip is connected to the buck converter to measure the improvement of efficiency in the optimal T_{DHL} compared to a fixed T_{DHL}. Fig. 15 shows the optimized buck converter design waveforms with optimal T_{DHL} and minimum T_{DLH} values. The converter specifications are R_L = 80Ω, V_{IN} = 12V, V_{out} = 2.0V, duty cycle = 16.7%, I_{Load} = 25mA, f_s =0.4MHz, T_{DLH} = 12ns, and T_{DHL} = 80ns. The conditions of t_{Df} = 0, t_{Dr} = 0, t_{rL} = 0, and t_{fL} = 0 in the V_{SW} waveform are achieved for optimal T_{DHL} and minimum T_{DLH}. In other

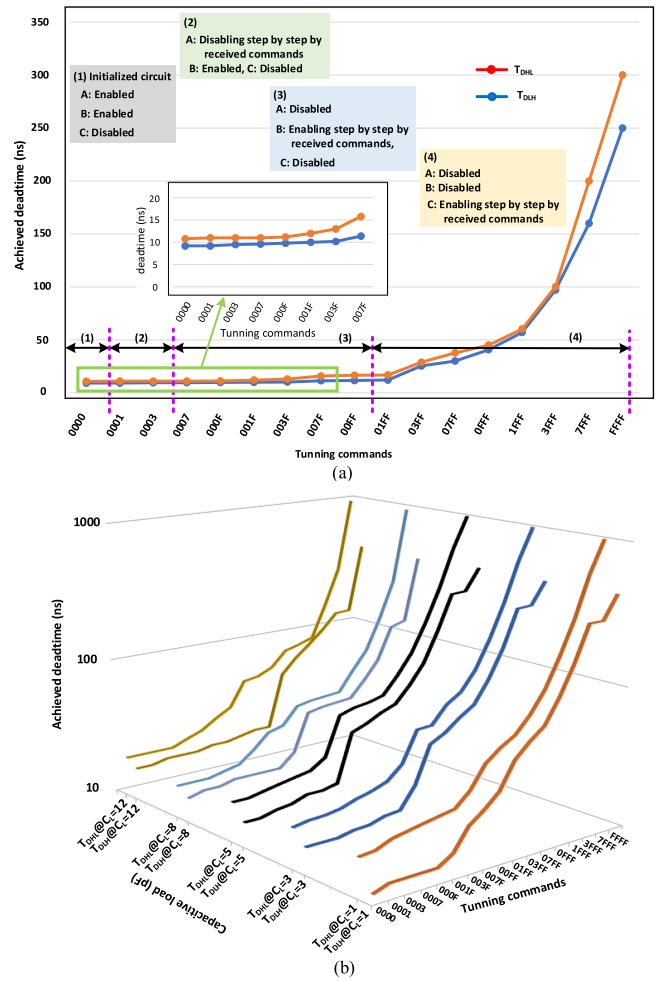

Fig. 12. Measured T_{DLH} and T_{DHL} from the fabricated chip in the various conditions: (a) different configurations of circuit at V_{dd} = 5.0 V, capacitive load C_L = 1 pF, and f_s = 1 MHz; (b) different configurations of the circuit at V_{dd} = 3.3 V, capacitive between C_L =1 pF to C_L = 12 pF, and f_s = 400 kHz.

words, the LSS Gate signal can increase exactly when the V_{SW} signal reaches zero (C_{eq} is fully discharged ($V_{Ceq}(T_{DHL}$ = 0))). Thus, compared with the use of a fixed random deadtime, the efficiency improves by 12%.

In order to set I_{load} = 25–400 mA (i.e. the inductor direct current resistance), the specifications of the buck converter are V_{IN} = 12 V, f_s = 0.4 MHz, V_{OUT} = 2 V, L = 100 μH, C_O = 4.4 μF, DCR =200 mΩ, ESR = 100 mΩ (capacitor equivalent series resistance), and R_L = 80Ω-5Ω. Thus, we can attain maximum efficiency of the buck converter at different loads (25–400 mA). Fig. 16 (a) presents the measured results in three different conditions including 1) T_{DLH} = 12 ns, T_{DHL} = optimum at different I_{load}, 2) T_{DLH} =T_{DHL} = 50 ns (fixed deadtime determined by proposed circuit), and 3) T_{DLH} =T_{DHL} = 12 ns (fixed deadtime). At f_s = 0.4 MHz, the measured efficiency is changed from 53% (at I_{out} =25 mA and T_{DHL} =T_{DLH} = 12 ns) to 80% (at I_{out} = 100 mA and T_{DLH} = 12 ns, T_{DHL} = optimum). The curves in Fig. 16 (a) are obtained using an array of resistive loads between 80 and 5.0 Ω. The resistive loads are connected to the output of the described buck converter and manually switched between each measurement from 80 Ω to 5.0 Ω. The buck converter is

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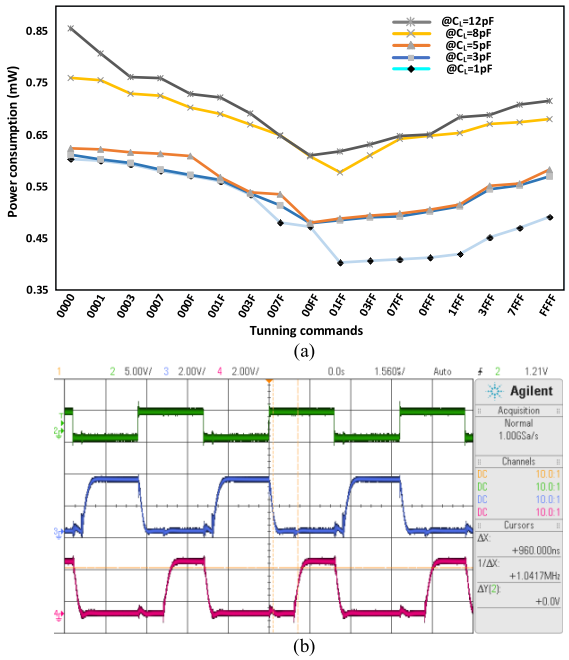

Fig. 13. (a) Measured power consumption versus tuning commands at different capacitive loads. (b) Measured waveforms of proposed circuit at $V_{dd} = 3.3$V, $f_s = 200$khz, and capacitive load of $C_L = 10$ nF at each output of chip.

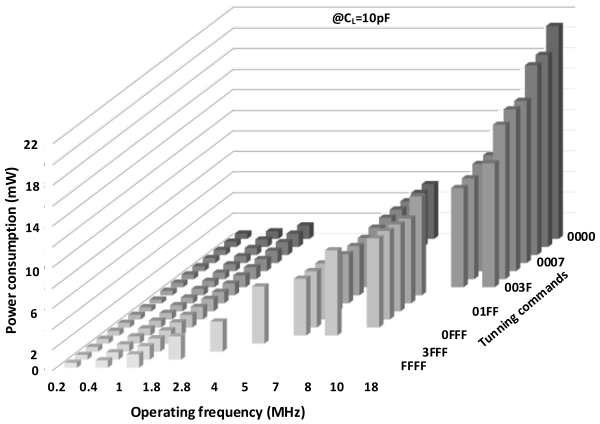

Fig. 14. Measured power consumption versus operating frequency at different tuning commands.

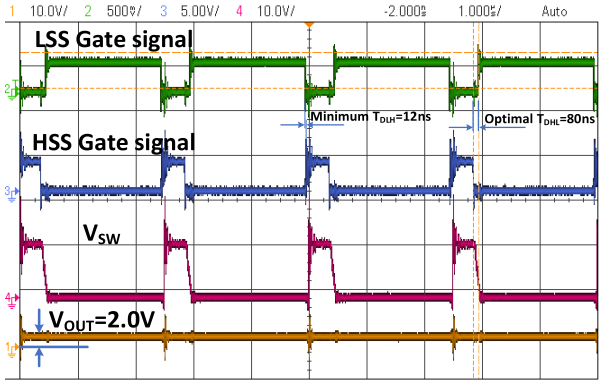

Fig. 15. Buck converter waveforms with optimal T_{DHL} and minimum T_{DLH} under efficient design.

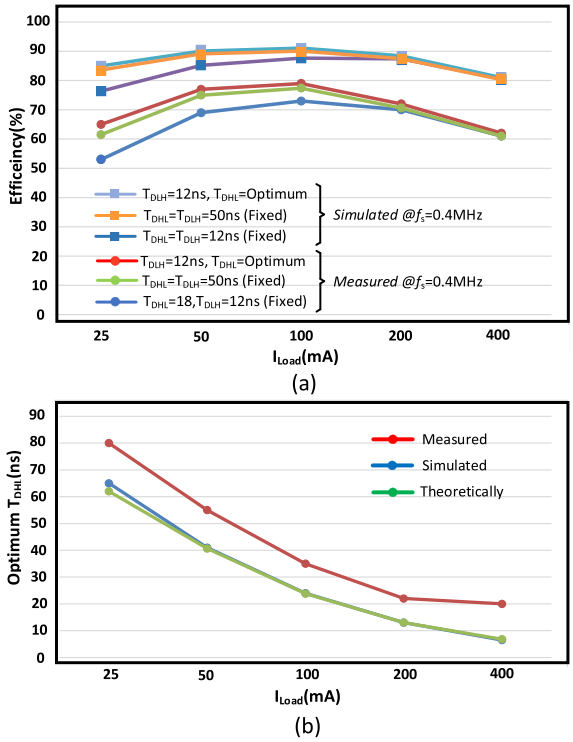

Fig. 16. Measured results (a) achieved efficiency of the implemented buck converter for different T_{DHL} and T_{DLH} at 0.4 MHz versus different I_{load}, (b) comparing the measured, simulated, and calculated optimal T_{DHL}.

connected to a 12.0V power supply and the duty cycle of the input PWM is set to 16.66% [duty cycle $= (V_O/V_{IN}) \times 100 = (2.0V/12.0V) \times 100 = 16.66\%$] by using a function generator. For each resistive load, the output and input power of the buck converter are measured, and the efficiency is then calculated. In addition, the three aforementioned deadtime scenarios are applied. Fig. 16 (a) shows the measured efficiencies versus I_{load} for these three deadtime scenarios. In Fig. 16(a), the red curve follows the maximum efficiency.

Fig 16 (a) shows that, although in the blue curve, the value of T_{DHL} is set to 12 ns (shorter than the optimal value in Fig 16 (b) for different loads), the achieved efficiency is lower than the others. Indeed, the efficiency of the buck converter with minimum T_{DLH} and optimal T_{DHL} at $I_{Load} = 25$mA is improved by 12% compared to converter with fixed deadtime of $T_{DLH} = T_{DHL} = 12$ns. In summary, a significant outcome of the analysis is that although the T_{DLH} must be as short as possible (before shoot through occurs) to attain maximum efficiency, it is different for T_{DHL}. In the buck converters at exact optimal T_{DHL} (no longer and no shorter than the optimal condition), the maximum efficiency would be achieved.

The efficiency of buck converter for $I_{load} = 100$ mA improved by 7% due to the optimal T_{DHL}. The optimal T_{DHL} that corresponds to different I_{out} for frequency of 0.4 MHz are plotted in Fig. 16(b). These optimal T_{DHL}, which are attained based on the measured maximum efficiency at different I_{out}, are compared with the calculated T_{DHL} on the basis of (10) and with the simulated optimal T_{DHL} as well. The results presented in Fig. 16(b) confirm the accuracy of (10). Fig. 16 (b) shows that the maximum efficiency reached by the

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TABLE II
PERFORMANCE COMPARISON OF THE PROPOSED WRM-TDC WITH SIMILAR WORKS

References	TPEL'21, [42]	ECCE'20, [48]	ISSC'16, [49]	ESSCIRC'11, [54]	JSSC'16, [55]	**This work**
Technology(nm)	--	250	350	65	180	**350**
Results	Measured	Measured	Measured	Measured	Measured	**Measured**
Input Voltage(V)	Up to 40V	12	3-40	Up to 5	12-18	**6-24**
Output Current (mA)	240-8800	200-1000	10-1200	Up to 120	50-500	**25-400**
Tunning range (ns)	Up to 50	0.4-9.4	0.9-10.4	1-32	3-28	**9.2-1000**
Power Switches	GaN	GaN	GaN	Si MOS	Si MOS	**GaN**
Bootstrap Capacitor	On-chip	On-chip	On-chip	External	External	**External**
Maximum efficiency (%)	95.8@V_{IN}=30V	87.9%	90.7@V_{IN}=12V	76.4@V_{IN}=3V	81.2@V_{IN}=12V	**90@V_{IN}=24V**
Efficiency improvement	1.9%@V_{IN}=40V, 4.5%@V_{IN}=30V	4%@I_{OUT}=1A	8.5%	3%	6%	**12%@I_{OUT}=25mA, 5.1%@V_{IN}=24V**

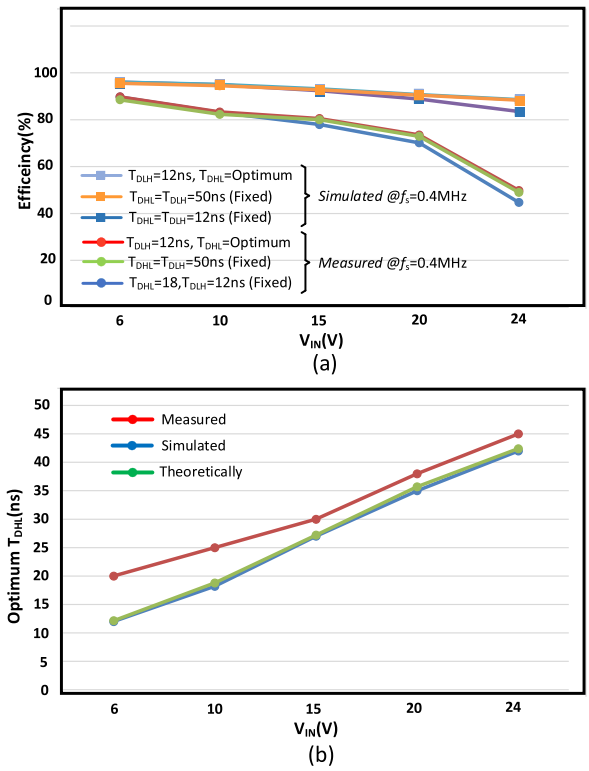

Fig. 17. Measured results (a) achieved efficiency of the implemented buck converter for different T_{DHL} and T_{DLH} at 0.4 MHz versus different V_{IN}, (b) comparing the measured, simulated, and calculated optimal T_{DHL}.

simulated converter at f_s = 0.4 MHz for I_{load} = 25-400 mA is achieved with the optimal deadtimes of 65–6.5 ns.

A buck converter with the following specifications is used to validate the anticipated dependency of T_{DHL} over V_{IN} in (10): V_{OUT} = 3.3 V, f_s = 0.4 MHz, L = 100 μH, C_O = 4.4 μF, DCR = 200 mΩ (inductor direct current resistance), ESR = 100 mΩ (capacitor equivalent series resistance), R_L = 33 Ω (I_{out} =V_{OUT}/R_L = 100 mA), and V_{IN} varied from 6.0 V to 24.0 V. The maximum efficiency of the buck converter for different V_{IN} (6.0–24.0 V) is attained. Fig. 17 (a) presents the measured results of the converter in three different conditions, 1) T_{DLH} = 12 ns, T_{DHL} =optimum at different V_{IN}, 2) T_{DLH} =T_{DHL} = 50 ns (fixed deadtime), and 3) T_{DLH} =T_{DHL} = 12 ns (fixed deadtime). The results are shown in Fig. 17(a). The efficiency changes from 44.1% (at V_{IN} = 24 V, T_{DLH} = 12 ns, and T_{DHL} = 18 ns) to 90% (at V_{IN} = 6.0 V, T_{DLH} = 12 ns, T_{DHL} = optimum). The presented curves in Fig. 17 (a) are obtained by setting the resistive load to 33 Ω. The buck converter is connected to the power supply of 6.0V and the duty cycle of the input PWM is set to 33.33% [duty cycle = $(V_O/V_{IN})\times100$ = $(2.0V/6.0V)\times100$ = 33.33%] by using a function generator. This setup is implemented for different V_{IN} from 6.0V to 24.0V and the duty cycle is set manually in each step. For each V_{IN}, the output and input power of the buck converter are measured and the efficiency is then calculated. In addition, the three aforementioned deadtime scenarios are applied. Fig. 17 (a) shows the measured efficiencies versus V_{IN} for these three deadtime scenarios. The efficiency of the converter with optimal deadtime for V_{IN} = 24 V is improved by 5.1% compared with the efficiency measured with a fixed deadtime (at V_{IN} = 6.0 V and T_{DLH} = T_{DHL} = 12 ns). The improvement of efficiency for V_{IN} = 6.0 V is of 0.4% due to the optimal T_{DHL} compared with the fixed T_{DHL}. In Fig. 17(b), the optimal T_{DHL} that corresponds to different V_{IN} is presented. These optimal T_{DHL}, which are attained based on the measured maximum efficiency at different V_{IN}, are compared with the calculated T_{DHL} based on (10) and with the simulated optimal T_{DHL} as well. The presented results in Fig. 17 (b) confirm the accuracy of (10). The maximum efficiency achieved for the simulated converter at f_s = 0.4 MHz for V_{IN} = 6.0–24 V with the optimal deadtimes of 12-42 ns is shown in Fig. 17(a).

IV. DISCUSSION AND PERFORMANCE COMPARISON

Table II compares the performance of the presented WRM-TDC with other solutions. A deadtime optimization technique based on mathematical analysis is introduced in [42]. As shown in Table II, the optimized deadtime circuit increases the efficiency by 4.5% compared to the fixed deadtime. One disadvantage of the approach described in [42] is that the values of both T_{DLH} and T_{DHL} must be changed based on the circuit parameters. However, we demonstrated that the value of T_{DLH} must be minimized while only the value of T_{DHL} should be determined using the derived equations. According to the measured results, the efficiency can be improved by up to 12% when using the proposed circuit and deadtime optimization method. A bang-bang deadtime circuit that can generate a deadtime ranging from 0.4 ns to 9.4 ns is presented in [48]. The circuit proposed in [48] is suitable for applications with low V_{IN} and high I_{out} requiring a short deadtime. The work presented in [49] can improve

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efficiency by 8.5%. However, the range of generated deadtime is restricted between 0.9 ns to 10.4 ns, which cannot support a wide range of power converter applications. The solutions presented in [54] and [55] lead to maximum efficiencies of 76.4% and 81.2%, respectively, while the efficiency improvement is between 3%-6%. In Table II, the proposed circuit achieves the wider tuning deadtime range, producing delays between 9.2 ns and 1000 ns. Additionally, the proposed optimization technique improves the efficiency by up to 12% compared to a fixed deadtime. Another advantage of the proposed circuit is to accommodate buck converters with a wide range of I_{out} and V_{IN}. In DC–DC converters, the three main types of losses are: 1-switching, 2-conduction, and 3-deadtime. Our method aims to minimize the deadtime loss. Switching and deadtime losses are dominant for light loads and high V_{IN} but conduction loss is dominant for heavy loads. Accordingly, given that our proposed circuit improves deadtime and switching losses, Figs. 16 (a) and 17 (a) show greater efficiency improvement in light loads and high V_{IN}.

V. Conclusion

We proposed a reconfigurable deadtime circuit to produce a vast range of delays between the high and low side waveforms activating a power converter. Three reconfigurable parts are allocated for the designed circuit to have a variable deadtime to accommodate different types of power converter loads and input voltage. In addition, the tunable procedure can help in finding an optimal deadtime for a given power converter to minimize deadtime loss, especially for GaN-based converters that suffer from the deadtime loss. The advantages of the proposed circuit include utilizing a digital approach to adjust the deadtime rely on three different adjustable topologies with different performance in the case of resolution. The circuit yields deadtimes ranging between 9.2 ns and 1000 ns, which a wide variety of power converters driving different loads and operating at various input voltages. According to the measured results, the fabricated chip dissipated 41 mW when configured to produce a long deadtime of 940 ns, while driving $C_L = 10$ nF with a slew rate of 0.62 V/ns. The circuit operates up to 18 MHz when configured to generate the shortest deadtime of 9.2 ns. The fabricated chip was connected to a buck converter to validate the operation of the proposed circuit. The efficiency of the buck converter with minimum T_{DLH} and optimal T_{DHL} at $V_{IN} = 24$V is improved by 5.1% compared to when the converter is using fixed deadtimes of $T_{DLH} = T_{DHL} = 12$ns.

Appendix

The power losses of a typical power converter shown in Fig. 1(a) using GaN power switches can be summarized in Table III. The P_{SW}, P_{CON}, P_{DT}, P_{CAP}, P_G, P_{DCR}, and P_{ESR} are switching loss, conduction loss, dead-time loss, output capacitance loss, gate charge loss, DC resistance of the output inductance loss, and output capacitance ESR loss, respectively. These power converter losses can be categorized into two families. Time-dependent losses are those related to the converter's operating frequency (P_{SW}, P_{DT}, P_{CAP}, and P_G). Time-independent losses (TIL) are due to physical specifications of the power switches and packaging specifications (P_{CON}, P_{DCR}, and P_{ESR}). One of the considerable TIL is due to the layout routing and bonding wires, which can account for approximately 24% of the total loss in a typical power converter [21]. In the P_{CON} equation, the $I_{RMS}$is calculated by

TABLE III
GaN Power Loss Formulas

Loss	*Equation*
P_{SW}	$P_{SW} = V_{IN} \times I_{OUT} \times f_{SW} \times (t_r + t_f)$
P_{CON}	$P_{CON} = R_{ON} \times I_{RMS}^2$
P_{DT}	$P_{DT} = f_S \times V_{SD} \times I_{OUT} \times (T_{DLH} + T_{DHL})$
P_{CAP}	$P_{CAP} = V_{IN} \times Q_{OSS} \times f_{SW}$
P_G	$P_G = (Q_{g-H} + Q_{g-L}) \times V_{gs} \times f_{SW}$
P_{DCR}	$P_{DCR} = (I_{OUT}^2 \times (\Delta I)^2 / 12) \times R_{DCR}$
P_{ESR}	$P_{ESR} = (\Delta I)^2 / 12 \times R_{ESR}$

$$I_{RMS} = \sqrt{\left(I_{OUT}^2 + (\Delta I)^2/12\right) D}, \tag{11}$$

where D is the on-state percentage of either the HSS or the LSS in one cycle of power converter operation.

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