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Bidirectional Parallel Capacitive Data Links: Modeling and Experimental Results

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ABSTRACT We present, in this paper, a bidirectional capacitive data link. Enhancement of the spatial pulse position modulation used on the downlink is introduced, and a load-shift keying modulation is implemented for the uplink. Different grounds on the transmitter and the receiver are discussed, and a compatible solution is proposed. A human skin electrical model is extracted using the agilent impedance analyzer 4294A while doing *in vivo* measurements on cheek skin and then applying curve fitting to the data between 2 and 20 MHz. Multiple geometries for the link are analyzed, and a 5-mm × 5-mm plate size is used for the design of the transceiver. The signal-to-noise ratio along with the capacity of the channel is analyzed theoretically while computing the limits for the downlink and the valid operating frequency to highlight the core parameters that affect the crosstalk interference between channels. The tradeoff in using the uplink on the same channel as the downlink is also discussed and analyzed. The operating frequency is 10 MHz, a bit-rate of 20 Mb/s is demonstrated on the uplink, and 10 Mb/s is demonstrated on the downlink. An *in vivo* human skin model for a 5-mm × 5-mm plate size with 21.2-mm separation is extracted, and the capacity's equation of the channel is computed using the equations for the analysis of the system.

INDEX TERMS Biomedical implants, data link, capacitive link, capacitive channel, skin impedance, load-shift keying, spatial pulse positioning, resistor network.

I. INTRODUCTION

Biomedical implants require communication links to communicate data and transmit power. The history of biomedical implants shows that many implemented designs use different types of communication links, ranging from mechanical push buttons going through wired baseband systems to wireless transceivers [1]–[3]. For most of these implants, the data transmitted is necessary for control and monitoring purposes. Today, most implantable devices target wire-free data transmission systems because they are extremely sensitive to external shocks and displacements. This is because they sit in critically important areas inside the body and are susceptible to physical forces exerted from the external world [3]. More factors that support the wireless trend include skin inflammation and infections that accompany wired data telemetry and most importantly the patient's mobility when connected wirelessly to an external controller system (signal processor, stimulator, camera, etc.).

During the past decade, many wireless data telemetries emerged and have been implemented in biomedical implants including the inductive link [3]–[7], optical link [8]–[12], ultrasonic link [13], [14], radio frequency link [4], [15]–[17] and capacitive link [2], [18]–[21]. All of these links have advantages and disadvantages and are classified first by the data rate, followed by the power consumption and then the size restrictions. The data rate is application-dependent, where some require small data rates like the pacemaker, which requires 1 kb/sec. Some other applications require higher data rates, such as a cortical implant monitoring different parts of the brain, which could require data rates of up to 200 Mb/s [18], [20]. Power consumption in these types of implants is critically limited; the implant could be

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powered internally using a rechargeable battery (limited by the available size for the implant, the heat limitation and the time required for one charge to last) or powered externally by a constant power link (where power is restricted due to the link's characteristics and the maximum allowed power transmission through skin) [3]. The size limitation depends on the location of the implant and how much space is available, along with how much area is useful for the data link.

The inductive link, using magnetic fields, is the most common data link used in recent implants [5]. The main drawback of this link is its low-pass nature, where the link itself acts as a low-pass filter, which makes the link's bandwidth and data rate-limited. The optical link is a good candidate, where data is transmitted using light and detected using light receivers. The RF link has a huge drawback due to signal loss in the skin and the human body and the limited radiation allowed for organ safety [15]. The ultrasonic link is low on bandwidth and requires a lot of power per bit [13].

The capacitive link, transmitting data using electric fields, is a good candidate where the power consumption is low; the modulation is baseband, which makes the transmitter/receiver design light and simple. There are no external limits for the capacitive link's geometry: it is limited by the available internal place within the body. Most capacitive data links designed in the literature use baseband modulation schemes such as amplitude engraving modulation [22], on-off keying [19], spatial pulse position modulation [20], and spatial carrier position modulation [23]. Capacitive data links are also used for inter-chip communication in integrated circuits where an array of plates is located on top of both chips and then placed one on top of the other in the package with a thin layer of insulation in between [22].

In biomedical implants, having a bidirectional data link is important and necessary for system control applications [25], [26]. Load-shift keying (LSK) is a modulation scheme that can be implemented for the uplink on top of most downlink baseband modulation schemes, where the interaction of the downlink signal transmitted with the load at the receiver can be sensed at the transmitter [27], [28]. This system is implemented with an inductive link [26], [27], where the resonance of the link changes on the internal coil and can be sensed by the external coil through voltage variation monitoring. In [5], the system is used on top of the inductive power link. When implementing an uplink on top of a downlink, there will be trade-offs where some of the downlink's performance will be sacrificed for the functionality of the uplink.

In this paper we focus on the implementation of the capacitive communication system theory where the novelty lies in the theory of the link. The tissue modeling is a tool to study this communication link specifically for the cortical implant application.

II. PREVIOUS SYSTEM IMPROVEMENTS

In our previous work, [23], the capacitive link was designed using four plates on the transmitter (Figure 1a), four on the receiver, and four comparators at the front-end of the receiver followed by a low-pass filter on every channel. The output of the low-pass filter is then fed to a flip-flop, where the clock is extracted by connecting the output of all channels to a 4-input OR gate. Separate power supplies for the transmitter and receiver were not taken into consideration with the floating grounds. The reference threshold of the comparators was designed to be set by the external controller by sweeping a feedback system until a reliable signal reception is achieved. In this work, five plates are used on the receiver side, as shown in Figure 1(b), where the fifth plate is used as the common plate and the reference for the comparators. One external physical capacitor is used to replace the insulation layer in [23] on the transmitting plates. A voltage divider is introduced to the receiver's front-end as described later to address the problem of different grounds. These improvements to [23] are elaborated upon in the next three sections.

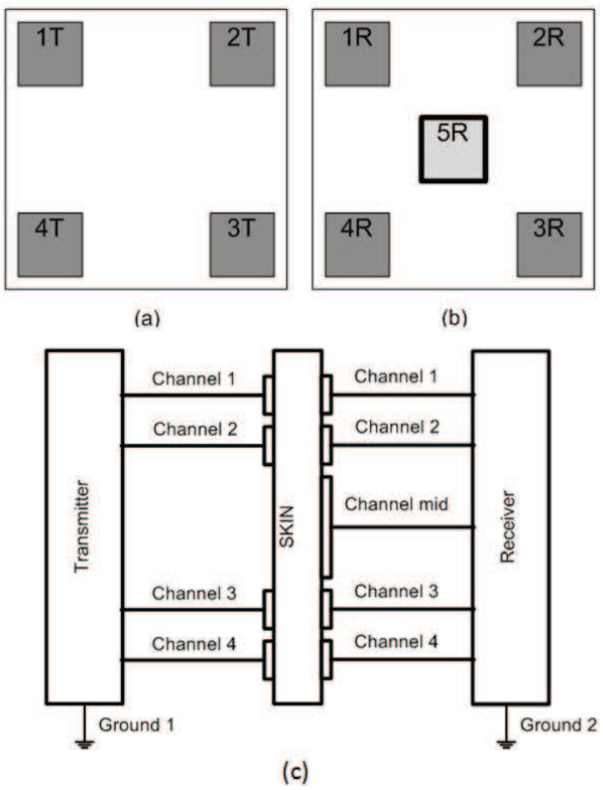

FIGURE 1. Capacitive link geometry and diagram, (a) Four transmitting plates, (b) Five receiving plates, (c) Transmitter and receiver connections to the link and a highlight for the different grounds.

A. COMMON PLATE

On the receiver side, a fifth plate is added in the middle of the matrix to automate the comparators' threshold as shown in Figure 1(b). The signal received on all plates is related to the impedance seen while propagating through skin; hence, the received signal will vary on each plate depending on its distance from the transmitting plate. The position of the 5th plate allows it to receive a signal smaller than the

overlapping intended plate and larger than the rest of the plates due to the smaller distance between itself and the transmitting plate.

B. DIFFERENT GROUNDS

When the system is implanted inside the body, the transmitter and the receiver will each be powered from a different power supply, which means that the transmitter ground will be floating compared to that of the receiver [28], as shown in Figure 1(c). The voltage at the front-end will risk being outside the operating region of the receiver or might even be oscillating. One solution for this drawback is to introduce a resistor network (voltage divider) at the front-end of the receiver, which acts as a differentiator and will eliminate the grounding difference.

III. SKIN IMPEDANCE MEASUREMENT

The impedance is measured using the Agilent impedance analyzer 4294A with different plate sizes. The equation illustrating the geometry to the impedance is extracted, and curve fitting is used. The measurements were split into two types, an overlapping plates measurement and a cross plates measurement, which are elaborated upon in the next sections.

A. OVERLAPPING MEASUREMENT

The overlapping measurement setup is defined by putting the plates with the same size each on one side of the skin while all of their area is overlapping. Figure 2(a) shows the link's geometry used to sample the frequency dependent impedance of in vivo human skin depending on the plate's area. Four square plates were chosen with widths of 5, 10, 15 and 19 mm. The plate of 19 mm sides is the largest one measured due to size limitations while doing in vivo measurements on human cheek skin. The thickness of the skin is estimated to be 4 mm and is not varied throughout the measurements.

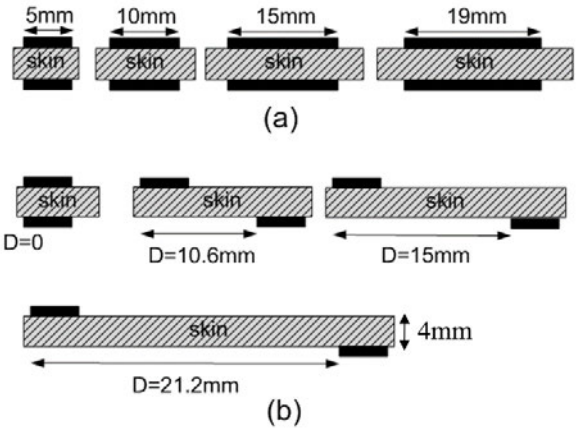

FIGURE 2. Measurement setup for (a) Overlapping plates and (b) Cross plates.

The measured skin impedance (Z) is

$$Z = \frac{\rho L}{A} \tag{1}$$

where ρ is the impedance density, which will be computed, A is the area of the plates and L is the thickness of the skin. In this analysis, ρ should be extracted from the measurements by applying $\rho = ZA/L$, derived from equation (1).

The maximum theoretical misalignment without rotation is when a transmission plate's position is in the middle of two receiving plates. In this position, the received signals on both plates are equal; hence, the signal will not be recovered correctly. If the transmitter is rotated on top of the receiver, the top-level architecture should detect this rotation and calibrate the system accordingly, an enhancement that will be included in future work. The fifth plate's utility is to automate the detection threshold, with the accompanying tradeoff of losing some precision due to the square root nature of the impedance, setting the threshold slightly higher than the middle of the difference of the signals received. These facts are demonstrated in Section III.

B. EXTERNAL CAPACITOR

The signal is applied to one plate on the transmitter, while five plates receive the signal on the receiver, which will be absorbed by five channels. The capacitance formed by the insulation layer is critical for the transmitting plate and is required to be five times greater than that on the receiving plates. We demonstrate in Section III why a small plate area is preferable, which will make it harder to maintain a large capacitance on the transmitter side, especially when the required insulation layer becomes smaller (in the micrometer range); it will become extremely fragile and could wear off quickly. Including a large on-chip capacitor would solve the problem and would maintain the functionality of the insulation layer, which is to block DC current from the transmitter. This method will allow us to use only one capacitor for all the channels since only one channel is transmitting at a time; the capacitor will be switched from channel to channel using a multiplexer.

The current will propagate throughout the medium, and the impedance can be approximated by equation (1). The measurements were sensitive to skin density.

C. CROSS MEASUREMENTS

The cross measurement consists of fixing the top plate and moving the bottom one while measuring the impedance on multiple positions. Figure 2(b) shows the setup used. The $(5\ \text{mm})^2$ plate size is chosen because it provides reasonably high impedance.

The plate separation d is taken to be 0, 10.6, 15 and 21.2 mm, which are the maximum separations due to the spatial limitations of human cheek skin. This measurement is proportional to the following equation:

$$Z = \frac{\rho\sqrt{d^2 + L^2}}{A} \tag{2}$$

Equation (2) is derived using the Pythagorean theorem, where d is the distance that separates the plates horizontally and ρ, used in equation (2), was extracted in the previous

section. The distance between all plates to the common plate is $\frac{15\sqrt{2}}{2}$ mm. The impedances seen at 10 MHz are 190 Ω for the 1st channel, 750 Ω for the 2nd and 3rd channels, 1040 Ω for the 4th channel (the inaccurate fitting below 10 MHz is not critical because the signal will be filtered by the external capacitor below this frequency) and 550 Ω for the common channel (5th channel).

D. SKIN ELECTRICAL MODEL

The skin electrical model is derived in [29] and is elaborated on in [30]. The model is defined as a capacitor in parallel with a resistor (equation (3)), then in series with another resistor. This model follows the in vivo human skin impedance behavior where the impedance is inversely proportional to the frequency, as shown in equation (4).

$$Z_{model} = R_s + (R_p || \frac{1}{jwC}) \tag{3}$$

$$Z_{model} = R_s + (R_p || \frac{1}{jwCR_p + 1}) \tag{4}$$

where Z_{model} is the modeled impedance of the skin, R_s is the resistance in series, R_p is the resistance in parallel with C, the capacitance, and ω is the angular frequency. Figure 3 displays the impedance variation along with the electrical model curves used to fit them. The results of equation (1) using the four square plates are shown in Figure 3(a) and those of equation (3) are depicted in Figure 3(b). The values of the electrical components are shown in Table 1 and are computed using equations (5) through (9).

$$Z_a = \frac{\rho\sqrt{d_a^2 + L^2}}{A} = (R_{1s} + \frac{R_{1p}}{jwC_1R_{1p} + 1}) \tag{5}$$

$$Z_b = \frac{\rho\sqrt{d_b^2 + L^2}}{A} = (KR_{1s} + \frac{R_{1p}}{jwC_1R_{1p} + 1}) \tag{6}$$

where

$$K = \frac{\sqrt{d_b^2 + L^2}}{\sqrt{d_a^2 + L^2}} \tag{7}$$

$$Z_b = (R_{2s} + \frac{R_{2p}}{jwC_2R_{2p} + 1}) \tag{8}$$

$$R_{2s} = KR_{1s}; \quad R_{2p} = KR_{1p}; \; C_2 = \frac{C_1}{K} \tag{9}$$

where Z_a is the impedance seen between a certain separation of the plates called d_a and Z_b is the impedance seen between another separation of the plates called d_b, which can be computed by Z_a and the parameters presented in Table 1.

IV. PULSE POSITION MODULATION ANALYSIS

In this section, the downlink receiver front-end will be analyzed. Important parameters that link the signal level of every channel and the signal difference between the channels will be discussed; then, the operating frequency will be computed, and the link capacity will be derived.

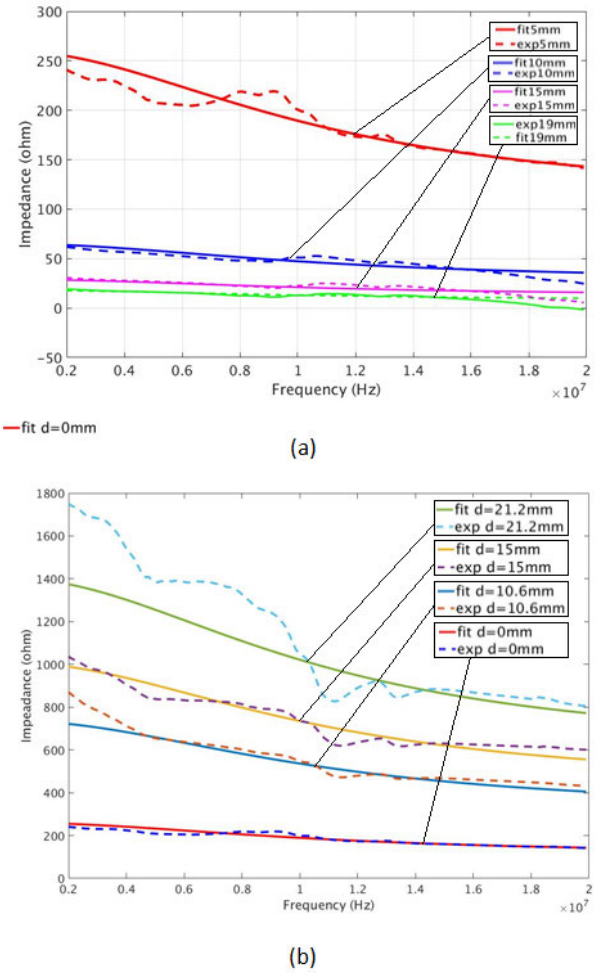

FIGURE 3. Impedance experimental measurement and fitting of (a) Overlapping plates, (b) Cross plates.

TABLE 1. Electrical model component values.

	R_s (Ω)	R_p (Ω)	C (F)	K
Channel 1	110	150	$2*10^{-10}$	1
Channel 2&3	427	582	$0.515*10^{-10}$	3.88
Channel 4	593	808	$0.37*10^{-10}$	5.393
Channel 5	311	425	$0.7*10^{-10}$	2.832

A. VOLTAGE TRANSFER

The voltage transfer function in Figure 4 for one channel can be obtained by equation (10), which illustrates the dependence of the output and input voltages on R and Z (where R is the resistance value in the front-end voltage divider and Z is the impedance of skin in series with front-end capacitor of the channel) shown in Figure 5.

$$\frac{Vout}{Vin} = \frac{R}{2Z + R} \tag{10}$$

To obtain a good voltage transfer ratio, R in equation (10) is required to be much greater than Z, as shown in Figure 5.

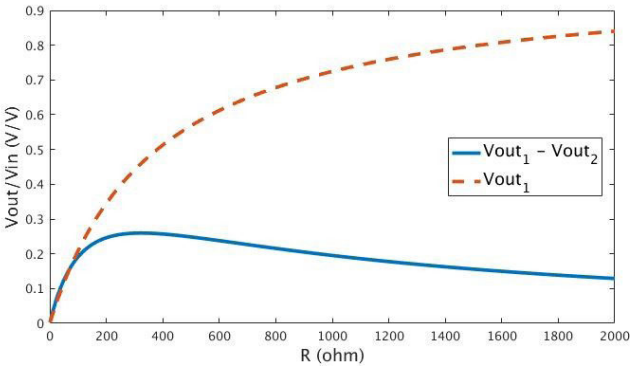

FIGURE 4. Voltage transfer function and voltage difference between channels.

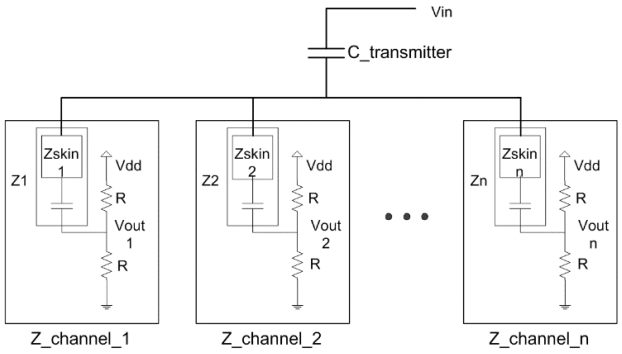

FIGURE 5. Resistor network (channel voltage divider).

B. CHANNEL INTERFERENCE

In this section, two channel outputs will be compared, where the first output "*Vout1*" is the direct facing channel and the second channel output "*Vout2*" is varying as a function of "*d*," the separation between the plates. The frequency is considered high enough to omit the capacitance in the equation:

$$Vout1 - Vout2 = \left(\frac{R}{Z_0 + R} + \frac{R}{Z_d + R}\right) Vin \tag{11}$$

$$\delta Vout = \left(\frac{R}{Z_d + R})(\frac{Z_d + R}{Z_0 + R} - 1\right) Vin \tag{12}$$

$$\frac{\delta Vout}{Vin} = \frac{Z_d - Z_0}{\frac{Z_d Z_0}{R} + Z_d + Z_{0+} R} \tag{13}$$

$$\frac{\delta Vout}{\partial R} = \frac{(Z_0 - Z_d)(R^2 - Z_0 Z_d)}{\left(R^2 + (Z_0 + Z_d)\, R + Z_0 Z_d\right)^2} \tag{14}$$

where Z_0 is the impedance seen between two overlapping plates and Z_d is the impedance seen between two non-overlapping plates. Equation (12) shows the relationship of the voltage difference ($\delta Vout$) between the outputs of each channel with respect to the input voltage depending on R, as shown in Figure 5. Equation (14) is the derivative of equation (12). For finding the $\delta Vout$maximum, the value of R is found by equating equation (14) to zero. The solution is the equation (15), where $(R^2 - Z_0 Z_d) = 0$.

$$R = \sqrt{Z_0 Z_d} \tag{15}$$

Equation (15) shows the dependence of R, the resistance value of the voltage divider at the front-end of the receiver, on the square root of the skin impedance seen on the main channel multiplied by the skin impedance seen on the second-closest channel. In this system, the first channel is the couple plates 1T/1R, and the second channel is 1T/5R as shown above in Figure 1(a-b). The resistance value chosen should maximize the voltage difference between the transmitting channel and the closest interfering channel.

C. CUTOFF FREQUENCY

Since the capacitive link is a high-pass channel, the operating frequency can be computed by finding $\tau = RC$, where the cutoff frequency is equal to $(1/2\pi\tau)$; then, the following high-pass filter's equation can be concluded as (16):

$$F_c \geq \frac{1}{2\pi\ (R + Z_n)_{eq}\, C_{eq}} \tag{16}$$

where $(R + Z_n)_{eq}$ is the equivalent impedance of the voltage divider in series with the skin impedance Z_n of all the parallel channels (the impedance seen between the transmitting plate and every receiving plate, all in parallel) and C_{eq} is the equivalent capacitance of the main transmission capacitor in series with all channel capacitors in parallel. Operating at a frequency higher than the cutoff frequency allows us to neglect the front-end main capacitor and the channel capacitors impedance by considering them as shorted.

D. CAPACITY

To determine the capacity of this system, first, the SNR at the front-end of the receiver should be computed. The SNR on the downlink is formed by the signal of the first channel minus the signal of the middle channel divided by the RMS voltage noise of the first channel and the second channel plus the voltage input referred noise of the comparator.

$$SNR = \frac{\partial Vout}{Noise} \tag{17}$$

$$SNR = \frac{\frac{Z_d - Z_0}{\frac{Z_d Z_0}{R} + Z_d + Z_{0+} R} Vin}{2 * \sqrt{4KTR} + Ncomparator} \tag{18}$$

The channel capacity of this system can be computed by equations (19) and (20).

$$C_{ty} = 2 * B \log_2 (1 + SNR) \tag{19}$$

$$C_{ty} = 2 * B \log_2 \left(1 + \frac{\frac{Z_d - Z_0}{\frac{Z_d Z_0}{R} + Z_0 + Z_d + R} Vin}{2 * \sqrt{4KTR} + Ncomparator}\right) \tag{20}$$

where B is the channel bandwidth. The bandwidth is defined mainly by the cutoff frequency of equation (16) for the lower

bound and the cutoff frequency of the front-end comparator for the upper bound.

V. TRANSCEIVER DESIGN

Figure 6(a) shows the transceiver block diagram. It consists of a downlink transmitter and receiver using spatial pulse position modulation and an uplink transmitter and receiver using Load-shift keying modulation. The uplink transmitter is embedded in the downlink receiver specifically in the resistor network (Figure 6(b)), which forms the load that will be varied. The uplink receiver is embedded in the downlink transmitter through the current sensor block, which will be elaborated on in Section *B* and which will sense the load value and extract the bits.

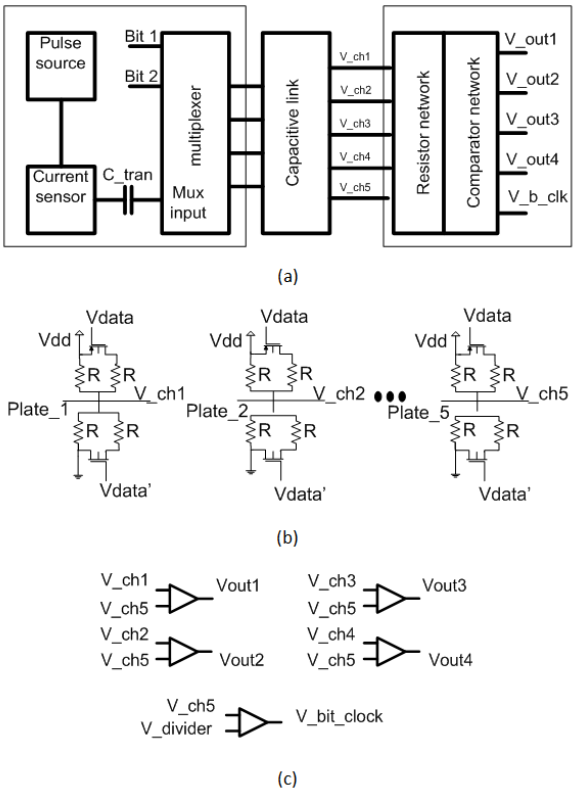

FIGURE 6. (a) Transceiver block diagram, (b) Downlink receiver: resistor network where each of its inputs is connected to the capacitive interface, (c) Comparator network connected to the resistor network.

A. SPATIAL PULSE POSITION MODULATION

The downlink in this system uses spatial pulse position modulation to transmit data from the outside to the implant. Sections *1* and *2* below illustrate the design of the transmitter and the receiver, while Section *3* elaborates on the simulation results.

1) *Transmitter:* The downlink transmitter is formed by a pulse generator, a current mirror (which is used by the uplink), a capacitor and a multiplexer. The pulse generator is connected to the current sensing circuit, then to a capacitor followed by the multiplexer. This forms a single transmitting path that can be connected to different channels one at a time. The capacitance used for transmission is chosen to be 5 times greater than the capacitance used for the reception, so it will be able to drive all 5 channels.
2) *Receiver:* The downlink receiver is formed by multiple voltage dividers, each connected to a channel as shown in Figure 6(b), followed by a comparator. Four two-input comparators compare the voltage output of every resistor network with the voltage output of the common channel. An additional comparator is added to extract the positive bit cycle of every transmitted bit where one end is connected to the fifth network and the other is connected to a voltage divider set 10% higher. In this way, the fifth comparator detects if a pulse is transmitted, while the other 4 comparators detect on which channel the pulse is transmitted (Figure 6(c)).
3) *Simulation:* Figure 7(a) shows the different voltages at the receiver resistor network. Each curve represents the signal received from a channel, where V1 is the output of the main receiving plate of the model and V5 is the output of the common plate, which is closest in distance to the main plate, followed V2 and V3, symmetrical to the main plates, and V4, the furthest away. There is a voltage difference of 97 mV between the main and 5th channel and an 85 mV difference between the 5th and the 2nd and 3rd channels. These signals are fed to comparators where each of the four channels will be compared with the common channel. An additional comparator is added that compares the common channel with a voltage divider set to 1/10 higher than the resistor network at rest, or in other words, the resistor connected to Vdd is R, and the resistor connected to ground is R+R/10. This comparator will trigger when a bit is sensed and will provide a clock that indicates when a bit is valid, as shown in Figure 6(b and c). Figure 7(b) shows the input pulse voltage Vin, the comparator output voltage on channels 1, 2, 3, and 4 and the bit clock.

B. LOAD-SHIFT KEYING

Load-shift keying is a modulation scheme that utilizes load variation to transmit data by directing a signal (electric or. magnetic) towards the load and sensing the power dissipated or reflected in the load. Each number of bits (NOB) is associated with a certain load, and the number of loads (NOL) required to transmit a number of bits at once is shown by equation (21)

$$NOL = 2^{NOB} \tag{21}$$

In this work, only one bit is transmitted at a time, which implies that only two load values are used. The signal that will be analyzed to differentiate between loads is the current variation. The current will vary depending on the impedance seen starting from the capacitive link until the voltage divider.

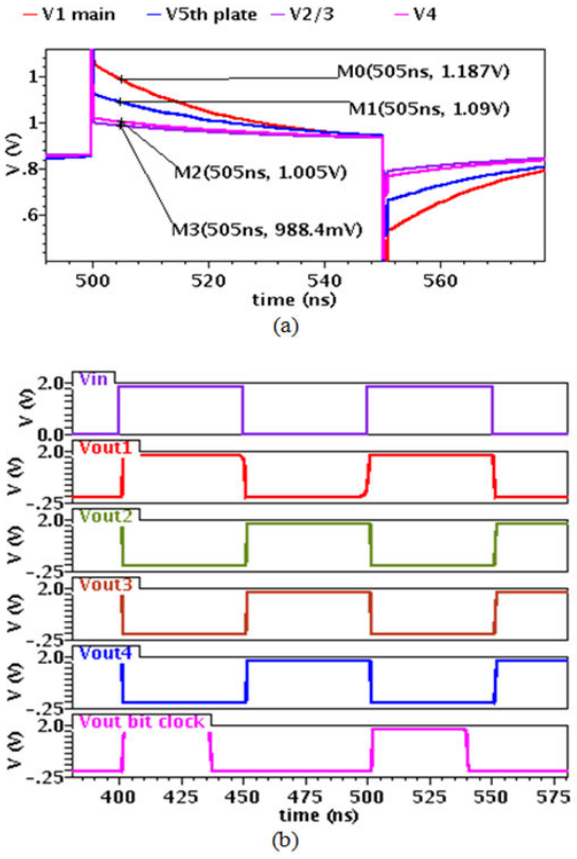

FIGURE 7. Simulation output of the downlink receiver. (a) Resistor network, (b) Comparator network (seen in Figure 6).

The current variation is computed by equation (22):

$$i = \frac{Vin}{Z_{C_{transmitter}} + \left(Z_{channel_1} + \cdots + Z_{channel_n}\right)} \tag{22}$$

$$Z_{channel_n} = Z_n + \frac{R}{2} \tag{23}$$

Considering one channel, when the load R varies, the current will vary according to equation (24):

$$\frac{\partial i}{\partial R} = \frac{Vin}{2(Z_n + (R||R) + Z_{C_{transmitter}})^2} \tag{24}$$

Equation (24) is the derivative of equation (22) with respect to R. It shows that the smaller R is, the greater the current variation.

An M-array load modulation can be applied in this case where multiple bits can be transmitted in one current amplitude level. The R values for this M-array system should be chosen and spaced apart depending on equation (24) while maintaining a reliable signal reception on the downlink. The same analysis applies to the multiple channel system where, to maintain symmetry, the load R should be varied across all channels. The current will be multiplied by n (the number of channels), leading to n times current gain. In this work, binary LSK is implemented for simplicity. M-array modulation will be the subject of a future study. The uplink in this system uses the load-shift keying modulation to transmit data from the implant to the external system. Next, Sections *1* and *2* illustrate the design of the current mirror and the load switching topology, respectively, while Section *3* elaborates on the simulation results.

1) *Current Mirror:* The current mirror used to sense the current at the uplink receiver is illustrated in Figure 8. V_in_pulse is the downlink transmitted signal where it propagates through M7 and C_trans to reach the input of the multiplexer presented in Figure 6(a). The current mirror and the following blocks (current/voltage amplifier, integrator and inverters) should be deactivated during the positive cycle of the transmitted signal. Therefore, transistors M4 and M5 are the heart of the mirror where the current going through M4 is mirrored to M5, and transistors M1 and M2 are used as switches to deactivate the current mirror during the positive cycle of the pulse. These two transistors are necessary to eliminate the effect of transistor M7 during both cycles and to provide a clean reading of the current syncing from the capacitor into the source. Transistor M3 is used to turn off the current mirror during the positive cycle by pulling the gate of M4 and M5 to ground and then switched out during the negative cycle where the current is evaluated (uplink receiving). Transistors M6 and M5 are used to form a current/voltage amplifier. The voltage between M6 and M5 is then fed to an integrator where its output is connected to two inverters each with a different threshold, as shown in Figure 8. The inverter 1 threshold is set between the maximum and minimum integrator outputs to detect the value of the transmitted bit (data input of the following flipflop), and the inverter 2 threshold is set below the voltage of both bits at the output of the integrator to detect the presence of bit transmission (clock input of the following flipflop). After that, the output of inverter 2 is used as the clock to the flip-flop, the input of which is the output of inverter 1.

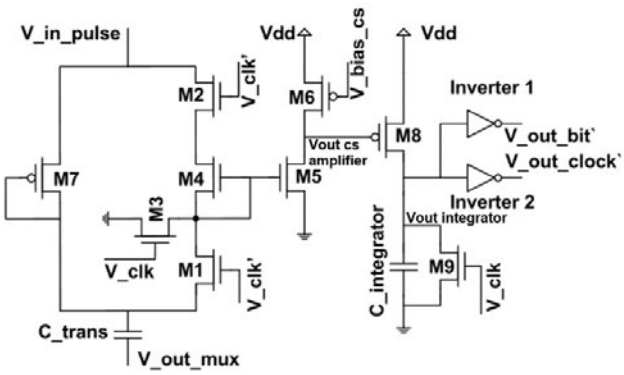

FIGURE 8. Elaboration of the current sensor block in Figure 6, which is the core of the uplink receiver implementing Load-shift keying. This figure contains the current mirror, the common source amplifier, the integrator and the inverters.

2) *Load Switching:* At the downlink receiver, the loads used to build the voltage divider are switched as a function of the bit to be transmitted. The bit is directly connected to all transistors of the voltage dividers, which will switch the R loads in and out in parallel with the already established voltage divider, which will divide the impedance in half. These voltage dividers are chosen to fit the maximum voltage of $Vout_1$ shown in Figures 4 and 5.
3) *Simulation:* Figure 9 shows the simulation result of the load-shift-keying receiver, where Vin is the input bit at the resistor network, which switches resistors in and out. Vout common source amplifier ($Vout_{cs}$) is used to amplify the output of the current mirror and convert it to a voltage; Vout integrator is the output of the integrator whose input is connected to the output of the common source amplifier; Vout_clock' is the output of inverter 2 which detects the presence of a bit; and Vout_bit' is the output of inverter 1, which detects the bit value. Note that the clock' and bit' variables have low logic values.

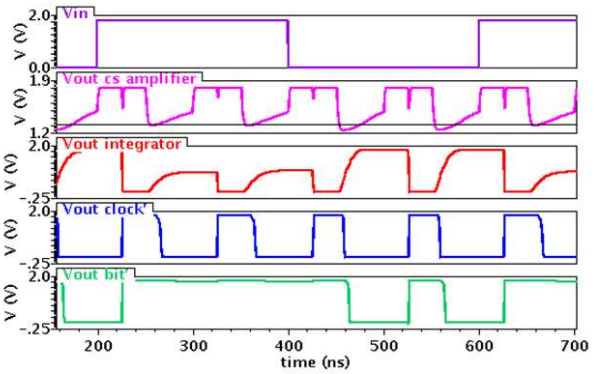

FIGURE 9. Simulation results of the current sensing block of the uplink receiver shown in Figure 8.

VI. DISCUSSION AND COMPARISON

The system is mainly dependent on the parameter discussed above; for a good voltage transfer ratio shown in equation (10), the R value in the resistor network is preferred to be as large as possible. This contradicts with the result of equation (11), where the value of R should be set as in equation (15) for a maximum voltage difference between the channels. Equation (16) sets the lower bound for the bandwidth in equation (20) for the capacity; hence, the higher the R is, the larger the bandwidth and the greater the channel capacity. The SNR is directly related to equations (10) and (11). The noise at the front-end of the receiver is proportional to R but does not affect the SNR as much as equations (10) and (11) and can be neglected. The upper bound for the bandwidth of this system is the cutoff frequency of the comparator, which is technology- and design-dependent. The trade-off presented by adding the Load-shift keying uplink is shown in equations (22) and (24), where the current value is inversely proportional to the value of R. The base-band modulation schemes used are the most compatible and simple to implement with this type of data link, and of course consume less power than other pass band modulation schemes.

The human skin impedance varies between different persons. The system can be adjusted to work for individual cases. A general model can be implemented with safe margins to compensate for human skin impedance variation while trading off performance and power consumption. This will be elaborated in future work.

As for power consumption, there is a great trade-off where the lower the R value, the higher the power consumption of the resistor network and vice-versa, but the smaller the signal, which requires a more power-demanding comparator to extract the bits. The power consumption of the comparators used in this system is high and can be easily improved by using low power comparator topologies due to the relaxed condition for the comparison and by doing a trade-off for the signal quality to reach a reasonably acceptable bit error rate of approximately 10^{-6}. The robustness of this system lies in the compatibility of the system with the Viterbi decoder, which allows an easy implementation for a convolutional code with R = 1/2.

The comparison of this system with other uni- or bi- directional capacitive, inductive and optical data telemetries is shown in Table 2. All existing capacitive-link based systems employ a unidirectional telemetry. Thus, no uplink modulation exists. The highest data rate of 200 Mb/s is achieved by [20] for a downlink capacitive data link system with simulation, while considering the skin model as a pure capacitor and ignoring the issue of different supply grounds. The capacitive link has an advantage over the inductive link in terms of bandwidth, as shown in Table 2.

TABLE 2. Comparison of main capacitive (Cap.), optical (Opt.) and inductive (ind.)-based telemetries.

Ref.	Downlink	Uplink	Bit rate	Medium	Power
Cap.					
[19]	SPI	N/A[1]	N/A	Chicken	N/A
[20]	SPPM	N/A[1]	200 Mb/s[2]	Simulation	3.75 pJ/bit
[21]	FSK	N/A[1]	N/A	Air	6 mW
[23]	SCPM	N/A[1]	20 Mb/s[2]	Sheep	150 pJ/bit
[30]	BPSK	N/A[1]	N/A	Chicken	N/A
Ind.					
[31]	FSK	LSK	1 kb/s[3]	N/A[4]	N/A
[32]	ASK	LSK	18.7 kb/s[3]	N/A[4]	N/A
[33]	N/A	LSK	20 kb/s[3]	N/A[4]	N/A
[34]	PSK	LSK	100 kb/s[3]	Simulation	N/A
Opt.					
[9]	PC	N/A[1]	128 Mb/s	Diffuser	4.6mW
[10]	VCSEL	VCSEL	1, 10^2 Mb/s	Porc	32 pJ/bit
[11]	N/A[1]	VCSEL	100 Mb/s[3]	Sheep	2.1 mW
[12]	PPM	N/A[1]	135 Mb/s[2]	Air	10 pJ/bit
This work	SPPM	LSK	20^2, 10^3 Mb/s	Human skin model	120 pJ/bit

[1]These telemetries are unidirectional, and they do not have an uplink modulation. [2]Downlink bit-rate. [3]Uplink bit-rate. [4]Medium is not mentioned.

VII. CONCLUSION

In this paper, a capacitive data link transceiver is implemented using spatial pulse position modulation for the downlink and load-shift keying for the uplink. A 20 Mb/s data rate is achieved on the uplink and 10 Mb/s on the downlink with a 10 MHz clock frequency. An in vivo human skin model for a 5 mm by 5 mm plate size with 21.2 mm separation is extracted, and the transmission capacity's equation of the channel is computed using the equations for the analysis of the system. This work shows that bidirectional communication using the capacitive link is possible while maintaining a high-data rate with minor trade-offs. Future work will concentrate on reducing the power consumption and increasing the data rate as much as possible while implementing an integrated version of the transceiver using 180 nm CMOS technology.

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