A Fully Integrated Low-Power Hall-Based Isolation Amplifier With IMR Greater Than 120 dB

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***Abstract*— A CMOS Hall-based fully integrated isolation amplifier for differential voltage sensing is presented in this work. The design is fabricated in a 0.35 μm CMOS process in which the high voltage (HV) side of the amplifier contains a coil driver while the low voltage (LV) side includes a Hall-effect sensor, low-noise amplifier, programmable-gain amplifier, filter, and chopper switches. Another Hall sensor performs the digital isolation using the on-off keying (OOK) technique for clock recovery. The introduced prototype achieves above 120 dB of isolation mode rejection (IMR) at 60 Hz and operates at a continuous isolation working voltage of 0.6 kV. It has also a maximum nonlinearity of 0.64 %, an input-referred offset of 1 mV, a 40 dB full-scale signal-to-noise ratio over a 40 kHz bandwidth, and a spurious-free dynamic range of 64 dB. The silicon area for each of the two separate dices employed for the HV and LV side of the isolation amplifier is 1 mm^2 with a power consumption of 7.6 mW and 9.9 mW respectively. The achieved miniaturized size of the isolation components, as well as their significantly low-power consumption, ensure the suitability of the proposed isolation amplifier for multi-channel readout circuit applications.**

***Index Terms*— Isolation amplifier, voltage sensing, current sensing, galvanic isolation, sensor interface, chopper amplifier, digital isolator, integrated spiral coil, CMOS Hall sensor.**

I. Introduction

SENSOR interfaces are elemental in several applications including robotic, industrial control, and aerospace where delivering stable high power to sensors and actuators is required. Accordingly, voltages and currents delivered to these loads are monitored for further processing [1]. The environmental working conditions of these actuators enforce sensor interfaces to satisfy certain safety insulation standards such as surge withstand voltage and continuous isolation working voltage V_{iso} through their operating lifetime [2].

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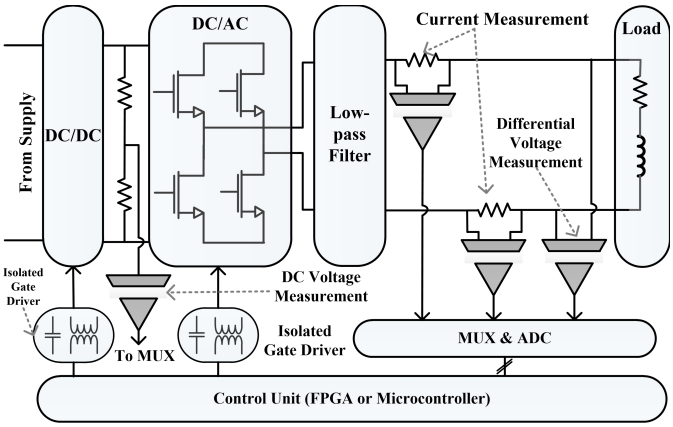

Fig. 1. Block diagram of a sensor interface unit.

A typical sensor interface unit, as shown in Fig. 1, incorporates numbers of isolated voltage and current reading units. One unit could be employed to read the DC input level of the rectifier bridge and others to monitor the delivered power or detect a fault condition. One of the viable current reading techniques is based on combining a Hall-effect sensor with a current transformer (CT) as it can detect both DC and AC signals [3]. The air-gapped ferrite of the CT amplifies the magnetic field resulting from the current line and compensates for the low sensitivity of the Hall sensors. However, when multiple sensors or actuators are being monitored, packaging of the sensor interface, due to the large footprint of the CT Hall-based sensing, would not be applicable. There exist current transducers that are fully integrated and use no C-shape toroid for low current applications [3]. CMOS or BiCMOS current transducers suffer from low resolution while anisotropic magnetoresistance (AMR) and giant magnetoresistor (GMR) transducers are utilized for precision current measurement. Nevertheless, regular foundries do not support deposition of magnetic material (e.g. ferrite) employed in magneto resistors which prevent them from being integrated along with amplifiers and filters. Finally, to protect those sensors against electromagnetic interference (EMI), they must be shielded and placed away from high current bus lines and devices generating magnetic fields (i.e. motor).

Shunt-based current sensing has features including small footprint, rapid response, and DC monitoring [3]. To unify power monitoring designs, a programmable isolation amplifier can be employed for differential voltage and shunt-based current sensing. Isolation amplifiers that are based on analog to

digital converters (ADC) transmit digitized data across the isolation medium, are very advantageous in terms of signal resolution and bandwidth [4]. However, placing an ADC on the HV side increases the amplifier consumption and is not suitable for multi-channel voltage and current sensing applications. For instance, the ADC of Ma, *et al.* [4] and ACPL-790X [5] consume 40 and 49.5 mW, respectively. In the non-ADC type of isolation amplifiers (IA), analog data are transmitted over the galvanic medium either directly like optocouplers or after modulation. Other than simple design approaches, analog IAs utilizing optocouplers have outstanding performance in terms of linearity, noise, and drift performance [6]. However, there are concerns regarding their effective lifetime due to electrical and thermal stresses [7]. In addition, the current transfer ratio variation of optocouplers [8] requires frequent calibration during their lifetime, which may not be acceptable in many applications. Also, optocouplers are not CMOS integrable as they employ GaAs substrate. As a result, every channel of an IA requires a dedicated optocoupler dice adding to the total dies in a package and increasing the manufacturing cost. The transformer-based approach employs modulation to transmit DC signal [9] where a good signal-to-noise (SNR) is obtained at a price of very high wattage and bulky designs as the transformer must be sized to achieve a high quality factor. This makes them not suitable for multi-channel sensor interfaces.

Recently our team has designed few versions of the sensor-based isolation voltage amplifier [10]–[12]. In [10], a MAGFET is used as a signal receiver. Despite the design simplicity in the receiver circuitry, MAGFETs suffer from a lower limit of detection than Hall sensors [13]. On the other hand, a CMOS Hall effect sensor in [11] receives the signal-dependent magnetic field ranging from DC to the bandwidth of interest. Without modulation, the device is sensitive to external DC fields, and constant calibration is required in mobile applications. Moreover, the sensor could receive the low-frequency magnetic field noise of industrial motors. In [12], minimal integration with off-chip components was used to achieve the modulation technique. However, a high external DC field could saturate the Hall amplifiers. Moreover, the high inductance of the employed magnetic coil would prevent modulation at higher frequencies and requires a higher filter order. In this paper, a fully integrated amplifier is proposed, overcoming the previous drawbacks which allow the approach to be suitable for dense integration.

This paper presents an IA based on an on-chip spiral coil and a CMOS Hall sensor which is suitable for amplifying shunt-based current and differential voltage sensing. The remaining of this paper is organized as follows: Section II describes the overall system architecture including integrated spiral coils, optimization of the cross-shaped Hall-effect sensor, and the clock recovery. The measurement results are reported in Section III, and conclusion remarks appear in Section IV.

II. Design and Implementation

A. System Architecture

Fig. 2(a) illustrates the proposed system in package (SiP) solution that includes two dices where one integrates a driver circuit and the other a Hall-effect sensor with corresponding amplification stages. On the HV dice, the chopper switches formed by transmission gates chop the input signal (V_{in-IA}) at 2 MHz and send it to the mid-band region. Then, an amplifier drives the integrated spiral coils formed by intermetal layers on the LV dice. The Hall sensor located under the center of the coil receives the transmitted magnetic field and generates a deflected voltage. Next, the sensed voltage goes through amplification stages starting from the low noise amplifier (LNA). The amplified DC offset and flicker noise of the sensor are removed by the passive high-pass filter (HPF) with a 500 kHz cutoff frequency, and a programmable gain amplifier (PGA) tunes the signal to be suitable for the desired output dynamic range. Then, a chopper demodulator brings the amplified signal back to the baseband region and a second-order anti-aliasing filter (AAF) attenuates mirrored spectral components and switching overshoots. Finally, a clock recovery circuit using a Hall-effect sensor forms a digital isolator with on-off keying (OOK) modulator to transmit the clocking signal generated on the HV side to the LV side.

The frequency spectrum of the IA at different nodes along the analog modulation/demodulation chain is demonstrated in Fig. 2(b). The modulation of node 2 and demodulation of node 8 allow the transmission of the baseband input signal without adding the DC offset and flicker noise of the amplifier's chain including the coil driver, Hall sensor, LNA, and PGA as shown in Fig. 2(b), nodes 3-5. The high pass filtering at node 6 removes the DC offset and weakens the amplified $1/f$ noise of the sensor and the LNA to protect the amplifier from saturation. Additionally, the chopper technique and the high-pass filtering, eliminate inherent offset drift of the Hall sensors and the DC signal generated by the geomagnetic field.

B. Driver Circuit

Fig. 3 demonstrates the schematic of the coil driver. A divider with $R_D = 250k$ divides the input differential voltage of the IA (V_{in-IA}) to extend the amplifier's input dynamic range. For the same reason, after the chopper modulator, a rail-to-rail architecture is chosen for the input differential pairs of the driver amplifiers. In parallel, as the system overall SNR in this Hall-based isolated voltage sensing is proportional to the strength of the generated magnetic field, the on-chip coil must be sourced with sufficient current to fulfill the required SNR of the application. As a result, the off-chip gain resistor $\left(R_g\right)$ adjusts the driver's gain from -20 to 4.44 dB to deliver the required coil current for different ranges of V_{in-IA}. Moreover, to reduce the current consumption on the HV side, a class AB output stage, that conducts only a half-wave signal, is employed for the output stage. The driver circuit has an input-referred noise of 25 nV/$\sqrt{\text{Hz}}$ and a gain-bandwidth product of 50 MHz. 474 kΩ is the differential input impedance resulting from the combined divider, chopper modulator, and drivers which is suitable for shunt resistor current sensing.

C. Integrated Spiral Coils

Using the integrated coil approach, intermetal filling of the CMOS process behaves as an isolation barrier (Fig. 4). In the employed 0.35 μm technology, the spacing between metal layers is SiO_2 and spacing between consecutive metal

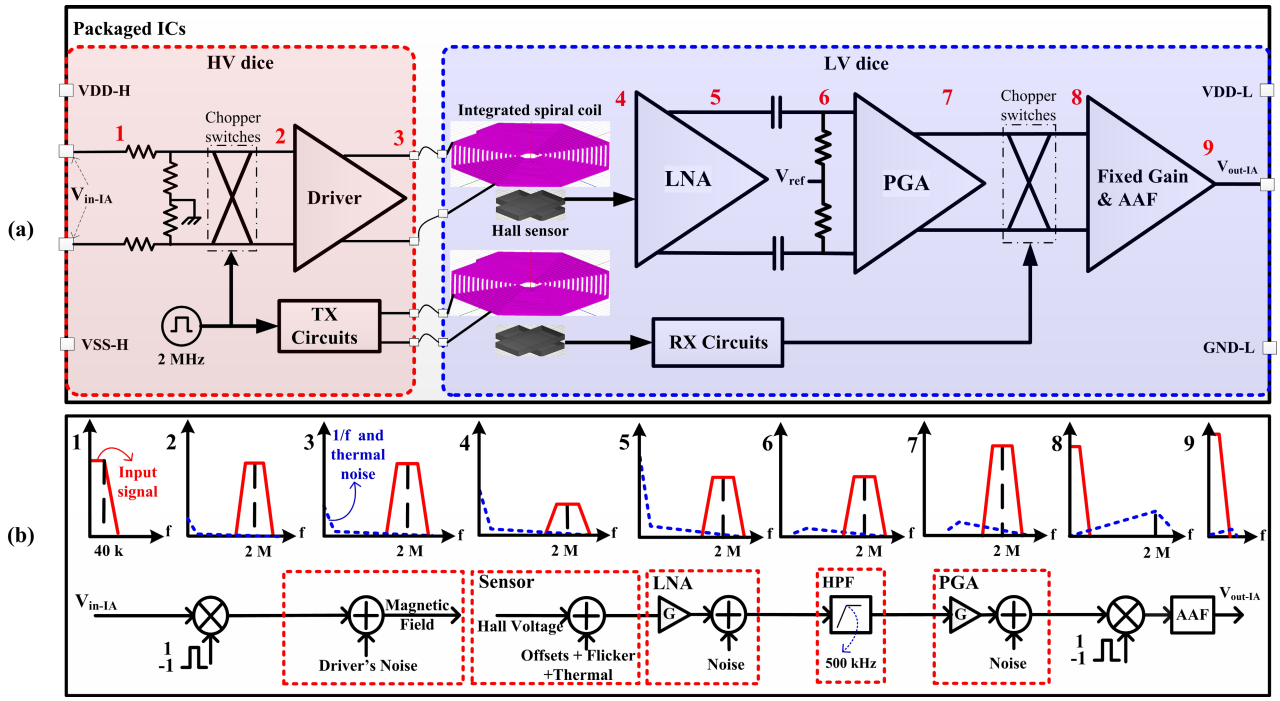

Fig. 2. (a) Architecture of the proposed isolation amplifier, and (b) signal spectrum of the structure presented at different nodes.

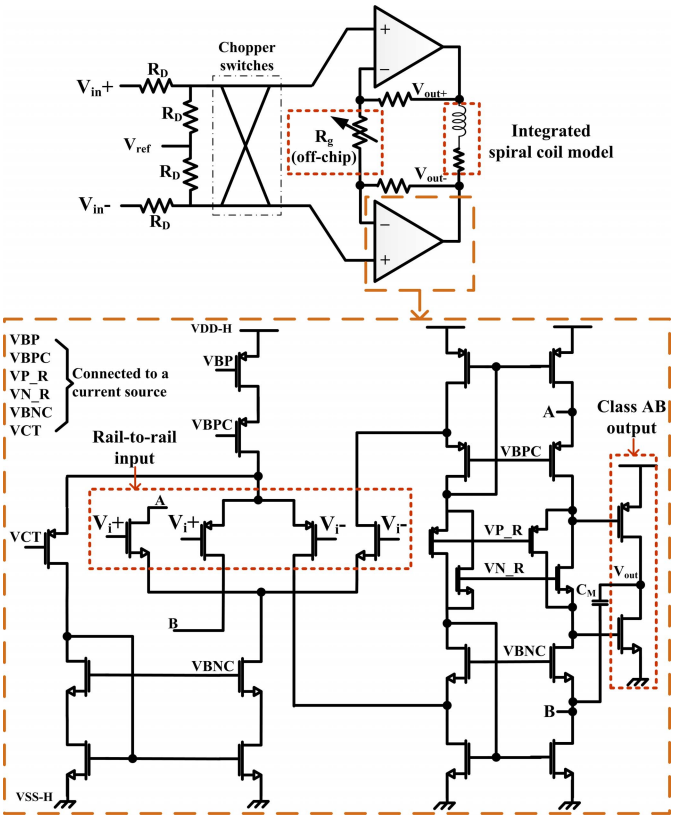

Fig. 3. Schematic of the coil driver.

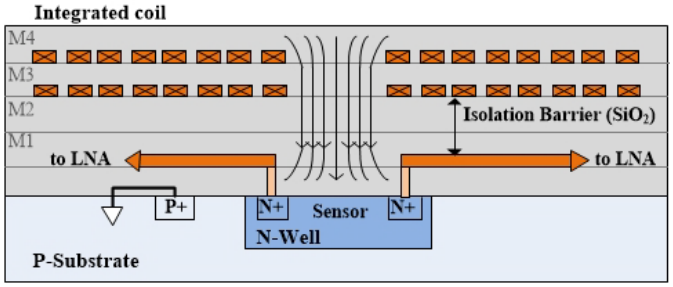

Fig. 4. Cross sectional view of the integrated coil and CMOS Hall sensor.

layers is one micron. Having process CMOS oxide as an isolation barrier is a common industrial practice (e.g. Texas Instrument ISO72xx [14]). Based on the oxide deterioration profile reported in [15], one micron of oxide has an isolation breakdown voltage of 0.45 MV/mm. Hence, having 2 μm of oxide, theoretical 900 V of isolation working voltage (V_{iso}) is expected. Further increase of V_{iso} can be obtained using a smaller process node (e.g. 65nm) with a greater number of metal layers and consequently a thicker galvanic barrier.

Creating a magnetic field in the Hall-based isolation amplifier involves several challenges. First, the amplifier's signal quality is directly proportional to the field, so an adequate magnetic field is required to achieve a reasonable SNR. Second, the coil behaves like a series of resistive-inductive loads (i.e. a low-pass filter); therefore, to avoid attenuating the carrier signal, the magnetic coil must have a low inductance. Finally, the coil must have a small footprint to lower the packaging size, simplify packaging complexity, and reduce cost. Therefore, as visualized in Fig. 4, a double layer of integrated hexagonal spiral coil is fabricated on top of the Hall plate with specifications listed in Table I. To determine the field strength of the coil, an ANSYS simulation is performed for a peak current of 2.5 mA, showing that the coil can generate a field of 1.25 mT according to the result of Fig. 5(a).

The other requirement from the Hall-based isolation amplifier is the ability to perform multi-channel isolated reading by

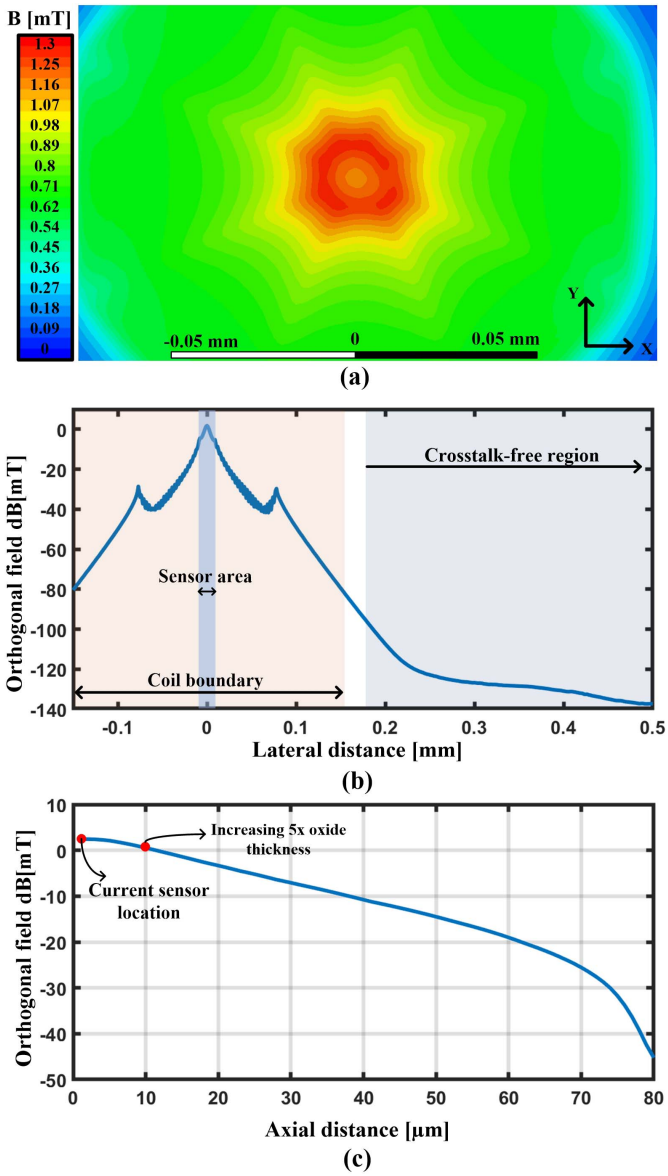

Fig. 5. (a) ANSYS simulation showing magnetic field of the integrated spiral coil for 2.5 mA of current and at 5 μm distance, and (b) perpendicular field to the substrate area respective with lateral distance, and (c) axial field strength.

TABLE I

PARAMETERS OF THE INTEGRATED SPIRAL COILS

Parameter	Metal-3	Metal-4
Number of turns	22	15
Turn spacing (μm)	0.5	2
Wire width (μm)	2.5	2.5
Inner diameter (μm)	20	22
Current density ($\frac{\text{mA}}{\mu\text{m}}$)	1	1.5
Outer diameter (μm)	154	158

placing several dices next to each other in the same package or using multiple transmitter coils in a single dice on the LV side. To determine this capability, the integrated Hall sensors must be crosstalk-free from the neighboring coils. For a 1 Hz bandwidth and an SNR of 95 dB, to place the sensor in a crosstalk-free distance, the far-field must be 95 dB lower than the adjacent coil; consequently, as Hall plates are sensitive to perpendicular magnetic fields, simulation of the vertical field strength of the integrated coil in logarithmic scale is shown Fig. 5(b). Based on this figure, multiple transmitter coils and receiver sensors can be placed 350 μm apart from each other. Increasing oxide thickness improves the isolation property at the expance of attenuating the field strength and consequently the overall signal quality; however, as shown in Fig. 5 (c), adding a maximum possible of 8 more microns attenuates the signal by a negligible amount of 1.8 dB.

D. Sensor Implementation

The Hall sensor converts the received magnetic field to an electrical signal via the Lorentz force, so optimization toward sensitivity and minimizing the noise floor improve the overall SNR of the system. Optimal sizing of cross-shaped Hall effect sensor respective with its width (W) and length (L) has been reported by.Xu, *et al.* [16]. However, other parameters, including the contact width of the signal nodes (C_W) and the sensor area, contribute to the Hall sensitivity. The variation of the sensitivity with respect to the area is described by Crescentini, *et al.* [17]; however, based on Fig. 5(b) the vector of the generated magnetic field orthogonal to the sensor's surface attenuates when the sensor's area becomes larger than the inner diameter of the integrated coil (20 μm). Besides, reported by Xu and Pan [18], expanding sensor size, decreases the sensor's 3 dB bandwidth.

To investigate the relationship between sensitivity and contact size, a COMSOL simulation is performed using an anisotropic conductivity tensor, σ, modeled by a 3×3 matrix [19]:

$$\begin{bmatrix} \sigma_{xx} & \sigma_{xy} & \sigma_{xz} \\ \sigma_{yx} & \sigma_{yy} & \sigma_{yz} \\ \sigma_{zx} & \sigma_{zy} & \sigma_{zz} \end{bmatrix} = \begin{bmatrix} \frac{\sigma_0}{1+(R_H B\sigma_0)^2} & \frac{R_H B\sigma_0^2}{1+(R_H B\sigma_0)^2} & 0 \\ \frac{R_H B\sigma_0^2}{1+(R_H B\sigma_0)^2} & \frac{\sigma_0}{1+(R_H B\sigma_0)^2} & 0 \\ 0 & 0 & \sigma_0 \end{bmatrix} \quad (1)$$

where R_H is the Hall coefficient, σ_0 is the conductivity, and B is the magnetic field. Fig. 6 shows the COMSOL simulation of the sensor sensitivity versus contact size. This simulation is performed based on the optimum ratio of L/W using methodologies described by Xu, *et al.* [16], for W and L of 19.3 μm and 11.2 μm, respectively. The current source contact sizes are equal to W. Based on Fig. 6, minimizing C_W increases the sensor sensitivity, i.e., a wide C_W shortens the voltage equipotential line deflection over the sensing nodes leading to a lower sensitivity. As a result, a narrow C_W of 1.2 μm is employed for the sensor contacts, and the Hall plate is fabricated in N-Well with an optimum L of 19.3 μm and W of 11.2 μm. Table II summarizes the process parameters being used in the simulation.

E. Analog Receiver Circuitry

To ensure that Hall node voltages are within the input swing range of the LNA, common-mode feedback (CMFB)

TABLE II

MODEL PARAMETERS OF THE COMSOL SIMULATION BASED ON THE AVAILABLE TECHNOLOGY AND INTEGRATED SPIRAL COIL

Symbol	PARAMETER	Value
n [cm^{-3}]	Dopping Concentration	$1.28e^{17}$
I [mA]	Biasing Current	2
B [mT]	Peak Magnetic field	1.25
R_s	N-Well Sheet Resistance	1e3
t [μm]	N-Well Thickness	2
σ_0 [$\frac{S}{m}$]	Conductivity	$\frac{1}{R_S \times t}$
R_H	Hall Coefficient	$\frac{1}{n \times q}$

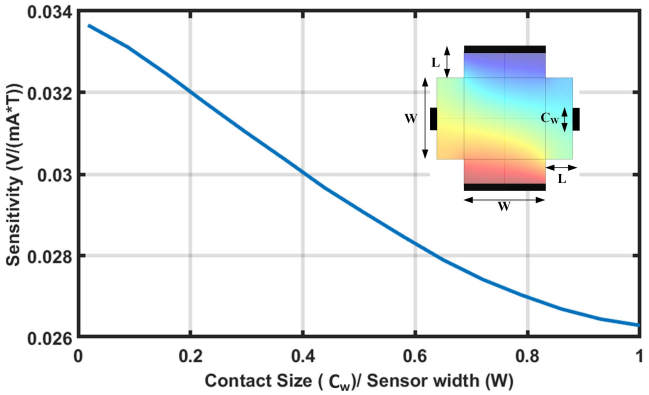

Fig. 6. COMSOL simulation of the cross-shape Hall sensor respective with various signal contact size for an optimum L/W ratio. The biasing contacts are equal to the sensor's width and located at the extremities of the arms.

is employed as shown in Fig. 7(a). Also, to avoid adding any capacitive load on the Hall signal nodes and limiting the bandwidth of the sensor, DC voltage reading of the CMFB branch is performed on the Hall current nodes.

CMOS Hall sensors have inherently a low sensitivity and a high DC offset. Hence, to optimally capture the Hall voltage induced by the generated magnetic field, the first amplifying stage must have low input-referred noise. Since the input signal of the LNA is at the modulation frequency of 2 MHz, the dominant noise of the sensor is thermal noise. Knowing that the sensor has a resistivity of 1.4 kΩ, 4.7 nV/$\sqrt{\text{Hz}}$ of thermal noise is expected from the sensor, so the amplifier must be designed to satisfy an input noise lower than the sensor's thermal noise at modulation frequency to not contaminate the received signal. Furthermore, the amplifier must have a sufficiently large bandwidth to not attenuate the received modulated signal. Considering these limits, available conventional instrumentation amplifier with triple operational amplifiers suffers from high consumption in large bandwidth. Moreover, the sensor does not have the driving capability which dictates the amplifier to have a high input impedance. This implies that the amplifiers with capacitive coupling attenuate the bandwidth spectrum of the Hall sensor. Thereafter, to satisfy the wide bandwidth as well as the high input impedance, a cross-coupled architecture is implemented as depicted in Fig. 7(b). Due to the inherent low $1/f$ noise, PMOS transistors are selected as the differential pair for the architecture, and they are sized to have an input-referred

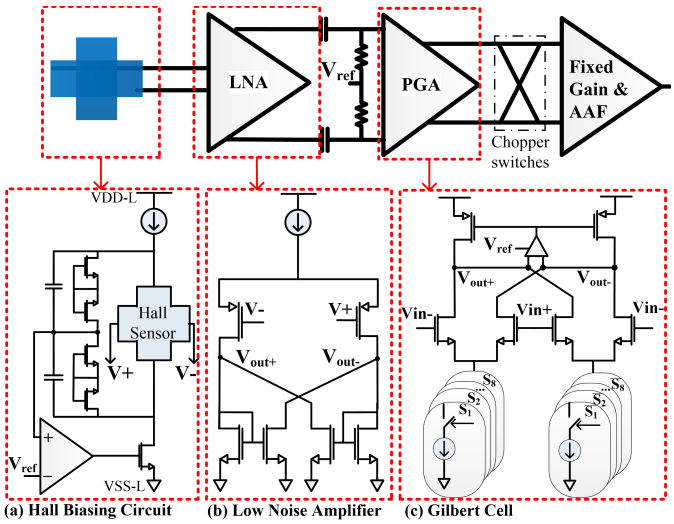

Fig. 7. (a) Biasing circuit of the Hall plate, (b) structure of the cross coupled preamplifier, and (c) topology of the integrated dB-linear PGA.

thermal noise of 3 nV/$\sqrt{\text{Hz}}$. Also, because CMOS Hall sensors are prone to high DC offset due to mask-misalignment [20], without active offset canceler circuitry, direct amplification with a high gain can saturate the amplifier. Therefore, a low gain of 26 dB is considered for the pre-amplifier stage. Also, the designed cross-coupled LNA architecture has 64 dB of CMRR and a gain-bandwidth of 250 MHz.

To adapt the output of the amplifier to ADCs with various input dynamic ranges or operating voltages, the LV side is equipped with a PGA. Also, the sensitivity of the sensor and the generated magnetic field of the miniature coil are not precisely quantified before the measurement, so the PGA can compensate for these variations. Design constraints impose the PGA to have a constant and wide bandwidth for all gain stages as well as a high input impedance. Neither of these features could be obtained by the resistive or capacitive closed-loop topologies. As a result, a folded Gilbert cell of Fig. 7(c) with active load is selected for this design. To achieve dB-linear gain variation using a 3-bit gain setting, a dB-linear function is obtained by varying the tail current source of the Gilbert cell branches. Current sources are switched by transmission gates and they operate in parallel.

The output stage is composed of an impedance matching circuit, a fixed gain amplifier, and an AAF. To properly filter the spurious signal of the modulation/demodulation process, a second-order Butterworth AAF with a Sallen-Key topology and a 40 kHz cutoff frequency eliminates the clocking harmonics.

F. Hall-Based Digital Isolator

Fig. 8 demonstrates the full clock recovery circuit based on a Hall-effect sensor and using OOK modulation [21]. Self-resonance frequency is an efficient approach in modulating integrated coils. However, very small coils with low inductance have a high self-resonance frequency in a GHz range. To address that, careful consideration is required for wire-bonding, dices separation, and pad capacitances as any added parasitic capacitance on the resonant nodes can damp

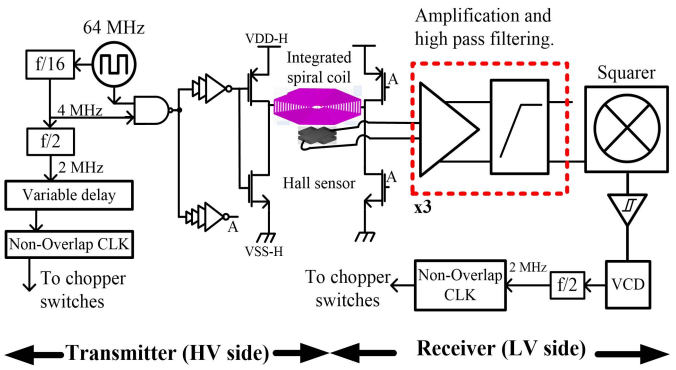

Fig. 8. Structure of the Hall-based digital isolator using OOK modulator.

the resonance frequency. Therefore, to avoid the damping and lower design constraints, first, an astable multivibrator generates a 64 MHz clocking signal as the carrier for the OOK modulation. Then, the weighted inverters drive the integrated spiral coil. On the receiver side (Rx), the Hall-effect sensor detects the signal. Three stages of amplification and the HPF amplify the modulated signal and eliminate the low-frequency noise, respectively. Finally, a squarer circuit rectifies the modulated signal. There are two sources of residual offset in chopper amplifiers: variation of the duty cycle from 50 % and the mismatch in charge injection of chopper switches. Therefore, to ensure a 50% duty cycle, D flip-flop dividers on both sides, with ratios shown in Fig. 8, ensure a duty cycle close to 50%.

Due to the digital nature and lower required resolution in the receiver circuit, the coil and the sensor can be fed with a much smaller current than the analog path. Therefore, to preserve the power, the Hall sensor is biased by 0.5 mA of current, and the coil current is limited to 1 mA through a limiting resistor. The analog coil has no active devices placed under the coil. However, to preserve the bandwidth of the Hall sensor in the digital isolator, the Rx circuitry is placed under the coil; this minimizes the inductive effect of the integrated coil and parasitic capacitances of the wirings. Therefore, the integrated coil has the same architecture as described in Section II-C but is only formed by Metal-4 which leaves more than 2 μm of SiO_2 for the isolation barrier. Based on the explanation of Section II-C this link can tolerate a similar 900 V of V_{iso}.

For any chopper circuit, it is essential to minimize the phase delay between the modulator and the demodulator switches, failing in adjusting the delay results in degraded amplifier's gain. Therefore, the propagation delay of the digital isolator must match the phase shift of the analog path that appears between the chopper modulator and demodulator at the 2 MHz modulation frequency. Sources of the phase shift are the driver and LV side's amplifiers. Although the digital isolator's propagation delay is partially compensated by the phase shift of the analog receiver circuitry, the Rx circuit is composed of a voltage-controlled delay (VCD) to further match the delay.

III. Measurement Results

The fully integrated Hall-based isolation amplifier composed of two dices is designed for voltage and current reading

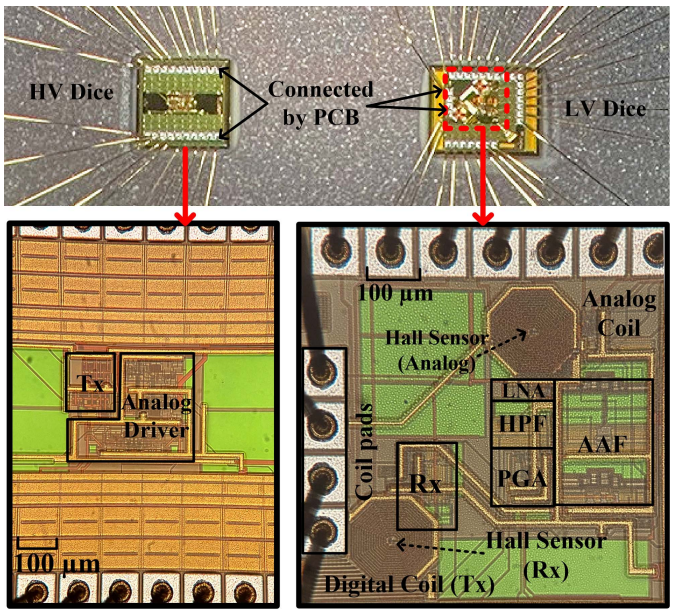

Fig. 9. Micrograph of the HV and LV dices packaged in PGA68.

of industrial read-back circuits. A micrograph of the packaged design along with the fabricated dices in a 0.35 μm technology is shown in Fig. 9. Each of the HV and LV dice has 1 mm^2 area. The HV-side has a supply range of 2 to 5 V and draws 3.8 mA from a 2 V supply. Also, the receiver dice consumes 3 mA from a 3.3 V supply.

A. Sensor, PGA, and Clock Recovery

The sensor response to a variable magnetic field is shown in Fig. 10. In this measurement, before the AAF, the output of the fixed gain stage is measured with a 2.6 mT peak-to-peak magnetic field at 2 MHz, and the process is repeated by decreasing the coil current. Based on the 80 dB gain of the amplifier's overall chain (i.e. LNA, PGA, and fixed gain stage) and 2 mA of biasing current, the sensor has a sensitivity of 0.032 $\frac{\text{V}}{\text{mA}\times\text{T}}$ which complies with the COMSOL simulation of Fig. 6.

To characterize the PGA of the LV side, the PGA circuit is isolated from the circuit and measured. The measured gain response of the PGA for various gain settings is illustrated in Fig. 11 and a gain variation of 17 dB to 39.2 dB with 3.16 dB steps is achieved. The 3 bits gain setting follows a dB-linear function with a maximum of 0.6 dB of dB-nonlinearity.

Lightning strikes or current surge in electromechanical systems are examples of transient noise that occurs between the VSS-H and VSS-L; this can cause the recovered clock on the LV side to not follow the generated clock on the HV side which distorts the demodulated signal and results in faulty reading. The robustness of digital isolators against the transient noise is determined by measuring the common-mode transient immunity (CMTI). The measurement setup of Fig. 12 (a) is employed to measure the CMTI. A 630-volt DC supply is connected to a HV pulser; The pulser is connected between the VSS-H and VSS-L grounds and generates pulses with a peak-to-peak value equal to the DC HV supply. The measured

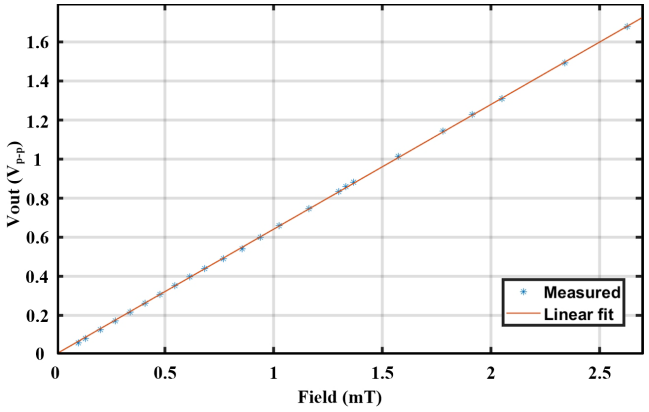

Fig. 10. Output of the amplifier respective with magnetic field variation measured for a 2 MHz input signal with no modulation.

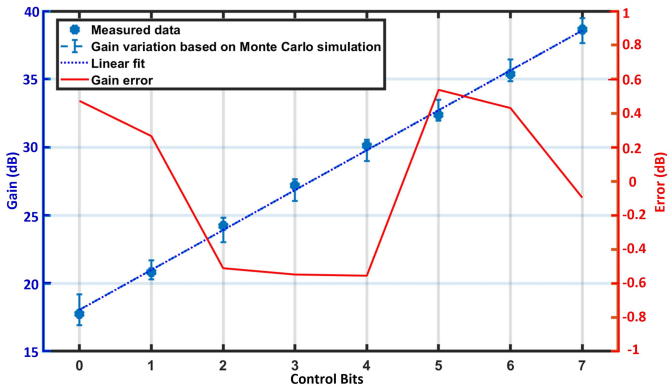

Fig. 11. Measured gain and dB-nonlinearity of the PGA for various gain settings.

CMTI of the Hall-based digital isolator is 12 kV/μs and higher CMTI measurement could not be achieved due to the limitation of the testing equipment.

The measured clock propagation delay is 35 ns. After performing post-layout simulation on phase response of the analog path for different gain ranges, the analog path has a delay between 32 to 42 ns for a 2 MHz modulation frequency. Therefore, 7 ns is the maximum unmatched delay between the analog signal (phase shift) and the clock on the demodulator side. This is equivalent to a negligible 1.4 % of the clock cycle which is further compensated by the VCD.

B. Isolation Amplifier

The measurement result of the full IA is described in this section. Depending on the IA's input amplitude range of 300 mV to 5V, the external gain resistor (R_g) of Fig. 12 could be tuned accordingly to obtain output (V_{out-IA}) swing of $\pm$1 V. Also, the PGA gain is tuned once based on the measured sensitivity, biasing current of the sensor, as well as the ADC specification being utilized.

To measure in a fully isolated environment, an off-package isolated DC-DC converter "RM-3.305S" is employed to provide the VDD-H. To measure the isolation mode rejection (IMR), as shown in Fig. 12 (b), a signal generator is placed between the IA input reference voltage and the LV ground

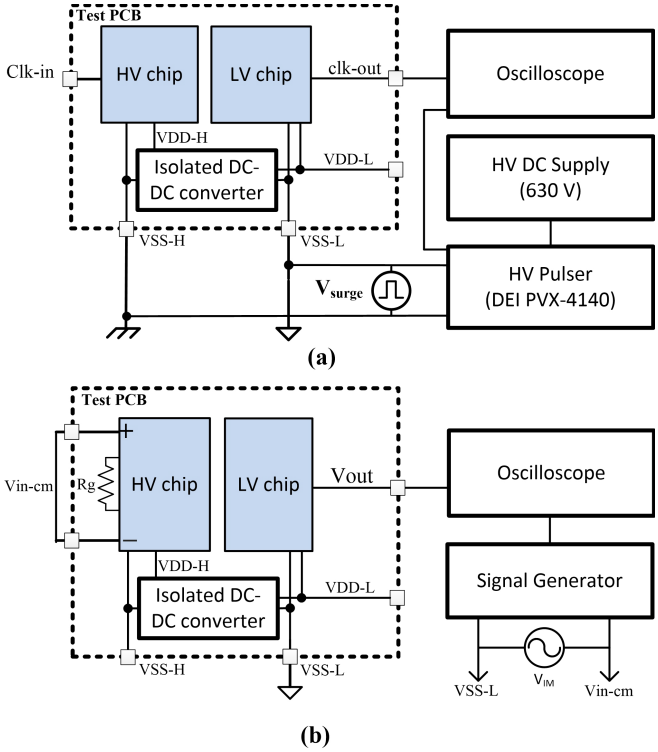

Fig. 12. Measurement setup of (a) CMTI, and (b) IMR.

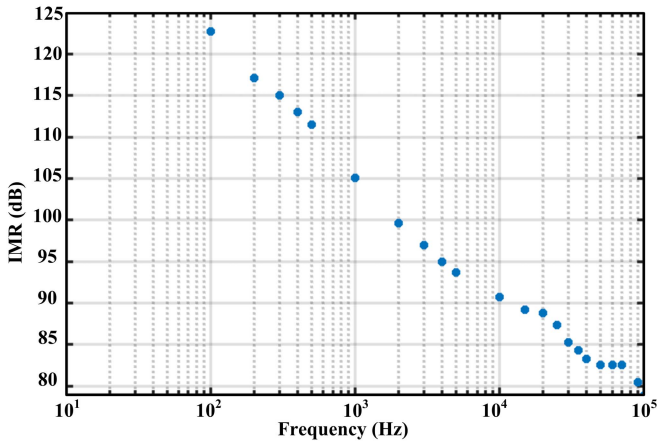

Fig. 13. Measured isolation mode rejection ratio of the Hall-based isolation voltage amplifier.

with a 20 V sinusoidal signal. The IMR is given by:

$$IMR = A_V + 20log\left(\frac{V_{IM}}{V_{out-n}}\right) \quad (2)$$

where A_V is the IA overall gain, V_{IM} is the signal generator voltage, and V_{out-n} is the output ripples resulting from the V_{IM}. Then using equation (2), the IMR is calculated for every frequency. The measured IMR is shown in Fig. 13 and demonstrates above 120 dB of IMR for frequencies lower than 60 Hz. No noise spectrum for frequencies lower than 100 Hz could be detected at the output stage, so the related data is not included. Based on the discussion of Section II-C, a theoretical V_{iso} of 900 V is expected; however, in this article, 600 V of isolation voltage is reported due to limitations in test equipment. Further validations including surge and short

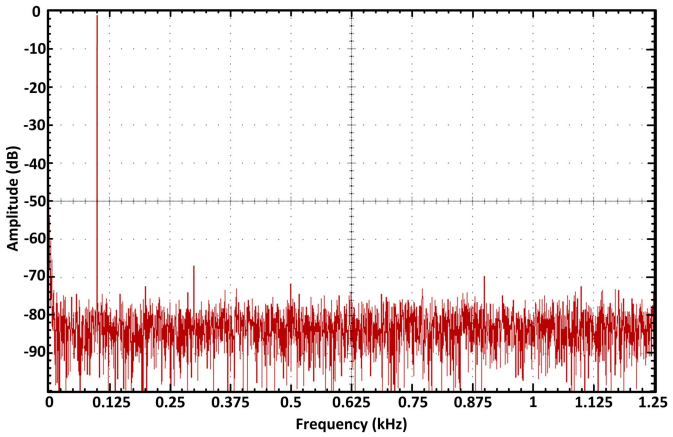

Fig. 14. Output voltage spectrum of the IA for a ±300 mV input signal at 100 Hz.

duration stress tests following international standards also were not applicable due to the limitation in testing apparatus.

The Hall-based approach of the proposed amplifier raises a concern regarding sensor saturation in presence of very high external magnetic noise. Before the high-pass filter that eliminates or attenuated the low-frequency high magnetic noises, the LNA is the amplification stage that can get saturated. The LNA output in presence of the high field can be calculated as:

$$V_{Out-LNA} = S_I I B A_{V-LNA} \tag{3}$$

where S_I is sensor sensitivity, I is the biasing current, B is the magnetic field, and A_{V-LNA} is the gain of the LNA. The LNA has a gain of 20 V/V and a maximum output swing of 1.5 V. Therefore, from equation (3), the sensor and LNA can operate in presence of 1.17 T of external magnetic noise, without getting saturated. Above the DC noise, the high-pass filter attenuates the low-frequency magnetic noise such as rotary equipment. So, the test is also conducted for a low-frequency noise (<200 kHz) with a lower magnetic field of 5 mT. In both cases, no saturation, sensitivity drift, or noise effect was observed in the signal spectrum. However, to be commercialized, this product must satisfy the CISPR-22 EMI standard, which we could not validate because of the limitation of our testing equipment. As a possible improvement solution, shielding of the dice can be achieved by selecting EMI resistant packages like the packaging technique employed for industrial current transducers.

The IA spectrum for a 300 mV amplitude of V_{in-IA} with frequency of 100 Hz is demonstrated in Fig. 14. This shows an SNR of 40 dB in 40 kHz bandwidth with spurious-free dynamic range (SFDR) of 64 dB. It should be noted that the sum of the sensor and LNA's input-referred thermal noise seen at the LNA's input is about 5.5 nV/$\sqrt{\text{Hz}}$; considering the measured sensor sensitivity and biasing current, 85 nT/$\sqrt{\text{Hz}}$ is the magnetic noise floor. This noise is multiplied by a total gain of the amplifier's path approximately creates a −86 dB noise floor of the signal spectrum. As the sensor defines the noise floor of the IA, various ranges of V_{in-IA} does not change the amplifier's noise floor. Additionally, based on the spectrum graph, the $1/f$ noise generated by the sensor and the LNA is eliminated due to modulation/demodulation and

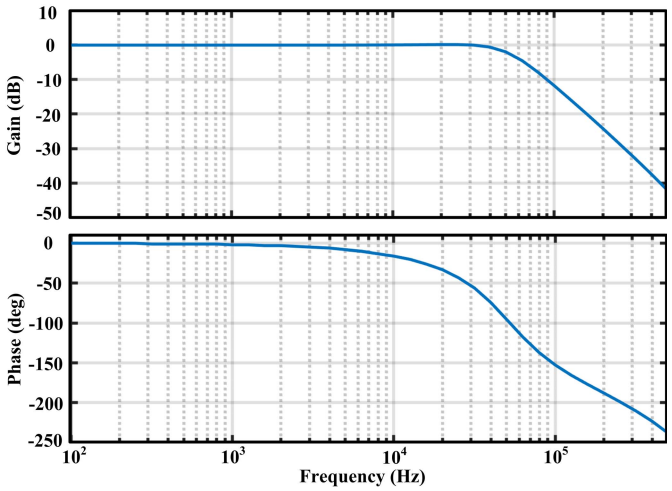

Fig. 15. Unity gain and phase response of the IA.

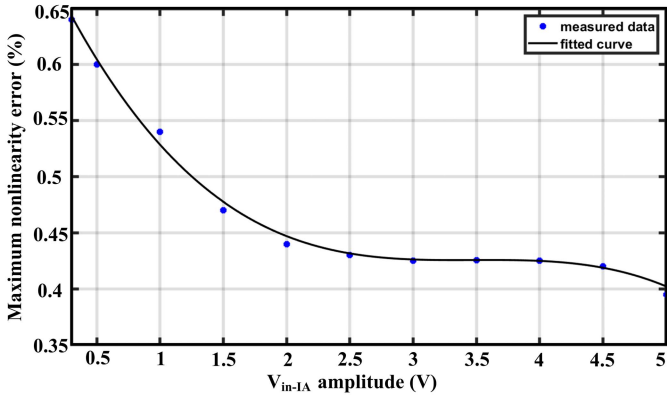

Fig. 16. Maximum output nonlinearity error of the IA for input differential voltage amplitudes ranging from 0.3 V to 5 V.

high pass filtering. Due to the low sensitivity of the CMOS Hall sensor, high gain stages are required, which amplifies the sensor noise and increases the output noise level. As a result, lowering the required gain by generating a stronger magnetic field or employing multiple sensors decreases the output noise. For instance, increasing the SNR could be achieved by implementing a CMOS process where more metal layers are available, so a stronger magnetic field can be generated for the same power.

The IA has a constant bandwidth for various gain tunings between −20 to 4.4 dB adjusted by R_g. Fig. 15 displays the bode plot of the unity gain response. The bode plot follows the response of the AAF and shows that the proposed architecture operates as a regular amplifier with a flat gain response. The measured few samples have an average input-referred offset of 1 mV. Finally, to measure the maximum nonlinearity error, for each amplitude of the V_{in-IA}, the R_g is tuned to deliver an output swing of 1 V. Then, the peak deviation of V_{out-IA} from a best linear fit over the full-scale range is reported as the maximum nonlinearity error. This process is repeated for different amplitudes of V_{in-IA}. The IA has a maximum nonlinearity error of 0.64 % for 300 mV amplitude of V_{in-IA} as can be depicted from Fig. 16.

TABLE III
PERFORMANCE SUMMARY

	Ma, et al. [4]	AD210BN [9]	HLSR 50-P/SP33 [22]	Takaya, et al. [23]	**This work**
Voltage/ Current	Voltage/ Current	Voltage/ Current	Current	Voltage/ Current	**Voltage/ Current**
Type	Inductive (Digital-SAR)	Inductive (Analog)	Hall Effect	Capacitive (Analog)	**Hall Effect (Analog)**
Isolated supply	Yes	Yes	-	No	**No**
Total chip area [mm^2]	2.5/2.5[(1)] (HV/LV)	-	-	4.2/8.8 (HV/LV)	**1/1 (HV/LV)**
Post processing	Yes	Yes	-	No	**No**
non-linearity %	0.02	0.01	0.8	1.2 (2-100mV)	**0.64 (300mV)**
V_{iso}[kV]	0.6	2.5	0.6	5	**0.6**
Power [mW] [(2)]	45/56 (HV/LV)	>750 (Total)	62.7 (Total)	63.4 (Total)	**7.6/9.9 (HV/LV)**
IMR @ 60 Hz [dB]	-	>100	-	110	**>120**
Input range [V]	±0.3	±15	±125 A	-	**±2** [(3)]
Input offset	0.7 [mV]	5 [mV]	0.25 A	-	**1** [mV]
Bandwidth [kHz]	200	20	450	35.2 [MHz]	**40**
Output noise [$\mu V/\sqrt{Hz}$]	0.4	0.18	4	~270[(4)]	**52**
Input resistance	-	1000 (GΩ)	-	-	**474** (kΩ)
SFDR [dB]	84.6	-	-	-	**64**
Gain temperature drift	50 $\frac{ppm}{°C}$	25 $\frac{ppm}{°C}$	200 $\frac{ppm}{°C}$	-	**4 % (-20 to 80°C)**

[(1)] The area is estimated based on chip micrograph.
[(2)] Power consumption of fully isolated amplifiers with isolated DC-DC converter is reported as "Total", otherwise, the HV and LV consumptions are separated.
[(3)] The input swing range is ±5 V when the HV side being supplied by 5 V.
[(4)] This number is obtained by estimating the noise level from the reported output spectrum and rescaling it by 46.4dB to correspond to an output signal of 1 Volt rms.

Table III compares the performance of the current work with the available commercial IAs and the state-of-the-art. Firstly, despite the superior performance of the amplifiers with digital isolators, they all have high consumption owing to the placement of an ADC on the HV side [4]. Inductive analog IA also suffers from high consumption because of the low quality-factor of miniature transformers. In comparison, the Hall-based analog IA represents a low consumption. Secondly, unlike Hall current sensors (e.g. HLSR 50-P/SP33 [22]), similar to the other compared items, the differential voltage sensing ability of the proposed amplifiers allows integration of multiple current and voltage readout circuits in only two dices. The compared amplifiers have various bandwidths and different representations of SNR. Thus, in this table, the amplifiers' resolution is compared by their noise spectral density for 300 mV amplitude of V_{in-IA} and for an output rms voltage of 1 V. Although this work has a higher output noise compared with Ma, *et al.* [4] and AD210 [9], the proposed architecture yet can be used in applications with a less stringent resolution. Also, doubling the number of serried spiral coils in a process with more metal layers doubles the generated magnetic field strength and increases the SNR by 6 dB.

Usage of inductive links in IAs with modulated analog data transmission (e.g. AD210BN [9]) is a challenge for multi-channel readout circuits because of the large size of transformers. Consequently, for every channel, it requires a large package size of 53 × 25 × 9 mm^3 [9]. The isolation amplifiers that are equipped with ADCs (e.g. Ma, *et al.* [4]) have a much smaller transformer diameter fabricated on a dedicated dice; however, the employed polyimide as an isolator requires costly post-processing. In addition, the ADC and DAC consume a large chip area. The capacitive analog isolation of Takaya, *et al.* [23] has the smallest reported footprint with a total core area of 0.99 mm^2. However, including the integrated coil with its pads, the reported Hall-based IA has the smallest total core area of 0.42 mm^2. In contrast with other arts, this work does not require any off-chip isolator or proprietary process and it uses only two dices for data transfer with a smaller footprint. Considering these challenges, our design is an ideal solution for dense integration in multi-channel isolated sensor interfaces due to its simple design, low power consumption, small footprint, and no requirement for post-processing.

IV. CONCLUSION

The present study demonstrates a CMOS Hall sensor-based analog isolation voltage amplifier for sensor interface units in a system-in-package setup. It is shown that the proposed design provides isolation working voltage of 600 V with an isolation-mode rejection ratio of greater than 120 dB for frequencies lower than 60 Hz. Furthermore, an SFDR of 64 dB, overall SNR of 40 dB in 40 kHz bandwidth, and an input-referred offset of 1 mV are fulfilled within the current work. Additionally, the power consumption of this amplifier is 7.6 mW and 9.9 mW on the HV and LV side, respectively. The fully integrated configuration makes the presented isolation system a proper candidate to support multi-channel readout circuits using only two dices and no external component.

REFERENCES

[1] M. Ali, M. Nabavi, A. Hassan, M. Honarparvar, Y. Savaria, and M. Sawan, "A versatile SoC/SiP sensor interface for industrial applications: Design considerations," in *Proc. 31st Int. Conf. Microelectron. (ICM)*, Dec. 2019, pp. 40–43, doi: 10.1109/ICM48031.2019.9021286.
[2] *Adjustable Speed Electrical Power Drive Systems—Part 5-2: Safety Requirements—Functional*, Standard IEC 61800-5-2, 2016.
[3] S. Ziegler, R. C. Woodward, H. H.-C. Iu, and L. J. Borle, "Current sensing techniques: A review," *IEEE Sensors J.*, vol. 9, no. 4, pp. 354–376, Apr. 2009, doi: 10.1109/JSEN.2009.2013914.
[4] S. Ma, J. Feng, T. Zhao, and B. Chen, "A fully isolated amplifier based on charge-balanced SAR converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 6, pp. 1795–1804, Jun. 2018, doi: 10.1109/TCSI.2017.2767678.
[5] *ACPL-790B, ACPL-790A, ACPL-7900 Precision Isolation Amplifiers*. Accessed: Oct. 2021. [Online]. Available: https://docs.broadcom.com/
[6] "Designing linear amplifiers using the IL300 optocoupler," Vishay Semicond., Appl. Note 50, Mar. 2012. Accessed: Jun. 2021. [Online]. Available: https://www.vishay.com

[7] T. I. Bajenesco, "Ageing problem of optocouplers," in *Proc. Medit. Electrotech. Conf. (MELECON)*, vol. 2, Apr. 1994, pp. 571–574, doi: 10.1109/MELCON.1994.381028.
[8] Broadcom. *Calculate Reliable LED Lifetime Performance in Optocouplers*. Accessed: Nov. 2021. [Online]. Available: https://www.broadcom.com/
[9] *AD210 Precision, Wide Bandwidth 3-Port Isolation Amplifier*. Accessed: Jun. 2021. [Online]. Available: https://www.analog.com
[10] S. S. Mirfakhraei, Y. Audet, A. Hassan, M. Ali, M. Nabavi, and M. Sawan, "A CMOS MAGFET-based programmable isolation amplifier," in *Proc. 18th IEEE Int. New Circuits Syst. Conf. (NEWCAS)*, Jun. 2020, pp. 9–13, doi: 10.1109/NEWCAS49341.2020.9159790.
[11] S. S. Mirfakhraei *et al.*, "Wide dynamic range front-end programmable isolation amplifier using integrated CMOS Hall effect sensor," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Oct. 2020, pp. 1–5, doi: 10.1109/ISCAS45731.2020.9180574.
[12] S. S. Mirfakhraei, Y. Audet, A. Hassan, and M. Sawan, "A galvanic isolated amplifier based on CMOS integrated Hall-effect sensors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 4, pp. 1388–1397, Apr. 2021, doi: 10.1109/TCSI.2021.3052476.
[13] A. Chovet, C. S. Roumenin, G. Dimopoulos, and N. Mathieu, "Comparison of noise properties of different magnetic-field semiconductor integrated sensors," *Sens. Actuators A, Phys.*, vol. 22, no. 1, pp. 790–794, 1990, doi: 10.1016/0924-4247(89)80079-2.
[14] *ISO72x Single Channel High-Speed Digital Isolators Data Sheet Rev. L.* Accessed: Jun. 2020. [Online]. Available: https://www.ti.com/
[15] D. J. Dumin, *Oxide Reliability: A Summary of Silicon Oxide Wearout, Breakdown, and Reliability*. River Edge, NJ, USA: World Scientific, 2002.
[16] Y. Xu, X. Hu, and L. Jiang, "An analytical geometry optimization model for current-mode cross-like Hall plates," *Sensors*, vol. 19, no. 11, p. 2490, May 2019, doi: 10.3390/s19112490.
[17] M. Crescentini, M. Biondi, A. Romani, M. Tartagni, and E. Sangiorgi, "Optimum design rules for CMOS Hall sensors," *Sensors*, vol. 17, no. 4, p. 765, Apr. 2017, doi: 10.3390/s17040765.
[18] Y. Xu and H.-B. Pan, "An improved equivalent simulation model for CMOS integrated Hall plates," *Sensors*, vol. 11, no. 6, pp. 6284–6296, Jun. 2011, doi: 10.3390/s110606284.
[19] I. N. Ruskova, E. E. Gieva, V. M. Yantchev, and M. H. Hristov, "COMSOL modeling of Hall sensors efficiency," in *Proc. 26th Int. Sci. Conf. Electron. (ET)*, Sep. 2017, pp. 1–4, doi: 10.1109/ET.2017.8124384.
[20] Z. Randjelovic, "Low-power high sensitivity integrated Hall magnetic sensor microsystems," Ph.D. dissertation, EPFL, Lausanne, Switzerland, 2000.
[21] S. S. Mirfakhraei, Y. Audet, A. Hassan, and M. Sawan, "A small footprint digital isolator based on CMOS integrated Hall-effect sensor," *IEEE Sensors J.*, early access, Nov. 16, 2021, doi: 10.1109/JSEN.2021.3128573.
[22] *Current Transducer HLSR-P/SP33 Series*. Accessed: Jun. 2021. [Online]. Available: http://www.lem.com
[23] S. Takaya, H. Ishihara, and K. Onizuka, "A DC to 35 MHz fully integrated single-power-supply isolation amplifier for current- and voltage-sensing front-ends of power electronics," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 298–300, doi: 10.1109/ISSCC19947.2020.9063124.

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