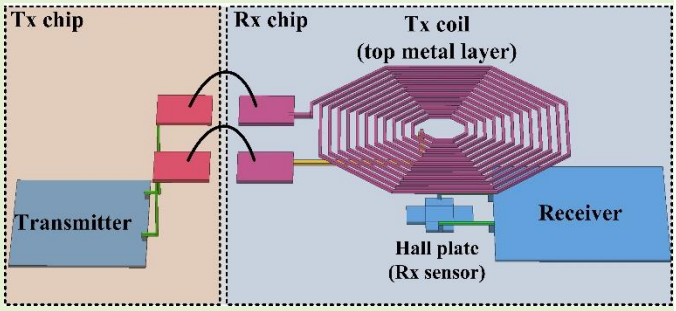
A Small Footprint Digital Isolator based on CMOS Integrated Hall-effect Sensor

Seyed Sepehr Mirfakhraei, Yves Audet, *Member, IEEE,* Ahmad Hassan, *Member, IEEE,* and Mohamad Sawan, *Fellow, IEEE*

***Abstract*— Digital isolators have been widely used to protect low voltage electronics as well as human safety from high voltage surges. However, conventional isolation links occupy large chip areas. In this article, a novel small-size on-chip digital isolator for medium-bitrate application based on a CMOS integrated Hall-effect sensor is reported. With the proposed approach, the area of the transmitter coil is reduced to lower than 50% of conventional transformers. The architecture reduces the chip area in isolation amplifiers, power control units, DC-DC converters, and clock recovery circuits. It allows the integration of multichannel isolators using two custom integrated circuits with no post-processing. The tested prototype achieves a data transfer rate of 20 Mbps with above 12 kV/µs of common-mode transient immunity (CMTI). It has 900 V of continuous isolation working voltage, 27 ns propagation delay, and consumes 2.3 mA of static current.**



***Index Terms*— Digital isolator, Galvanic isolation, CMOS Hall sensor, Gate driver, Integrated spiral coil.**

I. Introduction

MAGNETIC field sensors are broadly utilized across various applications. Linear or angular position sensors [1], magnetic field measurements, and switches are examples of industrial applications. Employing their magnetic field sensing capability, the sensor usage is expanded to provide galvanic isolation. For instance, contactless current sensors (current transducers) replaces shunt based sensing with no drop out voltage and achieve a remarkable V_{iso} [2]. Magneto resistors, have also been employed as digital isolators [3].

Isolated DC-DC converters, clock recovery of isolation amplifiers, power-over-ethernet, inter-integrated circuit (I^2C), and industrial programmable logic controllers (PLC) are applications that require the transmission of low to medium data rates over an isolation barrier. The digital isolators must satisfy stringent isolation standards including isolation working voltage (V_{iso}) and common-mode transient immunity (CMTI).

This work was supported in part by the Natural Sciences and Engineering Research Council of Canada (NSERC), in part by Mitacs, and in part by the design and simulation tools supported by CMC Microsystems.

Seyed Sepehr Mirfakhraei, Yves Audet, and Ahmad Hassan are with the Electrical Engineering Department, Polytechnique Montréal, Montréal, QC H3T 1J4, Canada (e-mail: seyed-sepehr.mirfakhraei@polymtl.ca). Mohamad Sawan is with the Polystim Neurotech Laboratory, Electrical Engineering Department, Polytechnique Montréal, Montréal, QC H3T 1J4, Canada, also with the CenBRAIN Laboratory, School of Engineering, West-lake University, Hangzhou 310024, China, and with the Westlake Institute of Advanced Sciences, Hangzhou 310024, China.

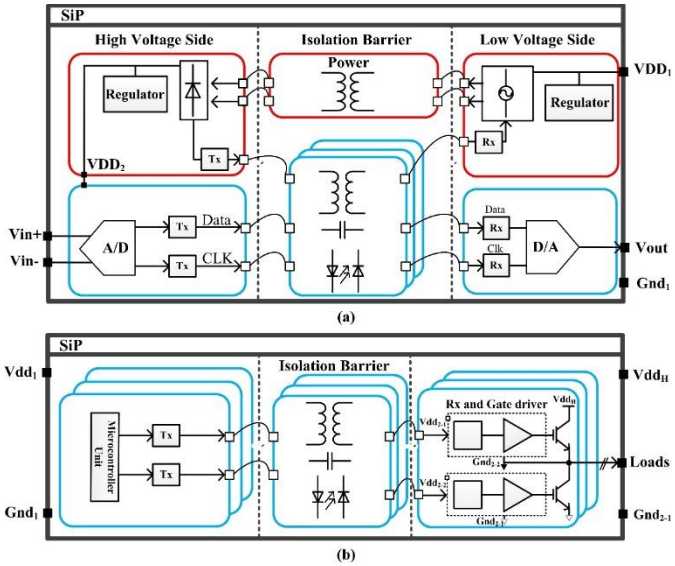


Fig. 1. (a) Isolated amplifier based on analog to digital converter, and (b) typical motor drive system.

Besides, reducing the number of chips and chip areas results in a low-cost product.

Fig. 1(a) shows a system in package (SiP) of a typical fully integrated isolation amplifier (IA) based on an analog-to-digital converter (ADC) [4]. This IA employs three digital isolator links: (i) a link for isolated DC-DC converter, (ii) clock recovery, and (iii) data. As another application, Fig. 1(b) shows a conventional three-phase motor driver. To avoid damaging

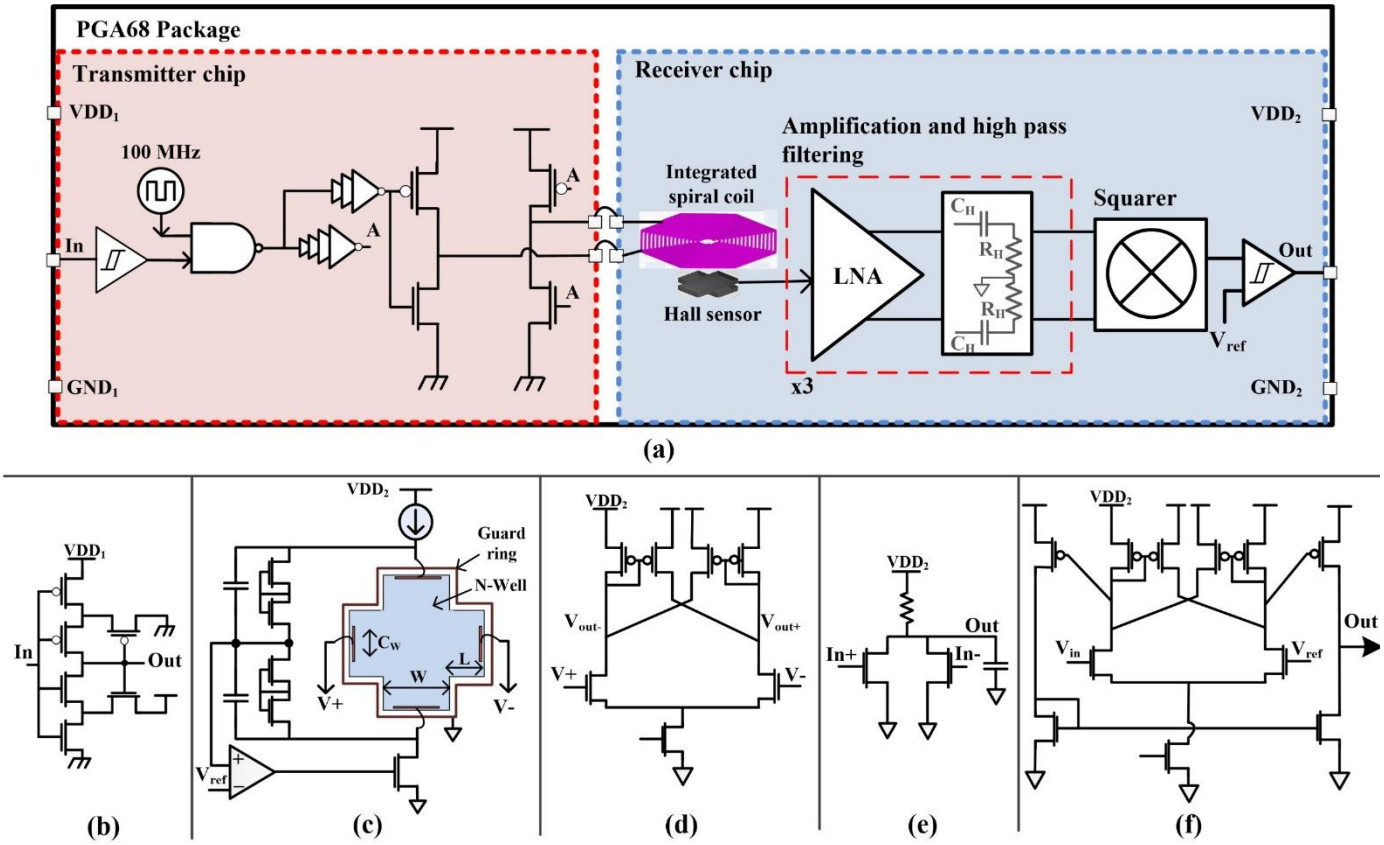


Fig. 2. (a) General architecture of the proposed Hall based digital isolator, (b) input Schmitt trigger inverter, (c) biasing circuit of the Hall sensor, (d) cross-coupled architecture of the sensor's LNA, (e) squarer circuit, and (f) output comparator.

the microcontroller unit (MCU) from HV pulses driving power transistor gates, the MCU needs to be isolated and six isolator links are required [5]. Therefore, integrating multiple isolator links in a small die can lower the consumed chip area and consequently the fabrication cost.

So far, all the isolation links including optic, capacitive, magneto resistor (MR), and inductive are employed in digital isolators. Despite unique isolation properties, optocouplers suffer from integration levels as they are made by GaAs, which cannot be integrated into a CMOS process. So, for every channel, a dedicated optocoupler chip is required. Also, optocouplers are prone to low lifetime due to electrical and thermal stress [6]. Capacitive digital isolators are highly integrable as capacitors can be formed by metal layers of a fabrication process, while the required isolation level is achieved using process silicon dioxide (SiO_2) available as intermetal fillings; laying out metal capacitors of both transmitter (Tx) and receiver (Rx) chips reinforces the isolation level. Besides, they require only two chips for any number of isolated links. However, transmitting of low-frequency signals requires an enlarged capacitor, so conventionally two data paths transfer the digital signal, one using a modulation scheme for transmission of low bitrate (<100 kbps) signals and one channel for high bitrate (>100 kbps) signals. Consequently, the dual-channel capacitors increase chip area. Besides, as a two-terminal device, capacitive digital isolators suffer from transmission of common-mode transient noise (CMTN), and they have lower CMTI than transformers.

Most industrial digital isolators that are based on inductive links form the primary side of transformers on top of a polyimide isolator deposited as the last layer of the dielectric stack. The secondary side of the transformer is shaped by the top thick metal layer of the CMOS process [4]. The added deposition of the polyimide layer increases the cost and is not available in regular foundries. Although the on-chip transformer-based isolators are suitable for dense integration of multiple isolation channels in a microcontroller or gate driver chips, conventional technology still has the problem of considerably large transformer area.

Giant magnetoresistance (GMR) or tunneling magnetoresistance (TMR) technology are the magnetic sensors that have been studied for digital isolators implementation [3] and commercialized through NVE's patented IsoLoop spintronic technology. Standard CMOS processes do not include deposition of ferrite/magnetic material for MR type digital isolators. Therefore, these types of isolators suffer from higher manufacturing cost. Employing CMOS Hall effect sensors is a cost-effective alternative.

This work presents an on-chip micro-transformer-based medium-speed digital isolator based on a Hall-effect sensor designed for dense integration. The rest of the paper is organized as follows: system architecture is explained in section II with the explanation of sensor and coil selection. Section III investigates the CMTI of the design. The measurement results and discussion are stated in Section VI, and finally, the conclusion and remarks appear in Section V.

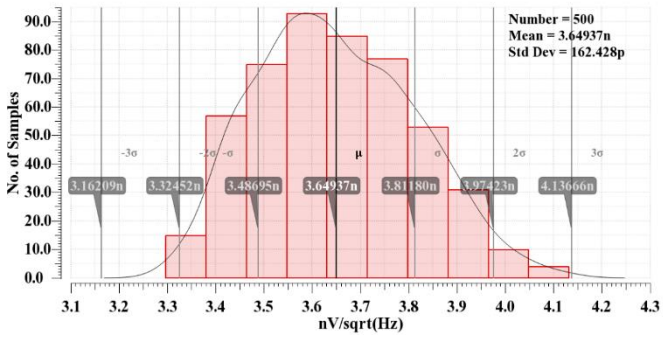


Fig. 3. Monte Carlo simulation of the LNA's input referred noise.

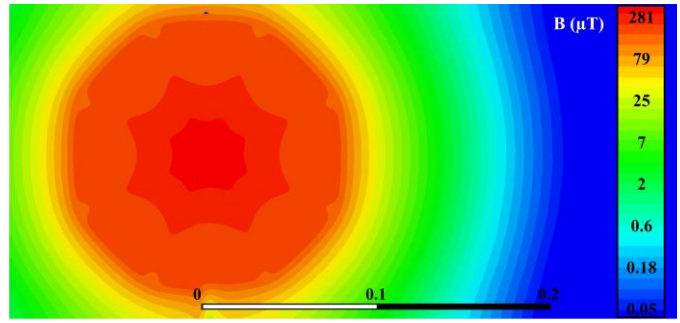


Fig. 4. Ansys Maxwell simulation of magnetic field strength of the integrated spiral coil showing central magnetic field of 281 μT for 1 mA of current.

TABLE I
PARAMETERS OF THE INTEGRATED SPIRAL COIL

Parameter	Value
Number of turns	15
Turn spacing (μm)	2
Wire width (μm)	2.5
Inner diameter (μm)	22
Current density (mA/μm)	1.5
Outer diameter (μm)	158

II. DESIGN AND IMPLEMENTATION

A. System Architecture

General architecture of the Hall-based digital isolator is illustrated in Fig. 2(a). First, located on the Tx chip, a Schmitt-trigger inverter conditions the digital input signal. Then, a 100 MHz bi-stable oscillator generates OOK modulation carrier frequency, and weighted inverters drive the integrated spiral coil located on the Rx chip. Next, a Hall-effect sensor placed under the coil center detects the signal, and three stages of amplification and passive high-pass filtering (HPF) amplify the modulated signal and filter the low-frequency noises, respectively. Each of the low-noise amplifiers (LNA) has a 35 dB gain. A 50 MHz of corner frequency is selected for each passive HPFs to attenuate the HV surges noises. The HPFs also remove flicker noises and DC offset of the combined sensor and amplification stages. Finally, a squarer circuit rectifies the modulated signal, and a comparator generates the output signal. The circuit schematic of each block is shown in Fig. 2(b-f).

B. CMOS Hall Sensor

Although Hall effect sensors are widely known for their limited bandwidth, about THz theoretical bandwidth limit of Hall sensors is experimentally validated by Mittleman, et al. [7]. This high-frequency behavior of the Hall plates is subject to parasitic capacitances and the conventional inductive effect that severely limits the frequency response [8]. Therefore, design and layout considerations are applied to avoid inductive and capacitive effects. First, according to Fig. 2(a), biasing voltage of the first amplifier stage must be provided by the sensor. Therefore, to avoid adding any capacitive load on the Hall voltage nodes, voltage reading of the common-mode feedback (CMFB) is performed from the biasing nodes of the Hall plate as seen in Fig. 2(c). Then, the common mode voltage is fixed to a V_{ref}. Second, the LNA must satisfy a low input gate capacitance as well as a wide bandwidth. For this purpose, the cross-coupled architecture of Fig. 2(d) with NMOS input differential pairs are chosen. Third, to address the inductive effect and lowering wiring capacitance, the LNA is placed under the coil and 40 μm away from the Hall voltage contacts. The wiring between the sensor and the differential pair are the minimum width with equal distances and any loop is avoided to minimize the inductive effect and conserve the sensor bandwidth.

The CMOS Hall plate converts the orthogonal magnetic field to an electrical signal via the Lorentz force, so optimization toward sensitivity and minimization of the sensor's noise floor improves the signal quality of the sensor. Optimal sizing of a cross-shaped Hall effect sensor of Fig. 2(c) relative to the width (W) and length (L) has been previously reported in [9]. The sensor is surrounded by a guard ring to eliminate noises induced by the P-substrate. The variation of sensitivity with respect to the sensor area is described by Crescentini et al [10] and an enlarged area increases the sensitivity of the sensor. In contrast, reported by Xu and Pan [11], expanding sensor size, decreases the sensor's 3 dB bandwidth. Therefore, to avoid limiting the bandwidth of the sensor, a small sensor is designed with W of 19.3 μm and L of 11.2 μm. Large contact width of the signal nodes (C_W) shortens the voltage equipotential line deflection over the sensing nodes leading to a lower sensitivity. Therefore, a short contact size of 1.2 μm is depicted for the design.

To optimally capture the Hall voltage induced by the generated magnetic field, the first amplifying stage must have a low input-referred noise (VN_{in}). At the 100 MHz of modulation frequency, the dominant noise of the sensor is thermal. Knowing the process has N-Well sheet resistance of 1 kΩ/square and using the methodology described by Xu and Pan [11], the sensor has a resistivity of 1.6 kΩ and consequently 5.1 nV/$\sqrt{\text{Hz}}$ of thermal noise. Therefore, the LNA must be designed with a VN_{in} lower than this thermal noise to avoid contaminating the received signal. The designed cross-coupled structure of Fig. 2(d) has a VN_{in} of 3.65 nV/$\sqrt{\text{Hz}}$ that can be observed from Fig. 3.

C. Integrated Spiral Coil

Generating a magnetic field in Hall-based digital isolator involves several challenges. First, the Hall sensor signal quality is directly proportional to the field, so an adequate magnetic field is required to achieve a reasonable signal-to-

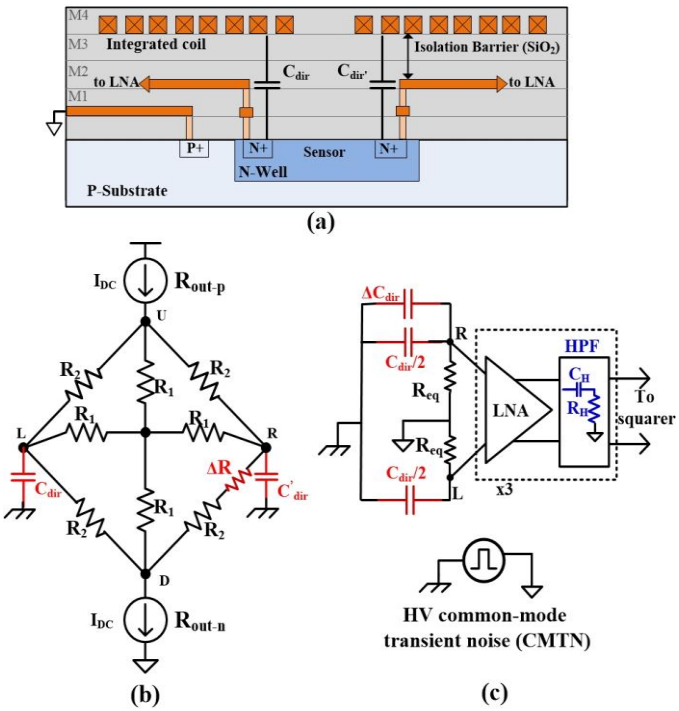


Fig. 5. (a) Side view of the Rx chip showing parasitic capacitances between the integrated spiral coil and the Hall plate, (b) resistive model of the Hall plate with the parasitics, and (c) simplified schematic showing impact of the parasitics to the Rx circuit.

noise ratio (SNR). Second, the coil behaves like a series of restive-inductive loads (i.e. a low pass filter); therefore, to avoid attenuating the carrier signal, the magnetic coil must have low inductance. Finally, the coil must have a small footprint to lower the transceiver size, simplify packaging complexity, and reduce cost. Therefore, on top of the Hall plate, a single layer of integrated hexagonal spiral coil is fabricated using process top thick metal layer with specifications listed in Table I. To determine the field strength of the coil, an Ansys Maxwell simulation is performed for the peak current of 1 mA. Fig. 4 shows 281 µT magnetic fields at the coil center where the sensor is located.

Using the integrated coil approach, SiO_2, the intermetal filling of the CMOS process behaves as the isolation barrier. Following the reported mean time to failure of 450 V/µm for 20 years [12], and 2 µm of spacing between process second and the top metal layer, above 900 V of isolation working voltage (V_{iso}) is achieved in this design. Further increase of the V_{iso} can be obtained through a smaller process with a greater number of metal layers and consequently a thicker isolation barrier.

To have multi-channel Hall-based digitally isolated links in the same chip, the Hall sensors must be in a cross-talk-free environment with its neighboring coil. To determine the cross-talk-free distance, the output voltage of the sensor resulting from the magnetic field of the neighboring coil must be smaller than sensor thermal noise. The sensor output is defined as:

$$V_{diff} = S_I\, B\, I \tag{1}$$

where S_I is current-related sensitivity, B is the magnetic field, and I is sensor biasing current. Assuming S_I is 0.03 $\left(\frac{\mathrm{V}}{\mathrm{mA.T}}\right)$ [13] and I is 0.5 mA, any magnetic field lower than 0.34 µT generates a peak voltage lower than the sensor's thermal noise of 5.1 nV and cannot be detected. Based on Fig. 4, multiple receiver sensors can be placed 200 μm apart from each other. Finally, based on simulation data, the coil has a self-resonance frequency of 4.2 GHz. The predicted oscillation frequency occurs is higher than the LNAs' bandwidth at the Rx circuit and cannot get amplified. However, to prevent the self-resonance frequency at higher bitrate applications, the Tx driver needs to be upgraded to avoid any current flowing through the coil when the input logic is low. This could be done with an LC tank oscillator or modifying the Tx logic circuitry.

III. Analysis of Noise Rejection

The output of digital isolators must always follow the input logic when a common-mode transient noise (CMTN) occurs between the grounds of the Tx and Rx side. The parasitic capacitance on the input node of the transmitter stores the charge and during HV surge causes the input inverter to follow the noise. Therefore, the Schmitt inverter protects the input from being contaminated by the CMTN.

Cross shape Hall plate sensors receive signals based on Lorentz force. Unlike the capacitive link, the different sensing mechanism comes with the advantage of not being sensitive to CMTN from the Tx side [4], [14]. However, miniaturization of the integrated magnetic coil with its close distance to the sensor form parasitic capacitances of C_{dir} and C'_{dir} as shown in Fig. 5(a). To investigate in detail the effect of parasitic capacitances, the resistive model of the sensor depicted from Xu and Pan [11] with the parasitic capacitances is illustrated in Fig. 5(b). The C_{dir} and C'_{dir} seen from the LNA nodes are not identical due to natural non-symmetry of the integrated spiral coils and it is assumed to have a difference of ΔC_{dir}. In Fig. 5(b), ΔR models the sensor offset due to masking misalignment or nonuniformity of dopant [13] which is the main source of DC offset in Hall effect sensors. Fig. 5(c) shows a simplified AC model of the available parasitic between the LNA and CMTN of the Tx side. Following the methodologies described by Lyu, et al. [13], ΔR is lower than one ohm, so the effect of ΔR can be ignored, and R_{eq} is calculated as:

$$R_{eq}=(R_{out\text{-}p}+R_S)||(R_{out\text{-}n}+R_S) \tag{2}$$

Here, R_S is the Hall sensor resistance between voltage or current nodes, and $R_{out\text{-}p}$ or $R_{out\text{-}n}$ are output resistance of the tail current sources.

While the main CMTN appears as a common-mode signal (N_{cm}), the ΔC_{dir} exhibits a differential noise (N_{dif}). Therefore, noise voltage at the input of LNA is defined as:

$$\mathrm{CMTN}= \mathrm{N_{cm}}+\mathrm{N_{dif}} \tag{3}$$

Next, the resulting output noise of the LNA is calculated as:

$$\mathrm{V_{out}^{LNA}}=\mathrm{N_{dif}}\, A_{dif}^{LNA} + \mathrm{N_{cm}}\, A_{cm}^{LNA} \tag{4}$$

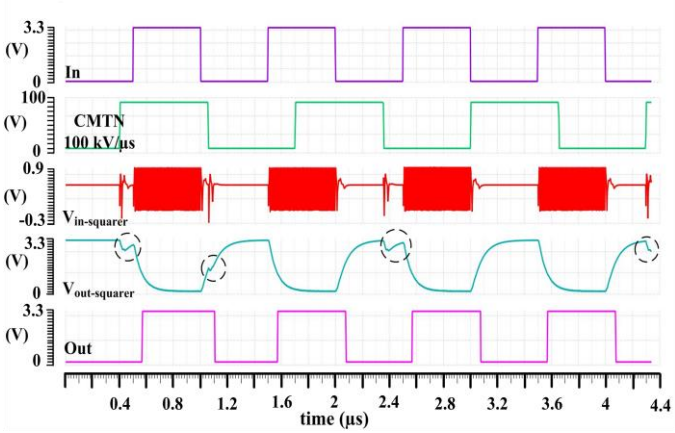


Fig. 6. Post layout simulation showing isolator's signal flow in presence of 100 kV/µs of common-mode transient noises.

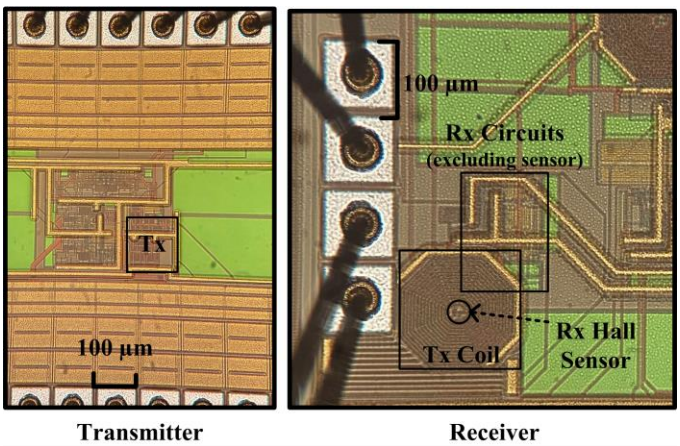


Fig. 7. Micrograph of the transmitter and receiver chips.

A_{dif}^{LNA} is the differential gain and A_{cm}^{LNA} is the common-mode gain of the LNA. Then, the V_{out}^{LNA} undergoes three stages of passive high pass filtering with capacitors of "C_H" and resistors of "R_H", and two stages of further amplification. Then, the input noise at the squarer will be calculated as:

$$V_{In}^{Squarer} = \left(\frac{S}{S + \frac{1}{C_H R_H}} \right)^3 \left(A_{dif}^{LNA}\right)^2 V_{out}^{LNA} \qquad (5)$$

Following the post-layout simulation, C_{dir} and ΔC_{dir} are extracted to be 100 fF and 20 fF, accordingly. Also, A_{dif}^{LNA} is 35 dB and A_{cm}^{LNA} is -40 dB. Based on work presented by Xu and Pan [11], R_{eq} can be calculated as approximately 1 kΩ. By solving for poles and zeros, V_{out}^{LNA} has a high pass pole located at 8 GHz. Therefore, in total, the received noise on the squarer circuit is suppressed by four HPFs; that includes three passive 50 MHz and one intrinsic coil-sensor filter at 8 GHz. Post layout simulation illustrating different signal stages of the Rx circuit for CMTN of 100 V in 1 ns rise/fall time (100 kV/µs of slew rate) is shown in Fig. 6. This figure illustrates that the HPFs pass the OOK modulated signal while attenuating the CMTN to lower than 0.75 V of impulse noise. The reference voltage of

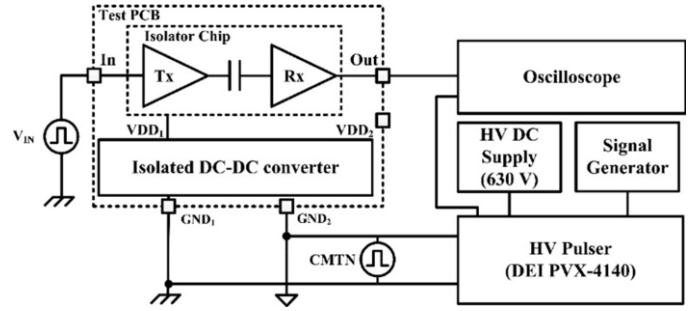


Fig. 8. CMTI measurement setup.

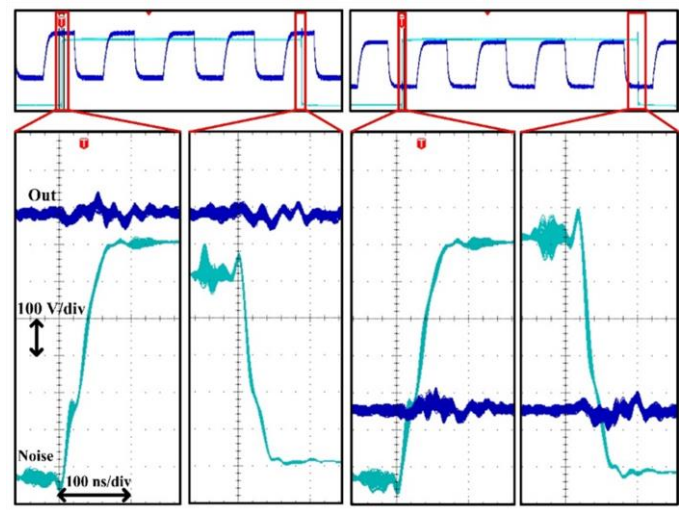


Fig. 9. CMTI test result for rising and falling edge when output state is high or low.

the last HPF is selected to be 200 mV lower than the threshold voltage (V_{th}) of the squarer input NMOSs transistors. This results in approximately 0.58 V of peak impulse noise at the squarer's input that is lower than the V_{th}; therefore, it does merely affect the output squarer as circled in Fig. 6. Finally, a hysteresis comparator eliminates the remaining CMTN effects and protects the output logic state.

IV. Measurement Results

The Hall-based digital isolator with the on-chip coil is composed of two dies. A micrograph of the packaged design along with the fabricated dies in Austria Microsystem (AMS) 0.35 µm technology is shown in Fig. 7. Excluding pad area, the Tx and Rx circuits occupy an area of $100 \times 70\ \mu m^2$ and $265 \times 185\ \mu m^2$, respectively. The integrated spiral coil of the Tx circuit has an area of $156 \times 156\ \mu m^2$, 12 nH of inductance, and resistance. The integrated coil has 80 Ω of resistance and is connected in series with a 3 kΩ resistor to limit the coil peak current flow. The measured sensitivity of the sensor is $0.032\ \frac{V}{mA \times T}$. Part of the Rx circuit is located under this coil to minimize the inductive effect as well as parasitic capacitance of wiring between the sensor and coil. A pad containing no metal-1 to metal-3 is considered for the coil connections; the Rx circuits located under the coil are free from metal-3. Therefore, above 2 µm of SiO_2 enables the design to

TABLE II
PERFORMANCE SUMMARY

Parameter	Isolation Type	Isolation material	Post Processing	# of Dies	Isolator size [mm^2]	Maximum bitrate [Mbps]	Propagation delay [ns]	CMTI [kV/µs]	V_{iso} [kV]	IDD (Tx+Rx) @ DC [mA](2)	IDD (Tx+Rx), @ 10 Mbps 15 pF load [mA] (2)
Kaeriyama , et al [15]	Inductive	SiO_2	No	2	0.053	250	5.9	35	1.5	1.6	1.9
ADuM131 [16, 17]	Inductive	Polyimide	Yes	3	0.5(1)	10	20-60	35	1-1.7	2	4.5
Si80xx [18]	Capacitive	SiO_2	No	2	-	10	40	50	1	1.98	2.3
ISO72X [19]	Capacitive	SiO_2	No	2	0.059(1)	100-150	10	50	0.56	4.3	5.6
IL01x [20]	TMR	-	Yes	-	-	10	25	50	1.5	0.3	1.8
HCPL-9000 [21]	GMR	-	Yes	-	-	100	15	15	2.5	3.3	4.3
This work	**Hall Effect**	**SiO_2**	**No**	**2**	**0.024**	**20**	**27**	**12<**	**0.9**	**2**	**2.9**

(1) Size is estimated based on chip photo
(2) At $VDD_1 = VDD_2 = 3.3$ V

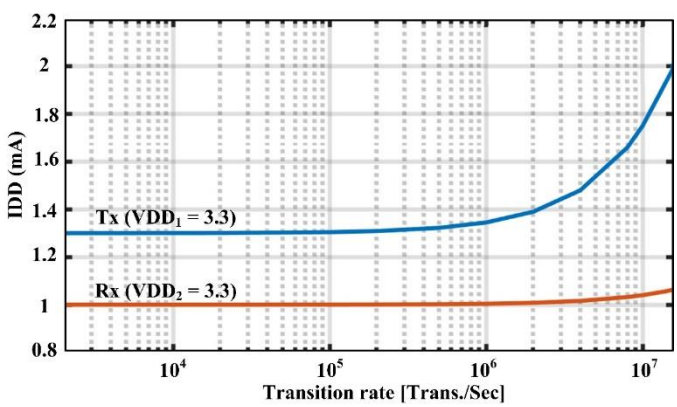


Fig. 10. Current consumption versus bitrate for the Tx and Rx circuit.

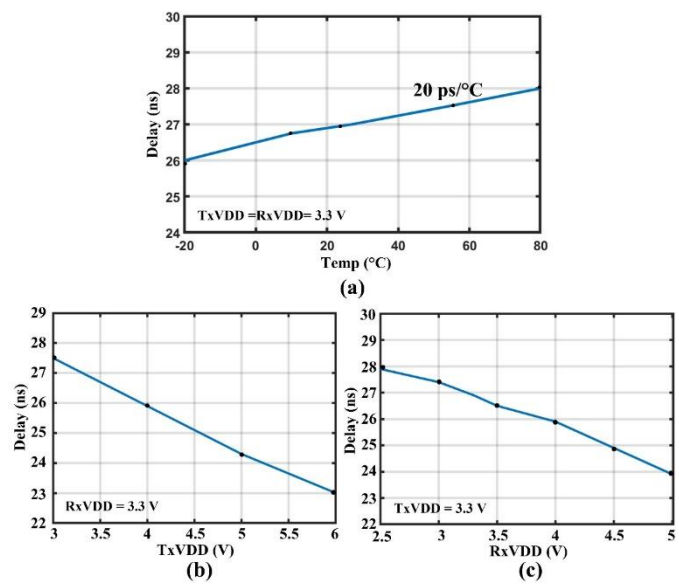


Fig. 11. Propagation delay versus (a) temperature, (b) Tx supply variation, and (c) Rx supply range.

tolerate more than 900 V of isolation voltage V_{iso} over a lifetime of 20 years.

Fig. 8 demonstrates the measurement setup being employed to test the common-mode transient immunity (CMTI). An HV pulser being connected between the Tx and Rx grounds generates pulses with a peak-to-peak value equal to the HV DC supply. To measure a fully isolated environment, an off-package isolated DC-DC converter "RM-3.305S" is employed to power up the Tx side. The ground level between the Tx and Rx dies is oscillated with 630 V and 12 kV/µs slew rate CMTN. The DEI PVX-4140 is equipped with a 1:1000 divider socket for monitoring the generated pulse since an oscilloscope cannot probe the high-voltage pulses. The CMTI test results for the rise and fall of transient noise during low and high output pulse are shown in Fig. 9 and a CMTI of 12 kV/µs is achieved for the Hall-based digital isolator. Although the simulation result of Fig. 6 demonstrates 100 kV/µs of surge immunity, higher CMTI measurement could not be achieved in this article due to the limited voltage of HV DC supply test equipment.

Current consumption variation with respect to bitrate is demonstrated in Fig. 10. For measurement purposes, in this work, connections between the Tx circuit and the integrated coil located on the Rx chip are made through the PCB of the measurement setup, which adds extra parasitic on the transmitter nodes. This increases the Tx consumption, particularly at higher bitrates. The reported bitrate is measured at supply voltages of 3.3 V and an input signal of 10-MHz square wave (equivalent to 20 Mbps toggle pattern).

Fig. 11(a) demonstrates the variation of propagation delay respective to temperature. At room temperature, 27 ns propagation delay is obtained which varies with the rate of 20 $\frac{ps}{°C}$. Propagation delay with respect to supply variation of Tx and Rx circuits is also shown in Fig. 11(b-c). Increasing supply voltage on the Tx side forces more current through the coil and increases the magnitude of the received signal on the Rx side, so it decreases the delay. The achieved data rate, as well as delay, are bounded by the bandwidth of the LNA which limits

the OOK modulation frequency, and further increase of the modulation frequency can increase the bitrate and lower the delay.

The performance summary of the work is shown in Table II. For purpose of comparison, medium-bitrate industrial products and the smallest transmitter size arts are selected. Kaeriyama et al. [15] presented the smallest on-chip coil for an inductive digital isolator. The reported Hall-based digital isolator, in comparison with other arts, has the smallest transmitter area. Unlike transformer-based or capacitive-based isolators, this approach does not require a secondary coil or a capacitive plate and allows the Rx circuitry to be fabricated under the coil which further reduces the consumed area. These miniaturizations make the device suitable for multi-channel digital isolators. Unlike GMR/TMR-based digital isolator that uses layers of ferrite material, this approach uses no proprietary process which makes it cost-effective.

Integration in a smaller process with more metal layers (i.e. 130 nm) helps reducing the coil area by doubling the layers of the integrated spiral coil to maintain the magnetic field strength; thicker oxide would also increase the V_{iso}, and inherently lower noise and supply voltage of smaller processes can reduce the power consumption. Finally, the silicon on isolator process helps isolating n-p wells and avoids crosstalk in a multi-channel isolator.

V. Conclusion

To the author's best knowledge, the reported work is a proof of concept of an approach in using integrated CMOS Hall sensors in digital isolators. The proposed architecture serves applications including clock recovery, isolated DC-DC converter, and I^2C with the maximum bitrate of 20 Mbps. The miniature footprint of the transmitter coil as well as the miniature size of the Hall sensor that allows placement of the receiver circuitry under the coil are unique parameters that significantly reduced the CMOS area and make the approach suitable for multi-channel digital isolator and dense integration. The design achieves a CMTI of greater than 12 kV/µs with a propagation delay of 27 ns.

The applied methodology in sensor implementation enabled the sensor to receive the on-off keying (OOK) modulation frequency of 100 MHz which is beyond most of the reported frequency response of Hall sensors. Although the implemented approach is not yet suitable for high or ultra-high bitrate applications, further increase of the bitrate is achievable by the methodologies described in this article for conserving the Hall plate bandwidth and modification of the receiver circuitry.

References

[1] G. Liu, B. Chen, and X. Song, "High-Precision Speed and Position Estimation Based on Hall Vector Frequency Tracking for PMSM With Bipolar Hall-Effect Sensors," *IEEE Sens. J.*, vol. 19, no. 6, pp. 2347-2355, 2019, doi: 10.1109/JSEN.2018.2885020.

[2] A. Ajbl, M. Pastre, and M. Kayal, "A Fully Integrated Hall Sensor Microsystem for Contactless Current Measurement," *IEEE Sens. J.*, vol. 13, no. 6, pp. 2271-2278, 2013, doi: 10.1109/JSEN.2013.2251971.

[3] J. Kim and S. Jo, "Modeling of giant magnetoresistance isolator for high speed digital data transmission utilizing spin valves," *Journal of Applied Physics - J APPL PHYS*, vol. 97, 05/15 2005, doi: 10.1063/1.1853913.

[4] S. Ma, J. Feng, T. Zhao, and B. Chen, "A Fully Isolated Amplifier Based on Charge-Balanced SAR Converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 6, pp. 1795-1804, 2018, doi: 10.1109/TCSI.2017.2767678.

[5] S. K. Biswas, B. Basak, and K. S. Rajashekara, "Gate drive methods for IGBTs in bridge configurations," in *Proceedings of 1994 IEEE Industry Applications Society Annual Meeting*, 2-6 Oct. 1994 1994, vol. 2, pp. 1310-1316 vol.2, doi: 10.1109/IAS.1994.377589.

[6] *"Gauging LED lifetime in optocouplers"*. [Online]. Available: https://www.machinedesign.com/news/gauging-led-lifetime-optocouplers. Accessed: June 2021.

[7] D. Mittleman, J. Cunningham, M. Nuss, and M. Geva, "Noncontact semiconductor wafer characterization with the terahertz Hall effect," *Applied Physics Letters*, vol. 71, pp. 16-18, 1997.

[8] R. S. Popoviū, *Hall effect devices: R.S. Popoviū*, 2nd -- ed. (no. Book, Whole). Bristol, [Angleterre]: Institute of Physics Publishing, 2004.

[9] S. S. Mirfakhraei, Y. Audet, A. Hassan, and M. Sawan, "A Galvanic Isolated Amplifier Based on CMOS Integrated Hall-Effect Sensors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, pp. 1-10, 2021, doi: 10.1109/TCSI.2021.3052476.

[10] M. Crescentini, M. Biondi, A. Romani, M. Tartagni, and E. Sangiorgi, "Optimum Design Rules for CMOS Hall Sensors," *Sensors*, vol. 17, no. 4, 2017, doi: 10.3390/s17040765.

[11] Y. Xu and H.-B. Pan, "An improved equivalent simulation model for CMOS integrated Hall plates," (in eng), *Sensors (Basel)*, vol. 11, no. 6, pp. 6284-6296, June 2011, doi: 10.3390/s110606284.

[12] D. J. Dumin, *Oxide reliability : a summary of silicon oxide wearout, breakdown, and reliability*, [River Edge, NJ]: World Scientific, 2002.

[13] F. Lyu *et al.*, "Performance comparison of cross-like Hall plates with different covering layers," (in eng), *Sensors (Basel)*, vol. 15, no. 1, pp. 672-686, 2014, doi: 10.3390/s150100672.

[14] Z. Tan *et al.*, "A Fully Isolated Delta-Sigma ADC for Shunt Based Current Sensing," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 10, pp. 2232-2240, 2016, doi: 10.1109/JSSC.2016.2581800.

[15] S. Kaeriyama, S. Uchida, M. Furumiya, M. Okada, T. Maeda, and M. Mizuno, "A 2.5 kV Isolation 35 kV/us CMR 250 Mbps Digital Isolator in Standard CMOS With a Small Transformer Driving Technique," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 2, pp. 435-443, 2012, doi: 10.1109/JSSC.2011.2170775.

[16] A. Devices. *High Speed Digital Isolators Using Microscale On-Chip Transformers*. [Online]. Available: https://www.analog.com/. Accessed: June 2021.

[17] *ADuM1310/ADuM1311 Triple-Channel Digital Isolators* [Online]. Available: https://www.analog.com/. Accessed: June 2021.

[18] *Si80xx-1kV three to six-channel digital isolations*. [Online]. Available: https://www.silabs.com/. Accessed: June 2021.

[19] *ISO72x Single Channel High-Speed Digital Isolators Data Sheet Rev. L*. [Online]. Available: https://www.ti.com/. Accessed: June 2020.

[20] *IL01x Low-Power Digital Isolators*. [Online]. Available: https://www.nve.com/. Accessed: Jun 2020.

[21] *HCPL-9000/-0900, -9030/-0930, HCPL-9031/-0931, -900J/-090J, HCPL-901J/-091J, -902J/-092J High Speed Digital Isolators*. [Online]. Available: https://www.broadcom.com/. Accessed: Oct. 2021.