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Fully Integrated Digital GaN-based LSK Demodulator for High-Temperature Applications

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***Abstract*— We present the first Gallium Nitride (GaN)-based demodulator system dedicated to demodulating Load-Shift Keying (LSK) modulated signals that can operate at high temperature (HT). GaN500 technology is adopted to implement the proposed demodulator. Stable DC output characteristics of epitaxial AlGaN/GaN Heterojunction Field Effect Transistors (HFETs) operating at up to 500ºC enable designing HT ICs. Conventional digital gates such as inverters, NAND2, NAND3, delay elements and a D Flip-Flop are employed to implement the proposed demodulator. The demodulation system is fabricated on a 2.67 mm^2 silicon carbide (SiC) substrate and experimentally validated at 160ºC, whereas the building blocks (inverters and NANDs) show a stable operation at HT up to 400ºC. A minimum of 1 V amplitude difference can be detected between the high voltage level (HVL = ± 5 V) and low voltage level (LVL = ± 4 V) of an applied LSK modulated signal to recover transmitted digital data. Two high-voltage supply levels (±14 V) are required to operate the system. Its total power consumption is 3.4 W.**

***Index Terms*—High-temperature ICs, GaN500 HFET, GaN demodulation system, high-temperature digital ICs, wireless sensor, GaN high-temperature characterization.**

I. Introduction

In many industrial applications, such as electrical vehicles and avionics, installing sensors in harsh environments is necessary to monitor critical parameters and to ensure some critical functions. There is a need to limit the complexity of the part of such systems that works in harsh environments. This sets a need for a wireless connection between the parts of the system subject to harsh conditions and external control units where conventional electronic technologies can be used. Conventional electronic technologies, such as silicon, cannot support the implementation of wireless transmission systems at temperatures exceeding 150ºC. By contrast, wide bandgap (WBG) semiconductors, especially gallium nitride (GaN) and silicon carbide (SiC), are very promising candidates to implement HT ICs [1, 2].

GaN offers key features, including a wide bandgap (3 eV), high drift-saturation velocity, high thermal-conductivity, and low intrinsic carrier concentration [3]. Several GaN devices were implemented and tested at HT, including AlGaN/GaN HEMT (400ºC) [4, 5], AlGaN/GaN MOS-HEMT (500ºC) [6] and InAlN/GaN HEMT (600ºC) [7].

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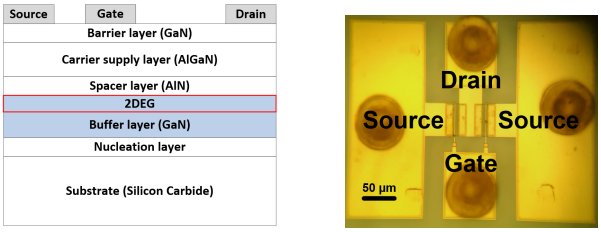

(a) (b)

Fig. 1. GaN500 device: (a) Not to scale cross-section architecture, and (b) Top view topography.

Despite considerable advances in GaN processing and their ability to operate at HT, only few published works have reported implementation of GaN-based HT ICs. For instance, an inverter and ring oscillator were demonstrated at 200ºC in [8], quantizer and flip-flop circuits were tested at 250ºC in [9], and an integrated gate driver was successfully tested at 250ºC in [10]. In addition, a GaN-based pulse width modulation circuit was developed and tested at 250ºC in [11].

In this paper, we present a novel fully integrated digital GaN-based demodulation system that can recover digital signals from an LSK modulated signal. The system aims to serve wireless sensing applications that must operate in HT environments. LSK modulation is adopted to provide power and data transfer using a single inductive link. The fabrication process and HT characterization of the adopted GaN500 devices are presented in Section II. While the design of the demodulation system and corresponding building blocks are provided in Section III. Section IV presents experimental measurements made using the proposed demodulator, and our main conclusions are summarized in Section V.

II. GaN500 Device Performance

A. GaN500 design and processing:

The adopted GaN500 technology is processed at the Canadian Photonics Fabrication Center (CPFC) of the National Research Council Canada (NRC). This technology offers Heterojunction Field Effect Transistors (HFETs), Metal-Insulator-Metal (MIM) capacitors and nichrome resistors. A simplified cross-section of the epitaxial layers of GaN500 HFET is shown in Fig. 1(a). GaN500 technology features double fingers 0.5 µm long metal gates (Fig. 1(b)). Further

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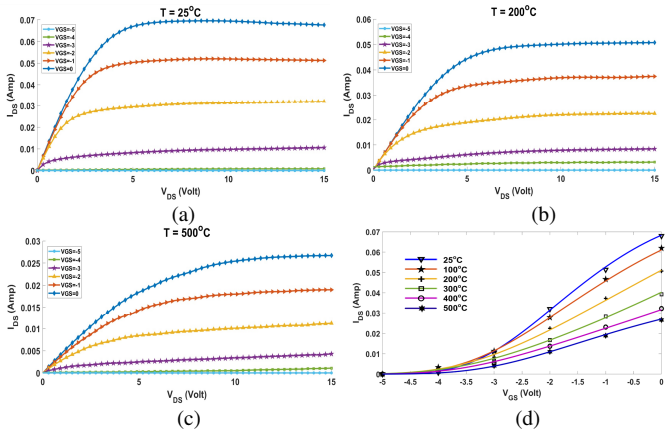

Fig. 2. I-V characteristics of GaN500 at: (a) 25°C, (b) 200°C, (c) 500°C, and (d) I_{DS} versus V_{GS} at different temperatures with V_{DS} = 14 V.

information about the fabrication process are available in [5].

B. GaN500 HT characterization:

The DC output characteristics at 25°C of the adopted GaN500 HEMT device are shown in Fig. 2(a). The gate width of tested device is 20 µm with gate length 0.5 µm. These plots were obtained by sweeping the drain-source voltage (V_{DS}) from0 to 15 V at different values of gate-source voltage (V_{GS}) stepping down from 0 to -5 V (step = 1 V). The maximum drain current (I_{DSmax}) is 70 mA at V_{GS} = 0 V, and the threshold voltage (V_T) is -4 V. This V_T remains stable with negligible change at high temperature up to 500°C. As shown in Fig. 2(b-c), the DC output characteristics at HT (200°C and 500°C) presents a drop in I_{DSmax} from 70 mA at 25°C down to 27 mA at 500°C. These results ensure the functionality and robustness of GaN500 devices at HT. Also, as shown in Fig. 2(d), the threshold voltage of GaN500 is remarkably stable around V_T = -4 V over the wide temperature range. However, the implemented design based on GaN500 should consider the impact of the drop in I_{DSmax} at HT on the design performance.

III. GaN Demodulator Design

The proposed demodulator is designed to recover digital data embedded into an LSK modulated signal. Fig. 3 shows the main blocks of a wireless power and data transmission system exploiting LSK, and an inductive link to perform wireless power transmission bridge between primary and secondary coils L1 and L2. The carrier power signal is modulated by a digital signal controlling a load impedance shunting L2, which reflects into two levels of amplitude (0 and 1) of the carrier signal on the primary side (L1). The role of the demodulator block is to recover the modulating digital signal from the modulated carrier signal.

A. Proposed digital demodulator:

The block diagram of the proposed GaN-based demodulator is shown in Fig. 4. Four digital cells are employed, including two inverters, a delay block, and a D Flip-Flop. The received modulated signal (IN) is applied in parallel on both inverters INV-D and INV-K. INV-D is carefully designed to detect the input signal "IN" only during the high amplitude zone "1" and to remain off during the low amplitude zone "0".

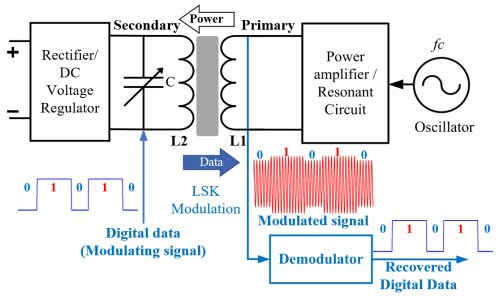

Fig. 3. Block diagram of a LSK-based wireless power and data transmission system.

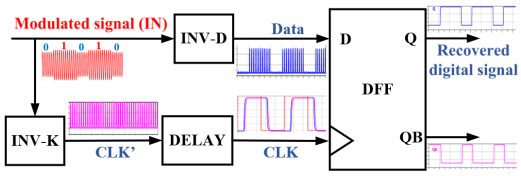

Fig. 4. Block diagram of proposed demodulation system.

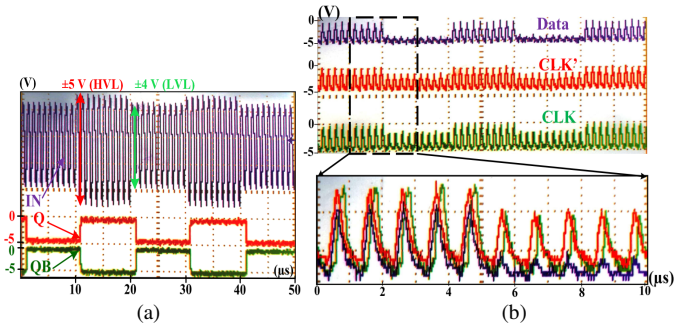

Fig. 5. Experimental validation of proposed demodulator at 25°C: (a) recovered digital signals (Q, QB), and (b) internal signals (Data, CLK', CLK).

The output signal of INV-D "Data" is applied to the D Flip-Flop, which is acting as an envelope detector, to filter out the carrier signal from the modulating digital data. To do that, the clock signal of the D Flip-Flop should be synchronized with the carrier frequency (f_c) to sample "Data" and perform the envelope detection of the digital signal. Consequently, the required clock is generated by INV-K, which is designed to switch continuously at f_c, regardless of the amplitude value of "IN". To ensure the sampling of "Data" by the generated clock, "CLK'" is slightly delayed passing through a delay circuit. The D Flip-Flop uses "Data" and "CLK" signals to deliver the recovered digital signal "Q" and its complement "QB".

Fig. 5(a) presents the experimental validation of the developed digital demodulator at 25°C. The two voltage levels of modulated signal "IN" are the high voltage level (HVL) = ± 5 V and the low voltage level (LVL) = ± 4 V respectively. Fig. 5(b) shows "Data", "CLK'" and "CLK" signals provided by INV-D, INV-K and DELAY respectively. The enlarged zone of Fig. 5(b) shows the synchronization of "CLK'" with "Data" and the matching between the delayed clock "CLK" and "Data". The following sections elaborate on the design of each building circuit and demonstrate their functionality at room temperature and HT.

B. Inverters:

The inverter is the principal building block to design the other circuits as well as the demodulator. As shown in the

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schematic of Fig. 6(a), the input signal (IN) of the inverter controls a GaN driver device. The latter has a drain current limited by a resistor in series to maintain a low power consumption. The remaining part of the circuit performs the role of a voltage level shifter that ensures the voltage level of the output signal (OUT) to be compatible with the input of the next logic circuit stage.

The following are the applied testing conditions: Input logic low = −5 V, input logic high = 0 V, VDD=+14 V and VSS=-14 V. The ±14 V are found to be the best supplies that ensure a stable operation of designed digital ICs. These supplies are required to let the level shifters ensure the compatibility between the output of one digital circuit and the input of the following digital circuit. In Fig. 6(b), the inverter shows a stable pulse response with no significant temperature effect up to 300°C (overlapping plots). Between 300°C and 500°C, the output logic low state (LS) is still stable at -5 V, but the output logic high state (HS) decreases from its initial value (0 V at 25°C) by 20% (of low-to-high difference) at 400°C and 60% at 500°C. In addition, an increase in the rise time was noticed, which is possibly due to a surface trap charge activation, but this phenomenon needs further detailed studies. In parallel, as shown in Fig. 6(a), the temperature has a direct proportional impact on the resistance value of integrated resistors. The significant increase of the resistance value with temperature would certainly affect the voltage level of the signal applied on the level shifter. Consequently, the HS of the output signal decreases significantly at HT as shown in Fig. 6(b).

Fig. 6(c) shows the voltage transfer characteristic (VTC) of the implemented inverter at room temperature. The main DC characteristics of the inverter can be obtained from that VTC, including the maximum output voltage in the low state (LS_{max}), the minimum output voltage in the high state (HS_{min}), the logic gate threshold voltage (VLT), the voltage gain (Gain), the noise margin for the low state (VNML), and the noise margin for the high state (VNMH). Fig. 6(d) shows the VTC of the inverter between 25°C and 500°C and Table I summarizes the six DC performance metrics for all measured temperatures. Up to 300°C, the gain and output voltage are remarkably stable. Beyond this temperature, the logic high-state HS_{min} varies significantly with temperature.

Back to the demodulation system, when (IN) is applied on INV-D and INV-K, each inverter switches when the voltage level of "IN" is around its own VLT. As shown in Table I, the VLT is mainly around -3 V. Therefore, the effective part of "IN" is only the negative voltage part, whereas the positive voltage part is always considered to be at HS and is converted to LS at the output of inverters.

In parallel, both HVL and LVL of "IN" are recommended to be as close to each other as possible to ensure higher power transfer efficiency during LSK modulation. Therefore, the studied modulated signal "IN" has HVL = ±5 V and LVL = ±4 V. Consequently, INV-D is designed to have VLT between -5 V and -4 V switching to HS only when the input signal is in the HVL zone. In parallel, to generate the clock signal of the D Flip-Flop, INV-K is designed with VLT lower than -4 V to continuously switch to HS in both HVL and LVL zones.

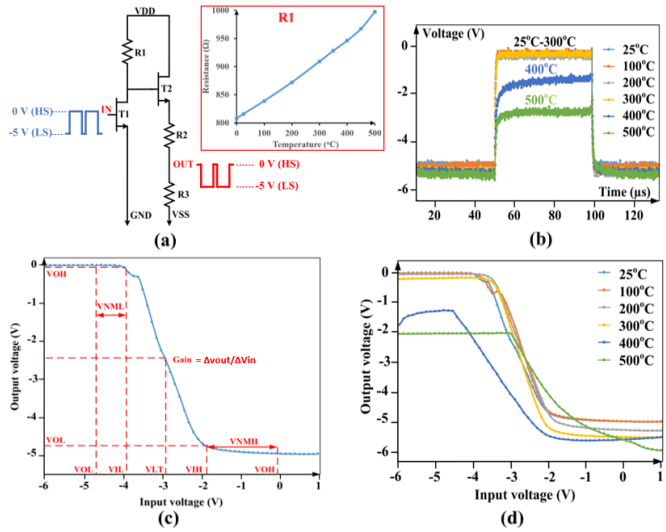

Fig. 6. Characterized inverter: (a) Schematic design, (b) Pulse characteristics over the temperature range 25- 500°C, (c) VTC at 25°C, and (d) VTC between 25°C and 500°C.

TABLE I
DC PERFORMANCE PROPERTIES OF A GAN INVERTER

	25°C	100°C	200°C	300°C	400°C	500°C
V_{OL}	-4.7	-4.66	-5	-5.2	-5.46	-5.87
V_{LT}	-2.9	-2.68	-3	-3	-3.27	-2.68
V_{OH}	-0.1	-0.11	-0.24	-0.33	-1.28	-2
Gain	-3.7	-3.9	-3.4	-3.9	-2	-2.2
V_{NML}	0.9	0.8	1.5	1.7	0.89	2.2
V_{NMH}	1.7	1.85	1.48	1.51	0.8	-

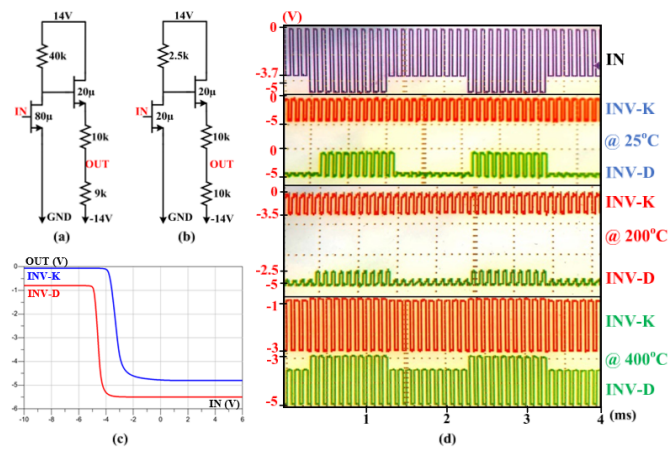

Fig. 7. Inverters INV-D and INV-K: (a) Schematic of INV-D, (b) Schematic of INV-K, (c) VTC of INV-D and INV-K, (d) Experimental validation.

The VTC of INV-D and INV-K are shown in Fig. 7 (c) with VLT of -4.5 V and -3.5 V for INV-D and INV-K respectively. The gate length of all transistors is 0.5µm and the gate width of each transistor is mentioned in Fig. 7(a) and (b) in addition to the values of integrated resistors. At higher temperature, the VLT of both inverters decreased to lower values up to -5 V and -4 V for INV-D and INV-K respectively at 400°C. This variation affects the functionality of the inverters during demodulation. As shown in Fig. 7(d), the HS and LS of INV-K are reduced with temperature to reach -1 V and -3 V respectively at 400°C. A similar impact of HT is observed on the performance of INV-D, with HS = -3 V and LS = -5 V at 400°C in addition to the appearance of undesirable pulses during the LVL zone.

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C. Delay block:

The implemented delay element shown in Fig. 8(a) comprises 20 inverters in series to provide the required delay for the recovered clock "CLK'" from INV-K. This time delay is required to ensure the intersection of the clock with the detected "Data" from INV-D. A 20 pF capacitor is added to the output of each stage of the inverters chain to obtain a delay of 125 ns with a minimum number of inverters. This delay is appropriate to sample "Data" at f_c = 10 MHz. To cover a wide range of carrier frequencies (1-10 MHz), 5 output signals (OUT_{1-5}) are extracted from the Delay circuit as shown in Fig. 8(a). An average delay of 25 ns is obtained between each two successive output stages of the delay block. Fig. 8(b) shows an almost constant delay introduced by the delay element (OUT_1, OUT_5) at different temperatures. This delay increases only by 20% at 160°C, compared to its value at ambient temperature. Above 160°C, the delay circuit stopped working due to the significant shift of HS and LS of internal inverters.

D. D Flip-Flop:

The schematic building block of the implemented D Flip-Flop is shown in Fig. 9(a), where 5 NAND2 and 1 NAND3 are employed. The schematic design of these NAND logic gates is presented in Fig. 10(a), where two series GaN devices are used in the driver stage of the NAND2 gate and three series GaNs are used to form the core of NAND3 gate. Fig. 10(b) shows the dynamic characteristics of the NAND2 between 25°C and 400°C (a similar behavior was observed for the NAND3). Above this range, the difference between the HS and LS output voltage reduces to inadequate levels. Although the NANDs show an acceptable functionality at 400°C, the D Flip-Flop does not operate above 160°C, as shown in Fig. 9(b). This is due to shifts of inputs and outputs levels of the NANDs. This corresponds to the shrinking of HS and LS pulse duration on the internal input/output signals.

IV. Test Setup and Experimental Results

A. HT measurement setup:

The GaN500 chips were diced at NRC. A regular ceramic dual in-line (DIL) package is used to perform the measurements. Die attachment is performed using Silver Epoxy (EPO-TEK H20E-PFC) from EPOXY TECHNOLOGY. This material is electrically and thermally conductive and it is qualified to operate at temperatures up to 325°C. Above this temperature, the epoxy starts losing its rigidity and may even melt. To perform testing at higher temperature, the tested package was maintained in a stable horizontal position to prevent die dislocation.

The measurement setup shown in Fig. 11 was built to perform circuit characterization at high temperatures. The heating chamber of the furnace can reach 1000°C. It has two top openings where HT cables are installed to connect the tested packages to the external measurement devices. The HT cables are Nickel-Plated Copper conductors that can endure 450°C. The ball bonder wires have a 25 µm diameter. Ball bonding is performed using an ASM Pacific Technology wire bonder

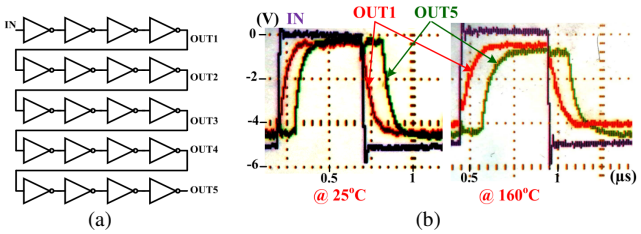

Fig. 8. Delay circuit: (a) Schematic design, and (b) Experimental validation.

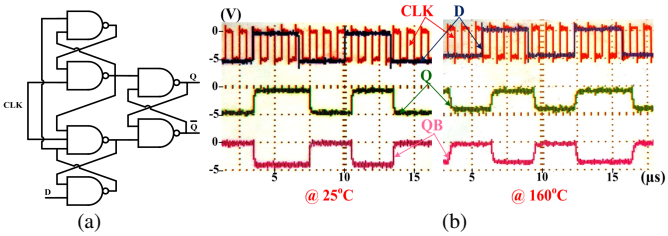

Fig. 9. D Flip-Flop circuit: (a) Block diagram, and (b) Experimental validation.

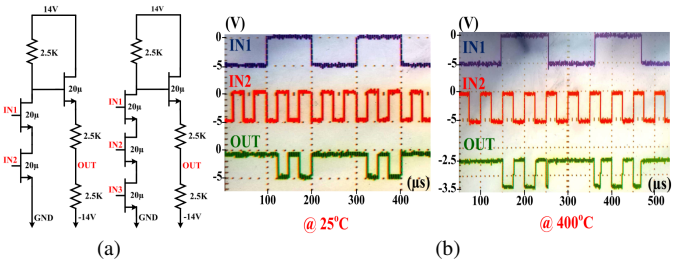

Fig. 10. (a) Schematic design of NAND2 (left) and NAND3 (right), and (b) Experimental validation of NAND2.

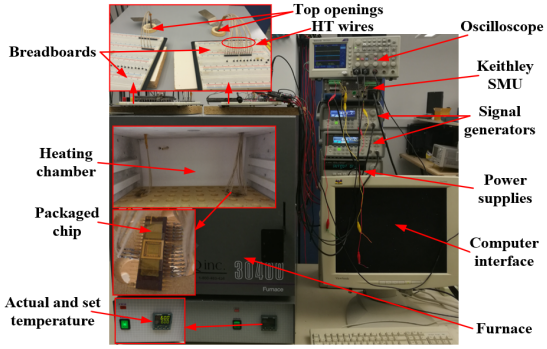

Fig. 11. Experimental setup of HT measurements.

(model Eagle Xtreme). Conventional breadboards are used to connect the HT part (packaging and wiring) with the measurement instruments. The latter provide the necessary input signals and supply voltages to monitor the signals received from the tested chips.

The measurements were performed using a 2-channel Keithley SMU to obtain the I-V characteristics of GaN500 transistors and Agilent 4294 Impedance Analyzer to measure the values of integrated capacitors. Two signal generators were used to test the functionality of the digital modules. DC power supplies were used to deliver the appropriate low and high DC voltage levels and a Tektronix oscilloscope was utilized for data acquisition and to monitor measured waveforms.

B. HT validation of digital demodulator:

A micrograph of the implemented demodulator is shown in Fig. 12, where the system occupies a total area of 2.67 mm^2. Measured waveforms obtained at HT are provided in Fig. 13.

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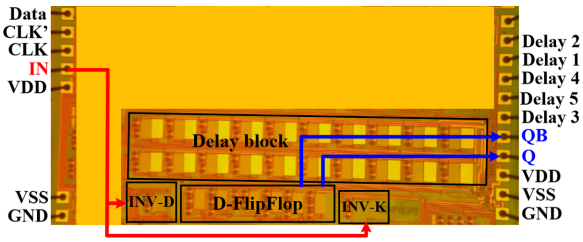

Fig. 12. Micrograph of the proposed demodulation system.

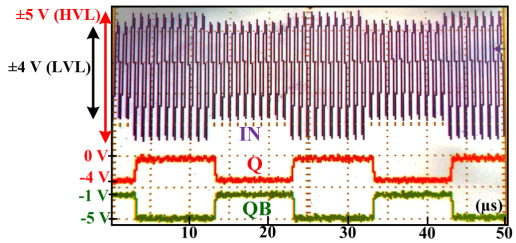

Fig. 13. Experimental validation of proposed demodulator at 160ºC.

TABLE II
GAN ICS WITH MAXIMUM OPERATING TEMPERATURE

GaN technology	Reported ICs	Temp	Year	Ref.
3µm E-mode GaN MIS-HFET	Gate driver	250ºC	2019	[10]
0.5µm E/D-mode GaN HEMT	Inverter, ring oscillator	200ºC	2017	[8]
E/D-mode GaN HEMT	Pulse width modulation (PWM)	250ºC	2015	[11]
E/D-mode GaN HEMT	2-level quantizer and S/R flip-flop	250ºC	2012	[9]
0.5 µm D-mode GaN HEMT	NOT, NAND	400ºC	2020	This work
	D Flip-Flop, DELAY, Demodulator	160ºC		

The applied modulated signal was stimulated with f_c=1 MHz carrier frequency using HVL and LVL of ±5 V and ±4 V respectively. The digital system was able to recover the digital data Q and its complementary QB at different temperatures up to 160ºC. Beyond this temperature, the demodulator is no longer stable and could not operate properly.

Based on the performed HT characterization results (Section II-B) and the HT validation of digital circuits (Section III), the operating temperature of the implemented demodulator could easily be extended above 160ºC. This could be done by extracting an adequate HT model of GaN devices and integrated resistors. Such improved HT device model would enable the simulation and prediction of HT impact on the implemented circuits during the design phase. From an improved device model, an adapted design that can handle the HT effect maintaining the functionality of the complete system could be obtained.

In addition, the applied HVL and LVL are selected to be the critical case of the modulated signal. In other words, HVL and LVL could be higher than ±5 V and lower than ±4 V respectively. Moreover, as mentioned in section III-b, f_c could be higher than 1 MHz (up to 10 MHz) by selecting a signal from the delay block that is less delayed. Doing that, the number of stages of the delay block could be reduced to significantly reduce the power consumption and occupied area.

The total power consumption (3.4 W) and area (2.67 mm^2) of the digital demodulator are dominated by the DELAY block, which should be optimized in future work. A summary and comparison of our work with recently published work exploiting GaN-based HT ICs and systems is presented in Table II. The basic building blocks of our circuit (NOT and NAND) worked robustly up to 400ºC. The proposed demodulator system showed stable operation up to 160ºC. Clearly, better high temperature models of internal circuits could allow extending the highest temperature at which the demodulator operates correctly if they were considered in the design phase.

V. CONCLUSION

A novel GaN-based demodulation system has been successfully demonstrated at temperatures ranging up to 160ºC. Basic cells implemented with the GaN500 technology were characterized and shown to operate at HT up to 500ºC. A complete LSK demodulator has been implemented using fully digital ICs including NOT, NAND, Delay and D Flip-Flop cells. The basic logic gates showed correct stable performance up to 400ºC. The range of temperatures at which the demodulator operate could be extended well beyond 160ºC if a new version of the design, leveraging improved HT models developed as part of this research, was implemented.

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