GaN-Based LSK Demodulators for Wireless Data Receivers in High-Temperature Applications

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***Abstract*— GaN (gallium nitride)-based fully-integrated demodulators are presented. These modules, intended for wireless applications, target high-temperature (HT) environments including monitoring devices in aerospace. The presented demodulators are dedicated to recover Load-shift keying signals modulating a low carrier frequency to maximize power transfer efficiency and increase data transmission rate through metallic barriers. Logic gates are implemented and successfully tested at HT exceeding 400ºC. Proposed demodulators are built from half and full bridge rectifiers, comparators, voltage references and inverters, and operate at a minimum carrier frequency (f_c) of 50 kHz. A demodulator based on a digital topology is proposed to cover MHz range f_c. A complementary ± 14V supply voltage is required to operate the circuits. Reported post-layout simulation results validate the functionality and performance offered by the proposed demodulators over the 25ºC to 400ºC temperature range. Also, a complete chip layout has been done, where the introduced demodulators occupy 10 mm^2 of a GaN die area.**

***Index Terms*—High-temperature applications, wireless data transmission, GaN HEMT, integrated circuits, demodulation system.**

I. Introduction

IMPLEMENTING electronics that can operate in harsh environments, including high temperature (HT), is needed by many industries such as downhole oil and gas, aerospace and automotive. Cooling solutions for conventional electronics are not always possible and may have negative impact on system reliability and cost. For instance, during well logging, a failed electronics assembly on a drill string operating at deep underground level can take more than a day to retrieve and replace. In parallel, the cost for operating a complex deep-water offshore is around $1M per day [1]. Further, influential corporations like AIRBUS, SAFRAN, and THALES are seeking alternative microelectronic technologies aiming for complete wirelessly controlled systems that can harvest power from the surrounding HT environment, exchange data through wireless links under HT conditions and be integrated in critical high-risk areas.

Among the available semiconductors dedicated for HT applications, wide bandgap (WBG) semiconductors are the main candidates in the foreseeable future to overcome the fundamental physical limits of the other electronics such as silicon on insulator (SOI), gallium arsenide (GaAs) and silicon germanium (SiGe), which are serving a relatively short range of temperature not exceeding 300ºC and for limited operation time [2-4]. Silicon carbide (SiC) and gallium nitride (GaN) are the best-known WBG devices that offer attractive features suitable for HT conditions. These features include wide bandgap (3eV), high-drift saturation velocity, high-thermal conductivity, and low-intrinsic carrier concentration [5].

Several studies have been done recently for SiC semiconductors at HT [6-9]. However, the HT measurements are performed only for devices [7] and circuits [8]. Even in [9], the proposed system represents only the RF transmitter part, where the receiver is a Tektronix RSA3303B real-time spectrum analyzer. In addition, no commercially available SiC integrated devices and circuits operating at temperature higher than 300°C were found [10]. Moreover, the direct temperature dependence of carrier concentration, due to the bulk nature of the active region in SiC devices, is considered as a common shortcoming [11] in addition to the crystal dislocation disorders which degrade junction leakage, particularly at the highest temperatures.

III-Nitride and primarily GaN technologies exhibit substantial performance improvement over SiC semiconductor with respect to response speed and operating temperature limits [12]. In addition, the temperature stability of electron concentration in the HEMT channel makes GaN devices more stable with respect to temperature. Despite considerable efforts to develop GaN devices dedicated to HT applications [12-13], few researches are directed toward the development of integrated microelectronic circuits and systems based on GaN devices. Nowadays, the reported works show the implementation of simple circuits like inverter, comparator, ring oscillator, and one stage differential amplifier [11,14-15].

In our group, the HT characterization of AlGaN/GaN HEMT devices was successfully performed over a 25ºC to 400ºC temperature range as a first step to ensure the ability of using them in circuits and systems design dedicated to HT applications. All information regarding the fabrication process,

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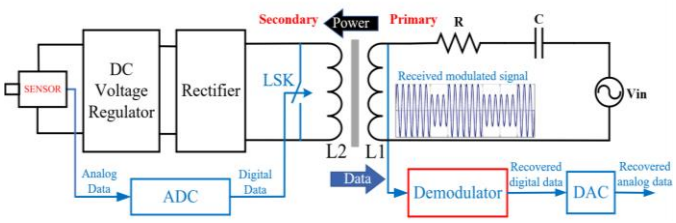

Fig. 1. Block diagram of the proposed power and data transmission system.

materials of the characterized GaN devices and performed HT characterizations were reported in [16]. This GaN-based epitaxial layer Heterojunction FET technology is provided by the Canadian Photonics Fabrication Center of the Canadian National Research Council (NRC). This technology called (GaN500) offers 500nm gate length transistors fabricated on 3-inch SiC wafers. The SiC substrate offers high-thermal conductivity and low-lattice mismatch to the GaN layer, which is compatible with HT applications. In addition to the active devices, the available technology allows the integration of some passive components (resistors, inductors, and capacitors).

In this paper, we present the design and implementation of three complete demodulation systems based on GaN500 technology. These proposed circuits demodulate LSK modulated signals for wireless monitoring applications operating in HT environment. We provide in Section II the main considerations about the adopted GaN technology and circuit design, in addition to the circuit level validation at 400ºC of GaN-based digital circuits. The building blocks, circuits and functionality of the proposed demodulators are discussed in section III, along with the impact of HT on them. Conclusions are the subject of section IV where our contributions are summarized.

II. Design Considerations and Digital Circuits Validation

Figure 1 shows a wireless power and data transmission system based on an inductive link. The power transfer path provides the supply voltage to a sensing device (pressure, temperature) located in a harsh environment. The data transmission path is based on the LSK modulation technique to reduce the complexity of the whole wireless power and data transmission system that operates through a single inductive coupling interface. In the transmitting side (secondary), the analog signal of the sensor is converted into digital data modulating the signal through a controllable switch.

The demodulator, located on the receiving side (primary), detects the received modulated signal and recovers the expected digital data. The modulated signal (Fig. 1) consists of two different amplitude voltage levels; high-level (data-on) and low-level (data-off). The voltage difference between data-on and data-off levels is strongly recommended to be as small as possible to maintain the highest power transfer efficiency during the data transmission process.

A. *Design and technology considerations*

The harsh environment condition of the targeted industrial applications is not only the high-temperature but also the metallic barrier between primary and secondary coils. That metallic barrier is an enclosure encapsulating hot high pressure gases. This metallic barrier (hard steel that can sustain high pressure and high temperature) obviously has fairly high-electrical conductivity and high-magnetic permeability that induce high Eddy current losses and form a shielding zone for inductive fields, respectively. Therefore, the carrier frequency of the applied power signal should be relatively low to obtain enough power transfer efficiency while being sufficiently high to allow an adequate data transfer rate [17].

To endure the HT environment, a GaN500 technology is adopted to build the proposed demodulation system. In this implementation technology transistors are normally-on and they operate as depletion mode devices with a threshold voltage of –4V. This imposes significant design constraints, in particular when the system specifications include limited power budget, and small-system geometry. Thus, it becomes a serious challenge to design a complete demodulation system based on this technology.

Considering the specifications and system constraints we based the circuit design on WBG normally-on devices [9, 15]. Then, a minimum number of transistors was used to obtain the desired functions and for better miniaturization of the complete system. Since GaN500 cells require VGS= -5V to completely switch off the established channel, a negative input logic level is needed to drive the circuits which leads to the necessity of matching the input-output controlling signals. Level shifters are added to solve the incompatibility between the input and output levels and three supply voltage levels are used (VDD = +14V, VSS = -14V, and Gnd).

Despite the promising performance of GaN500 devices at HT, there is still an effective impact of environmental temperature on the active devices [16] and passive components (resistors). For this reason, the proposed design must consider the temperature induced parametric variations of the available components (active and passive) over the expected temperature range that spans from 25ºC to 400ºC. The Keysight Advanced Design System (ADS) kit was used to perform the design and simulation of proposed system where the transistor model (Angelov model configured with several parameters not visible to the user) includes the effects of self-heating and external applied temperature giving the opportunity to simulate the temperature impact on the circuits and system behavior. Similarly, based on the provided Thermal Coefficient of Resistance (TCR) of the integrated resistors (200 ppm/ºC), equation (1) describes the change of resistance values over the temperature range

$$R_t = R_0 (1 + 2\ T10^{-4}) \quad (1)$$

where R_t is the actual resistance, R_0 is the resistance value at room temperature and T is the actual temperature (ºC).

B. *Digital circuits validation at HT*

To validate the concept, several GaN500-based logic gates were implemented and tested at several temperatures between 25ºC and 400ºC. The schematics of the implemented logic gates

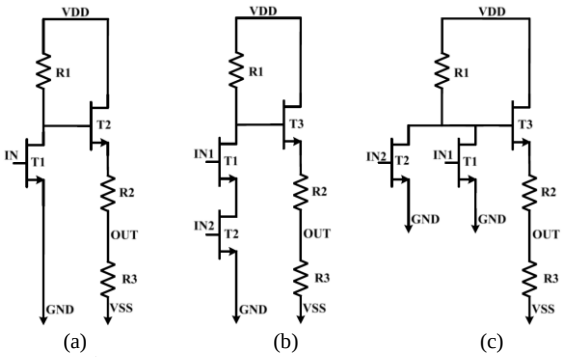

Fig. 2. Circuits of digital logic gates: (a) NOT, (b) NAND, and (c) NOR.

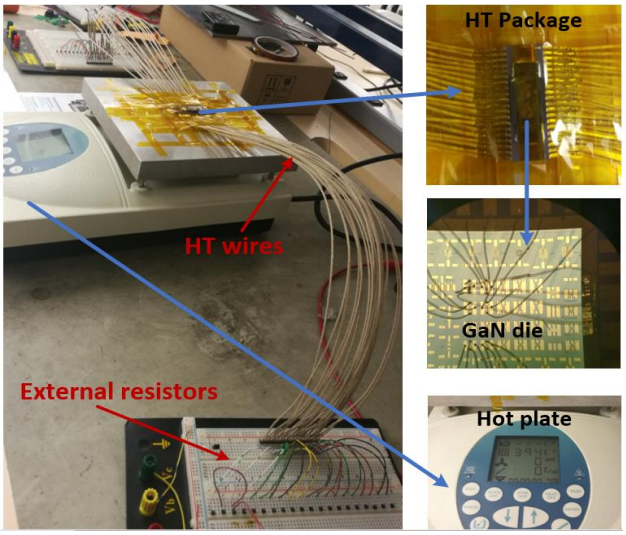

Fig. 3. Experimental setup for digital circuits testing.

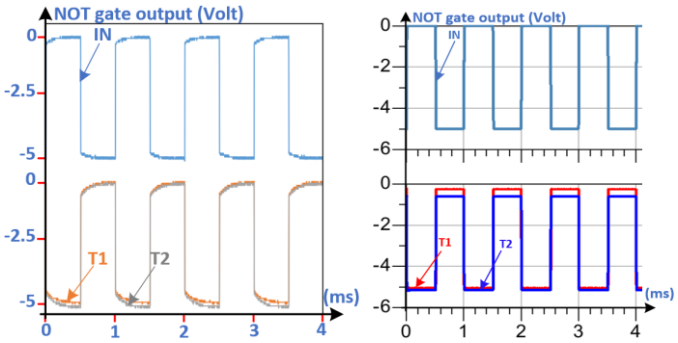

Fig. 4. Experimental (left) and simulation (right) results of NOT gate at 25ºC (T1) and 400ºC (T2).

are shown in Fig. 2. The experimental setup is depicted in Fig. 3 where the GaN500 devices are wire-bonded to the pads of a ceramic HT package and HT wires are used to connect the package to the measurement devices.

It is important to note that the GaN die that was used in those experiments comprises independent devices without resistors. Thus, external resistors were added to the test setup. Consequently, to perform a proper comparison between the experimental and simulation results, the temperature impact is applied only on GaN devices of the simulation kit, keeping the resistors at constant values. The measurements and simulation results are almost equal, thus showing the robustness and functionality over the wide temperature range tested for NOT,

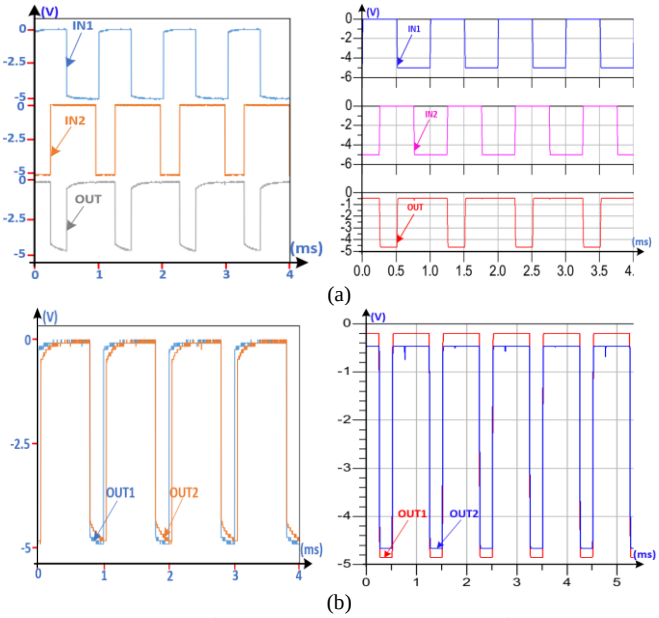

Fig. 5. Experimental (left) and simulation (right) results of NAND gate: (a) at 400ºC, (b) at 25ºC (OUT1) and 400ºC (OUT2).

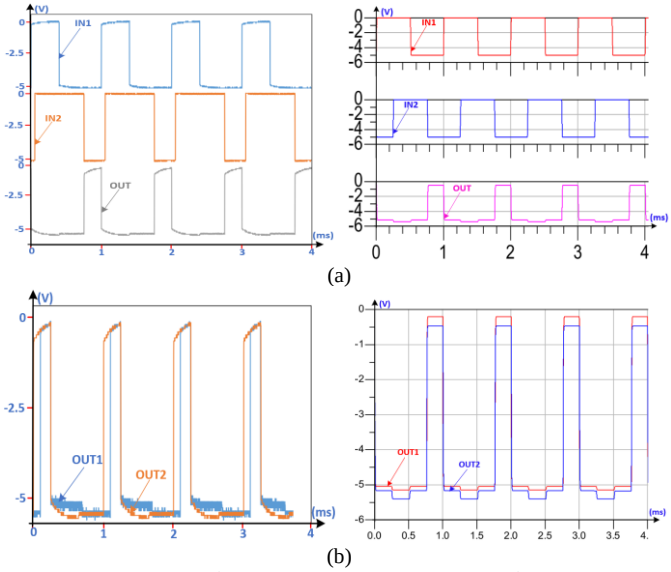

Fig. 6. Experimental (left) and simulation (right) results of NOR gate at: (a) 400ºC, (b) 25ºC (OUT1) and 400ºC (OUT2)).

TABLE I
GAN-BASED CIRCUITS FOR HT APPLICATIONS

	This work	[11]	[14]	[15]
Circuit	NOT, NAND and NOR gates	Dif. Amp. and NOT gate	NOT gate	NOT gate and ring oscillator
Tech.	AlGaN/GaN	AlInN/GaN	AlGaN/GaN	AlGaN/GaN
Foundry	NRC	Inhouse	Inhouse	Inhouse
Temp. (ºC)	400ºC	500ºC	300ºC	256ºC

NAND and NOR gates as shown in Figs. 4, 5 and 6 respectively.

Table I summarizes features of the implemented circuits based on GaN technology targeting HT applications, and it compares them with the only three published works that were found [11, 14-15]. To the best of our knowledge, none of these teams have reported system level design or implementation.

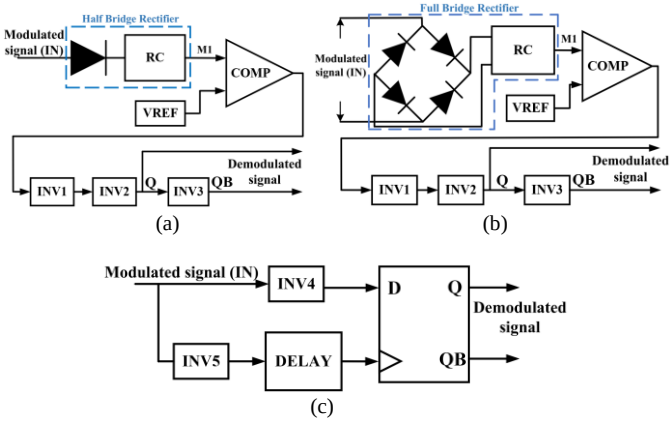

Fig. 7. Block diagrams of the proposed demodulators: (a) Half-bridge rectifier, (b) Full-bridge rectifier, and (c) Digital based.

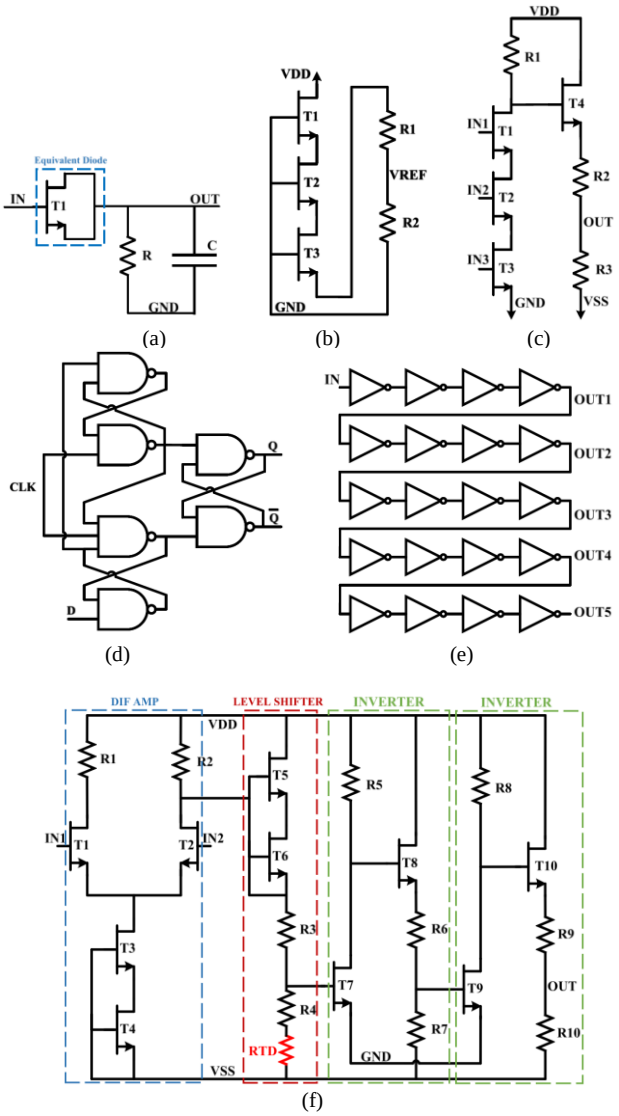

Fig. 8. Building circuits: (a) Half bridge rectifier, (b) Voltage reference, (c) NAND (3IN), (d) D-Flip Flop, (e) Delay, and (f) Comparator.

III. Proposed Demodulation Systems

A. Building blocks and functionality

Figure 7 presents the block diagram of the three proposed demodulation systems. The first demodulator is presented in

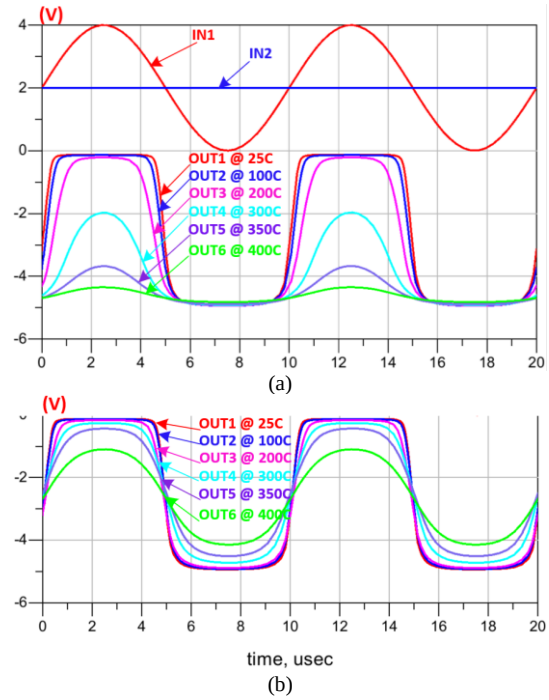

Fig. 9. Comparator simulations at different temperatures: (a) Without adaptation, and (b) With adaptation.

Fig. 7(a) where the modulated signal (IN) is applied to a half-bridge rectifier (HBR) followed by a bank of RC circuits that play the role of envelope detector and that shape the modulating signal (M1). The latter is compared to a reference voltage (VREF=2.6V) using a comparator block. Three inverters (INV1, INV2 and INV3) are used to sharpen the comparator output signal and to generate the initial digital data (Q) along with its complementary signal (QB). Q and QB are needed by a DAC block (Fig. 1) to recover the initial analog signal. The building circuit schematics of the half bridge rectifier (HBR) demodulator are provided in Fig. 2(b) (2IN-NAND) and Fig. 8(a) (half bridge rectifier), (b) (voltage reference) and (f) (comparator).

The minimum carrier frequency that could be handled by the HBR demodulation system is 60 kHz. Lower than this limit, the difference between data-on and data-off signals provided by the HBR could not be sensed by the comparator. To go beyond this limit, a full bridge rectifier (FBR) is utilized instead of the HBR keeping the remaining building circuits without any change (Fig. 7(b)). The FBR demodulation system operated properly at a carrier frequency as low as 50 kHz.

Another demodulator is fully based on digital circuits and is proposed for high carrier frequency applications (in the range of MHz). The block diagram of this digital demodulator is presented in Fig. 7(c). The novel idea of this demodulator is to use an inverter (INV4) which is carefully designed to detect only the data-on (high-amplitude voltage) and discard the data-off (low-amplitude voltage) of modulated signal. On the other hand, INV5 is used to switch continuously in both data-on and data-off cases to generate the clock signal of D-Flip Flop. This clock signal is delayed by the DELAY block to ensure matching with the detected data signal. For lower carrier frequency operation (range of kHz), a longer delay should be designed.

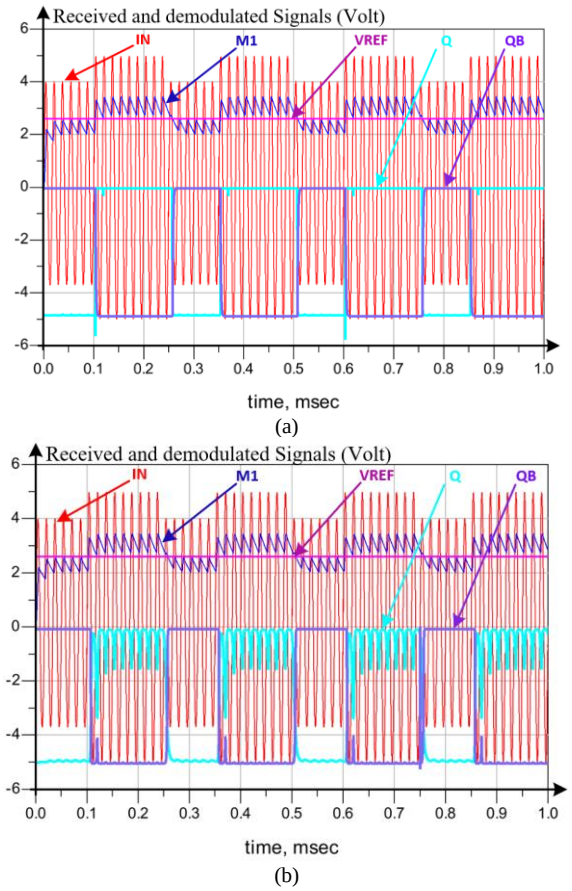

Fig. 10. HBR demodulator simulation results at: (a) 25ºC, and (b) 400ºC.

Figure 2(a) (2IN-NAND) combined with Fig. 8(d) (D-Flip Flop) and (e) (delay) shows the building circuit schematics of the digital demodulator. A long chain of inverters (20 stages) is utilized to design the DELAY block (Fig. 8(e)) and the D-Flip Flop design is based on five 2-input and one 3-input NAND logic gates, where the corresponding schematic design is shown in Fig. 2(b) and Fig. 8(c), respectively.

B. Simulation results

During the investigation of HT impact on the performance of each building circuit, we noticed that the comparator is the block most affected by HT operation, much more than the other circuits. As can be seen in Fig. 9(a), the comparator output fails dramatically after 250ºC. The circuit analysis shows the sensitivity of the comparator performance with the value of R4 (Fig. 8(f)). A resistive temperature detector (RTD) [9] is added in series to R4 to compensate the temperature impact. Due to its high-temperature coefficient and very linear temperature response from room temperature up to 500°C, the RTD made of platinum is an ideal candidate for our case. The new performance of the adapted comparator is presented in Fig. 9(b).

To validate the three proposed demodulators, a modulated signal (IN) is applied to retrieve the demodulated signal (Q) and its complement (QB). The system analysis shows that the minimum amplitude of the data-on signal is +-5V. This means that, to reach a higher power transfer efficiency, the amplitude of the data-on signal could be increased more than +-5V as much as needed until reaching the required power transfer efficiency, without applying any change on the proposed demodulators.

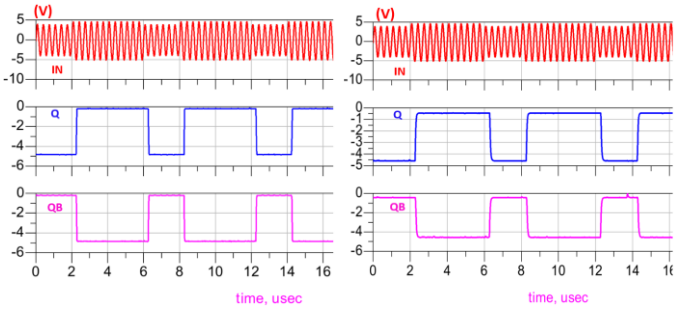

Fig. 11: Digital demodulator simulation results at: (a) 25ºC, and (b) 400ºC.

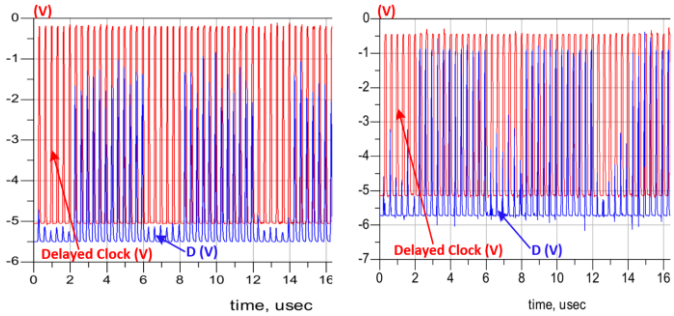

Fig. 12: Delayed clock and detected data intersection at: (a) 25ºC, and (b) 400ºC.

In parallel, the maximum amplitude of the data-off signal is +-4V and it could be less than that, but it would reduce the power transfer efficiency. Therefore, the modulated signal (IN) is selected with high-amplitude of +-5V (minimum data-on) and low-amplitude of +-4V (maximum data-off) to show the performance of modulators at the critical case. Consequently, a 1.0V amplitude difference (20% of the maximum amplitude) reached between the high-amplitude (data-on) and low-amplitude (data-of) of the modulated signal (IN) with the proposed demodulators.

Figure 10(a) presents the transient performance of the HBR demodulator at 25ºC. To ensure the reliability of the proposed demodulation system, simulations were repeated after applying the HT GaN500 model (Angelov model) and resistor values (using equation 1). At carrier frequency 60kHz, the simulation results at 400ºC shown in Fig. 10(b) are compatible with the results at 25ºC in Fig. 10(a) except for the ripples in the recovered signal (Q). These ripples could be easily solved by adding a small capacitor (C=10pF) at the output of INV2. Similar simulation results were obtained with the FBR demodulation system at a carrier frequency of 50kHz. In parallel, the simulation results of the digital demodulator with carrier frequency of 4MHz are presented at 25ºC and 400ºC in Figs. 11(a) and (b) respectively, where an excellent stability is shown. The detected data (D) of inverter (INV4) is presented in Fig. 12(a) and (b) at 25ºC and 400ºC respectively, along with the delayed clock signal generated from inverter (INV5).

A complete chip layout (Fig. 13) for the three proposed demodulators was performed. The overall area of the chip is

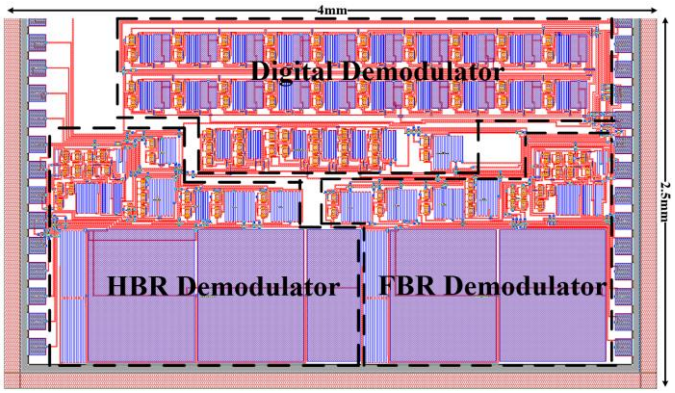

Fig. 13: Chip layout view of the proposed data transmission systems.

TABLE II
POWER CONSUMPTION AND AREA OF PROPOSED DEMODULATORS

Demodulator	Frequency (MHz)	Power (W) @ 25°C/400°C	Area (mm^2)
HBR	>0.06	0.77/0.42	2.24
FBR	>0.05	0.84/0.46	1.9
Digital	>1	4.3/4	2

4.0mm x 2.5mm. Table II summarizes the operating frequency, power consumption and occupied area of each module. The high-power consumption and large area of the digital demodulator are due to the Delay block which should be optimized in future work. As shown in Table II, the HT has a positive impact on power consumption especially for HBR and FBR demodulators with power reduction of more than 40% at 400ºC.

IV. CONCLUSION AND FUTURE WORK

The design and implementation of three different demodulators based on GaN500 devices are described. The introduced building blocks are designed to fit into wireless power and data transmission systems based on the LSK modulation technique targeting harsh environments and high temperature application HT environment. The design considerations of the proposed modules are discussed considering the specific requirements of the targeted applications and the limitations of adopted technology. Circuit validation of GaN-based logic gates was performed at 400ºC. Simulation results of proposed systems were performed to ensure their functionality over wide temperature range between 25ºC and 400ºC. Future work includes circuit design optimization to reduce the power consumption.

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