This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

Electronics and Packaging Intended for Emerging Harsh Environment Applications: A Review

Ahmad Hassan, *Student Member, IEEE*, Yvon Savaria, *Fellow, IEEE*, and Mohamad Sawan, *Fellow, IEEE*

***Abstract*— Several industrial applications require specific electronic systems installed in harsh environments to perform measurements, monitoring, and control tasks such as in space exploration, aerospace missions, automotive industries, down-hole oil and gas industry, and geothermal power plants. The extreme environment could be surrounding high-, low-, and wide-range temperature, intense radiation, or even a combination of above conditions. We review, in this paper, the main leading applications that demand advanced technologies to fit the unconventional requirements of extreme operating conditions, discussing their main merits and limits compared to established and emerging technologies in this field, including silicon (Si), silicon on insulator (SOI), silicon germanium (SiGe), silicon carbide (SiC) as well as III–V semiconductors particularly the gallium nitride (GaN) semiconductor. In spite of successfully exceeding extreme conditions borders by developing advanced semiconductor devices dedicated for harsh environments, especially in high-temperature applications, the packaging challenges are still limiting the reliability of the developed technologies. Those challenges are examined in this review in terms of limitations and proposed solutions.**

***Index Terms*— Extreme environment semiconductors and extreme environment packaging, harsh environment applications, high-temperature electronics.**

I. Introduction

IT IS obvious that the conventional electronics technologies are not appropriate choices to meet the full requirements of harsh environment applications. For instance, when a satellite is launched in space, it is exposed to an intensive flow of ionizing radiation from the well-known radiation belts "aurora borealis" and to the high-energy electrons and protons produced by the sun wind and also to the earth's magnetic field effect [1]. Such complicated conditions can affect conventional electronic systems and damage commercial electrical and electronic devices built into the satellite [2].

To mitigate the effects of such harsh environments, the systems must be hardened to endure the expected impacts. This can be done by changing the system architecture, by adapting the design flow or the fabrication flow. Commercial off-the-shelf (COTS) components are generally preferred to reduce design, certification, and fabrication costs. Indeed, a heavy price tag is associated with hardening by process and hardening by design. As systems built only with COTS components may not have a sufficient reliability if exposed directly to a harsh environment, their sensitive components can be protected in an enclosure that allows the system to withstand the harsh conditions. For instance, an enclosure can provide thermal isolation, heating, cooling, or protection against radiation or corrosive gas or fluids. An enclosure can protect the core of a system, but some components may have to support the harsh environment as in the case of a rover designed for an extraterrestrial mission that has many actuators and sensors.

Clearly, there are applications where parts of a system must be designed to withstand a harsh environment, with key electronic components having to sustain missions in extreme conditions. For instance, in the case of a rocket launch, the mission time can be measured in hundreds of seconds, but the electronic must work as intended. Developing electronics for some extreme environment implies that its essential functionality must be maintained with a sufficient reliability, while reducing its complexity, and ensuring safety or increasing the efficiency of the complete system in addition to save wiring and complex connection costs, particularly in sensitive applications such as aerospace [3], [4] and down-hole oil and gas industry, where the volume to put the electronic can be severely limited and the safety requirements are very stringent.

In addition to electronic components, passive components and packaging technologies can have significant impact on the device functionality and system reliability. Therefore, it becomes a must to discuss packaging limits and all alternative solutions to overcome some harsh environment application requirements.

Few review articles have discussed extreme environment electronics and their applications [4]–[7] and some of them are dating. In [5], the most known high-temperature applications have been intensively discussed along with the implemented electronics in such applications. But this paper does not cover significant technologies useful for implementing extreme environment electronics such as silicon-germanium and gallium-nitride. Likewise, recent reviews [4], [6], [7] neither cover all types of significant semiconductors nor discuss all harsh environments other than the high-temperature applications in addition to providing very limited information on high-temperature packaging.

This paper first reviews various types of harsh environments and related applications in Section II. The state of the art on extreme environment electronics is presented in Section III,

Manuscript received June 24, 2017; revised December 18, 2017 and March 8, 2018; accepted April 17, 2018. This work was supported in part by the Natural Sciences and Engineering Research Council of Canada, in part by SAFRAN, and in part by Airbus Defence and Space. *(Corresponding author: Ahmad Hassan.)*

The authors are with the Electrical Engineering Department, Polytechnique Montréal, Montreal, QC H3T 1J4, Canada (e-mail: ahmad.hassan@polymtl.ca).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TVLSI.2018.2834499

1063-8210 © 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

including advances and limitations of necessary passive components and packaging utilized to build complete electronic systems. Finally, conclusions are summarized in Section IV.

II. Extreme Environments

Some of harsh conditions environments are more challenging than others. Among the different types of extreme conditions, the following are the most influential on the design and implementation of electronic devices and systems.

A. Low-Temperature Environment

The commercial temperature range specification of CMOS integrated circuits is from 0 °C to +85 °C, whereas the military specification temperature range is from −55 °C to +125 °C. In general, any temperature outside these ranges is considered an extreme temperature environment. Temperatures below those ranges are often called "cryogenic" due to the common use of cryogen liquids to reach them.

Diverse applications mandate cryogenic environments operation such as superconductivity. Furthermore, many planetary bodies impose cryogenic environments, like the poles of Mars where the temperature drops below −143 °C in winter. Moreover, deep space applications, such as electronic detectors of the James Webb Space Telescope, operate at −246 °C.

Furthermore, in order to improve system sensitivity, diverse types of electronic instrumentations demand cryogenic temperatures as their operational temperature. Indeed, noise in resistors and electronic devices decreases with temperature and the dark current of diode detectors reduce exponentially with temperature. Thus, cooled detectors are found in various applications, such as in medical imaging instruments, high-performance computers, satellite receivers, and astronomical instruments.

B. High-Temperature Environments

On the other side of the extreme low-temperature environments, extreme high temperatures surpass the standard commercial and military temperature range of +85 °C and +125 °C, respectively. Indeed, many industrial applications require stable electrical and electronic systems for robust operation at high temperature. Aerospace electronic systems, automotive and on-engine electronics, as well as power electronics are important examples where operating temperature ranges could extend up to 500 °C and even more if the electronic could withstand them.

Energy exploration such as geothermal production wells and oil and gas well drilling are major applications of high-temperature electronics, where electronic systems must operate at temperatures ranging between 250 °C and 300 °C [4]. In addition, some space exploration projects mandate extremely high operating temperatures, which may exceed 600 °C, such as the missions targeting the surface of Venus.

C. Wide Temperature Range Environments

A classic example of an environment imposing wide ranges of operating temperatures is the Moon, where its surface temperature in straight sunlight surpasses +120 °C, while dropping below −230 °C during the night, especially inside shadowed craters. The upper and lower limits of the temperature range in such applications may not by themselves be the worst factors to consider, but by the wide range covered and the temperature cycles in which the system must operate normally may be more harmful.

The rate at which thermal cycles occur may also be a significant issue and thermal shock can be far more challenging with respect to long-term reliability when compared to high or low fixed operating temperatures.

D. Radiation-Rich Environment

The three main categories of radiation effects are: 1) displacement effects where high-energy particles displace atoms or nuclei; 2) ionization effects where the materials are ionized when they are traversed by high-energy charged particles; and 3) total dose that typically charges dielectric causing cumulative parametric shifts that render a device nonfunctional. Radiation-rich environments are mainly present in space applications, nuclear power plants, and biomedical instruments.

E. Multiextreme Environments

When more than one type of extreme environments is present in one application, this situation will be called as multi-extreme environments. It is actually the most prevalent case as several harsh environments combine diverse types of extreme conditions, such as extreme low temperature with extreme high pressure or vibration, or extreme high temperature combined with radiation-rich environments.

Back to the moon surface example, where low-temperature conditions (−230 °C) combine with high temperature (+120 °C) and radiation effects due to solar winds and galactic cosmic rays, all these extreme environments must be addressed at once.

These diverse harsh environments and the corresponding applications stress the necessity of developing microelectronic devices that can meet application requirements in the expected environmental conditions. The following parts will investigate the most known semiconductors dedicated to harsh environments along with the corresponding limitations and improvements done so far.

III. Harsh Environment Electronics

Billions of dollars are invested in the extreme environment electronic industries to spread outside the conventional commercial and military electronics specifications. In 2005, the high-temperature electronics market was estimated to be around $17 billion [8]. As a definition, extreme environment electronics are small volume systems with significant value-added propositions that are extremely important for harsh environment applications, but very costly to set and operate.

The following parts discuss the main existing electronic devices, along with their functionality at extreme environment conditions.

A. Silicon

Silicon-based microelectronic technologies are the most common devices nowadays. Even though they are highly

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

reliable in the majority of commercial applications, they are limited when the ambient conditions extend outside its normal temperature range from −55 °C to +125 °C. Outside this interval, temperature can have a brutal impact on the transistor behavior. Once the surrounding temperature rises to extreme high ranges, the energy bandgap of Si will drop down while the carrier density, which affects the thermal and electrical conductivity, exponentially increases, turning from stable extrinsic region into the intrinsic region. Another sensitive parameter affected by temperature variation is mobility, which determines the drift speed of a particle subject to an applied electric field. Moreover, the current density, carrier diffusion, velocity saturation, electromigration, leakage current, threshold voltage, and interconnect resistance are all significant mechanisms or parameters directly affected by extreme temperatures.

Another set of considerations with Si-based platforms is their sensitivity to radiation. Even though threshold voltage shift with total dose is a dielectric volumic effect that had reduced significantly with scaling, the subthreshold leakage current is still seriously affected with deep submicrometer technologies. More precisely, gamma rays, cosmic ray's ions, X-rays, neutrons, as well as high-energy electrons, and protons have significant effects on electronic circuits operation that can have major impacts on operating characteristics and may induce failures.

The main basic concepts used to express and model the interaction between Si devices and radiation are the total ionizing dose (TID), displacement damage (DD), and single event effects (SEEs). TID is the damage produced by ionizing radiation over a time interval. Electron–ion pairs are generated by this ionizing radiation inducing trapped charges which, in turn, produce transient and long-term effects, in addition to changing threshold voltage and current leakage path. The DD, which is resulted by heavy ions, alpha particles, protons, neutrons, and very high-energy photons, can modify the configuration of the atoms in the semiconductor. It may provoke a permanent damage augmenting the recombination centers number and lowering the minority carriers. SEE is caused by high-energy particle passes through a semiconductor keeping an ionized path behind. When this charge moves, it might be collected to another charge resulting in serious effects starting by a bit-flip and ending by tragic burnout.

B. Silicon on Insulator

Silicon-on-insulator (SOI) technology is an advanced alternative option of the silicon CMOS technology to mitigate the drain induced barrier lowering and restrain charge sharing and fringing field effects especially for the short-channel CMOS platforms and more precisely in 45- and 65-nm technologies.

SOI is mainly dedicated for aerospace and military applications exploiting its rigidity against the extreme temperature and radiation environments. Nowadays, it is more accepted as a commercially available technology.

SOI CMOS family is the most mature approach using traditional silicon process but includes an isolation process to ultimately reduce the leakage current at high temperature. Comparing to the conventional p-n junction isolation

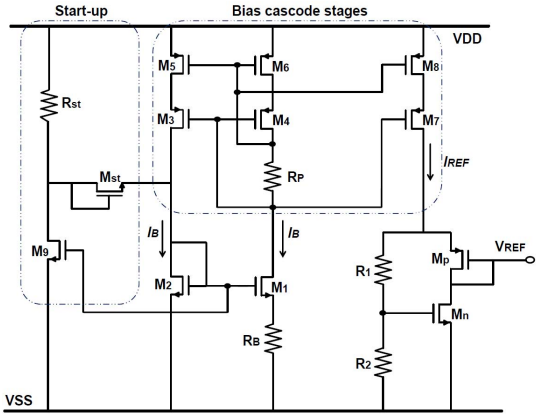


Fig. 1. CMOS SOI-based voltage reference circuit [11].

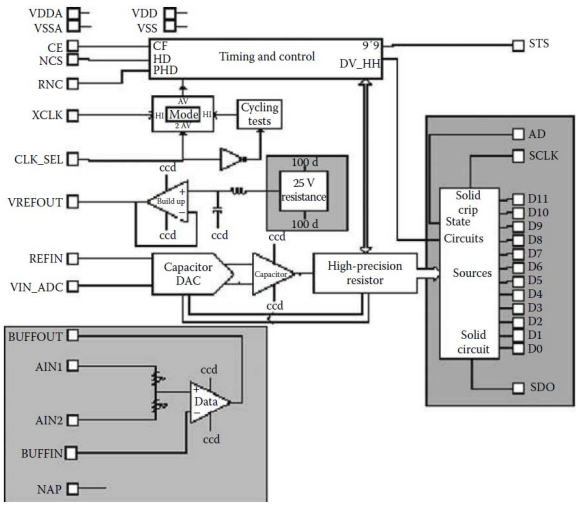


Fig. 2. SOI-based 12-bit analog-to-digital converter [12].

in Si CMOS technology, a silicon dioxide layer surrounds each SOI transistor giving an excellent electrical isolation characteristic even at high-temperature conditions [9].

Consequently, SOI CMOS device was successfully implemented to serve a universal gate driver circuit at temperature higher than 200 °C [10] and utilized in voltage reference circuit (shown in Fig. 1) for a range of temperature between −40 °C and 200 °C under total radiation dose of 1 Mrad [11]. In addition, Honeywell investments in high-temperature SOI electronics introduced several products and processes such as opamps, voltage references, voltage regulators, analog multiplexors, A-to-D converters (shown in Fig. 2), digital gate arrays, static random-access memory, 8-bit microprocessor, and clock interfaces [12] with endurable temperature exceeding 200 °C.

Another advantage of SOI appears in the omission of parasitic area junction capacitance and the decrease of crosstalk between digital and RF circuitry, in addition to the adequacy to integrate passive elements on-chip with high accuracy profiting from the large substrate resistivity. Other merits for the SOI are the reduction of a reverse body effect in stacked circuits and the junction of the floating body with source and drain is usually forward-biased.

The SOI flexibility with the radiation is returned to its geometric constrains limiting the volumes of active silicon

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

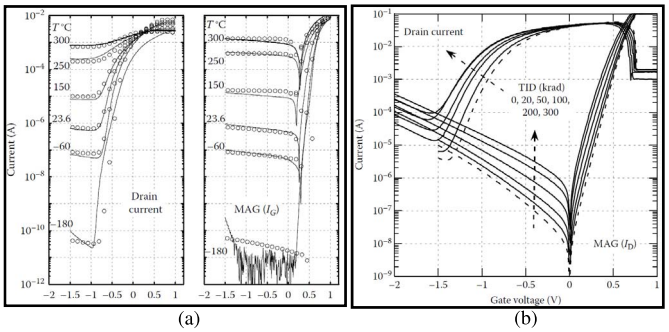


Fig. 3. MESFET SOI CMOS technology as a function of gate voltage (V) for a fixed drain bias of 2 V. (a) Drain current (left) and gate current magnitude (right) of 600-nm gate length. (b) Radiation response of 300-nm gate length MESFET after successive radiation exposure up to a TID of 300 krad(Si) where the MESFET was positioned at a distance from the ^{60}Co source that gave a dose rate of 0.9 krad(Si)/min [13].

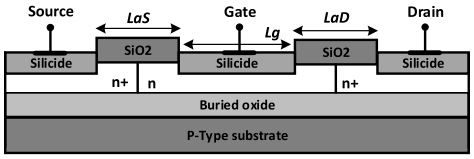


Fig. 4. Schematic cross section of the SOI MESFET [14].

TABLE I

PROTECTION TYPE OF PRESENTED SOI AND SIGE DEVICES

Device	Reference	Protection
SOI	[10]	Ceramic package + Polyimide test board
	[12]	Ceramic package + Al-wire bonding + Au-plate + Ni-bond pad
	[11] [13-14]	N/A
SiGe	[15] [18] [21]	Multi-chip Module Packaging: Al_2O_3 pacakge and lid, AlN substrate, Cu metallization, Au wire bond, In/Pb lid seal, polyimide and Cryogenic ribbon cable
	[19-20] [24-25]	N/A
	[22]	Ceramic flat package
	[23]	PC board sandwiched in between two gold plated brass carriers with the IC mounted in a VIA hole to minimize bond wire lengths
	[26]	Simulation
	[27]	Custom-designed, on-wafer, open-cycle liquid nitrogen (LN2) probe station

N/A*: Not mentioned in the related reference

regions with the radiation energy ionization and deposition, and the limited communication of deposited charge between the devices.

SOI metal–semiconductor field-effect transistors (MESFETs) are a different approach for the SOI technology which is also developed to support the extreme environment applications covering a wide range of temperature between −180 °C and +300 °C and enduring intense radiation dose as shown in Fig. 3(a) and (b), respectively [13]. The MESFET implementation, as shown in Fig. 4, requires a Schottky barrier which is composed of the silicide step providing the low resistance source–drain contacts. The gate silicide is isolated from the source–drain silicides by space regions of length $L_{a\mathrm{S}}$ and $L_{a\mathrm{D}}$ [14]. The silicide–silicon interface has the advantage of being extremely stable up to relatively high temperatures. Table I shows the utilized protection in each presented SOI devices [10]–[14].

The insulating regions of SOI are mainly achieved by SiO_2 deposits. Regretfully, this isolation layer has a thickness more than that of the gate itself and suffers a charge trap higher than the highly optimized gate stacks resulting in radiation responses by these isolation regions. To clarify this, the buried insulating oxide and associated TID for a thin SOI device can be represented as a secondary gate. This secondary gate modulates a pseudochannel at the bottom of the transistor producing backside leakage current or attaches to the top surface channel by electrostatic force modifying the transistor threshold voltage. Moreover, even for the modern SOI technology such as vertically stacked structures and multigate which are intended for harsh environments, the parasitic effects have significant impacts.

C. Silicon Germanium

SiGe is a BiCMOS technology implemented by adding heterojunction bipolar transistor (HBT) to Si CMOS platform. This implementation advocates the functionality of highly integrated system performing a mixed-signal technology which is qualified by its high-performance feature for RF, analog, and microwave circuits. The most preferable SiGe approach for extreme environment applications is the complementary SiGe BiCMOS on a thick-film SOI substrate to perform noise isolation which presents a critical topic in various analog and mixed-signal systems.

With decreasing temperature, the Si bipolar junction transistor (BJT) device suffers from degradation in the turn-ON voltage junction, base resistance, current gain, frequency response, cutoff frequency, and delay in digital circuits. Unlike the Si BJTs, the cooling impact (low-temperature environment) on SiGe HBT device is favorably improving its dc and ac properties [15]. A simple check of the SiGe HBT device equations shows the improvement in the transconductance, current gain, cutoff frequency, maximum frequency, and broadband noise [16], [17].

In fact, despite the performance degradation of Si BJTs in cryogenic conditions, the addition of SiGe dramatically changes the situation. The bipolar transistor properties will be strongly coupled to the band-edge effects induced by bandgap engineering. Physically, the minority carrier of bipolar transistor is the reason of this strong coupling which implies in terminal currents proportional to the intrinsic carrier concentration (n_{i0}^2) through the Shockley boundary conditions, and in turn, n_{i0}^2 is proportional to the exponential of the bandgap. Therefore, the currents will be coupled exponentially with any changes to the bandgap [15].

Moreover, from general mechanical considerations, these bandgap changes will be automatically divided by the thermal energy (kT), which means that a reduction in applied temperature will considerably increase any bandgap changes.

Consequently, SiGe HBT device equations inspire that both ac and dc properties are favorably influenced by cooling.

Comparing the equations of a SiGe HBT to a comparably constructed Si BJT, the thermal energy (kT) is arranged to favorably affect the low-temperature properties. For example, the following equations show with decreasing temperature a quasi-exponential increase in the current gain [$\beta(T)$] of

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

SiGe-to-Si ratio

$$\left.\frac{\beta_{\mathrm{SiGe}}}{\beta_{\mathrm{Si}}}\right|_{V_{\mathrm{BE}}} \simeq \left\{\frac{\tilde{\gamma}\,\tilde{\eta}\,\Delta E_{g,\mathrm{Ge}}(\mathrm{grade})/kT\,\mathrm{e}^{\Delta E_{g,\mathrm{Ge}}(0)/kT}}{1-\mathrm{e}^{-\Delta E_{g,\mathrm{Ge}}(\mathrm{grade})/kT}}\right\} \quad (1)$$

and an exponential increase in the ratio of the early voltage (V_A) and the current gain-early voltage (βV_A)

$$\left.\frac{V_{A,\mathrm{SiGe}}}{V_{A,\mathrm{Si}}}\right|_{V_{\mathrm{BE}}} \simeq \mathrm{e}^{\Delta E_{g,\mathrm{Ge}}(\mathrm{grade})/kT}\left[\frac{1-\mathrm{e}^{\Delta E_{g,\mathrm{Ge}}(\mathrm{grade})/kT}}{\Delta E_{g,\mathrm{Ge}}(\mathrm{grade})/kT}\right] \quad (2)$$

$$\frac{\beta V_{A,\mathrm{SiGe}}}{\beta V_{A,\mathrm{Si}}} = \tilde{\gamma}\,\tilde{\eta}\mathrm{e}^{\Delta E_{g,\mathrm{Ge}}(0)/kT}\,\mathrm{e}^{\Delta E_{g,\mathrm{Ge}}(\mathrm{grade})/kT}. \quad (3)$$

In addition, the temperature dependence of the base and emitter transit times

$$\frac{\tau_{b,\mathrm{SiGe}}}{\tau_{b,\mathrm{Si}}} = \frac{2}{\tilde{\eta}}\frac{kT}{\Delta E_{g,\mathrm{Ge}}(\mathrm{grade})} \times\left\{1-\frac{kT}{\Delta E_{g,\mathrm{Ge}}(\mathrm{grade})}[1-\mathrm{e}^{-\Delta E_{g,\mathrm{Ge}}(\mathrm{grade})/kT}]\right\} \quad (4)$$

$$\frac{\tau_{e,\mathrm{SiGe}}}{\tau_{e,\mathrm{Si}}} \simeq \frac{J_{C,\mathrm{Si}}}{J_{C,\mathrm{SiGe}}} = \frac{1-\mathrm{e}^{-\Delta E_{g,\mathrm{Ge}}(\mathrm{grade})/kT}}{\tilde{\gamma}\,\tilde{\eta}\frac{\Delta E_{g,\mathrm{Ge}}(\mathrm{grade})}{kT}\mathrm{e}^{\Delta E_{g,\mathrm{Ge}}(0)/kT}} \quad (5)$$

explains the temperature dependence of frequency response of a SiGe HBT. Thus, it is noticed that cooling temperature positively affects both transit times leading to improvement in both maximum oscillation frequency ($f_{\max}$) and cutoff frequency (f_T)

$$f_{\max} = \sqrt{\frac{f_T}{8\pi C_{bc} r_b}} \quad (6)$$

$$f_T = \frac{1}{2\pi\,\tau_{ec}} = \frac{1}{2\pi}\left[\frac{kT}{q\,I_c}(c_{te}+c_{tc}) + \tau_b + \tau_e\frac{W_{CB}}{2v_{\mathrm{sat}}} + r_c C_{tc}\right]^{-1} \quad (7)$$

All those improvements in the performance properties of SiGe HBTs with cooling have been confirmed experimentally. An extensive discussion with detailed analysis concerning the presented equations can be found in [18].

On the opposite side of cryogenic conditions, the high-operating temperature has a degradation effect on both dc and ac performance of SiGe HBTs. However, the degree of this degradation is a matter to be discussed and investigated. Accordingly, SiGe HBTs commercially available with current gain above 100 and cutoff frequency of 75 GHz normally operate at 300 °C [19]. In addition to the robustness of SiGe HBT device at extreme low and high temperatures, the durability of this device in radiation environment has been investigated as well [20] showing a favorable built-in TID great tolerance as presented in Figs. 5(c) and 5(d).

SiGe HBT, illustrated in Fig. 5(a) with its unique bandgap properties, presents a significant process for the extreme environment applications. The latter can be classified as following: extreme high-temperature conditions exceeding 300 °C as characterized in Fig. 5(b), extreme low-temperature environments lower than −200 °C (Fig. 6) [15], wide and cyclic temperature intervals such as the lunar surface temperature between −230 °C and +120 °C, and finally the intense radiation environments.

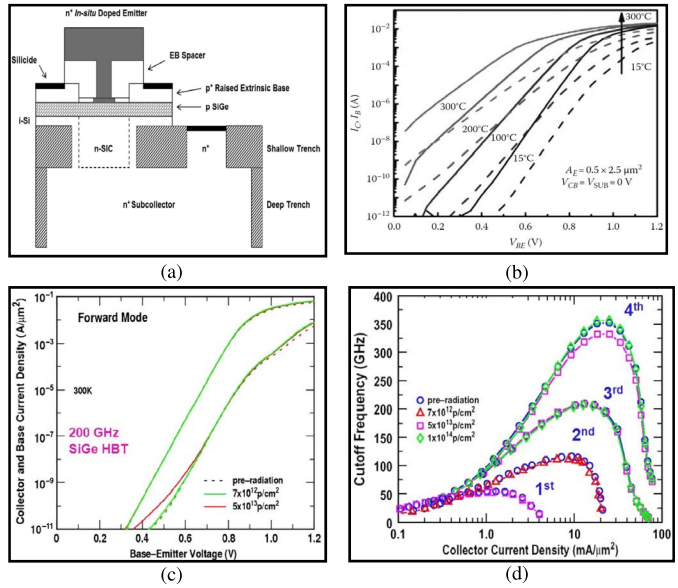


Fig. 5. SiGe HBT. (a) Cross-sectional view (third generation). (b) Current–voltage characteristics (first generation). (c) Current–voltage characteristics (third generation) exposed to space-relevant 63-MeV protons to multi-Mrad total dose. (d) Cutoff frequency for four generations before and after exposure to space-relevant 63-MeV protons to multi-Mrad total dose [15].

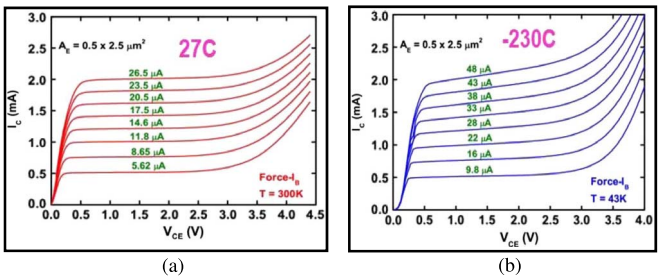


Fig. 6. Output characteristics of a SiGe HBT (first generation) operating at (a) $T = 27$ °C and (b) $T = -230$ °C [15].

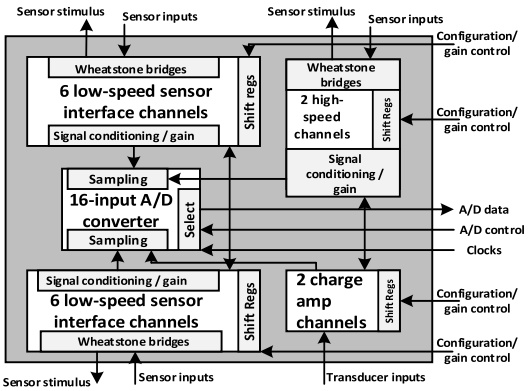


Fig. 7. SiGe BiCMOS (SiGe HBT + CMOS) based simplified block diagrams of the remote sensor interface [21].

As an example, the work in [21] was supported from NASA Exploration Technology Development Program to develop a remote electronics unit system based on SiGe HBT. The implemented remote sensor interface is depicted in Fig. 7. The implemented system was tested under cryogenic temperature less than −173 °C, 100-krad TID radiation exposures and at high temperature of 125 °C. Therefore, SiGe HBT is capable to satisfy the electronic requirements of all the preceding extreme environment

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

TABLE II
COMPARISON OF SELECTED SEMICONDUCTOR MATERIAL PROPERTIES [28]

Property	Silicon	GaN	4H-SiC	6H-SiC	3C-SiC
Bandgap energy (ev)	1.1	3.4	3.2	3.0	2.3
Relative dielectric constant	11.9	9.5	9.7	9.7	9.7
Breakdown electric Field at $N_D = 10^{17}$ cm^{-3} (MV/cm)	0.6	2-3	3.0	3.2	1.8
Intrinsic carrier Concentration (cm^{-3})	10^{10}	~10^{-10}	~10^{-7}	~10^{-5}	~10
Electron mobility at $N_D = 10^{16}$ cm^{-3} (cm^2/V.s)	1200	900	800	60- 400	750
Hole mobility at $N_D = 10^{16}$ cm^{-3} (cm^2/V.s)	420	200	115	90	40
Saturated electron velocity (10^7 cm/s)	1.0	2.5	2	2	2.5
Thermal conductivity (W/m.K)	150	130	400	480	500

conditions by slight process modifications providing considerable benefits regarding the weight, size, and power constraints.

Moreover, in [22] and [23] SiGe devices have been utilized to implement voltage reference and LNA circuits, respectively, for cryogenic applications. Similarly, a wide-range temperature test (from −180 °C to 120 °C) has been successfully applied to analog-to-digital converter [24] and digital-to-analog converter [25], respectively.

Diverse generations of SiGe are nowadays widely spread in the commercial communities with tens of fabrication companies. The frequency capability of available SiGe HBT is between 50 and 200 GHz. Recently, 90-nm SiGe BiCMOS technology was presented in a comparator circuit for wide temperature range application between −195 °C and −155 °C [26], and a fourth generation of this device is implemented in [27] for RF applications at cryogenic temperature exceeding −195 °C. Table I shows the utilized protection type in each presented SiGe device [15], [18]–[27].

D. Silicon Carbide

For the moderate intensity of extreme environment applications, the standard Si platforms, SOI and silicon germanium (SiGe) present suitable choice to be applied and cover the electrical and electronic requirements. However, when the surrounding conditions attain extremely harsh condition environment, the preceding semiconductors are no longer useful, and an alternative advanced semiconductor generation should be developed such as the silicon carbide (SiC) to fit the excessive environment requirements.

SiC is composed of numerous types of crystal structures, named polytypes. However, there are just three types commonly accepted as an electronic semiconductor, which are 4H-SiC, 6H-SiC, and 3C-SiC. Table II presents the most important electrical properties of these types compared with GaN and silicon [28]. The wide bandgap energy along with the high breakdown electric field is the two essential advantages of SiC over silicon semiconductor. Holding a very low intrinsic carrier concentration and a wide bandgap (same as the GaN device mentioned in Table I) nominates the SiC to join the team of extreme high-temperature semiconductors, giving the capability to operate theoretically at high temperatures up to 800 °C. It is experimentally proved that SiC devices

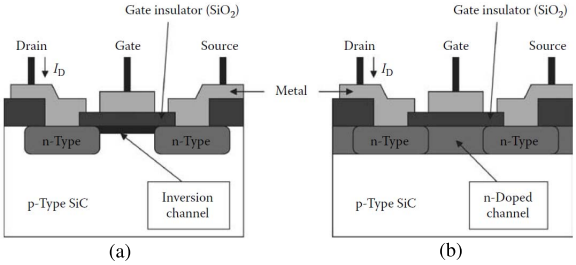


Fig. 8. Cross-sectional view of the two basic SiC MOSFETs. (a) Inversion-channel. (b) Doped-channel [28].

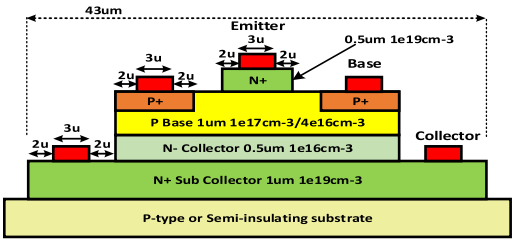


Fig. 9. Cross-sectional schematic of 4H-SiC BJT device topology [30].

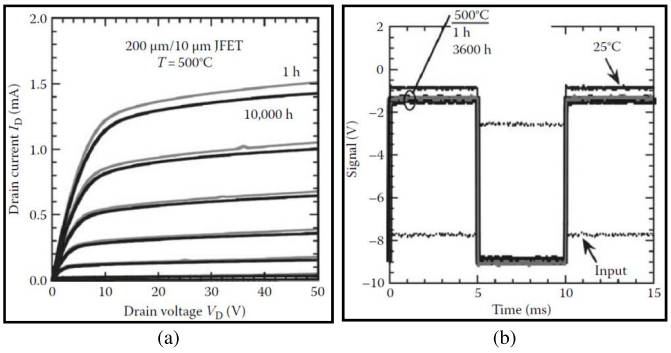


Fig. 10. 6H-SiC JFET. (a) Current–voltage characteristics. (b) NOT gate IC test waveforms [31].

can successfully operate for a limited time (few hours) at 600 °C [29].

Furthermore, SiC possesses a high-power density and efficiency due to its high-thermal conductivity along with the high-breakdown electric field and high-junction temperature. By these properties, SiC power converters have higher switching frequency implying to smaller transformers, inductors and capacitors reducing size, cost and weight of the power converters, and diminish the heat generation and energy loss. Various approaches of SiC have been developed to achieve a high performance and stable operation against the extreme conditions existed in harsh environments.

The main developed SiC approaches are SiC metal–oxide–semiconductor field-effect transistor (MOSFET) (Fig. 8) [28], MESFET, junction filed effect transistor (JFET), and BJT semiconductors (Fig. 9) [30]. The latter is mainly developed for high-temperature applications more than 300 °C.

As shown in Fig. 10(a), a packaged 6H-SiC JFET is tested for 10 000 h at 500 °C operational temperature measured at start (gray curve) and end (black curve) in air atmosphere. In Fig. 10(b), an experimental measurement of 6H-SiC JFET NOT gate IC test waveforms shows that the similar output is obtained at 25 °C and at the start (1 h) and end (3600 h) of prolonged 500 °C operational testing in air atmosphere [31].

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

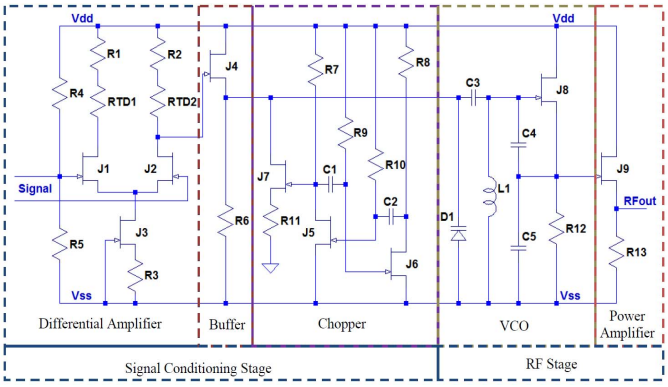


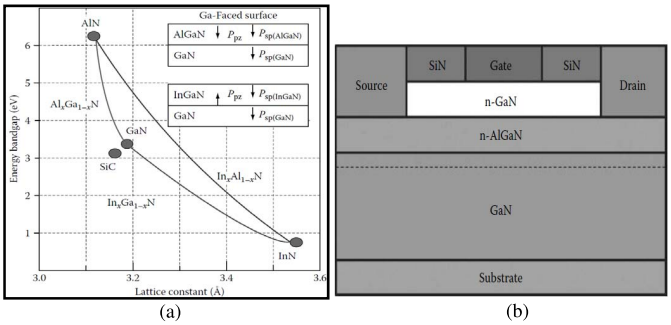
Fig. 11. SiC JFET-based circuit schematic of wireless sensing module for pressure and temperature measurement [36].

Generally, because of its low power consumption circuit, SiC-based CMOS may eventually become the principle type of SiC technology dedicated for harsh environments if the gate insulator durability and reliability issues can be overcome.

Until SiC designers sufficiently cope with the gate insulator challenges, SiC BJT-, MESFET-, and JFET-based IC technologies present a direct approach to fit the extreme environments demands. As an example, the NASA Glenn Research Center has successfully approved the durability and prolonged stability of SiC JFET development at 500 °C ambient temperature for continuous thousands of hours with experimental measurements on amplifier stages and logic gates [32].

Moreover, several studies and implementations have been done recently for SiC semiconductors such as in [33], where 17 samples of integrated circuits were successfully tested at 300 °C. The simulation results in [34] of 4H-SiC bipolar logic families are promising for operational temperature of 500 °C. In [35], a SiC CMOS comparator and op-amp are implemented and tested at 550 °C. Similarly, 4H-SiC JFET is characterized at 600 °C [29] and a wireless RF transmitter, as shown in Fig. 11, based on SiC technology was developed in [36] to serve pressure and temperature sensor systems at high-temperature applications exceeding 450 °C. Several logic gates have been implemented and tested in [37] at 250 °C based on MESFET SiC and a linear voltage regulator circuit based on SiC MOSFET device has been tested at 300 °C [38]. For intense-radiation applications, the impact of electron and proton irradiations on 4H-SiC MOSFET was investigated in [39], where the SiC device shows remarkable improvements in terms of electrical parameters after 15-MeV electron and 5-MeV proton irradiations.

On the other hand, and to date, there is no existence of a commercial SiC semiconductor transistor or IC that can be utilized in an ambient temperature more than 300 °C. Although over the last decade the improvement of SiC prototypes achieve an advanced stage, it remains a difficult challenge to reach long-term operational reliability for extreme temperature circuits and devices, especially regarding the reliability of contacts, passivation [40], interconnect, and packaging. Therefore, seemingly, the SiC technology will be solely dedicated for space applications where it is not possible for existing technologies to take place due to the extremely harsh environment condition. On the other hand, in the case of lower extreme environments (means less than space application), it is more effective to use the other existing technologies which are less expensive and more mature than SiC device especially in the low-power signal processing and digital logic circuit functions.



(a) (b)

Fig. 12. (a) Bandgap energy versus lattice constant [41]. (b) Cross-sectional structure of a GaN HEMT [42].

E. Gallium Nitride

To overcome several limitations in conventional low-bandgap semiconductors, new generations of semiconductors have been innovated combining column-III elements with nitrogen providing III-nitride materials such as indium nitride (InN), aluminum nitride (AlN), and gallium nitride (GaN), in addition to their alloys such as InAlN, InGaN, AlGaN, and AlInGaN. Fig. 12(a) shows that III-N semiconductors have wide ranges of bandgap energy ranged between 0.7 (with InN) and 6.2 eV (with AlN) [41]. However, the majority of III-nitride pursuing studies have been focused on GaN and its relatives such as AlGaN and InGaN.

Considering the high-voltage operation capabilities and low-resistive loss, GaN platform is nominated to be an appropriate candidate for power amplification and switching applications with wide operational temperature range. Moreover, GaN materials are obtainable with high quantity which makes this technology on the top of the investigation research list and puts it in the hot spot of promising engineering fields development. Taking into consideration the fabulous polarization field characterization of GaN material, modern valuable designs are easily obtainable.

In spite of the GaN technology has ensured its validity in the harsh environments especially the high-temperature applications, there are still many hurdles put off this technology to become on the successful commercialization map. Thermal management, manufacturing cost, wafer level uniformity, and reliability improvement are a bunch of these road blocks. Nevertheless, GaN high-electron-mobility transistors (HEMTs) have demonstrated their feasibility in microwave power amplifiers and many commercial products of wireless communication systems.

More deeply, when 2-D electron gas (2-DEG) is composed in a quantum well into the semiconductor structure, the attractive carrier transport mechanisms are reached. This cannot be happened unless in lateral devices like the power device GaN HEMT illustrated in Fig. 12(b) [42]. This characteristic is demonstrated in GaN devices, unlike the silicon and SiC power devices with vertical characteristics.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

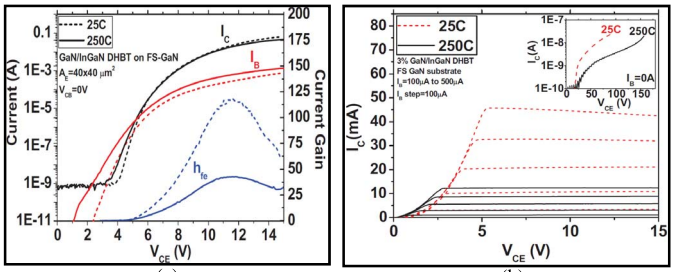


Fig. 13. DHBT grown on a GaN substrate. (a) Gummel plot. (b) Common-emitter characteristic [45].

Furthermore, it becomes rare to hear a discussion about power devices and extreme environments without the presence of GaN wide bandgap technology. In addition, the major trends of nowadays semiconductor studies are focusing on this GaN mature technology to go beyond the conventional silicon limits and perform a novel platform with higher operable blocking voltage, wider range of operational temperature and better energy conversion efficiency [43], [44]. Therefore, it is anticipated that GaN technology will attract more interests and open wide opportunities to develop the next generation of microelectronic systems.

Because of the difficulty to provide high quality GaN substrates, different types of starting substrates have been employed to build the GaN devices. For instance, it is common to find GaN platforms are established on a substrate made of silicon (GaN on Si) or made of silicon carbide (GaN on SiC), or even sapphire substrates.

In order to assess the behavior of GaN with high-temperature conditions, a large area device of 40 × 40 μm^2 of double heterostructure bipolar transistor (DHBT) has been studied in [45] at room temperature and high ambient temperature. Fig. 13(a) shows the current gain reduced from 115 to 43 when the temperature increases from 25 °C to 250 °C due to the I_B increment. This current gain reduction is referred to the increased recombination rate of trap state [46], [47] and the reduction of emitter injection efficiency. This reduction of emitter injection efficiency is due to the enhanced Mg ionization efficiency which in terms introduces to higher concentration of free hole in the base [45].

The common-emitter I_C-V_{CE} curves are shown in Fig. 13(b), where a reduction is happened to the knee voltage from 5.2 to 2.75 V with temperature rising from 25 °C to 250 °C, respectively, when the $I_B = 500$ μA. In parallel, the offset voltage also drops from 0.8 to 0.3 V for the same increasing of temperature.

The knee voltage and the offset voltage reduction are due to decreasing of base resistance at high temperature. The inset of Fig. 13(b) exhibits the temperature-dependent BV_{CEO} (common-emitter collector breakdown voltage) which augments from 90 to 157 V when the temperature increases from 25 °C to 250 °C, respectively. The increasing in temperature coefficient is attributed to the prevalent impact of the ionization process for GaN/InGaN HBTs. In parallel, another research investigating the feasibility of AlGaN/GaN HBTs at high temperature reports a current gain of 3 for high temperature of 590 °C [48]. All these reported results emphasize the susceptibility of GaN microelectronic devices to operate properly under high-temperature conditions.

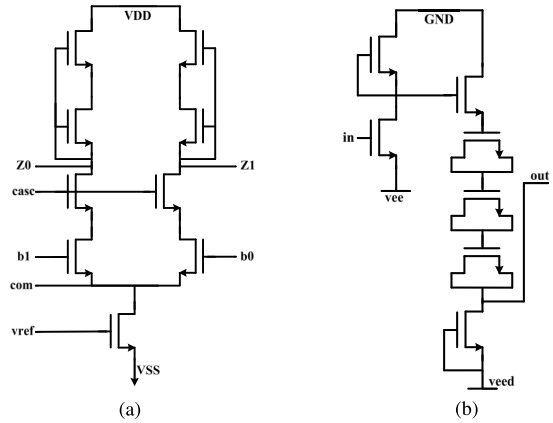


Fig. 14. Schematic of GaN HFET-based digital circuits. (a) Comparator. (b) Inverter block used in ring oscillator [55].

TABLE III
EXTREME ENVIRONMENT SEMICONDUCTORS COMPARISON

Extreme environments electronics				
Tech.	**High temp.**	**Low temp.**	**Intense Rad.**	**Availability**
Si	-	+	-	+
SOI	+	+	++	+
SiGe	+	++	++	+
SiC	++	+	++	-
GaN	++	++	++	-

The radiation effect on commercial GaN HEMT devices has been studied in [49] where no significant amount of degradation was reported. The effect of radiation-induced damage on AlGaN/GaN electric field has been simulated after applying proton irradiation [50]. On the other hand, InAlN/GaN HEMT shows promising characterization results at 1000 °C [51] and 600 °C with ultrathin body technology [52].

An integrated inverter based on enhanced mode MOSFET and depletion mode GaN devices has been characterized from temperature room to 300 °C [53] and a novel AlN/GaN integrated circuit is presented in [54] with operational temperature of 500 °C. In [55], a 31-stage ring oscillator, frequency dividers, several logic gates, and a comparator (shown in Fig. 14) have been implemented based on GaN/AlGaN HFET device and tested at 300 °C.

Table III provides a summary for the developed extreme environment electronics technologies so far, and Table IV lists the main foundries where the discussed harsh environment devices and implemented circuits were processed. As it is shown, standard silicon is only suitable for low-temperature applications. However, the SOI is better for intense radiation environment. SiGe is mostly appropriate for low temperature and intense radiation application. SiC and gallium nitride (GaN) are great candidates for all the extreme environments; however, they are still not commercially available.

F. Contacts

The conductive contacts functionality at high temperature is not less important than that of semiconductor itself. The reliability of contacts metallization and interconnects between

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

TABLE IV
FOUNDRIES OF HARSH ENVIRONMENT ELECTRONICS

Reference	Tech.	Foundry	Type
[9] [15]	SOI	Honeywell	CMOS 0.8um
[10]	SOI	N/A	0.8um BCD on SOI process
[11]	SOI	N/A	CMOS 0.13um
[13]	SOI	N/A	MESFET 0.6um
[14]	SOI	N/A	MESFET 0.15um
[17-20]	SiGe	IBM	SiGe HBT
[21]	SiGe	NASA	SiGe HBT and SiGe BiCMOS
[22]	SiGe	IBM	0.12um SiGe BiCMOS8HP
[23-24]	SiGe	NASA	0.5um SiGe BiCMOS
[25-26]	SiGe	IBM	90nm SiGe HBT BiCMOS
[28]	SiC	Cree Inc.	4H-SiC JFET
[30-31]	SiC	NASA	6H-SiC JFET
[29]	SiC	GE	4H-SiC BJT
[32]	SiC	Raytheon	4H-SiC CMOS
[34]	SiC	Raytheon	1.2um SiC CMOS
[35]	SiC	N/A	SiC JFET
[38]	SiC	N/A	4H-SiC MOSFET
[36]	SiC	Cree Inc.	SiC MESFET
[37]	SiC	Cree Inc.	4H-SiC MOSFET
[44]	GaN	N/A	GaN/InGaN DHBT
[47]	GaN	N/A	AlGaN/GaN HBT
[48]	GaN	Cree, Sumitomo and RFMD	GaN HEMT
[50]	GaN	III-V Lab	0.25um InAl/GaN HEMT
[51]	GaN	III-V Lab	0.25um InAlN/GaN HEMT
[52]	GaN	N/A	GaN MOSFET HEMT
[53]	GaN	N/A	AlInN/GaN HFET
[54]	GaN	HRL Lab	AlGaN/GaN HFET

*N/A: Mainly indoor fabrication or unknown

the on-chip devices presents a substantial challenge for devices dedicated to operating in high-temperature conditions particularly for applications beyond 400 °C. The generated self-heating during operation in addition to the surrounding high temperature provoke contact degradation and limit the long-term reliability of these devices.

One of the notable failure mechanism at high temperature is the electromigration process, where the current flowing into a conductor conducts to a bulk motion of the material and leads to open circuit. Depending on the current density and temperature, the time to failure for a conductor can be described by Black's equation

$$t_{\text{Fail}} = A j^{-n} e^{E_a/kT} \tag{8}$$

where t_{Fail} is the mean time to failure, A is the specific coefficient of a metal process, j is the current density, n is a coefficient typically between 2 and 3, and E_a is the thermal activation energy. As noticed from the equation, the life time of conductor is quickly decreasing with function of temperature and current density. The current density should be addressed by designers to limit it. On the other hand, for operating temperature more than 200 °C, the reliability issue of devices and corresponding conductors must be addressed.

Aluminum conductor is widely utilized in Si chips; however, it fails for temperature above 200 °C due to electromigration after few thousand operating hours and above 300 °C in hundreds of hours. In GaAs circuits, gold is commonly used with need of burrier metals and adhesion layers.

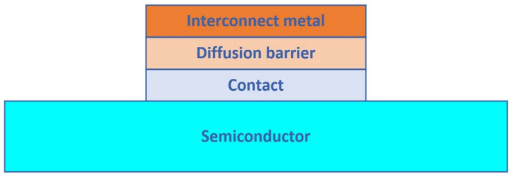


Fig. 15. Proposed structure for making contacts in high-temperature devices.

Comparing with Al, gold is more resistant to electromigration. However, it alloys with diffusion barrier and adhesion layer at high temperature causing a large increase in resistance and consequently affects the device and circuit performance. In parallel, tungsten is much more resistant to electromigration than Al and used as a conductor.

Another critical issue at high temperature is the failure possibility of interface between different materials due to diffusion, chemical reactions, and other metallurgical reactions. Consequently, there is a need to develop thermodynamically stable interfaces. In addition, mechanical stresses could be applied to the interfaces because of thermal expansion coefficient mismatches. Also, at extremely high-operating temperature (>600 °C), it would be necessary to take into consideration the degradation of p-n junctions and diffusion of dopants.

The interface stability issue has been solved by utilizing layers of materials. It is done by adding the ohmic and Schottky contacts to the semiconductor devices, followed by a diffusion layer to separate the contacts from the high electrical conductive interconnect layer as described in Fig. 15. The contact material, such as silicide, should ensure the completion with the semiconductor and maintain relatively high electrical conductivity. The diffusion layer must be inert to the interconnect metal and to the contact. The way of preparing this layered structure (contact–diffusion barrier–interconnect) is as important as the choice of the materials. The utilized processing techniques has a direct impact on the metallurgical properties, which in terms affect the diffusion rates and intermetallic formation due to chemical reactions between the layers. For devices operating at extremely high temperature, one of the main challenges is to develop such a stable structure of multilayer metallization systems.

Great efforts have been done toward developing ohmic contacts to SiC for high-temperature applications. In [56], TiW-based contacts with aluminum interconnect was successfully tested over 500 h at 400 °C. Similarly, Ti/$TaSi_2$/Pt multilayer contact to n-type SiC shows stable ohmic properties for 1000 h of annealing at 600 °C [57]. More studies are necessary to obtain similar results for p-type SiC.

Ti/Al/Ni/Au low resistance ohmic contact has been studied in [58] between 25 °C and 600 °C for n-type GaN. On the other hand, the Schottky contact of n-GaN Ni/Au, Ni/Pt/Au, Pt/Ni/Au, and Pt/Ti/Au has been investigated in [59] up to 400°C. In parallel, a novel Mo/Al/Mo metal stack is introduced in [54] to improve the robustness of ohmic contact at high temperature reaching 500 °C. A high-k dielectric is deposited to provide Schottky contact showing stable dielectric permittivity through wide temperature range in addition to the decreasing of the breakdown voltage and leakage current.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

TABLE V
CONTACTS AND METALLIZATION TYPES OF PRESENTED DEVICES

Device	Reference	Interconnect and contact
SOI	[10]	Oversized interconnect + multiple pad connections +N/A
	[11]	N/A
	[12]	TiN/Al
	[13] [14]	Silicon/silicide/metal
SiGe	[15] [18-24] [26-27]	N/A
	[25]	n-well and p-sub contacts
SiC	[28] [34-36] [38] [40	N/A
	[29]	Ti/Ni/TiW/Cr
	[30]	Ti/Al/Ti/Au
	[31-32]	$TaSi_2$/Pt
	[33]	P-WELL contacts
	[37]	Ni/Ti/W/Ti/Ti/Al (ohmic contact) + W/Ti/W/Ti/Ti/Al (gate contact)
	[39]	Ni (ohmic contact) + Al (gate contact)
GaN	[42-44] [46-47] [49-50] [53] [55]	N/A
	[41]	Ti/Al (ohmic contact) + Ni (gate contact) + Ti/Au (interconnect layer)
	[45]	Ti/Al/Ti/Au (emitter and collector contacts) + Ni/Au (base ohmic contact) + Ti/Au (interconnect layer)
	[48]	Pd/Au (p-type layer) + Al/Au (n-type layer)
	[51]	Ti/Al/Ni/Pt (ohmic contact) +Mo (gate metal)
	[52]	Ti/Al/Ni/Cu/Ti/Pt (ohmic contact) + Cu/Pt/Cu/Ti/Pt (gate metal)
	[54]	Ti/Mo/Al/Mo/Ni/Au (ohmic contact) + Ti/Ni/Au/Ni (interconnect)

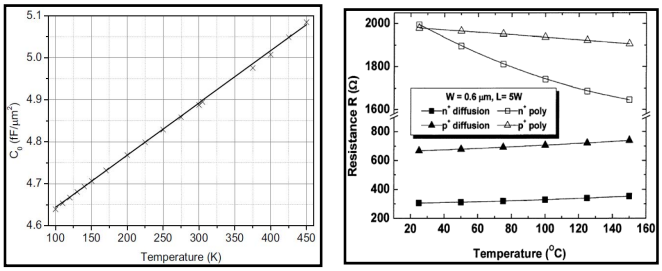
N/A*: Type not mentioned in the related reference

Due to the difficulties of realizing conductive p-type GaN layers, obtaining highly stable contacts of this material presents as serious challenge so far. In addition, more studies are still needed to investigate the reliability of GaNs ohmic contact in presence of electromigration and chemical reactions with applied electrical bias at oxidizing high temperature more than 400 °C. Thus, radical challenges in GaN contacts must be surmounted to enable this device to support long-term operation in real environment and at high temperature more than 600 °C.

Table V summarizes the utilized contacts and metallization systems of the presented harsh environment devices in Sections III-B–III-E (SOI, SiGe, SiC, and GaN).

G. Passive Components

The microelectronic devices dedicated for operating in extreme environment conditions have been developed to sustain such harsh conditions, such as SiGe technology for cryogenic conditions, SiC and GaN for high-temperature applications, and SOI for an intense radiation environment. These pioneering technologies support the transistor level of microelectronic systems to endure the harsh environments, while the integrated passive components are not well designed for such extreme conditions. Therefore, it is deeply needed to investigate the passive components responses with the variations of applied environment conditions.



(a) (b)

Fig. 16. (a) Modeled versus measured data for MIM capacitors [62]. (b) Resistance versus temperature range [63].

Military passive components operable temperature range is usually from −55 °C to +125 °C. The measurement of variation in component value is commonly reported by temperature coefficient in ppm/°C. The discrete passive components performance was characterized at extreme low temperature. It was noticed that commercial components suffered significant variations in value when the temperature falls below −50 °C. However, similar studies confirmed the capability to provide discrete passive components able to operate successfully at −200 °C [60].

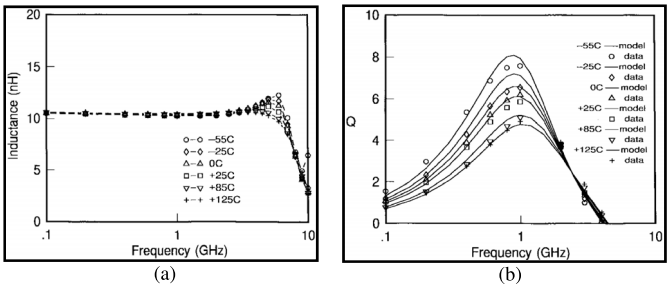
On the other hand, the on-chip passive components integrated on silicon platforms have low temperature operation limits as well, where the minimum temperature of Mil-Spec range is only −55 °C. However, different related studies [61] have successfully performed a wide range of operational temperature (from −180 °C to +120 °C) for integrated passive components.

Similar study on monolithic MIM capacitors investigates their behavior for wide temperature range (from −173 °C to +177 °C) [62]. Fig. 16(a) shows a linear relation between the capacitance values with the temperature variation. The total chance of capacitance across the full 350 °C temperature range is about 10%. In another research [63], the impact of temperature on both polysilicon and diffused resistors has been investigated. As shown in Fig. 16(b), it is noticed that the polysilicon resistors have a negative temperature coefficient which differs with doping type difference. On the opposite side, the diffused resistors have a positive temperature coefficient. Recent review [4] summarizes the available high-temperature commercial capacitors with temperature limit of 260 °C and commercial resistors with 350 °C.

Another important integrated passive component to be investigated and study its response with the temperature variation is the inductor. Several researchers examine the effect of temperature on both inductance and quality factor (Q) of monolithic inductors [64]. A slight variation of inductance in terms of temperature range from −55 °C to +125 °C for an on-chip spiral inductor printed in a SiGe platform has been revealed as shown in Fig. 17(a), whereas Fig. 17(b) indicates an improvement in Q along with the decreasing temperature. The latter has been confirmed by modeled and measured tests.

A discussion of the strong temperature dependence of Q explains the two mechanisms at work. The aluminum metallization of the inductor has a positive temperature coefficient of resistance, which makes the inductor loses more

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.



(a) (b)

Fig. 17. (a) Measured inductance versus frequency. (b) Modeled and measured Q versus frequency [64].

as temperature increases, but the substrate resistivity also increases with temperature, resulting in less substrate loss.

For the applications beyond the 250 °C step, most of the commonly used soft magnetic cores become paramagnetic where the inductors lose their magnetic properties. Therefore, new ferrite materials have been developed with Curie temperature more than 350 °C to overcome this issue [65].

The radiation studies are mainly focusing on microelectronic devices such as CMOS and bipolar transistors. However, less effort has been applied to investigate the impact of radiation on the passive components usually connected with the active devices and significantly affect the functionality of overall microelectronic system. The radiation effects, as mentioned before, can be distributed into three main phenomena: TID, DD, and SEEs. The passive components have no response for the TID due to the absence of the sensitive regions.

Nevertheless, the TID damage may appears as an increment of substrate coupling from the layers under the inductor, or as a deteriorated MIM capacitor dielectric. DD can affect the passive components by changing the resistivity of a resistor or modifying substrate coupling of an RF inductor. To quantify the impact of TID and DD on on-chip passive components, several studies have been done by exposing the passive elements to high proton flow [66]–[68]. The results of these studies indicate negligible variations in the passive elements values.

Regarding the SEE effect on the passive elements, a CMOS capacitor could be ruptured (fatal event), or charge might be added to a diffused region of a resistor by an ion strike with enough energy. Several studies have been performed to examine the influence of SEE on the passive elements [69]–[72].

H. Packaging

The electronic single chip and multichip packaging including the electrical, thermal, mechanical, and physical implementation have many serious challenges when the packaged electronic system is dedicated for extreme environments, especially extreme temperature applications [73]–[75].

For the low-temperature electronics, the variation of material characteristics is the principal defy of packaging. For example, the modulus of elasticity is increasing for polymers and metals, the coefficients of thermal expansion (CTE) are decreasing, the elongation is decreasing for metals and polymers, the phase transitions in metals and solders are affected, and the thermal conductivity for metals and ceramics is increasing [76].

TABLE VI

TEMPERATURE LIMITATIONS FOR VARIOUS WIRE AND PAD METALLURGIES

Pad-wire metals	Max. Temp. (°C)	Limitation
Al-Au	175	Intermetallic formation
Ni-Al	300	Kirkendal voiding
Al-Al	350-400	Decrease in mechanical properties
Au-Au	500-600	Decrease in mechanical properties
Au-Pt	600-700	Decrease in mechanical properties

Certain studies have been performed to investigate the reliability of thin-film multichip and chip on board packaging devoted for extreme low and wide range temperature applications (from −180 °C to +125 °C) [77]–[79], evaluating the materials of substrates, die attach, encapsulant, and wires. It is needless to say that the low-temperature packaging is a specialized domain limited in information and still need more investigation about the appropriate materials and reliability of different packaging approaches.

On the other face of extreme temperature applications, the high-temperature electronics packaging has faced several serious challenges like the melting of solder alloys, damage and cracking due to the CTE differences, polymeric material decomposition, diffusion, and intermetallic formation and creep.

The substrate, die and substrate attach, wire bonding, and packages are the principle sections of the packaging procedure. The recommended substrate types for high-temperature conditions are printed circuit board based on polyimide laminates to sustain a temperature of 250 °C, thick film substrates using Al_2O_3 with maximum endurable temperature of 500 °C [80] and thin film substrates with highest affordable temperature of 300 °C [81] based on Si_3N_4 and aluminum nitride (AlN).

Other substrate types dedicated for high-temperature operation are the low-temperature cofired ceramic achieving 300 °C [82], high-temperature cofired ceramic exceeding the gate of 225 °C [83], and copper foil on ceramic [84], where the researchers have demonstrated direct bond copper on aluminum oxide (Al_2O_3) for steady operation at 400 °C.

Regarding the die and substrate attach materials, we can include five main categories dedicated for high-temperature environments: the polymer attach materials reaching maximum temperature of 250 °C [85], Ag-glass with similar endurable temperature as well [85], solders and brazers where high-temperature soft solders at 200 °C have been evaluated successfully [86], and thermal cycling in the range from +40 °C to 400 °C shows cracking within the braze layer [87], transient liquid phase bonding with capability to reach 500 °C [88], and sintered nanoparticles capable to sustain 175 °C [89].

The wire-bonding materials for high-temperature conditions are mainly Au, Al, Pt, and Ni. The temperature limitations of several wire combination and pads are listed in Table VI and Al wiring to thick film Au is evaluated in [90] at 300 °C. Au and Pt wire bonding materials are investigated in [91] at 500 °C.

The packaging materials used in consumer applications are mainly plastics with endurable temperature less

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

TABLE VII
PACKAGING MATERIALS AND THEIR TEMPERATURE LIMITS

Substrate		Die & substrate attach		Wire bonding		Packages	
Material	Temp (°C)	Material	Temp (°C)	Material	Temp (°C)	Material	Temp (°C)
HTCC	225	Sintered nanoparticles	175	Nickel	300	Glass	220
PCB	250	Solders	200	Aluminum	300	Silicon	250
Thin film	300	Polymer	250	Platinum	500	Metal & ceramic	400
Cu on ceramic	400	Ag-glass	250	Gold	500	Prefired ceramic	500
Thick film	500	TLP	500			Brazed ceramic	800

than 175 °C, which is not suitable for high-temperature environments. Glass-packaging materials are appropriate for the temperature range from 180 °C to 220 °C [92], whereas the silicon encapsulants are demonstrated to perform 250 °C for continuous operation [93]. For high-temperature conditions, metal and ceramic are normally the required packaging materials exceeding the edge of 400 °C [94], with higher temperature performance of brazed ceramic reaching 800 °C [95]. Another succeeded study has been demonstrated at 500 °C using prefired ceramic layers metalized with thick Au conductors [96].

Table VII summarizes the essential parts of high-temperature packaging started by the substrate, die and substrate attach, wire bonding, and ended by types of packages including the temperature limits of the materials used in each part.

IV. CONCLUSION

The main harsh environment applications were reported in this paper. We presented the state of the art of the established and emerging electronic technologies devoted for extreme condition applications. The wide bandgap semiconductors, such as SiC and GaN, are presented as suitable candidates for extreme temperature applications exceeding the boundaries of 500 °C and 900 °C, respectively. The packaging challenges are still limiting the applicability of developed technologies despite enhancing many advanced packaging techniques with maximum endurable temperature of 500 °C for a defined time of operation. The harsh environment electronics topic and its corresponding assembly and packaging challenges are still forming hot research topics nowadays and the future will show great enhancing steps in these fields.

REFERENCES

[1] D. Brewer and J. Barth, "Extreme environment electronics in NASA's heliophysics vision," in *Extreme Environment Electronics*. Boca Raton, FL, USA: CRC Press, 2012, pp. 23–27.

[2] C. Claeys and E. Simoen, *Radiation Effects in Advanced Semiconductor Materials and Devices*. New York, NY, USA: Springer-Verlag, vol. 57, 2013.

[3] E. Kolawa, M. Mojarradi, and C. L. Del, "Extreme environments in NASA planetary exploration," in *Extreme Environment Electronics*, vol. 42. Boca Raton, FL, USA: CRC Press, 2012, pp. 11–22.

[4] J. Watson and G. Castro, "A review of high-temperature electronics technology and applications," *J. Mater. Sci., Mater. Electron.*, vol. 26, no. 12, pp. 9226–9235, 2015.

[5] P. L. Dreike, D. M. Fleetwood, D. B. King, D. C. Sprauer, and T. E. Zipperian, "An overview of high-temperature electronic device technologies and potential applications," *IEEE Trans. Compon., Packag., Manuf. Technol., A*, vol. 17, no. 4, pp. 594–609, Dec. 1994.

[6] P. G. Neudeck, R. S. Okojie, and L.-Y. Chen, "High-temperature electronics—A role for wide bandgap semiconductors?" *Proc. IEEE*, vol. 90, no. 6, pp. 1065–1076, Jun. 2002.

[7] H. A. Mantooth, M. M. Mojarradi, and R. W. Johnson, "Emerging capabilities in electronics technologies for extreme environments part 1—High temperature electronics," *IEEE Power Electron. Soc. Newslett.*, vol. 18, no. 1, pp. 9–14, 1st Quart., 2006.

[8] "The world market for high temperature electronics," AEA Technol. PLC, Oxford, U.K., HITEN Rep., 1997.

[9] B. W. Ohme, T. B. Lucking, G. R. Gardner, E. E. Vogt, and J. C. Tsang, *High Temperature 0.8 Micron 5V SOI CMOS for Analog/Mixed Signal Applications*, document DE-FC26-03NT41834, Oil & Natural Gas Technology, Nov. 2007, p. 43.

[10] M. A. Huque, S. K. Islam, L. M. Tolbert, and B. J. Blalock, "A 200 °C universal gate driver integrated circuit for extreme environment applications" *IEEE Trans. Power Electron.*, vol. 27, no. 9, pp. 4153–4162, Sep. 2012.

[11] E. H. Boufouss, L. A. Francis, V. Kilchytska, P. Gérard, P. Simon, and D. Flandre, "Ultra-low power high temperature and radiation hard complementary metal-oxide-semiconductor (CMOS) silicon-on-insulator (SOI) voltage reference," *Sensors*, vol. 13, no. 12, pp. 17265–17280, 2013.

[12] B. Ohme, "High-temperature SOI technologies at Honeywell," in *Extreme Environment Electronics*, J. D. Cressler and H. A. Mantooth, Eds. Boca Raton, FL, USA: CRC Press, 2013.

[13] T. J. Thornton, W. Lepkowski, S. J. Wilk, M. R. Ghajar, A. Balijepalli, and J. Ervin, "CMOS-compatible silicon-on-insulator MESFETs for extreme environments," in *Extreme Environment Electronics*. Boca Raton, FL, USA: CRC Press, 2012, pp. 253–261.

[14] W. Lepkowski, M. R. Ghajar, S. J. Wilk, N. Summers, T. J. Thornton, and P. S. Fechner, "Scaling SOI MESFETs to 150-nm CMOS technologies," *IEEE Trans. Electron Devices*, vol. 58, no. 6, pp. 1628–1634, Jun. 2011.

[15] J. D. Cressler, "Silicon-germanium as an enabling technology for extreme environment electronics," *IEEE Trans. Device Mater. Rel.*, vol. 10, no. 4, pp. 437–448, Dec. 2010.

[16] J. D. Cressler and G. Niu, *Silicon-Germanium Heterojunction Bipolar Transistors*. Norwood, MA, USA: Artech House, 2003.

[17] J. D. Cressler, Ed., *Silicon Heterostructure Handbook: Materials, Fabrication, Devices, Circuits and Applications of SiGe and Si Strained-Layer Epitaxy*. Boca Raton, FL, USA: CRC Press, 2005.

[18] J. D. Cressler, "Radiation effects in SiGe technology," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 3, pp. 1992–2014, Jun. 2013.

[19] T. Chen *et al.*, "On the high-temperature (to 300 °C) characteristics of SiGe HBTs," *IEEE Trans. Electron Devices*, vol. 51, no. 11, pp. 1825–1832, Nov. 2004.

[20] A. K. Sutton *et al.*, "An investigation of dose rate and source dependent effects in 200 GHz SiGe HBTs," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3166–3174, Dec. 2006.

[21] T. D. England *et al.*, "A new approach to designing electronic systems for operation in extreme environments: Part II—The SiGe remote electronics unit," *IEEE Aerosp. Electron. Syst. Mag.*, vol. 27, no. 7, pp. 29–41, Jul. 2012.

[22] L. Najafizadeh *et al.*, "Sub-1-K operation of SiGe transistors and circuits," *IEEE Electron Device Lett.*, vol. 30, no. 5, pp. 508–510, May 2009.

[23] J. C. Bardin and S. Weinreb, "A 0.1–5 GHz cryogenic SiGe MMIC LNA," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 6, pp. 407–409, Jun. 2009.

[24] N. Nambiar *et al.*, "SiGe BiCMOS 12-bit 8-channel low power Wilkinson ADC," in *Proc. 51st Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2008, pp. 650–653.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

[25] Z. Chen and F. F. Dai, "A 3mW 8-bit radiation-hardened-by-design DAC for ultra-wide temperature range from −180 °C to 120 °C," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2011, pp. 997–1000.

[26] B. Sissons, A. Mantooth, J. Di, J. A. Holmes, and A. M. Francis, "SiGe BiCMOS comparator for extreme environment applications," in *Proc. IEEE Aeros. Conf.*, Mar. 2015, pp. 1–8.

[27] A. S. Cardoso *et al.*, "On the cryogenic RF linearity of SiGe HBTs in a fourth-generation 90-nm SiGe BiCMOS technology," *IEEE Trans. Electron Devices*, vol. 62, no. 4, pp. 1127–1135, Apr. 2015.

[28] P. G. Neudeck, "SiC integrated circuit platforms for high-temperature applications," in *Extreme Environment Electronics*. Boca Raton, FL, USA: CRC Press, 2012, pp. 225–232.

[29] W. C. Lien, N. Damrongplasit, J. H. Paredes, D. G. Senesky, T. J. K. Liu, and A. P. Pisano, "4H-SiC N-channel JFET for operation in high-temperature environments," *IEEE J. Electron Devices Soc.*, vol. 2, no. 6, pp. 164–167, Nov. 2014.

[30] S. Singh and J. A. Cooper, "Bipolar integrated circuits in 4H-SiC," *IEEE Trans. Electron Devices*, vol. 58, no. 4, pp. 1084–1090, Apr. 2011.

[31] P. G. Neudeck *et al.*, "6H-SiC transistor integrated circuits demonstrating prolonged operation at 500 C," presented at the Int. Conf. High Temperature Electron., 2008.

[32] P. G. Neudeck *et al.*, "Extreme temperature 6H-SiC JFET integrated circuit technology," *Phys. Status Solidi A*, vol. 206, no. 10, pp. 2329–2345, 2009.

[33] N. Kuhns *et al.*, "Complex high-temperature CMOS silicon carbide digital circuit designs," *IEEE Trans. Device Mater. Rel.*, vol. 16, no. 2, pp. 105–111, Jun. 2016.

[34] H. Elgabra and S. Singh, "High temperature simulation of 4H-SiC bipolar circuits," *J. Electron Devices Soc.*, vol. 3, no. 3, pp. 302–305, May 2015.

[35] A. Rahman *et al.*, "High-temperature SiC CMOS comparator and op-amp for protection circuits in voltage regulators and switch-mode converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 935–945, Sep. 2016.

[36] J. Yang, "A harsh environment wireless pressure sensing solution utilizing high temperature electronics," *Sensors*, vol. 13, no. 3, pp. 2719–2734, 2013.

[37] M. Alexandru *et al.*, "SiC integrated circuit control electronics for high-temperature operation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 3182–3191, May 2015.

[38] J. A. Valle-Mayorga, A. Rahman, and H. A. Mantooth, "A SiC NMOS linear voltage regulator for high-temperature applications," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2321–2328, May 2014.

[39] M. Alexandru, M. Florentin, A. Constant, B. Schmidt, P. Michel, and P. Godignon, "5 MeV proton and 15 MeV electron radiation effects study on 4H-SiC nMOSFET electrical parameters," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 4, pp. 1732–1738, Aug. 2014.

[40] A. Siddiqui, H. Elgabra, and S. Singh, "The current status and the future prospects of surface passivation in 4H-SiC transistors," *IEEE Trans. Device Mater. Rel.*, vol. 16, no. 3, pp. 419–428, Sep. 2016.

[41] S. C. Shen, "III-nitride platforms," in *Extreme Environment Electronics*. Boca Raton, FL, USA: CRC Press, 2012, pp. 263–273.

[42] H. A. Mantooth and J. D. Cressler, "Power device platforms," in *Extreme Environment Electronics*, H. A. Mantooth, Ed. Boca Raton, FL, USA: CRC Press, 2013, p. 243.

[43] X. Ke, J. Sankman, Y. Chen, L. He, and D. B. Ma, "A 10 MHz 3-to-40V V_{IN} tri-slope gate driving GaN DC–DC converter with 40.5dB μV spurious noise compression and 79.3% ringing suppression for automotive applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 430–431.

[44] A. Seidel and B. Wicht, "A 1.3 A gate driver for GaN with fully integrated gate charge buffer capacitor delivering 11nC enabled by high-voltage energy storing," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 432–433.

[45] Y.-C. Lee *et al.*, "GaN/InGaN heterojunction bipolar transistors with ultra-high DC power density (> 3 MW/cm^2)," *Phys. Status Solidi A*, vol. 209, no. 3, pp. 497–500, 2012, doi: 10.1002/pssa.201100436.

[46] J. Du, K. Ma, Z. Zhao, and Q. Yu, "Simulation of trap state effects in GaN DHFETs on buffer leakage current and breakdown voltage," in *Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits (EDSSC)*, Jun. 2013, pp. 1–2.

[47] J. K. Kaushik, V. R. Balakrishnan, B. S. Panwar, and R. Muralidharan, "Analysis of fast and slow trap states on electrical performance of AlGaN/GaN HEMTs," in *Proc. IEEE 2nd Int. Conf. Emerg. Electron. (ICEE)*, Dec. 2014, pp. 1–3.

[48] K. Kumakura and T. Makimoto, "High-temperature characteristics up to 590 °C of apnp AlGaN/GaN heterojunction bipolar transistor," *Appl. Phys. Lett.*, vol. 94, no. 10, p. 103502, 2009.

[49] R. D. Harris *et al.*, "Radiation characterization of commercial GaN devices," in *Proc. IEEE Radiat. Effects Data Workshop*, Jul. 2011, pp. 1–5.

[50] E. Patrick *et al.*, "Modeling proton irradiation in AlGaN/GaN HEMTs: Understanding the increase of critical voltage," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4103–4108, Dec. 2013.

[51] D. Maier *et al.*, "InAlN/GaN HEMTs for operation in the 1000° regime: A first experiment," *IEEE Electron Device Lett.*, vol. 33, no. 7, pp. 985–987, Jul. 2012.

[52] P. Herfurth *et al.*, "Ultrathin body InAlN/GaN HEMTs for high-temperature (600 °C) electronics," *IEEE Electron Device Lett.*, vol. 34, no. 4, pp. 496–498, Apr. 2013.

[53] Z. Xu *et al.*, "High temperature characteristics of GaN-based inverter integrated with enhancement-mode (E-mode) MOSFET and depletion-mode (D-mode) HEMT," *IEEE Electron Device Lett.*, vol. 35, no. 1, pp. 33–35, Jan. 2014.

[54] R. Gaska *et al.*, "Novel AlInN/GaN integrated circuits operating up to 500 °C," *Solid-State Electron.*, vol. 113, pp. 22–27, Nov. 2015.

[55] T. Hussain *et al.*, "GaN HFET digital circuit technology," in *Proc. Int. Conf. Compound Semiconductor Manuf. Technol.*, 2004.

[56] K. Gottfried *et al.*, "A high temperature stable metallization scheme for SiC-technology operating at 400 °C in air," in *Materials Science Forum*, vol. 264. New York, NY, USA: Trans Tech, 1998, pp. 795–798.

[57] R. S. Okojie, D. Lucko, and D. Spry, "Reliability of Ti/TaSi/Pt ohmic contacts on 4H- and 6H-SiC after 1000 hours in air at 600 °C," in *Proc. Electron. Mater. Conf.*, Notre Dame, IN, USA, Jun. 2001, p. 6.

[58] F. Lin *et al.*, "Low resistance Ti/Al/Ni/Au ohmic contact to $(NH_4)_2S_x$ treated n-type GaN for high temperature applications," in *Proc. 9th Int. Conf. Solid-State Integr.-Circuit Technol. (ICSICT)*, Oct. 2008, pp. 726–729.

[59] R. Cuerdo, J. Pedros, and F. Calle, "Characterization of Schottky contacts on n-GaN at high temperature," in *Proc. Spanish Conf. Electron Devices*, Feb. 2005, pp. 175–178.

[60] J. Bourne, R. Schupbach, B. Hollosi, J. Di, A. Lostetter, and H. A. Mantooth, "Ultra-wide temperature (−230 °C to 130 °C) DC-motor drive with SiGe asynchronous controller," in *Proc. IEEE Aeros. Conf.*, Mar. 2008, pp. 1–15.

[61] D. Ma, X. Geng, F. F. Dai, and J. D. Cressler, "A 6th order butterworth SC low pass filter for cryogenic applications from −180 °C to 120 °C," in *Proc. Aeros. Conf.*, Mar. 2009, pp. 1–8.

[62] S. Becu, S. Cremer, O. Noblanc, J. L. Autran, and P. Delpech, "Characterization and modeling of Al_2O_3/MIM capacitors: Temperature and electrical field effects," in *Proc. 35th IEEE Eur. Solid-State Device Res. Conf.*, Sep. 2005, pp. 265–268.

[63] H.-M. Chuang, K.-B. Thei, S.-F. Tsai, and W.-C. Liu, "Temperature-dependent characteristics of polysilicon and diffused resistors," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1413–1415, May 2003.

[64] R. Groves, D. L. Harame, and D. Jadus, "Temperature dependence of Q and inductance in spiral inductors fabricated in a silicon-germanium/BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 32, no. 9, pp. 1455–1459, Sep. 1997.

[65] J. Galipeau and G. Slama, "Reliability testing on a multilayer chip inductor fabricated from a ferrite with a 350 °C curie point," *Additional Papers Presentations*, vol. 2011, pp. 14–20, Jan. 2011.

[66] J. D. Cressler *et al.*, "Proton radiation response of SiGe HBT analog and RF circuits and passives," *IEEE Trans. Nucl. Sci.*, vol. 48, no. 6, pp. 2238–2243, Dec. 2001.

[67] Z. Luo *et al.*, "Proton radiation effects in 4H-SiC diodes and MOS capacitors," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3748–3752, Dec. 2004.

[68] S. O. Dorst and L. H. Wurzel, "The effect of radiation environment on film resistors," in *Proc. IRE Nat. Convention*, Mar. 1962, pp. 206–214.

[69] T. Wang, K. Wang, L. Chen, A. Dinh, B. Bhuva, and R. Shuler, "A RHBD LC-tank oscillator design tolerant to single-event transients," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3620–3625, Dec. 2010.

[70] B. D. Olson, W. T. Holman, L. W. Massengill, B. L. Bhuva, and P. R. Fleming, "Single-event effect mitigation in switched-capacitor comparator designs," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 3440–3446, Dec. 2008.

[71] A. L. Sternberg, L. W. Massengill, M. Hale, and B. Blalock, "Single-event sensitivity and hardening of a pipelined analog-to-digital converter," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3532–3538, Dec. 2006.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

[72] G. K. Lum *et al.*, "New experimental findings for single-event gate rupture in MOS capacitors and linear devices," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3263–3269, Dec. 2004.

[73] A. Hassan, B. Gosselin, and M. Sawan, "Ultra-low power CMOS voltage reference for high temperature applications up to 300 °C," in *Proc. IEEE Int. Conf. Electron., Circuits, Syst. (ICECS)*, Dec. 2015, pp. 77–80.

[74] A. Hassan, A. Trigui, U. Shafique, Y. Savaria, and M. Sawan, "Wireless power transfer through metallic barriers enclosing a harsh environment; feasibility and preliminary results," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2016, pp. 2391–2394.

[75] A. Hassan, M. Ali, H. S. Trigui, Y. Savaria, and M. Sawan, "Stability of GaN150-based HEMT in high temperature up to 400 °C," in *Proc. 15th IEEE Int. New Circuits Syst. Conf. (NEWCAS)*, Jun. 2017, pp. 133–136.

[76] J. L. Sepulveda, "Advanced microelectronic packaging using BeO ceramics," in *Proc. 4th Int. Symp. Adv. Packag. Mater.*, Mar. 1998, pp. 287–293.

[77] S. Sivaswamy *et al.*, "System-in-package for extreme environments," in *Proc. 58th Electron. Compon. Technol. Conf. (ECTC)*, May 2008, pp. 2044–2050.

[78] A. A. Shapiro, C. Tudryn, D. Schatzel, and S. Tseng, "Electronic packaging materials for extreme, low temperature, fatigue environments," *IEEE Trans. Adv. Packag.*, vol. 33, no. 2, pp. 408–420, May 2010.

[79] Y. Chen, C. T. Weber, M. Mojarradi, and E. Kolawa, "Micro- and nano-electronic technologies and their qualification methodology for space applications under harsh environments," *Proc. SPIE*, vol. 8031, p. 80311Y, May 2011.

[80] J. E. Naefe, R. W. Johnson, and R. R. Grzybowski, "High-temperature storage and thermal cycling studies of thick film and wirewound resistors," *IEEE Trans. Compon. Packag. Technol.*, vol. 25, no. 1, pp. 45–52, Mar. 2002.

[81] K. Fang, R. Zhang, T. Isaacs-Smith, R. W. Johnson, E. Andarawis, and A. Vert, "Thin film multichip packaging for high temperature digital electronics," *Additional Papers Presentations*, vol. 2011, pp. 39–45, Jan. 2011.

[82] T. Zhang, D. Shaddock, A. Vert, R. Zhang, and R. W. Johnson, "Characterization of LTCC-thick film technology for 300 °C packaging," *Additional Papers Presentations*, vol. 2011, pp. 46–51, Jan. 2011.

[83] *Communication With Milton Watts*, Quartzdyne, Salt Lake, UT, USA.

[84] G. Dong, G. Lei, X. Chen, K. Ngo, and G. Q. Lu, "Edge tail length effect on reliability of DBC substrates under thermal cycling," *Soldering Surf. Mount Technol.*, vol. 21, no. 3, pp. 10–15, 2009.

[85] R. Klieber and R. Lerch, "Evaluation of materials for high temperature IC packaging," in *Proc. 15th Int. Workshop Thermal Invest. ICs Syst. (THERMINIC)*, Oct. 2009, pp. 117–120.

[86] H. Schoeller, S. Bansal, A. Knobloch, D. Shaddock, and J. Cho, "Effects of microstructure evolution on high-temperature mechanical deformation of 95Sn-5Sb," in *Proc. ASME Int. Mech. Eng. Congr. Expo.*, Jan. 2008, pp. 25–32.

[87] V. Bondarenko *et al.*, "Characterization and packaging of SiC JFET power modules for extreme environment motor drives," in *Proc. Int. High Temperature Electron. Conf.*, Santa Fe, NM, USA, May 2006, pp. 456–488.

[88] P. Hagler, R. W. Johnson, and L. Y. Chen, "SiC die attach metallurgy and processes for applications up to 500 °C," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 1, no. 4, pp. 630–639, Apr. 2011.

[89] C. Göbl and J. Faltenbacher, "Low temperature sinter technology die attachment for power electronic applications," in *Proc. 6th Int. Conf. Integr. Power Electron. Syst. (CIPS)*, Mar. 2010, pp. 1–5.

[90] D. Palmer and F. Ganyard, "Aluminum wire to thick-film connections for high-temperature operation," *IEEE Trans. Compon., Hybrids, Manuf. Technol.*, vol. CHMT-1, no. 3, pp. 219–222, Sep. 1978.

[91] J. S. Salmon, R. W. Johnson, and M. Palmer, "Thick film hybrid packaging techniques for 500 °C operation," in *Proc. 4th Int. High Temperature Electron. Conf. (HITEC)*, Jun. 1998, pp. 103–108.

[92] K. Okamoto, Y. Takematsu, M. Hitomi, Y. Ikeda, and Y. Takahashi, "Nanocomposite epoxy resin for SiC module," *Additional Papers Presentations*, vol. 2011, pp. 196–200, Jan. 2011.

[93] Y. Yao, G.-Q. Lu, Z. Chen, D. Boroyevich, and K. D. T. Ngo, "Assessment of encapsulants for high-voltage, high-temperature power electronic packaging," in *Proc. IEEE Electr. Ship Technol. Symp. (ESTS)*, Apr. 2011, pp. 258–264.

[94] M. R. Werner and W. R. Fahrner, "Review on materials, microsensors, systems and devices for high-temperature and harsh-environment applications," *IEEE Trans. Ind. Electron.*, vol. 48, no. 2, pp. 249–257, Apr. 2001.

[95] A. Friedberger *et al.*, "Reusable packaging for high temperature (800 °C) and high-pressure MEMS," in *Proc. High Temperature Electron. Conf. (HiTEC)*, May 2006, pp. 367–370.

[96] L. Y. Chen, "Improvement of dielectric performance of a prototype AlN high temperature chip-level package," *Additional Papers Presentations*, vol. 2011, pp. 52–57, Jan. 2011.

Ahmad Hassan (S'09) received the B.Eng. degree in electrical engineering from Beirut Arab University, Beirut, Lebanon, in 2011. He is currently working toward the Ph.D. degree at the Polystim Neurotechnologies Laboratory, Polytechnique Montréal, Montreal, QC, Canada.

His current research interests include high-temperature microelectronics, particularly design and implementation of wireless power and data transmission systems dedicated for harsh environment applications.

Yvon Savaria (S'77–M'86–SM'97–F'08) received the B.Ing. and M.Sc.A. degrees in electrical engineering from Polytechnique Montréal, Montreal, QC, Canada, in 1980 and 1982, respectively, and the Ph.D. degree in electrical engineering from McGill University, Montreal, QC, Canada, in 1985.

He was the thesis advisor of 140 graduate students who completed their studies. Since 1985, he has been at Polytechnique Montréal, where he is currently a Professor and a Chairman at the Department of Electrical Engineering. He is currently involved in several projects that relate to aircraft embedded systems, green IT, wireless sensor network, virtual network, computational efficiency and application specific architecture design. He has authored or coauthored 97 journal papers and 354 conference papers. He holds 16 patents. His current research interests include microelectronic circuits and microsystems such as testing, verification, validation, clocking methods, defect and fault tolerance, effects of radiation on electronics, high-speed interconnects and circuit design techniques, computer-aided design methods, reconfigurable computing and applications of microelectronics to telecommunications, aerospace, image processing, video processing, radar signal processing, and digital signal processing acceleration.

Dr. Savaria is a member of the Regroupement Stratégique en Microélectronique du Québec, of the Ordre des Ingénieurs du Québec. He has been a member of CMC Microsystems Board since 1999 and the Chairman of that board from 2008 to 2010. He was a Program Co-Chairman of ASAP'2006 and the General Co-Chair of ASAP'2007. He was a consultant or was sponsored for carrying research by Bombardier, CNRC, Design Workshop, Dolphin, DREO, Genesis, Gennum, Hyperchip, ISR, LTRIM, Miranda, MiroTech, Nortel, Octasic, PMC-Sierra, Technocap, Thales, Tundra, and VXP. He was a recipient of a Tier 1Canada Research Chair (www.chairs.gc.ca) on design and architectures of advanced microelectronic systems in 2001 and the Synergy Award of the Natural Sciences and Engineering Research Council of Canada in 2006.

Mohamad Sawan (S'88–M'89–SM'96–F'04) received the Ph.D. degree in electrical engineering from Sherbrooke University, Sherbrooke, QC, Canada, in 1990.

In 1991, he joined Polytechnique Montréal, Montreal, QC, Canada, where he is currently a Professor of Microelectronics and Biomedical Engineering. He is currently the Founder and the Director of the Polystim Neurotechnologies Laboratory, Polytechnique Montréal. He offered more than 225 talks in many cities around the world. He has authored more than 700 peer-reviewed papers, 2 books, and 12 book chapters. He holds 12 patents. His current research interests include mixed-signal circuits and microsystems.

Dr. Sawan is a Fellow of the Canadian Academy of Engineering, the Engineering Institute of Canada, and Officer of the National Order of Quebec. He was the General Chair of the 2016 IEEE International Symposium on Circuits and Systems. He is involved in co-chairing annual NEWCAS and ICM conferences. He leads the Microsystems Strategic Alliance of Quebec. He was a recipient of several awards, among them the Queen-Elizabeth II Diamond Jubilee Medal, the ACFAS Bombardier and Jacques-Rousseau Awards, the CIHR's Barbara Turnbull Award, and the Canada Research Chair in smart medical devices from 2001 to 2015. He is the Founder and/or Co-Founder of several IEEE international conferences, including NEWCAS, ICECS, and BioCAS. He is the Co-Founder and the Editor-in-chief of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS and an Associate Editor of the IEEE TRANSACTIONS ON BIOMEDICAL ENGINEERING, and the *International Journal on Circuit Theory and Applications*. He was the Deputy Editor-in-Chief of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS.