Toward an Energy-Efficient High-Voltage Compliant Visual Intracortical Multichannel Stimulator

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***Abstract*— We present, in this paper, a new multichip system aimed toward building an implantable visual intracortical stimulation device. The objective is to deliver energy-optimum pulse patterns to neural sites with needed compliance voltage across high electrode–tissue interface impedance of implantable microelectrodes. The first chip is an energy-efficient stimuli generator (SG), and the second one is a high-impedance microelectrode array driver (MED) output stage. The four-channel SG produces rectangular, half-sine, plateau-sine, and other types of current pulse with stimulation current ranging from 2.32 to 220 μA per channel. The microelectrode array driver is able to deliver 20 V per anodic or cathodic phase across the microelectrode–tissue interface for ±13 V power supplies. The MED supplies different current levels with the maximum value of 400 μA per input and 100 μA per output channel simultaneously to 8–16 stimulation sites through microelectrodes, connected either in bipolar or monopolar configuration. Both chips receive power via inductive link and data through capacitive coupling. The SG and MED chips have been fabricated in 0.13-μm CMOS and 0.8-μm 5-/20-V CMOS/double-diffused metal-oxide-semiconductor technologies. The measured dc power budgets consumed by low- and mid-voltage chips are 2.56 and 2.1 mW consecutively. The system, modular in architecture, is interfaced with a newly developed platinum-coated pyramidal microelectrode array. *In vitro* test results with 0.9% phosphate buffer saline show the microelectrode impedance of 70 kΩ at 1 kHz.**

***Index Terms*— Energy-efficient stimuli-generator (SG), high-impedance microelectrode driver, high-voltage compliance, implantable biomedical device, intracortical microstimulation, microelectrode array (MEA), visual prosthesis.**

I. Introduction

FUNCTIONAL electrical stimulation (FES), a technique to restore the impaired physiological functions, has been used in biomedical devices for various applications, such as cardiac pacemaker [1], urinary implant [2], stimulator for motor nerves [3] and epilepsy [4], and cochlear implant [5]. A growing effort among the researchers, since the experiments of Brindley and Lewin [6], is to apply FES to partially recuperate the loss of sight of completely blind people. Along the visual pathways, the locations for neural stimulation are the retina, the optic nerve, the dorsal lateral geniculate nucleus of the thalamus, and the primary visual cortex [7]. The intracortical implant takes into account more diseases to treat, and a high resolution of visual function can be restored, as many microelectrodes can be implanted in the spacious primary visual cortex. Research teams have estimated that 625 [9]–1000 [10]–[13] phosphenes in the visual field are needed to create useful vision. For a wirelessly controlled microstimulator, data rate higher than most neuroprosthetic devices is required to stimulate such a large number of sites.

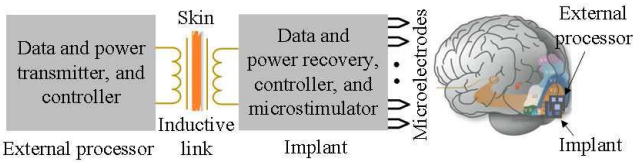

Fig. 1. Main parts of an implantable visual intracortical stimulator [8].

On the other hand, the complex electrode–tissue interface (ETI) impedance and the charge transfer capability through it play a critical role in the design of a low-power microstimulator. Therefore, results of chronic implantation of microelectrode arrays (MEAs) in the V1 area [14] have been studied, and models of ETI impedance have been proposed by different research groups [15]. This impedance is affected by various parameters, such as the electrode-geometry and fabrication material, exposed tip area, and coating material, in addition to the stimulus parameters. In the case of intracortical microstimulation, measured resistive impedance of micromachined microelectrodes varies from 70 to 400 kΩ [16]–[19].

The outcomes of these investigations and the progress in leading-edge microelectronic technologies allow the researchers to design custom miniaturized implantable intracortical brain–machine interfaces (BMIs). The typical architecture of a BMI intended for visual intracortical stimulation is presented in Fig. 1, which includes an external controller to transmit data and power wirelessly to the implant and an implant to recover both data and power, control the stimulation parameters, and apply the stimuli to neural sites through MEAs. Most of the reported microstimulators for visual prostheses aimed at retinal stimulation. A few architectures have been destined for intracortical microstimulation. A highly flexible microstimulation platform

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designed by Coulombe *et al.* [7] uses an external image sensor, an external controller, inductive-link for data and power transmission, an interface module, and an implant. This system was verified through *in vivo* experiments on rats. Another system, developed by Ghovanloo and Najafi [9], emphasizes on high-output impedance. *In vivo* experiments on rats were performed to verify the efficacy of the latter system. Also, Yao *et al.* [20] proposed a wired 64-channel implant, assembled in 3-D. This prototype has been tested on guinea pigs. However, high-voltage compliance issue was not dealt with, and energy-efficiency of stimulation waveforms was not addressed in those systems. More recently, both high-voltage compliance requirement and energy-optimum stimulation waveform have been considered in the design by Ethier and Sawan [21], but the output stage consumes large power due to the on-chip dc–dc step-up converter. Therefore, the dc–dc step-up converter has been eliminated in the output stage of our proposed architecture. The stimulator in [22] achieved only over 10 V for biphasic operation, when supplied with 12 V.

Regardless of applications and designs, all microstimulators must choose amplitude, interphase and pulse durations, frequency, and direction of stimulation pulses precisely to execute charge balanced stimulation and block the discharge of toxic ions in the stimulation sites, produced by irreversible faradic electrochemical reactions [23]. This condition can be met using current-mode stimulation, which allows to control delivered charge quantity meticulously. A number of charge balancing schemes have been presented in [24] and [25] to control stimulation precisely. The aforementioned stimulation parameters also modulate the threshold of action potential and elicited phosphene features (size, duration, and intensity) [26]. The stimulation current of around 100 μA [7], required to stimulate intracortical neurons and the aforesaid high ETI impedance, rationalizes the necessity of high-voltage compliance up to 15 V [21] across the microelectrodes. The first contribution of this paper is the design, fabrication, and validation of a highly configurable multichannel high-voltage compliant microelectrode array driver chip [27].

Most of the intracortical microstimulators use rectangular waveform for biphasic stimulation. Compared with other pulse types, this constant current pulse delivers maximum charge quantity and is relatively easy to generate [28]. A criterion to construct an energy-efficient stimulation-current waveform can be formulated applying the principle of least action [29] to FES [28]. Various waveforms have been studied by many authors, who came to different conclusions. In [30], truncated Gaussian waveform with a constant base current, which we call plateau-Gaussian, has been found to be energy optimal for pulse-widths of 20–200 μs. An extensive investigation on various waveforms carried out by Krouchev *et al.* [31] claimed that rectangular and half-sine (HS) pulses, latter one being a close approximation of a truncated Gaussian pulse, are energy optimum for short and long pulse (5 ms) durations. This plateau-Gaussian [or plateau-sine (PS)] pulse is nothing but a linear summation of rectangular and Gaussian (or sine) pulses. Therefore, it is highly desirable to design a stimuli generator (SG), which is capable to produce constant, HS, and

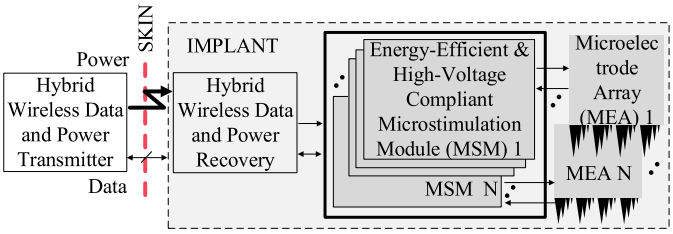


Fig. 2. Overview of the architecture of the proposed visual intracortical microstimulator. A single hybrid wireless data and power receiver block transmits stimulation parameters and delivers power to N number of MSMs. Each MSM is connected to a single MEA.

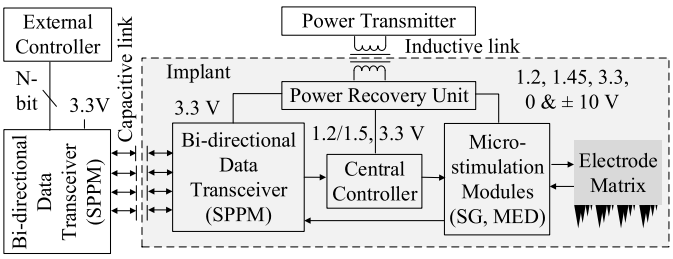


Fig. 3. Architecture of the proposed visual intracortical microstimulator. Each stimulation module is designed to drive an array of 16 microelectrodes.

PS current pulses for efficient stimulation of neural tissues and saving energy. To the best of our knowledge, microstimulators implemented in [32] and [33] considered stimulation-efficient waveforms. The second contribution of this paper is the design and fabrication of a SG chip, which implemented additional energy-optimum stimulation pulses.

The third contribution is the implementation of a rectifier chip satisfying the standard of biomedical devices, as a part of the wireless power recovery unit, which provides the required supply voltages to the implant.

The microstimulator has been assembled on a single platform, interfaced with a novel MEA [16] and successfully validated through *in vitro* experiments, which is the fourth contribution of this paper. The remaining parts of this paper are as follows. Section II presents the proposed microstimulator and working principles of some functional units. It is followed by Section III, which shows the experimental results, specifications, and comparison with other works. Finally, in Section IV, we conclude with recommendations for future work.

II. Proposed System

In this paper, we propose a new highly configurable microstimulation system. A brief overview of the proposed system is presented in Fig. 2, meeting our desired objectives. The system consists of hybrid wireless data and power transmitter and receiver blocks to transmit stimulation control parameters and deliver power to N number of energy-efficient and high-voltage compliant microstimulation modules (MSMs). Each MSM is modular in architecture and delivers stimulation current to 16 output channels, interfaced with a novel platinum-coated MEA. The detailed architecture, presented in Fig. 3, consists of four major building blocks: 1) high data-rate transceiver [34]; 2) power recovery unit; 3) central controller;

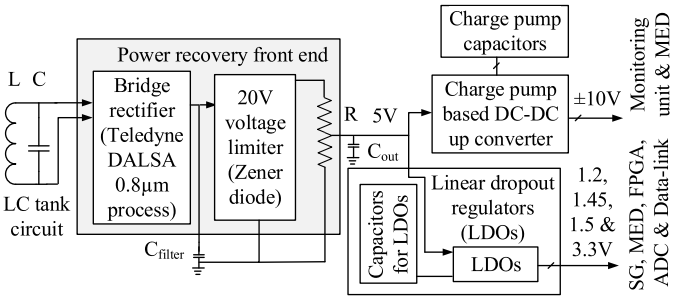


Fig. 4. Schematics of the power recovery unit. The rectifier chip is designed in Teledyne DALSA C08E 0.8-μm 20 V CMOS/DMOS process. The 20-V Zener diode, resistor R, inductor L, capacitors C, C_{filter}, C_{out}, LDOs, and the charge pump-based dc–dc converter are discrete components.

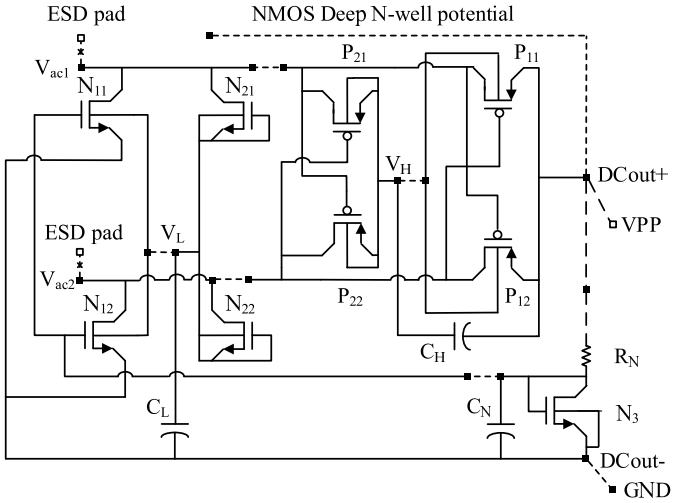


Fig. 5. Circuit diagram of the rectifier chip designed using 20-V transistors [37].

and 4) several MSMs. A comprehensive design description and the experimental results of block 1) along with the advantages of capacitive data link have already been presented in [35]. The working and design principles of building blocks 2)–4) are summarized in Sections II-A–II-C, with emphasis given primarily on three integrated circuits (ICs).

A. Power Recovery Unit

The architecture of this unit is shown in Fig. 4. The electromagnetic energy to the implant is transmitted from an external power transmitter through a spiral antenna. The parallel LC resonant circuit is tuned at 13.56-MHz frequency, which is within the industrial-scientific-medical radio band. The inductive voltage is rectified using a full-wave bridge rectifier, which is designed in Teledyne DALSA 5-/20-V CMOS/double-diffused metal-oxide-semiconductor (DMOS) technology [36], [37]. The functional principle and design methodology will be summarized here.

The main rectifier, presented in Fig. 5, consists of the transistors (N_{11}, N_{12}, P_{11}, and P_{12}), where (P_{11}, P_{12}) are connected in a cross-coupled manner and (N_{11}, N_{12}) are diode-connected with Vth canceling technique. With a large resistance R_N, a small current biases the diode-connected transistor N_3. The resulting voltage at the terminal of N_3 is maintained by the capacitor C_N and is applied to the gates of the transistors (N_{11}, N_{12}). This gate voltage allows to virtually cancel their threshold voltages. The transistors (N_{21}, N_{22}, P_{21}, and P_{22}) form a secondary rectifier, which, thanks to the integrated capacitors C_H and C_L, generates the higher voltage V_H and the lower voltage V_L. These voltages are applied to the substrates of the pMOS and nMOS transistors, respectively. The secondary rectifier, not carrying high currents, is much smaller but protects the main rectifier of a possible clamping and prevents leakage current to the substrate, when the output current increases. Moreover, the rectifier is optimized for maximum power efficiency at a load of 3–5 mA. For testability and investigation purposes, the chip was designed with many external connections from the outside, as shown by broken lines in Fig. 5. This design procedure not only allows access to certain internal nodes for measurements but also permits to apply external voltages to verify the impact on the performance of the rectifier. Thus, among others, the nodes which can be accessed are the common gate and common substrate of the transistors (N_{11}, N_{12}), and the common substrate of the transistors (P_{11}, P_{12}).

In Fig. 4, the 20-V off-chip Zener diode limits the rectified voltage to 20 V, which is the maximum possible value for the used technology. C_{filter} eliminates the effect of ripple in the rectified voltage. The rectified voltage is adjusted to 5 V, which is applied to a charge pump-based dc–dc step-up converter, to generate $\pm$10 V, required for the biphasic microstimulation, performed by the high-voltage output stage of the microstimulator. A number of low-dropout (LDO) dc voltage regulators have been used to generate 1.2, 1.45, 1.5, and 3.3 V needed by the rest of blocks of the implant. The rectifier chip and the discrete components are assembled on a single miniature printed circuit board (PCB).

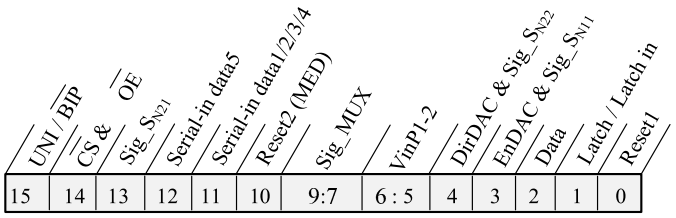


Fig. 6. 16-bit data stream containing stimulation parameters for the SG and microelectrode driver chips, and the SAR ADC.

B. Central Controller

The central controller receives stimulation control parameters serially from the internal capacitive-link data receiver [35] and stores the data in a 16-bit serial-in parallel-out (SIPO) shift register. The information bits of the register are shown in Fig. 6. Bit[0, 2, 5:9] are to program the SG and multiplexer (MUX), bit[1, 3:4] control both chips, bit[10:13] provide stimulation parameters to the microelectrode driver, and bit[14:15] program the SAR ADC. In the first clock pulse, a "Reset" signal clears the output of the register, and the data start to load from the rising edge of the second clock pulse. The 16-bit control signal is delivered after 17 clock pulses with the

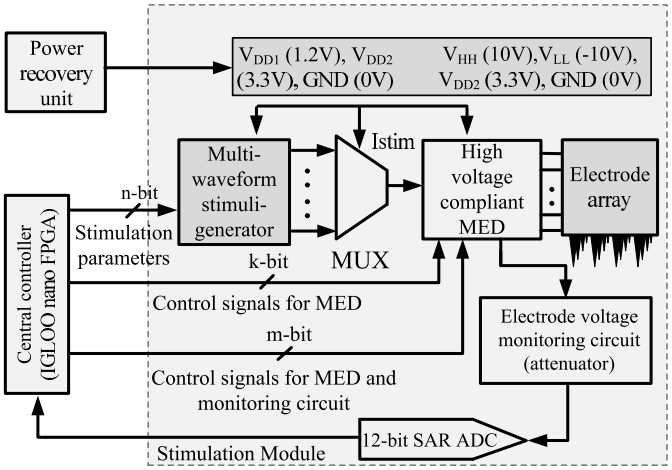


Fig. 7. Architecture of the proposed MSM along with its building blocks. Electrode array is not part of this design but connected to the MSM.

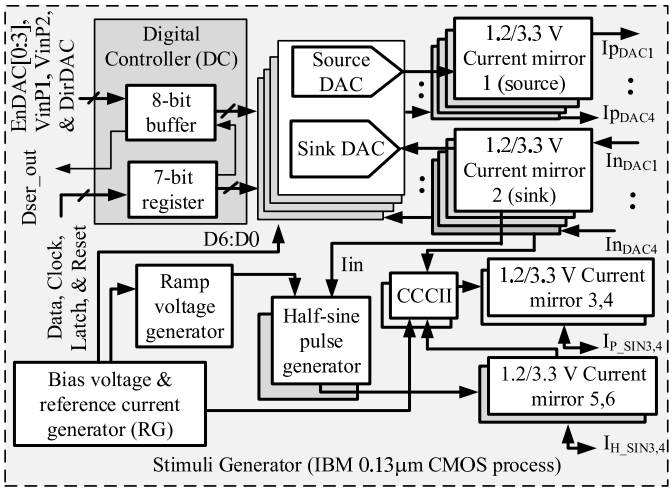


Fig. 8. Block diagram of the SG, implemented in 0.13-μm CMOS process.

rising edge of the "Load" signal. A 9 × 9 pin ball grid array and chip scale package IGLOO nano field-programmable gate array (FPGA) chip, supplied with 1.5 and 3.3 V, has been used to implement the central controller. The small area of 5 mm × 5 mm and an ultralow-profile pitch of 0.5 mm facilitate the miniaturization of the microstimulator.

C. Microstimulation Module

The proposed MSM, shown in Fig. 7, is a multichip (two microchips) interface between the central controller and the MEA. The MSM consists of an energy-efficient and multi-waveform SG, a high-voltage output-stage or microelectrode driver, an ETI voltage monitoring unit, and an analog-to-digital converter (ADC) to convert the monitored voltage into digital signal. The SG is implemented in IBM 0.13-μm 1.2-/3.3-V CMOS process [38], [39] to reduce power consumption in this current waveform generator. The high-impedance microelectrode array driver (MED) is realized in Teledyne DALSA 0.8-μm 5-/20-V CMOS/DMOS process to meet the required compliance voltage across the selected microelectrodes [27], [39]. The SG and MED are supplied with 1.2, 1.45, 3.3, and 0 V; and 3.3, ±10, and 0 V, respectively. Discrete components have been used to design the monitoring unit and the ADC. These functional blocks are as follows.

1) Stimuli Generator: The four-channel SG delivers energy-efficient pulse patterns (see Fig. 8) to the MEA through a high-impedance MED output stage. The SG consists of a digital controller (DC), a bias voltage and reference current generator (RG), a ramp voltage generator (RMPG), source and sink digital-to-analog converters (DACs), half-sine pulse generators (HSG), plateau-half-sine pulse generators (PSG), the second generation current conveyor (CCCII), and 1.2-/3.3-V current mirrors (CM1). More than three types of waveform: 1) constant current; 2) HS; 3) PS; and 4) mixed-type pulses are produced by this module. The SG is flexible to deliver biphasic stimulation using both source and sink currents. The included blocks are as follows.

a) Digital controller: This block receives DirDAC, V_{inP1}, V_{inP2}, EnDAC[0:3], Data, Clock, Latch, and Reset signals

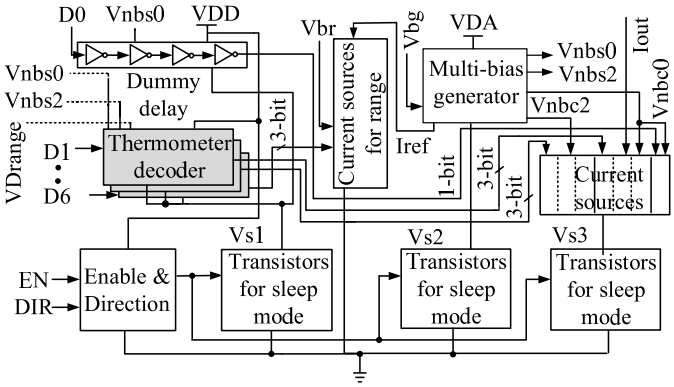


Fig. 9. Block diagram of the sink digital-to-analog converter included in four channels of the SG.

from the central controller to regulate the control parameters, such as stimulation current magnitude, direction of stimulation (anodic or cathodic), pulse-width, interpulse duration, and type of waveform. EnDAC[0:3] select the stimulation current channel, and DirDAC decides its phase. Data is applied serially to the 7-bit SIPO shift register. Signal dser_out is the internal serial data.

b) Current mode DAC: A low-area current-mode DAC, incorporated with mixed multibias [40] and thermometer-coded [41] techniques, is dedicated to supply constant current in each of four channels (see Fig. 9). Thermometer-coded topology has been selected to minimize the effects of process variation and switching glitches, and the multibias principle reduces the total area. Hence, this mixed topology allows area reduction without sacrificing the linearity of the DAC. The maximum stimulation current, allocated per source and sink DAC, is 220 μA to render two biphasic stimulations with 110 μA for each, per input channel. The resolution of each DAC is set to seven bits to meet the specified current limit [38], [39]. The EN and DIR signals select the channel and direction of the current (source or sink), respectively. Bits, D1–D6, are divided into three groups, D1–D2, D3–D4 and D5–D6, and thermometer decoded. This principle minimizes

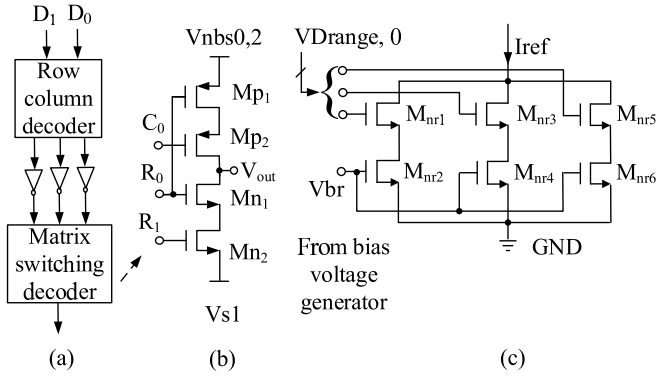


Fig. 10. (a) Block diagram of the thermometer decoder. (b) Modified circuit of the matrix switching decoder. (c) 2-bit DAC to set three ranges of I_{ref}.

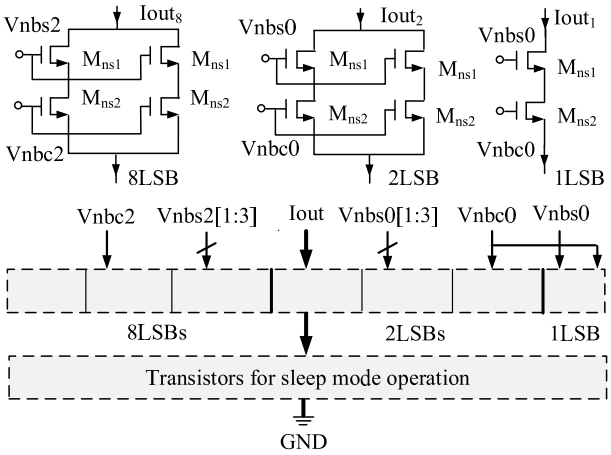


Fig. 11. Transistor-level representations and block diagram of 1-, 2-, and 8-LSB current sources of sink DAC.

the number of row-column decoder and the transistor count per decoder and, hence, the area of each DAC. An inverter chain, consists of four inverters, matches the delay of D0 to those of D1–D4. The DAC operates in three maximum full-scale currents, 73.67, 147.33, and 220 μA, which are set by three levels of I_{ref}. A 2-bit DAC, controlled by D5 and D6, establishes the value of I_{ref}, and D0–D4 determine the main DAC current. Transistors for the sleep mode operation are inserted between the respective analog and digital blocks, and supply ground to disable the DAC when microstimulation is not performed.

Fig. 10(a) shows the architecture of the thermometer decoder, used for switching the current sources in the DAC. The original matrix switching decoder, reported in [41], has been modified to a four-transistor model, which is presented in Fig. 10(b), as two additional transistors in the former have been found to be redundant in our segmented 2-bit thermometer decoder case. The 2-bit DAC, shown in Fig. 10(c), is controlled by a 2-bit thermometer decoder and sets three different values of I_{ref}, 19, 38, and 57 μA.

Fig. 11 shows 1-, 2-, and 8-LSB current sources of the DAC. Double cascode configuration has been selected to enhance the output impedance of current sources. Bias voltages Vnbc0,2 and Vnbs0,2 are generated from the multibias

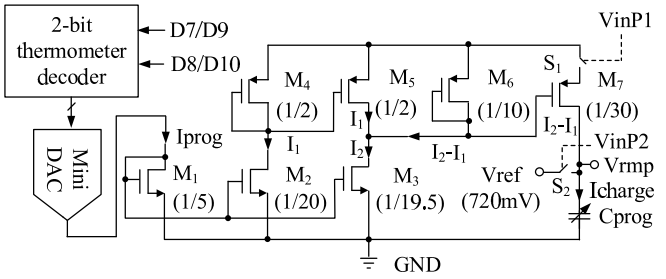


Fig. 12. Circuit for programmable RMPG to deliver increasing ramp voltage, required to set the durations of HS and PS pulses. Transistor dimensions are in μm.

generator. This DAC also determines the current magnitudes of HS, PS, and mixed-type pulses.

c) Half-sine pulse generator: MOS transistors in two differential pairs of a Gilbert cell are operated in the subthreshold region to generate an approximate HS pulse [42] following the equation:

$$\text{Ihsine} \propto \tanh\left(\frac{V_{\text{in}} - V_{\text{ref1}}}{2nV_T}\right) - \tanh\left(\frac{V_{\text{in}} - V_{\text{ref2}}}{2nV_T}\right) \quad (1)$$

where V_{in} is the ramp voltage input common to two differential pairs and ranges between 720 and 920 mV in our case, V_{ref1} and V_{ref2} are the fixed voltage levels, 720 and 920 mV, respectively, applied to the remaining inputs of the differential pairs, n is the slope factor, and V_T is the thermal voltage.

d) Ramp voltage generator: The width of the HS pulse, described previously, is determined by the slope of the ramp voltage (dV/dt). The charging property of a capacitor, according to $(dV/dt) = (I/C)$ relation, can serve to generate such increasing ramp voltage. Setting dV and C to 200 mV and 20 pF, respectively, the charging current required for pulse duration dt of 20 μs to 2 ms ranges from 2 to 200 nA. The circuit, demonstrated in Fig. 12, complies with this specification to generate nanoscale current, where the ramp is programmable by varying I_{prog} and output capacitor C_{prog}. Initially, C_{prog} is precharged to 720 mV closing the switch S_2, controlled by V_{inP2}. This voltage increases linearly to 920 mV, when V_{inP1} closes the switch S_1 and allows the nanoscale current I_{charge} to charge the capacitor. I_{charge} is generated by subtracting I_1 from I_2, both being the scaled versions of I_{prog}. In channels 3 and 4, two 20-pF capacitors are integrated, and additional capacitors can be added externally to modulate the pulse-width. A 2-bit thermometer-coded DAC, switched by D7 and D8 or D9 and D10, sets three different values of I_{prog}.

e) Plateau-sine pulse generator: A second generation current conveyor, configured as a current adder, linearly sums the scaled constant currents from DACs in channels 3 and 4 and the corresponding scaled HS pulses to generate PS pulses [38]. In fact, $\text{Ipsine}(t) = \text{Irect.}(t) + \text{Ihsine}(t - t1)$, where $t1 = 0$ results in the perfect PS pulse with a duration of T. However, shifting the relative position of $\text{Ihsine}(t - t1)$, where $-((3T)/4) \leq t1 \leq ((3T)/4)$, various waveforms can be generated and used in energy-optimum neural stimulation.

f) 1.2-/3.3-V current mirrors: These self-biased cascode current mirrors (CMs) enhance the compliance voltage [39]

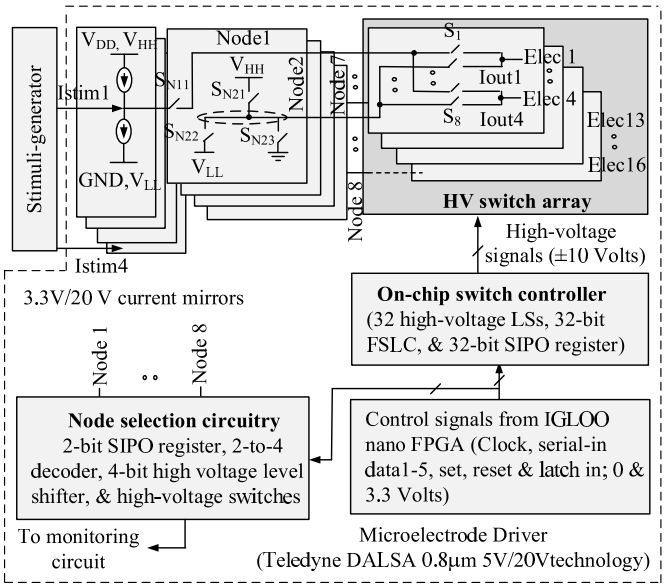


Fig. 13. Architecture of the proposed high-impedance MED. The 32-bit register and the FSLCs are implemented using low-voltage digital components. The other functional blocks are analog units.

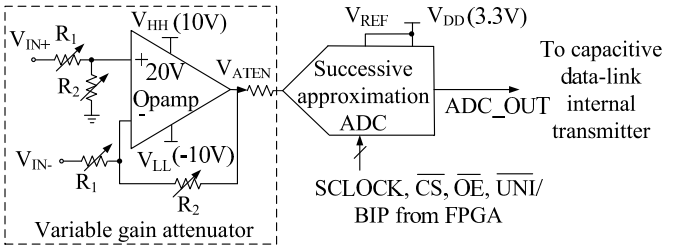


Fig. 14. Microelectrode–tissue interface voltage monitoring unit: variable gain attenuator followed by the 3.3-V SAR ADC.

and build interfaces between 1.2-V circuitries in the SG and 3.3-/20-V CMs in the MED.

2) Proposed Microelectrode Array Driver: The high-impedance MED, presented in Fig. 13, delivers microstimulation current to a high-impedance electrode array to meet the required compliance voltage across the microelectrode–tissue interface [38], [39]. This high-voltage output stage is designed and fabricated in Teledyne DALSA 0.8-μm 5-/20-V CMOS/DMOS technology to satisfy the required compliance voltage, which ranges from ± 10 to ± 13 V in our case. Detail descriptions of different designed circuits and characterization of the fabricated MED are presented in [27]. In this paper, we summarize its working principle and present additional experimental results, performed with the assembled MED and MEA.

A two-stage 3.3-/20-V cascode CM is incorporated in each of four input channels to supply up to 400-μA stimulation current and enhance the compliance voltage. Currents, Istim1 $-$ 4, from four input channels are distributed among 16-output channels, Iout1–Iout16; and injected into stimulation sites, Elec1–Elec16 through a switch matrix (SMX), composed of an array of 32 high-voltage switches. Thirty two high-voltage level shifters (LSs) provide ± 10–± 13 V (depending on high-voltage supplies, V_{HH} and V_{LL}) control signals to all high-voltage switches. An on-chip switch controller, consists of a 32-bit SIPO shift register and 32 forbidden state logic circuits (FSLCs), is included within the MED. This controller is the interface between the central controller of the microstimulator and 32 high-voltage LSs.

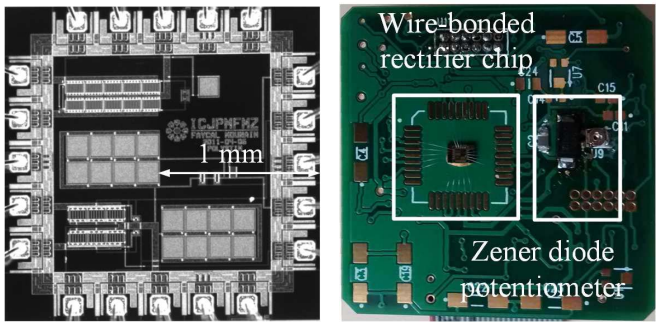
High-voltage switches $S_{N11} \ldots S_{N85}$, connected to Node1–Node8, are controlled by signals, applied directly from the central controller. Needless to mention that a high-voltage LS is inserted between each of these switches and the associated input chip pad. Two high-voltage supplies, V_{HH} (positive) and V_{LL} (negative), facilitate charge-balanced biphasic stimulation current preventing dc offset voltage across ETI impedance. This principle also avoids the use of bulky dc blocking capacitors [43]. All microelectrodes can be connected to the circuit ground (0 V) to discharge the charge, stored across the double-layer capacitances after microstimulation phase.

Node selection circuit establishes connection between two nodes from the same input channel, such as Node1 and Node2 in channel 1, and differential microelectrode voltage monitored circuit.

3) Monitoring Unit: Fig. 14 shows the schematic for the microelectrode–tissue interface voltage monitoring circuit. For stimulation current of about 100 μA through two microelectrodes, operating in bipolar configuration, peak electrode voltage reaches to ± 10 V. The input stage of the monitoring circuit is designed to sustain this high voltage. The 20-V operational amplifier is configured as a variable gain attenuator, where the attenuation factor is decided by the ratio of R_1 and R_2. This ratio is set to 1:6.67 to attenuate and bring the peak value of the monitored biphasic voltage within the conversion range of the successive approximation (SAR) ADC.

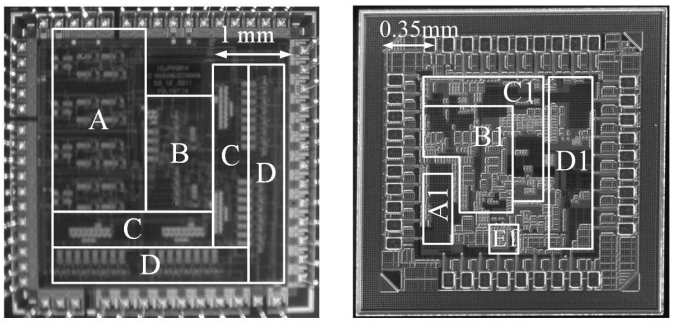
The 12-bit SAR ADC is supplied by 3.3 V, and the conversion rate can be up to 312.5 ksps with a clock frequency of 3 MHz. The reference voltage (V_{REF}) is set to 3.3 V to allow the maximum input voltage swing. The ADC is configured to digitize biphasic analog signal received from the attenuator. The converted bit stream is directed to the internal data transmitter of the capacitive link for monitoring purpose. Interestingly, an external current mode ADC can be connected to the same nodes (Node1–Node 8), where the monitoring unit is connected to, for harvesting stimulation currents from the output stages of 3.3-/20-V CMs or from electrodes before, during, or after stimulation. The validation of the stimulation current measurement is presented in Section III.

4) Charge Balancing Mechanism: The principle of charge balancing is to deliver and make sure equal amount of charge during anodic and cathodic phases of stimulation. We took a number of steps to design the: 1) SG; 2) interface CMs both in SG and MED; and 3) switching circuits in MED to ensure this. In SG, similar architecture and equal number of transistors in current sources were used to generate uniform currents from both source and sink DACs for a common digital input. The output impedances of 1.2-/3.3-V CMs in SG were matched to the input impedances of 3.3-/20-V CMs in MED. Common-centroid, multifingering, and dummy transistor techniques were used



(a) (b)

Fig. 15. (a) Microphotograph of the rectifier chip. (b) Assembled power recovery unit on miniature PCB: wire-bonded rectifier chip and discrete components.



(a) (b)

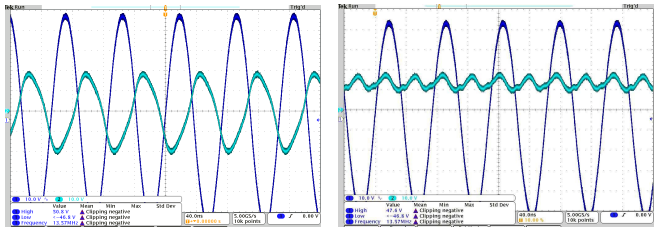
Fig. 16. Microphotograph of the fabricated microchips. (a) ICJPMSMX: A-CMs, high-voltage LSs, and switches; B-node selection circuitry; C-32-bit SIPO shift register; and D-32-bit LS and SMX. (b) ICGPMSTG: A1-DC; B1-DACs, and RG; C1-CM1s; D1-RMPGs, HSGs, CCCII, PSGs, and CM1s; and E1-20-pF capacitors and 2-bit DACs.

to prevent mismatch among the current sources in DACs and CMs while laying out the chips. In MED, positive and negative supply rails (+10 and −10 V) were used to perform biphasic stimulation around ground (0 V) and prevent dc level across microelectrodes. Voltage drop across six transistors in the current path from +10 to −10 V was made equal for any specific current during anodic and cathodic phases. All high-voltage switches were designed following the same architecture. In the worst case, only positive or negative current can be injected, and any residual charge across microelectrodes can be discharged to the ground.

III. Experimental Results

The microphotograph of the fabricated rectifier chip, the photograph of the assembled inductive-link-based front-end power recovery unit, and the microphotographs of the fabricated SG (ICGPMSTG) and microelectrode-driver (ICJPMSMX) chips are presented in Figs. 15 and 16, respectively. We present here the measurement results of the rectifier chip, when assembled to the power recovery unit, ICGPMSTG and ICJPMSMX chips, and the global microstimulator.

A six-layer and two-sided PCB of dimension 25 mm × 25 mm has been designed with different power planes



(a) (b)

Fig. 17. (a) Oscilloscope graphs of the transmitted and received RF signals at 13.56-MHz frequency. (b) Measurement results showing the transmitted signal and the output of the rectifier.

(0, 1.45, 1.5, 3.3, and ±10 V) in multiple layers. The Zener diode, dc–dc step-up converter, regulators, capacitors, and potentiometers are miniature commercial products with part numbers SMAZ20-13-F, MAX864, TPS763, F931D336KCC, 298D475X9010M-2T, TAJA105K035RNJ, PVZ2A104C04R00, and PVZ2A103-C04R00, respectively. For an input voltage of 5 V and 22.5-mA load current, the efficiency of MAX864 reaches 71%. The rectifier chip is wire bonded on top layer of the PCB, and the other surface mount components are soldered on both sides of it. The photograph of the assembled PCB is shown in Fig. 15(b). To validate the performance of this unit, we transmitted ac signal at 13.56 MHz from a custom built power transmitter [44]. Two four-turn inductive copper coils of 0.77 μH each were placed at about 6-mm distance with air medium between them. The LC tank circuit consisting of the receiver coil and a variable capacitor was tuned at 13.56 MHz to maximize the received power. The impedance of each coil at this frequency was 66 Ω. Fig. 17(a) shows the transmitted (100-V peak-to-peak) and received (38-V peak-to-peak) signals measured on an oscilloscope. The rectified filtered signal with some ripples and an average value of 12 V is presented in Fig. 17(b). It can support load current ranging from 1 to 13 mA for output voltage levels from 3.5 to 15 V. The maximum power efficiency reaches to 92% for load current of 6 mA. Placing the coils too close or too far (3 mm ≥ distance ≥ 10 mm) and misalignment between them deteriorate mutual inductance and coupling, causing the degradation of the recovered signal and, therefore, the power efficiency. The received power efficiency, when skin tissue is used as a medium, will undoubtedly be affected, which, however, has not been tested and verified in our case. The functionalities of the dc–dc step-up converter and regulators have also been verified, and they are able to generate the target voltage levels, which are 1.2, 1.45, 1.5, 3.3, and ±10 V.

The nominal voltages V_{DD}, V_{DA}, and V_{DD33} for the SG were set to 1.2, 1.2, and 3.3 V, respectively, during experimental validation. The measured dc and dynamic power consumptions of the SG chip are 1.92 and 0.64 mW, respectively. The applied clock frequency was 50 kHz. For characterizing this chip individually, control signals were applied from the Tektronix 714 logic analyzer and the IGLOO nano-FPGA board. The full-scale DAC current of 220 μA was obtained for V_{DA} of 1.45 V. Investigation shows that the reference generator cir-

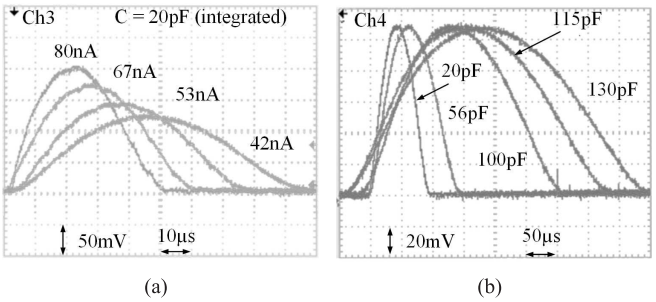


Fig. 18. Oscilloscope graphs of pulse-width variations of measured HS pulses (a) for multiple charging currents and (b) for various capacitances.

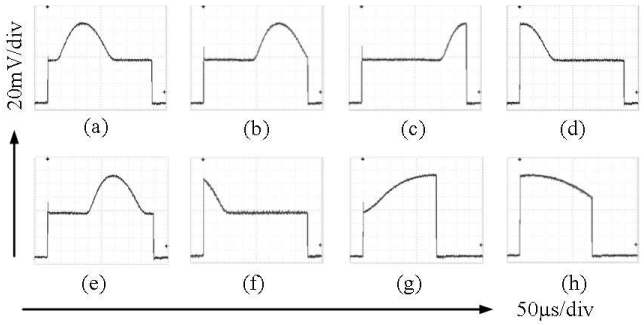


Fig. 19. Oscilloscope traces of the various forms of current signals, shown in (a)–(h), measured across 1-kΩ resistors, in Ch3 and Ch4 of the SG chip.

cuits are unable to provide the required voltages and currents, when V_{DA} is set to 1.2 V. The differential nonlinearity and integral nonlinearity errors of each DAC from the post-layout simulations are 0.29- and 0.75-LSB correspondingly.

Resistors of 1 kΩ each were used as loads while generating constant, HS, PS, and various waveforms from the SG. Pulse-widths were modulated varying the charging currents and capacitances in Ch3 and Ch4, respectively. External capacitors were connected in parallel with the integrated 20-pF capacitor/channel to obtain larger pulse-width of up to 500 ms. HS current (I_{HS}) was adjusted to 200, 175, 140, and 122 μA (approx.) in the first case, but kept constant at 110 μA in the second case. Fig. 18 shows the oscilloscope graphs of HS pulse-width variations, measured across 1-kΩ resistive loads for various charging currents and capacitances. Apart from the constant current, HS, and PS pulses, SG is also able to produce some other types of waveform, exhibited in Fig. 19(a)–(h), shifting the position and changing the pulse-width of the HS pulse relative to the rectangular (constant current) pulse. PS pulses in Ch3 and Ch4 were generated following the similar procedures as in the HS pulse case. The oscilloscope traces of the measured PS pulses, presented in Fig. 20(a), elucidate the pulse-width variations for several capacitances. The amplitude of each generated PS current pulse (I_{PS}), obtained across a 1-kΩ resistor, was 132 μA. Ideally, pulse-width variations with respect to different capacitances, according to $(dV/dt) = (I/C)$ equation, should be linear. Nonetheless, nonuniformity between 20-pF integrated and other external capacitors causes nonlinearity, which is visible both in Figs. 18(b) and 20(a). This pulse-width variation is quite uniform for all external capacitances.

The supply voltages (V_{DD}, V_{HH}, and V_{LL}) of the microelectrode driver chip, when characterized, were set to 3.3, +10, and −10 V, respectively. The average consumed quiescent power per chip for seven chips is 0.944 mW. For the clock frequency of 50 kHz, the dissipated dynamic power is 1.16 mW at no load. The linearity of the microelectrode driver was verified at the outputs of all 3.3-/20-V CMs (Node1, Node3, Node5, and Node7) and output channels (Iout1–Iout16). Linear stair source and sink current signals, with the ranges of 0–±400 μA and 0–±120 μA with increments of ±50 and ±20 μA in each step, respectively, were applied to Istim1–Istim4. Corresponding values of resistors, used in two cases, were 23 and 92 kΩ, respectively. Fig. 20(b) shows the oscilloscope traces,

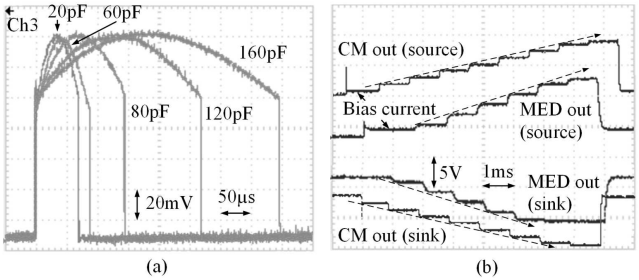


Fig. 20. (a) Pulse-width variations of the measured PS pulses in Ch3 of the SG for different capacitances. (b) Signals showing the linearity of the CM and at the output of the MED, illustrated in oscilloscope graphs.

when differential voltages were measured between Node1 and Node2 for the CM, and Iout1 and Iout2 for MED out. The output of the CM saturates beyond ±380μA, and stimulation current per output channel is unable to follow input current after ±110 μA for the specified load and compliance voltage limit (10 V). In the absence of input stimulation current, when switches are operated, a very small amount of bias current flow from V_{HH} to V_{LL} through the output load. This unwanted current builds up a dc offset as shown in Fig. 20(b).

HS and PS pulses and constant currents ranging from 11.6 to 120.64 μA were applied from the SG to four channels, Istim1–Istim4, to perform both monophasic and biphasic stimulations. Control signals were applied to switches, S_{N11}, S_{N22}, and S_1–S_4 in channel 1 while generating charge-balanced biphasic stimulation signals between Iout1 and Iout2. Each microelectrode was emulated by a resistor of 46 kΩ, and two of such a model were connected in series between these outputs. Similar steps were carried out from channel 2 to channel 4.

In Ch3, PS source current with a magnitude of ±120 μA and in Ch4, HS source current with an amplitude of ±110 μA were used for cathodic first and anodic first stimulations in succession. The generated waveforms across two 1-kΩ resistors for PS and HS current pulses from the SG are presented in the top of Fig. 21(a) and (b) successively. The respective measured waveforms across 92-kΩ (equivalent) impedance of resistive–capacitive (RC) and resistive (R) models, connected at the outputs of the MED, are shown in the bottom of Fig. 21(a) and (b).

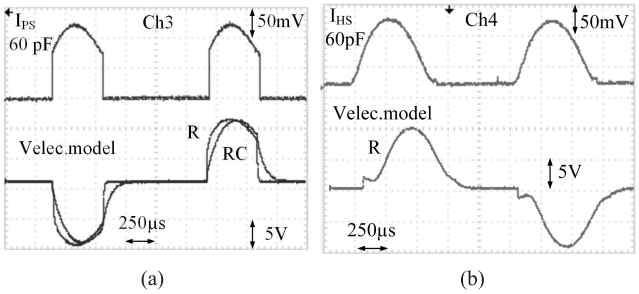


Fig. 21. Experimental results: generated waveforms due to (a) PS and (b) HS current pulses from the SG (top) and the corresponding stimulation signals at the output of the MED (a) and (b) (bottom).

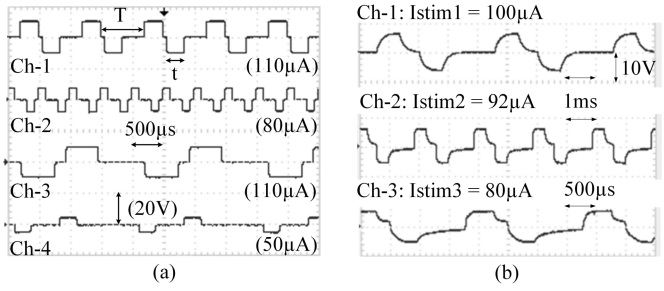


Fig. 22. (a) Measured stimulation signals in four output channels of the MED for resistive loads and different constant current levels. (b) *In vitro* experimental results obtained using Pt-coated MEA.

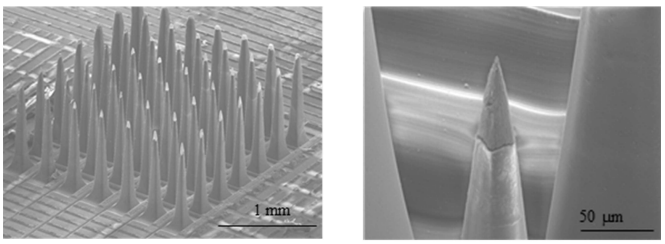


Fig. 23. SEM images of the MEA. (a) 3-D penetrating MEA. (b) Tips of the electrode sputter-deposited with Pt. The outermost electrodes are dummy to protect 5×5 inner electrodes.

Fig. 22(a) shows the oscilloscope traces of the measured differential voltages across the resistive loads of 92 kΩ, connected in four channels, for various input constant current amplitudes, pulse-widths, interpulse durations, and stimulation frequencies.

For performing *in vitro* tests, we have interfaced a novel 3-D MEA [17] with the proposed microstimulator. Fig. 23 shows the SEM images of the MEA. The high-density silicon-based MEA was designed and micromachined. Geometrical features of these MEAs provide more contacts between the electrodes and targeted neural tissues. To electrically isolate the electrodes, the polish side of the wafer was cut, filled with glass, and polished. To achieve 3-D structure, the other side of the substrate was cut with variable depths. As a result, we obtained 5×5 electrode array with 1.45-, 1.55-, and 1.65-mm heights. The electrodes in the outermost columns (1 and 7) and rows (1 and 7) with height 1.35 mm are

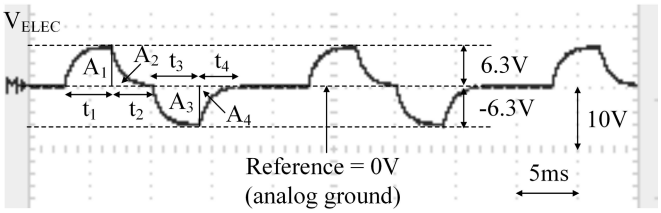


Fig. 24. Measured charge balanced biphasic stimulation signal across microelectrode for the calculation of delivered charge.

dummy to protect 5×5 inner electrodes. The thickness of the electrodes was 200 μm at the base and less than 2 μm at the tip with 100-μm spacing. The lateral surface area of the electrode tips was calculated to be about 1.6×10^{-5} cm^2 for a tip exposure (h) of 50 μm. To encapsulate and improve the biocompatibility of the electrodes, front side of the arrays was coated with Parylene-C. A new masking method was used to remove Parylene-C from the tips of electrodes. This method enhanced a uniform tip-exposure [17]. To facilitate the charge transfer from electrode to neural tissues, the active sites of the electrodes were sputter-deposited with thin film of platinum (Pt). Electrochemical impedance spectroscopy was performed using the Biostat VMP-300 electrochemical impedance system. The instrument was operated under the computer control with EC-Lab software. A solution of 0.9% phosphate buffer saline was used as the electrolyte in a three-electrode cell, which consists of a Ag/AgCl reference electrode and two others as counter and working electrodes. The average impedance of Pt-coated electrodes, measured at 1 kHz, was 70 kΩ.

Before carrying out microstimulation, the MEA was immersed in 0.15-M NaCl solution, poured in a basin with the diameter of 3.5 mm and a depth of 4 mm. Constant current was varied between 11.6 and 110 μA, and injected to different pairs of electrodes, connected in bipolar configuration in multiple sites. This investigation shows an average impedance of the microelectrodes of 65–70 kΩ. Fig. 22(b) demonstrates the *in vitro* test results, showing the variations of biphasic stimulation current, pulse-widths, interpulse durations, and stimulation frequencies in the output channels 1, 2, and 3 of the microstimulator. The effect of double-layer capacitances at the electrode–electrolyte interfaces is very prominent in the results.

In all cases, charge-balanced and biphasic stimulations were performed. Visual inspection shows that all biphasic waveforms presented till now are symmetric around the reference voltage 0 V. Indeed, in Fig. 24, we present the calculation to support our claim. The time constant for electrode $\tau = \mathrm{RC} = 4.138$ ms was calculated for an electrode impedance of $|70|\angle -68°$ kΩ [45]. Electrode voltage V_{ELEC} reaches ±6.3 V for applied stimulation current of ±92 μA. Charging and discharging times, (t_1 and t_3) and (t_2 and t_4), respectively, in anodic and cathodic phases were 3.8 and 3.2 ms. Following the equations of charging and discharging of an RC circuit, injected charge quantities for both phases, Q_{anodic} and Q_{cathodic}, were found to be 1.08 μC, which clearly indicates the charge balanced nature of this stimulation. In addition,

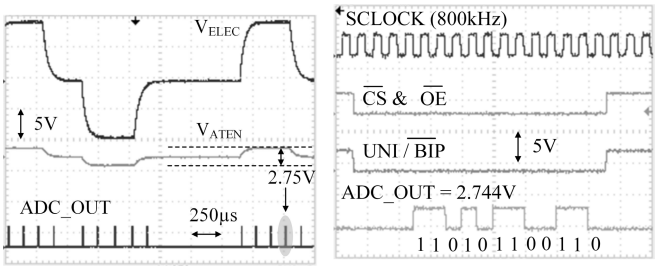


Fig. 25. Oscilloscope traces. (a) Biphasic stimulation signal in channel 1 output of the MED (top), attenuated signal (middle), and ADC output (bottom). (b) Control signals to the ADC and zoomed-in view of the resulting binary output.

V_{ELEC} decays to 0 V after every phase of stimulation and remains at this level, when no current is applied. This result also validates no need of blocking or coupling capacitor to prevent dc level. The achieved maximum compliance voltage across the loads was 10 V per phase or 20 V per anodic and cathodic phases. However, this compliance voltage rises to 20 V per phase when V_{HH} and V_{LL} are increased to ± 13 V.

Biphasic stimulation with a constant-current amplitude of 110 μA was performed to verify the functionality of the assembled monitoring unit. Two RC models of microelectrode, where $R = 46$ kΩ and $C = 1.2$ nF, were connected in series between Iout1 and Iout2 during the course of microstimulation in channel 1 of the MED. The chosen attenuation factor was 6.67. The ADC was operated at 800-kHz clock frequency. The digitized value of ADC output, which is 2.744 V, closely approximates the attenuated stimulation signal of 2.75 V. The measured stimulation signal at the output of the MED, attenuator output, and the signal converted by the ADC is presented in Fig. 25(a). The binary value of the ADC output (zoomed) and other control signals are shown in Fig. 25(b).

We have designed and fabricated three high-density interconnect PCB (PCB1–PCB3) for the assembly of different parts of the MSM and to interface with the newly fabricated MEA. PCB1, a four-layer PCB with the thickness of 0.8 mm, contains the wire-bonded SG chip die and the MUXs on its top side. The FPGA chip and the associated capacitors and resistors are soldered at the bottom side of this PCB. The MED chip die is wire bonded to the top side of PCB2, a two-layer PCB of thickness 0.5 mm. The surface mount components for the monitoring circuit are soldered at the bottom side of this PCB. The dimension of PCB1 and PCB2 is 44.45×44.45 mm^2 each. PCB1 and PCB2 are connected to each other by surface mount and ultralow profile Molex 20-pin connectors of 0.635-mm pitch. The end height of the stacked PCBs is 9 mm. Fig. 26(a)–(e) shows the different parts of the assembled MSM. PCB3, a two-layer PCB, has been used to interface with the MEA. A square-sized opening (hole) of 3.5 mm $\times$ 3.5 mm is created in the middle of this PCB to access the pads, located in the back side of the MEA. The MEA substrate is extended on four sides during microfabrication to support itself under PCB3. H20E epoxy has been used to attach the extended MEA substrate to the bottom side of PCB3; 24 rectangular pads, six pads on each side of the opening, are positioned

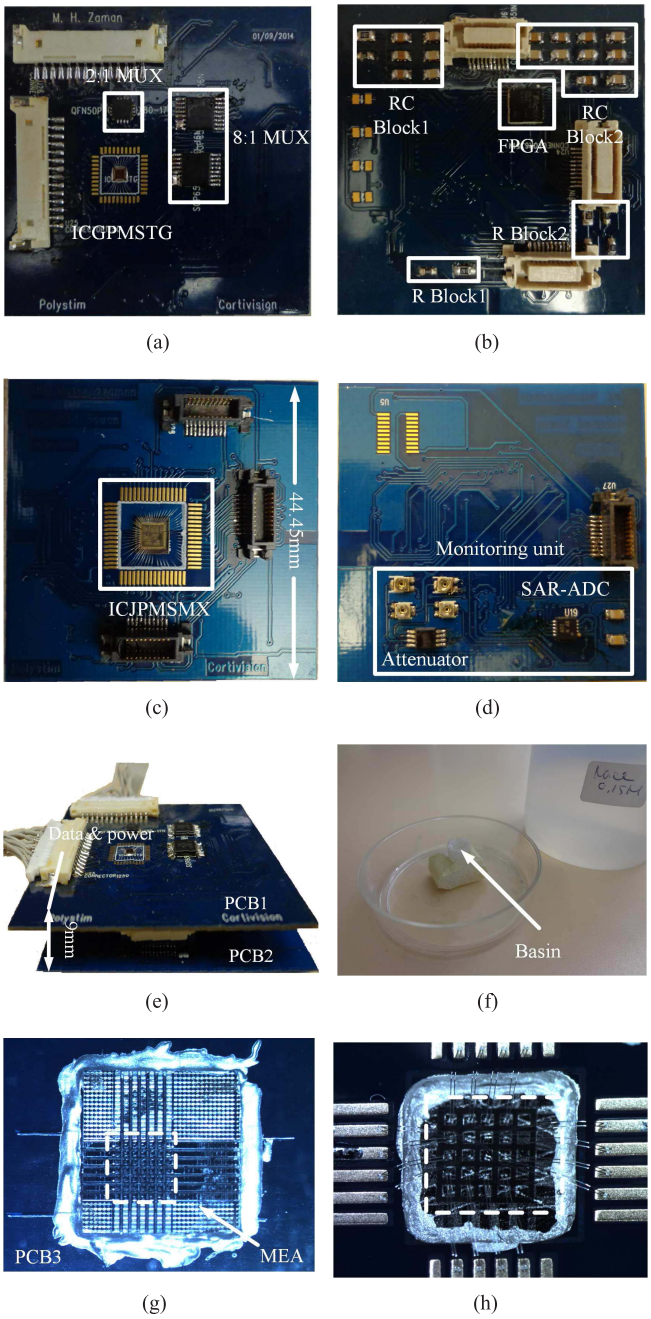


Fig. 26. Assembled microstimulator prototype. (a) Top view of PCB1. (b) Bottom side of PCB1. (c) Top side of PCB2. (d) Monitoring unit (the attenuator and ADC). (e) Vertically stacked PCBs. (f) Basin filled with 0.15-M NaCl solution for *in vitro* test. (g) MEA, glued underneath the opening in PCB3. (h) MEA pads, wire bonded to PCB3 pads.

to connect the MEA pads by wire bonding. However, only 16 microelectrode pads from the top-left corner are connected to the PCB pads for characterization. Compared with two other PCBs, the dimension of PCB3 is smaller to make it fit for the MEA. PCB2 is interfaced with PCB3 via a ribbon cable. The basin, filled with 0.15-M NaCl solution for *in vitro* tests and the assembled MEA are presented in Fig. 26(f)–(h).

Table I summarizes the specifications and the performance of this system. A comparison between our design and other microstimulators, reported in [9], [13], [20], [21], and [46], is presented in Tables II and III. The specific reason of anom-

TABLE I
SPECIFICATIONS AND PERFORMANCE RESULTS SUMMARY

Device	Microelectrode-driver (MED)	
Parameters	Post-layout sim. results	Experimental results
Technology	DALSA 0.8μm 5V/20V CMOS/DMOS	
V_{DD}, V_{HH}, V_{LL}, GND	3.3, 10, -10 and 0V	
No. of stimulation sites	16	
Die area	4x4mm^2	
Stim. ch. per MS module	4	
No. of stimulation channels	16 monopolar and 8 bipolar	
Electrode selectivity	Any	
Stim. current range per I/P	0 - 400μA	0 - 380μA
and O/P channel	0 - 100μA	0 - 100μA
Maximum load	100kΩ	92kΩ
Avg. DC power dissip.	12.44mW	0.944mW[a]
Dynamic power dissip.	-	1.16mW[b]
Compl. voltage (biphasic)	20V[c]	20V[c]
Device	**Stimuli-generator (SG)**	
Technology	IBM 0.13μm 1.2V/3.3V CMOS	
V_{DD}, V_{DA}, V_{DD33}, GND	1.2, 1.2, 3.3 and 0V	
Current waveform type	Rect., HS, PS, and others[d]	
Die area	1.75x1.75mm^2	
Avg. DC power dissip.	2.37mW	1.92[e] and 3.66mW[f]
Dynamic power dissip.	-	0.64[e] and 1.54mW[b,f]
DNL and INL	0.29 and 0.75LSB	-
Current per ch. (source/sink)	2.32 - 221μA[e,g]	$\leq$ 210μA[f,g]
Sub-system	**Data-communication link**	
Modulation-scheme and direction	SPPM (baseband), bi-directional	
Data-rate	10Mbps	
Sub-system	**Monitoring unit**	
Attenuation factor	-	6.67
ADC performance	-	12-bit, 312.5ksps

[a] Average value for seven chips, [b] f_{clock} = 50kHz, [c] This value increases to 20V/phase when V_{HH} and V_{LL} = $\pm$13V, [d] Fig. 19, [e,f] V_{DA} = 1.2 and 1.45V respectively, [g] Constant current only and the amplitude is 210μA for other waveforms.

TABLE II
PERFORMANCE COMPARISON

Parameters	This work	[9]	[21]
Technology	0.13 & 0.8μm	1.5μm	0.18 & 0.8μm
Compl. voltage (V)	20[a]	0.15 - 5,[b] 0 - 4.75[c]	13.7[a]
Stim. current (μA)	2.32 - 210	$\pm$270	1.6 - 167.2
Power dissip. (mW)	2.1,[d] 2.56[e]	8.25	54.91,[d] 0.12[e]
Area (mm^2)	4 X 4[d]	4.6 X 4.6	2.9 X 2.9[d]
	1.75 X 1.75[e]		1.01 X 1.01[e]
No. of channels	16	32	4
Load (kΩ)	70,[f] 92	45, 210[g]	100, 150
Data-communication	SPPM (cap.)	FSK (induc.)	No
Data-rate (Mbps)	3[h]	2.5	No
Power transmission carrier frequency	13.56MHz ISM[i]	5/10MHz[i]	No

[a] Combining anodic and cathodic phases,
[b,c] Source and sink correspondingly,
[d,e] Output-stages and stimuli-generators respectively, [f] Platinum coated microelectrode, [g] Iridium/Iridium-oxide coated microelectrode,
[h] Discrete approach [i] Carrier frequency.

aly of power consumption between postlayout simulation and measurement results of MED (12.44 and 0.944 mW), although investigated thoroughly, is quite unknown to us. The MSM in our developed microstimulator consumes 4.66-mW quiescent power, which is much lower compared with the system in [21]. The latter design includes an on-chip high-voltage dc–dc converter, which consumes high power and causes it to exceed the minimum allowable static power dissipation limit for an implantable biomedical device. The system in [46] is limited to four channels only, and therefore, low power consumption compared with our case is reasonable. The microstimulator in [20] consumes low power, as their design is implemented in a single chip using one CMOS technology. Moreover, it is not integrated with the high-voltage output stage to deliver the required high-voltage across the high-impedance of ETI. To the best of our knowledge, the achieved compliance voltage of this microstimulator is the highest among the reported custom integrated microstimulators. This compliance voltage increases up to 20 V per phase, when the high-voltage supplies (V_{HH} and V_{LL}) in the output stage MED are increased to $\pm$13 V. These supply levels do not affect the reliability in DALSA 0.8-μm CMOS/lateral current DMOS (LDMOS) process or cause the chip to malfunction, as each 20-V transistor is able to withstand the nominal voltage (20 V) across it. The stimulation current level, although not maximum compared with the other designs, is yet sufficient to meet our demand.

TABLE III
PERFORMANCE COMPARISON

Parameters	[46]	[13]	[20]
Technology	0.35μm	0.18μm	3.0μm
Compl. voltage (V)	20	VDD–0.5	< 10
Stim. current (μA)	1000	64	127
Power dissip. (mW)	1.16	N/A	0.78
Area (mm^2)	0.2[j]	4.0	22.8
No. of channels	4	16	64
Load (kΩ)	1, 10	71.4, 78.5	N/A
Data-communication	IR data link	FSK	
Data-rate (Mbps)	2[k]	1.2[l]	N/A
Power transmission carrier frequency	13.56MHz ISM	4.8	N/A

[j] Per four output channels, [k] Optical coupling,
[l] Inductive coupling

Moreover, we have considered energy efficiency of the stimulation waveforms. Although power is supplied externally, yet, energy efficiency plays a crucial role to reduce heat dissipation within the device enabling its long life for chronic implantation and to prevent tissue damage and corrosion of electrodes that may arise owing to heat generation during electrochemical reaction. Exponential pulse has not been implemented in our case, as investigation shows that it is not energy optimum [28], [30], [31]. The new types of stimulation current waveform, in addition to the constant, HS, and PS current pulses, facilitate exploring their efficiencies in exciting neural tissues and energy saving capabilities. Considering 3.66-mW power consumption of the SG, when V_{DA} is increased to 1.45 V, power dissipation per channel is $3.66/4 = 915$ μW. HSG and PSG consume about 140 μW power per channel, which is $(140/915) \times 100$ or 15.3% of total power consumed under no-load condition. On the other hand, these two waveforms

save 36% and 19% of the energy, respectively, compared with the rectangular pulse, when the total areas under the curves are calculated. According to Robillard *et al.* [47] HS pulse is able to save up to 44.8% energy. Therefore, taking the additional power consumption to generate these waveforms into account, 3.7–29.5% energy saving is possible, which, however, can vary depending on the design of circuits. Thus, a high data rate compatible SG, capable to stimulate hundreds of neural sites and implemented with these waveforms, can be a very effective solution to a low-power implantable stimulator. However, the total area, in our case, is greater compared with those in [9] and [46], owing to two different technologies used and the electrode voltage monitoring feature, and that in [21] due to the increased number of channels. Besides, this system has been assembled with a novel pyramidal-shaped MEA, and the functionality of the complete system has been validated through *in vitro* tests. The wireless power budget has been limited to 50 mW to satisfy the standard of biomedical devices.

However, the disadvantages of the power recovery unit are: 1) the unwanted power dissipation by the potentiometer after the Zener diode; 2) the use of commercial dc–dc converters and capacitors; and 3) power needed by the internal data transceiver was not considered. In addition, a power management unit to control power for the micostimulator, the central controller, and the data receiver is required. Therefore, considering all these cases, optimization of the architecture is needed. Concerning integration of the power recover unit, approaches mentioned in [21], [36], and [37] can be followed. A custom chip, which would include the presented bridge rectifier; 20-V voltage limiter; two adjustable series regulators to generate 5–10 V from 20 V; one Pelliconi charge pump-based dc–dc converter to generate -10 V from $+10$ V; and five LDO regulators to generate 1.2 (V_{DD}), 1.2 (V_{DA}), 1.45, 1.5, and 3.3 V from 5 V, can be designed in Austria Mikro Systeme (AMS) 0.35-μm CMOS/DMOS process along with some off-chip ultra-miniaturized capacitors. The estimated total silicon area can be between 6 and 9 mm^2. The SG, MED, ADC, central controller, and ETI voltage monitoring unit can be combined into a single custom chip with an estimated chip area of 9 mm^2 and designed in AMS 0.35-μm CMOS/DMOS process.

In the end, the effectiveness and possibilities of tissue damages resulted by chronic application must be addressed. Our target layer of stimulation is the IV-C of primary visual cortex. The average deepest level of this layer from top cortical side is around 1.55 mm. The heights of our designed microelectrodes comply with this depth. The 100-μA biphasic current is a maximum current level, but the expected needed current is much less, as low as 10 μA, and then, one has to consider the charge density, not only the current intensity. This charge density (d) is the ratio of charge quantity (Q) over the single microelectrode exposed tip area (S), which means $d = Q/S$ (where $Q = IT$, T is the pulse duration, and I is the stimulation current intensity). For I between 10 and 100 μA, T of 200 μs, and S of 1.6×10^{-5} cm^2, d varies between 0.125 and 1.25 mC/cm^2, which is very safe and far below the standard values causing minimum damage to tissue for chronic implantation, when charge balanced biphasic stimulation is performed. The charge density can be increased by altering the values of I and T.

IV. Conclusion

We have presented a new highly integrated electrical stimulator, dedicated for visual intracortical microstimulation. To this end, we made several ICs for the microstimulation subsystem and the power recovery unit. The corresponding experimental results validating their functionalities have also been presented. The assembly of the various parts along with the MEA, which poses the most challenges, is detailed here with successful *in vitro* experimentation. Although the microstimulator is built using several custom designed integrated chips, a commercial FPGA chip, and some other discrete components, yet, it shows the possibility of full integration. The proposed architecture is configurable for all types of microstimulations and featured with various types of energy-efficient waveforms. The MSM is modular in architecture and can be duplicated to maximize the stimulation sites. However, the end size of the integrated MSM has been retained to be large because of the functional verification purpose.

Because of higher compliance-voltage capability, the device can drive microelectrodes with an impedance of up to 200 kΩ, when stimulated with 100 μA. The reduced full-scale DAC current, when the low-voltage analog parts in the SG is supplied with 1.2 V, can be corrected by adjusting the dimensions of some transistors in the bias voltage and reference current generator (RG) circuits. As for full integration and miniaturization, all blocks of the MSM can be designed in a single chip and integrated to the MEA via flip-chip bonding, followed by the encapsulation of the complete MSM.

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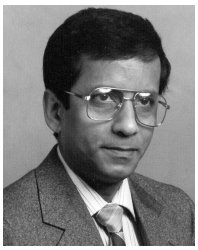

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