| | |
|---|---|
| **Titre:** Title: | Circuits Techniques for Wireless Sensing Systems in High-Temperature Environments |
| **Auteur:** Author: | Ahmad Hassan |
| **Date:** | 2019 |
| **Type:** | Mémoire ou thèse / Dissertation or Thesis |
| **Référence:** Citation: | Hassan, A. (2019). Circuits Techniques for Wireless Sensing Systems in High-Temperature Environments [Thèse de doctorat, Polytechnique Montréal]. PolyPublie. https://publications.polymtl.ca/3895/ |



| | |
|---|---|
| **URL de PolyPublie:** PolyPublie URL: | https://publications.polymtl.ca/3895/ |
| **Directeurs de recherche:** Advisors: | Mohamad Sawan, & Yvon Savaria |
| **Programme:** Program: | génie électrique |

**POLYTECHNIQUE MONTRÉAL**

affiliée à l'Université de Montréal

# Circuits techniques for wireless sensing systems in high-temperature environments

**AHMAD HASSAN**

Département de génie électrique

Thèse présentée en vue de l'obtention du diplôme de *Philosophiae Doctor*

Génie électrique

Avril 2019

**POLYTECHNIQUE MONTRÉAL**

affiliée à l'Université de Montréal

Cette thèse intitulée:

# Circuits techniques for wireless sensing systems in high-temperature environments

présentée par **Ahmad HASSAN**

en vue de l'obtention du diplôme de *Philosophiae Doctor*

a été dûment acceptée par le jury d'examen constitué de :

**Yves AUDET**, président

**Mohamad SAWAN**, membre et directeur de recherche

**Yvon SAVARIA**, membre et codirecteur de recherche

**François LEDUC-PRIMEAU**, membre

**Slim BOUMAIZA**, membre externe

# DEDICATION

*To my beloved parents*

*To my dear wife*

*To my daughter and son*

*To my sister and brothers*

*To my dear friends.*

# ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to my supervisor professor Mohamad Sawan for giving me the opportunity to pursue my Ph.D. program under his supervision, mentoring and helping me in research throughout my journey to achieve my goal. I would also like to express my gratitude to him for his great availability, for the financial and scientific support I received from him. He was not only a research supervisor but also a life mentor who has influenced a lot of decisions shaping my future career. My heartfelt gratitude also goes to my co-supervisor professor Yvon Savaria for his counsel and help in my endeavor.

My sincere thanks and gratitude also go to the jury members namely Prof. Yves Audet, Prof. Francois Leduc-Primeau and Prof. Slim Boumaiza for agreeing to be members of the examination board of my Ph.D. thesis.

I also would like to acknowledge the financial support from the National Science and Engineering Research Council (NSERC). Also, my thanks go for CMC Microsystems and Canadian National Research Council (NRC) for supporting me with their design tools and manufacturing facilities.

I would also like to thank everyone in the Polystim Neurotech Laboratory. I would specially thank our great technician Laurent Mouden for his technical help in the packaging and assembly of my developed chips.

Special thanks to my uncle Dr. Nasser Taleb and my cousin Dr. Ahmad Taleb who inspired me long time ago to pursue my studies in Canada and helped me to achieve that.

I am also grateful to my friends who have supported me from the beginning and along the way especially Monzer Hallak, Bilal Yassin, Mohamad Jarrah, Tarek Radieddine, Yahya El Meraabi, my English teacher Bilal Aldik at Al Iman School and Ms. Sereen Hariri the executive administrator at Beirut Arab University

I would like to express my deepest gratitude to my parents who have provided me through moral and emotional support in my life.

Finally, I am grateful to my wife for her support and encouragement in my higher education and my life. She has endured a lot from my research. Without her priceless support I could not accomplish my research and study.

# RÉSUMÉ

Dans ce projet, nous proposons de nouvelles techniques d'intégration basées sur la technologie de nitrure de gallium (GaN). Ces techniques permettent de mettre en œuvre un système de transmission de données sans fil entièrement intégré dédié aux capteurs de surveillance pour des applications d'environnement hostile. Le travail nécessite de trouver une technologie capable de résister à l'environnement sévère, principalement à haute température, et de permettre un niveau d'intégration élevé. Le système réalisé serait le premier dispositif de transmission de données basé sur la technologie GaN. En plus de supporter les conditions de haute température (HT) dépassant 600 $^{o}$C, le système de transmission sans fil attendu devrait fonctionner à travers une barrière métallique séparant le module émetteur du récepteur.

Une revue de la littérature sur les applications en environnements hostiles ainsi que sur l'électronique correspondante a été réalisée pour sélectionner la technologie AlGaN/GaN HEMT (transistor à haute mobilité d'électrons) comme une technologie appropriée. Le kit de conception GaN500, fourni par le Conseil national de recherches du Canada (CNRC), a été adopté pour concevoir et mettre en œuvre le système proposé. Cette technologie a été initialement introduite pour desservir les applications radiofréquences (RF) et micro-ondes. Par conséquent, elle n'avait pas été validée pour concevoir et fabriquer des circuits intégrés analogiques et numériques complexes et son utilisation à des températures extrêmes n'était pas validée.

Nous avons donc caractérisé à haute température des dispositifs fabriqués en GaN500 et des éléments passifs intégrés correspondants ont été réalisés. Ces composants ont été testés sur la plage de température comprise entre 25 et 600 $^{o}$C dans cette thèse. Les résultats de caractérisation ont été utilisés pour extraire les modèles HT des HEMT intégrés et des éléments passifs à utiliser dans les simulations. En outre, plusieurs composants intégrés basés sur la technologie GaN500, notamment des NOT, NOR, NAND, XOR, XNOR, registres, éléments de délais et oscillateurs ont été mis en œuvre et testés en HT. Des circuits analogiques à base de GaN500, comprenant un amplificateur de tension, un comparateur, un redresseur simple alternance, un redresseur double alternance, une pompe de charge et une référence de tension ont également été mis en œuvre et testés en HT.

Le système de transmission de données mis en œuvre se compose d'un module de modulation situé dans la partie émettrice et d'un module de démodulation situé dans la partie réceptrice. Le modulateur proposé est basé sur la technique de modulation Delta-Sigma et il est composé d'un

amplificateur, d’un comparateur, d’un registre, d’une pompe de charge et d'un oscillateur en anneau. L'étage de sortie de l'émetteur est conçu pour effectuer la modulation de «Load-Shift-Keying (LSK)» requise pour assurer la transmission de données par la liaison inductive dédiée. Au niveau du récepteur, trois topologies de démodulation ont été proposées pour acquérir les signaux modulés en LSK. Le premier démodulateur est destiné à la transmission de données à haute fréquence (plage des MHz) et basé sur des circuits entièrement numériques (inverseurs, registres, circuits à retard). Les deuxième et troisième démodulateurs sont orientés vers la transmission de données à basse fréquence (plage des kHz) qui sont basées sur la technique de rectification. Le deuxième démodulateur comprend un bloc redresseur simple alternance, un comparateur et des inverseurs. Le troisième démodulateur est comme le second, mais il est basé sur un redresseur double alternance.

Deux puces ont été fabriquées et testées, 4 articles de conférence et 5 articles de revues ont été publiés ou soumis pour diffuser les contributions de cette thèse

# ABSTRACT

In this project, we propose new integrated-circuit design techniques based on the Gallium Nitride (GaN) technology to implement a fully-integrated data transmission system dedicated to wireless sensing in harsh environment applications. The goal in this thesis is to find a proper technology able to withstand harsh-environments (HEs), mainly characterized by high temperatures, and to allow a high-integration level. The reported design is the first data transmission system based on GaN technology. In addition to high temperature (HT) environment exceeding 600 $^{o}$C, the expected wireless transmission systems may need to operate through metallic barriers separating the transmitting from the receiving modules.

A wide literature review on the HE applications and corresponding electronics has been done to select the AlGaN/GaN HEMT (high-electron-mobility transistor) technology. The GaN500 design kit, provided by National Research Council of Canada (NRC), was adopted to design and implement the proposed system. This technology was initially provided to serve radio frequency (RF) and microwave circuits and applications. Consequently, it was not validated to implement complex integrated systems and to withstand extreme temperatures. Therefore, the high-temperature characterization of fabricated GaN500 devices and corresponding integrated passive elements was performed over the temperature range 25-600 $^{o}$C in this thesis. The characterization results were used to extract HT models of the integrated HEMTs and passive elements to be used in simulations. Also, several GaN500-based digital circuits including NOT, NOR, NAND, XOR, XNOR, register, Delay and Ring oscillator were implemented and tested at HT. GaN500-based Analog circuits including front-end amplifier, comparator, half-bridge rectifier, full-bridge rectifier, charge pump and voltage reference were implemented and tested at HT as well.

The implemented data transmission system consists of a modulation module located in the transmitting part and a demodulation block located in the receiving part. The proposed modulation system is based on the delta-sigma modulation technique and composed of a front-end amplifier, a comparator, a register, a charge pump and a ring oscillator. The output stage of the transmitter is intended to perform the load-shift-keying (LSK) modulation required to accomplish the data transmission through the dedicated inductive link. At the receiver level, three demodulation topologies were proposed to acquire the delivered LSK-modulated signals. The first demodulator is intended for high-frequency data transmission (MHz range) and based on fully digital basic

blocks (inverters, register, and delay circuits). The second and third demodulators are oriented towards low-frequency data transmission (kHz range) which are based on rectification techniques. The second demodulator includes a half-bridge rectifier block, a comparator and inverters. The third demodulator is like the second one, but it is based on full-bridge rectifier.

Two chips were fabricated and tested, 4-conference papers and 5-journal manuscripts were published or submitted to disseminate the contributions of this thesis.

# TABLE OF CONTENTS

# LIST OF TABLES

# LIST OF FIGURES

# LIST OF SYMBOLS AND ABBREVIATIONS

| | |
|---|---|
| AC | Alternating current |
| ADC | Analog-to-digital converter |
| ADS | Keysight Advanced Design System |
| ALD | Atomic layer deposition |
| BEN | Bias enhanced nucleation |
| BiCMOS | Bipolar-CMOS |
| BJT | Bipolar junction transistor |
| CMOS | Complementary metal-oxide-semiconductor |
| COB | Chip on board |
| CPFC | Canadian Photonics Fabrication Center |
| CTE | Coefficient of thermal expansion |
| DAC | Digital-to-analog converter |
| DBC | Direct bond coper |
| DC | Direct current |
| DD | Displacement damage |
| 2DEG | Two-Dimensional Electron Gas |
| DIBL | drain induced barrier lowering |
| DIL | Dual in-line package |
| DHBT | Double Heterojunction Bipolar Transistor |
| $E_G$ | Energy bandgap |
| FBR | Full bridge rectifier |
| $f_c$ | Carrier frequency |
| $f_T$ | Cutoff frequency |

| | |
|---|---|
| GaAs | Gallium Arsenide |
| GaN | Gallium Nitride |
| gm | Transconductance |
| HBR | Half bridge rectifier |
| HFET | Heterostructure Field Effect Transistor |
| HEMT | High Electron Mobility Transistor |
| HT | High-temperature |
| HTCC | High temperature co-fired ceramic |
| HVPE | Hybrid vapor phase epitaxy |
| HBT | Heterojunction Bipolar Transistor |
| IC | Integrated circuit |
| IGFET | Insulated-Gate Field Effect Transistor |
| IMD | Implantable medical devices |
| IPT | Inductive power transfer |
| JFET | Junction filed effect transistor |
| LSK | Load Shift Keying |
| LTCC | Low temperature co-fired ceramic |
| MBE | Molecular beam epitaxy |
| MESFET | Metal semiconductor field effect transistor |
| MIM | Metal-Insulator-Metal |
| MOCVD | Metal-organic chemical vapor deposition |
| MOSFET | Metal oxide semiconductor field effect transistor |
| MOSHEMT | Metal-oxide-semiconductor high electron mobility transistor |
| MMIC | Monolithic Microwave Integrated Circuit |

| | |
|---|---|
| $N_c$ | Effective electron density |
| NCD | Nanocrystalline diamond |
| ni | Intrinsic carrier concentration |
| NRC | Canadian National Research Council |
| $N_v$ | Effective hole density |
| PCB | Printed circuit board |
| Q | Quality factor |
| RF | Radio frequency |
| RFID | Radio-frequency identification |
| RIE ECR | Reactive ion etching with electron cyclotron resonance |
| RT | Room temperature |
| RTD | Resistive temperature detector |
| SEE | Single event effects |
| Si | Silicon |
| SiC | Silicon Carbide |
| SiGe | Silicon Germanium |
| SOI | Silicon on Insulator |
| TC | Transient coefficient |
| TCR | Temperature coefficient or resistance |
| TLP | Transient liquid phase |
| TID | Total ionising dose |
| WBG | Wide bandgap |

# LIST OF APPENDICES

# CHAPTER 1 INTRODUCTION

## 1.1 Motivation: wireless sensors in high-temperature applications

Several manufacturing industries, such as aerospace and aircraft engines, geothermal or oil and gas exploration need to measure physical properties under extreme temperature environment in real-time. These measurands may be pressure, temperature, strain, flame speed, acceleration, etc [1, 2]. In many cases, sensors placed in harsh environment are frequently isolated from their control or power management unit, which is usually located outside the harsh zone [3]. Commonly, these entities are interconnected with regular wires. However, drilling holes through the separation medium which is mostly metallic is not always an acceptable solution given the potential risk of toxic chemicals leakage, pressure or vacuum loss, and mechanical structure integrity weakening. In addition, these wired connections present many challenges for preserving system light weight, simplicity and low-cost system implementation. Therefore, a wireless power transfer and data exchange through metallic barrier without any physical penetration is in urgent demand for the harsh environment sensing field. However, few hundred degrees suffice for ruining the operation of a circuit. In fact, when the environmental temperature exceeds the conventional limit (higher than 125 ºC), traditional electronics are no longer able to fit their requirements. Unfortunately, this limitation in the conventional technologies negatively impacts the proliferation of many domains and industries.

One of the proposed solutions to reduce the heating impact on electronics is to provide cooling systems. However, this additional thermal management solution introduces complexity and supplementary hardware. It adds wires, connectors, cooling tubing, special intakes, etc. Also, it increases overall weight and size which is not always acceptable or even feasible. Especially in critical applications such as aerospace where size, weight, and reliability should be optimized for achieving the required performance and lower the risks. Furthermore, the actual aerospace technological development does not leave much space for additional secondary systems. In fact, the number of installed sensors and microelectronic subsystems that control and monitor the critical parameters in vital high-temperature regions are intended to be increased in near future. Moreover, potential efforts are exerted to replace all hydraulic actuators and mechanical driven systems by electrical and electronic versions. These implemented electrical and electronic systems lower the

engine size and weight and require less maintenance compared to pumps, fluids, and vacuum piping. However, their wiring and connectors are exposed to harsh environment which is the principal cause of inspection and preventive maintenance on aircraft jet engines. Aiming to reduce wiring and corresponding accessories which adversely affect the system reliability, adopting a distributed electronic system architecture is an accepted approach in aircraft and automobiles applications. Still, having many wires is undesirable as they require shielding, routing, maintenance, additional size and weight. Consequently, the aerospace industry's long-term vision pursues complete wireless control systems that can even harvest their required power from the surrounding extreme temperature. Achieving this vision would be a revolution in high-temperature applications giving birth to more reliable systems requiring no electrical wires. This would reduce space missions' cost (1 kg of payload sent to space costs $20 000 US), extend deep-well drilling machine range (operational deep-drilling machines may reach 20,000 feet depth) and optimize weight, maintenance cost and fuel consumption in passenger aircrafts and automobiles. Therefore, the high-temperature electronics market is considered nowadays a niche market technology that can strongly affect the modern industrial fields.

For those reasons, worldwide influential aerospace industries like Safran Group, Airbus Defence & Space, etc. are seeking alternative microelectronic technologies developed to 1) sustain exceptional environmental conditions, 2) be installed in critical sensitive areas, 3) be implemented as microdevices, and 4) communicate wirelessly even through metal. Developing electronics tolerating such harsh environment while providing wireless communication would have a great economic impact on the extreme electronics market. The related high-temperature electronics market is still modest in commercial value compared to the worldwide market of conventional semiconductor technologies.

## 1.2 Wireless through metal

Several wireless solutions in ambient environment are proposed in the literature for through-metal-wall power and/or data transmission such as the RFID [4], the inductive coupling [5, 6], acoustic/ultrasound coupling [7], and capacitive coupling [8]. Capacitive couplings have very low power transfer efficiency, which makes them unsuitable for power delivery through metal walls. In an ultrasonic coupling, ultrasonic waves can propagate easily through various kinds of metals and allow both high-power transfer efficiency and high-data rates. However, exposition to extreme

high temperatures may alter the piezoelectric properties and consequently damage the functionality of ultrasonic transducers. On the other hand, inductive couplings can operate at temperatures far-exceeding the Curie point of piezoelectric materials and do not need a direct coupling with metal walls to provide a good transmission path, unlike piezoelectric transducers [3]. Using an inductive link allows power and data transfer without compromising the integrity of the physical structure. However, transferring AC magnetic fields through metallic medium presents few challenges to overcome. Due to the Faraday shielding and skin effects in metal, magnetic waves cannot effectively pass through metallic barriers, particularly those that have high electrical conductivity and magnetic permeability.

Nevertheless, systems relying on Inductive Power Transfer (IPT) has evolved in the last 20 years into a $1 billion industry [9]. Currently, the wireless energy transfer market is very dynamic. A wide range of products such as mobile phones in the lead, electric vehicles, robots, drones, and Implantable Medical Devices (IMD) use this technology.

## 1.3 GaN high-temperature technology

Silicon on insulator (SOI), gallium arsenide (GaAs) and silicon germanium (SiGe) are commercially available semiconductor technologies dedicated for high-temperature applications. However, they are serving a narrow range of temperatures not exceeding 300 $^{o}$C, and are often associated with limited operation time, due to fundamental physical limitations of these semiconductors at high temperature [10]. Many significant industrial applications have requirements far exceeding this limit. For example, in turbine engines, many sensors and electrical actuators should be located in 600 $^{o}$C ambient temperature. Similarly, in aerospace exploration, in addition to the extreme radiation environment that electronic must endure, the ambient temperature can exceed 500 $^{o}$C. This is the case for Venus and Mercury exploration. Moreover, in geothermal and automotive applications, telemetry devices and exhaust pipe sensors must sustain ambient temperatures above 500 $^{o}$C.

Wide bandgap (WBG) semiconductors are considered as main candidates in the foreseeable future to overcome the fundamental limits of available conventional electronics in high ambient temperature applications. Silicon carbide (SiC) and gallium nitride (GaN) are the best-known WBG devices offering attractive features suitable for high temperature conditions such as wide bandgap

(3 eV), high drift saturation velocity, high thermal conductivity, low intrinsic carrier concentration and large critical electric field [10]. By contrast, silicon-based technologies are more mature and generally less expensive for a given line-width.

In general, both GaN and SiC belong to the same WBG semiconductors family and share similar attractive properties. However, SiC have received a great deal of attention in the past decade, especially in the high temperature applications field. Although important advances have been made on SiC based ICs, most of the reported ICs either had large areas or comprised small number of devices, leading to low device density integration [11]. In addition, no commercially available SiC integrated devices and circuits operating at temperature higher than 300 °C were found [12]. The direct temperature dependence of carrier concentration, due to the bulk nature of the active region in SiC devices, is considered as a common shortcoming [13] in addition to the crystal dislocations that degrade junction leakage, particularly at the highest temperature levels.

III-Nitride and primarily GaN technologies exhibit substantial performance improvement over SiC semiconductor with respect to response speed and operating temperature limits [14]. In addition, the temperature stability of electron concentration in the HEMT channel makes GaN devices more stable at high temperature. The recent research on GaN technology in Europe is summarized in [15] showing incremental progress to establish an independent GaN supply chain in Europe. In addition, [16]-[17] summarize some major recent trends of semiconductor research toward mature GaN technology that goes beyond the conventional limits of silicon. These papers discuss means to offer higher blocking voltages, wider range of operational temperature and better energy conversion efficiency.

Considerable efforts have been done to develop GaN devices operating at HT above 600 °C [14], 800 °C [18], 900 °C [19] and 1000 °C [20]. However, few research projects are directed toward the development of integrated microelectronic circuits and systems based on GaN devices. Despite the suitability of GaN technology for HT environments, limited integrated circuits and sensors are implemented based on GaN devices for HT applications [13], [21], [22]. The reported works show only the implementation of simple circuits like inverters, comparators, ring oscillators, and one stage differential amplifiers with maximum operation temperature not exceeding 500 $^{o}$C. There are still many challenges with GaN based technologies, including material, ohmic and Schottky

contacts. These challenges should be overcome before the exceptional ability of GaN to function at extreme temperature exceeding 600 $^{o}$C can be fully leveraged.

## 1.4 Objectives and research work overview

In this research, we propose the complete design of a wireless data transmission system to serve wireless monitoring sensors installed in harsh environments. Most of the existing industrial sensors impose bulky protection and direct connection between the monitoring sensor front end and the central control system. This is due to the limitations of available electronic technologies that can sustain high-temperature while processing the monitored data properly. To reduce the installation complexity and the protection cost, and to improve the data monitoring process, an appropriate technology should be developed and validated at HT. This technology will form the building blocks to implement circuits and systems able to operate in harsh conditions.

The primary goal of this thesis is to develop a data transmission system based on GaN technology to support wireless monitoring sensors and simplify their use in high temperature applications.

Our specific objectives are:

**Objective 1: Investigation and validation of GaN500 technology at HT:** The selection of GaN500 technology to implement the proposed system is based on special properties of GaN devices suitable for harsh environment conditions and the availability of GaN500 technology provided by NRC. The HT characterization of several GaN500 devices is performed to validate the robustness of the adopted technology at HT. An improved Angelov model is extracted from the HT characterization of GaN500 to capture the temperature effects on the design simulations. The HT model of integrated passive elements available in the GaN500 technology is also extracted from HT characterization and included in the design kit. This research was reported in Article 1.

**Article 1:** **Hassan, A.**, Amer, M., A., Savaria, Y., & Sawan, M. High-Temperature Characterization, Modeling and circuit validation of GaN500 HEMT up to 600 $^{o}$C. *IEEE Transactions on Circuits and Systems I: Regular Papers,* submitted (March 2019).

**Objective 2: Design and implementation of GaN based building circuits:** For the first time, several digital and analog building circuits are implemented based on GaN500. These circuits form the building blocks of the proposed data transmission system. The normally-on depletion mode GaN500 devices impose significant design constrains which implies to use a minimum number of

transistors to obtain the desired functions and for better miniaturization of the complete system. In addition, three demodulators are implemented to recover the monitored data from LSK-based modulated signal. One of the demodulators is a fully digital demodulation system dedicated for high frequency data transmission (MHz range). While the other two demodulators are based on the rectification technique and are dedicated to low frequency data transmission (kHz range) mainly required for data transmission through metallic barriers. The functionality of implemented circuits and demodulators at HT is performed by simulation and by experimental measurements for some circuits. Article 2 is an outcome of the work conducted as part of objective 2.

**Article 2:** **Hassan, A.**, Ali, M., Savaria, Y., & Sawan, M. GaN-based LSK demodulators for wireless data receivers in high-temperature applications. *Microelectronics Journal*, published on 14 January 2019.

**Objective 3: Design and implementation of fully integrated GaN based modulation and demodulation systems:** The proposed modulation/demodulation system is the first GaN500-based integrated data transmission system. Simple design with minimum number of transistors is implemented to reach a high integrity level and reduce the power consumption. The modulation system is based on a simplified delta-sigma modulation technique. The fully digital demodulator is adopted to recover the monitored data from the modulated signal. The reported simulation results confirm the functionality of the proposed systems using the models extracted from HT characterization. This work was reported in Article 3.

**Article 3:** **Hassan, A.**, Ali, M., Trigui, A., Savaria, Y., & Sawan, M. A GaN-based Wireless Monitoring System for High-Temperature Applications. *Sensors*, published on 14 April 2019. This paper was invited to the Special Issue on "Advanced Interface Circuits and Systems for Smart Sensors" in the Sensors Journal.

While pursuing Objectives 1 to 3, a number of additional publications listed below were produced.

**Additional related articles:**

**Hassan, A.**, Savaria, Y., & Sawan, M. (2018). Electronics and packaging intended for emerging harsh environment applications: A review. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, (99), 1-14.

**Hassan, A.**, Savaria, Y., & Sawan, M. (2018). GaN Integration Technology, an Ideal Candidate for High-Temperature Applications: A Review. *IEEE Access*, 6, 78790-78802.

**Conference proceedings:**

**Hassan, A.**, Trigui, A., Shafique, U., Savaria, Y., & Sawan, M. (2016, May). Wireless power transfer through metallic barriers enclosing a harsh environment; feasibility and preliminary results. *In 2016 IEEE International Symposium on Circuits and Systems (ISCAS)* (pp. 2391-2394). IEEE.

**Hassan, A.**, Ali, M., Trigui, A., Hached, S., Savaria, Y., & Sawan, M. (2017, June). Stability of GaN150-based HEMT in high temperature up to 400° C. *In 2017 15th IEEE International New Circuits and Systems Conference (NEWCAS)* (pp. 133-136). IEEE.

Abubakr, A., **Hassan, A.**, Ragab, A., Yacout, S., Savaria, Y., & Sawan, M. (2018, May). High-Temperature Modeling of the IV Characteristics of GaN150 HEMT Using Machine Learning Techniques. In *2018 IEEE International Symposium on Circuits and Systems (ISCAS)* (pp. 1-5). IEEE.

Amer, M., **Hassan, A.**, Ragab, A., Yacout, S., Savaria, Y., & Sawan, M. (2018, May). High-Temperature Empirical Modeling for the IV Characteristics of GaN150-Based HEMT. In *2018 IEEE International Symposium on Circuits and Systems (ISCAS)* (pp. 1-5). IEEE.

## 1.5 Organization of the thesis

This Ph.D. thesis includes seven chapters. The first chapter (Introduction) discusses the motivation behind this research. It also presents some background about wireless transmission through metal and the operation of GaN semiconductor. The primary and specific objectives are presented in this chapter as well, in addition to the organization of the thesis and coherence of the articles with the research goals.

In chapter 2, we present a critical literature review of harsh environment applications and the developed semiconductors to serve such applications including the advantages, challenges and limitations of each technology. This review introduces more specifically the problem formulation related to high-temperature devices and integrated systems for harsh environment applications. It

also shows the superiority of WBG GaN devices on other developed technologies at high temperature.

Chapter 3, 4 and 5 include our three scientific articles. In the first article (chapter 3), we demonstrate the performance of the GaN500 technology at HT including the characterization and modeling of fabricated GaN500 devices covering the 25 $^{o}$C to 600 $^{o}$C temperature range. The second article (chapter 4) presents the design and implementation of three demodulation systems based on GaN500 technology in addition to the circuit level validation of GaN-based digital circuits at 400 $^{o}$C. In the third article (chapter 5), we present the complete design of a wireless data transmission system based on GaN500 technology including the description of the proposed system in addition to the main considerations about the adopted design kit.

Chapter 6 includes a general discussion that summarizes the work done in this research. It also discusses the main constraints and limitations of our work including the fabrication issues, packaging and HT testing.

Finally, chapter 7 summarizes our contributions and achievements in this project. It also includes our recommendations to be taken for further improvements on the present design as well as our suggestions for the future directions of the current research.

## 1.6 Coherence of the articles in relation to the research goals:

This thesis follows the article-based format that includes papers produced as part of this Ph.D. research. The proposed wireless data transmission system is introduced in chapters 3, 4 and 5 including the device characterization, modeling, circuit design and validation, as well as system design and implementation. Each one of the three chapters presents published or submitted research work. The articles are perfectly consistent with the research work in terms of complementarity and incrementality of proposed contributions.

In the first article, we intensively focused on the adopted technology to examine the maximum limit of GaN500 design kit reporting the electrical characteristics of devices and integrated passive elements as a function of temperature from 25 $^{o}$C to 600 $^{o}$C. This article is preceded by two review articles and two conference papers. The review articles summarize the harsh environment applications and the corresponding developed electronics nominating the GaN devices as an ideal candidate for HT applications. The conference papers validate the possibility of transferring power

and data through metallic barriers at low frequency (kHz range) and show the robust HT characterization of GaN devices exceeding 400 ºC. In the following two articles, the simulations at HT were performed using an Angelov model available in the GaN500 design kit. However, this model was not validated for temperatures higher than 350 ºC. Therefore, in this article, an improved version of Angelov model is extracted to cover the 25 ºC to 600 ºC temperature range for future work. In addition, we experimentally demonstrated prototype digital logic gates and voltage reference ICs implemented using GaN500. The prototype ICs are characterized at operating temperatures ranging from 25 ºC to 600 ºC. This work contributes to the development and improvement of GaN technology, especially for GaN-based wireless monitoring systems targeting high-temperature environments. The reported GaN basic logic gates enable further development of other essential dynamic blocks such as ring oscillators, D-Flip Flop, delay elements and other typical digital logic circuits able to operate at HT.

The second article introduces the design of three demodulation systems based on GaN500 technology. The implemented systems demodulate LSK modulated signals for wireless monitoring applications operating at HT. The proposed demodulators are designed to demodulate low frequency modulated signals in the range of kHz and few MHz. The performed simulation results ensure their functionality over a wide temperature range between 25 ºC and 400 ºC. The design considerations of the proposed building circuits are discussed considering the specific requirements of the targeted applications and the limitations of adopted technology. Circuit validation of GaN-based logic gates was performed at 400 ºC.

In the third article, we selected one of the three demodulators introduced in the second article to build the complete design of a wireless monitoring system. This wireless data transmission system is based on GaN500 technology that is proposed to acquire signals from sensors installed in HT environments. The HT characterization of GaN500 devices, integrated resistors, and integrated capacitors was performed to validate their corresponding models used in system simulations. Circuit simulations of subsystems and building blocks were performed over the 25 ºC to 350 ºC wide temperature range to validate the capability of the GaN technology to implement an integrated wireless system that can be used in harsh environment applications.

# CHAPTER 2 LITERATURE REVIEW

## 2.1 Harsh environments and corresponding applications

Some harsh environments are more challenging than others. Among the different types of extreme conditions, the following are the most influential on the design and implementation of electronic devices and systems.

### 2.1.1 Low Temperature Environment:

The commercial temperature range specification of CMOS integrated circuits is from 0 °C to +85 °C, whereas the military specification temperature range is from −55 °C to +125 °C. In general, any temperature outside these ranges is considered an extreme temperature environment. Temperatures below those ranges are often called “cryogenic” due to the common use of cryogen liquids to reach them.

Diverse applications mandate cryogenic environments operation such as superconductivity. Further, many planetary bodies impose cryogenic environments, like the poles of Mars where the temperature drops below −143 °C in winter. Moreover, deep space applications, such the electronic detectors of the James Webb Space Telescope, operate at -246 °C.

Furthermore, in order to improve system sensitivity, diverse types of electronic instrumentations demand cryogenic temperatures as their operational temperature. Indeed, noise in resistors and electronic devices decreases with temperature and the dark current of diode detectors reduce exponentially with temperature. Thus, cooled detectors are found in various applications, such as in medical imaging instruments, high performance computers, satellite receivers and astronomical instruments.

### 2.1.2 High Temperature Environments:

On the other side of the extreme low temperature environments, extreme high temperatures surpass the standard commercial and military temperature range of +85 °C and +125 °C respectively. Indeed, many industrial applications require stable electrical and electronic systems for robust operation at high temperature. Aerospace electronic systems, automotive and on-engine

electronics, as well as power electronics are important examples where operating temperature ranges could extend up to 500 °C and even more if the electronic could withstand them.

Energy exploration such as geothermal production wells and oil and gas well-drilling are major applications of high-temperature electronics, where electronic systems must operate at temperatures ranging between 250 °C and 300 °C [23]. In addition, some space exploration projects mandate extremely high operating temperatures, which may exceed 600 °C, such as the missions targeting the surface of Venus.

### 2.1.3 Wide Temperature Range Environments:

A classic example of an environment imposing wide ranges of operating temperatures is the Moon, where its surface temperature in straight sunlight surpasses +120 °C, while dropping below -230 °C during the night, especially inside shadowed craters. The upper and lower limits of the temperature range in such applications may not by themselves be the worst factors to consider, but by the wide range covered and the temperature cycles in which the system must operate normally may be more harmful.

The rate at which thermal cycles occur may also be a significant issue and thermal shock can be far more challenging with respect to long-term reliability when compared to high or low fixed operating temperatures.

### 2.1.4 Radiation-rich Environment:

The three main categories of radiation effects are: a) displacement effects where high-energy particles displace atoms or nuclei, b) ionization effects where the materials are ionized when they are traversed by high-energy charged particles, and c) total dose that typically charges dielectric causing cumulative parametric shifts that render a device non-functional. Radiation-rich environments are mainly present in space applications, nuclear power plants and biomedical instruments.

### 2.1.5 Multi Extreme Environments:

When more than one type of extreme environments is present in one application, this situation will be called multi extreme environments. It is actually the most prevalent case as several harsh environments combine diverse types of extreme conditions, such as extreme low temperature with

extreme high pressure or vibration, or extreme high temperature combined with radiation-rich environments and so on.

Back to the Moon surface example, where low-temperature conditions (-230 °C) combine with high-temperature (+120 °C) and radiation effects due to solar winds and galactic cosmic rays, all these extreme environments must be addressed at once.

These diverse harsh environments and the corresponding applications stress the necessity of developing microelectronic devices that can meet application requirements in the expected environmental conditions. The following parts will investigate the most known semiconductors dedicated to harsh environments along with the corresponding limitations and improvements done so far.

## 2.2 Harsh environment electronics and implementations

Billions of dollars are invested in the extreme environment electronic industries to spread outside the conventional commercial and military electronics specifications. In 2005, the high-temperature electronics market was estimated to be around $17 billion. As a definition, extreme environment electronics are small volume systems with significant value-added propositions that are extremely important for harsh environment applications, but very costly to set and operate.

The following parts discuss the main existing electronic devices, along with their functionality at extreme environment conditions.

### 2.2.1 Silicon

Silicon based microelectronic technologies are the most common devices nowadays. Even though they are highly reliable in the majority of commercial applications, they are limited when the ambient conditions extend outside its normal -55 °C to +125 °C temperature range. Outside this interval, temperature can have a brutal impact on the transistor behavior. Once the surrounding temperature rises to extreme high ranges, the energy band gap of Si will drop down while the carrier density, which affects the thermal and electrical conductivity, exponentially increases, turning from stable extrinsic region into the intrinsic region. Another sensitive parameter affected by temperature variation is mobility, which determines the drift speed of a particle subject to an applied electric field. Moreover, the current density, carrier diffusion, velocity saturation,

electromigration, leakage current, threshold voltage and interconnect resistance are all significant mechanisms or parameters directly affected by extreme temperatures.

Another set of considerations with Si based platforms is their sensitivity to radiation. Even though threshold voltage shift with total dose is a dielectric volumic effect that had reduced significantly with scaling, the subthreshold leakage current is still seriously affected with deep submicron technologies. More precisely, gamma rays, cosmic ray's ions, x-rays, neutrons as well as high-energy electrons and protons have significant effects on electronic circuits operation that can have major impacts on operating characteristics and may induce failures.

The main basic concepts used to express and model the interaction between Si devices and radiation are the total ionizing dose (TID), displacement damage (DD) and single event effects (SEEs). TID is the damage produced by ionizing radiation over a time interval. Electron-ion pairs are generated by this ionizing radiation inducing trapped charges which, in turn, produce transient and long-term effects, in addition to changing threshold voltage and current leakage path. The displacement damage (DD), which is resulted by heavy ions, alpha particles, protons, neutrons and very high energy photons, can modify the configuration of the atoms in the semiconductor. It may provoke a permanent damage augmenting the recombination centers number and lowering the minority carriers. SEE is caused by a high-energy particle passes through a semiconductor keeping an ionized path behind. When this charge moves, it might be collected to another charge resulting in serious effects starting by a bit-flip and ending by tragic burnout.

### 2.2.2 Silicon on Insulator

Silicon-on insulator (SOI) technology is an advanced alternative option of the silicon CMOS technology to mitigate the drain induced barrier lowering (DIBL) and restrain charge-sharing and fringing field effects especially for the short-channel CMOS platforms and more precisely in 45 and 65 nm technologies.

SOI is mainly dedicated for aerospace and military applications exploiting its rigidity against the extreme temperature and radiation environments. Nowadays, it is more accepted as a commercially available technology.

SOI CMOS family is the most mature approach using traditional silicon process but includes an isolation process to ultimately reduce the leakage current at high temperature. Comparing to the

conventional P-N junction isolation in Si CMOS technology, a silicon dioxide layer surrounds each SOI transistor giving an excellent electrical isolation characteristic even at high-temperature conditions [24].

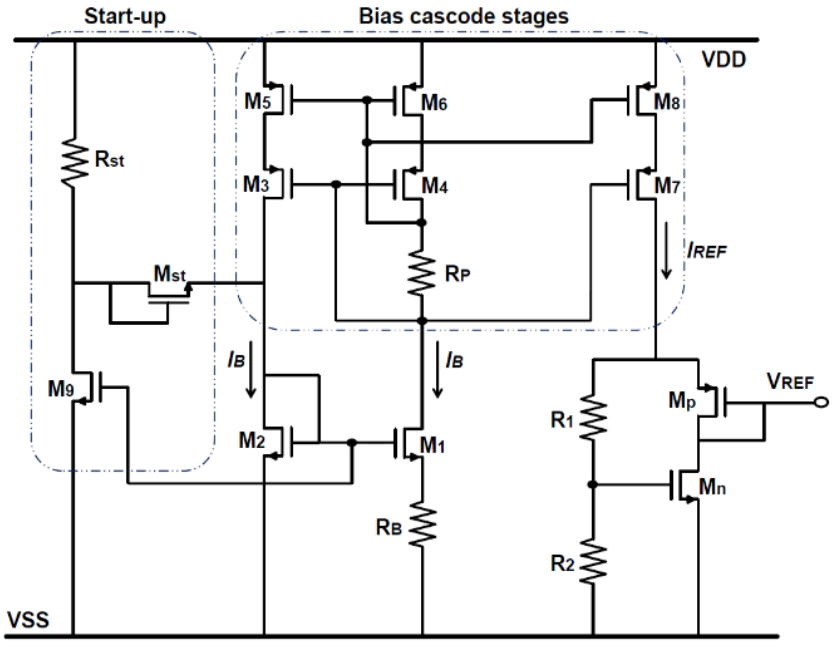



Figure 2.1: CMOS SOI based voltage reference circuit [25]

Consequently, SOI CMOS device was successfully implemented to serve a universal gate driver circuit at temperature higher than 200 $^{o}$C [25] and utilized in voltage reference circuit (shown in Figure 2.1) for a range of temperature between -40 $^{o}$C and 200 $^{o}$C under total radiation dose of 1 Mrad [26]. In addition, Honeywell investments in high-temperature SOI electronics introduced several products and processes like opamps, voltage references, voltage regulators, analog multiplexors, A-to-D converters (shown in Figure 2.2), digital gate arrays, SRAM, 8-bit microprocessor and clock interfaces [27] with endurable temperature exceeding 200 $^{o}$C.

Another advantage of SOI appears in the omission of parasitic area junction capacitance and the decrease of cross talk between digital and RF circuitry, in addition to the adequacy to integrate passive elements on chip with high accuracy profiting from the large substrate resistivity. Other merits for the SOI are the reduction of a reverse body effect in stacked circuits and the junction of the floating-body with source and drain is usually forward-biased.

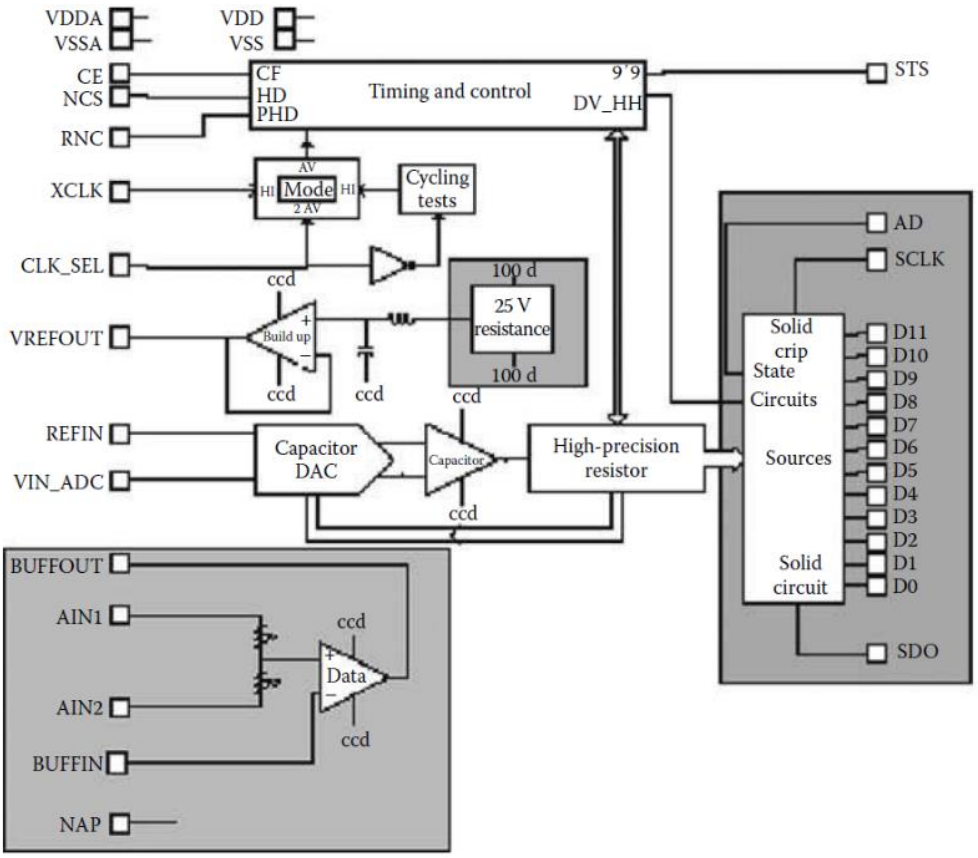
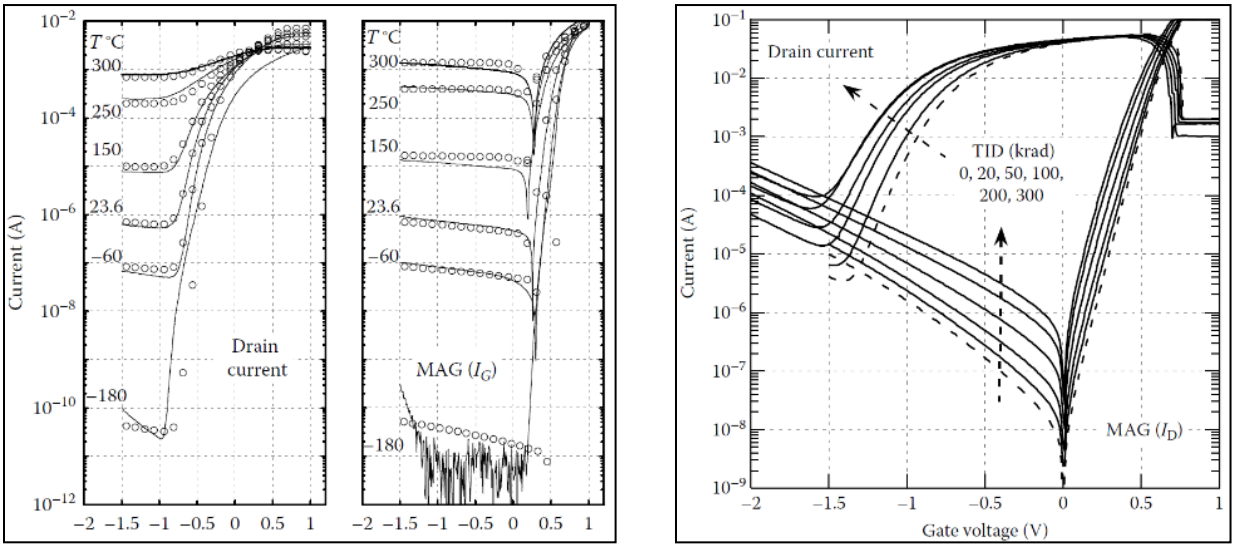



Figure 2.2: SOI based 12-bit analog-to-digital converter [27]

The SOI flexibility with the radiation is returned to its geometric constrains limiting the volumes of active silicon regions with the radiation energy ionization and deposition, and the limited communication of deposited charge between the devices.

SOI MESFET (Metal semiconductor field effect transistors) is a different approach for the silicon on insulator technology which is also developed to support the extreme environment applications covering a wide range of temperature between -180 °C and +300 °C and enduring intense radiation dose as shown in Figure 2.3(a) and (b) respectively [28]. The MESFET implementation, as shown in Figure 2.4, requires a Schottky barrier which is composed of the silicide step providing the low resistance source–drain contacts. The gate silicide is isolated from the source-drain silicides by space regions of length $L_{aS}$ and $L_{Ad}$ [29]. The silicide–silicon interface has the advantage of being extremely stable up to relatively high temperatures. Table 2.1 shows the utilized protection in each presented SOI devices.




(a) (b)

Figure 2.3: MESFET SOI CMOS technology as a function of gate voltage (V) for a fixed drain bias of 2 V: a) The drain current (left) and gate current magnitude (right) of 600 nm gate length, b) The radiation response of 300 nm gate length MESFET after successive radiation exposure up to a TID of 300 krad(Si) where the MESFET was positioned at a distance from the $^{60}$Co source that gave a dose rate of 0.9 krad(Si)/min [28]

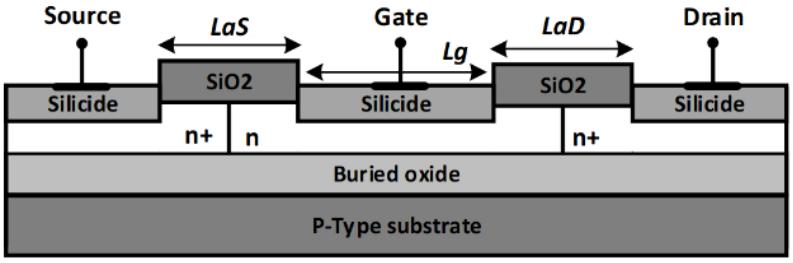



Figure 2.4: Schematic cross section of the SOI MESFET [29]

The insulating regions of SOI are mainly achieved by $SiO_2$ deposits. Regretfully, this isolation layer has a thickness more than that of the gate itself and suffers a charge trap higher than the highly-optimized gate stacks resulting in radiation responses by these isolation regions. To clarify this, the buried insulating oxide and associated TID for a thin SOI device can be represented as a secondary gate. This secondary gate modulates a pseudo-channel at the bottom of the transistor producing backside leakage current or attaches to the top surface channel by electrostatic force modifying the transistor threshold voltage. Moreover, even for the modern SOI technology such as

vertically stacked structures and mutli-gate which are intended for harsh environments, the parasitic effects have significant impacts.

### 2.2.3 Silicon Germanium (SiGe)

SiGe is a BiCMOS technology implemented by adding heterojunction bipolar transistor (HBT) to Si CMOS platform. This implementation advocates the functionality of highly integrated system performing a mixed-signal technology which is qualified by its high-performance feature for RF, analog and microwave circuits. The most preferable SiGe approach for extreme environment applications is the complementary SiGe BiCMOS on a thick-film SOI substrate to perform noise isolation which presents a critical topic in various analog and mixed-signal systems.

With decreasing temperature, the Si BJT device suffers from degradation in the turn-on voltage junction, base resistance, current gain, frequency response, cutoff frequency and delay in digital circuits. Unlike the Si BJTs, the cooling impact (low temperature environment) on SiGe HBT device is favorably improving its dc and ac properties [30]. A simple check of the SiGe HBT device equations shows the improvement in the transconductance, current gain, cutoff frequency, maximum frequency and broadband noise [31, 32].

In fact, despite the performance degradation of Si BJTs in cryogenic conditions, the addition of SiGe dramatically changes the situation. The bipolar transistor properties will be strongly coupled to the band-edge effects induced by bandgap engineering. Physically, the minority carrier of bipolar transistor is the reason of this strong coupling which implies in terminal currents proportional to the intrinsic carrier concentration ($n_{i0}^2$) through the Shockley boundary conditions, and in turn $n_{i0}^2$ is proportional to the exponential of the bandgap. Therefore, the currents will be coupled exponentially with any changes to the bandgap [30].

Moreover, from general mechanical considerations, these bandgap changes will automatically be divided by the thermal energy (kT), which means that a reduction in applied temperature will considerably increase any bandgap changes. Consequently, SiGe HBT device equations inspire that both ac and dc properties are favorably influenced by cooling.

Comparing the equations of a SiGe HBT to a comparably constructed Si BJT, the thermal energy (kT) is arranged to favorably affect the low-temperature properties. An extensive discussion with detailed analysis can be found in [33].

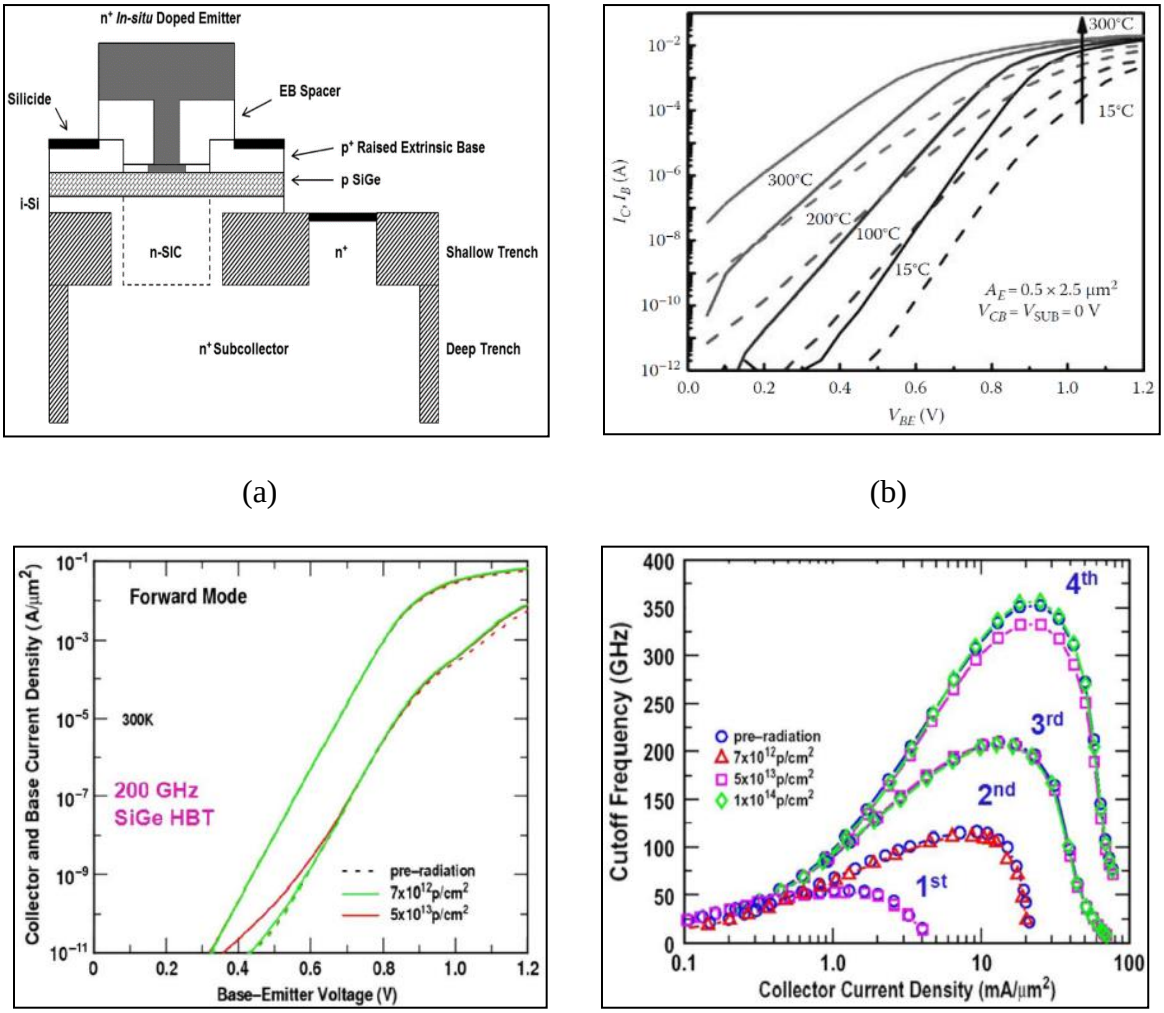
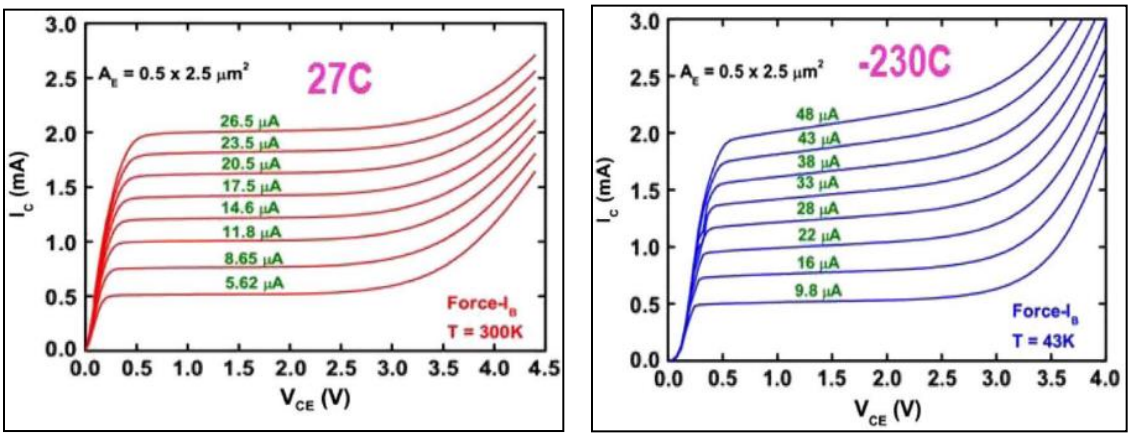



Figure 2.5: SiGe HBT: a) Cross-sectional view (3rd generation), b) Current–voltage characteristics (1st generation), c) Current-voltage characteristics (3rd generation) exposed to space-relevant 63-MeV protons to multi-Mrad total dose, and d) Cutoff frequency for four generations before and after exposure to space-relevant 63-MeV protons to multi-Mrad total dose [30]

On the opposite side of cryogenic conditions, the high-operating temperature has a degradation effect on both dc and ac performance of SiGe HBTs. However, the degree of this degradation is a matter to be discussed and investigated. Accordingly, SiGe HBTs commercially available with current gain above 100 and cutoff frequency of 75 GHz normally operate at 300 $^{o}$C [34]. In addition to the robustness of SiGe HBT device at extreme low and high temperatures, the durability of this

device in radiation environment has been investigated as well [35] showing a favorable built-in TID great tolerance as presented in Figure 2.5(c) and (d).

SiGe HBT, illustrated in Figure 2.5(a) with its unique bandgap properties, presents a significant process for the extreme environment applications. The latter can be classified as following: extreme high-temperature conditions exceeding 300 °C as characterized in Figure 2.5(b), extreme low-temperature environments lower than -200 °C (Figure 2.6) [30], wide and cyclic temperature intervals such as the lunar surface temperature between -230 °C and +120 °C, and finally the intense radiation environments.




(a) (b)

Figure 2.6: Output characteristics of a SiGe HBT (first-generation) operating at a) T = 27 $^{o}$C, and b) T = -230 $^{o}$C [30]

As an example, the work in [36] was supported from NASA ETDP to develop a remote electronics unit system based on SiGe HBT. The implemented remote sensor interface is depicted in Figure 2.7. The implemented system was tested under cryogenic temperature less than -173 $^{o}$C, 100 krad TID radiation exposure and at high temperature of 125 °C. Therefore, SiGe HBT is capable to satisfy the electronic requirements of all the preceding extreme environment conditions by slight process modifications providing considerable benefits regarding the weight, size and power constraints.

Moreover, in [37] and [38] SiGe devices have been utilized to implement voltage reference and LNA circuits respectively for cryogenic applications. Similarly, a wide-range temperature test (from -180 °C to 120 °C) have been successfully applied to ADC [39] and DAC [40] respectively.

Diverse generations of SiGe are nowadays widely spread in the commercial communities with tens of fabrication companies. The frequency capability of available SiGe HBT is between 50 and 200 GHz. Recently, 90 nm SiGe BiCMOS technology was presented in a comparator circuit for wide temperature range application between -195 $^{o}$C and -155 $^{o}$C [41], and a fourth generation of this device is implemented in [42] for RF applications at cryogenic temperature exceeding -195 $^{o}$C. Table 2.1 shows the utilized protection type in each presented SiGe device [30], [33-42].

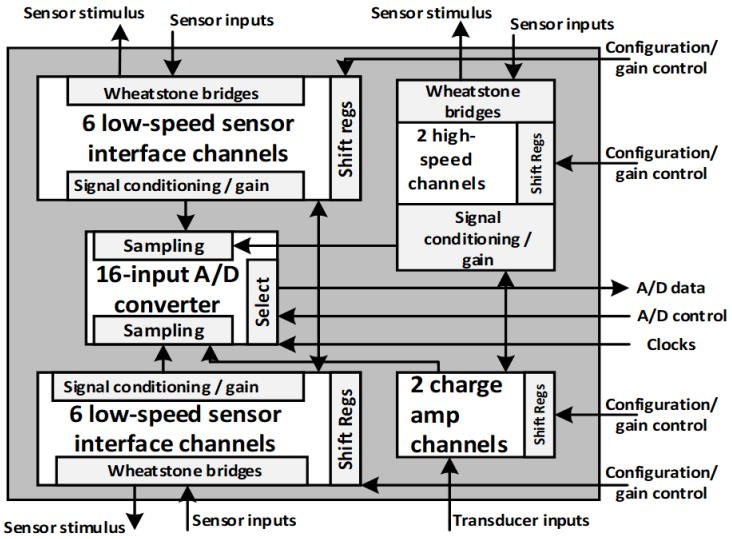



Figure 2.7: SiGe BiCMOS (SiGe HBT + CMOS) based simplified block diagrams of the Remote Sensor Interface [36]

Table 2.1: Protection type of presented SOI and SiGe devices

| Device | Reference | Protection |
|---|---|---|
| **SOI** | [25] | Ceramic package + Polyimide test board |
| | [27] | Ceramic package + Al-wire bonding + Au-plate + Ni-bond pad |
| | [26], [28, 29] | N/A |
| **SiGe** | [30, 33, 36] | Multi-chip Module Packaging: $Al_2O_3$ pacakge and lid, AlN substrate, Cu metallization, Au wire bond, In/Pb lid seal, polyimide and Cryogenic ribbon cable |
| | [34, 35], [39, 40] | N/A |
| | [37] | Ceramic flat package |
| | [38] | PC board sandwiched in between two gold plated brass carriers with the IC mounted in a VIA hole to minimize bond wire lengths |
| | [41] | Simulation |
| | [42] | Custom-designed, on-wafer, open-cycle liquid nitrogen (LN2) probe station |

N/A$^{*}$: Not mentioned in the related reference

### 2.2.4 Silicon Carbide (SiC)

For the moderate intensity of extreme environment applications, the standard Si platforms, silicon on insulator (SOI) and silicon germanium (SiGe) present suitable choice to be applied and cover the electrical and electronic requirements. However, when the surrounding conditions attain extremely harsh-condition environment, the preceding semiconductors are no longer useful, and an alternative advanced semiconductor generation should be developed such as the silicon carbide (SiC) to fit the excessive environment requirements.

SiC is composed of numerous types of crystal structures, named polytypes. However, there are just three types commonly accepted as an electronic semiconductor, which are 4H-SiC, 6H-SiC and 3C-SiC. Table 2.2 presents the most important electrical properties of these types compared with GaN and silicon [12]. The wide bandgap energy along with the high breakdown electric field are the two essential advantages of SiC over silicon semiconductor. Holding a very low intrinsic carrier concentration and a wide bandgap (same as the GaN device mentioned in Table 2.2) nominates the SiC to join the team of extreme high-temperature semiconductors, giving the capability to operate theoretically at high temperatures up to 800 °C. It is experimentally demonstrated that SiC devices can successfully operate for a limited time (few hours) at 600 °C [43].

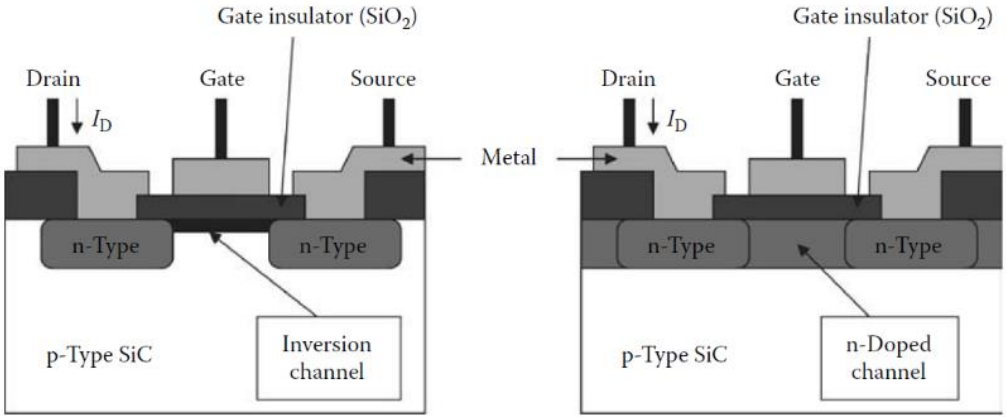
Table 2.2: Comparison of Selected Semiconductor Material Properties [12]

| **Property** | **Silicon** | **GaN** | **4H-SiC** | **6H-SiC** | **3C-SiC** |
|---|---|---|---|---|---|
| Bandgap energy (ev) | 1.1 | 3.4 | 3.2 | 3.0 | 2.3 |
| Relative dielectric constant | 11.9 | 9.5 | 9.7 | 9.7 | 9.7 |
| Breakdown electric Field at ND = 1017 $cm^{-3}$ (MV/cm) | 0.6 | 2-3 | 3.0 | 3.2 | 1.8 |
| Intrinsic carrier Concentration ($cm^{-3}$) | 1010 | ~$10^{-10}$ | ~$10^{-7}$ | ~$10^{-5}$ | ~10 |
| Electron mobility at ND = $10^{16}$ $cm^{-3}$ ($cm^2$/V.s) | 1200 | 900 | 800 | 60- 400 | 750 |
| Hole mobility at ND = $10^{16}$ $cm^{-3}$ ($cm^2$/V.s) | 420 | 200 | 115 | 90 | 40 |
| Saturated electron velocity ($10^7$ cm/s) | 1.0 | 2.5 | 2 | 2 | 2.5 |
| Thermal conductivity (W/m.K) | 150 | 130 | 400 | 480 | 500 |

Furthermore, SiC possesses a high-power density and efficiency due to its high-thermal conductivity along with the high-breakdown electric field and high-junction temperature. By these properties, SiC power converters have higher switching frequency implying to smaller transformers, inductors and capacitors reducing size, cost and weight of the power converters and

diminish the heat generation and energy loss. Various approaches of SiC have been developed to achieve a high performance and stable operation against the extreme conditions existed in harsh environments.

The main developed SiC approaches are SiC MOSFET (metal oxide semiconductor field effect transistor) (Figure 2.8) [12], MESFET, JFET (junction filed effect transistor), and BJT (bipolar junction transistor) semiconductors (Figure 2.9) [44]. The latter is mainly developed for high-temperature applications more than 300 °C.




(a) (b)

Figure 2.8: Cross-sectional view of the two basic SiC MOSFET: a) Inversion-channel, b) Doped-channel [12]

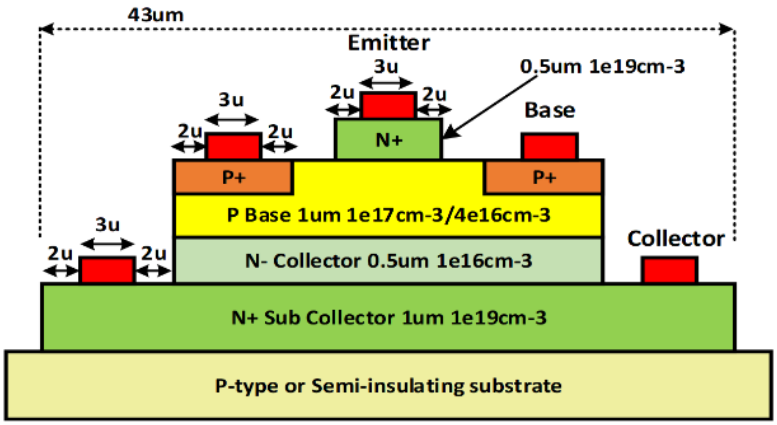
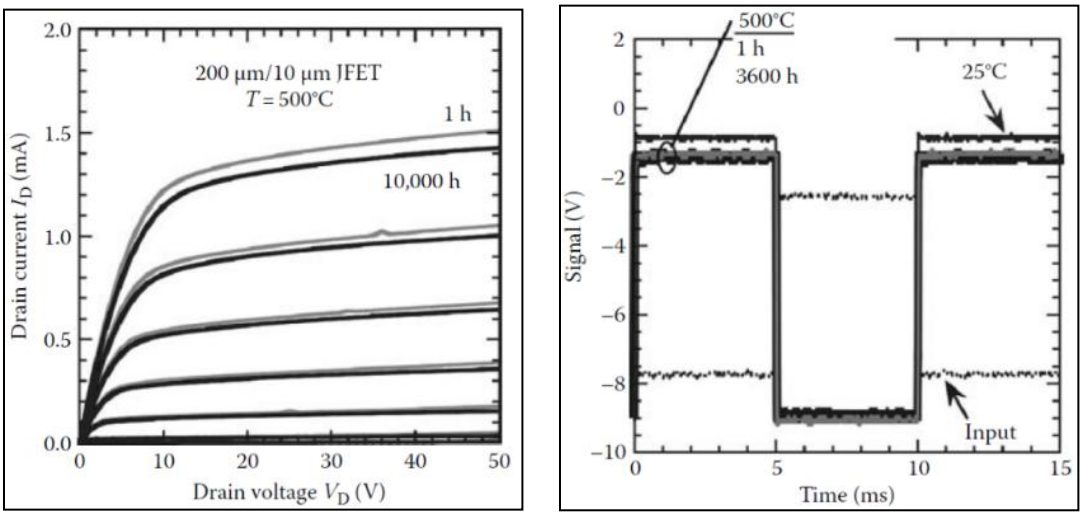



Figure 2.9: Cross-sectional schematic of 4H-SiC bipolar junction transistor (BJT) device topology [44]

As shown in Figure 2.10(a), a packaged 6H-SiC JFET is tested for 10,000 h at 500 °C operational temperature measured at start (gray) and end (black) in air atmosphere. In Figure 2.10(b), an experimental measurement of 6H-SiC JFET NOT gate IC test waveforms shows that similar output is obtained at 25 °C and at the start (1 h) and end (3600 h) of prolonged 500 °C operational testing in air atmosphere [45].

Generally, because of its low power consumption circuit, SiC-based CMOS may eventually become the principle type of SiC technology dedicated for harsh environments if the gate insulator durability and reliability issues can be overcome.




(a) (b)

Figure 2.10: 6H-SiC JFET: a) Current–voltage characteristics, b) NOT gate IC test waveforms [45]

Until SiC designers sufficiently cope with the gate insulator challenges, SiC BJT, MESFET and JFET based IC technologies present a direct approach to fit the extreme environments demands. As an example, the NASA Glenn Research Center has successfully approved the durability and prolonged stability of SiC JFET development at 500 °C ambient temperature for continuous thousands of hours with experimental measurements on amplifier stages and logic gates [46].

Moreover, several studies and implementations have been done recently for SiC semiconductors such as in [47] where seventeen samples of integrated circuits were successfully tested at 300 °C. The simulation results in [48] of 4H-SiC bipolar logic families are promising for operational temperature of 500 °C. In [49], a SiC CMOS comparator and Op-Amp are implemented and tested

at 550 °C. Similarly, 4H-SiC JFET is characterized at 600 °C [43] and a wireless RF transmitter, as shown in Figure 2.11, based on SiC technology was developed in [50] to serve pressure and temperature sensor systems at high-temperature applications exceeding 450 °C. Several logic gates have been implemented and tested in [11] at 250 °C based on MESFET SiC and a linear voltage regulator circuit based on SiC MOSFET device has been tested at 300 °C [51]. For intense-radiation applications, the impact of electron and proton irradiations on 4H-SiC MOSFET was investigated in [52] where the SiC device shows remarkable improvements in terms of electrical parameters after 15 MeV electron and 5 MeV proton irradiations.

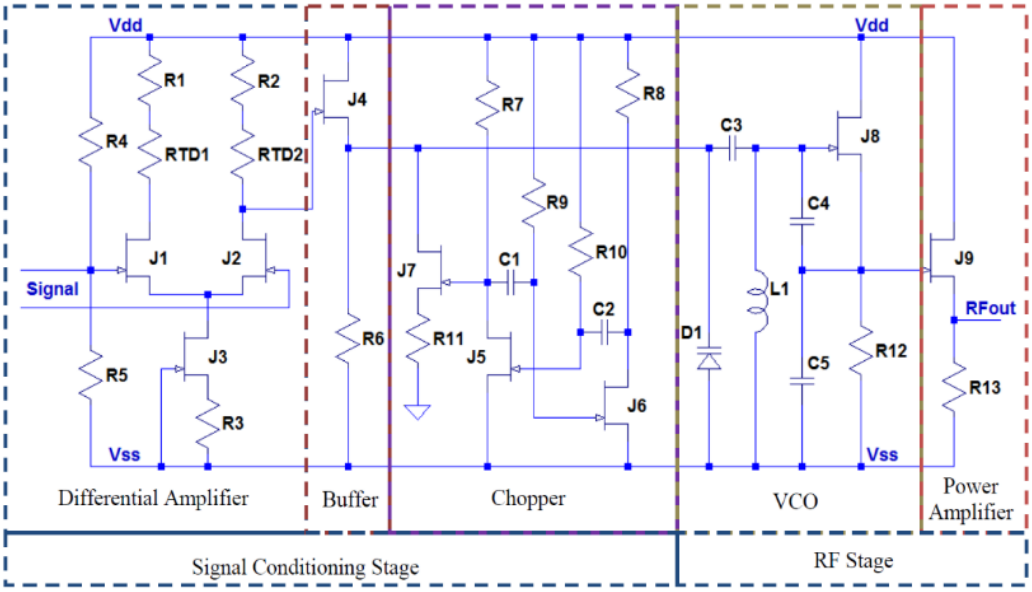



Figure 2.11: SiC JFET based circuit schematic of wireless sensing module for pressure and temperature measurement [50]

On the other hand, and to date, there is no existence of a commercial SiC semiconductor transistor or IC that can be utilized in an ambient temperature more than 300 °C. Although over the last decade the improvement of SiC prototypes achieve an advanced stage, it remains a difficult challenge to reach long-term operational reliability for extreme temperature circuits and devices especially regarding the reliability of contacts, passivation [53], interconnect and packaging. Therefore, seemingly, SiC technology will be solely dedicated for space applications where it is not possible for existing technologies to take place due to the extremely harsh environment condition. Whereas, in case of lower extreme environments (means less than space application), it

is more effective to use the other existing technologies which are less expensive and more mature than SiC device especially in the low-power signal processing and digital logic circuit functions.

## 2.2.5 Gallium Nitride (GaN)

### 2.2.5.1 Operation of GaN semiconductor

The III-nitride semiconductors include broad ranges of bandgaps varying from 0.7 eV for InN, 3.4 eV for GaN, up to 6.2 eV for AlN. Profiting from their wide range of energy bandgap, these materials can be utilized to emit light in various visible ranges (violet, blue and green) in addition to be used in high frequency and high-power application [54], [55], [56]. A great deal of research focused on GaN and its alloys like AlGaN and InGaN. These alloys were investigated for their special properties, such as low resistivity and high voltage capability. Obtaining good substrate material for GaN remains challenging due to the difficulty of providing a good quality GaN substrate layer. Other alternatives are utilized such as sapphire, SiC and silicon substrates, which are available at lower cost. These substrate materials are thermally compatible and have proper lattice matching with GaN.

#### *2.2.5.1.1 GaN basic principle:*

The thermodynamic stability of GaN is due to its wurzite crystal structure and bandgap energy of 3.4 eV, which makes it capable of sustaining high temperature. Growing GaN layers is typically done by molecular beam epitaxy (MBE), metal-organic chemical vapor deposition (MOCVD) and hybrid vapor phase epitaxy (HVPE). These various methods open a wide variety of epilayers quality and surface roughness.

The first GaN epitaxial layer grown on sapphire substrate was reported in 1969 [57]. Due to the high n-type background carrier concentration of GaN layers and the lack of p-doping, GaN could not be used rapidly in electronic devices and its adoption was very limited until the 1980s. Hetero-epitaxy problems could be eliminated by utilizing GaN substrates, giving better control of stress, dopant concentration, polarity, lattice constant mismatch and thermal expansion coefficient mismatch. However, the difficulty of obtaining large GaN wafers and their costly fabrication further hindered its adoption. With the availability of large sapphire ($Al_2O_3$) wafers that provide perfect electrical insulation, while offering high quality, excellent temperature stability and low

fabrication cost, this material was considered as a candidate substrate for GaN. Unfortunately, using sapphire substrates leads to high defect density, because of low thermal conductivity and large lattice mismatch to GaN.

Silicon carbide (SiC) and silicon (Si) offer higher thermal conductivity and smaller lattice mismatch to GaN, and combining them gives good candidate solutions for high temperature applications. However, the disadvantages of SiC substrates are their small area, intermediate quality and high price. These disadvantages of SiC play in favor of silicon as a substrate of choice for GaN epitaxy with its good thermal conductivity, low cost and availability of larger wafers, in addition to the possibility of integrating GaN devices with mature silicon devices. On the other hand, the high thermal expansion coefficient mismatch and large lattice mismatch between Si and GaN favor the appearance of cracks on the surface. Table 2.3 summarizes the physical properties of several substrates considered for GaN.

The attention with GaN has focused on HEMTs (High Electron Mobility Transistors), which are also called HFETs (Heterostructure Field Effect Transistors). To explain the theory of operation of GaN HEMT devices, AlGaN/GaN will be used [58]. These devices are the dominant GaN HEMT structure. When an AlGaN alloy is deposited on a thick GaN layer, an AlGaN/GaN heterostructure is formed. Band bending happens due to the difference in bandgap energies between the two semiconductors, and a two-dimensional electron channel is created in the upper side of the GaN layer (Figure 2.12(a)).

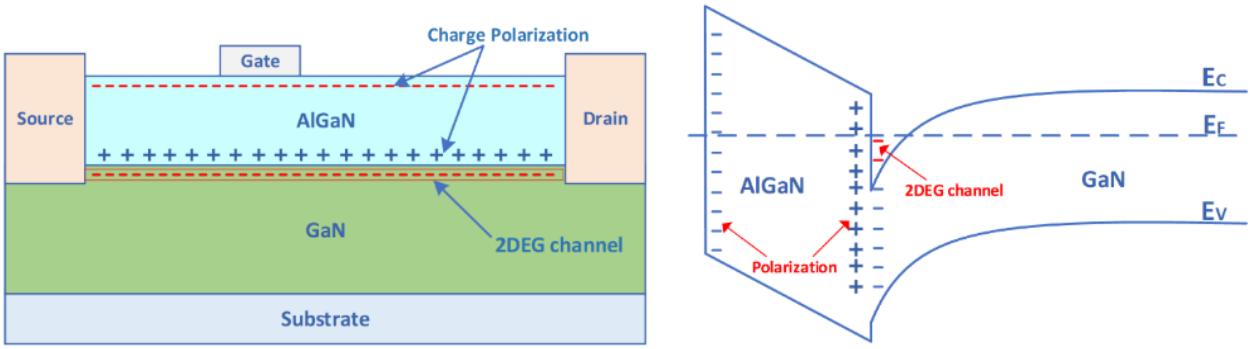
Table 2.3: Physical Properties of Substrates Considered for GaN Technologies

| **Properties** | **Substrate** | | | |
|---|---|---|---|---|
| | GaN | $Al_2O_3$ | SiC | Si |
| Thermal expansion coefficient ($10^{-6}$ $K^{-1}$) | 5.59 | 6.9 | 2.77 | 2.6 |
| Lattice mismatch (%) | - | -16 | +3.5 | -17 |
| Thermal conductivity (W/cmK) | 1.3 | 0.5 | 3.8 | 1.5 |
| Wafer size (inches) | 2 | 6 | 3 | 12 |
| Cost | high | low | High | low |
| Resistivity | high | high | High | mediate |
| Temperature stability (°C) | >900 | >1600 | 1700 | 900 |

The wurtzite structure of GaN is tetrahedrally coordinated with a lack of symmetry in the c-direction [59]. A spontaneous polarization along the c-direction takes place because of this lack of

symmetry and the large iconicity of the covalent bond in the GaN structure. The lattice mismatch between AlGaN and GaN induces a piezoelectric polarization oriented in the same direction as the spontaneous polarization. The total polarization charge is the combination of both the piezoelectric effect and difference of spontaneous polarization. Therefore, a positive polarization charge appears at the lower interface between AlGaN and GaN due to the superiority of AlGaN polarization over the GaN layer.

To compensate this positive charge, electrons are attracted to form a 2DEG (Two-Dimensional Electron Gas) dropping below the Fermi Level $E_F$. This creates a triangular quantum well at the AlGaN/GaN interface as shown in Figure 2.12(b). Even without doping the AlGaN layer, the 2DEG is produced due to the strong piezoelectric and spontaneous polarization effects in nitrides, resulting in high electron density and high drift mobility. The carrier concentration is limited by the strain relaxation of the top layer. The AlGaN layer thickness, as well as the Al concentration have a direct effect on the maximum sheet charge. A positive polarization is formed in Ga-faced structures. A negative polarization will take place in the case of N-faced structures, which will be compensated by holes instead of electrons, and these charges are accumulated at the AlGaN/GaN interface.




(a) (b)

Figure 2.12: AlGaN/GaN based HEMT: a) Physical structure and b) Band structure

Electron trapping may occur due to the presence of impurities in the lattice structure or at the interface between the heterostructure layers, which produces a current collapse that in turn deteriorates the device performance. After applying drain-source voltage, the trapped carriers remain, even when removing this voltage, leading to degeneration of the device output power. This can be compensated by light illumination on the device, giving enough energy to the trapped

carriers to be released. There are various scattering mechanisms that affect the total mobility of the 2DEG channel, such as polar optic scattering, ionized impurity scattering, piezoelectric scattering and acoustic phonon scattering.

A simplified cross-sectional representation of a typical GaN HEMT structure is depicted in Figure 2.13. The substrate layer could be one of several materials like silicon, silicon carbide or sapphire as discussed previously. The nucleation layer is very important to ensure better growth quality of the following layers and to allow a good polarity of the upper buffer layer. Usually, AlN and GaN are utilized as nucleation layers. The buffer layer ensures device isolation and improves the material quality. A thick GaN layer is present on the upper side of the 2DEG. A thin undoped AlGaN layer (AlGaN/GaN case) acts as a spacer for carriers injected into the 2DEG by the carrier supply layer. The carrier supply layer could be Si-doped GaN layer or an undoped AlGaN layer supplying the 2DEG with electrons. The main purpose of the barrier layer is to maintain an effective barrier for the Schottky contact typically placed over this layer.

By default, when a positive voltage is applied to the drain, the current flows between the drain and the source through the 2DEG sheet. This current can be controlled by the applied gate voltage, which, in turn, controls the space charge of the two- dimensional conductive channel. The quality of the 2DEG sheet depends on various parameters such as the substrate material, the method used to grow the layers composing the device and the doping level of carrier supply layer. With negative gate voltage values, the space charge under the gate area expands toward the 2DEG loaded with electrons gradually depleting this channel until the 2DEG sheet is pinched off.

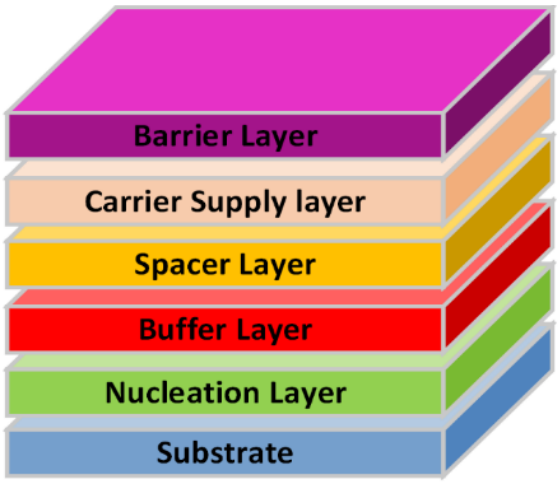



Figure 2.13: Schematic drawing of a typical GaN HEMT layer structure

#### 2.2.5.2 GaN advantages

To understand the superiority of GaN technology over conventional devices at high temperatures, it is very important to identify the main factors that affect the physical limits and operation of semiconductors at high temperature.

##### *2.2.5.2.1 Intrinsic carriers:*

All semiconductors have thermal electron and hole carriers in their crystals. The intrinsic carrier concentration ($n_i$) varies exponentially with semiconductor temperature [60] following equation (2.1), where k is the Boltzmann constant.

$$n_i = \sqrt{Nc\ Nv}e^{-E_G/2kT} \quad (2.1)$$

In (2.1), $E_G$, $N_C$ and $N_V$ are respectively the energy bandgap and the effective electron and hole density of the semiconductor that vary only slowly with the device temperature (T) when compared to the ($e^{-E_G/2KT}$) term that grows exponentially with temperature. Consider the temperature dependence of the intrinsic carrier concentration [61], the $n_i$ of silicon at room temperature is around $10^{10}$ $cm^{-3}$. This concentration is almost negligible if it is compared to the device doping level around $10^{15}$. However, when the temperature exceeds 300 $^oC$, this concentration becomes higher than the dopant carriers' concentration in typical doped silicon semiconductor. This undesirably affects the electrical properties of this device that is supposed to be controlled by well-designed doping levels.

On the other hand, the GaN intrinsic carrier concentration, with its wide bandgap (around 3 eV), is much lower than the one observed in silicon, even at higher temperatures beyond 600 $^oC$. This prevents problems due to excessive intrinsic carrier concentration. As shown in Figure 2.14 [62], at any temperature, the intrinsic carrier concentration (and consequently, the intrinsic leakage current) is around 12 orders of magnitude lower in WBG semiconductors than in the more common ones such as silicon.

##### *2.2.5.2.2 Leakage current of p-n junctions:*

The leakage current of p-n junctions is the reverse current passing through the equivalent diode of this junction when a reverse bias voltage is applied. This reverse current must be negligible particularly in power applications where high switching frequency is needed at high applied voltage

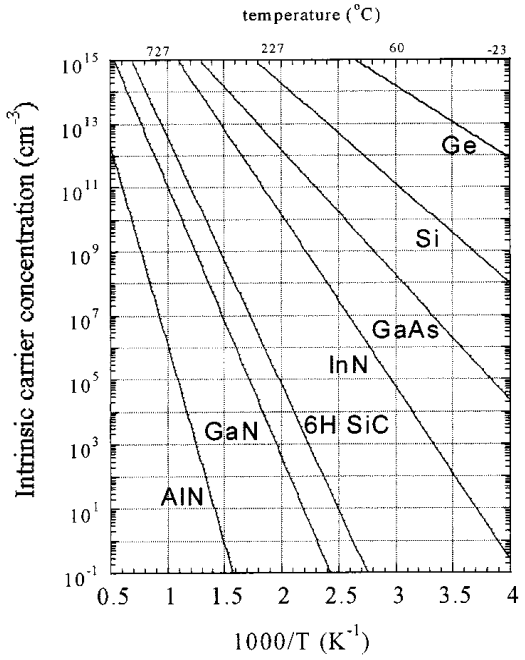



Figure 2.14: Semiconductor intrinsic carrier concentration versus temperature [62]

[63]. The mobile carriers, which are depleted at the junction area, form the depletion region of p-n junctions. The p-type junction is positively charged with hole carriers and the n-type junction is negatively charged with electron carriers. The I-V characteristic of a p-n junction diode is given by (2.2) when the p-type doping is larger than n-type doping [64]

$$I = qAn_i\left(n_i/ND\sqrt{DP/\tau}\,A\left(e^{qV_A/kT}-1\right)+W/2\tau\left(e^{qV_A/2kT}-1\right)\right) \qquad (2.2)$$

At applied voltage $V_A$, the depletion region width is $W$ and $\tau$ is the lifetime of effective minority carrier in seconds. The minority carrier diffusion current is represented in the first exponential term in (2.2), while thermal generation appears in the second exponential term. Assuming that few tens of mV of reversed bias voltage $V_A$ are applied at high temperature less than 1000 $^{o}$C, equation (2.2) can be simplified to (2.3)

$$I = -qAn_i\left(n_i/ND\sqrt{DP/\tau}+W/2\tau\right) \qquad (2.3)$$

where it is obvious that the leakage current of the reversed biased p-n junction is substantially related to the intrinsic carrier concentration $n_i$. Therefore, a harmful leakage current on the device and the system using such junctions is observed when the reversed biased junction is used at high applied temperature. In GaN semiconductor devices, this leakage current is orders of magnitude

lower than in silicon devices, due to their lower intrinsic carrier concentration $n_i$. Thus, GaN and all wide bandgap semiconductors are much better candidates for applications where the temperature exceeds 300 °C and can reach 600 °C.

*2.2.5.2.3 Carrier emission leakage current:*

Another type of leakage current that can affect device operation is the carrier emission leakage current. When the carriers gain sufficient energy to pass through an energy barrier, this process is called emission and is directly related to the temperature which is considered as the source of thermal energy. This mechanism appears in Schottky barrier contact rectifying metal-semiconductor diodes. The carrier emission current can be expressed by:

$$I = AK^*T^2 e^{-q\Phi_B/kT}\left(e^{qV_A/kT} - 1\right) \quad (2.4)$$

where $\Phi_B$ is the Schottky barrier height (effective potential barrier height). For a significant reverse bias voltage $V_A$, the current in (2.4) can be simplified to:

$$I = -AK^*T^2 e^{-q\Phi_B/kT} \quad (2.5)$$

where the carrier emission leakage current decreases according to an exponential relation in $\Phi_B$. It is easy to see that the leakage current can be controlled by the effective potential barrier height. Although this $\Phi_B$ depends on the junction formation, the semiconductor and the metal, it cannot be larger than the device bandgap and, in most cases, less than 75% of the bandgap energy. Therefore, the Schottky barrier heights are limited to 0.9 V for silicon device (1.1 eV bandgap), whereas the barrier heights in GaN semiconductors (<3.3 eV) are three times larger. This advantage in wide bandgap devices reduces the junction leakage current by several orders of magnitude at any operating temperature, thus enabling the implementation of devices operating at high voltage and high temperature where conventional semiconductors are no longer usable.

*2.2.5.2.4 Power applications:*

In power applications, there exist several sources of power dissipation. Large currents flowing through power semiconductor devices always imply significant dissipated power in the device resistance. In addition, considerable instantaneous dynamic power dissipation appears during on-off switching of power devices. Also, a large amount of power dissipation is induced by off-state leakage currents flowing while the power devices block high voltages. In case of high ambient

temperature, the influence of those power dissipation sources becomes more serious and increases the internal temperature of power devices significantly beyond the surrounding temperature, which typically results in undesired interaction between power dissipation and device temperature.

However, the special properties of GaN devices, including their wide bandgap, high-drift saturation velocity, thermal conductivity (SiC substrate), high-breakdown electric field and low-intrinsic carrier concentration, put them as leading candidates for high-power applications [54, 55], [65], [66], [67]. Table 2.4 presents the most important electrical properties of GaN compared with GaAs, silicon and SiC (wide bandgap semiconductor family) [68]. The most common polytypes of SiC semiconductors are the hexagonal 4H and 6H structures. These polytypes are differentiated by the stacking sequence of the biatom layers of the SiC structure [69].

Table 2.4: Comparison of Selected Semiconductor Material Properties [68]

| **Property** | **Silicon** | **GaAs** | **4H-SiC** | **6H-SiC** | **2H-GaN** |
|---|---|---|---|---|---|
| Bandgap energy (eV) | 1.1 | 1.42 | 3.2 | 3.0 | 3.4 |
| Relative dielectric constant | 11.9 | 13.1 | 9.7 | 9.7 | 9.5 |
| Breakdown electric Field at $N_D$ = $10^{17}$ $cm^{-3}$ (MV/cm) | 0.6 | 0.6 | 3.0 | 3.2 | 2-3 |
| Intrinsic carrier Concentration ($cm^{-3}$) | $10^{10}$ | 1.8 x $10^6$ | ~$10^{-7}$ | ~$10^{-5}$ | ~$10^{-10}$ |
| Electron mobility at $N_D$ = $10^{16}$ $cm^{-3}$ ($cm^2$/V.s) | 1200 | 6500 | 800 | 60- 400 | 900 |
| Hole mobility at $N_A$ = $10^{16}$ $cm^{-3}$ ($cm^2$/V.s) | 420 | 320 | 115 | 90 | 200 |
| Saturated electron velocity ($10^7$ cm/s) | 1.0 | 1.2 | 2 | 2 | 2.5 |
| Thermal conductivity (W/m.K) | 150 | 55 | 400 | 480 | 130 |

### 2.2.5.3 GaN challenges and limitations

#### *2.2.5.3.1 Challenges*

In spite of the promising properties of GaN devices as great candidates for extreme temperature applications, there still exist major technical challenges that must be surmounted before their beneficial properties can be fully leveraged in high temperature electronic systems.

Materials:

The material quality and crystal growth of GaN and III-Vs devices remain inherent hinders that should be overcome to enable these devices to withstand high temperature conditions. The

heteroepitaxial growth of GaN devices is typically performed on foreign substrates such as SiC and sapphire instead of single crystal GaN wafer. The I-V characteristics of p-n junctions are undesirably affected by the crystal dislocation defects in GaN semiconductor inducing leakage currents greater than estimated in (3), which may hinder the merits of GaN in high temperature applications due to specific types and density of defects. For high power GaN devices, material defects have large effects because of the large junction area and high electric fields [55], [66].

Moreover, the device efficiency can be also adversely affected by surface morphological defects and variations of thickness across the wafer. Therefore, more improvements in material quality and crystal growth are still required to enable effective use of GaN devices in high temperature environments. Although demonstration of GaN devices operation at high temperature between 300 $^{o}$C and 600 $^{o}$C has been successful [70], long-term reliable functionality is still unachievable and more fundamental technological adjustments are needed.

Contacts:

Due to the absence of metal contacts with suitably low barrier with the semiconductor, it becomes difficult to produce ohmic contact to GaN wide bandgap semiconductor. For that reason, a low resistance ohmic contact is obtained by doping heavily the semiconductor region close to the metal interface.

Ideally, the Schottky contacts that constitutes the gate should possess a high breakdown voltage and low leakage current. Generally, Ni and Au are the common metallic Schottky contact materials, with high work function conducting to high Schottky barrier heights. It is of interest that Ni offers excellent adhesion to nitride, while Au offers an excellent thermal stability.

The conductive contacts functionality at high temperature is not less important than that of the semiconductor itself. The reliability of contacts metallization and interconnects between the on-chip devices presents a substantial challenge for GaN operation at high temperature, particularly for applications beyond 400 $^{o}$C. The self-heating generated during normal operation combines to the surrounding high temperature to cause contact degradation and limit the long-term reliability of GaN devices.

The metal-semiconductor ohmic and Schottky contacts of n-type and p-type layers must have thermal stability during the device lifetime. The conductive n-type are more easily obtained than p-type doping layers due to the difference of acceptor and donor dopant ionization energies. Thus,

n-type contacts are more mature than p-type contacts and they offer better performance. Understanding the electrical characteristics and reaction kinetics of metal/GaN interface are the main focus of several researchers who also study diffusion barriers in case of multilayer metallization. Although hermetic packaging is a good solution to protect the contacts at high temperature, developing contacts that are thermally stable at high ambient temperature leads to simpler and less expensive packaging.

The Ti/Al/Ni/Au low resistance ohmic contact has been studied in [71] between 25 $^{o}$C and 600 $^{o}$C for n-type GaN. On the other hand, various Schottky contacts such as n-GaN Ni/Au, Ni/Pt/Au, Pt/Ni/Au and Pt/Ti/Au have been investigated in [72] for temperatures going up to 400 $^{o}$C. In parallel, a novel Mo/Al/Mo metal stack is introduced in [13] to improve the robustness of ohmic contacts at high temperature reaching 500 $^{o}$C. A high-K dielectric is deposited to provide Schottky contacts showing stable dielectric permittivity and reduced leakage over a wide temperature range. However, it offered breakdown voltages decreasing with temperature due to the ionization of deep traps in the dielectric material.

Due to the difficulties of realizing conductive p-type GaN layers, obtaining highly stable contacts of this material has presented serious challenges so far. Additionally, more studies are still needed to investigate the reliability of GaN ohmic contacts in presence of electromigration and chemical reactions with applied electrical bias at oxidizing high temperature above 400 $^{o}$C. Thus, significant challenges related to GaN contacts must be surmounted to enable GaN devices to support long-term operation in real environment and at temperatures higher than 600 $^{o}$C.

#### *2.2.5.3.2 Limitations*

The limitations of GaN HEMT can be separated into two types: 1) technological, such as barrier scaling, thermal limitations and chemical limitations, and 2) intrinsic associated with current collapse and device self-heating.

Technological limitations:

The output power is proportional to the barrier thickness. On the other hand, this barrier thickness is inversely proportional to the device cut off frequency. This conflict could be resolved with several techniques such as using a thin barrier with a low surface potential and high polarization discontinuity as well. For example, an AlN barrier layer can be applied [73] and the break down

voltage could be maximized by utilizing slanted gates [74]. Optimizing the buffer layer growth with an extremely insulating materials would reduce the buffer leakage current [75]. It is very important to suppress the leakage current of Schottky contacts on the Mesa edge to improve the mesa isolation. Reducing of gate source resistance by shortening the gate source distance and contact resistance would decrease the knee voltage which directly affects power devices. The influence of tunneling of ohmic contact could be minimized by contact recess [76], selective doping [77] or re-growth of ohmic contact region [78].

In addition, the so-called recessing process avoids undesired kink effects and prevents $R_C$ (contact resistance) and gm (transconductance) nonlinearities [79]. A piezoelectric polarization is also related to the Al concentration, which leads to a drop in the electron mobility and increases the barrier strain and strain relaxation [80]. Additionally, stress in the barriers hinders the growth of thick barriers to prevent cracking and defects.

Additional challenges can appear when the recessing process is applied on thick barriers. One of the challenges is damage of the heterostructure polarization by discriminatory etching [81]. Another type of faults that can result from physical defects is an increase of gate leakage currents, which are dominated by the tunneling mechanism, especially when the junction is forward biased. The leakage current can be shrunk by raising the Schottky barrier height through some higher metal barrier or by modifying the surface potential with wet chemical or plasma treatments [82, 83]. Another alternative is a gate dielectric approach forming a MOSHEMT [84] or an InGaN cap layer on the barrier layer [85].

Chemical limitations appear when the GaN HEMT device is utilized in chemical applications [86, 87]. In this case, a stable passivation layer is required to protect the free surfaces of the device. And the thermal limitations present when the device operates in high temperature environment or during high power operation causing self-heating effects. In such conditions, the heterostructure may suffer degradation or surface decomposition [88] if materials reach their chemical stability limit. Thermal management is a key solution when dealing with self-heating, but in high temperature applications, the device, the passivation material, and the contact metallization should be thermally stable.

A promising solution is to overgrow a diamond layer over the HEMT devices, taking advantage from its high thermal conductivity to obtain an efficient heat management system. However, this

approach is not applicable to all GaN HEMT devices, because of the harsh growth environment conditions which could degrade the GaN device [89].

Intrinsic limitations:

The previous technological limitations can be avoided by selecting a suitable heterostructure and proper device design. On the other hand, the intrinsic limitations discussed here are of prime interest when considering the device reliability because they cannot be prevented. For instance, the dispersion effect (lag effects) that can induce the current collapse phenomenon is inherent in all GaN heterostructures. Dispersion is due to the polarization counter charge on the top surface. Current collapse can degrade power performance and DC characteristics of GaN devices, even before the predicted theoretical values.

In planar GaN HEMT devices, a high-breakdown voltage can be obtained by removing the surface donor charge localized in the area between the gate and drain. On the other side, this will induce drain-lag current collapse if the injected charges are not able to track the swing frequency of the applied voltage. This phenomenon is observed when the device operates at high power, but it does not appear in small signal operation and it does not affect the cutoff frequency and the fmax. Several experimental techniques can be used to detect current collapse, such as large signal pulsing, switching operation and dual gate methods. In addition, current collapse effects can be observed by combining DC characteristics with dynamic load lines at RF operation.

Current collapse effects can be controlled by regulating the injected lateral charge. To do that, a passivation layer could be added to prevent the injected charges from running on the surface [90]. In this case, charges will concentrate in the passivation layer, far away from the surface. This is obtained with suitable surface treatment and passivation type. With an efficient passivation, the impact of virtual gate effects can be reduced very significantly.

Moreover, a lossy dielectric can be used to augment the injected charges mobility shifting the current collapse to higher operation frequencies. Additionally, this effect can be reduced by using gate recess and the field plate mechanism. Eventually, controlling the charge and discharge of surface traps traveling between the gate and drain is an essential factor to reduce current collapse. This can be done by controlling the device fabrication steps and the passivation deposition.

The most common passivation to reduce the current collapse of GaN HEMT devices are MOCVD $Si_3N_4$ [91] and PCVD (plasma chemical vapor deposition) $Si_3N_4$ [92], in addition to combinations

of gate dielectric and passivation ALD-$Al_2O_3$ [93, 94] and high dielectric constant oxides such as MgO, $HfO_2$ and $ZrO_2$ [95, 96].

Self-heating represents a major factor that can limit the reliability and performance of GaN HEMTs. Indeed, the device temperature increases with the dissipated power. This self-heating affects the device high-frequency operation and output power due to the reduction in drift velocities and mobility respectively [97]. In addition, higher device temperatures accelerate electromigration and aging of device metallization that can affect reliability and induce device failure [98]. Therefore, an effective heat dissipation management is necessary to get a reliable device, especially in power applications.

The device temperature could be estimated by several techniques such as scanning thermal microscopy [99], photo-current measurements [100], microphotoluminescence [101], micro-Raman spectroscopy and infrared thermography [102]. It was reported that efficient device design and packaging have a significant impact on thermal management. Notably, the substrate has a major role as it is the main heat removal path connecting the device to the package heat sink. Thus, for more efficient heat management, a higher thermal conductivity substrate is required. For that reason, SiC is considered the most appropriate substrate material when compared to Si and Sapphire since it has a superior thermal conductivity. However, extraction of heat can also be done from the top of the device by coating it with high-thermal conductivity materials such as diamond [103].

#### 2.2.5.4 High-temperature GaN generations

As they already provide reliable contacts, interconnections and packaging, the III-N semiconductors are suitable candidates for high ambient temperature. However, the major obstruction of these devices is represented by charge trapping effects. The latter is a function of operation temperature and adversely affects the electrical characteristics of the device. Although junction devices (p-junctions) are possibly reliable for high temperature, the Insulated-Gate Field Effect Transistors (IGFETs) are favorable for practical electronic system implementation.

To obtain reliable high temperature IGFETs, gate insulating material should maintain adequate insulation and interfacial characteristics at the targeted high-temperatures (300 $^oC$-600 $^oC$) and high-electric field stress. However, such properties high quality insulating materials are extremely difficult to obtain with III-N semiconductors.

While the high-temperature operation of III-N IGFETs exceeding 600 ºC has been demonstrated [104], long-term operation at such operation temperature still demands more improvements in the gate insulation ability due to two essential defections. The first one is the insufficient insulation properties which lead to undesirable charge leakage from the device channel. This leakage may change the threshold voltage ($V_T$) of the IGFET by creating traps in the insulator. Adding the degradation mechanism to insulator carrier leakage, these two defects are undesirably accelerated with higher operation temperature. Secondly, in case of GaN device, the undesirable electric charges at the interface of the semiconductor and insulator have higher densities negatively leading to fragile channel mobility (μ). This, in terms, damages the electrical performance of the IGFET [61].

Aiming to improve the III-N IGFET devices, research efforts have focused on alternative insulation materials and improved processing. However, compared to the advanced reliability and performance of $Si/SiO_2$ MOSFET devices even at low operation temperature, massive challenges should be overcome until the III-N IGFETs can be considered as acceptable devices with proper functionality for operation ambient temperature well beyond 500 ºC.

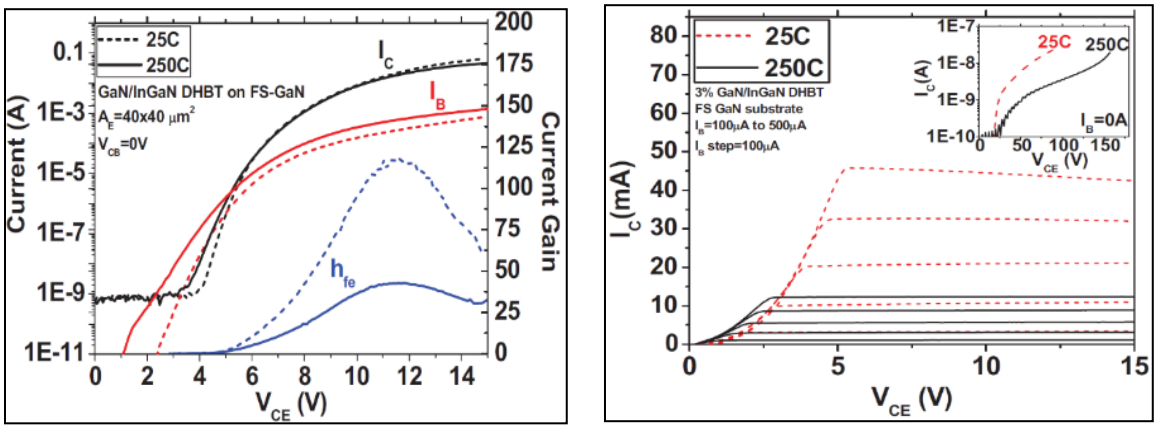
#### *2.2.5.4.1 GaN HBT*

Compared with FET devices, GaN based HBTs provide better options for RF applications. They offer significant advantage from the IC manufacturing point of view. They rely on uniform turn on characteristics and are convenient for current amplification and impedance matching for high-power applications. Also, GaN HBTs offer important benefits in harsh environments subject to high total dose of radiation, corrosive and particularly extreme temperature applications.

Many researches focused on AlGaN/GaN HBTs aiming to provide junction transistors [105], [106]. However, only marginal improvements were reported. The limited success appears related to the unavailability of low resistance base layers, combined with limited fabrication techniques, and shortage in high crystalline quality epitaxial structures and low defect density substrates. Moreover, a fundamental factor in GaN HBT devices is the low free hole concentration in p-type epitaxial GaN layers that introduces serious emitter crowding effect. This deficiency is treated in GaN/InGaN HBTs by utilizing InGaN base layer aiming to minimize the resistances of base sheet and p-type contacts [107].

Some researchers have tried to reduce etching deteriorations in the base layer by using an epitaxial regrowth approach in npn GaN/InGaN HBTs [108]. The response of GaN HBT was studied between room temperature and 250 $^{o}$C to investigate the performance of this device at high temperature [109]. This Double Heterojunction Bipolar Transistor (DHBT) was grown on a Free State (FS) 40 x 40 $\mu m^2$ GaN substrate. When the temperature increases from room temperature to 250 $^{o}$C, the device gain current is reduced from 115 to 43 respectively as shown in Figure 2.15(a). The current reduction was related to a reduced emitter injection efficiency and a higher recombination rate introduced by Mg ionization and free-hole concentration in the base.

Similarly, the $I_C - V_{CE}$ characteristics in Figure 2.15(b) show a drop in the knee voltage from 5.2 V to 2.75 V for $I_B$ = 500 µA in addition to a reduction of the offset voltage from 0.8 to 0.3 V. The knee voltage and offset voltage reduction are due to the drop in base resistance at high temperature. Moreover, as the temperature increases to 250 $^{o}$C, the breakdown voltage $BV_{CEO}$ is shifted from 90 to 157 V, which highlights the dominant role of the impact ionization process on GaN/InGaN HBTs. In the case of pnp AlGaN/GaN HBTs, it is reported that these devices can endure operating temperatures of 590 $^{o}$C with current gain = 3 [110]. Considered globally, these results confirm that GaN HBTs can operate at extreme operating temperatures.

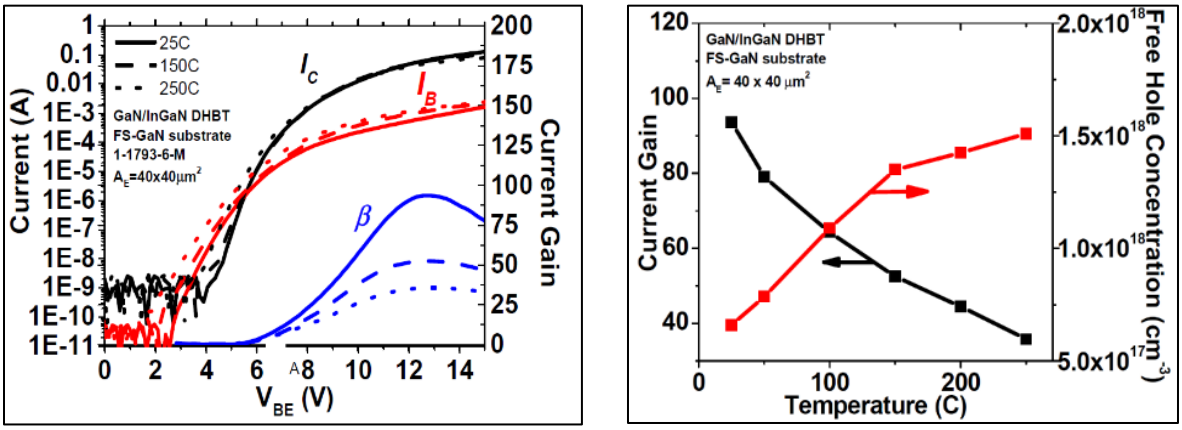



(a) (b)

Figure 2.15: DHBT grown on a GaN substrate, a) Gummel plot, b) Common-emitter characteristic [109]

A high performance of InGaN npn HBTs has been reported in [111]. This device was grown on a sapphire substrate by MOCVD and it showed high collector current density ($J_C$), low knee voltage ($V_{knee}$), low offset voltage ($V_{offset}$) and high $BV_{CEO}$ characteristics. In the same work, another

InGaN HBT was grown on free-standing GaN substrate. This device showed reduction in peak current gain from 93 at 25 ºC to 35 at 250 ºC (see Figure 2.16(a)) in addition to higher free-hole concentration as shown in Figure 2.16(b) leading to base resistance and $V_{knee}$ reduction.



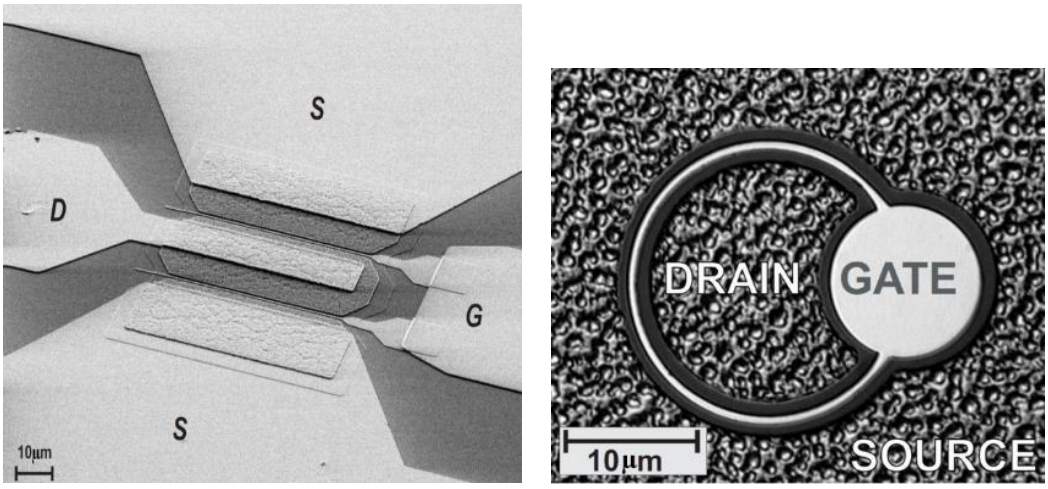

(a) (b)

Figure 2.16: A measured Gummel plot of the DHBT at different temperatures, b) Measured current gain ($\beta = I_C / I_B$) and free hole concentration ($p$) calculated from $1/C^2$ v.s. $V_{BE}$ curve fittings at different temperatures from 25 to 250 ºC [111]

### 2.2.5.5 Recently developed devices:

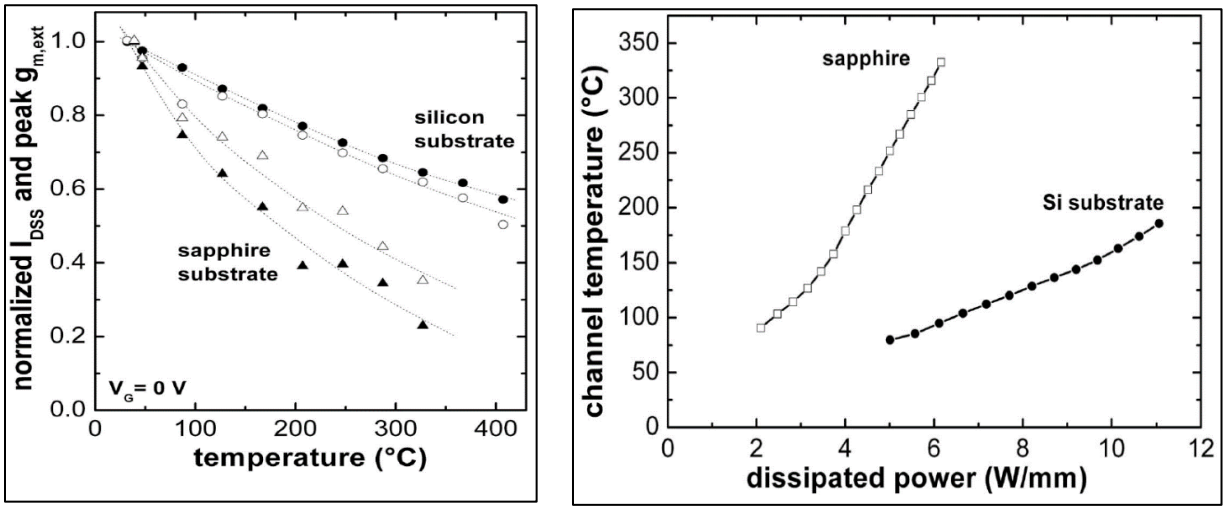
The fabrication processes and the characterization of AlGaN/GaN HEMT devices (depicted in Figure 2.17(a)) are discussed in [59]. These processes used sapphire and silicon substrates. The ohmic contacts reported in that work are multilayered Ti/Al/Ni/Au contacts annealed at 900 ºC and the Schottky contacts are Ni/Au metal layers. Three etching techniques are investigated: RIE ECR (reactive ion etching with electron cyclotron resonance), photochemical etching and Ion beam etching. The latter, using Ar+ ion sputtering, is more reliable and leads to a better controlled process, smooth surfaces, sharp edges, well defined sidewalls and an etching rate of 30nm/min. The HEMT on sapphire substrate was optimized by RoundHEMT technology (depicted in Figure 2.17(b)).

As plotted in Figure 2.18(a), the degradation of maximum saturation drain current ($I_{DSS}$) and peak extrinsic transconductance ($g_{m,ext}$) increase with temperature for both sapphire and silicon substrate devices. In parallel, the study of self-heating effects shows higher temperature dissipation in the channel of sapphire substrate device when compared to the one observed in devices built over silicon substrates as plotted in Figure 2.18(b).




a) b)

Figure 2.17: a) Photograph of a AlGaN/GaN HEMT. Three ohmic contacts (drain D and source S) and two finger Schottky contacts (gate G) at the top of the mesa are placed, b) Simple RoundHEMT layout with ohmic contacts (source and drain) and Schottky contact (gate) [59]



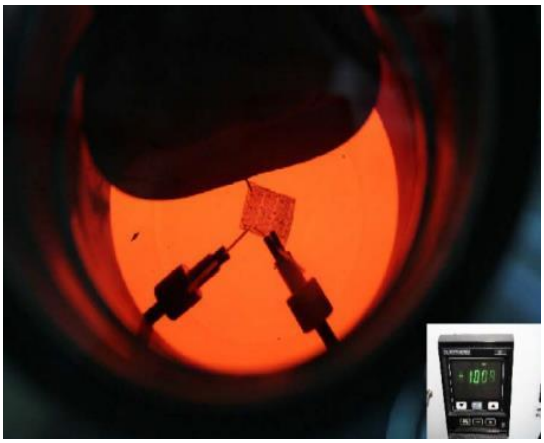

(a) (b)

Figure 2.18: AlGaN/GaN HEMTs on Si and sapphire substrates: a) Temperature dependence of $I_{DSS}$ and peak of $g_{m,ext}$ normalized to their room temperature values, b) Dissipated power-to-channel temperature transfer characteristics [59]

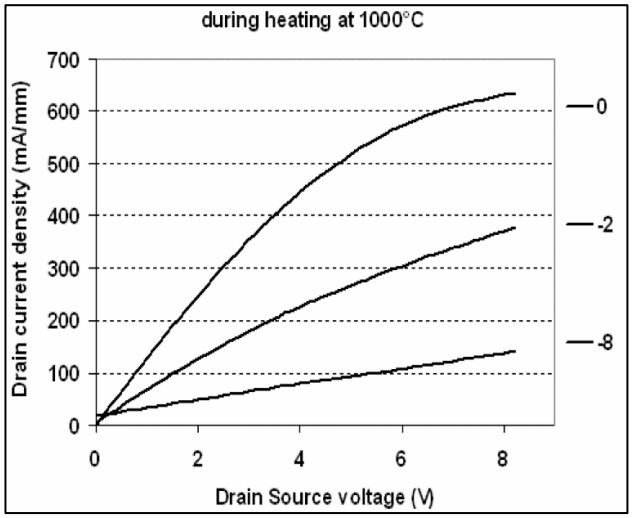
In addition, the influences of doping density of an AlGaN carrier supply layer combined with an AlGaN barrier layer or various thickness are studied in [59] along with their impacts on the electrical properties. By reducing the gate length and source to drain distance, the device

performance is improved due to the reduction in source and gate resistance. However, due to its poor thermal conductivity, the sapphire substrate is not suitable for high power and high temperature applications. The AlGaN/GaN RoundHEMTs (depicted inFigure 2.18(b)) on silicon substrate shows better performance at higher temperature (320 $^{o}$C) and high power (6 W/mm). The DC and RF performance of this device increased with the doping density. It was observed that $Si_3N_4$ passivation has better impact than $SiO_2$. It improved the DC and RF performance, the 2DEG concentration and the output power density.

A novel AlInN/GaN HEMT is presented in [20] as an alternative of AlGaN/GaN. The performance of this device with 0.25 µm and 0.15 µm gate lengths is discussed. The reported measurements indicate a surface more stable than in AlGaN/GaN devices in addition to high-chemical stability at temperatures of 1000 $^{o}$C in vacuum as shown in Figure 2.19. The key solution, as depicted in Figure 2.20, is to insert a thin AlN interfacial layer between a thick GaN buffer and a thick undoped AlInN barrier layer resulting in high mobility, low sheet resistance and high sheet charge density. The device is grown using an AIXTRON Metalorganic Vapor Phase Epitaxy system on 2-inch diameter sapphire substrate. The ohmic contacts with this technology are obtained from a Ti/Al/Ni/Au metal sequence annealed at 890 $^{o}$C. Ni/Au Schottky gates and contacts are defined by e-beam lithography.



(a)




(b)

Figure 2.19: 0.25 × 50 µm$^2$ AlIn/GaN HEMT device tested at 1000 $^{o}$C: a) Sample under test, b) I-V characteristics where $V_{GS}$ is swept from -8 V to 0 V by steps of 4 V [20]

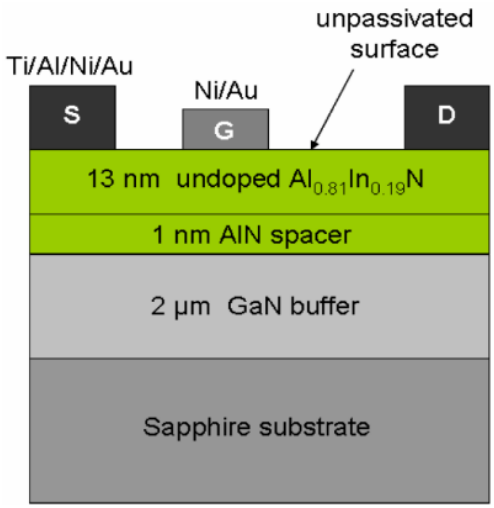



Figure 2.20: Schematic cross section of an AlInN/GaN HEMT structure [20]

Between 2009 and 2011, the MORGaN project [112] was an extension of UltraGaN project launched in 2005 under the FP6 (FET-IST) program [113]. MORGaN focused on InAlN/GaN as a candidate for extreme environment applications [114], [19, 115-118]. Investigating the availability of GaN growth on polycrystalline diamond and Si substrates, MORGaN provided the first European demonstration of 2-inch wafers. Moreover, the same team had already demonstrated the first AlGaN/GaN HEMT with direct growth on '111' single crystal diamond, in addition to the first InAlGaN HEMT grown on 2-inch free standing wafers using a substrate combining 2 µm of '111' silicon grown over a 70 µm polycrystalline diamond layer. Also, they had successfully developed diffusion barriers for Ti/Al ohmic contacts dedicated to HEMTs and harsh environments (800 $^{o}$C). Multilayer structures of TiN/TiSiN (Cu mounting layer coverage) and ZrN/$ZrB_2$ (Au mounting coverage layer) were investigated and realized.

In [103], significant work on fabrication and characterizion of InAlN/GaN HEMT devices was reported. A nanocrystalline diamond (NCD) coated lattice matched (LM) InAlN/GaN technology is proposed to solve the self-heating device problem. Due to the high lattice mismatch, AlN suffers serious limitations with respect to mechanical stability that makes it unfavorable for NCD overgrowth. However, InAlN possesses better matching of grown lattice over a GaN buffer layer with 83% of Al content. This avoid mechanical stability issues and preserve a high density of the 2DEG taking into account the larger polarization discontinuity with the buffer layer. Investigating the performance and limitations of the LM-InAl/GaN HEMT, the results showed an interesting high thermal stability of the device. This leads to accept uncommon treatment of HEMT inherent

limitations such as current collapse and gate leakage by utilizing thermal oxidation of the LM-InAlN which, in terms, appears as a perfect surface passivation component.

Preliminary testing at 800 $^{o}$C ensures the compatibility of NCD growth with the HEMT capability while observing degradation in metallization and passivation. The optimization is done by Diamond growth process developing Diamond coated HEMT devices (Figure 2.21(a)) capable for continuous operation at 1000 $^{o}$C (Figure 2.21(b)). Additional improvement can be achieved with this HEMT structure to sustain higher temperature. The observed degradations were not in the transistors but only in other peripheral elements such as metallization and passivation.

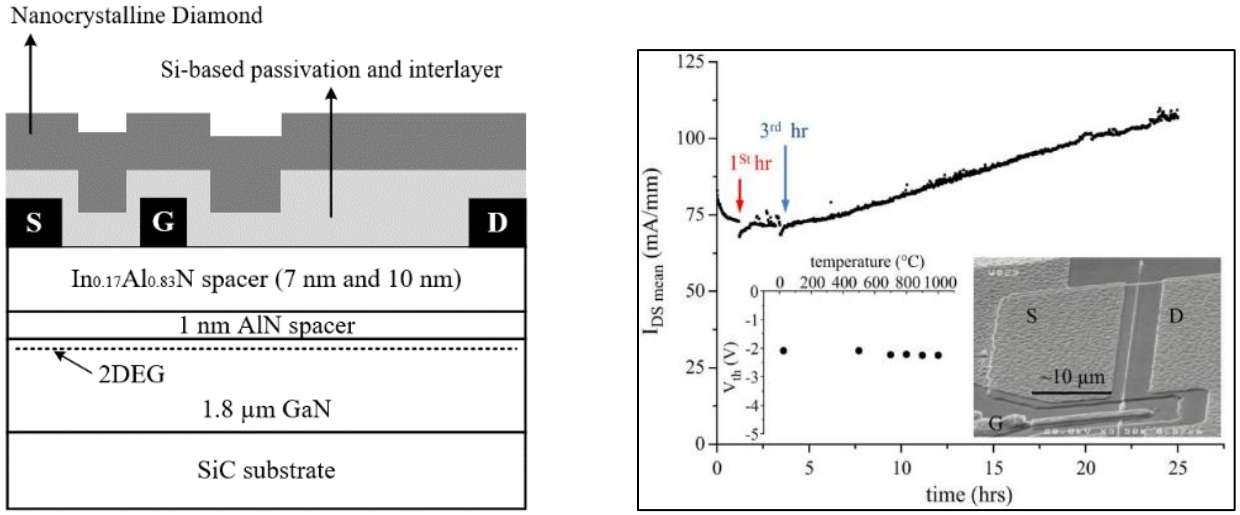



Figure 2.21: a) Cross section of NCD overgrown $In_{0.17}Al_{0.83}N$/GaN HEMT [115], b) Evolution of the mean drain–source current ($I_{DS,mean}$) with test time. (Inset left) Evolution of threshold voltage ($V_{th}$) from RT up to 1000 $^{o}$C. Small changes above 600 $^{o}$C can be attributed to a slight increase in the gate diode leakage current. (Inset right) SEM picture of the device, SiN passivation removed, after 25 h testing at 1000 $^{o}$C. No visible damage can be observed [114]

Aiming to increase NCD films thickness, the overgrowing was performed with no other changes besides the omission of Cu from ohmic contacts that was used as gate metal only. At storage temperature of 1000 $^{o}$C, Cu diffuses into the $Si_3N_4$ passivation layer, thus inducing conduction paths on the surface that eventually lead to short circuits between contacts.

To solve the situation, Mo or Pt replaced the Cu and the deposition conditions of PCVD $Si_3N_4$ was regulated. The following step was the deposition of the bias enhanced nucleation (BEN) interlayer

system and a NCD layer approximately 3 µm thick obtained after 28 hours of growth at 750 ºC. After that, in-situ $Si_3N_4$ was used as an alternative to the PCVD $Si_3N_4$ showing convenience for high power GaN devices.

Another alternative was the utilization of an $Al_2O_3$ layer obtained by atomic layer deposition (ALD) that showed high thermal stability. This passivation layer is good in MOSHEMT as it allows improving the gate diode stability at high ambient temperature by considerably lowering the gate leakage. As proposed future work, the single crystal Diamond substrate can be integrated with the top NCD coating layer leading to Diamond encapsulated GaN HEMT devices with exceptional heat extraction capability and durable surface.

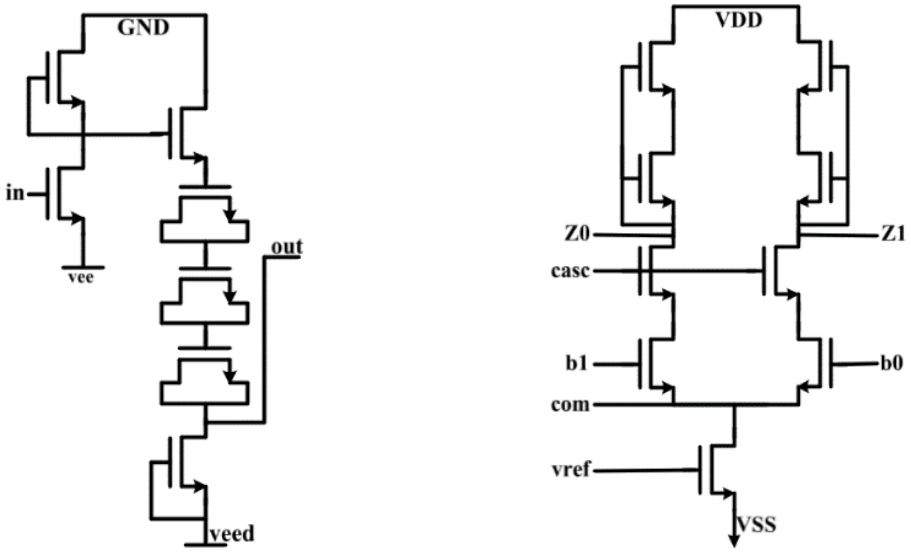
A homojunction vertical GaN PIN rectifier was characterized at various temperatures [119]. The device was fabricated on a free-standing GaN substrate and tested from room temperature up to 175 ºC with free carrier concentration of $2x10^{16}$ $cm^{-3}$. The positive impact of a thin layer of $Gd_2O_3$ gate dielectric on an AlGaN/GaN MOSHEMT was demonstrated in [120]. The device was grown on a silicon substrate and tested at 500 ºC, where reported results show lower gate leakage current and stable DC performance when compared with conventional AlGaN/GaN HEMTs. Moreover, it was concluded that the thermal stability of GaN with this $Gd_2O_3$ dielectric layer could be enhanced by a soft thermal annealing process.

#### 2.2.5.6 GaN implementation:

Despite the suitability of GaN technology for HT environment, limited integrated circuits and sensors are implemented based on GaN devices for HT applications [13], [21, 22]. In [22], a 31-stage ring oscillator, frequency dividers, several logic gates, and a comparator as shown in Figure 2.22 have been implemented based on GaN/AlGaN HFET device and tested at 300 ºC. Another work [21] presents an AlGaN/GaN-based inverter grown on sapphire substrate by MOCVD and integrated with depletion mode HEMT and enhanced mode MOSFET. The inverter is characterized at high temperature between room temperature and 300 ºC. The relative variations of voltage swing, threshold voltage, logic-low noise margin and logic-high noise margin are respectively 2.2%, 5.7%, 12.9% and 4.9% from RT to 300 ºC.

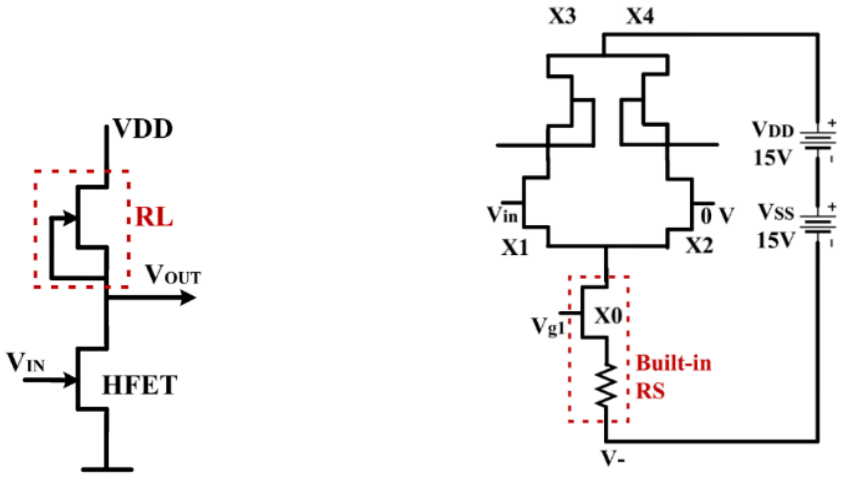
Novel AlInN/GaN integrated circuits had been demonstrated in [13] operating at 500 ºC. The fabricated inverter and differential amplifier (shown in Figure 2.23) were tested at 500 ºC showing stable performance with internal response time 45 ns and unit-gain bandwidth above 1 MHz. High-

K passivation/gate dielectrics and new metallization scheme sustainable at high operation temperature are the main advancements in that work. Mo/Al/Mo ohmic metal stack was utilized to solve the problems of Ti/Al/Ti/Au ohmic contact and Ti/Au interconnect at high operation temperature of 500 ºC.




(a) (b)

Figure 2.22: Schematic of GaN HFET-based digital circuits. (a) Inverter block used in ring oscillator, and (b) Comparator [22].




(a) (b)

Figure 2.23: Schematic of GaN HFET-based integrated circuits. (a) Inverter, and (b) Differential amplifier [13].

Table 2.5: Extreme environment semiconductors comparison

| **Extreme environments electronics** | | | | |
|---|---|---|---|---|
| **Tech.** | High temp. | Low temp. | Intense Rad. | Availability |
| **Si** | - | + | - | + |
| **SOI** | + | + | ++ | + |
| **SiGe** | + | ++ | ++ | + |
| **SiC** | ++ | + | ++ | - |
| **GaN** | ++ | ++ | ++ | - |

Table 2.6: Foundries of harsh environment electronics

| **Reference** | **Tech.** | **Foundry** | **Type** |
|---|---|---|---|
| **[30, 34]** | SOI | Honeywell | CMOS 0.8um |
| **[25]** | SOI | N/A | 0.8um BCD on SOI process |
| **[26]** | SOI | N/A | CMOS 0.13um |
| **[28]** | SOI | N/A | MESFET 0.6um |
| **[29]** | SOI | N/A | MESFET 0.15um |
| **[31], [33], [34], [35]** | SiGe | IBM | SiGe HBT |
| **[36]** | SiGe | NASA | SiGe HBT and SiGe BiCMOS |
| **[37]** | SiGe | IBM | 0.12um SiGe BiCMOS8HP |
| **[38], [39]** | SiGe | NASA | 0.5um SiGe BiCMOS |
| **[40], [41]** | SiGe | IBM | 90nm SiGe HBT BiCMOS |
| **[12]** | SiC | Cree Inc. | 4H-SiC JFET |
| **[44], [45]** | SiC | NASA | 6H-SiC JFET |
| **[43]** | SiC | GE | 4H-SiC BJT |
| **[46]** | SiC | Raytheon | 4H-SiC CMOS |
| **[48]** | SiC | Raytheon | 1.2um SiC CMOS |
| **[49]** | SiC | N/A | SiC JFET |
| **[51]** | SiC | N/A | 4H-SiC MOSFET |
| **[50]** | SiC | Cree Inc. | SiC MESFET |
| **[11]** | SiC | Cree Inc. | 4H-SiC MOSFET |
| **[17]** | GaN | N/A | GaN/InGaN DHBT |
| **[110]** | GaN | Cree, Sumitomo and RFMD | GaN HEMT |
| **[114]** | GaN | III-V Lab | 0.25um InAlN/GaN HEMT |
| **[21]** | GaN | N/A | AlInN/GaN HFET |
| **[13]** | GaN | HRL Lab | AlGaN/GaN HFET |

*N/A: Mainly in-house fabrication or unknown

Recently, a team at the Polystim Neurotechnologies Laboratory [121] is investigating the possibility to develop microelectronic systems for harsh environment based on AlGaN/GaN HEMT

[122-125]. Some preliminary results showed relatively stable characteristics of GaN devices tested at temperatures ranging from room temperature to 400 ºC. By completing the development of robust models for the desired GaN device, the next step is directed towards implementing wireless power and data transmission systems dedicated to aerospace harsh-environment applications.

Table 2.5 provides a summary for the developed extreme environment electronics technologies so far, and Table 2.6 lists the main foundries where most of the discussed harsh environment devices and implemented circuits were processed. As it is shown, standard silicon is only suitable for low-temperature applications. However, the silicon on insulator (SOI) is better for intense radiation environment. Silicon germanium (SiGe) is mostly appropriate for low temperature and intense radiation application. Silicon carbide (SiC) and gallium nitride (GaN) are great candidates for all the extreme environments however they are still not commercially available.

### 2.2.6 Contacts

The conductive contacts functionality at high temperature is not less important than that of semiconductor itself. The reliability of contacts metallization and interconnects between the on-chip devices presents a substantial challenge for devices dedicated to operating in high-temperature conditions particularly for applications beyond 400 ºC. The generated self-heating during operation in addition to the surrounding high temperature provoke contact degradation and limit the long-term reliability of these devices.

One of the notable failure mechanisms at high temperature is the electromigration process, where the current flowing into a conductor conducts to a bulk motion of the material and leads to open circuit. Depending on the current density and temperature, the time to failure for a conductor can be described by Black's equation (equation (2.8)),

$$t_{Fail} = Aj^{-n}e^{E_a/kT} \quad (2.6)$$

where $t_{Fail}$ is the mean time to failure, $A$ is the specific coefficient of a metal process, $j$ is the current density, n is a coefficient typically between 2 and 3, and $E_a$ is the thermal activation energy. As noticed from the equation, the lifetime of conductor is quickly decreasing with function of temperature and current density. The current density should be addressed by designers to limit it. On the other hand, for operating temperature more than 200 °C, the reliability issue of devices and corresponding conductors must be addressed.

Aluminum conductor is widely utilized in Si chips; however, it fails for temperature above 200 °C due to electromigration after few thousand operating hours and above 300 °C in hundreds of hours. In GaAs circuits, gold is commonly used with need of burrier metals and adhesion layers. Comparing with Al, gold is more resistant to electromigration. However, it alloys with diffusion barrier and adhesion layer at high temperature causing a large increase in resistance and consequently affects the device and circuit performance. In parallel, tungsten is much more resistant to electromigration than Al and used as a conductor.

Another critical issue at high temperature is the failure possibility of interface between different materials due to diffusion, chemical reactions and other metallurgical reactions. Consequently, there is a need to develop thermodynamically stable interfaces. In addition, mechanical stresses could be applied to the interfaces because of thermal expansion coefficient mismatches. Also, at extremely high-operating temperature (>600 $^{o}$C), it would be necessary to take into consideration the degradation of p-n junctions and diffusion of dopants.

The interface stability issue has been solved by utilizing layers of materials. It is done by adding the ohmic and Schottky contacts to the semiconductor devices, followed by a diffusion layer to separate the contacts from the high electrical conductive interconnect layer as described in Figure 2.24. The contact material, such as silicide, should ensure the completion with the semiconductor and maintain relatively high electrical conductivity. The diffusion layer must be inert to the interconnect metal and to the contact. The way of preparing this layered structure (contact-diffusion barrier-interconnect) is as important as the choice of the materials. The utilized processing techniques has a direct impact on the metallurgical properties, which in terms affect the diffusion rates and intermetallic formation due to chemical reactions between the layers. For devices operating at extremely high-temperature, one of the main challenges is to develop such a stable structure of multilayer metallization systems.

Great efforts have been done toward developing ohmic contacts to SiC for high-temperature applications. In [126], TiW-based contacts with aluminum interconnect was successfully tested over 500 hours at 400 $^{o}$C. Similarly, Ti/$TaSi_2$/Pt multilayer contact to n-type SiC shows stable ohmic properties for 1000 hours of annealing at 600 $^{o}$C [127]. More studies are necessary to obtain similar results for p-type SiC.

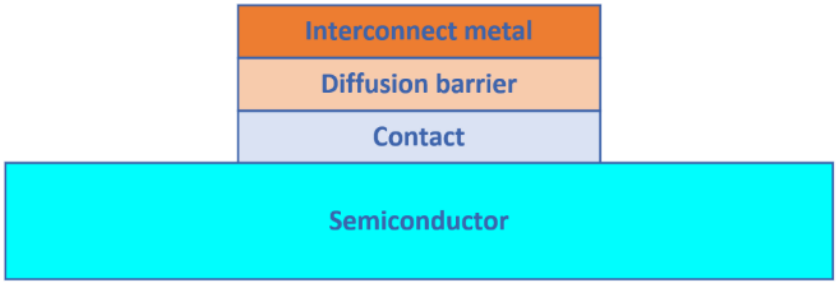



Figure 2.24: Proposed structure for making contacts in high-temperature devices

Table 2.7: Contacts and metallization types of presented devices

| Device | Reference | Interconnect and contact |
|---|---|---|
| **SOI** | [25] | Oversized interconnect + multiple pad connections +N/A |
| | [26] | N/A |
| | [27] | TiN/Al |
| | [28], [29] | Silicon/silicide/metal |
| **SiGe** | Other references | N/A |
| | [40] | n-well and p-sub contacts |
| **SiC** | Other references | N/A |
| | [43] | Ti/Ni/TiW/Cr |
| | [44] | Ti/Al/Ti/Au |
| | [45], [46] | $TaSi_2$/Pt |
| | [47] | P-WELL contacts |
| | [11] | Ni/Ti/W/Ti/Ti/Al (ohmic contact) + W/Ti/W/Ti/Ti/Al (gate contact) |
| | [52] | Ni (ohmic contact) + Al (gate contact) |
| **GaN** | Other references | N/A |
| | [128] | Ti/Al (ohmic contact) + Ni (gate contact) + Ti/Au (interconnect layer) |
| | [109] | Ti/Al/Ti/Au (emitter and collector contacts) + Ni/Au (base ohmic contact) + Ti/Au (interconnect layer) |
| | [110] | Pd/Au (p-type layer) + Al/Au (n-type layer) |
| | [114] | Ti/Al/Ni/Pt (ohmic contact) +Mo (gate metal) |
| | [129] | Ti/Al/Ni/Cu/Ti/Pt (ohmic contact) + Cu/Pt/Cu/Ti/Pt (gate metal) |
| | [13] | Ti/Mo/Al/Mo/Ni/Au (ohmic contact) + Ti/Ni/Au/Ni (interconnect) |

N/A*: Type not mentioned in the related reference

Ti/Al/Ni/Au low resistance ohmic contact has been studied in [71] between 25 ºC and 600 ºC for n-type GaN. On the other hand, the Schottky contact of n-GaN Ni/Au, Ni/Pt/Au, Pt/Ni/Au and Pt/Ti/Au has been investigated in [72] up to 400 ºC. In parallel, a novel Mo/Al/Mo metal stack is introduced in [13] to improve the robustness of ohmic contact at high temperature reaching 500

$^{o}$C. A high-K dielectric is deposited to provide Schottky contact showing stable dielectric permittivity through wide temperature range in addition to the decreasing of the breakdown voltage and leakage current.

Due to the difficulties of realizing conductive p-type GaN layers, obtaining highly stable contacts of this material presents as serious challenge so far. Additionally, more studies are still needed to investigate the reliability of GaNs ohmic contact in presence of electromigration and chemical reactions with applied electrical bias at oxidizing high temperature more than 400 $^{o}$C. Thus, radical challenges in GaN contacts must be surmounted to enable this device to support long-term operation in real environment and at high temperature more than 600 $^{o}$C.

Table 2.7 summarizes the utilized contacts and metallization systems of the presented harsh environment devices in the previous sections (SOI, SiGe, SiC and GaN).

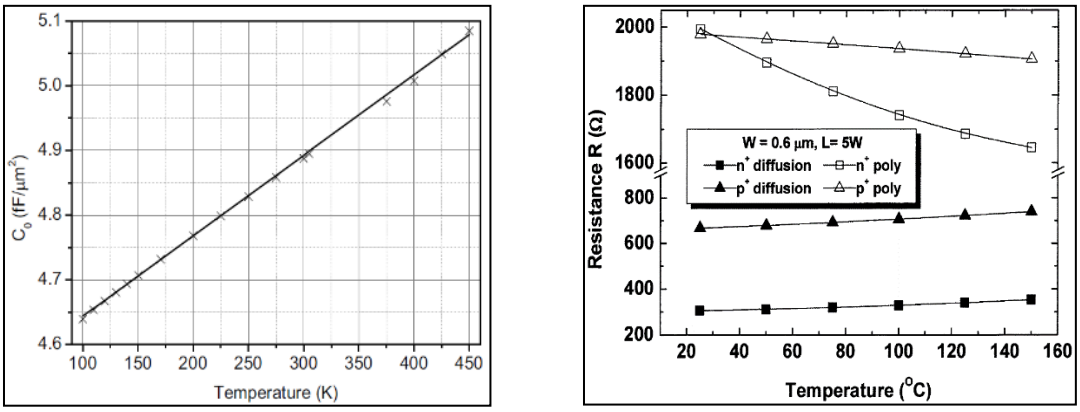
### 2.2.7 Passive components

The microelectronic devices dedicated for operating in extreme environment conditions have been developed to sustain such harsh conditions, such as SiGe technology for cryogenic conditions, SiC and GaN for high temperature applications and SOI for intense radiation environment. These pioneering technologies support the transistor level of microelectronic systems to endure the harsh environments, while the integrated passive components are not well designed for such extreme conditions. Therefore, it is deeply needed to investigate the passive components responses with the variations of applied environment conditions.

Military passive components operable temperature range is usually −55 °C to +125 °C. The measurement of variation in component value is commonly reported by temperature coefficient in ppm/°C. The discrete passive components performance was characterized at extreme low temperature. It was noticed that commercial components suffered significant variations in value when the temperature falls below −50 °C. However, similar studies confirmed the capability to provide discrete passive components able to operate successfully at -200 °C [130].

On the other hand, the on-chip passive components integrated on silicon platforms have low temperature operation limits as well, where the minimum temperature of Mil-Spec range is only −55 °C. However, different related researches [131] have successfully performed a wide range of operational temperature (−180 °C to +120 °C) for integrated passive components.

Similar study on monolithic MIM capacitors investigates their behavior for wide temperature range (−173 °C to +177 °C) [132]. Figure 2.25(a) shows a linear relation between the capacitance values with the temperature variation. The total chance of capacitance across the full 350 °C temperature range is about 10%. In another research [133], the impact of temperature on both polysilicon and diffused resistors has been investigated. As shown in Figure 2.25(b), it is noticed that the polysilicon resistors have a negative temperature coefficient which differs with doping type difference. In the opposite side, the diffused resistors have a positive temperature coefficient. Recent review [23] summarizes the available high temperature commercial capacitors with temperature limit of 260 $^{o}$C and commercial resistors with 350 $^{o}$C.




(a) (b)

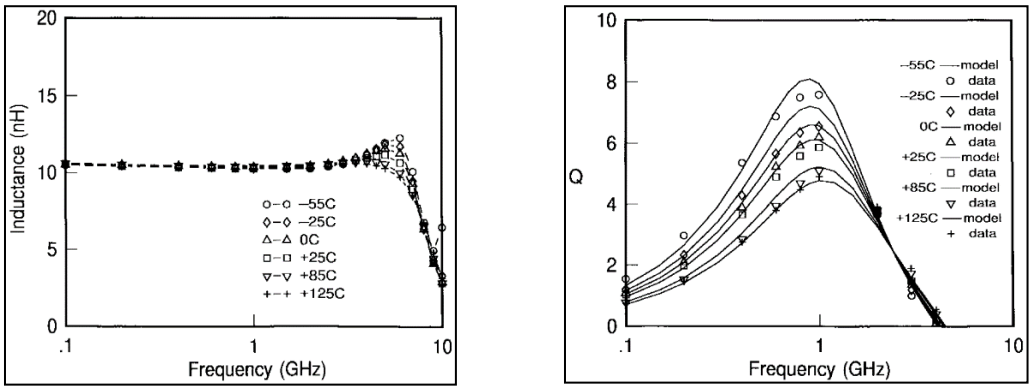
Figure 2.25: a) Modeled vs measured data for MIM capacitors [132], b) Resistance vs temperature range [133]

Another important integrated passive component to be investigated and study its response with the temperature variation is the inductor. Several researchers examine the effect of temperature on both inductance and quality factor (Q) of monolithic inductors [134]. A slight variation of inductance in terms of temperature range −55 °C to +125 °C for an on-chip spiral inductor printed in a SiGe platform has been revealed as shown in Figure 2.26(a), whereas Figure 2.26(b) indicates an improvement in Q along with temperature decreasing. The latter has been confirmed by modeled and measured tests.

A discussion of the strong temperature dependence of *Q* explains the two mechanisms at work. The aluminum metallization of the inductor has a positive TCR (temperature coefficient of

resistance) which makes the inductor loses more as temperature increases, but the substrate resistivity also increases with temperature, resulting in less substrate loss.

For the applications beyond the 250 $^{o}$C step, most of the commonly used soft-magnetic cores become paramagnetic where the inductors lose their magnetic properties. Therefore, new ferrite materials have been developed with Curie temperature more than 350 $^{o}$C to overcome this issue [135].




(a) (b)

Figure 2.26: a) Measured inductance versus frequency, b) Modeled and measured Q versus frequency [134]

The radiation studies are mainly focusing on microelectronic devices such as CMOS and bipolar transistors. However, less effort has been applied to investigate the impact of radiation on the passive components usually connected with the active devices and significantly affect the functionality of overall microelectronic system. The radiation effects, as mentioned before, can be distributed into three main phenomena: Total ionizing dose (TID), displacement damage (DD) and single-event effects (SEE). The passive components have no response for the TID due to the absence of the sensitive regions.

Nevertheless, the TID damage may appears as an increment of substrate coupling from the layers under the inductor, or as a deteriorated MIM capacitor dielectric. DD can affect the passive components by changing the resistivity of a resistor or modifying substrate coupling of an RF inductor. To quantify the impact of TID and DD on on-chip passive components, several researches have been done by exposing the passive elements to high proton flow [136-138]. The results of these studies indicate negligible variations in the passive elements values. Regarding the SEE effect on the passive elements, a CMOS capacitor could be ruptured (fatal event), or charge might

be added to a diffused region of a resistor by an ion strike with enough energy. Several studies have been performed to examine the influence of SEE on the passive elements [139-142].

### 2.2.8 Packaging

The electronic single chip and multichip packaging including the electrical, thermal, mechanical and physical implementation has many serious challenges when the packaged electronic system is dedicated for extreme environments, especially extreme temperature applications [143], [125], [124].

For the low-temperature electronics, the variation of material characteristics is the principal defy of packaging. For example, the modulus of elasticity is increasing for polymers and metals, the coefficients of thermal expansion (CTES) is decreasing, the elongation is decreasing for metals and polymers, the phase transitions in metals and solders is affected, and the thermal conductivity for metals and ceramics is increasing [144]. Certain studies have been performed to investigate the reliability of thin-film multichip and chip on board (COB) packaging devoted for extreme low and wide range temperature applications (-180 °C to +125 °C) [145-147], evaluating the materials of substrates, die attach, encapsulant and wires. It is needless to say that the low temperature packaging is a specialized domain limited in information and still need more investigation about the appropriate materials and reliability of different packaging approaches.

On the other face of extreme temperature applications, the high temperature electronics packaging has faced several serious challenges like the melting of solder alloys, damage and cracking due to the coefficients of thermal expansion (CTE) differences, polymeric material decomposition, diffusion, intermetallic formation and creep. The substrate, die and substrate attach, wire bonding and packages are the principle sections of the packaging procedure. The recommended substrate types for high-temperature conditions are printed circuit board (PCB) based on polyimide laminates to sustain a temperature of 250 °C, thick film substrates using $Al_2O_3$ with maximum endurable temperature of 500 °C [148] and thin film substrates with highest affordable temperature of 300 °C [149] based on $Si_3N_4$ and Aluminum nitride (AlN). Other substrate types dedicated for high-temperature operation are the low-temperature cofired ceramic (LTCC) achieving 300°C [150], high-temperature cofired ceramic (HTCC) exceeding the gate of 225 °C [151], and copper foil on ceramic [152], where the researchers have demonstrated direct bond coper (DBC) on Aluminum oxide ($Al_2O_3$) for steady operation at 400°C.

Regarding the die and substrate attach materials, we can include five main categories dedicated for high temperature environments: the polymer-attach materials reaching maximum temperature of 250 °C [153], Ag-glass with similar endurable temperature as well [153], solders and brazers where high temperature soft solders at 200 °C has been evaluated successfully [154] and thermal cycling of +40 °C to 400 °C shows cracking within the braze layer [155], transient liquid phase (TLP) bonding with capability to reach 500 °C [156], and sintered nanoparticles capable to sustain 175 °C [157]. The wire bonding materials for high-temperature conditions are mainly Au, Al, Pt and Ni. The temperature limitations of several wire combination and pads are listed in Table 2.8 and Al wiring to thick film Au is evaluated in [158] at 300 °C. Au and Pt wire bonding materials are investigated in [159] at 500 °C.

The packaging materials used in consumer applications are mainly plastics with endurable temperature less than 175 °C, which is not suitable for high-temperature environments. Glass packaging materials are appropriate for 180 °C-220 °C of temperature range [160], whereas the silicon encapsulants are demonstrated to perform 250 °C for continuous operation [161]. For high-temperature conditions, metal and ceramic are normally the required packaging materials exceeding the edge of 400 °C [162], with higher temperature performance of brazed ceramic reaching 800 °C [163]. Another succeeded study has been demonstrated at 500 °C using prefired ceramic layers metalized with thick Au conductors [164].

Table 2.9 summarizes the essential parts of high-temperature packaging started by substrate, die and substrate attach, wire bonding and ended by types of packages including the temperature limits of the materials used in each part.

Table 2.8: Temperature Limitations for Various Wire and Pad Metallurgies

| **Pad-wire metals** | **Max. Temp. (ºC)** | **Limitation** |
|---|---|---|
| **Al-Au** | 175 | Intermetallic formation |
| **Ni-Al** | 300 | Kirkendal voiding |
| **Al-Al** | 350-400 | Decrease in mechanical properties |
| **Au-Au** | 500-600 | Decrease in mechanical properties |
| **Au-Pt** | 600-700 | Decrease in mechanical properties |

Table 2.9: Packaging materials and their temperature limits

| **Substrate** | | **Die & substrate attach** | | **Wire bonding** | | **Packages** | |
|---|---|---|---|---|---|---|---|
| Material | Temp | Material | Temp | Material | Temp | Material | Temp |
| HTCC | 225 °C | Sintered nanoparticles | 175 °C | Nickel | 300 °C | Glass | 220 °C |
| PCB | 250 °C | Solders | 200 °C | Aluminum | 300 °C | Silicon | 250 °C |
| Thin film | 300 °C | Polymer | 250 °C | Platinum | 500 °C | Metal & ceramic | 400 °C |
| Cu on ceramic | 400 °C | Ag-glass | 250 °C | Gold | 500 °C | Prefired ceramic | 500 °C |
| Thick film | 500 °C | TLP | 500 °C | | | Brazed ceramic | 800 °C |

### 2.2.9 Conclusion

The main harsh environment applications and the state-of-the-art of the established and emerging electronic technologies devoted for extreme condition applications are presented. The wide bandgap semiconductors, such as SiC and GaN, are presented as suitable candidates for extreme temperature applications exceeding the boundaries of 500$^{o}$C and 900$^{o}$C respectively. The packaging challenges are still limiting the applicability of developed technologies despite enhancing of many advanced packaging techniques with maximum endurable temperature of 500$^{o}$C for a defined time of operation. The harsh environment electronics topic and its corresponding assembly and packaging challenges are still forming hot research topics nowadays and the future will show great enhancing steps in these fields.

This review also summarized several significant recent developments of GaN devices as well as their use in harsh environments. In spite of the significant reported recent developments, the maturity of GaN technologies still limit their use in systems that must withstand harsh environments. On the road to maturity, further work is required to obtain integrated devices that are reliable at high temperature. Significant efforts are required to characterize and improve GaN fabrication processes.

# CHAPTER 3 ARTICLE 1: HIGH TEMPERATURE CHARACTERIZATION, MODELING AND CIRCUIT VALIDATION OF GAN500 HEMT UP TO 600 $^{O}$C

Ahmad Hassan, Student member, IEEE, Mostafa Amer, Yvon Savaria, Fellow, IEEE, and Mohamad Sawan, Fellow, IEEE

This article addresses the first objective of this thesis, namely the investigation and validation of GaN500 technology at HT. The manuscript was submitted to IEEE Transactions on Circuits and Systems I as a Regular Paper in March 2019.

## 3.1 Abstract

This paper is an important step toward the implementation of GaN-based integrated circuits (IC) and systems intended for high-temperature (HT) applications. We report significant progress in the development of extreme temperature IC technology based on wide bandgap (WBG) semiconductors, especially SiC and GaN. We present the implementation and characterization of epitaxial AlGaN/GaN Heterojunction Field Effect Transistors (HFETs) and of a set of integrated passive components available as part of the GaN500 technology. The AlGaN/GaN HFETs and passive components are remarkably stable, enabling operation above 500 $^{o}$C. The characterization results are used to extract HT models of the integrated HFETs and passive elements. These models are included in a design kit to capture the temperature effects on the design simulations. Four logic gates (NAND-2IN, NAND-3IN, NOR-2IN and NOR-3IN) are implemented and successfully validated. In addition, two voltage reference circuits and an inverter are tested at temperatures ranging from 25 $^{o}$C to 600 $^{o}$C.

**Index Terms:** High-temperature ICs, GaN500 HFET, High-temperature modeling.

## 3.2 Introduction

Electronics for harsh environments has become a popular research topic in recent years [10] due to three main factors: 1- The necessity of more robust and reliable electronics for industrial

applications, 2- The limitation of traditional silicon in high-temperature and high-voltage conditions, and 3- The evolution of substrate materials that can sustain harsh conditions in industrial applications. Many applications, such as combustion engines, hybrid vehicles, aerospace, and deep earth drilling, need electronics operating at extreme temperatures and that is also capable of enduring high system voltages [165]. While silicon is used as the conventional Integrated Circuit (IC) material for most applications, its use in harsh applications is limited by its maximum operating temperature (<170 $^{o}$C for diode-junction isolated Si and <300 $^{o}$C for silicon on insulator) [25].

The development of new substrate materials, such as gallium arsenide (GaAs), silicon carbide (SiC), and gallium nitride (GaN), accelerates the proliferation of ICs usage in harsh environmental applications. Particularly, the two wide bandgap materials, SiC and GaN are well equipped to withstand high temperatures and high system voltages [166], [61]. The bandgap of these materials (> 3 eV) is almost three times that of bulk Si (1.1 eV), which makes the leakage current in devices exploiting wide bandgap (WBG) materials much lower at extreme temperatures. In addition, the electric breakdown field of WBG devices is six times larger than that of silicon, allowing them to withstand much higher system voltages.

While GaN is found to be an excellent candidate in high-frequency and high-voltage applications, SiC has three times the thermal conductivity of GaN or Si, allowing the heat generated in the circuit to be dissipated more easily [167]. On the other hand, in recent years, GaN Heterojunction Field Effect Transistors (HFETs) have been extensively studied for power and high-frequency applications. The same material properties of the GaN HFET heterostructure that make it attractive for high-power and low-noise applications, namely the high breakdown field, wide band-gap, and high saturation velocity, make GaN a very promising material for high-temperature electronics [166].

Combining the excellent thermal conductivity of SiC and the exceptional properties of GaN heterostructure technology, GaN semiconductors processed on SiC substrates are strong candidates for implementing highly durable/stable ICs for extreme ambient temperatures of 500 $^{o}$C or higher.

We demonstrate in this paper the performance of a GaN500 technology processed on SiC substrate operating at up to 600 $^{o}$C. We describe the state-of-the-art in extreme temperature ICs based on WBG (SiC and GaN) semiconductors. GaN500 devices are fabricated and characterized at high

temperature (HT), and a model is extracted covering the 25 ºC to 600 ºC temperature range. Different logic gates and voltage reference circuits made of GaN500 HFETs and integrated load resistors have been implemented and validated at HT. This development is intended to exploit the inherent ability of GaN500 technology to operate at temperatures over 300 ºC.

## 3.3 HT ICs and GaN Selection

The most common polytypes of SiC semiconductors are the hexagonal 4H and 6H structures. These polytypes are differentiated by the stacking sequence of the biatom layers of the SiC structure [69]. Several studies have been recently reported on developing SiC based ICs for high temperature applications. Multistage digital (master–slave data flip-flop and data-reset FF) and analog (voltage reference) SiC-ICs using 4H-SiC MESFETs are demonstrated in [11]. SiC ICs integrated with power devices on the same chip, based on the mature and stable Tungsten–Schottky interface, were shown to operate correctly at 300 ºC. Seventeen circuits implemented with the Raytheon's 4 H-type HTSIC process were reported in [47]. They were successfully tested at 300 ºC. The report set of circuits includes a Digital to Analog Converter (DAC) Controller, a NULL Convention Logic (NCL) multiply accumulate unit (MAC), a 4-bit NCL counter, adders, shift registers, DFFs and logic gates.

In [168], high-temperature voltage and current references are designed with a silicon carbide CMOS process. Their operation and stability were reported in the 25 ºC to 540 ºC temperature range. Using 6H-SiC depletion-mode JFET transistors, the design characterization of various logic circuits (inverter, NAND, and NOR) were reported in [169], with some performance being reported at extreme temperatures reaching 550 ºC. In [170], low-voltage 4H-SiC n-p-n bipolar devices are used to implement OR–NOR gates and a three-stage ring oscillator. The integrated circuits have been successfully tested up to 300 ºC. Based on 6H-SiC n-channel depletion-mode JFETs, differential amplifiers were successfully fabricated using commercial 2-in epitaxial wafers obtained from CREE [171], [172] and the reported circuits were characterized at temperatures reaching 450 ºC. A simple analog amplifier and a NOT logic gate reported in [46] were fabricated using 6H-SiC JFET technology and were successfully operated for thousands of hours at 500 ºC. Reference [173] reports the first ADC implemented using SiC along with the first CMOS DAC. These circuit were tested in the 25 ºC to 400 ºC temperature range.

Although remarkable advances have been achieved, the development of SiC-based ICs is still at its early beginning. Indeed, the majority of the reported SiC ICs are realized with either small number of implemented devices or on large integrated areas having low density of device integration. There are still many obstacles limiting widespread adoption of SiC ICs, including immature foundry processes, design kits and device models. Also, these ICs offer significantly lower operating frequencies compared to Si ICs. They also suffer from their high power-supply voltage and larger device sizes.

On the other hand, despite considerable efforts to develop GaN devices operating at HT above 600 $^{o}$C [14], 800 $^{o}$C [18], 900 $^{o}$C [19] and 1000 $^{o}$C [20], few research projects are directed toward the development of ICs based on GaN devices [21], [22], [13]. In [21], A GaN-based E/D-mode inverter is successfully fabricated and tested from room temperature to 300 $^{o}$C. This technology integrates E-mode MOSFETs with D-mode HEMTs. The AlGaN/GaN wafer that were used are grown on sapphire substrates and the gate insulator consists of an $Al_2O_3$ layer.

GaN HFET depletion mode devices are used in [22] to implement various circuits: NOT gate, comparator, ring-oscillator and frequency divider. In these circuits, AlGaN/GaN HFETs are grown on a semi-insulating SiC substrate, and the threshold voltage is adjusted using gate-recess etching. Schottky diodes were used to provide voltage-level shifting required to implement complementary logic functions. A 31-stage ring oscillator was tested at temperatures reaching 265 $^{o}$C and it was shown that this circuit returns to the original performance after returning to room temperature.

A novel AlInN/GaN based IC was demonstrated in [13]. The fabricated ICs comprise an inverter and a differential amplifier that showed stable performance up to 500 $^{o}$C. Along with the exceptional quality of AlInN/GaN heterostructure and very high carrier concentration and mobility, fabrication advances were reported. Indeed, a novel metallization and high-K passivation/gate dielectrics enabling suitable high temperature operation were reported.

## 3.4 HT Characterization and Modeling

### 3.4.1 GaN500 design and processing:

The adopted GaN500 technology is processed at the Canadian Photonics Fabrication Center (CPFC) of the National Research Council of Canada (NRC). The offered GaN Heterojunction Field

Effect Transistors (HFETs) Monolithic Microwave Integrated Circuit (MMIC) process includes GaN HFETs, Metal-Insulator-Metal (MIM) capacitors and nichrome resistors. This GaN-based HFET technology is fabricated on 3-inch silicon carbide wafers of 75 μm thickness. It features 0.5 μm long metal gates, 50 Ω/sq nichrome (NiCr) resistors, MIM capacitors of 0.19 fF/μm$^2$ and two metal layers for interconnect. All transistors are field-plated designs. The technology is appropriate for RF and microwave circuit design, suitable for 40 V maximum drain voltage bias and it supports 5 W/mm of power levels.

The AlGaN/GaN epitaxial layer processed and delivered to NRC by an approved supplier allows integrating HFETs over a SiC wafer. A simplified cross-section of the epitaxial layers is shown in Figure 3.1 The ohmic contacts are defined and fabricated by high-temperature annealing to ensure a low-resistance contact to the two-dimensional electron gas (2DEG), which acts as the active conduction layer. The active area of the device is isolated by etching the GaN buffer layer. The gate fingers are formed by depositing a passivation dielectric in which a slot is etched for the gate contacts. Then, the gate contact metal is deposited, and a second dielectric encapsulation is applied.

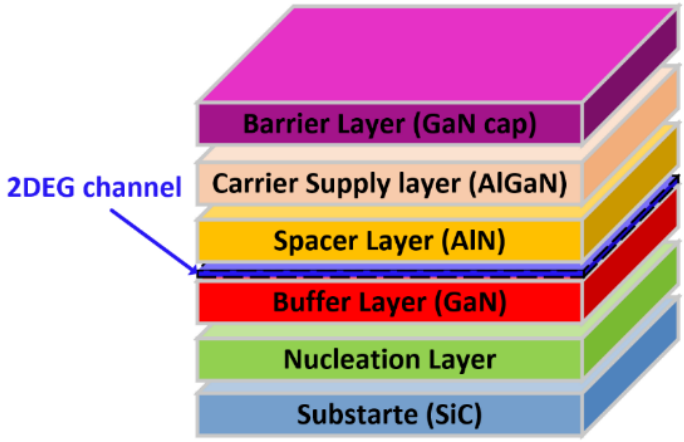



Figure 3.1: Not to scale cross-section of GaN HFET epitaxial layers.

Openings are etched into the dielectric to provide connections to the ohmic and gate contacts. The resistors are patterned with nichrome, followed by deposition of the first interconnect metal layer. The first metal layer (1ME) forms contacts to the ohmic metal, the gate pads and the nichrome layer. The 1ME layer is also used to form the field plate, which is connected to the source and which overlaps the gate. A dielectric deposition is used to isolate the 1ME layer and via openings are defined. The dielectric is also used as the insulator in MIM capacitors.

The second interconnect metal regions are defined in a temporary photoresist layer. The second metal layer (2ME) is required to bridge over other layers. It is used as the top layer of MIM capacitors and is also used to form the air-bridge structures. The composition of the dielectrics, gate layer and ohmic metals are proprietary to NRC. The photolithography is performed by a stepper. The mesa and dielectric vias are etched by a dry etch plasma process. The metal layers are deposited by e-beam evaporation and patterned by a lift-off process.

### 3.4.2 Measurement setup and HT packaging:

The GaN500 chips are diced at NRC. A typical ceramic dual in-line (DIL) package is used to perform the measurements. The back metallization of the fabricated GaN500 die is a 5 µm Au layer. The die attachment is performed using Silver Epoxy (EPO-TEK H20E-PFC) from EPOXY TECHNOLOGY. It is an electrically and thermally conductive epoxy qualified to operate at temperatures up to 325 $^{o}$C. Above this temperature, the epoxy starts losing its rigidity and may even melt. Therefore, to perform testing at higher temperature, the tested package remains in a stable horizontal position to prevent the possibility of die dislocation.

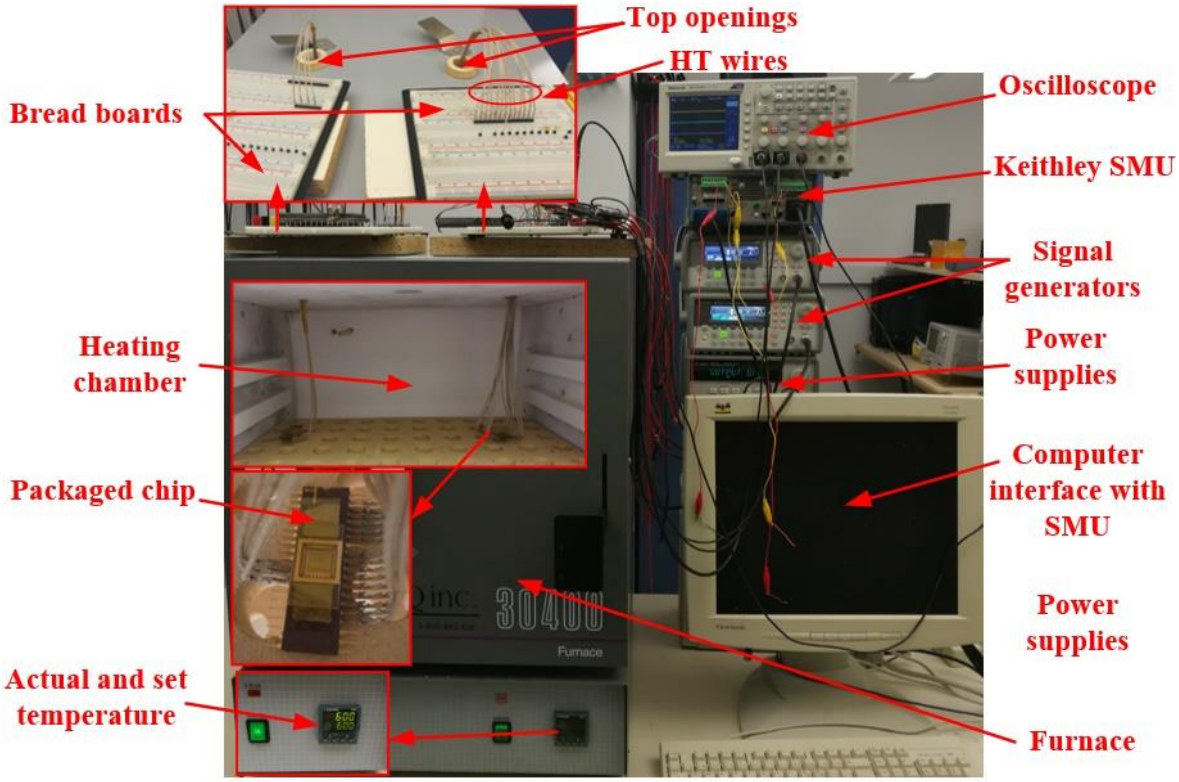
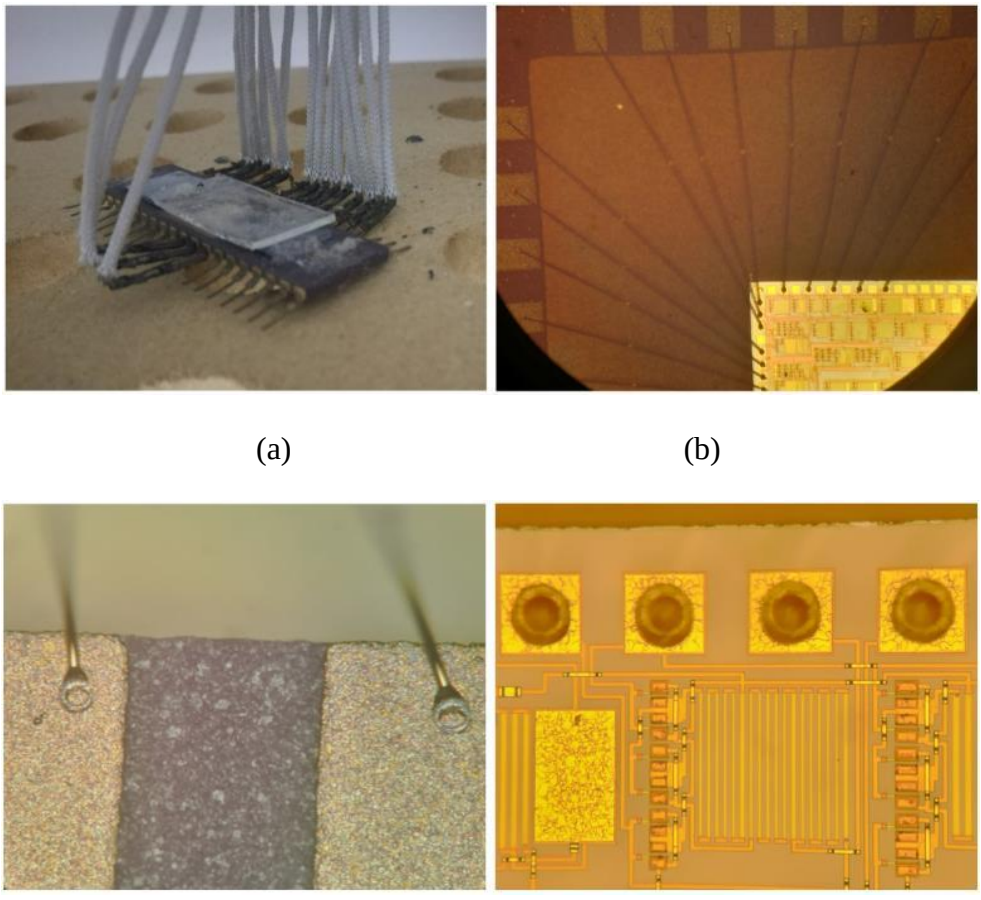



Figure 3.2: Experimental setup of HT measurements.

The measurement setup shown in Figure 3.2 was built to perform circuit characterization at high temperatures. The heating chamber of the furnace can reach 1000 $^{o}$C. It has two top openings where HT cables are installed to connect the tested packages to the external measurement devices. The HT cables are Nickel-Plated Copper conductors that can endure 450 $^{o}$C. The ball bonder wires have a 25 µm diameter. Ball bonding is performed using an ASM Pacific Technology wire bonder (model Eagle Xtreme [174]). Conventional bread-boards are used to connect the HT part (packaging and wiring) with the measurement instruments. The latter supply the necessary voltages and input signals and monitor the received signals from the tested chips.



(a) (b)

(c) (d)

Figure 3.3: HT packaging (at 600 $^{o}$C): (a) HT wires connected to a DIL ceramic package, (b) Bonding wires between the pads of the chip and the package, (c) Wire bonding terminals on the package pads, and (d) Ball bonding on the chip pads.

The measurements were carried out using a 2-channel Keithley SMU to perform the I-V characteristics of GaN500 transistors, 4294 Impedance Analyzer [175] to measure the values of

integrated capacitors, two signal generators were used to test the functionality of digital ICs. DC power supplies were used to set the proper high and low levels of the ICs and a Tektronix oscilloscope was used to visualize the circuit's input/ output waveforms and for data acquisition. Figure 3.3 shows the HT packaging at 600 $^{o}$C including the wire bonding and the external wiring of the ceramic package.

### 3.4.3 HT characterization and modeling:

This work was motivated by the need to realize GaN-ICs with a higher device density integration than previously reported circuits. Still, we were targeting operating temperatures higher than several recently reported GaN ICs. To succeed designing complex ICs with the available GaN technology, the first step was to develop trustworthy HT models not provided by the foundry. In the adopted GaN500 HFET technology, the provided models in the Physical Design Kit are the Root model and an Angelov model. For active and passive components, both models do not support HT simulations above 300 $^{o}$C. Therefore, we performed the HT characterization of GaN500 devices and passive elements to develop an accurate model that enables simulating the temperature effects on the design.

#### 3.4.3.1 GaN500 HEMT HT modeling

Modeling of electronic devices is typically done either by obtaining physical equations or by solving the well-known Poisson and Schrodinger equations. This allows describing the exact behavior of the device. It can also be done by forming a compact empirical model that consists of fundamental circuit components combined in a certain way to mimic the device behavior [176, 177]. Both ways have their advantages and disadvantages. However, empirical modeling proved effective for use in circuit simulators because of its computational simplicity and the lower development time required [178], [123].

Several types of empirical models were developed and used to model GaN HEMTs, such as the Angelov model and the EEHEMT model [179, 180]. Though the EEHEMT model is very accurate, its piecewise nature made it hard for us to extract the device characteristics. On the other hand, we found it easy to use the Angelov model because of its closed form nature that facilitates the extraction methodology.

In our previous work [123], high-temperature modeling of the I-V characteristics for GaN150-based HEMT technology was done up to 250 $^{o}$C using an extended Angelov model to better describe the device behavior. The model consists of 14 different parameters, that describe the geometrical properties of the I-V characteristic curves at different operating conditions ($V_{GS}$, $V_{DS}$), as shown in equations (3.1)-(3.6) below. Equations (3.2)-(3.6) develop the parts of the main equation (3.1) that express the drain source current $I_{DS}$ of the device.

$$I_{DS} = I_{PKT} * (1 + tanh(\psi)) * tanh(\alpha_T V_{DS} + K_T V_{DS}) * (1 + \lambda V_{DS}) \quad (3.1)$$

$$\psi = sinh(P_{1t}(V_{GS} - V_{PKT}) + P_{2t}(V_{GS} - V_{PKT})^2 + P_{3t}(V_{GS} - V_{PKT})^3) \quad (3.2)$$

$$P_{it} = P_{i0} + (P_i - P_{i0}) * tanh(\alpha_R V_{DS}) \quad (3.3)$$

$$\alpha_T = \alpha_R + \alpha_s(1 + tanh(\psi)) \quad (3.4)$$

$$V_{PKT} = V_{pk0} + \left(V_{pk} - V_{pk0}\right) tanh(\alpha_R V_{DS}) \quad (3.5)$$

$$I_{PKT} = I_{pk0} + \left(I_{pk} - I_{pk0}\right) tanh(\alpha_R V_{DS}) \quad (3.6)$$

Over the following sections, we present the high-temperature modeling process and results of the I-V characteristics for that GaN500 HEMT technology up to 600 $^{o}$C. The same methodology applied in [123] was used. It uses the temperature as a variable in the model equations. The whole modeling process is summarized in Figure 3.4.

First, I-V experimental measurements were collected and put in tabular form to represent the independent ($V_{DS}$, $V_{GS}$) and dependent ($I_{DS}$) variables, corresponding to each temperature step ($T_i$) starting from 25 $^{o}$C up to 600 $^{o}$C. At each step ($T_i$), the data were fitted to the extended Angelov model equations using non-linear regression functions available in MATLAB. Then, each of the 14 parameters were plotted against temperature to identify their temperature dependence. Some of the parameters showed unusual behavior at temperature values above 500 $^{o}$C as shown in Figure 3.5. For example, parameter $K_T$, which is responsible for describing the knee shape of the I-V characteristic curve between the linear and saturation regions, shoots up at temperature values higher than 500 $^{o}$C. For this reason, the modeling process was performed over the 25 $^{o}$C-500 $^{o}$C temperature range.

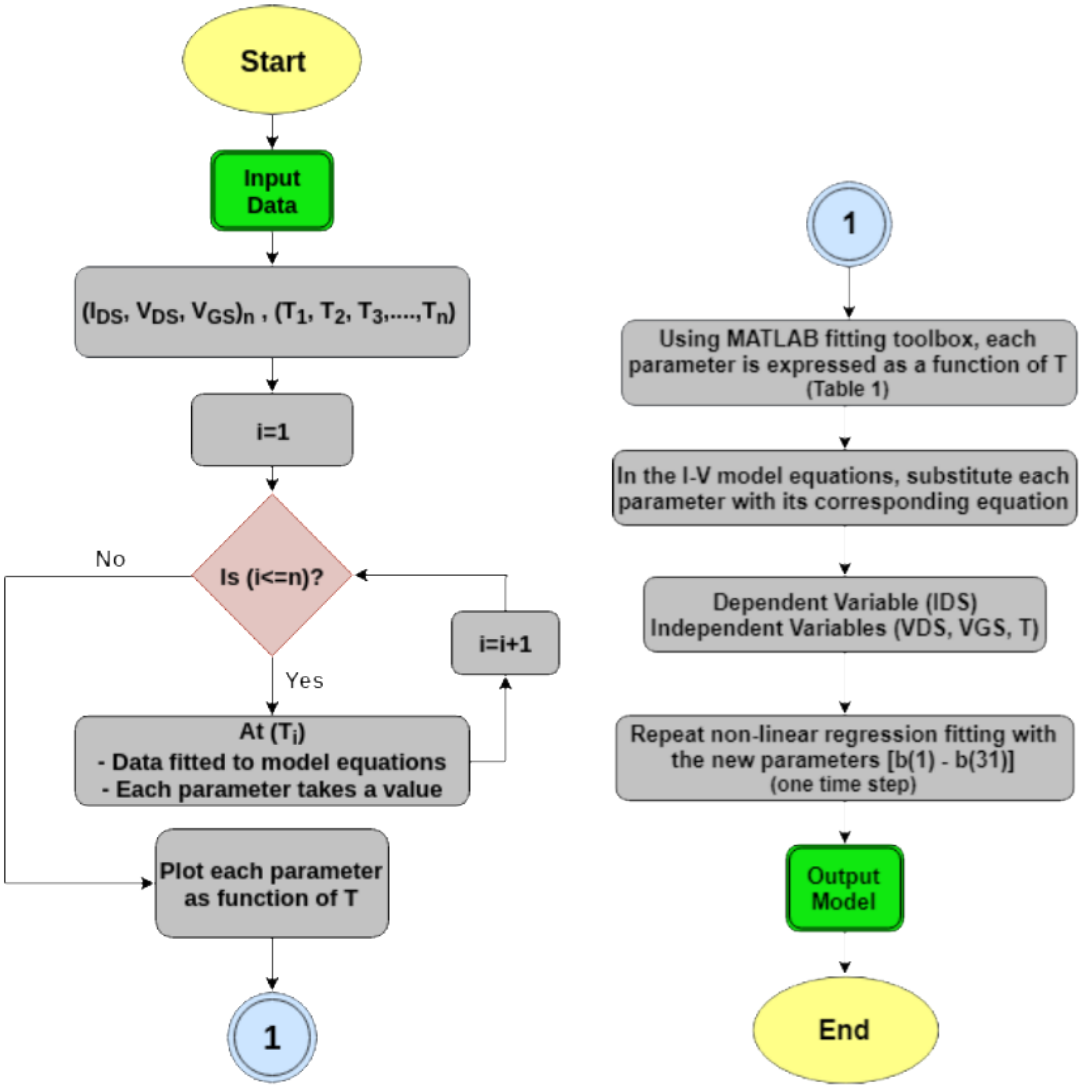
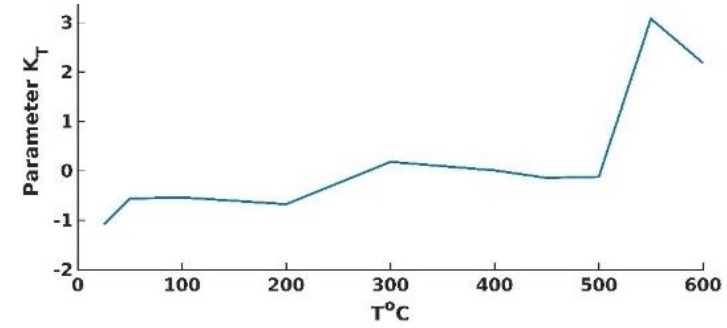
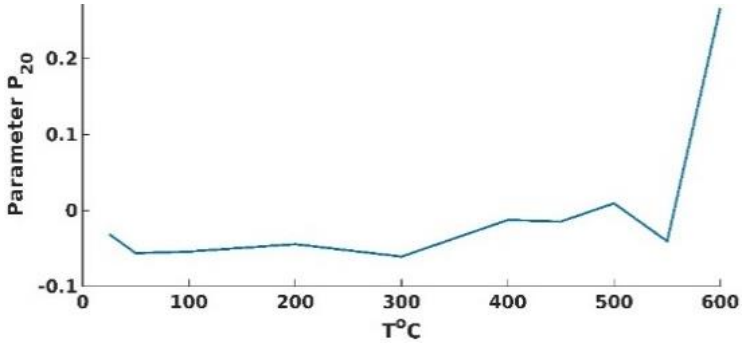



Figure 3.4: Flowchart summarizing the HT modeling process.

Five of the 14 parameters ($\alpha_S$, $P_{30}$, $P_1$, $I_{pk0}$, $V_{pk}$) were varying around certain average values without a clear trend. Consequently, each of these five parameters was set to its average value, and each of the remaining 9 parameters were expressed as a function of temperature. These functions were summarized into five 3rd-order polynomials, three 2nd-order polynomials and one 1st-order polynomial as shown in Table 3.1, where b(1)-b(31) are the parameters assumed to model the temperature as a variable. The parameters were substituted back in the equations (3.1)-(3.6) describing the drain source current but, this time, with the temperature added as an independent variable. Finally, the temperature was increased to the tabulated data and the non-linear regression fitting was performed one last time with b(1)-b(31) as the new fitting parameters to form the final model.




(a)




(b)

Figure 3.5: Variations of two modeling parameters with temperature: (a) $K_T$, and (b) $P_{20}$.

Table 3.1: Angelov fitting parameters as a function of temperature

| No. | Fitting Parameters | Temperature Dependence |
|---|---|---|
| **1** | $\lambda$ | $b(1)T^3 + b(2)T^2 + b(3)T + b(4)$ |
| **2** | $K_T$ | $b(5)T^2 + b(6)T + b(7)$ |
| **3** | $\alpha_S$ | $Constant = 0.0563$ |
| **4** | $\alpha_R$ | $b(8)T + b(9)$ |
| **5** | $P_3$ | $b(10)T^3 + b(11)T^2 + b(12)T + b(13)$ |
| **6** | $P_{30}$ | $Constant = 0.3$ |
| **7** | $P_2$ | $b(14)T^3 + b(15)T^2 + b(16)T + b(17)$ |
| **8** | $P_{20}$ | $b(18)T^3 + b(19)T^2 + b(20)T + b(21)$ |
| **9** | $P_1$ | $Constant = -0.0133$ |
| **10** | $P_{10}$ | $b(22)T^3 + b(23)T^2 + b(24)T + b(25)$ |
| **11** | $I_{pk}$ | $b(26)T^2 + b(27)T + b(28)$ |
| **12** | $I_{pk0}$ | $Constant = -0.0251$ |
| **13** | $V_{pk}$ | $Constant = -8.57 * 10^{-5}$ |
| **14** | $V_{pk0}$ | $b(29)T^2 + b(30)T + b(31)$ |

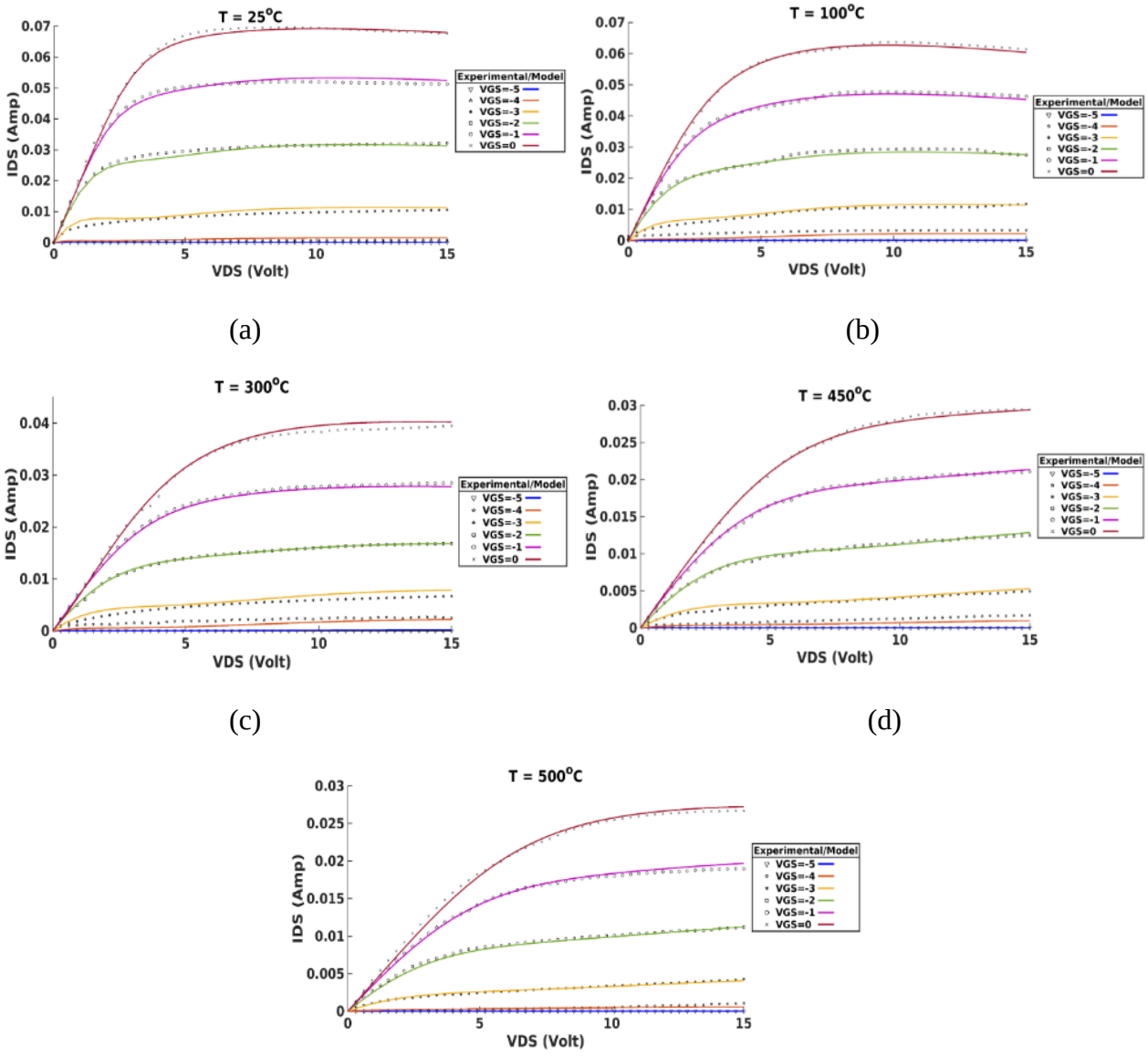
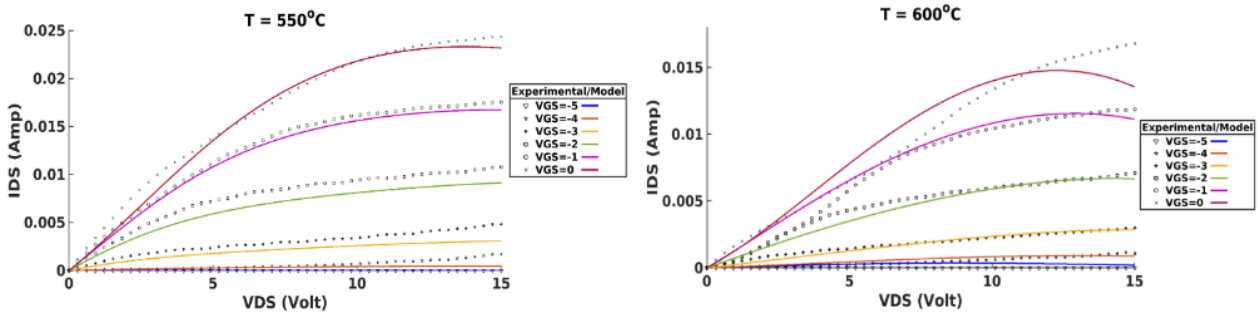



Figure 3.6: Experimental and fitted output I-V characteristics at: (a) T = 25 ºC, (b) T = 100 ºC, (c) T = 300 ºC, (d) T = 450 ºC, and (e) T = 500 ºC.

The accuracy of the fitted I-V equations can be compared to the experimental measurements giving a sum of squared errors (SSE) less than (< 0.001). Figure 3.6 presents the fitted I-V curves along with the experimental measurements at variable $V_{GS}$ and $V_{DS}$ for different temperature values; 25 ºC, 100 ºC, 300 ºC, 450 ºC and 500 ºC covering the temperature model range (25 ºC – 500 ºC). In Figure 3.7, the developed model is tested for generating the I-V curves for temperature values (550ºC, 600 ºC) outside the model range. It is clear that the model fails to predict the knee shape

of the I-V curves at high $V_{GS}$ values (0, -1) specially at 600 °C. This is expected because we did not consider the variation of the knee parameter $K_T$ and the other parameters at such high temperature values as discussed before.

The proposed modeling process is very efficient in terms of time and accuracy as proved here and before in [123], where the model was verified with the Spectre simulator. The only limitation to the modeling process is the initial values that should be supplied to the non-linear regression functions in MATLAB, corresponding to each fitting parameter. These initial values affect significantly the fitting parameters in determining the accuracy of the model. However, we can overcome this limitation by obtaining approximate values of these parameters from simple calculations on the experimental data using an Excel program.




(a) (b)

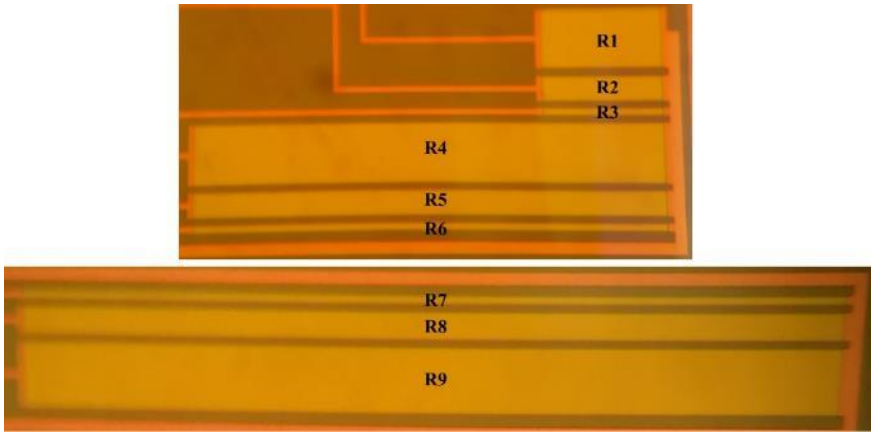
Figure 3.7: Model validity tested for temperature values higher than the model calibration range: (a) At 550 °C, and (b) 600 °C.

### 3.4.3.2 Passive elements HT characterization and modeling

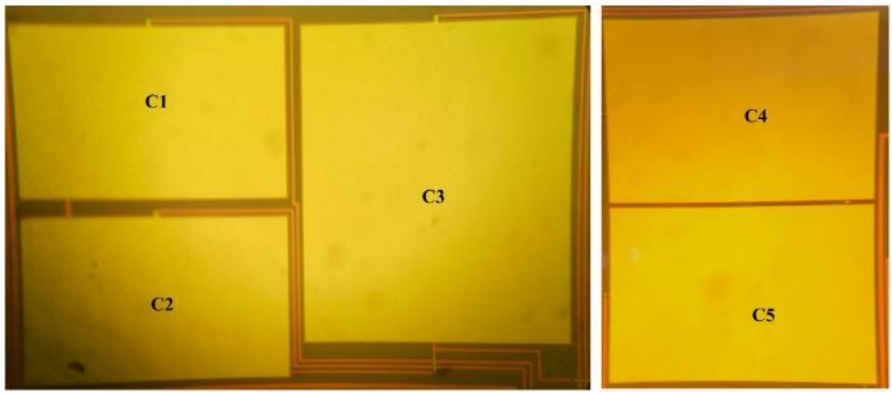
Due to the lack of complementary devices for the normally-on GaN500 HFET, the adopted solution is the use of resistors for the GaN-IC development. For IC proper operation over a wide temperature range, it was proven in [165] that the temperature matching between the various components is successfully accomplished using epitaxial resistors. To provide an accurate model that considers the temperature impact on the values of passive elements, we performed the HT characterizations of integrated resistors and capacitors.

Different sizes of resistors ($R_1$ to $R_9$) and capacitors ($C_1$ to $C_5$) were fabricated as shown in Figure 3.8 and their values are summarized in Table 3.2 and Table 3.3. The experimental setup shown in Figure 3.2 was also used to perform the HT characterizations of passive components between 25°C

and 600ºC. It was found that the measured resistances of $R_{1-9}$ linearly increase with temperature in the 25-600ºC range. However, the value change rate (slope), listed in Table 3.2, is different from one resistor to another. Figure 3.9 shows that the relationship between the slope and the initial value of the resistors is linear.




(a)




(b)

Figure 3.8: Integrated passive components for HT characterization: (a) Resistors, and (b) Capacitors.

Equation (3.7) propose a general expression relating the resistance value and the applied temperature. Where $R_0$ is the initial resistance at 0 ºC, T is the actual temperature (ºC) and α is the slope of resistance variation with temperature. From Figure 3.9, we extract the expression of α (equation (3.8)) and substitute it in equation (3.7) to formulate the final expression of the resistance as a function of temperature (equation (3.9)).

Table 3.2: Integrated Resistors

| Resistors | | Resistance (kΩ) at different temperatures (°C) | | | | | | | | | | Slope (Ω/ °C) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | W/L (µm/ µm) | 25 | 100 | 200 | 300 | 350 | 400 | 450 | 500 | 550 | 600 | |
| $R_1$ | 50/100 | 0.10 | 0.1 | 0.11 | 0.12 | 0.13 | 0.14 | 0.14 | 0.15 | 0.16 | 0.17 | 0.11 |
| $R_2$ | 20/100 | 0.22 | 0.23 | 0.24 | 0.25 | 0.26 | 0.27 | 0.28 | 0.29 | 0.30 | 0.32 | 0.16 |
| $R_3$ | 5/100 | 0.8 | 0.82 | 0.85 | 0.89 | 0.91 | 0.92 | 0.94 | 0.97 | 0.99 | 1.03 | 0.36 |
| $R_4$ | 50/400 | 0.34 | 0.35 | 0.37 | 0.39 | 0.4 | 0.41 | 0.42 | 0.44 | 0.45 | 0.46 | 0.2 |
| $R_5$ | 20/400 | 0.81 | 0.83 | 0.87 | 0.9 | 0.92 | 0.94 | 0.96 | 0.99 | 1.0 | 1.03 | 0.37 |
| $R_6$ | 5/400 | 3.61 | 3.24 | 3.35 | 3.47 | 3.53 | 3.58 | 3.64 | 3.72 | 3.74 | 3.78 | 1.1 |
| $R_7$ | 5/650 | 5.16 | 5.27 | 5.45 | 5.64 | 5.73 | 5.81 | 5.91 | 6.01 | 6.02 | 6.05 | 1.6 |
| $R_8$ | 20/650 | 1.31 | 1.35 | 1.4 | 1.45 | 1.48 | 1.5 | 1.53 | 1.57 | 1.59 | 1.62 | 0.52 |
| $R_9$ | 50/650 | 0.54 | 0.55 | 0.58 | 0.6 | 0.62 | 0.63 | 0.65 | 0.67 | 0.68 | 0.69 | 0.26 |

Table 3.3: Integrated Capacitors

| Capacitor | W/L (µm) | Value @25 °C (pF) |
|---|---|---|
| $C_1$ | 500/315 | 58 |
| $C_2$ | 500/315 | 56 |
| $C_3$ | 500/600 | 83 |
| $C_4$ | 400/600 | 75 |
| $C_5$ | 400/600 | 73 |

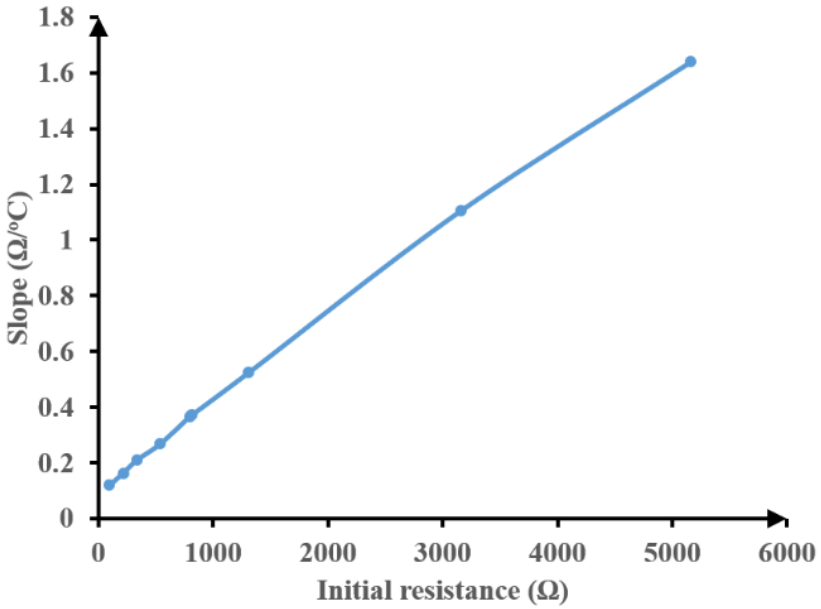



Figure 3.9: Variation of resistance slope with respect to the initial value of resistors.

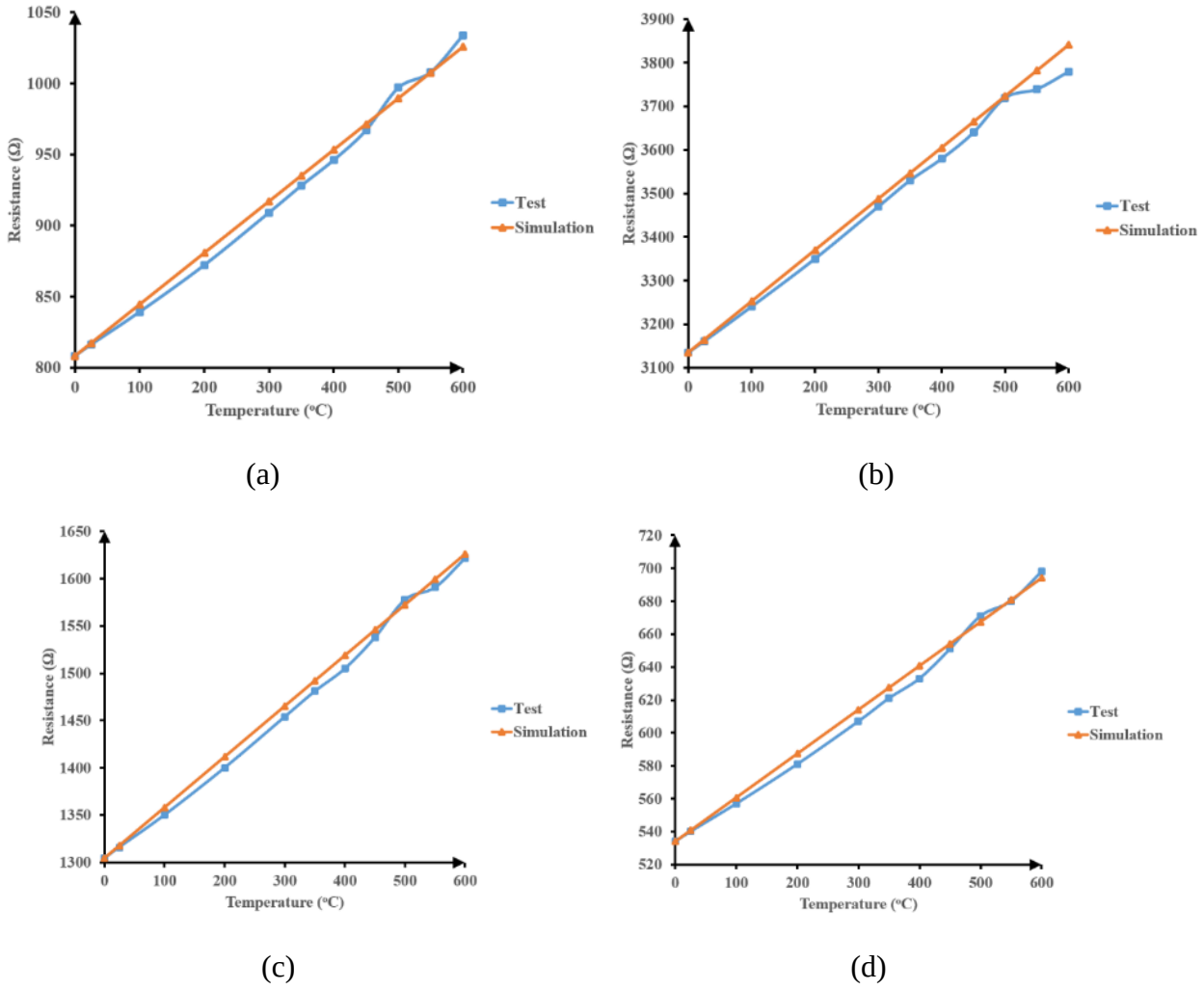



Figure 3.10: HT characterization of different integrated resistors: (a) $R_5$, (b) $R_6$, (c) $R_8$, and (d) $R_9$.

To validate equation (3.9), the simulations of $R_{1\text{-}9}$ are compared with experimental measurements over the temperature range 25-600 °C. Figure 3.10 shows the good matching between simulated and measured resistance of ($R_5$, $R_6$, $R_8$, $R_9$) resistors.

$$R_t = R_0 + \alpha T \quad (3.7)$$

$$\alpha = 3.5 \times 10^{-4} R_0 + 0.08 \quad (3.8)$$

$$R_t = R_0(1 + 3.5 \times 10^{-4} T) + 0.08T \quad (3.9)$$

Using the Agilent impedance analyzer, the sensitivity of various capacitor values was characterized. Figure 3.11 shows the capacitance of 3 different capacitors ($C_1 = C_2$ and $C_4 = C_5$) over the temperature range between 25 °C and 600 °C. Table 3.3 summarizes the values of the

integrated capacitors. The results in Figure 3.11 show the capacitance stability of each capacitor up to 550 ºC, with minor variations due to the variable parasitic capacitance of testing probes. Above 550 ºC, the capacitance started to increase gradually. Therefore, the capacitance could be considered as a constant value within the temperature range 25-550 ºC. Further measurements should be performed at higher temperature to extract temperature models of capacitors covering the temperature beyond 550 ºC.

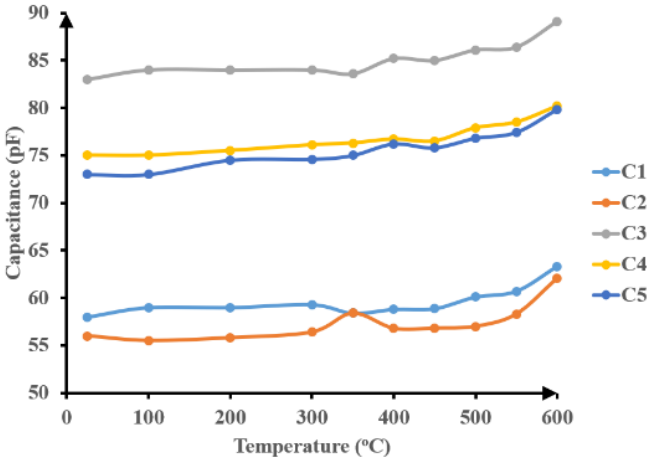



Figure 3.11: HT characterization of different integrated capacitors.

## 3.5 HT Circuit Validation

### 3.5.1 Logic gates:

Circuit schematics of a set of implemented logic gates are shown in Figure 3.12. In the inverter circuit (Figure 3.12(a)), the input signal (IN) controls a GaN driver device whose drain current is supplied by a 20 kΩ resistor that acts as a current source. The remaining part of the circuit performs the role of a voltage level shifter that ensures the voltage level of the output signal (OUT) to be compatible with the input of the next logic circuit stage. The NAND-2IN gate in Figure 3.12(b) uses two series GaN devices in the pull-down driver network. Similarly, three series GaNs are used to form the core of NAND-3IN gate as shown in Figure 3.12(c). The NOR-2IN gate and NOR-3IN gates in Figure 3.12(d) and Figure 3.12(e), respectively, use two and three parallel GaN devices in the pull-down driver network.

The gate length of all transistors is 0.5µm and the gate width of each transistor is mentioned in Figure 3.12. The resistors are fabricated from a Nichrome (NiCr) layer and their values are shown

in the schematic design (Figure 3.12). Testing conditions for all logic gates were as follows: $V_{DD}$ = +14 V, $V_{SS}$ = -14 V, input logic low = −5 V and input logic high = 0 V.

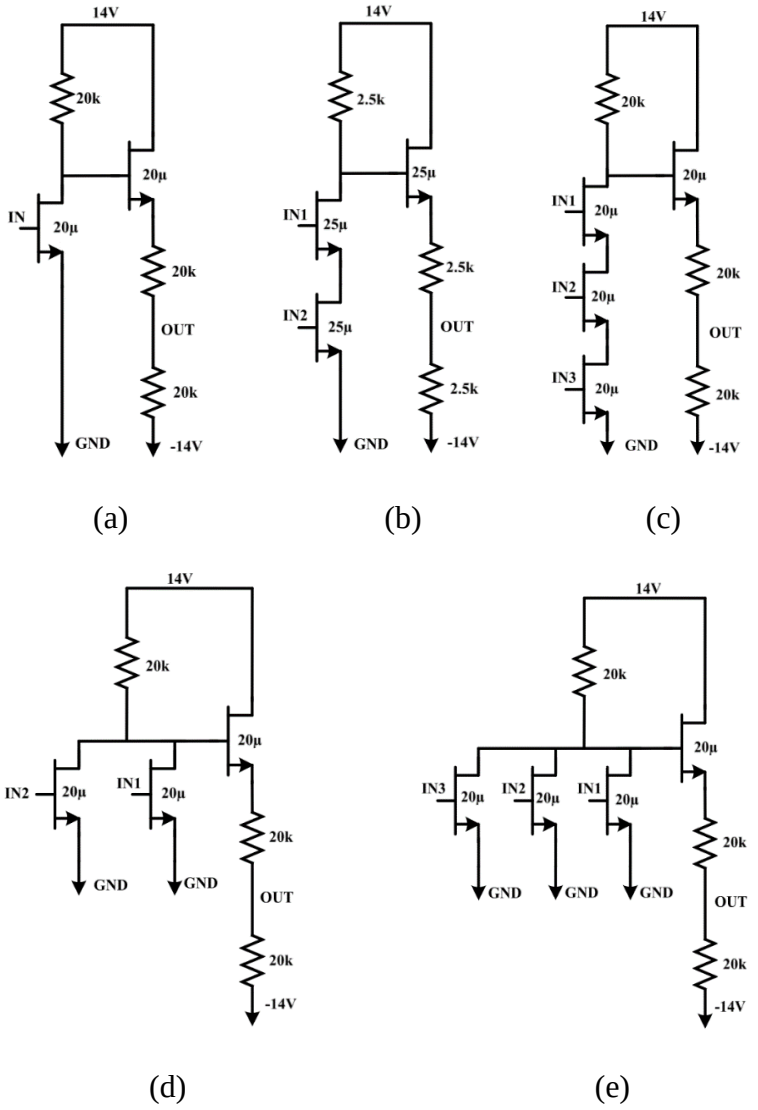
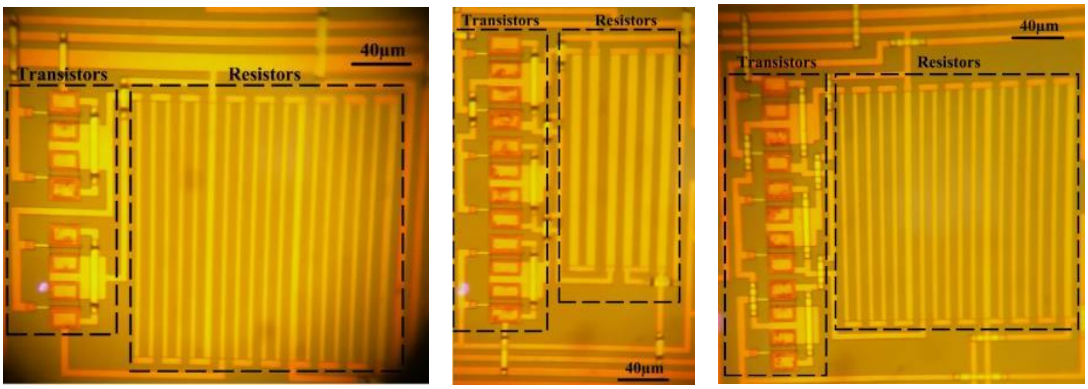


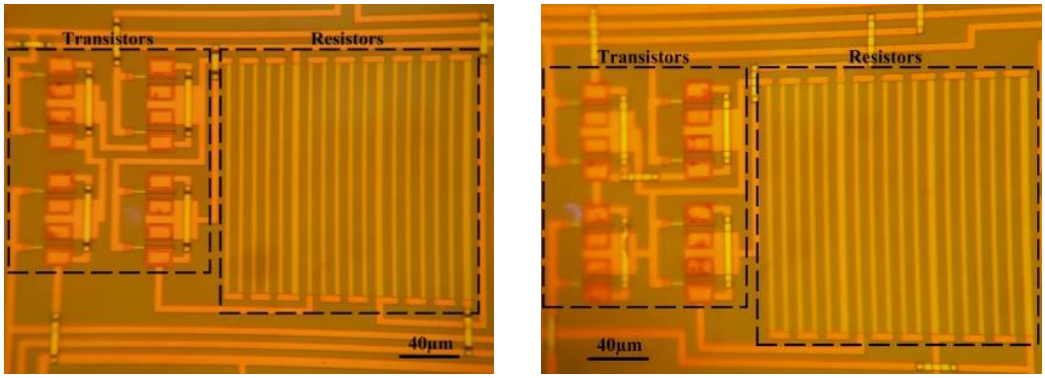

Figure 3.12: Circuit structure of various digital logic gates: (a) NOT, (b) NAND-2IN, (c) NAND-3IN, (d) NOR-2IN, and (e) NOR-3IN.

Figure 3.13 shows the micrographs of the fabricated logic gates which were tested in the 25 to 600 $^{o}$C temperature range. The pulse response of the inverter, depicted in Figure 3.14, shows a stable output with no significant temperature effect up to 300$^{o}$C (overlapping plots). Between 300 $^{o}$C and 500 $^{o}$C, the output logic low level is still stable at -5 V, but the output logic high level drops from its initial value (0 V at 25 $^{o}$C) by 20% (of low-to-high difference) at 400 $^{o}$C and 60% at 500 $^{o}$C. In addition, an increase in the rise time was observed. This increase is possibly due to a surface trap

charge activation, but this phenomenon requires further and more detailed studies. Above 500 ºC, the output logic low and high values dropped drastically below the desired levels.




(a) (b) (c)




(d) (e)

Figure 3.13: Micrograph of implemented logic gates: (a) Inverter, (b) NAND-2IN, (c) NOR-2IN, (d) NAND-3IN, and (e) NOR-3IN.

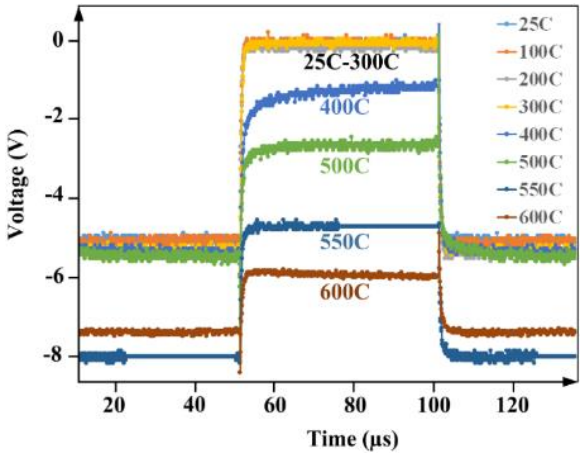
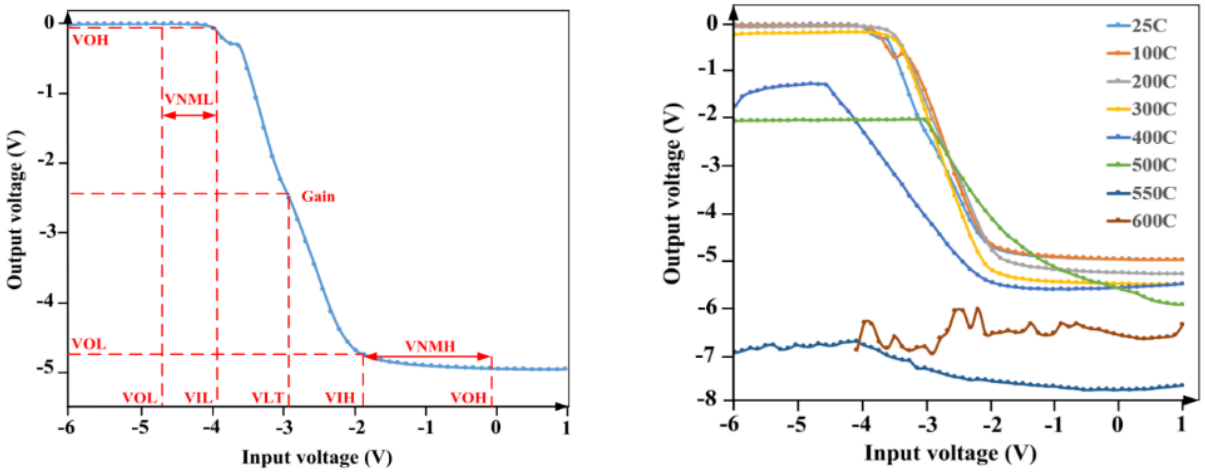



Figure 3.14: Pulse characteristics of the inverter in the temperature range 25- 600 ºC.

The voltage transfer characteristic (VTC) of the AlGaN/GaN based inverter at room temperature is shown in Figure 3.15(a). Six key dc performance metrics of the inverter can be obtained from that VTC, namely: the maximum output voltage in the low state ($V_{OL}$), the minimum output voltage in the high state ($V_{OH}$), the logic gate threshold voltage ($V_{LT}$), the voltage gain (Gain), the noise margin for low level ($V_{NML}$), and the noise margin for high level ($V_{NMH}$). Figure 3.15(b) shows the VTC of the inverter between 25 ºC and 600 ºC and Table 3.4 summarizes the six dc performance metrics for all measured temperatures. Up to 300 ºC, the output voltage and gain were remarkably stable. Beyond this temperature, the logic high-level $V_{OH}$ varies at a significant rate. Consequently, $V_{NMH}$ is noticeably degraded at the highest temperatures.




(a) (b)

Figure 3.15: VTC of the GaN inverter (a) At 25C, and (b) Between 25 ºC and 600 ºC.

Table 3.4: DC Performance Metrics of a GaN Inverter

| | **25 ºC** | **100 ºC** | **200 ºC** | **300 ºC** | **400 ºC** | **500 ºC** | **550 ºC** | **600 ºC** |
|---|---|---|---|---|---|---|---|---|
| **$V_{OL}$** | -4.7 | -4.66 | -5 | -5.2 | -5.46 | -5.87 | -7.5 | -6.64 |
| **$V_{LT}$** | -2.9 | -2.68 | -3 | -3 | -3.27 | -2.68 | -3.62 | -0.18 |
| **$V_{OH}$** | -0.1 | -0.11 | -0.24 | -0.33 | -1.28 | -2 | -6.7 | -6.33 |
| **Gain** | -3.7 | -3.9 | -3.4 | -3.9 | -2 | -2.2 | -0.8 | -0.4 |
| **$V_{NML}$** | 0.9 | 0.8 | 1.5 | 1.7 | 0.89 | 2.2 | 3.4 | 5.98 |
| **$V_{NMH}$** | 1.7 | 1.85 | 1.48 | 1.51 | 0.8 | - | - | - |

Figure 3.16 and Figure 3.17 show the dynamic characteristics of the NAND (2IN and 3IN) and NOR (2IN and 3IN) gates, respectively, between 25 $^{o}$C and 300 $^{o}$C. Above this range, the gates lost its functionality. It should be mentioned that the third input (IN3) of NAND-3IN and NOR-3IN is connected to IN1 due to the unavailability of a third signal generator during the measurements. However, this connection is sufficient to validate the functionality of the gates.

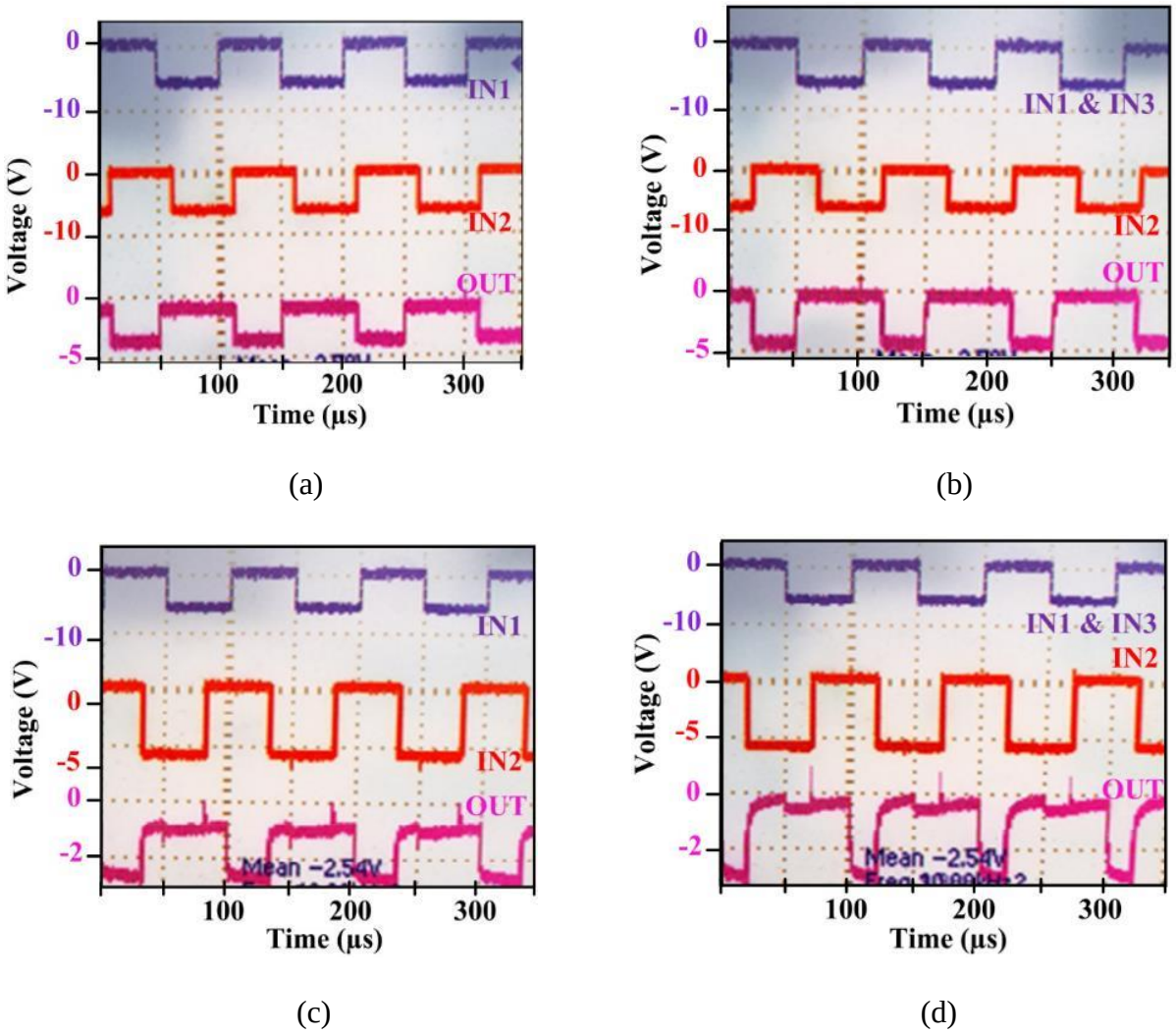



Figure 3.16: Measured dynamic characteristics of NAND gates: (a) NAND-2IN at 25 $^{o}$C, (b) NAND-3IN at 25 $^{o}$C, (c) NAND-2IN at 300 $^{o}$C, and (d) NAND-3IN at 300 $^{o}$C.

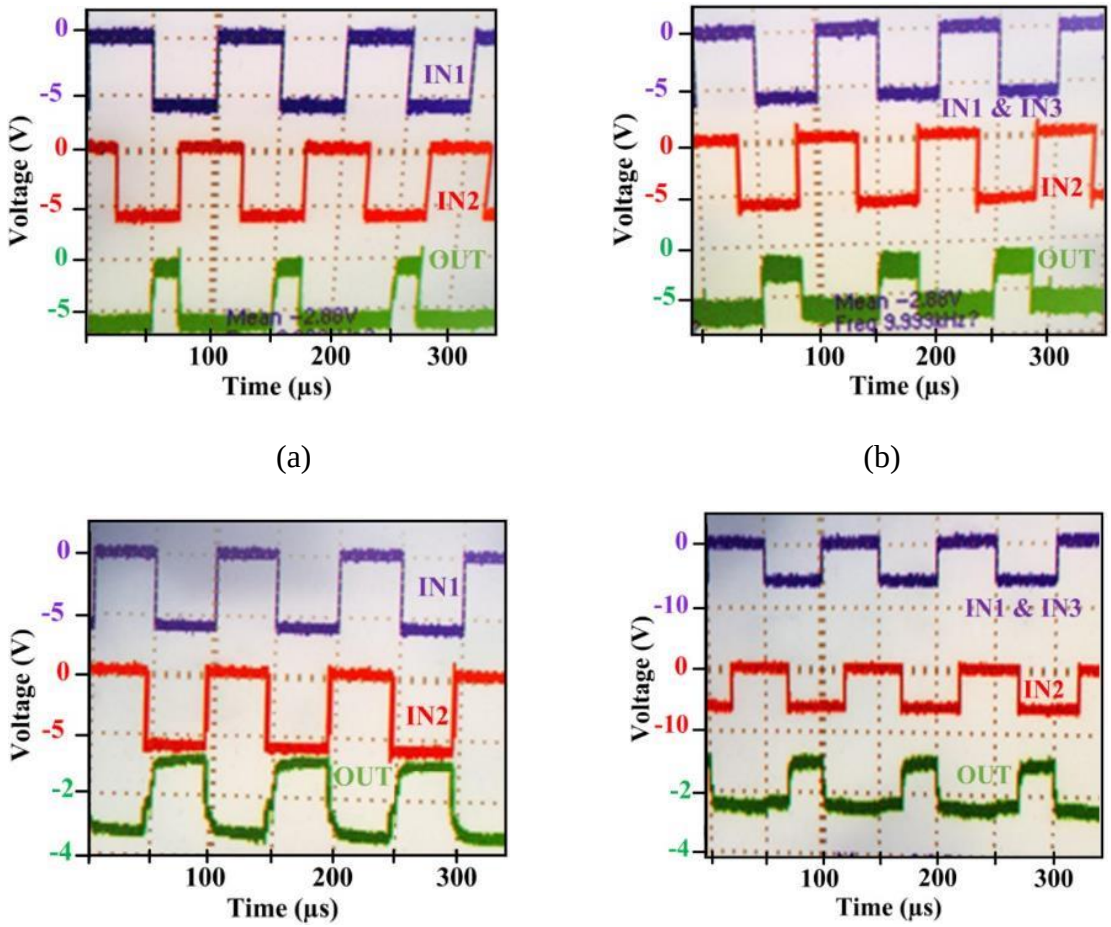
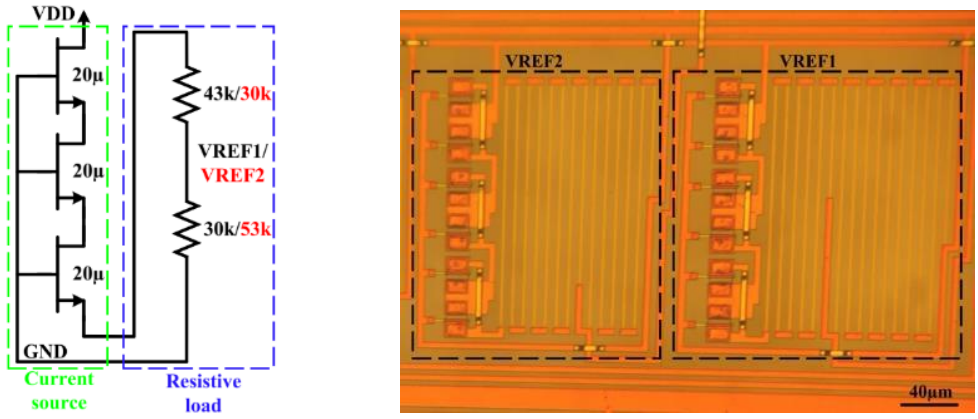



Figure 3.17: Measured dynamic characteristics of GaN NOR gates: (a) NOR-2IN at 25 $^{o}$C, (b) NOR-3IN at 25 $^{o}$C, (c) NOR-2IN at 300 $^{o}$C, and (d) NOR-3IN at 300 $^{o}$C.

### 3.5.2 Voltage reference:

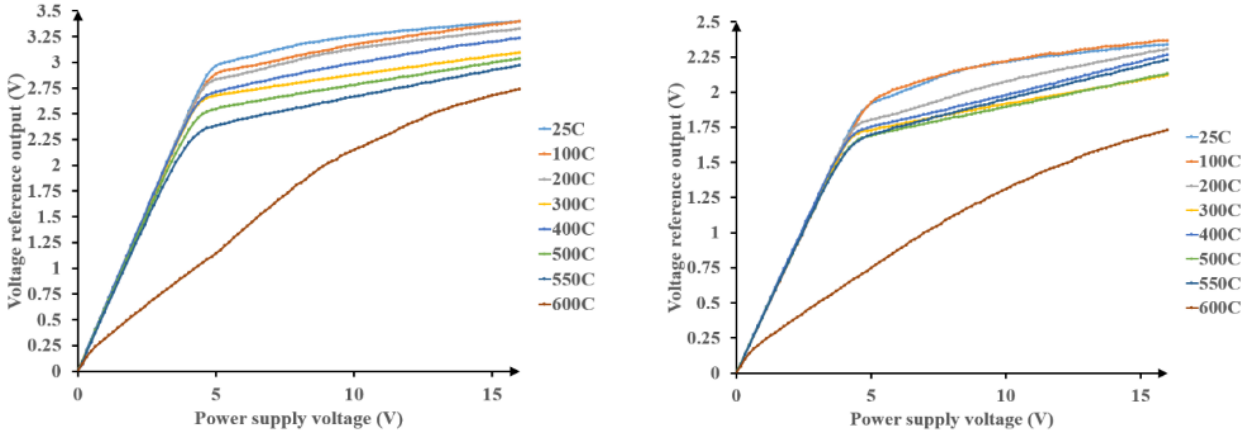
Another circuit embedded on the same chip is a voltage reference. This first reported voltage reference implemented with GaN devices is able to operate up to 550 $^{o}$C. It is built with three GaN500 devices and two resistors as shown in Figure 3.18. The idea behind the proposed voltage reference is based on using the GaN transistor in its saturation region (after $V_{DS}$ = 5 V) as a constant current source. The latter feeds a resistive load to generate a constant voltage. When the temperature increases, the decreasing current passing through the conductive channel of GaN is compensated by the increasing resistance of load resistors. Three GaN devices are connected in series to improve the stability of generated saturation current and to reduce its value. The load resistors are adapted to give the desired voltage reference.




(a) (b)

Figure 3.18: Integrated voltage references: (a) Schematic design, and (b) Micrograph.

As any reference circuit, when the supply voltage increases, the output voltage starts to increase and becomes stable after the supply reaches a certain threshold. Then, the output voltage remains constant over a range of supply voltages at a specific temperature. The experimental measurements shown in Figure 3.19 shows the outputs of the voltage reference with the supply voltage swept from 0 to 16 V at the wide temperature range between 25 $^{o}$C and 600 $^{o}$C. The results show that the reference voltage over the full temperature range until 550 $^{o}$C is more uniform at supply voltages above 4 V.




(a) (b)

Figure 3.19: Supply voltage dependence of the proposed voltage references in the temperature range 25- 600 $^{o}$C: (a) VREF1, and (b) VRREF2.

Two voltage references are required to operate other systems not mentioned in this work with VREF1 = 3.3 V and VREF2 = 2.3 V. The outputs of VREF1 and VREF2 at nominal supply voltage (14 V) over a temperature range of 25-600 $^{o}$C are shown in Figure 3.20. These references exhibit temperature coefficients TC1 = 293 ppm/$^{o}$C and TC2 = 242 ppm/$^{o}$C. Although these values do not match the performance of silicon bandgap references, they operate at much higher temperatures and are the first reported integrated references at such temperatures.

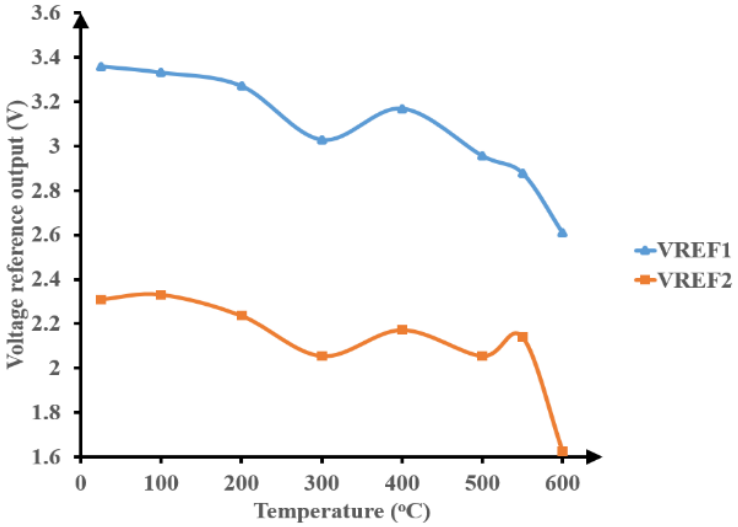



Figure 3.20: Experimental voltage reference outputs in the temperature range 25- 600 $^{o}$C.

## 3.6 Conclusion

This paper reports AlGaN/GaN depletion-mode JFET devices and integrated circuits that were successfully fabricated using the GaN500 technology provided by the National Research Council of Canada (NRC). Electrical characteristics of devices and integrated passive elements have been measured as a function of temperature, from 25 $^{o}$C to 600 $^{o}$C. Throughout the temperature range, the measured data is in good agreement with predictions of an improved version of Angelov model. In addition, we experimentally demonstrated prototype digital logic gates and voltage reference ICs implemented using GaN500. The prototype ICs are characterized at operating temperatures ranging from 25 $^{o}$C to 600 $^{o}$C. NOT, NAND and NOR logic circuits were tested and have very stable characteristics at temperatures up to 300$^{o}$C. The inverter remains functional with somewhat degraded characteristics up to 500 $^{o}$C. A proposed voltage reference circuit was fabricated and validated experimentally. It exhibits a stable operation at high-temperature up to 550 $^{o}$C.

This work is intended to be a contribution to the further development and improvement of GaN technology, especially for GaN-based wireless monitoring systems targeting high-temperature environments. The reported GaN basic logic gates enable further development of other essential dynamic blocks such as ring oscillators, D-Flip Flop, delays elements and other typical digital logic circuits able to operate at high temperature.

# CHAPTER 4 ARTICLE 2: GAN-BASED LSK DEMODULATORS FOR WIRELESS DATA RECEIVERS IN HIGH-TEMPERATURE APPLICATIONS

Ahmad Hassan [a,*], Mohamed Ali [a,b], Yvon Savaria [a], Mohamad Sawan [a]

[a] Department of Electrical Engineering, Polytechnique Montreal, QC H3T 1J4, Canada

[b] Microelectronics Department, Electronics Research Institute, Cairo, 12622, Egypt

This article addresses the second objective of this thesis, namely the design and implementation of GaN based building circuits. This paper was published in the Microelectronics journal (2019).

## 4.1 Abstract

GaN (gallium nitride)-based fully-integrated demodulators are presented. These modules, intended for wireless applications, target high-temperature (HT) environments including monitoring devices in aerospace. The presented demodulators are dedicated to recover Load-shift keying signals modulating a low carrier frequency to maximize power transfer efficiency and increase data transmission rate through metallic barriers. Logic gates are implemented and successfully tested at HT exceeding 400 $^{o}$C. Proposed demodulators are built from half and full bridge rectifiers, comparators, voltage references and inverters, and operate at a minimum carrier frequency ($f_c$) of 50 kHz. A demodulator based on a digital topology is proposed to cover MHz range $f_c$. A complementary ±14 V supply voltage is required to operate the circuits. Reported post-layout simulation results validate the functionality and performance offered by the proposed demodulators over the 25 $^{o}$C to 400 $^{o}$C temperature range. Also, a complete chip layout has been done, where the introduced demodulators occupy 10 mm$^2$ of a GaN die area.

**Index Terms:** High-temperature applications, wireless data transmission, GaN HEMT, integrated circuits, demodulation system.

## 4.2 Introduction

Implementing electronics that can operate in harsh environments, including high temperature (HT), is needed by many industries such as downhole oil and gas, aerospace and automotive. Cooling solutions for conventional electronics are not always possible and may have negative impact on system reliability and cost. For instance, during well logging, a failed electronics assembly on a drill string operating at deep underground level can take more than a day to retrieve and replace. In parallel, the cost for operating a complex deep-water offshore is around $1 M per day [2]. Further, influential corporations like AIRBUS, SAFRAN, and THALES are seeking alternative microelectronic technologies aiming for complete wirelessly controlled systems that can harvest power from the surrounding HT environment, exchange data through wireless links under HT conditions and be integrated in critical high-risk areas.

Among the available semiconductors dedicated for HT applications, wide bandgap (WBG) semiconductors are the main candidates in the foreseeable future to overcome the fundamental physical limits of the other electronics such as silicon on insulator (SOI), gallium arsenide (GaAs) and silicon germanium (SiGe), which are serving a relatively short range of temperature not exceeding 300 $^{o}$C and for limited operation time [28], [36], [41]. Silicon carbide (SiC) and gallium nitride (GaN) are the best-known WBG devices that offer attractive features suitable for HT conditions. These features include wide bandgap (3 eV), high-drift saturation velocity, high-thermal conductivity, and low-intrinsic carrier concentration [68].

Several studies have been done recently for SiC semiconductors at HT [10], [43], [49], [50]. However, the HT measurements are performed only for devices [43] and circuits [49]. Even in [50], the proposed system represents only the RF transmitter part, where the receiver is a Tektronix RSA3303B real-time spectrum analyzer. In addition, no commercially available SiC integrated devices and circuits operating at temperature higher than 300 $^{o}$C were found [12]. Moreover, the direct temperature dependence of carrier concentration, due to the bulk nature of the active region in SiC devices, is considered as a common shortcoming [13] in addition to the crystal dislocation disorders which degrade junction leakage, particularly at the highest temperatures.

III-Nitride and primarily GaN technologies exhibit substantial performance improvement over SiC semiconductor with respect to response speed and operating temperature limits [14]. In addition, the temperature stability of electron concentration in the HEMT channel makes GaN devices more

stable with respect to temperature. Despite considerable efforts to develop GaN devices dedicated to HT applications [14], [181], few researches are directed toward the development of integrated microelectronic circuits and systems based on GaN devices. Nowadays, the reported works show the implementation of simple circuits like inverter, comparator, ring oscillator, and one stage differential amplifier [13], [21], [22].

In our group, the HT characterization of AlGaN/GaN HEMT devices was successfully performed over a 25 °C to 400 °C temperature range as a first step to ensure the ability of using them in circuits and systems design dedicated to HT applications. All information regarding the fabrication process, materials of the characterized GaN devices and performed HT characterizations were reported in [124]. This GaN-based epitaxial layer Heterojunction FET technology is provided by the Canadian Photonics Fabrication Center of the Canadian National Research Council (NRC). This technology called (GaN500) offers 500-nm gate length transistors fabricated on 3-inch SiC wafers. The SiC substrate offers high-thermal conductivity and low-lattice mismatch to the GaN layer, which is compatible with HT applications. In addition to the active devices, the available technology allows the integration of some passive components (resistors, inductors, and capacitors).

In this paper, we present the design and implementation of three complete demodulation systems based on GaN500 technology. These proposed circuits demodulate LSK modulated signals for wireless monitoring applications operating in HT environment. We provide in Section 4.3 the main considerations about the adopted GaN technology and circuit design, in addition to the circuit level validation at 400 °C of GaN-based digital circuits. The building blocks, circuits and functionality of the proposed demodulators are discussed in Section 4.4, along with the impact of HT on them. Conclusions are the subject of Section 4.5 where our contributions are summarized.

## 4.3 Design considerations and digital circuits validation

Figure 4.1 shows a wireless power and data transmission system based on an inductive link. The power transfer path provides the supply voltage to a sensing device (pressure, temperature) located in a harsh environment. The data transmission path is based on the LSK modulation technique to reduce the complexity of the whole wireless power and data transmission system that operates through a single inductive coupling interface. In the transmitting side (secondary), the analog signal of the sensor is converted into digital data modulating the signal through a controllable switch.

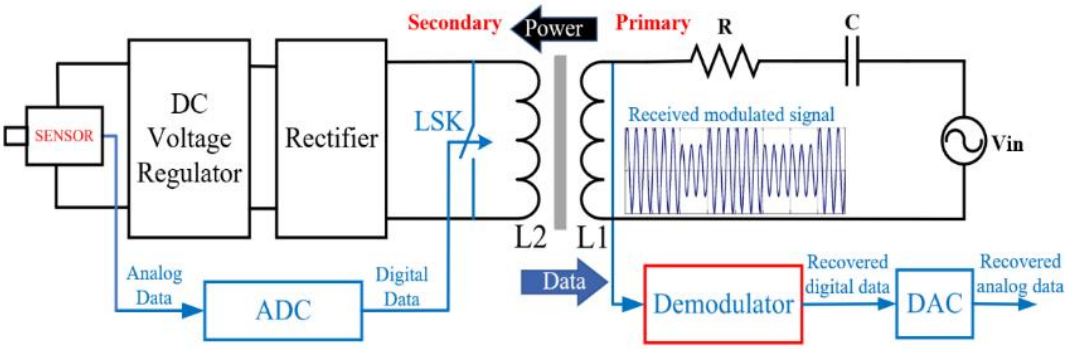



Figure 4.1: Block diagram of the proposed power and data transmission system

The demodulator, located on the receiving side (primary), detects the received modulated signal and recovers the expected digital data. The modulated signal (Figure 4.1) consists of two different amplitude voltage levels; high-level (data-on) and low-level (data-off). The voltage difference between data-on and data-off levels is strongly recommended to be as small as possible to maintain the highest power transfer efficiency during the data transmission process.

### 4.3.1 Design and technology considerations

The harsh environment condition of the targeted industrial applications is not only the high-temperature but also the metallic barrier between primary and secondary coils. That metallic barrier is an enclosure encapsulating hot high-pressure gases. This metallic barrier (hard steel that can sustain high pressure and high temperature) obviously has fairly high-electrical conductivity and high-magnetic permeability that induce high Eddy current losses and form a shielding zone for inductive fields, respectively. Therefore, the carrier frequency of the applied power signal should be relatively low to obtain enough power transfer efficiency while being sufficiently high to allow an adequate data transfer rate [125].

To endure the HT environment, a GaN500 technology is adopted to build the proposed demodulation system. In this implementation technology transistors are normally-on and they operate as depletion mode devices with a threshold voltage of -4 V. This imposes significant design constraints, in particular when the system specifications include limited power budget, and small-system geometry. Thus, it becomes a serious challenge to design a complete demodulation system based on this technology.

Considering the specifications and system constraints we based the circuit design on WBG normally-on devices [22, 50]. Then, a minimum number of transistors was used to obtain the desired functions and for better miniaturization of the complete system. Since GaN500 cells require VGS = -5 V to completely switch off the established channel, a negative input logic level is needed to drive the circuits which leads to the necessity of matching the input-output controlling signals. Level shifters are added to solve the incompatibility between the input and output levels and three supply voltage levels are used (VDD = +14 V, VSS = -14 V, and Gnd).

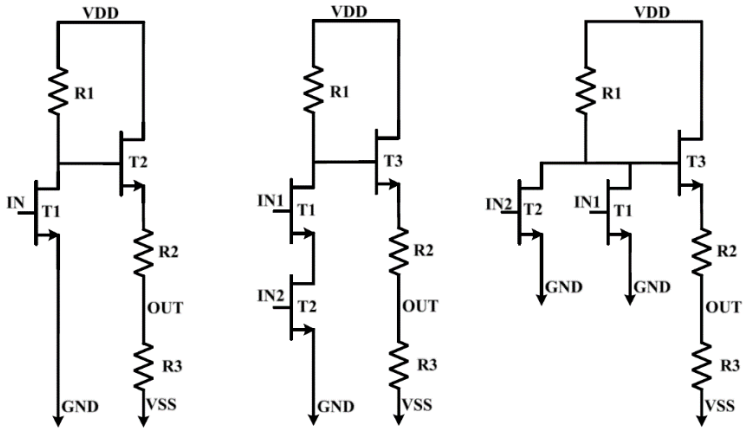
Despite the promising performance of GaN500 devices at HT, there is still an effective impact of environmental temperature on the active devices [124] and passive components (resistors). For this reason, the proposed design must consider the temperature induced parametric variations of the available components (active and passive) over the expected temperature range that spans from 25 $^{o}$C to 400 $^{o}$C. The Keysight Advanced Design System (ADS) kit was used to perform the design and simulation of proposed system where the transistor model (Angelov model configured with several parameters not visible to the user) includes the effects of self-heating and external applied temperature giving the opportunity to simulate the temperature impact on the circuits and system behavior. Similarly, based on the provided Thermal Coefficient of Resistance (TCR) of the integrated resistors (200 ppm/$^{o}$C), Equation (3.1) describes the change of resistance values over the temperature range.

$$R_t = R_0(1 + 2T10^{-4}) \quad (4.1)$$

Where $R_t$ is the actual resistance, $R_0$ is the resistance value at room temperature and T is the actual temperature ($^{o}$C).

### 4.3.2 Digital circuits validation at HT

To validate the concept, several GaN500-based logic gates were implemented and tested at several temperatures between 25 $^{o}$C and 400 $^{o}$C. The schematics of the implemented logic gates are shown in Figure 4.2. The experimental setup is depicted in Figure 4.3 where the GaN500 devices are wire-bonded to the pads of a ceramic HT package and HT wires are used to connect the package to the measurement devices.




(a) (b) (c)

Figure 4.2:Circuits of digital logic gates: (a) NOT, (b) NAND, and (c) NOR

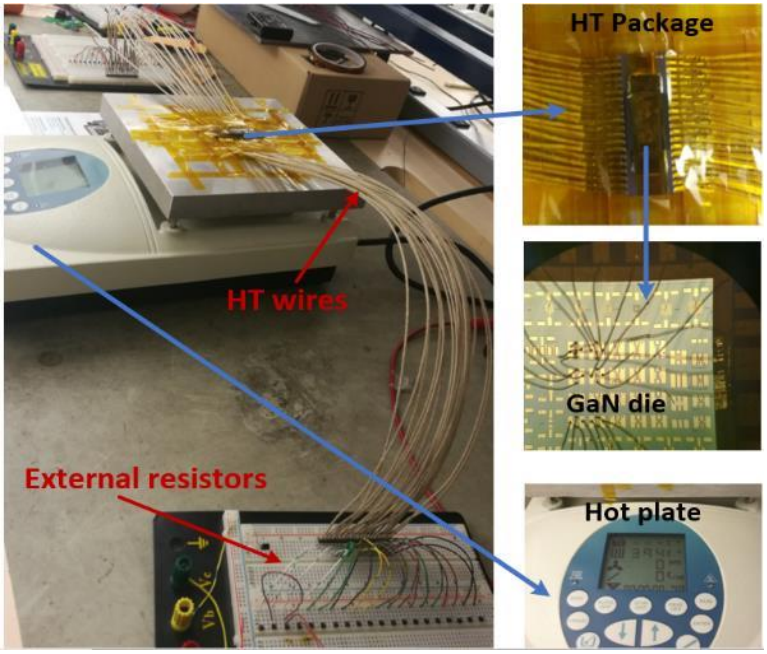



Figure 4.3:Circuits of digital logic gates: (a) NOT, (b) NAND, and (c) NOR

It is important to note that the GaN die that was used in those experiments comprises independent devices without resistors. Thus, external resistors were added to the test setup. Consequently, to perform a proper comparison between the experimental and simulation results, the temperature impact is applied only on GaN devices of the simulation kit, keeping the resistors at constant values. The measurements and simulation results are almost equal, thus showing the robustness and functionality over the wide temperature range tested for NOT, NAND and NOR gates as shown in Figure 4.4, Figure 4.5 and Figure 4.6 respectively.

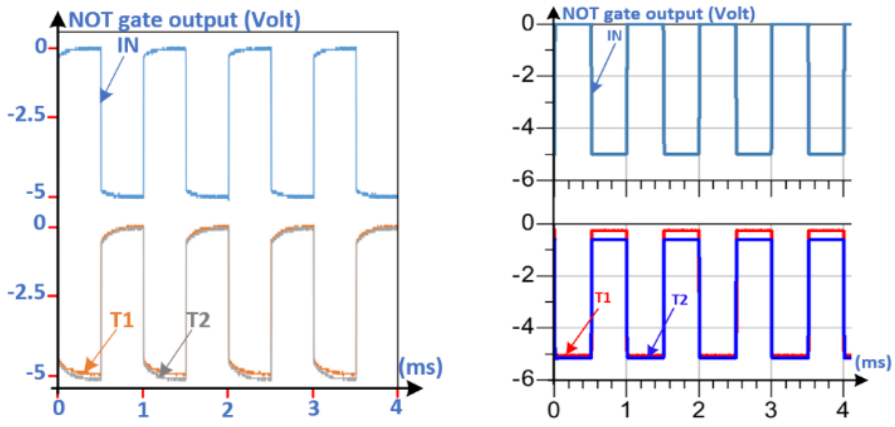
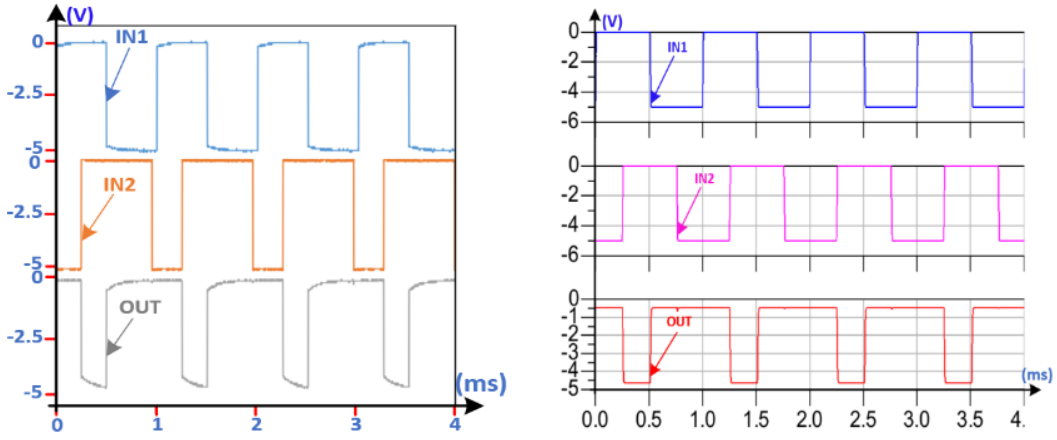
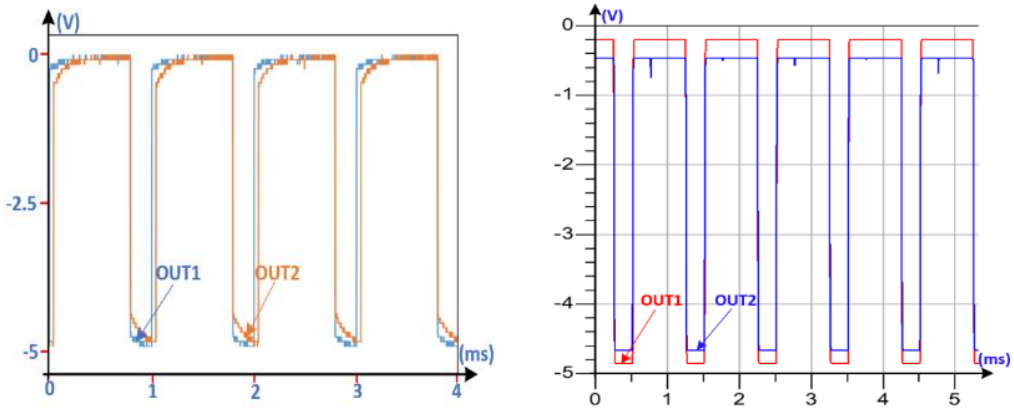



Figure 4.4: Experimental (left) and simulation (right) results of NOT gate at 25 $^{o}$C (T1) and 400 $^{o}$C (T2)

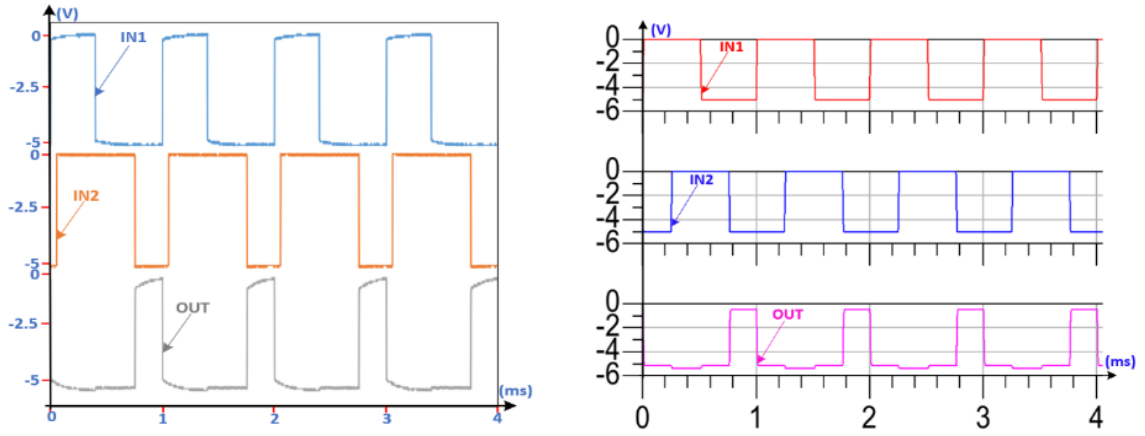



(a)

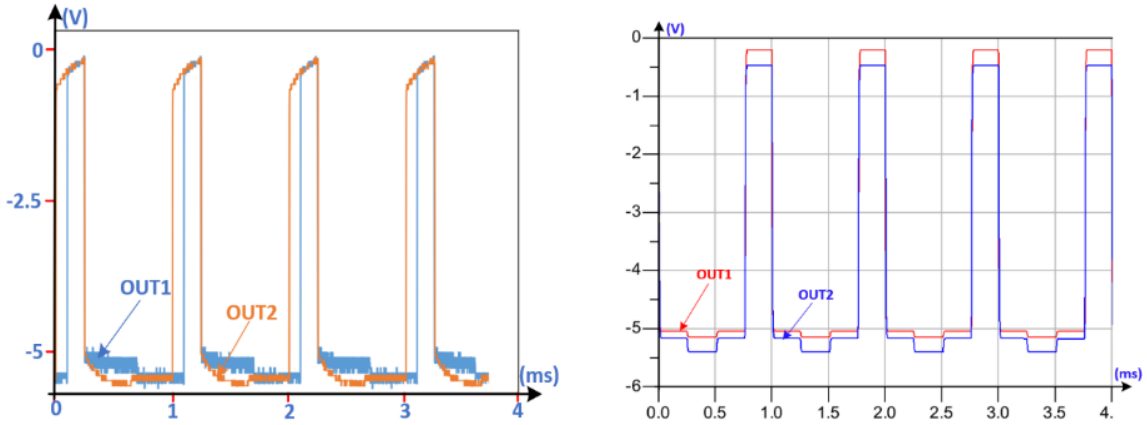



(b)

Figure 4.5: Experimental (left) and simulation (right) results of NAND gate: (a) at 400 $^{o}$C, (b) at 25 $^{o}$C (OUT1) and 400 $^{o}$C (OUT2)




(a)




(b)

Figure 4.6: Experimental (left) and simulation (right) results of NOR gate: (a) at 400 ºC, (b) at 25 ºC (OUT1) and 400 ºC (OUT2)

Table 4.1 summarizes features of the implemented circuits based on GaN technology targeting HT applications, and it compares them with the only three published works that were found [13], [21], [22]. To the best of our knowledge, none of these teams have reported system level design or implementation.

Table 4.1: GaN-based circuits for HT applications

| | **This work** | **[13]** | **[21]** | **[22]** |
|---|---|---|---|---|
| **Circuit** | NOT, NAND and NOR gates | Dif. Amp. and NOT gate | NOT gate | NOT gate and ring oscillator |
| **Tech.** | AlGaN/GaN | AlInN/GaN | AlGaN/GaN | AlGaN/GaN |
| **Foundry** | NRC | Inhouse | Inhouse | Inhouse |
| **Temp. (ºC)** | 400 ºC | 500 ºC | 300 ºC | 256 ºC |

## 4.4 Proposed demodulation systems

### 4.4.1 Building blocks and functionality

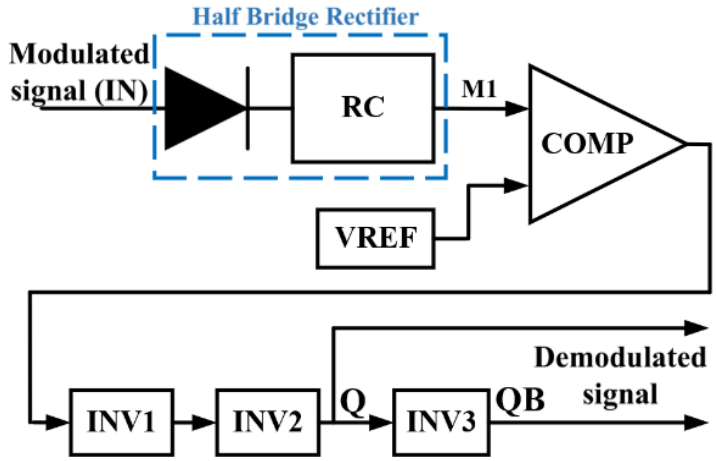
Figure 4.7 presents the block diagram of the three proposed demodulation systems. The first demodulator is presented in Figure 4.7(a) where the modulated signal (IN) is applied to a half-bridge rectifier (HBR) followed by a bank of RC circuits that play the role of envelope detector and that shape the modulating signal (M1). The latter is compared to a reference voltage (VREF = 2.6 V) using a comparator block. Three inverters (INV1, INV2 and INV3) are used to sharpen the comparator output signal and to generate the initial digital data (Q) along with its complementary signal (QB). Q and QB are needed by a DAC block (Figure 4.1) to recover the initial analog signal. The building circuit schematics of the half bridge rectifier (HBR) demodulator are provided in Figure 4.2(b) (2IN-NAND) and Figure 4.8(a) (half bridge rectifier), Figure 4.8(b) (voltage reference) and Figure 4.8(f) (comparator).

The minimum carrier frequency that could be handled by the HBR demodulation system is 60 kHz. Lower than this limit, the difference between data-on and data-off signals provided by the HBR could not be sensed by the comparator. To go beyond this limit, a full bridge rectifier (FBR) is utilized instead of the HBR keeping the remaining building circuits without any change (Figure 4.7(b)). The FBR demodulation system operated properly at a carrier frequency as low as 50 kHz.

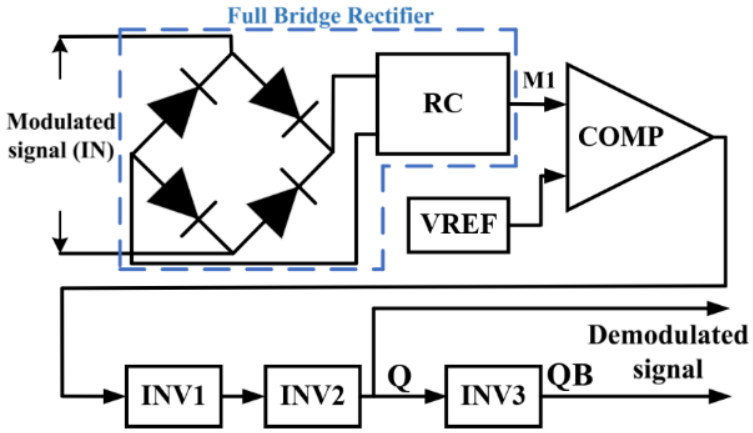
Another demodulator is fully based on digital circuits and is proposed for high carrier frequency applications (in the range of MHz). The block diagram of this digital demodulator is presented in Figure 4.7(c). The novel idea of this demodulator is to use an inverter (INV4) which is carefully designed to detect only the data-on (high-amplitude voltage) and discard the data-off (low-amplitude voltage) of modulated signal. On the other hand, INV5 is used to switch continuously in both data-on and data-off cases to generate the clock signal of D-Flip Flop. This clock signal is delayed by the DELAY block to ensure matching with the detected data signal. For lower carrier frequency operation (range of kHz), a longer delay should be designed.

Figure 4.2(a) (NOT) combined with Figure 4.8(d) (D-Flip Flop) and Figure 4.8(e) (delay) shows the building circuit schematics of the digital demodulator. A long chain of inverters (20 stages) is utilized to design the DELAY block (Figure 4.8(e)) and the D-Flip Flop design is based on five 2-

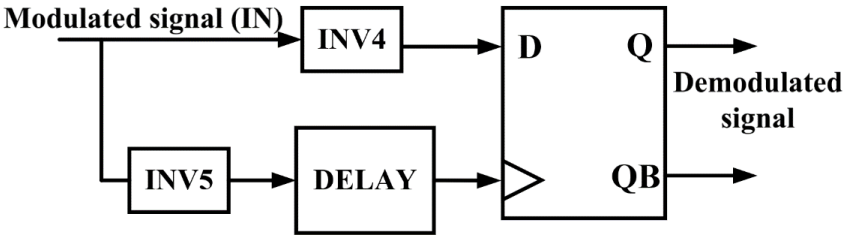
input and one 3-input NAND logic gates, where the corresponding schematic design is shown in Figure 4.2(b) and Figure 4.8(c), respectively.




(a)




(b)




(c)

Figure 4.7: Block diagrams of the proposed demodulators: (a) Half-bridge rectifier, (b) Full-bridge rectifier, and (c) Digital based

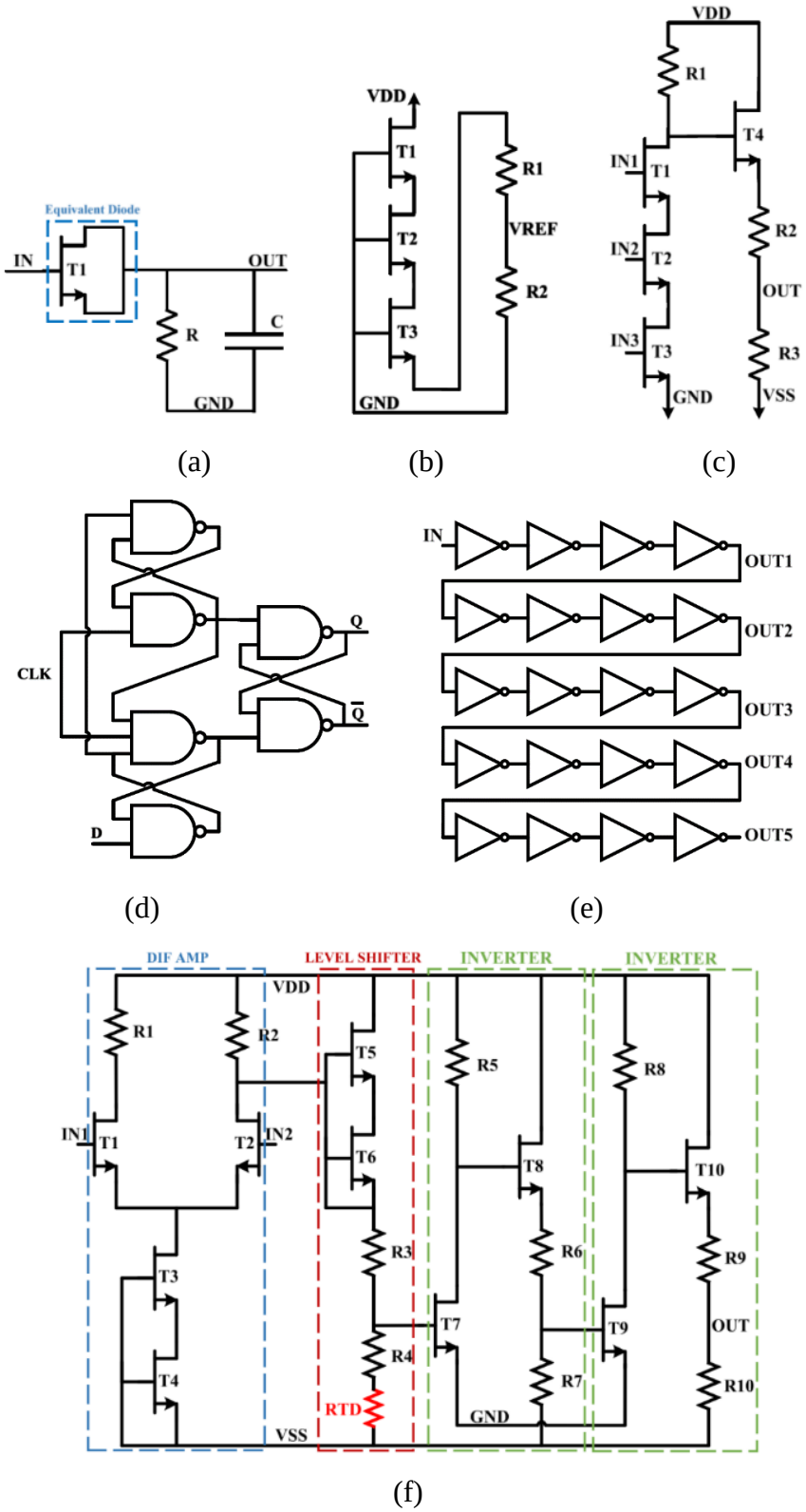
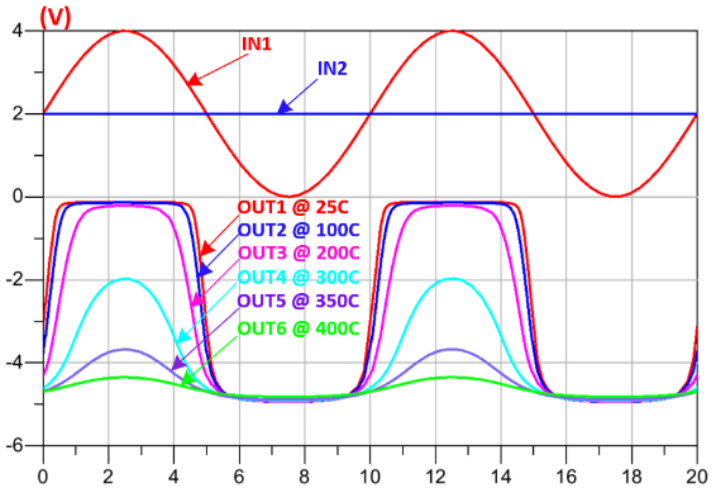


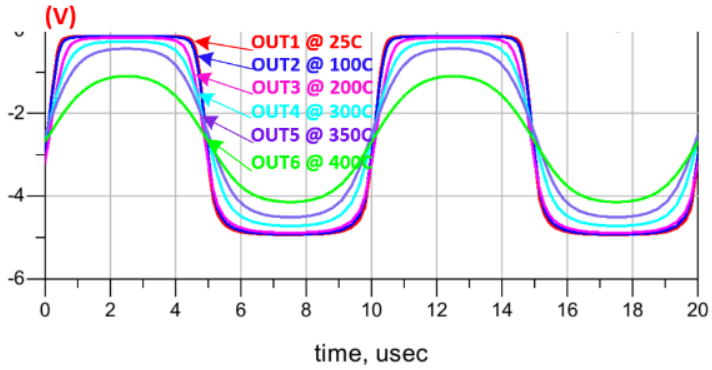

Figure 4.8: Building circuits: (a) Half bridge rectifier, (b) Voltage reference, (c) NAND (3IN), (d) D-Flip Flop, (e) Delay, and (f) Comparator

### 4.4.2 Simulation results

During the investigation of HT impact on the performance of each building circuit, we noticed that the comparator is the block most affected by HT operation, much more than the other circuits. As can be seen in Figure 4.9(a), the comparator output fails dramatically after 250 $^{o}$C. The circuit analysis shows the sensitivity of the comparator performance with the value of R4 (Figure 4.8(f)). A resistive temperature detector (RTD) [50] is added in series to R4 to compensate the temperature impact. Due to its high-temperature coefficient and very linear temperature response from room temperature up to 500 $^{o}$C, the RTD made of platinum is an ideal candidate for our case. The new performance of the adapted comparator is presented in Figure 4.9(b).



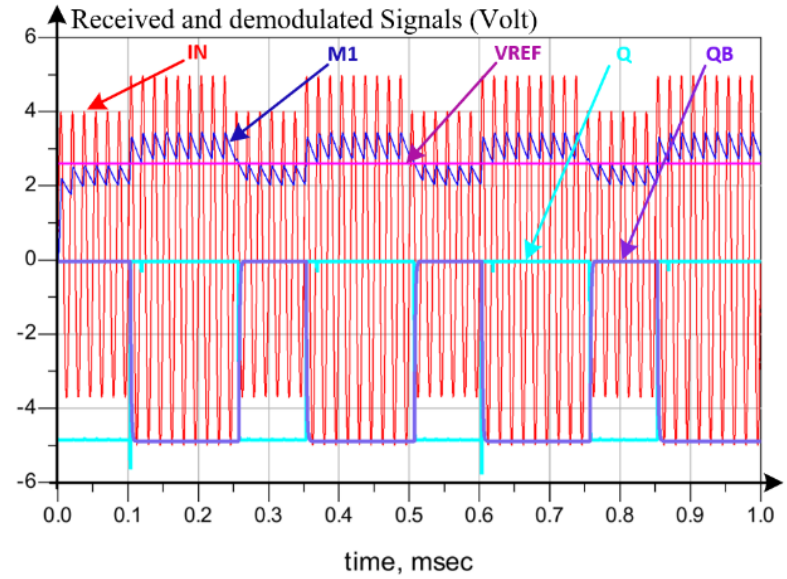

(a)



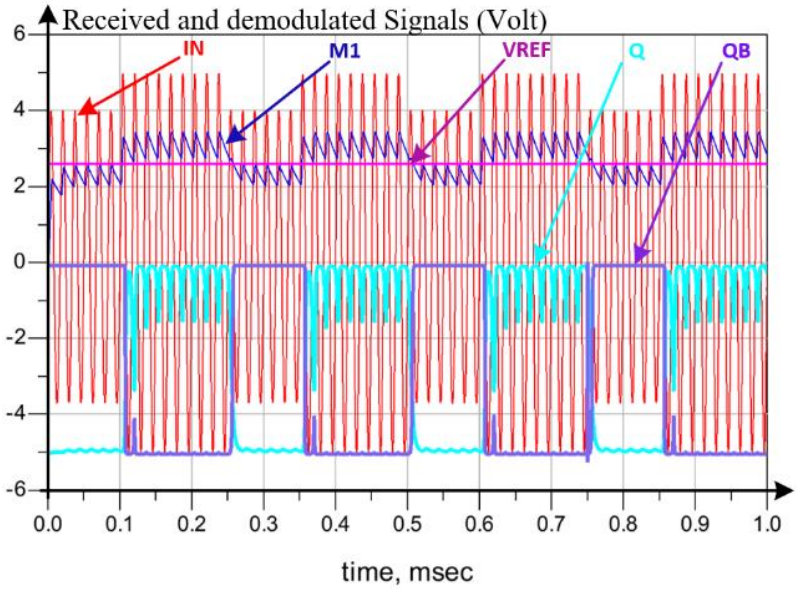

(b)

Figure 4.9: Comparator simulations at different temperatures: (a) Without adaptation, and (b) With adaptation

To validate the three proposed demodulators, a modulated signal (IN) is applied to retrieve the demodulated signal (Q) and its complement (QB). The system analysis shows that the minimum amplitude of the data-on signal is ±5 V. This means that, to reach a higher power transfer efficiency, the amplitude of the data-on signal could be increased more than ±5 V as much as needed until reaching the required power transfer efficiency, without applying any change on the proposed demodulators.




(a)

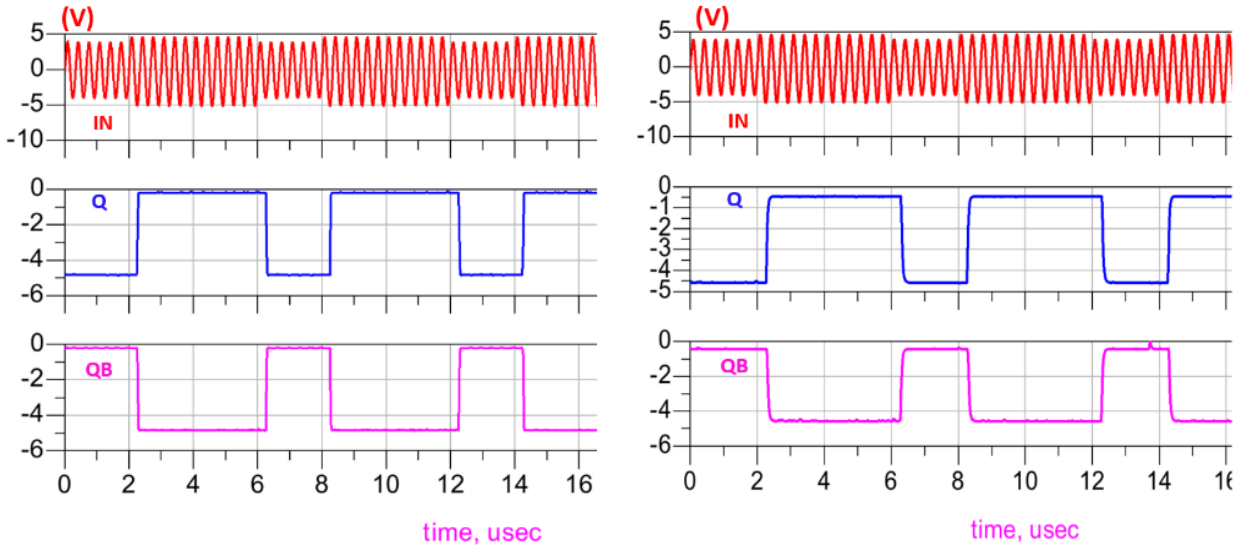



(b)

Figure 4.10: HBR demodulator simulation results at: (a) 25 $^{o}$C, and (b) 400 $^{o}$C

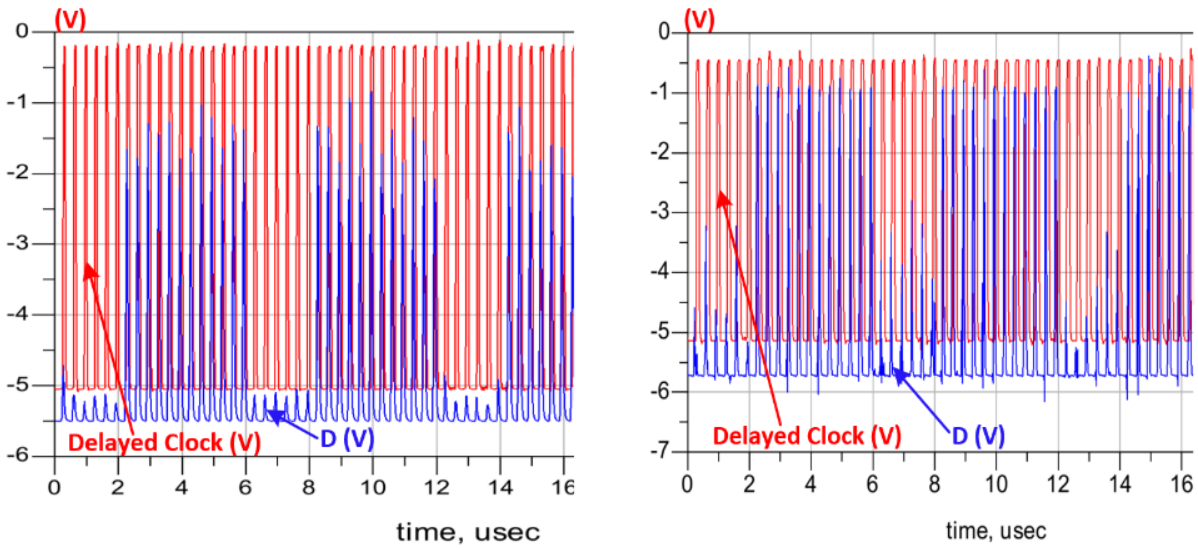
In parallel, the maximum amplitude of the data-off signal is ±4 V and it could be less than that, but it would reduce the power transfer efficiency. Therefore, the modulated signal (IN) is selected with high-amplitude of ±5 V (minimum data-on) and low-amplitude of ±4 V (maximum data-off) to show the performance of modulators at the critical case. Consequently, a 1.0 V amplitude difference (20% of the maximum amplitude) reached between the high-amplitude (data-on) and low-amplitude (data-of) of the modulated signal (IN) with the proposed demodulators.

Figure 4.10(a) presents the transient performance of the HBR demodulator at 25 $^{o}$C. To ensure the reliability of the proposed demodulation system, simulations were repeated after applying the HT GaN500 model (Angelov model) and resistor values (using equation (3.1)). At carrier frequency 60kHz, the simulation results at 400 $^{o}$C shown in Figure 4.10(b) are compatible with the results at 25 $^{o}$C in Figure 4.10(a) except for the ripples in the recovered signal (Q). These ripples could be easily solved by adding a small capacitor (C = 10 pF) at the output of INV2. Similar simulation results were obtained with the FBR demodulation system at a carrier frequency of 50 kHz. In parallel, the simulation results of the digital demodulator with carrier frequency of 4 MHz are presented at 25 $^{o}$C and 400 $^{o}$C in Figure 4.11(a) and Figure 4.11(b) respectively, where an excellent stability is shown. The detected data (D) of inverter (INV4) is presented in Figure 4.12(a) and (b) at 25 $^{o}$C and 400 $^{o}$C respectively, along with the delayed clock signal generated from inverter (INV5).




(a) (b)

Figure 4.11: Digital demodulator simulation results at: (a) 25 $^{o}$C, and (b) 400 $^{o}$C




(a) (b)

Figure 4.12: Delayed clock and detected data intersection at: (a) 25 $^{o}$C, and (b) 400 $^{o}$C

A complete chip layout (Figure 4.13) for the three proposed demodulators was performed. The overall area of the chip is 4.0 mm x 2.5 mm. Table II summarizes the operating frequency, power consumption and occupied area of each module. The high-power consumption and large area of the digital demodulator are due to the Delay block which should be optimized in future work. As shown in Table 4.2, the HT has a positive impact on power consumption especially for HBR and FBR demodulators with power reduction of more than 40% at 400 $^{o}$C.

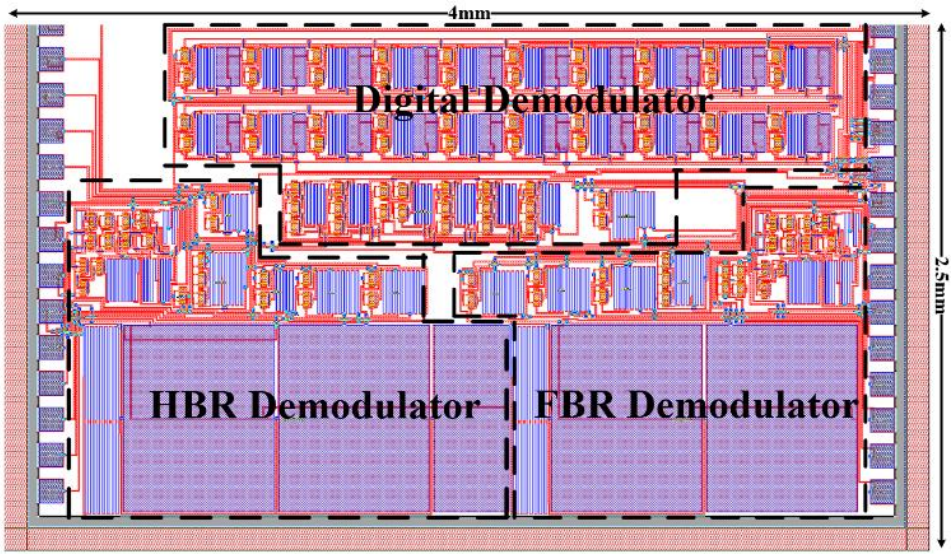



Figure 4.13: Chip layout view of the proposed data transmission systems

Table 4.2: Power consumption and area of proposed demodulators

| **Demodulator** | **Frequency (MHz)** | **Power (W) @ 25 °C/400 °C** | **Area ($mm^2$)** |
|---|---|---|---|
| HBR | >0.06 | 0.77/0.42 | 2.24 |
| FBR | >0.05 | 0.84/0.46 | 1.9 |
| Digital | >1 | 4.3/4 | 2 |

## 4.5 Conclusion and future work

The design and implementation of three different demodulators based on GaN500 devices are described. The introduced building blocks are designed to fit into wireless power and data transmission systems based on the LSK modulation technique targeting harsh environments and high temperature application HT environment. The design considerations of the proposed modules are discussed considering the specific requirements of the targeted applications and the limitations of adopted technology. Circuit validation of GaN-based logic gates was performed at 400 $^{o}$C. Simulation results of proposed systems were performed to ensure their functionality over wide temperature range between 25 $^{o}$C and 400 $^{o}$C. Future work includes circuit design optimization to reduce the power consumption.

# CHAPTER 5 ARTICLE 3: A GAN-BASED WIRELESS MONITORING SYSTEM FOR HIGH-TEMPERATURE APPLICATIONS

Ahmad Hassan [1,*], Mohamed Ali [1,2], Aref Trigui [1], Yvon Savaria [1], and Mohamad Sawan [1,3,4]

[1] Department of Electrical Engineering, Polytechnique Montreal, QC H3T 1J4, Canada;

[2] Microelectronics Department, Electronics Research Institute, Cairo, 12622, Egypt;

[3] School of Engineering, Westlake University, Hangzhou 310024, China;

[4] Institute of Advanced Study, Westlake Institute for Advanced Study, Hangzhou 310024, China;

This article addresses the third objective of this thesis, namely the design and implementation of fully integrated GaN based modulation and demodulation systems. It is an invited paper to the Special Issue on "Advanced Interface Circuits and Systems for Smart Sensors" of Sensors Journal. This paper was published in Sensors journal (14 April 2019).

## 5.1 Abstract

A fully-integrated data transmission system based on GaN (gallium nitride) HEMT (high-electron-mobility transistor) devices is proposed. This system targets high-temperature (HT) applications, especially those involving pressure and temperature sensors for aerospace in which the environment temperature exceeds 350 ºC. The presented system includes a front-end amplifying the sensed signal (Gain of 50 V/V), followed by a novel analog-to-digital converter driving a modulator exploiting the Load-Shift Keying technique. An oscillation frequency of 1.5 MHz is used to ensure a robust wireless transmission through metallic-based barriers. To retrieve the data, a new demodulator architecture based on digital circuits is proposed. A 1 V amplitude difference can be detected between a high-amplitude (data-on) and a low-amplitude (data-off) of the received modulated signal. Two high-voltage supply levels (+14 V and -14 V) are required to operate the circuits. The layout of the proposed system was completed in a chip occupying 10.8 $mm^2$. The HT characterization and modeling of integrated GaN devices and passive components are performed to ensure the reliability of simulation results. The performance of the various proposed building blocks, as well as the whole system, have been validated by simulation over the projected wide operating temperature range (25-350 ºC).

**Keywords:** High-temperature applications; Wireless data transmission; GaN HEMT; Integrated circuits; Harsh environment.

## 5.2 Introduction

Monitoring some critical parameters, such as temperature and pressure, in industrial applications is needed to control sensitive areas like combustion engines, gas turbines and oil wells. Placing sensors in harsh environments allows more accurate measurements to be made. However, it is still a very challenging task especially at extremely high temperatures and pressures. In addition, many systems in industrial applications operate in multi harsh environment situations, such as in combustion engines, where the high temperature is often directly proportional to the high pressure. Therefore, it becomes necessary to develop advanced harsh environment sensing technologies.

Silicon Carbide (SiC) based piezoresistive and capacitive sensors as well as polycrystalline diamond sensors are suitable for high-temperature (HT) and high-pressure (HP) measurements [182], [183]. However, the output signal of these types of sensors is usually low and requires considerable embedded signal conditioning electronics. Platinum-based thermocouples are stable at extreme temperatures up to 2000$^{o}$C. However, their sensitivity is normally low and could be seriously affected by induced common-mode noise. Optical fiber sensing technology is a promising solution for HT and HP measurements. It is favorable because of the HT capability of optical fibers up to 1000$^{o}$C [184], [185], in addition to their small size, light weight and resistance to electromagnetic interference (EMI). However, special housing for optical fibers is required at HT. This affects the applicability of optical sensors in several harsh environments.

Moreover, in many cases, sensors placed in harsh environments are frequently isolated from their control or power management units, which is usually located outside the harsh zone [3]. Commonly, these entities are interconnected with regular wires. However, these wired connections present many challenges in harsh environments for preserving system light weight, simplicity and low-cost system implementation. In addition, drilling holes through the separation medium which is mostly metallic is not always an acceptable solution giving the potential risk of toxic chemicals leakage, pressure or vacuum loss, and mechanical structure integrity weakening.

As a solution of this problematic, passive wireless sensing technologies in extreme environments have been investigated. Surface acoustic wave (SAW) sensors have been demonstrated at HT up

to 800ºC [186], [187]. However, SAW sensors are very sensitive to the variation of material properties that is expected in harsh environments. Another possible solution is RF coupling sensors with a LC resonator circuit installed in the harsh environment [188]. The main drawback of RF coupling sensors is their limited HT capability, in addition to their sensitivity to EMI.

To address the aforementioned hindrances, a promising solution is to build an integrated microelectronic-based wireless transmission system. The transmission part of proposed integrated system is embedded along with the sensor interface into the harsh environment. The acquired information by the sensor interface is processed by the microelectronic system and wirelessly transmitted to an external receiver. However, when the high environmental temperature exceeds around 150ºC-175ºC, traditional Si-based systems are no longer able to fit the requirements, due to the effective impact of high temperatures (HTs) on the physical and electrical behavior of the technology used.

A possible solution is to provide cooling systems. However, such solutions introduce complexity in terms of added components and wires that increase weight and size, which is often not acceptable, especially in aerospace applications. Therefore, several influential corporations like AIRBUS, SAFRAN, and THALES are seeking alternative microelectronic technologies that can work under HT conditions to develop wirelessly controlled systems that can harvest power from the surrounding HT and exchange data through wireless links [10], [124], [125]. Available semiconductors dedicated to HT applications, such as silicon on insulator (SOI), gallium arsenide (GaAs), and silicon germanium (SiGe) are serving a relatively short range of temperature not exceeding 300 ºC and for limited operation time [10], [28], [36], [41], while the real industrial requirements can be much higher than this limit.

Wide bandgap (WBG) semiconductors are main candidates in the foreseeable future to overcome the fundamental limits of available conventional electronics in HT applications [10], [61]. Silicon carbide (SiC) and gallium nitride (GaN) are the best-known WBG devices that offer attractive features suitable for HT conditions. These features include wide bandgap (3 eV), high drift-saturation velocity, high thermal-conductivity, and low intrinsic carrier concentration [68]. Although GaN and SiC belong to the same WBG semiconductors family and share similar attractive properties, SiC has received a great deal of attention in the past decade, especially in the high temperature applications field. Several research results have been recently reported on

developing SiC based ICs for HT applications. For instance, multistage digital and analog SiC-ICs using 4H-SiC MESFETs are demonstrated in [11] showing correct operation at 300ºC. Seventeen circuits implemented with the Raytheon's 4H-type HTSIC process were reported in [47] and successfully tested at 300ºC. In [168], HT voltage and current references are designed with a silicon carbide CMOS process. Their operation and stability were reported in the 25ºC to 540ºC temperature range. Using 6H-SiC depletion-mode JFET transistors, the design characterization of various logic circuits (inverter, NAND, and NOR) were reported in [169] at extreme temperatures reaching 550ºC. In [170], low-voltage 4H-SiC n-p-n bipolar devices are used to implement OR–NOR gates and a three-stage ring oscillator. The integrated circuits have been successfully tested up to 300ºC. Based on 6H-SiC n-channel depletion-mode JFETs, differential amplifiers were successfully fabricated for use in HT differential sensing [171]. The reported circuits were characterized at temperatures reaching 450ºC. A simple analog amplifier and a NOT logic gate reported in [46] were fabricated using 6H-SiC JFET technology and were successfully operated for thousands of hours at 500ºC. Authors in [173] report the first analog-to-digital converter (ADC) implemented using SiC along with the first CMOS digital-to-analog converter (DAC). These circuits were tested in the 25ºC to 400ºC temperature range.

Although remarkable advances have been achieved, the development of SiC-based systems dedicated for sensing applications is still at its early beginning. Indeed, the majority of the reported SiC ICs are realized with either small number of implemented devices or on large integrated areas having low density of device integration. There are still many obstacles limiting widespread adoption of SiC sensing systems, including immature foundry processes, design kits and device models. Only in [189] and [50] of integrated SiC-based wireless sensing systems were reported for temperature and pressure measurements respectively. The developed RF transmitters were successfully demonstrated from 25°C to 450°C. However, the proposed system represents only the RF transmitter part, where the receiver is a Tektronix RSA3303B real-time spectrum analyzer. In addition, the EMI effect on the wireless transmission performance was not investigated in spite of the expected metallic environment between the transmitter and receiver.

On the other hand, III-Nitride technologies, primarily GaN, exhibit substantial performance improvements over the other semiconductors with respect to response speed and operating temperature limits [14], in addition to the temperature stability of electron concentration in the HEMT channel that makes GaN devices more stable over wide temperature ranges. Despite

considerable efforts to develop GaN devices operating at HT above 600°C [14], 800°C [18], 900°C [19] and 1000°C [20], few research projects are directed toward the development of integrated microelectronic circuits and systems based on GaN devices.

To the best of our knowledge, none of the previously reported results relate to system level design or implementation. The reported works only show the implementation of simple circuits like inverters, comparators, ring oscillators, and one stage differential amplifiers [13], [21], [22]. In [13], a GaN-based enhancement/depletion (E/D)-mode inverter was successfully fabricated and tested from room temperature to 300°C. GaN heterojunction FET (HFET) depletion mode devices are used in [21] to implement various circuits: Not gate, comparator, ring-oscillator and frequency divider. A 31-stage ring-oscillator was tested at temperatures reaching 265°C and it was shown that this circuit returns to the original performance after returning to room temperature. A novel AlInN/GaN based IC was demonstrated in [22]. The fabricated ICs comprise an inverter and a differential amplifier that showed stable performance up to 500°C.

In this paper, we present the complete design of a wireless data transmission system based on GaN500 technology that is proposed to acquire signals from sensors installed in HT environments and transmit the data through an inductive link to an external receiver. We focus on the electronic part, including the transmitter and the receiver, rather than on the sensor interface itself. The main goal is to implement a generic integrated system that could be utilized in different types of harsh environment sensors, including pressure and temperature sensors, with minor adaptation. Section 5.3 includes the description of the proposed system. The HT modeling and characterization of GaN devices and passive elements are presented in Section 5.4. The main considerations about the adopted GaN technology and the circuit building blocks are described in Section 5.5, along with corresponding simulation results. Conclusions are the subject of Section 5.6.

## 5.3 Proposed wireless system:

Typical monitoring sensors in HT applications require two types of connections; a power source coming from an external power supply and the data connection to send the data monitored by the sensor interface to the external system. In addition, most of the harsh environment sensors are installed into compact metallic capsules. For this reason, different techniques have been adapted for transmission through metallic barriers [3] for example RFID [190], planar IPT [5] and

piezoelectric ultrasound [7]. However, these approaches are limited due to the low-transfer efficiency and are restricted to specific applications (soft and thin metals).

Furthermore, harsh environment conditions intensively affect the curie point of piezoelectric materials at which their functionality is lost. In addition, the system performance of ultrasound techniques is highly reliant on the coupling quality and requires a direct grounding through the metal wall. A weak coupling leads to significant impedance mismatch over the acoustic-electric channel and causes a direct drop in the power-transfer efficiency and transmission data rate. Moreover, an inductive power transfer (IPT) system is rarely used to transfer power through a metallic medium, due to the high electrical conductivity that induces high Eddy current losses, and also due to the high magnetic permeability of metal walls, which form a shielding zone for inductive fields.

However, in our previous work [125], we described the design of a robust inductive link that can wirelessly transmit power to pressure and temperature sensors installed in harsh environments. The link was designed to operate at temperatures up to 500°C and pressure differential of up to 100 Bar. Different materials were evaluated, including Titanium and steel, and their properties were investigated.

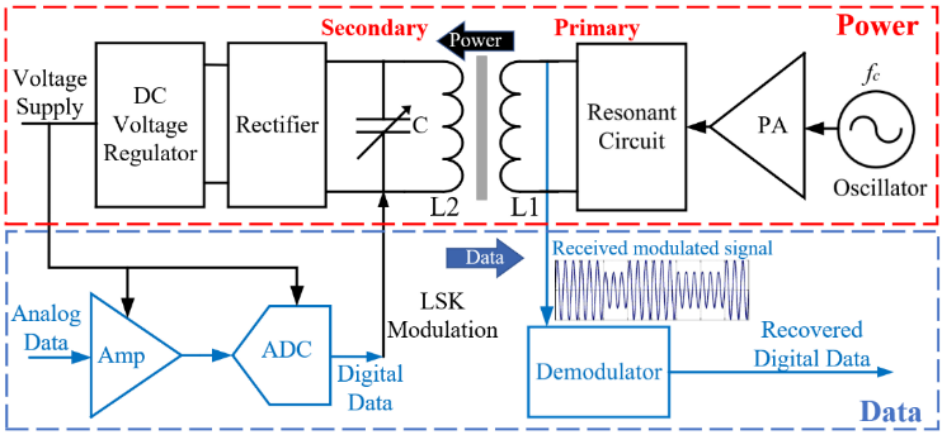



Figure 5.1: Block diagram of the proposed power and data transmission system.

Figure 5.1 shows the proposed wireless power and data communication system based on an inductive link to transmit power and data through a metallic barrier. The work presented in this paper deals only with the data path linking a low-amplitude analog signal provided by a sensor interface (on the secondary side) to the delivered data on the primary side. The amplified signal is then applied to an analog-to-digital converter (ADC) to provide a digital signal that can modulate

the power signal coming from the primary inductive coil using Load Shift Keying (LSK). On the primary side, the demodulator block detects the modulated signal and recovers the transmitted digital data.

Load-shift keying modulation is a technique that produces a variation in a secondary circuit impedance that is reflected as a variable impedance in a primary circuit. This impedance change allows recovering digital data that is virtually transmitted from one side to the other side of the inductive link by sensing the reflected impedance variations. In our system, the inductive link used to deliver power from an external system is the same path that can be utilized to send back the data coming from the sensor. Therefore, LSK modulation is used to ensure simplicity of the wireless path implemented using a single inductive link providing power and data transmission.

## 5.4 Modeling and Characterization:

The technology adopted to implement the proposed GaN-based data communication system is the GaN500 HEMT provided by the Canadian Photonics Fabrication Center (CPFC) of the National Research Council of Canada (NRC). This technology is fabricated on 3-inch silicon carbide (SiC) wafers of 75 µm thickness. It features 0.5 µm long metal gates, two metal layers (1ME and 2ME) for interconnect, 50 Ω/sq nichrome resistors, and MIM capacitors (0.19 fF/$\mu m^2$). The SiC substrate offers high-thermal conductivity and small lattice mismatch to a GaN layer, which is compatible with high-temperature applications. The transistors are field-plated designs that exhibit much lower gate leakage current and higher breakdown voltage than non-field plated devices.

The design and simulation of the proposed wireless system are completed under the Keysight's Advanced Design System (ADS) tool using the NRC Gallium Nitride MMIC Foundry Design kit (GaN500v3.10). This kit provides a transistor based on Angelov model that integrates temperature effects and can be used to simulate the impact of internal self-heating and external ambient temperature on the behavior of simulated circuits. However, in this GaN500v3.10 design kit, the Angelov model of GaN500 device was not validated at temperature higher than 200$^o$C and the passive components were assumed to have values constant with temperature. Therefore, we performed the HT characterization of GaN500 devices and passive elements to validate the Angelov model at HT and we developed an accurate model of passive elements that enables simulating the temperature effects on the proposed design.

### 5.4.1 GaN500 HEMT

To ensure the validity of the available transistor model over the desired temperature range, we performed the HT I-V characterization of several fabricated GaN500 devices at various temperatures ranging from 25 $^{o}$C to 350 $^{o}$C. The experimental setup that was used is depicted in Figure 5.2 that shows GaN500 devices wire-bonded to the pads of a ceramic HT package and HT wires that are used to connect the package to the measurement devices.

High-temperature experiments were performed using a hot plate providing temperatures controllable over time. Temperatures were cycled between room temperature (25 $^{o}$C) and 400 $^{o}$C. An infrared thermometer and a direct-contact thermocouple were utilized to measure the operating temperature of the tested die surface that was used in combination with the temperature displayed on the hot plate control.

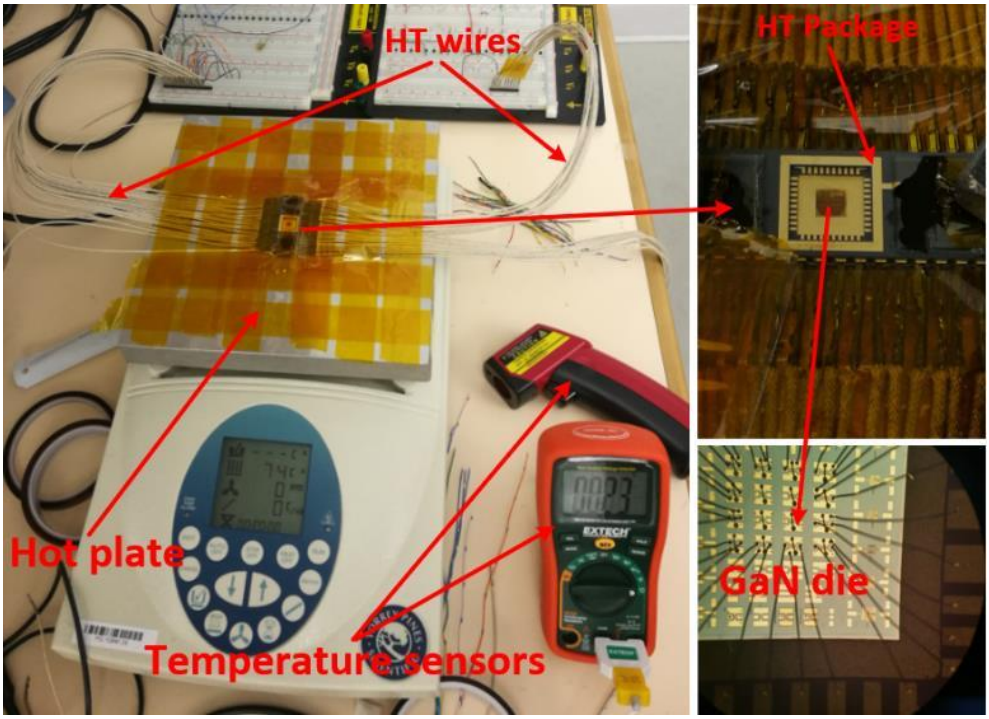



Figure 5.2: Experimental setup for HT GaN500 device characterization.

The output I-V characteristics of a typical GaN500 transistor ($L_{Gate}$ = 500 nm and $W_{Gate}$ = 50 µm) are depicted in Figure 5.3. Each graph reports measured and simulated I-V characteristics for each of the following temperatures: a) 25 $^{o}$C, b) 200 $^{o}$C, c) 300 $^{o}$C, and d) 350 $^{o}$C. Each graph plots curves for each of six voltage levels, from -5 V (switch-off voltage) to 0 V (maximum switch-on

voltage) applied to the device gate ($V_{GS}$). The different curves are obtained by sweeping the drain-source voltage ($V_{DS}$) from 0 V until 15 V. The reported results show the good match obtained between simulated and measured values for a given transistor aspect ratio and applied temperature. These results confirm the suitability of Angelov's model over a 25 $^{o}$C to 350 $^{o}$C temperature range. The saturation current $I_{DS}$ at $V_{GS}$ = 0 V drops from 80 mA at T = 25$^{o}$C to 33 mA at T = 350 $^{o}$C. This is a 40% drop of $I_{DS}$ at $V_{GS}$ = 0 V between 25 $^{o}$C and 350 $^{o}$C. Very similar current drops are obtained for the other $I_{DS}$ at different $V_{GS}$ levels.

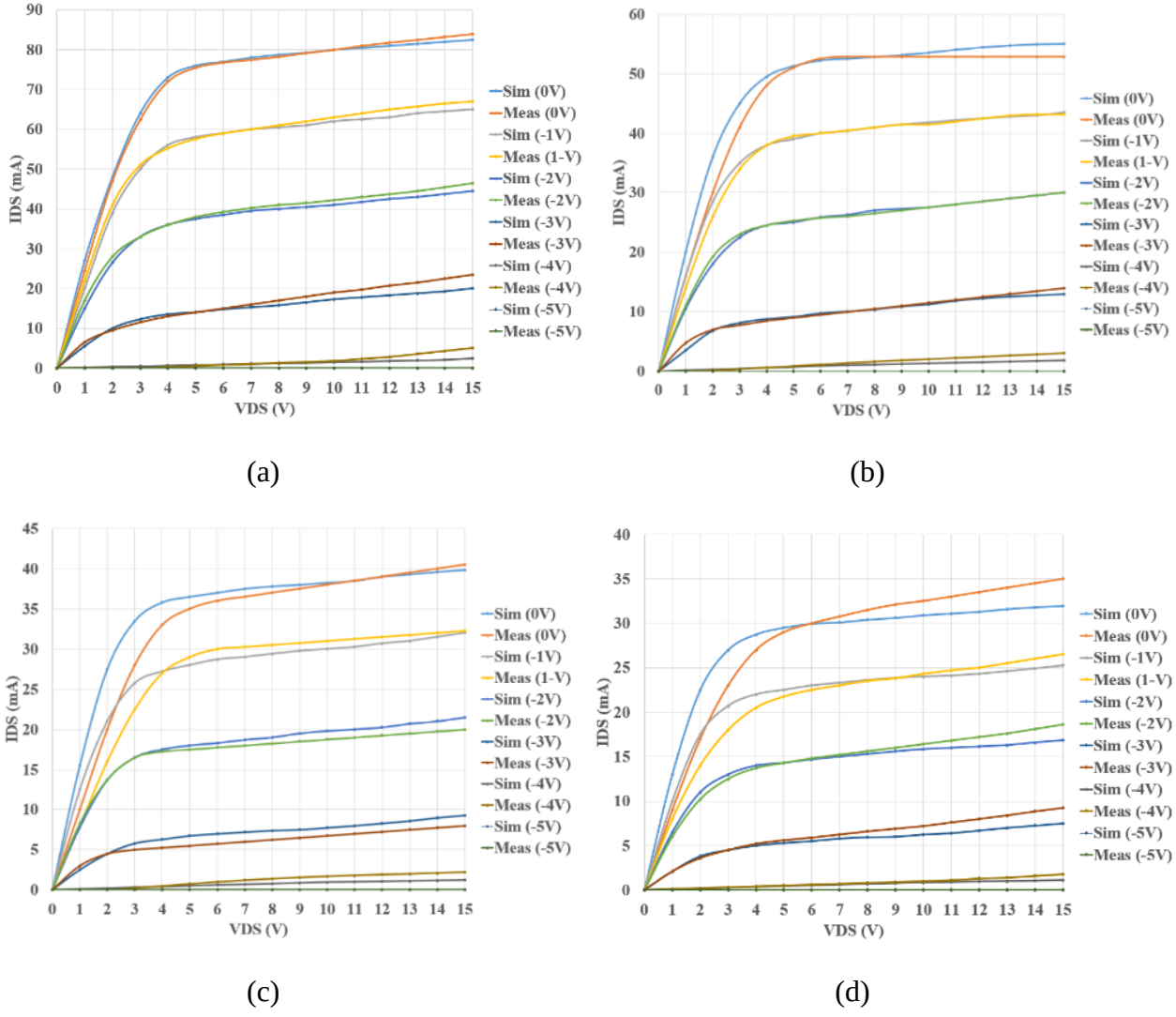
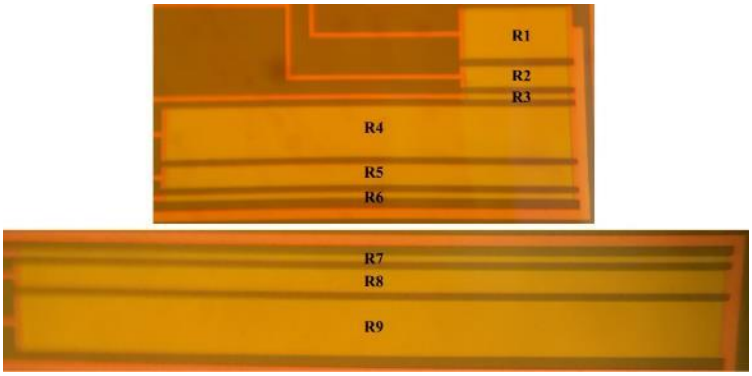


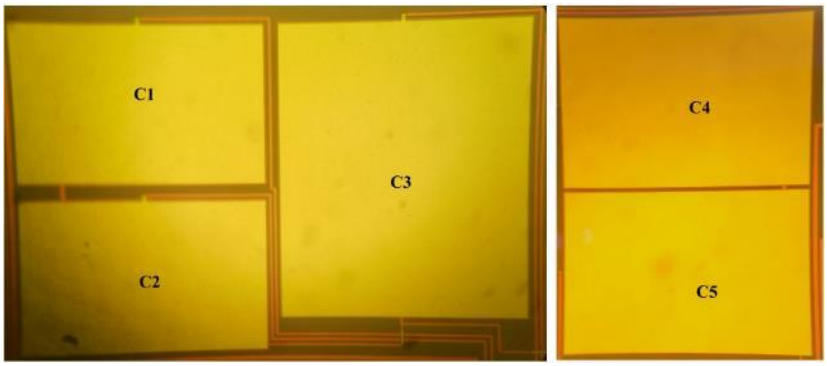

Figure 5.3: Measured and simulated I-V characteristics of a GaN500 device at: (a) 25 $^{o}$C; (b) 200 $^{o}$C; (c) 300 $^{o}$C; (d) 350 $^{o}$C.

### 5.4.2 Integrated Passive Components

As shown in Figure 5.4, the process allows integrating compact passive devices, but provides no model of their sensitivity to temperature. As we intend to operate circuits reliably over a wide temperature range, the sensitivity of various passive components was characterized. Therefore, resistors ($R_1$ to $R_9$) and capacitors ($C_1$ to $C_5$) of various sizes (see Table 5.1) were fabricated as shown in Figure 5.4. The same experimental setup shown in Figure 5.2 was used to perform their HT characterization over the 25 $^oC$ to 350 $^oC$ temperature range.




(a)




(b)

Figure 5.4: Integrated passive components for HT characterization: (a) Resistors; (b) Capacitors.

The measured resistances of $R_{1,3,7,8}$, as shown in Figure 5.5, linearly increase with temperature. From the collected data, equation (4.1) was extracted.

$$R_t = R_0(1 + 4\,10^{-4}\,T) + 0.08\,T \qquad (5.1)$$

It predicts the new resistance ($R_t$) at any temperature (T) between 0 $^oC$ and 350 $^oC$ from its value at room temperature ($R_0$). The resistance values predicted with equation (4.1) are plotted in Figure

5.5 which allows comparing them with the experimental results. This confirms the accuracy of the proposed model over the explored wide temperature range for all resistors. This predicted temperature variation of resistor values is included in all wireless monitoring system models.

Table 5.1: Integrated Resistors and Capacitors.

| Resistor | W/L (µm) | Value @25 ºC (Ω) | Capacitor | W/L (µm) | Value @25 ºC (pF) |
|---|---|---|---|---|---|
| **$R_1$** | 50/100 | 103 | $C_1$ | 500/315 | 57 |
| **$R_2$** | 20/100 | 220 | $C_2$ | 500/315 | 60 |
| **$R_3$** | 5/100 | 805 | $C_3$ | 500/600 | 86 |
| **$R_4$** | 50/400 | 340 | $C_4$ | 400/600 | 77 |
| **$R_5$** | 20/400 | 815 | $C_5$ | 400/600 | 77 |
| **$R_6$** | 5/400 | 3150 | | | |
| **$R_7$** | 5/650 | 5150 | | | |
| **$R_8$** | 20/650 | 1320 | | | |
| **$R_9$** | 50/650 | 540 | | | |

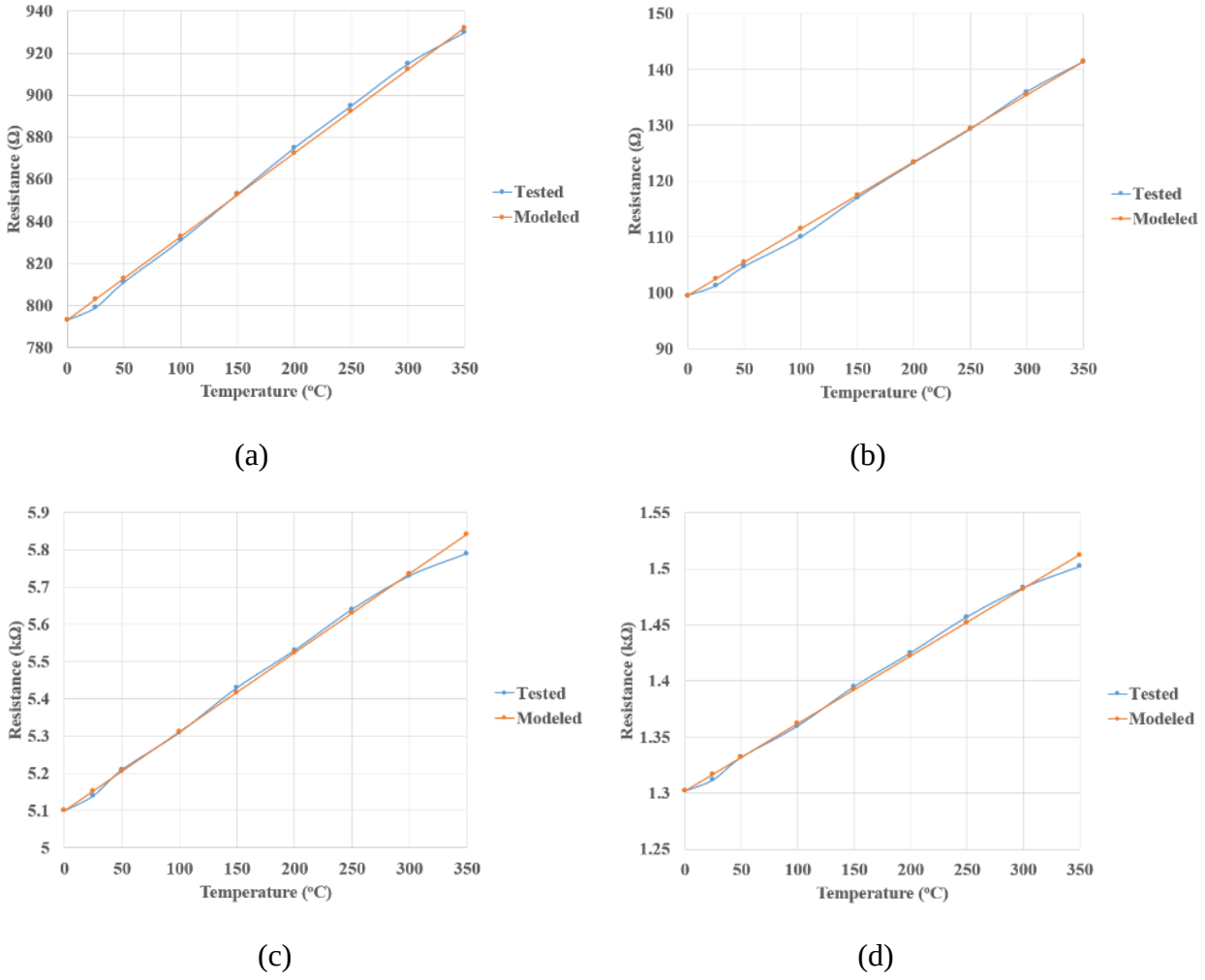



Figure 5.5: HT characterization of different integrated resistors: (a) $R_1$; (b) $R_3$; (c) $R_7$; (d) $R_8$.

The stability of the capacitors was characterized with an impedance analyzer (Agilent 4294A). Figure 5.6 shows the capacitance of 3 different capacitors ($C_1 = C_2$ and $C_4 = C_5$) over the 25 $^oC$ to 350 $^oC$ temperature range. The results show the stable values observed for each capacitor with minor variations observed due to the added variable testing probe parasitic capacitance. Therefore, the capacitors in our design are considered to have constant values with temperature.

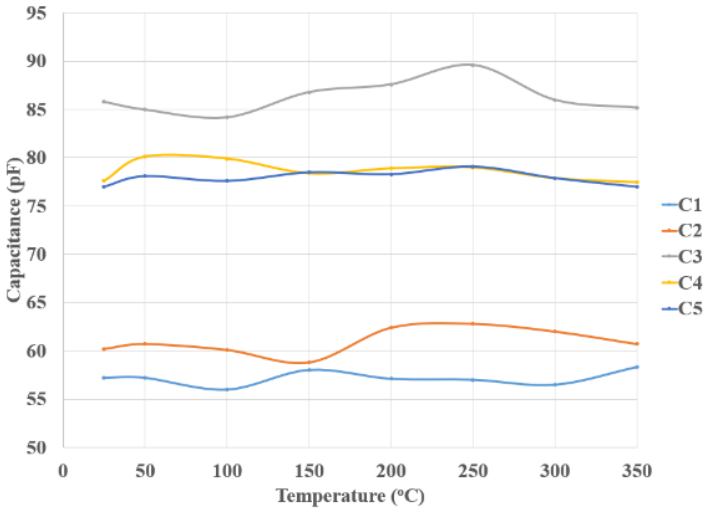



Figure 5.6: HT characterization of different integrated capacitors.

## 5.5 Circuit design and simulation results

After we confirmed the validity of the GaN500 Angelov model available in the design kit and the passive elements model at HT up to 350$^o$C, we used these devices and passive elements to design the proposed wireless transmission system (including modulator and demodulator) and corresponding building block circuits taking into consideration the impact of temperature on the circuits and systems behavior.

However, since there is only one transistor type available in the GaN500 kit, thus implementing a complete modulation/demodulation system became a challenging task. First, we reviewed the applicable circuit design techniques used with WBG normally-on devices [22, 50]. The available GaN500 depletion mode normally-on transistor requires $V_{GS}$ = -5 V to completely switch off its conductive channel. Therefore, a negative input logic level is needed to drive the various circuits and consequently it sets a need to match the input-output controlling signals. Level shifters were added to the logic circuits to solve the incompatibility between the input and output levels and three supply voltage levels are needed ($V_{DD}$ = +14 V, $V_{SS}$ = -14 V, and Gnd).

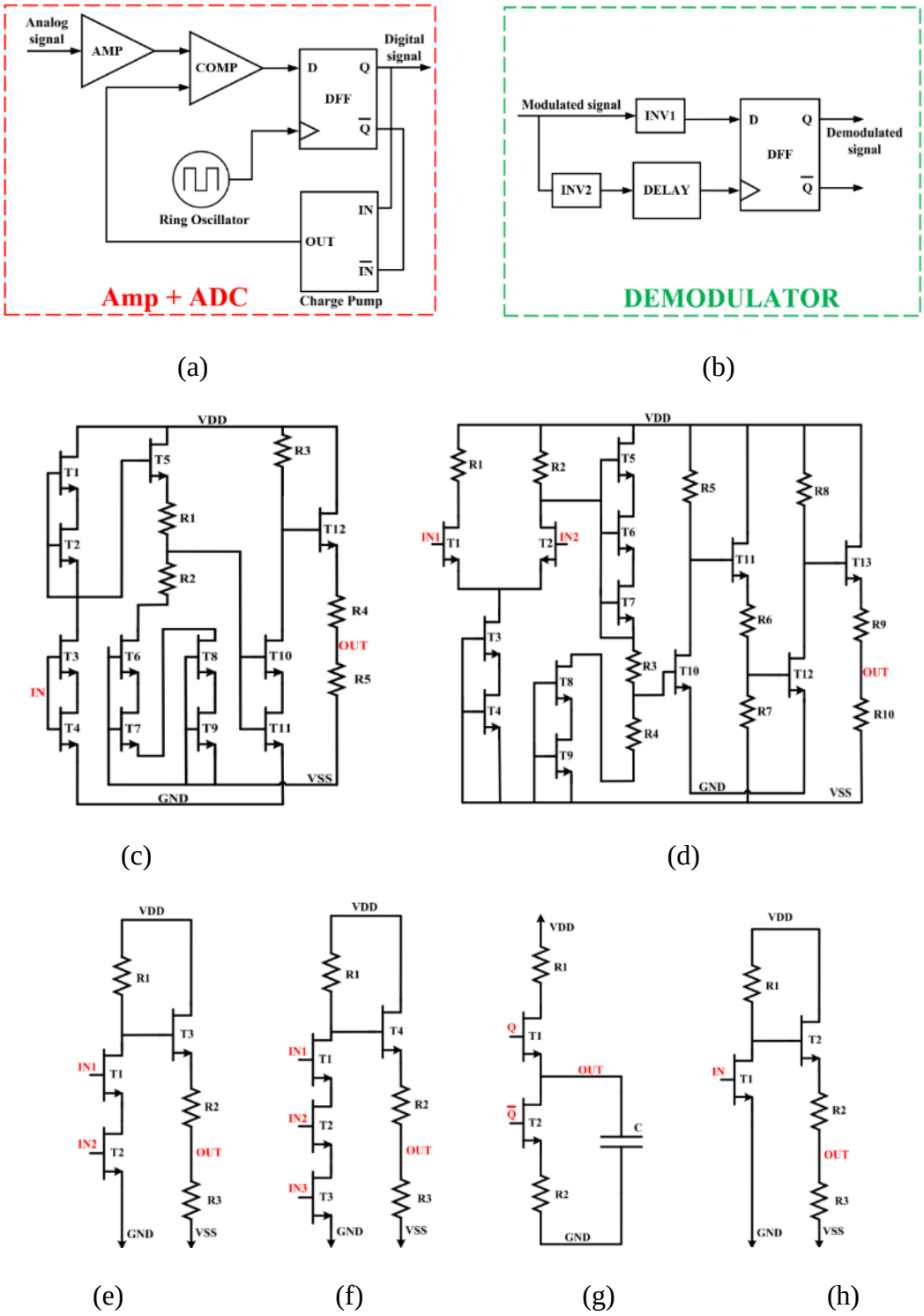



Figure 5.7: Data transmission system: (a) Block diagram of the transmitter; (b) Block diagram of the receiver; (c) Schematic of the amplifier; (d) Circuit diagram of the comparator; (e) Schematic of a 2-input NAND gate; (f) Schematic of a 3-input NAND gate; (g) Charge pump circuit; (h) Schematic of an inverter.

Another challenging condition is the HT (350 ºC) operating environment that the system should endure reliably while monitoring various sensors. Those two hindrances reduce the possibilities of adopting complex design techniques and are a strong motivation to reduce the number of transistors used to implement the various system building blocks.

Figure 5.7 presents the block diagram of the proposed data transmission system, as well as the circuit implementation of its building blocks. The main goal of this work is to implement a generic integrated system that could be utilized in different types of harsh environment sensors such as HT and HP sensors. The proposed system could be adapted to fit the specific requirements of many types of sensors. To validate our system concept, a possible example is a pressure sensor [191]. It is a piezoresistive MEMS pressure sensor from Kulite Semiconductor Products, Inc. (Model No. XTEH-10L-190L). This sensor is a static pressure transducer with rated temperature of 500°C (only for the sensor head) and rated pressure up to 210 Bar. It typically produces a small amplitude signal ranging between 0 and 100mV when the measured pressure ranges from 0 to 210 Bar.

### 5.5.1 Front-end Amplifier

A front-end amplifier block is used in the data transmission path as shown in Figure 5.7(c). Its input signal is provided by the pressure sensor with minimum and maximum voltage of 0V and 100mV respectively. To amplify that signal, a 50 V/V two-stage amplifier architecture was adopted. Each stage of this amplifier comprises a level shifter to maintain the input-output compatibility. Simulation results, reported in Figure 5.8, show a sinusoidal input signal (IN = 0, +100 mV) and the corresponding stable amplified output signal (OUT = 0, +5 V) over the wide temperature range of 25 ºC to 350 ºC.

### 5.5.2 Analog to Digital Converter (ADC)

The amplified signal obtained from the pressure sensor is applied to an ADC. The block diagram of this ADC is presented in Figure 5.7(a). The proposed ADC is based on the delta modulation technique. Its architecture is optimized to reduce complexity while consuming little power and area. The analog input signal, coming from the amplifier, is compared with the analog feedback signal produced by the charge pump to provide a digital output applied to a D-Flip Flop. Note that the charge pump in Figure 5.7(g) includes an output capacitor converting current pulses into an analog value that can be compared with the amplified analog signal coming from the sensor. The

latter is used to synchronize the extracted digital signal by the clock signal coming from a ring oscillator to provide the final digital modulating waveform. The latter waveform is used along with its complementary value to drive a charge pump. The output data from the ADC is employed to drive the LSK modulator.

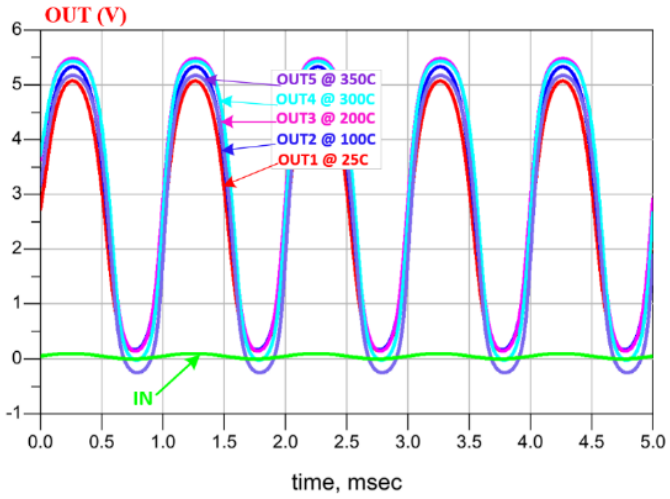
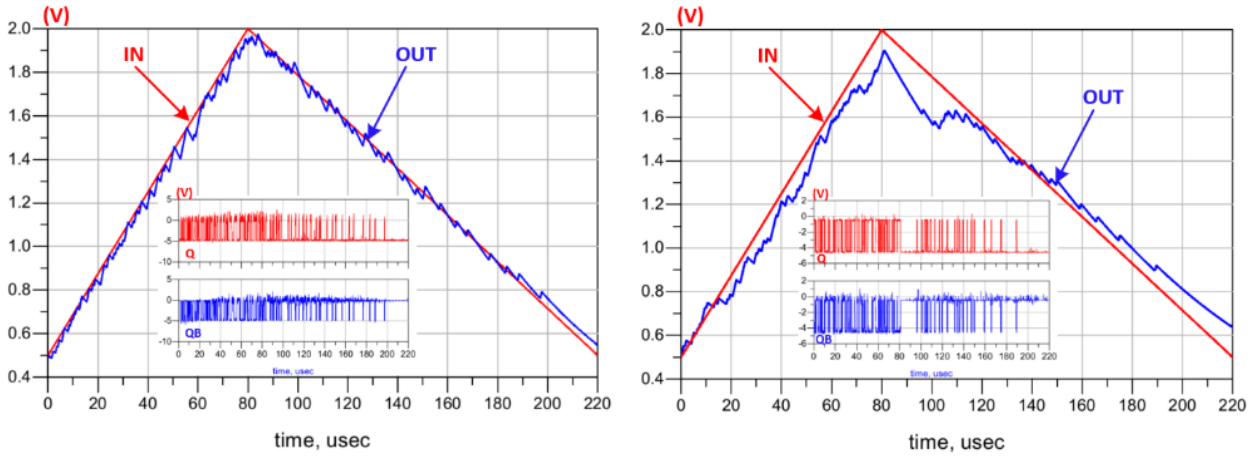



Figure 5.8: Amplifier simulated results at different temperatures.




(a) (b)

Figure 5.9: Simulation results of the data transmission chain with the input in red and the output in blue at: (a) 25 ºC; (b) 350 ºC. The recovered Q an QB streams are plotted in the embedded graphs.

The simulation results at 25 ºC are shown in Figure 5.9(a). Note that the feedback signal (OUT), coming from the charge pump, follows the amplified analog input signal (IN), where IN presents the monitored analog signal of the pressure sensor after amplification. Q and QB (plot embedded

in Figure 5.9(a)) are used to control the direction of the charge pump current. At 350 ºC, the ADC is still working, as shown in Figure 5.9(b), despite the observable impact of the HT on its performance. The remaining of this section describes the main circuits composing the ADC as well as the simulation results confirming their functionality.

### 5.5.2.1 Comparator

Figure 5.7(d) presents the schematic design of the comparator where a first stage differential amplifier is followed by a series of adapted inverters and level shifters to reach the desired comparison accuracy. Figure 5.10 shows the comparator output and its good performance over the 25 ºC to 350 ºC temperature range.

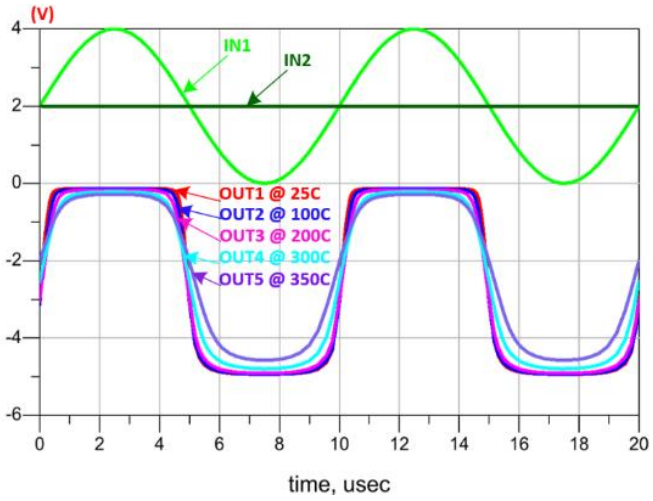
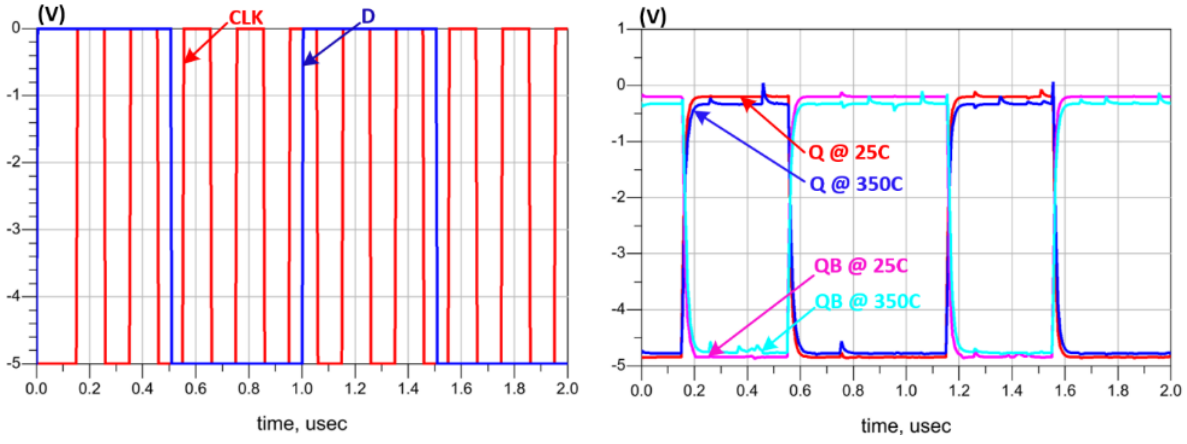



Figure 5.10: Comparator simulations at different temperatures.




(a) (b)

Figure 5.11: D-Flip Flop simulation results: (a) Input signals; (b) Output Data.

#### 5.5.2.2 D-Flip Flop

The D-Flip Flop design is based on five 2-input and one 3-input NAND logic gates where the corresponding schematic design is shown in Figure 5.7(e) and Figure 5.7(f), respectively. The simulation results, shown in Figure 5.11, confirm the good operation of the D-Flip Flop even at 350 $^{o}$C.

#### 5.5.2.3 Charge Pump

As briefly mentioned before, the purpose of the charge pump circuit is to convert its digital input stream into an analog output (DAC). It is required by the ADC to provide an analog feedback signal to be compared with the initial input analog signal and minimize the error rate of the modulation process. For our specific application (pressure sensor), the charge pump is designed to provide an output with minimum voltage ($V_{min}$ = 0 V) and a maximum voltage ($V_{max}$ = 2 V) to fit into the proposed ADC system.

The schematic of the charge pump circuit is shown in Figure 5.7(g) where two complementary inputs (Q and QB) are needed to charge and discharge the capacitor (C). The proposed charge pump shows a correct behavior at 25 $^{o}$C and 350 $^{o}$C during charging and discharging as depicted in Figure 5.12(a) and (b) respectively.

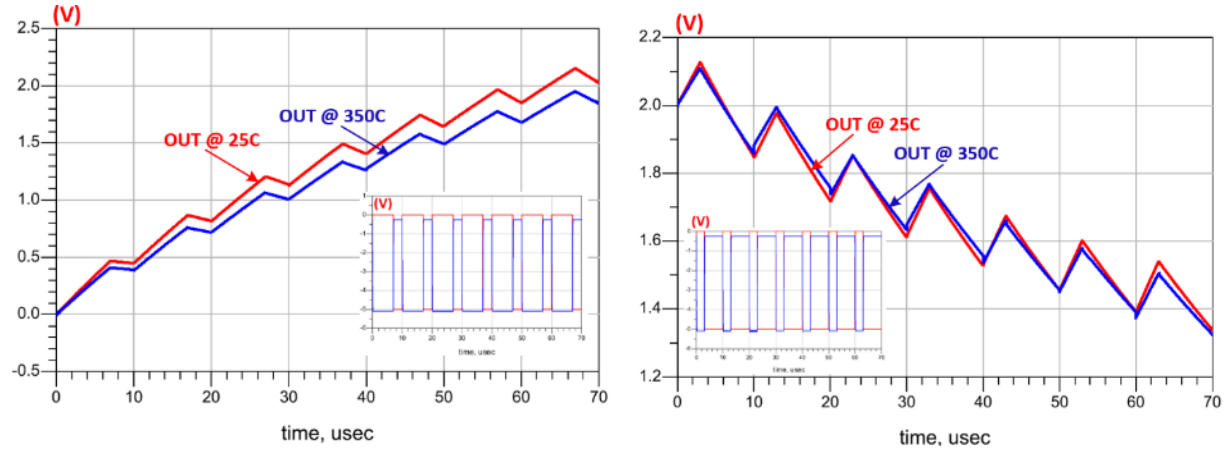
#### 5.5.2.4 Ring Oscillator

A 7-stage ring oscillator is implemented to generate a 1.5 MHz output signal followed by an inverter to sharpen the generated waveform. This frequency value is appropriate with the specific requirements of wireless inductive link through metallic barrier where a low-frequency signal is highly recommended [125]. Figure 5.13(a) shows the variation of the oscillation frequency as a function of temperature. Note that the maximum deviation of the frequency is around 4.2% over the considered wide temperature range of 25 $^{o}$C to 350 $^{o}$C.

#### 5.5.2.5 Inverter

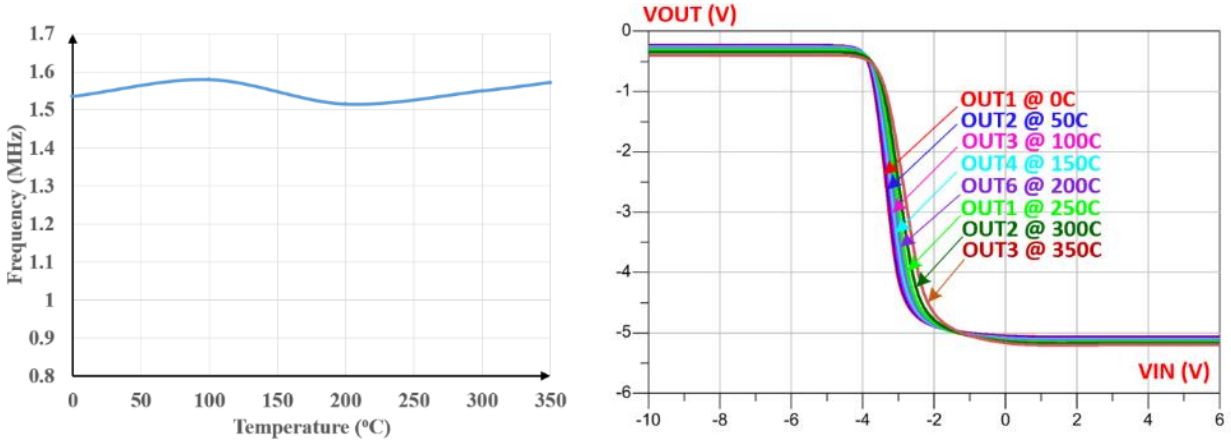
The schematic of the inverter that was used is shown in Figure 5.7(h). This design must be modified in terms of transistors size, resistor values and sometimes by adding parallel capacitors to the output based on design requirements. The simulated voltage transfer characteristics of a typical inverter

are depicted in Figure 5.13(b), confirming its correct operation over the whole range of temperatures considered.




(a) (b)

Figure 5.12: Impact of the temperature on Charge pump during: (a) Charging; (b) Discharging.




(a) (b)

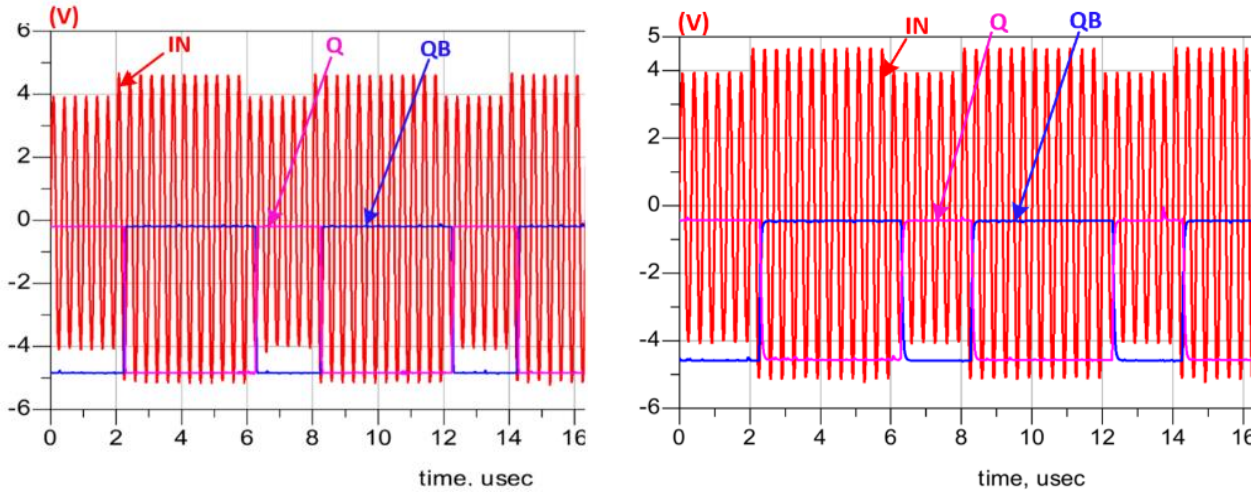
Figure 5.13: Impact of the temperature on: (a) Oscillation frequency; (b) voltage transfer characteristics of the inverter.

### 5.5.3 Proposed demodulation system

The block diagram of the proposed demodulator is presented in Figure 5.7(b). The demodulator receives the LSK modulated signal (where there are two different amplitudes, high-level for data-on and low-level for data-off) and recovers the initial data.

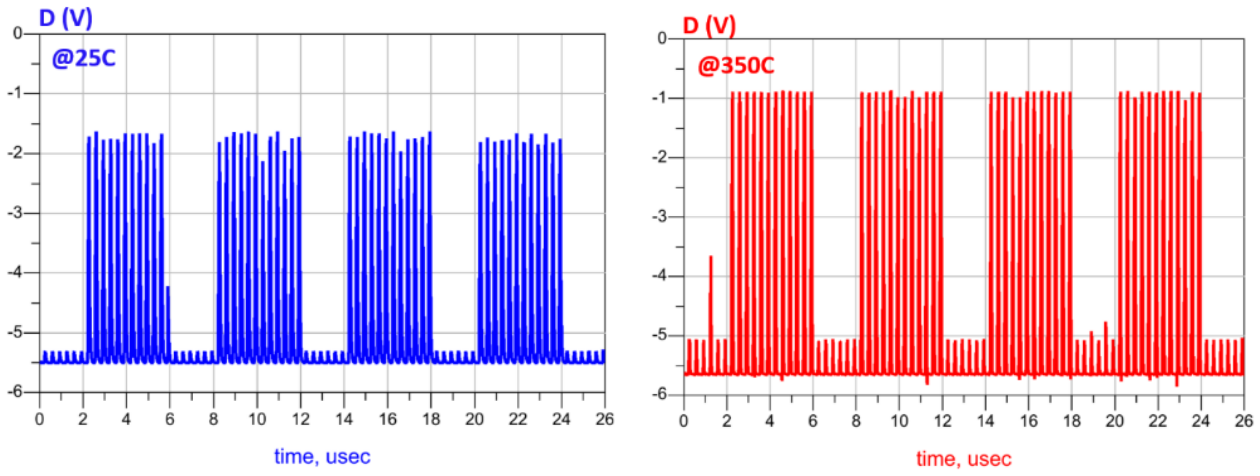
The novel idea here is to use an inverter (INV1) which is carefully designed to detect only the high amplitude voltage (data-on) of input signal. On the other hand, INV2 is used to switch continuously regardless of the input voltage signal amplitude to generate the clock signal of the D-Flip Flop. This signal is delayed by the average of the DELAY block to ensure matching with the detected data signal. Both data-on and data-off amplitude voltage are recommended to be as close to each other as possible to ensure higher power transfer efficiency during LSK modulation.

The minimum amplitude of the data-on signal that can be detected by INV1 is ±5 V. In other words, to reach a higher power transfer efficiency, the amplitude of the data-on signal could be increased to more than ±5 V, as much as needed, until reaching the required power transfer efficiency, without applying any change on the proposed demodulators. In parallel, the maximum amplitude of the data-off signal is ±4 V and it could be less than that, but it would reduce the power transfer efficiency. Therefore, to validate the concept, the modulated signal (IN) is selected with a high-amplitude of ±5 V (minimum data-on) and low-amplitude of ±4 V (maximum data-off) to show the performance of modulators in the critical case. Consequently, a 1.0 V amplitude difference (20% of the maximum amplitude) is reached between the high-amplitude (data-on) and the low-amplitude (data-off) of the modulated signal (IN) with the proposed demodulators.




(a) (b)

Figure 5.14: Demodulator simulation results of input/output signals at: (a) 25 ºC; (b) 350 ºC.




(a) (b)

Figure 5.15: Impact of the temperature on detected data (D) at: (a) 25 ºC; (b) 350 ºC.

The retrieved demodulated signal (Q) and its complementary (QB) at 25 ºC are shown in Figure 5.14(a). INV1 detects only the high-level (±5 V) pulses of IN and ignores the low-level (±4V) ones as seen in Figure 5.15(a). The required time delay to shift the clock (CLK) and ensure its intersection with the detected data (D) is comparatively large due to the low operating frequency. Therefore, a long chain of inverters (20 stages) is utilized to design the DELAY block. At 350 ºC, the demodulator shows an excellent stability as seen in Figure 5.14(b) and Figure 5.15(b). In Figure 5.16, the simulation results confirm the robustness of the designed DELAY block that shows a slight increase (10.5%) of its time delay at 350 ºC.

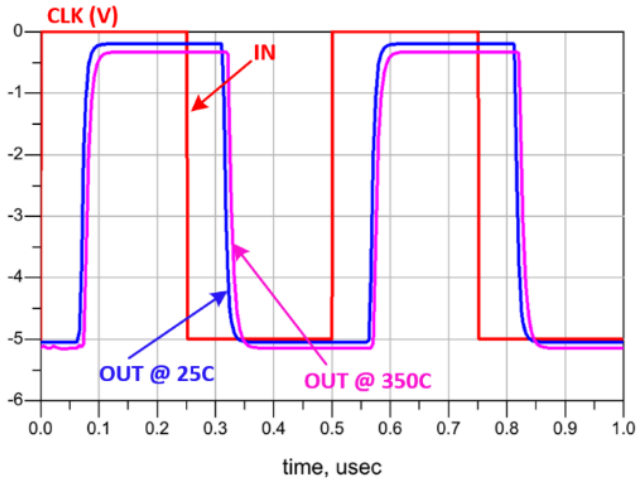



Figure 5.16: Temperature impact on DELAY circuit.

A complete chip layout (Figure 5.17) for the proposed system was performed. The overall area of the chip is 4.0 mm x 2.7 mm. The power consumption and the occupied area of the ADC, demodulator and their corresponding building blocks are listed in Table 5.2. It is remarkable that the HT has a positive impact on power consumption, with power consumption reduced by more than 40% at 350 ºC for some blocks. The power consumption and area of the digital demodulator are dominated by the DELAY block, which should be optimized in future work.

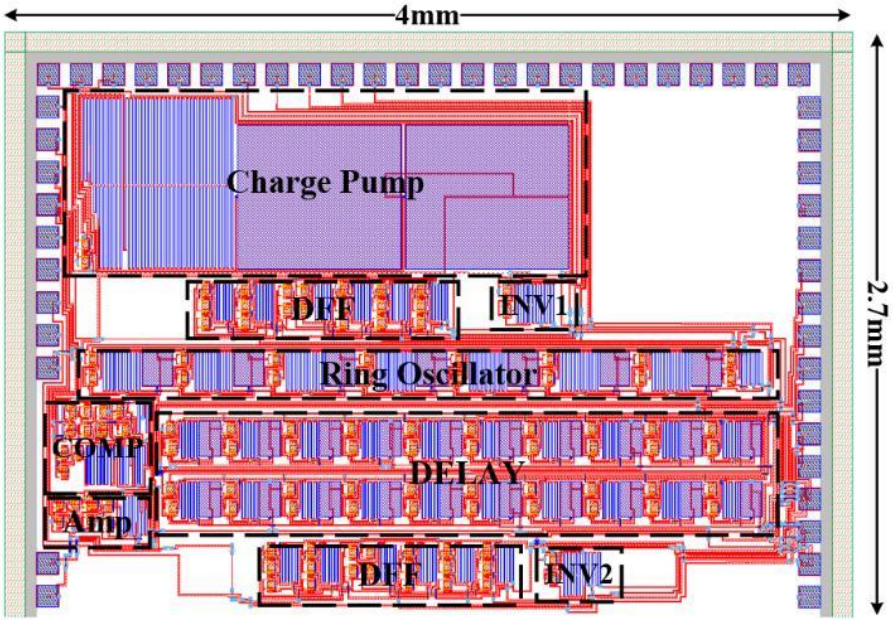



Figure 5.17: Chip layout view of the proposed data transmission system.

Table 5.2: Power consumption and area of the various system building blocks.

| Circuit | Power (mW) @ 25 ºC | Power (mW) @ 350 ºC | Area ($mm^2$) |
|---|---|---|---|
| **ADC** | 1100 | 720 | 3.2 |
| **Amp** | 658 | 308 | 0.45x0.2 |
| **COMP** | 770 | 420 | 0.42x0.46 |
| **D-FLIP FLOP** | 126 | 108 | 1.2x0.25 |
| **Ring Oscillator** | 210 | 189 | 3.2x0.22 |
| **Charge pump** | 1.4 | 1.2 | 2.4x0.8 |
| **Demodulator** | 4438 | 4000 | 2.01 |
| **INV1** | 32 | 28 | 0.27x0.21 |
| **INV2** | 91 | 70 | 0.26x0.23 |
| **DELAY** | 3318 | 3010 | 2.9x0.55 |

## 5.6 Conclusion and Future Work

We described novel circuits techniques intended for implementing wireless data transmission systems dedicated for high-temperature (HT) applications. The introduced system is integrated using AlGaN/GaN HEMT devices to benefit from its corresponding outstanding properties, commercial availability, and ability to endure the HT environment. The HT characterization of GaN500 devices, integrated resistors, and integrated capacitors was performed to validate their corresponding models used in system simulations. The design considerations of the proposed system were discussed taking into account the specific requirements of the targeted applications and the limitations of adopted technology. Circuit simulations of subsystems and building blocks were performed over the 25 ºC to 350 ºC wide temperature range to validate the capability of the GaN technology to implement an integrated wireless system that can be used in harsh environment applications. Future work should focus on circuit design optimization to further reduce area and power consumption.

# CHAPTER 6 GENERAL DISCUSSION

Monitoring sensors installed in harsh environment applications, such as deep-well drilling, automotive and space exploration, are needed to enable improved safety, optimized fuel efficiency and reduced emissions. The ability to use electronic systems in these sensors will eliminate heavy complex cooling and protection solutions. Consequently, the cost of current sensing systems would be decreased, and reliability would be improved by reducing the weight and size of cabling.

Implementing circuits and systems able to process the monitored data in high-temperature environment is not an easy task. Indeed, serious challenges and severe constraints had to be addressed throughout our research. A comprehensive literature review was conducted on harsh environment electronics. This led us to identify WBG semiconductors as the best technology for building the targeted class of desired system. The most known WBG technologies are the SiC and GaN. Further investigation was needed to decide which one is most available and appropriate for our application. Although SiC received a great deal of attention in the past decade as a proper candidate for high-temperature applications, the low device density integration and the unavailability of SiC integrated devices and circuits for HT applications prevented the SiC to be our first option. On the other hand, the GaN500 HEMT technology commercialized by NRC that is available through CMC was found to be an ideal option for our research.

In fact, two GaN design kits were available at NRC; GaN150 and GaN500. However, the fabrication runs were not regularly available and mainly depended on requested fabrication area. Consequently, and due to the low number of fabrication request, NRC was forced to stop the fabrication of GaN150 and keep the fabrication of GaN500 in condition of complete wafer fabrication request. This instability in the fabrication timeline and the selection of design kit imposed us to redesign our circuits and systems based on GaN500 kit after we spent a long time to implement our systems based on GaN150. Moreover, to benefit from multi project wafer (MPW) option, we were forced to wait until the submission of two other unrelated projects to fabricate their design with GaN500.

Our literature review confirms the robustness of GaN devices in HT. However, the provided GaN150 and GaN500 kits by NRC was developed to suit the needs of RF applications and they were not characterized at HT. Therefore, we performed the HT characterization of few independent GaN150 and GaN500 devices. Due to the shortage in HT packaging and wiring, we were forced to

do the HT testing using probe station to establish the electrical connection with GaN terminals. This experiment could not support the very high temperatures due to the instability of probe needles at such temperatures set on the surface of GaN device terminals. For this reason, we developed another packaging solution by attaching HT wires to the pins of the tested package. Then, the package is deposited on the surface of a hot plate. This packaging and setup experiment allowed the HT characterization to reach 400 $^{o}$C.

The normally-on depletion mode GaN devices provided by GaN500 design kit imposed significant design constraints to build the desired data transmission system including digital and analog blocks. In addition, only few published works (3-4) were found successful to implement GaN-based circuits in HT applications, which added more challenges to develop new design solutions based on our GaN500 kit. Taking into consideration the limited power budget in our wireless based system and the small desired implementation area, a minimum number of transistors was used to obtain a simple design of the desired functions and for better miniaturization of the complete system.

After two years of interaction with NRC, we successfully submitted and fabricated two chips based on GaN500. Each one has a size of 4 mm x 4 mm. The first chip mainly includes the building blocks of digital and analog circuits (See Appendix A), and the second chip contains the proposed systems based on the circuits validated in chip 1 (See Appendix B). In addition to the building blocks and systems, the chips comprise samples of integrated passive components (resistors, capacitors and inductors) (See Appendix A) and active devices (GaN500) with different values and sizes (See Appendix B) to perform the reliability tests and generate simulation models of those components at high temperature.

During the first measurements of the received chips, we noticed that the self heating is very high reaching around 80 $^{o}$C in less than one minute. The main reason of the high self heating is the power dissipation in the integrated resistors. We were imposed to shrink the area of each circuit to be able to include all the designed circuits and systems. For this reason, the resistors are designed with minimum width to reach the desired resistance with minimum resistor dimension. In addition, we limited the number of voltage supply terminals to gain more pads and get access to all designed circuits and systems. However, the strategy of limited number of power supplies and minimum

width of integrated resistors negatively affect the performance of implemented circuits. We did not use larger chips or more chips because of the high fabrication cost and the limited fabrication runs.

We performed the HT measurements of digital circuits at temperature reaching 350 $^{o}$C, the maximum we could handle due to limitation in HT packaging and testing setup. The analog circuits and main systems did not show a good functionality even at normal temperature 25 $^{o}$C. The fab supplier (NRC) mentioned that the GaN500 devices of the fabricated chips have a higher gate leakage current (1E-3 A/mm) than mentioned in the design manual (1E-4 A/mm). The tested gate leakage current in our lab confirmed the fab supplier notification in addition to the increase of threshold voltage from expected $V_{GS}$ = -3.5 V to measured $V_{GS}$ = -4.5 V and the increase of integrated resistors values by 20% over the designed ones. All these reasons affected the performance of analog circuits and systems based on the analog blocks.

The fab supplier mentioned that another fabrication run is almost finished, and a new copy of the same designed chips will be delivered soon in the coming few months. They confirmed that the preliminary tests of the new run show a normal rate of gate leakage current (1E-4 A/mm). This will give us the opportunity to do more measurements and compare between the two runs. In addition, we may see better functionality specially in the analog blocks. However, the supplier mentioned that the resistors have values less than designed by 20%. This will increase the power consumption, self-heating and affect the functionality of sensitive blocks and systems. A third run is also expected as a backup of the previous two runs. The delivery time is expected to be with the delivery of the second run. With the third run, we are expecting better performance of sensitive circuits and systems in addition to more measurement data to perform the reliability tests and develop accurate HT models.

# CHAPTER 7 CONCLUSION AND RECOMMENDATIONS

In this thesis, we present our work on new building block circuits to implement a wireless data transmission system dedicated for high temperature applications. Our main objectives were to support monitoring sensors in harsh environment by improving the recovery and transmission of measured data and by simplifying their use to reduce cost, improve safety and optimize efficiency. The GaN500 technology was selected to perform the implementation of circuits and systems due to its robustness at high temperature and availability for fabrication. New ideas and techniques have been conducted to design new simple building circuits and to overcome the limitations imposed by the normally-on depletion mode GaN500 devices. The thesis is organized in a way that each chapter introduces an original contribution from this research.

Chapter 3 presents the implementation and characterization of GaN500 devices and of integrated passive components available as part of the GaN500 technology. The GaN devices and passive components are remarkably stable, enabling operation above 500 $^{o}$C. The characterization results are used to extract HT models of the integrated GaN500 devices (Angelov model) and passive elements (empirical model). These models would be included in the GaN500 design kit to capture the temperature effects on the design simulations. Four logic gates (NAND-2IN, NAND-3IN, NOR-2IN and NOR-3IN) were implemented and successfully validated at HT. In addition, two voltage reference circuits and an inverter were tested at temperatures ranging from 25 $^{o}$C to 600 $^{o}$C. This work is an important step toward the implementation of GaN-based integrated circuits (IC) and systems intended for high-temperature (HT) applications.

In chapter 4, the design and implementation of three different demodulators based on GaN500 devices are described. The introduced systems are designed to fit into data transmission systems based on the LSK modulation technique implemented in HT applications. To serve data transmission through metallic barrier, two of the proposed systems were designed to demodulate low carrier frequencies in the range of kHz. The third system is dedicated more for higher carrier frequency. The design considerations of the proposed modules are discussed considering the specific requirements of the targeted applications and the limitations of adopted technology. Simulation results of proposed systems are performed to ensure their functionality over wide temperature ranges between 25 $^{o}$C and 400 $^{o}$C.

In chapter 5, a fully-integrated data transmission system based on GaN500 devices is proposed to acquire signals from sensors installed in HT environments. The presented system comprises of modulation and demodulation blocks. The modulator includes a front-end amplifier (Gain of 50V/V), followed by a novel analog-to-digital converter driving a modulator exploiting the Load-Shift Keying technique. To retrieve the data, a fully digital demodulator is proposed. The HT characterization and modeling of integrated GaN devices and passive components are performed to ensure the reliability of simulation results. The performance of the various proposed building blocks and systems have been validated by simulation over the projected wide operating temperature range (25-350 $^{o}$C).

## 7.1 Contributions

The main contributions claimed in this thesis relate to the development of proposed wireless data transmission systems. These contributions can be summarized as follows:

- We conducted in-depth investigations on the available high-temperature semiconductors and based on this analysis, we selected the GaN500 technology to implement our system. We performed the HT characterization of GaN500 devices at temperatures reaching 600 $^{o}$C. From that experimental characterization, we extracted an improved Angelov model with which we can simulate the impact of temperature on designed circuits and systems. Integrated passive elements have also been characterized at HT and the HT models have been extracted as well.
- We designed the first GaN500-based building circuits using simple design. The circuits were validated at HT, thus confirming the ability of GaN500 technology to implement digital circuits operating at HT.
- We designed the first modulation/demodulation system based on GaN500 technology. This system was validated with simulations reflecting the impact of temperature on active and passive elements and the results are promising as they show stable performance of proposed system over the temperature range 25 $^{o}$C to 350 $^{o}$C.

## 7.2 Future work

Our planned future work is to further validate the functionality of the implemented systems at HT using the devices from two fabrication runs of our chips that are expected in the near future at the time of completing this thesis. Those runs are expected to have better performance after the applied improvements on fabrication process by NRC. In parallel, the fabricated independent GaN500 devices will be used to complete the extracted improved Angelov model including the AC modeling and transient modeling. In addition, we aim to develop new approaches, techniques, and structures for harsh-environment packaging. The HT packaging will give us the opportunity to validate the functionality of developed systems at HT higher than 400 $^{o}$C. The validated modulation and demodulation systems will be used to implement a complete chain of wireless monitoring starting from the interface of an installed sensor to the external control unit passing through an inductive link to transmit the data through a metallic barrier.

Another future work is to implement a GaN-based power transfer system able to transfer sufficient power to a data transmission system operating at high temperature. To prevent low fabrication quality or long delivery times, we will explore fabricating our future design with another supplier. One available option is United Monolithic Semiconductors (UMS) in Europe which provides fabrication of GaN250 HEMT (GH25) technology. This technology is very close to the GaN500 technology utilised in our design. This technology offers faster fabrication and delivery time.

Finally, we aim to implement a complete prototype of a GaN-based data and power transmission system. We will examine the characteristics of the material used in construction of applications where an inductive link will be applied. Another important area of future research relates to inductive coupling for power and data transmission. There are several but finding the best one is challenging research.

A complete prototype consisting of both data and power systems based on GaN technology could be implemented and tested to ensure the reliability of the developed systems and the effective functionality between them. Experimental validation of the prototype could be performed using a real helicopter engine bench provided by Safran. The engine bench would serve the testing measurements to ensure the practical simulation of real harsh environment applications.

## 7.3 Publications

**Journal articles:**

1- Hassan, A., Ali, M., Savaria, Y., & Sawan, M. (2019). GaN-based LSK demodulators for wireless data receivers in high-temperature applications. Microelectronics Journal. Published on 14 January 2019.

2- Hassan, A., Ali, M., Trigui, A., Savaria, Y., & Sawan, M. (2019). A GaN-based Wireless Monitoring System for High-Temperature Applications. *Sensors* (invited paper). Published on 14 April 2019

3- Hassan, A., Amer, M., A., Savaria, Y., & Sawan, M. (2019). High-Temperature Characterization, Modeling and circuit validation of GaN500 HEMT up to 600 $^{o}$C. Submitted to IEEE Transactions on Circuits and Systems I: Regular Papers.

4- Hassan, A., Savaria, Y., & Sawan, M. (2018). GaN Integration Technology, an Ideal Candidate for High-Temperature Applications: A Review. IEEE Access, 6, 78790-78802.

5- Hassan, A., Savaria, Y., & Sawan, M. (2018). Electronics and packaging intended for emerging harsh environment applications: A review. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, (99), 1-14.

**Conference articles:**

1- Amer, M., Hassan, A., Ragab, A., Yacout, S., Savaria, Y., & Sawan, M. (2018, May). High-Temperature Empirical Modeling for the I-V Characteristics of GaN150-Based HEMT. In Circuits and Systems (ISCAS), 2018 IEEE International Symposium on (pp.1-5). IEEE.

2- Abubakr, A., Hassan, A., Ragab, A., Yacout, S., Savaria, Y., & Sawan, M. (2018, May). High-Temperature Modeling of the I-V Characteristics of GaN150 HEMT Using Machine Learning Techniques. In Circuits and Systems (ISCAS), 2018 IEEE International Symposium on (pp. 1-5). IEEE.

3- Hassan, A., Ali, M., Trigui, A., Hached, S., Savaria, Y., & Sawan, M. (2017, June). Stability of GaN150-based HEMT in High Temperature up to 400$^{o}$C. In 2017 IEEE International NEWCAS Conference. IEEE.

4- Hassan, A., Trigui, A., Shafique, U., Savaria, Y., & Sawan, M. (2016, May). Wireless power transfer through metallic barriers enclosing a harsh environment; feasibility and preliminary results. In 2016 IEEE International Symposium on Circuits and Systems (ISCAS) (pp. 2391-2394). IEEE.

# BIBLIOGRAPHY


[1] D. G. Senesky, B. Jamshidi, K. B. Cheng, and A. P. Pisano, "Harsh environment silicon carbide sensors for health and performance monitoring of aerospace systems: A review," *IEEE Sensors Journal,* vol. 9, no. 11, pp. 1472-1478, 2009.

[2] J. Watson and G. Castro, "High-temperature electronics pose design and reliability challenges," *Analog Dialogue,* vol. 46, no. 2, pp. 3-9, 2012.

[3] D.-X. Yang, Z. Hu, H. Zhao, H.-F. Hu, Y.-Z. Sun, and B.-J. Hou, "Through-metal-wall power delivery and data transmission for enclosed sensors: A review," *Sensors,* vol. 15, no. 12, pp. 31581-31605, 2015.

[4] P. C. Arribas, P. Sanchez, and C. Aroca, "RFID in Metal Environments: An Overview on Low (LF) and Ultra-Low (ULF) Frequency Systemsled," in *Radio frequency identification fundamentals and applications design methods and solutions*: IntechOpen, 2010.

[5] M. Yamakawa, Y. Mizuno, J. Ishida, K. Komurasaki, and H. Koizumi, "Wireless power transmission into a space enclosed by metal walls using magnetic resonance coupling," *Wireless Engineering Technology,* vol. 5, no. 01, p. 19, 2014.

[6] H. Zangl, A. Fuchs, T. Bretterklieber, M. J. Moser, and G. Holler, "Wireless communication and power supply strategy for sensor applications within closed metal walls," *IEEE transactions on instrumentation measurement,* vol. 59, no. 6, pp. 1686-1692, 2010.

[7] T. J. Lawry, K. R. Wilt, J. D. Ashdown, H. A. Scarton, and G. J. Saulnier, "A high-performance ultrasonic system for the simultaneous transmission of data and power through solid metal barriers," *IEEE transactions on ultrasonics, ferroelectrics, frequency control,* vol. 60, no. 1, pp. 194-203, 2013.

[8] L. Huang, A. P. Hu, A. Swain, S. Kim, and Y. Ren, "An overview of capacitively coupled power transfer—A new contactless power transfer solution," in *2013 IEEE 8th Conference on Industrial Electronics and Applications (ICIEA)*, 2013: IEEE, pp. 461-465.

[9] G. A. Covic and J. T. Boys, "Inductive power transfer," *Proceedings of the IEEE,* vol. 101, no. 6, pp. 1276-1289, 2013.

[10] A. Hassan, Y. Savaria, and M. Sawan, "Electronics and packaging intended for emerging harsh environment applications: A review," *IEEE Transactions on Very Large Scale Integration Systems,* no. 99, pp. 1-14, 2018.

[11] M. Alexandru *et al.*, "SiC integrated circuit control electronics for high-temperature operation," *IEEE Transactions on Industrial Electronics,* vol. 62, no. 5, pp. 3182-3191, 2015.

[12] P. Neudeck, "SiC integrated circuit platforms for high-temperature applications," in *Extreme Environment Electronics*: CRC Press, 2013, pp. 225-232.

[13] R. Gaska *et al.*, "Novel AlInN/GaN integrated circuits operating up to 500 C," *Solid-State Electronics,* vol. 113, pp. 22-27, 2015.

[14] P. Herfurth *et al.*, "GaN-on-insulator technology for high-temperature electronics beyond 400° C," *Semiconductor Science Technology,* vol. 28, no. 7, p. 074026, 2013.

[15] K. N. Martin, "European gallium nitride capability," in *2015 IEEE Radar Conference (RadarCon)*, 2015: IEEE, pp. 0248-0252.

[16] X. Ke, J. Sankman, Y. Chen, L. He, and D. B. Ma, "A Tri-Slope Gate Driving GaN DC–DC Converter With Spurious Noise Compression and Ringing Suppression for Automotive Applications," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 1, pp. 247-260, 2018.

[17] A. Seidel and B. Wicht, "25.3 A 1.3 A gate driver for GaN with fully integrated gate charge buffer capacitor delivering 11nC enabled by high-voltage energy storing," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, 2017: IEEE, pp. 432-433.

[18] F. Medjdoub *et al.*, "Evaluation of AlInN/GaN HEMTs on sapphire substrate in microwave, time and temperature domains," *Electronics Letters*, vol. 43, no. 5, pp. 309-311, 2007.

[19] D. Maier *et al.*, "Testing the temperature limits of GaN-based HEMT devices," *IEEE Transactions on device materials reliability*, vol. 10, no. 4, pp. 427-436, 2010.

[20] F. Medjdoub *et al.*, "Can InAlN/GaN be an alternative to high power/high temperature AlGaN/GaN devices?," in *2006 International Electron Devices Meeting*, 2006: IEEE, pp. 1-4.

[21] Z. Xu *et al.*, "High temperature characteristics of GaN-based inverter integrated with enhancement-mode (E-mode) MOSFET and depletion-mode (D-mode) HEMT," *IEEE Electron Device Letters*, vol. 35, no. 1, pp. 33-35, 2014.

[22] T. Hussain *et al.*, "GaN HFET digital circuit technology," 2004.

[23] J. Watson and G. Castro, "A review of high-temperature electronics technology and applications," *Journal of Materials Science: Materials in Electronics*, vol. 26, no. 12, pp. 9226-9235, 2015.

[24] B. W. Ohme, T. B. Lucking, G. R. Gardner, E. E. Vogt, and J. C. Tsang, "High Temperature 0.8 Micron 5V SOI CMOS for Analog/Mixed Signal Applications," *Oil Natural Gas Technology*, p. 43, 2007.

[25] M. A. Huque, S. K. Islam, L. M. Tolbert, and B. Blalock, "A 200° C universal gate driver integrated circuit for extreme environment applications," *IEEE Transactions on Power Electronics*, vol. 27, no. 9, pp. 4153-4162, 2012.

[26] E. Boufouss, L. Francis, V. Kilchytska, P. Gérard, P. Simon, and D. Flandre, "Ultra-low power high temperature and radiation hard complementary metal-oxide-semiconductor (CMOS) silicon-on-insulator (SOI) voltage reference," *Sensors*, vol. 13, no. 12, pp. 17265-17280, 2013.

[27] B. Ohme, "High-temperature SOI technologies at Honeywell," in *Extreme Environment Electronics*: CRC Press, 2012, pp. 319-329.

[28] T. J. Thornton, W. Lepkowski, S. J. Wilk, M. Ghajar, A. Balijepalli, and J. Ervin, "CMOS-compatible silicon-on-insulator MESFETs for extreme environments," in *Extreme Environment Electronics*, 2012, pp. 253-261.

[29] W. Lepkowski, M. R. Ghajar, S. J. Wilk, N. Summers, T. J. Thornton, and P. S. Fechner, "Scaling SOI MESFETs to 150-nm CMOS technologies," *IEEE Transactions on Electron Devices*, vol. 58, no. 6, pp. 1628-1634, 2011.

[30] J. D. Cressler, "Silicon-germanium as an enabling technology for extreme environment electronics," vol. 10, no. 4, pp. 437-448, 2010.

[31] J. D. Cressler, *Silicon Heterostructure Handbook: Materials, Fabrication, Devices, Circuits and Applications of SiGe and Si Strained-Layer Epitaxy*. CRC press, 2005.

[32] J. D. Cressler and G. Niu, *Silicon-Germanium heterojunction bipolar transistors*. Artech house, 2003.

[33] J. D. Cressler, "Radiation effects in SiGe technology," vol. 60, no. 3, pp. 1992-2014, 2013.

[34] T. Chen *et al.*, "On the high-temperature (to 300 C) characteristics of SiGe HBTs," *IEEE Transactions on Electron Devices*, vol. 51, no. 11, pp. 1825-1832, 2004.

[35] A. K. Sutton *et al.*, "An investigation of dose rate and source dependent effects in 200 GHz SiGe HBTs," *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3166-3174, 2006.

[36] T. England *et al.*, "A new approach to designing electronic systems for operation in extreme environments: Part II-The SiGe remote electronics unit," *IEEE Aerospace Electronic Systems Magazine*, vol. 27, no. 7, pp. 29-41, 2012.

[37] L. Najafizadeh *et al.*, "Sub-1-K operation of SiGe transistors and circuits," *IEEE Electron Device Letters*, vol. 30, no. 5, pp. 508-510, 2009.

[38] J. C. Bardin and S. Weinreb, "A 0.1–5 GHz Cryogenic SiGe MMIC LNA," *IEEE Microwave Wireless Components Letters*, vol. 19, no. 6, pp. 407-409, 2009.

[39] N. Nambiar *et al.*, "SiGe BiCMOS 12-bit 8-channel low power Wilkinson ADC," in *2008 51st Midwest Symposium on Circuits and Systems*, 2008: IEEE, pp. 650-653.

[40] Z. Chen and F. F. Dai, "A 3mW 8-Bit radiation-hardened-by-design DAC for ultra-wide temperature range from− 180° C to 120° C," in *2011 IEEE International Symposium of Circuits and Systems (ISCAS)*, 2011: IEEE, pp. 997-1000.

[41] B. Sissons, A. Mantooth, J. Di, J. A. Holmes, and A. M. Francis, "SiGe BiCMOS comparator for extreme environment applications," in *2015 IEEE Aerospace Conference*, 2015: IEEE, pp. 1-8.

[42] A. S. Cardoso *et al.*, "On the cryogenic RF linearity of SiGe HBTs in a fourth-generation 90-nm SiGe BiCMOS technology," *IEEE Transactions on Electron Devices*, vol. 62, no. 4, pp. 1127-1135, 2015.

[43] W.-C. Lien, N. Damrongplasit, J. H. Paredes, D. G. Senesky, T.-J. K. Liu, and A. P. Pisano, "4H-SiC N-channel JFET for operation in high-temperature environments," *IEEE Journal of the Electron Devices Society*, vol. 2, no. 6, pp. 164-167, 2014.

[44] S. Singh and J. A. Cooper, "Bipolar integrated circuits in 4H-SiC," *IEEE Transactions on Electron Devices*, vol. 58, no. 4, pp. 1084-1090, 2011.

[45] P. G. Neudeck *et al.*, "6H-SiC transistor integrated circuits demonstrating prolonged operation at 500 C," 2008.

[46] P. G. Neudeck *et al.*, "Extreme temperature 6H-SiC JFET integrated circuit technology," *physica status solidi*, vol. 206, no. 10, pp. 2329-2345, 2009.

[47] N. Kuhns *et al.*, "Complex high-temperature CMOS silicon carbide digital circuit designs," *IEEE Transactions on Device Materials Reliability,* vol. 16, no. 2, pp. 105-111, 2016.

[48] H. Elgabra and S. Singh, "High temperature simulation of 4H-SiC bipolar circuits," *IEEE Journal of the Electron Devices Society,* vol. 3, no. 3, pp. 302-305, 2015.

[49] A. Rahman *et al.*, "High-temperature SiC CMOS comparator and op-amp for protection circuits in voltage regulators and switch-mode converters," *IEEE Journal of Emerging Selected Topics in Power Electronics,* vol. 4, no. 3, pp. 935-945, 2016.

[50] J. Yang, "A harsh environment wireless pressure sensing solution utilizing high temperature electronics," *Sensors,* vol. 13, no. 3, pp. 2719-2734, 2013.

[51] J. A. Valle-Mayorga, A. Rahman, and H. A. Mantooth, "A SiC NMOS linear voltage regulator for high-temperature applications," *IEEE Transactions on Power Electronics,* vol. 29, no. 5, pp. 2321-2328, 2014.

[52] M. Alexandru, M. Florentin, A. Constant, B. Schmidt, P. Michel, and P. Godignon, "5 MeV proton and 15 MeV electron radiation effects study on 4H-SiC nMOSFET electrical parameters," in *2013 14th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, 2013: IEEE, pp. 1-6.

[53] A. Siddiqui, H. Elgabra, and S. Singh, "The current status and the future prospects of surface passivation in 4H-SiC transistors," *IEEE Transactions on Device Materials Reliability,* vol. 16, no. 3, pp. 419-428, 2016.

[54] P.-C. Chou, S.-H. Chen, T.-E. Hsieh, S. Cheng, J. del Alamo, and E. Chang, "Evaluation and reliability assessment of GaN-on-Si MIS-HEMT for power switching applications," *Energies,* vol. 10, no. 2, p. 233, 2017.

[55] T. J. Flack, B. N. Pushpakaran, and S. B. Bayne, "GaN technology for power electronic applications: a review," *Journal of Electronic Materials,* vol. 45, no. 6, pp. 2673-2682, 2016.

[56] D. W. Runton, B. Trabert, J. B. Shealy, and R. Vetury, "History of GaN: High-power RF gallium nitride (GaN) from infancy to manufacturable process and beyond," *IEEE Microwave Magazine,* vol. 14, no. 3, pp. 82-93, 2013.

[57] H. á. Maruska and J. Tietjen, "The preparation and properties of vapor-deposited single-crystal-line GaN," *Applied Physics Letters,* vol. 15, no. 10, pp. 327-329, 1969.

[58] C. Yang, "Fabrication and characterization of AlGaN/GaN high electron mobility transistor," 2015.

[59] P. Javorka, "Fabrication and Characterization of AIGaN/GaN High Electron Mobility Transistors," PhD dissertation, Rheinisch-Westfalischen Technischen Hochschule Aache, Bibliothek der RWTH Aachen, 2004.

[60] R. F. Pierret and G. W. Neudeck, *Advanced semiconductor fundamentals*. Addison-Wesley Reading, MA, 1987.

[61] P. G. Neudeck, R. S. Okojie, and L.-Y. Chen, "High-temperature electronics-a role for wide bandgap semiconductors?," *Proceedings of the IEEE,* vol. 90, no. 6, pp. 1065-1076, 2002.

[62] R. T. Kemerley, H. B. Wallace, and M. N. Yoder, "Impact of wide bandgap microwave devices on DoD systems," *Proceedings of the IEEE,* vol. 90, no. 6, pp. 1059-1064, 2002.

[63] J. Baliga, "Modern power devices," 1987.

[64] S. M. Sze and K. K. Ng, *Physics of semiconductor devices*. John wiley & sons, 2006.

[65] K. J. Chen *et al.*, "GaN-on-Si power technology: Devices and applications," *IEEE Transactions on Electron Devices,* vol. 64, no. 3, pp. 779-795, 2017.

[66] E. A. Jones, F. F. Wang, and D. Costinett, "Review of commercial GaN power devices and GaN-based converter design challenges," *IEEE Journal of Emerging Selected Topics in Power Electronics,* vol. 4, no. 3, pp. 707-719, 2016.

[67] R. S. Pengelly, S. M. Wood, J. W. Milligan, S. T. Sheppard, W. L. Pribble, and Techniques, "A review of GaN on SiC high electron-mobility power transistors and MMICs," *IEEE Transactions on Microwave Theory Techniques,* vol. 60, no. 6, pp. 1764-1783, 2012.

[68] H. Mantooth and J. Cressler, "Power device platforms," in *Extreme Environment Electronics*: ed Boca Raton, FL: CRC Press, 2013, p. 243.

[69] A. R. Powell and L. B. Rowland, "SiC materials-progress, status, and potential roadblocks," *Proceedings of the IEEE,* vol. 90, no. 6, pp. 942-955, 2002.

[70] S. Pearton, J. Zolper, R. Shul, and F. Ren, "GaN: Processing, defects, and devices," *Journal of applied physics,* vol. 86, no. 1, pp. 1-78, 1999.

[71] F. Lin *et al.*, "Low resistance Ti/Al/Ni/Au Ohmic contact to (NH 4) 2 S x treated n-type GaN for high temperature applications," in *2008 9th International Conference on Solid-State and Integrated-Circuit Technology*, 2008: IEEE, pp. 726-729.

[72] R. Cuerdo, J. Pedros, and F. Calle, "Characterization of Schottky contacts on n-GaN at high temperature," in *Conference on Electron Devices, 2005 Spanish*, 2005: IEEE, pp. 175-178.

[73] F. Medjdoub, M. Zegaoui, D. Ducatteau, N. Rolland, and P. Rolland, "High-performance low-leakage-current AlN/GaN HEMTs grown on silicon substrate," *IEEE Electron Device Letters,* vol. 32, no. 7, pp. 874-876, 2011.

[74] Y. Dora, A. Chakraborty, L. McCarthy, S. Keller, S. DenBaars, and U. Mishra, "High breakdown voltage achieved on AlGaN/GaN HEMTs with integrated slant field plates," *IEEE Electron Device Letters,* vol. 27, no. 9, pp. 713-715, 2006.

[75] S. Haffouz, H. Tang, J. Bardwell, E. Hsu, J. Webb, and S. Rolfe, "AlGaN/GaN field effect transistors with C-doped GaN buffer layer as an electrical isolation template grown by molecular beam epitaxy," *Solid-state electronics,* vol. 49, no. 5, pp. 802-807, 2005.

[76] A. Corrion *et al.*, "Enhancement-mode AlN/GaN/AlGaN DHFET with 700-mS/mm gm and 112-GHz fT," *IEEE Electron Device Letters,* vol. 31, no. 10, pp. 1116-1118, 2010.

[77] V. Adivarahan, M. Gaevski, A. Koudymov, J. Yang, G. Simin, and M. A. Khan, "Selectively doped high-power AlGaN/InGaN/GaN MOS-DHFET," *IEEE electron device letters,* vol. 28, no. 3, pp. 192-194, 2007.

[78] C.-H. Chen *et al.*, "High-transconductance self-aligned AlGaN/GaN modulation-doped field-effect transistors with regrown ohmic contacts," *Applied physics letters,* vol. 73, no. 21, pp. 3147-3149, 1998.

[79] J. W. Chung, W. E. Hoke, E. M. Chumbes, and T. Palacios, "AlGaN/GaN HEMT With 300-GHz fmax," *IEEE Electron Device Letters,* vol. 31, no. 3, pp. 195-197, 2010.

[80] S. Arulkumaran, T. Egawa, H. Ishikawa, and T. Jimbo, "Characterization of different-Al-content Al x Ga 1− x N/GaN heterostructures and high-electron-mobility transistors on sapphire," *Journal of Vacuum Science Technology B: Microelectronics Nanometer Structures Processing, Measurement, Phenomena,* vol. 21, no. 2, pp. 888-894, 2003.

[81] X. Cao *et al.*, "Depth and thermal stability of dry etch damage in GaN Schottky diodes," *Applied physics letters,* vol. 75, no. 2, pp. 232-234, 1999.

[82] C. Chen *et al.*, "Fabrication of Enhancement-Mode AlGaN/GaN MISHEMTs by Using Fluorinated Al2O3 as Gate Dielectrics," *IEEE Electron Device Letters,* vol. 32, no. 10, pp. 1373-1375, 2011.

[83] D. S. Lee *et al.*, "245-GHz InAlN/GaN HEMTs with oxygen plasma treatment," *IEEE Electron Device Letters,* vol. 32, no. 6, pp. 755-757, 2011.

[84] F. Medjdoub *et al.*, "Characteristics of Al2O3/AlInN/GaN MOSHEMT," *Electronics letters,* vol. 43, no. 12, pp. 691-692, 2007.

[85] H. Zhang and E. Yu, "Demonstration and analysis of reduced reverse-bias leakage current via design of nitride semiconductor heterostructures grown by molecular-beam epitaxy," *Journal of applied physics,* vol. 99, no. 1, p. 014501, 2006.

[86] M. Dipalo *et al.*, "Combining diamond electrodes with GaN heterostructures for harsh environment ISFETs," *Diamond Related Materials,* vol. 18, no. 5-8, pp. 884-889, 2009.

[87] J. Song, W. Lu, J. S. Flynn, and G. R. Brandes, "Pt-Al Ga N⁄Ga N Schottky diodes operated at 800° C for hydrogen sensing," *Applied Physics Letters,* vol. 87, no. 13, p. 133501, 2005.

[88] O. Ambacher *et al.*, "Thermal stability and desorption of Group III nitrides prepared by metal organic chemical vapor deposition," *Journal of Vacuum Science Technology B: Microelectronics Nanometer Structures Processing, Measurement, Phenomena,* vol. 14, no. 6, pp. 3532-3542, 1996.

[89] P. May, H. Tsai, W. Wang, and J. Smith, "Deposition of CVD diamond onto GaN," *Diamond Related materials,* vol. 15, no. 4-8, pp. 526-530, 2006.

[90] H. Kim, R. M. Thompson, V. Tilak, T. R. Prunty, J. R. Shealy, and L. F. Eastman, "Effects of SiN passivation and high-electric field on AlGaN-GaN HFET degradation," *IEEE Electron device letters,* vol. 24, no. 7, pp. 421-423, 2003.

[91] X. Hu *et al.*, "Si3N4/AlGaN/GaN–metal–insulator–semiconductor heterostructure field–effect transistors," *Applied Physics Letters,* vol. 79, no. 17, pp. 2832-2834, 2001.

[92] Y.-F. Wu, M. Moore, A. Saxler, T. Wisleder, and P. Parikh, "40-W/mm double field-plated GaN HEMTs," in *2006 64th device research conference*, 2006: IEEE, pp. 151-152.

[93] J. W. Chung, O. I. Saadat, J. M. Tirado, X. Gao, S. Guo, and T. Palacios, "Gate-Recessed InAlN/GaN HEMTs on SiC Substrate With Al2O3 Passivation," *IEEE Electron Device Letters,* vol. 30, no. 9, pp. 904-906, 2009.

[94] T. Hashizume, S. Ootomo, and H. Hasegawa, "Suppression of current collapse in insulated gate AlGaN/GaN heterostructure field-effect transistors using ultrathin Al2 O3 dielectric," *Applied physics letters,* vol. 83, no. 14, pp. 2952-2954, 2003.

[95] S. Abermann *et al.*, "MOCVD of HfO2 and ZrO2 high-k gate dielectrics for InAlN/AlN/GaN MOS-HEMTs," *Semiconductor Science Technology,* vol. 22, no. 12, p. 1272, 2007.

[96] Y. Irokawa *et al.*, "MgO/p-GaN enhancement mode metal-oxide semiconductor field-effect transistors," *Applied physics letters,* vol. 84, no. 15, pp. 2919-2921, 2004.

[97] S. Nuttinck *et al.*, "Thermal analysis of AlGaN-GaN power HFETs," *IEEE transactions on microwave theory techniques,* vol. 51, no. 12, pp. 2445-2452, 2003.

[98] M. Kuball *et al.*, "Thermal management and device failure assessment of high-power AlGaN/GaN HFETs," in *60th DRC. Conference Digest Device Research Conference*, 2002: IEEE, pp. 99-100.

[99] R. Aubry *et al.*, "SThM temperature mapping and nonlinear thermal resistance evolution with bias on AlGaN/GaN HEMT devices," *IEEE transactions on electron devices,* vol. 54, no. 3, pp. 385-390, 2007.

[100] P. Regoliosi *et al.*, "Experimental validation of GaN HEMTs thermal management by using photocurrent measurements," *IEEE Transactions on Electron Devices,* vol. 53, no. 2, pp. 182-188, 2006.

[101] M. Gonschorek, J.-F. Carlin, E. Feltin, M. Py, and N. Grandjean, "Self heating in AlInN/AlN/GaN high power devices: Origin and impact on contact breakdown and IV characteristics," *Journal of Applied Physics,* vol. 109, no. 6, p. 063720, 2011.

[102] A. Sarua *et al.*, "Integrated micro-Raman/infrared thermography probe for monitoring of self-heating in AlGaN/GaN transistor structures," *IEEE Transactions on Electron Devices,* vol. 53, no. 10, pp. 2438-2447, 2006.

[103] M. Alomari, "Technology and characterization of InAlN/GaN FETs," Universität Ulm, 2013.

[104] I. Daumiller, C. Kirchner, M. Kamp, K. J. Ebeling, and E. Kohn, "Evaluation of the temperature stability of AlGaN/GaN heterostructure FETs," *IEEE Electron Device Letters,* vol. 20, no. 9, pp. 448-450, 1999.

[105] H. G. Xing and U. K. Mishra, "Temperature dependent iv characteristics of algan/gan hbts and gan bjts," *International journal of high speed electronics systems,* vol. 14, no. 03, pp. 819-824, 2004.

[106] B. Shelton *et al.*, "AlGaN/GaN heterojunction bipolar transistors grown by metal organic chemical vapour deposition," *Electronics Letters,* vol. 36, no. 1, pp. 80-81, 2000.

[107] K. Kumakura, T. Makimoto, and N. Kobayashi, "Low Resistance Non-Alloy Ohmic Contact to p-Type GaN Using Mg-Doped InGaN Contact Layer," *physica status solidi,* vol. 188, no. 1, pp. 363-366, 2001.

[108] T. Makimoto, Y. Yamauchi, and K. Kumakura, "High-power characteristics of GaN/InGaN double heterojunction bipolar transistors," *Applied physics letters,* vol. 84, no. 11, pp. 1964-1966, 2004.

[109] Y. C. Lee *et al.*, "GaN/InGaN heterojunction bipolar transistors with ultra-high dc power density (> 3 MW/cm2)," *physica status solidi*, vol. 209, no. 3, pp. 497-500, 2012.

[110] K. Kumakura and T. Makimoto, "High-temperature characteristics up to 590 C of apnp AlGaN/GaN heterojunction bipolar transistor," *Applied Physics Letters*, vol. 94, no. 10, p. 103502, 2009.

[111] R. D. Dupuis *et al.*, "Bipolar III-N high-power electronic devices," in *The 1st IEEE Workshop on Wide Bandgap Power Devices and Applications*, 2013: IEEE, pp. 96-99.

[112] *MORGAN: Materials for Robust Gallium Nitride. Accessed: Jan. 31, 2018. [Online]. Available: https://cordis.europa.eu/project/rcn/89921_en.html.*

[113] *ULTRAGAN: InAlN/(In)GaN Heterostructure Technology for Ultra-high Power Microwave Transistor. Accessed: Jan. 31, 2018. [Online]. Available: https://cordis.europa.eu/project/rcn/75935_en.html.*

[114] D. Maier *et al.*, "InAlN/GaN HEMTs for Operation in the 1000° C Regime: A First Experiment," *IEEE Electron Device Letters*, vol. 33, no. 7, pp. 985-987, 2012.

[115] M. Alomari *et al.*, "Diamond overgrown InAlN/GaN HEMT," *Diamond Related Materials*, vol. 20, no. 4, pp. 604-608, 2011.

[116] D. Maier *et al.*, "Above 500 C Operation of InAlN/GaN HEMTs," in *2009 Device Research Conference*, 2009: IEEE, pp. 285-286.

[117] D. Maier *et al.*, "Towards electronics at 1000° C," in *69th Device Research Conference*, 2011: IEEE, pp. 73-74.

[118] D. Maier *et al.*, "High temperature stability of nitride-based power HEMTs," in *18-th INTERNATIONAL CONFERENCE ON MICROWAVES, RADAR AND WIRELESS COMMUNICATIONS*, 2010: IEEE, pp. 1-4.

[119] T.-T. Kao *et al.*, "Temperature-dependent characteristics of GaN homojunction rectifiers," *IEEE Transactions on Electron Devices*, vol. 62, no. 8, pp. 2679-2683, 2015.

[120] Z. Gao, M. F. Romero, M. Á. Pampillón, E. San Andrés, and F. Calle, "Thermal assessment of AlGaN/GaN MOS-HEMTs on Si substrate using Gd2O3 as gate dielectric," *IEEE Transactions on Electron Devices*, vol. 63, no. 7, pp. 2729-2734, 2016.

[121] *POLYSTIM Neurotechnologies. Accessed: Jan. 31, 2018. [Online]. Available: http://polystim.org/.*

[122] A. Abubakr, A. Hassan, A. Ragab, S. Yacout, Y. Savaria, and M. Sawan, "High-Temperature Modeling of the IV Characteristics of GaN150 HEMT Using Machine Learning Techniques," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2018, pp. 1-5.

[123] M. Amer, A. Hassan, A. Ragab, S. Yacout, Y. Savaria, and M. Sawan, "High-Temperature Empirical Modeling for the IV Characteristics of GaN150-Based HEMT," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2018: IEEE, pp. 1-5.

[124] A. Hassan, M. Ali, A. Trigui, S. Hached, Y. Savaria, and M. Sawan, "Stability of GaN150-based HEMT in high temperature up to 400°C," in *2017 15th IEEE International New Circuits and Systems Conference (NEWCAS)*, 2017, pp. 133-136.

[125] A. Hassan, A. Trigui, U. Shafique, Y. Savaria, and M. Sawan, "Wireless power transfer through metallic barriers enclosing a harsh environment; feasibility and preliminary results," in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2016, pp. 2391-2394.

[126] K. Gottfried *et al.*, "A High Temperature Stable Metallization Scheme for SiC-Technology Operating at 400 C in Air," in *Materials Science Forum*, 1998, vol. 264: TRANS TECH PUBLICATIONS LTD, pp. 795-798.

[127] R. Okojie, D. Lucko, and D. Spry, "Reliability of Ti/TaSi/Pt ohmic contacts on 4H-and 6H-SiC after 1000 hours in air at 600 C," in *Proc*, 2001, p. 6.

[128] S. C. Shen, "III-nitride platforms," in *Extreme Environment Electronics*. Boca Raton, FL, USA: CRC Press, 2012, pp. pp. 263–273.

[129] P. Herfurth *et al.*, "Ultrathin Body InAlN/GaN HEMTs for High-Temperature (600°C) Electronics," *IEEE Electron Device Letters*, vol. 34, no. 4, pp. 496-498, 2013.

[130] J. Bourne, R. Schupbach, B. Hollosi, J. Di, A. Lostetter, and H. A. Mantooth, "Ultra-Wide Temperature (-230° C to 130° C) DC-Motor Drive with SiGe Asynchronous Controller," in *2008 IEEE Aerospace Conference*, 2008: IEEE, pp. 1-15.

[131] D. Ma, X. Geng, F. F. Dai, and J. D. Cressler, "A 6th order Butterworth SC low pass filter for cryogenic applications from− 180° c to 120° c," in *2009 IEEE Aerospace conference*, 2009: IEEE, pp. 1-8.

[132] S. Becu, S. Cremer, O. Noblanc, J. Autran, and P. Delpech, "Characterization and modeling of Al2O3 MIM capacitors: temperature and electrical field effects," in *Proceedings of 35th European Solid-State Device Research Conference, 2005. ESSDERC 2005.*, 2005, pp. 265-268.

[133] C. Hung-Ming, T. Kong-Beng, T. Sheng-Fu, and L. Wen-Chau, "Temperature-dependent characteristics of polysilicon and diffused resistors," *IEEE Transactions on Electron Devices*, vol. 50, no. 5, pp. 1413-1415, 2003.

[134] R. Groves, D. L. Harame, and D. Jadus, "Temperature dependence of Q and inductance in spiral inductors fabricated in a silicon-germanium/BiCMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 9, pp. 1455-1459, 1997.

[135] J. Galipeau and G. Slama, "Reliability Testing on a Multilayer Chip Inductor Fabricated From a Ferrite With a 350 °C Curie Point," vol. 2011, no. HITEN, pp. 000014-000020, 2011.

[136] J. D. Cressler *et al.*, "Proton radiation response of SiGe HBT analog and RF circuits and passives," *IEEE Transactions on Nuclear Science*, vol. 48, no. 6, pp. 2238-2243, 2001.

[137] S. O. Dorst and L. H. Wurzel, "The Effect of Radiation Environment on Film Resistors," in *1962 IRE National Convention*, 1962, pp. 206-214.

[138] L. Zhiyun *et al.*, "Proton radiation effects in 4H-SiC diodes and MOS capacitors," *IEEE Transactions on Nuclear Science*, vol. 51, no. 6, pp. 3748-3752, 2004.

[139] G. K. Lum *et al.*, "New experimental findings for single-event gate rupture in MOS capacitors and linear devices," *IEEE Transactions on Nuclear Science*, vol. 51, no. 6, pp. 3263-3269, 2004.

[140] B. D. Olson, W. T. Holman, L. W. Massengill, B. L. Bhuva, and P. R. Fleming, "Single-Event Effect Mitigation in Switched-Capacitor Comparator Designs," *IEEE Transactions on Nuclear Science,* vol. 55, no. 6, pp. 3440-3446, 2008.

[141] A. L. Sternberg, L. W. Massengill, M. Hale, and B. Blalock, "Single-Event Sensitivity and Hardening of a Pipelined Analog-to-Digital Converter," *IEEE Transactions on Nuclear Science,* vol. 53, no. 6, pp. 3532-3538, 2006.

[142] T. Wang, K. Wang, L. Chen, A. Dinh, B. Bhuva, and R. Shuler, "A RHBD LC-Tank Oscillator Design Tolerant to Single-Event Transients," *IEEE Transactions on Nuclear Science,* vol. 57, no. 6, pp. 3620-3625, 2010.

[143] A. Hassan, B. Gosselin, and M. Sawan, "Ultra-low power CMOS voltage reference for high temperature applications up to 300°C," in *2015 IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, 2015, pp. 77-80.

[144] J. L. Sepulveda, "Advanced microelectronic packaging using BeO ceramics," in *Proceedings. 4th International Symposium on Advanced Packaging Materials Processes, Properties and Interfaces (Cat. No.98EX153)*, 1998, pp. 287-293.

[145] Y. Chen, C. T. Weber, M. Mojarradi, and E. Kolawa, *Micro- and nano-electronic technologies and their qualification methodology for space applications under harsh environments* (SPIE Defense, Security, and Sensing). SPIE, 2011.

[146] A. A. Shapiro, C. Tudryn, D. Schatzel, and S. Tseng, "Electronic Packaging Materials for Extreme, Low Temperature, Fatigue Environments," *IEEE Transactions on Advanced Packaging,* vol. 33, no. 2, pp. 408-420, 2010.

[147] S. Sivaswamy *et al.*, "System-in-package for extreme environments," in *2008 58th Electronic Components and Technology Conference*, 2008, pp. 2044-2050.

[148] J. E. Naefe, R. W. Johnson, and R. R. Grzybowski, "High-temperature storage and thermal cycling studies of thick film and wirewound resistors," *IEEE Transactions on Components and Packaging Technologies,* vol. 25, no. 1, pp. 45-52, 2002.

[149] K. Fang, R. Zhang, T. Isaacs-Smith, R. W. Johnson, E. Andarawis, and A. Vert, "Thin Film Multichip Packaging for High Temperature Digital Electronics," vol. 2011, no. HITEN, pp. 000039-000045, 2011.

[150] T. Zhang, D. Shaddock, A. Vert, R. Zhang, and R. W. Johnson, "Characterization of LTCC-Thick Film Technology for 300°C Packaging," vol. 2011, no. HITEN, pp. 000046-000051, 2011.

[151] "Communication with Milton Watts, Chief Technology Officer, Quartzdyne, Inc., Salt Lake City, UT.," ed.

[152] G. Dong, G. Lei, X. Chen, K. Ngo, and G. Q. Lu, "Edge tail length effect on reliability of DBC substrates under thermal cycling," vol. 21, no. 3, pp. 10-15, 2009.

[153] R. Klieber and R. Lerch, "Evaluation of materials for high temperature IC packaging," in *2009 15th International Workshop on Thermal Investigations of ICs and Systems*, 2009, pp. 117-120.

[154] H. Schoeller, Bansal, S., Knobloch, A., Shaddock, D., & Cho, J. , "Effects of microstructure evolution on high-temperature mechanical deformation of 95Sn–5Sb. ," in *ASME 2008*

*International Mechanical Engineering Congress and Exposition* Boston, MA, New York, NY, 2008, vol. 6: American Society of Mechanical Engineers., pp. pp. 25-32.

[155] V. Bondarenko *et al.*, "Characterization and packaging of SiC JFET power modules for extreme environment motor drives," in *Proceedings of the 2006 International High Temperature Electronics Conference, Santa Fe, NM*, 2006, pp. 488-456.

[156] P. Hagler, R. W. Johnson, and L.-Y. Chen, "SiC Die Attach Metallurgy and Processes for Applications up to 500 °C," *IEEE Transactions on Components, Packaging*

*Manufacturing Technology,* vol. 1, no. 4, pp. 630-639, 2011.

[157] C. Göbl and J. Faltenbacher, "Low temperature sinter technology die attachment for power electronic applications," in *2010 6th International Conference on Integrated Power Electronics Systems*, 2010: IEEE, pp. 1-5.

[158] D. Palmer and F. Ganyard, "Aluminum wire to thick-film connections for high-temperature operation," *IEEE Transactions on Components, Hybrids, Manufacturing Technology,* vol. 1, no. 3, pp. 219-222, 1978.

[159] J. S. Salmon, R. W. Johnson, and M. Palmer, "Thick film hybrid packaging techniques for 500C operation," in *1998 Fourth International High Temperature Electronics Conference. HITEC (Cat. No. 98EX145)*, 1998: IEEE, pp. 103-108.

[160] K. Okamoto, Y. Takematsu, M. Hitomi, Y. Ikeda, and Y. Takahashi, "Nanocomposite epoxy resin for SiC module," *Additional Papers and Presentations*, vol. 2011, no. HITEN, pp. 000196-000200, 2011.

[161] Y. Yao, G.-Q. Lu, Z. Chen, D. Boroyevich, and K. D. Ngo, "Assessment of encapsulants for high-voltage, high-temperature power electronic packaging," in *2011 IEEE Electric Ship Technologies Symposium*, 2011: IEEE, pp. 258-264.

[162] M. R. Werner and W. R. Fahrner, "Review on materials, microsensors, systems and devices for high-temperature and harsh-environment applications," *IEEE Transactions on Industrial Electronics,* vol. 48, no. 2, pp. 249-257, 2001.

[163] A. Friedberger *et al.*, "Reusable Packaging for High Temperature (800 C) and High Pressure MEMS," in *High Temperature Electronics Conference (HiTEC)*, 2006, pp. 367-370.

[164] L.-Y. Chen, "Improvement of dielectric performance of a prototype AlN high temperature chip-level package," *Additional Papers and Presentations,* vol. 2011, no. HITEN, pp. 000052-000057, 2011.

[165] P. Dreike, D. Fleetwood, D. King, D. Sprauer, and T. Zipperian, "An overview of high-temperature electronic device technologies and potential applications," *IEEE Transactions on Components, Packaging, Manufacturing Technology: Part A,* vol. 17, no. 4, pp. 594-609, 1994.

[166] A. Hassan, Y. Savaria, and M. Sawan, "GaN Integration Technology, an Ideal Candidate for High-Temperature Applications: A Review," *IEEE Access,* vol. 6, pp. 78790-78802, 2018.

[167] A. Elasser and T. P. Chow, "Silicon carbide benefits and advantages for power electronics circuits and systems," *Proceedings of the IEEE,* vol. 90, no. 6, pp. 969-986, 2002.

[168] A. Rahman, A. M. Francis, S. Ahmed, S. K. Akula, J. Holmes, and A. Mantooth, "High-temperature voltage and current references in silicon carbide CMOS," *IEEE Transactions on Electron Devices,* vol. 63, no. 6, pp. 2455-2461, 2016.

[169] C.-W. Soong, A. C. Patil, S. L. Garverick, X. Fu, and M. Mehregany, "550° C Integrated Logic Circuits using 6H-SiC JFETs," *IEEE electron device letters,* vol. 33, no. 10, pp. 1369-1371, 2012.

[170] L. Lanni, R. Ghandi, B. G. Malm, C.-M. Zetterling, and M. Ostling, "Design and characterization of high-temperature ECL-based bipolar integrated circuits in 4H-SiC," *IEEE Transactions on Electron Devices,* vol. 59, no. 4, pp. 1076-1083, 2012.

[171] A. C. Patil, X.-a. Fu, C. Anupongongarch, M. Mehregany, and S. L. Garverick, "6H-SiC JFETs for 450C Differential Sensing Applications," *Journal of microelectromechanical systems,* vol. 18, no. 4, pp. 950-961, 2009.

[172] *https://www.cree.com/*.

[173] A. Rahman *et al.*, "High temperature data converters in silicon carbide CMOS," *IEEE Transactions on Electron Devices,* vol. 64, no. 4, pp. 1426-1432, 2017.

[174] *http://www1.asmpacific.com/en/products?equipment=4*.

[175] *https://www.keysight.com/en/pd-1000000858%3Aepsg%3Apro-pn-4294A/precision-impedance-analyzer-40-hz-to-110-mhz?cc=US&lc=eng*.

[176] S. Khandelwal *et al.*, "Robust surface-potential-based compact model for GaN HEMT IC design," *IEEE Transactions on Electron Devices,* vol. 60, no. 10, pp. 3216-3222, 2013.

[177] U. Radhakrishna, "A compact transport and charge model for GaN-based high electron mobility transistors for RF applications," Massachusetts Institute of Technology, 2013.

[178] H. Zhang, "Physics Based Virtual Source Compact Model of Gallium-Nitride High Electron Mobility Transistors," University of Waterloo, 2017.

[179] I. Angelov, H. Zirath, and N. Rosman, "A new empirical nonlinear model for HEMT and MESFET devices," *IEEE Transactions on Microwave Theory Techniques,* vol. 40, no. 12, pp. 2258-2266, 1992.

[180] L. Dunleavy, C. Baylis, W. Curtice, and R. Connick, "Modeling GaN: powerful but challenging," *IEEE Microwave Magazine,* vol. 11, no. 6, pp. 82-96, 2010.

[181] M. Germain *et al.*, "GaN-on-Si power field effect transistors," in *Proceedings of 2010 International Symposium on VLSI Technology, System and Application*, 2010: IEEE, pp. 171-172.

[182] L. Chen and M. Mehregany, "A silicon carbide capacitive pressure sensor for in-cylinder pressure measurement," *Sensors and Actuators A: Physical,* vol. 145, pp. 2-8, 2008.

[183] E. Obermeier, "High temperature microsensors based on polycrystalline diamond thin films," in *Proceedings of the International Solid-State Sensors and Actuators Conference-TRANSDUCERS'95*, 1995, vol. 2: IEEE, pp. 178-181.

[184] J. Xu, G. Pickrell, X. Wang, W. Peng, K. Cooper, and A. Wang, "A novel temperature-insensitive optical fiber pressure sensor for harsh environments," *IEEE Photonics Technology Letters,* vol. 17, no. 4, pp. 870-872, 2005.

[185] Y. Zhu, K. L. Cooper, G. R. Pickrell, and A. Wang, "High-temperature fiber-tip pressure sensor," *Journal of lightwave technology*, vol. 24, no. 2, pp. 861-869, 2006.

[186] Y. Wang, Y. Jia, Q. Chen, and Y. Wang, "A passive wireless temperature sensor for harsh environment applications," *Sensors*, vol. 8, no. 12, pp. 7982-7995, 2008.

[187] H. Trang *et al.*, "Temperature-compensated structure for SAW pressure sensor in very high temperature," in *2007 IEEE International Frequency Control Symposium Joint with the 21st European Frequency and Time Forum*, 2007: IEEE, pp. 40-44.

[188] M. A. Fonseca, J. M. English, M. Von Arx, and M. G. Allen, "Wireless micromachined ceramic pressure sensor for high-temperature applications," *Journal of Microelectromechanical Systems*, vol. 11, no. 4, pp. 337-343, 2002.

[189] J. Yang, "A silicon carbide wireless temperature sensing system for high temperature applications," *Sensors*, vol. 13, no. 2, pp. 1884-1901, 2013.

[190] O. Imoru, A. Jassal, H. Polinder, E. Nieuwkoop, J. Tsado, and A. A. Jimoh, *An inductive power transfer through metal object*. Piscataway, NJ: IEEE, 2013.

[191] *https://www.kulite.com/docs/products/XTEH-10L-190.pdf*.

# APPENDIX A– CHIP 1

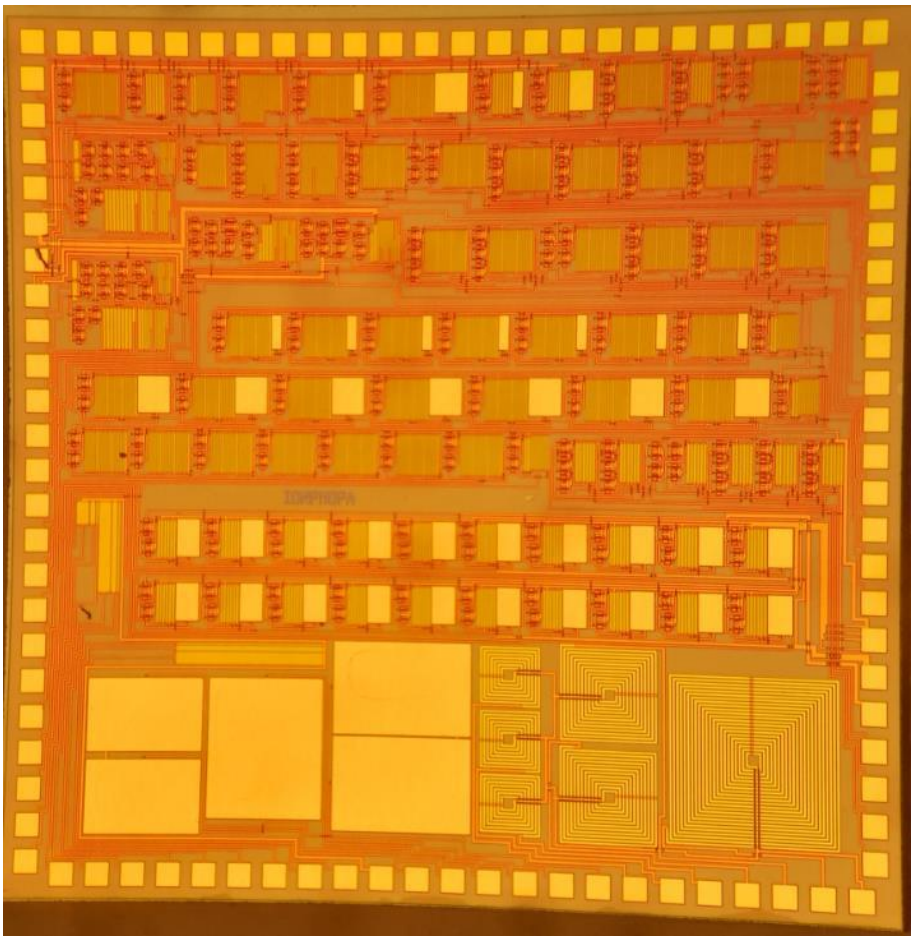


Figure 1: Micrograph of fabricated Chip1 (4 mm x 4 mm)

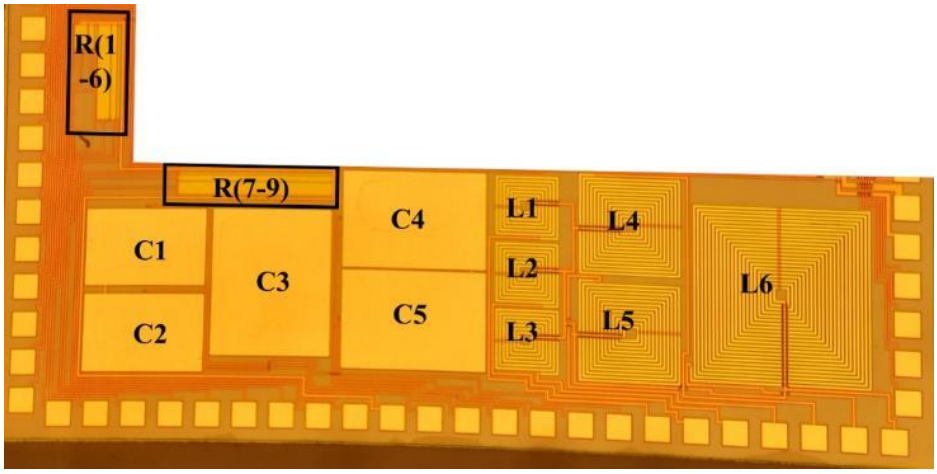
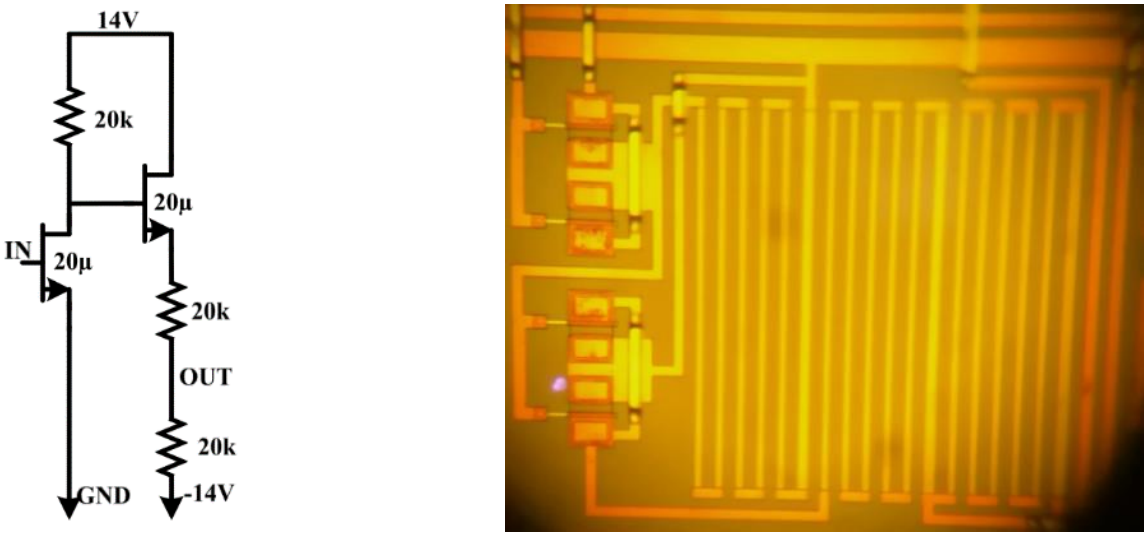



Figure 2: Micrograph of fabricated passive components

Table 1: Circuits of chip 1 and corresponding current and power consumption (simulation)

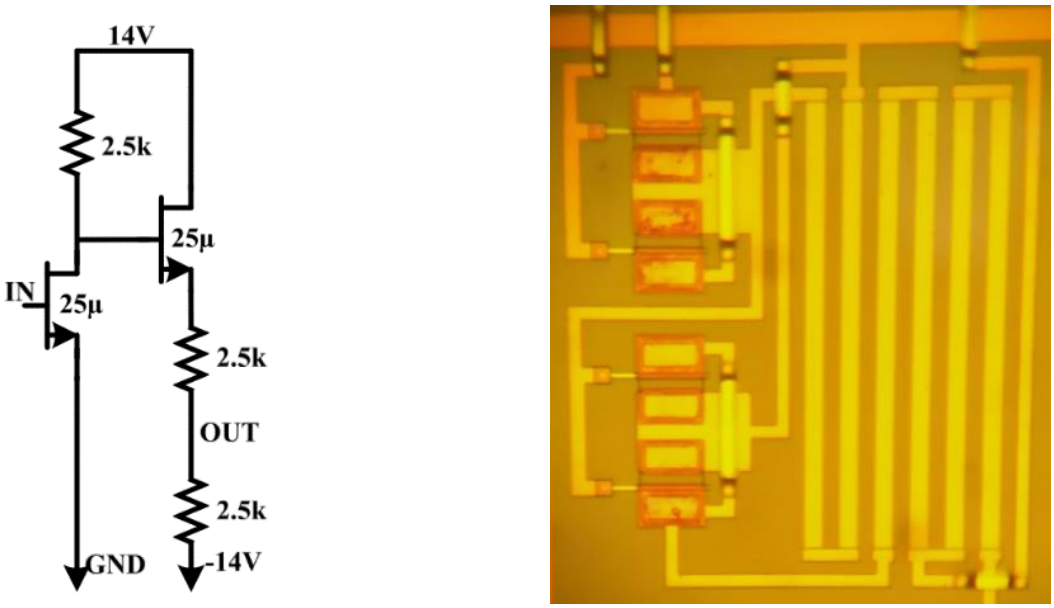
| Circuit | IDD (mA) | IGND (mA) | ISS (mA) | POWER (mW) |
|---|---|---|---|---|
| **INV1** | <1 | <1 | <1 | 20 |
| **INV2** | 9 | 5 | 4 | 182 |
| **INV3** | 6 | 5 | 1 | 98 |
| **INV4** | <1 | <1 | <1 | 20 |
| **INV5** | <1 | <1 | <1 | 20 |
| **INV6** | <1 | <1 | <1 | 20 |
| **INV7** | 9 | 5 | 4 | 182 |
| **INV8** | 9 | 5 | 4 | 182 |
| **NAND-2IN-1** | <1 | <1 | <1 | 20 |
| **NAND-2IN-2** | 9 | 5 | 4 | 182 |
| **NAND-3IN-1** | <1 | <1 | <1 | 20 |
| **NAND-3IN-2** | 9 | 5 | 4 | 182 |
| **NOR-2IN** | <1 | <1 | <1 | 20 |
| **NOR-3IN** | 1.5 | 1 | <1 | 25 |
| **XOR/XNOR** | 5 | 2 | 3 | 112 |
| **VREF1** | <1 | <1 | NA | 0.7 |
| **VREF2** | <1 | <1 | NA | 0.6 |
| **DFF1** | 6 | 3 | 3 | 126 |
| **DFF2** | 44 | 30 | 14 | 812 |
| **COMPARATOR** | 30 | 5 | 25 | 770 |
| **OSC1** | 13 | 8 | 5 | 252 |
| **OSC2** | 13 | 8 | 5 | 252 |
| **OSC3** | 13 | 8 | 5 | 252 |
| **DELAY** | 150 | 60 | 90 | 3360 |
| **AMPLIFIER** | 27 | 23 | 4 | 434 |

*NA: The circuit doesn’t need VSS power supply (only VDD and GND)



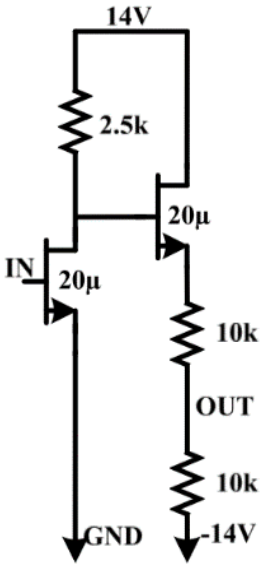

(a) (b)

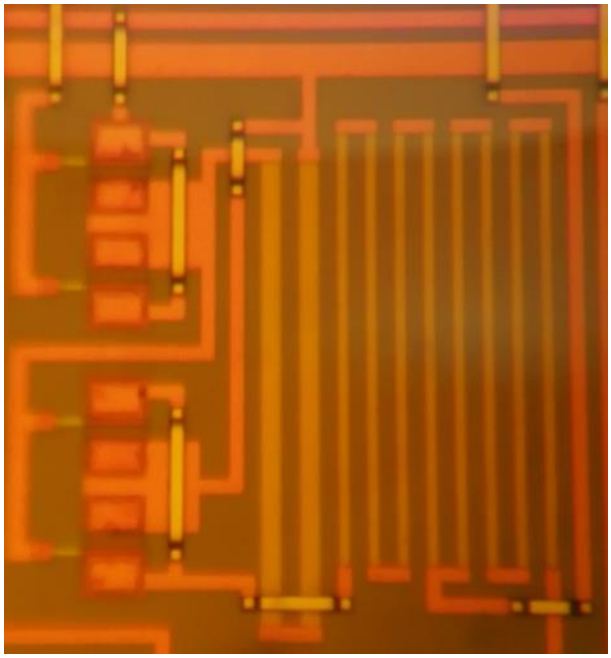
Figure 3: INV1: (a) Schematic, and (b) Micrograph




(a) (b)

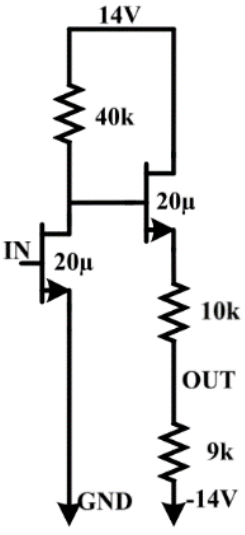
Figure 4: INV2: (a) Schematic, and (b) Micrograph

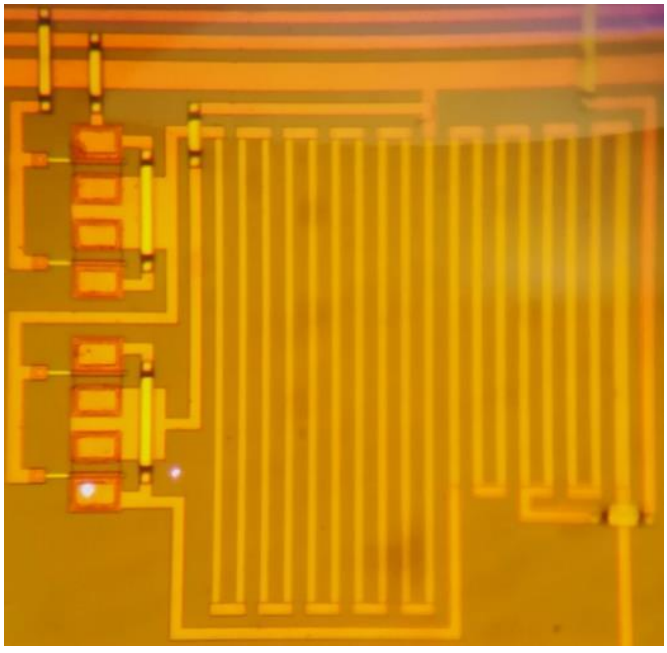


(a) (b)

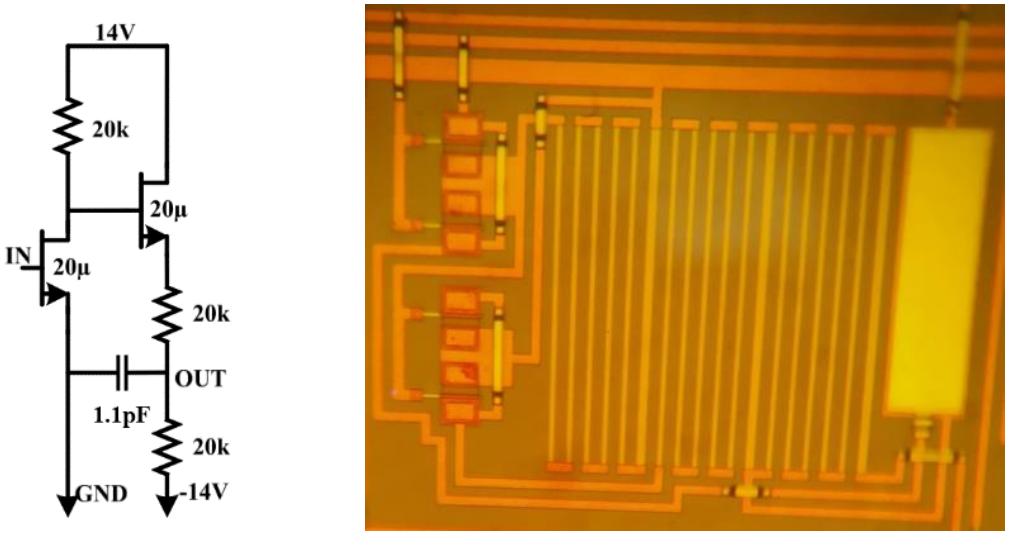
Figure 5: INV3: (a) Schematic, and (b) Micrograph



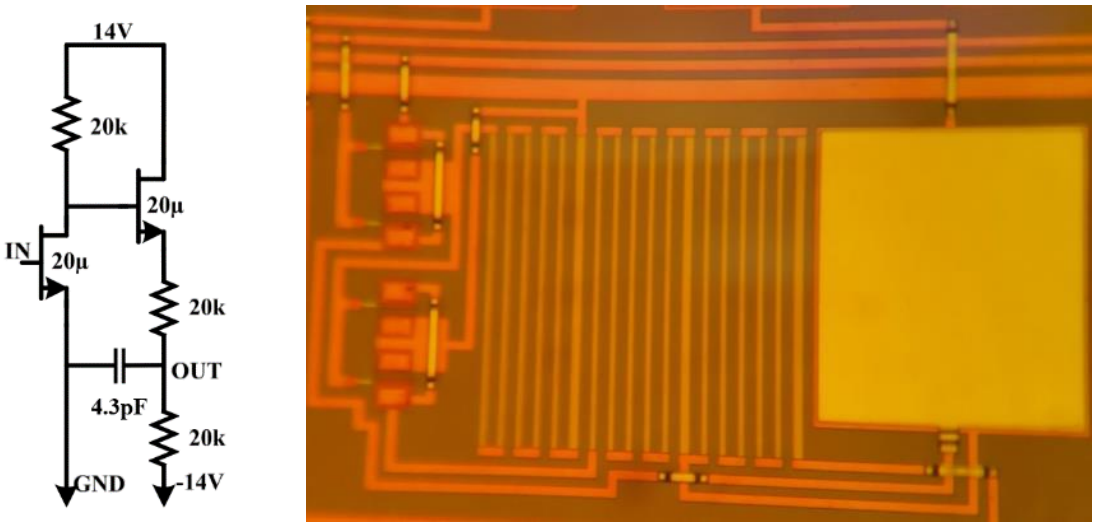
(a) (b)

Figure 6: INV4: (a) Schematic, and (b) Micrograph



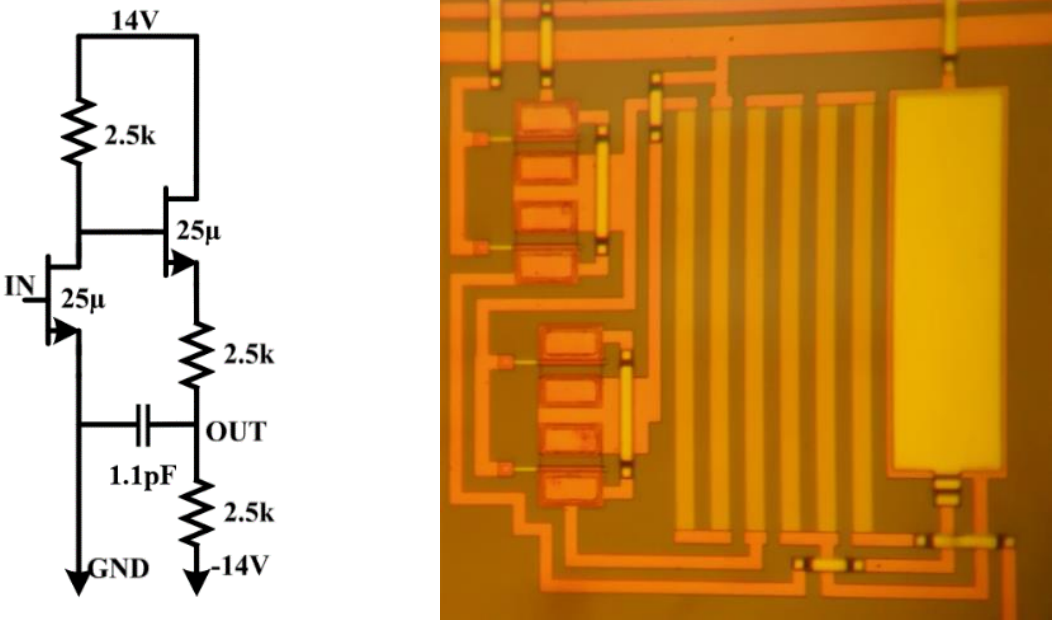

(a) (b)

Figure 7: INV5: (a) Schematic, and (b) Micrograph



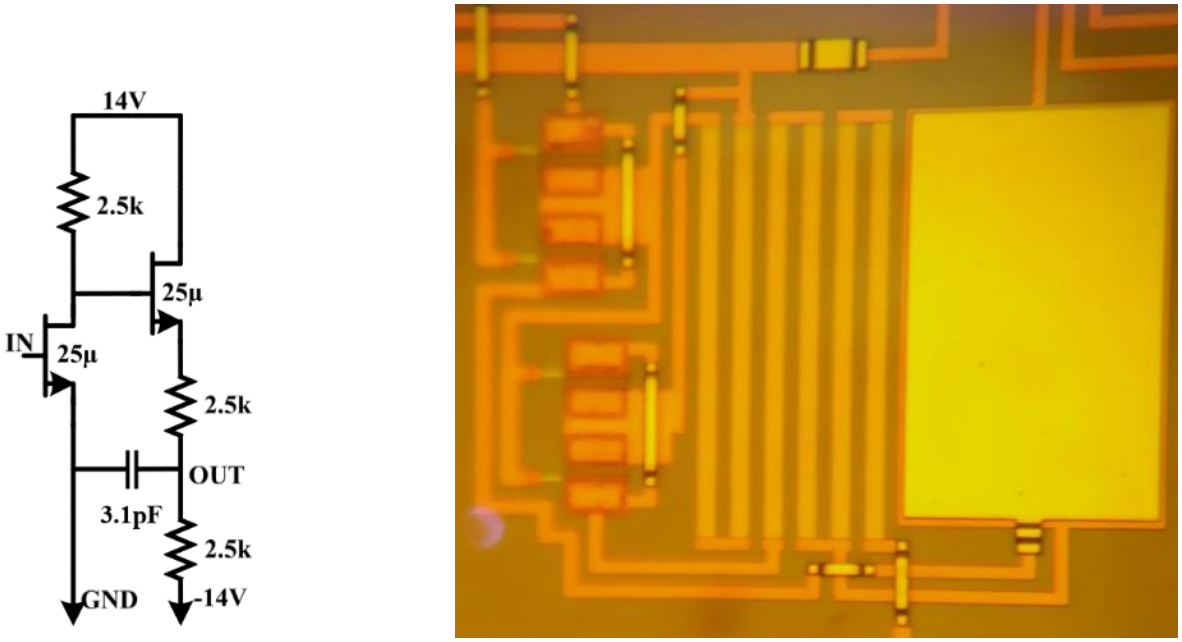

(a) (b)

Figure 8: INV6: (a) Schematic, and (b) Micrograph



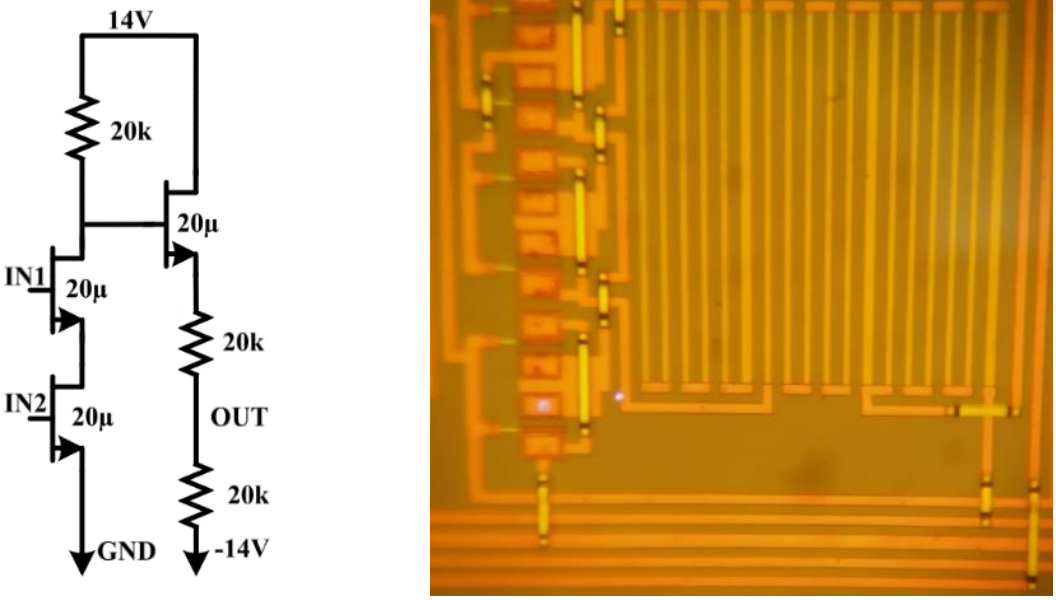

(a) (b)

Figure 9: INV7: (a) Schematic, and (b) Micrograph



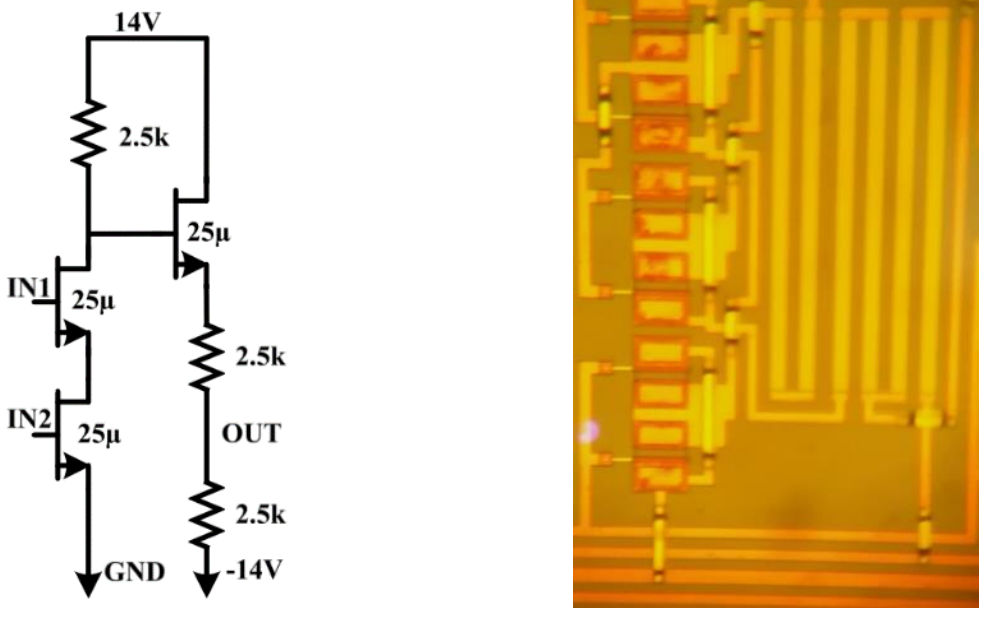

(a) (b)

Figure 10: INV8: (a) Schematic, and (b) Micrograph



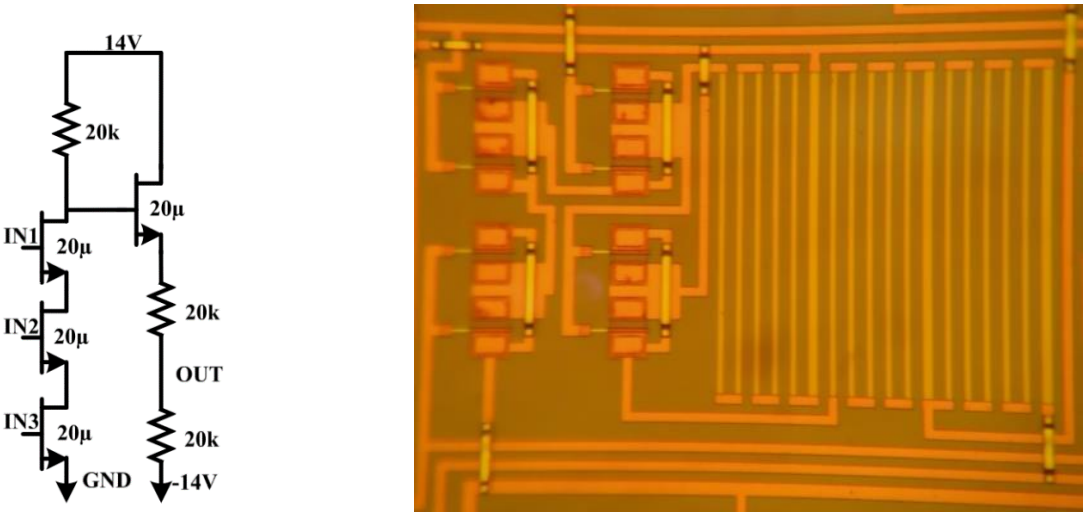

(a) (b)

Figure 10: NAND-2IN-1: (a) Schematic, and (b) Micrograph



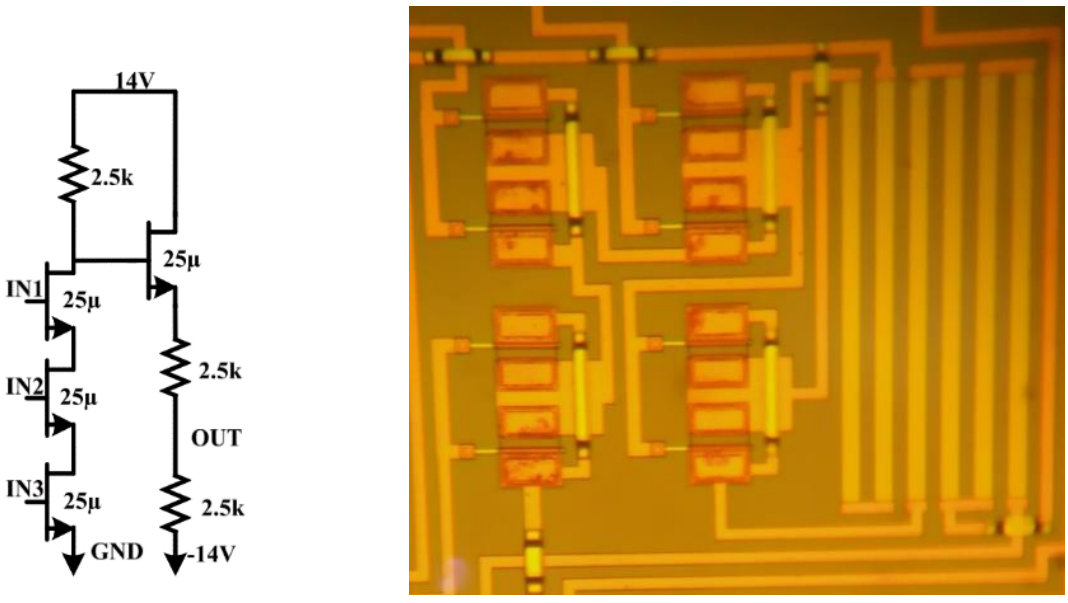

(a) (b)

Figure 11: NAND-2IN-2: (a) Schematic, and (b) Micrograph



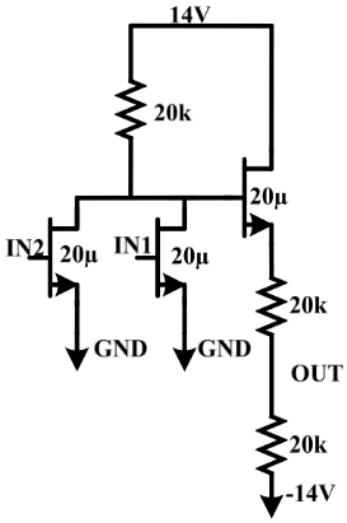

(a) (b)

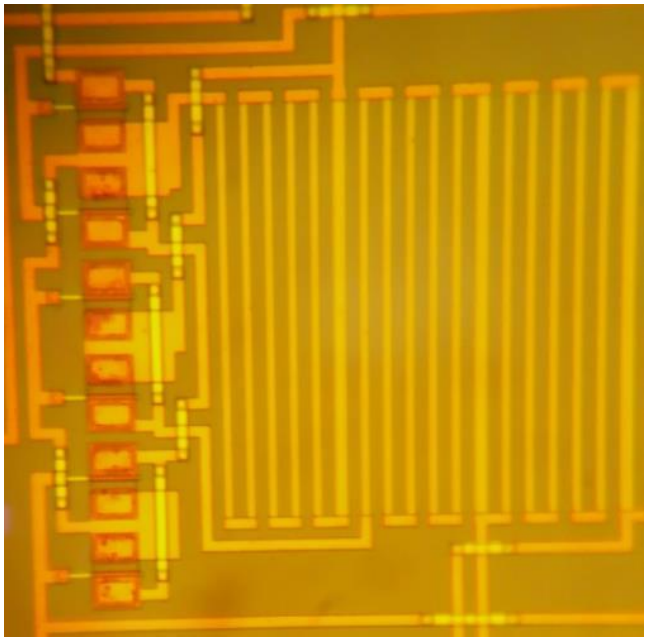
Figure 12: NAND-3IN-1: (a) Schematic, and (b) Micrograph




(a) (b)

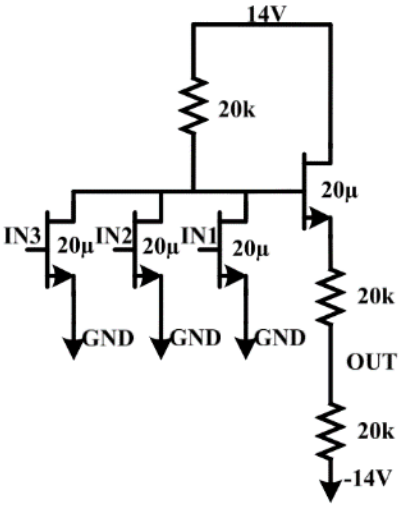
Figure 13: NAND-3IN-2: (a) Schematic, and (b) Micrograph

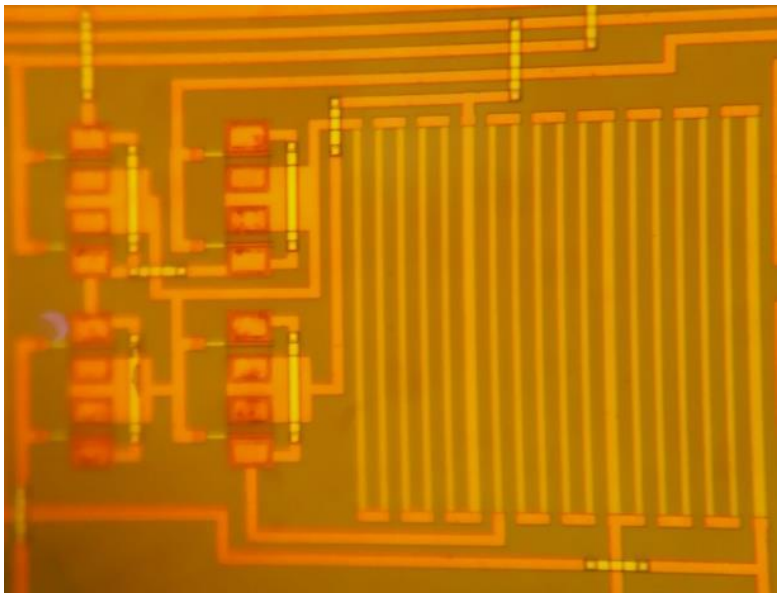


(a) (b)

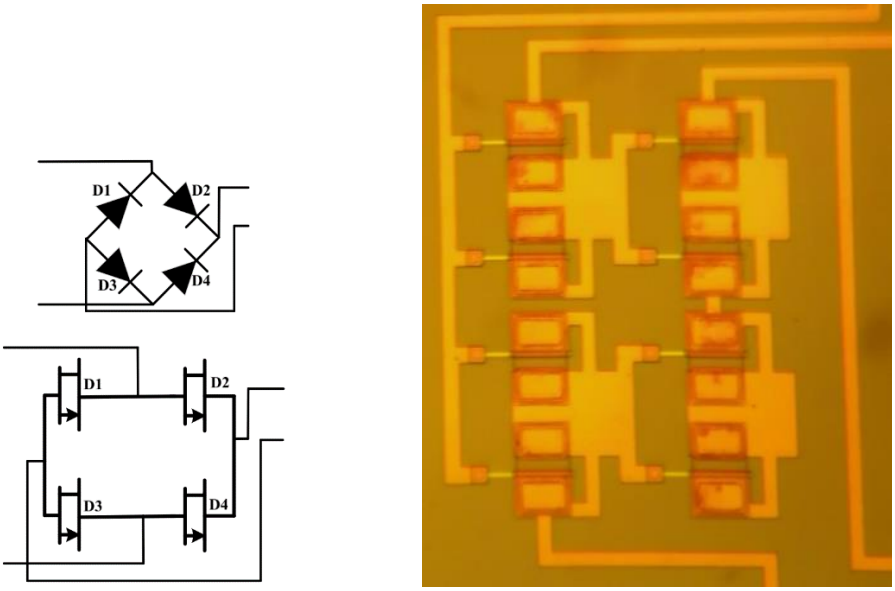
Figure 14: NOR-2IN: (a) Schematic, and (b) Micrograph



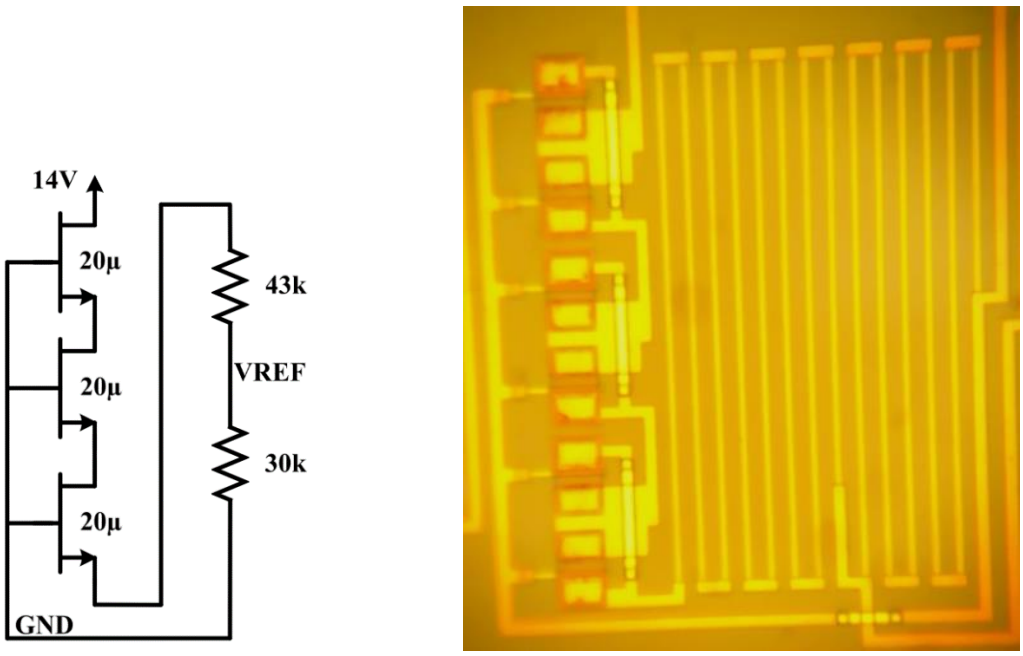
(a) (b)

Figure 15: NOR-3IN: (a) Schematic, and (b) Micrograph



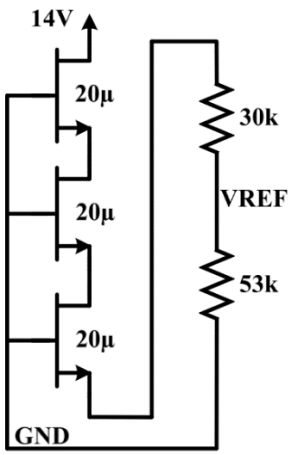

(a) (b)

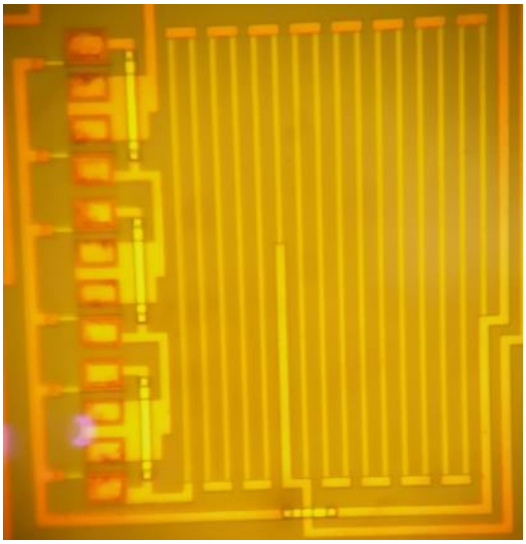
Figure 16: FBR: (a) Schematic, and (b) Micrograph




(a) (b)

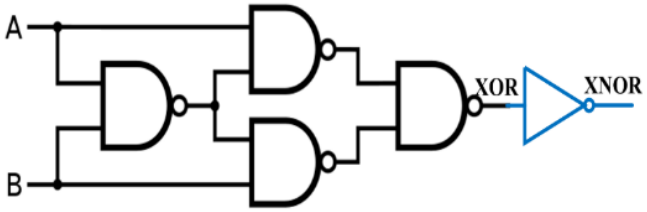
Figure 17: VREF1: (a) Schematic, and (b) Micrograph



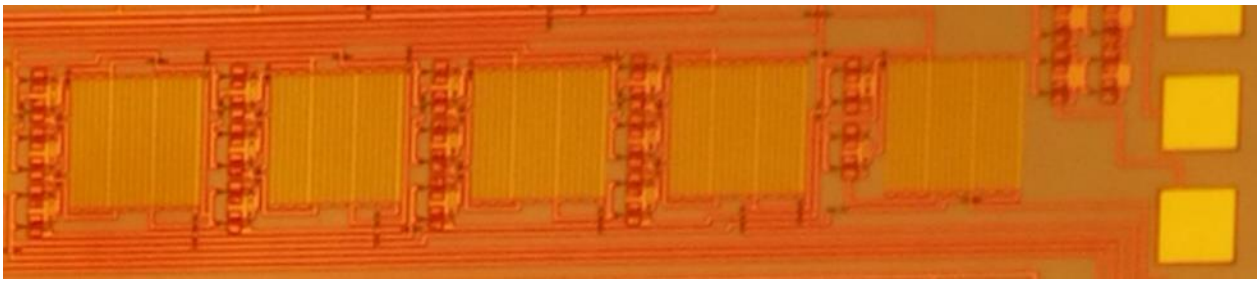



(a) (b)

Figure 18: VREF2: (a) Schematic, and (b) Micrograph

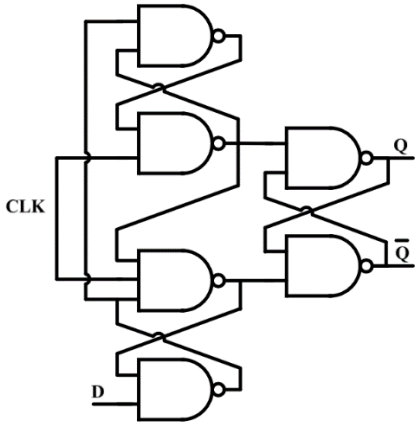



(a)

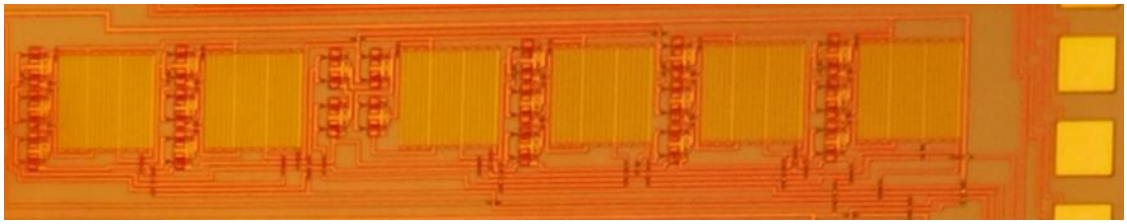


(b)

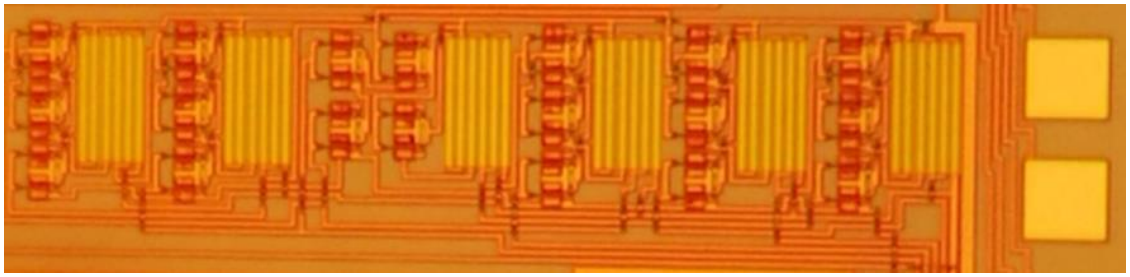
Figure 19: XOR+XNOR: (a) Schematic, and (b) Micrograph




(a)

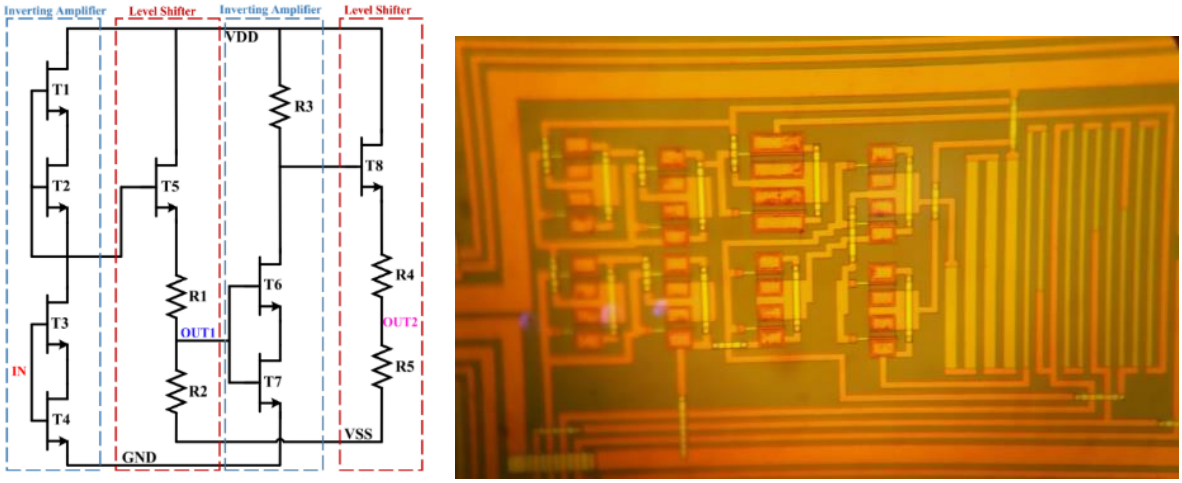


(b)



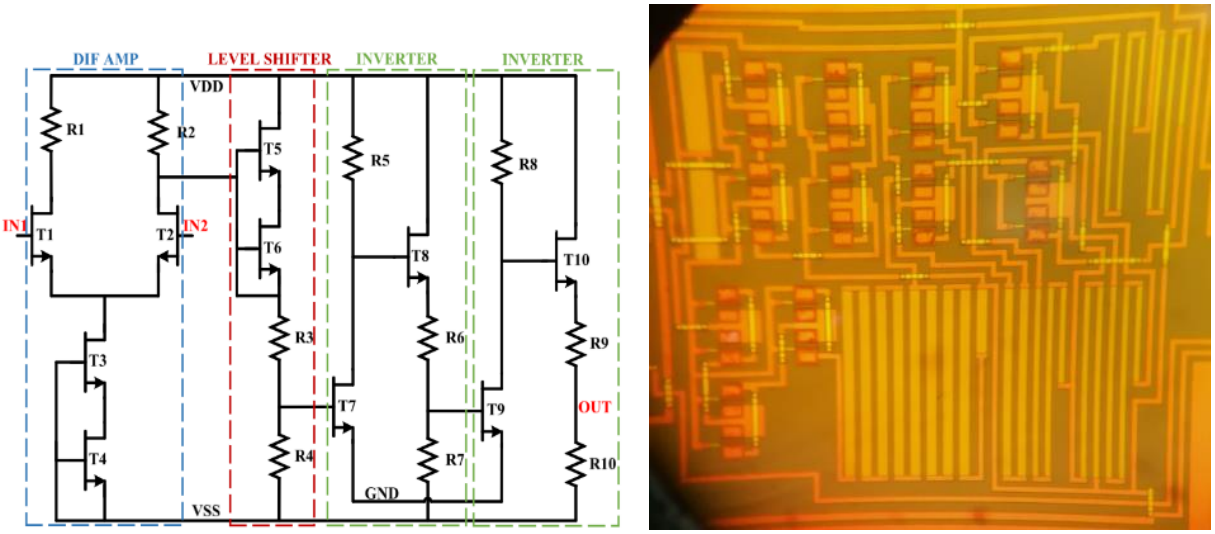
(c)

Figure 20: D-FlipFlop: (a) Schematic, (b) Micrograph of DFF1, and (c) Micrograph of DFF2



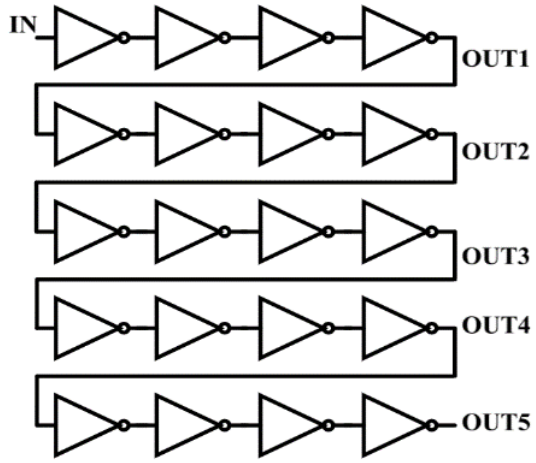

(a) (b)

Figure 21: Amplifier: (a) Schematic, and (b) Micrograph

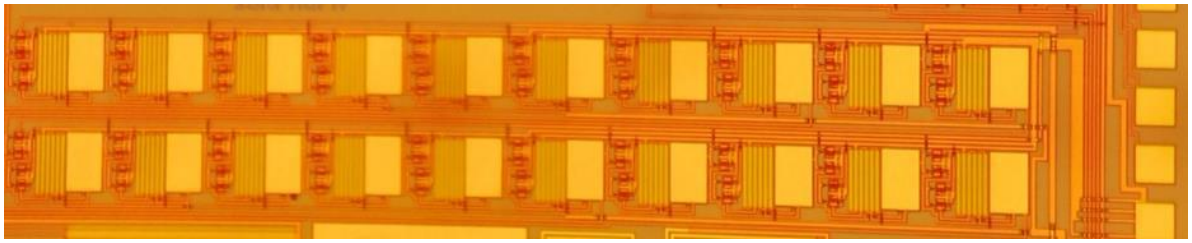



(a) (b)

Figure 22: Comparator: (a) Schematic, and (b) Micrograph

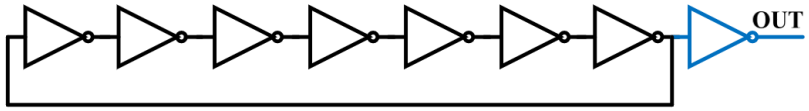



(a)

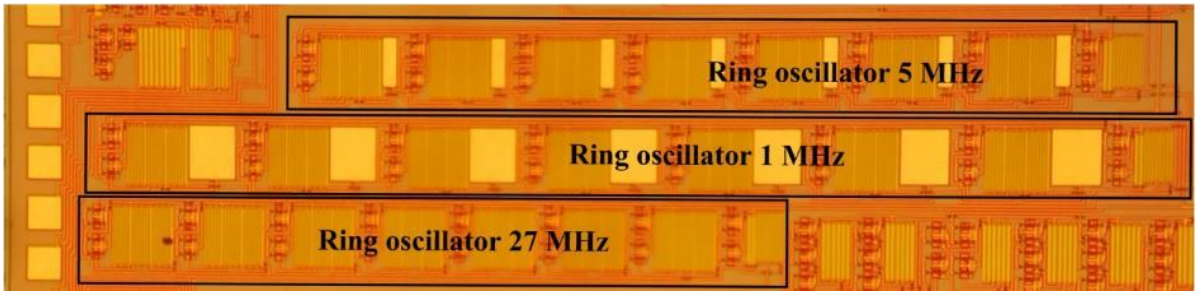


(b)

Figure 23: Delay: (a) Schematic, and (b) Micrograph




(a)




(b)

Figure 24: Ring oscillator: (a) Schematic, and (b) Micrograph

# APPENDIX B– CHIP 2

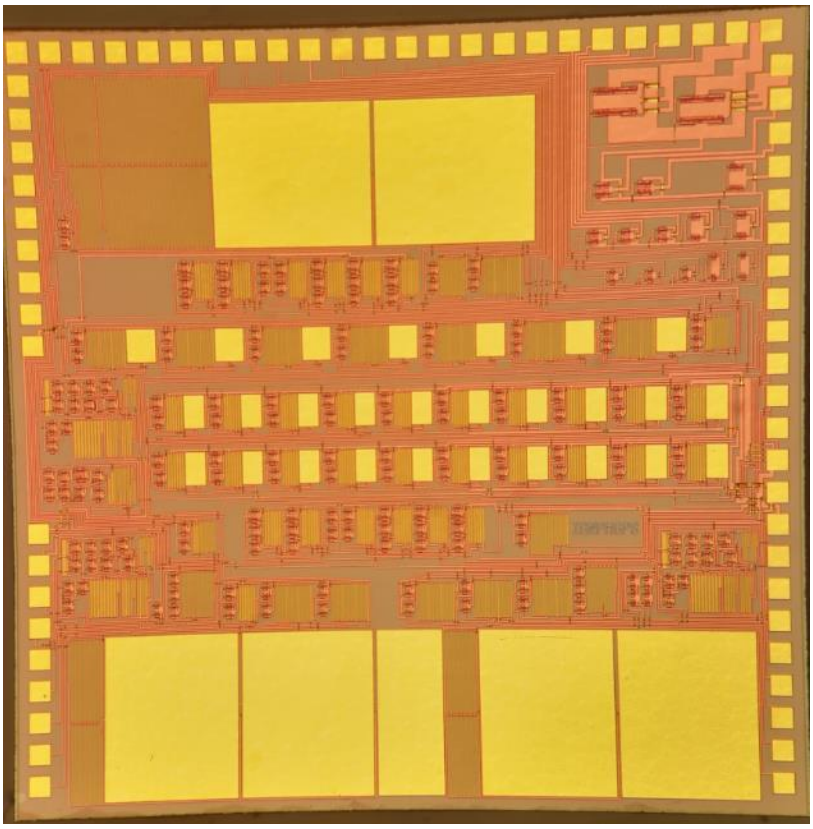


Figure 1: Micrograph of fabricated chip 2 (4 mm x 4 mm)

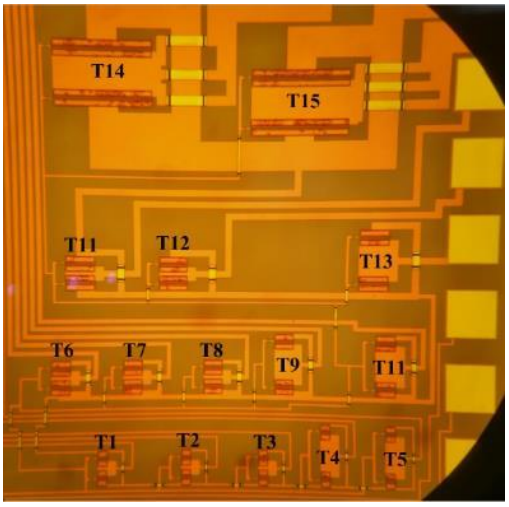



Figure 2. Micrograph of fabricated GaN devices.

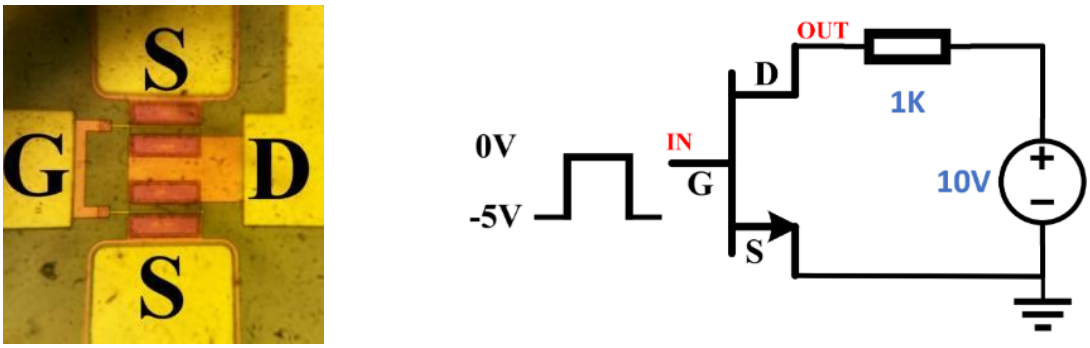
Table 1: Implemented GaN500 devices

| Transistor | W (µm) | S (µm) |
|---|---|---|
| **T1, T2, T3** | 20 | 43 |
| **T4, T5** | 20 | 100 |
| **T6, T7, T8** | 40 | 43 |
| **T9, T10** | 40 | 100 |
| **T11, T12** | 60 | 43 |
| **T13** | 60 | 100 |
| **T14, T15** | 200 | 100 |

Table 2: Blocks of chip 2 and corresponding current and power consumption (simulation)

| Block | IDD (mA) | IGND (mA) | ISS (mA) | POWER (mW) |
|---|---|---|---|---|
| **Modulator** | 86 | 48 | 38 | 1700 |
| **Digital Demodulator** | 160 | 60 | 100 | 3640 |
| **FBR Demodulator** | 35 | 5 | 30 | 910 |
| **HBR Demodulator** | 45 | 15 | 30 | 1050 |

*NA: The circuit doesn't need VSS power supply (only VDD and GND)




(a) (b)

Figure 3 : (a) Micrograph of a single GaN500 transistor and (b) Testing setup of transistors.

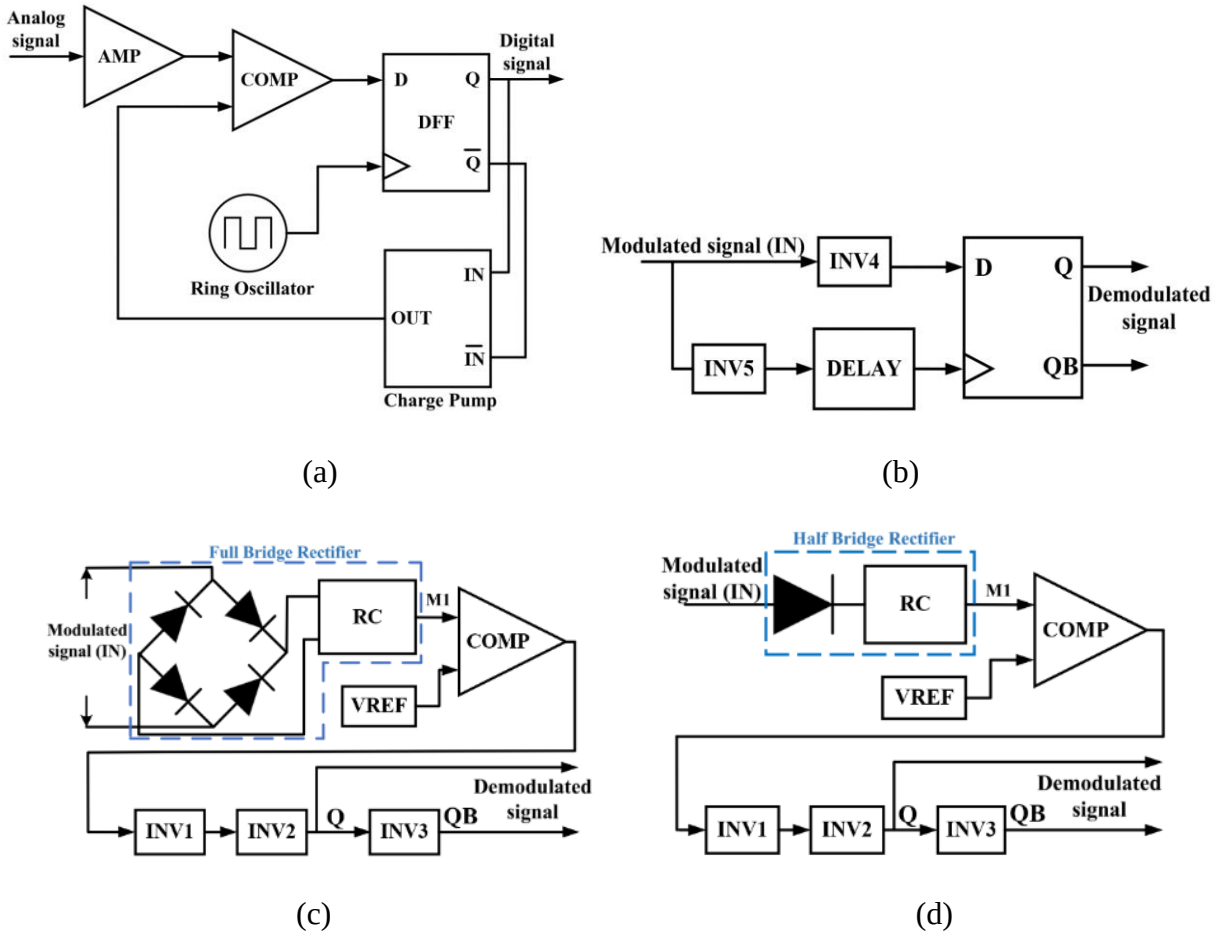



Figure 4: Block diagram of designed systems: (a) Modulator, (b) Digital demodulator, (c) FBR Demodulator, and (d) HBR Demodulator

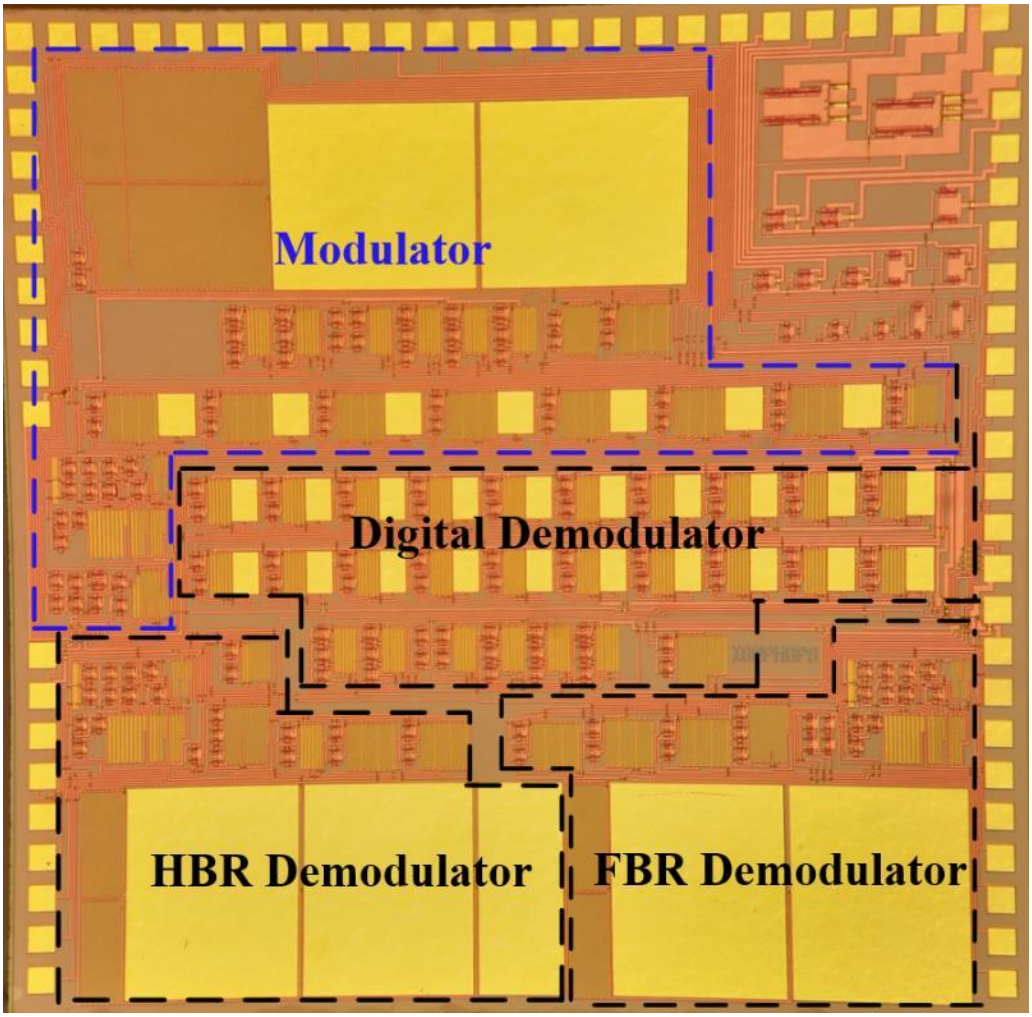



Figure 5: Micrograph of implemented systems (4 mm x 4 mm)