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EXPLORATION OF NONLINEAR DEVICES AND NONLINEAR TRANSMISSION LINE
TECHNIQUES FOR MICROWAVES APPLICATIONS

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en vue de l'obtention du diplôme de : Philosophiae Doctor

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DEDICATION

To my parents and sisters

To my wife Xian Liu

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During my Ph.D. study, I co-founded a non-for-profit organization, called Research & Development Frontiers Institute, which aims to build the youth generation high-tech talent ecosystem. The platform is helping hundreds and thousands of researchers and entrepreneurs. Thanks for the effort of my partners and our team, we already gained considerable achievements, which makes my research career more colorful.

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RÉSUMÉ

Les systèmes de communication modernes dépendent fortement des circuits non linéaires, tels que les amplificateurs de puissance (PA), les mélangeurs, les multiplicateurs, les oscillateurs, les commutateurs, etc., qui sont construits à partir de composants non linéaires passifs (comme des diodes) ou actifs (par exemple des transistors). Cette thèse étudie les dispositifs non linéaires passifs traditionnels et émergents, ainsi que les techniques de lignes de transmission non linéaires (NLTL). Plusieurs de leurs applications micro-ondes ont également été étudiées, y compris la récupération d'énergie sans fil, la synthèse d'impédance électronique et l'adaptation d'impédance bidimensionnelle (inductive et capacitive).

Dans le chapitre 1, sont d'abord étudiés les dispositifs non linéaires traditionnels résistifs, capacitifs et inductifs. Les dispositifs non linéaires émergents, y compris les dispositifs MEMS et la spindiode, sont ensuite explorés. La construction physique de base, les principes de fonctionnement, ainsi que les caractéristiques et applications pour divers types de dispositifs non linéaires sont expliqués et comparés. Les lignes de transmission non-linéaires (NLTL) traditionnelles utilisant des dispositifs non linéaires capacitifs (varactor, BST etc.) ou inductifs (ferrite saturée), et la technique hybride NLTL émergente utilisant à la fois des dispositifs non linéaires capacitifs et inductifs sont également étudiées.

Le chapitre 2 examine les techniques de conversion d'énergie micro-ondes à courant-continu de faible puissance à la fine pointe de la technologie. Une image complète de l'état de l'art sur cet aspect est donnée graphiquement. Elle compare différentes technologies telles que le transistor, la diode et les technologies CMOS. Depuis le tout début des techniques intégrées RF et micro-ondes et de la récupération d'énergie, les diodes Schottky ont été le plus souvent utilisées dans les circuits de mélange et de redressement. Cependant, dans des applications spécifiques de récupération d'énergie, la technique des diodes Schottky ne parvient pas à fournir une efficacité satisfaisante de conversion RF-dc. Suite aux limitations mises en évidence des dispositifs actuels, ce travail introduit, pour la première fois, un composant non linéaire pour une redressement de faible puissance, basé sur une découverte récente en spintronique, à savoir, la jonction tunnel magnétique, parfois appelée spindiode. Un modèle équivalent de spindiode est développé pour décrire le comportement en fréquence. Des études paramétriques complètes montrent que la capacité d'interface, plutôt que la capacité géométrique, joue un rôle clé dans son efficacité aux

hyperfréquences. L'ingénierie de la résistance d'interface est proposée comme une solution pour améliorer les pertes dues aux composants parasites, ainsi que la fréquence de fonctionnement de la spindiode. En plus d'une analyse du rôle de la non-linéarité et de la résistance en absence de polarisation dans le processus de redressement de la spindiode, le travail explique comment la spindiode pourrait améliorer le rendement de redressement même à très faible puissance et comment cette technique changerait les paradigmes de conception des dispositifs et circuits à diodes.

Au chapitre 3, un syntoniseur d'impédance électronique utilisant la résistance négative des diodes à effet tunnel est proposé. Outre le fait qu'il s'agisse d'une solution intéressante pour synthétiser l'impédance avec un coefficient de réflexion supérieur à un, ce schéma s'avère plus simple et consomme moins de puissance que les techniques de l'état de l'art. La topologie globale du circuit comprend deux parties, à savoir un bloc d'impédance comprenant une diode PIN combiné avec une diode à effet tunnel pour générer un ensemble de points d'impédance, et un déphaseur à 360° basé sur une géométrie de ligne de transmission non linéaire (NLTL) pour faire tourner l'ensemble des points d'impédance autour du diagramme de Smith de 1.5 à 5 GHz. La puissance de fonctionnement du syntoniseur électronique est inférieure à -25 dBm, limitée par la diode à effet tunnel. Dans le cas le plus défavorable, la consommation d'énergie maximale du syntoniseur électronique est inférieure à 3 mW, ce qui signifie qu'il pourrait fonctionner avec une pile. Un tel accordeur électronique serait utile pour le développement de systèmes de caractérisation du bruit sur gaufre.

Dans le chapitre 4, nous proposons et présentons tout d'abord une procédure de conception analytique pour le synthétiseur à impédance électronique distribuée (EIS). Bénéficiant de caractéristiques avantageuses tels qu'un réglage rapide, un faible encombrement et une intégration facile, l'EIS a été développé pour les systèmes de caractérisation load-pull sur gaufre, les réseaux accordables (TMN), les appareils et systèmes reconfigurables, etc. Les conceptions précédentes de l'EIS étaient principalement basées sur des données empiriques plutôt que sur des solutions analytiques. Dans ce travail, la méthode d'optimisation d'essaim de particules (PSO) est également introduite pour optimiser l'EIS non uniformément distribué que nous proposons et qui comprend un circuit de réglage et un circuit non uniformément distribué. Les résultats expérimentaux démontrent que la structure non uniformément distribuée proposée permet non seulement d'améliorer la couverture de l'abaque de Smith, mais aussi de réduire sa taille (par rapport à une structure uniforme). L'EIS non uniforme fabriqué fonctionne de 0.8 à 2.5 GHz et présente un bon

accord entre la théorie et la mesure. En outre, un ensemble complet de figures de mérite est présenté pour évaluer l'EIS fabriqué, parmi lesquelles une théorie de distribution de tension qui est développée pour l'EIS distribué et fournit un moyen de comprendre et prédire la tenue en puissance et la non-linéarité de EIS au bord de sa région linéaire.

Dans le chapitre 5, un circuit d'accord bidimensionnel basé sur une technique hybride de ligne de transmission non linéaire NLTL est analysé dans les domaines temporel et fréquentiel. Les paramètres de la permittivité et perméabilité effective sont extraits des S-paramètres de la structure périodique. L'impédance caractéristique ainsi que la vitesse de phase de la ligne de transmission non linéaire NLTL sont étudiées théoriquement en accordant à la fois la permittivité effective et la perméabilité. La théorie sera ensuite validée par des expériences et des simulations pour les matériaux non-magnétiques, NLTL avec varactors ainsi que la ligne microruban à base de ferrite. Enfin, les applications en mode petit et grand signaux des circuits d'accord bidimensionnel sont discutés.

ABSTRACT

Modern communication systems are heavily dependent on nonlinear circuits, such as PA, mixer, multiplier, oscillator, switch, etc., the core of which are either passive nonlinear elements and devices (e.g. diodes) or active nonlinear components and devices (e.g. transistors). This thesis aims at investigating a number of traditional and emerging passive nonlinear devices and nonlinear transmission line (NLTL) techniques, and developing four of their microwave applications such as wireless power harvesting, electronic impedance synthesizer, and two-dimensional tuning circuit.

In Chapter 1, traditional nonlinear devices in terms of the categories of resistive, capacitive and inductive are firstly investigated. Emerging nonlinear devices including microelectromechanical system (MEMS) devices and spindiodes are then explored. The basic physical constructions, operation principles, and characteristics as well as applications of various types of nonlinear devices are explained and compared. Traditional NLTL techniques make use of either capacitive nonlinear devices (varactor, BST etc.) or inductive nonlinear devices (saturated ferrite), and emerging hybrid NLTL techniques are also studied through the deployment of both nonlinear capacitive and inductive devices.

Chapter 2 examines the state-of-the-art low-power microwave-to-dc energy conversion techniques. A comprehensive picture of the state-of-the-art on this aspect is given graphically, which compares different technologies such as transistor, diode, and CMOS schemes. Since the very beginning of RF and microwave integrated techniques and energy harvesting, Schottky diodes as the undisputable dominant choice, have been widely used in mixing and rectifying circuits. However, in specific µW power-harvesting applications, the Schottky diode technique seemingly fails to provide a satisfactory RF–dc conversion. Subsequent to the highlighted limitations of current devices, this work introduces, for the first time, a nonlinear component for low-power rectification based on a recent discovery in spintronics, namely, the Magnetic Tunnel Junction, also called spindiode. An equivalent model of spindiode is developed to describe the frequency behavior. Full parametric studies show that the interfacial capacitance, rather than the geometric capacitance, as it is usually the case for diode, plays a crucial role in the drop of efficiency in microwave frequency applications. Interfacial resistance engineering is proposed as a solution to improve the parasitic factor, as well as the operation frequency of spindiode. Along with an analysis of the role of nonlinearity and zero bias resistance in the rectification process of the spindiode, it is shown how

the spindiode could enhance the rectification efficiency even at a very low-power level and how this technique would shift the design paradigms of diode-based devices and circuits.

In Chapter 3, an electronic impedance tuner using the negative resistance of a tunneling diode is proposed. Aside from the fact that it is an interesting solution to synthesize impedance with reflection coefficient larger than one, this scheme is proven to be simpler and consume less power than the state-of-the-art techniques. The overall circuit topology consists of two parts, namely impedance tuning circuit including a hybrid block of PIN and tunneling diode for generating a set of impedance points, and wideband nonlinear transmission line (NLTL)-based 360º phase shifter for rotating the set of impedance points around the Smith chart from 1.5 to 5 GHz. The operating power of the electronic tuner is below -25 dBm, which is limited by the tunneling diode negative slope range. The worse-case maximum power consumption of the electronic tuner is as low as 3 mW, which would allow battery-powered operation. Such an electronic tuner should be useful for the development of on-wafer noise characterization systems.

In Chapter 4, we propose and present, first of all, a semi-closed form design procedure for the distributed electronic impedance synthesizer (EIS). Benefiting from advantageous features of fast tuning, small size and easy integration, the EIS has been developed for on-wafer load-pull characterization systems, tunable matching networks (TMN), reconfigurable devices and systems etc. However, the previous designs of the EIS were mostly based on empirical data instead of closed-form design. Moreover, incomplete figures of merit are usually utilized to optimize and evaluate the EIS. In this work, a particle swarm optimization (PSO) method is introduced to optimize the proposed non-uniformly distributed EIS, which comprises an adjusting circuit and a non-uniformly distributed circuit. Experimental results demonstrate that the proposed non-uniformly distributed structure can not only improve the Smith chart coverage but also reduce the size, as compared to the uniform counterpart. The fabricated non-uniform EIS operating from 0.8 to 2.5 GHz, exhibits a good agreement between theory and measurement. Furthermore, the most comprehensive figures of merit are presented to evaluate the fabricated EIS, among which a voltage distribution theory is developed for the distributed EIS, it provides a way of understanding and predicting the power-handling capacity and nonlinearity of EIS from its linear region.

In Chapter 5, two-dimensional tuning circuit based on hybrid NLTL technique is analyzed in both time domain and frequency domain. The parameter extraction method of effective permittivity and

permeability is developed based on the S-parameters analysis. The characteristics of the impedance and phase velocity of ferrite-based NLTL are studied theoretically by tuning both the effective permittivity and permeability. The theory is then validated by experiments and simulations for non-magnetic material, namely NLTL with varactors as well as ferrite-based microstrip line. Finally, the small signal and large signal applications of two-dimensional tuning circuits are discussed.

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LIST OF SYMBOLS AND ABBREVIATIONS

ADS	Advanced Design System
AP	Anti-parallel
BST	Barium strontium titanate
C(V)	Capacitance-voltage
CMOS	Complementary Metal-Oxide-Semiconductor Transistor
CPW	Coplanar waveguide
CW	Continuous wave
dc	Direct current
DUT	Device under test
EIS	Electronic impedance synthesizer
FCC	Federal Communications Commission
FMR	Ferromagnetic resonance
FOM	Figures of merit
GaAs	Gallium arsenide
GMR	Giant magnetoresistance
GSG	Ground-Signal-Ground
GPIB	General Purpose Interface Bus
HB	Harmonic Balance
HFSS	High Frequency Structural Simulator
IIP3	Input third-order intercept point
IMD	Intermodulation Distortion
IMPATT	IMPact Avalanche Transit Time
IP3	Third-order intercept point
I(V)	Current-voltage
LC	Inductance-capacitance
MEMS	Microelectromechanical Systems
MIM	Metal-Insulator-Metal

MMIC	Monolithic microwave integrated circuit
MPH	Microwave power harvesting
MPT	Microwave power transfer
MR	Magnetoresistance
MRAM	Magnetic random access memory
MTJ	Magnetic tunnel junction
NLTL	Nonlinear transmission line
NVNA	Nonlinear Vector Network Analyser
P	Parallel
PA	Power amplifier
PCB	Printed circuit board
PIN	P-Intrinsic-N
PSO	Particle Swarm Optimization
RF	Radio frequency
RTD	Resonant tunneling diode
SDD	Symbolically Defined Devices
SRD	Step recovery diode
ST-FMR	Spin-torque-driven ferromagnetic resonance
TED	Transferred electron device
TMN	Tunable matching networks
TMR	Tunnel magnetoresistance
VNA	Vector Network Analyser
VSWR	Voltage standing wave ratio
WPT	Wireless power transfer
YIG	Yttrium Iron Garnet
ZBR	Zero-bias resistance

CHAPTER 1   INTRODUCTION

Modern wireless and communication systems are heavily dependent on nonlinear circuits such as power amplifier (PA), mixer, multiplier, oscillator, switch, etc., the core of which are passive nonlinear devices (e.g. diodes) or active nonlinear devices (e.g. transistors). The term "nonlinear" intuitively means that the output signals and input signals are not in a linear relationship, it essentially indicates that one parameter is nonlinear with voltage or current. It should be noted that it is different from the nonlinearity of frequency responses, for instance, dispersion.

In this work, we focus on passive nonlinear devices. One purpose of this thesis is to provide a way for the readers to understand and choose proper nonlinear devices in accordance with different applications. Traditional nonlinear devices in terms of the categories of resistive, capacitive and inductive are firstly investigated in the following.

As listed in Table 1.1, the resistive devices include conventional PN junction diode, Point-Contact diode, Schottky diode, PIN diode, Step-Recovery diode (SRD), Metal-Insulator-Metal (MIM) diode, Tunnel diode (Esaki diode), Backward diode, Resonant Tunneling diode (RTD), Gunn diode, IMPATT diode, etc. [1, 2], among which the last five diodes present a differential negative resistance region in their current-voltage (I(V)) characteristics. The basic physical construction, operation principles as well as characteristics and applications for various types of diode are explained and compared.

The capacitive nonlinear devices include semiconductor and ferroelectric ceramics, whereas the inductive nonlinear devices usually use ferrite and other magnetic materials. Emerging nonlinear devices includes microelectromechanical system (MEMS) devices and spindiodes.

Nonlinear transmission line (NLTL) is a transmission line periodically loaded with nonlinear devices. Traditional NLTL technique uses either capacitive nonlinear devices (varactor, BST, PZT etc.) or inductive nonlinear devices (saturated ferrite). Emerging hybrid NLTL technique uses both nonlinear capacitive and inductive devices.

Table 1.1: Comparison of traditional and emerging passive nonlinear devices.

Categary	Nonlinear Type	Nonlinear Device	Specialty	Applications
traditional nonlinear devices	resistive	PN junction diode		detector, rectifier, modulator, switch, demoudulator circuit, etc.
		point-contact diode		mixer, detector, etc
		Schottky diode		detector, mixer, rectifier, etc.
		PIN diode		switch, attenuator, phase shifter, limiter, modulator, etc.
		step-recovery diode		short pulse generator, frequency multiplier, comb generator, etc.
		MIM diode		Mixer, rectifier, etc.
		tunnel diode	negative resistance	oscillator, amplifier, mixer, detector, etc.
		backward diode		detector, rectfier, switch, etc.
		RTD		Oscillator, switch, etc.
		Gunn diode		Oscillator, amplifier, radar speed gun, etc.
		IMPATT diode		power generation, etc.
	capacitive	semiconductor varactor		VCO, parametric amplifier, harmonic generator, frequency multipliers, mixer, microwave signal synthesizers, tunable circuit, etc.
		BST		phase shifter, capacitor, DRAM, etc.
		PZT		
	inductive	ferrite		tunable filter, oscillator, amplifier, circuilator, isolators, phase shifter, bandstop filter, magnet recording, etc.
emerging nonlinear devices		MEMS devices		phase shifters, tunable filters, impedance tuners, oscillators, mixer, switch, etc.
		MTJ		MRAM, oscillator, rectifier, etc.

1.1 Traditional RF and microwave nonlinear devices

1.1.1 Resistive nonlinear devices

1.1.1.1 Conventional PN junction diode

Construction

The conventional PN junction diode is the most basic and simplest solid state electronic device. It is constructed by the combination of P-type and N-type of semiconductors [1, 2]. By doping an

intrinsic semiconductor with acceptor impurities, a P-type semiconductor is formed, in which holes are the majority carriers while electrons are the minority carriers. The term P-type denotes the positive charge of the hole. As opposed to P-type semiconductors, N-type semiconductors are formed by doping an intrinsic semiconductor with donor impurities, in which free electrons have a more massive concentration than holes. The term N-type refers to the negative charge of the electron.
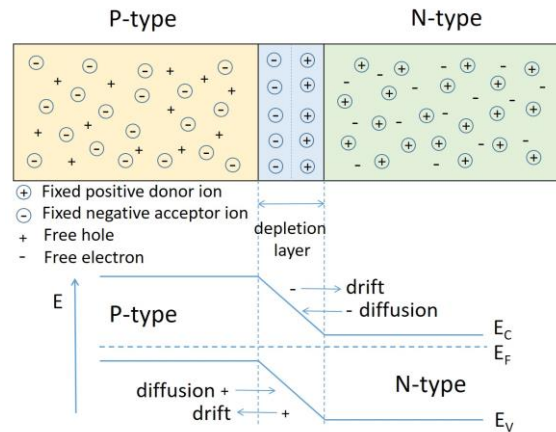
Figure 1.1: Energy band diagram of PN junction diode.

Operation principle and characteristics

As depicted in Fig. 1.1, a PN junction will be formed when a P-type semiconductor is placed in contact with a N-type semiconductor. The density gradient at both sides of the PN junction results in the free holes in P-type side that diffuse across the interface and recombine when they reach N-type side, and leave behind the fixed negatively charged acceptor ions. Similarly, it also results in the free electrons that diffuse from N-type side to P-type side, and leave behind the fixed positively charged donor ions. The negatively and positively charged ions will create an electrostatic potential barrier, which will prevent the diffusion of free charge carriers. A depletion layer will be formed when an equilibrium state will be reached, and no free charge carriers will exist in this layer. The extra energy that is required to overcome the barrier is called the barrier potential, which depends on the semiconductor material, doping level as well as temperature, and is about 0.7 V for silicon and 0.3 V for germanium.

Opposite to the diffusion current that is caused by the majority carriers, the drift current is due to the minority carriers that are moving across the junction and accelerated by the barrier potential. In

the unbiased condition, the net current is zero since the drift current and diffusion current are equal to each other.

Ohmic effects

In the forward bias condition, the P-type and N-type semiconductors are connected with the positive and negative electrode of the voltage source, respectively. The external voltage can push the majority carriers (holes) in the P-type side and the majority carriers (electrons) in the N-type side toward and then neutralize the depletion layer so that the width of the depletion layer is reduced. There is almost no current when the external voltage is less than the barrier potential since the free electrons and holes cannot overcome the barrier. As shown in the I(V) characteristic of PN junction diode in Fig. 1.2, with the increases of the forward bias, the depletion zone decreases, eventually results in an electrical resistance reduction. The relationship of IV characteristic of PN junction diode can be expressed as [2]

$$I = I_S(e^{\frac{q(V-IR_s)}{nKT}} - 1) \tag{1.1}$$

where I_s is the reverse saturation current, q is the electron charge, V is the external bias, R_s is the series resistance of PN junction, n is ideality factor, K is Boltzmann constant, and T is absolute temperature.
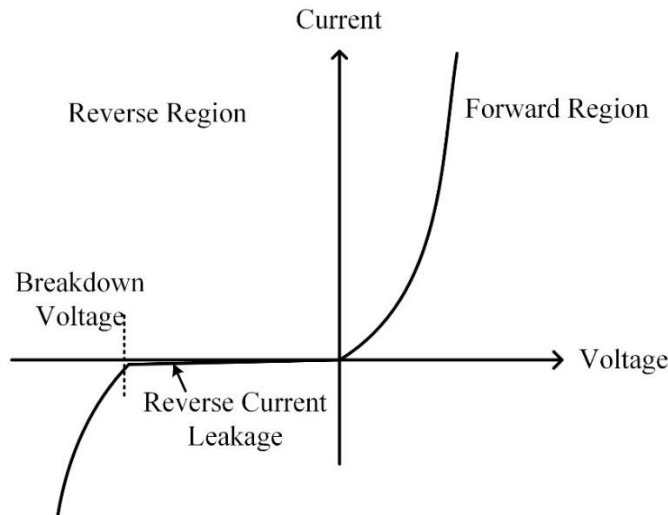
Figure 1.2: IV characteristic of conventional PN junction diode.

In the reverse bias condition, the P-type and N-type semiconductors are connected with the negative and positive electrode of the voltage source, respectively. The reverse bias pulls the holes in the P-type side and electrons in the N-type side away from the junction, which increases the width of the depletion layer, so that results in a high resistance allowing a small current across the junction. As shown in Fig. 1.2, when the reverse bias increases beyond a critical level, the depletion region breaks down and current begins to flow, and it is called the avalanche effect.

Junction capacitance

Two types of capacitance mechanisms are involved in PN junction, namely depletion capacitance and diffusion capacitance, respectively, as shown in the capacitance-voltage (C(V)) characteristic of a PN junction diode in Fig. 1.3. The depletion capacitance is caused by the impurity atoms, and it dominates under the reverse bias condition. It can be calculated as [2]

$$C_j = \frac{C_0}{(1 - \frac{V}{V_0})^\gamma}$$

(1.2)

where C_0 is the zero-bias capacitance, V is the reverse bias voltage, V_0 is built-in potential, γ is a constant, it is 1/2 for an abrupt junction, 1/3 for a graded junction, and 1 to 2 for a hyperabrupt junction. The diffusion capacitance is caused by the injected minority charge, and it dominates under the forward bias condition. It is proportional to the minority carrier lifetime, therefore related to the switching characteristic of the PN junction diode.
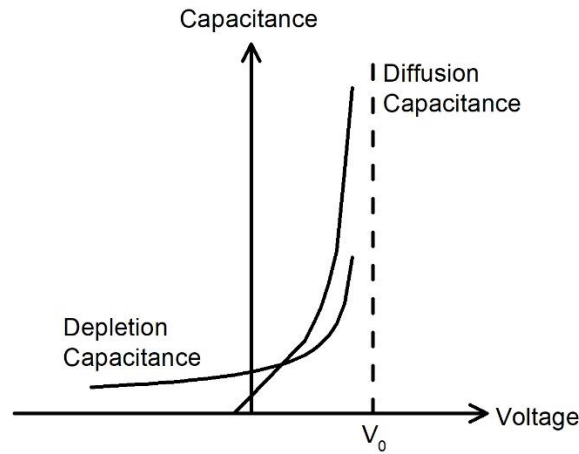
Figure 1.3: Junction capacitance-voltage characteristic of PN junction diode.

Application

The PN junction diodes can be found in the applications of detector, rectifier, modulator, switch, demodulation circuit, clamping circuit, clipping circuit, clamping circuit, etc. [2]

1.1.1.2 Point-Contact diode

Construction

Similar to conventional PN junction, Point-Contact diode is also one of the most basic forms of diodes. It has been developed during the Second World War, and is often used as mixer or detector. As depicted in Fig. 1.4, it is made by a cat whisker metal wire placed on a piece of N-type semiconductor [1, 2]. During the formation of a Point-Contact diode, a relatively high current will pass through the cat whisker wire to the semiconductor, part of the metal will migrate into the semiconductor, a small P-type region will be formed in the vicinity of the point contact, thus a PN junction is formed which behaves the same as a conventional PN junction.
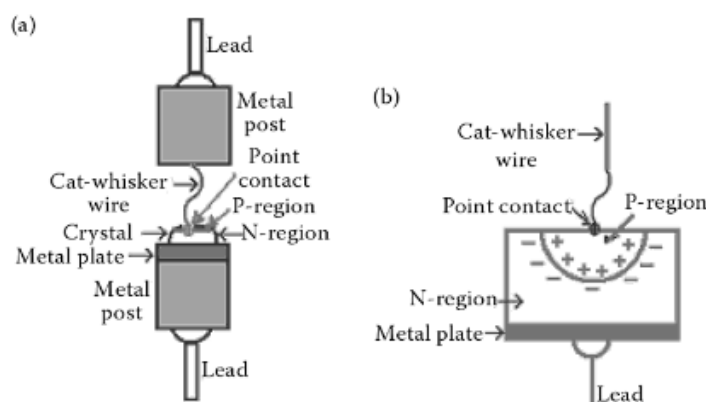
Figure 1.4: Point-Contact diode. (a) Construction and constituents and (b) p-region around point contact [1].

Operation principle

The operation mechanism of Point-Contact diode is quite similar to a conventional PN junction diode. However, the characteristics are different under forward and reverse bias conditions, mainly because of the small contact between the cat whisker and the semiconductor. The resistance of Point-Contact diode in the forward bias condition is larger than the conventional PN junction diode, while the capacitance in the reverse bias condition is smaller. The very low junction capacitance

leads to a better switching ability than a conventional PN diode, thus ideal for many RF applications. However, the small junction also limits the power handling of a high current [1].

Applications

With the advantages of fast switching and the small junction capacitance due to small junction area, Point-Contact diode is suitable for high-frequency applications, such as mixer, detector, etc. [1].

1.1.1.3 Schottky diode

Construction

The Schottky diode can be considered as a variation of point-contact diode, it can be manufactured in different forms, in which the simplest form is a point-contact diode (Fig. 1.5(a)). As shown in Fig. 1.5(b), the metal-semiconductor junction in the deposited metal Schottky diode is a surface rather than a point contact [1]. A large contact area between the metal and the semiconductor enables a low forward resistance and low capacitance.
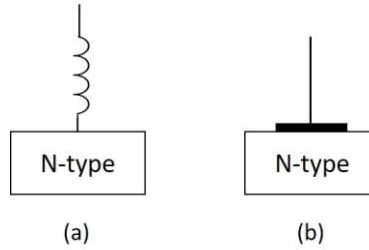
Figure 1.5: Schottky diode. (a) Point-contact type, (b) deposited metal type [1].

Operation principle and chracteristics
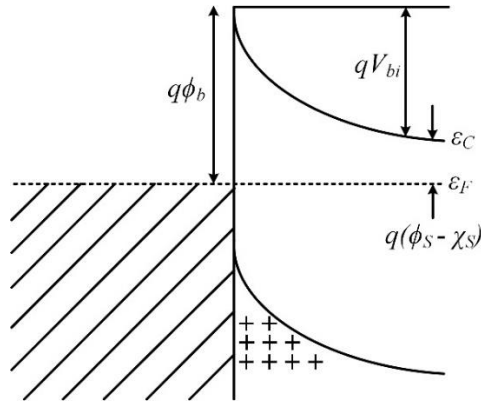
Figure 1.6: Energy band diagram for ideal Schottky barrier junction [2].

In a metal, the energy gap between the valence band and conduction band is too small, so that it is conductive. By contrast, no free electron exists at the Fermi level in the semiconductor because the Fermi level lies within the energy gap. When a metal contacts with a semiconductor, a Schottky junction is formed, and the Fermi levels must align, the energy band diagrams for the Schottky junction is illustrated in Fig. 1.6 [2]. Since the work function of the metal is greater than that of the semiconductor, an electrostatic barrier is formed, which enables a Schottky diode to have the rectifying properties.

The current-voltage characteristics of a Schottky diode is similar to that of a PN junction diode. However, there are still some differences: by using the same semiconductor material, the reverse leakage current of a Schottky diode is higher, and the reverse breakdown voltage is lower than a PN junction diode. While at a specific forward current, the forward voltage for a Schottky diode is lower than a PN junction diode.

Equivalent circuit model

The equivalent circuit model of PN junction diode is shown in Fig. 1.7 [2, 3]. C_j and R_j represent the nonlinear junction capacitance and junction resistance, respectively. R_s denotes the total series resistance that includes the resistance of the epitaxial layer and the substrate, L_s denotes the series inductance, and C_p represents the packaging capacitance.
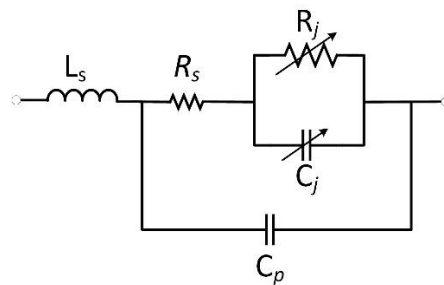
Figure 1.7: Equivalent circuit of Schottky diode.

Applications

Similar to the point-contact diode, the Schottky diodes can be used in applications requiring high switching speed, high power and high frequency capacity. They have the following advantages [1]: (i) Low turn-on voltage due to the high current density, it is 0.2 - 0.3 V for a Silicon Schottky diode that is similar to a germanium PN junction diode. The less waste of energy makes them suitable for the applications that require high efficiency; (ii) High frequency capacity and fast recovery time

due to almost no minority carrier charge storage. Unlike the conventional PN junction diode that relies on the recombination of holes or electrons when they move to the other side of semiconductor, Schottky diode is a majority carrier device; (iii) Low noise generation; (iv) Low forward resistance; (v) Low junction capacitance due to the small contact area. The reduction of RC time constant makes them faster than the conventional PN junction diodes, which enables them suitable for many applications requires fast speed. The characteristics of low parasitic parameters and fast recovery time make them suitable for high frequency applications.

1.1.1.4 PIN diode

Construction

PIN stands for P-Intrinsic-N, it is a PN junction device. Located between the P-type and N-type semiconductors, a minimally doped thicker layer or an intrinsic semiconductor is inserted, so that a high resistivity is presented. PIN diodes are usually constructed on Silicon due to its better power-handling capability, however, GaAs can be chosen if higher speed is required [1].

Operation principle and characteristics

When a PIN diode is forward biased, holes and electrons are injected from P-type and N-type region into the intrinsic region (I-region), respectively. Instead of combining immediately, a finite quantity of charges will remain in the I-region. The quantity of charges relies on the recombination time or carrier-lifetime as well as the forward bias current. The thick intrinsic layer increases the transit time for electrons to cross the I-region, resulting in the accumulation of electrons in the I-region. PIN diode acts as a traditional rectifying device up to about 100 MHz, and beyond this frequency, the storage of charges in the I-region makes the diode act as a variable resistance[1].

When PIN diode is reverse biased, the reverse current flows until the I-region is depleted of charges. The switching time or recovery time is defined as the time required to remove the charges stored in the I-region due to the forward bias. When PIN diode is used as switch, the switching time can be understood as the time to switch from a low-impedance state (forward bias) to a high-impedance state (reverse bias) [1].
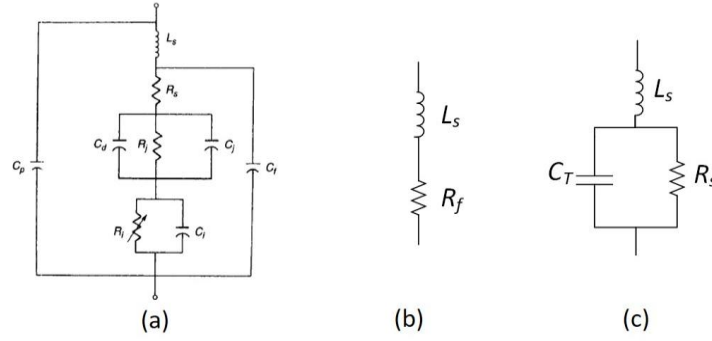
Figure 1.8: (a) Equivalent circuits of PIN diode; Simplified equivalent circuit (b) under forward bias and (c) under reverse bias [1, 2].

Equivalent circuit model

The equivalent circuit of PIN diode is described in Fig. 1.8(a) [2], it mainly consists of two sets of elements in series: the first part is similar to a PN junction, it includes diffusion capacitance C_d in parallel with junction resistance R_j and junction capacitance C_j; while the second part consists of the undepleted I-region resistance R_i and capacitance C_i. Besides the core parts, L_s denotes the lead inductance, R_s represents the resistance of the bulk semiconductor and the contacts, C_p denotes the packaging capacitance, C_f represents fringing capacitance of the structure which can be neglected as compared to other capacitances.

Although the model shown in Fig. 1.8(a) can describe the physical model, it is not practical in the circuit design. It can be simplified for both forward bias and reverse bias conditions. Under the forward bias condition, the diffusion capacitance C_d is large so that shorts out the junction parameters. The charge carriers will be injected into the I-region, the C_i will vanish so that only R_i left. The equivalent circuit for the forward bias condition is simplified as Fig. 1.8(b) [1, 2, 4, 5], Rt is the total RF resistance (R_s plus R_i), which is a current-controlled resistance.

Under the reverse bias condition, the diffusion capacitance C_d vanishes, and the junction resistance R_j becomes large, only C_j remains. The R_i-C_i part will vanish if the reverse bias is high enough to deplete the I-region. The equivalent circuit for a reverse bias condition will be simplified as Fig. 1.8(c) [1, 2, 4, 5].

Applications

The presence of the intrinsic layer provides two benefits for the reverse bias condition: high breakdown voltage so as to have high power handling capacity, small junction capacitance due to

the separation between P-type and N-type semiconductors. The benefits make PIN diode useful for high frequency and high power rectification application. Under the forward bias condition, the I-region is controlled by the amount of injected charge carriers, which makes the possibility to control the large RF signal with a small level of dc excitation. It is extensively used in the low loss and low distortion applications, for instance, RF switches, attenuators, phase shifters, limiters and amplitude modulator, etc. [1, 2].

1.1.1.5 Step-Recovery diode (SRD)

Construction

A SRD is usually constructed upon the PIN structure, although in principle it can be constructed on any diode structure. The difference with PIN diode is that the SRD is fabricated with gradually decreased doping level as the close of the junction, which results in fewer charge carriers stored in the I-region so as to have shorter switching time [1, 2]. This advantage makes SRD suitable for applications that require fast switching.

Operation principle and characteristics

The operation of a SRD relies on the charges storage and extraction characteristics in the semiconductor. As illustrated in Fig. 1.9, in the positive conduction region (forward bias), the SRD operates like a normal diode, the RF current will follow the RF voltage waveform, the charges will be stored in the I-region of the diode. In the negative portion of the RF voltage cycle (reverse bias), the charges start to extract from the I-region. Once the free charges are removed from the I-region, the RF current suddenly reduces to zero in a very short time. The rapid vanish of current in time domain stands for rich harmonics in frequency domain.
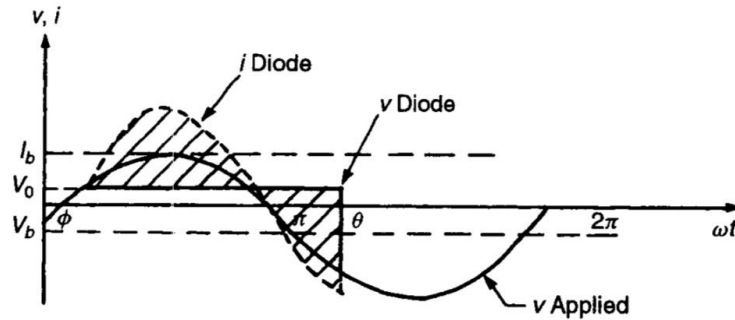
Figure 1.9: Diagram of current and voltage waveforms of SRD [2].
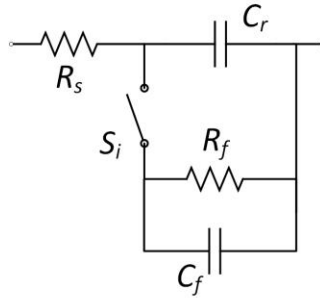
Figure 1.10: Equivalent circuit of SRD [2].

Equivalent circuit model

The equivalent circuit of the SRD can be modeled by combining the forward- and reverse-biased circuit with a switch, as shown in Fig. 1.10, in which the series resistance R_s denotes the voltage drop across the diode [2]. The switch is closed under the forward bias condition, the circuit consists of a relatively large diffusion capacitance C_f, accounting for the large charge storage in the I-region, in shunt with a resistance R_f. Under the reverse bias condition, the switch is still closed until all the charges are extracted from the diffusion capacitance C_f, the circuit also includes the depletion layer capacitance C_r.

Applications

Due to the fast switching times characteristic, the SRD is suitable for the applications of short pulse generator, high-efficiency high-order frequency multiplier, comb generator, etc. [1, 2].

1.1.1.6 Tunnel diode (Esaki diode)

Construction

Tunnel diode, also called Esaki diode, has a junction that enables tunneling transport, classically use P-type and N-type semiconductors. The semiconductors are heavily doped with impurity, resulting in a depletion layer thin enough for majority carriers to cross by tunneling [1]. Since it is the movement of majority carriers, the operation of tunnel diode is faster than conventional PN junction diode. Different from the conventional transit time concept, the time of tunneling is proportional to quantum transition probability.
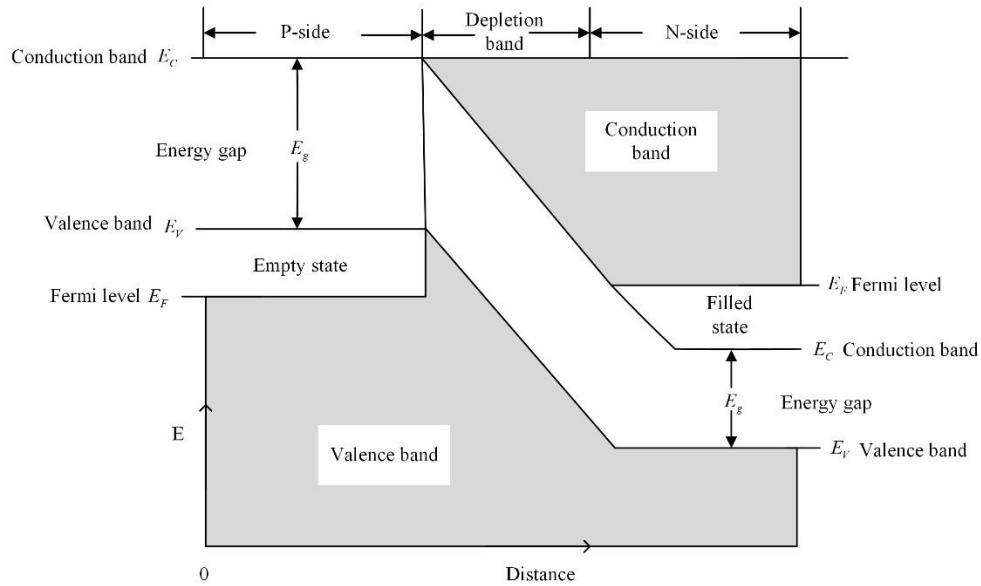
Figure 1.11: Energy bands of tunnel diode at zero-bias condition [1].

Operation principle and characteristics

Fig. 1.11 illustrates the energy bands of tunnel diode at the zero-bias condition [1]. Only when the filled state at N-side and empty state at P-side are aligned at the same level, tunneling will occur. The current-voltage characteristic of a tunnel diode is presented in Fig. 1.12. When the applied forward bias increases, electrons start to tunneling from N-side to P-side, because the filled state at N-side starts to align at the same level with an empty state at P-side. When they are aligned exactly, the maximum current will be reached, after that the current starts to decrease until a very low level. With the further increases of bias, ordinary injection current starts to increase exponentially, which is similar to a PN junction diode.
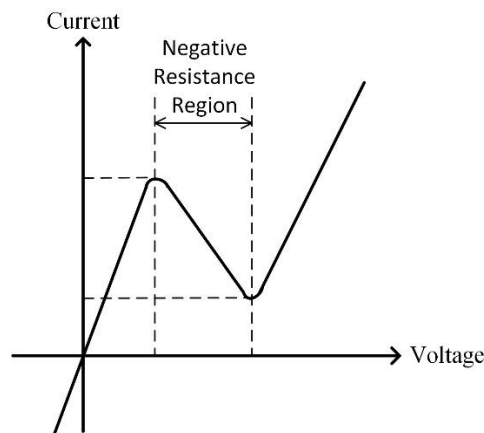
Figure 1.12: Current-voltage characteristic of tunnel diode.

Applications

Tunnel diode has advantages of high speed, low operation voltage, low noise generation, high peak current-to-valley current ratio, low cost and lightweight. It exhibits a negative resistance under the forward bias condition, thus can be used in microwave oscillators and amplifiers. It also can be used in microwave mixers, detectors, and binary memory.

1.1.1.7 Backward diode

The backward diode, is also a form of PN junction diode. The operation mechanism is similar to the tunnel diode, the difference is that backward diode operates by tunneling only under the reverse current condition. In the backward diode, doping level in one side of the junction is less than the other, the doping profile gives a freedom to modify some characteristics from the tunnel diode [6].

Operation principle and characteristics

Under the reverse bias, the tunneling effect of the backward diode is similar to the tunnel diode, while under the forward bias the tunneling effect reduces and it is similar to a conventional PN junction diode [6]. In other words, its name comes from the fact that the diode can be used backward.

As can be seen from Fig. 1.13, the forward IV curve is similar to a conventional PN junction diode. Zener breakdown starts at a low reverse bias voltage, the voltage remains relatively constant and is independent of the reverse current. It should be noted that the negative resistance region is not presented in the IV curve, because the tunneling phenomenon is only incipient.
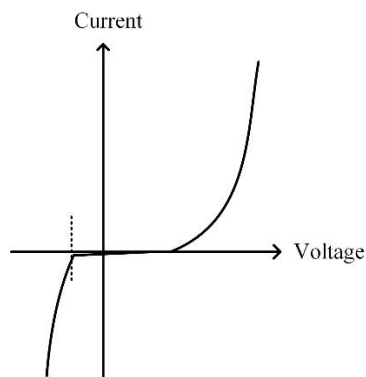
Figure 1.13: Current-voltage characteristic of backward diode.

Applications

The backward diode has a strong nonlinearity at a small signal region, and it does not have a charge storage effect so that it can be used as a detector and rectifier at high frequency (more than 40 GHz) with weak signals, and it also can be used for high speed switching applications [6].

1.1.1.8 Resonant tunneling diode (RTD)

Resonant Tunneling Diode (RTD) is a two-terminal quantum device, it consists of a quantum well locating between two quantum barriers. It works by the resonant tunneling effect so that negative differential resistance regions are often present in the current-voltage characteristics, which enables many high-speed applications. An RTD can be fabricated with a variety of semiconductor materials and different resonant tunneling structures [7, 8].

Operation principle and characteristics

Fig. 1.14 illustrates the operation mechanism of a double-barrier RTD [7, 8]. The charge carriers in the quantum well only can present at discrete energy states. As the bias of RTD increases, the first confined state is close to Fermi level, the current increases, as shown from point A to B in Fig. 1.14(d). As the bias further increases, the first confined state becomes lower than Fermi level and fall into the bandgap, the current decreases, as shown from point B to C in Fig. 1.14(d). When the second confined state is close to Fermi level, the current will increase again, as shown from point C to D in Fig. 1.14(d).
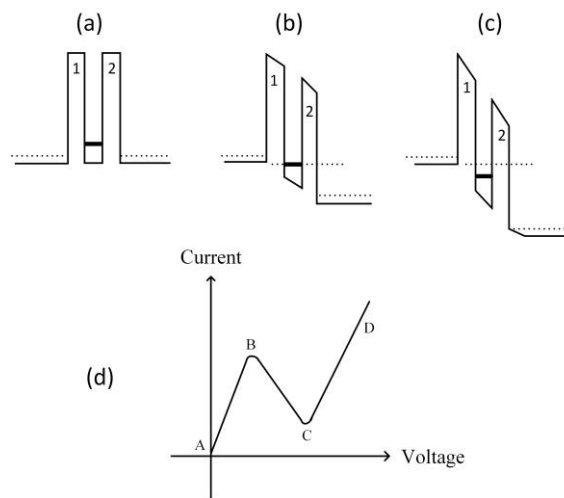
Figure 1.14: Operation mechanism of double-barrier RTD. Energy bands for three different bias (a)-(c); (d) IV curve of RTD.

Applications

Since the quantum tunneling effect through the thin barriers and quantum well is very fast, RTD is capable of enabling high-speed and high-frequency applications, such as oscillators and switching devices at terahertz frequencies [7, 8].

1.1.1.9 MIM Diode

Construction

Metal-Insulator-Metal (MIM) diode is similar to a semiconductor diode, it consists of an insulating layer sandwiched two layers of metal [9-11]. It is based on the tunneling mechanism. The insulating layer should be thin enough in the order of tens of atom layers for the tunneling. The fabrication process of thin film deposition for an insulating layer with a few nanometers thickness was achieved in the 1960s, the simple materials and fabrication technology make the MIM diode more competitive with other techniques. Multiple insulating barriers can be built in MIM diode to overcome the thermal voltage limitation of a Schottky diode [9, 12].

Operation principle and characteristics

Two operation mechanisms involve in a MIM diode, namely quantum tunneling and thermal activation (also called Schottky effect) [9, 13]. The geometry of the insulating layer, such as thickness, barrier height as well as temperature, will determine the domination of each mechanism. Tunneling will dominate only when the barrier is high and thin enough. The two mechanism can be sorted out by the measurements for MIM diodes with two barrier thicknesses at two different temperatures [14].

Applications

MIM diode can be used in the high-speed applications due to the tunneling mechanism and very low junction capacitance, for instance, a mixer at 148 THz [15]. It also could be used in the rectifier, the state-of-the-art MIM diode with multiple insulating layers has already presented very similar zero-bias current responsivity with the Schottky diode [9].

1.1.1.10 Gunn diode

Construction

A Gunn diode is a type of transferred electron device (TED), it operates on the principle of Gunn effect that is discovered by physicist J.B. Gunn in 1963 [16]. It presents a negative resistance region. Unlike other semiconductor diode consisting of P- and N-type semiconductor materials, Gunn diode is composed of only N-type semiconductor material, therefore, it is not a unidirectional device. A Gunn diode consists of two heavily doped materials on the terminals, and a thin layer of lightly doped material in the middle [1].

Operation principle and characteristics

In Gunn diode, the conduction electrons transfer between different energy levels with the influence of the electric field, it is also referred to as TED. When the bias at the two terminals of the Gunn diode increases, the current increases. At a certain bias level, the resistivity of the thin middle layer increases, which results in the drop of the current. In other words, the Gunn diode presents a negative differential resistance region, in which the increases of the bias will cause a decrease in current [1].

Applications

The property of negative resistance allows the Gunn diode can be used in the amplification application at microwave frequency, such as amplifier, oscillator, etc. Gunn diode oscillator can be used in airborne collision avoidance radar, anti-lock brakes, radar speed guns, motion detector, air traffic control, millimeter-wave radio astronomy receivers [16].

1.1.1.11 IMPATT diode

Construction

IMPATT (IMPact Avalanche Transit Time) diodes are semiconductor devices that use the properties of avalanche effect and transit time of semiconductors, also referred to as avalanche transit time devices. As illustrated in Fig. 1.15, IMPATT diode is made from a heavily doped N-type semiconductor layer (N^+ layer), beside which another lightly doped layer (N layer) is deposited epitaxially. At the other terminal, P-type semiconductor layer is heavily doped (P^+ layer) [1]. IMPATT diodes can be fabricated with Si, GaAs or InP. The Si-based IMPATT diode can work up

to above 200 GHz with high output and is cheaper due to the simple fabrication process. By contrast, the GaAs-based IMPATT diode has higher efficiency and lower noise than others.
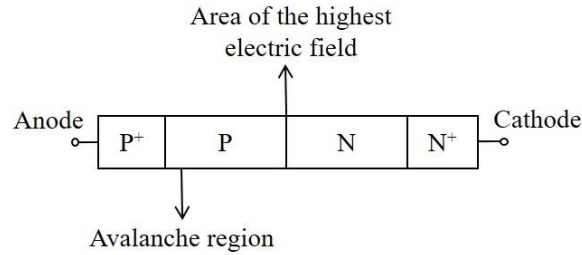
Figure 1.15: Schematic diagram of IMPATT diode.

Operation principle and characteristics

Although the structure of IMPATT diodes are similar to traditional Schottky or PIN diodes, the operation principle is quite different. Similar to a Schottky diode, it will break down at a certain level of reverse bias, the IMPATT diodes operate in this breakdown region and based on avalanche effect. When a certain level of reverse bias is applied, a high potential gradient is generated across the PN junction due to the narrow gap, which results in the acceleration of minority carriers. The accelerated carriers will collide with the crystal lattice, as a result more carriers will be freed and accelerated. This process will cause avalanche breakdown due to the fast multiplication of carriers [1, 17].

Applications

With the advantage of high-power capability, IMPATT diodes are used for solid-state microwave and millimeter wave power generation. Compared to Gunn diodes, IMPATT diodes are more efficient and have higher output power with lower power supply [1].

1.1.2 Capacitive nonlinear devices

1.1.2.1 Varactor

A varactor is a type of PN junction, having the junction capacitance optimized for a reverse bias scenario. It presents a variable capacitance with the control of the reverse bias [1, 2].

Operation principle and characteristics

A depletion layer is formed between P- and N-type of semiconductors when a reverse bias is applied, it can be seen as a dielectric between two semiconductors. With the increases of reverse bias, the width of the depletion layer increases, thus the junction capacitance decreases [1, 2]. The C(V) characteristic of a varactor is similar to a PN junction diode, as illustrated in Fig. 1.3. It also shares the same equivalent circuit model with a Schottky diode, as shown in Fig. 1.7.

Applications

Varactors are usually used in the application of tuning circuits, voltage-controlled oscillator (VCO), parametric amplification, harmonic generation, frequency multipliers, mixer, microwave signal synthesizers, active filters, signal detection and modulation, up-conversion, etc. [1, 2].

1.1.2.2 Ferroelectric ceramic

Barium Strontium Titanate (BST) [18, 19] and Lead Zirconate Titanate (also called PZT) [20, 21] are two most popular ferroelectric ceramics. BST is made by the complete solid solution of strontium titanate and barium titanate. PZT exhibits piezoelectric effect, its shape changes with the applied electric field.

Applications

BST and PZT have advantages of high dielectric constant, high tunability and low dielectric loss, it has been used in the application of phase shifter, capacitor, microsensors, dielectric ceramics with high energy storage, dynamic random access memory (DRAM), pyroelectric infrared detector, etc. [18-21].

1.1.3 Inductive nonlinear devices

Ferrite is a type of ferrimagnetic material made by iron oxide blended with other metallic materials. In terms of magnetic property, ferrites can be divided as soft ferrite, hard ferrite, and gyromagnetic ferrite. According to the type of crystal, the gyromagnetic ferrite can be classified as spinels (e.g. nickel ferrite), garnets (e.g. Yttrium Iron Garnet (YIG)) and hexaferrites (e.g. barium ferrite) [22].

Applications

With the advantages of low dielectric loss, narrow resonance line width at microwave frequency region, small saturation magnetism, YIG can be found in the applications of tunable filter, oscillator, circulator, isolator, phase shifter, bandstop filter, magnet recording, etc. [1, 23].

1.2   Emerging RF and microwave nonlinear devices

1.2.1   MEMS devices

A microelectromechanical system (MEMS) indicates a small size component/system that integrates both electrical and mechanical functionalities. Micromachining techniques are the key to MEMS fabrication process, the most generally used techniques are surface micromachining, bulk micromachining, and Lithographie, Galvanoformung, Abformung (LIGA) techniques. Assembly techniques and packaging techniques are also essential for MEMS fabrication, which can transfer MEMS devices to RF circuits, the most generally used techniques are flip-chip assembly, solder self-assembly, and wafer-level assembly [2, 24].

MEMS switch

RF MEMS switch can be classified as resistive contact switch and capacitive contact switch. The cross-sectional view of MEMS switch, as well as the equivalent circuit of the two switches are shown in Fig. 1.16 and Fig. 1.17, respectively [2].
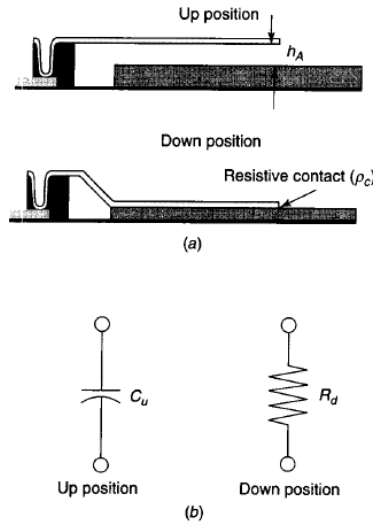
Figure 1.16: (a) Cross-sectional view and (b) equivalent circuit of resistive contact MEMS switch [2].

MEMS varactor

Similar to the capacitive contact MEMS switch which has two capacitive states, the capacitance of MEMS varactor can be changed continuously by controlling the physical dimension of the device with voltage [2].

Applications

With the advantages of small size, low weight, low insertion loss, high isolation, RF MEMS switch and varactor are used in the applications of phase shifters, tunable filters, impedance tuners, oscillators, mixer, information storage, materials science, switching devices in cell phones, etc. [2].
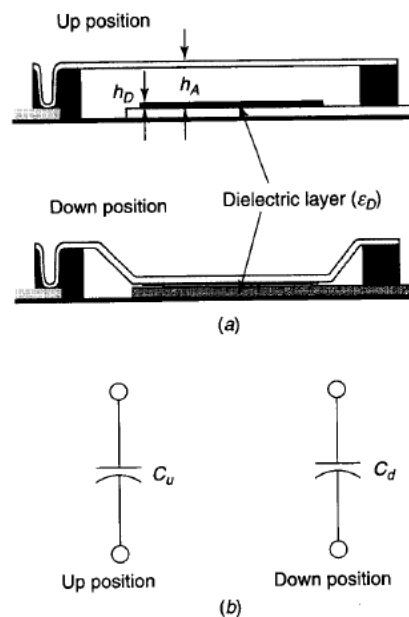
Figure 1.17: (a) Cross-sectional view and (b) equivalent circuit of capacitive contact MEMS switch [2].

1.2.2 Magnetic Tunnel Junction (MTJ)

Introduction and construction

As is well known that an electron has a charge and a spin, in conventional electronic device only charges are utilized, and spins are ignored. Until the discovery of giant magnetoresistance (GMR) of magnetic multilayers in 1988 [25], people started to control the motion of electrons efficiently by acting on the spins, which can be changed with the orientation of magnetization. This great discovery promoted the development of a new technology called spintronics (spin-electronics) [26].

The magnetic stack of the MTJ was deposited on a Si substrate and then etched into elliptical shape pillars of nanometric dimensions. As illustrated in Fig. 1.18, the magnetic stack consists of substrate PtMn 20 / CoFe 2.27 / Ru 0.8 / Cox1Fey1Bz1 2.2 / CoFe 0.5 / MgO 1.2 / $Co_{x2}Fe_{y2}B_{z2}$ 2.5, where the numbers following the composition are thicknesses in nm [27].
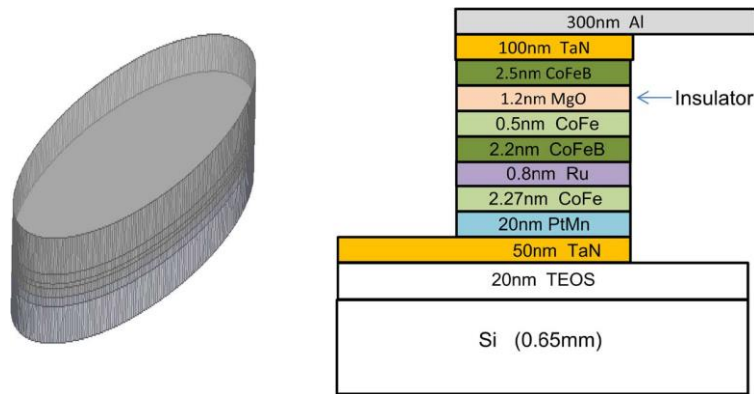
Figure 1.18: Description of the device (sketch on the right not to scale). Elliptical pillars have a typical section of 85 nm x 220 nm [27].
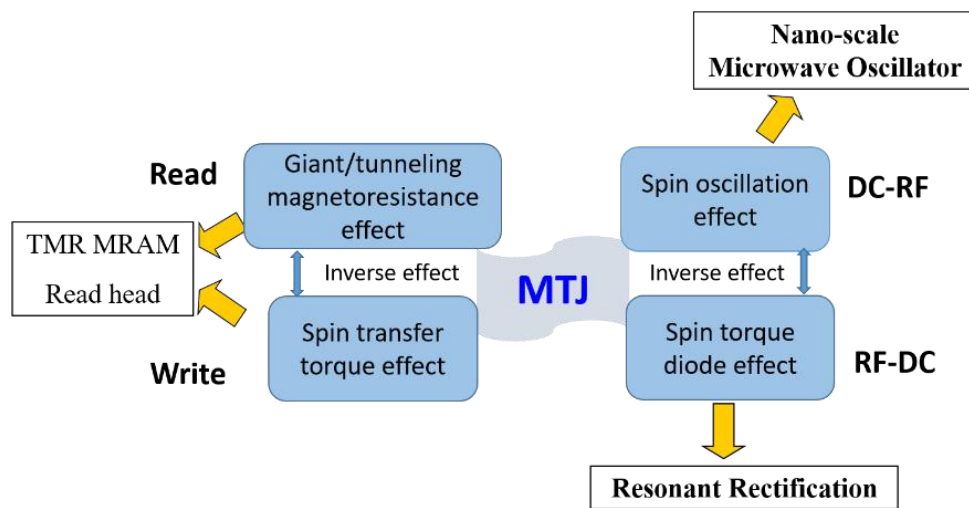
Figure 1.19: Four properties and corresponding applications of MTJ.

Operation principle and applications

As shown in Fig. 1.19, there are four essential properties in MTJ: (a) Tunneling magnetoresistance effect, (b) Spin-transfer torque effect, (c) Spin oscillation effect, (d) Spin torque diode effect [28]. 2007 Nobel Prize in physics was awarded to Albert Fert and Peter Grünberg for their discoveries

of giant magnetoresistance. The GMR based sensor was successfully applied in the read heads of hard disk drives in the 1990s. The research on tunneling magnetoresistance of MTJ was an essential step in the development of spintronics since MTJ can provide high TMR ratio at room temperature [26].

Spin transfer torque effect (b) is the opposite effect of (a), which is considered as the promising technique in the next generation Magnetic Random Access Memory (MRAM) [29]. Benefiting from the successful application in read heads and MRAM, intensive research on MTJ has been done from different perspectives. Another application of spin transfer torque effect is the microwave oscillator, the polarized current can result in the magnetization precession in the free layer, and hence excites steady state oscillation. The oscillation frequency is in GHz and can be tuned by dc bias current and external magnetic field, this tunability and compatibility with conventional CMOS process make MTJ based oscillator as a potential candidate for microwave generator [30].

The MTJ also has rectification behavior due to the spin torque diode effect, it is also called spindiode in this perspective. When applying a small RF current to MTJ, the spin-polarized current which is polarized in the reference layer can cause a magnetization precession in the free layer. As shown in Fig. 1.20, once the frequency of applied RF current is close to the precession frequency, this effect can excite a ferromagnetic resonance (FMR) mode, and result in oscillation of resistance and hence a rectification [31]. It is noticed that the spin torque diode effect (d) is also the reverse effect of (c).

Due to the tunnel magnetoresistance effect [26], the resistance of the structure depends on the relative alignment of magnetizations of the reference and free layers. As described in the inset of Fig. 1.21, the heterostructure can have two stable states at zero volts, namely low resistance when the magnetizations of the two layers are parallel (P) and high resistance when the magnetizations are anti-parallel (AP). Due to the different compositions and thickness in the free layer and reference layer, the current-voltage characteristics of MTJs are not symmetric [32]. For an asymmetrical tunneling barrier, the resistance-voltage characteristic is roughly a parabola and the maximum resistance is not at zero bias due to the asymmetry (Fig. 1.21). The nonlinearity of resistance-voltage characteristic derives from the change of the tunneling probability, which is inversely proportional to the barrier height. When the applied voltage increases, the barrier height

decreases and then the tunneling probability increases, so that the resistance decreases [33, 34]. In other word, the MTJs exhibit nonlinearity in both anti-parallel (AP) state and parallel (P) state. This nonlinearity is a crucial factor for the non-resonant rectification that converts RF power into DC.
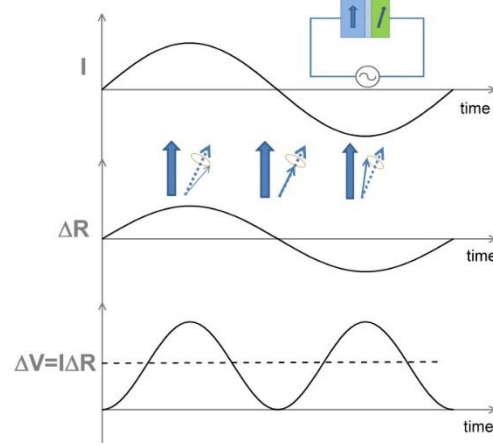
Figure 1.20: Spin torque diode effect.
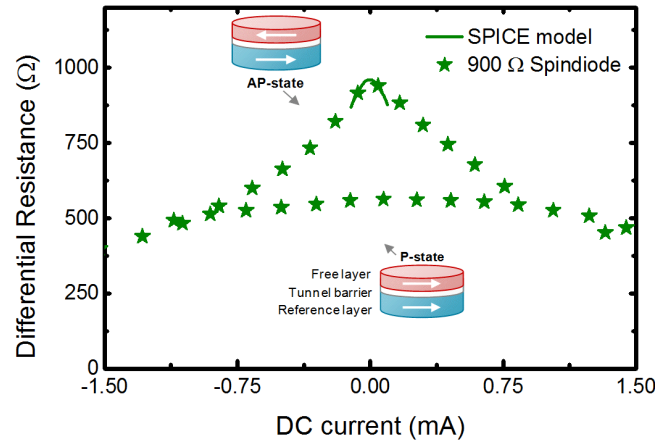
Figure 1.21: Measurements and modeling results of differential resistance of devices obtained by taking the first derivative of voltage with respect to current.

The magnetic state of an MTJ can be changed upon the application of an external magnetic field or a voltage via a physical phenomenon called spin transfer-torque [35]. The state switching is visible in Fig. 1.22 at $\pm$ 600mV. The mainstream use of the MTJ hard disk read heads and magnetic random access Memory (MRAM). Since this technology is now widespread and will continue to expand into new applications, all the tools are available for a mass production of RF spindiodes.
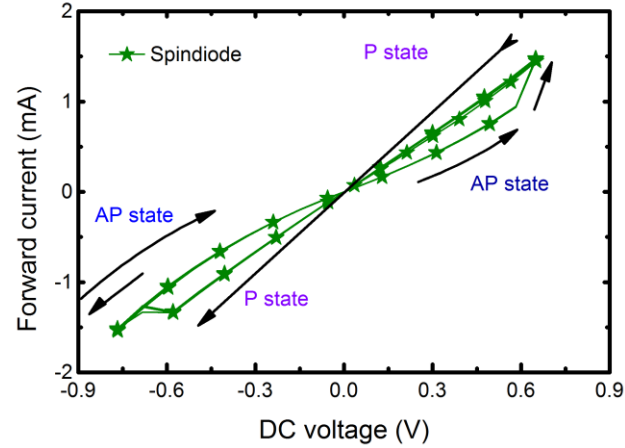
Figure 1.22: IV characteristic of spindiode. Transitions between the two magnetic states of a spindiode are obtained for an applied voltage of 600 mV for AP-to-P and -600 mV for P-to-AP.

Table 1.2: Comparison of traditional and emerging nonlinear transmission line (NLTL) techniques.

Categary	Nonlinear Type	Nonlinear Device	Applications
traditional NLTL techniques	capacitive	semiconductor varactor	pulse sharpener, shock wave, true time delay line, phase shifter, harmonic generation, comb generator, high power RF generation, soliton wave, etc.
	inductive	ferrite	
emerging NLTL techniques	hybrid	varactor and ferrite	

1.3 Traditional NLTL techniques

Traditional NLTL is a transmission line loaded periodically with nonlinear elements, such as nonlinear capacitance or nonlinear inductance. As listed in Table 1.2, the traditional NLTL can be classified as capacitive NLTL, inductive NLTL according to the types of nonlinear elements used in the NLTL. There are three characteristics for NLTL, nonlinearity, dispersion and dissipation [36]. The nonlinearity arises from the voltage-dependent capacitance or current-dependent inductance of the nonlinear elements. The dispersion means the variation in phase velocity with frequency, which is caused by the periodicity of the structure. The dissipation is from the conductive loss of the transmission line and series resistance of the nonlinear elements. NLTLs can be found in a variety of applications, such as ultra-short pulse generation, true time delay line for

wideband antenna array, phase shifter, soliton wave, high power generation, harmonic generation, filtering, etc.

1.3.1 Classification of NLTL

1.3.1.1 Capacitive NLTL

Capacitive NLTL is implemented either by periodically loading nonlinear devices (varactor [37-40], BST [41-43] or PZT [20, 21]), also called periodically loaded NLTL, or by continuously distributing the nonlinearity in semiconductor substrate [44], also called fully distributed NLTL. The circuit diagram and equivalent LC circuit model of a periodically loaded capacitive NLTL with varactor are shown in Fig. 1.23 And Fig. 1.24, respectively.
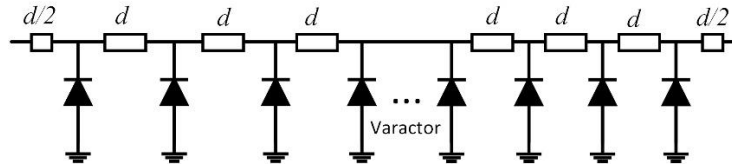
Figure 1.23: Circuit diagram of varactor-loaded NLTL.
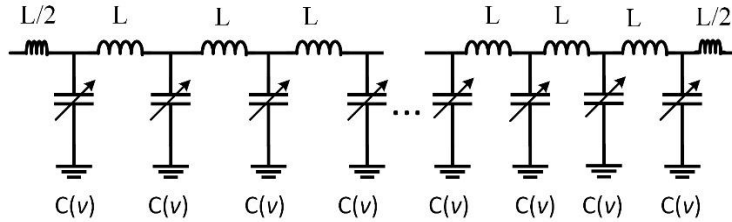
Figure 1.24: Equivalent LC circuit of varactor-loaded NLTL.

1.3.1.2 Inductive NLTL

As shown in Fig. 1.25, inductive NLTL can be constructed by coaxial line loaded with nonlinear inductance that arises from ferromagnetic, such as ferrite [45]. The equivalent LC circuit model of inductive NLTL is shown in Fig. 1.25, in which the ferrite is modeled as variable inductance. A particular application of ferrite-loaded coaxial NLTL is for high-voltage pulse-sharpening and microwave power generation [45-50]. The ferrite can be pre-biased by a dc current through the center conductor of the coaxial line, then it will be driven to saturation region by a high voltage pulse of 10 - 100 kV.

<div align="center">(a)   (b)</div>
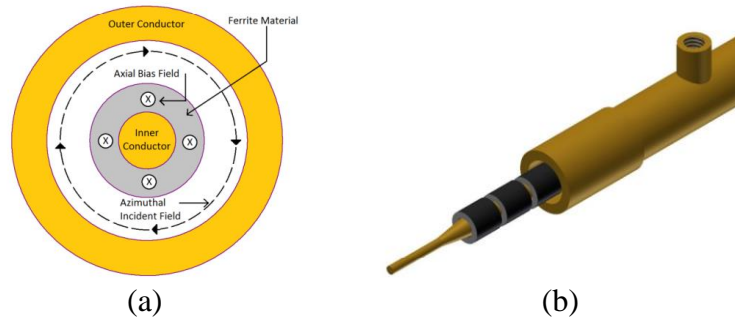
Figure 1.25: (a) Cross sectional diagram and (b) 3D model of the ferrite-loaded NLTL [48].

1.3.2 Application of NLTL

Table 1.2 lists the applications of NLTL, it can be classified by the balance of nonlinearity and dispersion, operation frequency compared to Bragg cutoff frequency, small signal or large signal, etc. [36, 51]. Because the input impedance of a NLTL is almost real, it is helpful for the wideband matching.

Pulse sharpener / shock wave

For varactor-loaded NLTL, the nonlinearity arises from the voltage-dependent capacitance of varactor. As is known that different capacitance can result in different phase velocity, in other words, the wave travels at different velocities when voltages are different, which results in the sharpening of either rise-time or fall-time of a pulse [40, 51-56]. By contrast, the dispersion of the structure will expand the pulse. When nonlinearity and dispersion come to a balance, limited rise-time or fall-time is reached [51].

For ferrite loaded NLTL, the nonlinearity arising from the current dependent inductance of ferrite. High voltage with the order of kV is used in this case to drive the ferrite to saturation region [46-48, 50, 57], a sub-nanosecond rise time of pulse can be obtained.

True time delay line / phase shifter

NLTL is by nature a delay line / phase shifter when operating in small signal regime [51, 58-60]. The dc bias of the varactor controls its capacitance, so as to control the phase velocity of NLTL. The bandwidth of the phase shifter is determined by the Bragg cutoff frequency as well as the cutoff frequency of the varactor. Compared to the phase shifter that is frequency dependent, true time delay line can provide the same delay time for a range of frequency, in other words, the true time delay line is frequency independent. It can be used for wideband phased array. In addition, for a

true time delay line, the operation frequency is much smaller than f_{Bragg}, the dispersion is negligible over the operation frequency band.

Harmonic generation / comb generator

NLTL can be used for harmonic generation, its lowpass behavior can filter higher order harmonics so as to increase the conversion efficiency [51, 61-63]. NLTL operates at intermediate dispersion region which is less than a half of the Bragg cutoff frequency. When the operation frequency is much less than the Bragg cutoff frequency, NLTL can be used for comb generator [64].

High power RF generation

Ferrite-loaded NLTL can be used to generate a high power RF and microwave signal up to sub-gigawatt level [43, 65-69]. Similar to the pulse generator, pulse with the order of kV voltage needs to be applied.

Soliton wave

When the dispersion and nonlinearity come to a balance, soliton wave will occur along the NLTL. Soliton wave is an ultra-short pulse, it has special propagation characteristics [70, 71]. Similar to the pulse sharpener, soliton wave can be used in the application of ultra wideband communication system, sampling oscillator, vector network analyzer, etc. the NLTL operates at high dispersion region with the operation frequency close to the Bragg cutoff frequency.

1.4 Emerging hybrid NLTL

In [72], the concept of hybrid NLTL was first proposed, which includes both nonlinear capacitance and nonlinear inductance. For a lossless NLTL, the characteristic impedance can be expressed as $Z = \sqrt{L(i)/C_T(v)}$, the phase velocity can be expressed by $v_p = 1/\sqrt{L(i)C_T(v)}$, where L($i$) and C($v$) denotes the equivalent inductance and capacitance, respectively, per unit length. Traditional NLTL is made by either voltage-dependent capacitance and linear inductance, or current-dependent inductance and linear capacitance. Although the characteristic impedance of traditional NLTL is real, it will change with the voltage or current which makes the matching difficult in a large dynamic range [72]. The proposal of a hybrid NLTL gives more freedom to manipulate the characteristic impedance and phase velocity. For instance, if L(i) and C(v) are tuned in the same manner (Fig. 1.26(a)), the characteristic impedance can be kept constant (Fig. 1.26(b)), while the

phase velocity changes faster than the traditional NLTL, which results in a larger phase shift or pulse compression for each unit of NLTL. In [72], the nonlinear inductance is made by a saturating ferrimagnetic inductor on A9 Ferroxcube core. The experiments show a good agreement with the theory. However, the fabrication of inductors are complicated.

Since the last four decades, some works related to hybrid NLTL have been conducted but only based on simulation [73-77]. So far, no further experiment has been reported to our knowledge. As it will be seen later, this thesis work discusses the possibility to realize a hybrid NLTL at circuit level.

(a)   (b)
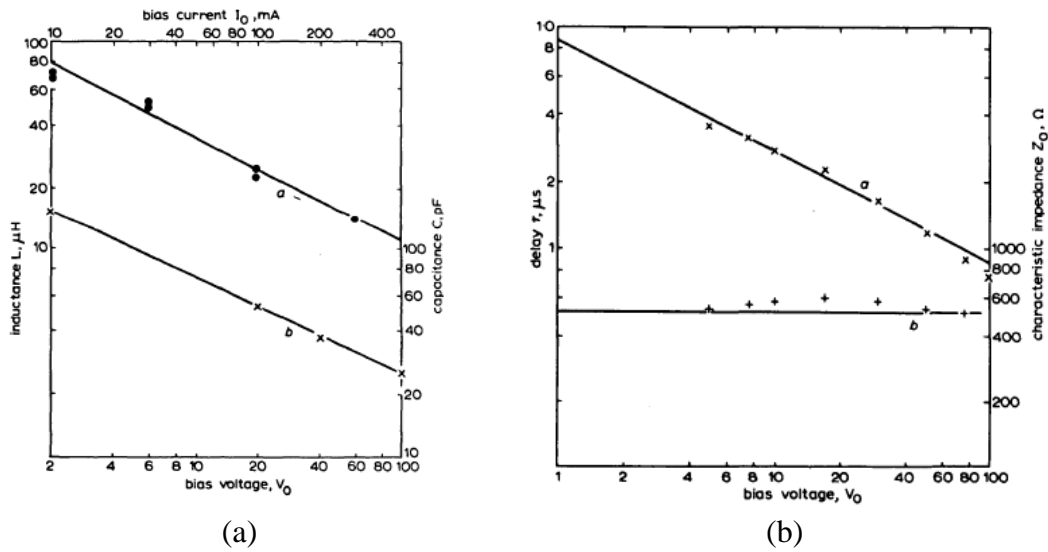
Figure 1.26: (a) Characteristics of nonlinear inductance and capacitance; (b) variation of delay and characteristic impedance with bias [72].
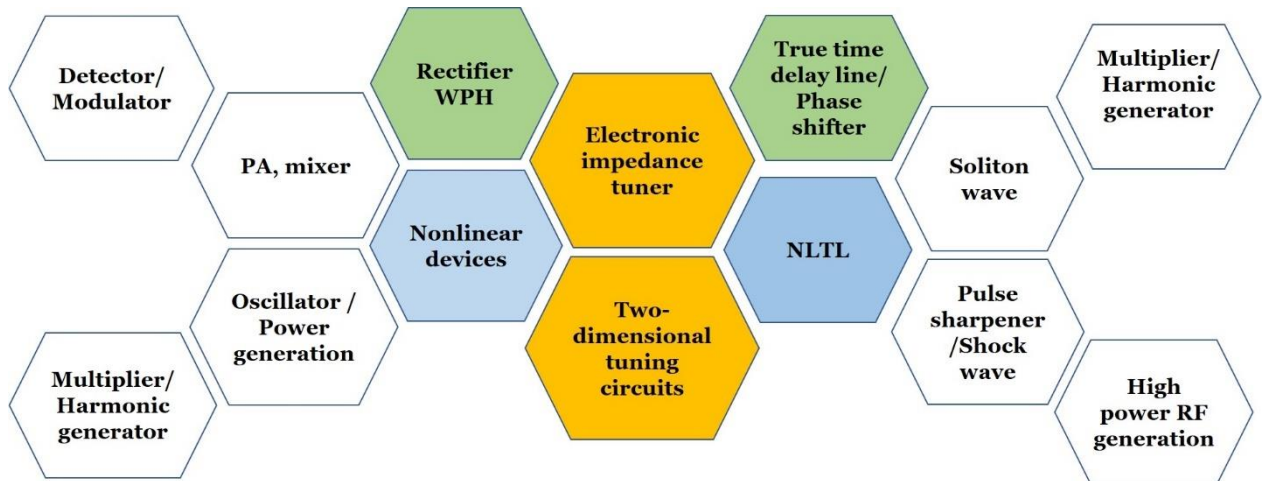
Figure 1.27: Applications of nonlinear devices and NLTL techniques

1.5 Thesis Outline

This thesis research investigates the traditional and emerging passive nonlinear devices and nonlinear transmission line (NLTL) techniques. In addition, different microwave applications for nonlinear devices (the left half in Fig. 1.27) and NLTL-technique (the right half in Fig. 1.27) are explored. Four applications [78-81] will be presented in this thesis. Application of a new type of nonlinear device is investigated in Chapter 2, in which Schottky diode and spindiode are analyzed for the applications of RF and microwave energy harvesting in order to achieve a high efficiency at low power environment [27, 79]. Three common applications of nonlinear device and NLTL technique are implemented in Chapter 3, 4 and 5. In Chapter 3, negative resistance device and NLTL-based phase shifter are utilized to realize an electronic impedance tuner with reflection coefficient larger than one [80]. In Chapter 4, a non-uniform distributed electronic impedance synthesizer is developed based on PIN diode and NLTL techniques [81, 82]. In Chapter 5, a hybrid NLTL is analyzed in both time domain and frequency domain. Parameters of effective permittivity and permeability are extracted based on the f, and the theory is validated with simulations and experiments. Then, small signal and large signal applications of two-dimensional tuning circuits are discussed. Our hybrid NLTL technique is investigated and developed in an attempt to overcome the impedance matching problems.

CHAPTER 2   LOW-POWER HIGH-EFFICIENCY RF AND MICROWAVE ENERGY HARVESTING

Much progress has been made in the research and development of rectifiers since the first high-frequency power detectors were fabricated by Hertz. In the last decades, Schottky diodes have increased the efficiency of RF rectifiers while integrated electronic devices, following the Moore's law, have become less energy consuming [83, 84]. The result of this device research suggests the ability to power simple devices, such as low-duty cycle sensors, microcontrollers and RF transmitters, without a battery but powered instead by means of a Wireless Power Transfer (WPT) [85]. Regarding the powering capabilities, RF and microwave WPT systems can be divided into three types (qualitative output dc powers are given with respect to FCC compliant systems): Near-field Power Transfer (tens of watts, but limited to a meter-range distance), Microwave Power Transfer (MPT) or Power Beaming Transfer (tens of milliwatt, up to a few meters distance with a limited space positioning freedom), and Surrounding or Ambient Microwave Power Harvesting (MPH) (up to hundreds of microwatts, but without a distance limitation if the receiver is in the proximity of a statistically concentrated area of RF transmitters or base-stations like the areas covered by broadcasting stations and cell phone systems).

The core enabling part of MPH and MPT system is the rectifying circuit. This is because it should convert a limited available RF power into an exploitable dc energy. The work of Brown [86] is one of the most important milestones in this field. Before that, research was focused on obtaining highest possible microwave-to-dc efficiency. After that, efforts have been redirected toward pushing the maximum efficiency of rectifying circuit to the handling of a lower input RF power.

In the mid-70s, using GaAs fast solid state diodes, the team of Brown yielded outstanding RF/dc rectification efficiencies, such as 82.5% for 8 W input power reported in [87]. In 2001, with the introduction of a new diode [88], the record was brought to 84.4% overall rectification efficiency for an input power of 105mW (~20dBm) [89]. A high efficiency can be obtained at this power level because the high barrier Schottky diode operates as a switch: an open circuit for applied negative voltages and nearly a short circuit for applied positive voltages.

However, the MPT community is facing a fundamental dilemma because RF rectifiers have a poor low power efficiency and the efficiency decreases with transmission distance (Fig. 2.1, calculated with [90]). In Fig. 2.1, measured efficiency vs input power is extracted from [89] for the M/A-COM device, from [91] for the Powercast device and from [92] & [93] for the Skyworks device at medium power & low power, respectively. The data are presented to provide a qualitative view of the situation. Data are calculated and generated using the read range equation [94] with typical value i.e. 1W of radiated power, 5 dBi circularly polarized transmitting antenna, 5 dBi linearly polarized receiving antenna, CW frequency of 915MHz and efficiencies presented in Fig. 2.2. Consequently, the output dc power drops abruptly as transmission distance increases. This is a difficult-to-overcome issue because a high efficiency at a long transmission distance is needed to maximize the powering range. An efficient low power rectifier could increase the effective range of the rectenna. The problem is similar for ambient RF energy harvesting. With current low power limitations, the low surrounding energy cannot be harvested in most areas.
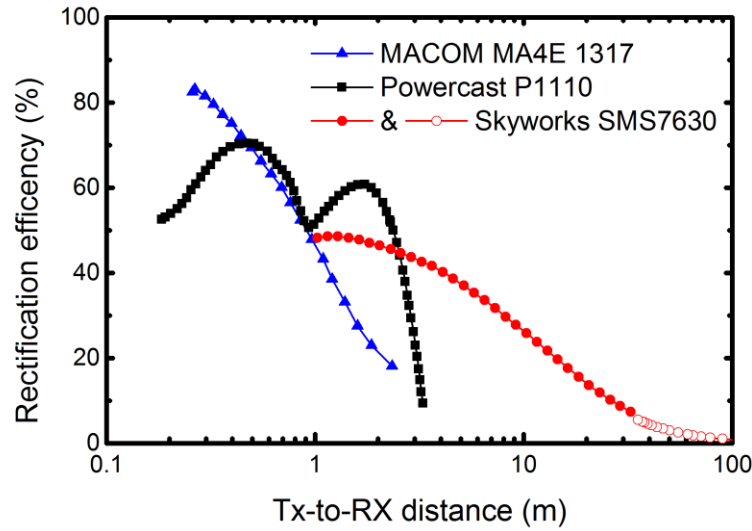
Figure 2.1: Maximum rectification efficiency that can be expected from state-of-the-art commercial rectifying devices.

Comprehensive state of the art rectifiers reported in the literature with Schottky diodes [87, 89, 95-102], CMOS [103-105] and transistors [106] are presented in Figure 2.2. The corresponding works are listed in Table 2.1 for simplifying the presentation. It gives a very good picture of the maximum RF-dc conversion efficiency that can be reached for a large range of RF power. It also highlights the critical role of those nonlinear devices in the functionality of a rectifying circuit.
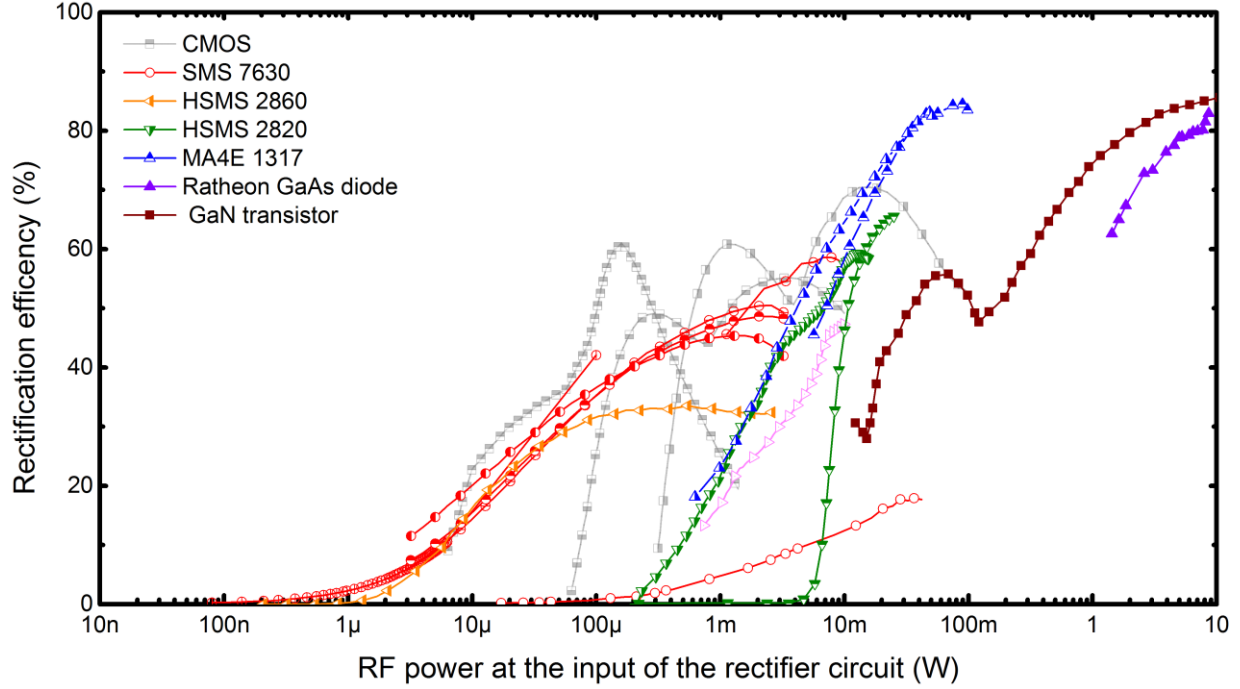
Figure 2.2: State of the art microwave rectifier circuits (measurements). Color/shape of the scatters indicate on which nonlinear device a circuit of interest is based (see Table 2.1). Rectifiers that do not include matching circuit losses are not reported here.

This is particularly obvious for rectifier designs based on SMS7630 Schottky diode. Although the works reported in the graph are related to a number of very different circuit architectures, harmonic termination techniques, substrate and frequencies, the outcomes are all limited by the junction nonlinearity. In other words, using the same diode would yield similar results. The circuit in [99] was an exception because the diode is directly mounted on a spiral antenna with neither matching condition nor harmonic termination. In this case, most of the energy does not reach the junction. This is a good example that reflects the difficulties of a broadband rectifier matching.

The devices operating at a power higher than 10 mW (transistor and high barrier Schottky diode) are the only ones that can reach more than 80% efficiency. Due to the low ON resistance, the matching is quite easy, and the dc power can be delivered efficiently to the load. To operate as a switch, however, the device needs to be biased/self-biased, which requires energy. For this reason, those devices cannot operate with a low input power.

As for low power rectifications (µW and lower), the principle is significantly different because it operates around the zero-bias point. Thus, it is the zero-bias nonlinearity that plays a major role in

the physical and electrical mechanism of RF-dc conversion. On the other hand, the zero-bias resistance (ZBR) is a strong limiting factor for the RF energy to enter the diode (matching conditions and parasitic losses) and for the dc power to be delivered to the load. This limits the conversion efficiency to only a few percent at µW level.

Table 2.1: Description of circuits reported in Fig. 2.2

Symbol	Reference	Year	Rectifying device	Frequency
	[87]	1976	Custom GaAs diode	2.388GHz
	[89]	2002	MA4E1317	2.45GHz
	[89]	2002	MA4E1317	5.8GHz
	[90]	2006	HSMS2820	2.45GHz
	[96]	2010	HSMS2820	2.45GHz
	[97]	2009	HSMS2850	-
	[107]	2010	HSMS2860	2.45GHz
	[93]	2004	SMS 7630	broadband
	[92]	2010	SMS 7630	2.45GHz
	[108]	2010	SMS 7630	2.45GHz
	[108]	2010	SMS 7630	1.85GHz
	[108]	2010	SMS 7630	0.9 GHz
	[109]	2012	SMS 7630	1.96 GHz
	[91]	2008	CMOS	2.45GHz
	[104]	2009	CMOS	915MHz
	[105]	2009	CMOS	915MHz
	[110]	2012	GaN transistor	2.14GHz

The third operation region is related to the medium power. In this region, there is a progressive transition from the zero-bias nonlinearity to the "switch" behavior. To give a simplified explanation, the device nonlinearity plays the same role as in the low power region. But the device is self-biased, resulting in a lower video resistance, thus leading to an improved efficiency. It should be noted that

due to their ON/OFF behavior, the high barrier diodes have a very high ZBR and therefore cannot operate at a low power level. That is why a single device cannot operate in a large power span.

It can be concluded from this above discussion that the nonlinear device is the key of the rectifier circuit. Even if a high-power rectification has not been a challenge since a long time, there is still a lot that needs to be done for low power scenarios. This chapter addresses the low power rectification from the perspective of the zero-bias responsivity and the ZBR. It will be shown that existing Schottky and CMOS devices exhibit fundamentally limited low power rectification capabilities. A novel type of nonlinear device, called Magnetic Tunnel Junctions (MTJ), or simply spindiode, is introduced and investigated in this chapter. This device is based on Spintronics, a new field that explores not only the electron charge but also its spin effects [26]. Exploiting the intrinsic non-linearity of spindiodes and given their significantly lower ZBR than Schottky counterparts, the goal of this work is to determine the potential of MTJs for achieving a low power RF-dc high conversion efficiency.

2.1 Physical limitation of RF and microwave rectification

The principle of RF and microwave rectification is to transpose the energy carried by a wave at RF and microwave frequency to dc by a frequency conversion. During this process, the energy goes through four loss stages that prevent a rectifying device from being efficient. The efficiencies related to those different losses are displayed in Fig. 2.3 and explained in the following sub-sections. The overall rectifying circuit efficiency is based on the following [78]

$$\frac{P_{DC}}{P_{RF}} = \eta_M \cdot \eta_p \cdot \eta_0 \cdot \eta_{DCT} \tag{2.1}$$
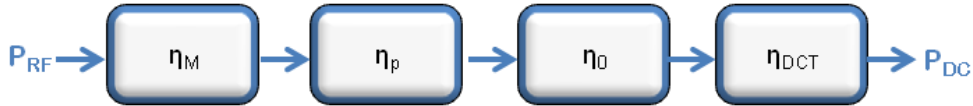
Figure 2.3: Efficiency link of a rectifying circuit, from RF power to dc power. η_M stands for matching efficiency, η_p is the efficiency associated with parasitic losses, η_0 is the efficiency of conversion that takes place in the nonlinear device (core conversion), and η_{DCT} is the efficiency of dc power transfer from the nonlinear device to the dc load. (A full rectenna would also include

the antenna radiation efficiency and dc/dc converter efficiency). The efficiency link is illustrated in Fig. 2.7 for SMS7630 diode.

2.1.1 Matching efficiency

Due to an impedance discontinuity, the RF and microwave signal experiences reflection losses when it enters a nonlinear device. The reflections can be canceled using a matching circuit, but potentially with the disadvantage of narrowing operating frequency band and adding insertion losses that can be troublesome at high frequency. Those effects can be seen in the single stage matching network case [111]:

$$\eta_M = \frac{1}{1+\dfrac{Q}{Q_c}} \tag{2.2}$$

but trends also stand for any matching networks. In (2.2), $Q = f(\rho_0)$ is the network quality factor that should be obtained to attain a matching condition, and is a function of initial unmatched reflection coefficient ρ_0 (Fig. 2.4). The net component quality factor $Q_c = f(1/R_c)$ describes the non-ideality of a real network. Q_c is a function of the inverse of resistance R_c, which is the equivalent parasitic resistance of the network's reactive component. To maximize the matching efficiency, $Q << Q_c$ should be satisfied, which means that for a given matching network technology, ρ_0 should be minimized. Besides, the higher the frequency is, the more lossy the matching circuit will be.

From Fig. 2.4, and assuming that the source impedance is 50 Ω, the initial unmatched reflection coefficient can be written as [23]:

$$|\rho_0|^2 = \frac{\left(R_j + (R_s - 50)\cdot\left(C_j^2 \cdot R_j^2 \cdot \omega^2 + 1\right)\right)^2 + C_j^2 \cdot R_j^4 \cdot \omega^2}{\left(R_j + (R_s + 50)\cdot\left(C_j^2 \cdot R_j^2 \cdot \omega^2 + 1\right)\right)^2 + C_j^2 \cdot R_j^4 \cdot \omega^2} \tag{2.3}$$

where ω is the pulsation or angular frequency, C_j and R_j are the junction capacitor and resistor and R_s is the series resistor (Fig. 2.4). For a better understanding, (2.3) can be simplified as follows:

$$|\rho_0| \approx \frac{R_j + (R_s - 50) \cdot (C_j^2 \cdot R_j^2 \cdot \omega^2 + 1)}{R_j + (R_s + 50) \cdot (C_j^2 \cdot R_j^2 \cdot \omega^2 + 1)} \qquad (2.4)$$

From (2.4), it is clear that at high frequency or when $C_j^2 \cdot R_j^2 \cdot \omega^2 \gg 1$, only R_s is required to be close to $Z_0 = 50\Omega$ because the junction resistor is "shorted" by the junction capacitor. However, an optimal operation is found at low frequency if $R_j + R_s$ is close to $Z_0 = 50\Omega$. Therefore, since rectifying diodes are not used above cut-off frequency, and since $R_j \gg R_s$ the main parameter to enhance the matching efficiency is the junction resistance R_j.

2.1.2 Parasitic component efficiency

A portion of the energy of wave is dissipated in the parasitic resistance R_s and passes through reactive parasitic component C_j of the nonlinear device and therefore cannot be converted. A major limitation is associated with a low-pass filter effect [112] where the junction resistance R_j is involved. Assuming that at zero-bias $R_j \gg R_s$,

$$\eta_p = \frac{1}{\left(1 + \left(2 \cdot \pi \cdot f \cdot C_j\right)^2 \cdot R_S \cdot R_j\right)^2} \qquad (2.5)$$

For (2.5) and the following equations, the junction resistance is a function of the dc current flowing through the junction (I_{bias}), that comes from self-biasing. The value of those components can be extracted from S-parameters measurements and I(V) measurements. The junction capacitance C_j is typically a function of the voltage across the junction. Special care should be given during the fabrication process of the nonlinear device and its packaging to minimize the parasitic losses.
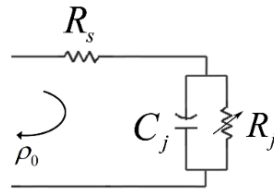
Figure 2.4: Model of a nonlinear component used in the analysis of this section.

2.1.3 RF-to-dc conversion efficiency

At a low power level, the nonlinear part of a rectifying device cannot be considered as a simple switch but needs to be modeled by a variable resistance. The nonlinearity of a device is inherently described by the dc voltage-current relationship. This can be expanded in power series about I_{bias} :

$$v(i) - v(I_{bias}) = \frac{v^{(1)}(I_{bias})}{1!} \cdot (i - I_{bias}) + \frac{v^{(2)}(I_{bias})}{2!} \cdot (i - I_{bias})^2 + ... \tag{2.6}$$

where $v^{(1)}, v^{(2)}, ...$ are derivative of $v(i)$ with respect to i. For the power range addressed in this work, higher-order (larger than two) nonlinearity terms can be neglected. If an RF current of magnitude M and frequency ω

$$i_{f_0}(t) = M \cdot \cos(\omega t) \tag{2.7}$$

flows through a perfectly matched junction, the rectified voltage can be calculated by replacing i by $i_{f_0}(t)$ in (2.6), and keeping only the terms for which $\omega = 0$:

$$v_{rect} = \frac{M^2}{4} \cdot \frac{d^2 v}{di^2} \tag{2.8}$$

In (2.8), it is considered that no power goes to the harmonics (ideal harmonic terminations). Keeping the term depending on ω will give the RF voltage across the junction:

$$v_{f_0}(t) = M \cdot \cos(\omega t) \cdot \frac{dv}{di} \tag{2.9}$$

which can be used to calculate the RF power absorbed by the junction, if we consider the later one as an integration of the product of the RF current and voltage over period T:

$$P_{f_0} = \frac{1}{T} \int_0^T v_{f_0}(t) \cdot i_{f_0}(t) \cdot dt$$

$$P_{f_0}(I_{bias}) = \frac{M^2}{2} \cdot \frac{dv}{di} \tag{2.10}$$

The voltage responsivity is the ratio of the output dc voltage by the input RF power and its unit is [V/W]:

$$\mathfrak{R}_v = \frac{v_{rect}}{P_{f_0}} \qquad (2.11)$$

With (2.8) and (2.10), one can extract $\mathfrak{R}_v$ from the I(V) measurements.

$$\mathfrak{R}_v = \frac{1}{2} \cdot \frac{\dfrac{dR_j}{di}}{R_j} \qquad (2.12)$$

with $R_j = \dfrac{dv}{di}$ being the differential junction resistance depending on I_{bias}. Responsivity is a parameter that is quite convenient to measure because it does not vary at low frequency, low power and high load resistor, and can be thus easily obtained experimentally. The open circuit voltage responsivity $\mathfrak{R}_v$ can be linked to the short circuit current responsivity $\mathfrak{R}_I$ by the differential junction resistance [112]:

$$\mathfrak{R}_v = \mathfrak{R}_I \cdot R_j \qquad (2.13)$$

The current responsivity will be used later because it does not depend on the junction resistance, but rather on the process and diode technology. The generated dc power that will be dissipated in the dc circuit can then be calculated by

$$P_{DC} = \frac{v_{rect}^2}{R_v + R_L} \qquad (2.14)$$

with $R_v = R_j + R_s$ being the video resistance. The conversion efficiency can now be expressed as a function of the junction resistance:

$$\eta_0 = \frac{P_{f_0} \cdot \mathfrak{R}_{I_0}^2 \cdot R_j^2}{R_L + R_s + R_j} \qquad (2.15)$$

The trend observed in Fig. 2.2, for which the efficiency increases with power can be explained with (2.15) as follows. The higher the input power becomes, the more the nonlinearity of the device will be used. This scenario is in a very similar manner as in the case of a square law detector, the higher the RF power becomes, the higher the dc voltage will be. Usually the current responsivity is limited by junction technology; therefore, one can try to fabricate a device with low series resistance and

high junction resistance to maximize (2.15). From the standpoint of conversion efficiency, it is also better to use a load that is small compared to the junction resistance.

2.1.4 DC power transfer efficiency

Once the RF wave is rectified, dc power should be used by the load, with minimum losses in the diode. This is expressed with the well-known dc power transfer efficiency [78]:

$$\eta_{DCT} = \frac{1}{1+\dfrac{R_v}{R_L}} \tag{2.16}$$

The nonlinear device can be seen by the load as a Thevenin generator. v_{rect} and R_v corresponds then to the Thevenin voltage resistance, respectively. Maximum dc power transfer efficiency is obtained for low video resistance and high load. However, if using a Maximum Power Point Tracking (MPPT) circuit that will show an optimum load to the rectifier, the dc power transfer losses can be strongly reduced.

2.1.5 Overall efficiency

It is difficult to integrate the matching efficiency into a generalized analytical model because this efficiency depends too much on the circuit technologies, but trends can be considered and will be discussed afterwards. Thus, considering low power and ideal matching conditions ($\eta_M = 1$ and $R_j \gg R_s$), the optimum diode efficiency is found when $R_j = R_L$:

$$\frac{P_{DC}}{P_{RF}} = \left(\frac{\Re_I \cdot \sqrt{R_j}}{2} \cdot \frac{1}{1+\omega^2 \cdot C_j^2 \cdot R_j \cdot R_s} \right)^2 \cdot P_{in} \tag{2.17}$$

As a conclusion, the conversion efficiency competes against other losses when considering the optimal value of the ZBR.

At low frequency (when $1 \gg \omega^2 \cdot C_j^2 \cdot R_j \cdot R_s$), it is desirable to have the highest possible junction resistance. This statement should be tempered by the matching consideration. As a matter of fact, most antennas have an impedance that is below 300 Ω, so going too far with R_j will result in a decrease of the overall efficiency because of the matching losses. However, at high frequency

(when $1 << \omega^2 \cdot C_j^2 \cdot R_j \cdot R_s$), it is vital to have a ZBR that is as small as possible. As for intermediate frequencies, it is preferred to choose the ZBR depending on the operating frequency and diodes inner parasitic. Therefore, it is highly desirable to have the ability to tune the ZBR, depending on applications. This is not possible for Schottky diode technology but very easy for spindiode.

2.2 Strength and limitation of Schottky diodes

The exponential I-V relationship of low and high Schottky barrier heights are given in Fig. 2.5. As it is emphasized by the differential junction resistance plotted in Fig. 2.6, the variation of resistance of the high barrier diode is greater than the low barrier diode. The result is a switch-like behavior but also a very high ZBR. The low Schottky barrier diodes (also called zero-bias diodes) are sacrificing the strong nonlinearity and small series resistance to reach a lower ZBR. In the case of a Skyworks diode SMS7630 used as a reference in this study, the responsivity value is about 100mV/µW, and it has a ZBR of 5 kΩ (Fig. 2.6). This value is rather small for a diode, but it is still very high for a low power rectifying device.
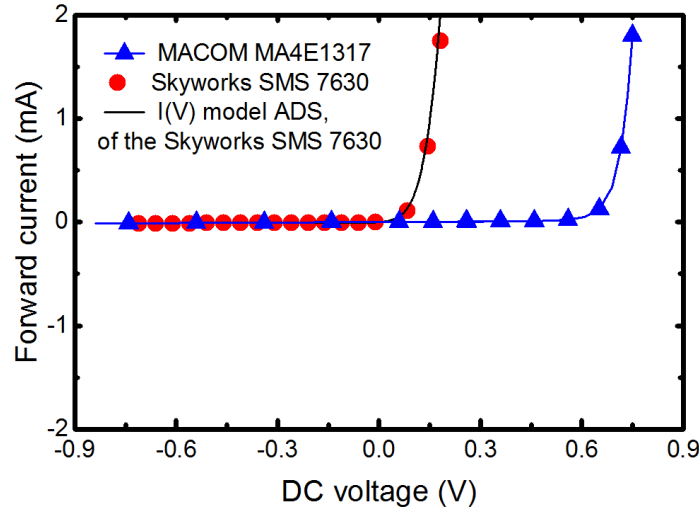
Figure 2.5: I (V) curve of Skyworks SMS7630 low barrier Schottky diode (red dots) and M/A-COM MAE1317 high barrier Schottky diode
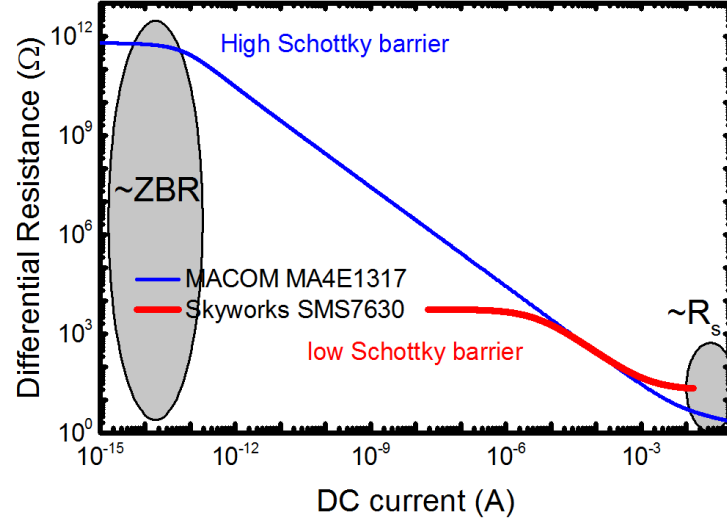
Figure 2.6: Differential resistance of the devices obtained by taking the first derivative of the voltage with respect to the current (Data calculated from the spice model). Under high bias (> 100mA), the differential resistance is very close to the series resistance (R_s). Also, under low bias ($< $ pA), the value tends to the Zero Bias Resistance (ZBR). Note that in reality, differential resistance does not reach value higher than few hundreds of kilo-Ohm due to leakage current in the device.
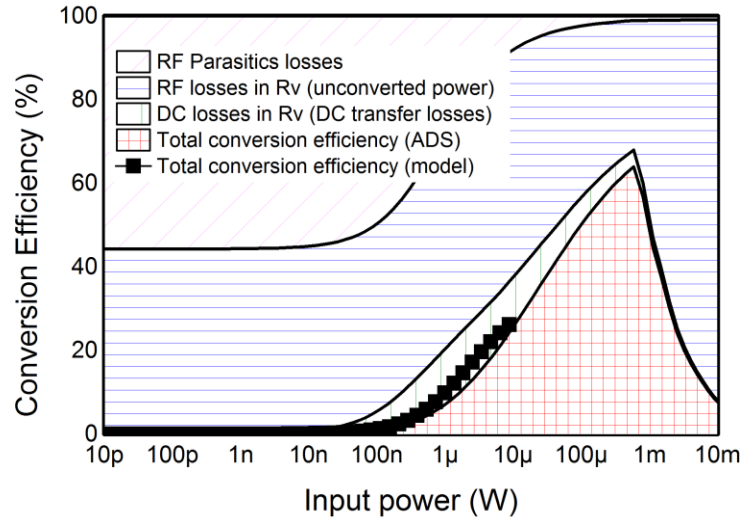
Figure 2.7: Study of the losses in a rectifying circuit based on the SMS7630 diode. Result are given considering a perfect matching and no circuit losses based on circuit simulation (ADS). The low power analytical model described in section 2.1 is plotted with boxes. Frequency is 2.45GHz and output load is 1 kΩ.

Because of the parasitic elements and this kilo-Ohm ZBR, the impedance changes rapidly with frequency, thereby resulting in the impossibility to match it for a wide frequency band, whereas a rectifier circuit would gain in rectifying a wideband signal [113]. Moreover, at high frequency, this ZBR is short-circuited by the low impedance shunt junction capacitor. This results in a shunt-cutoff frequency limiting the operation over the GHz range.

Fig. 2.7 provides a quantitative view of the operating losses. Data are obtained using Agilent Advanced Design System (ADS) circuit simulation software. In order to show only the diode losses, the device is considered as ideally matched, and the RF circuit losses are not taken into account. The simulation is run in a typical condition, i.e. 2.45 GHz CW input signal with a load of 1kΩ. Fig. 2.7 also plots the efficiency calculated using the equations presented in section 2.1. This model is good enough to describe the rectification mechanisms at µW level.

As it can be observed, the RF-dc conversion starts to be efficient from 100nW, but there is no impact on the overall rectification efficiency because of the parasitic losses and dc transfer losses that are both induced by the high 5 kΩ ZBR. As the power gets higher, the self-biasing starts to operate and the junction resistance progressively decreases, leading to a decrease of the dc transfer losses and the parasitic losses. Beyond 1mW, the breakdown voltage of the diode starts to have an impact on the rectification, leading to a decrease of the conversion efficiency [114].

Although the zero-bias Schottky diodes are better than high barrier diodes for medium power rectification, they are not well adapted for µW operation under those conditions, mainly because of their high zero-bias resistance. If one looks for a new device capable of increasing the low power rectification at high efficiency, focus should be given on the ZBR.

2.3 Use of spindiode for rectification

The spindiode is a MTJ composing of two ferromagnetic electrodes, called reference and free layers, separated by an MgO insulating layer. Fig. 2.8 compares the photograph of the MTJ device with a millimeter-wave Schottky diode. It can be seen that the junction area of the MTJ is much smaller (0.015 µm², cf. Fig. 2.8) than the Schottky junction, offering a possibility of high-density integration. The resistance-area product (RA) of the MgO junction in this work is about 10 Ω.µm², and the bit area varies from 0.006 to 0.04 µm^2. The samples can be classified in four subgroups of ellipse with different hard axis, designed to be equal to 63, 85, 100 and 120 nm. In each group, the

aspect ratio ranges from 1.7 to 2.5. For a given magnetic stack, the ZBR of the spindiode can be tailored to any resistance by simply adjusting the junction area.
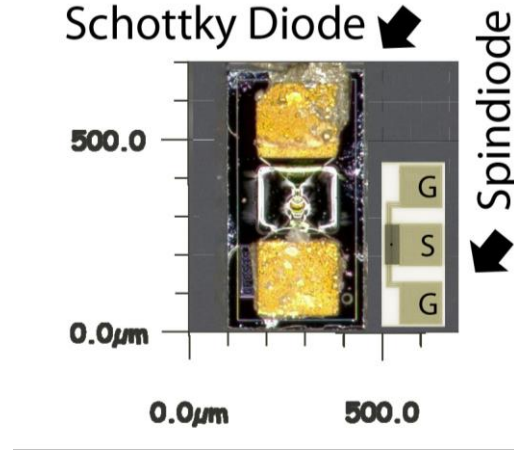
Figure 2.8: Photograph describing the Schottky diode MACOM MA4E13 (left) and the on-wafer spindiode (right) from Everspin Technologies. Three pads are used for measurement purposes using a Ground-Signal-Ground (GSG) RF probe. The spindiode area is less than 0.015µm² and is therefore not visible on the microscope image. Its location is indicated by a black dot.

2.3.1 Device modeling

The understanding of underlying physical mechanism is necessary prior to a spread use of the technology. Early electrical investigations have been focused on the analysis of junction resistance and tunnel magnetoresistance (TMR) as well as low frequency phenomena [115-117]. Nonetheless, the nature of the measurements done in those studies did not allow a comprehensive analysis of the effects observable only at microwave frequencies. In a recent attempt to extract the peak power of a spin-transfer induced precession oscillator, a lossy capacitance signature has been identified [118] in the parasitic impedance of MTJ at microwave frequencies, but has been incorrectly attributed to the top and bottom electrodes. It suggested that the samples with the same test pads should have the same parasitic impedance, obviously this is not true in the reality. Actually, the parasitic parameters of MTJ should be bit area-dependent.

2.3.1.1 Measurement setup

The samples of MTJs we studied in this work are from Everspin Technologies, Inc. The on-wafer samples were fabricated for the application of MRAM, and there is no available datasheet and commercial document. The set up used in this work was controlled by a Labview automation

software to run 3 measurements in sequence, the frame and front panels of the program are shown in Fig. 2.9. First, the I(V) curve is measured in order to extract the device nonlinearity and ZBR. Those values were used to control the quality of the device. Then, RF measurements of S_{11} parameter and dc rectified voltage were done to evaluate the applicability of MTJ for RF and microwave applications. Finally, another I(V) curve was measured to control the integrity of the device after RF and microwave measurements.
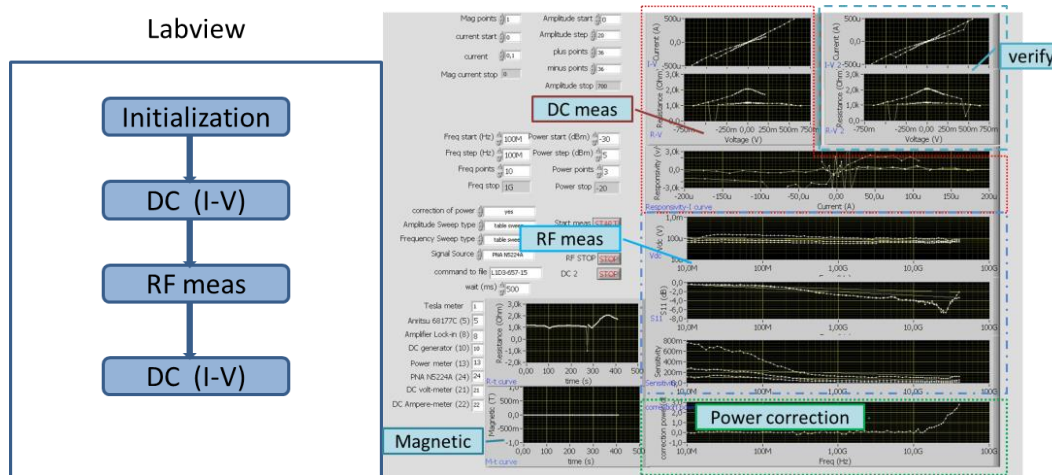
Figure 2.9: The frame and front panel of the developed program for spin diode measurement.
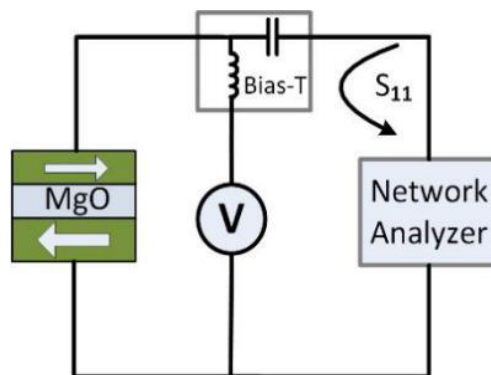
Figure 2.10: Schematic diagram of the setup based on Vector Network Analyzer that is used to measure voltage coefficient, the voltmeter is assigned to measure the non-resonant rectification through a bias-T.

The RF measurements were mainly based on a dc voltmeter and an one-port Vector Network Analyser (VNA) that is not only used to measure the voltage reflection coefficient (S_{11}) but also used as RF signal source for rectification measurement (Fig. 2.10). All measurements were done on a Summit Cascade Probing station, using GSG (Ground-Signal-Ground) GGB industry 150 µm

pitch probes. It should be noted that the output power of VNA is frequency dependent, this should be taken into consideration especially for the measurement at high frequency. Fig. 2.11 shows the diagram of power calibration with the internal de-embedding tool from VNA, and a power correction was made to compensate the loss from VNA, cable and probe. It can be seen clearly that the power correction was significant at high frequency especially above 10 GHz. During the measurements, the power delivered to the end of the GSG probe always remains constant at -20 dBm (10 µW). The sensitivity was computed later using this power as a reference. The dc voltages were retrieved using the bias-T of the VNA and measured using a 6½ digit HP 34401A voltmeter with more than 1 s of integration time. I(V) characterization of the samples were done using an Agilent 33250A as voltage source, an HP 3457A as ampere meter, and a HP 34401A as voltmeter.
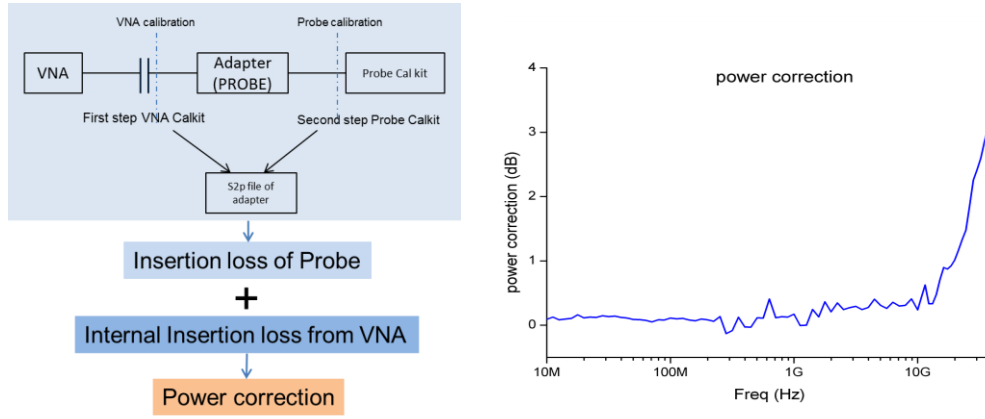
Figure 2.11: Power calibration with de-embedding technique and power correction.

2.3.1.2 Equivalent circuit

Due to the novelty of this device, however, the research community working on the MTJ has not yet come to a consensus on this point. In this work, it has been chosen not to enter the debate in order to focus on targeted RF and microwave applications. Similar to emerging X-parameters, a behavioral model will be considered (Fig. 2.12). The model merges a nonlinear description of the junction tunnel magnetoresistance with a set of high frequency parasitic components. The former is the core of the MTJ behavior, while the latter significantly yields adverse effect at microwave frequencies. The junction resistance dependence with the bias voltage is approximated by:

$$R(i) = R_0 + i \cdot v_j^{(2)} + i^2 \cdot v_j^{(3)} \tag{2.18}$$

for a very small current, where $v_j^{(2)}$ describes the zero bias detector capability of the MTJ and the parameter $v_j^{(3)}$ is mostly related to the I(V) curve point symmetry [9]. The zero bias resistance R_0 is commonly defined as:

$$MR = (R_{AP} - R_P) / R_P * 100 \qquad (2.19)$$

where θ is the angle between fixed layer and free layer.
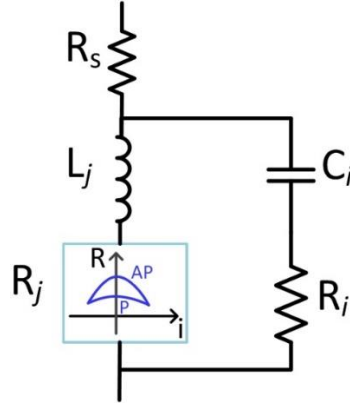
Figure 2.12: Equivalent MTJ model with nonlinear description of junction resistance and high frequency parasitic components. Test pads effect is not shown in this model.

The set of parasitic components comprise series resistance Rs, accounting for the access leads and the top and bottom contacts losses. With the definition of magnetoresistance ratio $MR = (R_{AP} - R_P) / R_P * 100$, our samples are supposed to have MR ratio of 80% since the MR ratio measured at a constant voltage should be independent from the bit area. By measuring MTJs with different bit area, it is possible to extract the series resistance Rs that makes the corrected MR ratio independent of bit areas. With the correction of $MR = (R_{AP} - R_P) / (R_P - R_S) * 100$, R_s is extracted and has a value of roughly 30 Ω for all samples. L_j is anticipated to represent the change of MTJ characteristics as response to magnetic field and current variations in the ferromagnetic materials and is extracted to be 0.1 nH for all samples. For a typical sample of $R_0 = 600\ \Omega$, the impact of L_j on the MTJ behavior is negligible below 50 GHz. Interfacial capacitance C_i and interfacial resistance R_i are used to express the spin-dependent screening effect at the interface of ferromagnet/insulator [119, 120]. The model has been rigorously checked on tens of samples for every elliptic shape and size to allow more accurate inferences to be drawn from our measurements.

As an electric field is applied to the MTJ, the buildup of electric charges gives rise to an electron screening effect. The induced charges will impact the surface magnetization of ferromagnet [119, 120] due to the exchange interaction. As a result, the unbalanced chemical potential between spin up and spin down will result in a spin-dependent voltage drop at the interface, which is modeled in Fig. 2.13 with the interfacial resistance R_i, while the spin accumulation at the interface is described by an interfacial capacitance. It should be noted that the use of a series branch of a resistor and a capacitor in shunt with the junction resistance in an MTJ model has been properly applied to MTJ [118], but was previously attributed to measurement artefacts.

The model parameters are extracted from Current-Voltage characteristic measurements, impedance measurements, and non-resonant rectification measurements. The details of extraction are shown in the following sections. Errors are analyzed by taking the uncertainty from the measurement instruments and extraction method into consideration.

2.3.1.3 Linear model extraction and validation

The linear part of the model in terms of parameters R_s, L_j, C_i and R_i is extracted from impedance measurements. Fig. 2.17 shows the real part (Re (Z)) and imaginary part (Im (Z)) of the impedance in both antiparallel (AP) and parallel (P) states for two elliptical MTJs with different junction areas (0.02 and 0.0096 μm^2). Error bar is added to the results by considering the uncertainty from the VNA. SPICE simulations are compared to the measurements in the figures. The real part of the impedance at low frequency is equal to the junction resistance defined by the tunneling probability of the barrier and the junction areas. As frequency increases, the real part of the impedance decreases as the alternating currents flow through the interfacial capacitance. The imaginary part of impedance stays negative, which witnesses the strong capacitive property of the magnetic tunnel junction.

The interfacial resistance and capacitance are related to the unbalance of spin up and spin down, and the amount of spin accumulation at the interface of ferromagnet/insulator. Therefore, they are bit area-dependent, and cannot be credited to the measurement procedure. As shown in Fig. 2.14(a) – (d), the interfacial resistance and interfacial capacitance in AP state are not the same as in P state, which indicates the resistance shall be related to the magnetization of MTJ. More investigations are necessary to establish what physical mechanism is standing behind this.
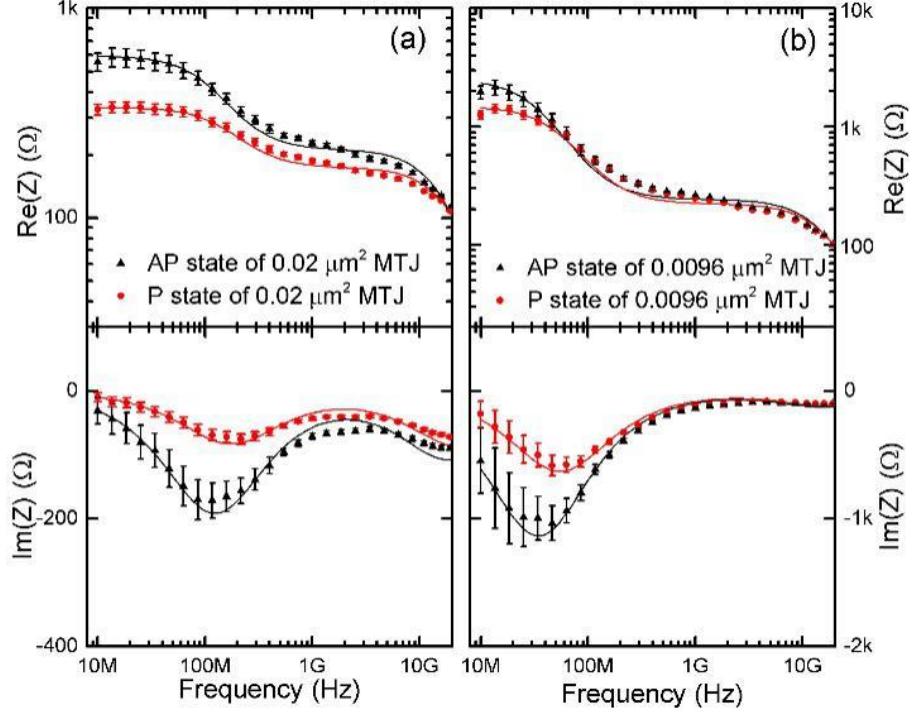
Figure 2.13: Real and imaginary parts (Re(Z) and Im(Z), respectively) of the impedance for two MTJs with different junction areas (a) 0.02 and (b) 0.0096 μm^2 in both AP and P states. The points with error bar denote the experimental data while the solid lines represent the simulation data using the model.

The interfacial capacitance suggests also a few counterintuitive observations. Firstly, by comparing Fig. 2.14(c) and (d) with (e), we can see that the interfacial capacitances C_i extracted for MTJs are much larger than the related geometrical capacitances C_g that can be calculated from parallel-plate capacitor theory: $C_g = \varepsilon_0 \varepsilon_r A / h$, where ε_0 denotes the permittivity of space, ε_r denotes the relative permittivity of MgO that is around 9.7, A is the bit area of junction and h is the thickness of MgO. The same phenomenon has been already reported previously [115-117], while some works [119-121] suggested the measured capacitance should be less than the geometric capacitance in MTJ. Negative interfacial capacitance [115-117] has been introduced to explain the larger observed capacitance. However, the physical mechanism of negative interfacial capacitance is not clear so far. In contrast, positive interfacial capacitance has been demonstrated for aluminum oxide based MTJs [119, 122]. More research needs to be done on the issue of a larger value of measured capacitance compared to geometrical capacitance. Furthermore, contrary to our expectation, the interfacial capacitance is not a monotonic function of bit area.
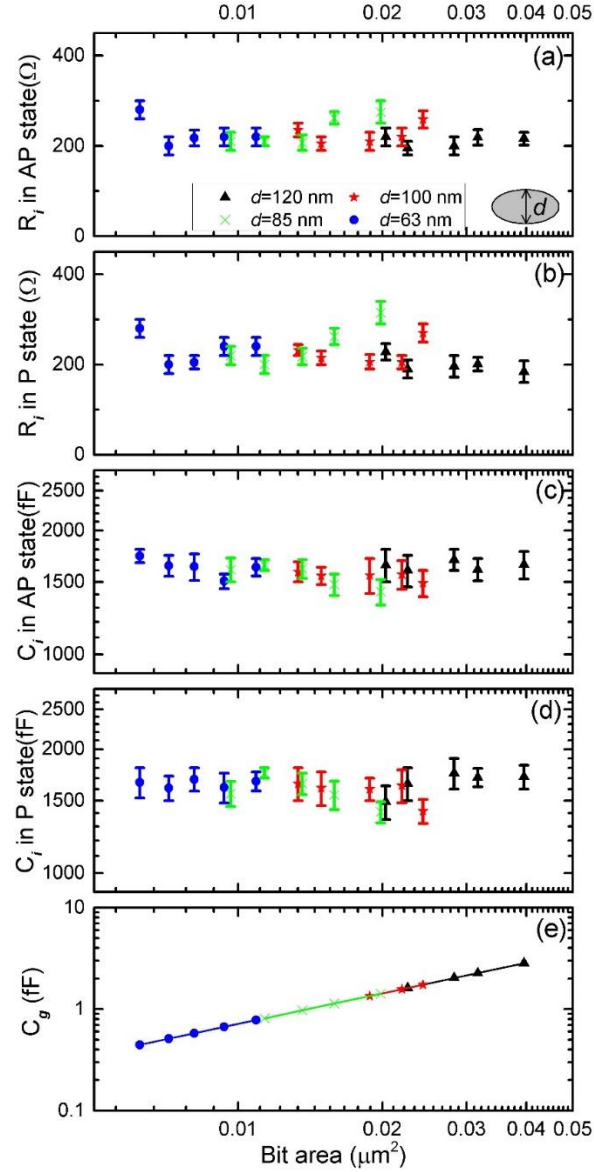
Figure 2.14: (a) - (d) Parametric study of interfacial resistance and interfacial capacitance with error bar in both AP and P state. (e) Calculated geometrical capacitance for all of the samples with different bit area. Circle and cross denote the samples with short axis 63 nm and 85 nm, respectively, while star and triangle denote the samples with short axis 100 nm and 120 nm, respectively.

2.3.1.4 Test pads effect extraction

The 3-D electromagnetic model of the test pads has been built in 3-D full wave simulation software High Frequency Structural Simulator (HFSS) based on the physical structure, while the equivalent

circuit model has been built in ADS. As shown in Fig. 2.15(a) and (b), test pads are patterned as GSG mode in order to be tested easily using a GSG probe, and the equivalent circuit can be simplified as a low pass structure consisting of a series inductor L_p and a shunt capacitor C_p. The inductance comes from the leads, and the capacitance comes from the narrow gap where the MTJ is placed. S-parameters used here are to describe the transmission and reflection characteristics of the two-port network. As shown in Fig. 2.15(c), the parameters of test pads can be extracted when similar results are obtained from the simulation in HFSS and ADS, and the extracted L_p and C_p are 30 pH and 35 fF, respectively.
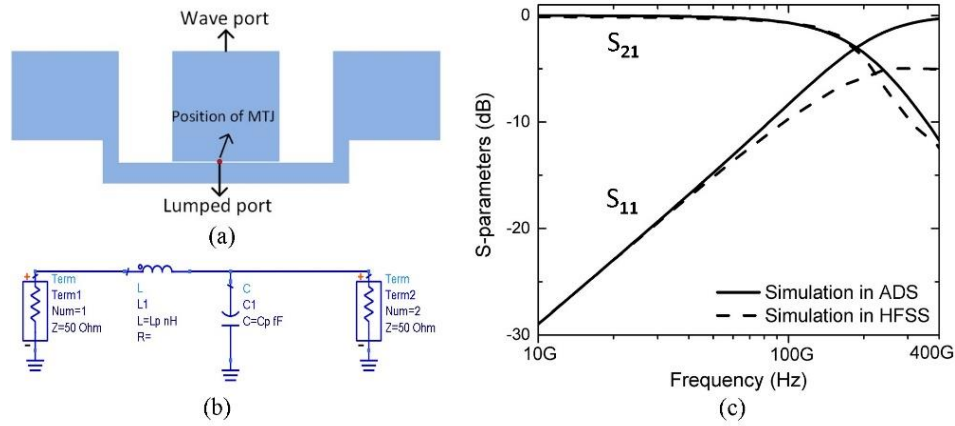
Figure 2.15: (a) 3-D electromagnetic model of test pads, in which the wave port is defined as port 1, and the lumped port is defined as port 2. (b) Equivalent circuit model in ADS. (c) Comparison of S-parameters from two simulations.

2.3.1.5 Nonlinear model extraction and validation

There are two kinds of rectifications involved in MTJs: non-resonant rectification operating as a classical nonlinear device due to the nonlinearity of current-voltage characteristic, and resonant rectification due to spin-torque-driven ferromagnetic resonance (ST-FMR) [31]. The resonant rectification voltage in our experiment is ignorable comparing to the non-resonant rectification in both AP and P states. So, we focus on the non-resonant rectification in the absence of external magnetic field. The physical mechanisms of non-resonant rectification include tunneling effect, spin mixing [9], and Seebeck effect [123] which can generate a dc voltage due to the temperature gradient crossing the MTJ junction. The effects of all the mechanisms are involved in the second term of (2.18). The nonlinear aspects of the model are extracted from Current-Voltage

characteristic measurement and non-resonant rectification measurements. In this part, both the uncertainty from VNA and volt-meter are taken into consideration.

Input reflection coefficient was being constantly monitored during the rectifying operation. It is very valuable information that allows to retrieve the input impedance of the device, but also to know what quantity of the input power effectively enters the device. To enhance the accuracy of the device characterization, a nonlinear VNA (NVNA) could be used to operate a calibrated measurement of the reflected energy at harmonic frequencies. However, in this work, basic S_{11} results are enough to describe the main frequency behavior of the nonlinear device. The matching efficiency denotes the proportion of power that is injected into the MTJ, and can be simply calculated as:

$$\eta_M = 1 - |S_{11}|^2 \tag{2.20}$$

The nonlinearity of the current-voltage characteristic of MTJs, early reported by Julliere [124], is responsible for the non-resonant rectification. As a figure of merit to represent the nonlinearity, the matched voltage sensitivity γ_M is defined as the ratio of the rectified dc voltage to the input RF power [125]:

$$\gamma_M = V_{rect} / (P_{RF} \eta_M) \tag{2.21}$$

where V_{rect} is the rectified voltage, and P_{RF} is the RF power from the VNA source. $P_{RF}\eta_M$ represents the power that is delivered to the MTJ. The matched voltage sensitivity indicates how much dc voltage will be generated per unit power. Fig. 2.16 (a) shows the matched voltage sensitivity of the 0.02 μm^2 MTJ sample, as can be seen that the sensitivity in AP state is higher than in P state because of its stronger nonlinearity.

The parasitic effect can be seen on the stacked area chart of power distribution for the 0.02 μm^2 MTJ sample given in Fig. 2.16(b). The data presented in the figure are obtained from a harmonic balance (HB) simulation in electronic design automation software ADS. As frequency increases, the matching between the source and the MTJ improves as a result of the drop of impedance, resulting in more power is injected into MTJ. Nonetheless, less power is delivered to R$_j$ at high frequencies and more power is dissipated in the series resistance R$_s$ and interfacial resistance R$_i$. At high frequency, the interfacial capacitance presents a low impedance path for the signal, and the

lower impedance at R_i and C_i path compared to R_j path gives rise to less power go through R_j. Fig. 2.16(b) reveals the decrease of microwave current injected into the junction resistance due to parasitic effect, leading to the drop of rectified voltage as well as voltage sensitivity that is shown in Fig. 2.16(a). The nonlinear parameters are extracted from the current-voltage measurements and validated by the non-resonant rectification measurements.
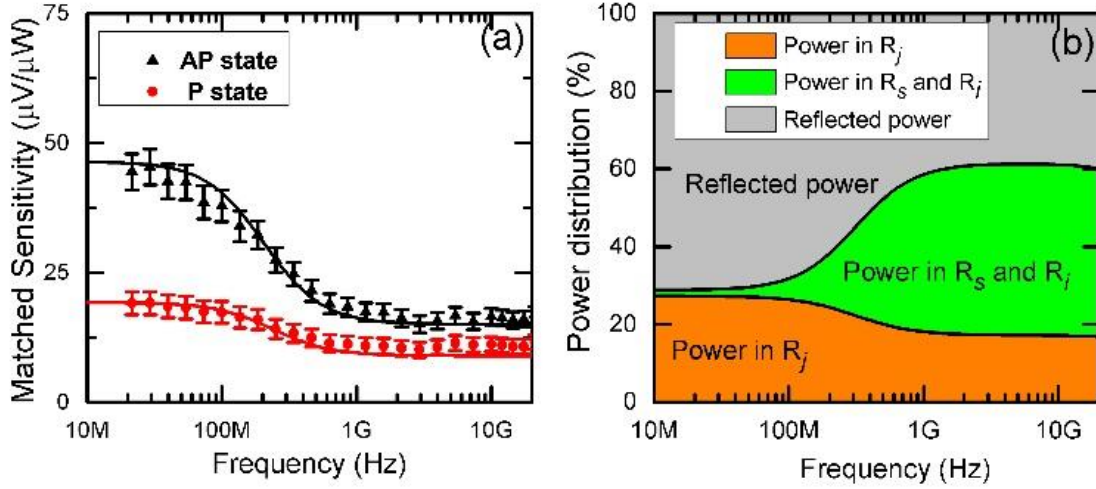
Figure 2.16: (a) Matched sensitivity calculated from measurement of rectified voltage and injected power, considering the uncertainty from VNA and volt-meter. (b) Stacked area chart of power distribution analysis for the 0.02 μm^2 MTJ sample, the gray part stands for the power reflected towards the generator, the orange part represents the power passing through the nonlinear junction resistance and the green part represents the power consumed in the series resistance R_s and interfacial resistance R_i.

The non-resonant rectification measurements were done under a small RF signal condition, the effects of parasitic parameters can be summarized using the parasitic factor metric that can be calculated as [126]: $k = \gamma_M / \gamma_0$, while γ_0 indicates the voltage sensitivity when frequency tends to zero hertz. This factor is a key parameter to describe the efficiency of the MTJ used in microwave applications. It indicates how much the parasitic parameters affect the frequency-dependent performance of the MTJ, while no effect is observed at low frequencies (k = 1). The extracted parasitic factor for the 0.02 μm^2 MTJ sample in both AP and P states are shown in Fig. 2.17, as can be seen that the simulation based on the equivalent model agrees well with the measurement except the small difference at high frequencies, and less sensitive to parasitic parameters is seen in P state compared to AP state.
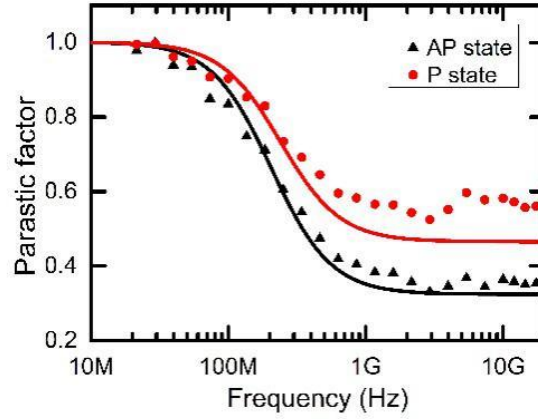
Figure 2.17: Extracted parasitic factor is used to evaluate the performance of MTJs at microwave frequencies. The points denote the experimental data of the 0.02 μm^2 MTJ sample while solid lines are from simulation using the equivalent model.
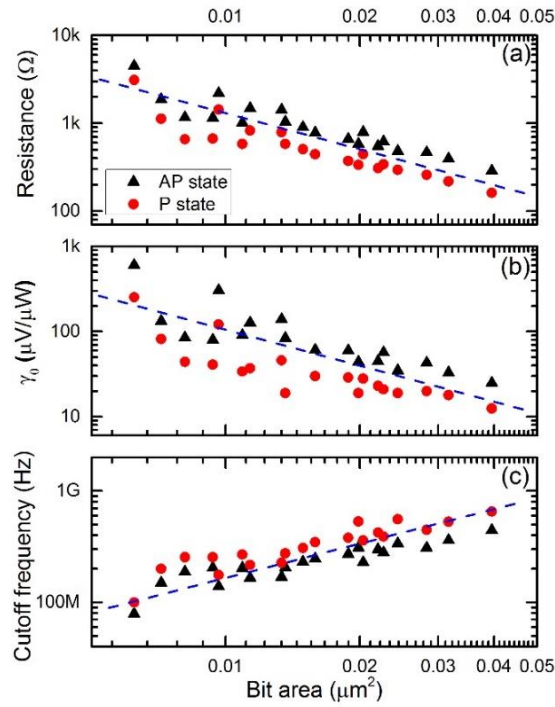
Figure 2.18: Analysis of (a) junction resistance (b) voltage sensitivity when frequency tends to zero hertz, and (c) 3 dB cutoff frequency for all of samples in both AP and P state. The points are from measurements, the blue dash line is just a guide for the eyes.

To give a full parametric study, the junction resistance and voltage sensitivity γ_O are also presented with different bit area. As shown in Fig. 2.18(a), junction resistance of MTJ is inversely proportional to bit area. Fig. 2.18(b) shows that the voltage sensitivity is higher in AP state than in P state, and the sensitivity decreases as bit area increases. Since γ_O is proportional to the curvature coefficient $d^2i / dv^2 / (di / dv)$, the nonlinearity in AP state is stronger than in P state, and smaller bit area MTJ has stronger nonlinearity.

2.3.1.6 Cutoff frequency derivation

Cutoff frequency is an essential metric to quantify the maximum operation frequency of devices and circuits. The 3-dB cutoff frequency is defined as the frequency boundary at which energy flowing through junction resistance reduces to half of the energy injected into the MTJ. After this frequency, the performance of the MTJ degrades dramatically.
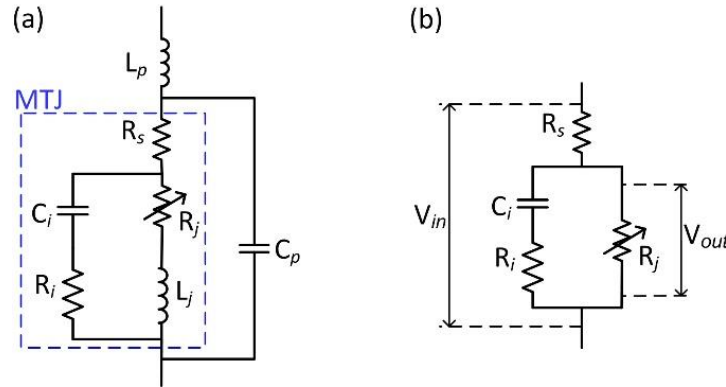
Figure 2.19: (a) Complete model for MTJ including test pads effect. (b) Simplified model in order to analyze cutoff frequency.

Since L_j, L_p and C_p only have impact on frequency beyond 50 GHz, they can be ignored when we analyze the cutoff frequency that is in the range of hundreds of MHz. As shown in Fig. 2.19 (b), V_{in} denotes the voltage across the MTJ while V_{out} denotes the voltage across the junction resistance. The input impedance of MTJ Z_{in} and the relationship of V_{out} and V_{in} can be expressed as:

$$Z_{in} = R_s + \frac{R_j(R_i + 1/ j\omega C)}{R_j + R_i + 1/ j\omega C} \tag{2.22}$$

$$H = \frac{V_{out}}{V_{in}} = \frac{R_j(R_i + 1/ j\omega C)}{R_j + R_i + 1/ j\omega C} / Z_{in} \tag{2.23}$$

Then the injected power and the power that goes through junction resistance can be obtained:

$$P_{in} = \mathrm{Re\,al}(\frac{1}{2}V_{in} \cdot I_{in}^*) = \mathrm{Re\,al}(\frac{1}{2}V_{in} \cdot \left(\frac{V_{in}}{Z_{in}}\right)^*) = \frac{V_{in}^{\,2}}{2}\mathrm{Re\,al}(\frac{1}{Z_{in}^*}) \tag{2.24}$$

$$P_{out} = \mathrm{Re\,al}(\frac{1}{2}V_{out} \cdot I_{out}^*) = \mathrm{Re\,al}(\frac{1}{2}V_{out}^{\,2} \cdot \frac{1}{R_j}) = \frac{V_{in}^{\,2}}{2R_j}\mathrm{Re\,al}(H^2) \tag{2.25}$$

where we consider V_{in} as a real value in order to simplify the calculation. According to the definition of 3 dB cutoff frequency, we can express the power ratio as:

$$\frac{P_{out}}{P_{in}} = \mathrm{Re\,al}(\frac{1}{Z_{in}^*})/(\frac{\mathrm{Re\,al}(H^2)}{R_j}) = \frac{1}{2} \tag{2.26}$$

The 3-dB cutoff frequency $\omega/2\pi$ can be obtained by solving the above equation. Since the calculation is complicated, we did not show the final expression of 3-dB cutoff frequency here.

As shown in Fig. 2.18(c), the 3-dB cutoff frequency for all our samples is between 80 and 650 MHz, we believe that the high interfacial capacitance is responsible for this limitation. On the other hand, contrary to a typical microwave device that has a cutoff frequency decreasing with higher area, in the MTJ the cutoff frequency increases as bit area increases, which means MTJs with higher bit area or lower junction resistance are less sensitive to parasitic parameters and then can be applied at higher frequency. It also can be seen that cutoff frequency in P state is higher than in AP state.

In fact, due to the current divider nature of the MTJ equivalent circuit, the interfacial resistance is limiting the current flowing through the parasitic capacitance C_i. Therefore, R_i could be engineered in the future design to improve the parasitic factor. Increasing the unbalance between spin up and spin down should increase the interfacial resistance, which in turn, would allow the operation of Spintronics devices at higher frequency.
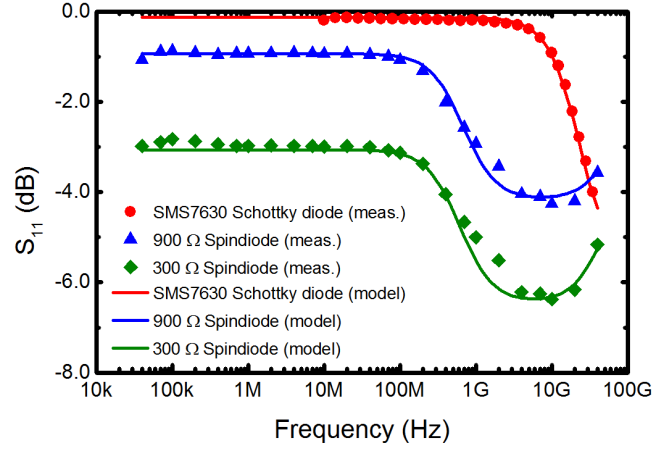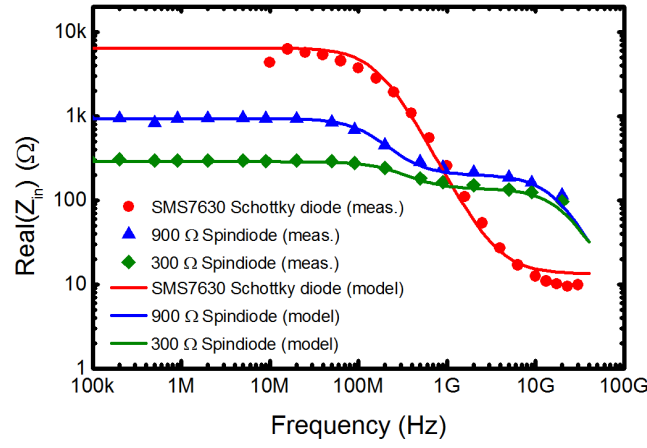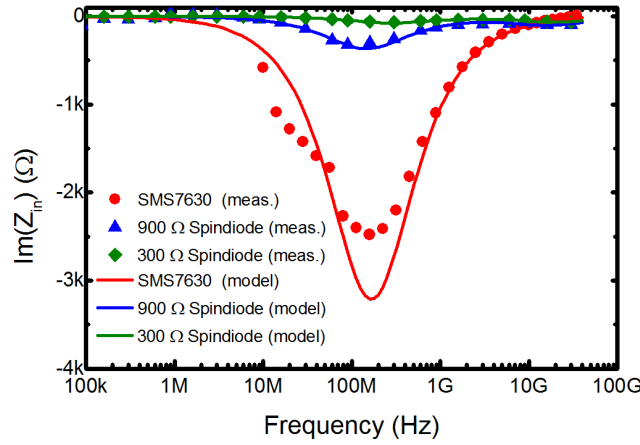
Figure 2.20: Comparison of (a) S_{11}, (b) real part and (c) imaginary part of impedance between two spindiodes with different junction resistances and a commercial SMS7630 Schottky diode. During measurement, power entering the nonlinear device was kept below – 40 dBm.

2.4 Comparison of Schottky diode and spindiode

2.4.1 Comparison of parasitic factor and parasitic components

Input reflection coefficients (referenced to 50 Ω) for one SMS 7630 diode and two spindiodes having different pillar section are plotted in Fig. 2.20(a). As expected, due to a lower ZBR, more RF power enters the spin-devices. As it can be seen in Fig. 2.20(b) and (c), the impedance varies much less than in the case of the Schottky diode, especially for low ZBR MTJ. The spindiode will then support higher efficiency, wider band matching capability than the Schottky diode.

The parameters given in Table 2.2 are extracted from the impedance measurements. Interfacial resistance R_i that reduces the low pass effect of the junction capacitance is another advantage of spindiode over Schottky diode for high frequency operation. A nice example can be seen in Fig. 2.21 with the measured parasitic efficiency. At high frequency, the Schottky diode curve decreases abruptly, but the slope of the spindiode is small and even becomes positive. The direct conclusion of this fact is that the low pass filter's cut-off frequency commonly used is not a good criterion to describe the capabilities of the spindiode as rectifying devices. As expected, the junction resistance has a strong impact on the parasitic losses, and a low ZBR provides a better efficiency, even for wider area sample, like the 300 Ω device in Fig. 2.21.
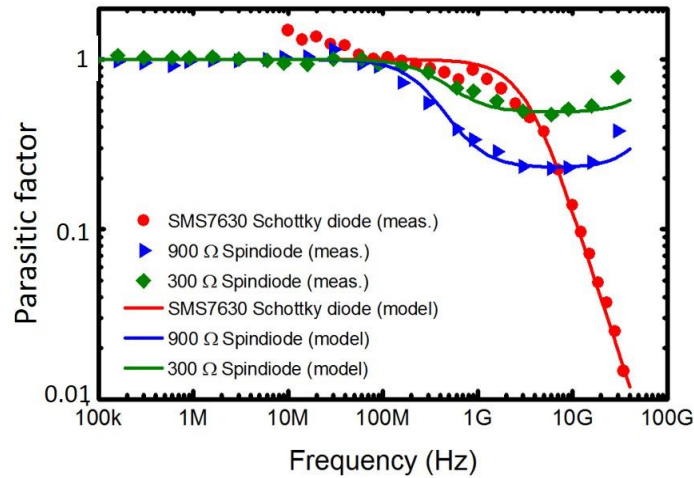
Figure 2.21: Efficiency related to the parasitic losses. Data shown are calculated as the square of measured responsivity, normalized to low frequency value, with a compensation of insertion losses.

Table 2.2: Value of equivalent model elements shown in Fig. 2.12.

Symbol	COMMENT	SMS7630 Schottky diode	900 Ω spindiode	300 Ω spindiode
C_p	Package capacitance	--	35 fF	35 fF
L_p	Package inductance	0.35nH	0.01 nH	0.01 nH
L_j	Junction inductance	--	0.275nH	0.14nH
R_s	Series resistance	20 Ω	1 Ω	1 Ω
C_j	Junction capacitance	90 fF	10 fF	20 fF
R_i	Interfacial resistance	--	272 Ω	272 Ω
C_i	Interfacial capacitance	--	0.88 pF	1 pF
a	Coefficient for $I_j = (V_j)$	--	4.9e-3	2.55e-3
b	Coefficient for $I_j = (V_j)$	--	2.84e-4	4.73e-5
c	Coefficient for $I_j = (V_j)$	--	2.39e-3	1.04e-3
$\Re_0$	Zero-bias Responsivity	100 mV/µW	128 µV/µW	47 µV/µW
ZBR	Zero-bias Junction Resistance	7000	890 Ω	280 Ω
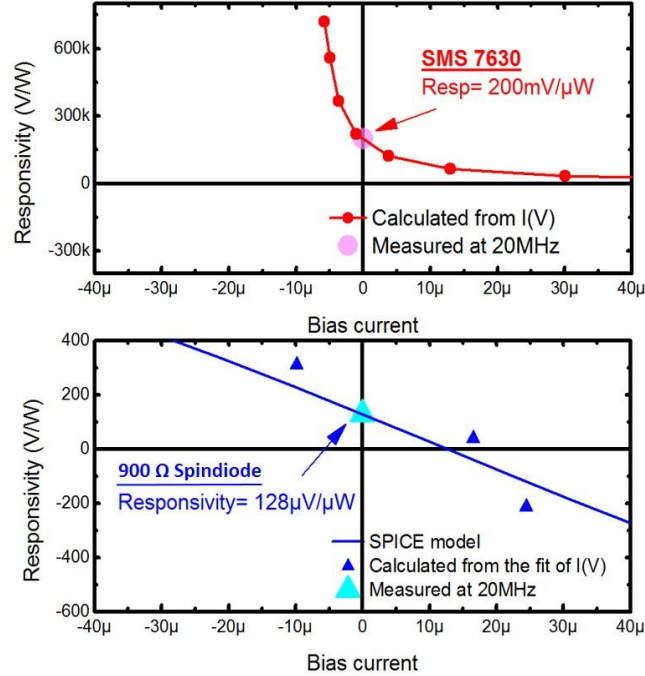
Figure 2.22: Calculated dc responsivity from I(V) measurements results. The point located at zero-bias indicates a low frequency low power measurements to validate the responsivity extraction.

2.4.2 Comparison of responsivity

As described in section 2.1, the responsivity can be used to evaluate the device nonlinearity. Fig. 2.22 compares responsivity values calculated from the I(V) curve for a 900 Ω spindiode and for the SMS7630 Schottky diode. For verification purpose, the responsivity is measured directly from a low RF signal of 20 MHz. There are about 3 orders of magnitude of difference between the two technologies. That may seem an extremely large ratio, but it should be noted that the nonlinearity of Schottky diode is a result of more than 40 years of development, and that the MTJ investigated in this work is in fact a MRAM bit, operating as a spindiode, but optimized only for memory applications.

2.5 Discussion of capability of spindiode rectification

With their scalable ZBR capabilities, the spindiodes are very promising devices for low power rectification with high-efficiency, but also for low power mixer applications. Unfortunately, the spindiode sample measured in this work does not have enough nonlinearity to be used for a practical rectifier demonstration. However, a proper diode design should lead to a significant improvement of the RF-to-dc conversion efficiency. The magnetic stack deposition process is also a key element that could be optimized in several ways. For example, the tunnel barrier could be optimized to enhance the nonlinearity, and consequently the sensitivity [127]. The MTJ ferromagnetic resonance could also be adjusted to coincide with the input signal frequency. In this configuration, the low nonlinearity of the spindiode would be compensated by an enhanced magnetic susceptibility. A recent work presented conditions to obtain a 500 Ω magnetic tunnel junctions having a sensitivity of about 10000 mV/mW [128]. This factor combined with the improvement in parasitic losses would lead to a surpass of the current Schottky diodes (which do not have any room for improvement).

Although the model in Fig. 2.12 works up to 20 GHz, complex model (Fig. 2.23) could be used for up to 40 GHz [129]. Fig. 2.24 shows the low power efficiency

$$\eta_M = \Re_I^2 \cdot P_{in} \cdot \frac{R_j}{4} \cdot \eta_p \tag{2.27}$$

calculated using the dc value of the current responsivity $\Re_I$ and the parasitic efficiency data measured at 30 GHz. As stated earlier, the MTJ samples measured here would not provide a

satisfying low power efficiency, but following the projection of [128], the spindiode can surpass the diode, therefore paving the way for a bright future for low RF and microwave power harvesting and rectification with high-efficiency. In particular, millimeter-wave to dc rectification will benefit from the special features of spindiodes.
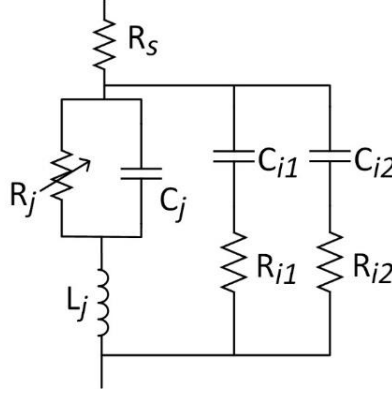
Figure 2.23: Complex model of MTJ [129].
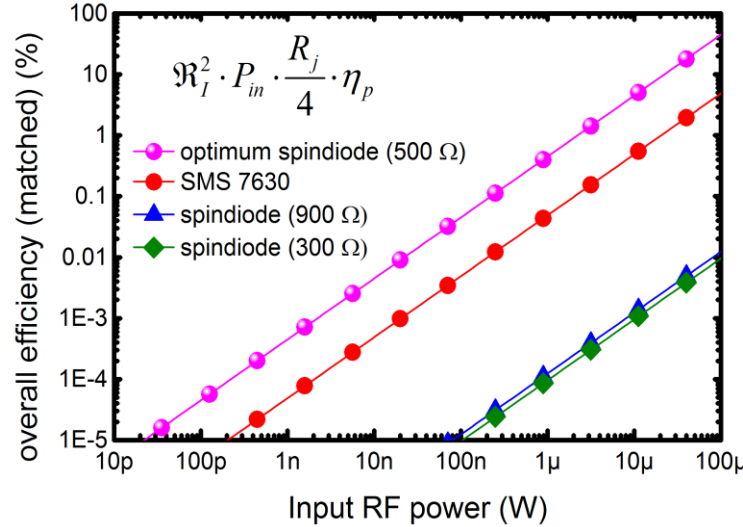
Figure 2.24: Low power diode efficiency under the matched conditions and the load condition $R_j = R_L$. Data were calculated based on the measurement of responsivity, ZBR and parasitic efficiency at 30 GHz.

2.6 Conclusion

This present work has highlighted electrical and physical behaviors and limitations of the Schottky-based low power RF-to-dc rectifiers. It has been shown that MPH circuits based on spindiodes are

a promising alternative. Besides, this work shows the role of the nonlinearity as well as the value of the zero bias resistance in the RF-to-dc power conversion. Detailed analysis and modeling are carried out to suggest the advantageous features of spindiodes as the next generation of active devices for RF and microwave rectifications and other nonlinear applications. The concluding remarks have been supported by theoretical and experimental results as well as physical explanations and discussions.

CHAPTER 3   NEGATIVE RESISTANCE-BASED ELECTRONIC IMPEDANCE TUNER

Negative resistance can manifest in some electronic devices or circuits, such as tunneling diode, Gunn diode, IMPATT diode, transistor and operational amplifier with feedback, etc. The intrinsic amplification has been applied in PA and oscillator [130, 131]. As a matter of fact, the negative resistance can also to be used in electronic impedance tuner to compensate the inner insertion loss and therefore enable the reflection coefficient up to the full unity.

In RF characterization systems, electronic tuner is most often found in niche market, as compared with its electromechanical and active counterparts, although it has advantages of small size, low cost and fast tuning. In fact, the realizable maximum reflection coefficient is systematically limited by its large insertion loss [132]. To reach a larger reflection coefficient, one has to compensate the loss by an amplification. A reflection coefficient larger than one means that the reflected signal is somewhere amplified by the circuit. From the standpoint of impedance, this implies that the signal has to be reflected by a negative resistance.

The main contribution of this work is to use the amplification property of a negative resistance device to compensate the loss stemmed from an electronic tuner. Somehow it is similar to an active tuner, but it is more cost-effective due to its simplicity and low power consumption. Interestingly, the very intuitive operation of this circuit could be used for pedagogical purposes.

3.1 Principle of negative resistance-based tuner

The proposed topology includes a wideband phase shifter and an impedance tuning circuit (Fig. 3.1), in which port 2 is usually connected to 50 Ω, while port 1 presents different impedance states. As depicted in the ideal circuit (Fig. 3.2(a)), the core part is a shunt tunneling diode and a series PIN diode. The tunneling diode is biased to the level that presents a negative resistance ($-R_{TD}$). The PIN diode is forward-biased in order to provide a variable positive resistance (R_{PIN}).

Without considering any parasitic effect, this topology generates a set of impedance points by a negative resistance in parallel with an equivalent positive resistance (R_{eq}) after considering the 50 Ω port effect (Fig. 3.2(b)). The total resistance can be calculated by $-R_{TD} \cdot R_{eq} / (R_{eq} - R_{TD})$. Ideally, when R_{eq} is swept from low resistance (e.g. 50 Ω) to high resistance (e.g. 600 Ω), as illustrated in

Fig. 3.2(c), the generated impedance points will be distributed from center to open circuit, then to outside of Smith chart (negative resistance region).
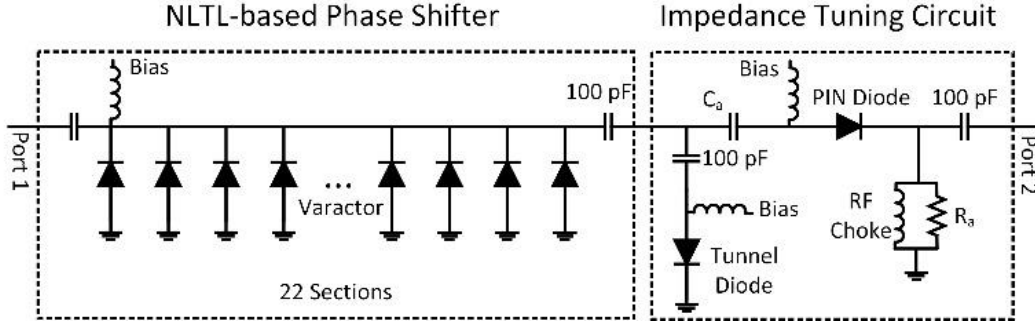
Figure 3.1: Diagram of electronic tuner: it consists of a wideband NLTL-based phase shifter and an impedance tuning circuit.
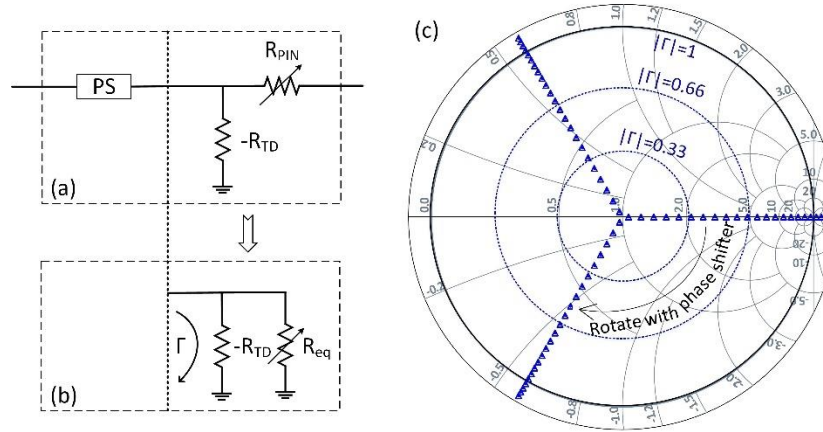
Figure 3.2: (a) Ideal circuit of the proposed topology; (b) Simplified circuit to generate impedance values; (c) Operation principle illustrated on Smith chart.

One criterion to evaluate the electronic tuner is Smith chart coverage [82], a simple way to improve the coverage is to use a 360° phase shifter before the impedance tuning circuit. As shown in Fig. 3.2(c), the set of impedance points generated by the impedance tuning circuit will be rotated by the 360° phase shifter. With the advantages of broadband, easy impedance matching and low loss, nonlinear transmission line (NLTL) technique is a good solution for controlling the phase shift over a wide frequency range.

However, the tunneling diode and PIN diode are not pure resistances, parasitic parameters can not be ignored over the GHz frequency range. The consequence is that the impedance distribution would be distorted. Therefore, two adjusting components, C_a and R_a, can be presented in the

impedance tuning circuit in order to adjust the impedance distribution (Fig. 3.1). The values will be determined according to the operation frequency range as well as the impedance distribution on Smith chart.

3.2 Modeling of tunneling diode and PIN diode

Since parasitic parameters from device and connection pads have impact on the impedance, accurate models of tunneling and PIN diodes should be established prior to the design. A behavioral model, more relevant in field operation, is developed from I(V) characteristic and C(V) characteristic as well as measured S-parameters.

It is important to mention that the I(V) curve of the tunneling diode is measured with a known positive resistor in parallel with it, in order to avoid unexpected oscillation and irregular discontinuity in the I(V) curve [133]. In Fig. 3.3(a), the equation of the I(V)curve of the tunneling diode is expressed in a Symbolically Defined Devices (SDD) model. 7th order polynomial is applied to fit the measured I(V) curve that is shown in Fig. 3.3(b)

$$
\begin{aligned}
i(\mathrm{v}) = & -1.5e - 5 + 0.01879 \cdot v - 0.18638 \cdot v^2 + 0.15171 \cdot v^3 + \\
& 7.16518 \cdot v^4 - 45.47 \cdot v^5 + 110.9539 \cdot v^6 - 97.13563 \cdot v^7
\end{aligned}
$$

(3.1)

The derivation of the I(V) equation is also shown in Fig. 3(b). As it can be seen, the resistance remains -409 Ω in the bias range of 0.1 to 0.25 V. Parasitic parameters inductance L_s (0.7 nH) related to the long lead, series resistance R_s (0.3 Ω), and total capacitance C_T (0.1 pF) are extracted from S-parameters measurements. It is worthwhile to note that there is still no proper model that can represent the RF characteristics of a tunneling diode. The parasitic parameters of tunneling diode extracted in this work are only approximate.

So far there is no accurate SPICE model for PIN diode, mainly because it shows distinct features under reverse and forward bias conditions. A PIN diode under forward bias condition can be modeled as a current-controlled series resistance with a parasitic inductance (Fig. 3.4(a)). The series resistance can be extracted from S-parameters measurements under different biases. As depicted in Fig. 3.4(b), the PIN diode can be considered as a variable RF resistance from a few Ω to hundreds Ω when current is swept from μA to mA level. However, it should be mentioned that a precise bias source is required. The parasitic inductance is dependent on the package, which is 0.7 nH for SMP1320 with package of SC-79.
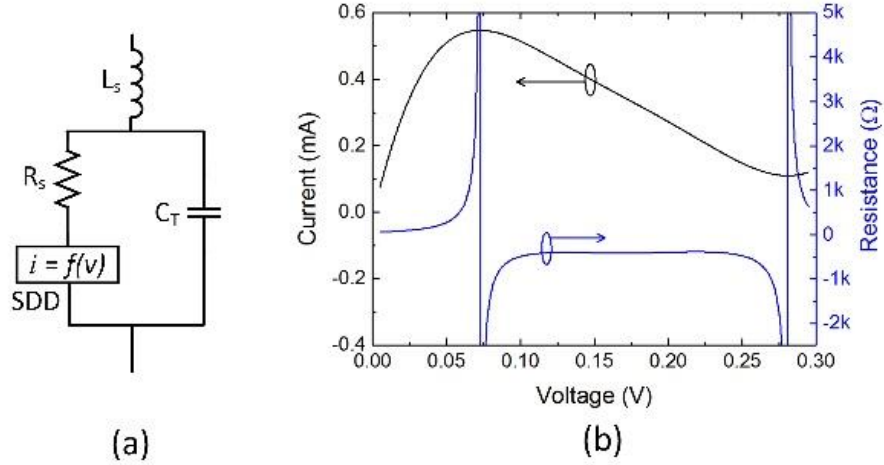
Figure 3.3: (a) Tunneling diode model with Symbolically Defined Devices (SDD), (b) I(V) curve and extracted resistance of tunneling diode MBD5057-E28X from MACOM Technology Solutions.
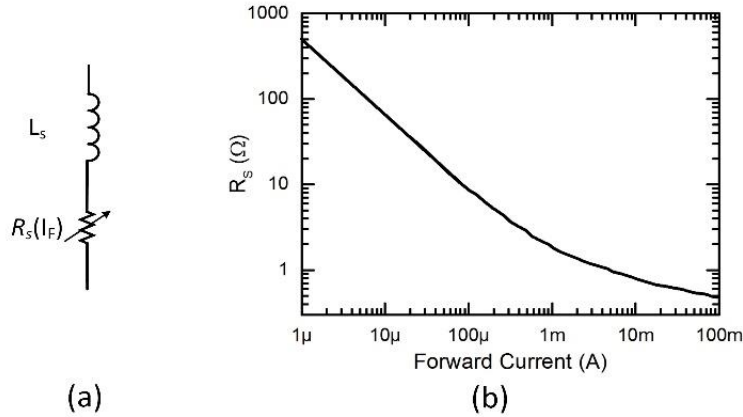
Figure 3.4: (a) SPICE model for PIN diode under forward bias; (b) Equivalent series resistance Rs of PIN diode SMP1320 from Skyworks Solutions Inc.

3.3 Design of NLTL-based phase shifter

3.3.1   Theory of NLTL-based phase shifter

Fig. 3.5 shows the LC model of unit cell of NLTL, C_d is the capacitance of varactor, L_t and C_t are equivalent inductance and capacitance of the transmission line. The unloaded characteristic impedance of the transmission line can be expressed as

$$Z_0 = \sqrt{\frac{L_t}{C_t}} \qquad (3.2)$$

The loaded characteristic impedance of the NLTL is

$$Z_L = \sqrt{\frac{L_t}{C_t + C_d}} \qquad (3.3)$$
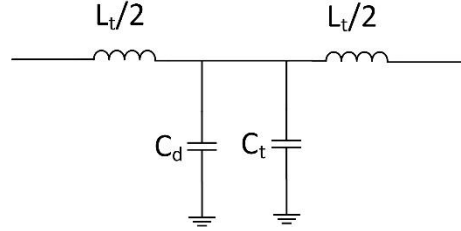
Figure 3.5: LC model of unit cell of NLTL.

It means the impedance of NLTL is also a real value, so that it is easy to realize a wideband impedance matching. In order to remain a wideband matching when tuning the capacitance of varactor from the minimum C_{dmin} to the maximum C_{dmax}, usually the impedance of NLTL at a middle point $a \cdot C_{dmax}$ is set as 50 Ω (a is coefficient), so that the matching at both C_{dmin} and C_{dmax} conditions are reasonable. The middle point $\alpha \cdot C_{dmax}$ is usually chosen as large signal capacitance, however, it is not the optimized case since the phase shifter is a small signal application. The coefficient α can be optimized in simulation according to the tuning range of the varactor. In this work, $\alpha = 0.5$ is chosen.

Define the loading factor as

$$x = \frac{C_{dmax}}{C_t} \qquad (3.4)$$

Then the loaded impedance at middle point can be written as

$$Z_L = \sqrt{\frac{L_t}{C_t + aC_{dmax}}} = \sqrt{\frac{L_t}{C_t + axC_t}} = \sqrt{\frac{L_t}{C_t(1 + ax)}} = \frac{Z_0}{\sqrt{1 + ax}} = 50 \qquad (3.5)$$

It can be rewritten as

$$Z_0 = 50\sqrt{1 + ax} \qquad (3.6)$$

The transmission line can therefore be designed from the unloaded impedance Z_0, afterwards the equivalent permittivity ε_{reff} can be calculated [23].

According to the Floquet analysis in Chapter 1, the lowest cutoff frequency $f_{Bragg}|_{min}$ can be calculated at the condition of C_{dmax}

$$f_{Bragg}\,|_{min} = \frac{1}{\pi\sqrt{L_t(C_t + C_{d\,max})}} = \frac{1}{\pi\sqrt{L_t(C_t + xC_t)}} = \frac{c/\sqrt{\varepsilon_{reff}}}{\pi d\sqrt{1+x}} \tag{3.7}$$

Then we have

$$d = \frac{c/\sqrt{\varepsilon_{reff}}}{\pi\sqrt{1+x}\,f_{Bragg}\,|_{min}} \tag{3.8}$$

After calculating the distance per section, the equivalent inductance and capacitance of the transmission line can be calculated by the distance and unloaded phase velocity v_{p0} [52]

$$L_t = \tau Z_0 = \frac{d \cdot Z0}{v_{p0}} \tag{3.9}$$

and

$$C_t = \frac{d}{Z_0 \cdot v_{p0}} \tag{3.10}$$

where $v_{p0} = c/\sqrt{\varepsilon_{reff}}$. Then the relationship between the maximum capacitance C_{dmax} and loading factor x can be calculated from (3.4), which can be used as a criterion to choose a proper commercial varactor.

Let us define the ratio of the maximum capacitance C_{dmax} and the minimum capacitance C_{dmin} of varactor as $y = \frac{C_{d\,max}}{C_{d\,min}}$. Larger y denotes a larger capacitance variation. Then the minimum and maximum phase velocity of NLTL can be calculated as:

$$v_p\,|_{min} = \frac{1}{\sqrt{L_t(C_t + C_{d\,max})}} = \frac{c/\sqrt{\varepsilon_{reff}}}{\sqrt{1+x}} \tag{3.11}$$

and

$$v_p \mid_{\max} = \frac{1}{\sqrt{L_t (C_t + C_{d\min})}} = \frac{c / \sqrt{\varepsilon_{reff}}}{\sqrt{1 + x / y}} \tag{3.12}$$

The time delay per unit can be obtained as:

$$\Delta \tau = \frac{d}{v_p \mid_{\min}} - \frac{d}{v_p \mid_{\max}} = \frac{d}{c / \sqrt{\varepsilon_{reff}}} (\sqrt{1 + x} - \sqrt{1 + x / y}) \tag{3.13}$$

and the phase shift per unit can be calculated as:

$$\Delta \phi = \omega \Delta \tau = 2\pi f \frac{d}{c / \sqrt{\varepsilon_{reff}}} (\sqrt{1 + x} - \sqrt{1 + x / y}) \tag{3.14}$$

Finally, knowing $\Delta \phi$ it is possible to calculate the number of sections required to obtain 360° phase shift:

$$n = \frac{2\pi}{\Delta \phi} \tag{3.15}$$
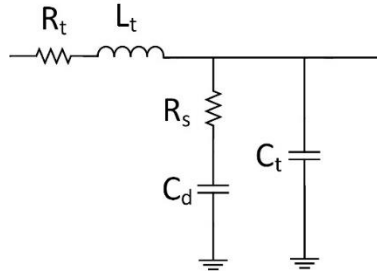
Figure 3.6: LC model of unit cell of NLTL with loss.

To be integrated with impedance tuner, the NLTL-based phase shifter is designed on microstrip line technology. The losses of microstrip line includes dielectric loss, conductive loss as well as radiation loss, in which the first two dominate. Since the conductive loss is much larger than dielectric loss, in this work, we only consider the conductive loss. The analysis of NLTL on Chapter 1 is based on lossless transmission line, by taking the conductive loss of the transmission line and diode loss into consideration, the unit cell model is modified as Fig. 3.6, in which R_t denotes the skin resistance per unit, and R_s represents the series resistance of varactor. Then the loss per unit cell is expressed as [134]

$$\alpha = \alpha_{\mathrm{var}\,actor} + \alpha_{TL} = \frac{\omega^2 C_{d\,\max}^2 R_s Z_L}{2} + \frac{R_t}{2Z_L} \qquad (3.16)$$

where C_{dmax} is used to calculate the largest insertion loss of each varactor. In other words, (3.16) represents the largest loss per unit cell of NLTL. Then the total insertion loss of NLTL can be calculated

$$IL_{total} = \mathrm{n} \cdot \alpha \cdot 8.686 \quad \mathrm{dB} \qquad (3.17)$$
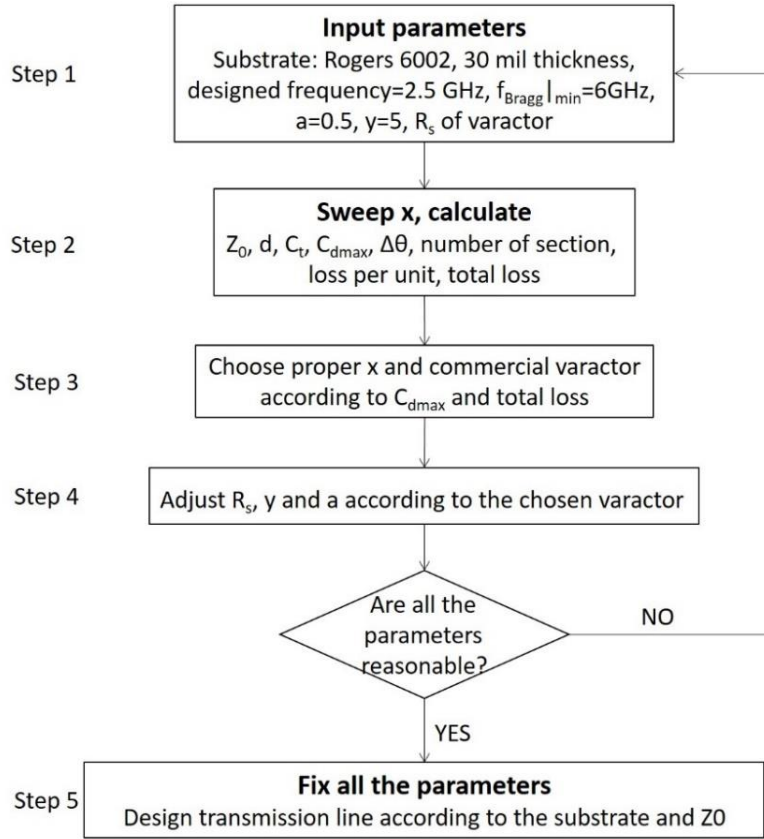
Figure 3.7: Diagram of design procedure of NLTL-based phase shifter.

3.3.2 Design procedure of NLTL-based phase shifter

Based on the design principle of NLTL-based phase shifter in the previous section, the diagram of design procedure is described in Fig. 3.7. The most important step is to choose a commercial varactor according to the calculated C_{dmax}, since there are limited choices. As discussed in Chapter 1, for a true time delay line, the Bragg cutoff frequency will be chosen as 5 times of the highest operation frequency, the time delay is independent of frequencies. However, this may result in a

small *d* as well as small capacitance, which is not easy to realize by PCB technique and commercial varactor. In this work, it is not necessary to have a true time delay for the tuner, since the tuner is for single tone rather than broadband signal. The minimum Bragg cutoff frequency is chosen as 6 GHz at the condition of C_{dmax}.
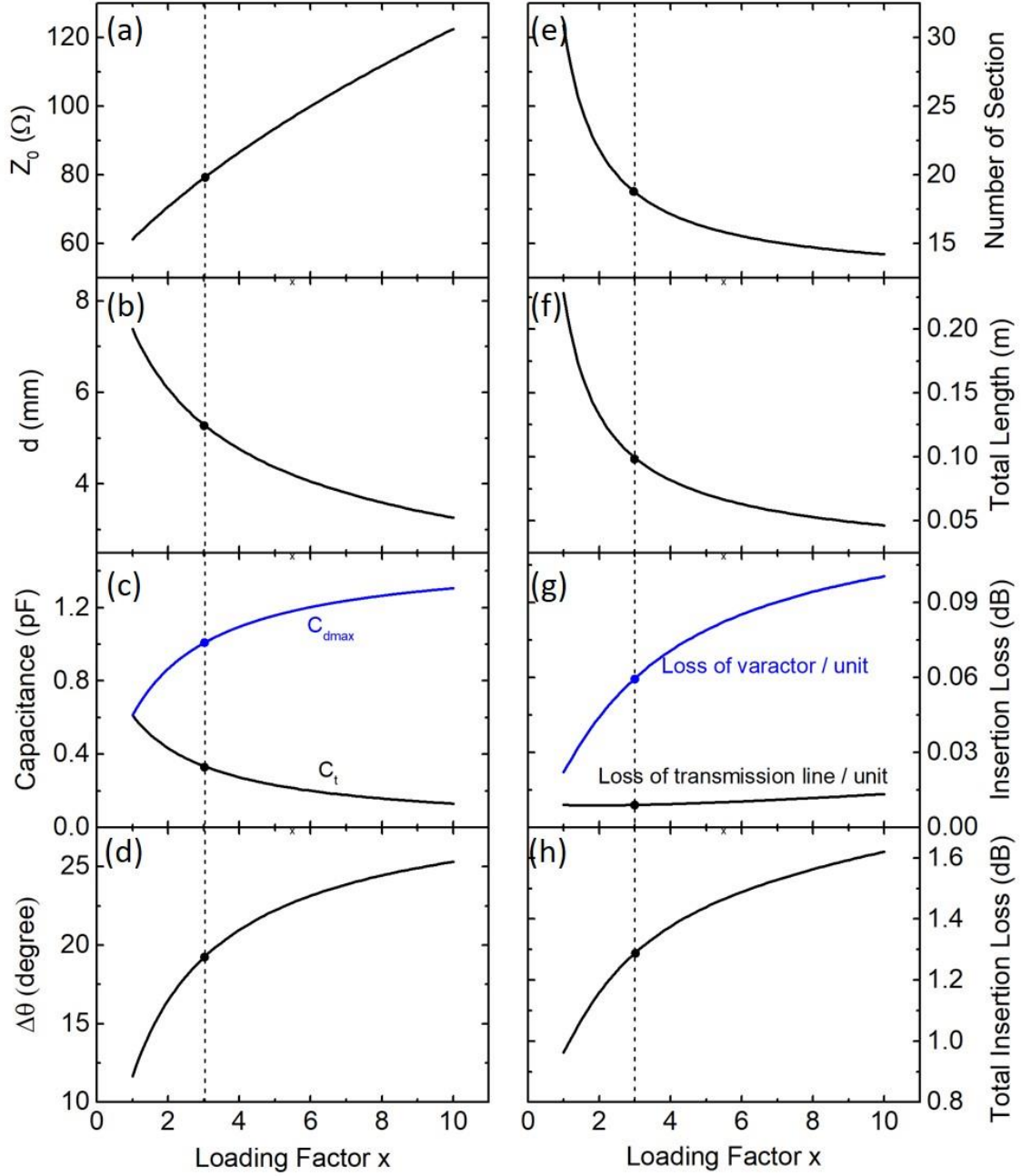
Figure 3.8: Design results of NLTL-based phase shifter.

Following the design procedure in Fig. 3.7, the NLTL-based phase shifter is designed on Rogers 6002 with thickness of 30mil, and the designed frequency is set to 2.5 GHz in order to verify the amount of phase shift. Fig. 3.8 shows the calculated results, and the loading factor x is chosen as 3. As shown in Fig. 3.8(c), the maximum capacitance is around 1 pF, varactor of MA46H120 from MACOM is chosen to provide 0.15 - 1.1 pF capacitance with bias from -15V to 0 V. The distance between every two sections is chosen to be 5.27 mm so as to have a minimum Bragg cutoff frequency of 6 GHz (Fig. 3. 8(b)). Fig. 3.8(d) - (h) are calculated results for the designed frequency 2.5 GHz, as can be seen that the 360° requires 17 sections, in order to have a large phase shift for low frequencies, the number of sections is chosen as 22.

3.4 Validation of the proposed tuner

3.4.1 NLTL-based phase shifter

The fabricated circuit is shown in Fig. 3.9, the long transmission line of phase shifter is bended in order to reduce the total circuit size. Measurement results of the phase shifter are presented in Fig. 3.10. It can be seen that 360° phase shifter is realized at different frequencies with a different voltage tuning range so as to limit the maximum loss to 3 dB. Since the wideband tuning is for single tone signal rather than broadband signal, different bias is not a problem.
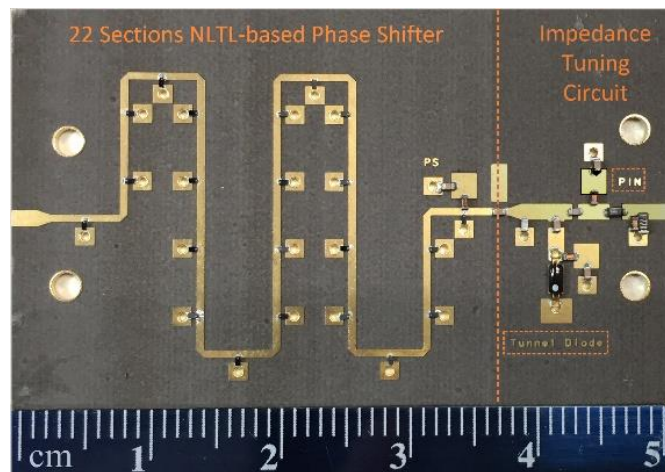
Figure 3.9: Photo of the fabricated electronic impedance tuner.
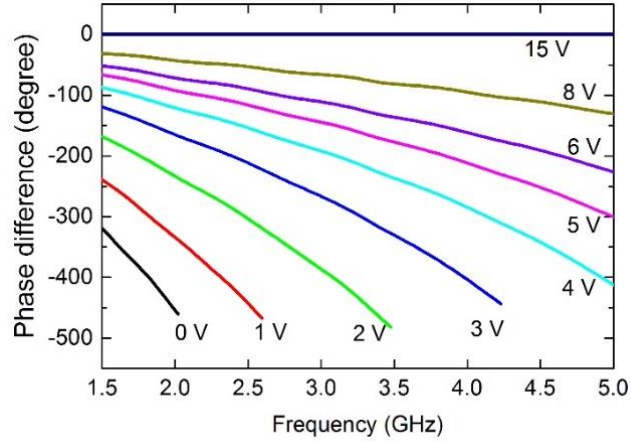
Figure 3.10: Measured phase difference of the NLTL-based phase shifter.
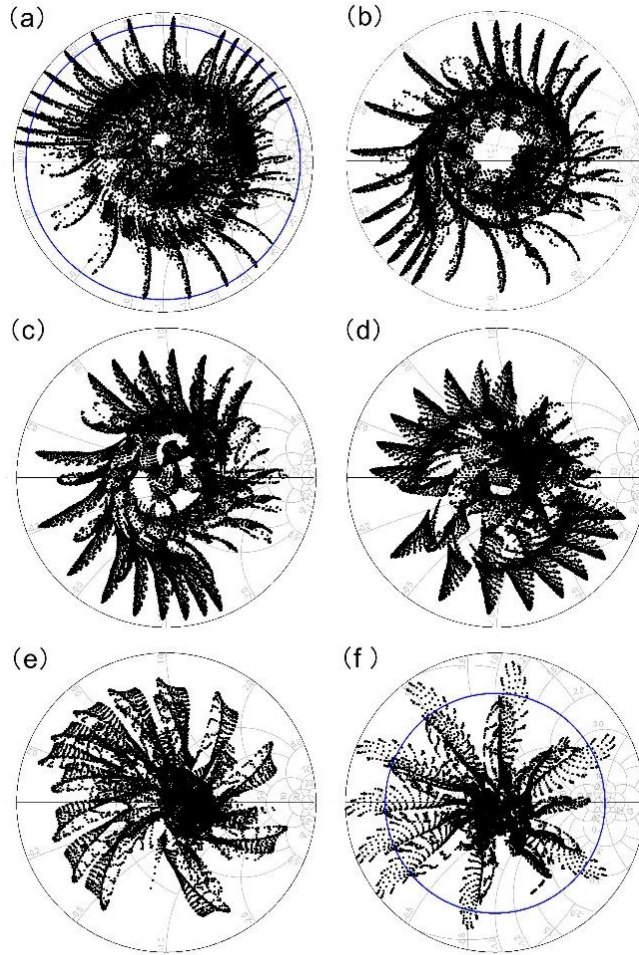
Figure 3.11: Measured 25740 impedance states for the proposed electronic impedance tuner at (a) 1.5 GHz, (b) 2 GHz, (c) 2.5 GHz, (d) 3 GHz, (e) 4 GHZ, and (f) 5 GHz. The blue circle in (a) and (f) stands for the reflection coefficient equals to 1.

3.4.2 Impedance tuner

Ideally, the bias of the tunneling diode could be fixed, and the bias of the PIN diode was swept from 0.3 to 0.8 V while the bias of phase shifter was swept from -15 to 0 V, in order to generate impedance points all over the Smith chart. However, the parasitic parameters distort the impedance distribution, and a fine bias of the tunneling diode becomes necessary (swept from 0.14 to 0.7 V) to adjust the impedance distribution on Smith chart. The adjusting components C_a and R_a are chosen as 1.8 pF and 68 Ω, respectively, to have a better distribution for frequency range 1.5 - 5 GHz.

For an analog tuner, the impedance can be tuned continually. In other words, there are infinite impedance states. 25740 impedance states are tested for each frequency with the automatic test program, and the results for different frequencies are shown in Fig. 3.11. The maximum reflection coefficient Γ is larger than one for 1.5 - 1.9 GHz and 4.5 – 5 GHz, while it is in the range of 0.8 – 1 for other frequencies. The insertion loss of the phase shifter will reduce the maximum Γ generated by the impedance tuning circuit, which means the maximum Γ will decrease after the rotation (Fig. 3.11(a)). However, in practice, we only care about the coverage inside the Smith chart without considering the impedance outside of Smith chart.

The comparison of the proposed electronic tuner with the recent work as well as with conventional mechanical tuner is listed in Table 3.1. The proposed tuner presents the largest maximum Γ compared to other work, which can be used in the noise characterization system for active device with impedance near 0 Ω. It also presents the lowest power consumption, which is mainly consumed by the tunneling diode and PIN diode. Limited by the tunneling diode, the maximum operation power of the proposed tuner is around -25 dBm, which is lower than the MOS FET and PIN diode based electronic tuner and the mechanical tuner. However, this power level still can be used for noise measurement, since the output power of the noise source is always below -50 dBm. Further work can be done to improve the power handling capability. For instance, two transistors and linear positive resistors could be combined to a generate negative resistance that can handle a large power [135].

Table 3.1: Comparison with the state-of-the-art work of electronic impedance tuner.

	This work	[136]	[137]	[138]
Frequency band (GHz)	1.5 - 5	130 - 170	0.3 - 0.8	0.8 - 8
Smith chart coverage	High	Small	High	High
Nonlinear device	Varactor, PIN diode, tunneling diode	MOS FET	PIN diode	Mechanical probe
Maximum Gamma	> 1	0.5	~ 0.87	0.9 - 0.98
Power handling	-25 dBm	8 dBm	> 30 dBm	1414 W
Power consumption	3mW	--	--	--
Loss	2 – 25 dB	6 – 22 dB	< 2 dB	< 1 dB
Repeatability	25 dB	--	--	45 dB

It should be noted that the proposed electronic tuner requires precise bias sources for both PIN diode and tunneling diode. A small variation of biases may lead to the shift of impedance. Repeatability is presented to describe the stability of tuner, which denotes the difference between two S-parameters measurements. As can be seen in the Table 3.1, the repeatability of the proposed tuner is around 25 dB, which is limited by the stability and precision of the bias sources.

Over the GHz frequency range, the distorted impedance distribution, caused by the parasitic parameters, can be corrected for different frequency ranges by replacing the adjusting components. Small footprint devices and shorter connection pads can be chosen to further reduce the parasitic effects so as to improve the performance. In practice, the high insertion loss of the proposed electronic tuner will be calibrated prior to the noise measurement.

3.5 Conclusion

In this work, we illustrate the potential use of a negative resistance device in the development of an electronic impedance tuner. The experiments exhibit a good performance of the electronic tuner over the frequency range 1.5 – 5 GHz. The proposed topology can be an alternative solution for on-wafer noise characterization systems. Although only parts of frequencies can have impedance states with reflection coefficient larger than one, accurate modeling of tunneling diode and PIN diode can be further investigated to predict the impedance distribution efficiently. In addition, large power negative resistance devices can be studied to make the electronic tuner work for high power condition.

CHAPTER 4   NON-UNIFORMLY DISTRIBUTED ELECTRONIC
IMPEDANCE SYNTHESIZER

A growing number of wireless communication devices sold per year requires that the suppliers of PAs or radio modules to dramatically increase their testing capabilities. Positioned at the output of PA or radio module, an antenna generally has a limited area and is susceptible to human factor and environmental effect. As a result, a whole set of specifications of the PAs or radio modules must be evaluated with a stress test under different impedance conditions simulating a mismatch of the antenna.

Industry is using an electromechanical impedance tuner, a well-established technique for the field testing. This equipment allows for a very high level of mismatch and power but with the cost of an extremely low tuning speed. For on-wafer measurements, electromechanical impedance tuner can only be placed far away from device under test (DUT) due to its large size and weight. Additionally, the adjustable positioner also limits the flexibility and accuracy of measurement. The industry has therefore greatly promoted the development of a fast tuning electronic impedance synthesizer (EIS) in the past years. The tuning speed of the EIS is in the range of milliseconds whereas tuning speed of electromechanical impedance synthesizer in the range of seconds. The synthesis rate is almost instantaneous and can reduce the measurement time dramatically. This is very important for full range testing of several dc and RF parameters of a PA or a radio module in production runs, especially when a large throughput is required.

Beside the application in characterization system, EIS has also been widely used as a tunable matching network (TMN) for reconfigurable devices or systems [139-147]. The development of software-defined radio (SDR) and new generation communication systems require a number of reconfigurable devices that can operate in different frequency bands and with different communication standards. In a reconfigurable PA, TMN can be placed in both input and output of the PA to match the impedances so as to improve the power transfer gain and efficiency. In a reconfigurable antenna, TMN can improve the maximum radiation power [147].

A traditional digital EIS is made by a set of switches combined with fixed capacitors, which are placed periodically along the transmission line. The switches can be PIN diodes [141, 142],

varactors [143, 144, 148, 149], MMICs or transistors [150-155] and MEMS switches [139, 140, 145, 146, 156]. The position of a capacitor can be varied virtually along the transmission line by choosing the appropriate switch. In such a configuration with a number of n switches, the EIS can only provide limited impedance states (2^n) by combing different states of switches: ON and OFF. The EIS was mostly developed based on the topology of single-stub, double-stub and triple-stub [157], pi-structure [144, 147, 158], T-structure [159], as well as multi artificial transmission lines [153] and transmission line with tunable impedance [160].

The topology with the distributed transmission line technique has been proved having better performance than double- or triple- stub topology [139, 140, 152, 154, 157, 161-163], mainly because of the physical features of distributed structure. In the distributed double-slug EIS [140], eighty sections of minimal-contact MEMS varactors are located periodically along the transmission line. Although it has a uniform Smith chart distribution, a limited voltage standing wave ratio (VSWR) is realized, and large number of varactors and control signals are needed for low frequency, which increases the complexity of control circuit.

In fact, uniform topology is always a compromise solution, it does not guarantee the best performance. Non-uniform distributed structure has been demonstrated in sampling VNAs [164] with better performance than traditional uniform topology. The distance between two sections decreases along the propagation direction, the Bragg cutoff frequency increases so as to have a sharper rise time or fall time for the sampling. Although the application is different, the concept of non-uniform distributed topology could be implemented for an EIS.

A type of non-uniform distributed EIS has been presented in a patent [163], in which only one PIN diode is turned ON at any time, and it is not fully turned ON. The PIN diode in series with a grounded capacitor somehow acts like a varactor but with large series resistance, which results in a large dissipation loss. Although this EIS can be applied to wideband application, non-fully turned ON PIN diode will cause serious intermodulation distortion problem in high power application. Based on the same non-uniform distributed topology in [163], EIS comprising two arrays of solid state tuner and a combiner network has been proposed [161]. The combination of two arrays with a total of 2*N switching elements can only generate N^2 impedance states in lieu of 2^n, somehow it is a waste of resources and space. In both works [161, 163], a prime number relationship of the

physical lengths of transmission lines was proposed to avoid generating repeated reflection coefficient, however, this relationship does not guarantee the best Smith chart coverage.
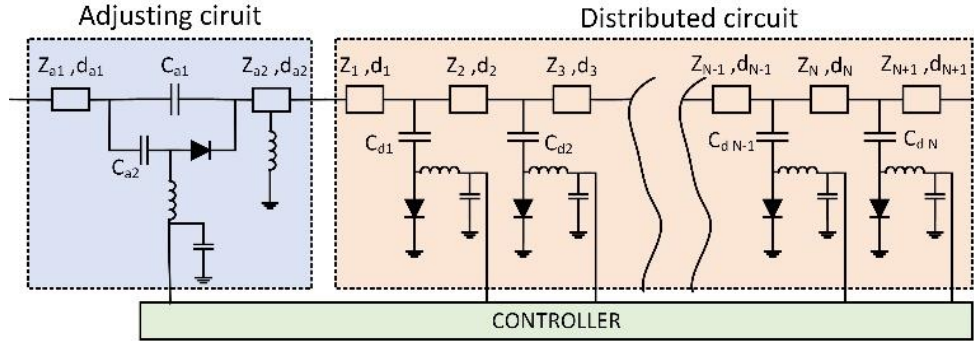
Figure 4.1: Topology of non-uniform EIS consists of an adjusting circuit and a distributed circuit.
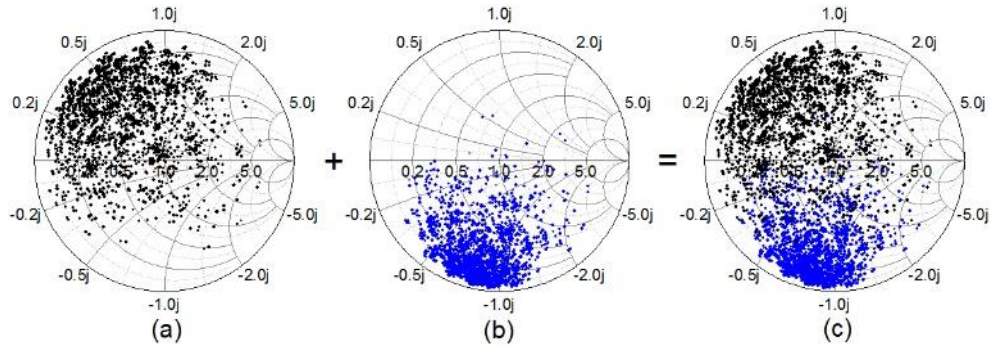
Figure 4.2: Illustration of the effect of the adjusting circuit. Impedance distribution on Smith chart when PIN diode is (a) ON, and (b) OFF; (c) the total effect of the adjusting circuit on the improvement of Smith chart coverage.

In this work, we propose a non-uniform distributed EIS, it consists of an adjusting circuit and a non-uniform distributed circuit (Fig. 4.1). Not only the transmission line length, but also the impedance and loading capacitance for each section are non-uniform. The distributed circuit comprises a high impedance transmission line non-uniformly loaded with different values of capacitors. The adjusting circuit comprises a small value capacitor (e.g., 2 pF) in parallel with a combination of large value capacitor (e.g., 30 pF) in series with a PIN diode. When the PIN diode is turned ON, the total capacitance is around 32 pF, it almost does not have impact on the impedance distribution of the distributed circuit (Fig. 4.2(a)). By contrast, when the PIN diode is turned OFF, the total capacitance is around 2 pF, which can rotate the impedance distribution in counterclockwise direction on Smith chart (Fig. 4.2(b)). As illustrated in Fig. 4.2, the role of the

adjusting circuit is to compensate the uncovered area so as to improve the Smith chart coverage, at the same time keep the total circuit length as short as possible. The adjusting circuit can be replaced by a variable phase shifter or the combination of several different TLs with switches, which can rotate the distributed points in clockwise direction. However, the circuit proposed in this work is simpler and smaller.

So far, except the double-slug distributed EIS [140, 165], it is difficult to have closed-form design process for other topologies due to the unpredictable jumping of impedance states. This work addresses the design and optimization of the proposed non-uniform distributed EIS.

4.1 Semi-closed form design procedure

A semi-closed form design procedure is proposed for uniform distributed topology in order to obtain the initial values and boundaries for the multiple parameters. The range of loading capacitance is firstly determined from the approximate estimation of the maximum reflection coefficient. Then the maximum distance d between each two sections is determined by the Bragg cutoff frequency according to NLTL theory [139, 165, 166], while the minimum distance d is determined by the rule of that total length should be larger than half wavelength of the lowest frequency so as to have a large Smith chart coverage.

A quantitative analysis of Smith chart coverage, which describes the percentage of Smith chart covered by an EIS, is helpful for the evaluation and optimization of the EIS. Visual observation on Smith chart was always used to evaluate the coverage [139, 162]. However, a subjective judgment leads to different results from person to person, and it is not helpful for the parametric study and optimization. To yield a meaningful result and build a goal function for optimization, a quantitative analysis is therefore required. Although the Smith chart coverage has been studied for tunable matching network [141, 142], this definition is not applicable to the case of EIS due to the different scenario. In this work, a similar criterion is developed for the EIS. As shown in Fig. 4.3(a), let us first discretize the whole Smith chart, and make sure there are enough points at each constant VSWR circle. In other words, the discretization process should guarantee enough resolution for applications. We predefined 1116 impedance points in this work for the whole Smith chart, the number of the predefined points varies with the application. Then the measured 4096 impedance points (Fig. 4.3(b)) are projected to the predefined Smith chart, and the redundant points are removed, during which the point with minimum loss is preserved if several points are close to each

other. Finally, Smith chart coverage can be expressed by the ratio of the selected predefined points to the total predefined points.
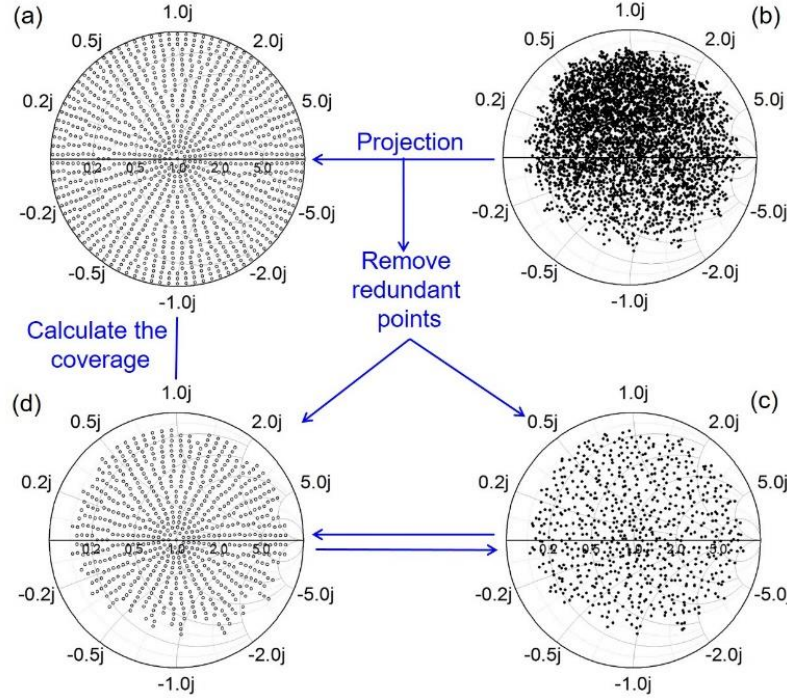
Figure 4.3: (a) Predefined 1116 impedance points on Smith chart; (b) measured impedance points; (c) selected measured points; and (d) selected predefined points.

4.1.1 Determination of the range of loading capacitance

As shown in Fig. 4.1, the input admittance Y_{in} of the EIS can be calculated from the load side easily. In order to simplify the scenario which is similar to the real calibration condition, the admittance of source and load are set as $Y_s = Y_L = 0.02$. Fig. 4.4 illustrates how the impedance moves on Smith chart when multiple capacitors are loaded along the transmission line. As can be seen in Fig. 4.4(a), only when the impedance distributed in the capacitive part of Smith chart, the loaded capacitance can further increase the reflection coefficient. For finding out the maximum Γ, we need to focus on the capacitive part of Smith chart. Since the total length of N sections transmission line needs to be longer than half wavelength of the minimum frequency, there must be at least N/4 times to load capacitors in the capacitive part of Smith chart for each frequency. Therefore, the maximum Γ can be estimated approximately by only one transmission line loaded with $C \cdot N / 4$. Then the input admittance can be calculated by

$$Y_{in} = Y_L + j\omega C \cdot N / 4 \tag{4.1}$$

And the estimated maximum reflection coefficient Γ can be expressed as

$$\Gamma = \frac{Y_s - Y_{in}}{Y_s + Y_{in}} = \frac{-j\omega C \cdot N / 4}{2Y_s + j\omega C \cdot N / 4} \tag{4.2}$$

The magnitude of estimated Γ needs to be larger than the required reflection coefficient Γ_{req},

$$|\Gamma| = \frac{\omega C}{\sqrt{(8Y_0 / \text{N})^2 + (\omega C)^2}} \geq |\Gamma_{req}| \tag{4.3}$$

Then we can obtain the lower boundary of the loading capacitance

$$C_d \geq \frac{4Y_s}{N\pi f} \frac{|\Gamma_{req}|}{\sqrt{1 - |\Gamma_{req}|^2}} \tag{4.4}$$

To have as large as possible Smith chart coverage and keep the impedance points distributed in Smith chart as uniform as possible, another restriction condition will be applied. When only one capacitance C is loaded, the reflection coefficient should be smaller than the required Γ_{req}, otherwise most of the impedance points will distribute at the edge of the Smith chart. This can be expressed as

$$|\Gamma| = \frac{\omega C}{\sqrt{(2Y_s)^2 + (\omega C)^2}} \leq |\Gamma_{req}| \tag{4.5}$$

Then we can obtain the upper boundary of the loading capacitance

$$C_d \leq \frac{Y_s}{\pi f} \frac{|\Gamma_{req}|}{\sqrt{1 - |\Gamma_{req}|^2}} \tag{4.6}$$

For a requirement of $|\Gamma_{req}| = 0.875$, the maximum and minimum loading capacitance are plotted in Fig. 4.5 as a function of frequency for a 12 sections EIS. A proper capacitance can be chosen ideally to have operation bandwidth more than 1 octave. In practice, the results on upper and lower boundary of frequency band are not good. For low frequencies, the impedance distribution will be concentrated on the center of Smith chart due to the small loading capacitance, while the impedance distribution for high frequency will be close to the edge of Smith chart because of the larger loading capacitance. As a matter of fact, the operation bandwidth of a real circuit is smaller than 1 octave,

which is limited by the parasitic parameters from the commercial PIN diode and capacitor as well as the pads.
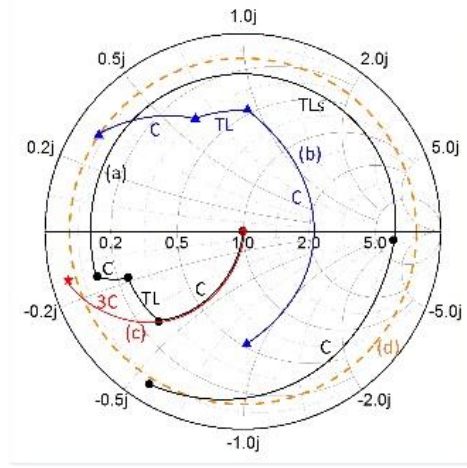
Figure 4.4: Impedance movement after (a) loading capacitance on the capacitive part of Smith chart, (b) loading with $C \cdot N / 4$ (N = 12), (c) loading with capacitance on the inductive part of Smith chart; (d) Required constant reflection coefficient circle.
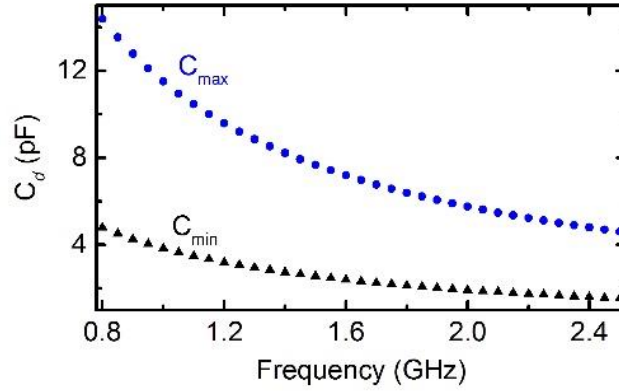
Figure 4.5: Lower and upper boundaries of loading capacitance.

4.1.2   Determination of the range of distance d

When all of the PIN diodes are turned ON, the distributed circuit (Fig. 4.1) is similar to a conventional NLTL [54], and the Bragg cutoff frequency will be applied due to the low pass property [23, 139, 166]

$$f_{Bragg} = \frac{1}{\pi d} \frac{1}{\sqrt{K}} \frac{c}{\sqrt{\varepsilon_{reff}}}$$

(4.7)

where d denotes the distance between two sections, c is the speed of the light, ε_{reff} is the effective dielectric constant of unloaded transmission line. The scaling factor K is expressed as

$$K = 1 + \frac{C}{d} \frac{cZ_0}{\sqrt{\varepsilon_{reff}}} \tag{4.8}$$

where C is the loading capacitance, Z_0 is the impedance of unloaded transmission line. The cutoff frequency should be larger than highest operation frequency $f_{Bragg} > f_H$, otherwise it will cause serious loss problem (Fig. 4.5). Then the upper boundary for the distance d can be expressed as

$$d < \frac{c}{2\sqrt{\varepsilon_{reff}}} \left[\sqrt{(C \cdot Z_0)^2 + \left(\frac{2}{\pi f_{Bragg}} \right)^2} - C \cdot Z_0 \right] \tag{4.9}$$

The effect of Bragg cutoff frequency are illustrated in Fig. 4.6, where the transmission response and loss feature with different d leading to f_{Bragg} of 3 GHz, 4 GHz and 5 GHz are shown. The loss will increase dramatically after the cutoff frequency, and higher cutoff frequency will result in lower loss in the operation frequency band, but at the cost of a smaller d. In other words, more sections will be needed to have a high Smith chart coverage, which in turn increase the total loss. So that a tradeoff needs to be made, in this work, a cutoff frequency of 4 GHz will be chosen for the EIS with operation frequency band of 0.8 to 2.5 GHz.
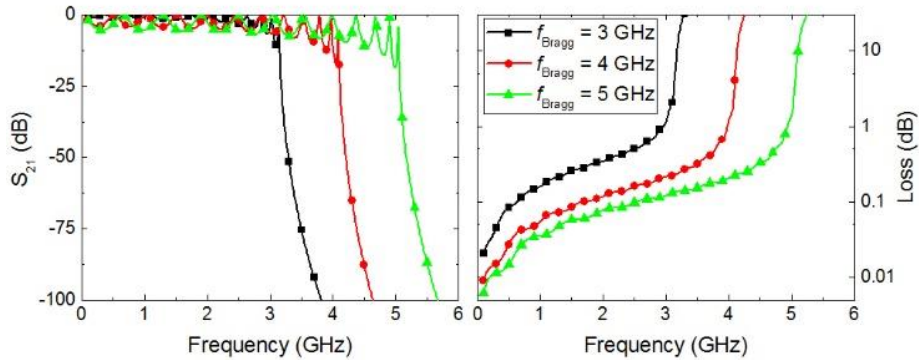
Figure 4.6: (a) Transmission response and (b) loss feature of EIS with f_{Bragg} of 3 GHz, 4 GHz and 5 GHz. Only the conductive loss and dielectric loss are taken into consideration in the total loss. The ripples in transmission response are because of the mismatching at this impedance state. Note that it is only the response of the impedance state with all the PIN diode turned ON.

To guarantee there are enough impedance points at the starting frequency point, the total length of transmission line should be larger than half wavelength of the lowest frequency. Then the distance between two sections should be

$$d > \lambda_{max} / 2(N+1) \qquad (4.10)$$

Compared to the strict limit factor in (4.9), the lower boundary of d is more flexible. If a small starting frequency and a high Bragg cutoff frequency are chosen, conflict will occur between (4.9) and (4.10). In this case, restriction of (4.9) should be followed. In general case, (4.9) and (4.10) will limit d to a small range, which is critical for the design.

The Smith chart coverage and mean loss are investigated for the EIS with different numbers of sections (Fig. 4.7) while keeping f_{Bragg} as 4 GHz. As can be seen that when d is limited by (4.9), the Smith chart coverage can be improved by increasing the number of sections, but with the sacrifice of loss. It also can be seen from Fig. 4.7, the minimum coverage within a certain bandwidth always occurs at both sides of the frequency range. Therefore, the relationship between the minimum coverage for a certain bandwidth and the number of sections N could be obtained, which can be used as a preliminary guidance to determine the minimum N according to the required coverage.
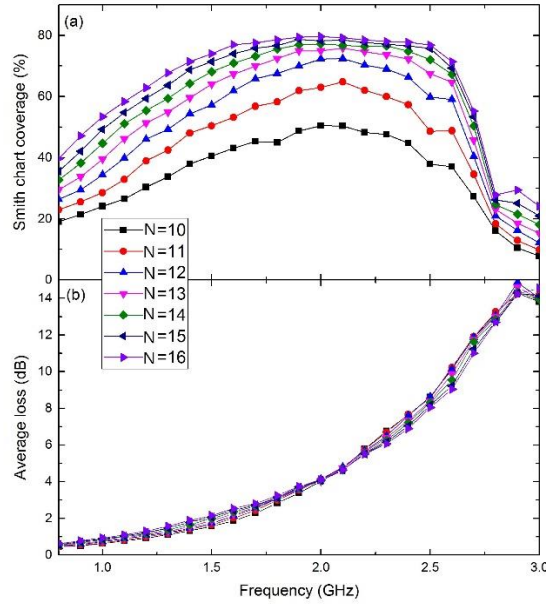
Figure 4.7: The investigation of (a) Smith chart coverage as well as (b) mean loss of the EIS with different number of sections while keeping f_{Bragg} as 4 GHz. Mean loss is the average loss for the

selected impedance points. Reactive parasitic parameters from commercial PIN diode and capacitor are not taken into consideration in the loss.

4.1.3   Selection of PIN diode and determination of Z_0

The PIN diode has wide intrinsic layer, therefore it can handle high RF voltage [167] and then has good linearity [168]. In addition, a PIN diode has fast switching time [169, 170]. In this work, commercial PIN diodes will be selected for the design of the EIS mainly based on two aspects: the parasitic parameters and the power-handling capacity. Tradeoff needs to be made between series resistance and capacitance because of their opposite relationship with junction area.

The power-handling capacity and nonlinearity of an EIS are highly dependent on the performance of each PIN diode. Therefore, the PIN diode needs to be evaluated prior to applying it in the design of an EIS. Appropriate biases of PIN diode for both ON and OFF states will be determined firstly from the intermodulation distortion (IMD) measurements.

For OFF state, the PIN diode can be considered as a voltage-controlled capacitor in series with an inductor (inset in Fig. 4.8(a)), the IMD is dominated by the nonlinearity of depletion capacitance with reverse bias (Fig. 4.8(a)). The third-order intercept point can be predicted by [171]

$$IP3 = 6.5 - 10\log(\mathrm{f} \cdot Z_0{}^2 \cdot d^2C/dV^2) \quad dBm \tag{4.11}$$

where Z_0 denotes the characteristic impedance of system, and d^2C/dV^2 denotes the second derivative of C(V) characteristic. It should be noted that the breakdown effect has not been considered in (4.11), so the reverse bias close to breakdown voltage will result in a decrease of IP3. It has been demonstrated that PIN diode with thicker intrinsic layer has flatter C(V) characteristic due to the small portion of depletion layer compared to the overall thickness [171]. Therefore, the third order intercept point (IP3) for OFF state is proportional to the width of intrinsic layer, and inversely proportional to the operation frequency.

For ON state, PIN diode can be considered as a current controlled resistor in series with an inductor (inset in Fig. 4.8(b)), the nonlinear IV characteristics in intrinsic layer is the main source of IMD (Fig. 4.8(b)). The third-order intercept point can be expressed theoretically by [172]

$$IP3 = 69 + 15\log(\mathrm{I_F}\,\tau\,\mathrm{f/\,Rs}) \quad dBm \tag{4.12}$$

where I$_F$ stands for the forward current, τ denotes the minority carrier lifetime or recombination lifetime, and f represents operation frequency while R$_S$ is the high frequency resistance. Since $R_s = W^2 / 2\mu I_F \tau$, where W is the width of intrinsic layer and μ is ambipolar mobility, then the IP3 is proportional to forward current and operation frequency, and inversely proportional to the width of intrinsic layer.

In order to have a higher IMD for both ON and OFF states, PIN diode needs to be chosen with a tradeoff. In this work, SMP1320-079LF from Skyworks Solution Inc. with 8 μm intrinsic layer, and BAR95-02LS from Infineon Technologies with 19 μm intrinsic layer are chosen for the experiments to handle at least 0.5 watt CW power. The IMD test of PIN diode SMP1320 under different reverse bias and forward currents are depicted in Fig. 4.8(c) and (d). A low input IP3 (IIP3) is measured when a small reverse bias or small forward current is applied. In this case, smaller test power needs to be used for IMD test, otherwise too high test power will result in stronger nonlinearity [173]. As can be seen from Fig. 4.8(c) and (d), the theoretical calculation based on (4.11) and (4.12) can be used to predict the power-handling capacity of the PIN diode. Finally, a half of the breakdown voltage -25 V is selected for OFF state, and forward bias 30 mA is selected for ON state, so that single PIN diode will have IIP3 more than 50 dBm.
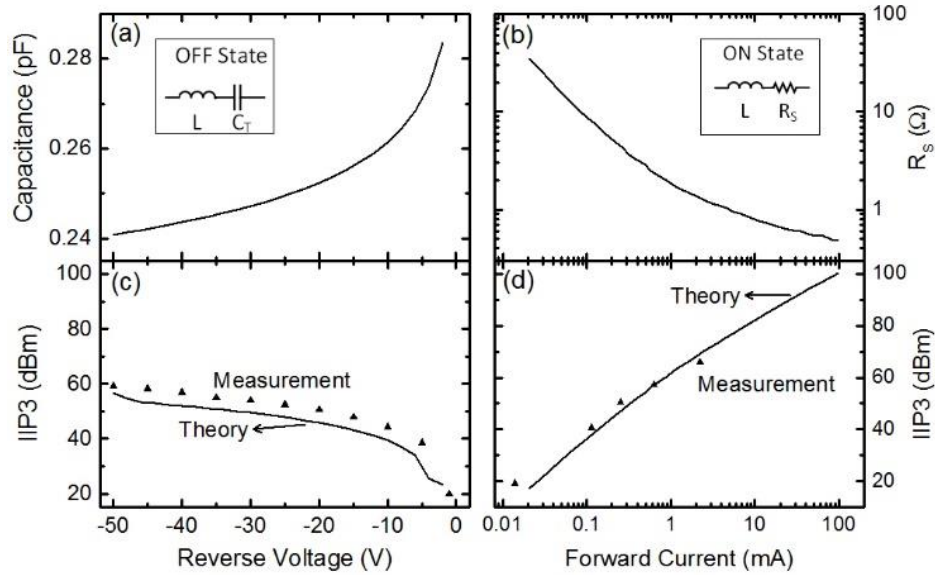
Figure 4.8: Nonlinearity of (a) R$_s$ (I$_F$) and (b) C$_T$ (V$_r$) characteristics of PIN diode SMP1320. IMD test for both (c) OFF and (d) ON states. Dots denote measurement while line denotes theoretical predictions.

Similar to NLTL theory, the initial impedance of unloaded transmission line Z_0 is set to a high value, in order to keep the loaded impedance close to 50 Ω after loading the capacitors. Increasing Z_0 improves the Smith chart coverage of the EIS, but a high Z_0 leads to a narrow trace, where soldering the commercial components becomes challenging.

4.2 Optimization

For an EIS with N sections (Fig. 4.1), 3*N+6 variables will be involved in the optimization process, including N loading capacitors, N+1 lengths of transmission line and N+1 impedances for distributed circuit, 2 capacitors and 2 lengths of 50 Ω transmission line for adjusting circuit. The complexity of the optimization problem grows with the number of sections. This work is the first to introduce Particle Swarm Optimization (PSO) to solve the multi-parameter microwave design problem of an EIS, which can dramatically shorten the development cycle.

PSO is an emerging heuristic search method, which is inspired by the collaborative behavior or information sharing mechanism of biological populations, such as flocks of birds, schools of fish. As a population-based search method, the best solution can be discovered by moving around a population (swarm) of candidate solutions (particles) in the multi-dimensional search space. The movement of each particle is guided not only by its local best-known position, but also by the best known positions of the entire swarm so as to move the swarm toward the best solution after several iterations.

4.2.1 Definition of fitness function

A fitness function is a figure of merit that indicates how close the design solution is to the goal. Smith chart coverage will be considered as the fitness function since it is the most important criterion to evaluate an EIS. In addition, several criteria such as loss, uniformity factor, power handling also can be integrated into the fitness function according to different applications.

4.2.1.1 Loss

Three loss definitions, transducer power gain G_T, power gain G_P, and available power gain G_A [174], can be utilized for a mismatched two port network in either logarithm [140, 141, 145] or linear format [139, 146]. The selection of loss definition depends on the different scenario as explained in Fig. 4.9.
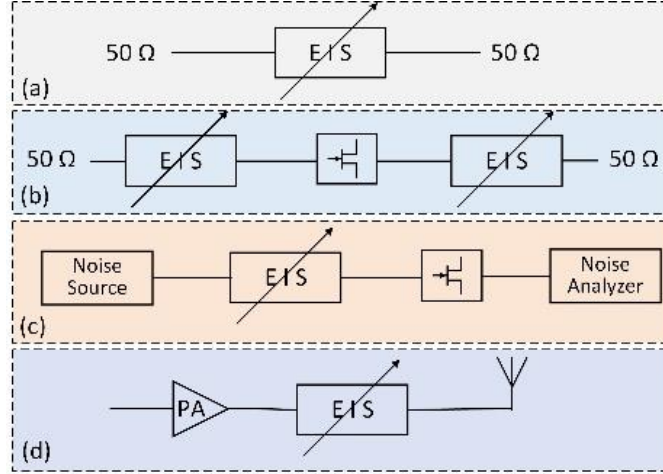
Figure 4.9: Four different scenarios to use EIS: (a) Calibration with VNA; (b) Load-Pull characterization system; (c) Noise measurement; (d) TMN for reconfigurable PA or antenna.

Except acting as a one-port variable load, EIS is normally used as a two-port network in four scenarios (Fig. 4.9). In the calibration process (Fig. 4.9(a)), the EIS will be connected to a 50 Ω VNA, then we have $\Gamma_S = \Gamma_L = 0$. In this case, the power gain G_P, the ratio of power available from the network and power input to the network, is suitable to describe the loss of the EIS. It describes the power dissipated in the network, and it can be simplified as

$$G_P = \frac{|S_{21}|^2}{1-|S_{11}|^2} \tag{4.13}$$

Since the EIS will not be used in practical application with both sides terminated by 50 Ω, this loss definition only can used as a reference.

When the EIS used as a load tuner in Load-Pull characterization system (right side in Fig. 4.9(b)), the impedance at the output port of DUT is unknown (but not 50 Ω), then we have $\Gamma_S \neq 0$ and $\Gamma_L = 0$. Power gain G_P only can be calculated and it has the same simplified form as (4.13). In practical application, the impedance of the EIS will be swept until maximum power is detected by the power meter that is placed at the output of the EIS, then we consider the output of DUT and the input of the EIS are conjugation matched. From power gain G_P, we can estimate the output power from the DUT. In fact, the optimal impedance and maximum power at the output port of DUT are what one expects from Load-Pull system. Since the load tuner scenario shares the same loss

equation with the calibration scenario (Fig. 4.9(a)), the loss from the calibration process can be considered as a reference for load tuner.

In source tuner scenario (left side in Fig. 4.9(b)) or noise measurement (Fig. 4.9(c)), $\Gamma_S = 0$ and $\Gamma_L \neq 0$, we will select available power gain G_A that is defined by the ratio of power available from the EIS and power available from the source. G_A can be simplified as

$$G_A = \frac{|S_{21}|^2}{1 - |S_{22}|^2} \tag{4.14}$$

from which we can estimate the power output from EIS or the power input to DUT if the conjugation matching is considered.

When an EIS is used as a TMN for reconfigurable devices (Fig. 4.9(d)), both sides are probably not 50 Ω, which means $\Gamma_S \neq 0$ and $\Gamma_L \neq 0$. In this case, we select transducer power gain G_T, which is defined by the ratio of power delivered to the load and power available from the source, because we care about the maximum power transferred to the load. G_T considers the power dissipated in the EIS and the mismatching loss on both sides, as well as the conductive and dielectric loss. It can be expressed as

$$G_T = \frac{1 - |\Gamma_S|^2}{|1 - \Gamma_{IN}\Gamma_S|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \tag{4.15}$$

where

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{4.16}$$

From the above analysis, one knows that the loss is not always describing the power dissipated inside the EIS. As used in most of work, the definition of (4.13) is also chosen in this work for two reasons: 1) It is similar to the real calibration process with both sides terminated by 50 Ω. 2) Although it is not suitable for all the scenarios, it is the only measurable loss compared to others, and the measured results can be used to verify the theory.

4.2.1.2 Uniformity factor

The ideal EIS should have a uniform distribution, which can be understood as same number of impedance points distributed in an equal area. The Smith chart coverage criterion can provide a total number of useful points, but it does not show where those points are distributed on Smith chart. A high coverage does not guarantee a uniform distribution. We propose to apply the criterion of uniformity factor from TMN [145] into the EIS so as to compensate the deficiency of Smith chart coverage. It is a numerical solution to roughly estimate the uniformity of distribution on Smith chart, therefore it also can be used as restriction condition in optimization. A lower value indicates a better distribution over the entire Smith chart.

The uniformity factor calculation process is described as the following: first the Smith chart will be divided into N_r and N_θ subsections from radius and phase directions, respectively (Fig. 4.10). It should be noted that non-uniform division will be done in radius direction in order to ensure each subsection has same area. Then the number of impedance points N (i,j) in each subsection will be counted. Finally, the uniformity factor can be expressed by calculating the variance

$$U_F = \frac{\sum_{i=1}^{N_r}\sum_{j=1}^{N_\theta}(N(i,j) - \frac{N_{total}}{N_r N_\theta})^2}{N_r N_\theta} \tag{4.17}$$
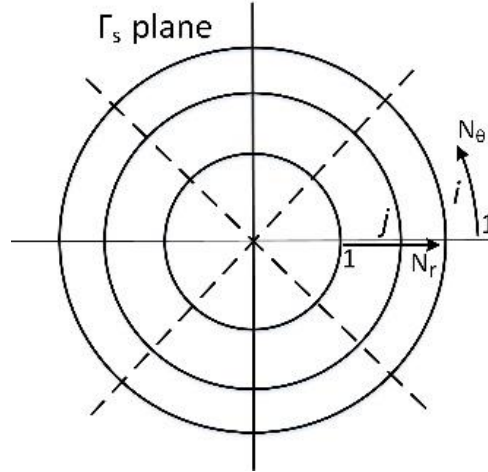
Figure 4.10: The division of Smith chart to calculate the uniformity factor.

4.2.1.3 Maximum peak voltage

Voltage distribution theory developed in this section is to estimate the power handling and nonlinearity of the distributed EIS in an easy way. It helps to know the peak voltage at any position of the distributed structure. During the optimization, we can improve the power handling of an EIS by limiting the maximum peak voltage to a certain level.

Power-handling capacity is defined as the maximum average power that could be delivered to EIS without degrading its performance. The 1 dB gain compression point (P1dB) is often used as a metric to evaluate the power-handling capacity. As a matter of fact, every electronic component or system has some degree of nonlinearity, which can be described by the IIP3 from IMD test. As listed in Table 4.1, limited work has been done on the power-handling capacity and HB simulation, but only for a limited number of impedance states because the simulations and measurements are time-consuming and inefficient, especially for the statistic study of an EIS involving thousands of impedance states. They are always used as verification [139, 157], which are, however, not able to be considered in the design and optimization process.
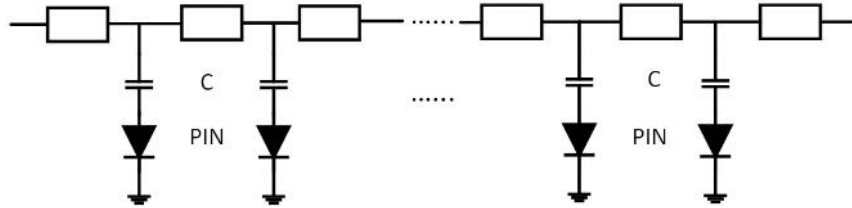
Figure 4.11: Traditional topology of distributed electronic impedance synthesizer.

It is quite a challenge to measure the voltage distribution, so that simulation of voltage distribution is commonly used to verify the impedance states [139, 140, 157], or predict the power-handling capacity qualitatively [162]. By contrast, the proposed voltage distribution theory in this work can prove to be very useful to predict the power-handling capacity and nonlinearity quantitatively for distributed nonlinear circuits. Since the nonlinearity of EIS comes from the nonlinear devices (PIN diodes) in the circuit, the power handling capacity of an EIS is related to the operation status of each PIN diode. The analysis of voltage distribution enables to find out the maximum peak voltage along the transmission line. Larger maximum peak voltage will result in lower power-handling capacity, and vice versa. Consequently, if the relationship between power-handling capacity and maximum peak voltage can be established from a small amount of simulations (e.g., 20), it is

possible to estimate the power-handling capacity as well as nonlinearity by the proposed voltage distribution theory, and then use it as a criterion in the design and optimization process to boost the power-handling capacity and linearity.

Table 4.1: Studies of power-handling capacity and nonlinearity of EIS.

Reference	Voltage distribution	P1dB	IP3
[157]	Simulation	Measurement, 24 dBm	Measurement, 33 dBm
[139]	Simulation	Measurement, 28.5 dBm (self-actuation power)	Measurement, 31 dBm
[140]	Simulation	--	--
[175]	--	--	Measurement, OIP3 $\approx$ 48 dBm
[158]	--	Measurement, $\approx$ 33 dBm	--
[154]	--	Measurement, -1 dBm (P_{out}1dB)	--
[147]	--	Measurement, $>$ 40dBm	--
[162]	Simulation	Measurement, 36 dBm (self-actuation power)	--
[161]	--	Measurement, 38.5 dBm	--
This work	Theory & Simulation	Measurement & Simulation 35 dBm	Measurement & Simulation IIP3 = 57 dBm

In order to simplify the analysis of distributed topology, lossless transmission line is first considered (Fig. 4.11). Fig. 4.12(a) shows the circuit of (m-1)th and mth sections of the distributed EIS. The circuit before the (m-1)th diode can be replaced by Thevenin voltage $V_{th,m-1}$, and Thevenin impedance $Z_{th,m-1}$ (Fig. 4.12(b)). $Z_{th,m-1}$ is the impedance seen on the left side the diode m-1 by considering the voltage source as RF short circuit. In Fig. 4.12(c), the right-handed side circuit is considered as open circuit when calculating the Thevenin voltage at node m. The voltage and current at position z can be expressed as [23]

$$V(z) = A \cdot (e^{-j\beta z} + e^{j\beta z}) = 2A\cos(\beta z) \tag{4.18}$$

$$I(z) = -j2\frac{A}{Z_0}\sin(\beta z) \tag{4.19}$$

The voltage at z = -*l* can also be calculated by

$$V(-l) = V'_{th,m-1} - I(-l) \cdot Z'_{th,m-1} = V'_{th,m-1} - j2A \frac{Z'_{th,m-1}}{Z_0} \sin(\beta l) \tag{4.20}$$

From (4.18) and (4.20), one can obtain the coefficient A

$$A = \frac{V'_{th,m-1}}{2(\cos(\beta l) + j\sin(\beta l) \frac{Z'_{th,m-1}}{Z_0})} \tag{4.21}$$

Substitute (4.21) into (4.18), the Thevenin voltage at node m can be obtained by letting z = 0, and $V_{th,m}$ can be iterated until m = 1. If $Z_s = Z_0$, then $V_{th,1} = V_s e^{-j\beta l}$, where V_s is the source voltage, and it is expressed as $V_s = \sqrt{8 \cdot P_0 \cdot real(Z_s)}$. In order to further simplify the scenario, we assume the PIN diode used here as an ideal switch. As illustrated in Fig. 4.12(b), the Thevenin voltage $V'_{th,m-1}$ can be calculated from $V_{th,m-1}$ by the theory of voltage divider,

$$V'_{th,m-1} = V_{th,m-1} \cdot \frac{Z_c}{Z_c + Z_{th,m-1} \cdot S_{m-1}} \tag{4.22}$$

where $Z_c = 1/j\omega C_d$, and S_{m-1} denotes the status (0 or 1) of the $(m-1)^{th}$ PIN diode. With iteration, one could obtain the relationship between the Thevenin voltage at each node and the source voltage as follows,

$$V_{th,m} = V_s \cdot \frac{1}{\cos(\beta l) + j\sin(\beta l) \frac{Z'_{th,m-1}}{Z_0}} L \frac{1}{\cos(\beta l) + j\sin(\beta l) \frac{Z'_{th,1}}{Z_0}} \cdot \\ \frac{1}{\cos(\beta l) + j\sin(\beta l) \frac{Z_s}{Z_0}} \cdot \frac{Z_c}{Z_c + Z_{th,m-1} \cdot S_{m-1}} L \frac{Z_c}{Z_c + Z_{th,1} \cdot S_1} \tag{4.23}$$

where m > 2. As depicted in Fig. 4.12(d), the voltage at node m can be calculated by

$$V_m = V_{th,m} \cdot \frac{Z_{in,m}}{Z_{in,m} + Z_{th,m}} \tag{4.24}$$
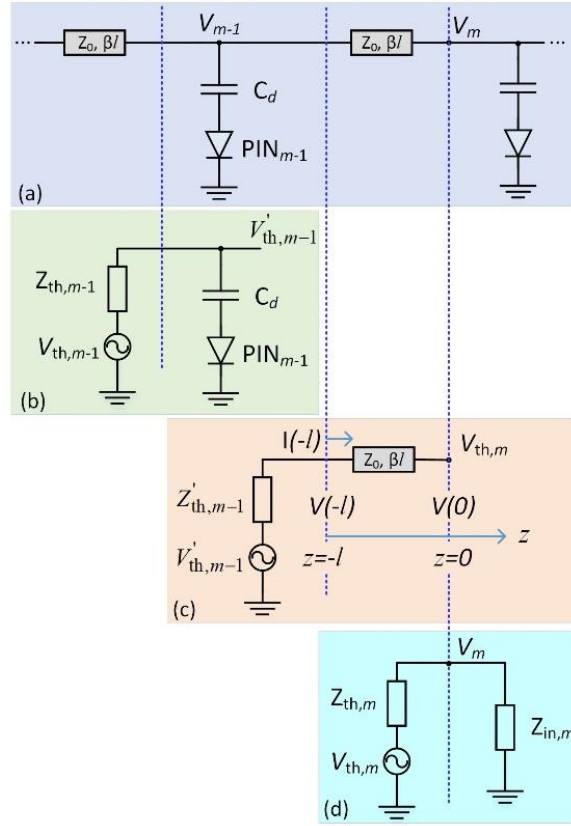
Figure 4.12: Diagram for voltage distribution analysis. (a) Equivalent circuit of (m-1)th section; Thevenin equivalent circuit (b) at node m-1 with open termination; (c) at node m with open termination; (d) at node m with load.
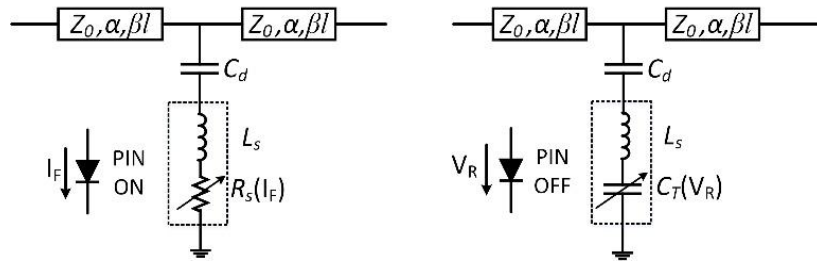
Figure 4.13: Equivalent unit circuit model with PIN diode at (a) ON state, and (b) OFF state. Loading capacitor is still considered as ideal capacitor in order to keep the calculation concise. The biasing circuit is not shown in the model.

In practice, the switch and capacitor, as well as transmission line are not ideal components, the equivalent circuit model can be described as in Fig. 4.13, in which α denotes the dielectric loss and conductive loss of transmission line. Let us take the parasitic parameters of PIN diode into account,

PIN diode at ON state can be described by series inductor L$_s$ and series resistor R$_s$, the R$_s$ is controlled by forward current I$_F$. On the other hand, PIN diode at OFF state is described by series inductor L$_s$ and total capacitor C$_T$, which is controlled by reverse voltage V$_R$. The loss of transmission line can be included in the calculation by replacing $j\beta$ by $\alpha + j\beta$ in the above calculation. The Z$_c$ in (4.24) is then changed to

$$Z_c = \frac{1}{j\omega C_d} + j\omega L_s + R_s \tag{4.25-1}$$

$$Z_c = \frac{1}{j\omega C_d} + j\omega L_s + \frac{1}{j\omega C_T} \tag{4.25-2}$$

for $S_{m-1} = 1$ and $S_{m-1} = 0$, respectively. And (4.22) will become

$$V'_{th,m-1} = V_{th,m-1} \cdot \frac{Z_c}{Z_c + Z_{th,m-1}} \tag{4.26}$$

Through the voltage divider theory, the peak voltage on the mth PIN diode will be obtained (Fig. 4.3)

$$V_{PIN,m} = V_m \cdot \frac{jwL_s + R_s}{1/jwC_d + jwL_s + R_s} \tag{4.27-1}$$

for $S_{m-1} = 1$, while

$$V_{PIN,m} = V_m \cdot \frac{jwL_s + 1/jwC_T}{1/jwC_d + jwL_s + 1/jwC_T} \tag{4.27-2}$$

for $S_{m-1} = 0$. Although the voltage distribution theory developed in this work is based on the distributed topology as shown in Fig. 4.11, similar method can be applied to any other distributed topology to help understanding the nature of voltage distribution.

Since the peak voltage is proportional to square root of power, it should have linear relationship with P1dB or IIP3 (dBm) under a linear power region. This relationship can be integrated in the analytical model, then we can calculate the power-handling capacity and nonlinearity for all the impedance points quickly.
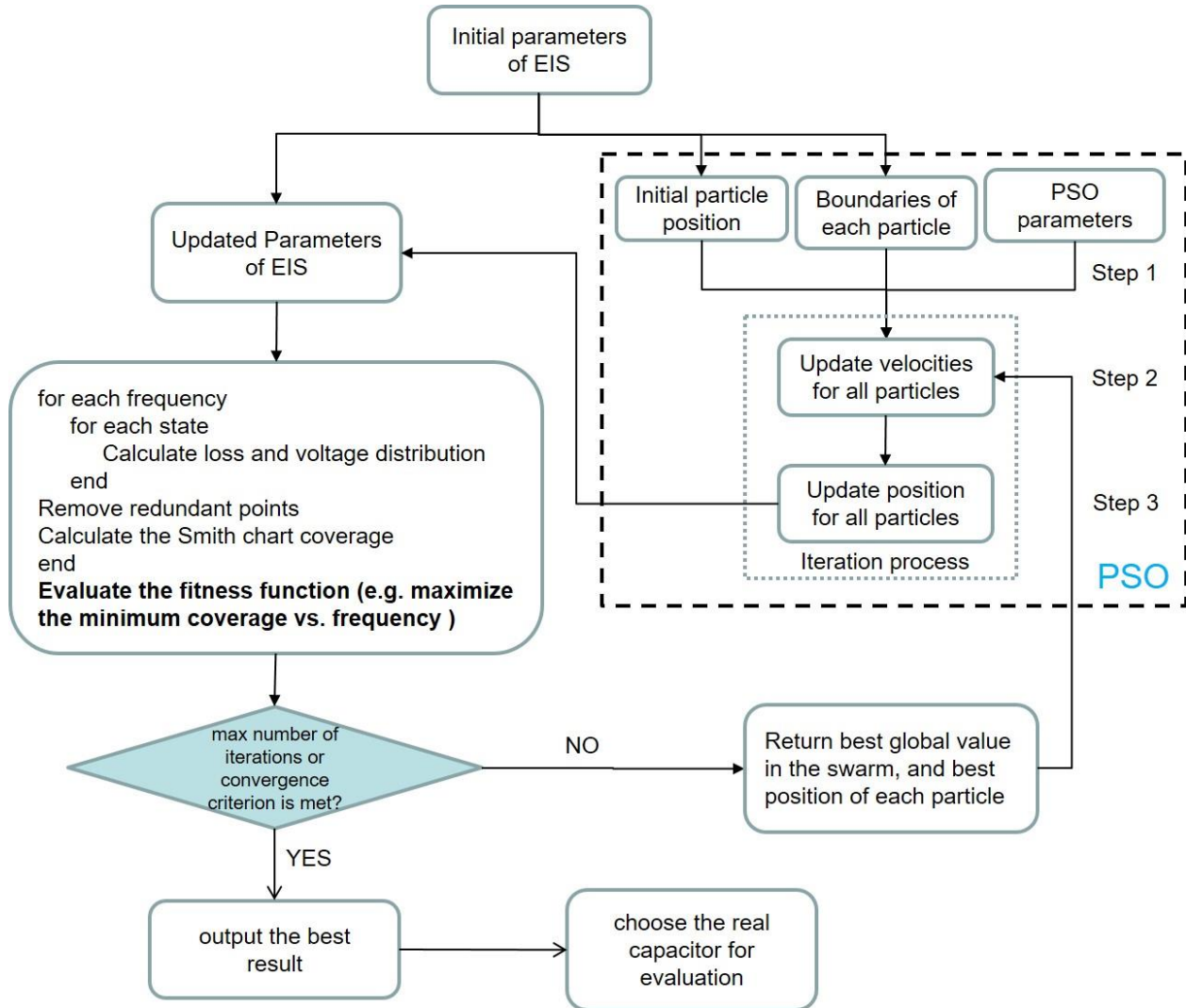
Figure 4.14: Diagram of optimization process using PSO.

4.2.2 Description of optimization process of PSO

Fig. 4.14 shows the diagram of optimization process of an EIS, the engineering problem with multiple parameters can be considered as a multidimensional space in PSO, and each combination of parameters will be a position in the space. PSO algorithm consists of three steps, namely, generating particles' positions and velocities, velocity update, and position update. In basic PSO algorithm, the initial position $x_{k,i}$ and velocity $v_{k,i}$ of each particle are generated randomly based on the upper and lower bounds of each particle. In this work, we directly use the initial parameters that are obtained from the semi-closed form design procedure. The initial position will dramatically reduce the searching time for the best solution.

In second step, the velocity of particle i at time k+1 $v_{k+1,i}$ will be updated from its current velocity $v_{k,i}$ by the equation [176]:

$$v_{k+1,i} = c_0 v_{k,i} + c_1 r_p \frac{p_i - x_{k,i}}{\Delta t} + c_2\, r_g \frac{g_k - x_{k,i}}{\Delta t} \tag{4.28}$$

where p_i stands for the best position for particle i, while g_k represents the best global position value in the current swarm. It shows that the next search direction for each particle is influenced not only by its best position, but also the best position in the swarm. Three weight factors are introduced to express the portion of influence for each term, namely inertia factor, c_0, self-confidence factor, c_1, and swarm confidence factor, c_2. In addition, two uniformly distributed random parameters r_p and r_g are applied to guarantee a good coverage and avoid local optimal. The last step of PSO in each iteration is to update the position with the following equation:

$$x_{k+1,i} = x_{k,i} + v_{k+1,i}\Delta t \tag{4.29}$$

The updated parameters after PSO will be used to evaluate the fitness function. One important step to calculate the Smith chart coverage is to remove the redundant impedance points and choose useful points. Several restriction conditions can be applied in this step for specific application, for instance, limit the maximum loss to 10 dB, limit the uniformity factor to a certain value, and limit the maximum peak voltage as a certain level. In order to have a high coverage for the whole frequency band, in each iteration, we will find out the minimum coverage versus frequency. Then in PSO, we will define the optimization goal as maximizing the minimum coverage. The best solution will be obtained when the maximum iteration is reached, or the optimization goal is satisfied. It should be noted that the developed optimization method can be applied to optimize the specific area on Smith chart if special requirement is asked in the application.

Optimization results show that the difference of impedance of N+1 transmission line does not improve the results obviously. Therefore, we can remove some optimization variables in order to reduce the optimization time. PSO is inherently a continuous optimization method, one can modify it to handle discrete design variables according to the commercial value of capacitors. Actually, a slight change of capacitance does not have much effect on the performance of an EIS. Therefore, we can just replace the optimized capacitance by the closest practical capacitor value.

About the computational efficiency of PSO, for an optimization with 27 parameters, it averagely takes about 1.5 seconds for each iteration when the number of particle is set as one. In this work, 20 particles are set for PSO, it usually can reach the optimal value after 20 iterations, which means 10 hours for the optimization of an EIS with 27 variables. It is worthwhile to note that the total optimization time will decrease when the number of parameters reduces.

4.3   Experiment

In order to validate the design procedure and the optimization method, three general purpose EISs (Fig. 4.15(a) - (c)) are proposed for 0.8 – 2.5 GHz. Only Smith chart coverage and loss are considered in the fitness function of optimization to simplify the verification of the theory. As shown in Fig. 4.15, three circuits are optimized and fabricated on Rogers 6002 substrate with thickness of 20 mil. Circuit 1 is a 12-section uniform distributed topology with $d = 4.71$ mm, $C_d =$ 1.8 pF, and $Z_0 = 83$ Ω (Fig. 4.15(a)). Based on circuit 1, circuit 2 adds an adjusting circuit (Fig. 15(b)), in which C_{a1} is 1.8 pF, and C_{a2} is 30 pF (Fig. 4.1). All the parameters of circuit 2 are optimized as different values (Fig. 4.15(c)), the distance d in circuit 3 varies from 1.48 to 9.16 mm, while the loading capacitance C varies from 0.7 to 9.1 pF. It is apparent that the circuit 3 has a smaller size than circuit 1 and 2.

The three circuits (Fig. 4.15(a) - (c)) are measured automatically with the software FDCS from Focus Microwaves Inc., and a controller is dedicated to switch the states of EIS. The measured and theoretically calculated Smith chart coverage of these three circuits are depicted in Fig. 4.16. Theoretical result of circuit 2 has a Smith chart coverage 10% better than circuit 1, which validates the effect of adjusting circuit. Theoretical result of non-uniform circuit 3 further improves the Smith chart coverage compared to circuit 2. However, the measurement results for all three circuits deviate from the theory at high frequency. Measurement results prove the effectiveness of non-uniform topology and PSO method, even though the deviation is observed between theory and measurement. Parametric studies are carried out to investigate the intrinsic reason of the deviation, which show that the series inductance and series resistance are the two main factors resulting in the deviation in Fig. 4.16.
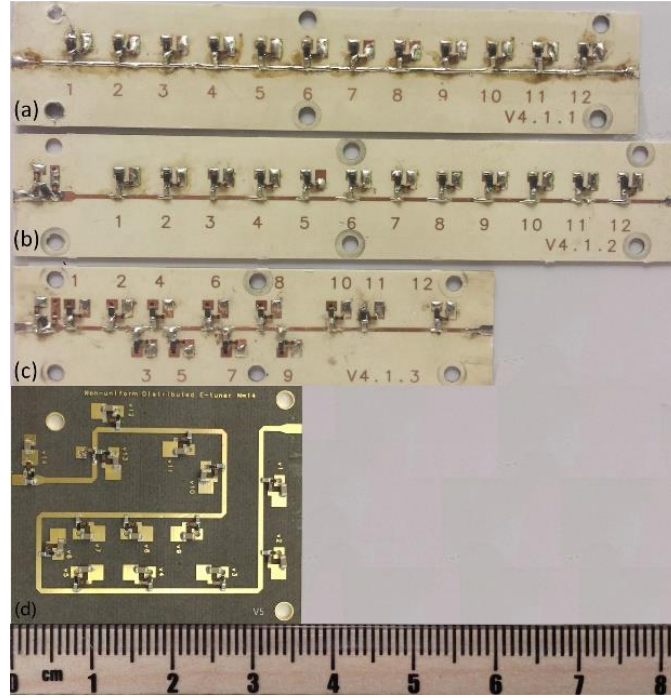
Figure 4.15: Fabricated uniform and non-uniform circuits, biasing wires are not shown. (a) Circuit 1: 12 section uniform distributed topology without adjusting circuit. (b) Circuit 2: 12 section uniform distributed topology with one section of adjusting circuit. (c) Circuit 3: 12 section non-uniform distributed topology with one section of adjusting circuit. (d) Circuit 4: New 13 section non-uniform distributed EIS with one section of adjusting circuit.

The EIS is sensitive to every parasitic parameter in the real circuit, so the equivalent circuit model of a unit circuit of the EIS is necessary to be built. As depicted in Fig. 4.17, the commercial capacitor is modeled by a series circuit of RLC. The L_{cap} is around 0.4 nH for a capacitor with 0402 footprints, which is obtained by fitting the self-resonance frequency of the capacitor. The PIN diode at ON state can be modeled by a series inductor L_{PIN} and a series resistor R_{PIN}, while OFF state is modeled by a series inductor L_{PIN} and a series capacitor C_{PIN}. L_{PIN} is dependent on the footprint selection of PIN diode. The effects of connection pads and via holes can be modeled as an inductor, which is around 0.2 - 0.4 nH obtained from modeling the measured S-parameters of a unit circuit.

Among the parasitic parameters, the series inductance from the PIN diode, the capacitor, and the connection pads and via holes has critical effect on the performance of an EIS, since it will resonate with the loading capacitor near the operation frequency band. The effect of the parasitic inductance is studied at the impedance state with all PIN diodes are turned ON. When the total parasitic

inductance L is 0, the Bragg cutoff frequency dominates, when L increases to 0.8 and 1.5 nH, the resonance frequency starts to dominate. The consequence is that the loss increases dramatically near the resonance frequency. The effect of parasitic inductance on the performance of an EIS is also studied for all the impedance states. The Smith chart coverage at high frequency are distorted seriously due to the increases of the parasitic inductance, and the mean loss at high frequency becomes worse.
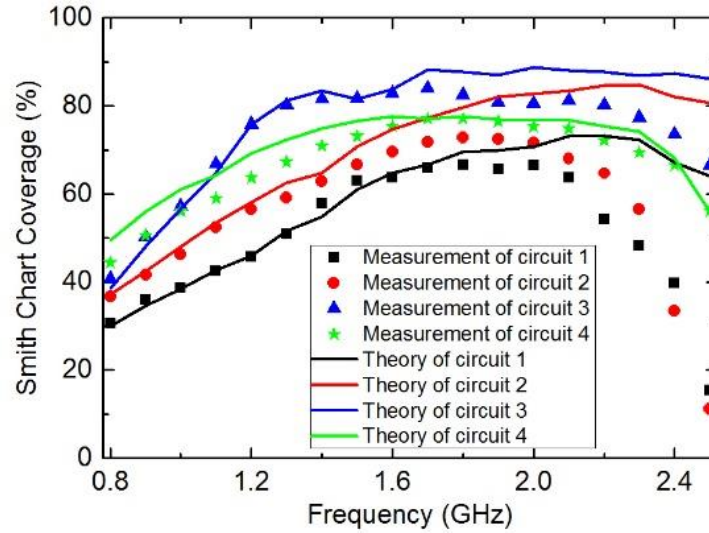
Figure 4.16: (a) Comparison of measured and theoretically calculated Smith chart coverage for four fabricated circuits.
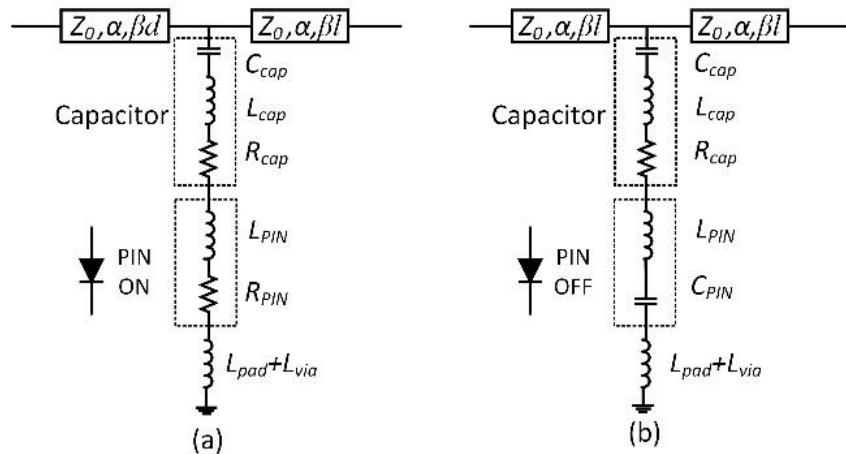
Figure 4.17: Equivalent circuit model of a unit circuit when PIN diode is turned (a) ON and (b) OFF.

In addition to the parasitic inductance, the series resistance is also a critical factor leading to the degradation of performance at high frequency. In a circuit with high standing wave, a small parasitic resistance will cause obvious loss problem due to the multipath loss. The sweep of resistance from 0 to 3 Ω leads to an increase of the loss before resonance frequency. The parametric study of the series resistance on the performance of EIS for all impedance states show that the increases of resistance reduces the Smith chart coverage more than 20% and increases the loss more than 10 times at high frequency.

In the circuit 1 to 3, PIN diode of SMP1320-079LF from Skyworks Solution Inc. is chosen, which has series inductance around 0.7 nH. Therefore, the total parasitic inductance should be around 1.5 nH after considering the inductance from a commercial capacitor (0.4 nH) and the inductance from the connection pads and via holes (0.4 nH). It will resonate with the loading capacitance near the operation frequency band. However, only 0.9 nH parasitic inductance was considered in the first experiment due to the inaccurate modeling for the parasitics. In addition, total series resistance should be around 3 Ω after taking into account R_{PIN} of 1 Ω from the PIN diode, and the series resistance of 2 Ω from the commercial capacitor and the connection pads. However, only 1 Ω parasitic inductance was considered in the first experiment. In summary, the inaccurate modeling of series inductance and series resistance lead to the deviation between theory and measurement at high frequency for circuit 1-3.

After considering the parasitic parameters in the design of PIN diode-based EIS, some degree of correction should be made on (4), (6) and (9). However, these complicated corrections can be done in the optimization process instead of the design procedure. By contrast, the EIS based on MEMS [139, 140] does not suffer from the parasitic problem, so that it can be designed at millimeter wave frequency band.

The first experiment (Fig. 4.15(a) - (c)) shows that the non-uniform topology not only has a smaller physical size, but also have a better Smith chart coverage than the uniform topology, which validates the effectiveness of the proposed non-uniform topology. In order to further eliminate the gap between measurement and theory at high frequency, a new non-uniform circuit is designed and optimized (Fig. 4.15(d)). Two steps are done to reduce the parasitic inductance. First, PIN diode of BAR95-02LS from Infineon Technologies with parasitic inductance of 0.2 nH is selected. Then, shorter and smaller connection pads and larger via are made to have minimum parasitic inductance

around 0.2 nH. Even so, the total parasitic inductance is around 0.8 nH, and the total parasitic resistance is around 3 Ω. However, they are not avoidable if commercial components are used.

Since the minimum parasitic inductance 0.8 nH is determined, the maximum loading capacitance will be limited to 2 pF so as to keep the resonance frequency at 4 GHz. From Fig. 4.4, we can see that this restriction will largely narrow the choices of loading capacitance. In other words, the small selectable capacitance will reduce the Smith chart coverage in the desired frequency band, especially for low frequency. As illustrated in Fig. 4.7, one solution to improve the Smith chart coverage is to increase the number of sections. In this work, we choose the total number of sections as 14, which includes one section of adjusting circuit and 13 sections of distributed circuit. One reason is that the improvement of Smith chart coverage is not obvious with section number more than 14. Another reason is that the test limitation with the tuner controller from Focus Microwave Inc. is 14 bits. It should be noted that the fabrication on wafer will not have so large limitation thanks to the small parasitic inductance, e.g. MEMS technique.

In circuit 4 (Fig. 4.15(d)), we use the same capacitance of 2 pF for all the capacitors in the non-uniform topology. Then PSO is applied to optimize the distances between sections, and the optimized circuit dimensions are listed in Table 4.2. Compared to circuit 3, the limitation of fixed loading capacitance in circuit 4 leads to a larger d in order to have as large as possible the Smith chart coverage. The circuit is bended to reduce the total size. Fig. 4.18 depicts the good match between measured and theoretical results of S parameters for two impedance states with all the PIN diodes are turned ON and OFF, respectively.

Table 4.2: Final dimension of non-uniform distributed EIS. Unit: capacitor: pF; impedance: Ω; distance: mm.

C_{a1}	2	d_1	8.26	d_8	4.49
C_{a2}	30	d_2	8.82	d_9	8.55
Z_{a1}, Z_{a2}	50	d_3	8.62	d_{10}	8.55
$Z_1 \sim Z_{14}$	74.4	d_4	8.82	d_{11}	7.98
$C_{d1} \sim C_{d13}$	2	d_5	8.82	d_{12}	8.58
d_{a1}	3	d_6	8.27	d_{13}	4.64
d_{a2}	2	d_7	8.75	d_{14}	8.82
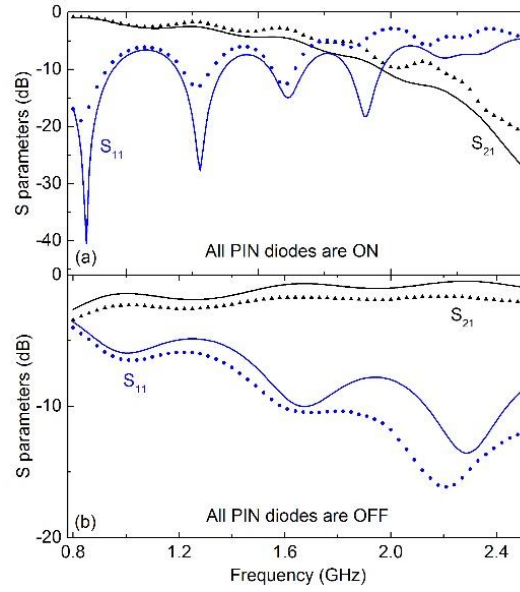
Figure 4.18: Comparison of measured and theoretical S parameters for impedance states with all PIN diodes are turned (a) ON and (b) OFF. Dots denotes measurement, while solid line denotes theory.

4.4   Evaluation

A variety of figures of merit (FOM) have been presented to evaluate the TMN [139-142, 145] and the EIS [146, 156, 177, 178] in previous works. Indeed, the core of a TMN is an EIS, therefore, the evaluation FOM for a TMN and an EIS can be studied together. Table 4.3 lists all the FOM that have been used to evaluate TMN or EIS. Certain FOM can be selected from them for specific application.

Tuning range

For either optimization or evaluation of an EIS, a quantized criterion is always helpful. Tuning range of EIS usually can be represented by Smith chart coverage [141, 142], uniformity factor [145], maximum VSWR [140], or maximum reflection coefficient [179]. Most of published work used one or two of them, however, each criterion has its own pros and cons. None of them can describe the tuning range alone. In this work, we list all of them according to their significance.
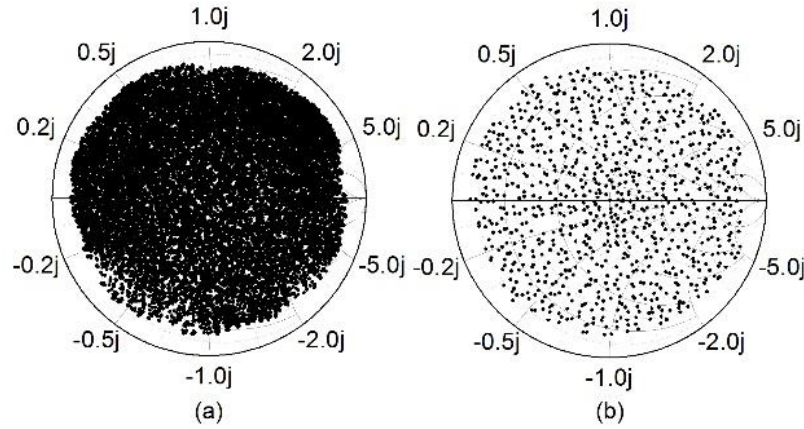
Figure 4.19: (a) All 16384 measured impedance points; (b) Selected points for the calculation of Smith chart coverage.

Smith chart coverage

After removing the redundant points as described in the definition of Smith chart coverage, useful impedance points are selected from the measured points (Fig. 4.19(a) and (b)). The measured and simulated Smith chart coverage are compared in Fig. 4.16. The Smith chart coverage of circuit 4 is lower than circuit 3 mainly because of the limitation of loading capacitance. However, the measured results show a good match with simulation after eliminating the impacts from Bragg cutoff frequency and resonance problem, the difference is within 5%. In other words, the design of the EIS is reliable after considering the accurate parasitic parameters.

The measured and theoretical impedance distribution on Smith chart at several frequencies are compared in Fig. 4.20. Since the impedance generated by the EIS is sensitive to the parasitic parameter, it is difficult to have exact point to point matching between the theory and measurement, especially for the EIS with soldered commercial components. For the PIN-diode based EIS, the acceptable differences presented in Fig. 4.18 and Fig. 4.20 indicate that the theory can be used to predict the real performance approximately and statistically.

Uniformity factor

An ideal distribution should have Smith chart coverage as high as possible, at the same time, have uniformity factor as low as possible. The calculation of uniformity factor has been described in section 4.2. A lower uniformity factor indicates a better distribution on Smith chart. N_r of 16 and

N_θ of 64 are chosen to divide the Smith chart from radius and phase directions, respectively. As shown in Fig. 4.21, the measurement results show good match with theory.

Table 4.3: Summarization of criteria to evaluate TMN and EIS.

Criteria / Reference		Tunable Matching Network (TMN)					Electronic Impedance Synthesizer (EIS)				
		[139]	[140]	[145]	[141]	[142]	This work	[177]	[178]	[156]	[146]
Tuning range	Smith chart Coverage (subjective)	×							×	×	
	Smith chart Coverage (numerical)				×	×	×				×
	Maximum VSWR constant circle		×				×				
	Uniformity factor			×			×				
	Maximum reflection coefficient						×	×	×		
	bandwidth						×	×	×		×
	Loss	×	×	×	×		×	×			×
	Case study	×									
Power handling	Voltage distribution	×					×			×	
	P_1 dB point test						×		×		
Nonlinearity	Linearity test	×					×	×			
	Noise figure						×	×			
Other concerns	Tuning accuracy						×		×		
	Tuning resolution						×	×	×		
	tuning speed						×	×	×		
	Size, weight, ease of integration						×	×	×		
	Others: spurious oscillations, temperature drift						×	×			

Maximum VSWR

In practical application, it is important to have enough points for each constant VSWR circle, which is useful to check the performance of the DUT by varying the phase while the VSWR keeps constant. The VSWR is larger than 15 for 1.5 - 2.2 GHz, and larger than 10 for 1.2 - 1.4 GHz and 2.3 - 2.5 GHz. In fact, this criterion is not so accurate because of the subjective judgement on the irregular distribution.

Maximum reflection coefficient

Maximum reflection coefficient Γ refers to the radius of the farthest point away from the center of Smith chart. Compared to the previous three criteria, maximum Γ is most meaningless criterion, since it is only one impedance point that carries on very limit information. Fig. 4.22 depicts the comparison of required, estimated, theoretical and measured maximum Γ. As can be seen that the measurement results are close to the theory, and both of them are higher than the required Γ. The estimation of maximum Γ using (4.2) is lower than the required Γ particularly at low frequency, because the parasitic inductance limits the loading capacitance to 2 pF which is too small for the low frequency (Fig. 4.4). If no restriction is applied to the loading capacitance, the estimated maximum Γ should be larger than the requirement.

Bandwidth

Bandwidth describes the frequency range over which a minimum given Smith chart coverage, maximum uniformity factor, and maximum VSWR are satisfied. Bandwidth must be not wide when satisfying these harsh criteria. Nevertheless, we could choose different values for those three criteria according to different application. For the non-uniform topology in Fig. 4.15(d), the bandwidth is 800 MHz when we choose minimum Smith chart coverage as 60%, maximum uniformity factor as 500, and maximum VSWR as 10.
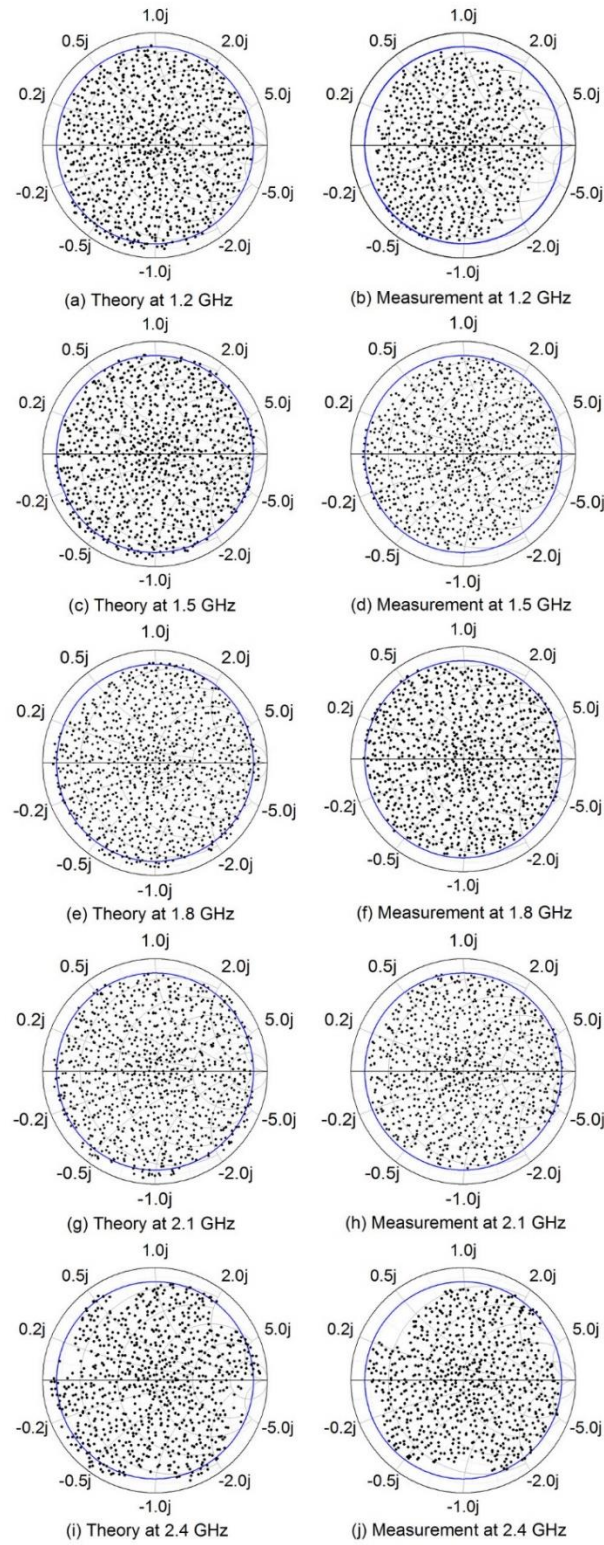
Figure 4.20: (a) Measured and (b) theoretical impedance distribution at 1.2 GHz; (c) Measured and (d) theoretical impedance distribution at 1.5 GHz; (e) Measured and (f) theoretical

impedance distribution at 1.8 GHz; (g) Measured and (h) theoretical impedance distribution at 2.1 GHz; (i) Measured and (j) theoretical impedance distribution at 2.4 GHz. The blue circle represents the constant VSWR=15 circle ($|\Gamma|$=0.875).
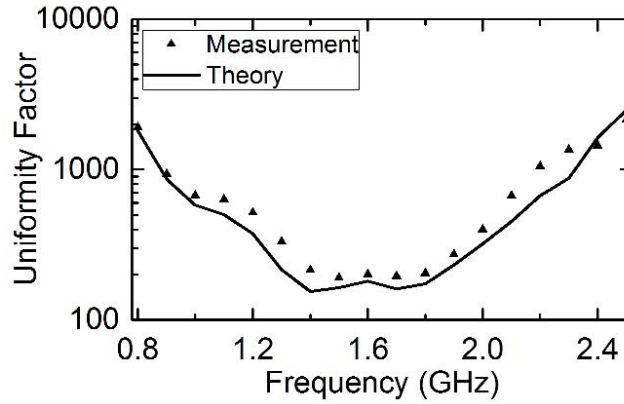
Figure 4.21: The comparison of measured and theoretically calculated uniformity factor.
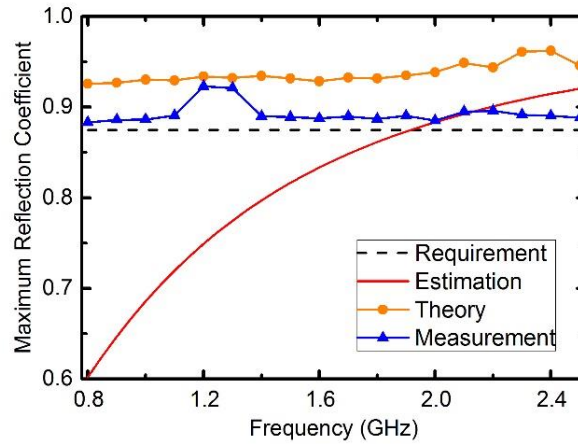
Figure 4.22: Comparison of required Γ (black dash line), estimated maximum Γ (red solid line), theoretical maximum Γ (orange solid line with circle marker), and measured maximum Γ (blue solid line with triangle marker).

Loss

As discussed in Section 4.2.1, the measurable loss is considered as a reference for the load tuner scenario. The sources of the loss of the EIS includes dielectric loss, conductive loss, parasitic R_{PIN} from PIN diode, equivalent resistance of capacitor and connection pads. In addition, parametric studies show that it will be largely affected by the resonance caused by the parasitic inductance and

loading capacitance. Fig. 4.23(a) and (b) show the theoretical and the measured loss for the selected impedance states at 1.5 GHz, it can be seen that the loss increases with the increases of reflection coefficient because of the multipath loss at high reflection condition. The comparison of measured and theoretical mean loss at different frequencies (Fig. 4.23(c)) presents good match between them.
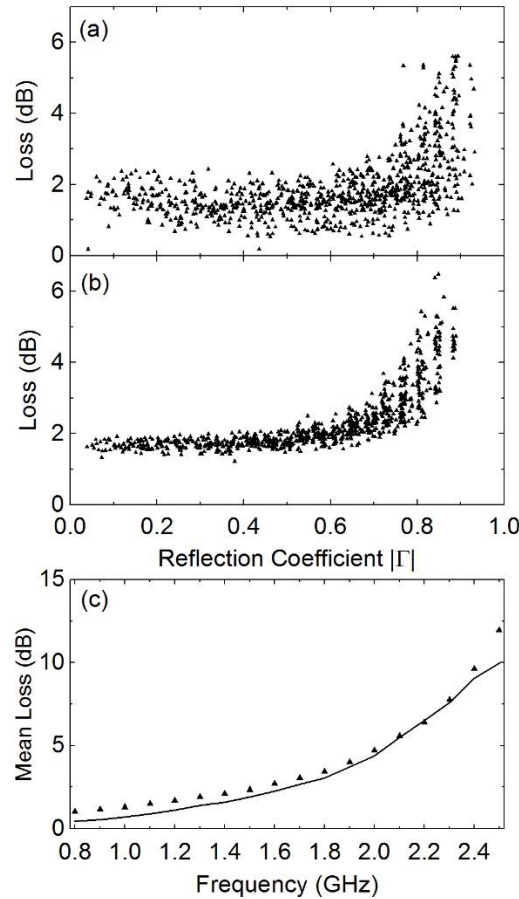
Figure 4.23: (a) Theoretical and (b) measured loss for the selected impedance points at 1.5 GHz; (c) Comparison of theoretical and measured mean loss over frequency.

Power handling analysis

Voltage distribution theory for a traditional distributed EIS has been developed in section 4.2, similar theory can be applied to the proposed non-uniform distributed EIS, and maximum peak voltage at the position of each diode can be monitored. Voltage distribution of two limiting Γ states, called the highest Γ (0.91) and lowest Γ (0.01), with 0.5 watt input power are shown in Fig. 4.24 (a) and (b). Simulations with ADS have been presented to validate the theory, because it is not able to measure the voltage distribution in real circuit. As can be seen that the theory matches the

simulation very well. Due to the inhomogeneous property, the standing wave that presents at the input port (steady state) is not as same as the one exists along the transmission line. Two observations can be highlighted from Fig. 4.24. Firstly, large peak voltage always appears at the position of PIN diode with the OFF state. Since for the ON state, the series resistance is small, small voltage will be assigned to the PIN diode according to the power divider theory. In the OFF state, compared to the loaded capacitance C_d, total capacitance of PIN diode C_T is small. According to the theory of two series capacitor, PIN diode will get most of the voltage. Secondly, the VSWR presented at the input port is not the same as the VSWR existing along the transmission line. For instance, in the lowest Γ case, the equivalent voltage standing wave presented at the input port is 1.02, while the standing wave existing in the transmission line is around 9.08.
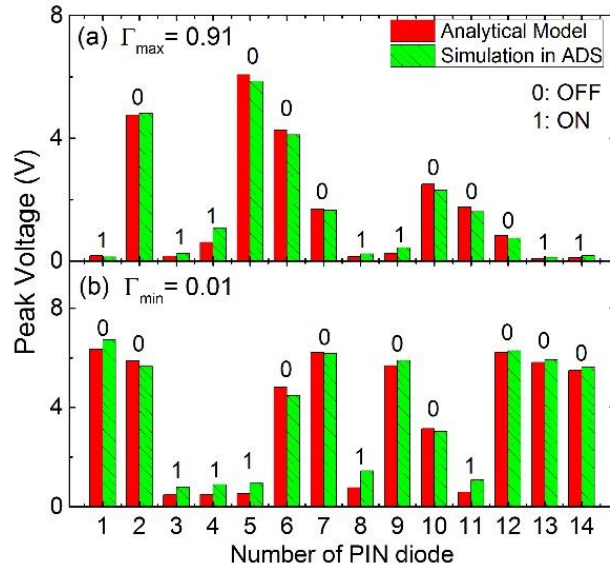
Figure 4.24: Comparison of theoretical and simulated voltage distribution along the transmission line under average power of 0.5 watt for the (a) highest Γ state ($|\Gamma|$=0.9) and (b) lowest Γ state ($|\Gamma|$=0.01).

The nonlinearity of the EIS is mainly caused by those PIN diodes with OFF states. Larger maximum peak voltage existing on the transmission line will lead to a lower power handling capacity. Under a linear operation power, the maximum peak voltage is proportional to the input power (dBm). The voltage distribution theory has been proved to be able to predict the P1dB without doing the actual power handling test [168]. As depicted in Fig. 4.25(a), 20 impedance states with large maximum peak voltage have been chosen for Harmonic Balance simulation in ADS with

input power of 0.5 watt. Then linear fitting (solid line) is applied for the 20 simulations, and the extension line (dash line) can be used to predict the P1dB for impedance states with low maximum peak voltage. And this linear fitting has been proved can fit all the impedance states [168]. It shows that the PIN diode-based non-uniform EIS has P1dB higher than 33 dBm. In other words, the EIS can handle 0.5 watt average power linearly.

Nonlinearity analysis

Ideal EIS should be as linear as possible. The IIP3 can be applied to express the nonlinearity of the EIS. Similar to the prediction of P1dB, the IIP3 can also be estimated from a small amount of simulation in ADS without doing actual IMD measurement. As illustrated in Fig. 4.25(b), the IIP3 of the PIN diode-based non-uniform EIS is higher than 53 dBm.
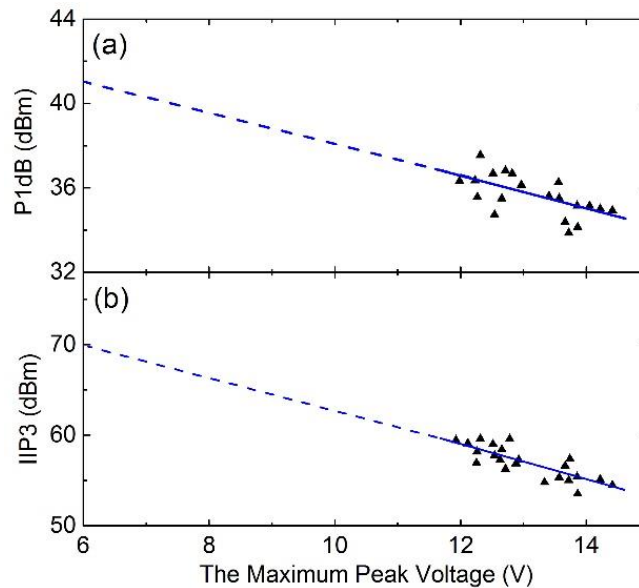
Figure 4.25: Simulated relationship of (a) P1 dB and (b) IIP3 with the maximum peak voltage along the transmission line for 20 impedance points under input power of 0.5 watt. Solid line is the linear fitting curve of the selected 20 points, while the dash line is the extension of the fitting curve.

Noise figure

For any active device, high noise figure stands for significant influence to the noise performance of the system. The EIS will introduce noise to the practical application, therefore the noise performance of the EIS itself is significant. In this work, noise source, noise analyzer and a tuner

controller along with an automation program are presented to measure the noise figure of the EIS automatically. Fig. 4.26 shows the results for 816 selected useful impedance states. As can be seen that, the noise figure of the EIS increases while the reflection coefficient increases. Although the EIS has maximum noise figure of 17.5 dB at 1.5 GHz, it can be calibrated in the noise characterization system without affecting the accuracy of the noise figure test for the DUT.

Other concerns

Repeatability

Repeatability indicates the differences of S-parameters among several time measurements for the same impedance state. It shows how well the EIS can repeat each impedance state. The EIS used in non-real-time measurement system requires pre-calibration. Therefore, it is critical for the EIS to repeat the same impedance state, which means that the EIS should be stable. The repeatability test must be done over a large number of impedance states and a range of frequencies to find the worst case. The proposed non-uniform EIS exhibits at least 55 dB repeatability. It will make the test data precise enough when evaluating the PA or radio module.

Tuning resolution

Tuning resolution of the EIS refers to the resolution of impedance points generated by the EIS. An EIS with high resolution is important for precise measurement. Traditional EIS exhibits irregular impedance pattern with unpredictable jumping of impedance states so that it is difficult to have an exact value for tuning resolution. However, the tuning resolution can be described by the pre-defined density in the discretization process when the Smith chart coverage is calculated.

Tuning speed

Tuning speed is the time taken by the impedance synthesizer moves from one impedance state to the next one. The switching time of the selected PIN diode is in the order of 0.1 µs, so the switch time of the EIS from one state to another state is also in the same order. In the pre-calibrated procedure, the speed is mainly limited by the VNA and also the reading via GPIB interface, in the order of 0.1 s. In the real application, the speed is limited by the controller, which is in the order of 10 ms. Even so, it only need a few seconds to finish the measurement with 1000 useful impedance states, which is much faster than electromechanical tuner. In other words, the EIS can be used in the application where high measurement throughput is required.
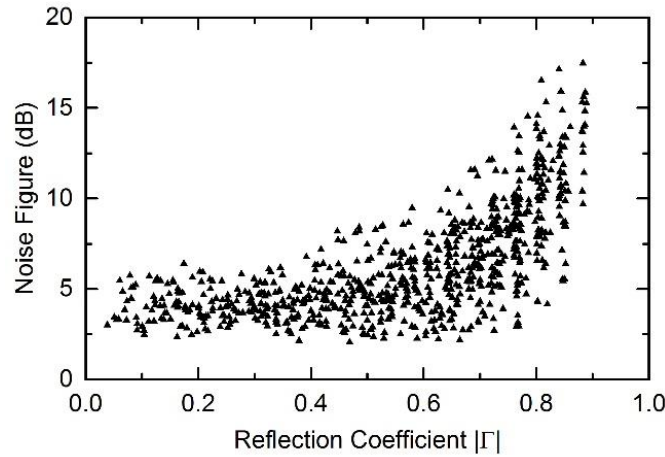
Figure 4.26: Noise figure of the proposed non-uniform EIS at 1.5 GHz for 816 selected impedance states.

Temperature drift

Temperature drift can describe how the performance of the EIS changes when temperature varies. Experiments with thermotank show that when temperature varies from -40 to 40 °C, the repeatability keeps 50 dB, which means that the EIS works stable when temperature changes in this range.

Cost, size, weight, ease of integration

The advantages of EIS compared to electromechanically tuner and active tuner are the size and weight. They are essential for the on-wafer test. Although the size of the EIS in this work is around 36 mm × 32 mm, the whole circuit can be further integrated on the wafer for high frequency if other switching technique, e.g. MEMS, can be adopted.

4.5   Conclusion

We have presented a semi-closed form design procedure for a uniform electronic impedance synthesizer (EIS). Initial values and boundaries of multiple parameters have been determined in this procedure. Then Particle Swarm Optimization (PSO) method is introduced to solve the multi-parameter optimization problem of the proposed non-uniform the EIS. The effectiveness of the proposed non-uniform topology and the optimization method are validated by experiments. Experimental results show that the proposed non-uniform distributed topology not only has better

Smith chart coverage, but also has smaller size than uniform topology. Parametric studies demonstrate that inappropriate consideration of parasitic parameters can degrade the performance at high frequency. With accurately modeling of parasitics, the measurement of non-uniform EIS present a good match with the theory.

This work provides a computer aided design for the non-uniform EIS. The successful utilization of PSO can shorten the development period of an EIS to a few hours. Different criteria can be configured in the fitness function of the optimization process so as to satisfy specific requirements for different applications. Furthermore, comprehensive figures of merit (FOM) are studied and summarized, different FOM can be chosen to evaluate the EIS according to their application. Although we designed a general purpose EIS in this work, the PSO and complete list of FOM give more freedom to design EIS for different purposes.

CHAPTER 5   TWO-DIMENSIONAL TUNING CIRCUITS AND APPLICATIONS

In this chapter, the theory of two-dimensional (electrical and magnetic) tuning circuits using a ferrite-based hybrid NLTL technique will be proposed and studied. Firstly, the hybrid NLTL technique will be analyzed in both time and frequency domain. Secondly, an extraction method of complex permittivity and permeability will be developed based on the S-parameters. The theory will then be validated by experiments and simulations for the case of a non-magnetic material, NLTL with varactors as well as YIG-based microstrip line. Finally, small signal and large signal applications of two-dimensional tuning circuits will be discussed.

5.1   Analysis of hybrid NLTL technique

In order to characterize the periodically loaded structure of a hybrid NLTL, both time domain and frequency domain analyses are carried out. The time domain analysis gives the phase velocity as well as characteristic impedance. The frequency domain method Floquet Theorem [23] is applied to find out the Bragg cutoff frequency [51], since the frequency domain analysis is more suitable to analyze the lowpass nature of a periodically loaded structure.

5.1.1 Time domain analysis

Although this time domain analysis is based on a fully distributed hybrid NLTL, which is a transmission line consisting of uniformly distributed nonlinear shunt capacitance, the conclusions are also validated for a ferrite-based transmission line loaded with varactor periodically when the unit length is much smaller than the wavelength [51]. The hybrid NLTL can be characterized by a variable inductance per unit length L(i) and a variable capacitance per unit length C(v), as shown in Fig. 5.1.
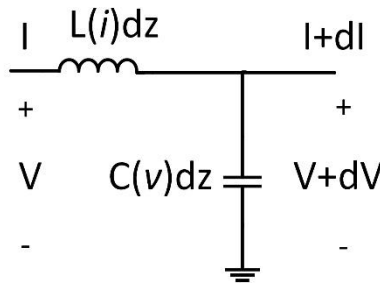
Figure 5.1: Equivalent circuit model of fully distributed hybrid NLTL per unit length.

Assuming V and I are differentiable single-valued functions of distance z and time t, and applying Kirchhoff's voltage and current law:

$$\frac{\partial V}{\partial z} + L(i)\frac{\partial I}{\partial t} = 0 \tag{5.1}$$

$$\frac{\partial I}{\partial z} + C(v)\frac{\partial V}{\partial t} = 0 \tag{5.2}$$

Since the principle of superposition of forward wave and backward wave are not applicable for nonlinear differential equations, the method of characteristics is applied in this case [39, 180]. A linear combination of these two equations can be made with undetermined multiplier λ

$$\lambda\frac{\partial V}{\partial z} + C(v)\frac{\partial V}{\partial t} + \frac{\partial I}{\partial z} + \lambda L(i)\frac{\partial I}{\partial t} = 0 \tag{5.3}$$

$$\lambda = \pm\sqrt{\frac{C(v)}{L(i)}} \tag{5.4}$$

By introducing a nonlinear mapping

$$\partial z = \partial\alpha + \partial\beta \tag{5.5}$$

$$\partial t = \sqrt{L(i)C(v)}\partial\alpha - \sqrt{L(i)C(v)}\partial\beta \tag{5.6}$$

four ordinary differential equations, also called characteristic equations, can be obtained

$$\frac{\partial z}{\partial\alpha} = \frac{1}{\sqrt{L(i)C(v)}}\frac{\partial t}{\partial\alpha} \tag{5.7-1}$$

$$\frac{\partial V}{\partial\alpha} = -\sqrt{\frac{L(i)}{C(v)}}\frac{\partial I}{\partial\alpha} \tag{5.7-2}$$

$$\frac{\partial z}{\partial\beta} = -\frac{1}{\sqrt{L(i)C(v)}}\frac{\partial t}{\partial\beta} \tag{5.7-3}$$

$$\frac{\partial V}{\partial\beta} = \sqrt{\frac{L(i)}{C(v)}}\frac{\partial I}{\partial\beta} \tag{5.7-4}$$

From (5.7-1) and (5.7-3), the propagation velocity of the forward and backward traveling wave can be obtained as

$$vp = \pm\sqrt{\frac{1}{L(i)C(v)}} \tag{5.8}$$

From (5.7-2) and (5.7-4), the characteristic impedance of the forward and backward traveling wave can be obtained as

$$Z = \pm\sqrt{\frac{L(i)}{C(v)}} \tag{5.9}$$

5.1.2 Floquet analysis
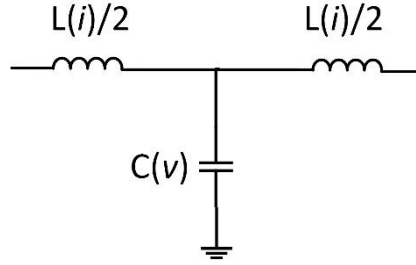
Figure 5.2: Equivalent LC circuit model of unit cell of periodically loaded hybrid NLTL.

Floquet analysis is applied to the periodically loaded hybrid NLTL to capture the lowpass nature of the structure [23, 51]. Fig. 5.2 shows the equivalent LC circuit model of the unit cell of hybrid NLTL, then the ABCD matrix can be written as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 - \omega^2 \dfrac{L(i)C(v)}{2} & j\omega L_t - \dfrac{j\omega^3 L^2 C(v)}{4} \\ j\omega C(v) & 1 - \omega^2 \dfrac{L_t C(v)}{2} \end{bmatrix} \tag{5.9}$$

By using a Floquet analysis, we can obtain the dispersion equation

$$\cosh(\gamma\,\mathrm{d}) = \frac{A+D}{2} = 1 - \omega^2 \frac{L(i)C(v)}{2} \tag{5.10}$$

Since the right-hand side of (5.10) is real, the solution will be either $\alpha = 0$ or βd = (0 or π). While in the latter case, there is no propagation along the transmission line. By solving the dispersion

equation under the condition of $\beta d = (0 \text{ or } \pi)$, the approximate closed-form expression of Bragg cutoff frequency can be obtained [51]

$$\omega_{Bragg} = \frac{2}{\sqrt{L(i)C(v)}} \tag{5.11}$$

It can be seen that the lowpass characteristic is performed in the periodically loaded hybrid NLTL.

5.2 Study of ferrite

The hybrid NLTL of interest in this work is based on a ferrite substrate. This section will explain the operation principle of ferrite. As is well known that, an electron has two properties: charge and spin. In most solids, the spins of electrons usually occur in pairs but with opposite directions so-called spin up and spin down, resulting in a negligible net magnetic moment. In a magnetic material, e.g. ferrite, although the number of spin up and spin down are unpaired, the random orientation leads to a small net magnetic moment. When an external magnetic field is applied, the dipole moments will align along the same direction of magnetic field, a large magnetic moment will be generated.

Two frequency concepts will be used in the following analysis [23]. Larmor frequency or precession frequency ω_0 can be expressed as

$$\omega_0 = \mu_0 \gamma H_0 \tag{5.12}$$

where μ_0 is the permeability of vacuum, γ is the gyromagnetic ratio, H_0 is the applied external magnetic field. And another frequency concept can be expressed as

$$\omega_m = \mu_0 \gamma M_s \tag{5.13}$$

where M_s is the dc saturation magnetization. The relationship of magnetization M and internal magnetic field H can be expressed with a tensor susceptibility $[\chi]$,

$$\bar{M} = [\chi]\bar{H} = \begin{bmatrix} \chi_{xx} & \chi_{xy} & 0 \\ \chi_{yx} & \chi_{yy} & 0 \\ 0 & 0 & 0 \end{bmatrix} \bar{H} \tag{5.14}$$

where the tensor elements can be calculated as

$$\chi_{xx} = \chi_{yy} = \frac{\omega_0 \omega_m}{\omega_0^2 - \omega^2} \tag{5.15-1}$$

$$\chi_{xy} = -\chi_{yx} = \frac{j\omega\omega_m}{\omega_0^2 - \omega^2} \tag{5.15-2}$$

According to the relationship between the magnetic flux density B and magnetic field H, we can obtain

$$\bar{B} = \mu_0(\bar{M} + \bar{H}) = [\mu]\bar{H} = \mu_0([U] + [\chi])\bar{H} \tag{5.16}$$

then the permeability tensor $[\mu]$ with magnetiv field bias in z direction can be given as

$$[\mu] = \begin{bmatrix} \mu & jk & 0 \\ -jk & \mu & 0 \\ 0 & 0 & \mu_0 \end{bmatrix} \tag{5.17}$$

where

$$\mu = \mu_0(1 + \chi_{xx}) = \mu_0(1 + \chi_{yy}) = \mu_0(1 + \frac{\omega_0 \omega_m}{\omega_0^2 - \omega^2}) \tag{5.18-1}$$

$$k = -j\mu_0\chi_{xy} = j\mu_0\chi_{yx} = \mu_0\frac{\omega\omega_m}{\omega_0^2 - \omega^2} \tag{5.18-2}$$

Then the effective permeability can be calculated as

$$\mu_e = \frac{\mu^2 - k^2}{\mu} \tag{5.19}$$

As can be seen in (5.18), when the operation frequency ω equals to ω_0, the μ and k are infinite, this phenomenon is called gyromagnetic resonance.

By considering the loss of the ferrite, the resonance frequency becomes complex $\omega_0 \to \omega_0 + j\alpha\omega$, where α is the damping factor. Then the susceptibilities in (5.15) becomes complex

$$\chi_{xx} = \chi'_{xx} - j\chi''_{xx} \tag{5.20-1}$$

$$\chi_{xy} = \chi'_{xy} + j\chi''_{xy} \tag{5.20-2}$$

And the elements of permeability tensor in (5.18) also become complex

$$\mu = \mu' - j\mu''$$
(5.21-1)

$$k = k' - jk''$$
(5.21-2)

The effective permeability can be calculated as

$$\mu_e = \frac{\mu'^2 - k'^2}{\mu'}$$
(5.22)

The linewidth of ferrite ΔH is related to the damping factor. In the curve of χ''_{xx} versus magnetic field bias H_0, the linewidth is defined as the width of H when the magnitude of χ''_{xx} decreases to a half of its peak, and it can be calculated as

$$\Delta H = \frac{\Delta \omega_0}{\mu_0 \gamma} = \frac{2\alpha\omega}{\mu_0 \gamma}$$
(5.22)

A small linewidth represents a low loss. For the YIG used in this work, the linewidth is around 17 Oe, and the saturation magnetization $4\pi M_s$ is 1780 Oe. Fig. 5.3 shows the relationship of permeability tensor elements and effective permeability with the external applied magnetic field at an operation frequency of 12.5 GHz, the effective permeability is calculated based on (5.22).
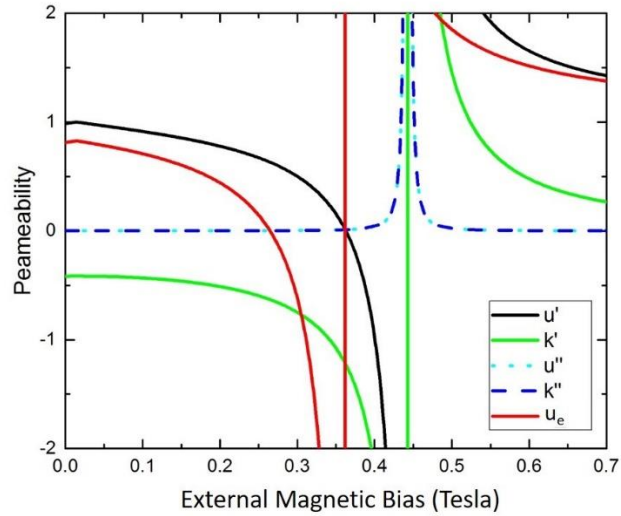
Figure 5.3: Permeability tensor elements and effective permeability versus magnetic bias.

When the magnetic bias is perpendicular to the ferrite plate (in z direction), the internal magnetic bias H_i is related the shape of the ferrite and the direction of external magnetic bias, it can be expressed as [23]

$$H_i = H_0 - N\,M \tag{5.23}$$

where $N = Nx$, Ny, or Nz represents the demagnetization factor of external bias in different direction. Different ferrite shapes result in different demagnetization factors, and they have the relationship of $Nx + Ny + Nz = 1$. Kittel's equation

$$\omega_r = \mu_0 \gamma \sqrt{[H_0 + (N_x - N_z)M_s][H_0 + (N_y - N_z)M_s]} \tag{5.24}$$

can be used to calculate the gyromagnetic resonance frequency. Based on (5.24), Fig. 5.4 shows a linear relationship between gyromagnetic resonance frequency and external magnetic bias in z direction.
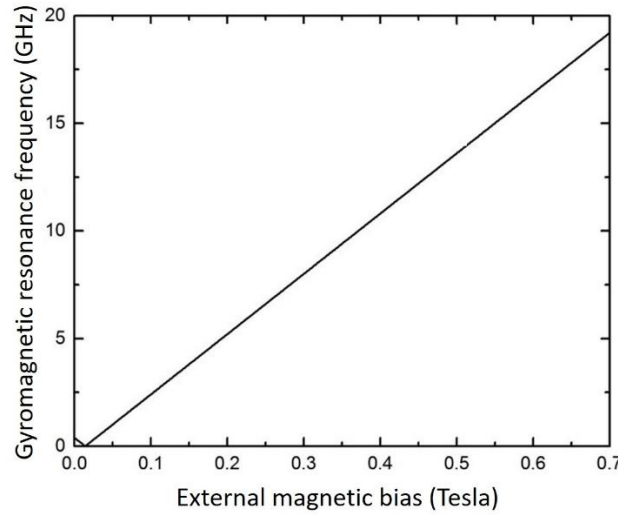
Figure 5.4: Gyromagnetic resonance frequency versus external magnetic bias.
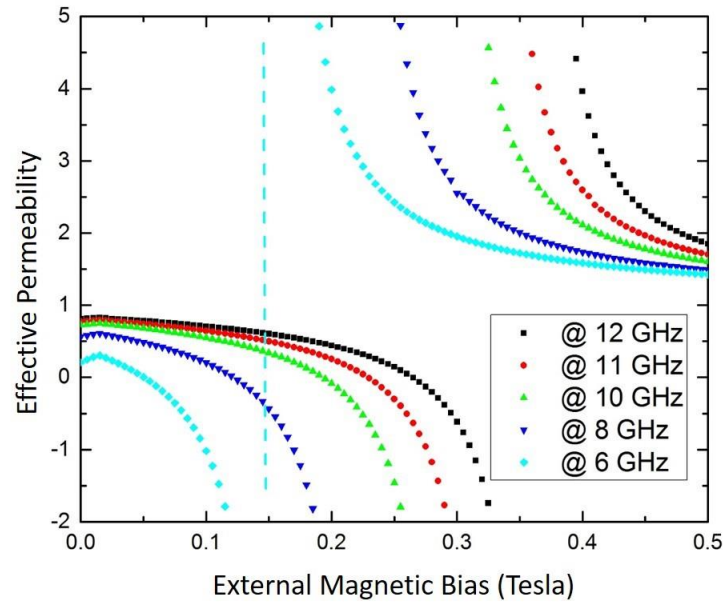
Figure 5.5: Effective permeability versus external magnetic bias at different operation frequency.

Fig. 5.5 shows the relationship of effective permeability with the external magnetic bias at different operation frequencies. As can be seen that, in the tunable circuit application, the effective permeability can be tuned from 1 to almost 0, and the magnetic bias will be swept from 0 Tesla to a certain value less than the corresponding magnetic field of gyromagnetic field.
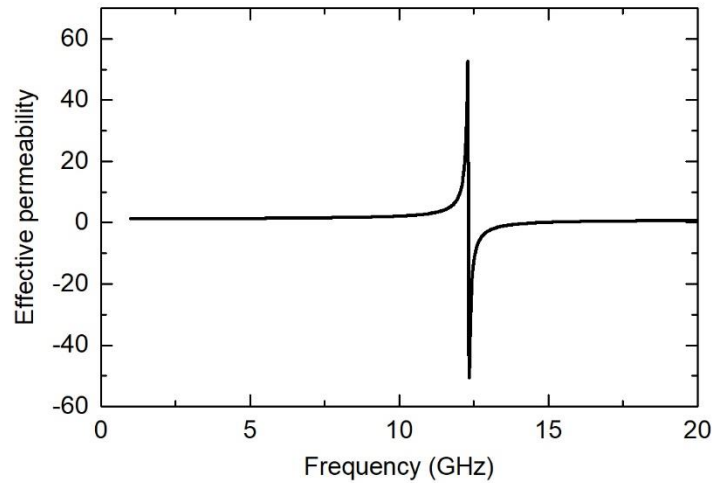
Figure 5.6: Effective permeability versus operation frequency at 0.44 tesla magnetic bias condition.

Fig. 5.6 shows the relationship of effective permeability with the operation frequency at 0.45 Tesla external magnetic bias. It can be seen that the YIG is very dispersive when close to the gyromagnetic resonance frequency. When the magnetic bias increases, the corresponding gyromagnetic resonance frequency increases, which results in the influence at low frequency. Therefore, for a tunable circuit, the operation frequency is higher than the gyromagnetic resonance.

5.3 Parameters extraction of complex permittivity and permeability

Prior to the design of a hybrid NLTL, the characterization of ferrite material over a wide range of frequencies should be studied first. A tremendous amount of methods [181-195] have been used to extract the complex permittivity and permeability from the measured S parameters of the material sample. As shown in Fig. 5.7, three measurement setups are usually used for the measurement of S parameters, namely free space measurement [191, 196], air-filled coaxial configuration [192] and waveguide configuration [185, 193]. The first two techniques are based on TEM propagation mode in a broadband frequency range, while the last one is based on TE_{10} mode with a limited frequency range.
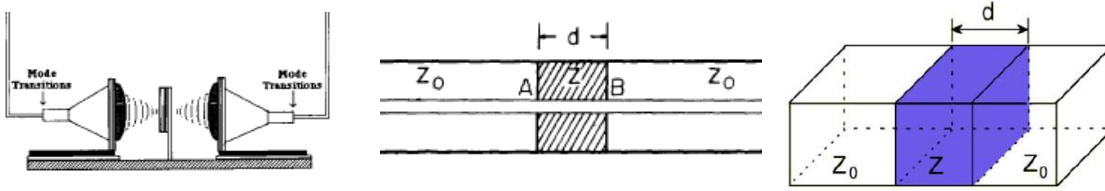
Figure 5.7: (a) Free space measurement [196], (b) air-filled coaxial line configuration [192], (c) waveguide configuration [185].

The conventional transmission-reflection (T/R) method is the Nicolson-Ross-Weir (NRW) method [181, 182, 192, 193], it gives closed-form solutions. However, one or more resonances are observed in the extracted parameter at frequencies corresponding to integer multiples of one-half wavelength, as shown in Fig. 5.8. This phenomenon has been investigated in [188], because the phase of S_{11} becomes unstable and uncertain when the magnitude of S_{11} close to 0, so as to result in the ambiguity problem. Alternative methods have been studied, including zero-order and high-order approximation method [188], phase unwrapping method [185, 186], iterative method [182, 183], 1st order regression [184], Kramers-Kronig technique [194], multiline method [197, 198]. However, most of the methods only work for certain scenarios, either assume the permeability as one or do

not have a unique and stable solution according to different tolerance in numerical methods. The analysis in this work is based on the modified NRW method and time domain smoothing technique.
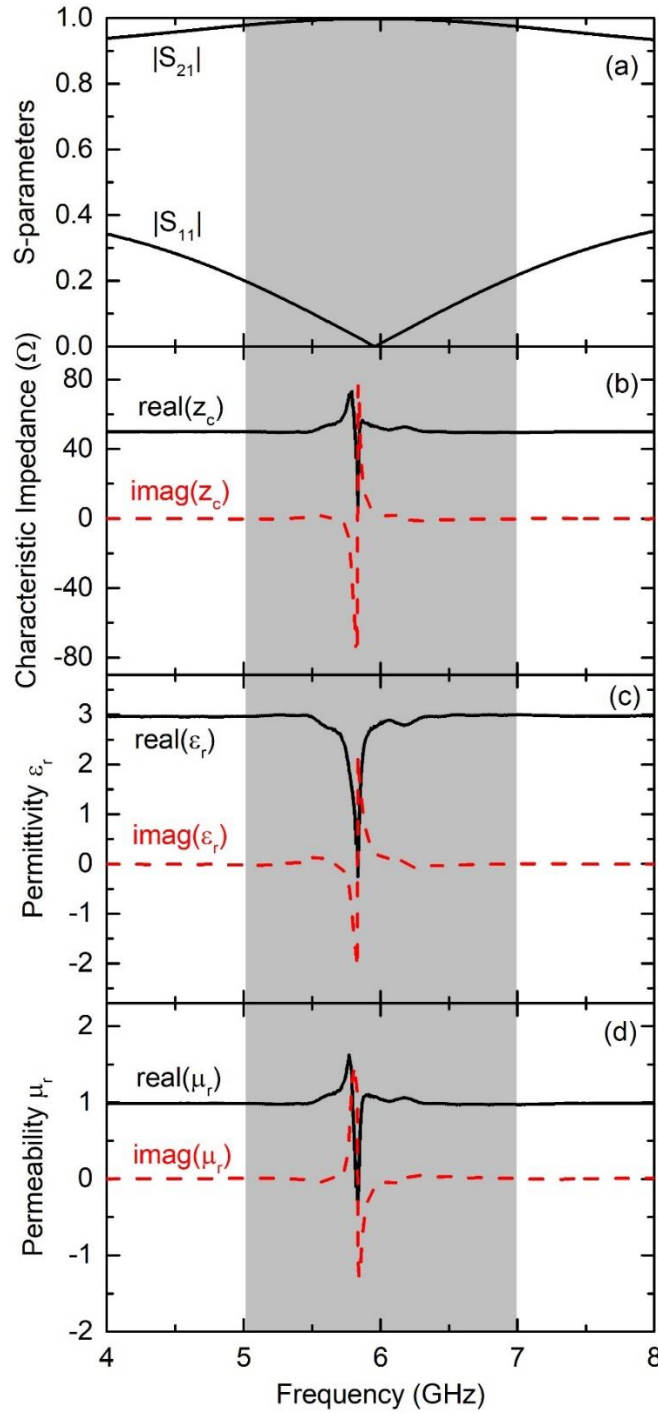
Figure 5.8: (a) Measured S-parameters, (b) extracted impedance, (c) extracted permittivity and (d) extracted permeability.

5.3.1　Methodology

5.3.1.1　Analysis of air-filled coaxial line configuration
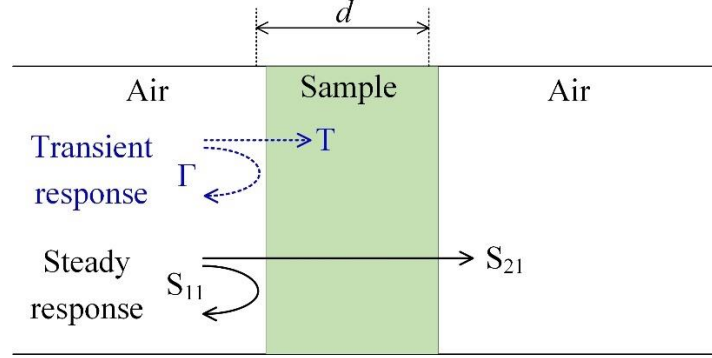
Figure 5.9: Diagram of setup of air-filled coaxial line.

In order to simplify the analysis, the calculation is based on the air-filled coaxial line with cutoff frequency at zero. As shown in Fig. 5.9, the reflection coefficient Γ at the interface of air and sample can be defined as

$$\Gamma = \frac{Z - Z_0}{Z + Z_0} = \frac{z_c - 1}{z_c + 1} = \frac{\sqrt{\mu_{eff} / \varepsilon_{eff}} - 1}{\sqrt{\mu_{eff} / \varepsilon_{eff}} + 1} \tag{5.25}$$

where Z is the non-normalized characteristic impedance of transmission line filled with sample, Z_0 is the reference impedance of the system, z_c is the normalized impedance. Then we have

$$z_c = \sqrt{\frac{\mu_{reff}}{\varepsilon_{reff}}} \tag{5.26}$$

The characteristic impedance can also be calculated from the measured S_{11} and S_{21} [181, 182, 184, 195]

$$z_c = \sqrt{\frac{(1 + S_{11})^2 - S_{21}{}^2}{(1 - S_{11})^2 - S_{21}{}^2}} \tag{5.27}$$

In the conventional NRW method, the reflection coefficient can also be calculated from the measured S_{11} and S_{21}

$$\Gamma = K \pm \sqrt{K^2 - 1} \tag{5.28}$$

where

$$K = \frac{S_{11}{}^2 - S_{21}{}^2 + 1}{2S_{11}} \tag{5.29}$$

The sign in (5.28) is determined by the restriction of $|\Gamma| \le 1$. It should be noted that Γ is a transient response while S_{11} is a steady response which can be explained by the multi-reflection theory [23]. Only when the length of the sample is infinite, Γ will equal to S_{11}. As can be seen from (5.29), K becomes algebraically unstable when S_{11} approaches zero, which in turn results in the ambiguity problem. Then the propagation/transmission factor T can be found as

$$T = \frac{S_{11} + S_{21} - \Gamma}{1 - (S_{11} + S_{21})\Gamma} \tag{5.30}$$

The propagation factor is also defined as [23]

$$T = e^{-\gamma d} = e^{-(\alpha + j\beta)d} \tag{5.31}$$

where γ is the propagation constant of wave through the material, α denotes attenuation constant, and β denotes phase constant. From (5.31), the propagation constant can be written as

$$\gamma = -\ln(T)/d \tag{5.32}$$

The propagation constant can be also expressed as

$$\gamma = \gamma_0 \sqrt{\mu_{reff} \varepsilon_{reff}} \tag{5.33}$$

where the propagation constant at vacuum γ_0 can be calculated from the wavelength at vacuum λ_0

$$\gamma_0 = j2\pi / \lambda_0 \tag{5.34}$$

If it is coaxial line, the λc will be considered as infinite. From (5.33) we can obtain

$$\sqrt{\mu_{reff} \varepsilon_{reff}} = \frac{\gamma}{\gamma_0} \tag{5.35}$$

From (5.26) and (5.35), we can obtain the analytical results of ε_{reff} and μ_{reff}

$$\varepsilon_{reff} = \frac{\gamma}{\gamma_0} / z_c \tag{5.36}$$

$$\mu_{reff} = \frac{\gamma}{\gamma_0} \cdot z_c \tag{5.37}$$

In the air-filled coaxial line and waveguide, the extracted ε_{reff} and μ_{reff} from the S-parameters equal to the parameters of the material. However, if a microstrip line or CPW line is used in the measurement, the extracted of ε_{reff} and μ_{reff} are the effective permittivity and permeability of the whole structure. The parameters of material then can be calculated based on the filling factor of the microstrip line or CPW line.

5.3.1.2 Analysis of microstrip line

For free space measurements, complex test setup as well as precise calibration are required, and the extraction range is limited by the test antennas. Microstrip line or CPW line however, can operate across a much broader frequency range. In this case, the line needs to be fabricated on the material that is used as a substrate.

In the previous analysis, the geometry structure of air-filled coaxial section and material filled section are the same, so that same geometrical factor can be applied. However in the measurement of a microstrip line, the section of connector and substrate are different, the geometrical factor of microstrip line must be considered. In this case, normalized impedance cannot be used due to the different reference, and the non-normalized impedance will be used instead. The impedance in (5.27) is normalized to the system impedance that is 50 Ω, so that the non-normalized impedance can be expressed as

$$Z = 50 \cdot \sqrt{\frac{(1+S_{11})^2 - S_{21}{}^2}{(1-S_{11})^2 - S_{21}{}^2}} \tag{5.38}$$

The non-normalized impedance of microstrip line can be calculated as

$$Z = \sqrt{\frac{\mu_{reff}\mu_0}{\varepsilon_{reff}\varepsilon_0}} \cdot g = \sqrt{\frac{\mu_{reff}}{\varepsilon_{reff}}} \cdot \bar{\eta}_0 g \tag{5.39}$$

where $\bar{\eta}_0$ is the wave impedance of free space, and g is the geometrical factor of microstrip line, it can be calculated as [23]

$$g = \frac{1}{2\pi} \ln\left(\frac{8d}{W} + \frac{W}{4d}\right), \text{ if } W/h \leq 1 \tag{5.40-1}$$

$$g = \frac{1}{\frac{W}{d} + 1.393 + 0.667 \ln\left(\frac{W}{d} + 1.444\right)}, \text{ if } W/h > 1 \tag{5.40-2}$$

From (5.38) and (5.39), we can obtain

$$\sqrt{\frac{\mu_{reff}}{\varepsilon_{reff}}} = 50 \cdot \sqrt{\frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2}} / (\bar{\eta}_0 g) \tag{5.41}$$

Then the analytical results of ε_{reff} and μ_{reff} can be obtained from (5.35) and (5.41)

$$\varepsilon_{reff} = \varepsilon_{reff}{}' + j\varepsilon_{reff}{}'' = \frac{\gamma}{\gamma_0} \cdot (\bar{\eta}_0 g) / \left(50 \cdot \sqrt{\frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2}}\right) \tag{5.42}$$

$$\mu_{reff} = \mu_{reff}{}' + j\mu_{reff}{}'' = \frac{\gamma}{\gamma_0} \cdot 50 \cdot \sqrt{\frac{(1+S_{11})^2 - S_{21}^2}{(1-S_{11})^2 - S_{21}^2}} / (\bar{\eta}_0 g) \tag{5.43}$$

Actually, the ε_{reff} and μ_{reff} are enough for the design of circuit if the same topology will be used. However, if material parameters are needed, one more step is needed in order to extract the parameters. The relationship between the effective permittivity of circuit and permittivity of the substrate can be expressed according to the parameters of the microstrip line [23]

$$\varepsilon_{reff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12\frac{h}{W}}}, \text{ if } W/h \geq 1 \tag{5.44-1}$$

$$\varepsilon_{reff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\frac{1}{\sqrt{1 + 12\frac{h}{W}}} + 0.04\left(1 - \left(\frac{W}{h}\right)^2\right)\right], \text{ if } W/h > 1 \tag{5.44-2}$$

By using the duality relationship, the relationship between the effective permeability of circuit and permeability of substrate can be expressed as

$$u_{reff} = \cfrac{1}{\cfrac{\mu+1}{2\mu} + \cfrac{1-\mu}{2\mu}\cfrac{1}{\sqrt{1+12\cfrac{h}{W}}}} \quad , \text{if } W/h \geq 1 \qquad (5.45\text{-}1)$$

$$u_{reff} = \cfrac{1}{\cfrac{\mu+1}{2\mu} + \cfrac{1-\mu}{2\mu}\left[\cfrac{1}{\sqrt{1+12\cfrac{h}{W}}} + 0.04\left(1-\left(\cfrac{W}{h}\right)^2\right)\right]} \quad , \text{If } W/h < 1 \qquad (5.45\text{-}2)$$

From (5.42) and (5.44), the permittivity of substrate can be extracted. Similarly, the permeability of substrate can be extracted from (5.43) and (5.45).

5.3.1.3 Time domain smoothing technique

As shown in Fig. 5.10(a), one or more resonances occur in the measured S-parameters, which results in the resonance in the extracted impedance z_c as well as ε_{reff} and μ_{reff} , so that the extracted parameters of material are not accurate. A time domain smoothing technique can be used to eliminate the resonance of extracted z_c and therefore eliminate the resonance in the extracted ε and μ [189].

Actually, in (5.36), the γ/γ_0 within the frequency range is flat, the resonance of extracted ε_{reff} shown in Fig. 5.10(c) is due to the resonance in the extracted impedance (Fig. 5.10(a)). The main idea of the time domain smoothing technique is to filter the time domain response of the resonance in the frequency domain. Firstly, the frequency range in real part and imaginary part of impedance (Fig. 5.10(a)) that covers the resonance will be truncated and transformed to the time domain by an inverse discrete Fourier transform (DFT) [189]

$$z'[n] = \sum_{k=0}^{N-1} Z'[k] \cdot e^{\frac{j2\pi nk}{N}} \qquad (5.46\text{-}1)$$

$$z''[n] = \sum_{k=0}^{N-1} Z''[k] \cdot e^{\frac{j2\pi nk}{N}} \qquad (5.46\text{-}2)$$

where k=0, 1, …, N-1 is the index in frequency domain, and n=0, 1, …, N-1 is the index in time domain, N is the number of measured data points. Z' and Z'' are the real part and imaginary part

of impedance, respectively. The time domain responses of the resonance in the real and imaginary parts of impedance are shown in Fig. 5.10(a) and (c). Then time domain rectangular windows are applied to filter the zero-time components, the modified time domain impedance can be expressed as

$$z'[n]\_windowed = w1[n] \cdot z'[n] \qquad (5.47\text{-}1)$$

$$z''[n]\_windowed = w2[n] \cdot z''[n] \qquad (5.47\text{-}1)$$

where the window functions $w1[n]$ and $w2[n]$ filter almost only the zero-time components, they can be defined as

$$w1[n], w2[n] = \begin{cases} 1, & n = 0,1,... \\ 0, & others \end{cases} \qquad (5.48)$$

The windows applied in the time domain means applying a lowpass filter in the frequency domain. In other words, this process only keeps the data in the starting frequency range and gets rid of the resonance data. The modified time domain impedances are shown in Fig. 5.10(b) and (d).
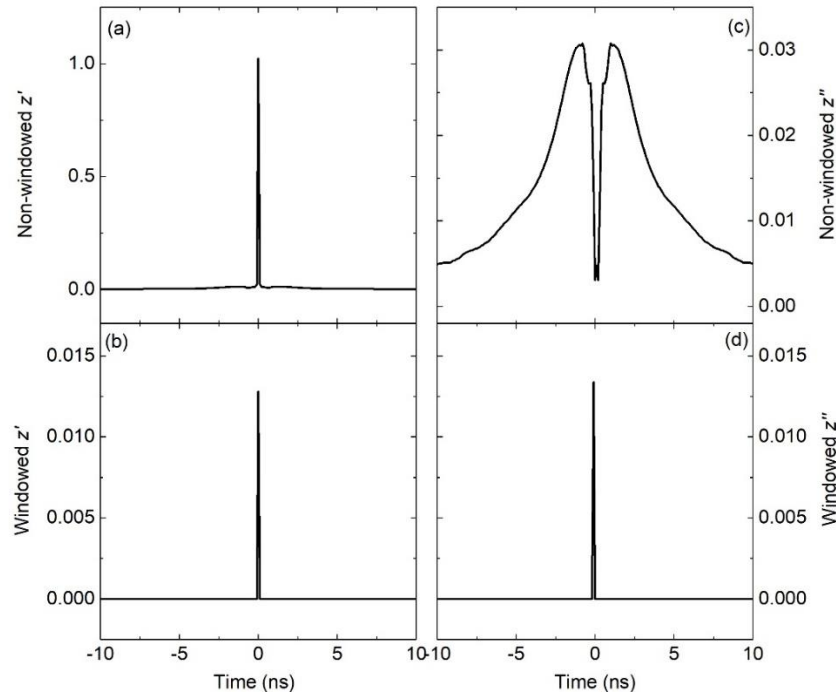
Figure 5.10: (a) Non-windowed and (b) windowed real part of time domain impedance, (c) Non-windowed and (d) windowed imaginary part of time domain impedance.

Finally, the time domain impedance will be transformed to the frequency domain by the forward DFT, and the modified response can be expressed as [189]

$$Z'[k]\_smoothed = \sum_{n=0}^{N-1} z'[n]\_windowed \cdot e^{-\frac{j2\pi nk}{N}}$$ (5.46-1)

$$Z''[k]\_smoothed = \sum_{n=0}^{N-1} z''[n]\_windowed \cdot e^{-\frac{j2\pi nk}{N}}$$ (5.46-2)

Since the time domain response of real and imaginary parts of impedance is different, the window width in (5.48) can be chosen differently, as long as the modified responses in (5.46) are smooth enough. Time domain window with $n = 0$ indicates that only zero-time components are preserved.

5.3.2 Validation

The validation of the parameter extraction theory is from three experiments and simulations. The first experiment is for a non-magnetic material, which is based on the measurement of a transmission line on the substrate of ROGERS 6002. The second experiment is based on the simulation of NLTL with commercial varactors in ADS, effective permittivity is extracted under different reverse bias conditions. The third experiment is based on the simulation of a microstrip line on YIG substrate in HFSS, effective permeability is extracted under different magnetic bias conditions. The effective permittivity and permeability will be used in the design of a YIG-based hybrid NLTL.

5.3.2.1 Non-magnetic material

A microstrip line on the substrate of ROGERS 6002 is designed and measured. The thickness of the substrate is 0.508 mm, the width and length of the microstrip line are 0.5 mm and 10 mm, respectively. The measured and modified frequency domain responses of impedance are shown in Fig. 5.11, as can be seen that the resonance in the truncated frequency range (gray region) is already eliminated, replaced by a flat curve.
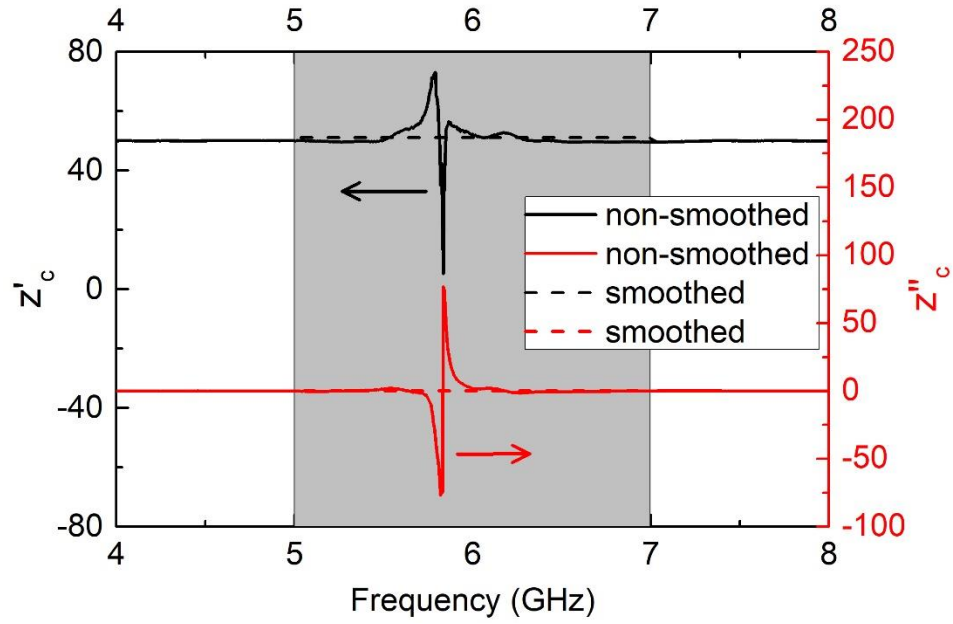
Figure 5.11: Frequency domain response of impedance with and without time domain smoothing technique. The gray region indicates the truncated frequency range.
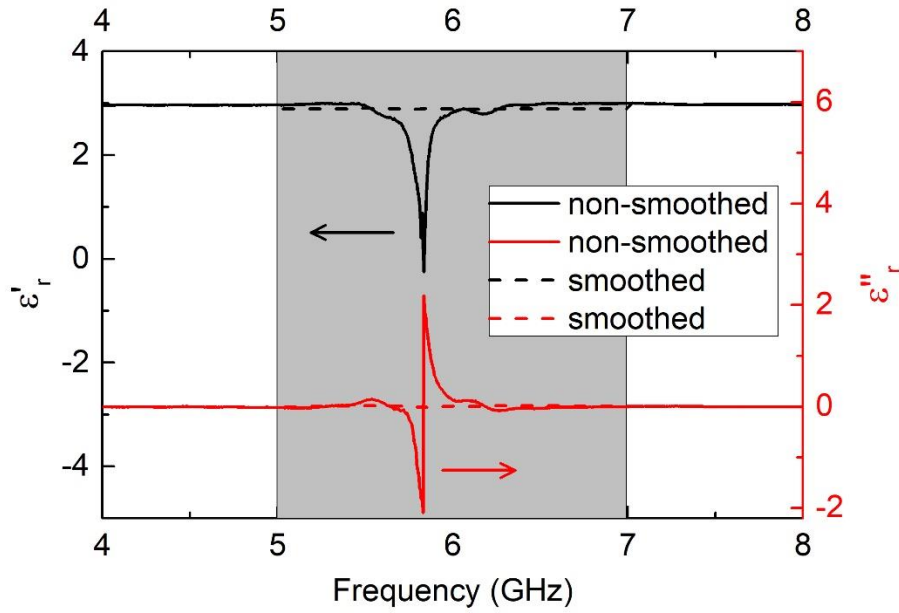
Figure 5.12: Extracted permittivity with and without time domain smoothing technique. The gray region indicates the truncated frequency range.

Based on the modified impedance, the extracted ε_{reff} and μ_{reff} are shown in Fig. 5.12 and Fig. 5.13, respectively. As can be seen that, the time domain smoothing technique is demonstrated as an efficient way to eliminate the resonance problem. By using the theory in Section 5.3.1, the extracted real part of the permittivity of the substrate is 2.92 ± 0.05, which is close to the datasheet 2.94 ± 0.05. If more resonances occur, a similar process could be done for each resonance [189].
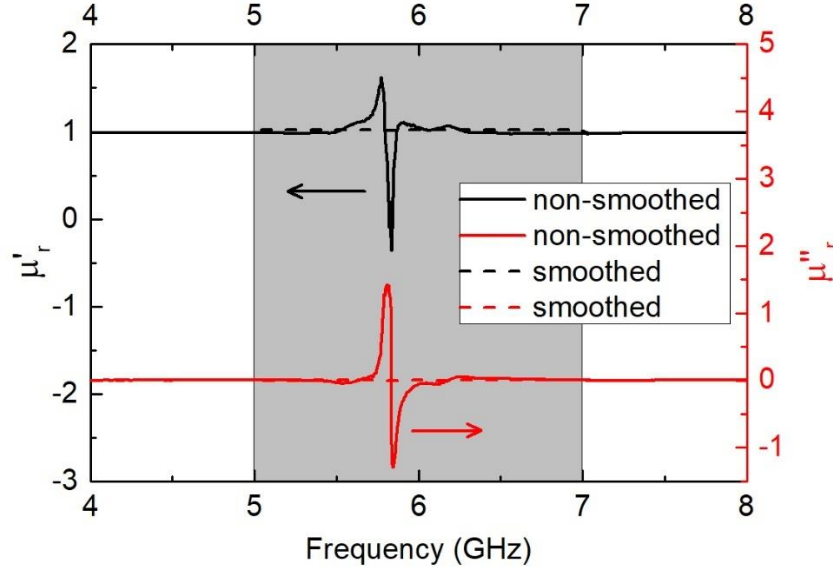
Figure 5.13: Extracted permeability with and without time domain smoothing technique. The gray region indicates the truncated frequency range.

5.3.2.2 NLTL with varactors

Since the NLTL loaded with varactors is a periodic structure, the total circuit can be equally considered as a uniform transmission line. The loading of capacitance means the increases of effective permittivity, in other words, the effective permittivity can be tuned by the reverse bias voltage. The equivalent model of varactor MAVR011020 from MACOM Technology Solutions has been used in the ADS simulation, six units circuit with detailed parasitic parameters of pads has been designed. The total circuit length is 8.25 mm, and the width of the transmission line is 0.5 mm. The permittivity of the substrate is chosen as 15, which is the same as YIG.

The effective parameters extractions are based on (5.42) and (5.43) with the simulated S-parameters from ADS. The reverse bias is tuned from 0 to 15 V, the corresponding loading capacitance is from 0.275 pf to 0.05 pf. The extracted effective permittivity at three frequencies is

shown in Fig. 5.14, as can be seen that the effective permittivity decreases when the reverse bias increases due to the reduction of loading capacitance. The missed points at 9 GHz at low bias conditions are due to the influence of Bragg cutoff frequency, a smaller distance between two units will result in higher Bragg cutoff frequency, which in turn improve the performance at 9 GHz. It also can be seen in Fig. 5.14, the difference between different frequencies become larger when the loading capacitance increases, in other words, the dispersion becomes strong.
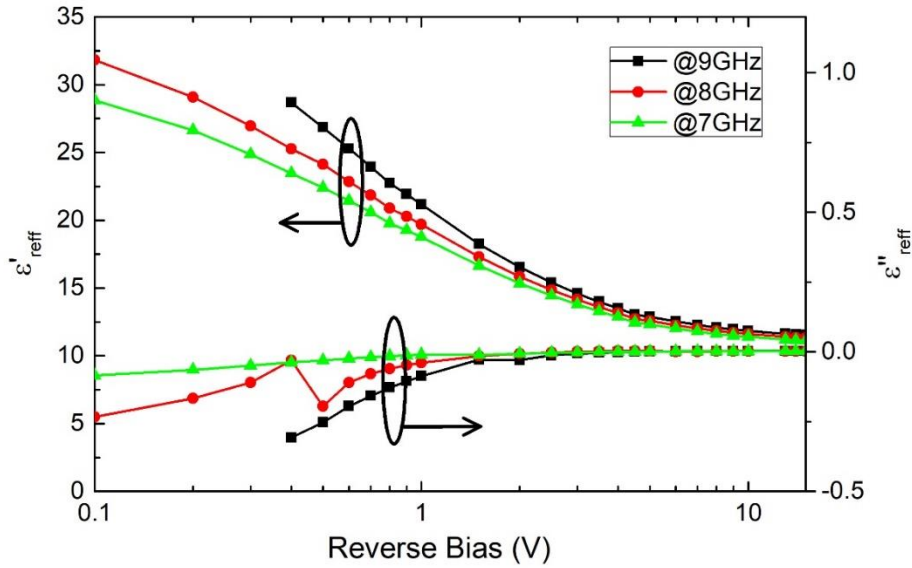
Figure 5.14: Extracted effective permittivity at three frequencies for NLTL with varactor.

5.3.2.3 YIG-based microstrip line

In this section, microstrip line with the thickness of 0.5 mm on YIG substrate with the thickness of 0.762 mm is simulated in HFSS. And the effective permeability is extracted based on the simulated S-parameters. From (5.42) and (5.43) we can see that the extraction does not include the information on gyromagnetic resonance. In addition, Fig. 5.5 and Fig. 5.6 indicate that YIG is very dispersive. If YIG is used in a tunable circuit, frequencies higher than gyromagnetic resonance should be chosen because the low frequencies will be influenced by the corresponding gyromagnetic resonance during the tuning of the magnetic field. In addition, the YIG should operate at saturation region in order to reduce the loss [23]. The applied magnetic bias is perpendicular to the YIG substrate, and the bias setting in HFSS is internal bias instead of external bias, as expressed in (5.23).

The extracted effective permeability at three frequencies is shown in Fig. 5.15. Compared with Fig. 5.6, they have the same trend, although Fig. 5.6 presents the calculated permeability of YIG, and Fig. 5.15 presents the effective permeability of the YIG-based circuit. Due to the influence of gyromagnetic resonance, the magnetic bias larger than 800 Oe will destroy the performance at 7 GHz, while the magnetic bias larger than 1300 Oe will destroy the performance at 8 GHz.
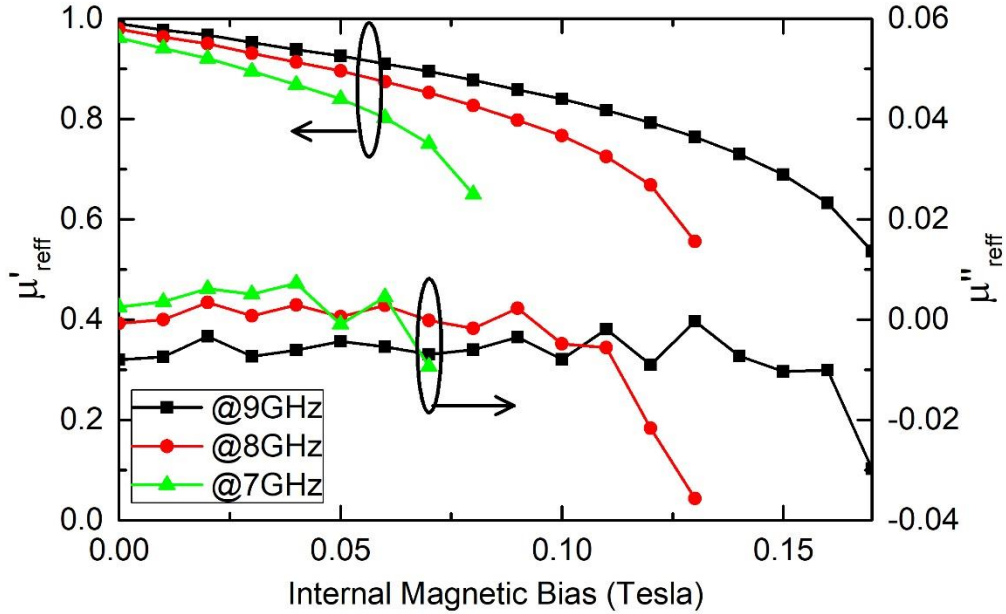
Figure 5.15: Extracted effective permittivity at three frequencies for YIG-based circuit.

5.4   Small signal application of two-dimensional tuning circuits

One of the small signal applications of two-dimensional tuning circuits is phase shifter. Hybrid NLTL technique can be utilized, and the NLTL with commercial varactors will be fabricated on the YIG substrate. The tuning of capacitance will not affect the permeability characteristic of the structure, and the tuning of magnetic bias will not affect the permittivity characteristic of the structure. In other words, the tuning of permittivity and permeability are independent. The extracted parameters in Section 5.3 could be used to design a two-dimensional tuning circuit if the same structure is used. Compared to pure electric tuning or magnetic tuning circuit, the two-dimensional tuning circuit has more freedom to manipulate the electrical and magnetic fields so as to keep impedance constant while changing the phase velocity rapidly.
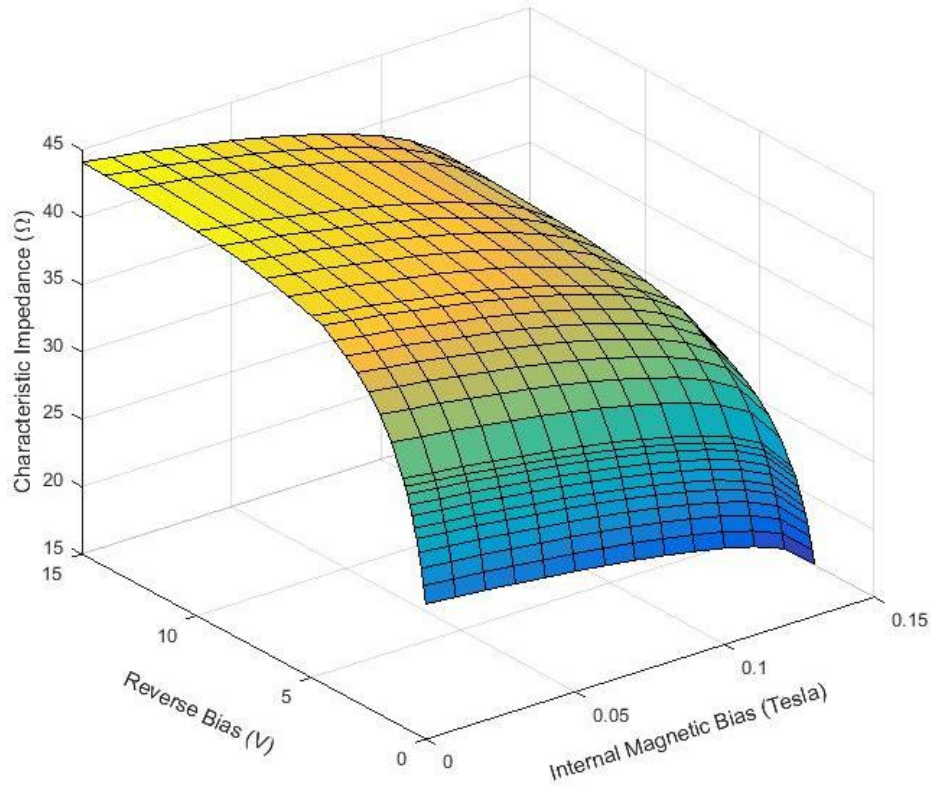
Figure 5.16: Calculated characteristic impedance of hybrid NLTL when tuning the internal magnetic bias and reverse voltage bias.

It can be seen from Fig. 5.14 and Fig. 5.15 that the operation frequency will be limited by the gyromagnetic resonance frequency of YIG and the Bragg cutoff frequency of NLTL. Based on the extraction of Fig. 14 and Fig. 15, the characteristic impedance of YIG-based NLTL at 8 GHz can be calculated by (5.39), and the result is shown in Fig. 5.16, as can be seen that the impedance increases when the magnetic bias H_i decreases and the reverse bias voltage V_r increases. It is easy to find a combination of H_i and V_r that can result in the constant impedance.

The phase velocity can be calculated as

$$v_p = \frac{c}{\sqrt{\mu_{reff} \varepsilon_{reff}}} \tag{5.47}$$

where c is the speed of light. The result is shown in Fig. 5.17, as can be seen that the phase velocity increases when H_i increases and V_r increases. It can be seen from (5.47), the delay variation of the hybrid NLTL is larger than the capacitive or inductive NLTL, at the same time, the impedance can

be kept constant. For a certain value of delay of the phase shifter, a less number of unit will be required for the hybrid NLTL. Actually, it is also easy to find a combination of H_i and V_r that results in a constant phase velocity while the impedance changes rapidly.
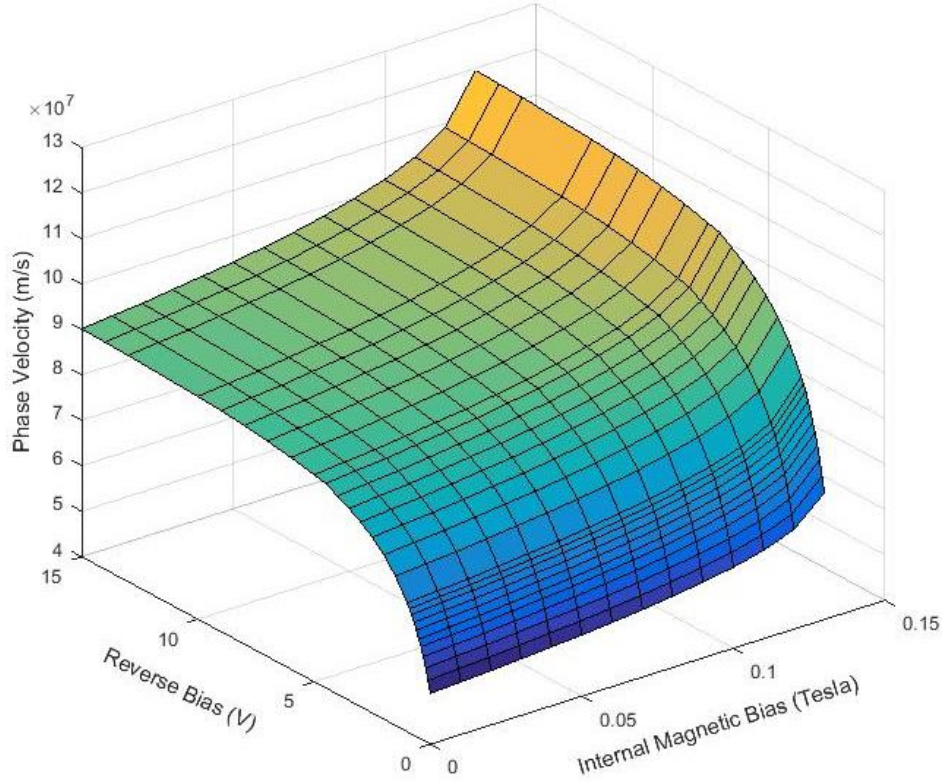
Figure 5.17: Calculated phase velocity of hybrid NLTL when tuning the internal magnetic bias and reverse voltage bias.

5.5   Large signal application of two-dimensional tuning circuits

It can be seen from (5.26) and (5.47) that the hybrid NLTL could have higher compression rate [72] than the traditional capacitive or inductive NLTL while keeping the input impedance constant. For a small signal application, the circuit operates in a linear condition, and the parameters of the circuit are tuned by the external biases. By contrast, for a large signal application, e.g. pulse sharpener, the hybrid NLTL needs to be driven by the signal itself or large dc bias.

The capacitive component in a hybrid NLTL can be varactor, BST or PZT, and the inductive component is usually ferrite. The varactor [37-40] in NLTL can be driven by the signal with amplitude from a few volts to tens of volts, BST [41-43] can be driven by the signal with amplitude

from hundreds of volts to a few kilo volts, PZT [20, 21] can be driven by a few kilo volts. The ferrite is usually driven to its saturation region by a high voltage pulse of 10 - 100 kV [45-50]. It can be seen that proper ceramic dielectric material and ferrite can be chosen for the design of a hybrid NLTL, a possible topology can be multilayers or alternate material blocks, in which the materials can be driven by the same pulse signal. However, the application of an extremely large pulse signal is out of the scope of this work.

One of the goals of this work is to explore the possibility of developing ahybrid NLTL using varactor and ferrite, which means the maximum amplitude of the signal is tens of volts. The work in [72] provides a possible way to drive the abrupt-junction varactors and ferrite-based inductors with a small-signal plus bias, or a large-signal plus bias. However, the large loss in the inductor at high frequencies limits the cutoff frequency in the range of MHz. So far, there is no experimental work of hybrid NLTL has been done at microwave frequency, mainly because of a required large magnetic bias for ferrite at microwave frequency range. The relationship between current bias and external magnetic bias could be investigated firstly, then more work could be done from the following aspects: 1) If the required magnetic bias is high, the YIG substrate can be pre-biased close to the saturation region, and then use the amplitude of the signal to tune the permeability. 2) If the small ferrite core is used, the inductor can be fabricated with a small size, it can not only work at microwave frequency, but also require a similar bias level as varactors. 3) Use the microwave ferrite material at low frequency region since higher frequency needs higher magnetic bias (Fig. 5.15), the required magnetic bias may reduce to the similar bias level as varactors.

5.6   Conclusion

In this chapter, we analyze the ferrite-based hybrid NLTL in both time domain and frequency domain. Then, parameter extraction of complex permittivity and permeability have been developed and validated. The two-dimensional tuning theory can provide more freedom to manipulate the electrical and magnetic fields of the circuit in order to have a constant impedance or constant phase velocity. Finally, the small-signal and large-signal applications of two-dimensional tuning circuits have been studied theoretically.

CHAPTER 6   CONCLUSION AND FUTURE WORK

Conclusions

This PhD thesis explores the traditional and emerging nonlinear devices and nonlinear transmission line (NLTL) techniques and their microwave applications. So far, the research work has resulted in 5 journal publications and 1 patent. The principal scientific contributions of this research work can be summarized as follows:

- An equivalent circuit model is developed for spindiode up to 20 GHz.

- Investigation of the use of spindiode is conducted for low-power wireless power harvesting application. Detailed analysis and modeling are carried out to suggest the advantageous features of spindiodes as the next generation of active devices for RF and microwave rectifications and other nonlinear applications.

- A negative resistance device is demonstrated for using in the development of an electronic impedance tuner, which can generate a reflection coefficient beyond one.

- A semi-closed form design procedure is developed for the distributed electronic impedance synthesizer (EIS).

- A non-uniformly distributed EIS is proposed and it has a smaller size and better Smith chart coverage than the uniform topology.

- A Particle Swarm Optimization (PSO) method is introduced to solve the multi-parameter optimization problem of the proposed non-uniform EIS. The successful utilization of PSO can shorten the development period of an EIS to a few hours.

- A voltage distributed theory is developed for the distributed EIS, and it can predict the power-handling capacity and nonlinearity from its linear operation region. In addition, the voltage distribution analysis can largely reduce the computation complexity of EIS, especially involving thousands of discrete impedance states.

- Comprehensive figures of merit (FOM) of EIS and tunable matching network (TMN) are studied and summarized, different FOM can be chosen to evaluate the EIS according to their applications.

- Hybrid NLTL is analyzed in both time domain and frequency domain.

- Parameters extraction method of complex permittivity and permeability is developed.

- Small-signal application of two-dimensional tuning circuits is studied theoretically.

- Future work of the large-signal application of two-dimensional tuning circuits is discussed.

Future Work

The research presented in this thesis could be continued from the following aspects.

For the application of wireless power harvesting with spindiode:

- In this work, we only focus on the non-resonant rectification of Spindiode. Actually, there are two more rectification mechanisms present in Spindiode: resonant rectification and Seebeck effect [123]. These two mechanisms could be studied more from the physics point of view. And then the rectification with the combination of two or three mechanisms could be studied theoretically and validated with the experiments. Although the current spindiode with non-resonant rectification is much lower than Schottky diode, it has potential to compete with Schottky diode if two or more mechanisms could be implemented simultaneously.

- The spindiodes we used in this work were designed for MRAM instead of real diodes, more physical studies could be done to find out the crucial physical parameters that could result in a better current responsivity. Then physical construction could be optimized to improve the characteristics of the spindiode.

For the application of electronic impedance tuner:

- In this work, we focus on the design and optimization of the electronic impedance tuner, more studied could be done from the application side, such as Load-Pull system and noise measurement.

- More importantly, the design of electronic impedance tuner could be modified to tunable matching network, so that it can be used in the reconfigurable devices, such as PA and antenna.

For the application of hybrid NLTL:

- The parameter extraction method for NLTL-based circuit need to be further improved. Although the time domain smoothing technique can solve the jumping problem in the extracted parameters, it filters most of the components in a large frequency region. More investigation need to be done for the influence of the missing components.

- The theory hybrid NLTL needs to be further validated through the experiments. The NLTL on ferrite substrate should be fabricated and measured.

- Since the phase velocity of hybrid NLTL varies faster than the traditional NLTL while keeping the impedance constant, low-power high-speed Analog-Digital Converter (ADC) with high dynamic range may be possibly realized by the hybrid NLTL techniques.

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APPENDIX - LIST OF PUBLICATIONS

1. Peer-reviewed journal publications

Published papers:

[J1] **Y. Zhao**, S. Hemour, T. Liu, and K. Wu, "Non-uniformly Distributed Electronic Impedance Synthesizer." *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 11, pp. 4883-4897, Nov. 2018.

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