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Perception SoC Based on an Ultrasonic Array of Sensors: Efficient DSP Core Implementation and Subsequent Experimental Results

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We are concerned with the design, implementation, and validation of a perception SoC based on an ultrasonic array of sensors. The proposed SoC is dedicated to ultrasonic echography applications. A rapid prototyping platform is used to implement and validate the new architecture of the digital signal processing (DSP) core. The proposed DSP core efficiently integrates all of the necessary ultrasonic B-mode processing modules. It includes digital beamforming, quadrature demodulation of RF signals, digital filtering, and envelope detection of the received signals. This system handles 128 scan lines and 6400 samples per scan line with a 90° angle of view span. The design uses a minimum size lookup memory to store the initial scan information. Rapid prototyping using an ARM/FPGA combination is used to validate the operation of the described system. This system offers significant advantages of portability and a rapid time to market.

Keywords and phrases: perception SoC, ultrasonic, focusing, beamforming, DSP, FPGA circuit techniques.

1. INTRODUCTION

Ultrasound imaging is an efficient, noninvasive, method for medical diagnosis. Employed ultrasound waves allow to obtain information about the structure and nature of tissues and organs of the body [1]. They are generated by converting a radio frequency (RF) electrical signal into mechanical vibration via a piezoelectric transducer sensor. The frequencies of these ultrasound acoustic waves are located above the 20 kHz sensitivity limit of the human ear. Among the applications of ultrasound imaging, it is extensively used in obstetrics to estimate the size and weight of a baby by measuring the head diameter, the abdominal circumference, and the femur length of the fetus. It is also used to visualize the heart, and measure the blood flows in arteries and veins [2].

The ultrasonic diagnostic imaging systems are mostly operated in the pulse-echo mode. The transducer is used both for transmitting an ultrasonic pulse into the objects and receiving the return echoes from those objects. The pulse-echo systems can be classified as A, B, or M modes. The first display mode, called A-mode (A for amplitude), is 1D display ultrasonic imaging. It displays the amplitude according to the depth of the received echoes. The second one, B-mode (B for brightness), is 2D display ultrasonic imaging which consists of pixels. The brightness of each pixel is determined by the amplitude of the received echo.

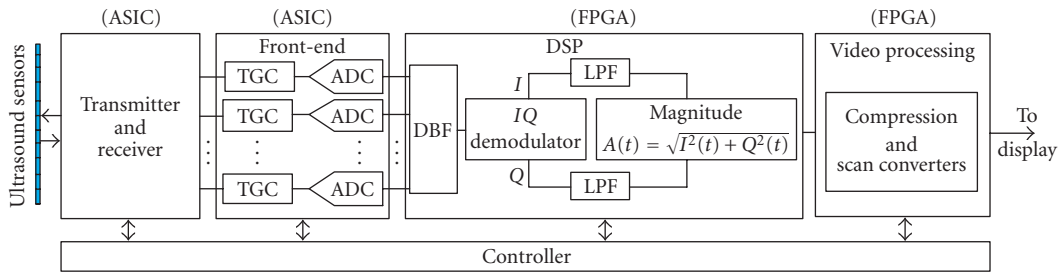


Figure 1: Perception SoC of the B-mode processing of the ultrasonic imaging system.

Finally, M-mode (M for motion) is 2D display ultrasonic imaging; it displays the depth in tissue according to time of the received echoes. The amplitude of the echoes is measured at a given number, of depths.

In this paper only the B-mode is considered due to the popularity in the echography industry of the brightness of imaging display.

The majority of commercially available ultrasonic systems occupy large spaces in clinic rooms; their power consumption may exceed hundreds of watts and they are mainly used near the bedsides of patients. Most units are built with discrete components mounted on several printed circuit boards [3], with software drivers used to control them [4]. More recently, several research efforts are being made to minimize the size of such systems by combining multiple processors with dedicated components, but the dimensions of improved devices still miss the required hand-held format [5, 6, 7, 8, 9, 10, 11]. The current efforts are motivated by advances in microelectronics that make it possible to design and implement an SoC that allows to build hand-held devices. Our work dedicated to build an echography device follows this approach. It aims to develop a compact DSP core as the main computing engine of an ultrasound imaging system and first prototype it on a programmable logic device (FPGA) subsequent to an SoC device. This miniaturization enables a design with low power consumption, low noise, and light weight [12].

In this paper, we describe in Section 2 the general description of the ultrasonic perception SoC. The DSP core architectural features, and its various stages, sensing front-end and its digital beamforming (DBF) module, quadrature demodulation, LPF, and envelope detection are subjects of Section 3. Section 4 contains the implementation process of the DSP core in an FPGA and its experimental results. Finally, conclusion is given in Section 5.

2. GENERAL DESCRIPTION OF THE ULTRASONIC PERCEPTION

Perception SoC can integrate functionally different computational elements traditionally built around several mixed-signal ASICs and FPGAs [13]. Figure 1 shows the ultrasonic perception SoC of the B-mode processing of the imaging system. The emitter generates high-voltage pulses to excite a transducer that is composed of multielement sensors. The latter are used to generate and detect pulsed ultrasonic echoes. The received echoes are preamplified, digitalized, and passed on to a digital signal processor (DSP) block by the receiver front-end [12]. This DSP core performs beamforming, quadrature demodulation, filtering, and envelope detection of the received echoes. The scan converter resamples the amplitude of the obtained video signal in order to convert it to pixel brightness on a rectangular display screen [14]. A controller synchronizes the sweeping of the image area, and the transmission, reception, digitization, and displaying of the acquired data.

B-mode processing involves signal acquisition, echo signal processing, and display. In the signal acquisition stage (also called the front-end), the acoustic echoes received from the tissues are converted to electrical signals by the transducer. These signals are amplified with a variable gain (TGC, time-gain-compensation) that depends on the scan depth and, then, they are digitalized by the analog-to-digital converter (ADC) circuit.

3. ARCHITECTURE OF THE DSP CORE

The DSP core performs the DBF to achieve the dynamic focusing and steering of the received echoes. This DSP core includes also a digital IQ demodulator to remove the high-frequency carrier and reduce noise by quadrature demodulation. It results in in-phase (I) and quadrature (Q) samples of a complex signal $I(t) + jQ(t)$. After lowpass filtering, the envelope (magnitude) of the received echo at time t is computed [9]:

$$A(t) = \sqrt{I^2(t) + Q^2(t)}. \quad (1)$$

Usually, the obtained signal has a large dynamic range, 70 dB or higher, while a typical display monitor has a dynamic range of only 35–40 dB, compatible with human vision. As a result, the dynamic range of the received echoes may be compressed before feeding them to the scan conversion stage. The required compression can be achieved by implementing a logarithm function [11]. Finally, the compressed signal is scan-converted from beam-space to a standard Cartesian grid [5, 15, 16] and stored in a 2D image memory, which serves for display. The controller is also responsible for interacting with the user, so that operating parameters such as imaging depth, gain, mode, and thresholds may be set in real-time according to the operator's desires.

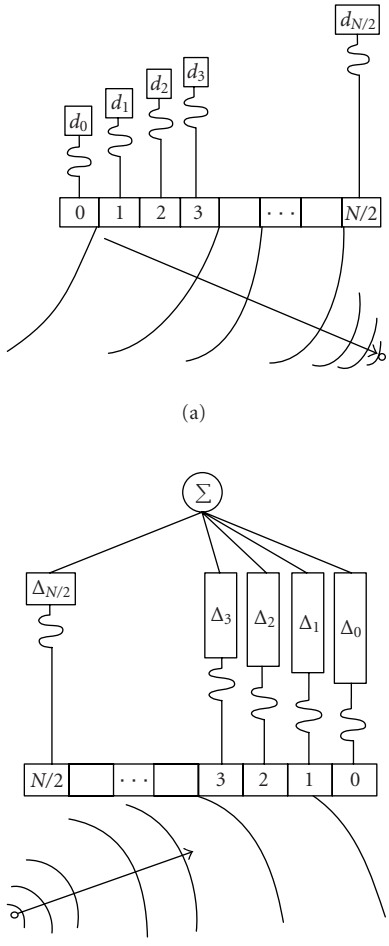


Figure 2: Beamforming: (a) resulting focal point, and (b) delay generation.

3.1. Digital beamforming

For ultrasound medical imaging, ultrasonic pulses are sent into a patient's organ and the resulting reflections (echoes) from tissues are detected by an array of sensors. One important step is the electronic dynamic focusing and steering of the echoes by means of a phased transducer array to meet the quality of the real-time processes [17]. The geometrical approach is used to realize focusing and steering by inserting a variable time delay after each transducer element in the array to compensate echoes for different arrival times. Using such an array of sensors transducer, the beam is focused and steered by exciting each one of the array sensors at specific time. As a result, the resulting sound waves coming from all sensors arrive simultaneously at a given focal point, during the transmission. Figure 2a shows an example of this principle. During reception, a beam focusing must also be accomplished; the signals coming into the ultrasound scanner from the various sensors must be delayed to arrive at the same time, as shown in Figure 2b.

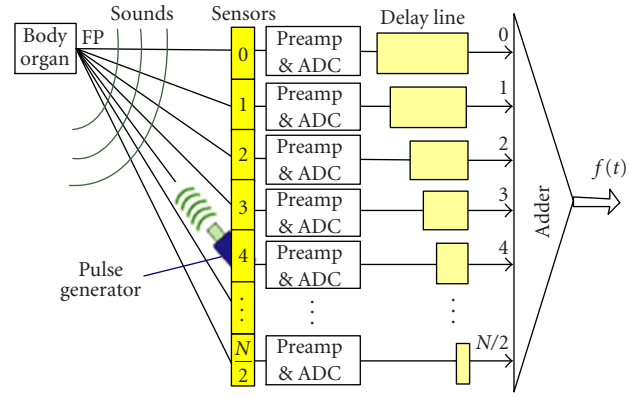


Figure 3: Simplified schematic of the pipelined digital beamforming.

The focusing process can be accomplished by using analog discrete components, but such an approach does not allow to deliver the precise delays, and it generally results in a complex and bulky circuitry [18]. To improve the quality of the acquired images, analog circuit implementations as well as software calculations must be avoided. Instead, DBF technique is used. Its implementation can be based on sampled-delay focusing (SDF), which consists of combining memories (FIFO) to delay and store the sampled signals, and lookup tables (LUT) that contain precalculated scan lines [17, 19]. In order to improve the system design, pipelined SDF technique can be adopted to implement the variable delay without using FIFO memories and with a minimum of LUTs.

3.1.1. Delay variation

Figure 3 illustrates echoes coming from a specific point (focal point-FP) that are preamplified, digitized, adequately delayed, and then added to produce a focused signal. The focused signal $f(t)$ can be expressed as [19]

$$f(t) = \sum_{n=-N/2}^{N/2} X_n(t - \tau_n), \tag{2}$$

where X_n is the received echo from the nth sensor element, $N + 1$ is the total number of sensors, and τ_n is the focusing and steering delay required for the nth element at depth R and is driven by

$$\tau_n = \frac{R}{c}\left[\sqrt{1 + \left(\frac{nd}{R}\right)^2 + 2\left(\frac{nd}{R}\right)\sin\theta} - 1\right], \tag{3}$$

where $c = 1540\,\text{m/s}$ is the average propagation speed of sound in the medium, d is the sensor spacing, and θ is the steering angle (Figure 4) [19].

After exciting the sensor array, a signal is transmitted with the steering angle θ and, then, echo signals are propagated back from the focal point to the sensors. The distance from the focal point to the sensor located in the center of the array is R and it is different from the distance to a sensor

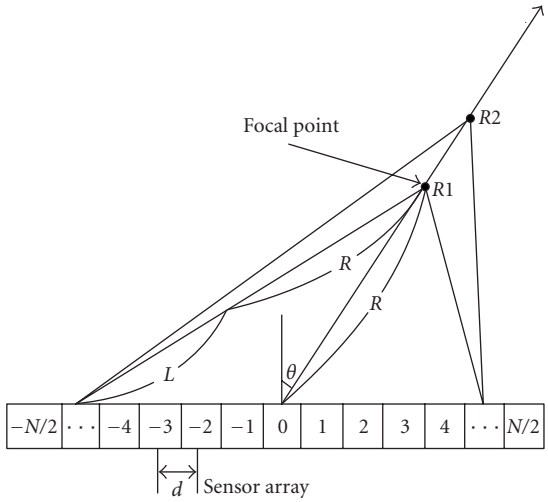


Figure 4: Dynamic focusing and steering delay.

element located at another position $(R + L)$, where L is the propagation distance (Figure 4).

The delay information for a complete scan line can be precalculated and stored in a lookup table, using a first-in-first-out (FIFO) memory with a sampling clock generator (SCG) [19]. In a typical ultrasound image, a sector is formed of 128 beams (scan lines) and corresponds to a propagation depth of about 20 cm. The total memory requirement for such case to store the precalculated delays is about 1 Mbytes per channel (sensor), assuming that the sampling time resolution used for focusing the phased array is 10 times if the selected transducer center frequency is 5 MHz. This would require a large memory [20, 21, 22, 23]. To resolve this problem, a pipelined sampled-delay focusing architecture is used.

The variable delay circuit architecture is shown in Figure 5. It includes a controller, a simplified lookup table that stores $\sin(\theta)$ values, where θ is the rotation angle with values between -45° and 45°, with a step of 0.7°, the next focal point (FP) pointer calculation block and the delay calculation block (DCB) are activated by the controller. At the same time, the initial FP value (R) is delivered to the DCB. The delay (τ_n) defined in (3) is computed for the line delay of each array element and for specific angle and FP. The next FP is determined in parallel when computing τ_n and delivered to the DCB, and this operation is repeated M sampled times to produce a complete scan line, where M is the sampled pixel per scan line. For each angle, a scan line is formed to produce a scanned image frame. To reduce the delay quantization error, and to obtain precise sampling values, fast digital circuitry is required, and the ADC must have a fast conversion rate. In our design, the clock frequency is 50 MHz which corresponds to 10 times if the transducer selected center frequency (f_0) is 5 MHz [24].

As an example, assume the following conditions: array aperture (Nd) of 20 mm, scanning angle (θ) varying between $+45^\circ$ and -45°, scanning done to a depth (R) of 20 cm, and transducer center frequency (f_0) of 5 MHz. The

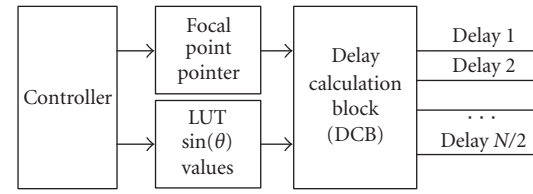


Figure 5: Proposed delay calculation architecture.

maximum time to sample one scan line is $t_{\mathrm{MAX}}(2R/c =$ 260 microseconds), which corresponds to 6400 samples at 50 MHz. For the whole 128 scan lines (SL), the total scan time needed is 128×260 microseconds (0.033 second), corresponding to one frame of the scanned image. The memory required to store this image is $128\times6400\times8$ bits/sample = 800 Kbytes.

To minimize the operations of the delay calculation, (3) can be modified as follows:

$$\begin{aligned}\tau_n &= \frac{1}{c}\left[\sqrt{R^2 + (nd)^2 + 2ndR\sin\theta} - R\right] \\ &= \frac{1}{c}\left[\sqrt{(R + nd)^2 - ndR(2 - 2\sin\theta)} - R\right].\end{aligned} \tag{4}$$

As shown in (4), the division-by-R and one multiplication operation were eliminated, thus reducing the complexity of the required hardware.

3.1.2. Pipelined sampled-delay focusing implementation

The most important factors in implementing the pipelined SDF are the number of registers and the registers control. For each channel i of the transducer, there is a variable number of registers Reg_i [25]:

$$\mathrm{Reg}_i = f_s\left(\frac{L_n - L_i}{c}\right), \tag{5}$$

where L_n is the maximum distance delay, n is the nth array channel and L_i is the distance delay of ith channel, and f_s is the sampling frequency. The maximum number of registers is determined by the sampling frequency f_s and the maximum distance delay of the array channel:

$$\mathrm{Reg}_{\mathrm{MAX}} = f_s\left(\frac{L_n}{c}\right). \tag{6}$$

Note that the number of registers required for each channel of the transducer array varies from zero to the maximum value $\mathrm{Reg}_{\mathrm{MAX}}$. To implement such pipelined SDF, we use a counter, variable registers, and an adder, assuming that the data is coming from an array of ADCs, as shown in Figure 6. For each channel, the data acquisition is valid at the transducer when the time distance $2(R + L_i)$ is attained, where $i = 0, \ldots, n$, $L_0 = 0$ is the free delay, and L_i is the time distance of channel i (this distance is the 2-way sound trip from the transducer to the FP). This data is controlled by a main counter and a comparator at each channel. The sequences of

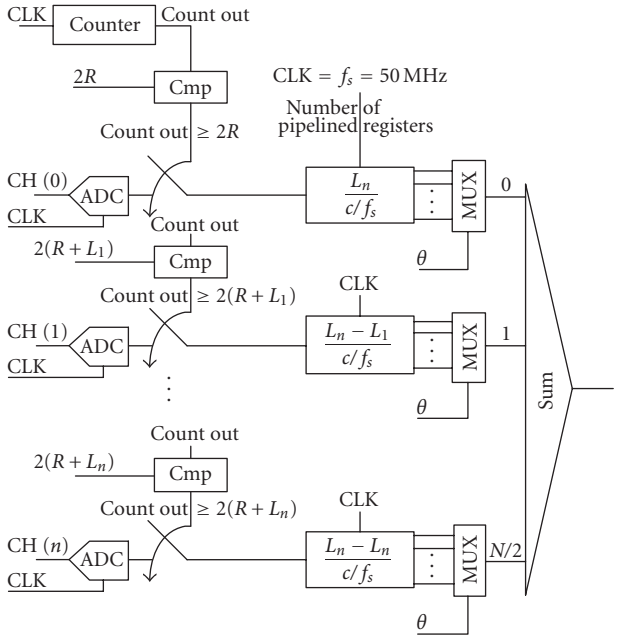


Figure 6: Block diagram of the pipelined sampled-delay.

sampled data are inserted into the variable registers at each clock cycle. As a result of the variable registers, the echo signals that were sampled at different times to compensate for different propagation path delays will be aligned at the output of each variable register and they will be summed to obtain the focused signal. For each angle, the counter and all the variable registers are reset, and the outputs of these registers are selected according to the specific pipelined registers (Reg_i) [25]. The time distance for each channel can be computed by (7) adapted from (4):

$$\begin{aligned} L_n + R &= \sqrt{R^2 + (nd)^2 + 2ndR\sin\theta} \\ &= \sqrt{(R+nd)^2 - ndR(2 - 2\sin\theta)}. \end{aligned} \tag{7}$$

For each angle, a scan line is formed to produce a scanned image frame. The distance times ($L_i + R$) are calculated in series from L_1 to L_n for each element. As an example, assume the same conditions as defined in the previous section with a distance spacing between channels of 0.154 mm ($d = \lambda/2$) for 129 channels (sensors) and starting scan line from 10 mm ($R = a/2$). The delay time distance before starting the first sample of the scan line is $2(R + L_i)$ where $L_0 = 0$, $L_1 = 131\,\mu\text{m}, \ldots, L_{64} = 8450\,\mu\text{m}$, and the number of pipelined registers is zero registers for channel 64, 4 registers for channel 63, and the number is 274 registers for channel 0 according to (5). By scheduling few operations, (7) can be realized as shown in Figure 7, which gives an optimized pipelined architecture.

3.2. Quadrature demodulation and envelope detection

The received echo is envelope-detected signal after focusing by the DBF. To reconstruct the envelope of the received

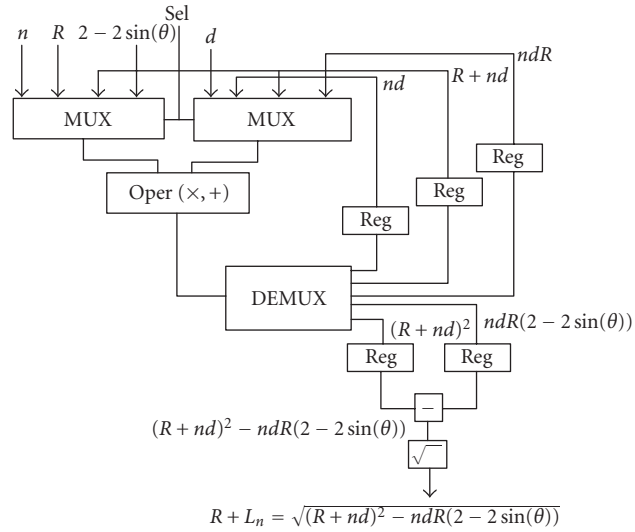


Figure 7: Block diagram of the delay time distance calculation.

signal, the sampling rate must be greater than twice the maximum signal frequency, according to the Nyquist criterion. However, since the bandwidth of the envelope is less than that of the received signal, it is possible to reduce the sampling rate accordingly. This can be achieved by using the quadrature sampling method, which splits a band-pass signal into in-phase and quadrature baseband components, and each of them is sampled separately [17]. Such bandpass signal can be expressed by

$$\begin{aligned} f(t) &= A(t)\cos\left[w_0 t + \varphi(t)\right] \\ &= A_I(t)\cos\left(w_0 t\right) + A_Q(t)\sin\left(w_0 t\right), \end{aligned} \tag{8}$$

where

$$\begin{aligned} A(t) &= \sqrt{A_I^2(t) + A_Q^2(t)}, \\ \varphi(t) &= \tan^{-1}\left(\frac{A_Q(t)}{A_I(t)}\right). \end{aligned} \tag{9}$$

In (8), ω_0 and $\varphi(t)$ are the center frequency of the transducer and its phase, and $A_I(t)$ and $A_Q(t)$ are the envelopes of the in-phase and quadrature-phase components. They are obtained by mixing the bandpass beamformed signal with sine and cosine references, and subsequently are lowpass filtered (Figure 8). Since $A_I(t)$ and $A_Q(t)$ are baseband signals, they may be sampled at their bandwidth rate [26]. The envelope detection is achieved by evaluating $A(t)$ where t is replaced by KT_s, where

$$T_s \leq \frac{1}{\text{bandwidth}}. \tag{10}$$

The implementation of the IQ demodulation is accomplished by using two lookup tables for the sine and cosine, with a finite impulse response (FIR) digital lowpass filter (LPF). Finally, the Cordic method can be used to detect the envelope of the echoes [27, 28].

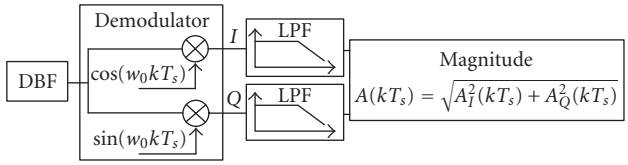


Figure 8: Quadrature sampling technique for bandpass signals.

3.3. Digital filter

Equation (11), represents the FIR filter transfer function in the time domain [29, 30]:

$$y(n) = \sum_{i=0}^{N-1} a_i x(n-i-1). \tag{11}$$

In this equation, N data memories are required to hold the intermediate results and, for each output of index n, N multiplications and $N-1$ additions have to be performed [30]. By designing a linear phase filter, the symmetry of the coefficients allows to reduce by half the number of multiplications. Figure 9 shows a realization of the filter and the corresponding structure when the number of coefficients is odd. To minimize the memory size required to implement the filter, we used the minimum possible number of bits such that the characteristics of the filter are not affected for both the input data (16 bits) and/or the coefficients (12 bits).

For the needed LPF for our application that requires a sampling frequency of 50 MHz, and a cut-off frequency of 5 MHz, the transition bandwidth is 4 MHz and the stop band attenuation is greater than 35 dB. To design such a filter, Matlab was used to simulate the required 23rd order.

4. IMPLEMENTATION OF THE DSP CORE

In order to validate the proposed architecture of the DSP core, a front-end of eight sensors was simulated and implemented. There were three main steps achieved: (1) Simulink model study using Matlab, (2) VHDL code generation using Synospys, and (3) hardware implementation using the ARM Integrator/LM logic module rapid prototyping platform (ARM-RPP). The Matlab simulation was performed in a DSP core composed of 9 modules. They are the image input matrix, the input delay, the beamforming block, the IQ demodulation, the lowpass filter, the envelope detector, the logarithmic compressor, the decimator, and the image output matrix.

The ARM-RPP platform contains an ARM7TDMI processor and a Xilinx Virtex II FPGA which provides logic and core modules. The logic module contains the FPGA, SSRAM, connectors, and several interface circuits. The core module contains an ARM processor and some configurations, and interface circuits. The communication between these modules is possible via a 32-bit bidirectional bus (AMBA). Due to this limitation, a modified block diagram of the ARM platform is done to produce 64-bit data as input in the DSP block,

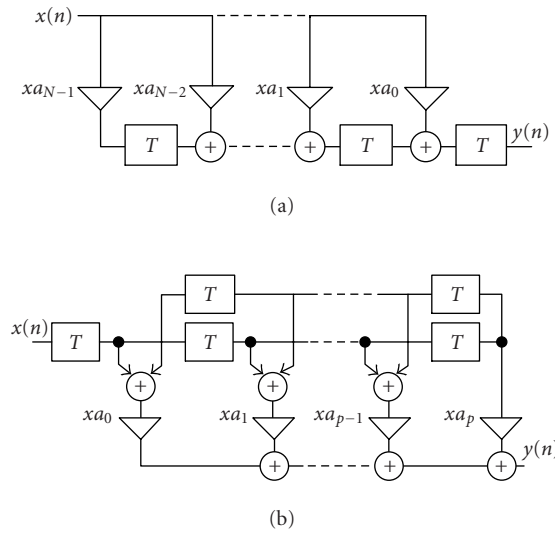


Figure 9: Realization of FIR filter: (a) simple direct structure and (b) direct structure for a linear phase filter.

as shown in Figure 10. These data are the sampled signals from all eight channels of the ADC array, where each sample is 8 bits wide. The ARM processor writes and reads the sampled data via the AMBA bus at a 100 MHz clock frequency (HCLK). Because of the 50 MHz sampling period of the DSP core, each read/write cycle from the ARM processor must be divided by two to meet the DSP sampling period (50 MHz). The DSP module, programmed in the FPGA, reads the data from the AMBA bus, computes the digital beamforming, eliminates the high frequency and maintains the phase-angle by IQ demodulating and digital lowpass filtering, and finally, produces the magnitude received signal.

The DSP core requires a 50 MHz clock (CLK) that is derived from the main HCLK clock. HCLK is generated using one of the ICS525 programmable oscillators integrated on board of the logic module. Table 1 summarizes the DSP core parameters, and the operation of the system is as follows:

(i) the ARM processor sends data (32 bits) across the AMBA bus at the effective rate of HCLK;
(ii) a frequency divider generates CLK from the HCLK;
(iii) each 2 HCLK clock cycles, a data of 64 bits is inputted to the DSP core module;
(iv) each 64-bit data is separated into eight 8-bit words data, which represent the output sampled data from the eight ADC channels;
(v) the data is processed at a clock rate of 50 MHz in the DSP core module;
(vi) the ARM processor receives data from AMBA bus, and processes it at 2 HCLK clock cycles.

A hardware reset initializes the whole system. Then, the counter addresses of the sine/cosine LUTs and all FIFO registers are set to zero and R is set to its minimum value (10 mm).

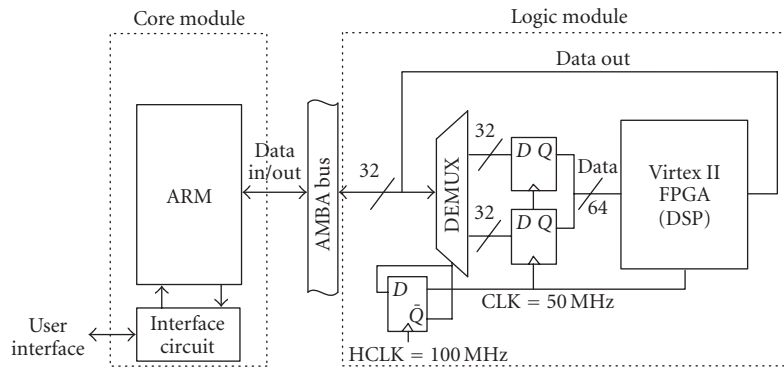


Figure 10: Block diagram of the ARM platform used for DSP core implementation.

Table 1: DSP core parameters.

Parameter name	Notation	Value	Unit
Center frequency	f_0	5	MHz
ADC sampling frequency	f_s	50	MHz
DSP clock frequency	f_{CLK}	50	MHz
Angle of view	θ	90°	Degree
Number of scan lines	SL	128	N/A*
Number of sampled data per scan line	D**	6400	N/A*
Distance between sensors	d	0.154	mm
Maximum distance	R	200	mm
Number of sensors	n	8	N/A*

*N/A = Not applicable.
**According to this table setting.

5. SIMULATION AND EXPERIMENTAL RESULTS

To test the implemented design, a phantom fetus image was generated by the Field-II ultrasound simulation software program [31, 32]. Then, the simulated image data in polar coordinates (R, θ) was inputted to the DSP core. All sampled data were stored in files corresponding to the data of the ADC channels, including the estimated delay of each channel at the transmission. These data were organized as one column of 128×6400 values. The first 6400 values represented the first sampled scan line at −45°, while the last 6400 values represent the last sampled scan line at +45° for each file. The ARM processor retrieves the sampled data values from the previously created files, and sends them to the DSP core prototype via the AMBA bus. The DSP processes the sampled data and produces the magnitude values, which are saved in a new file by the ARM processor.

Prior to building a hardware prototype on the ARM-RPP, a Matlab model using a fetus image was implemented and simulated in order to familiarize us with the DSP core architecture. The model used a depth range of 1–20 cm, and a view angle of 90°.

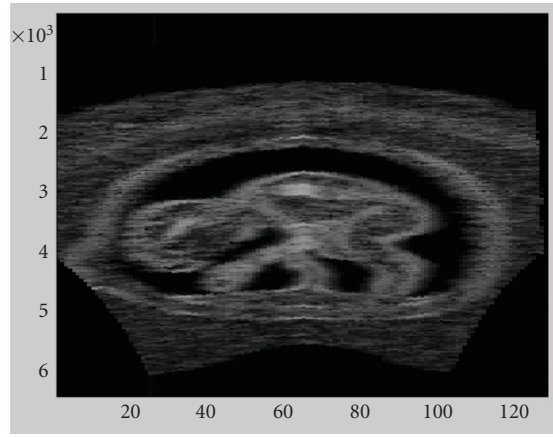
To demonstrate the flexibility of the DSP core, the simulations are done using 2, 4, and 8 ADC channels. Figure 11 illustrates the fetus images created by taking the values from the DSP prototype for 2, 4, and 8 ADC channels, built around the ARM-RPP platform, and after logarithmic compression using Matlab simulation. Also, this figure shows that when the number of ADC channels increases, the image resolution increases too. The number of the ADC channels used in this application is eight due to the ARM bus limitation which is 32 bits, as explained in the previous section.

Functionality of this prototype has been tested on a Xilinx FPGA, satisfying all timing constraints for the required application. The timing requirements for 30 frames at 50 MHz sampling frequency is 0.5 second. Moreover, timing results for FPGA implementation show that higher data rate could be operated correctly for 60 frames/s.

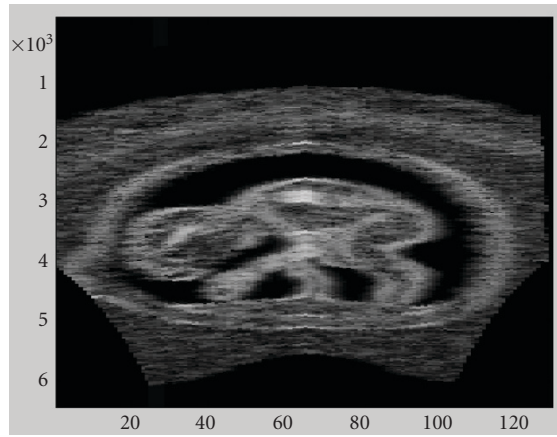
The DSP prototype occupies 61% (314 535 gates) of the XCV2000E FPGA, including the AMBA protocol and interface drivers. Table 2 summarizes the implementation results such as the needed area and the timing constraints. Finally, using this prototype, we could demonstrate that the proposed DSP core architecture works properly and can be efficiently integrated for the purpose of building a perception SoC.

6. CONCLUSION

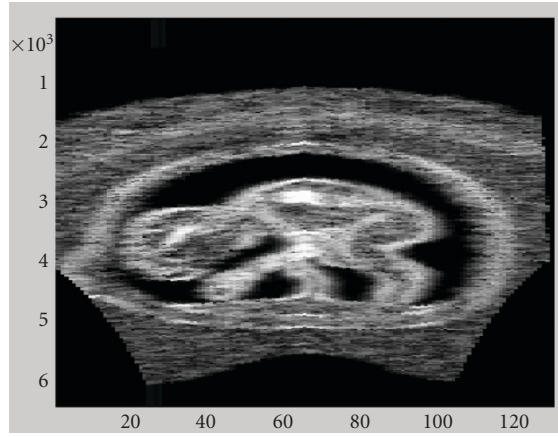
A perception SoC based on an array of sensors dedicated for ultrasound imaging system is reported. It is an



(a)



(b)



(c)

Figure 11: Images produced by ARM data using (a) 2 ADC channels, (b) 4 ADC channels, and (c) 8 ADC channels.

implementation for an efficient DSP core. Also, subsequent experimental results are demonstrated. The DSP core is based on the digital beamforming, digital IQ demodulation, LPF, and envelope detection. The proposed system was implemented in a reduced complexity architecture that only uses an FIFO register and some LUTs to store the cosine and sine angle requirements.

The proposed architecture reduces the complexity and the needed memory and increases the performance of the processed images by taking multirate sampling. The

Table 2: Report from implemented DSP core in the Xilinx Virtex II FPGA.

Using target part "v2000efg680-6."		
Design summary:		
Number of errors:	0	
Number of warnings:	223	
Logic utilization:		
Total number of slice registers:	11 936 out of 38 400	31%
Number used as flip flops:	10 334	
Number used as latches:	1 602	
Number of 4-input LUTs:	18 349 out of 38 400	47%
Logic distribution:		
Number of occupied slices:	14 850 out of 19 200	77%
Number of slices containing only related logic:	14 850 out of 14 850	100%
Number of slices containing unrelated logic:	0 out of 14 850	0%
*See notes below for an explanation of the effects of unrelated logic.		
Total number of 4-input LUTs:	18 584 out of 38 400	48%
Number used as logic:	18 349	
Number used as a route-thru:	235	
Number of bonded IOBs:	330 out of 512	64%
IOB flip flops:	67	
Number of block RAMs:	1 out of 160	1%
Number of GCLKs:	4 out of 4	100%
Number of GCLKIOBs:	1 out of 4	25%
Number of RPM macros:	18	
Total equivalent gate count for design:	298 647	
Additional JTAG gate count for IOBs:	15 888	
Peak memory usage:	357 Mbytes	
Start of timing report		
Timing report written on Monday, January 19th, 17:25:22, 2004		
Top view:	AHBAHBTop	
Requested frequency:	100 MHz	
Wire load mode:	top	
Paths requested:	5	
Constraint file(s):	—	
Worst slack in design:	0.344	

Starting clock	Requested frequency	Estimated frequency	Requested period	Estimated period	Slack
AHBAHBTop|HCLK	100 MHz	103.6 MHz	10	9.656	0.344
System	100 MHz	122.1 MHz	10	8.190	1.810

described DSP core is reconfigurable according to the number of channels. It is dedicated to the front-end receiver part of a real-time medical ultrasound imaging device. The XCV2000E FPGA built in the ARM Integrator/LM RPP is one of the most appropriate available design platforms to rapidly prototype a miniaturized version of an echograph. This platform is needed to validate, in addition to the proposed DSP core, the remaining blocks of the ultrasound system, such as the logarithmic compression, digital scan converter, and the global controller.

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