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1 mm³-sized optical neural stimulator based on CMOS integrated photovoltaic power receiver

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In this work, we present a simple complementary metal-oxide semiconductor (CMOS)-controlled photovoltaic power-transfer platform that is suitable for very small (less than or equal to 1–2 mm) electronic devices such as implantable healthcare devices or distributed nodes for the Internet of Things. We designed a 1.25 mm × 1.25 mm CMOS power receiver chip that contains integrated photovoltaic cells. We characterized the CMOS-integrated power receiver and successfully demonstrated blue light-emitting diode (LED) operation powered by infrared light. Then, we integrated the CMOS chip and a few off-chip components into a 1-mm³ implantable optogenetic stimulator, and demonstrated the operation of the device. © 2018 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>). <https://doi.org/10.1063/1.5024243>

A large number of wireless powering and energy-harvesting technologies have been proposed and demonstrated by different research groups. Some of these techniques, such as RFID or Qi, have been successfully commercialized. However, to our knowledge, there is no *de facto* standard for wireless powering technologies for devices with dimensions less than or equal to 1–2 mm.

The need for battery-less microelectronic devices with very small dimensions has increased with advancements in the design of implantable healthcare devices or in distributed intelligent nodes for Internet of Things (IoT) systems. Some groups have discussed small implantable devices that are powered by electromagnetic wireless power transfer.^{1–5} However, there is an inevitable tradeoff to be considered between the antenna size and available power. When the size of the receiver coil is reduced, both the voltage and current decrease as well. This is a major constraint in electromagnetic power transfer.

In order to develop a wirelessly powered microelectronic platform having dimensions of less than 1 mm, we propose the use of a CMOS-controlled photovoltaic (PV) power-transfer mechanism.^{4,6–10} For biomedical devices, red or infrared (IR) light can be used to power the implanted electronics because this type of light can penetrate human tissue. For IoT devices, we expect to develop intelligent IoT nodes using indoor ambient light. Unlike in electromagnetic energy transfer, the voltage of PV cells does not depend on the size of the device. Only the photocurrent decreases as the area of the PV cell is reduced, and this reduction is proportional. Taking advantage of this inherent characteristic of PV cells, we developed a CMOS-controlled power receiver applicable for biomedical or IoT devices. We demonstrated a battery-less, optical ID transmission device with a diameter of 12 mm that includes off-chip PV cells.¹⁰

In this work, we integrated PV cells onto a CMOS chip.^{11–14} This allowed us to reduce the size of the power receiver platform. With the help of a low-current self-powered CMOS voltage-detection circuit, we succeeded in powering an InGaN blue LED. We aim to apply the LED to optical

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(optogenetic) neural stimulation. Finally, we integrated the CMOS chip and the off-chip components into an implantable optical stimulator, whose volume was as small as 1 mm^3 .

Figure 1 shows (a) the block diagram and (b) the schematic of the proposed CMOS-controlled PV power receiver.¹⁰ As the power receiver, we used series-connected PV cells along with a bias generator. Using this strategy, we were able to mitigate the requirement for a voltage booster circuit.^{7,8,15,16} We were able to simplify the circuit design and the matching between operational conditions of the power receiver and the load circuit. As a drawback of the circuit simplicity, this approach is potentially disadvantageous from the viewpoint of power efficiency because it requires multiple photons to generate an electron at a multiplied voltage. The CMOS circuit simply monitors the voltage of the capacitor, V_{CAP} , which is charged by the power-receiving PV cells, and it turns on and off the CMOS switch to the load circuit (an LED in this study).¹⁷

The circuit shown in Fig. 1(b) is based on the self-powered Schmitt trigger presented in Ref. 18. However, owing to the transition current of the CMOS inverters in the circuit, the circuit is not compatible with the low currents (typically less than $1 \mu\text{A}$) provided by the integrated PV cells. To enable the circuit to adapt to the small PV current, we modified it in order to limit the transition current with n-channel MOS (NMOS) transistors, which are indicated as M_{n4} , M_{n5} , and M_{n7} in Fig. 1(b).

Turn-on and turn-off voltages (V_{on} and V_{off} , respectively) can be determined by choosing the appropriate bias voltages. Four bias inputs (V_{bn1} , V_{bn2} , V_{bp1} , and V_{bp2}) were taken from intermediate nodes of the series-connected PV cells for biasing. Therefore, the bias voltages are denoted by the intermediate node number of the series-connected PV cells at which the voltages are taken, as shown in Fig. 1(b). When the device is illuminated, the bias voltages rapidly reach steady values, and this is different from the case with the powering capacitor, V_{CAP} . Considering the chosen bias conditions, we expected $V_{\text{on}} = 3.5 \text{ V}$ and $V_{\text{off}} = 2.5 \text{ V}$ as typical values. However, V_{on} and V_{off} depend on the illumination because the bias voltages from the second series of PV cells depend on the illumination. The experimentally obtained V_{on} and V_{off} will be resented later in Fig. 5(b).

In this work, we integrated two sets of series PV cells (for powering and biasing) onto a CMOS chip. Figure 2 shows (a) the layout of the CMOS chip and (b) the post processing performed to separate the integrated PV cells. The chip was fabricated using $0.35\text{-}\mu\text{m}$, 2-poly, 4-metal standard CMOS technology. We used an n-well/p-sub diode structure as the integrated PV cell. Ten series PV cells with size $270 \mu\text{m} \times 270 \mu\text{m}$ were integrated for powering, and seven series PV cells of size $120 \mu\text{m} \times 170 \mu\text{m}$ were integrated for biasing, as shown in Fig. 2(a).

Although we designed multiple PV cells on the CMOS chip, as fabricated, they did not work as power receivers or as bias generators. All of the p-layers of the PV cells were shorted at the substrate, thereby requiring us to separate the PV cells, as shown in Fig. 2(b).¹⁹

Figure 3 shows a schematic of the PV cell-separation process. The chip separation was performed using the Bosch etching process (Deep RIE). Prior to the Bosch process, a patterned mask layer was formed by photolithography. A film resist (Photec RY-3315EE, Hitachi-Kasei) was used as the etching mask layer. The Bosch process was performed using MUC-21 (SPP technologies) with SF_6 and C_4F_8

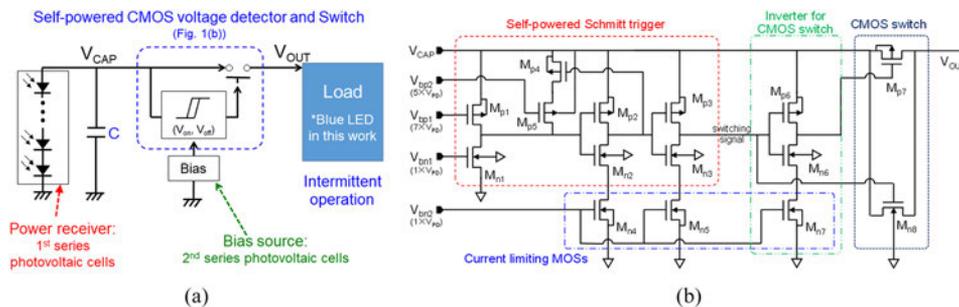


FIG. 1. (a) Block diagram of the proposed CMOS-controlled PV power receiver and (b) schematic of the self-powered voltage detector and switch.

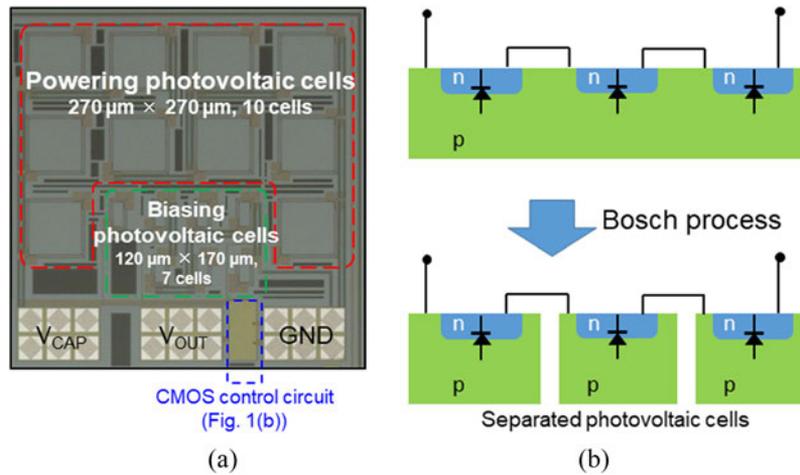


FIG. 2. (a) Layout of the CMOS chip and (b) post processing to separate the integrated PV cells.

as process gases, which are widely used for Si. The conditions for the process are: 180 cycles of etching for 12 s with SF₆ and 8-s-long passivation with C₄F₈.

The etching process separates the Si substrate structure that works as the p-layer of the PV cells; the cells are physically and electrically connected by the metal wiring layers in the remaining upper structure of the CMOS chip. The total thickness of the remaining upper structures is typically less than 10 μm, and the structure is quite fragile. Therefore, after the separation process, in order to prevent breakage of the chip, the chip was molded with an epoxy resin from the backside before detachment from the glass substrate.

It should be noted that some previous reports suggested the idea of using a p⁺-diff/n-well/p-sub structure for an integrated PV cell.^{20,21} Because we had a pn junction (p⁺-diff/n-well diode) isolated from the substrate by a reverse-biased pn junction (n-well/p-sub), we expected stacked p⁺-diff/n-well PV cells to generate an increased PV voltage without any post processing. However, the photocurrent generated between the n-well and (grounded) p-sub reduces the voltage and current generated by the stacked p⁺-diff/n-well PV cells, especially at longer wavelengths.²¹ Therefore, we opted to physically separate the integrated PV cells using post processing.

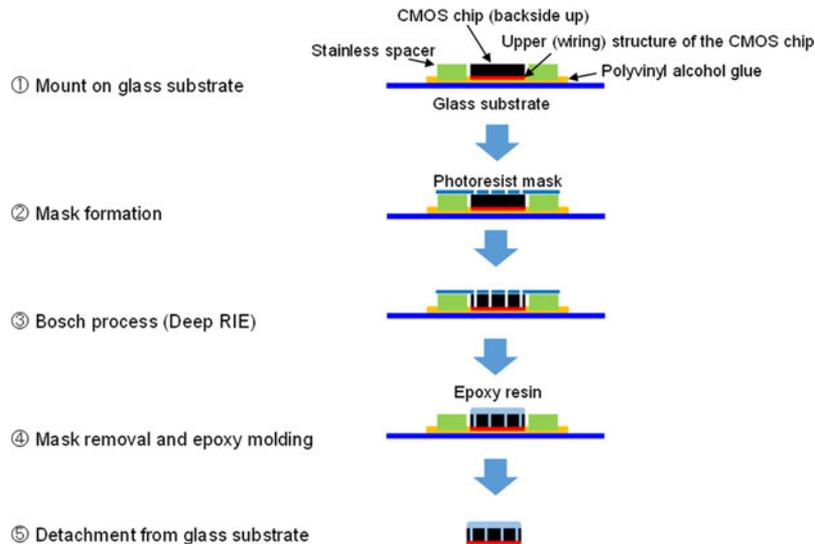


FIG. 3. Process flow to separate the integrated PV cells.

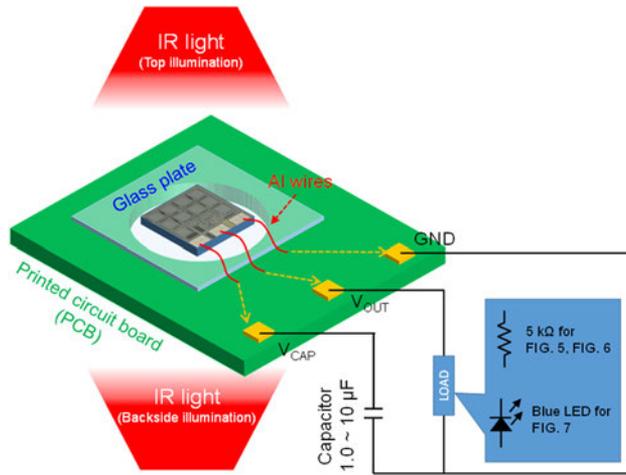


FIG. 4. Experimental setup for the bench-top characterization.

We optimized the separation process and successfully obtained a voltage of 400–450 mV for each PV cell. Not only did we confirm the expected functionality of the series PV cells, we also discovered that we could obtain PV energy from backside illumination. This finding provides additional options for device integration. The external quantum efficiencies of the integrated PV cells were approximately 44% for topside illumination and 2.3% for backside illumination for a chip thickness of 150 μm. The chip was illuminated by an IR LED light source with a peak wavelength of 860 nm.

We tested the CMOS-controlled charge and operation cycles using bench-top measurements. Figure 4 shows the experimental setup for the bench-top characterization with a resistive load (for Figs. 5 and 6) and an InGaN blue LED load (Fig. 7). As seen in Fig. 4, the CMOS integrated PV

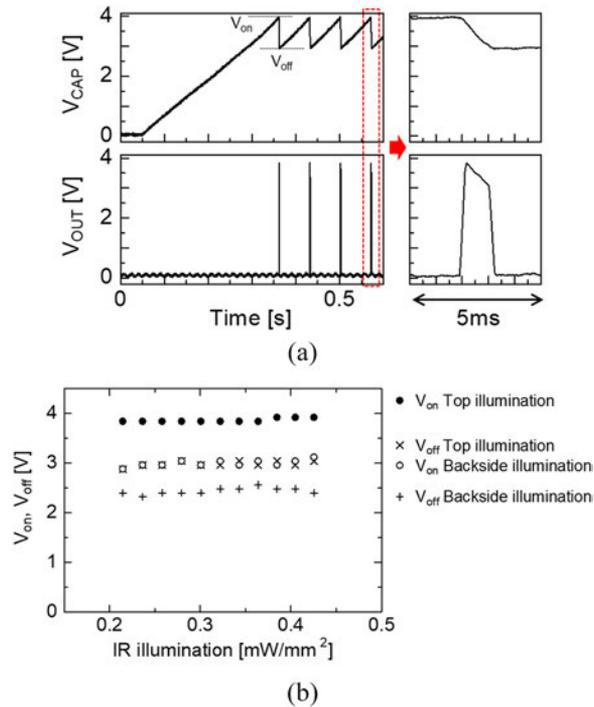


FIG. 5. (a) V_{CAP} and V_{OUT} traces during the PV charge and operation cycles. (b) V_{on} and V_{off} as functions of illumination. The IR excitation light with 860 nm was supplied by arrayed IR LEDs. A 1-μF capacitor and a 5-kΩ resistance load were used for these measurements.

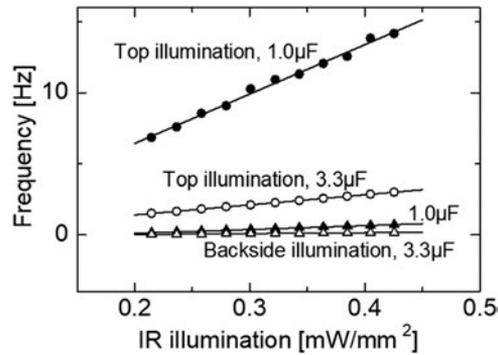


FIG. 6. Operating frequency of CMOS-controlled integrated PV power receiver. The experimental setup was the same as in Fig. 5.

power receiver chip was mounted on a universal printed circuit board (PCB). The CMOS chip was mounted on a glass placed over the hole on the PCB to perform backside illumination. V_{CAP} , GND, and V_{OUT} pads on the CMOS chip were connected to printed patterns on the PCB. The external capacitor and the load device (a 5-k Ω resistance or a blue LED) were connected outside the PCB. The CMOS chip was illuminated by an array of 5 \times 5 IR LEDs (Osram SFH4550) operated with 47 mA. The peak wavelength of the IR LED was 860 nm. The illumination intensity was varied by changing the distance between the IR LED array and the CMOS chip. The illumination intensity at the CMOS chip was calibrated using a conventional optical power meter (Thorlabs S112C).

Blue LED emission intensity traces shown in Fig. 7 were measured with a Si photodiode sensor (0.8 \times 0.9 mm², Optotechno Co. LTD., custom-made) placed close to the blue LED. The sensitivity

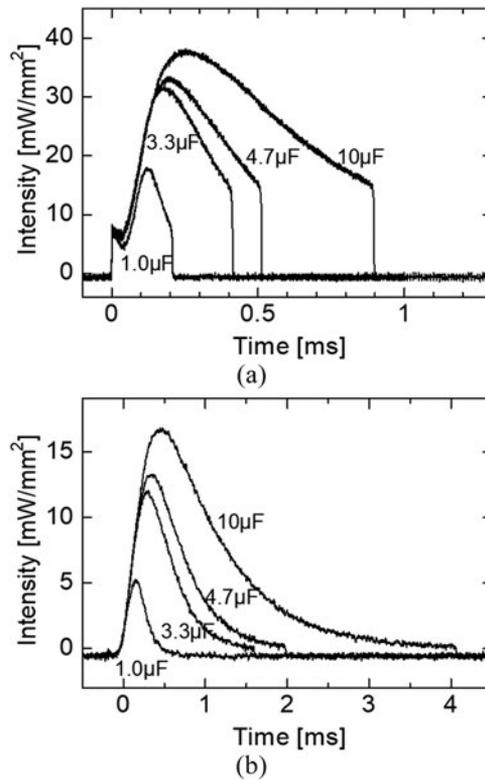


FIG. 7. Emission intensity trace obtained for an InGaN blue LED driven by the CMOS-controlled integrated PV power receiver with different capacitances. (a) shows the top-side illumination, and (b) shows the back-side illumination.

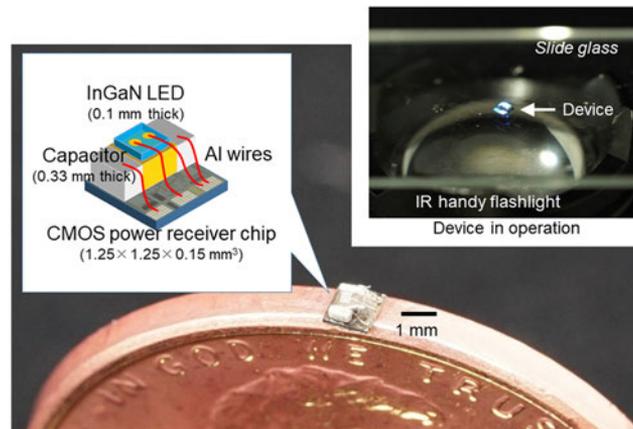


FIG. 8. Implantable optogenetic neural stimulator based on a CMOS-integrated PV power receiver. The upper-right photo shows the light-emitting operation of the device. The device was mounted on a slide glass and operated by an IR handy flashlight. Multimedia view: <https://doi.org/10.1063/1.5024243.1>

of the photodiode sensor was experimentally calibrated using a continuously operated blue LED and the above-mentioned optical power meter (Thorlabs S112C).

To demonstrate the 1-mm³-large device [Fig. 8 (Multimedia view)], we mounted it on a slide glass and illuminated the backside of the CMOS chip using a commercially available IR flashlight. The emission peak wavelength of the IR flashlight was 850 nm and the illumination intensity was approximately 0.6 mW/mm².

Figure 5(a) shows V_{CAP} and V_{OUT} traces obtained during the IR-driven operation in the setup shown in Fig. 4. A 5-k Ω resistance was used as the load. The capacitance was 1.0 μ F and the illumination was 0.43 mW/mm². The chip was illuminated from the top side. The CMOS integrated PV power receiver successfully generated pulses of power. Under this operating condition, $V_{on} = 3.92$ V and $V_{off} = 3.04$ V were obtained. Figure 5(b) shows the turn-on voltage V_{on} and turn-off voltage V_{off} as functions of the IR illumination on the integrated PV power receiver chip. As shown in Fig. 5(b), V_{on} and V_{off} are almost independent of IR illumination within each operating mode, i.e., top-illumination and backside-illumination. The values of V_{on} and V_{off} show a very small increase according to the IR illumination in each of the operating modes. However, between the threshold voltages for top-illumination and backside-illumination operations, the difference is as large as 1 V. As previously mentioned, the quantum efficiency of the integrated PV cell in the backside-illumination operation is less than 1/10 of that for the top-illumination operation. The mismatch of the V_{on} and V_{off} between the top-illuminated and backside-illuminated operations is attributed to lower open-circuit voltages, which are due to the lower photocarrier generation in the backside-illumination operation. They give lower bias voltages shown in Fig. 1(b), which lead to lower V_{on} and V_{off} .

Figure 6 shows the operating frequency of the CMOS integrated PV power receiver as a function of the illumination and the capacitance. The operation frequency was roughly proportional to the illumination intensity, and was inversely proportional to the capacitance. This result is consistent with the linear relationship between the photocurrent and illumination, as well as with the relationship between the charging time and capacitance.

One of the primary target applications of the proposed integrated PV power receiver is implantable electronic devices, especially implantable optical neural stimulators,²⁻⁵ which can provide local light stimulation to the brain or any other neural system. To confirm the functionality of the proposed device as an implantable optical stimulator, we replaced the 5-k Ω load with an InGaN LED chip. The LED chip is a commercially available bare chip of size 280 μ m \times 355 μ m, and has a peak emission wavelength of 470 nm. It typically produces an output power of 1.4 mW (\sim 13 mW/mm²) at 5 mA.

Figure 7 shows the experimentally obtained emission intensity traces in (a) top-illumination and (b) backside-illumination operation modes. The emission traces were measured for different

capacitances, ranging from 1.0 to 10 μF . In both operation modes, peak emission intensities greater than 10 mW/mm^2 were successfully obtained. This covers the stimulation intensity range required for ChR2, which is a commonly used protein in optogenetics.²² The typical stimulation intensity for well-expressed ChR2 is suggested to be 1–10 mW/mm^2 or even smaller.

We obtained a longer pulse duration for larger capacitances. In the top-illumination operation, the turn-off voltage V_{off} is approximately 3 V, at which time the LED emits light. Therefore, the ends of the light pulses in Fig. 7(a) are defined by the turn-off of the power supply from the capacitor to the blue LED. On the other hand, in the backside-illumination operation (Fig. 7(b)), V_{off} is approximately 2.4 V, at which time the LED does not emit light. This makes the ends of the emission pulses in Fig. 7(b) gradually decrease to zero. The power supply to the LED was turned off after the end of the blue light emission observed in Fig. 7(b). This difference causes a longer pulse duration under backside-illumination conditions.

In either operation mode, the pulse duration is as short as 0.2–4 ms, and this spans only a part of the required stimulation duration in optogenetic applications. In many cases, pulse durations within the range of 1–20 ms are selected for wireless optogenetic stimulation.^{3,23–25} For the current design, we did not integrate a current-conditioning circuit for the LED. Therefore, the emission intensity of the LED exhibited a temporal dependence owing to the voltage change during the operation. The circuit drives the LED at a maximum available voltage, and it causes the capacitor to rapidly discharge, after which it has a shorter pulse duration. To control the stimulation intensity and maximize the pulse duration, it is important to control the LED drive current. In future studies, we will introduce a current-limiting MOS transistor to regulate the illumination intensity. We expect to achieve a stimulation intensity of 10 mW/mm^2 with a pulse duration of 10 ms by implementing a current regulator in the CMOS chip, and by subsequently selecting an appropriate capacitor to provide the required pulse duration.

As shown in Figs. 5–7, the present CMOS integrated PV power receiver can be operated with an IR intensity range less than 1 mW/mm^2 . Generally, IR illumination causes heat generation and other biological effects. The effect of IR illumination on tissues has been an area of interest as a method of phototherapy for a long time because it is expected to have various positive effects in living bodies, such as enhanced recovery from injuries or strokes in the brain.^{23–26} Based on studies in the area of phototherapy, the illumination intensity of 1 mW/mm^2 is within the intensity range of low-level laser (or LED) therapy (LLLT).^{23,24} Further, from simulations²⁵ and experiments,²⁶ it is found that the temperature elevation due to this level of IR illumination (1 mW/cm^2) is less than 1°C, or may even be negligible. This means that the application of IR illumination to drive the present CMOS integrated power receiver will not cause any serious damage to target tissues such as the brain. In addition, even if any positive biological response is available as a therapeutic scheme, it will be a long-term response,^{23,24} and will not have an effect in most optogenetic applications.

After the bench-top functional characterization, we integrated the CMOS chip with an external capacitor, and the InGaN LED chip into an implantable optical neural stimulator. Figure 8 (Multimedia view) shows the structure and the photograph of the device. We took advantage of the voltage generation from backside illumination to develop the compact structure shown at the top-left of Fig. 8 (Multimedia view). A 2.2- μF capacitor was integrated for this specific device. As shown in Fig. 3, we made wafer-penetrating trenches to separate the integrated PV cells on the CMOS chip, and we filled the trenches with epoxy resin. Therefore, the CMOS chip may be handled using conventional tweezers. We mounted the CMOS chip on a glass slide using poly(vinyl alcohol) (PVA) for the packaging process. The capacitor and the InGaN blue LED were integrated by hand on the CMOS chip using epoxy or UV-cure acryl resin. Typical dimensions of the capacitor are 1.0 mm \times 0.5 mm \times 0.33–0.5 mm. As mentioned previously, the size of the InGaN LED is 280 μm \times 355 μm , and the thickness is approximately 90 μm . After the resin was cured, Al wires were bonded between the components (two wires between the CMOS chip and the capacitor, and two wires between the CMOS chip and the LED). A conventional manual wedge-wire bonder was used for the bonding process. Finally, the top side of the device, including the CMOS chip surface and all off-chip components were molded with epoxy or UV-cure acryl resin.

The total thickness of the stacked devices is approximately 0.6 mm (with a 0.33-mm-thick capacitor), and the estimated volume of the device is less than 1 mm^3 , including the epoxy and acryl

resin for molding. To the best of our knowledge, this device is the world's smallest wireless optical neural stimulator powered using an electric circuit. The device can be operated by IR light sources (such as the IR handy flashlight at the top-right side of Fig. 6), as is expected from the characteristics shown in Figs. 5–7.

Table I shows specifications of the present CMOS-integrated PV power receiver chip and the implantable optogenetic neural stimulator. Table II shows a comparison with other wireless optogenetic stimulators in previous works.^{3,4,27–32} The greatest advantages of the present device are its small dimensions and light weight. Both the volume and weight are almost one order of magnitude smaller than any of the preceding works. This size is realized by the PV power transfer and intermittent operation scheme adopted in this work. Electromagnetic power transfer is a limiting factor in the integration of the power receiving coil. The minimum diameter of the coils for the devices in Table II is 1.6 mm,³ which is larger than any dimension of the device realized in this work. However, as a drawback, the present device can be applied only for pulse stimulation, and requires a charge time for each stimulation. As mentioned previously, we aim to improve the circuit in order to realize optogenetic stimulation with 10 mW/mm² and 10 ms. Furthermore, we can increase either the stimulation intensity or pulse duration by integrating a larger capacitor.

Considering that most optogenetic stimulations are performed not with a single pulse, but with multiple pulses (pulse train), we also need to improve the power-receiving and conversion efficiency. As shown in Table I, the system-wise power-conversion efficiency from IR excitation light to blue stimulation light is 4.7% for the top-illumination operation and 0.16% for the backside-illumination operation. These values are realistic limits of the duty ratio in pulse-train stimulation (with no intensity boost from IR to blue light). In general, a duty ratio value of less than 20% is employed in optogenetic stimulations. It is reasonable to adopt the top-illumination scheme for the next-generation optogenetic stimulation device, and this will improve the system-wise power-receiving and conversion efficiency from 4.7% to over 20% by performing circuit refinements.

In this work, we developed a CMOS-based power receiver using integrated PV cells. The expected application is the field of implantable microelectronic devices and IoT micro-nodes. We obtained the expected functionality of the chip using the integrated-series PV cells, and an adequate PV voltage was generated. A self-powered voltage-monitoring circuit monitored the voltage of the capacitor and automatically switched for an intermittent LED operation. We demonstrated blue light emission from an InGaN LED powered by IR light. We integrated the components and developed a 1-mm³ implantable optical neural stimulator.

TABLE I. Specifications of the present optogenetic neural stimulator with integrated PV power receiver.

CMOS chip size	1.25 mm × 1.25 mm × 0.15 mm
Integrated PV cells for powering	270 μm × 270 μm N-well/P-sub 10 series photodiodes
Integrated PV cells for biasing	120 μm × 270 μm N-well/P-sub 7 series photodiodes
External quantum efficiency of integrated PV cell	Top illumination: 44% Backside illumination: 2.3%
Power consumption for control circuit	Approx. 1 μW
Minimum illumination for stable operation	0.21 mW/mm ² (860 nm)
Integrated LED	InGaN on sapphire, 470 nm
System-wise optical power conversion efficiency (Up-conversion efficiency from IR to blue light)	Top illumination: 4.7% Backside illumination: 0.16%
Integrated device size	Approx. 1.3 mm × 1.3 mm × 0.6–1.0 mm
Integrated device weight	2.3 mg
	Top-illumination C=1 μF: 18mW/mm ² , 0.21 ms C=10 μF: 38 mW/mm ² , 0.9 ms
Peak stimulation intensity and pulse duration	Backside-illumination C=1 μF: 5 mW/mm ² , 0.7 ms C=10 μF: 17 mW/mm ² , 4 ms

TABLE II. Comparison of the specifications with preceding wireless optogenetic devices.

Reference	Kim <i>et al.</i> ^{27,28}	Montgomery <i>et al.</i> ³	Shin <i>et al.</i> ²⁹	Lee <i>et al.</i> ³⁰	Park <i>et al.</i> ⁴	Park <i>et al.</i> ³¹	Jia <i>et al.</i> ³²	This work
Architecture	Discrete device based	Discrete device based	Discrete device based	LSI-based	Discrete device based	Discrete device based	LSI-based	LSI-based
Substrate	Flexible/rigid PCB	Rigid PCB	Flexible PCB	Stacked Rigid PCB	Rigid PCB	Stretchable polymer	Flexible PCB	Substrate-less
Dimensions	Approx. 14 mm × 12.5 mm × 3 mm ^a	Approx. 2 mm × 2 mm × 2 mm ^a	Diameter 9.8 mm, Thickness <1.3 mm	12 mm × 7 mm × 11 mm	2.4 mm × 3.5 mm × 8.5 mm	3.8 mm × 6 mm × 0.7 mm	Diameter 4.5 mm Thickness 0.6 mm	1.3 mm × 1.3 mm × 0.6–1.0 mm
Approximate volume	300 mm ³	8 mm ³	98 mm ³	924 mm ³	71 mm ³	16 mm ³	9.5 mm ³	1–1.7 mm ³
Weight	0.7 g	20–50 mg	~30 mg	~1.6 g	70 mg	16 mg	24 mg	2.3 mg
Power supply scheme	RF 910 MHz	RF 1.6 GHz	RF 13.56 MHz	RF 2.4 GHz	RF 1.6–2.5 GHz	RF 2.0–2.5 GHz	RF 60 MHz	Photovoltaic Visible–NIR
Number of LEDs	4	1	2	1	1	1	4	1
Available stimulation intensity	17.7 mW/mm ²	25.8 mW/mm ²	Up to 100 mW/mm ²	27 mW/mm ²	75 mW/mm ²	10 mW/mm ²	10 mW/mm ²	15 mW/mm ²

^a Approximate dimensions were estimated from figures/photographs in the references.

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- ¹ H. M. Lee, H. Park, and M. Ghovanloo, *IEEE J. Solid-State Circuits* **48**, 2203 (2013).
- ² A. J. Yeh, J. S. Ho, Y. Tanabe, E. Neofytou, R. E. Beygui, and A. S. Y. Poon, *Appl. Phys. Lett.* **103**, 163701 (2013).
- ³ K. L. Montgomery, A. J. Yeh, J. S. Ho, V. Tsao, S. Mohan Iyer, L. Groseknick, E. A. Ferenczi, Y. Tanabe, K. Deisseroth, S. L. Delp, and A. S. Y. Poon, *Nat. Methods* **12**, 969 (2015).
- ⁴ S. Il Park, G. Shin, A. Banks, J. G. McCall, E. R. Siuda, M. J. Schmidt, H. U. Chung, K. N. Noh, J. G.-H. Mun, J. Rhodes, M. R. Bruchas, and J. A. Rogers, *J. Neural Eng.* **12**, 056002 (2015).
- ⁵ D. Ahn and M. Ghovanloo, *IEEE Trans. Biomed. Circuits Syst.* **10**, 125 (2016).
- ⁶ D. Brunelli, C. Moser, L. Thiele, and L. Benini, *IEEE Trans. Circuits Syst. I Regul. Pap.* **56**, 2519 (2009).
- ⁷ H. Kim, Y. Min, C. Jeong, K.-Y. Kim, C. Kim, and S. Kim, *IEEE Trans. Circuits Syst. II Express Briefs* **60**, 331 (2013).
- ⁸ J. Sankman, H. Chen, and D. Ma, Proc. IEEE Int. Symp. Circuits Syst. 2011, 2541 (2011).
- ⁹ W. Nattakarn, M. Haruta, T. Noda, K. Sasagawa, T. Tokuda, M. Sawan, and J. Ohta, 39th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC17), FrDT16-05.1 (2017).
- ¹⁰ W. Nattakarn, M. Haruta, T. Noda, K. Sasagawa, T. Tokuda, M. Sawan, and J. Ohta, *Jpn. J. Appl. Phys.* **57** (2018) in press.
- ¹¹ N. J. Guilar, T. J. Kleeburg, A. Chen, D. R. Yankelevich, and R. Amirtharajah, *IEEE Trans. Very Large Scale Integr. Syst.* **17**, 627 (2009).
- ¹² S. Ayazian, V. A. Akhavan, E. Soenen, and A. Hassibi, *IEEE Trans. Biomed. Circuits Syst.* **6**, 336 (2012).
- ¹³ G. Moayeri Pour, M. K. Benyhesan, and W. D. Leon-Salas, *IEEE Trans. Circuits Syst. II Express Briefs* **61**, 501 (2014).
- ¹⁴ U. Cilingiroglu, B. Tar, and C. Ozmen, *IEEE Trans. Circuits Syst. I Regul. Pap.* **61**, 2491 (2014).
- ¹⁵ A. S. Weddell, G. V. Merrett, and B. M. Al-Hashimi, *IEEE Trans. Circuits Syst. I Regul. Pap.* **59**, 1196 (2012).
- ¹⁶ S. Mondal and R. P. Paily, 19th International Symposium on VLSI Design and Test, 1 (2015).
- ¹⁷ G. Liu, R. Fuentes, H. Koser, and T. Kaya, *Analog Integr. Circuits Signal Process.* **83**, 203 (2015).
- ¹⁸ K. Takakubo and H. Takakubo, *IEICE Trans. Fundamentals of Electronics, Communications and Computer Sciences* **E92-A**, 443 (2009).
- ¹⁹ I. Mori, M. Kubota, E. Lebrasseur, and Y. Mita, 2014 Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP) 1 (2014).
- ²⁰ R. D. Prabha and G. A. Rincón-Mora, IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS 2013), 368 (2013).
- ²¹ Y.-J. Hung, H.-W. Su, C.-L. Chun, J.-F. Chen, C.-W. Huang, and M.-S. Cai, *IEEE Electron Device Lett.* **36**, 1169 (2015).
- ²² E. S. Boyden, F. Zhang, E. Bamberg, G. Nagel, and K. Deisseroth, *Nat. Neurosci.* **8**, 1263 (2005).
- ²³ S. Farivar, T. Malekshahabi, and R. Shiari, *J. Lasers Med. Sci.* **5**, 58–62 (2014).
- ²⁴ M. R. Hamblin, *BBA Clin.* **6**, 113–124 (2016).
- ²⁵ M. Nourhashemi, M. Mahmoudzadeh, and F. Wallois, *Neurophotonics* **3**, 15001 (2016).
- ²⁶ T. A. Henderson and L. D. Morries, *Neuropsychiatr. Dis. Treat.* **11**, 2191–2208 (2015).
- ²⁷ T.-i. Kim *et al.*, *Science* **340**, 211–216, (2013).
- ²⁸ J. G. McCall *et al.*, *Nat. Protoc.* **8**, 2413–2428 (2013).
- ²⁹ G. Shin *et al.*, *Neuron* **93**, 509–521 (2017).
- ³⁰ S. T. Lee, P. A. Williams, C. E. Braine, D. Lin, S. W. M. John, and P. P. Irazoqui, *IEEE Trans. Neural Syst. Rehabil. Eng.* **23**, 655–664 (2015).
- ³¹ S. Il Park *et al.*, *Nat. Biotechnol.* **33**, 1280–1286 (2015).
- ³² Y. Jia, S. A. Mirbozorgi, B. Lee, W. Khan, F. Madi, A. Weber, W. Lee, and M. Ghovanloo, Digest of technical papers, 2018 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 468-470 (29.5) (2018).