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A CMOS 90NM DIGITAL PIXEL SENSOR INTENDED FOR A VISUAL CORTICAL STIMULATOR

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MÉMOIRE PRÉSENTÉ EN VUE DE L'OBTENTION DU DIPLÔME DE MAÎTRISE ÈS SCIENCES APPLIQUÉES
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UNIVERSITÉ DE MONTRÉAL

ÉCOLE POLYTECHNIQUE DE MONTRÉAL

Ce mémoire intitulé :

A CMOS 90NM DIGITAL PIXEL SENSOR INTENDED FOR A VISUAL CORTICAL STIMULATOR

présenté par : Mme. GHANNOUM Roula.
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M. SAWAN Mohamad, Ph.D., membre et directeur de recherche.
M. ZHU Guchuan, Doct., membre.

"Learn from the mistakes of others. You cannot live long enough to make them all yourself."
- Eleanor Roosevelt

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Résumé

La capture d'images et le traitement d'images et de signaux font partie des domaines les plus en vogue de nos jours. Un autre domaine qui retient l'attention des chercheurs à travers le monde est celui qui regroupe les applications biomédicales - en particulier celles qui font le pont entre l'électronique et la biologie. L'équipe Polystim œuvre sur différents projets à la pointe de la technologie qui touchent à ces domaines, dont le projet Cortivision: un stimulateur visuel cortical. Le système englobe la capture et le traitement d'images ainsi que la stimulation du cortex pour donner une certaine perception d'images aux patients souffrant de cécité. Le but de ce travail est de concevoir le module de capture d'images de ce système. Les modes d'opération du capteur d'images doivent être configurables par l'usager. Il doit se distinguer par une gamme dynamique élevée, une consommation de puissance réduite, une haute vitesse d'acquisition, une surface réduite, la portabilité, la possibilité d'avoir du traitement d'images sur puce, et la facilité de l'intégrer dans un système sur puce avec le reste des modules de Cortivision. Un DPS (Digital Pixel Sensor) CMOS a été conçu et fabriqué avec la nouvelle technologie CMOS 90nm. Chaque pixel comprend une photodiode, un circuit de conversion de photocourant, un convertisseur analogique à numérique et une mémoire numérique de 8 bits, dans une surface de 9 μm x 9 μm avec un facteur de remplissage de 26% et 57 transistors. Le capteur offre plusieurs modes d'opération:

- Un mode d'intégration linéaire.
- Un mode logarithmique avec une gamme dynamique étendue qui permet d'accéder aux pixels indépendamment du temps mais avec une diminution de linéarité et un bruit plus prononcé.
- Un mode différentiel qui soustrait deux images successives à même la puce pour obtenir une image binaire. Ce mode permet d'accélérer le traitement d'images et fonctionne à une vitesse plus élevée. Il peut être utilisé simultanément avec le mode linéaire ou avec le mode logarithmique.
- Un mode d'expositions multiples qui est une option du mode linéaire pour augmenter la gamme dynamique, mais qui aurait l'effet de réduire la vitesse d'acquisition.

Des prototypes de puces ont été fabriqués avec la technologie CMOS 90nm offerte par STMicroelectronics avec des matrices de 64x48 pixels et un module de test avec plusieurs points d'accès pour caractériser la puce. Un PCB doté d'une architecture très flexible a aussi été conçu et fabriqué afin de tester la puce et de l'interfacer avec un contrôleur VHDL implanté dans un FPGA Spartan-3. L'implémentation finale démontre une réduction d'un facteur de trois de la surface du pixel comparé à une architecture moins récente implémentée en CMOS $0.18\mu m$ dans le Laboratoire de Neurotechnologies Polystim, tout en proposant une méthode pour régler une fuite potentielle de l'obturateur du pixel en atteignant un débit d'au moins 400 images par seconde. Par contre, les courants de fuite de la technologie CMOS 90nm ont contribué à un décalage non-négligeable entre les mesures expérimentales et les simulations "post-layout". Une partie des résultats a fait l'objet d'un article de conférence IEEE intitulé "A 90nm CMOS Multimode Image Sensor Intended for a Visual Cortical Stimulator".

Abstract

The image sensing and image processing fields make up some of the hottest topics in today's industrial and research communities. Another field that is getting a lot of attention is biomedical applications - especially the combination of electronics to biology. The Polystim team is working on some state-of-the-art projects encompassing all that. One of these is the Cortivision project that consists of a visual cortical stimulator. The system comprises image sensing, image processing, and brain cortex stimulation to help blind patients acquire a sense of visual perception.

The goal of this work is to cover the image sensing portion of the system. This requires the design and implementation of an image sensor which is user configurable to operate in several modes, has a high dynamic range, low power consumption, high frame rate capability, reduced surface area, is portable, allows some on-chip image processing, and can easily be integrated in a system-on-chip with the rest of the Cortivision modules.

A CMOS Digital Pixel Sensor was designed and fabricated using the novel CMOS 90nm technology. Each pixel consists of a Photodiode, a photo-current conversion circuit, an Analog-to-Digital Converter and a digital 8-bit memory. It has a pixel pitch of 9μm with a Fill-Factor of 26% and 57 transistors. The sensor offers several modes of operation:

- A linear integration mode.
- A logarithmic mode that extends the dynamic range and allows time-independent pixel access at the cost of a forsaken linearity and an increase in noise.
- A differential (or better termed difference) mode that allows subtracting two consecutive frames to obtain a binary image. This mode helps speed up the image processing and allows a very high frame rate. It can be used in conjunction with either the linear or the logarithmic modes of operation.
- A multiple exposure mode that can be used in combination with the linear mode to increase the dynamic range at the expense of a decrease in frame rate.

Prototype chips were manufactured using the CMOS 90nm process offered by

STMicroelectronics with 64x48 pixel matrices and a test module with different access nodes to characterize the design. A PCB was also designed and manufactured with a very flexible architecture to allow testing the chip and interfacing it with a VHDL controller implemented using a Spartan-3 Development Board. The final implementation shows a three-fold reduction in the surface area of the pixel as compared to a less recent architecture implemented in CMOS 0.18μm at the Polystim Neurotechnologies Lab, all while putting forth a method for circumventing shutter leakage while still reaching an acquisition rate exceeding 400 frames per second. Nevertheless, current leakage in the CMOS 90nm technology has led to a substantial discrepancy between experimental measurements and post-layout simulation results. An IEEE paper entitled "A 90nm CMOS Multimode Image Sensor Intended for a Visual Cortical Stimulator" sheds some light on part of the results.

Condensé

Le but de ce travail est de concevoir et d'implémenter un système de capture d'images capable d'acquérir des images de qualité à un débit élevé tout en étant flexible, portable, et capable de transmettre des images à un module de traitement qui est chargé de reconstituer une image tridimensionnelle. Cette image serait ensuite échantillonnée et utilisée pour stimuler le cortex visuel par des courants transmis par des microélectrodes créant des points de lumière (des phosphènes). Ceci est considéré comme une extension des travaux de notre équipe en CMOS $0.18\mu m$ [1].

Pour parvenir à cela, une revue des capteurs d'images électroniques était nécessaire pour établir une comparaison entre les capteurs CCD et les CMOS, pour conclure que les capteurs CMOS sont mieux adaptés à notre application, Cortivision, car ils permettent d'intégrer plusieurs fonctionnalités et modules à même la puce - ce qui essentiel pour créer des systèmes compacts à basse consommation de puissance. De plus, les capteurs CCD constituent une charge capacitive non-négligeable qui est plus difficile à intégrer dans un système. Aussi, la qualité d'image des capteurs CMOS est devenue assez proche de celle des CCD ces dernières années, tout en offrant la possibilité d'avoir un débit plus élevé à cause des convertisseurs analogique à numérique (CAN) intégrés sur la puce, et en ayant une sortie numérique qui est plus pratique qu'une sortie analogique. Le procédé de fabrication CMOS est aussi moins dispendieux que le procédé CCD, et nous est disponible à travers la CMC et STMicroelectronics. Ce procédé permet aussi un redimensionnement moins compliquée de la matrice de pixels ainsi que la sélection d'une sous-fenêtre de la matrice.

La conception du capteur a mis l'emphase sur l'acquisition d'images de bonne qualité à un débit élevé pour ne pas être le goulot d'étranglement du système de traitement d'images 3D. Ceci inclut la conception d'un CAN précis avec une assez haute fréquence d'opération. La caméra conçue offre à l'usager la possibilité de choisir parmi plusieurs modes d'opérations linéaires ou logarithmiques. Le mode linéaire est le préféré pour les cas ou le bruit est un paramètre important. Cependant, ce mode a un débit moins élevé qui dépend du temps d'intégration requis. Le mode logarithmique est intéressant pour les scènes qui ont des régions avec des intensités vraiment faibles et d'autres avec des intensités assez prononcées à cause d'une gamme

dynamique plus étendue. Cela est accompagné par contre d'un manque de linéarité et d'une augmentation du bruit. Le mode d'intégration linéaire permet à l'usager aussi d'utiliser des expositions multiples pour augmenter la gamme dynamique, par contre en devant réduire le débit encore plus. Un autre mode d'opération est le mode différentiel qui soustrait deux images consécutives dans le pixel. Le résultat est une image binaire. Ce mode a un gros impact sur la rapidité du traitement 3D.

En ce qui concerne l'architecture adoptée, un DPS (Digital Pixel Sensor) a été choisi au lieu d'un APS (Active Pixel Sensor). La différence principale entre ces deux architectures est que la première intègre le CAN (Convertisseur Analogique-Numérique) dans le pixel tandis que la deuxième a un seul CAN partagé par toute la matrice. Le DPS permet donc d'avoir un débit plus élevé car la conversion se fait à l'intérieur des pixels simultanément. Ceci dit, le DPS a un nombre plus élevé de transistors par pixel, ce qui réduit le facteur de remplissage. Aussi, les variations du procédé CMOS entrainent plus de différences entre les pixels que pour un APS. Par contre, l'augmentation du nombre de pixels est moins critique pour le débit dans le cas d'un DPS. Aussi le DPS permet de repartir la matrice sur plusieurs sorties de la puces - si le nombre d'entrées-sorties le permet, car la valeur lue du pixel est une valeur numérique facile à manipuler.

Pour le DPS, le circuit de chaque pixel est formé d'une photodiode, d'un amplificateur (un suiveur), un CAN, et une mémoire de 8 bits (voir la Figure 2.13 pour une architecture typique). Cette mémoire permet d'avoir un accès aléatoire aux pixels de la matrice si le circuit de lecture utilise un décodeur. L'architecture utilisée pour la mémoire est régénérative, donc la valeur n'est pas perdue facilement (voir Figure 4.6) . Ceci était nécessaire car la technologie CMOS 90nm souffre de beaucoup de courants de fuite. Par contre, cela a entrainé une augmentation du nombre de transistors par pixel. Chaque pixel comprend 57 transistors (dont 40 pour la mémoire). La technologie CMOS 90nm facilite l'intégration de plus de transistors dans la même surface. Chaque pixel occupe 9 μm x 9 μm avec un facteur de remplissage de 26%. La surface du circuit (sans les entrées-sorties) est de 603 μm x 477 μm pour une matrice de 64x48 pixels. Une méthode a été introduite pour éviter toute fuite de l'obturateur du pixel (voir Figure 4.4), mais avec un effet sur la linéarité du système. Pour régler le problème de manque de précision du CAN du prototype conçu par notre groupe avant celui-ci, le nombre supérieur de masques possible avec la technologie CMOS 90nm a été exploité pour concevoir un condensateur à capacité plus élevée

(voir Figure 4.5). Une autre topologie de CAN à entrées différentielles a été étudiée (voir l'Annexe C) ; cependant, le mode différentiel a nécessité l'ajout d'un condensateur et les simulations montraient une tension de décalage plus prononcé - donc la topologie de capacité commutée a été retenue (avec quelques modifications). En ce qui concerne l'alimentation, les tensions ont été baissées de 1.8V/3.3V à 1V/2.5V offrant une meilleure consommation de puissance.

Des puces ont été fabriquées avec une matrice de 64x48 pixels avec la technologie CMOS 90nm offerte par STMicroelectronics et un article IEEE qui rapporte une partie des résultats a été publié [2]. Un module de test a été ajouté pour caractériser le pixel. La première ébauche de ce prototype utilisait un décodeur et un multiplexeur pour lire les valeurs des pixels. Cependant, la surface allouée par la CMC posait une limitation sur le nombre d'entrées-sorties de la puce, donc le circuit de lecture a été remplacé par des registres à décalage. Ceci a aussi limité le nombre de modules de tests à un seul, ainsi que le nombre de nœuds intermédiaires capables d'être sondés.

Pour valider le système, des tests sur la puce ont été effectués avec un montage de test fait sur mesure avec un PCB conçu et implémenté à cette fin qui interface un contrôleur numérique VHDL dans un Spartan-3 de Xilinx, ainsi qu'un analyseur logique pour lire les sorties numériques de la puce. Le PCB est alimenté par un adaptateur qui se branche sur le réseau électrique et qui alimente des régulateurs de tensions sur le PCB qui eux alimentent le reste des composantes ainsi que la puce du capteur. Le PCB comprend aussi des diviseurs de tension qui baissent les sorties du Spartan-3 de 3.3V/0V à 2.5V/0V ou 1V/0V tel que nécessaire. Le PCB comprends aussi des convertisseurs numérique à analogique (CNA) pour générer les tensions de polarisation de la puce (remise en circuit de la photodiode) ainsi que la rampe analogique/numérique. Un CNA à sortie de courant fourni le courant de polarisation de la puce. Ces CNA sont contrôlés par le Spartan-3, et leur opération a été testée et validée.

Finalement, une discussion sur les améliorations possibles a été élaborée. Celle-ci comprend une architecture basée sur des PPD et des microlentilles pour réduire les fuites et augmenter le facteur de remplissage, l'utilisation de filtres de couleur, l'augmentation de la précision du système (au-delà de 8 bits), l'emploi d'un circuit de lecture à plusieurs sorties pour augmenter le débit, l'intégration d'une correction appliquée à chaque pixel pour améliorer la qualité de l'image si le module de traitement l'exige, l'intégration de modules de test additionnels en suivant une stratégie de

conception basée sur la flexibilité de test, l'intégration des signaux de contrôle et de polarisation sur la puce, le choix de la technologie, les condensateurs MiM, le partage de pixels, l'optimisation de l'architecture de la mémoire, et une approche modulaire pour s'assurer que les différentes parties du systèmes sont fonctionnelles avant de l'embarquer dans un système complexe et très varié. Le système final devrait être un système sur puce comprenant le capteur d'images, un module de traitement 3D, et un circuit de contrôle et d'alimentation des électrodes externe au crâne, en espérant avoir un système fonctionnel et efficace pour exaucer notre vœux ultime : rendre la vue aux personnes souffrant de cécité.

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List of Notations and Symbols

3D-IC	Three-Dimensional Integrated Circuit
ADC	Analog-to-Digital Converter
APS	Active Pixel Sensor
BCCD	Buried/Bulk-channel Charge-Coupled Device
BPSG	Boro-Phospho Silicate Glass
CAN	Convertisseur Analogique-Numérique
CAPS	Complementary Active Pixel Sensor
CCD	Charge-Coupled Device
CDS	Correlated Double Sampling
CFA	Color Filter Array
CMC	Canadian Microelectronics Corporation
CMOS	Complementary Metal Oxide Semiconductor
CMY	Cyan, Magenta, Yellow
CNA	Convertisseur Numérique-Analogique
DAC	Digital-to-Analog Converter
DPS	Digital Pixel Sensor
DR	Dynamic Range
DRAM	Dynamic Random Access Memory
DRC	Design Rule Check
DSNU	Dark Signal Non-Uniformity
EHP	Electron-Hole Pair
ESD	Electro-Static Discharge
FD	Floating Diffusion
FET	Field Effect Transistors
FF	Fill-Factor
FIT	Frame Interline Transfer
FPN	Fixed Pattern Noise
fps	frames per second
FT	Frame Transfer
H-CCD	Horizontal Charge-Coupled Device

HDTV	High-Definition Television
ILT	Interline Transfer
I/O	Input/Output
IR	Infrared
IT	Interline Transfer
IT-CCD	Interline Transfer Charge-Coupled Device
JPL	Jet Propulsion Lab
LSB	Least Significant Bit
LVS	Layout Versus Schematic
LWIR	Long-Wave Infrared
MBW	Modified Barrier Well
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MSB	Most Significant Bit
MiM	Metal-Insulator-Metal
MWIR	Mid-Wave Infrared
NASA	National Aeronautics and Space Agency
NIR	Near Infrared
PAPS	Pseudoactive-Pixel-Sensor
PCB	Printed Circuit Board
PD	Photodiode
PG	Photogate
PGA	Programmable Gain Amplifier
PPD	Pinned Photodiode
PPS	Passive Pixel Sensor
PRNU	Pixel Response Non-Uniformity
PT	Phototransistor
QE	Quantum Efficiency
RAM	Random Access Memory
RDS	Reflection-Delayed noise Suppression
RGB	Red, Green, Blue
SCCD	Surface-channel Charge-Coupled Device
SNAP	Shuttered-Node Active Pixel
SNR	Signal-to-Noise Ratio
SoC	System on Chip

STI	Shallow-Trench oxide Isolation
SWIR	Short-Wave Infrared
TDI	Time-Delay-to-Integration
TFA	Thin Film on ASIC
TG	Transfer Gate
V-CCD	Vertical Charge-Coupled Device
VHDL	Very Highly Descriptive Language
VLWIR	Very-Long Wave Infrared

Chapter 1

INTRODUCTION

Image sensors have easily found their way into our everyday lives. They have become part of our daily routines â sometimes without us being even completely aware of it. If you look around you right now, you would probably find a cell phone with an integrated camera lying on some table, a digital camera put away in a drawer, a webcam nonchalantly attached to your desktop computer or even a tiny camera integrated in the screen of your laptop. You leave your apartment, coming down the hallway a security camera is sending your picture to a control center to be relieved by another one in the parking lot of your building. You are backing out of your parking space, and the built-in sensor in your bumper shows you that you are getting too close to that dreaded pillar you had crashed into last time. You then stop at an ATM machine for some cash almost oblivious to the fact that you are getting your picture taken. You are finally on the highway, nothing in sight (or at least so you think), you get carried away and âforgetâ your foot on the accelerator; a few days later you receive a speeding ticket by mail... And this goes on and on... As a consequence, it goes without saying that the prevalence of image sensors in today's society is beyond any shred of doubt. But are image sensors just associated with regular daily tasks and monitoring? The fact is that image sensors are just as important for consumer and professional applications as they are for industrial and medical applications amongst others. These applications vary from still imaging going through video imaging and attaining fast imaging.

For more concrete examples, it is quite tempting to mention some interesting applications in imaging. These could include Sony's Dream Robot, Orange's Mobile VideoPhone, Identix's Fingerprint Scanner, Canesta's Virtual Keyboard, Bendix's IR Night Vision, Toyota Prius' Self-Parking Car, Honda's Lane Control, Given Imaging's Wireless Endoscope Capsules, Suni Medical Imaging's Digital Intraoral Camera â and one of particular interest here: Polystim Neurotechnologies Laboratory's Visual Cortical Stimulator. This project, dubbed Cortivision, is the intended application for

the image sensor which is the subject of this work.

The Cortivision project aims at creating an intra-cortical visual prosthesis to induce visual perception in blind patients by stimulating the visual cortex. Since the system bypasses the retina and the optic nerve, it might be â unlike some of the other projects doted with the same humanitarian aim â a viable solution for people who were born blind or have been blind for a lengthy duration leaving them with damaged retinas or optic nerves. The system to be conceived has certain criteria set in stone; two of which are its portability and the absence of wires or other obvious structures penetrating the cranium. This sets harsh limitations as to the dimensions, power consumption, and means of data transfer. The image acquisition module consists of a projector and an image sensor integrated on glasses â each of them replacing one of the human eyes as per the principle of active stereoscopy. The acquired images are then transmitted to an external image processing module that intelligently selects pixels and shades of gray to create a 3D-feel for the patient. These are then wirelessly transmitted to electrodes implanted in the brain to stimulate the visual cortex producing bright spots â hereafter called phosphenes â allowing the patient to have a good idea of the environment in which s/he is located endowing him or her with a certain extent of autonomy by allowing him or her to avoid obstacles and accomplish basic tasks without seeking the help of others.

The subject of this thesis is the image sensor which constitutes the frontend of the system and is an extension of the work started by Trépanier et al. [3]. As a result, it is to abide by the requirements set by the Cortivision application, while preserving the versatility that accompanies the possibility of it being used for other applications as well.

A question that may arise though: why design and implement our own image sensor and not just buy one off-the-shelf? Basically, our sensor is to be integrated in a complete portable system for our application â so we need to have the possibility to integrate on it as much control circuitry and as much of the image processing circuitry as possible to make the whole processing the quickest possible, the least power consuming possible, and with the least possible area overhead. Part of the processing is already sped up and simplified by a special mode of operation of our sensor, the differential mode (which is actually a difference mode), that subtracts two consecutive image captures.

Since the camera is basically supposed to replace a human eye, a high dynamic

range is a necessity â this would allow the capture of feeble as well as strong light signals in the same image. To boost the dynamic range, a logarithmic mode of operation is implemented along with the regular linear mode of operation. Another important constraint is the frame rate. The image processing module requires the capture of 20 images to generate a single processed image. Therefore, if we aim at having a final system having a rate of 20 images per second (to rival the human eye), we are required to have an image sensor that can deliver images at a rate of at least 400 frames per second (fps). Furthermore, the portability of the finished system imposes minimal possible dimensions and power consumption. Also, many particularities inherent to the CMOS 90nm technology have led to its adoption for the implementation of the Cortivision image sensor. These include, but are not limited to, reduced feature size (hence reduced area) and the novelty of this technology in image sensor research. This is while bearing in mind that smaller technologies (even 65nm) are being used by the image sensor industry, but are yet to appear in academic research mainly due to the higher cost of these, decreased availability and design overhead. Moreover, industrial research is in its greater part confidential and not accessible to scholars.

The first chapter will discuss the fundamentals of electronic image sensors. The second one will highlight some of the state-of-the-art work in CMOS image sensor research. Chapter 3 will describe the adopted architecture, and Chapter 4 will deal with the implementation, issues faced, and discuss any possible future improvements or suggestions. Details that might be of lesser impact to the reader have been placed in the Appendices.

Chapter 2

FUNDAMENTALS OF ELECTRONIC IMAGE SENSORS

Conventional film photography is one of the most eminent and prevalent technologies with lots of applications. It is a chemical process that transduces light into a physical image through a series of reactions. Electronic imaging provides an alternative to this chemical technology by employing image sensors to transduce light into electrical signals which expands the applications due to the ease bestowed upon the processing, storage and transmission of electronic images.

The basic operation of an electronic image sensor can be summed up as the collection of photons, the generation of charges, the collection of these charges, their conversion into an electrical signal, the readout of this signal and finally the processing of what has been read out. In a nutshell: the conversion of optical signals into exploitable electrical signals.

2.1 Photosensing Principles

A sensor typically consists of a two-dimensional array of pixels. Each of these pixels contains a photosensing element. The portion of the pixel sensitive to light is measured by a percentage called the Fill-Factor (FF). A good start for understanding electronic imaging, is acquiring basic insight into the behavior of charge carriers in semiconductors. An idiosyncrasy of semiconductors is that both electrons and holes act as mobile charges as opposed to only electrons in conductors. Light photons may be absorbed and hence make their way through the semiconductor. The absorbed energy induces the shift of electrons creating holes [4]. Each photon reaching the photosensitive element may generate one or no electron in the silicon, which in turn may or may not be collected by the pixel [5]. The efficiency of the conversion of received photons to free electron-hole pairs (EHPs) (that give rise to a photocurrent)

is denoted by the Quantum Efficiency (QE) of the detector [6].

$$QE = \frac{Number\ of\ free\ EHPs\ generated\ and\ collected}{Number\ of\ incident\ photons} \tag{2.1}$$

This puts in perspective one of the main evaluation criteria of photodetectors: light sensitivity (which is also wavelength-dependent). The absorption coefficient of the photosensing element is an indicator of its sensitivity [4]. The photon absorption process for photogeneration, i.e. the creation of EHPs, necessitates a photon energy superior to the bandgap energy E_g of the semiconductor material to supply enough energy for an electron to leave its valence band [6]. The bandgap energy, which is a property of the material, is also inversely proportional to the wavelength of the incident light. Hence, for greater wavelengths, the bandgap energy is lower, and the sensitivity higher since more photons can be detected [4]. This sets an upper cut-off wavelength (or threshold wavelength) λ_g for absorption [6].

$$\lambda_g = \frac{1.24}{E_g} \tag{2.2}$$

For silicon, $E_g = 1.12eV$ which yields a threshold wavelength of $\lambda_g = 1.1\mu m$. This means that silicon photodetectors can be used for light in the visible spectrum, i.e. around 380nm to 750nm. As for sensitivity to the infrared spectrum, Miller [7] devised a scheme for dividing the band based on the response of various detectors:

- ⋆ Near Infrared (NIR) [0.7μm - 1.0μm]
- ⋆ Short-Wave Infrared (SWIR)[1.0μm - 3μm]
- ⋆ Mid-Wave Infrared (MWIR) [3μm - 5μm]
- ⋆ Long-Wave Infrared (LWIR) [8μm - 12μm]
- ⋆ Very-Long Wave Infrared (VLWIR) [12μm - 30μm]

This means that NIR light can be detected by silicon (which is usually the part of the band used for imaging), and it "filters" out as well interference from other infrared light; for e.g. optical communication which typically uses wavelengths between 1.3μm and 1.5μm [7]. This makes it very suitable for our application where we would like to project and capture patterns of infrared light invisible to the human eye, yet without interfering with existing radiation.

Another important factor in photodetectors is the responsivity. It is defined as the ratio of the generated photocurrent density to the optical power per unit area

of the light; i.e. the electric output to the optical input [4]. So basically, greater photocurrents for lesser optical power beget enhanced responsivity. Responsivity at a given wavelength is given by [6]

$$R = \frac{Photocurrent(A)}{Incident\ Optical\ Power(W)} = \frac{I_{ph}}{P_o} \tag{2.3}$$

For larger pixels, the FF is larger as well. This increases the number of photons that can be collected; however, this decreases the number of pixels in a given area, hence the number of devices on a wafer, which in turns boosts the production cost. Therefore, an important compromise in pixel design is pixel pitch versus FF to achieve a good photoresponse.

Several types of silicon-based photosensing elements exist, the most prominent of which are photoconductors, phototransistors (PTs), photogates (PGs), Thin-Film on ASIC (TFA) and photodiodes (PDs).

2.1.1 Photoconductors

They are the most basic type of photodetectors consisting of a semiconductor with ohmic contacts. Absorbed photons generate electrons and holes increasing the conductivity of the material, hence increasing the current flowing for a constant applied voltage bias. The gain is defined as the change in current with respect to the primary photocurrent. Photoconductors are distinguished for their high gain, but this comes at the expense of slow response and high noise [4].

2.1.2 Phototransistors

As a notion, all transistors are sensitive to light and can be used as photosensing elements. In practice, however, the narrow channel of Field Effect Transistors (FETs) drastically limits their responsivity - which is why bipolar transistors are favored over PTs. A large collector-base junction area is required to increase the number of photons collected and hence the sensitivity. Nevertheless, this results in a slower response speed [8]. Since our application requires a high frame rate, response speed is an issue, and bipolar transistors are not as readily available as FETs - noting that a combination of both requires special processing and additional expenses - which swayed the balance towards other photosensing elements.

2.1.3 Photogates

A PG is a MOS capacitor with a top plate formed of polysilicon. Consequently, it transduces optical signals into charges as compared to voltages and currents for the other semiconductor photosensing elements. These charges would then have to be transformed using other components into voltages or currents to become useful. The transfer of charges generates thermal noise due to the conductance of the transfer channel [8]. This makes it less appealing to us.

2.1.4 Photodiodes

The advantage of the PD as compared to other photosensing elements is mainly the ease of fabricating it in the inexpensive and widely available CMOS technology. It basically consists of a PN junction. Light generates electron-hole pairs that move to the N and P regions of this junction. Some of these carriers diffuse into the depletion region and are swept from the junction by the electric field prevailing in that region. The holes then move towards the anode and the electrons head towards the cathode generating a photocurrent or photovoltage that will be used to determine the incident light intensity. A thicker depletion layer increases the number of absorbed photons. To widen the depletion region, a reverse-biased configuration is opted for; however, this decreases the response speed [4]. Nevertheless, the response speed of PDs remains superior to that of the other photosensing elements and they remain the easiest to implement using a standard CMOS process because of their simple topology [9].

2.1.5 Pinned Photodiodes

The pinned photodiode (PPD) is more promising that both the PD and the PG. It provides a solution to the fact that a standard PD cannot be fully depleted upon readout, which creates image lag and FPN. In a PPD, the N-P structure of a regular PD is traded in for a P-N-P one as shown in 2.1. This structure allows the N- region to be fully depleted while there are still holes in the uppermost P region eliminating lag and FPN while preserving responsivity [10]. The voltage is then “pinned” to a fixed value.

PGs and PPDs both offer charge transfer from a large collection area of large capacitance to a small FD capacitance, but the QE of PPDs is far superior and require

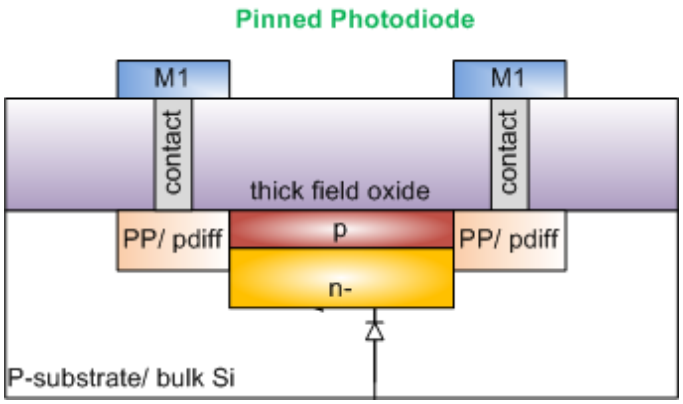


Figure 2.1 Pinned Photodiode

less control signals than PGs aside from the fact that PGs require additional care to reduce leakage currents, which is intrinsic in PPDs. Nevertheless, PPDs require special process adaptation. Furthermore, as is the case for PDs, the PPD does not allow true CDS and the decrease of supply voltages with the newer technologies make it harder to have a pinned voltage while keeping enough head room for integration [11].

2.1.6 Thin Film on ASIC

TFA is basically the placement of the PD on top of the circuitry by a special technique as illustrated in Figure 2.2, with the rear electrode connected to the circuitry underneath, hence creating a 100% FF. The QE varies typically between 60% and 80% depending on the wavelength in question [11]. Another advantage of TFA is that it can be used with any process generation, and that the optical problems introduced by stacking several layers with newer processes are avoided, nevertheless, capacitive coupling becomes an issue [11].

2.2 Color Imaging

We have seen in the Section 2.1 that Silicon PDs are sensitive to a certain range of light wavelengths. This means that they cannot differentiate between different colors. Typically, to circumvent that, a Color Filter Array (CFA) is placed on top of the pixel array. Each pixel would thus become sensitive solely to the wavelength

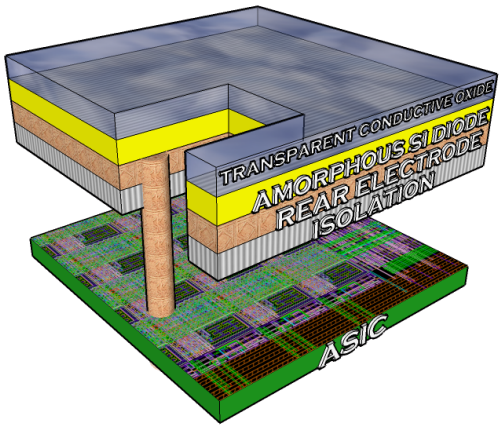


Figure 2.2 Thin Film on ASIC

that can traverse the filter on top of it. An algorithm is then used to recombine the gathered data and to produce a colored image.

Primary or complementary color filters can be used. The former imply the use of red, green and blue (RGB) filters while the latter make use of cyan, magenta and yellow filters (CMY). White filters can also be used in conjunction with color filters to measure the luminance signal [12].

One of the most popular filter configurations is the Bayer filter featured in Figure 2.3. People are more sensitive to high spatial frequencies in luminance (which contains the brightness information of the image) than in chrominance (that contains the color information of the image), and luminance is composed primarily of green light.

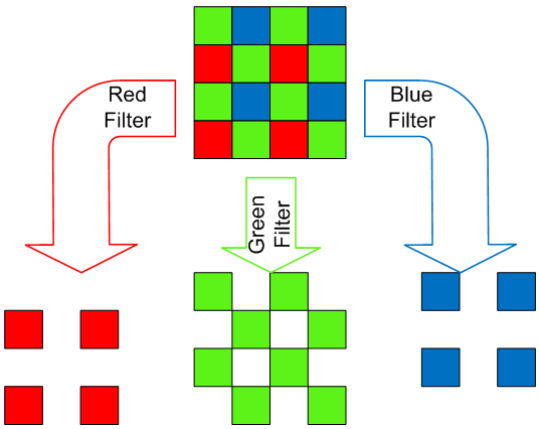
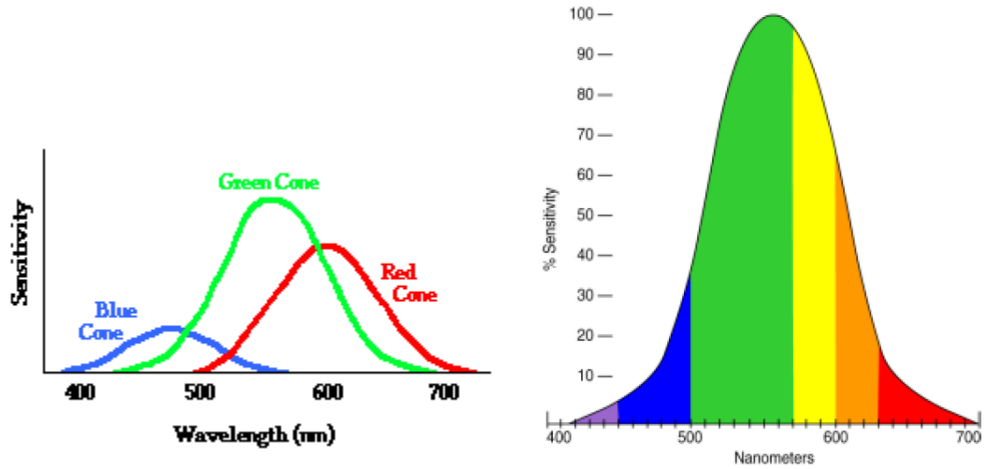


Figure 2.3 Bayer Color Filter Array and Color Patterns

Therefore, the Bayer CFA improves the perceived sharpness of the digital image by allocating more spatial samples to the green image record [13]. Being an RGB filter, this is why it has two green filters for each red/blue pair. This way the filter better depicts the human retina that is more responsive to green as shown in Figure 2.4.



(a) (b)

Figure 2.4 Light responsivity of cones in the human retina: (a)[14], (b)[15]

Concurrently, another popular filter is the complementary mosaic pattern that has equal proportions of magenta, green, yellow, and cyan sensitive photosites arranged in magenta-green and yellow-cyan rows. It provides an improved image SNR (Signal-to-Noise Ratio) at low illumination levels relative to RGB patterns, as the sensor output signal level is much higher. However, the RGB patterns normally provide a better image SNR at higher illumination levels [13].

Patterns are thus built for each color, as shown in Figure 2.3 for the RGB in the Bayer CFA. An interpolation is then applied to find the color values in the intermediate pixels. Many algorithms exist for that which is another very extensive topic that I shall not delve into.

Another interesting method that has more recently been put forth takes advantage of the fact that different wavelengths have different absorption depths in silicon. Longer wavelengths penetrate deeper. As a result, a vertical pixel can be constructed so that the RGB information can be collected at the same location in the 2D image plane but at different depths eliminating the need for filters and interpolation algorithms [16].

2.3 Lenses and Microlenses

The use of a lens to concentrate the light emanating from a scene on the image sensor is necessary to achieve a meaningful image. A typical camera lens system comprises several lenses redirecting the light in such a way as to recreate the image the most accurately possible on the image sensor while minimizing artifacts the likes of loss of contrast, blurring, distortion, etc.

Several parameters have to be taken into consideration in selecting a lens. The focal length determines the angle of view. A smaller focal length implies a wider angle of view and less susceptibility to image deterioration due to the shaking of the camera. Longer focal lengths require shorter exposure times to minimize blurring. Another important parameter of lenses is aperture. The aperture range indicates how much the lens can open up or close down to increase or decrease the amount of light reaching the sensor. Aperture is measured with an f-number (e.g. f/1.4). Lower f-numbers correspond to larger apertures and thus "faster" lenses because the shutter speed can be increased to obtain the same exposure [17].

On a slightly different note, having discussed photosensing and photosensitive elements, it is obvious that it is much coveted to increase the size of the photoreceptive area. One way of doing that without enlarging the pixel size is by employing microlens arrays. Figure 2.5 shows an example of such an array.

The microlens would focus the light on the photosensitive region of the pixel. This

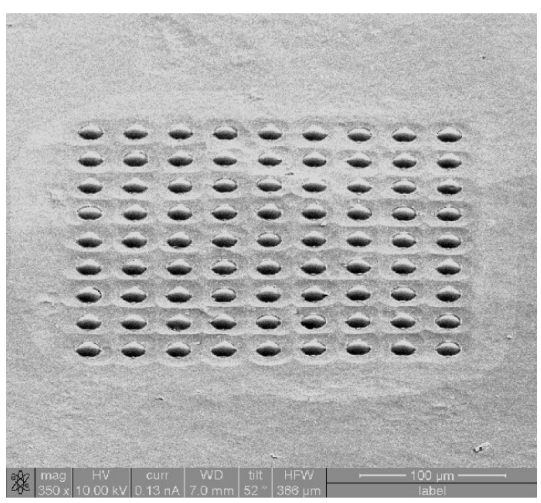


Figure 2.5 Microlens Array [18]

can double or triple the fill-factor for CMOS image sensors raising it from a typical 20 to 30% to a much more desirable 70 to 80% [5]. Several methods can be used to create such arrays, from polymer-thin film [19] to etching glass [20] that is placed on top of the image sensor to even more innovative methods such as a process of surface tension and injection [18].

Figure 2.6 shows a typical cross-section of a pixel with a color filter and microlens. The photodiode occupies a portion of the pixel. The remainder of the pixel is covered by a metal shield to prevent light from interfering with the circuitry underneath it. The color filter is on top of the sensor and a microlens concentrates the incident photons on the photodiode covered by the filter. Nevertheless, I shall not delve any deeper into this topic since it is beyond the scope of this thesis.

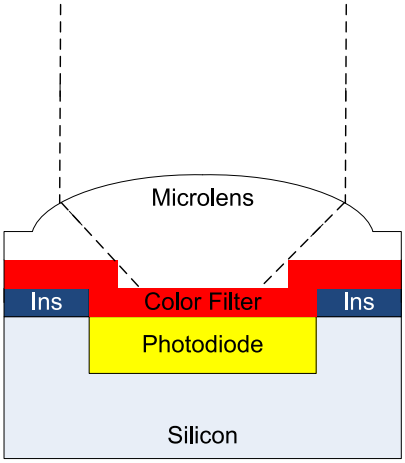


Figure 2.6 Typical cross-section of a pixel with a color filter and microlens

2.4 Electronic Image Sensors

The two basic types of electronic image sensors available nowadays are Charge-Coupled Devices (CCDs) and CMOS (Complementary Mos Oxide Semiconductor) image sensors. CCDs have long been established as a technology for image sensors, however, CMOS image sensors surfaced after that offering several advantages compared to CCDs; namely the possibility of lower power consumption, higher frame rates, use of existing technology processes and incorporating circuitry on the image sensing chip which meant lower costs and greater integration potential. A battle

thus erupted between the proponents of CCDs and CMOS image sensors. A lot of people were drawn to the potential of CMOS sensors by mere curiosity despite their being uncertain of the benefits. This led to a lot of experimentation but also to a distorted market behavior where a lot of greedy startups went bankrupt: a lot of people were investing in CMOS sensors "blindly" [21] and CMOS imagers were at first priced below their cost to win business [22]. The battle cooled off around 2002 and took on a more realistic turn based on cash-flow and not on capital investment in a "new technology" that sparked curiosity. Nevertheless, the sudden interest in CMOS sensors did have some advantages in making it a norm in a lot of applications such as video-conferencing, desktop and barcode scanners, etc [21]. The current market focuses more now on long-term consumer stability than on high-risk startups [22].

2.4.1 CCD Image Sensors

CCDs saw the light of day in 1969 at the Components Division of Bell Labs with Drs. Willard Boyle and George Smith. This was the dawn of digital photography [23]. CCDs are basically arrays of photosites with charge collecting buckets that can transfer their charges to each other [23]. These "buckets" are actually capacitors connected together that can transfer their charge to and receive charges from neighboring capacitors via voltage control. MOS capacitors are typically used in such cases. Each consists of a gate above a silicon oxide layer in a p-type silicon substrate. When a positive voltage is applied to the gate, a depletion region is formed under the silicon oxide layer causing electrons to accumulate. These electrons can then be transferred to neighboring capacitors by changing the gate potentials. This makes charges among the capacitors coupled, hence the origin of the name of this type of sensors.

Since silicon has a bandgap energy of around $E_g = 1.12eV$, and pertaining to the discussion in Section 2.1, the silicon substrate can readily absorb photons if they have sufficient energy and if they hit the silicon, preferably at the depletion region. This generates EHPs and the number of electrons accumulated in the depletion well becomes proportional to the number of absorbed photons. This makes it possible for CCDs to take on the role of image sensors [12].

CCDs shift electrons through stages to an output amplifier. Relatively high voltages are required to be able to pull the electrons between stages. They are usually directed to a single amplifier at the corner of the array and an analog video signal is

outputted. Shifting can nevertheless cause image blurring, which is why light shields should be used [5]. CCD sensors can roughly be classified into three architectures.

The first is the linear array architecture shown in Figure 2.7. The charges from each CCD are transferred to a shift register that then redirects them to an output amplifier. This type of architecture is common in scanners where the possibility of using low-cost high-resolution linear arrays exists [12].

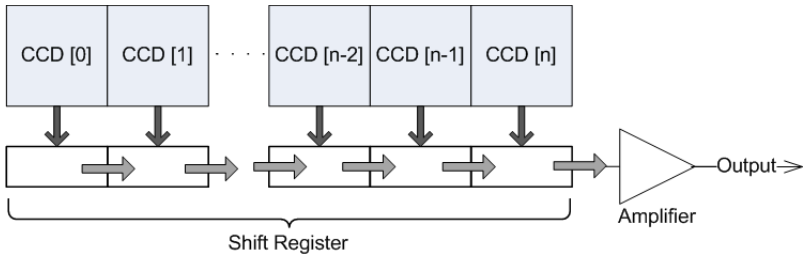


Figure 2.7 Linear Array CCD Architecture

The second architecture is the Frame Transfer (FT) one [5; 12] featured in Figure 2.8. In this case, the entire CCD image is shifted vertically into an identical shielded CCD. This, however, results in a large smear since it takes around a millisecond to transfer the image [5]. FT sensors have high FFs of 100%, but suffer from slow readout rates [12].

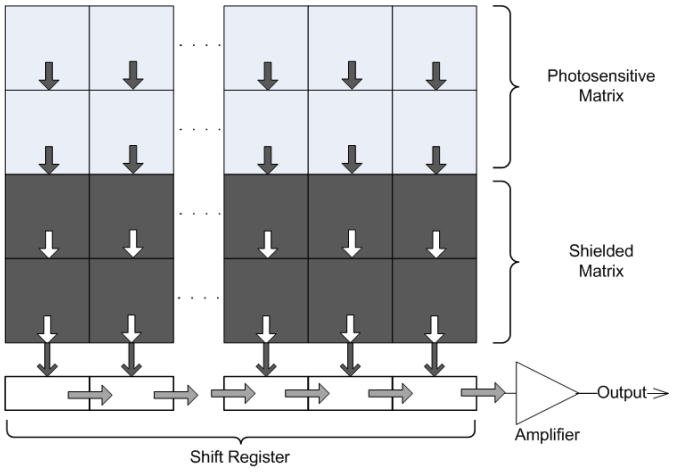


Figure 2.8 Frame Transfer CCD Architecture

The third architecture is the Interline Transfer (ILT)[5; 12] one portrayed in Figure 2.9. In this architecture, each pixel has its own diode and shielded storage and

transfer area. This, nevertheless, results in a decrease in FF, which can be, however, compensated by using microlenses [5] as discussed in Section 2.3. The low FF attributed to this architecture is counterbalanced by a fast readout rate though [12].

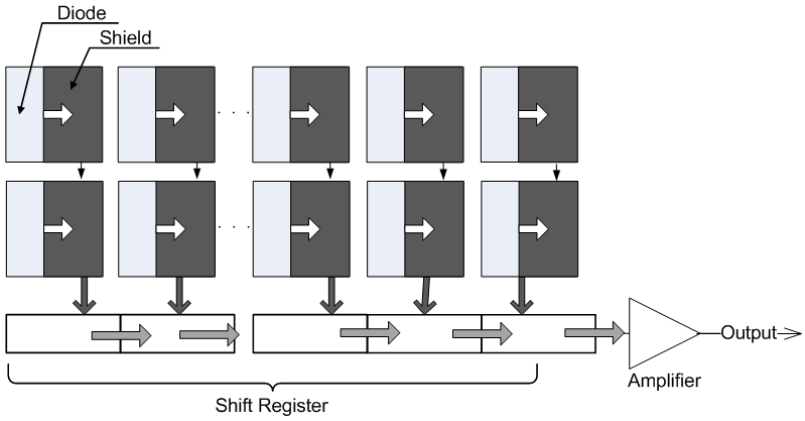


Figure 2.9 Interline Transfer CCD Architecture

Combinations of these architectures also exist. One of these is Frame Interline Transfer (FIT)[5; 12] which reduces smear. Nevertheless, it should be noted that the FT and FIT architectures both entail an increase in die size and hence an inevitable increase in cost [5].

When it comes to refinement, CCDs are well-renowned for their excellent image quality and output uniformity. The CCD process is acclaimed for its high fidelity; nevertheless, this comes at an increase in cost. The high image quality standards also come at an increase in power consumption to be able to decrease noise. This is also partially due to high clocking voltages, typically between 2.5V and 10V, and the need for multiple supply and biasing voltages. Another drawback is the sequential readout which contravenes the attainment of higher frame rates [23] and window-of-interest readout without the risk of charge overflow. Furthermore, no other circuitry (e.g. ADCs or clocks) can be added to the sensor chip since they would contribute to substrate noise. Therefore, a set of chips is needed which makes miniaturization harder [5].

Regardless, CCDs are very well-established. They have been around and have evolved for close to 40 years, so CMOS sensors do have quite a challenge to overcome if they want to replace CCDs - so they better have something astounding to offer to make them stand out.

2.4.2 CMOS Image Sensors

CMOS image sensors have evolved over the last decades. The first CMOS image sensor was the Passive Pixel Sensor (PPS). The pixel consisted of a photodiode and an access transistor [24] as shown in Figure 2.10. As a consequence, it had a very high fill-factor. However, the signal quality was poor and the analog-to-digital voltage conversion time increased with the number of pixels because the architecture had a single external ADC common to all pixels. PPSs were offered by Reticon starting in the late 1960s. Their use in camcorders was tackled by Hitachi and Matsushita in the 1980s [25]. Nonetheless, Peter Denyer was the first to implement a PPS with substantial integrated electronics in 1991 describing it as "extending the CMOS ASIC marketplace in a sector of high growth rates" which is image sensing. This sensor had a matrix of 312 x 287 pixels, with pixel sizes of 19.6μm x 16μm. Each column had a sense amplifier and pixels could be addressed and shifted out via an output amplifier as the last stage [26]. Denyer then went on to establish a company VLSI Vision to commercialize this sensor in 1990. His company was acquired by STMicroelectronics in early 1999, becoming their Imaging Division, and continues to produce CMOS image sensors [27]. For these sensors, wire capacitance is an issue. This makes them less scalable and less enviable in high rate applications for as capacitance increases and speed increases, noise increases as well [25], making their advantages of high fill-factor and small pixel size take a backseat.

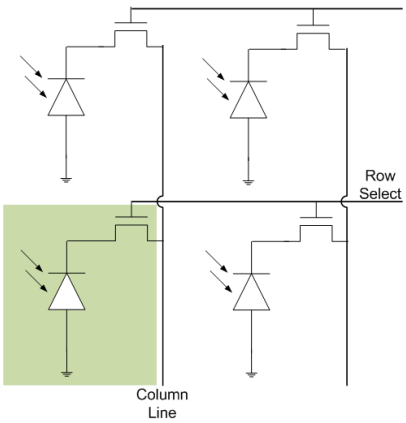


Figure 2.10 PPS Architecture

An improvement over the PPS was the Active Pixel Sensor (APS). The original APS was developed by Noble in 1968 [28]. For the APS, a follower was added inside

each pixel, as delineated in Figure 2.11(a) thus improving the signal quality - rivaling CCD quality. However, no improvement was brought upon the conversion time [29]. So basically, each pixel has its own amplifier to create a charge gain between the photodetector and the analog signal at the bottom of each column. The in-pixel amplifier is typically a source follower due to its simple configuration and uniform gain. This makes the sensor less susceptible to noise at an expense of a decrease in fill-factor. The first real advocates for it were researchers from the National Aeronautics and Space Agency's (NASA's) Jet Propulsion Lab (JPL), namely E.R. Fossum [25]. The initial goal of JPL while developing their APS CMOS image sensor was to get an image sensor that consumes less power and that is less susceptible to radiation damage in space [23]. They founded Photobit Corp. that commercialized the first APS-based systems [25]. It was purchased by Micron in 2002 that combined Photobit's imaging design technology with its own DRAM process [30].

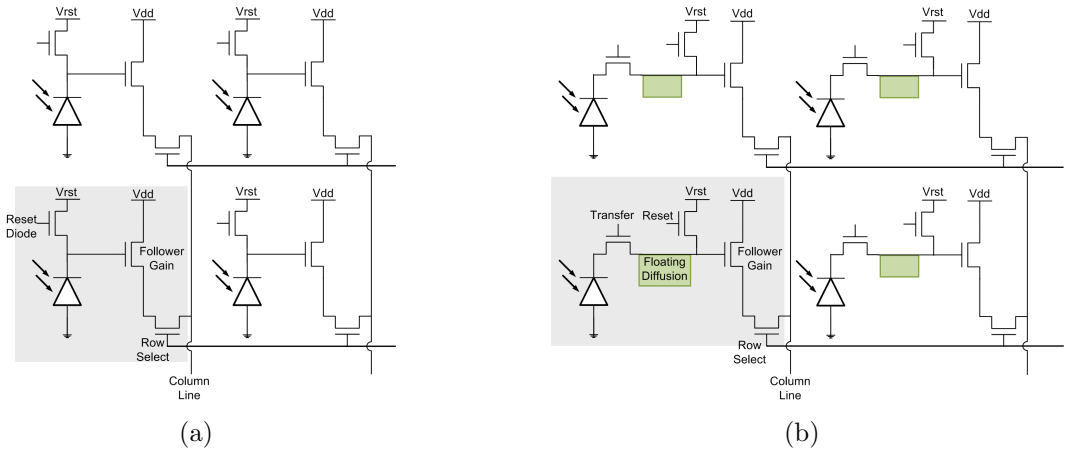


Figure 2.11 APS Architectures: (a) 3-Transistor, (b) 4-Transistor

APSs are very common in today's research and industry. Several architectures for APSs have been developed over the years. The original configuration was a 3-Transistor one as the one featured in Figure 2.11(a). It basically consists of a photodiode, a reset transistor, a source follower and a row select transistor. The diode is initially reset to a high voltage and is then left to integrate decreasing the voltage across the diode as the photons are absorbed and converted to charges. Disadvantages of this architecture are typically that the sense node where the diode and reset transistor meet incurs an elevated dark current contributing additional noise. Moreover,

the output response is non-linear because the capacitance of the photodiode depends on the voltage affecting the charge-to-voltage conversion as the diode fills up. Furthermore, residual charge on the photodiode can create ghost images in fast-changing light settings [31].

An alternative APS architecture is shown in Figure 2.11(b) where 4-Transistors are used in each pixel. A transfer gate is added to separate the photodiode from the floating diffusion. In this case, a reset implies the activation of both the reset and transfer transistors applying a high voltage to both the diode and the floating diffusion. Next, the transfer gate is disconnected and the diode is left to integrate. Prior to measurement, the reset transistor is activated again to reset the floating diffusion only this time. Afterwards, the transfer gate is activated to transfer the charge from the diode to the floating diffusion. This design permits true Correlated Double Sampling (CDS) (see Section 2.4.4) since the same reset level is used to measure the reset value and the signal value [31]. Several other APS architectures have appeared in the literature that have common-element or shared configurations. Figure 2.12(a) shows a 1.75T architecture. It is basically a readaptation of a 4T architecture where four pixels share the same floating diffusion, reset gate, source follower and row-select transistor. Nevertheless, each pixel still has its own transfer gate that should be activated one at a time to read out the values at the photodiodes.

An even greedier architecture is the 1.5T architecture shown in Figure 2.12(b). It is similar to the 1.75T architecture but eliminates an extra transistor: the row-select

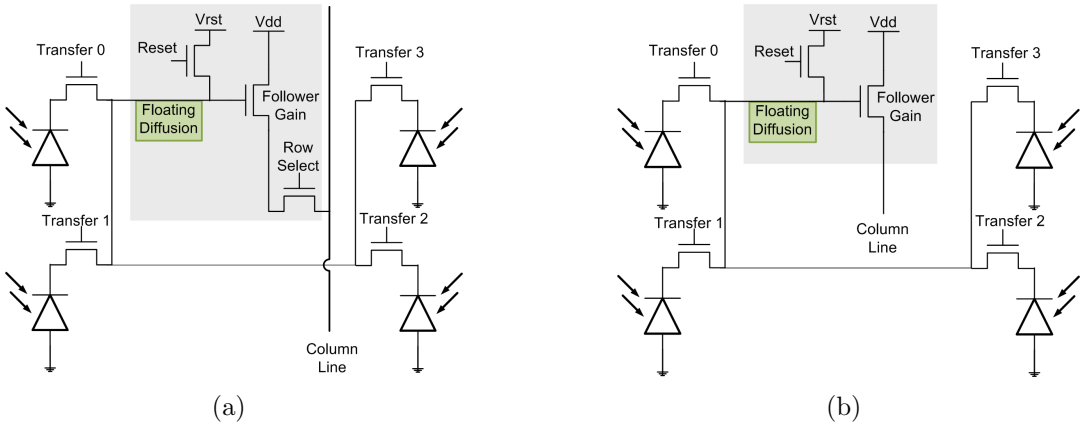


Figure 2.12 Common-Element APS Architectures: (a) 1.75-Transistor, (b) 1.5-Transistor

one. By doing this, however, the readout strategy is modified. We no longer read out row by row.

Instead, the reset voltage and Vdd of the pixel are sent as pulses to be able to turn the follower transistor on and off to give or deny access to the column bus. The readout strategy also involves reading out blocks of pixels and separating even columns from odd ones to be able to multiplex the values on the signal buses. Details can be found in [32]. A 1.25T pixel is also achievable by having two blocks of four pixels arranged in parallel that share a readout and reset transistor [33].

Despite the good performance of APSs, they are still not as sensitive as CCDs: light may land on transistors, the gain is lower and the noise greater [23].

The most recent architecture is the Digital Pixel Sensor (DPS) depicted in Figure 2.13. The first DPS was developed by El-Gamal at Stanford University around 1994 [34]. The DPS integrates an Analog-to-Digital Converter (ADC) within each pixel along with a digital memory. This allows parallel conversions to occur in each pixel making the conversion time independent of the number of pixels (not to be confused with the readout time). This however is done at the expense of a decrease in fill-factor since more circuitry is added to each pixel. The incorporation of an ADC in each pixel allows for massively parallel conversion, very high-speed readout and

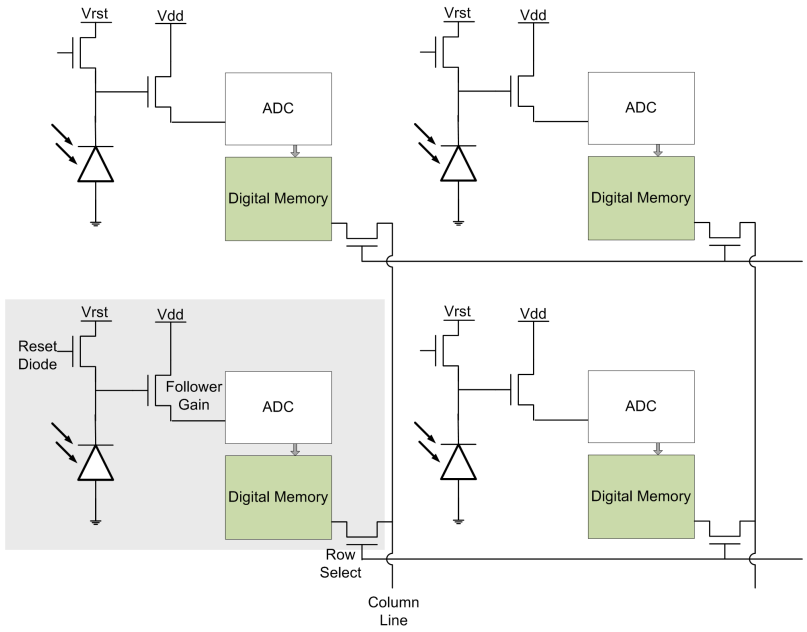


Figure 2.13 DPS Architecture

greater Dynamic Range (DR) [29]. DPSs are particularly interesting since they have more potential for higher frame rates and since with the new design technologies, the dimensions of transistors are becoming smaller and smaller lessening the impact on the fill-factor and making it less overwhelming.

To wrap up this section on a slightly different note, an interesting approach has lately been introduced into the image sensor world due to the advent of 3D-ICs (Three Dimensional Integrated Circuits). These should not be confused with 3D packages that consist of different chips with different functions stacked inside a single package and connected together [35]. A 3D-IC is a stack of multiple dies with direct connections tunneling through them. This reduces the interconnect length due to the key advantage of allowing wires to be routed directly between and through the wafers [36]. It is basically integrating planar device layers with short vertical interconnections. 3D interconnect boasts the advantages of decreased cost, improved performance and ameliorated integration [37]. The main drawback, however, is that area enough for thousands of transistors is sacrificed. Nevertheless, this waste in area can be somehow compensated by smart placement and routing strategies to use these vacant areas for through-hole wiring [36]. Image sensors that use this technology usually place the different modules of the sensor on different layers or "tiers" with the uppermost tier having the photosensing element with minimal circuitry to improve the fill-factor making it very close to 100%. Figure 2.14 shows a generalized example of a DPS pixel with the first tier containing the photosensing circuit, the second the ADC and the third the digital memory. The layers are connected together with vias. This reduces the overall area of the sensor and minimizes parasitics as well by shortening traces. Several 3D-IC image sensor architectures have been brought forth the likes of [38] and [39].

2.4.3 CCD vs. CMOS Image Sensors

The companies that manufacture image sensors can be divided into four groups each favoring a specific technology being CCD or CMOS. Japanese electronic firms - such as Sony, Matsushita and Sharp - tend to have an inclination towards CCDs, while semiconductor suppliers and foundries - like Agilent, TSMC, UMC and ST - along with fabless suppliers - namely Omnivision - are advocates of CMOS sensors. Established companies in the image sensing field - the likes of Kodak, Canon, Dalsa and

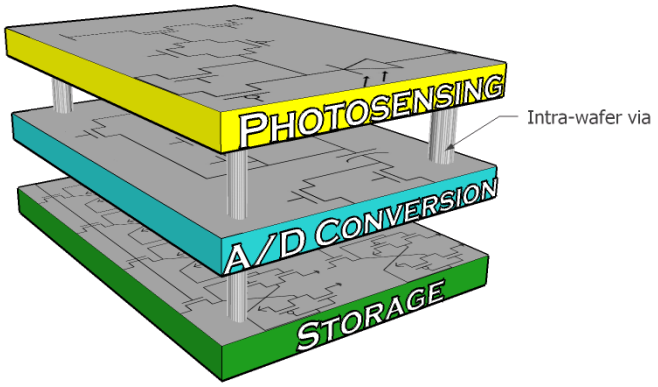


Figure 2.14 General example of a 3D-IC DPS pixel

Fujifilm - tend to have both [40]. So this is enough to see that both image sensing technologies are widely spread and extensively commercialized. The overpromotion of both CCD and CMOS sensors and the relentless battle between them have engendered a lot of fear, doubt and uncertainty in the domain of image sensors. As Dalsa puts it, it is much like comparing apples to oranges: both can be good for you [22]. So essentially, depending on ones needs, s/he would sway towards one or the other.

The concepts of both CCD and CMOS image sensors have been around since the late 1960s, early 1970s. Nevertheless, CMOS image sensors took a longer time to emerge since the CMOS technology was not mature enough at that time to allow CMOS sensors to compete with CCD ones. Feature sizes were not small enough and process uniformity was left to be desired. That was true until the 1990s when CMOS technology flourished and there was revived interest in CMOS image sensors: they were proponents of integration, miniaturization, portability, low-power consumption, low defect and contamination levels and low fabrication cost since they used already-existing processes with new circuit techniques adapted from CCDs to achieve low noise and high DR. However, some unexpected surprises were waiting around the corner: design time was greater, quality was inferior and even the cost was higher since process adaptations turned out to be necessary to achieve certain image quality standards [22; 5]. The following discussion compares some of the issues faced by the two imager types.

An important factor when dealing with CCDs is Antiblooming. In general, blooming occurs when the full-well capacity of the pixel is exceeded, causing charges to overflow into adjacent pixels. This is usually addressed by biasing the region around

the cells during integration [41] or adding an overflow CCD to contain the superfluous charges that would then be transferred to an output and eliminated [42]. This problem is not intrinsic to CMOS imagers - what one might mistake for "blooming" in CMOS sensors is usually caused by Image Lag or Sticking. Image lag/sticking/ghosting occurs when there is an improper reset or improper/incomplete charge transfer. A residue of the previous image would appear in the current frame, and perhaps additional subsequent frames creating a "ghost". This can be observed in both CMOS and CCD imagers. Another important similar phenomenon is Image Smear. In general, image smear occurs when charges are shifted (CCDs) or with rolling shutters if the image scene is non-stationary (CMOS).

Resolution is one of the first parameters that one inquires about when buying a sensor. Increasing the resolution was one of the greatest initial goals in image sensor design. Nevertheless, such sensors had to overcome certain obstacles to become practical. Basically, the resolution increase if not matched by a photosensitive area increase, impairs the sensitivity of the sensor [43]. CMOS pixels usually have a smaller fill-factor (percentage of the pixel sensitive to light) which can be 20% or less because they have circuits integrated in them [44] while it is close to 100% for CCDs [22]. However, putting sensitivity on the side, CCD and CMOS imagers have an identical response to light collection of photogenerated electrons [5], which makes the most notable differences between them the charge-conversion and readout techniques. In CCDs, charge is transferred from pixels to a common element to convert them to voltages and send them off the chip serially [45] as a single output analog signal [22]. For CMOS sensors, the charge to voltage conversion is done within each pixel and the voltages are transferred out of the pixels instead [45] to be read out like in a RAM (Random Access Memory) with column and row addressing circuits.

One of the essential contributors to image quality is dynamic range (DR) which is defined as the ratio of the saturation level of the pixel to the signal threshold [45]. In simpler terms, it is the ability of the sensor to differentiate between very low and very high light intensities in the same image thus preserving the details in both the dark and bright areas of the image [46]. Here, CCDs are better due to their lower noise because of their quieter substrates [45]. However, CMOS imagers offer better SNR and DR at higher rates [23]. They allow high-speed readout and hence higher resolutions [29]. This strength comes mainly from their parallel output structure [22] and the integration of all the functions on the same chip making them popular in

high-speed machine-vision applications [23]. Such applications often require tracking a single object in motion, which makes windowing extremely useful - an area where CMOS sensors have an edge because of their ability of random addressing. CCD capabilities are limited as to that [45] without risking charge overflow. Nonetheless, it is also essential in high-speed imagers to capture images quickly. This depends on shuttering: the ability to start and stop exposure arbitrarily. CCDs lead the game here since they need a smaller fill-factor compromise to achieve that. CMOS sensors, on the other hand, can have two main types of shutters: uniform synchronous shutters that decrease the fill-factor but introduce no motion distortion, and rolling shutters that are non-uniform and that expose different lines at a time bettering the fill-factor by reducing the number of transistors per pixel but inducing image distortion at high speeds - but are still quite suitable for regular consumer applications [45]. So basically, for high-speed CMOS imagers, uniform shutters are essential but come at the compromise of a decrease in fill-factor.

CMOS sensors were initially thought to be able to be implemented using standard CMOS processes, which turned out to be fallacious. Process adaptation was required to achieve a quality comparable to that of CCDs which entailed higher development costs and design complexity than CCDs [22]. This massively affects uniformity - the ability of getting the same response under the same illumination [45]. Nevertheless, it remains that CCD wafer sizes are smaller which increases the fabrication cost [22]. Also, CCDs are at the base capacitors, which makes them susceptible to charge overflow when overexposure occurs requiring special engineering for antiblooming (draining) which is not an issue with CMOS imagers [45]. But despite that, it remains that the development time for CCDs is shorter especially since they are more general-purpose than CMOS image sensors. CMOS imagers are basically systems on chip necessitating development times of around 18 months as compared to 8 months for CCDs. Changes in CMOS imagers require new wafer runs, while for CCDs new PCBs can do the trick [45]. In this same point lies one of the key advantages of CMOS imagers which is that they require less off-chip circuitry. Yet, it should be noted that even though CMOS imagers require fewer components, companion chips are usually necessary to improve on image quality [22]. This makes them popular in low-power and portable applications [23] also because of the ease of placing low-power high-gain amplifiers which increase responsivity. Amplification in CCDs, on the other hand, induces a power penalty [45]. As do clocking and biasing since CCDs

need several higher voltage biases and high-voltage clocks to maintain a certain image quality and to reduce noise [23] in comparison to CMOS sensors that require one bias voltage and a single low-voltage clock level. Other levels can be generated on-chip [45]. With time, however, both CCD and CMOS imagers have worked on their deficiencies. CCDs have been able to lower their power consumption, clock levels [45] and pixel sizes, and CMOS imagers have been able to boost their image quality. Crossovers between the two types of sensors have been conducted by established players with years of experience in both technologies [22] - so at the end of the day, they are still both good for you, depending on your application. Table 2.1 shows a comparison summary between the two types of image sensors.

Table 2.1 Comparison between CCD and CMOS imagers

	CMOS	CCD		CMOS	CCD
Antiblooming	Intrinsic	Varies	Size	Smaller	Bigger
Image Smear	Varies	Varies	Sensor Output	Bits	Voltage
Development Cost	High	Low	System Output	Bits	Bits
DR	Medium	High	Shuttering	Poor	Excellent
Fill-factor	Low	High	Windowing	Excellent	Limited
Flexibility (*)	Lower	Higher	Power-consumption	Lower	Higher
Noise	Higher	Lower	Speed	Higher	Lower
Pixel Output	Voltage	Charge	Turnaround time	Longer	Shorter
Responsivity (**)	Higher	Lower	Uniformity	Lower	Higher
Sensor Complexity	High	Low	System Complexity	Low	High
Sensitivity	Same	Same	Biasing / Clocking	Single, low-volt	Multiple, high-volt
Image Lag	Varies	Varies			

(*) PCB modifications are usually enough to change the application of CCDs.
(**) Same sensitivity for both, but easier to add amplifiers to CMOS sensors.

2.4.4 Noise in CMOS Image Sensors

Any good discussion in microelectronics cannot condone one of its greatest enemies: noise. Noise in image sensors is basically classified temporally and spatially resulting in two main types of noise: random noise that differs between frame and frame and pattern noise that is almost the same for all frames. Pattern noise, shown in Figure

2.15(b), usually has a more drastic effect on the quality of the image as compared to random noise, shown in Figure 2.15(c). Fortunately, the advantage is that it completely correctable, which is not the case for random noise [47]. The diagram in Figure 2.16 has been added to clarify the following discussion.

The pixel is usually the dominant random-noise source in an image sensor - noise that can occur anywhere and anytime. CMOS imagers have a greater propinquity for this type of noise because of the transistors inside the pixels. Random noise has to be minimized by taking design considerations [46]. It can also be reduced by averaging successive frames and can be described by statistic distributions [47]. It encompasses pixel noise (reset noise, flicker noise and shot noise), amplifier noise (column amplifier noise and Programmable Gain Amplifier noise), and ADC noise.

In a pixel the level of the signal is measured relative to its reset level. The error emanating results in reset or kT/C noise [50] which is actually thermal noise in presence of a filtering capacitor [51]. It is due to the reset of the photodiode or the diffusion through a MOSFET. This is equivalent to a capacitor being charged through the resistance of the MOSFET channel. The RMS noise voltage is given by [47]:

$$\langle V_{reset} \rangle = \sqrt{\frac{kT}{C}} \tag{2.4}$$

where k is Boltzmann's constant, T the absolute temperature and C the capacitance of the sense node. Image sensor designers prefer to refer to this noise as kTC noise since they tend to count charges instead of volts, and $Q^2 = kTC$ [51]. This type of noise is proportional to $\frac{W}{L}^{-1}$. But too small a W would result in a decrease in gain, and opting for too large a W would result in an increase in capacitance; so a compromise is mandatory. It is also advantageous to decrease L to have a smaller noise equivalent bandwidth [47]. Several reset schemes have been elaborated to overcome this problem including Correlated Double Sampling (CDS) [50]. CDS consists of taking two samples of the pixel: the first during reset and the second to get the real signal value. The two samples are then used as differential signals in further stages (such as amplifiers and ADCs) [52].

The second type of pixel noise is flicker noise, or 1/f noise, which is caused by fluctuations that can occur at any junction including metal/metal, metal/semiconductor and semiconductor/semiconductor junctions. At low frequencies, it can be a dominant component, however, at higher frequencies it is overshadowed by thermal noise

(a) (b) (c)

Figure 2.15 Image Noise: (a) Original, (b) Random noise [48], (c) Pattern noise [49]

which is white noise with constant power over all frequencies [47]. The output noise voltage per unit bandwidth is given by:

$$\overline{V_{flicker}^2} = \frac{K}{C_{ox}WL}\frac{1}{f} \tag{2.5}$$

where K is a process dependent constant around $10^{-25}V^2F$ and C_{ox} is the oxide capacitance [53]. We may notice that decreasing the area $W \times L$ of a transistor would decrease the flicker noise. However, the $\frac{W}{L}$ ratio has to remain big enough to drive the column capacitance for pixel readout [47].

The third and final type of pixel noise is shot noise which in turn incorporates photon shot noise and current shot noise. To understand the former type, the detection of photons is a random process obeying a Poisson distribution [50]. Assuming that the mean number of photons detected is N, Poisson noise is given by the fluctuations about this mean value. The standard deviation is a better representation of the noise level because the mean of many noise sources is usually zero [47]. The RMS noise voltage is given by:

$$\langle V_{photon}^2 \rangle = \frac{I_{photo}\Delta t_{reset}}{C_{pdiode}^2}q \tag{2.6}$$

where I_{photo} is the photocurrent, Δt_{reset} the reset time, C_{pdiode} the capacitance of the photodiode and q the unit charge [4]. As for current shot noise, it is associated with

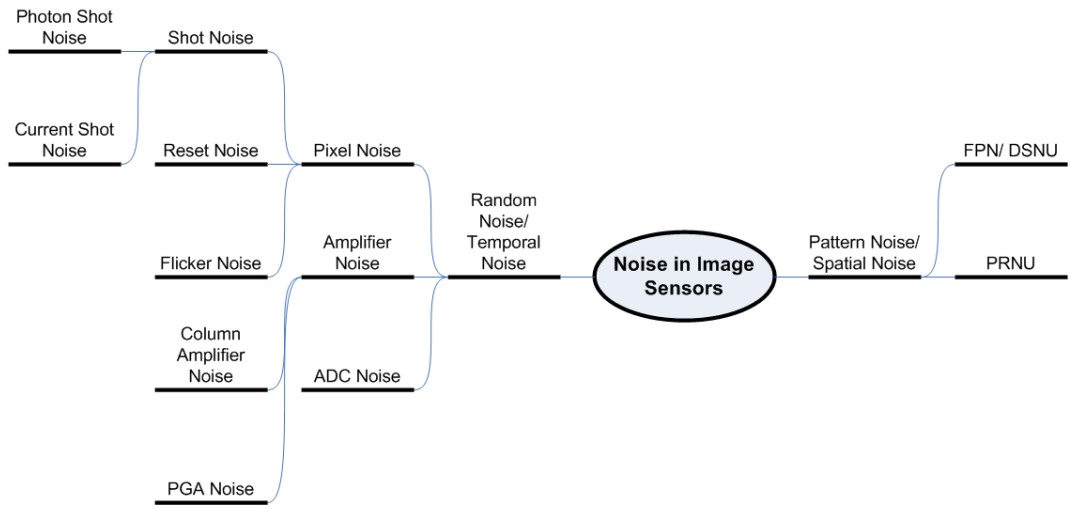


Figure 2.16 Types of Noise in Image Sensors

the leakage current (dark current) of the photodiode [47]. Its RMS value is given by:

$$\langle V_{current}^2 \rangle = \frac{I_{dark} \Delta t_{reset}}{C_{pdiode}^2} q \tag{2.7}$$

where I_{dark} is the dark/leakage current, Δt_{reset} the reset time, C_{pdiode} the capacitance of the photodiode and q the unit charge [4]. Photon shot noise limits the SNR and DR for large signals. The only way to improve it is to increase the well-capacity of the sensor. Leakage current is largely dependent on the CMOS process used [50].

As for amplifier noise, the first type is column amplifier noise. The column amplifier samples both the pixel reset and signal levels and then amplifies the difference signal. The second type of amplifier noise is Programmable Gain Amplifier (PGA) Noise. The sampling $\frac{kT}{C}$ component of these noises is dominant compared to their thermal and flicker components and is given by:

$$V_{amplifier} = \sqrt{\frac{2kT}{C}} \tag{2.8}$$

where C is either the column sampling capacitance or the PGA capacitance respectively, k is Boltzmann's constant and T the absolute temperature [50].

The final type of random noise is ADC noise. Its main component is quantization noise and is ideally given by:

$$\langle V_{ADC} \rangle = \frac{LSB}{\sqrt{12}} \tag{2.9}$$

In practice, ADC noise would exceed this figure due to other noise sources and mismatch in ADC components might also contribute to pattern noise - which leads us to our second noise classification.

Pattern noise is usually divided into two components. The first is Dark Signal Non-Uniformity (DSNU) which means that under no illumination, the pixels would have different "zero-illumination" levels. The second is Photo-Response Non-Uniformity (PRNU), meaning that the different pixels would react differently under the same illumination. The former can be corrected by subtracting a dark frame from the captured image, and the latter can be corrected by the addition of a digital gain for every pixel [46]. PRNU, however, is often neglected and focus is kept on DSNU which is what is usually referred to when talking about Fixed Pattern Noise (FPN) [47].

It is very important to note as well that image processing circuits outside the image sensor apply lots of algorithms and filtering to further improve image quality [54], so the aim behind designing an image sensor is to minimize the noise but keeping in mind that the final image would pass through image processing before being delivered.

2.4.5 Technology and Process Modification

Many particularities inherent to more recent CMOS technologies give them an edge. These include, but are not limited to, reduced feature size (hence reduced area) and the novelty of these technologies in image sensor research (particularly academic). Pixel pitch is one of the parameters that can vary immensely with the technology. Nevertheless, one has to be aware of the fact that minimal dimensions are not solely dictated by the most recent CMOS technology; optical limitations have to be taken into account as well. Dierickx et al. had estimated this size to range between 3μm and 5μm [44]. Such smaller pixel sizes almost necessarily require the use of microlenses to increase the effective FF and, consequently, the sensitivity of the sensor.

The reduced feature size of newer technologies is also accompanied by a greater number of metal layers; a characteristic that offers the possibility of a greater capacitance density [55] - which could be an advantage if proper design considerations are used, yet putting forth setbacks or hindrances some cases. Less recent CMOS

technologies, such as 0.5μm to 1μm, can achieve acceptable image sensor performance without requiring process modification. Scaling the technology beyond that, however, usually increases the necessity for process modification to achieve adequate results. Image sensors using technologies inferior to 0.35μm are faced with performance degradation due to, amongst others, shallower junctions, thinner gate oxide and greater junction and transistor leakage. As a consequence, the photosensitive elements of the pixel require a separate implantation process to increase Quantum Efficiency (QE) (with goes hand in hand with charge collection and responsivity), to improve conversion gain and also to decrease noise. Guidash et al. state that in such cases PPDs are preferred over other photosensitive elements, because PGs suffer from reduced photoresponse, particularly for shorter wavelengths. Also, PDs are not optimized for a broader spectral response and their junction dark current has a negative impact on noise performance [56]. A deep PD junction, nevertheless, can improve charge collection and hence the effective FF. This, however, increases dark current, which has the consequence of increasing noise. Another scaling issue is that thin gate oxide may contribute to leakage and degrade image signals. Low-Voltage-Threshold or depletion transistors, that require an extra mask, can be used to improve that [57]. But, in general, PPDs present lower leakage and offer better blue response for color imagers [56].

2.5 Conclusion

We have seen in this section the fundamentals of photosensing, color filters, lenses and microlenses, basic architectures of CCD as well as CMOS image sensors, discussed the drawbacks and advantages of the different approaches and given the lowdown on some key concepts required for the design and implementation of image sensors.

The following section will make use of all these concepts and ideas to explain who is doing what in image sensing research and what improvements or innovative ideas have been brought forth to attain these state-of-the-art image sensors delving into the most recent achievements and highlighting the main breakthroughs.

Chapter 3

STATE-OF-THE-ART CMOS IMAGE SENSORS

It goes without saying that adopting the "ostrich approach" is not condonable in research. One has to be tuned in with past and current trends to circumvent redundancy and curtail errors. After all, one has to

> Learn from the mistakes of others. You cannot live long enough to make them all yourself.
>
> *Eleanor Roosevelt*
> *US diplomat and reformer (1884 - 1962)*

CMOS image sensors are now the undisputed technology of choice for most consumer imaging applications encompassing, but not limited to, digital still cameras and camcorders. This is mainly due to the fact that they offer a performance rivaling that of CCDs at lower cost, size and power. This pushes towards the reduction of pixel size through avant-gardist designs tapering die size. For this, most CMOS image sensors found in the literature are APSs: they offer better image quality than PPSs and have fewer transistors than DPSs allowing for smaller pixel sizes with higher FFs. The standard 3T structure as well as the 4T structures are still used, but researchers aiming at decreasing pixel pitches have been heading towards common-element structures ending up with 1.75T or 1.5T (and in some cases 1.25T) pixel structures. APS structures, however, have a limited frame rate because the analog-to-digital conversions are external to the pixel. So as the resolution increases, the conversion time increases and the frame rate decreases. Most APS sensors featured in the literature offer a frame rate varying between 15 and 30 fps - which is not suitable for high speed applications but is very adequate for consumer applications. Performance parameters and state-of-the-art CMOS imagers, the imagers of interest in this Master's thesis, will be discussed in this chapter.

3.1 Sensitivity and Downscaling

CMOS imagers are competing with CCD ones because of their system-on-a-chip capability. This goes hand in hand with reduced die size. Evidently, for an image sensor to have a smaller size, smaller pixels are inevitable. And for CMOS image sensors to be able to reach pixel sizes as small as those of CCDs that have nearly 100 % FFs without a dramatic decrease in performance, downscaled CMOS processes with smaller minimal feature sizes are a must [11]. This does however have its toll on sensitivity.

Several detector structures have been designed throughout the years with sensitivity improvement in mind. These include the PG, the PPD and TFA (Refer back to Section 2.1). However, the performance of PGs was left to be desired, making the PPD and TFA more appealling [11].

Regular diodes, such as drain-substrate or well-substrate ones, from standard CMOS processes can be used as PDs. To reduce the pixel interference, some CMOS sensors with bulk PDs make use of vertical overflow drains like CCDs. This also increases the photosensitive area of the pixel [58] with the disadvantage of decreased responsivity for the red and IR frequencies [59; 60]. However, the QE of PDs is not very attractive. This is in part due to the fact that the large load capacitance of PDs decreases the pixel gain and increases the reset noise. This drove some designers to reduce the size of PDs, but introduce an integration capacitor within the pixel, hence increasing the gain but degrading the FF [61]. Another limitation of FF is the collection of photons by insensitive junctions. A means of improving the FF could be the use of a bigger PD, however this implies a higher capacitance [62]. Furumiya et al. developed a deep P-Well PD covered with an antireflective Si_3N_4 film. The photodiode structure improved sensitivity by 110% and the film by 24% for 550nm light [63]. Another interesting method to increase the FF to what they labeled "nearly 100%" was brought forth by Dierickx et al. who basically indirectly increased the FF by increasing the photosensitive volume (not incident area) of the pixel, by adding a barrier between the charge-collection volume and the unrelated transistors; hence the photodiode would collect all the photons incident on the pixel, with the exception of those collected by the circuitry or reflected by the metals [59].

As CMOS technology scales down below $0.35\mu m$, process modification becomes important to counterbalance performance degradation (QE, conversion gain, noise

etc.) to compensate for shallower junctions, thinner gate oxide, and higher leakage. The PPD is one such example [56]. Its use decreases dark current.

Another problem that arises with the decrease in technology size is due to the increase in number of routing layers, which goes with an increase in thickness, inducing absorption, reflection and diffraction problems; making it harder for the light to reach the photosensitive element and requiring better microlenses [11]. A method has been put forth to counter that, which is Shallow-Trench oxide Isolation (STI) that creates optical windows in the substrate. Wong et al. demonstrated in 1998 that for a 36% STI to photosensitive area ratio, an improvement of around 50% in sensitivity was observed for PDs [64]. However, Lule et al. claim that the shrink in capacitance favored by this approach cannot fully compensate for the reduction in sensitive area, keeping PPDs still ahead in the race [11].

Nevertheless, PPD and TFA sensors also face low sensitivity issues due to the reduction of pixel sizes. Lule et al. claim that PPDs can be advantageous over TFA for CMOS $0.18\mu m$ technology for large pixel sizes in the order of $5\mu m \times 5\mu m$, but still maintained that TFA remains better if pixel sizes keep shrinking [11].

Since the addition of amplifiers inside the pixel exerced a limitation on pixel pitch, researchers resorted to amplifier sharing resulting in 1.5T, 1.75T and 2.5T pixels [65; 66; 67; 68] allowing more space for the photosensitive sites.

Nevertheless, a usually more effective means of improving the FF is the use of microlenses. These can enhance the FF up to 90%. However, as the dimensions decrease, the efficiency of microlenses is reduced as well [69]. Dimensions have their toll on sensitivity.

On a slightly different note, wavelength sensitivity is also an issue. This was discussed in Section 2.1. While the usual way of adding color to sensors is placing color filter arrays on top, Sommer et al. went a step further and made use of the TFA technology to create a diode with controllable spectral sensitivity to be able to detect the three primary color signals independently and then read them out of the pixel in parallel [70].

3.2 Frame Rate

When it comes to high-speed imaging, CCD imagers have not made as much progress as CMOS imagers if we take into account the maturity of both. CCDs of resolutions

of 250kPixels have reached a frame rate of 1000 fps [71] after decades of evolution. However, CMOS started out with high frame rates [72; 73; 74] closing to 1000 fps with short integration times adequate for fast object tracking [75]. Moreover, a lot of these sensors operate with low power consumptions like 350mW for 500fps [76].

Parallel acquisition is a key element for high rates. Photobit Corp. has patented an alternative APS pixel to favor parallel acquisition with integrated analog memory that they christened SNAP (Shuttered-Node Active Pixel). All charges are integrated in parallel in pixels, sampled, and stored in per-pixel analog memories. After that, each row is digitized in turn and read out of the sensor [77]. Pipelining is yet another method of allowing parallel sensing. Digital data readout must be performed at the same time as pixel readout and analog-to-digital conversion to minimize crosstalk between digital signal paths and sensitive analog nodes [71].

The shutter type also has its toll. Two main types of shutters typically exist: rolling shutters that are activated row by row and are not suitable for high frame rates that are required for object tracking, since the scene can change, and non-rolling shutters (or global shutters) that are all activated at the same time.

3.3 Dynamic Range

A higher DR usually requires a greater photosensitive area, a longer integration time, and a lower noise floor. Several methods have been put forth to extend the DR of CMOS sensors. These include multiple exposure techniques applied to linear sensors or logarithmic sensors that are however more sensitive to noise.

Logarithmic sensors (the likes of Chamberlain et al.'s [78]) are characterized by increased DR, an output proportional to the signal, and random access in space and time. Nevertheless, they suffer from slow response time for low light and from large FPN degrading the image quality [79; 80; 81; 82]. On the other hand, linear sensors have better FPN but their DR is more restricted [83; 84; 85; 86]. This has led some researchers to combine both into one sensor [87; 88; 89; 90; 2; 1].

An interesting native logarithmic pixel sensor was designed by Bermak et al. in 2000 with a FF of 46% in CMOS $0.7\mu m$ technology. For conventional logarithmic pixels, the size of the follower is a tradeoff between bandwidth and output gain. However, for a native logarithmic follower, Bermak et al. showed that they were able to increase both simultaneously. Moreover, the use of native transistors as transfer

gates lowers the potential barrier for electron transfer due to lower channel doping, which aids in the transfer of photogenerated charges and decreases image lag [91].

3.4 Noise

An increase in kTC noise (Refer back to Section 2.4.4) is inevitable with the downscaling of the integration capacitance with smaller lambda technologies, and CDS, or an alternative, would become a necessity on every sensor. Some chips use both CDS to suppress pixel FPN and Double Delta Sampling (DDS) to suppress column FPN. DDS subtracts voltages from two consecutive reads of each channel [92]. Many alternative techniques have seen the light of day that can be applied to PPDs and TFA sensors as well, such as the one put forth by Pain et al. that uses column-based feedback circuitry [93]. Special resetting techniques to reduce reset noise and image lag have also been elaborated [94; 95; 96]. The noise is also resolution-dependent. The greater the resolution and the readout rate, the higher the noise level. CMOS noise reduction techniques can reduce the readout noise though. If this noise can be made negligible enough, photon-counting could be achieved in CMOS sensors without requiring photon-electron multiplication. This would require a very precise quantizer to count the number of electrons. It could be done digitally with a linear high-resolution ADC [68].

3.5 Digitization and Readout

Several column parallel ADC architectures have been implemented, including single-slope integration ADCs [97], successive approximation ADCs [98] as well as cyclic ones [99; 100]. Despite the single-slope integration architecture's good linearity and simple circuit, it suffers from a lengthy conversion time proportional to a factor of 2^n for an n-bit ADC making it less than desirable for high-speed high-resolution sensors, though not non-existent [101]. Successive approximation ADCs are not always suitable for high-resolution sensors either. The most suitable ADC architecture, according to Kawahito et al., for resolutions exceeding 12 bits are cyclic ADCs [68].

Special readout schemes have also been elaborated to work with the reduced supply voltages of technologies smaller that $0.25\mu m$. Xu et al. came up with a Complementary APS (CAPS) capable of operating at voltages below 1V supply while

maintaining high performance. The CAPS increases the output swing, which is even more important for lower voltage supplies, by adding a complementary signal path. Two complementary output signals are produced by each pixel that are then recombined by the column amplifier [102].

3.6 Recent CMOS Image Sensors

In the late 1990s and early 2000s, more research was invested into APSs. Variable resolution sensors were also implemented [103; 104; 105], self-correcting architectures came to be [106; 107], different techniques were tried out such as pixels on SOI substrate [108] and low-light CMOS sensors were manufactured [61; 109; 110]. However, little research was made on pixel shape optimization [111]. Moreover, new technologies emerged due to downscaling, the likes of TFA [11]. This section will discuss some of the latest CMOS imagers found in the literature, and Table 3.1 will summarize their characteristics for increased readability.

Table 3.1 State-of-the-Art CMOS imagers

Ref	Pitch	FF	fps	Resolution	DR	Architecture	Technology
[112]	2μm	30%	30	1200x1600	-	1.5T APS	0.15μm
[113]	1.75μm	-	15	3264x2448	63dB	1.75T APS	0.13μm
[100]	10μm	54.5%	30	664x488	117dB	3T APS	0.25μm
[114]	20μm	-	3500	512x512	60dB	3T APS	0.25μm
[115]	7.5μm	-	-	-	100dB	4T APS	0.35μm
[116]	7.5μm	-	-	64x64	200dB	4T-APS	0.35μm
[117]	40μm	8.1%	-	128x128	120dB	26T Log	0.35μm
[118]	15x165μm^2	80%	-	2x256	120dB	-	0.35μm
[119]	9.4μm	15%	10,000	352x288	-	37T DPS	0.18μm
[105]	50μm	20%	-	64x32	90dB	>14T-DPS	0.35μm
[120]	32x35μm^2	12.6%	var.	128x128	var.	DPS	0.35μm
[121]	9.4μm	24%	72	640x480	90dB	10T DPS	0.25μm
[122]	14.7x13.8μm^2	13.9%	30	64x64	120dB	47T DPS	0.18μm
[39]	30x150μm^2	-	1000	16x5	138dB	3D 34T DPS	0.18μm
[38]	15x16μm^2	95%	30	97x97	DR	3D APS	0.15μm
[123]	4.95μm	-	30	364x294	71dB	4T APS	0.25μm

In 2007, Cho et al. presented a 8.1Mpixel CMOS image sensor with a pixel pitch of 1.75μm using a 1.75T common-element configuration. Each four diodes share one Floating Diffusion (FD) to maximize the active area FF [113]. Kasano et al. reduced the number of transistors per pixel to 1.5 making the pixels share a readout (detection) and a reset transistor [112]. Such architectures, however, mean that no additional circuitry can be integrated within the pixel, implying that the A/D conversions are external to the pixel, which limits the frame rate.

Some sensors have for main aim achieving a higher DR. Different techniques have been put in place for such a goal. Mase et al. developed an image sensor with a DR of 117 dB by merging multiple exposures using a 12 bit ADC. However, this was done using pixel sizes of 10μm x 10μm [100]. Nevertheless, all this comes with an increase in the required time for image acquisition and thus a decrease in the frame rate. The same sensor was modified by this group to achieve a high frame rate of 3500 fps using a higher pixel pitch of 20μm. But this also resulted in a drop in DR to 60 dB [114]. Sugawa et al. increased the DR by using an overflow capacitor in each pixel to integrate the overflow charges from the diode when it reaches saturation achieving a DR of 100 dB using a single exposure [115] and a hyper DR extension exceeding 200 dB using a multiple exposure technique [116]. A sensor that stirs a bit of interest for our application is the vision sensor inspired by the human retina developed by Lichtsteiner et al. boasting a 120dB DR that responds to light intensity changes in less than 100μs [117]. Posch et al. modified that sensor to create a dual-line temporal contrast vision sensor for high-speed machine vision applications and a DR superior to 120 dB, but a pixel size of 15μm x 165μm with a FF of 80% [118]. Sakakibara et al. took a different approach by adaptively varying the gain by means of a comparator in each column noise cancelling amplifier to prevent pixels from saturating at higher output levels, hence increasing the DR [123].

In an aim to increase frame rate, Kleinfelder et al. deviated from the very popular APS structure to the DPS structure which features in-pixel A/D conversions. This does however induce an increase in pixel pitch and decrease in FF due to the considerable number of transistors per pixel. Nevertheless, a frame rate exceeding 10,000fps was achieved [119].

Bermak et al. published a DPS prototype in early 2006 that offered programmable coding (4 or 8 bits) and spatial resolution using a Pulse-Width Modulation (PWM) technique with a DR of 90dB, but a pixel pitch of 50μm [105]. One of their most recent

prototypes published in 2007 features a variable reference time domain encoding DPS, with an 8-bit in-pixel memory using the same CMOS process. The pixel size was of 32μm x 35μm [120].

Lai et al. published a DPS with clock count output and an amplified logarithmic output response similar to the light response of the human eye with a pixel that can operate at a supply voltage as low as 1.2V without affecting its output characteristics [121].

Shi et al. presented a DPS with exponential multiple sampling and variable reset voltage to enhance the DR with a 64 x 64 pixel array and a simulated power consumption of 2.7mW at video rate [122].

Another new trend in CMOS image sensors is 3D integration. Several 3D-IC image sensor architectures have been put forth. The layers are connected together with vias. This reduces the overall area of the sensor and minimizes parasitics as well by shortening traces. Kavusi et al. brought forth a prototype using a 0.18μm process comprising a 16 x 5 pixel array with a DR of 138 dB and capable of attaining a frame rate of 1000 fps with a pixel power consumption of 25.5μW [39].

Fu et al. have put forth an image sensor using 3D integrated 0.15μm CMOS. The APS featured a matrix of 97 x 97 pixels, with dimensions of 15μm x 16μm with a FF of 95% and an analog output voltage ranging between 0 and 1V [38].

3.7 Conclusion

The physics of silicon is identical for both CCD and CMOS image sensors. Ideally, one should be able to reach the same levels of dark current, QE, and lag performance as long as the CMOS process is optimized. Rhodes et al. claim that CMOS performance can rival that of CCDs down to a pixel pitch of 3.2μm and that dark current on CMOS imagers is improving but still requires a push to match CCDs' 30 years of maturity [124]. Recent CCD research emphasis has been placed on electronic shutters, low power consumption and simplified voltage supply and clocking. When it comes to power consumption, CCD sensors typically consume several Watts [125] while CMOS ones consume in the order of tens of milliwatts of power [126]. CMOS sensors have the advantage of low power consumption, low supply voltage, low cost, compatibility with CMOS technology, being apt for miniaturisation, suitable for random access, windowing, high speed operation and do not suffer from antiblooming nor smearing.

However, they are more prone to noise, hence reducing the sensitivity. They also have a lower fill-factor since the pixel incorporates circuitry. Sensors integrating both CCD and CMOS have been ventured into [127; 128] but have not been deemed fruitful because of the increased cost and the difficulty of driving the large capacitive CCD loads [125; 68]

Chapter 4

CMOS IMAGE SENSOR ARCHITECTURE AND DESIGN CONSIDERATIONS

4.1 Why CMOS?

The initial incentive behind favoring a CMOS image sensor for our application versus a CCD one was the availability of the technology. Nevertheless, several other advantages pertaining to our application exist and tilt the balance yet again towards CMOS. The use of CMOS provides more leeway to adding image processing to our system, either by integrating it inside the image sensor chip creating a System-on-Chip (SoC), or by using 3D-ICs with an image processing layer, or by 3D-packaging a sensor chip with an image processing one or even by simply having several chips on the same Printed Circuit Board (PCB) communicating together - a CMOS chip is an easier load to drive than a CCD one. Another important feature is lower power consumption which is mandatory for portable applications the likes of Cortivision. Moreover, the required image processing to generate a 3D image adequate for stimulating the visual cortex necessitates grabbing several frames to generate a single image, which calls for a frame rate superior to 400 fps. This is easier to achieve using a CMOS imager. This latter requirement also backs up the incentive to opt for a Digital Pixel Sensor (DPS) architecture that allows in-pixel Analog-to-Digital conversions speeding up image acquisition. The extended binning ability is another characteristic of CMOS imagers that can be useful. Therefore, in the case where a decrease in resolution can be afforded, sensitivity can be increased by combining several pixels to form one pixel. This would of course require additional circuitry or external processing for the time being, but could be at a later time integrated either in the analog part or in the digital controller part of the system. A final advantage of CMOS imagers is the

ability of having several taps which can be a plus in multiplexing output data.

4.2 Why a Digital Pixel Sensor?

The high frame rate required by the Cortivision application rendered the choice of a highly-parallelized architecture particularly appealing. This made the DPS (which has pixel-level A/D conversion) get a head-start over the APS. This, however, implied a smaller Fill-Factor (FF) due to the greater number of transistors per pixel, which in turn addresses a blow to sensitivity. In short, a bigger pixel pitch is required to have the same light performance as an APS. Some ways around that include the optimization of the architecture to reduce the number of transistors, adopting an efficient layout (placement and routing) scheme and employing newer technologies with reduced feature size - like the CMOS 90nm technology that is the technology of choice for this Master's Thesis.

4.3 Why the CMOS 90nm Technology?

Many particularities inherent to the CMOS 90nm technology back up the choice to adopt it for the implementation of the Cortivision image sensor. These include, but are not limited to, reduced feature size (hence reduced area) and the novelty of this technology in image sensor research. This is while bearing in mind that smaller technologies (even 65nm) are being used by the image sensor industry, but are yet to appear in academic research mainly due to the higher cost of these, decreased availability and design overhead. Moreover, industrial research is in its greater part confidential and not accessible to scholars.

Pixel pitch is one of the parameters that can vary immensely with the technology. The use of the CMOS 90nm technology for this work enables further reduction of the size of the pixel. Nevertheless, one has to be aware of the fact that minimal dimensions are not solely dictated by the most recent CMOS technology; optical limitations have to be taken into account as well. Dierickx et al. had estimated this size to range between 3μm and 5μm [44]. Such smaller pixel sizes almost necessarily require the use of microlenses to increase the effective FF and, consequently, the sensitivity of the sensor. So basically, the reduced feature size should be taken advantage of to reduce the size of the pixel without, nonetheless, reducing the photosensitive area.

The reduced feature size of newer technologies is also accompanied by a greater number of metal layers; a characteristic that offers the possibility of a greater capacitance density [55] - which could be an advantage if proper design considerations are used, yet putting forth setbacks or hindrances some cases. It should be also noted that using the additional layers available to the CMOS 90nm technology as compared to the 0.18μm ones around the photosensitive area could make it harder for the light to reach the silicon.

The reduction in overall chip area possible with the CMOS 90nm technology has its own appeal to us, even if the Pixel Pitch is not reduced. The Cortivision application requires on-chip processing. Reduced feature-size allows the integration of additional transistors inside the pixel as well as integrating other on-chip (out-of-pixel) processing circuitry. So basically, the final version of this image sensor prototype would have most of its clocking circuitry integrated on-chip (instead of having to use a complex External Controller PCB with a VHDL state-machine). The gain in area would become even more substantial at that point. Added to that that the supply voltages used by CMOS 90nm (1V/2.5V in our case) are lower than those used in the CMOS 0.18μm technology (1.8V/3.3V) - which gives the possibility of reduced power consumption. Table 4.1 shows a brief comparison of the advantages/disadvantages considered.

4.4 Pixel Architecture

The pixel featured in this work is divided into four major parts: the photosensitive element, the photosensing circuit, the ADC and the digital memory. Each of these will be thoroughly described and discussed.

4.4.1 Photosensitive Element

Different types of photosensitive elements have been discussed in Chapters 1 and 2. To recapitulate, PTs offer higher gain which allows higher signal levels, but which also renders them more sensitive to process variations between transistors. This leads to an increase in FPN compared to PDs. PGs have a lower capacitance than PDs and are the same for both CMOS and CCD processes. Since charges are collected underneath the gate, current leakage is minimal. They are, however, better adapted

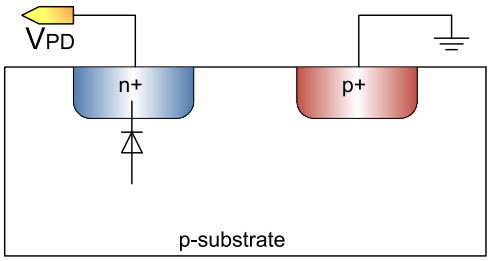
Table 4.1 Comparison between CMOS 90nm and CMOS 0.18μm Technologies

CMOS 90nm	CMOS 0.18μm
+ Smaller Feature Size	- Larger Feature Size
+ Greater Number of Layers (Routing)	- Fewer Number of Layers (Routing)
- Greater Number of Layers (Shading)	+ Fewer Number of Layers (Shading)
+/- Greater Number of Layers (Capacitance)	-/+ Greater Number of Layers (Capacitance)
- Higher Leakage	+ Lower Leakage
+ Higher Fill-Factor	- Smaller Fill-Factor
+ Lower Supply Voltages	- Higher Supply Voltages
+ Less Power Consumption	- More Power Consumption
+ More integrated electronics in same area	- Less integrated electronics in same area
+ Newer technology (obsoleteness)	- Older technology (obsoleteness)
- Probably requires microlenses	+/- Might require microlenses
- Probably requires process modification	+/- Might require process modification

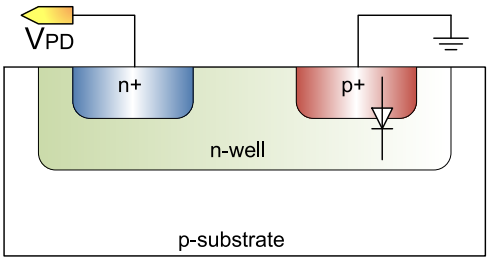
to CCD processes that allow less spacing between the PG and TG wells, hence improving charge transfer. Another disadvantage lies in the fact that light needs to traverse the PG to reach the substrate. This results in a decrease in QE that is particularly noticeable for the blue spectrum. It is also worthwhile to note that the lower capacitance of the PG with respect to the PD does imply a higher conversion gain, which in turn means a higher signal level; nevertheless, the use of PGs entails a decrease in FF which decreases the signal level beneath that of a PD to the point that the PD would result in a better SNR despite having a higher noise level. The TFA process does provide better light absorption compared to a standard silicon process and the PDs in that case are placed on top of the pixel matrix resulting in a near-100% FF eliminating the requirement for microlenses. The TFA process permits excellent pixel isolation, hence reducing crosstalk, is perfectly CMOS compatible and has the advantages of the CMOS process the likes of high per-pixel transistor count and reduced power consumption. As for PPDs, they are usually less prone to current leakage than PDs and offer better QE than both PDs and PGs. Nevertheless, they call for two additional masks which makes a high market demand key to making it worthwhile. In spite of everything, the use of PDs is the best option with the stan-

dard CMOS process offered by the Canadian Microelectronics Corporation (CMC) - keeping in mind that we are taking high risks using such an implementation with the CMOS 90nm technology which is not recommended. It would be less effective than PPDs, especially when it comes to image lag and ghosting, but would still do the job for a prototype such as the one required by this Master's Thesis. PDs, despite being less attractive than PPDs, are still used in middle-end industrial cameras to reduce the cost induced by the necessity of having additional masking layers. It is, however, interesting to note that if performance and sensitivity do turn out to be an issue, the same pixel circuit could be migrated to a TFA process. We will now focus the remainder of the discussion on PDs, their functioning, and modeling.

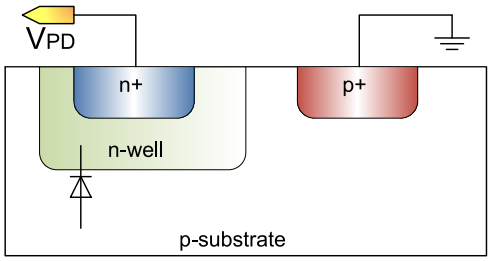
Having settled for a PD implementation, our CMOS process of interest is an N-Well/P-Substrate process. It allows for the use of n+/p-substrate, p+/n-well and n-well/p-substrate PDs. The first type, shown in Figure 4.1(a), suffers from more parasitic coupling, leakage and crosstalk because it is not isolated. It does boast the advantage of higher sensitivity though. The second type, featured in Figure 4.1(b), allows the isolation of each pixel in its own well, reducing parasitic coupling and routing unwanted charges to the supply; thereby reducing leakage and crosstalk. The



(a) n+/p-substrate



(b) p+/n-well

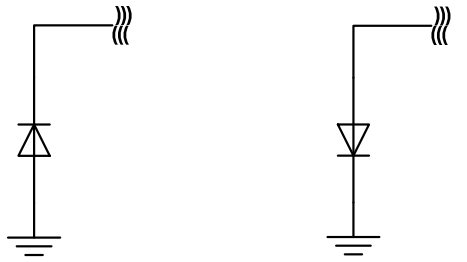


(c) n-well/p-substrate

Figure 4.1 Photodiode Implementations (Note that the diodes are represented here in reverse-biased configuration)

use of this type of PD does, however, entail a reduction in sensitivity [129]. The third configuration, shown in Figure 4.1(c), will result in a better QE as compared to the other two due to its deeper larger junction, knowing that the photons are absorbed in the PN depletion junction. This is an important parameter for reduced pixel area which reduces the FF making sensitivity an important issue - particularly if microlenses are not available. This option has been opted for, keeping in mind that there is a very important leakage versus sensitivity compromise that might resurface to become an issue.

A PD can be operated in reverse-biased (Photoconductive) mode (Figure 4.2(a)) or unbiased (Photovoltaic) mode (Figure 4.2(b)). On one hand, the photovoltaic mode of operation is preferred for low-frequency (up to 350 kHz) ultra-low light-level applications. They are also less prone to variations in responsivity over temperature. The photoconductive mode, on the other hand, is favored in the case where response speed and linearity are crucial. It permits an increase in the width of the depletion region, and hence a decrease in junction capacitance. It does however have a negative impact on dark current and noise. This latter configuration was opted for [130].



(a) Reverse-Biased (Photoconductive)

(b) Unbiased (Photovoltaic)

Figure 4.2 Photodiode Biasing Configurations

For this, the anode is grounded and the cathode is reset to a high voltage before the start of integration. The incident photons induce a current proportional to the light intensity. Hence, the voltage drop across the PD would constitute an indicator of light intensity. The ideal voltage variation is a function of irradiance (light power) and is given by [131]:

$$\frac{dV}{dt} = \frac{1.2\lambda P\eta}{C_{PD}} \tag{4.1}$$

where: λ is the light wavelength in μm,
P is the light power in Watts,
η is the QE,
C_{PD} is the diode capacitance in F/cm^2,
and 1.2 incorporates several constants.

This equation clearly indicates that the PD is less sensitive to wavelengths in the lower end of the spectrum (e.g. blues) and more sensitive to those in the higher end (e.g. reds and IRs). Ideally, the size of the PD has no effect. In practice, however, an increase in area leads to an increase in capacitance. This decreases the sensitivity and affects the linearity of the variation in voltage across the PD. A larger perimeter, however, means a larger junction, which means that more photons could be collected. This could make it advantageous to reduce the area of the PD without a corresponding reduction in perimeter. This can be achieved by adding transistors or contacts inside the PD. But the increase in perimeter could also be accompanied by an increase in dark-current [131]. A design compromise needs to be made.

A PD model was used based on [132] to be able to simulate the circuit. The model consists of a diode, a shunt resistor, a series resistor and a capacitor. For an ideal PD, the shunt resistance is infinite, and the series resistance is negligible. The capacitance reflects the area of the PD. A current source is used to model the photocurrent. Figure 4.3 shows the configuration used.

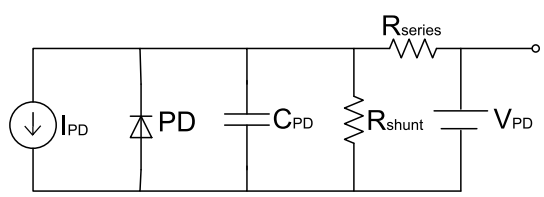


Figure 4.3 Photodiode Model

4.4.2 Photosensing Circuit

The photosensing circuit consists of the PD reset and biasing transistors, the shutter and the in-pixel amplifier. It is implemented using thick oxide transistors to reduce leakage. The circuit is shown in Figure 4.4.

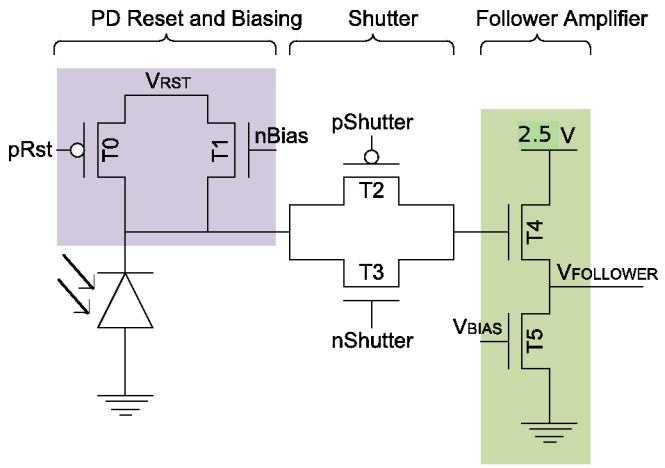


Figure 4.4 Pixel Photosensing Circuit

The PD basically acts as a capacitor that is discharged by the photons hitting it. The greater the light intensity, the faster the discharge (i.e. the higher the discharge rate). Therefore, the PD needs to be initially charged to a certain potential, which is why it is required to reset it to a certain voltage, termed V_{RST} hereafter.

A typical reset circuit consists of a single NFET with a constant (or controllable) voltage applied to one of its terminals, the PD connected to the other and the reset signal controlling its gate. A variant to this was used, since the sensor at hand is supposed to operate in several modes - including linear and logarithmic - so an exclusively hard reset would not provide this possibility. This is why an additional transistor was added to the reset/PD voltage biasing circuit.

The circuit for this particular architecture consists of two transistors connected in parallel: an NFET and a PFET, both connected on one end to a constant, controllable, voltage source, and on the other to the PD. The NFET is required to operate the pixel in logarithmic mode. This is done by applying a constant voltage to its gate to force it to operate in the weak inversion region. This would cause the current generated by the PD to have a logarithmic behavior - hence the term logarithmic mode.

This approach has the advantage of being time-independent (the current is constantly generated, and no reset of the PD is required since the NFET is always supplying a voltage) so the value of the pixel can be read at any time. Another advantage, is that the DR is increased since the linear response is traded in for a

logarithmic one. A disadvantage, however, of this mode of operation is its sensitivity to noise, and of course the tradeoff of linearity which might be a requirement for certain applications - which is why we offer this mode as an option to our sensor and not as an exclusive method of operation. The NFET from the "typical" architecture was traded in for a PFET to conduct a better hard reset of the PD in the linear mode of operation [133].

Shutter and Leakage Compensation

A typical shutter consists of an NFET transistor. It can in some cases be boosted up to a CMOS transmission gate for better conductivity. However, a problem with all such shutters is leakage. This occurs when the PD voltage becomes negative, and a shutter that is supposed to be off (not conducting) will conduct, rendering the results erroneous. A quick fix to this problem would be resetting the PD while the shutter is supposed to be non-conducting. This would prevent the voltage from draining too much - and thus from becoming negative. A problem with that fix is that the PD integration and readout of the pixel would no longer have the possibility of being done in parallel - so the pixel rate would decrease, hence decreasing the frame rate. Another fix, would be applying a constant offset voltage to the PD which would raise its minimum voltage to slightly above zero. This can be achieved with no additional circuitry since shutter leakage is an issue only in the linear mode - and not in the logarithmic mode- since in the latter mode, the shutter is always conducting and pixel access is time-independent. Therefore, the NFET transistor is typically off (not conducting) when operating in linear mode. A fix to that would be to give a certain biasing gate voltage to the NFET transistor while operating in linear mode. This would apply a constant offset voltage to the PD, preventing its potential from dropping below zero. However, the voltage applied to the gate is not as substantial as the full 2.5V applied during logarithmic mode operation. Of course, such a fix would affect the linearity of the sensor. This is why it is to be used only with the concurrent integration-readout mode, and to be dispensed of during non-concurrent mode. The compromise would therefore be: good linearity and lower pixel rate versus slightly modified linearity and higher pixel rate.

In-Pixel Amplifier

The in-pixel amplifier is typically a source follower in an APS or DPS. This is the case for this architecture as well, except for a twist that allows the output of the follower to be biased by a current source. So the follower consists of two NFETs: the first being the follower, with its gate connected to the PD output via the shutter, and one terminal connected to a constant voltage source (the supply) and the other connected to the output to be fed into a comparator. This same output node is connected to another NFET transistor that is actually part of a current mirror. The other half of this current mirror is located outside the pixel and is shared by pixels. This biasing is required to control the output voltage swing of the photosensitive circuit since this part of the pixel circuit is implemented using thick oxide 2.5V transistors to minimize leakage, while the remaining part of the pixel circuit (the ADC and memory) are implemented in regular 1V transistors to minimize power consumption. This also allows the output of the follower to take on values between 0 and 1V - which covers the whole input dynamic range of the ADC. In the case where all the circuit was implemented with the same type of transistors, the maximum output of the follower would not have been capable of attaining the maximum voltage of 2.5V due to the inevitable voltage drop across the NFET, which would have as a consequence the result of decreasing the DR of the sensor.

4.4.3 In-Pixel Analog-to-Digital Converter

As mentioned in the previous subsection, the ADC is implemented using 1V transistors. It is also required to be able to differentiate between 256 different shades of gray which dictates a minimum precision of 8-bits. The image processing also requires the capture of 20 frames per image while having an image rate of at least 20 images per second to rival the response of the human eye. This means that the DPS is required to operate at a rate of at least 400 frames/sec (fps) â which in turn dictates the frequency of operation of the comparator.

Several ADC architectures are typically used in DPSs. An ADC - to be contained inside a single pixel - is basically a comparator. These comparator architectures include differential input architectures and switched-capacitor architectures. The former are usually better favored since they do not have the requirement for a capacitor - which takes up a substantial amount of area in a chip layout - particularly in the

case where linearity is sought after and a Metal-Insulator-Metal (MiM) capacitor is required. This requires process adaptation (extra masks) which means an increase in cost but provides a higher capacitance for a given area and better linearity. Nevertheless, such a capacitor cannot accommodate any circuitry underneath it despite the fact of having unused metal layers beneath it (a design rule constraint). Which is why the differential type comparator is the most widespread. However, part of our image processing requires subtracting two consecutive images. A switched-capacitor comparator provides us with the ability to do so in the analog domain even before having to read out the pixel. This speeds up the image processing tremendously (and is the basis for our differential mode of operation). However, this is not easy to achieve with a differential input comparator since a storage node would have to be added, which is nothing but a capacitance - which would revoke the initial reason for preferring such a comparator.

Such an implementation was done and simulated in Cadence, and the simulation results were compared with those of a switched-capacitor implementation. It is important to note that this comparison was done using the CMOS 01.8μm technology and that corner simulations have been performed. Both topologies were operated with frequencies of 0.333MHz (1 / 3μs). This exceeded by far the requirements of 400fps for the proper functioning of the DPS. The switched-capacitance comparator used a capacitance of 5fF. It was a clocked comparator with three clocking signals and their inverses plus an additional validation signal for borderline cases. The offset obtained was of $4.23mV$. The differential-input comparator had an added an analog memory with a capacitance of 7fF to allow for the comparison of two consecutive pixel voltages (which is intrinsic to the topology of the former comparator type). The offset in this case was of $6.01mV$ which, while still being less than the $7.03mV$ upper limit required for an 8-bit precision, was still greater than that of the switched-capacitor topology. However, the differential comparator required two clocks which were operated less frequently thus minimizing the possibility of clock feedthrough especially in the normal operating mode where one of them is operated only once to set the mode and the other is not used. The differential comparator also required two biasing voltages. In short, the switched-capacitor comparator gave a better offset at the expense of more clocking signals with a non-escapable reliance on a capacitor for comparisons. On the other hand, the differential comparator gave a greater, but still acceptable, offset while using less control signals and less clocking with its sole reliance on capacitance

being in the mode that requires the comparison of two consecutive voltages of the pixel. Nevertheless, minimizing offset and silicon area being some of the top objectives, the results were in favor of the switched-capacitor architecture that required a smaller capacitance and hence had a smaller area. More details can be found in Appendix C.

Comparator Architecture: Switched-Capacitor

The final topology adopted for this thesis is the switched-capacitor one, but implemented in the CMOS 90nm technology. The circuit had to be revised and reoptimized to that avail. The final circuit schematic is featured in Figure 4.5.

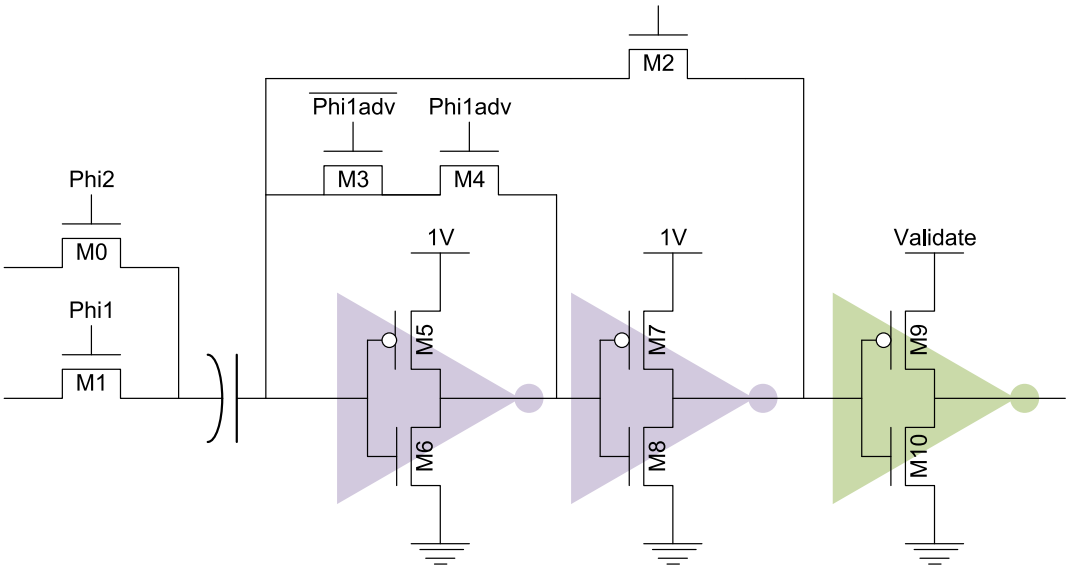


Figure 4.5 Switched-Capacitor Comparator Architecture (CMOS 90nm)

The photosensing circuit in each pixel converts the photocurrent into a voltage. This voltage is fed into the comparator that latches an equivalent digital value into an 8-bit memory. The other input to the comparator is an analog 1kHz ramp going from 0 to 1V generated by an external digital-to-analog converter (DAC). The clocking signals operate at a frequency of 256 kHz resulting in 256 comparisons per ramp period to select the appropriate level of gray which is done by latching the equivalent digital value of the ramp into the per-pixel memory. Large-length NMOS transistors were used at the input to decrease charge injection and clock feedthrough and achieve the required offset. This also eliminated the need to route the complement signals

of $Phi1$ and $Phi2$ into each pixel as compared to transmission gates. Moreover, the greater number of layers in the 90nm technology also allowed us to have a greater value for our capacitor in a more restricted area, and the transistor sizes had to be reoptimized. It has a single input node that is connected to a capacitor. V_{PIXEL} and V_{RAMP} are applied to the input node one after the other by activating $Phi1$ and $Phi2$ respectively. The initial voltage across the capacitor is at the metastable value of $\frac{V_{DD}}{2}$. V_{PIXEL} is then applied giving a voltage drop of $V_{PIXEL} - \frac{V_{DD}}{2}$. After that V_{RAMP} is applied leaving us with a voltage of $V_{RAMP} - V_{PIXEL} + \frac{V_{DD}}{2}$. This means that the capacitor subtracts the two input voltages and then decides which is greater. If V_{PIXEL} is less, V_{CMP} would oscillate between ground and the metastable value. In the opposite case, V_{CMP} would oscillate between the metastable value and V_{DD}. The *validate* signal has been added to force the output value in limiting cases to a valid value. The final inverter has been added to make sure that the output to the memory, V_{OUT}, is always a valid digital value.

The top plate of the capacitor is connected to the comparator since it is deemed more sensitive than the inputs. The signal $Phi1_{ADV}$ is a slightly advanced version of the signal $Phi1$ to limit the effect of charge injection to the closing of switch $Phi1_{ADV}$. A dummy transistor is added next to the $Phi1_{ADV}$ transistor having half its width to absorb the injected charges. For the mode of operation particular to our DPS requiring the comparison of two consecutive pixel values, V_{PIXEL} is applied twice in a row to the input by activating $Phi1$ twice instead of activating $Phi2$. The resultant output would indicate which capture was darker.

A digital state controller was implemented in verilog to generate the clocking signals $Phi1$, $\overline{Phi1}$, $Phi1_{ADV}$, $\overline{Phi1_{ADV}}$, $Phi2$, $\overline{Phi2}$ and *validate*.

Capacitor Design

The choice of capacitor design is mainly a compromise between area, linearity and the ability of adding active components underneath it. Four types of capacitors can be considered: Poly-Insulator-Gate capacitors, Metal-Metal capacitors, transistors connected in a capacitor configuration and Metal-Insulator-Metal (MiM) capacitors. Also, newer technologies put forth smaller feature sizes and a greater number of metal layers. This allows for a greater capacitance density [55].

Poly capacitors were disregarded because it is impossible to have transistors (which also require poly) in the same area. And since the chip is an image sensor, a pixel

is required to have the smallest possible area, and this would substantially increase the area. Moreover, they have a parasitic capacitance to ground that can reach 18% while MOS capacitors can have a parasitic capacitance ranging between 2 and 20% depending on the design. [55].

A transistor in a capacitor configuration (source and drain shorted) gives a good capacitance per area ratio, but gives a non-linear output. This configuration results in $V_{DS} = 0V$ and a capacitance $C = C_{GS}$ that varies depending on the region of operation of the transistor. Capacitors that utilize the MOSFET gate oxide have the highest capacitance density that can exceed $6fF/\mu m^2$ with recent technologies. However, they have a non-linear response with temperature fluctuations and face a tradeoff between the gate oxide thickness and the breakdown voltage [55].

If a good linear response is required, the MiM-Cap technology is very appealing. Nevertheless, it offers a capacitance density of around $1fF/\mu m^2$ which is much less than that of a transistor capacitor. Design rules also forbid the insertion of transistors underneath a MiM-Cap [134], so using a transistor-capacitor might be a more area-saving option; not to mention that MiM-Caps require special processing steps. Nevertheless, with temperature variations, the MiM-Cap provides us with a linear response.

Metal-Metal capacitors have good temperature characteristics as well (linearity), but the absolute value of the capacitance is difficult to control. They also require a large area depending on C_{OX}. The capacitance is basically made up of three components [55]:

- Vertical Fields: Parallel-Plate Capacitance between two conductors on different metal layers
- Horizontal Fields: Parallel-Plate Capacitance between two conductors on the same metal layer
- Fringe Fields: Fringe Capacitance

The further the metal layers from the substrate, the less the parasitic capacitance to ground. Nevertheless, this comes at a decrease in capacitance density. Also, the use of narrower fingers and spacings increases the capacitance, but at an increase in resistance. The location and frequency of vias also affects the resistance. The voltage withstand ability of the capacitor also decreases with the reduction in dimensions [55].

4.4.4 In-Pixel Digital Memory

An 8-bit memory is integrated inside each pixel. The initial design that was implemented using the CMOS 0.18μm technology made use of a 3T architecture as shown in Figure 4.6. This architecture requires careful design because it is very susceptible to leakage. Also, the memory in 0.18μm could hold the value for a limited amount of time and was operated with destructive readout. Despite that it could function for our application and required a reduced number of transistors.

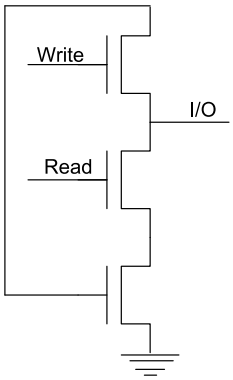


Figure 4.6 3T 1-bit Memory Cell

The attempts at reimplementing this architecture in CMOS 90nm technology were fruitless. The leakage was too high, and simply opening the gate after writing the value caused the value to be drained. There was nothing stored to be read. The only solution to implement this architecture was to increase the capacitance of the storage node by adding a capacitance, and this led to a huge increase in memory size. This made this memory architecture lose its appeal.

A more standard and simpler memory cell was reverted to using a 5T architecture that is refreshable, shown in Figure 4.7. This architecture has the disadvantage of having an increased number of transistors that increases the area required in the pixel, and that it requires both NFETs and PFETs. The requirement for PFETs means the addition of an NWELL. The photodiode also has an NWELL. The design rules force a minimum spacing between the wells, which adds more constraints to the placement and routing of the pixel.

The way the memory functions is by either writing the content of the bus to the memory or by writing the content of the memory to the bus. The comparator generates the Memory Enable ($MemEn$) signal that shorts the memory content with

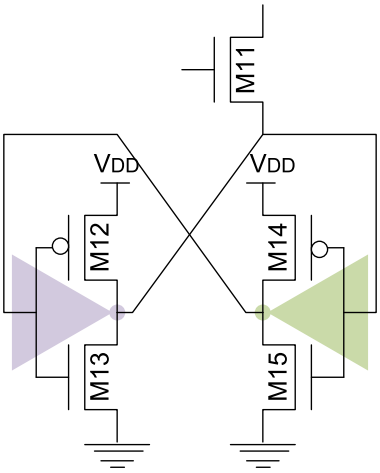


Figure 4.7 5T-Memory Cell Architecture

the bus. When comparing, the memory is initially reset to zero by setting a zero value on the bus. The bus is then disconnected (set to high impedance) when the time comes to read from memory. The bus is an 8-bit bus that is connected to buffers to be able to read out the values from the chip and to avoid loads at the output of the chip from affecting the bus.

1V transistors were chosen for the memory to take advantage of both the reduced area and power consumption. The disadvantage of these with respect to thick oxide transistors is the increased leakage. Nevertheless, the use of thick oxide transistors for the digital memory would have forgone the utility of reducing the technology size, and the comparator that is implemented with 1V transistors as well would not have been an adequate input stage to the memory without a workaround.

4.5 Modes of Operation

The image sensor supports several modes of operation to support the different image processing modes required by the image processing module in the Cortivision project. Four modes of operation were implemented.

- A standard linear integration mode of operation.
- A linear integration mode of operation with multiple exposures
- A logarithmic mode of operation

- A differential (or difference) mode of operation

A discussion follows about each of these modes.

4.5.1 Single-Exposure Linear Integration

This is the standard mode of operation of the sensor. It has an average DR, and relatively high readout rate. It is not very susceptible to noise.

For this mode of operation, a low signal is applied to the gate of M1 (to disable it) and the PFET M0 is used as reset transistor for the PD. This is done by giving a low pulse before the start of integration which applies the PD reset voltage V_{RST} to the PD charging it. M0 is then set to high, and the PD is left to integrate. That is, the light incident on the PD would generate a photocurrent I_{PD} that would discharge the PD at a different rate depending on the intensity. The shutter (M2 and M3) does not conduct at first. After a certain programmable integration time, the shutter is operated to conduct, and the follower (M4 and M5) gives a voltage output proportional to the light intensity. The output of the follower goes into the comparator that would compare it to a ramp signal V_{RAMP} going from 0 to 1V generated outside the chip. 256 comparisons (2^8) will take place to be able to discretize the output of the follower into an 8-bit digital value. The 8-bit digital value of the ramp signal is also fed into the chip on the 8-bit bus connected to the memory. This value is latched into the 8-bit memory every time the comparator finds that the follower voltage still has not reached the ramp voltage. When the voltages are equal or greater, the value is no longer latched (the MemEn signal given by the comparator no longer latches the memory), so the old value is retained.

This mode has two flavors: non-concurrent (shown in Figure 4.8) and concurrent (Figure 4.9) where integration and readout can overlap. Shutter leakage is observed in the latter case, as discussed previously in Section 4.4.2.

4.5.2 Multiple-Exposure Linear Integration

The multiple exposure mode is an extension of the linear integration one. The sensing circuit operates in the same manner, and so does the comparator, except that the control signals are different. The ramp voltage is only ramped from half its value (0.5V) to 1V to be able to latch a value only for the pixels that have reached half the

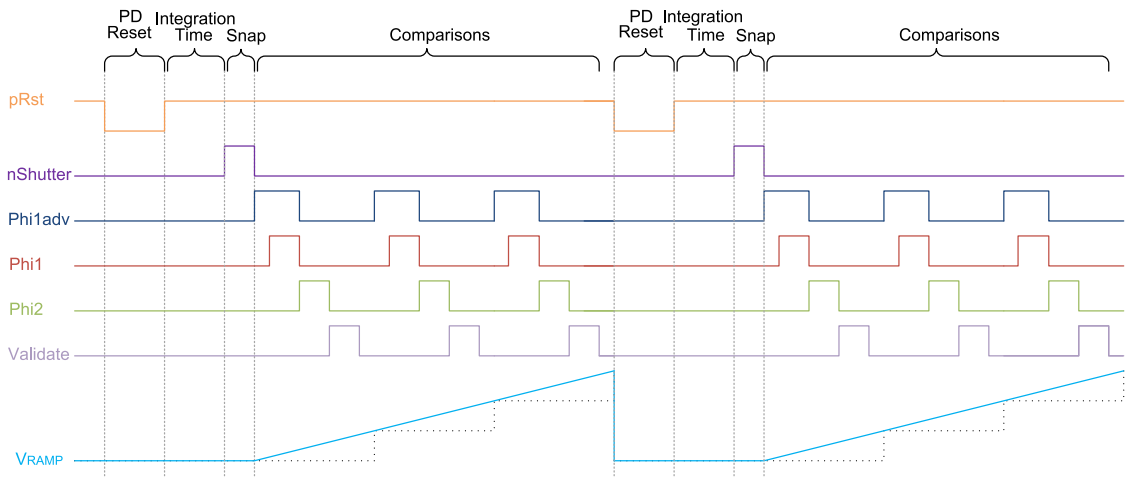


Figure 4.8 Linear Integration Mode Non-Concurrent Clocking Signals

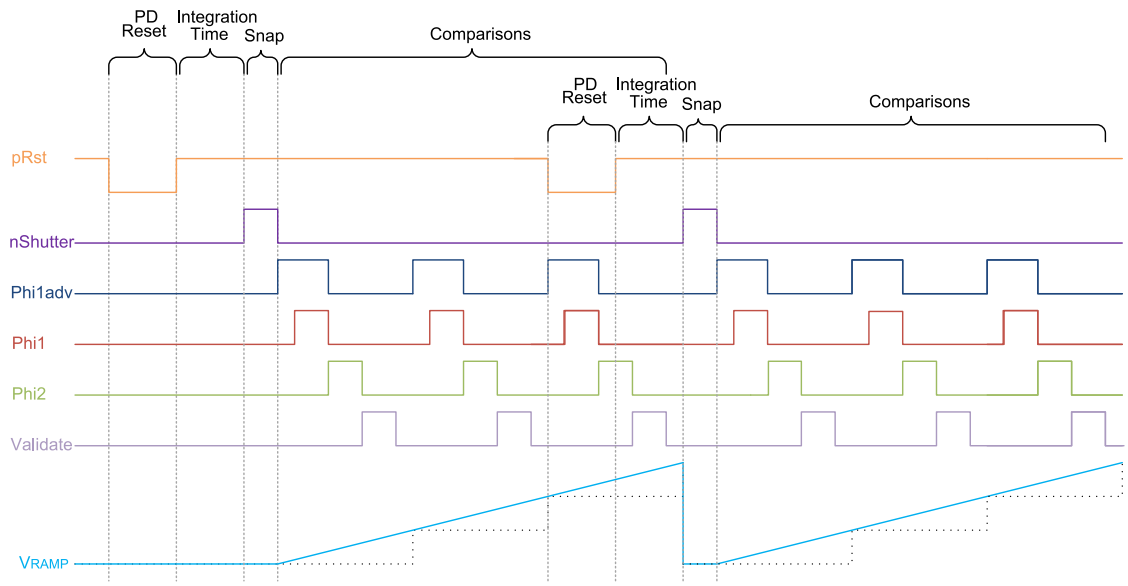


Figure 4.9 Linear Integration Mode Concurrent Clocking Signals

voltage DR. The shutter is activated at a programmable time T for the first iteration and the output compared to the ramp. This is then repeated at times 2T, 4T, ..., 2^kT to achieve a floating point representation where k is chosen depending on the required extension in DR that would be increased by a factor of 2^k.

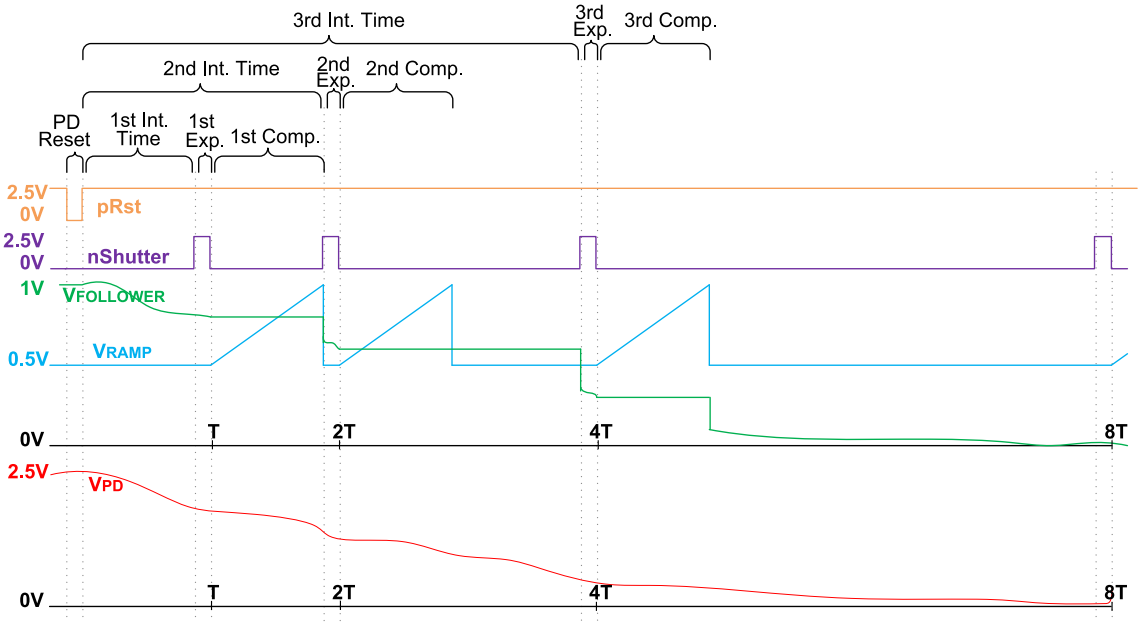


Figure 4.10 Multiple Exposure

4.5.3 Enhanced Dynamic Range Logarithmic

For this mode of operation, the gate of M0 is set to a high voltage (to disable it) and the NFET M1 is used to bias the PD. This is done by placing a high voltage at the gate of this transistor which would force it to operate in the weak inversion region. This would cause the photocurrent to vary logarithmically, and the voltage output from the follower to abide by the following equation [90]:

$$V_{FOLLOWER} = V_{RST} - \frac{kT}{q} ln(\frac{I_{PD}}{I_0}) \tag{4.2}$$

where $\frac{kT}{q}$ is the thermal voltage (the voltage a single charge falls through to pick up the thermal energy kT) and I_0 is a constant.

The PD no longer needs to be reset because a constant voltage is continuously applied to it. The voltage output is compared to a ramp as for the linear integration mode, except that the absence of integration time allows the pixel to be read out at any time. The shutter is always conducting as well. This mode of operation increases the DR, but is sensitive to noise, which decreases the SNR, and again impacts the DR. The voltage swing is reduced as well. Logarithmic pixels are also more sensitive

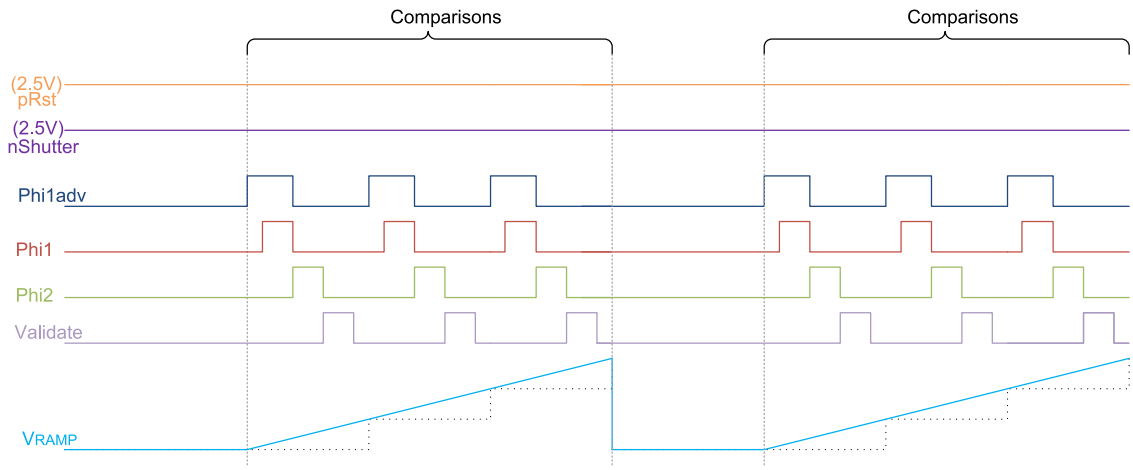


Figure 4.11 Logarithmic Mode

to pixel parameter variations introduced during fabrication. This gives rise to a considerable fixed pattern noise (FPN) [80].

4.5.4 High-Speed Differential

For this mode, the ramp input is no longer used. The follower output is compared to a delayed version of itself to achieve a binary value. The memory is initialized to 0, and the value of the pixel is compared to the previous value of itself resulting in "0000 0000" or "1111 1111". This would end up giving a binary image that is useful for Cortivision's 3D image processing module that requires subtracting two consecutive scenes with inverse light patterns projected on them. More details concerning that can be found in Doljanu's work [135; 136].

4.6 Overall Architecture Overview

The overall architecture of the proposed DPS is shown in Figure 4.13. One row is selected at a time, and the 8-bit digital values stored in the memories of the corresponding pixels are transferred to a shift register for readout. The row select circuitry is made up of a shift register (as compared to a decoder) to decrease the number of inputs, and thus pads, required. The control signals are generated by an external VHDL digital controller as well as some analog circuitry. Control of the shift registers allows the selection of a subset of the matrix for readout, decreasing

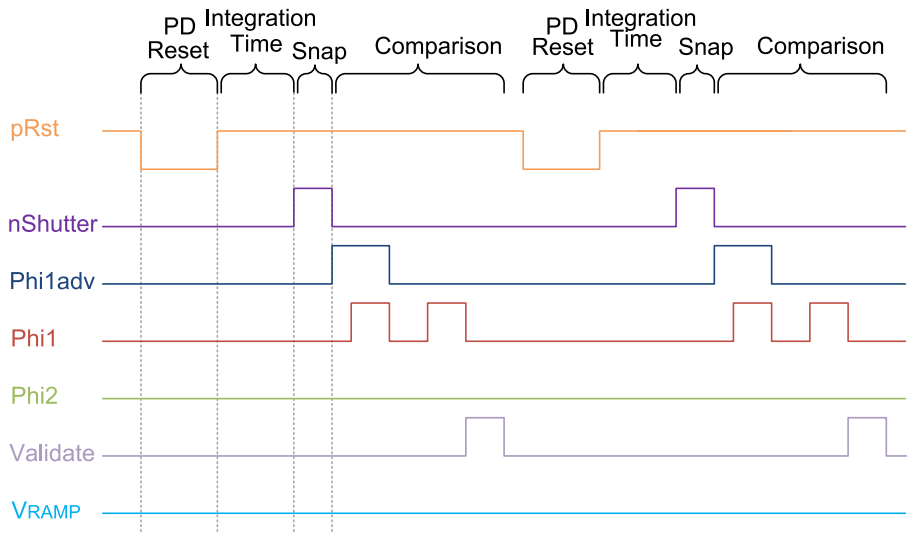


Figure 4.12 Differential Mode Clocking Signals

the resolution as well as the readout time and hence increasing the frequency of operation. A common digital to analog converter (DAC) external to the chip delivers a reference voltage (usually a ramp) to the comparators within each pixel to convert the photocurrent into a digital value.

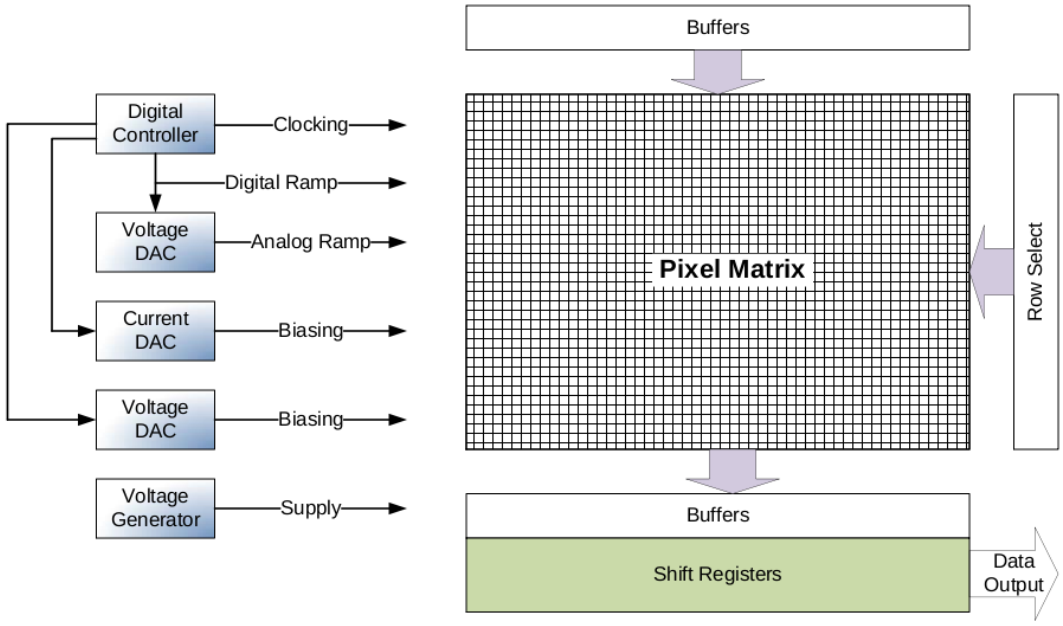


Figure 4.13 Overall Image Sensor Chip Architecture

4.7 External Controller

Since the chip requires external clocking signals and biasing, a PCB is required. The external controller was designed to be flexible and to accommodate this chip and give enough leeway to be reused in any eventual designs using similar packages of an image sensor chip or of any other chip with the same package that requires external control.

The external controller comprises several modules: an FPGA board to supply the digital clocking signals, and a custom-made PCB to supply biasing, analog, and power signals alongside with any other required nuances, and a computer to visualize the output of the chip.

This, however, does pertain to an ideal case. In reality, several intermediate strategies were devised. A logic analyzer was used to supply and to probe signals, as well as an oscilloscope, a ramp generator, and a frequency generator.

The ideal setup aimed at is shown in Figure 4.14. More details can be found in Appendix B.

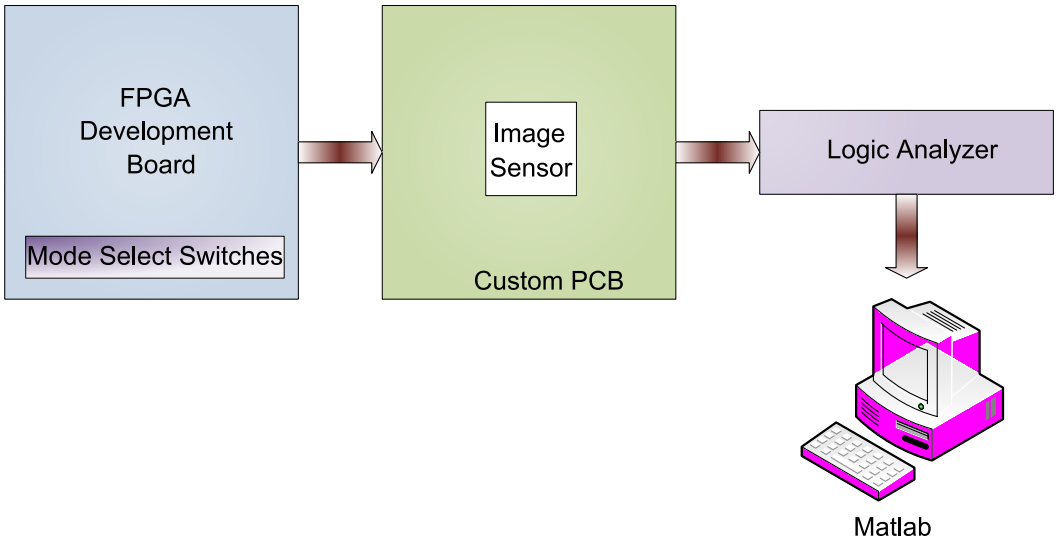


Figure 4.14 Ideal Overall Test Setup

4.8 Conclusion

The schematic design of the chip was discussed, detailing the different parts of the pixel (photodiode, image sensing circuit, ADC and memory), and the overall chip

configuration was overviewed. Tradeoffs were discussed, decisions were justified, and risks were laid down. The final pixel uses a photodiode, switched-capacitor comparator, 5T-memory and the readout circuit replaces a conventional decoder by a shift-register to minimize the required number of pads.

The test setup design was also described, and the details of the Printed Circuit Board to be used to that avail were put forth as well as its schematic. The requirements for the components were stated, and the choices were justified. The flexibility of the designed was also emphasized, as well as its versatility if debugging is required - without forgetting the possibility of reusing it for other prototypes or even different projects.

Chapter 5

IMPLEMENTATION AND RESULTS

The implementation of this work is divided into several parts: the ASIC, the PCB and the VHDL Controller. Each of these will be discussed alongside with the implementation considerations that were taken into account. Simulation results will be presented, and measurements where applicable.

5.1 ASIC Implementation

The image sensor chip was implemented using Cadence and Spectre in the CMOS 90nm technology. The circuits were initially implemented and simulated as schematics, parts were modeled using Verilog-A, the digital controller was modeled using Verilog to be able to interface it with the transistor circuit, and finally the layout was drawn, post-layout simulations were conducted and the circuit was modified where required to compensate for the additional parasitics that came to be. Transistor sizes were optimized to obtain an adequate response, decrease the offset of the comparator, and make sure the memory is able to store a value for an appropriate length of time. Minimal dimensions and optimal layout being key for image sensor design, the layout was optimized to be compact and to avoid unnecessary spaces.

One thing that became an issue was the design rules forcing a minimum spacing between N-Wells. The design had to be carefully manipulated so that tiling the pixels next to each other did not create any DRC violations among the PD well, thick oxide reset PMOS transistor well, and memory PMOS transistors wells. Figure 5.1 shows the layout for a single pixel.

Each pixel also requires a substantial amount of clocking and supply signals to be routed in, as well as data buses to be routed in (Digital Ramp) and out (Memory Content Readout). Manually routing pixels one by one is cumbersome, and next to

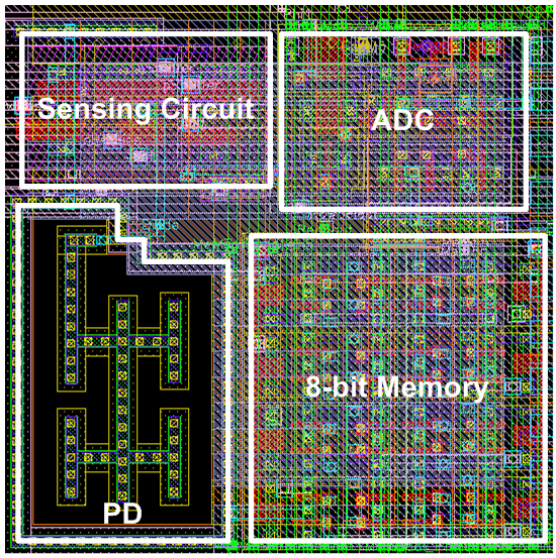


Figure 5.1 Pixel Layout

impossible with the exponential increase in the size of the matrix with the increase in resolution. To avoid that, the pixel layout was carefully designed so that the signal wires passing through the array would be connected simply by aligning the pixels next to each other.

As for the capacitor, several architectures were implemented in layout, extracted, and compared. The details may be found in Appendix A. Our technology of choice being the CMOS 90nm technology, seven metal layers are offered. Layers M1 and M2 were used for connecting the pixel circuit. Layers M3 and M4 were used to route the signals in and out of the pixel. This left us with layers M5 through M7 to be used to form a capacitor. Layer M5 was used as a plate to decrease the influence on the circuitry underneath and was connected to the less sensitive node to decrease the effect of parasitics, while layers M6 and M7 were divided into alternating fingers to increase the capacitance density. This allowed us to achieve an extracted capacitance of around $14.9fF$.

Buffers were added to each column bus to make sure that the contents of the memories read out from the pixels are valid digital values before reaching a shift register used to shift out the frame pixel by pixel. Figure 5.2 shows a subcircuit of the chip combining pixels, shift registers, and buffers.

The silicon area attributed by CMC was limited to $1.0mm^2$. This did not hinder

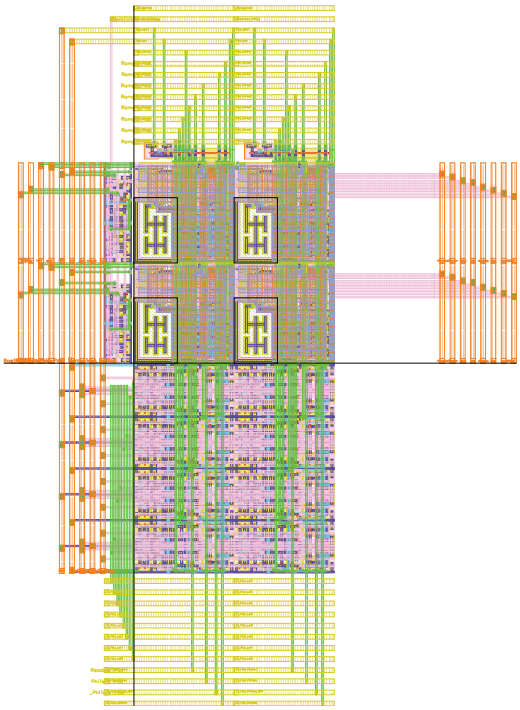


Figure 5.2 Representative Circuit Layout

us in the design itself, but did lead to issues due to the high number of required inputs and outputs. The CMOS 90nm technology itself requires a maximum spacing between VDD and Ground pads that are required for both supplies of the core, and of the ring - this is not to mention ESD Clamps. So basically, insufficient pads became an issue. To try and circumvent that, the initial architecture that used a decoder to select the row of the pixel matrix to be read out was traded in for a shift register and signals that required their complements to be input as well were inverted on-chip. Also, the inputs and outputs of the Test Module were multiplexed with other signals. Appendix A has more details.

5.2 Printed-Circuit Board Implementation

The PCB was designed and implemented using Mentor Graphics PADS. The components were selected considering the frequencies of operation and supply voltages. Another important parameter was the packages: these were chosen so that they were relatively straightforward for myself to solder them on the PCB by hand. Resistors

and capacitors were added to the design based on the individual components spreadsheets and on the supply. The resistor-based voltage divider was simulated using Cadence and was shown to work at a frequency of 60 MHz to convert a 3.3V square wave to a 1.0V one (see Figure 5.3) as well as with a breadboard setup.

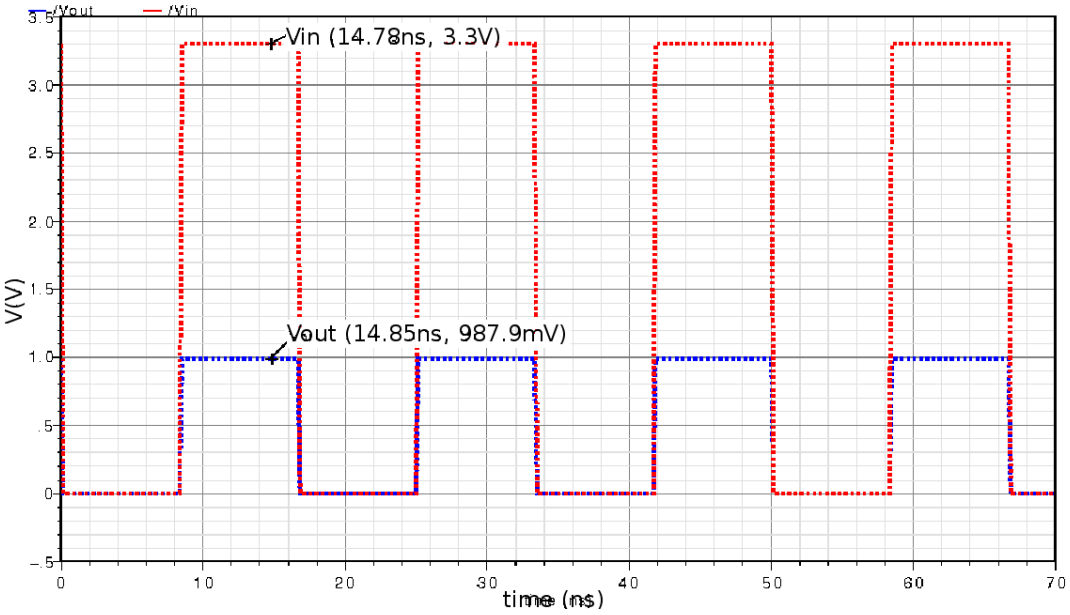


Figure 5.3 Voltage Divider Simulation using Cadence

Figure 5.4 shows the routed footprint of the PCB. More detailed drawings can be found in Appendix B.

5.3 Controller Implementation

The details pertaining to the implementation of the controller in VHDL, the interfacing with Matlab, and with the Logic Analyzer have been confined to the Appendix to simplify the main text.

5.4 Post-Layout Simulation Results

This section deals with the simulation results of the implemented circuits and modules. These would mainly be centered around the Comparator (or ADC) with its

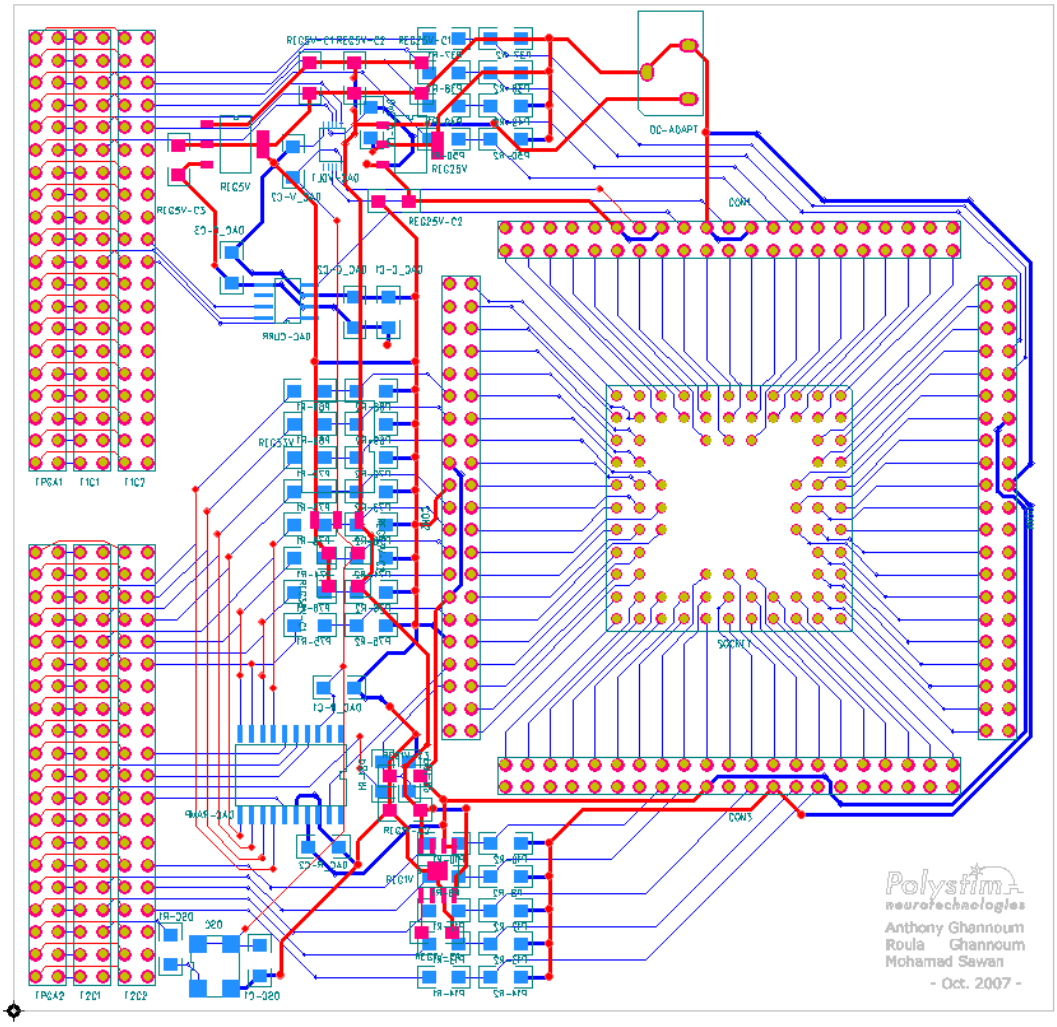


Figure 5.4 PCB Routing using Mentor Graphics PADS

various clocking schemes, the photosensing circuit in its different modes of operation, as well as the test setup PCB. The subsequent section would cover the experimental measurements.

5.4.1 Comparator

The switched-capacitor comparator is used in the same manner for both the Linear and the Logarithmic Modes. The clocking signals are different, however, for the Differential Mode. The following subsections review these.

Linear and Logarithmic Modes

The comparator clocking signals are the same for both the Linear and Logarithmic modes since in both cases the voltage output of the follower has to be compared to an analog ramp. The digital 8-bit equivalent of that analog ramp is fed into buses going into the per-pixel memories, and the memory enable (MemEn) signal is repetitively activated to latch the digital value inside the memory until the two signals are equal - therefore the last value will be retained - which corresponds to the digitized value of the follower voltage. Figure 5.5 shows some of the pertinent concurrent signals for a comparator in these modes starting with the pixel reset and shutter signals, followed by the MemEn and comparator output signals, the simulated diode voltage with the corresponding follower output voltage, the digital ramp (Mem[7:0]), the clocking signals (Phi's and Validate) and finally the biasing and reset voltages.

Figure 5.6(a) shows a more vivid depiction of the operation of the comparator where the MemEn signal is shown to stop "latching" when the follower output and the ramp are equal. Figure 5.6(b) shows a closer view of the point where the follower voltage and the ramp are equal. The difference between the point of the last memory latch and the crossing of the two signals of interest is of 1.613mV in this case - which is below the 3.9mV required for an 8-bit precision over a 1-V swing.

Differential Mode

The comparator when operated in Differential Mode, subtracts two consecutive values of the output of the follower. Figure 5.7 shows a simulation output for the comparator in this mode. Notice that the MemEn signal latches for one of the cases and not for the other indicating which signal is higher.

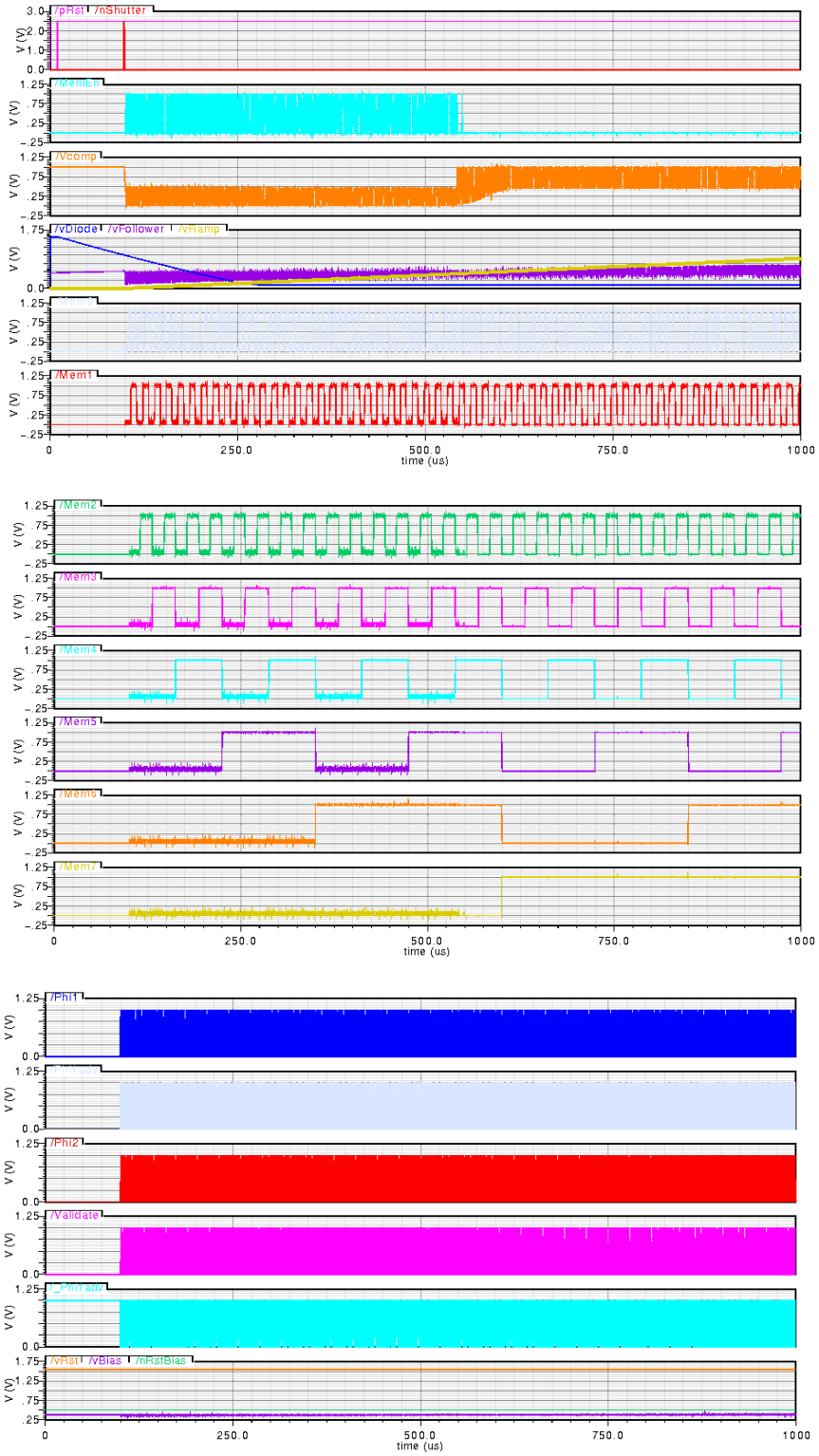
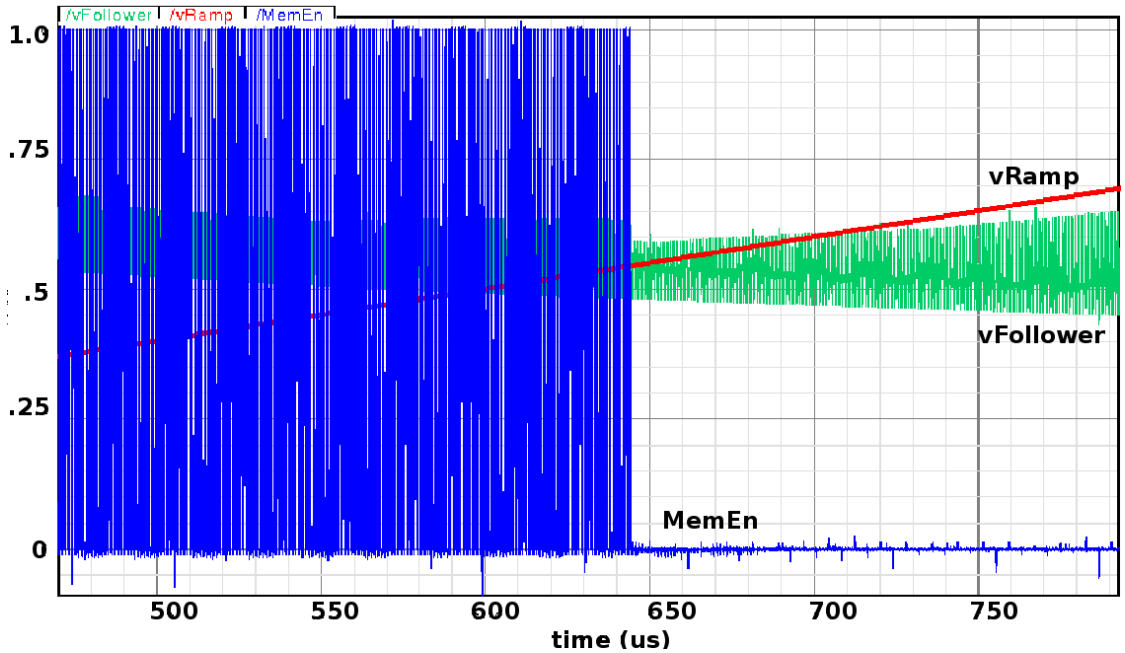
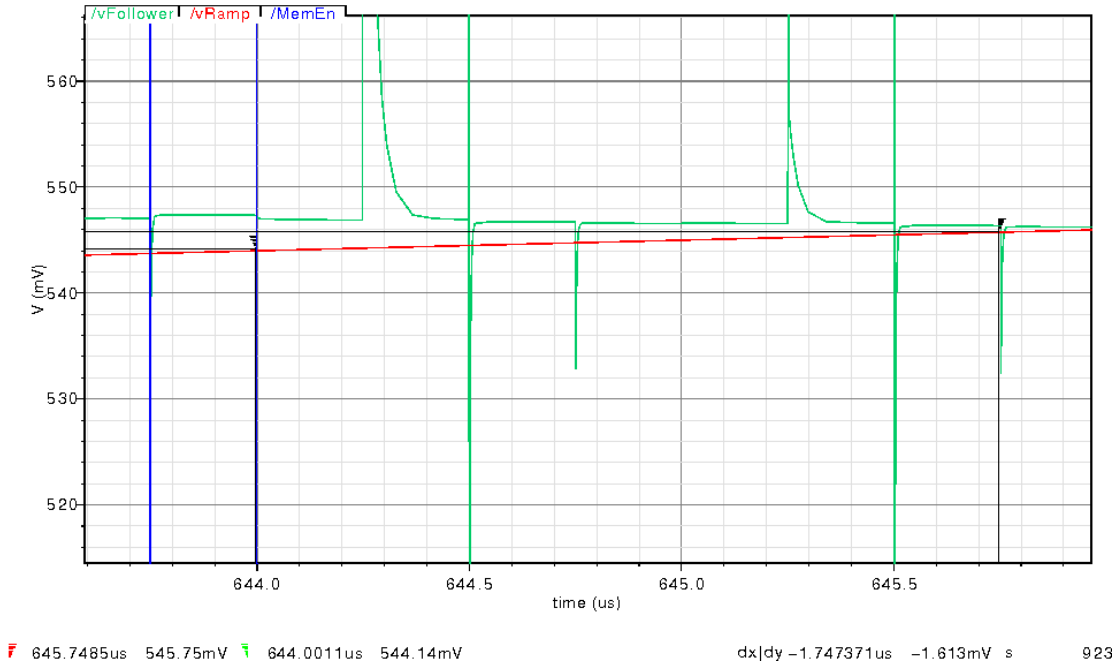


Figure 5.5 Pertinent Comparator Signals Simulation in Linear and Logarithmic Modes



(a) Comparator $MemEn$ signal comparing $V_{FOLLOWER}$ to an Analog Ramp



(b) Zoom on subfigure (a) showing an offset $dy = 1.613mV$

Figure 5.6 Comparator Operation Simulation (Linear and Logarithmic Modes)

5.4.2 Photosensing Circuit

The photosensing circuit consists of the photodiode, reset circuitry, shutter and follower. It can be operated in a regular Linear Integration mode or in a Logarithmic mode for enhanced Dynamic Range. The following subsections show curves and descriptions for these two modes.

Logarithmic Mode

Figure 5.8 shows the output of the photosensing circuit when operated in logarithmic mode. The subfigure to the left depicts the output of the follower versus the diode current. The subfigure to the right shows the time response of the follower output at different diode currents. One may notice that the output of the follower is constant for a given diode current which makes it possible to consider the readout of logarithmic pixels time-independent - of course assuming that the scene is not changing or in motion.

Figure 5.9 shows a somewhat more linear response when the curve is plotted over a logarithmically scaled axis. One should keep in mind that this mode enhances the DR by increasing the light threshold at which the sensor saturates, but at the expense of a decrease in SNR and a non-linear response.

Linear Mode

For the Linear Integration mode of operation, the diode voltage decreases at a rate proportional to the photo-current. Figure 5.10 shows the output of the photosensing circuit when operated in this mode. The subfigure to the left depicts the output of the follower versus the diode current - notice that it varies linearly. The subfigure to the right shows the time response of the follower output at different diode currents. One may notice that the rate of decrease of the voltage output of the follower is constant for a given diode current, but increases for higher photo-currents. Since the output of the follower will change with time, it is mandatory to use a shutter to take a snapshot of the image. The delay between the reset pulse of the photodiode and the shutter pulse is the integration time.

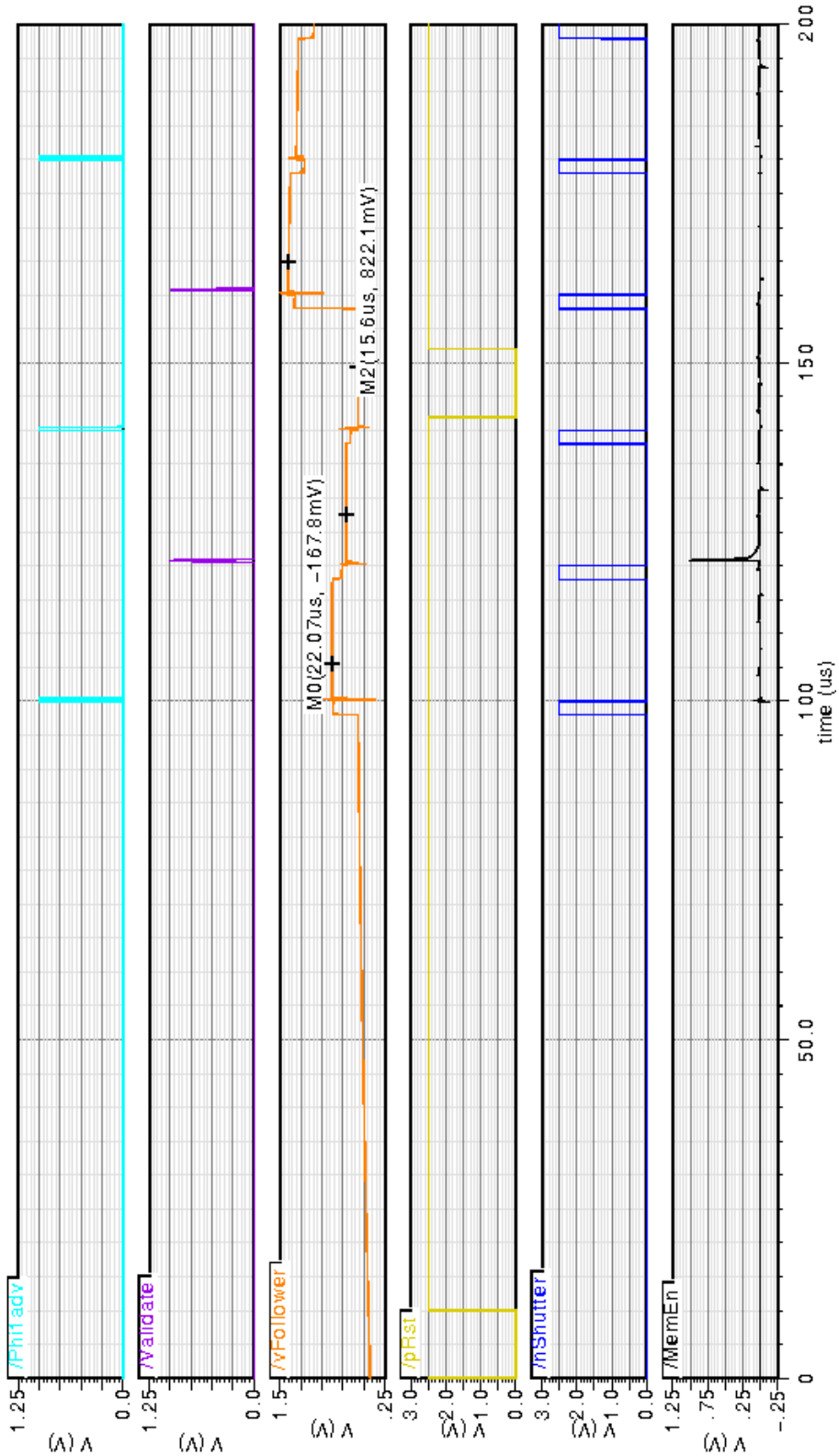


Figure 5.7 Comparator Simulation (Differential Mode)

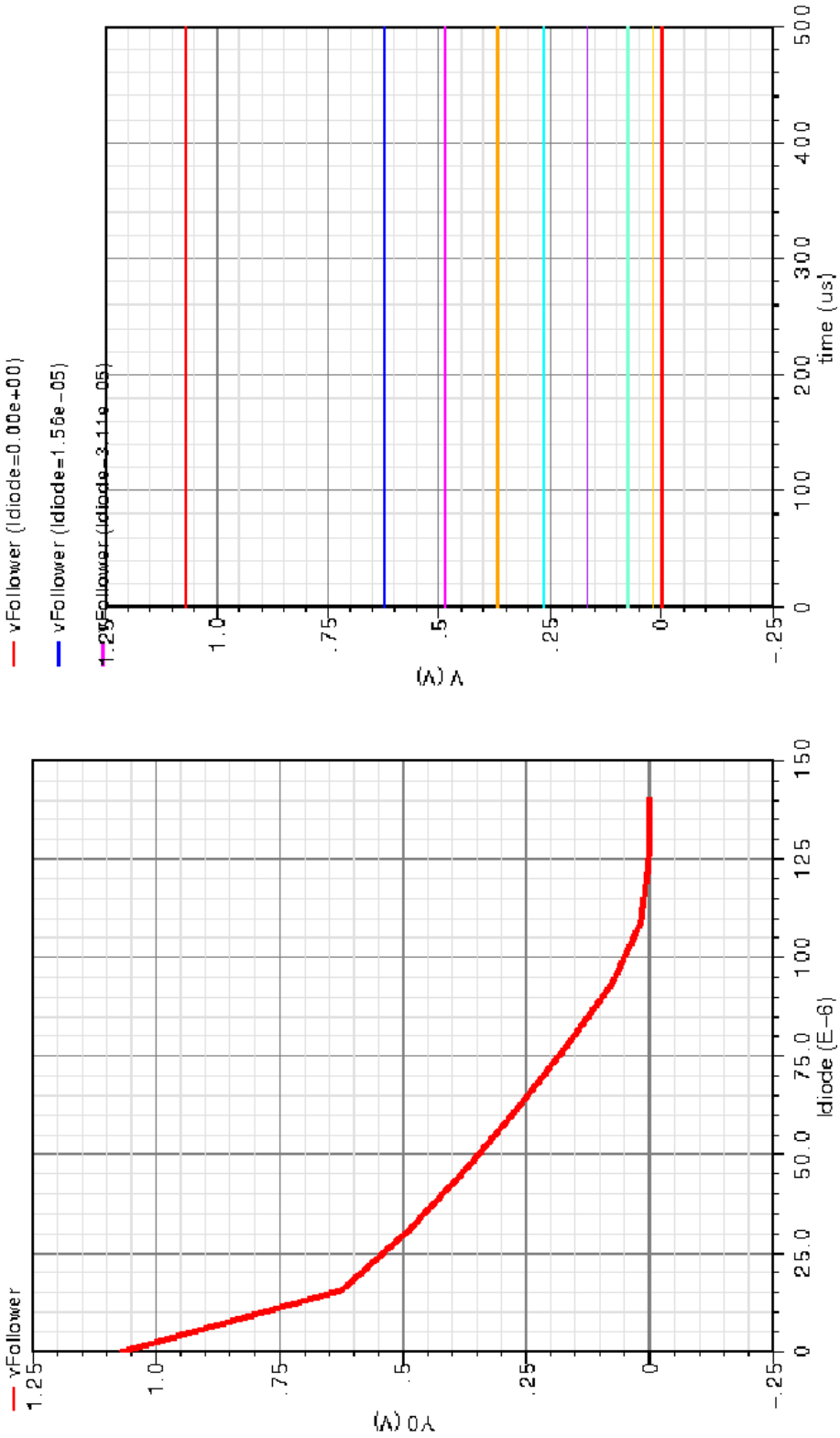


Figure 5.8 Logarithmic Mode Output Simulation

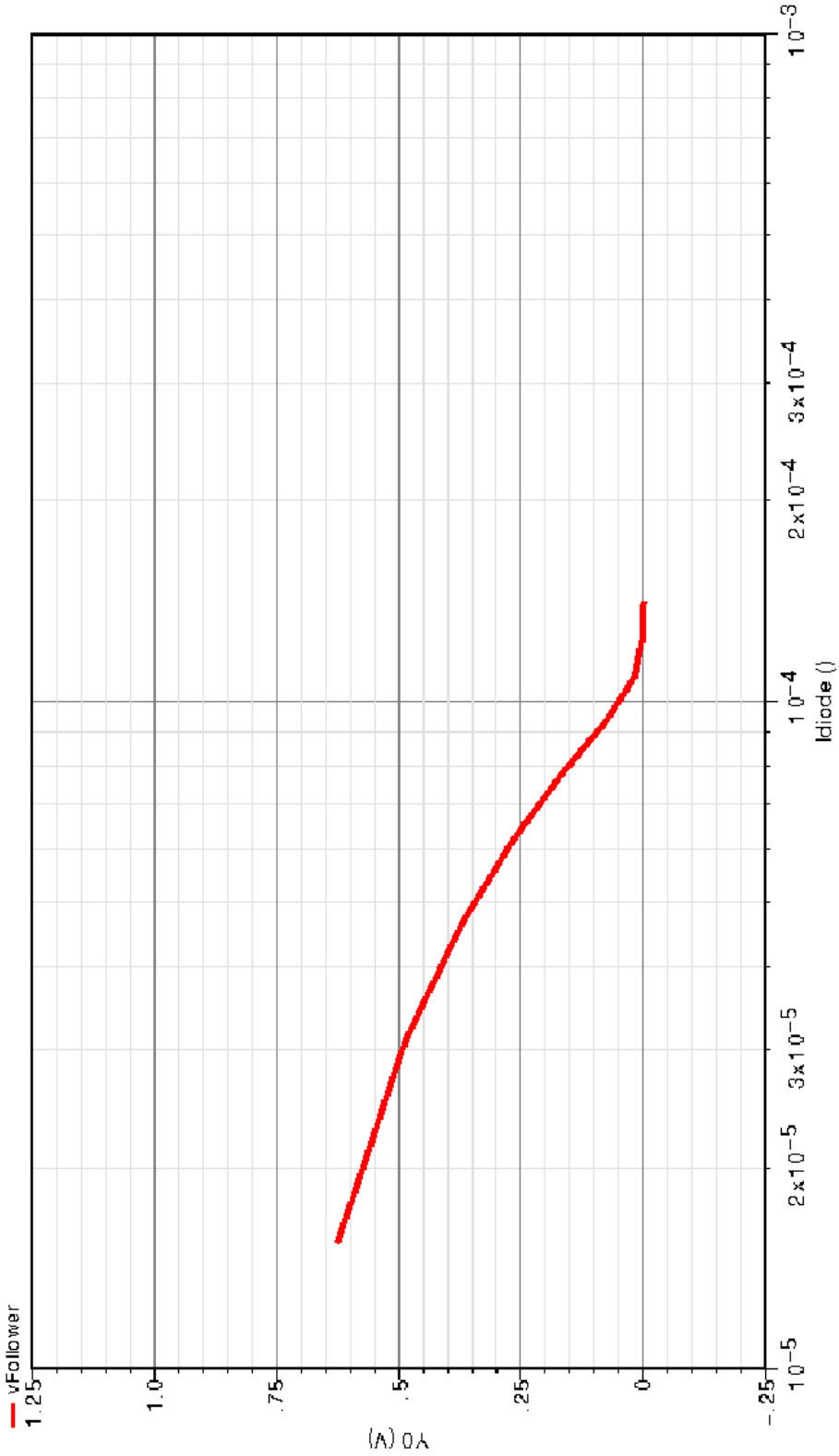


Figure 5.9 Logarithmic Mode Output Simulation (Log Axis)

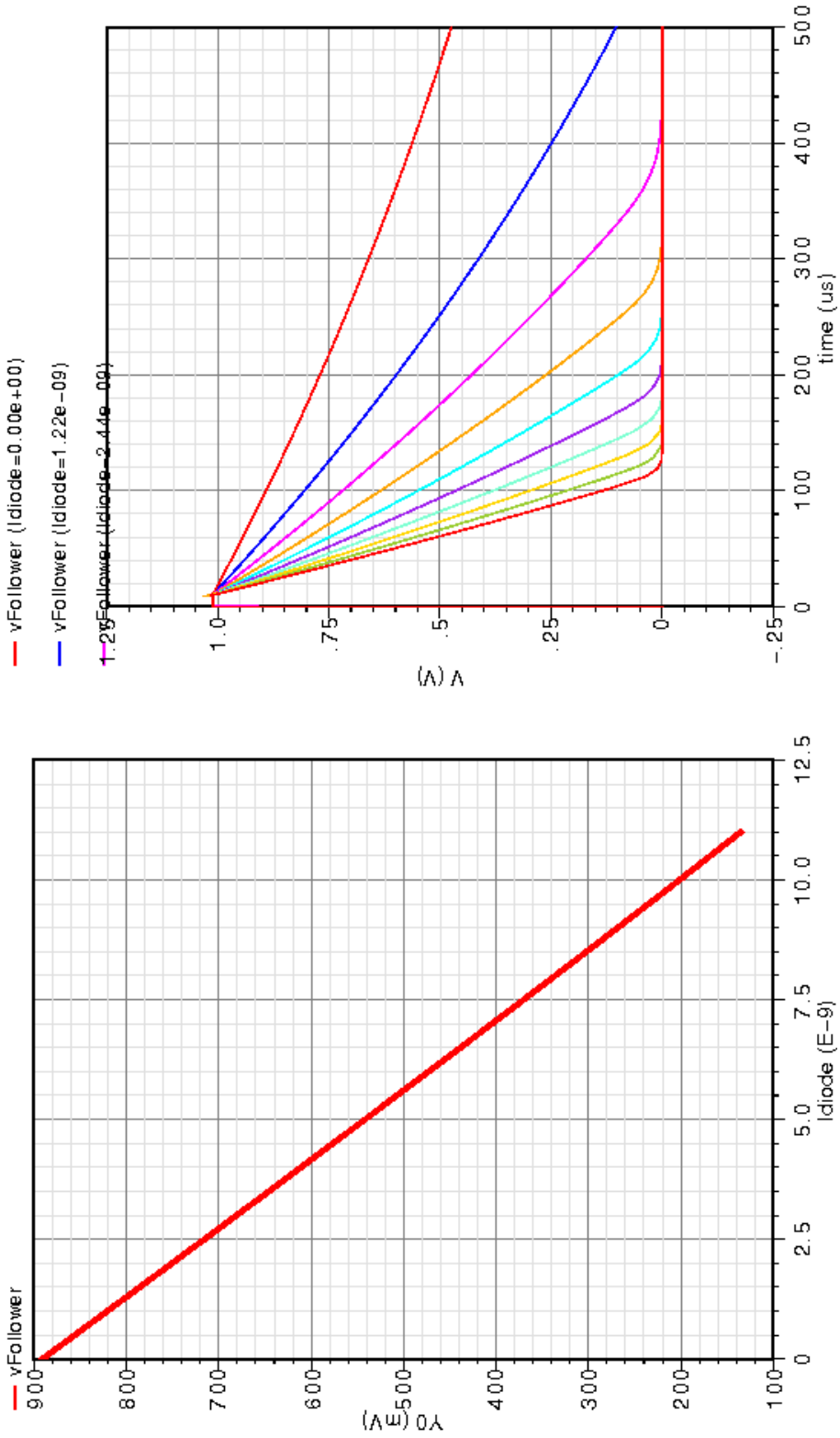
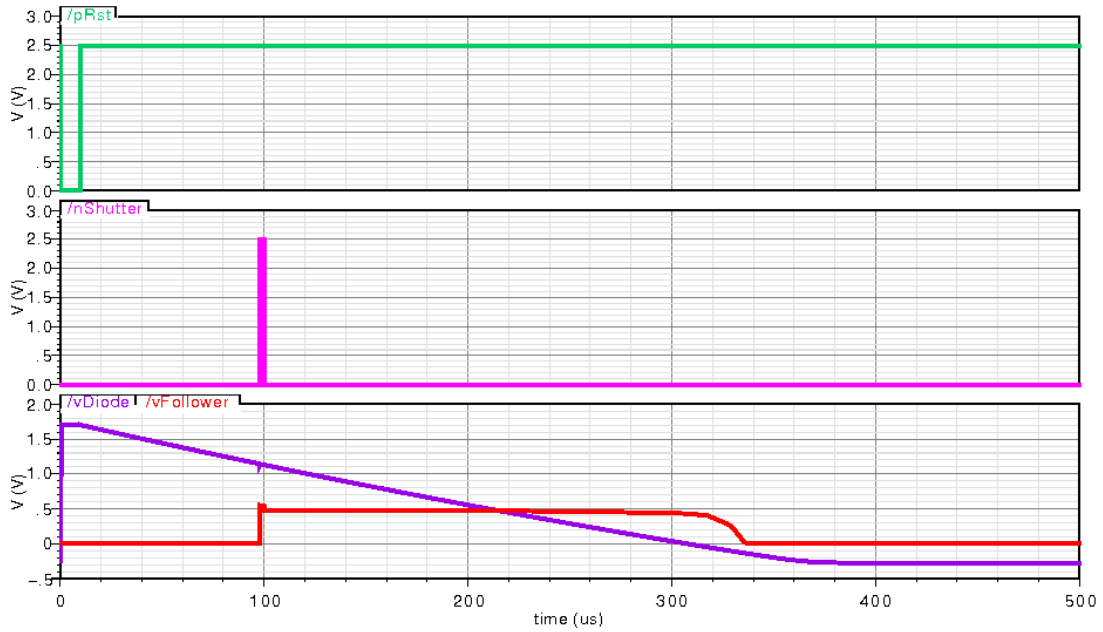


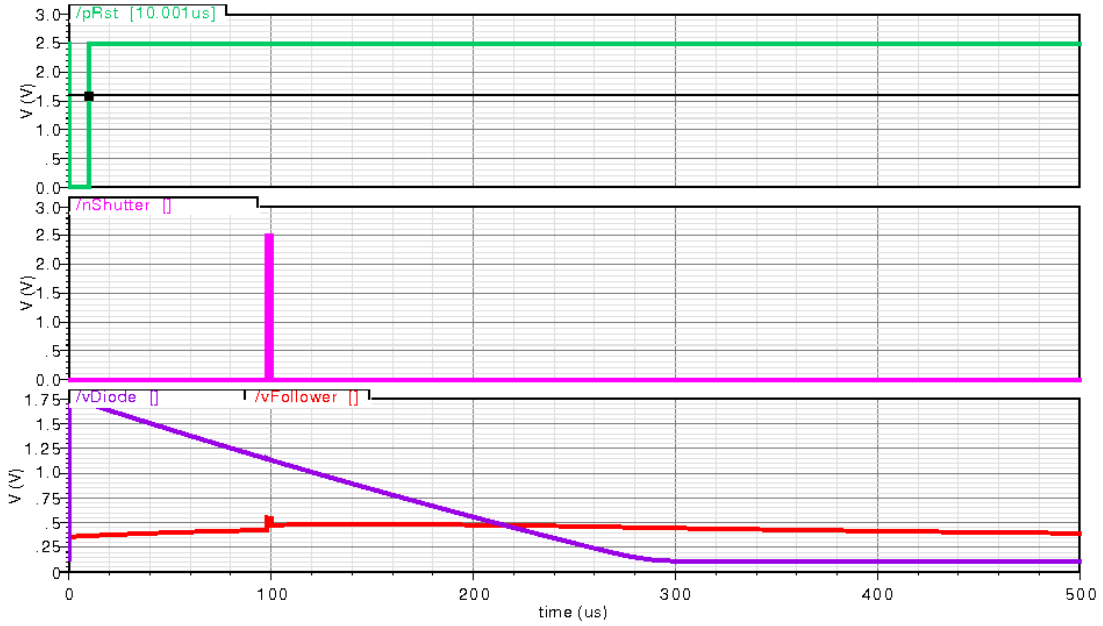
Figure 5.10 Linear Mode Output Simulation

Shutter Leakage

The issue of the shutter leaking for negative photodiode voltages is illustrated in Figure 5.11(a). Notice the drop in the output of the follower when the photodiode voltage drops below zero. To avoid that, a biasing voltage was applied to prevent the PD voltage from becoming negative. Figure 5.11(b) shows that the follower output retains its value.



(a) Shutter Leakage



(b) Elimination of Shutter Leakage

Figure 5.11 Shutter Leakage Rectification Simulation

5.5 Experimental Measurements

This section deals with the experimental measurement results of the implemented circuits and modules comprising both the chip and the PCB.

5.5.1 Comparator

Linear and Logarithmic Modes

Figure 5.12 shows some of the signals pertinent to the comparator generated and measured by the test setup. The upper signal is the ramp generated by a DAC on the custom-made PCB and controlled by the VHDL FPGA controller on the Spartan-3 Development Board. The middle one is Phi1 (the fluctuations are not clear since the image is "zoomed out", and the third signal is the shutter that is activated once per exposure (i.e. once per ramp in regular Linear and Logarithmic modes).

Figure 5.13(a) shows a measurement of the $MemEn$ signal from the test setup. The upper signal is the $Phi1$ clock, the two middle superposed signals are the analog ramp (going from 0 to 1V) and the forced follower output of the test module, and the lowest signal is the $MemEn$ one. We may notice that the $MemEn$ signal is taking on a valid value of 0 or 1 when comparing or resetting the comparator, with an output value at a metastable value (around 500mV) when the comparator is not used and the Validate signal that supplies the $MemEn$ inverter is low. However, the signal is not behaving as expected regarding the comparison. The output of the follower is never found to be equal to that of the ramp. This is probably due to the fact that charge leakage is a considerable issue for this technology, and the clocking signals are draining the value of the capacitor when activated, despite the Post-Layout simulations indicating no problem.

Multiple Exposures Mode

The Multiple Exposures mode is a variant of the Linear Integration Mode where the shutter is activated several times (i.e. at several exposures) and the ramp signal goes from $\frac{V_{DD}}{2}$ to $V_{DD} = 1V$ for each exposure instead of from 0 to 1V; as shown in Figure 5.14(a) and its zoomed counterpart Figure 5.14(b).

Figure 5.15 shows the $MemEn$ output of the comparator of the test module.

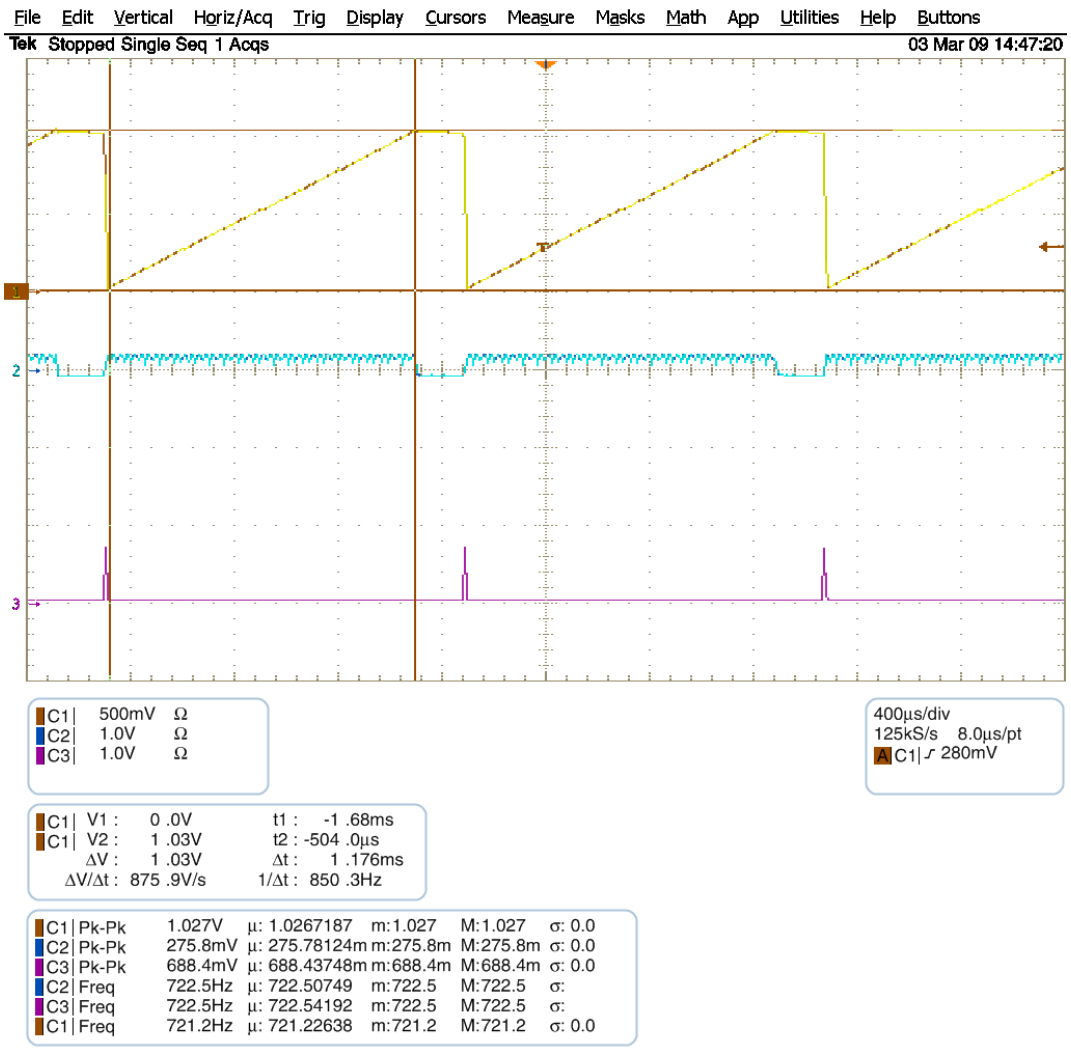
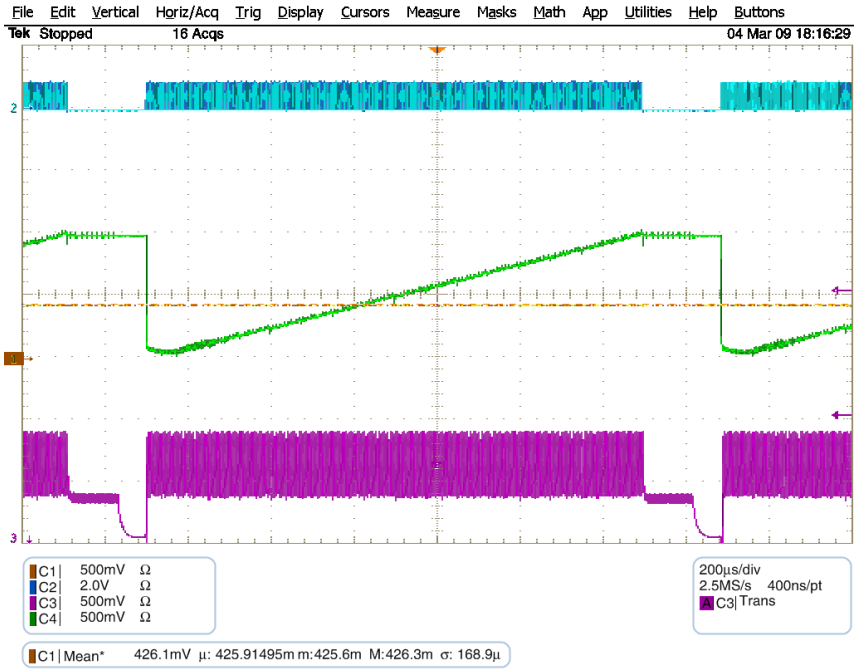


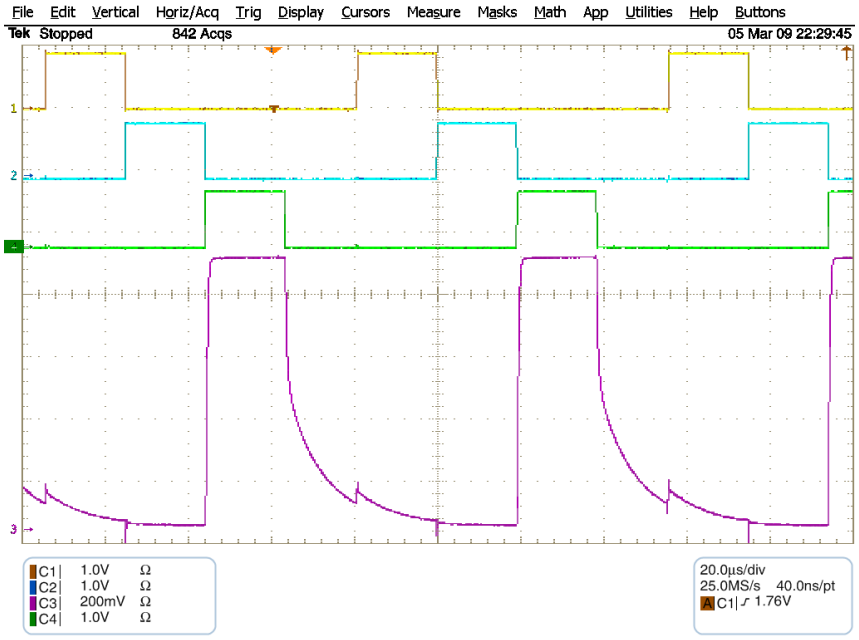
Figure 5.12 Experimental Measurements of the Linear Mode Signals ($V_{RAMP}, Phi1, nShutter$)

Differential Mode

To get a test measurement for this mode, the follower node of the test module was forced to two different voltages while applying the correct clocking signals. Figure 5.16(a) and its scaled counterpart Figure 5.16(b) show the clocking signal $Phi1$ at the top and the $MemEn$ signal at the bottom. The $MemEn$ signal is latching the memory; however, for the same reason as in the previous sections, the memory is latching inappropriately.



(a)



(b)

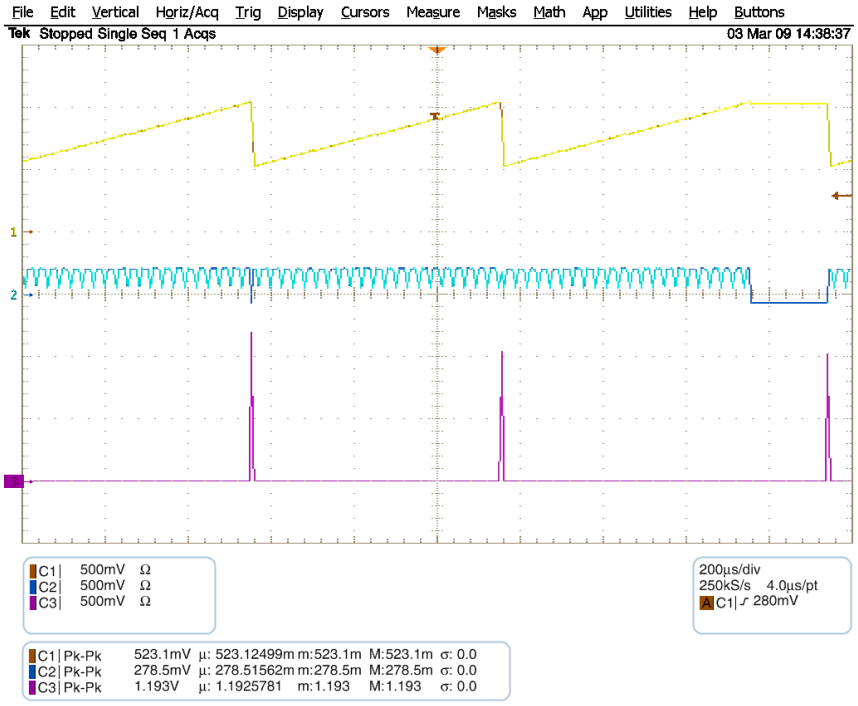
Figure 5.13 Comparator $MemEn$ Experimental Measurements (Linear and Logarithmic Modes)

5.5.2 Shutter Leakage

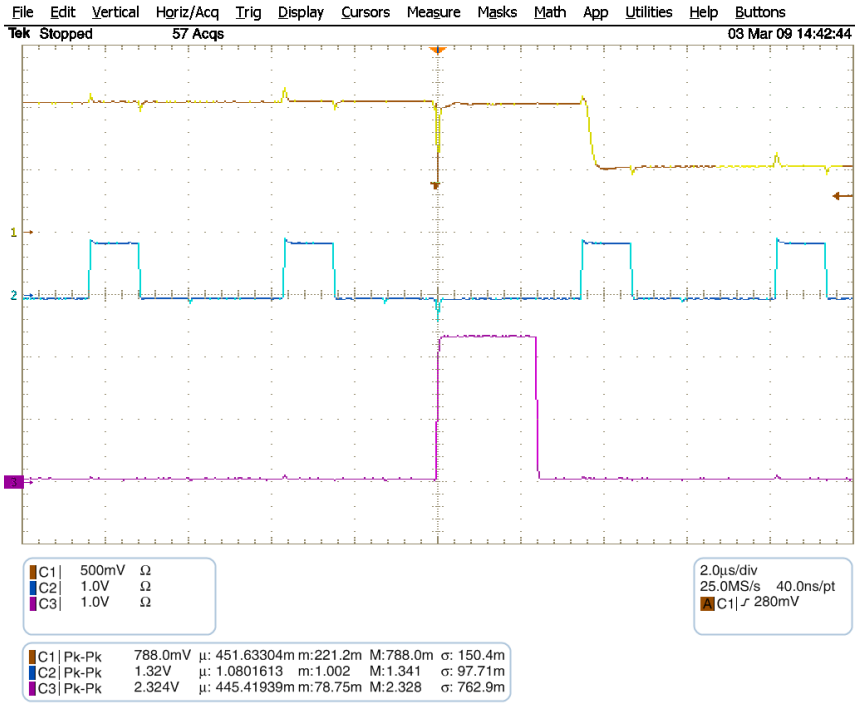
The follower voltage was shown to follow the reset voltage of the PD in a scaled manner. Figure 5.17(a) shows a reset to a low voltage, while Figure 5.17(b) depicts a reset to a high voltage.

The PD voltage was then ramped, with $nRstBias$ set to 0V (no leakage control). The follower voltage scaled the ramp correctly as shown in Figure 5.18(a) where the follower output goes between 0V and 1V. $nRstBias$ was then set to 500mV to prevent possible shutter leakage. The linearity was expected to be affected by that, and Figure 5.18(b) shows that the lower voltages of the ramp scale less well than the higher voltages.

Figure 5.19 sees the effect of activating the shutter on the output with nRstBias at 0. One may notice that the shutter does not leak for lower voltages (first shutter activation) but has more trouble with that at the second shutter activation.



(a)



(b)

Figure 5.14 Multiple Exposures Mode Ramp and Shutter Experimental Measurements

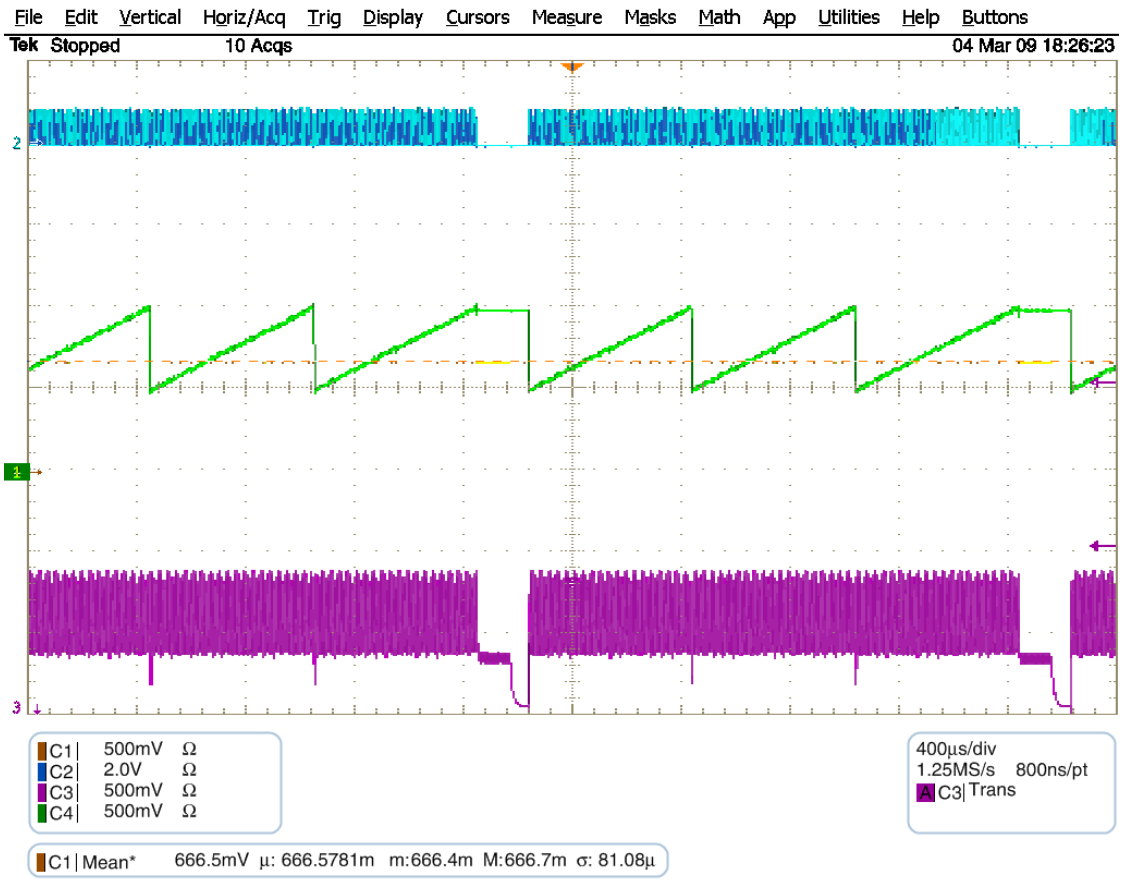
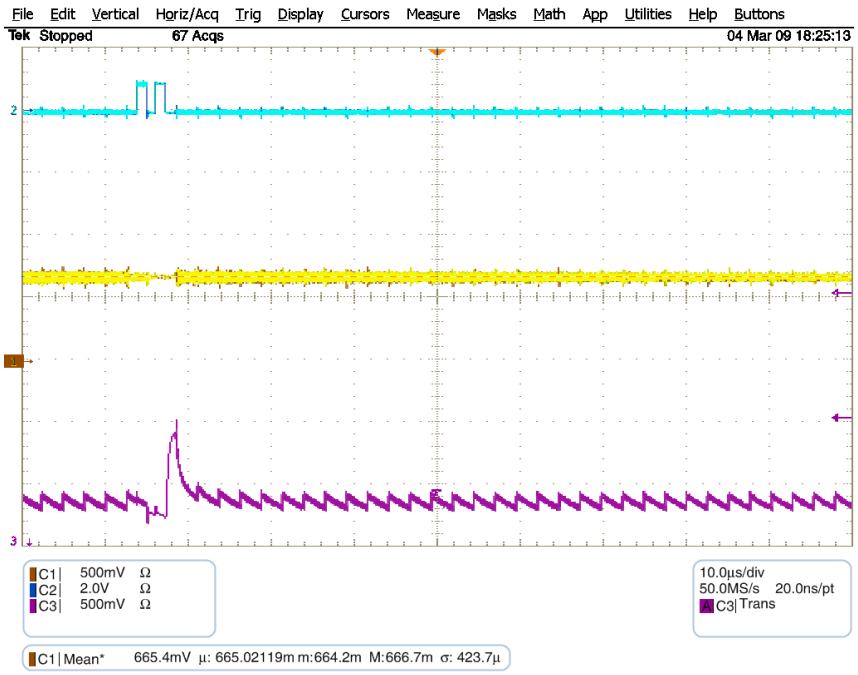
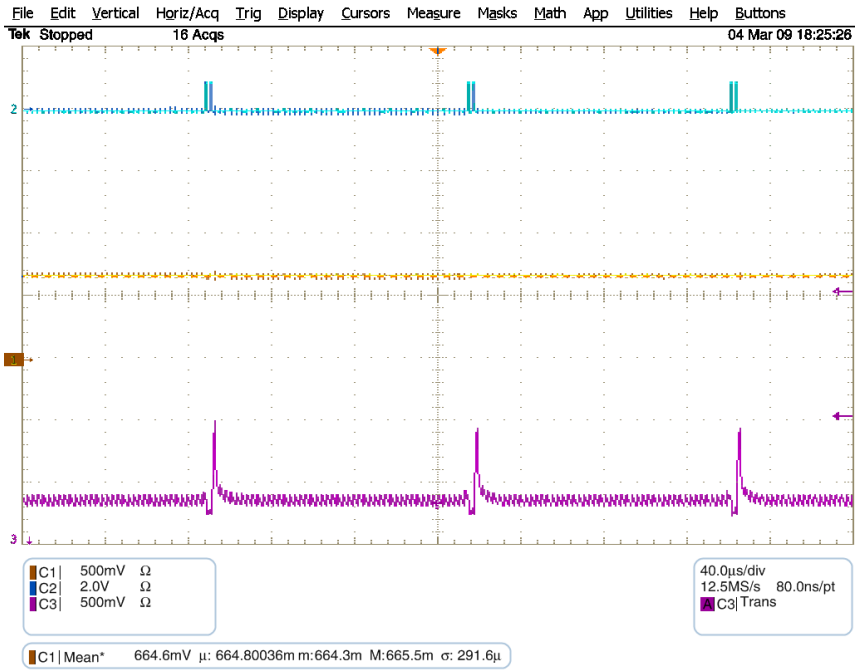


Figure 5.15 Comparator Operation Experimental Measurements (Multiple Exposures Mode)

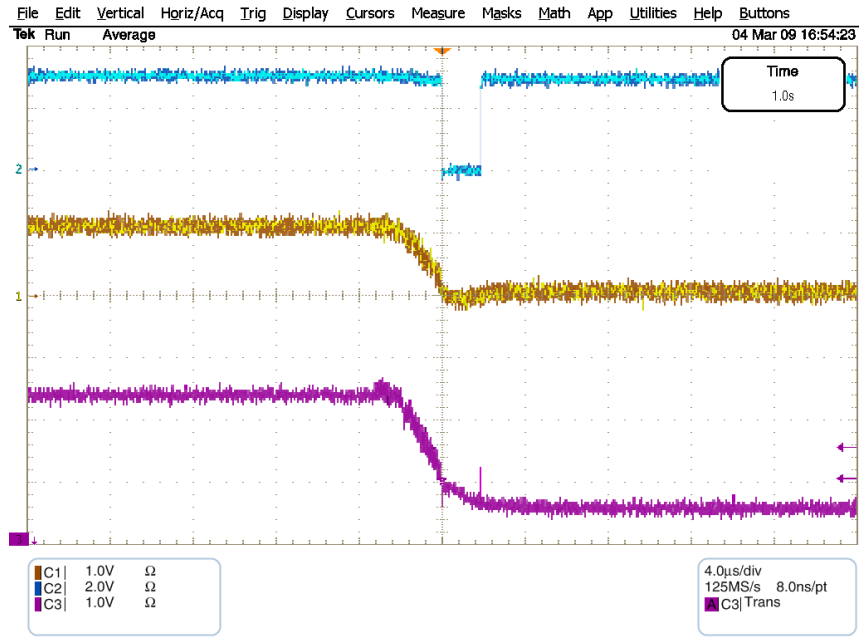


(a)



(b)

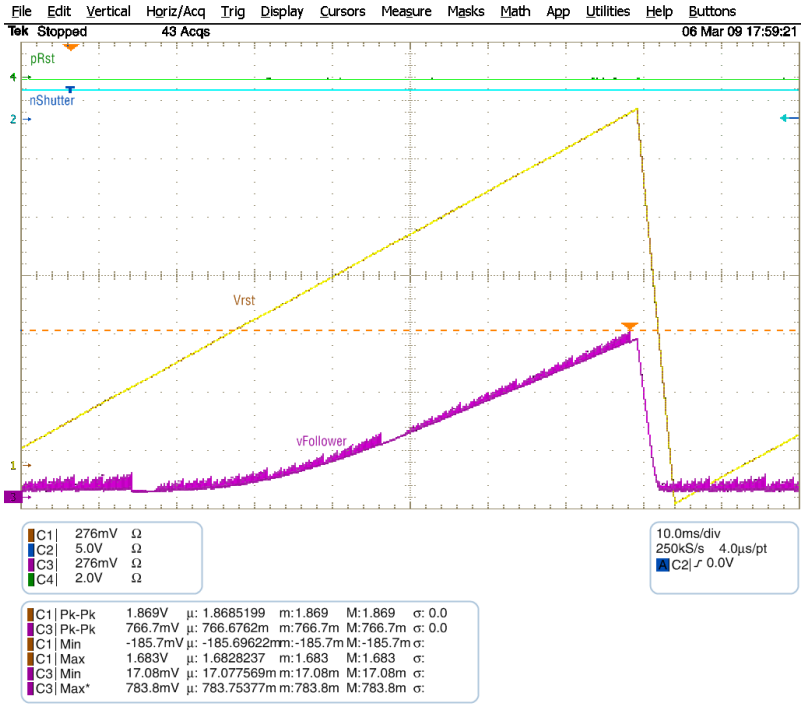
Figure 5.16 Differential Mode Experimental Measurements



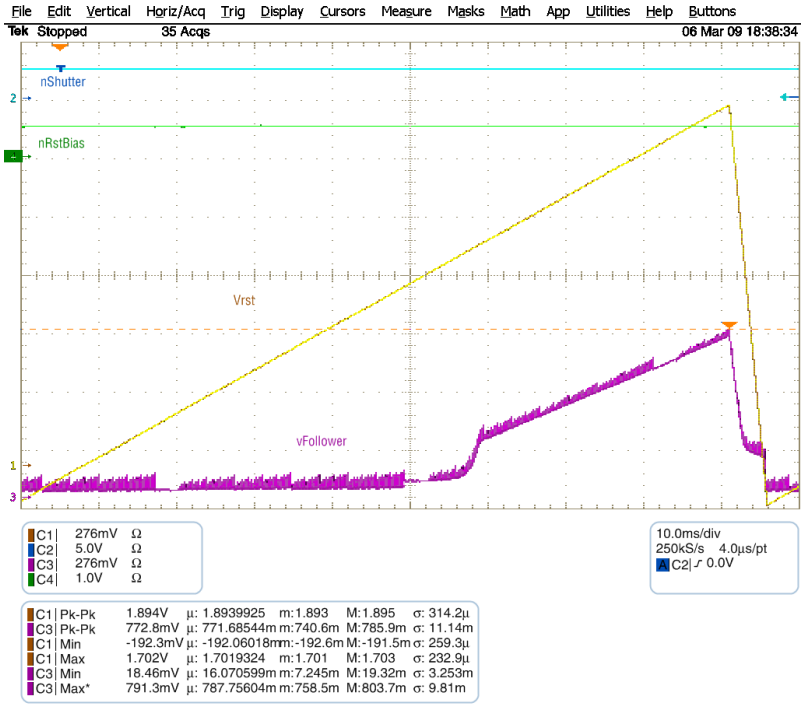
(a) Reset Low

(b) Reset High

Figure 5.17 Experimental Measurements of Follower Voltage on PD Resets



(a) $nRstBias = 0V$



(b) $nRstBias = 500mV$

Figure 5.18 Experimentally Measured Follower Voltage while Ramping the PD Voltage

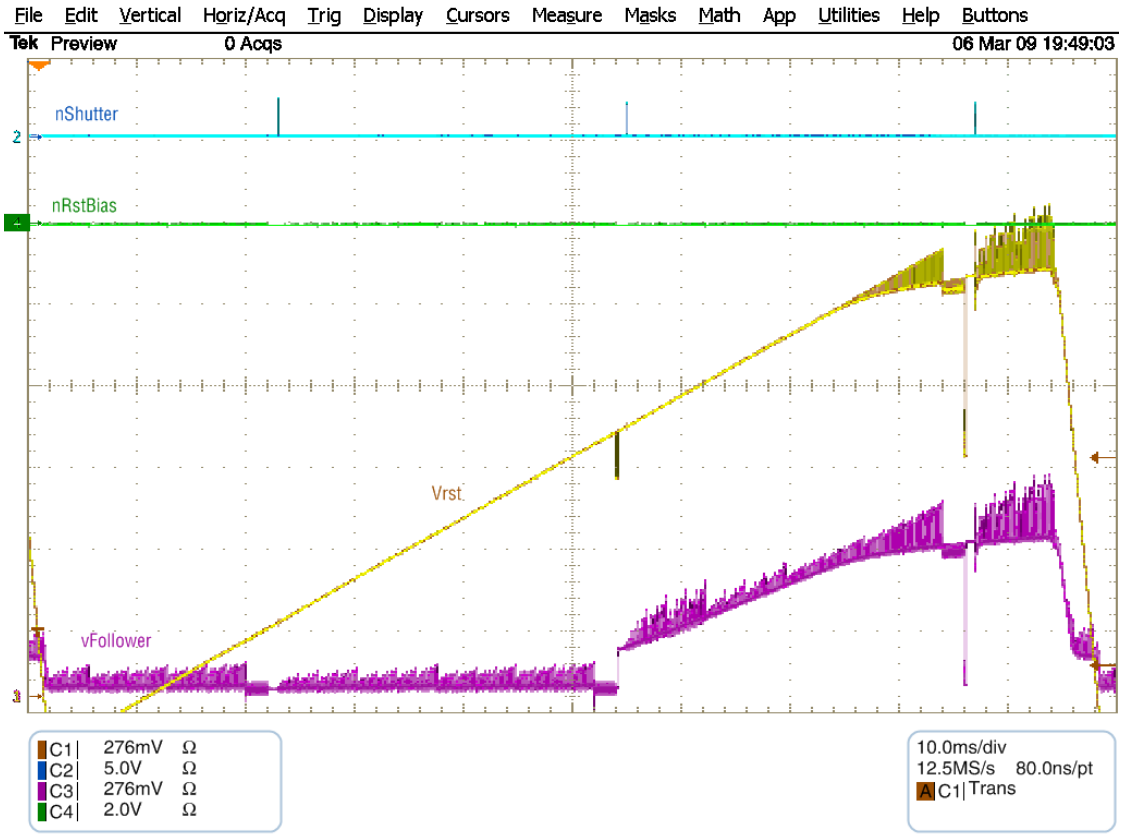


Figure 5.19 Experimentally Measured Follower Voltage with Shutter Activation

5.5.3 Test Setup Validation

The custom-PCB and controller were validated, and were both operating as expected. The details were inspected prior to plugging the chip in its socket to make sure that all the voltages and signals are in the expected range. Figure 5.20 shows that the analog ramp generated by the DAC on the PCB takes on the correct voltages. The digital Most Significant Bit (MSB) supplied by the FPGA controller is also shown in the figure to see the relationship between the analog and the digital counterparts of the ramp.

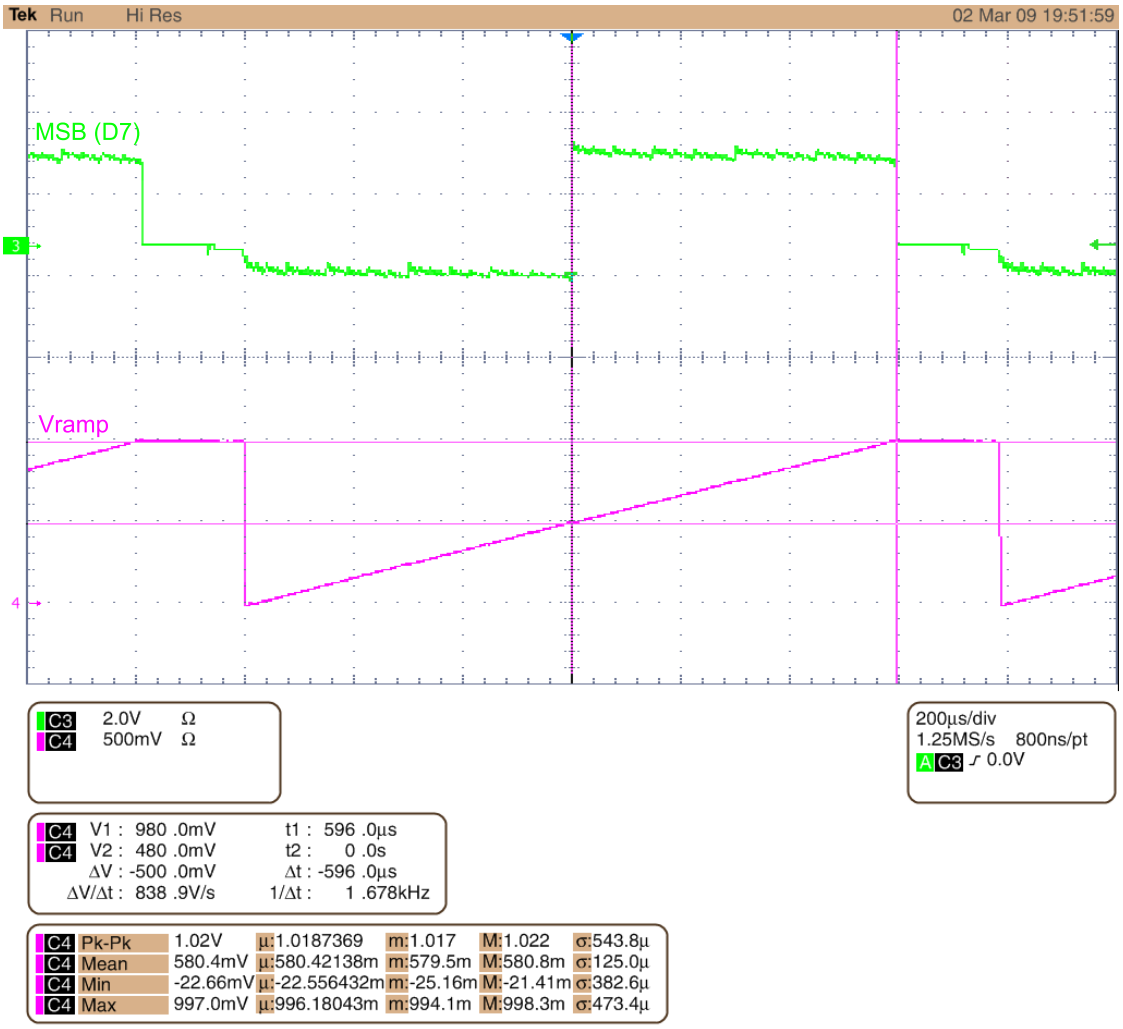


Figure 5.20 Analog Ramp and Digital Ramp MSB Experimental Measurements

The generated clocking signals for the Linear/Logarithmic and Differential Modes

were measured as shown in Figures 5.21(a) and 5.21(b). The PD reset and shutter signals were also measured and checked to have the correct output of 2.5V/0V (Figure 5.22(a) - notice the Exposure Time of 840μs in this case) and the voltage divider circuits were validated (Figure 5.22(b) shows the 3.3V Phi1 output from the FPGA controller which is scaled to a 1V output before being fed to the chip).

The various required supply voltages generated by the regulators on the custom PCB were measured and validated as shown in Figure 5.23(a) and the 120 MHz oscillator that is also part of the custom PCB was tested as well (see Figure 5.23(b)). The output of this oscillator can be fed into the Spartan-3 Development Board to increase the clocking speeds.

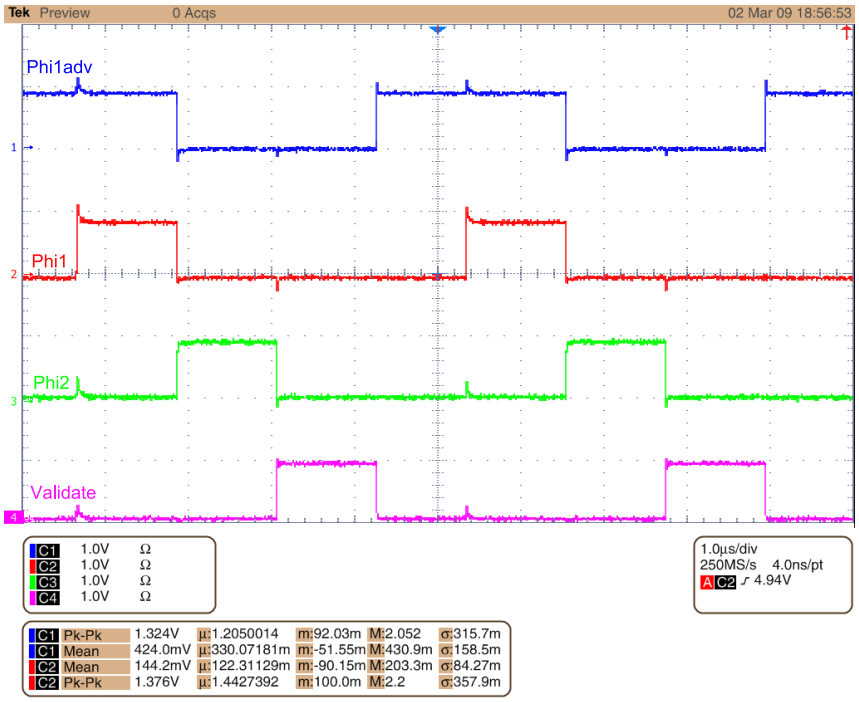
5.6 Experimental Results Discussion

Both simulation and measurement results place emphasis on pros and cons of the design and implementation choices adopted in this Master's thesis. The use of the CMOS 90nm made it possible to scale down the pixel pitch, to integrate more transistors and processing within the pixel, and to achieve a higher capacitance value as compared to the previous prototype designed by our research group increasing the capacitance from around 5fF to around 15fF without having to resort to MiM capacitors that require a special process and prevent the integration of transistors beneath the capacitor. A fill-factor of 26% was also achieved, which is a good value for a 9μm CMOS pixel and which can be easily expanded to over 80% by the use of microlenses. The clocking signals generated by the VHDL controller were also validated and were flexible which allow optimization prior to the next step which is integrating clocking signals on the die. The use of voltage dividers was also proven to be adequate at the required frequency of operation, and the on-PCB oscillator was shown to operate at the required frequency of 120Mhz. The DACs on the PCB were also shown to have been correctly programmed by the digital controller to give the adequate ramp and biasing signals to the chip. The amplification circuit of the pixel was also shown to be working properly by forcing the PD voltage. The effect of applying a bias voltage to prevent shutter leakage was also shown. These also prove that the supply voltages of 2.5V and Ground, PD reset and Bias signals were properly routed to the pixels in the tiled configuration, and that the pads of the chip were properly routed and connected with no shorts.

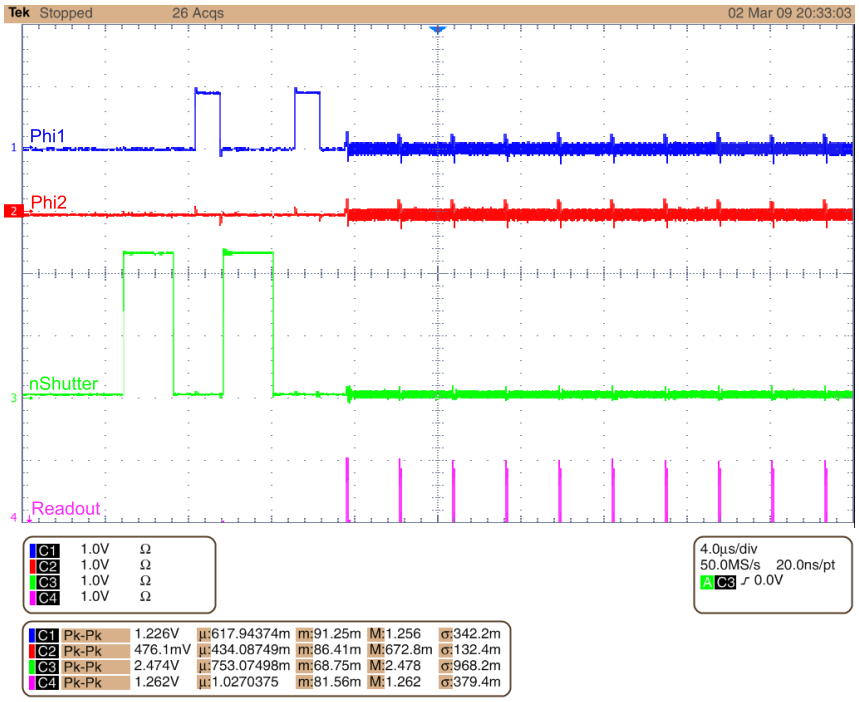
The news were obviously not all great, starting with the response of the PD to light which seems to indicate that a process modification should probably be in line to prevent photocurrent leakage. Leakage could also be pinpointed as a source of the comparator not giving the expected performance. The measured output signal of the comparator was properly oscillating between ground and VDD, which shows that the 1V and Ground supplies were properly routed to the comparator, and that the clocking signals were also reaching the pixels. The compare signal not being properly generated does however suggest that the value is leaking from the capacitor when the clocking transistors are being turned on and off. Another drawback for the characterization is the limited available number of test nodes and test modules which made it very hard to further dissect the circuit - but this was dictated by the limitation in the number of pads forced by the allocated silicon area for the design.

5.7 Conclusion

This chapter discussed the implementation and design issues encountered. It also presented simulation results for the different parts of the system, as well as measurement results when applicable or possible. The chapter was concluded with a discussion of these results. Suggestions for future improvement and criticism of the approaches selected during this Master's Thesis, with some suggestions of better paths to opt for in future endeavours can be found in the concluding chapter. A published IEEE paper [2] also highlights some of the results.

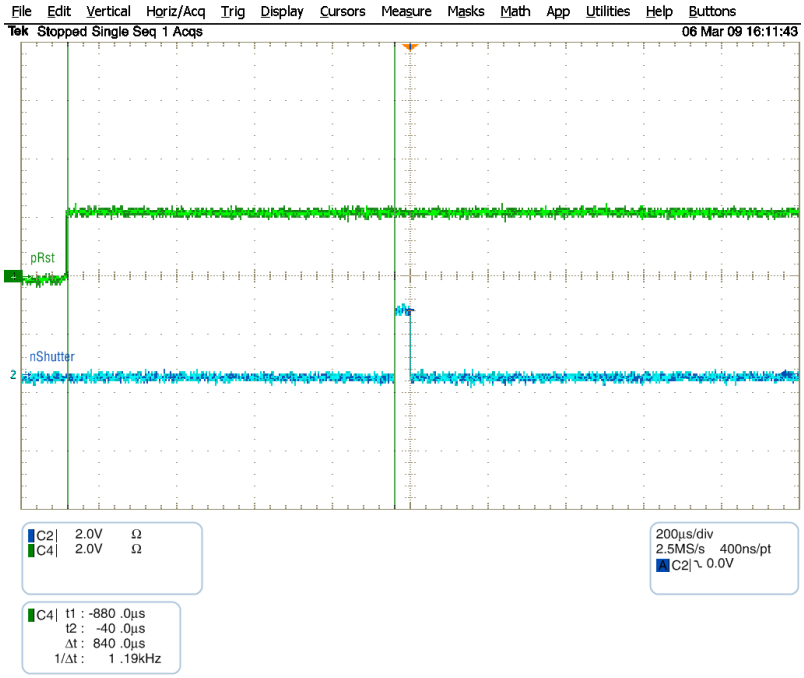


(a) Linear and Logarithmic Modes

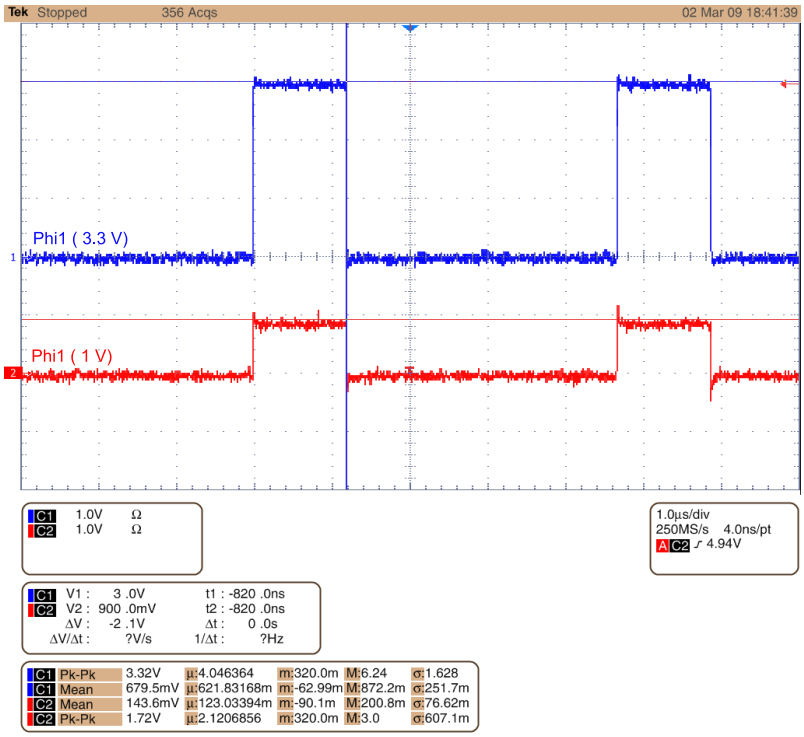


(b) Differential Mode

Figure 5.21 Experimentally Measured Clocking Signals

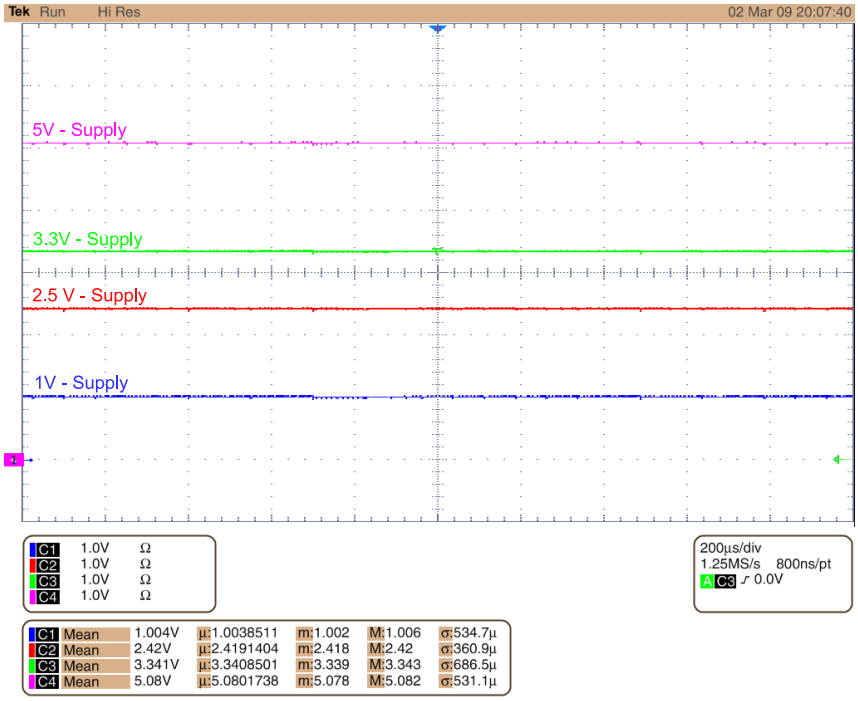


(a) PD Reset and Shutter

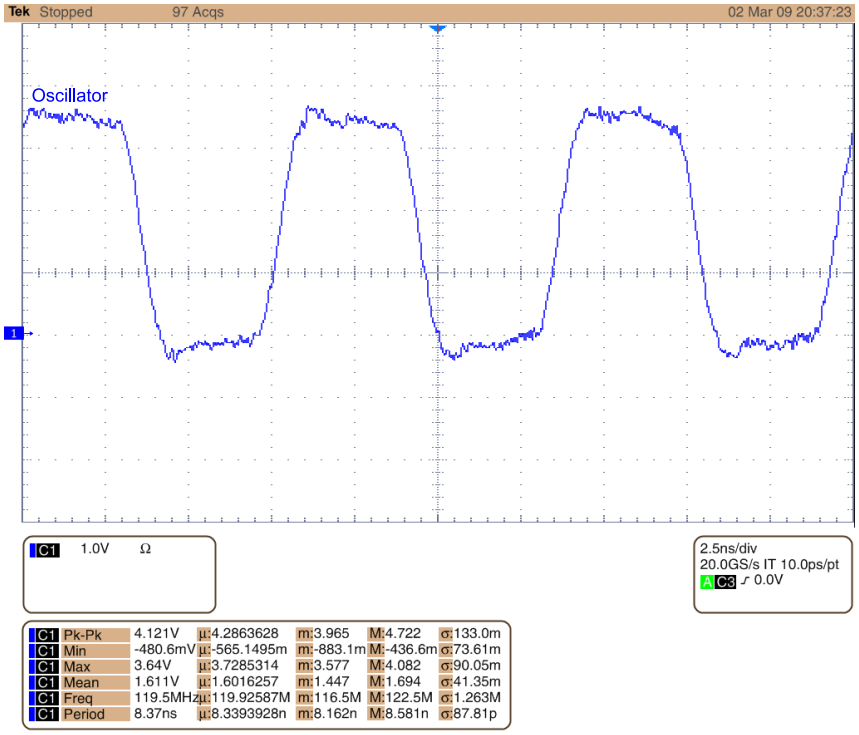


(b) Voltage Divider

Figure 5.22 Experimentally Measured PD Reset, Shutter and Voltage Divider Signals



(a) Supply Voltages



(b) 120 MHz Oscillator

Figure 5.23 Experimentally Measured Supply Voltages and Oscillator Clock

Chapter 6

CONCLUSION

The main aim behind the project of this Master's thesis is to provide the front-end of a system allowing fast and versatile image capture within a compact, flexible, and portable module that is capable of transmitting images at a high rate to an image processing module that would use these to reconstruct an image with a three-dimensional feel. This image would then be sampled and used to electrically stimulate the visual cortex of the patient by currents passing through microelectrodes creating spots of light (phosphenes).

For that, a review of electronic image sensors was performed establishing a comparison between CCD and CMOS ones and concluding that CMOS sensors are better adapted to our application since they allow the integration of custom processing modules on the chip itself which is a very essential point in creating a compact and low-power system. Moreover, CCD sensors basically constitute a large capacitive load, and are more difficult to drive than CMOS sensors. Also, image quality for CMOS sensors has improved over the past decade or so, letting it rival CCD sensors for many applications. CMOS sensors also allow for higher acquisition rates since they have on-chip ADCs, and they deliver a digital output as compared to an analog output for CCD sensors. Moreover, the CMOS manufacturing process is less expensive and is readily available to us via the CMC and ST Microelectronics. The CMOS process also lends itself to easy array size expansion and windowing. It is easy to read out part of the pixel matrix and dump or ignore the rest of the data without having to accommodate a high data bandwidth.

The design of the sensor paid careful attention to the capture of good quality images at a high frame rate so as not to constitute a bottle-neck for the 3D image processing. This included designing an ADC with a well-defined precision while operating at higher frequencies. The implemented camera also allows the user to select between a linear integration mode and a logarithmic mode of operation. The linear mode is favored for operating conditions that require good image quality (lesser noise)

at the cost of a reduced frame rate. The logarithmic mode has an edge for scenes that have both very dark and very bright elements because of the increase in DR at the expense of non-linearity and increase in noise. This mode does however, allow the operation at higher frame rates because the integration time is not required (the pixel is always active and does not need to be reset). The linear integration mode also gives the user the option of multiple exposures which increase the DR at the expense of a decrease in frame rate. Another mode available is the differential mode which speeds up the 3D image processing since it subtracts two consecutive images and outputs a binary image (pixels are either black or white). Basically, a light pattern is projected on the scene followed by its inverse. The image sensor subtracts the two acquired images, and the resulting image is read out of the sensor. This mode operates at a much higher speed since the comparator needs to compare two values only (versus comparing the output of the pixel to 256 values of a digital ramp for an 8-bit output). All the timings are user configurable by properly setting timings signals.

As for the design of the sensor, a DPS architecture was privileged over an APS. The difference between the two is that the former integrates an ADC (basically a comparator) within the pixel, while the latter has a single ADC common to all pixels. The advantage of the DPS is that the A/D conversion is done in parallel inside the pixels allowing higher frame rates; nevertheless, this comes at the expense of a decrease in fill-factor (since the pixel has more circuitry) and any attempt at increasing the fill-factor would lead to a larger pixel pitch. Also, the process variations would lead to more differences between the pixels, which would increase spatial noise. The increase in the size of the pixel matrix, however, would not affect the DPS as much as an APS. Moreover, a DPS lends itself well to a multi-tap readout scheme since the value that is read out of the pixel is already digital. This also prevents the degradation of reading out analog values from the pixel, which could also be affected by increasing the size of the pixel matrix: it is basically harder to have erroneous values read out of the pixel if its output is digital than if its output is analog.

For the DPS, the circuit of each pixel comprises a PD, an amplifier (a follower), an ADC, and an 8-bit memory. The in-pixel memory makes it easy to use windowing or to read out random pixels especially if coupled with a decoder pixel selection architecture that could allow reading out pixels in random order and without having to be concerned as much about losing the value since digital values are easier to retain than analog ones. This is particularly true for the memory architecture used

in this case which is a refreshable one. The disadvantage of that is the increase number of transistors required for this implementation. This was, however, deemed mandatory during the design because of the leakage of the stored value in CMOS 90nm for a 3T-memory architecture. Each pixel is made up of 57 transistors (40 of them being required for the memory - an obvious overhead). The use of the CMOS 90nm technology does, however, make integrating more pixels in the same area possible. The optimized pixel pitch is of 9μm with a Fill-Factor of 26%. The circuit area (excluding the pads) is of around 603μm x 477μm for a 64x48 pixel matrix. Notice that the increase in number of pixels is due to the memory architecture. The remainder of the circuit actually uses fewer transistors. A method was also introduced to prevent shutter leakage, but at the cost of a decrease in the linearity of the system. To try and circumvent the lack of precision of the ADC in the previous prototype of our group, the additional number of available layers in the CMOS 90nm technology was exploited to have a greater capacitance for a given surface area. An alternative differential-input architecture for the ADC was also tackled; however, simulations tipped the balance towards the switched-capacitor architecture which showed a better offset. In addition to that, trying to adapt the differential mode of operation of the sensor to the differential-input comparator required adding a capacitor for storage, which relinquished the gain in area overhead. On a different note, the supply voltages were changed from 1.8V/3.3V to 1V/2.5V which would be advantageous for power consumption. The following table also based on a published IEEE paper [2] briefly compares this work to a previous work by our group.

	Previous Work	This Work
Technology	0.18μm CMOS	90nm CMOS
Pixel size	16μmx16μm	9μmx9μm
Fill factor	22 %	26 %
Transistors/pixel	44	57
ADC resolution	8 bits	8 bits
Supply voltages	1.8V and 3.3V	1V and 2.5V
Dynamic range	$>$ 88 dB	$>$ 83 dB
Number of Pixels	90 x 45	64 x 48
Circuit Area	1520μm x 780μm	603μm x 477μm

A prototype chip was fabricated having a matrix of 64x48 pixels using ST Mi-

croelectronic's CMOS 90nm process. A test module was added to characterize the pixel. The original design featured a decoder and multiplexer to select the pixels to be read out. This design was trade in for another based on shift registers because of the limited number of input pads available to the chip resulting from the allocated area on the wafer. This limited numbers of I/Os has also forced a limitation on the number of test modules and probing nodes.

To validate the system, tests on the chip were performed using a test setup consisting of a custom PCB designed and manufactured for that purpose; a digital controller implemented using VHDL in a Xilinx Spartan-3 that interfaces the custom-PCB, and a logic analyzer to capture the digital outputs of the chip. The PCB is powered by an adaptor that plugs into a wall socket. This adapter is connected to various voltage regulators that generate all the required voltages and feeds them into the image sensor chip and the other discrete components on the board. The PCB also has voltage dividers that lower the Spartan-3 outputs from 3.3V/0V to 1V/0V or 2.5V/0V when required. It also has voltage DACs to supply the required biasing voltages to the chip (PD reset voltage), and the analog ramp/digital ramp. And a current DAC supplies the current bias to the chip. Note that all these DACs are initialized and controlled by the FPGA. Their operation was validated at the required frequency of operation and coincided with the expectations of this flexible design/implementation.

Finally, suggestions for future work and considerations can be put forward to avoid reenacting the same issues. Some of these are highlighted in the list hereafter.

- **Choice of Technology -** Scaling the technology of image sensors to 90nm makes process modification an important aspect to consider to achieve the required performance. An important suggestion is to consider a photonics process to implement the prototype - even though it might be slightly more expensive. PPDs would be an interesting option to adopt. They present, in general, lower leakage, offer better blue response for colour imagers, and better performance when it comes to image lag and ghosting.

- **Pixel Sharing -** One interesting method for reducing silicon area is to reuse some of the components in the pixel and to share them between the pixels. Some transistors can be shared, or even capacitors. This could, however, affect the speed of operation.

- **Incremental Approach -** An incremental approach is strongly suggested

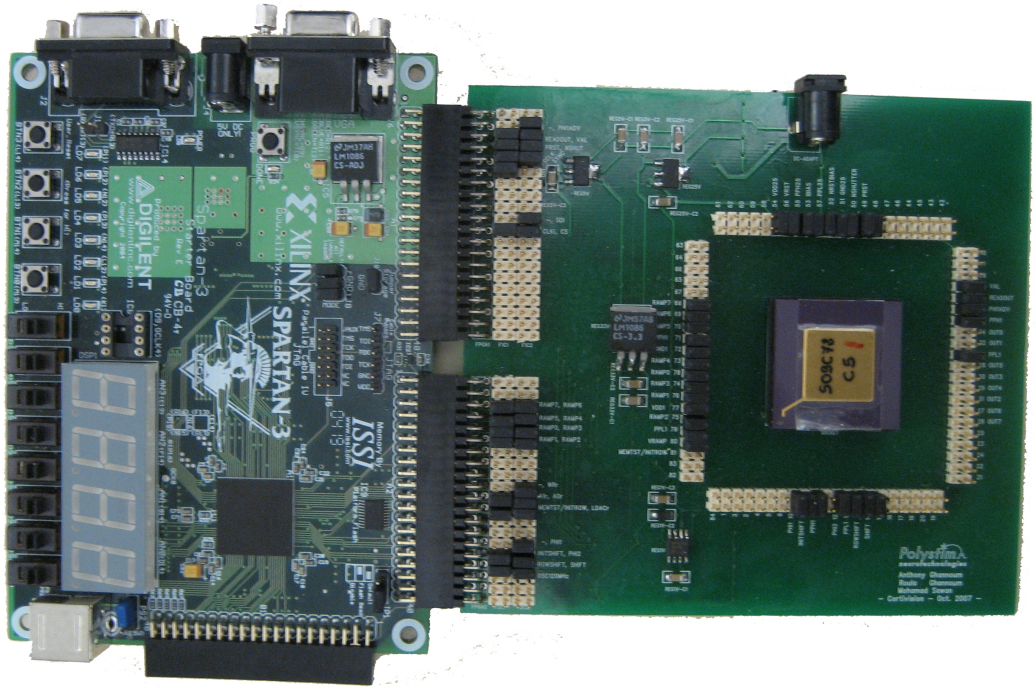


Figure 6.1 Custom PCB Interfaced with Spartan-3 Development Board

starting with several separate and different pixel modules to validate the functionality before attacking a complete system approach.

- **MiM-Capacitors -** Replacing the in-pixel capacitor by a MiM-Cap would have a negative effect on the overall pixel pitch (since no circuitry could be integrated below it), but it would help out with the leakage for newer technologies. It would also decrease the capacitance mismatch between pixels, and hence improve spatial noise (mainly FPN).

- **Differential Mode -** Implementing the differential mode digitally outside the sensor chip would waive the requirement for an in-pixel capacitor. This would decrease the pixel area, and the FPN - giving an improved image quality. The downside to such an implementation, would however be a reduced frame rate. A counter-argument to that could be that such a subtraction could be implemented in parallel with the readout or in parallel for all pixels, which would not have a significantly detrimental impact on speed. A requirement for additional memory on the PCB would however be created.

- **Microlenses -** For smaller pixel sizes, the sensitivity of the image sensor is degraded. One widely employed method is the deposition of microlenses on the pixels to focus the incident light on the photosensitive area. This would however, require a special process, which is more expensive, and the difference between one microlens and the other would again degrade the quality of the image by increasing spatial noise.

- **Integrated Clocking and Biasing -** Clocking, biasing and the analog ramp should eventually be generated on the sensor chip. This would further reduce the size of the system. However, this is *strongly not recommended* prior to validating the adequate operation of the remaining modules.

- **Test Modules and Test Driven Design -** More space should be allocated for test modules, and a greater variety of modules should be implemented to compare alternatives. Moreover, a test-driven design approach should be favoured, adding probe signals to several paths. These would both help in probing and could be sometimes useful in adjusting the operation of the chip by varying the capacitance at some nodes. Two of the hindrances to this are the available silicon area and possible number of pads (or I/Os) - which should also be taken into account in the earlier design stages.

- **Binning -** An option to increase the sensitivity is by binning pixels. This means that the output of several pixels would be combined to form a "single" pixel. This would of course reduce the resolution of image sensor. If a DPS architecture is maintained, digital binning would be the only option and should be performed by an FPGA. If the DPS architecture is traded in for an APS one, some kind of analog binning could be achieved.

- **Flat-Field Correction -** CMOS cameras suffer from considerable spatial noise. This would be detrimental for any image processing required by the Cortivision application which would probably involve edge detection. One way to improve the image quality is by applying a Flat-Field Correction to the image. This means having separate memories with stored offset and gain coefficients for each pixel. This correction would be digital and would influence the frame rate. The coefficients should also be calculated using bright and dark test images and on per-sensor basis.

- **Colour Integration -** Some image processing algorithms could take advantage of colour images. The Cortivision application, at this point, makes use of an infrared light projector and the sensor should capture infrared images. If, for some reason, the image processing part is modified to require two sensors instead of a projector-sensor system, adding colour support could have advantages. This would require depositing colour filters on the pixels and special considerations for reading out the colours and for balancing them. This topic will not be delved into any further.

- **Bit Resolution -** The current system is limited to 8-bits since the in-pixel comparator in the DPS architecture is limited to 8-bits. Increasing the resolution further in a DPS architecture is not a foreseeable option since the comparator needs to be integrated inside each pixel. If a precision higher than 8-bits is required, the architecture would have to be migrated to an APS one that has a single ADC per tap. This would allow a better ADC architecture. The FPGA could then decide whether to transmit the whole bit-resolution of the sensor or to truncate some of the LSBs (Least Significant Bits) for higher frame rates.

- **Multi-Tap Approach -** A method to increase the frame rate even further would be implementing a multi-tap approach to be able to read out several pixels in parallel from the sensor. This could, nevertheless, introduce an artifact since the taps are different (e.g. odd/even discrepancy for a two-tap approach) which might require correction or compensation.

The final design should be a SoC with the image sensor, image processing, and external electrode control circuitry, hoping to have a fully-functional SoC that would help us achieve our ultimate goal that has driven the whole Cortivision project: helping blind patients see.

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Appendix A

Layout Implementation Details and Considerations

A.1 Schematic Implementation

The schematics were drawn based on the architectures described in Chapter 4. Simulations were conducted, and transistor sizes were optimized to obtain an adequate response, decrease the offset of the comparator, make sure the memory is able to store a value for an appropriate length of time, and that the values can be shifted out of the pixels. For the sake of brevity, schematic simulations will not be reproduced in this document. Simulations will be limited to Post-Layout ones that are deemed more substantial and that better reflect reality and parasitics.

A.2 Verilog and Verilog-A Implementation

The digital clocking sequences were implemented in Verilog. This allowed us to integrate both the external controller and the ASIC in our simulations. So we mainly had a "black box" coded in Verilog that supplied clocking voltages to another "box" which is the ASIC. Figure A.1 shows an example of a mixed simulation which includes a component that generates the clocking signals in the upper-left corner with a reset signal and a clock as inputs, inverters implemented in Verilog-A to change the clocking voltages to the required values by our schematic, and the schematic.

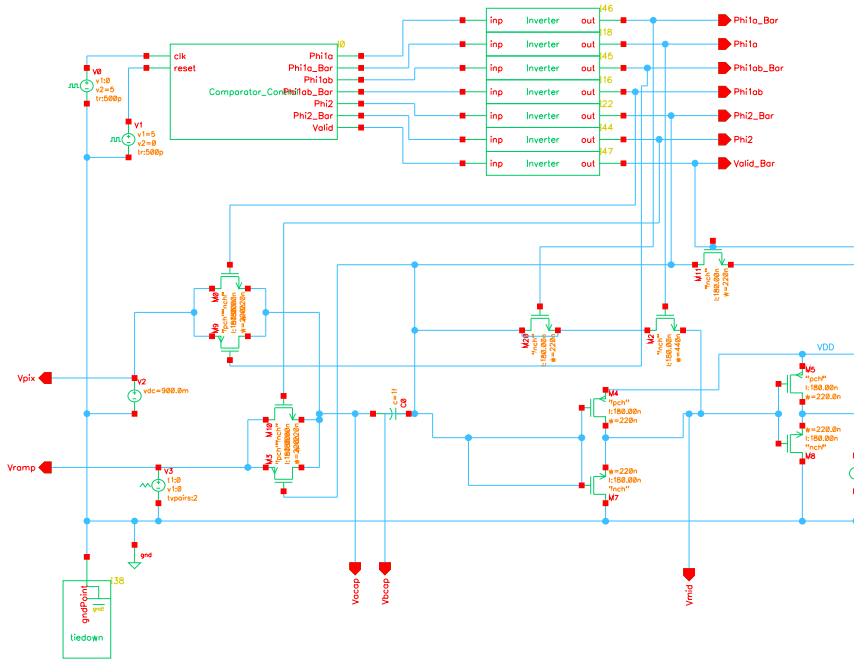


Figure A.1 Example of Mixed Simulation: Verilog, Verilog-A, Schematic

A.3 Layout Implementation, Issues and Considerations

The layout was optimized to be compact and to avoid unnecessary spaces, while still satisfying DRC rules and having an optimal pixel-tiling ability. Several issues arose and several considerations were taken into account while doing the layout of the chip. These will be detailed in the following discussion. Minimal dimensions and optimal layout are key for image sensor design to get reduced pixel sizes.

A.3.1 Minimum Well Spacing

Another thing that became an issue was the design rules forcing a minimum spacing between N-Wells. This spacing was even more substantial for thick-oxide transistor

wells. The design had to be carefully manipulated so that tiling the pixels next to each other did not create any Design Rule Check (DRC) violations. Moreover, since the 3T NMOS per-pixel memory was traded in for a simpler (but more transistor-hungry) architecture because of leakage in CMOS 90nm, the memory implementation required PMOS transistors. This made it quite challenging to be able to place the Photodiode well, thick oxide reset PMOS transistor well, and memory PMOS transistors wells in a smart configuration to minimize the size of the pixel while still avoiding having unused space between the pixels. Figure A.2 shows the layout for a single pixel.

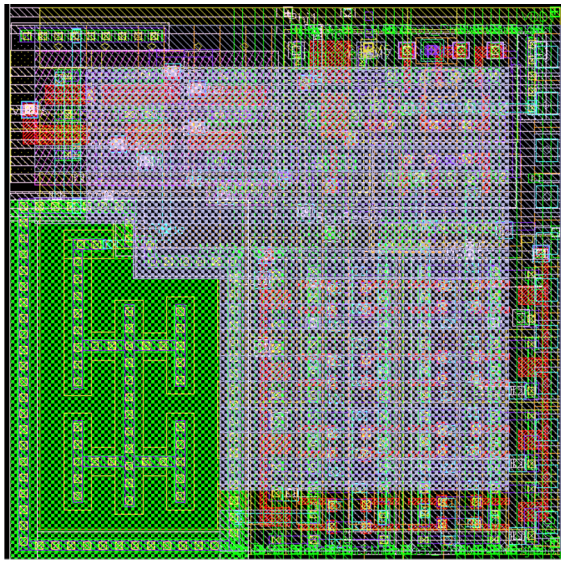


Figure A.2 Pixel Layout

A.3.2 Pixel Signals Routing

Each pixel requires a substantial amount of clocking signals to be routed in, not to mention supply voltages (2.5V, 1V and Ground), as well as requiring data buses to be routed in (Digital Ramp) and out (Memory Content Readout). Manually routing pixels one by one is cumbersome, and next to impossible with the exponential increase in the size of the matrix with the increase in resolution. To avoid that, the pixel layout was carefully designed so that the signal wires passing through the array would be connected simply by aligning the pixels next to each other. This made it possible to increase the array size simply by creating an array of these cells without having to worry about a connection overhead. Figure A.3 shows a matrix of 2x2 pixels.

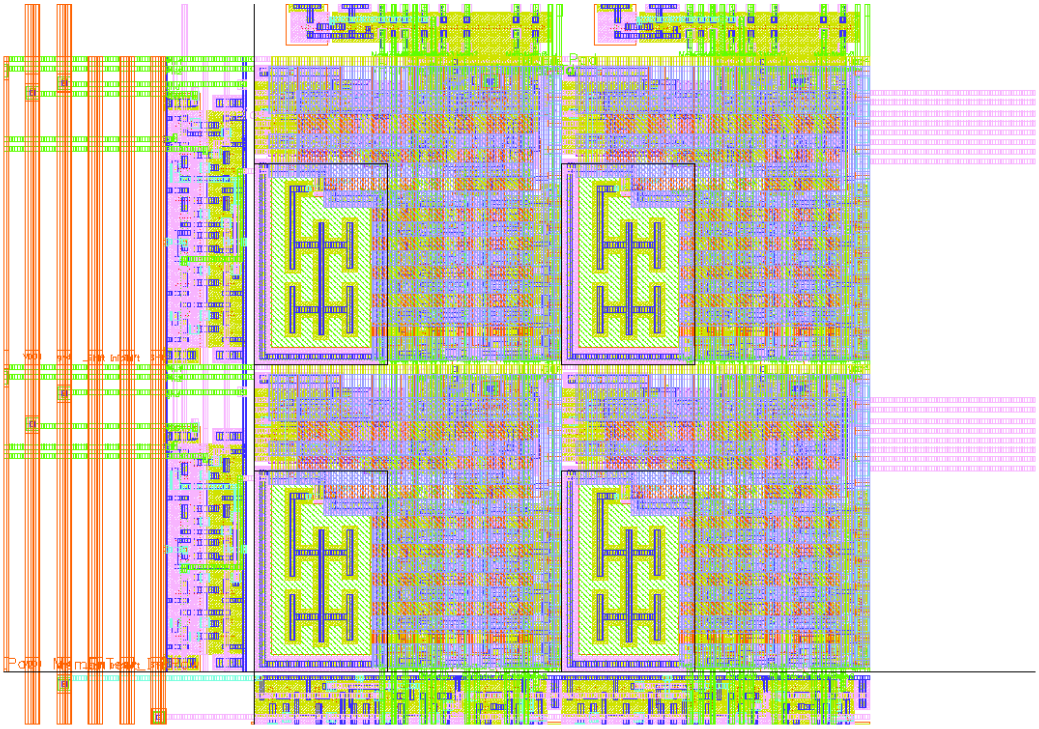


Figure A.3 2x2 Pixel Matrix Layout

A.3.3 Capacitance

Several Metal-Metal capacitor architectures have been put forth. Sowlati et al. describe, implement and compare some of these architectures [137]. Table A.1 summarizes their findings.

Taking these into consideration, alongside with the available area and metal layers, to select the optimal capacitor configuration for the space at hand, several architectures were implemented in layout, extracted, and compared. Table A.2 shows the results of that comparison.

For our application, the use of so many layers is not possible because we would no longer be able to add transistors underneath and route signals. Our technology of choice being the CMOS 90nm technology, seven metal layers are offered. Layers M1 and M2 were used for connecting the pixel circuit. Layer M3 and M4 were used to route the signal in and out of the pixel. This left us with layers M5 through M7 to

Table A.1 Capacitance Densities with Various Architectures [137]

Architecture	$0.25\mu m$ Extracted	$0.25\mu m$ Measured	$0.18\mu m$ Extracted	$0.18\mu m$ Measured
Metal-Sandwich	0.15	0.18	0.22	0.22
Pillar Stripe	0.5	0.44	0.69	0.66
Ring	0.46	0.4	0.71	0.63
IM	0.34	0.33	0.55	0.55
Horseshoe	0.53	0.38	0.69	0.52
IMS	0.42	0.33	0.59	0.5

Table A.2 Capacitance Extraction Simulation Results $Area = 20\mu m \times 20\mu m = 400\mu m^2$

Capacitance Type	Capacitance	Capacitance Density
Parallel Plates	$18.4fF$	$0.0471fF/\mu m^2$
Comb	$101.79fF$	$0.2545fF/\mu m^2$
Comb with Vias	$95.84fF$	$0.2396fF/\mu m^2$

be used to form a capacitor.

Layer M5 was used as a plate to decrease the influence on the circuitry underneath and was connected to the less sensitive node to decrease the effect of parasitics, while layers M6 and M7 were divided into alternating fingers to increase the capacitance density. This allowed us to achieve an extracted capacitance of around $14.9fF$ for a total area of around $60\mu m^2$ which boils down to a capacitance density of $0.25fF/\mu m^2$. The actual metal area is $27.5\mu m^2$ with a perimeter of $203.48\mu m$.

A.3.4 Buffers

Buffers were added to each column bus to make sure that the contents of the memories read out from the pixels are turned into valid digital values before reaching the shift register to be shifted out of the image sensor chip. Buffers were also added to the column buses to connect them or disconnect them from each other and from the 8-bit digital ramp input to the chip.

A.3.5 Shift Registers

Shift registers are used to shift out the frame pixel by pixel out of the image sensor. The shift register has a length equal to that of a row of the pixel matrix and readout is performed by loading a new row (all the pixels simultaneously) in the register and then shifting out the pixels one by one; followed by another row and so on.

Figure A.4 shows a representative subcircuit of the chip combining pixels, shift registers, and buffers.

A.3.6 Chip Area and Number of Pads

The silicon area attributed by CMC was limited to $1.0mm^2$. This did not hinder us in the design itself, but it did lead to issues due to the high number of required inputs to and outputs from the chip. The CMOS 90nm technology itself (with the CMC design rules) requires a maximum spacing between VDD and Ground pads that are required for both supply of the core, and of the ring. This not to mention the required ESD Clamps. So basically, insufficient available pads became an issue. To try and circumvent that, the initial architecture that used a decoder to select the row of the pixel matrix to be read out was traded in for a shift register - which requires less inputs. Moreover, signals that required their complements to be input as well were inverted on-chip. Also, the inputs and outputs of the Test Module were multiplexed with other signals - reuse being the only option. This did also have an adverse effect on the number of possible Test Modules in our chip (which ended up having to be limited to a single one) and to the number of signals that can be used to probe the different nodes of that test module - which also had to be limited to the bare minimum. Figure A.5 shows the layout of the complete chip with the pads.

A.4 Test Module

Due to the lack of chip area, and the resulting reduced number of available pads, the number of test modules in this chip was limited to a single entity whose signals had to be superimposed with other signals with two pertinent signals representing $V_{FOLLOWER}$ and $MemEn$. The former can be used as an output to see if the photo-sensing circuit is operating properly or as an input to control one of the comparator's inputs. The latter probe, $MemEn$, can only be used as an output to verify the op-

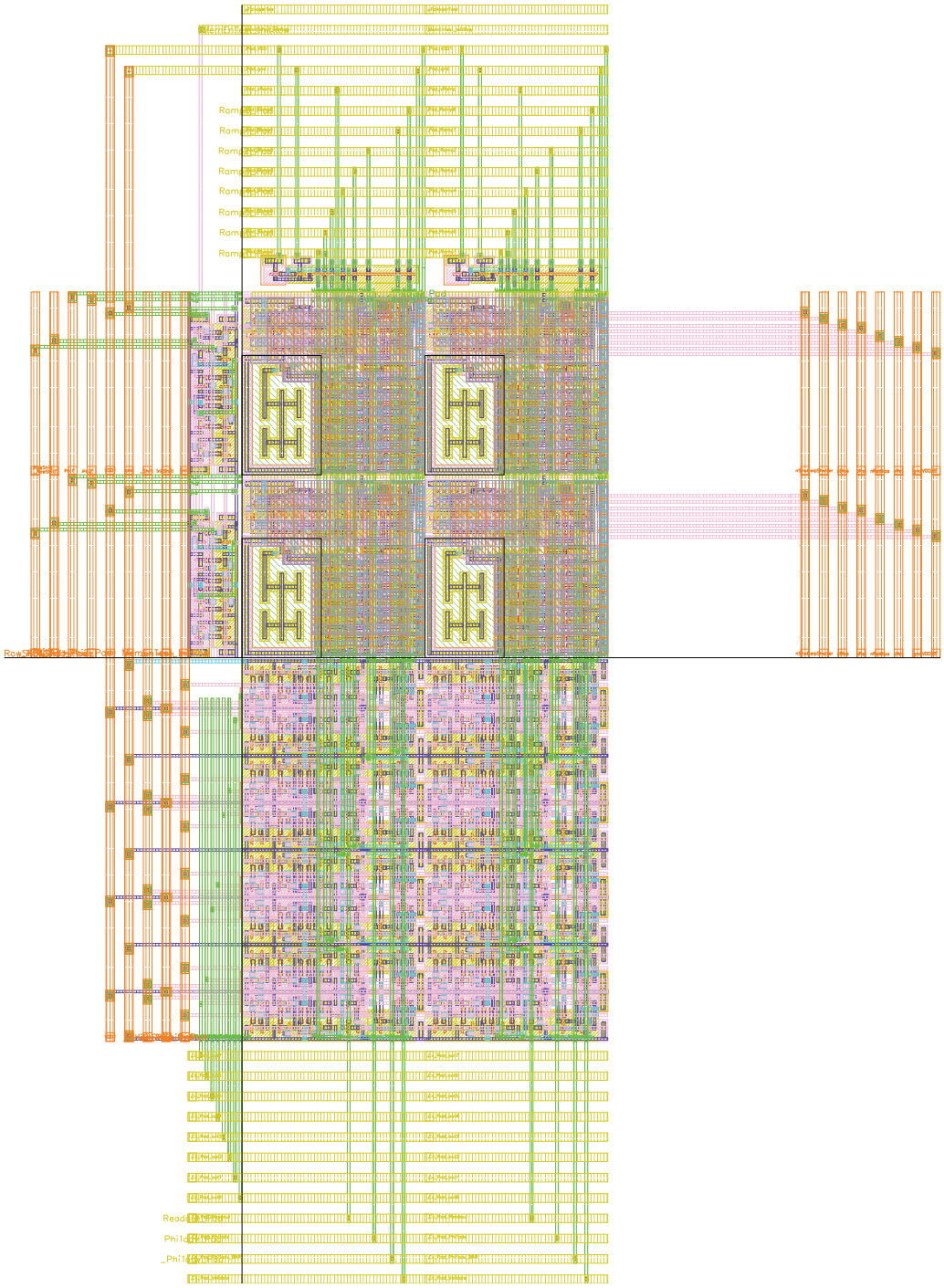


Figure A.4 Representative Circuit Layout

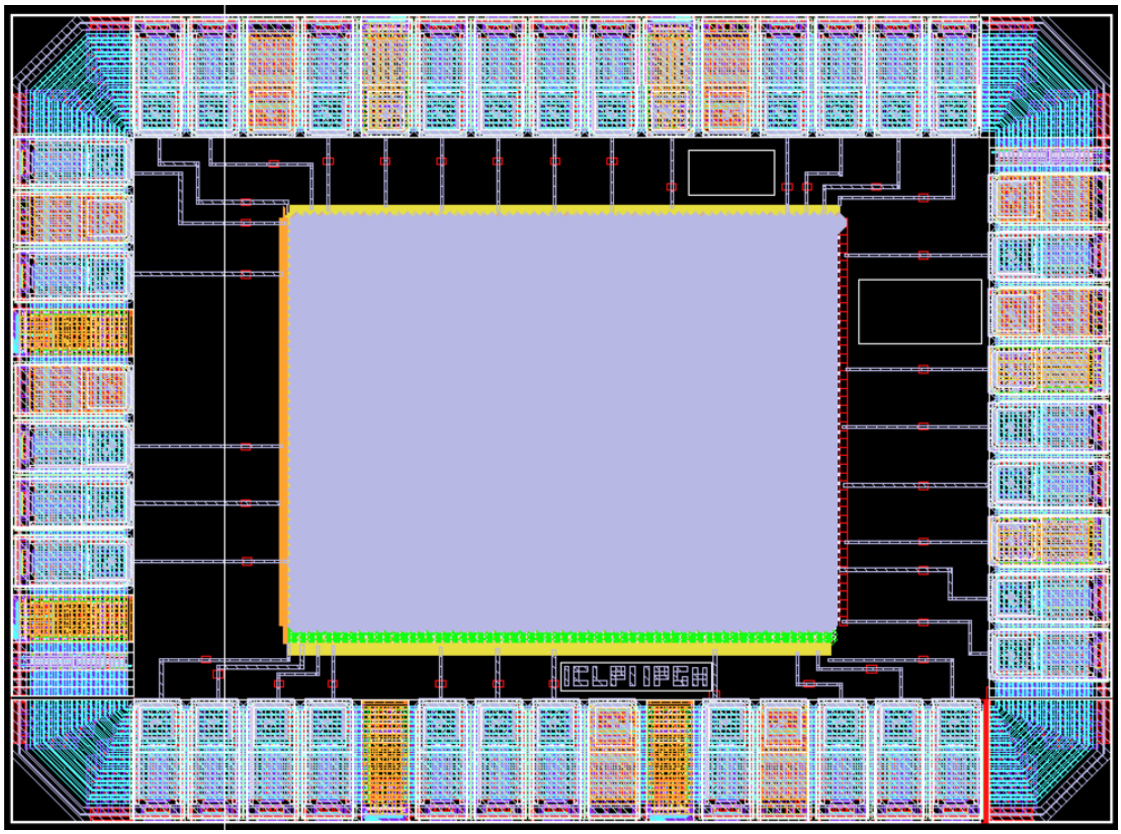


Figure A.5 Chip with Pads

eration of the comparator. The clocking signal and supply voltages are shared with the rest of the chip and pixels.

A.5 Other Layout Details and Considerations

LVS was conducted on a pixel-level and on a representative part of matrix, and then on the whole matrix. The photodiodes, however, were not considered in this LVS. The parameters had to be changed for the LVS to successfully pass. Moreover, since the layout process was aimed at having the highest capacitance possible for the capacitor in the comparator, the final value of the capacitance was determined by extracting the layout, and the schematic was then updated with this value prior to reconducting the LVS. DRC was successfully conducted using Calibre on our local Cadence copies, as well as on the CMC's server. Antennae errors were generated by the DRC on the

CMC server. To deal with that, diodes were added between the metal wires and the substrate.

The CMOS 90nm process offered by the CMC also covers the whole chip by "tiles". If this is not explicitly specified, the photodiode will end up being covered, and hence light will not be able to reach the photosensitive element. To avoid that, the photodiode area of the pixel is covered by a layer called "Tile Not" during the design phase.

Appendix B

External Controller

Since the chip requires external clocking signals and biasing, a PCB is required. The external controller was designed to be flexible and to accommodate this chip and give enough leeway to be reused in any eventual designs using similar packages of an image sensor chip or of any other chip with the same package that requires external control.

The external controller comprises several modules: an FPGA board to supply the digital clocking signals, and a custom-made PCB to supply biasing, analog, and power signals alongside with any other required nuances, and a computer to visualize the output of the chip.

This, however, does pertain to an ideal case. In reality, several intermediate strategies were devised. A logic analyzer was used to supply and to probe signals, as well as an oscilloscope, a ramp generator, and a frequency generator.

The ideal setup aimed at is shown in Figure B.1.

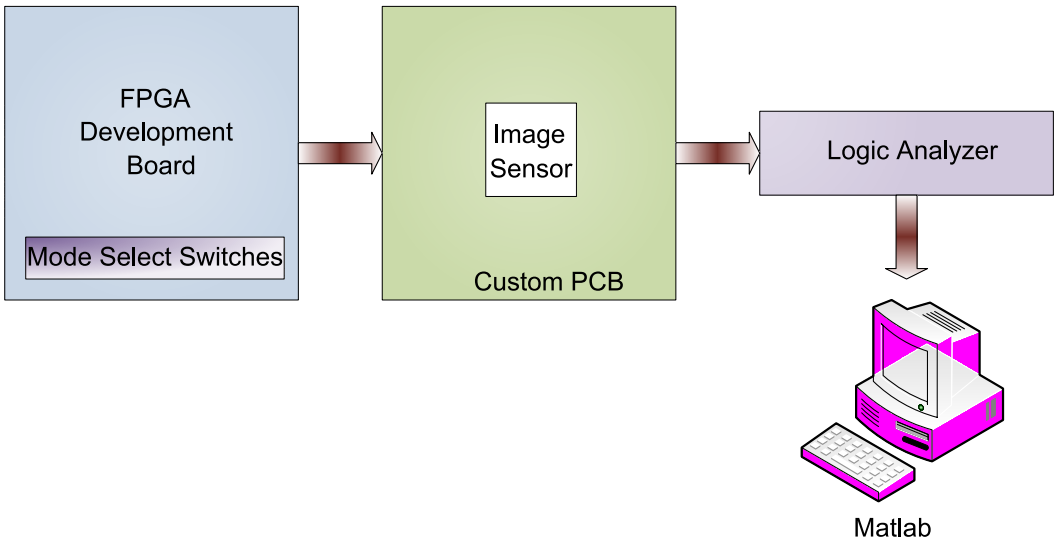


Figure B.1 Ideal Overall Test Setup

B.1 Custom PCB

One of the main goals behind the design of this PCB was to make it flexible and reusable. This was achieved by connecting it to a reprogrammable FPGA board, and by adding jumpers on the board to manage connections.

The PCB comprises a socket for the sensor chip, connectors that plug directly into the FPGA board that is the topic of Section B.2, a connector to draw power from a wall supply (instead of having to use a DC power supply), voltage dividers, DACs to supply reference voltages and biasing currents to the chip, and of course plenty of pins to probe intermediate and final signals leading to a chip socket corresponding to an 84-PGA package. A 120 MHz Oscillator (3HM57) is also added that can be input to the FPGA and whose frequency can very easily be reduced in VHDL.

B.1.1 Power Supply

The image sensor chip in itself requires several supply voltages, and the other chips required on the PCB necessitate even more supply voltages. To avoid having to use several DC power supplies - which can be both cumbersome and impractical, an AC adaptor plug was added to the PCB that is connected to a voltage regulator (LM2937-5V) that would supply 5V to the entire PCB. This voltage would go to voltage regulators on the chip that would supply the remaining voltage levels to the different modules. LM2937-2PT5 is a voltage regulator that supplies 2.5V, LP3879 supplies the 1V required by the image sensor chip, and LM1086-33 the 3.3V required by other chips on the PCB.

B.1.2 Ramp Generator DAC

The image sensor requires an analog ramp signal alongside with its 8-bit digital equivalent to be input to it. To achieve that, the FPGA module generates the digital values that are input both to the image sensor chip and to a DAC. A high-speed parallel input DAC from Analog Devices (AD7305) is used to convert the digital 256 counter to an analog value. The parallel input structure was chosen instead of a serial input one to reduce the lag between the digital and the analog inputs to the image sensor.

B.1.3 Voltage Reference DAC

A DAC from National Instruments (DAC084S085) was selected, having an 8-bit precision . This DAC also has several outputs that can be programmed ONCE and kept the same, so it can be used to supply several reference signals. It is used to supply both the V_RST signal that is used to set the reset voltage of the PDs and n_{BIAS} signal that controls the n-transistor connected to the PD. This DAC, however, uses serial input (the value of the biases is ideally not supposed to vary for a single mode of operation, so in that way we can save on the number of signals required. Of course, the design of the controller would be more complicated, and the setup time would be greater, but the number of required pins would be less. This is an architecture that we can afford in this case.

B.1.4 Current DAC

A biasing current is also required by the image sensor. The easiest way of controlling that is by using a current DAC to generate this value. The value of the current would be programmed in VHDL and the corresponding value would be fed into the chip. A current DAC from Analog Devices (AD5543) was chosen. This DAC has a serial-input structure; this is tolerable since the biasing current is not required to change during a specific mode of operation, but what drove to the selection of this part in particular was its ability to supply the low current values required by our application. This DAC has a 16-bit precision.

B.1.5 Voltage Dividers

The FPGA development board used supplies 3.3V voltages (which is very common). The reasons why this board in particular was chosen is discussed in Section B.2. This requires us to lower the digital clocking signals supplied by the FPGA board for certain signals that interface the image sensor to either 2.5V or to 1V. Several DC to DC converters or level converters were considered, however, the required frequencies did not fall within the specifications. This pushed us to go to a very basic approach using resistors. This is probably not a power-efficient solution, but the resistor precision did give us the required output, and resistors could be changed on the board to alter the voltages - in case this is required, giving us some flexibility. We need to bear in mind

that this is a prototype and a final version of this camera would require a low-power consumption setup, but it would have its own custom FPGA controller which would give the correct voltage levels to start with making these voltage dividers useless.

A first attempt at proving the concept was made using regular resistors on a bread-board with a signal generator able to supply the same frequencies required by our application. After this proof of concept, resistor voltage dividers were integrated on the PCB.

B.1.6 Flexible Connections

To allow for maximum reuse of the PCB and flexibility in probing intermediate signals, jumpers were used to configure the signal paths. As a result, the signals from the FPGA Board to the Custom-PCB are connected by jumpers, and the signals between the Custom-PCB and the image sensor socket are also connected by jumpers. This allows us both to cut off a signal, and to force or probe custom intermediate signals.

B.1.7 Comparators

The output of the image sensor chip is an 8-bit output. This can be read out directly because of the jumper connections or passed to comparators. The 1V 8-bit output could then be regenerated (the digital signal boosted) before being read off of the PCB using Analog Devices' ADCMP600 to convert the 1V output of the chip into a 3.3V output for the logic analyzer, but it turned out that we would not be using these since the logic analyzer can accommodate to various voltage levels. These comparators can operate at the required frequency for our application.

B.2 FPGA Board

The FPGA board used is a standard Xilinx Spartan-3 Development Board. The FPGA is programmed by VHDL written using ISE and simulated with Modelsim. The code is actually downloaded in the board's EPROM that in its turn programs the FPGA after power-up (since the FPGA is volatile).

The VHDL generates the clocking signals specific to each mode of operation of the image sensor. The mode is selected using switches on the Spartan board. The board evidently comprises a reset switch as well. All the Image Sensor clocking signals are

generated, as well as the control for all DACs. A 120MHz clock (from the oscillator on the custom-PCB) is also input to the FPGA board and can be used instead of the on-board oscillator that cannot achieve such a high frequency. More details about the digital controller as well as the code can be found in the Appendix.

B.3 MATLAB

An 8-bit digital output coming from the image sensor is very hard to interpret using a logic analyzer if we need to see any "meaningful" frames. To get a better feel of the output, the Logic Analyzer is used to store some of the frame outputted (this is limited by the memory available on the instrument). These are saved as a text file which is then fed into Matlab. Two ".m" files were written to perform this task. The first converts the text file to image files (bitmaps), and the second combines the bitmaps into an AVI file to generate a video. This does not, of course, live up to real-time image viewing, but is enough to validate that the prototype does generate valid images. Any more extensive work would be much beyond the scope of this Master's Thesis.

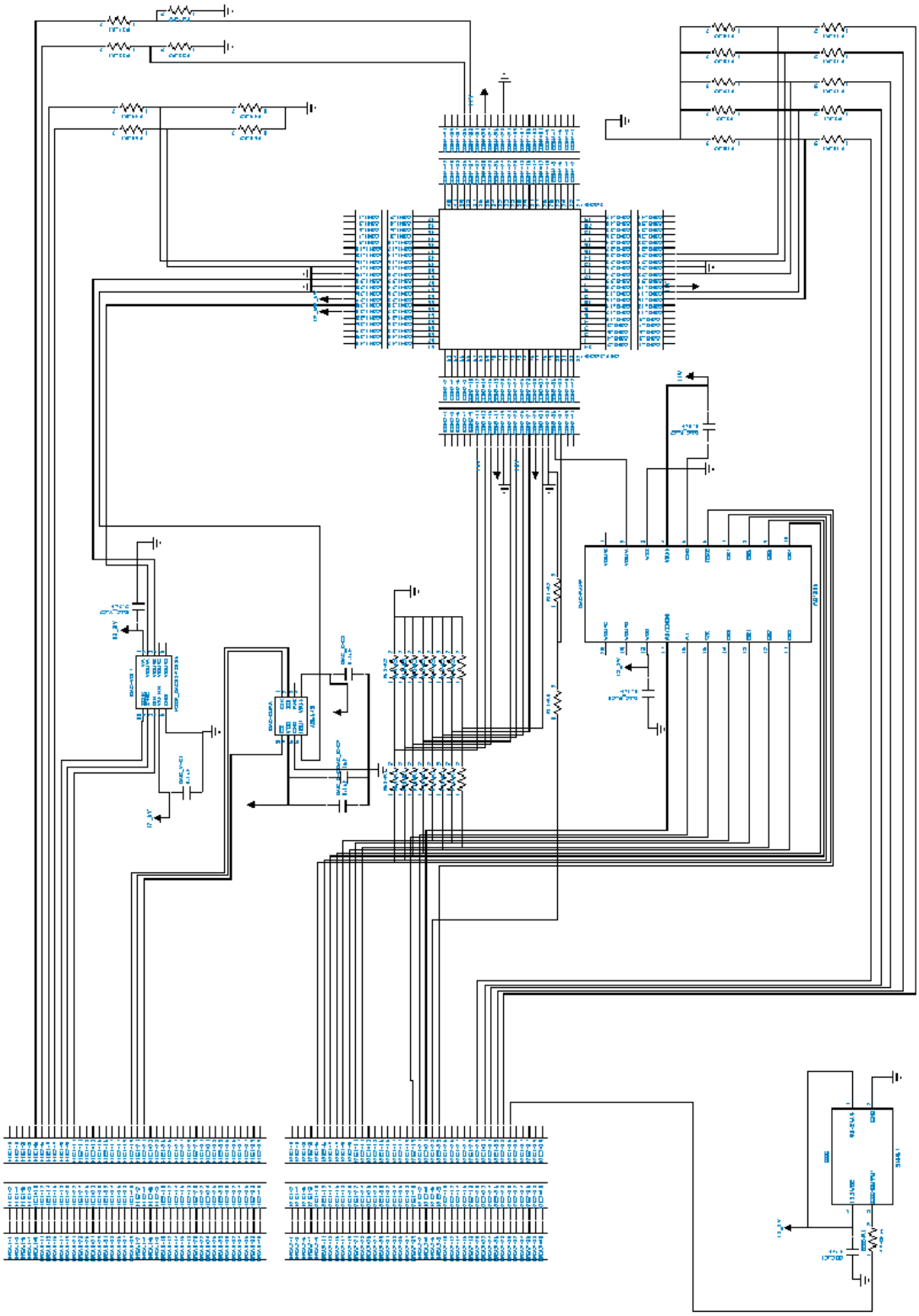


Figure B.2 PCB Schematic

Appendix C

CMOS 0.18μm Blocks

C.1 Switched-Capacitor Comparator Architecture (CMOS 0.18μm)

Essentially, the voltages to be compared are the pixel voltage V_{PIXEL} supplied by the photodiode and the analog-equivalent of an 8-bit digital ramp V_{RAMP} which is generated by an external digital-to-analog converter (DAC). The comparator compares V_{PIXEL} to the analog value of V_{RAMP} and latches the equivalent digital value of the ramp into an 8-bit memory. The commuted-capacitance comparator based on [1] and [138] is shown in Figure C.1.

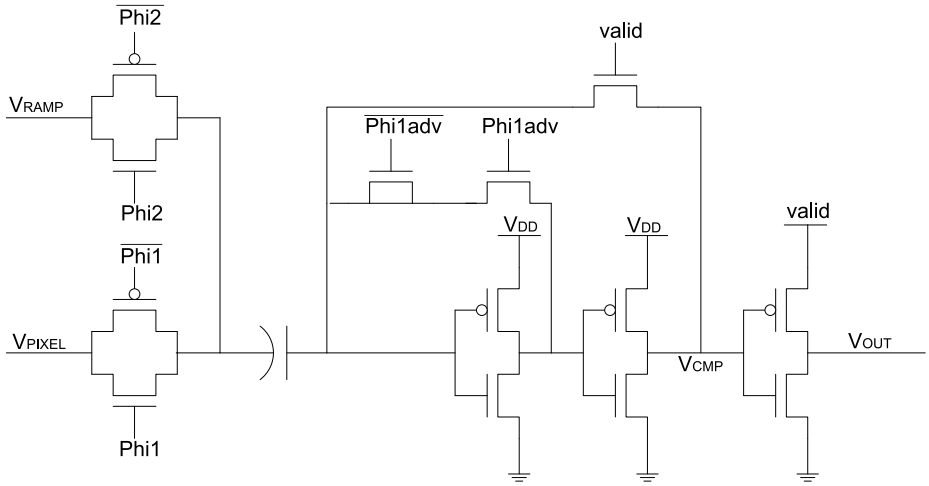


Figure C.1 Switched-Capacitor Comparator (CMOS 0.18μm)

It has a single input node that is connected to a capacitor. V_{PIXEL} and V_{RAMP} are applied to the input node one after the other by activating the transmission gates of $Phi1$ and $Phi2$ respectively. The supply voltage being of 1.8V, the initial voltage across the capacitor is at the metastable value of $\frac{V_{DD}}{2}$. V_{PIXEL} is then applied giving

a voltage drop of $V_{PIXEL} - \frac{V_{DD}}{2}$. After that V_{RAMP} is applied leaving us with a voltage of $V_{RAMP} - V_{PIXEL} + \frac{V_{DD}}{2}$. This means that the capacitor subtracts the two input voltages and then decides which is greater. If V_{PIXEL} is less, V_{CMP} would oscillate between ground and the metastable value. In the opposite case, V_{CMP} would oscillate between the metastable value and V_{DD}. The *valid* signal has been added to force the output value in limiting cases to a valid value. The final inverter has been added to make sure that the output to the memory, V_{OUT}, is always a valid digital value.

The top plate of the capacitor is connected to the comparator since it is deemed more sensitive than the inputs. The signal $Phi1_{ADV}$ is a slightly advanced version of the signal $Phi1$ to limit the effect of charge injection to the closing of switch $Phi1_{ADV}$. A dummy transistor is added next to the $Phi1_{ADV}$ transistor having half its width to absorb the injected charges. For the mode of operation particular to our DPS requiring the comparison of two consecutive pixel values, V_{PIXEL} is applied twice in a row to the input by activating $Phi1$ twice instead of activating $Phi2$. The resultant output would indicate which capture was darker.

C.2 Switched-Capacitor Comparator Simulations (CMOS 0.18μm)

A digital state controller was implemented in verilog to generate the clocking signals $Phi1$, $\overline{Phi1}$, $Phi1_{ADV}$, $\overline{Phi1_{ADV}}$, $Phi2$, $\overline{Phi2}$ and *valid*. A ramp of period T = 3μs rising from 0 to 1.8V was applied to the input V_{RAMP}. Several test values were applied to the input V_{PIXEL} to validate the functioning of the circuit. The value of the capacitor was swept and a value of 5fF was selected. Decreasing this value introduced a big offset. The capacitance is also best kept to a minimum because of the large silicon area it occupies on the chip. Furthermore, an increase of the capacitance beyond 10fF led to problems at the required operating frequency. A corner analysis of the circuit was conducted, and the worst-case result is shown in Figure C.2. The figure shows a time interval of 3μs with the ramp signal, one of the test pixel values $V_{PIXEL} = 900mV$ and the output of the comparator V_{CMP}. The measured offset was of $4.23mV$ which is below the limit set by an 8-bit precision which is of $7.03mV$ for a $1.8V$ voltage range. ($\frac{1.8V}{256} = 7.03mV$). Figure C.3 shows the equivalent memory-latching output, V_{OUT}, for the same corner analysis, which took

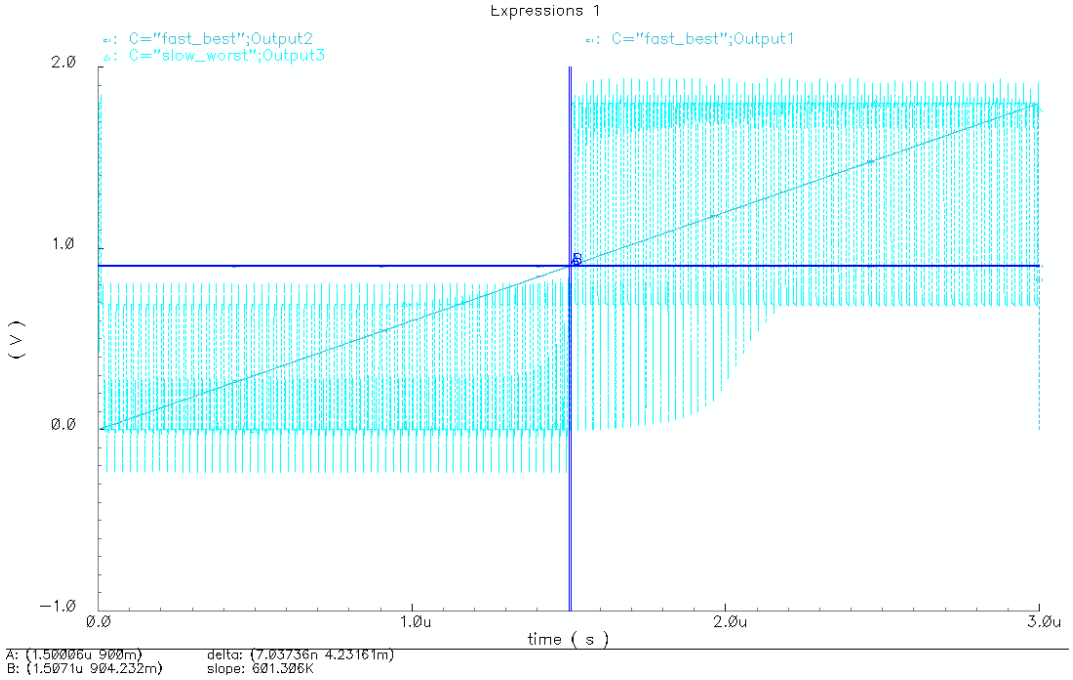


Figure C.2 Switched-Capacitor Comparator Worst-Case Corner Offset Simulation (Signals shown: V_{RAMP}, $V_{PIXEL} = 900mV$, V_{CMP})(Offset = $4.23mV$).

on a valid digital value at all times.

C.3 Differential-Input Pair Comparator Architecture (CMOS 0.18μm)

The customized differential-input comparator was based on a standard architecture [119; 138] and is featured in Figure C.4. It has an input differential-pair having input voltages V_{IN1} and V_{IN2}. V_{IN1} is connected at all times to the voltage coming from the photosensing circuit, V_{PIXEL}. V_{IN2}, however, is in the normal mode of operation connected to the same ramp voltage V_{RAMP} as was the case for the comparator in the previous section by setting the signal $CTRL_{RAMP}$ to high. On the other hand, for the mode of operation specific to the DPS in our application requiring the comparison of two consecutive pixel voltages, an analog memory cell was added to the pixel input of the comparator. The control signal $CTRL_{RAMP}$ is set to low to disconnect the ramp. Afterwards, the signal $CTRL_{IN}$ is set to high to store the value of V_{PIXEL} on the

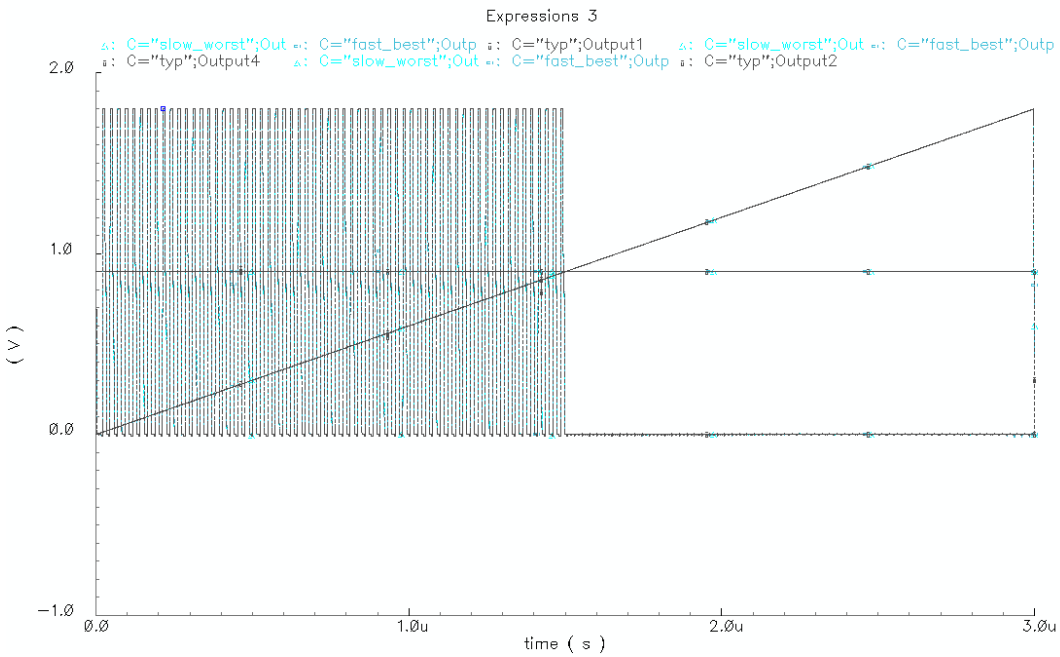


Figure C.3 Switched-Capacitor Comparator Worst-Case Corner Simulation Memory Latching (Signals shown: V_{RAMP}, $V_{PIXEL} = 900mV$, V_{OUT}).

node V_{CAP}. $CTRL_{IN}$ is then set to low and the newer value of V_{PIXEL} is placed on the node V_{IN1}. As a result, the output of the comparator would be the comparison between the current value of V_{PIXEL} placed on V_{IN1} and the older value of V_{PIXEL} now stored on the node V_{CAP} and applied to the input V_{IN2}. The final inverter added to the circuit has the same role as that in the circuit of the previous section which is to provide a valid digital output from the comparator at all times. Two biasing voltages, V_{BIAS1} and V_{BIAS2} are provided to the circuit by current mirrors.

C.4 Differential-Input Pair Comparator Simulations (CMOS 0.18μm)

A ramp of period $T = 3\mu$s going from 0 to 1.8V was applied to the input V_{RAMP}. Several test values were also set to the input V_{PIXEL} to validate the functioning of the circuit. The biasing voltages V_{BIAS1} and V_{BIAS2} were then varied and their optimal values selected to be of $550mV$ and $500mV$ respectively to minimize the offset. A corner analysis of the circuit was conducted, with the worst-case result shown in

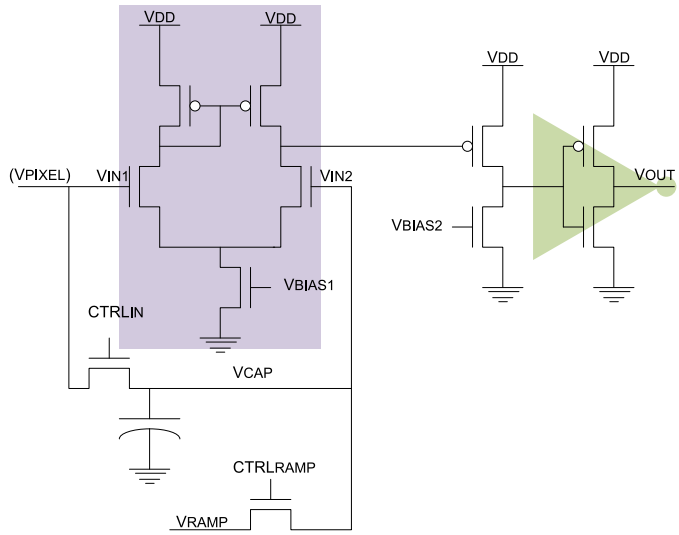


Figure C.4 Differential-Input Comparator (CMOS 0.18μm)

Figure C.5. The figure shows a time interval of 3μs with the ramp signal, one of the test pixel values $V_{PIXEL} = 900mV$ and the output of the comparator V_{OUT}. The measured offset was $6.01mV$ which is below the limit set by an 8-bit precision which is of $7.03mV$ for a $1.8V$ voltage range. For the mode of operation specific to the DPS in our application requiring the comparison of two consecutive pixel voltages, the ramp was disconnected from the circuit by setting the signal $CTRL_{RAMP}$ to low. A capacitance of 7fF was selected for the analog memory.

The simulation setup consisted of a time interval of 12μs with four different values of V_{PIXEL}: $1.3V, 0.7V, 0.7V$ and $1.3V$ each lasting for a duration of 3μs. The following describes the details:

- 0 - 3μs: $V_{PIXEL} = 1.3V$, $CTRL_{IN}$ was high to store V_{PIXEL} in V_{CAP}, V_{OUT} was irrelevant;
- 3μs - 6μs: $V_{PIXEL} = 0.7V$ and was applied to V_{IN1}, $CTRL_{IN}$ was low, V_{IN2} had the value of V_{CAP} from the memory, V_{OUT} was low since $V_{IN2} > V_{IN1}$;
- 6μs - 9μs: $V_{PIXEL} = 0.7V$, $CTRL_{IN}$ was high to store V_{PIXEL} in V_{CAP}, V_{OUT} was irrelevant;
- 9μs - 12μs: $V_{PIXEL} = 1.3V$ and was applied to V_{IN1}, $CTRL_{IN}$ was low, V_{IN2} had the value of V_{CAP} from the memory, V_{OUT} was high since $V_{IN2} < V_{IN1}$.

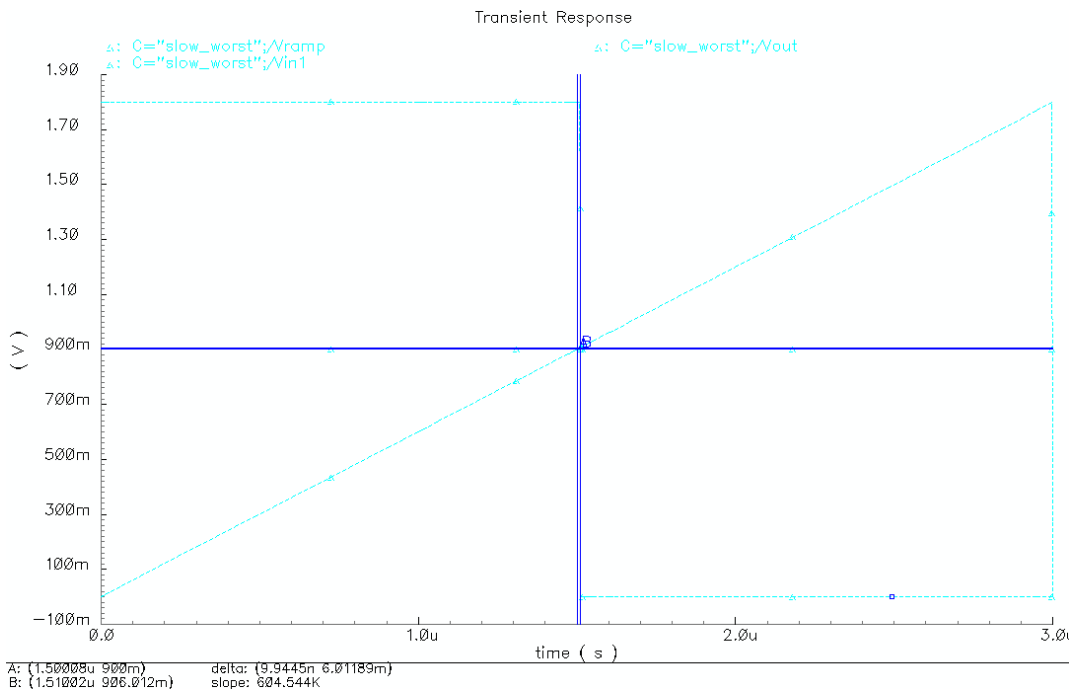


Figure C.5 Differential Comparator Offset Worst-Case Corner Simulation (Signals Shown: V_{RAMP}, V_{PIXEL} = 900mV, V_{OUT})($Offset = 6.01mV$)

The worst-case results of the corner-analysis of the simulation setup appear in Figure C.4.

C.5 Differential versus Switched-Capacitor Comparator

Similar worst-case corner-analysis simulations were conducted on two different topologies of comparators. Both of them were operated with frequencies of 0.333MHz (1 / 3μs). This exceeded by far the requirements of 400fps for the proper functioning of the DPS. The switched-capacitance comparator used a capacitance of 5fF. It was a clocked comparator with three clocking signals and their inverses plus an additional validation signal for borderline cases. The offset obtained was of $4.23mV$. The differential-input comparator had an added an analog memory with a capacitance of 7fF to allow for the comparison of two consecutive pixel voltages (which is intrinsic to the topology of the former comparator type). The offset in this case was of $6.01mV$

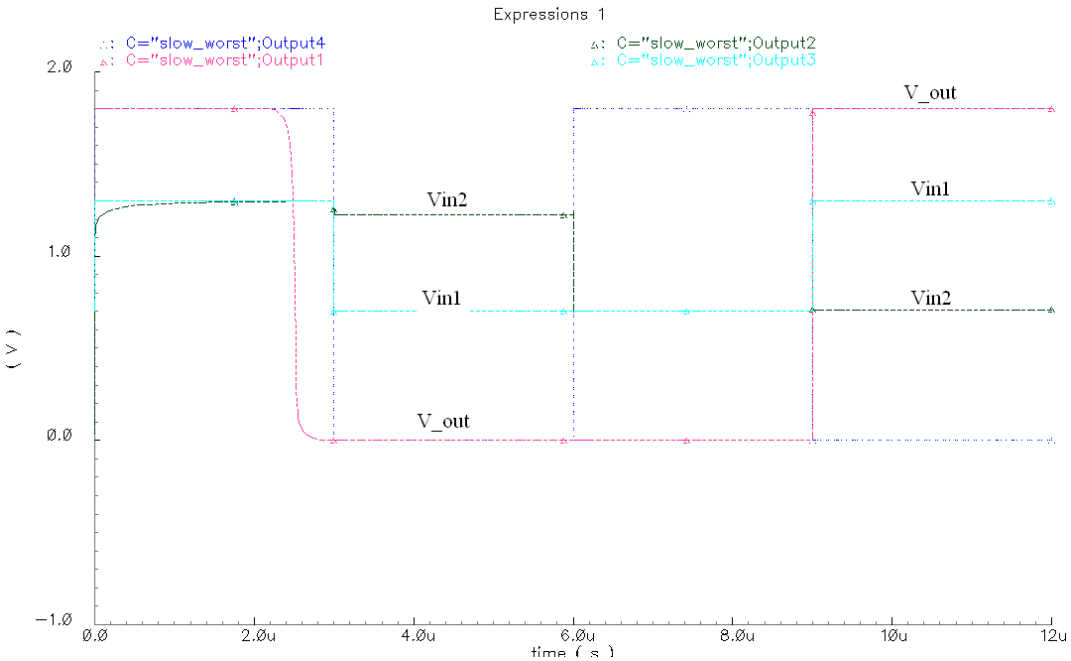


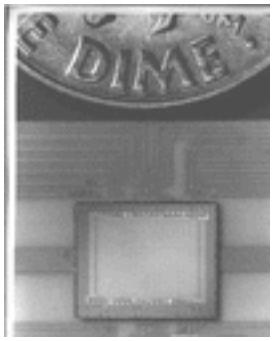
Figure C.6 Differential Comparator Behavior Simulation

which, while still being less than the $7.03mV$ upper limit required for an 8-bit precision, was still greater than that of the switched-capacitor topology. However, the differential comparator required two clocks $CTRL_{RAMP}$ and $CTRL_{IN}$ which were operated less frequently thus minimizing the possibility of clock feedthrough especially in the normal operating mode where $CTRL_{RAMP}$ is operated only once to set the mode and where $CTRL_{IN}$ is not used. The differential comparator also required two biasing voltages. In short, the switched-capacitor comparator gave a better offset at the expense of more clocking signals with a non-escapable reliance on a capacitor for comparisons. On the other hand, the differential comparator gave a greater, but still acceptable, offset while using less control signals and less clocking with its sole reliance on capacitance being in the mode that requires the comparison of two consecutive voltages of the pixel. Nevertheless, minimizing offset and silicon area being some of the top objectives, the results were in favor of the switched-capacitor architecture that required a smaller capacitance and hence had a smaller area.

Appendix D

Performance Parameters in State-of-the-Art CCD Image sensors

The first Charge-Coupled Device image sensor (featured in Figure D.1(a)) saw the light of day at Bell Laboratories in 1969 [139; 140]. It was inspired by the bubble technology - a shift register where the presence or absence of a magnetic dipole represented a 0 or a 1 and the shifts were conducted by rotating an external magnetic field. Boyle and Smith (appearing in Figure D.1(b)) applied this principle to semiconductor technology and came up with the basic structure of the CCD where the magnetic bubble was replaced by a packet of charges stored in a MOS capacitor and charges where moved between the tightly spaced capacitors by applying a "more attractive" voltage to the receiver [141]. In January 2006, Boyle and Smith were awarded the National Academy of Engineering Charles Stark Draper Prize for their work on the CCD [142].



(a) Early version of a CCD sensor

(b) the inventors of the CCD sensor, Boyle and Smith (left to right)

Figure D.1 Invention of the CCD sensor [143]

A period of rapid development followed both at Bell and at other companies focusing on two types of devices: area imaging devices for picture cameras and linear imaging devices for use in scanning applications [141]. Among these companies were Fairchild Semiconductor, RCA and Texas Instruments. The first commercial device was marketed by Fairchild in 1974 with a matrix of 100 x 100 pixels. Iwama et al. at Sony later on picked up the pace to mass produce CCDs for their camcorders [144].

It is worth noting though that image sensing is not the only application for CCDs. A charge packet in a CCD structure can be directed anywhere within that structure using digital clocking. The simplest CCD signal processing device is the analog delay line (a serial input-output CCD). More complex applications arise from using CCDs in digital mode where full packets represent ones and empty packets zeros. This can be used to create components such as the serial to parallel shift register proposed by Chan et al. in 1973 [145] or even adders and multipliers. Plus, cells in digital CCDs can be much smaller than in analog ones since we are looking at discrete values for the former [146]. This is without forgetting one of the initial applications that CCDs were conceived for: memories [147]. An interesting recent (2007) overview on the future of charge-trapping memories is presented by Mikolajick et al. [148].

Nevertheless, applications of CCDs have lost their sparkle around the 1990s with the exception of CCD imagers; which is why when most people refer to CCDs they are actually referring to CCD image sensors. Since this thesis is centered on image sensors, the subsequent discussion will be utterly focused on this application of CCDs.

D.1 Antiblooming and Exposure Control

In general, blooming occurs when the full well capacity of the pixel is exceeded, causing charges to overflow into adjacent pixels.

In the early 1980s, IT-CCDs had already been developed and placed on the market, and had reached sensitivity and noise levels close enough to the performance of electron-beam tubes. Nevertheless, the blooming was still left to be desired. Research had started on antiblooming as early on as 1972 [149; 150]. Solutions for antiblooming had already emerged by the mid-seventies by biasing the region around the cells during integration [41] or adding an overflow CCD to contain the superfluous charges that would then be transferred to an output and eliminated [42]. Many other antiblooming strategies and variations have been adopted throughout the evolution of

CCD sensors, such as the blooming suppression achieved by Ishihara et al. in 1984 for an IT architecture by means of a vertical overflow drain positioned under (rather than beside) a PD without sacrificing photosensitivity or DR [151].

D.2 Image Smear

In general, image smear occurs when charges are shifted. This could show up as blur. CCD imagers had early on been designed in two architectures: Frame Transfer (FT) and Interline Transfer (IT) - each of which has its own advantages and disadvantages. The FT architecture proved to be more versatile and to have better sensitivity than the IT one. However, the latter provides an improved response to higher spatial frequencies [152]. FT architectures have the disadvantage of the introduction of image smear when transferring images in the storage section while IT architectures have the disadvantage of having more complex cells [152]. Conventional IT-CCD technology, for instance, can face a decrease of 75% in sensitivity and an increase of 200% in smear value for a 67% reduction in pixel size [153]. Several smear reduction methods came to be: using microdefects to kill unwanted charges in bulk Silicon [154], or using a P-Well structure to prevent carriers from diffusing into the V-CCD [155] or the introduction of FIT-CCDs (a combination of both the FT and IT architectures) with smear carrier sweep-out [156] or even external circuit collection that stores the smear component in an external memory to be subsequently subtracted from the signal [157]. Ohba et al. conducted in 1985 a quantitative study on smear noise considering capacitive coupling, carrier diffusion and light leakage that led them to the conclusion that the main cause of smear is light leakage [158].

Aside from architectural approaches for smear reduction, novel fabrication methods saw the light of day. Teranishi et al. reduced the oxide thickness under the aluminum photoshield diminishing the smear by about 12 times as compared to a conventional IT-CCD [157]. Sakakibara et al. put forth a Modified Barrier Well (MBW) with a new impurity profile of a buried P+ layer and an on-chip microlens array accomplishing a low smear ratio while maintaining high sensitivity [159]. Furumiya et al. also put forward their contribution to smear reduction and sensitivity increase with a new flattened-pear- shaped PD exhibiting a wide, low-concentration N-layer below the conventional photodiode N-layer [160]. Tanabe et al. used BF_2 ion implantation for the shallower P+ layer of the PD decreasing the surface electron

diffusion flow at the channel stopper side reducing smear [161].

D.3 Image Lag (or Sticking)

In general, image lag/sticking/ghosting occurs when there is an improper reset of the CCD and improper/incomplete charge transfer. A residue of the previous image would appear in the current frame, and perhaps additional subsequent frames creating a "ghost".

It was initially believed that solid-state imagers were immune to image lag; nevertheless, this turned out to be fallacious for the case of interline CCDs spawning an additional torment that is not dealt with in some sensors. Teranishi et al. drew out in 1982 analytical formulae based on subthreshold current analysis to quantitatively characterize image lag pertaining to the principle that subthreshold current dominates the electron transfer from the PD to the V-CCD in the final stage when the potential difference between the diode and the transfer gate channel closes to null. This impedes some of the electrons from transferring because of the short period creating residual charges that would appear in the subsequent frame as image lag. To get around that, Teranishi et al. proposed a new structure for a PD capable of having a decently large potential difference to allow all the electrons to be transferred. To accomplish that, the N-type region was given a lower donor density and a P+ layer was formed on it to enhance the charge storage capacity and to dispense with carrier trapping and dark current generation rendering image lag imperceptible even at low illumination hence extending the lower light threshold [162; 163]. However, this does not address higher intensities, for if we delve deeper into the topic, image lag can be photoconductive lag in the Silicon layer or capacitive lag from incomplete charge transfer through the readout transistor. The latter lag is pronounced at low illumination levels, and can be eliminated by proper resetting of the diode potential for each frame. As for the total lag, it can be ephemeral for low or medium light intensities, but for higher intensities, conventional devices are prone to image sticking caused by charge trapping in deep levels of Silicon. Sasaki et al. were able to sidestep this issue by injecting bias charges into the Silicon layer filling the deep level traps in advance [164].

D.4 Resolution

Increasing the resolution was one of the greatest initial goals in image sensor design. One of the earlier players was NASA's JPL that began investigating the CCD technology in 1974 to improve it by increasing the number of pixels in the array from the 100×100 matrix limit reached at the time. By 1978 they had produced CCD arrays of 500×500 pixels. The matrix size was then increased to 800×800 used by Galileo launched in 1989 and the Hubble Space Telescope launched in 1990 [165]. The early 1980s saw the dawn of a second generation of CCD sensors that surpassed their predecessors in almost every characteristic: better resolution, smaller pixels, lower noise, lower cost and improved reliability. Sensors with greater matrices of 1024×1024, with smaller pixels (12 μm as compared to the older 15 μm) and lower noise [165]. In the mid 1980s, new CCDs for HDTV applications were developed [166; 167]. Nevertheless, such sensors had to overcome certain obstacles to become practical. Basically, the resolution increase to migrate from NTSC to HDTV, if not matched by a photosensitive area increase, impairs the sensitivity of the sensor due to the reduction in aperture size coerced by the increased V-CCD and device isolation channels, and downgrades the DR due to the narrowing of the width of the V-CCD's charge transfer channel [43].

D.5 Sensitivity

Several methods have been put forth to increase sensitivity, one of them is to introduce a photoconductive film over a silicon surface creating a multi-layer approach [168; 169] making the DR independent of the silicon underlayer. This circumvents the problem without directly addressing its roots and without amending the issue of image lag. Another proposed approach was the Trench CCD sensor which enlists the trench technique originally used in DRAMs [170; 171]. Its main feature is a long trench formed in the charge transfer direction on the silicon surface and an N-region formed over the sides and bottom of the trench as the charge transfer channel creating a three-dimensional structure increasing the effective channel width and hence the charge handling capacity which is correlated to the DR. Moreover, it occupies a small percentage of the pixel area, increasing the aperture area, and consequently boosting the sensitivity [43]. A third technique developed by Tabei et al. is what they

called Sea-of-Photosensor Array (SPA-CCD), both the interline pixels and the vertical charge transfer lines are used as photosensitive elements to improve simultaneously the resolution and sensitivity [172]. In 1994, Chen and Ginosar designed an adaptive sensitivity CCD image sensor. The sensitivity of each pixel was individually controlled (by changing its exposure time) to ensure that it is operating in the linear range of the CCD response, yielding a much wider DR enabling the imager to capture details in both the light and dark areas of high-contrast scenes. The controller had an exposure time memory for each pixel [173]. A more recent novel pixel architecture was ventured into by Tsukamoto et al. having two notable elements: a thin refractory metal light shield and an inner-layer microlens. An increase of 30% in sensitivity in addition to a 6dB smear reduction were observed with a pixel area size of 22.6μm^2 flaunting performance levels comparable to a conventional CCD with pixel area size of 33.6μm^2 [153].

D.6 Readout Schemes

The one-dimensional aspect of CCDs was outflanked in 1974 by Sequin et al. at Bell Laboratories who put forth a new two-dimensional charge-transfer orthogonal array scheme allowing the transfer of charges in more than one direction [174]. In 1994, Burke et al. presented a new 64 x 64 pixel prototype two-dimensional CCD imager structure capable of transferring charge packets in all four directions [175]. In 2006, Smith et al. described the development, operation, and characterization of such two-dimensional transfer CCDs as opposed to conventional one-dimensional transfer CCDs presenting and validating two schemes [176].

Also, color CCDs require special readout considerations. The first conventional linear CCD had a row of red sensors, another of blue ones and a third of green ones, each having its own color shift register. This, however, required a large memory to compensate for position deviations in the image between the different color-sensors. Basically, the image is scanned three times and should not have moved in between. The second conventional architecture has alternating red, green and blue sensors arranged in the same row. However, they are also shifted out of the sensor in the same shift register which may cause color mixing from one cell overflowing into the other or residual color in one cell affecting the other. As an alternative, Kawamoto et al. proposed a third architecture that combined both by having a single row of

alternating sensors but three separate color registers [177].

With the trend going towards HDTV resolution requirements, several sensors were developed satisfying these. Nevertheless, these were not well-suited for high-resolution robotic vision and electronic camera applications because their interlaced architecture forced a 50% reduction in resolution if they had to be used in applications that generated an image after a single scan. For this, Stevens et al. came up with an IT-CCD sensor with a novel non-interlaced scan (or progressive scan) architecture characterized by low smear, no lag and high responsivity and doted with the ability to clock out the image one or two lines at a time allowing high-resolution single-scan high-speed image capture [178].

Another point worth mentioning is that in single-output CCDs, the charge is transferred from the V-CCD to the H-CCD and then pushed through the register to an output structure for conversion to current or voltage. A common problem encountered though is the nonuniformity in the video level of the first pixels read out. To circumvent that, isolation pixels are added next to the output structure. These are read out first, allowing the performance of the output node to settle before receiving valid pixels. An output node with a very small capacitance increases the charge-conversion efficiency. However, the transition from large pixel geometry in the H-CCD required for large storage capacity to small geometry of the node has to be carefully designed to optimize efficiency and linearity. Nevertheless, the speed of the sensor is limited by the existence of a single output. That is why in 1997 Kiik et al. used multiple outputs to boost the data throughput of their FT-CCD. For this, they divided the H-CCDs into equal length segments reducing the number of pixels being read out by each node and hence the readout time. However, this requires additional physical space. This also restricts the use of isolation pixels [179].

D.7 Noise

The pervasiveness of noise being always an issue, many schemes have been devised throughout the years for noise reduction or elimination. The scope of the topic led Hopkinson and Lumb to form a discussion on noise reduction techniques in 1982 deriving formulae based on a known noise spectrum founded on the fact that the relative merits of each technique depend on the nature of the noise source [180]. Fixed Pattern Noise (FPN) was proved to be caused mainly by gate capacitance and

threshold-voltage variations. Based on that, Ohba et al. designed a simple circuit containing an emitter-follower amplifier, an integration capacitor, a reset switch and a load resistor reducing FPN by around 20dB to achieve an SNR close to 68dB [181]. Another way to eliminate FPN was put forth by Hiroshima et al. that makes use of a new epitaxial wafer fabrication process for CCD imagers. The use of the epitaxial layer was found to eliminate the concentric circle image pattern and to suppress thermally induced white blemishes [182]. Moreover, many noise suppression methods came to be other than the conventional CDS with which it was difficult to generate narrow pulses and obtain stable clamping at HDTV speeds. One such method was the Reflection-Delayed noise Suppression (RDS) proposed by Ohbo et al. The principle of operation is to mix the signal with a delayed version of itself and to find the difference between the feedthrough level and the signal level [183]. Matsunaga and Ohsawa also introduced alternate gain inversion (AGI) signal processing to suppress 1/f noise in an IT-CCD [184]. In 1992 Hynecek analyzed theoretically the CDS method providing some insight into the choice of circuit parameters [185].

Sources of image noise have been very well documented throughout the lifespan of CCDs, but little work has been done on the assessment and validation of these noise sources. This has encouraged Irie et al. to publish in 2008 a comprehensive noise model for CCD cameras. They used this technique to evaluate the noise of a commercially available CCD video camera by experimentation and analysis [186].

D.8 Trends in State-of-the-Art CCD Image Sensors

Decreasing the size of sensors while maintaining satisfactory performance levels has been the topic of a lot of research. The tendency towards an increase in the number of pixels got even more intense in the late 1990s especially with the advent of more advanced applications such as the introduction of a stereoscopic IT-CCD color video movie camera by Yamaguchi and Takemura in the late-eighties/early-nineties. It basically records two images from two viewpoints and the user sees these through special glasses so that the brain mixes them to create a 3D image eliminating the need of having two cameras and two recorders that need to be synchronized; therefore creating a compact portable system [187; 188]. The growing need for better resolutions

compelled researchers to invest even more time into compensating for the inevitable increase in the size of the image sensor, which in its turn triggered the motivation for pixel size shrinkage.

The drive towards smaller imagers led Yamada et al. to develop in 1998 what they called the smallest IT-CCD with SXGA format yet to be found [189]. Its 5μm $\times$ 5μm pixel was 56% smaller than the pixel size of 2/3-inch 1.3M-Pixel CCDs manufactured the previous year by the same group with 6.7μm $\times$ 6.7μm pixels [190].

Van Kuijk et al. were able in 2000 to reduce the pixel size of an FT-CCD to 4.1μm $\times$ 4.1μm by using gapless microlenses to increase the sensitivity by 25 to 30% and by using a low noise high-linearity output amplifier [191]. In 2002, Le Cam et al. came up with a manner of doubling the readout rate without changing the readout frequency by introducing horizontal subsampling with binning for an even smaller 3.7μm $\times$ 3.7μm pixel FT-CCD [192].

An IT-CCD with pixels of 2.2μm $\times$ 2.2μm was available on the market by 2005. This pushed Oda et al. to reduce the pixel size of FT-CCDs even further to 1.56μm in that same year. The imager was intended to be used for mobile applications. It is quite easier to scale down FT-CCDs than IT-CCDs because of the simpler pixel structure and greater aperture. The decrease in pixel size is nevertheless inevitably accompanied by a decrease in sensitivity. To circumvent that, the authors have decreased the gate electrode spacing, optimized the shape of the microlenses and improved the conversion factor. They were also able to reduce the overall power consumption by decreasing the operating voltage to 7V [193] (as compared to somewhere around 12V for conventional CCDs [192]).

Another decrease in pixel size was undertaken by Fife et al. in 2007. They reported the first FT-CCD with submicron pixel pitch. Their prototype consisted of a matrix of 16×16 pixels with pitch of 0.5μm using a single-poly 110nm CMOS process with DR of 60dB, peak SNR of 28dB, DSNU of 25% and PRNU of 5.8% - which are values that can still be compared to consumer image sensors [194]. The pixel size is around three times smaller than for recently reported CCDs by Oda et al. in 2005 [193] and CMOS sensors by Cohen et al. in 2006 [195].

High-speed CCD imagers have also been manufactured. A notable one is the ISIS (In-SItu Storage) image sensor patented by Etoh and Mutoh in 2005 [196]. Their first sensor was developed in 1991 with a frame rate of 4500 fps rising up to 1,000,000 fps by 2001. The sensor is capable of recording signals in all pixels in parallel. In

2007 their worked was concentrated on the development of a new photon-counting PC-ISIS for microscopic biological observation. A review of the evolution of their CCD imagers can be found in [197].

Recent CCD technology efforts have been focused on understanding radiometric accuracy for very sensitive measurements (such as searching for planets around other stars) and on improving CCD response in the ultraviolet region of the electromagnetic spectrum.