UNIVERSITÉ DE MONTRÉAL

DESIGN AND VALIDATION OF A GM-C BANDPASS SIGMA-DELTA MODULATOR DEDICATED TO FRONT-END ULTRASONIC RECEIVERS

LISHENG QIN

DÉPARTEMENT DE GÉNIE ÉLECTRIQUE

ÉCOLE POLYTECHNIQUE DE MONTRÉAL

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DESIGN AND VALIDATION OF A GM-C BANDPASS SIGMA-DELTA MODULATOR DEDICATED TO FRONT-END ULTRASONIC RECEIVERS

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a été dûment accepté par le jury d'examen constitué de :

M. AUDET Yves, D.Sc.A., président

M. SAWAN Mohamad, Ph.D., membre et directeur de recherche

M. SAVARIA Yvon, Ph.D, membre

DEDICATE

To all my beloved

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First of all, I would like to thank my director, Professor Mohamad Sawan of École Polytechnique and Director of Polystim Laboratory, for his valuable guidance that conducted my research until the successful completion of the project. I also give my gratitude for his kind encouragement and for offering such a wonderful researching environment.

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RÉSUMÉ

Les équipements ultrasons sont largement répandus dans le domaine du diagnostic médical. Cependant, leur encombrement vis-à-vis du volume et de la consommation de la puissance a limité d'une manière significative leur utilisation à l'intérieur des hôpitaux. Avec l'avancement technologique continuel de la microélectronique, la miniaturisation des systèmes ultrasons a eu un grand intérêt chez les développeurs d'appareils médicaux. Dans un système ultrason miniaturisé, le convertisseur analogique numérique (CAN) joue le rôle de l'interface entre le monde analogique et numérique et son efficacité marque énormément la fiabilité globale du système.

L'objectif principal de ce mémoire est la conception d'un CAN type Sigma-Delta dédié au récepteur ultrason. Ce CAN est marqué par une haute résolution et une faible consommation de puissance. En plus, il est doté d'une programmabilité de sa fréquence centrale afin d'assurer la multifonctionnalité des dispositifs ultrasons miniaturisés pour accommoder plusieurs types de sondes dédiées aux différentes régions du corps.

Dans ce mémoire, on examine les différentes techniques existantes pour la conception d'un CAN de type Sigma-Delta et on propose un modulateur passe-bande de 4-ième ordre en mode continu dans le temps. La cellule de transconductance Gm, qui constitue l'unité de base du filtre Gm-C utilisé dans le modulateur, a la capacité d'être programmeé d'une façon grossiére et fine. Cette programmabilité, ainsi que la flexibilité du filtre du 4ième ordre proposé, garantit au modulateur la capacité d'être adaptable entre différentes fréquences centrales et avec différentes bandes passantes. Un modulateur possédant une

fréquence centrale de 3 MHz a été fabriqué en utilisant la technologie CMOS 0.18 µm. Ce modulateur dissipe 2.5 mW puissance d'une tension d'alimentation de 1.8V. La simulation post-layout du modulateur dans l'outil Cadence donne un SNR de 78 dB. Le chip fabriqué, après avoir été ajusté de 3 MHz à 750 kHz, donne un SNR de 56 dB.

ABSTRACT

Ultrasound equipments have been widely used in the medical diagnostics domain. But their bulkiness and high-power consumption significantly limit the traditional ultrasonic systems inside hospitals. With the continuing progress in microelectronics technology, the miniaturization of ultrasonic systems attracts great interests. In such a system, analog to digital converter (ADC) acts as the exact interface between analog and digital signal processing and often contributes the system bottleneck.

The aim of this master thesis is to design a Sigma-Delta ADC dedicated to front-end ultrasonic receiver. This ADC features high resolution, low power consumption and adequate programmability which are necessary for hand-held multi-function ultrasonic devices.

This thesis examines the options of Sigma-Delta ADC techniques and proposes a fourth-order continuous-time bandpass modulator. The Gm-cell, which is the basic unit of the Gm-C filter, can be programmed within a wide range through coarse and fine tunings. This programmability, together with the flexibility of the proposed fourth-order filter, guarantees that the modulator is capable of being programmed between different central frequencies with different bandwidth. A Sigma-Delta ADC for 3 MHz application has been implemented in a 0.18 μm CMOS and consumes 2.5 mW drawn from a 1.8V power supply. Post-layout simulations in Cadance give 78 dB SNR. The fabricated chip is measured after being tuned from 3 MHz to 750 kHz and a 56 dB SNR is achieved.

CONDENSÉ EN FRANÇAIS

I. INTRODUCTION

Les équipements ultrasons sont largement utilisés dans le domaine des diagnostics médicaux afin d'identifier les anomalies du corps humain. Cependant, leur encombrement vis-à-vis du volume et de la consommation de puissance a limité d'une manière significative leur utilisation à l'intérieur des hôpitaux. Avec l'avancement technologique continuel de la microélectronique, la miniaturisation des systèmes ultrasons a eu un grand intérêt chez les développeurs d'appareils médicaux. Le schéma bloc d'un système ultrason miniaturisé, illustré à la Figure 1, a été proposé par notre équipe de recherche.

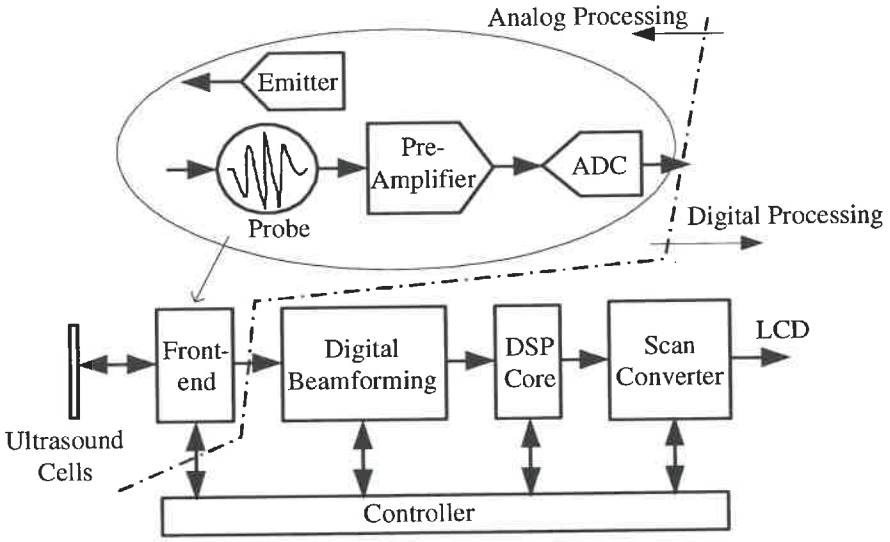


Figure 1: Schéma bloc global d'un système ultrason.

Le convertisseur analogique à numérique (CAN) dans ce schéma bloc convertit les signaux analogiques à signaux numériques afin de les préparer pour le traitement numérique subséquent. Vue que le CAN est l'interface entre les monde analogique et numérique, sa performance marque énormément la fiabilité globale du système ultrason. La modulation Sigma-delta ($\Sigma\Delta$) a devenu le meilleur choix pour les applications qui nécessitent des CAN à haute résolution dans une bande passante relativement étroite. En utilisant la technique de sur-échantillonnage et de modulation du bruit, le CAN type $\Sigma\Delta$ diminue les contraintes demandées aux circuits analogiques en terme de précision et aussi contribue énormément à la réduction de la consommation de puissance.

II. THÉORIES FONDAMENTALES DE LA MODULATION SIGMA-DELTA

Le rapport signal sur bruit (SNR) pour un CAN de N-bit de résolution en mode Nyquist f_S est donné par :

$$\mathrm{SNR} = 6.02\mathrm{N} + 1.76.$$

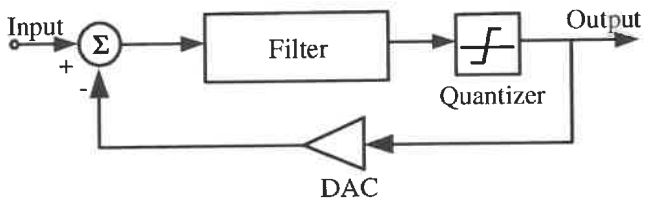
Pour un CAN utilisant la technique de sur-échantillonage, avec un taux de sur-échantillonnage (OSR) par rapport à la fréquence de Nyquist f_S, le SNR est donné par

$$\mathrm{SNR} = 6.02\mathrm{N} + 1.76 + 10\log(OSR).$$

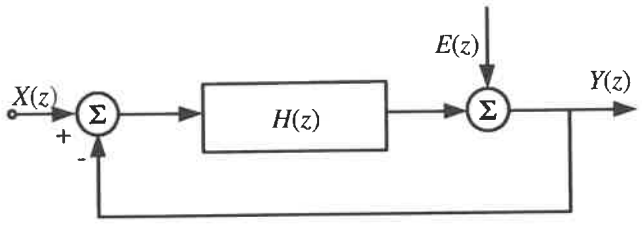
Notez qu'à chaque fois qu'on double la fréquence d'échantillonnage, la résolution augmente de 3dB. Cependant, la dépendance directe de SNR à l'OSR limite la résolution du système parce que la fréquence d'échantillonnage est limitée par la vitesse de la

technologie utilisée. Pour éviter l'utilisation d'une fréquence d'échantillonnage extrêmement élevée, la modulation du bruit est adoptée avec le sur-échantillonnage pour augmenter la résolution du CAN.

Selon la Figure 2, la technique de la modulation du bruit soustrait la sortie du quantificateur de signal d'entrée dans une boucle de rétroaction afin d'être filtré par le filtre de la boucle.



(a)



(b)

Figure 2: Schéma bloc du modulateur Sigma-Delta et son modèlle linéaire

(a) Structure du modulateur (b) model linéaire en forme Z

La fonction de transfert du signal STF(z) et la fonction de transfert du bruit NTF(z) sont données par:

$$S_{TF}(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)},$$

$$N_{TF}(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)},$$

et $$Y(z) = S_{TF}(z)X(z) + N_{TF}(z)E(z).$$

Si H(z) a un pôle(s) situé dans la bande passante, le signal d'entrée peut être restauré avec exactitude car STF(z) approche de l'unité dans cette bande de fréquence. D'autre part, le bruit de quantification est fortement atténué dans la bande passante. Pour un modulateur du Nième ordre, le SNR est donné par :

$$SNR=6.02N + 1.76 - 20L\log(\pi) + 10\log(2L+1) + 10(2L+1)\log(OSR).$$

La résolution visée de notre modulateur est de 12 bits, ce qui correspond à un SNR de 72dB. Pour assurer la stabilité du modulateur, le signal d'entrée doit être plus petit que la tension de la référence. En outre, le CAN souffre également de diverses imperfections dus aux circuits analogiques. Par conséquent, le SNR théoriquement réalisable par le modulateur doit être au alentour de 100 dB pour assurer le 72 dB du modulateur après fabrication. Les paramètres qui décident la résolution du modulateur sont l'OSR, l'ordre de la modulation du bruit L et le nombre de bits N du quantificateur. Après un étude approfondie basée sur la théorie et la simulation, un modulateur ΣΔ passe-bande de 4ième ordre à OSR de 128 et N de 1-bit a été choisi.

III. IMPLEMENTATION DU CIRCUIT

1. FILTRE DU 4 IÈME-ORDRE

Nous proposons un filtre de boucle de 4ième ordre obtenu en cascadant deux filtres identiques de 2ième ordre H1 et H2 comme représenté à la Figure 3. Chacun des deux

filtres contribue à un pôle. Les positions des pôles et les facteurs de qualité Q des deux filtres peuvent être programmés séparément pour assurer plus de flexibilité au modulateur réalisé.

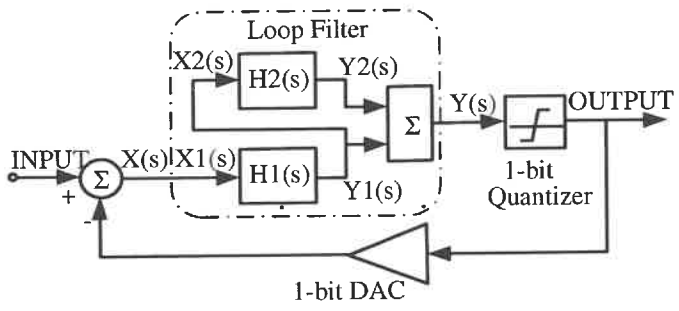


Figure 3: Schéma bloc du modulateur Σ-Δ de 4ième ordre

La structure du filtre de 2ième ordre est présentée à la Figure 4. Sachant que les impédances de sortie des transconductances sont beaucoup plus grandes que R1 et R2, leurs valeurs ont été négligées. Dans ce cas la fonction de transfert correspondante de H1 est donnée par:

$$H1(s)=\frac{\frac{Gm3}{C}s+\frac{1}{C^2}\cdot\left(Gm1\cdot Gm2+\frac{Gm3}{R1}\right)}{s^2+\frac{1}{C}\cdot\left(\frac{1}{R1}+\frac{1}{R2}\right)s+\frac{1}{C^2}\left(\frac{1}{R1\cdot R2}-Gm2\cdot Gm4\right)}$$

La fréquence centrale $\omega_0 1$, le facteur de qualité Q1 et la bande passante BW1 sont dérivées comme suit:

$$\omega_0 1=\sqrt{\frac{1}{R1\cdot R2}-Gm2\cdot Gm4}$$

$$Q1=\frac{\omega_0 1}{\frac{1}{C}\left(\frac{1}{R1}+\frac{1}{R2}\right)}$$

$$BW1=\frac{1}{C}\left(\frac{1}{R1}+\frac{1}{R2}\right)$$

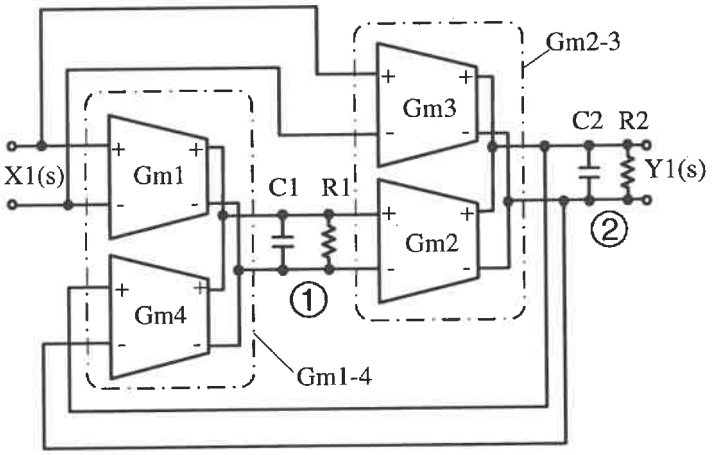


Figure 4: Schéma bloc du filtre de 2ième ordre H1

Les mêmes résultats sont obtenus pour l'autre filtre de 2ième ordre H2. La Figure 5 présente la réglage du facteur de qualité Q des filtres H1 et H2, ainsi que la fonction de transfère du filtre de 4ième ordre.

2. Cellule du Gm

La cellule transconductance Gm constitue l'unité de base du filtre Gm-C utilisé dans le modulateur en mode continu dans le temps. La réalisation des transconductances Gm1-4 (Figure 4) est illustrée à la Figure 6. La valeur de transconductance est donnée par:

$$Gm=2\mu_n C_{OX}\left(\frac{W}{L}\right)V_C$$

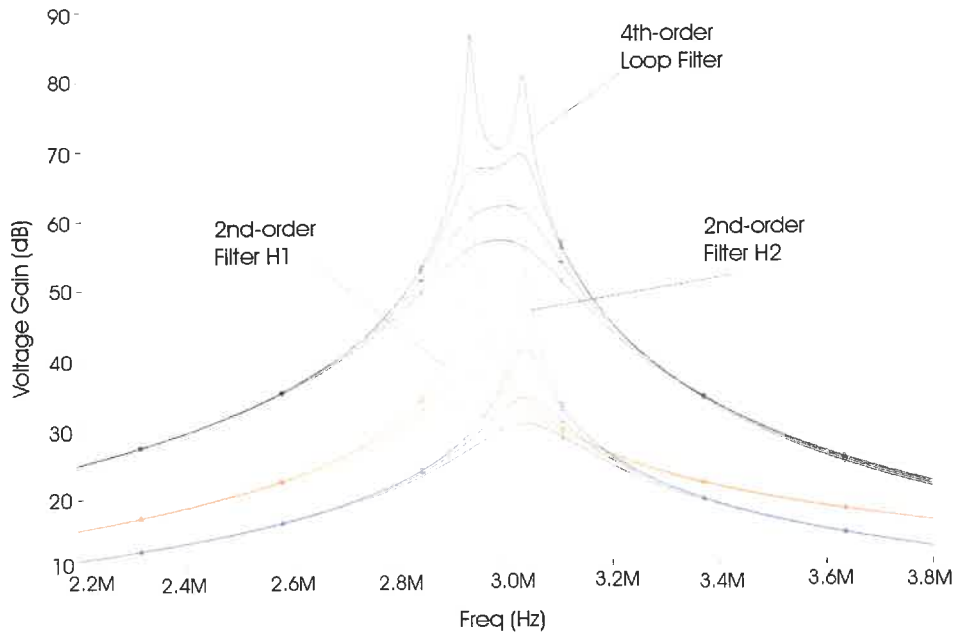


Figure 5: Réglage de Q du filtre de 2ième ordre et du filtre de 4ième ordre

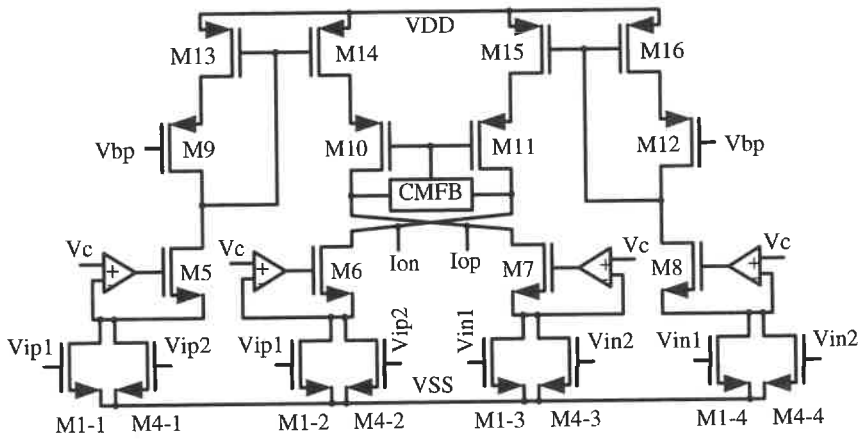


Figure 6: Schéma bloc de la transconductance proposée

Les résultats de simulation de cette transconductance en utilisant l'outil Cadence donne une linéarité de -250 à 250 mV (voir Figure7). La Figure 7 montre également la programmabilité de la valeur de Gm contrôlée par la tension Vc.

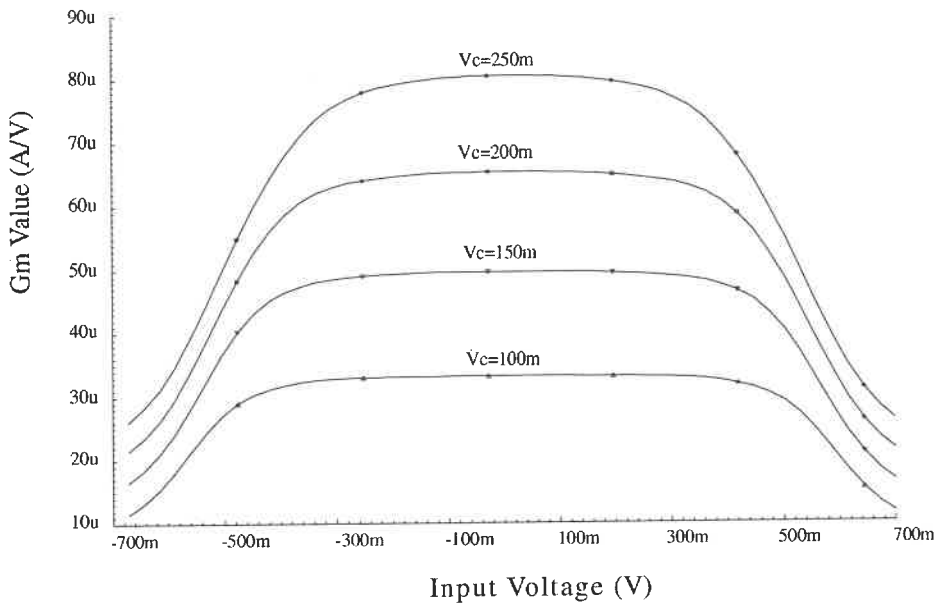


Figure 7: Programmation de la linéarité et de la valeur de la transconductance Gm

3. Quantificateur

Le quantificateur se compose d'un comparateur dynamique et d'une bascule type RS comme représenté à la Figure 8. Pendant la phase de précharge (φ=0), les sorties du comparateur sont chargées à VDD. La bascule RS est utilisé pour maintenir le résultat de la dernière comparaison du comparateur. Quand le signal φ passe de 0 à 1, le comparateur entre dans la phase de comparaison. Les paires M32-M33 et M38-M39 régénèrent et amplifient la différence entre les signaux d'entrés Vip et Vin pour atteindre les niveaux des signaux numériques. Ces signaux numériques résultant sont mémorisés par la bascule RS en attendant la prochaine comparaison.

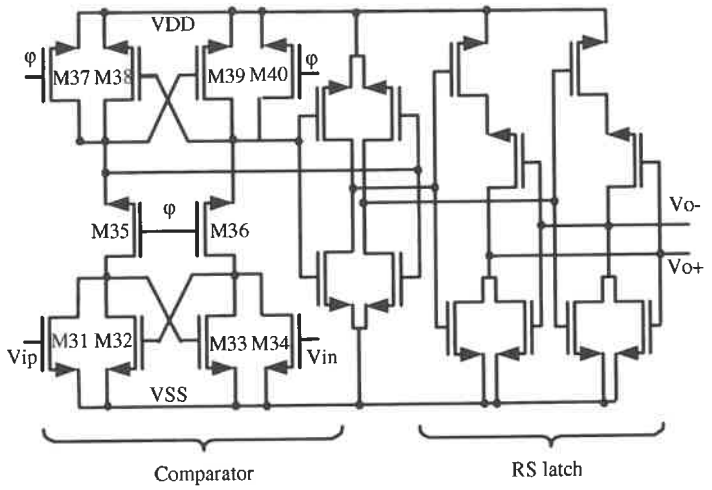


Figure 8: Structure du quantificateur

V. PROGRAMMABILITY DU SYSTÈM

La transconductance proposée peut être ajustée d'une façon continue en utilisant la tension du contrôle Vc ou d'une façon discrète en ajustant les valeurs de W/L. Comme représenté par la fig. 9, une transconductance est ajustée en passant de W1/L1 à W2/L2, puis la tension Vc est utilisé pour l'ajustement final.

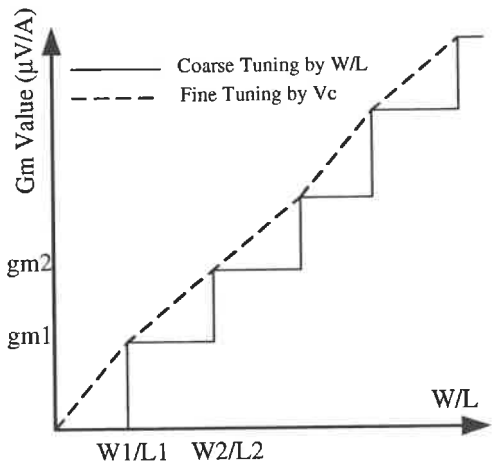
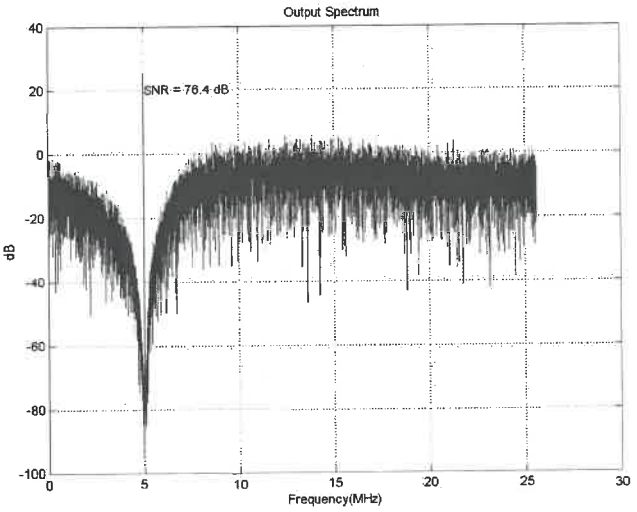
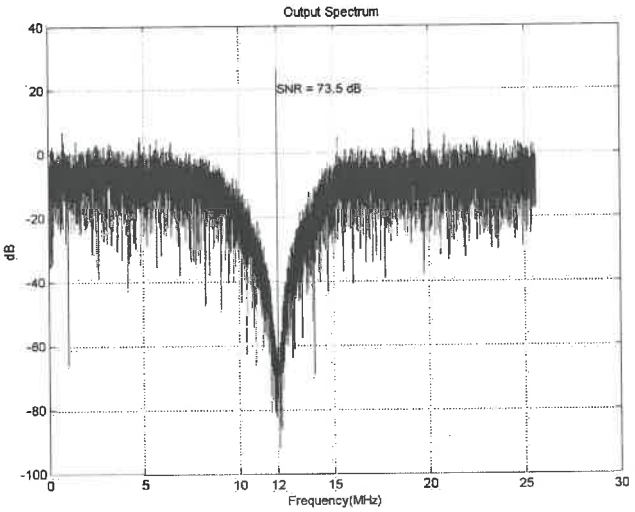


Figure 9: Ajustement de la valeur de la transconductance grossière et fine

La simulation au niveau circuit en utilisant l'outil Cadence prouve que le modulateur peut être programmé de 3 MHz à 5 et 12 MHz par ajustement grossière des W/L (Figure 10). En ajustant la valeur du Vc d'une façon continue et en fixant les valeurs W/L pour le modulateur de 3 MHz, la fréquence centrale de ce dernier peut être ajustée de 1.5, 0.75, 0.375 à 0.1875 MHz (Figure.11).



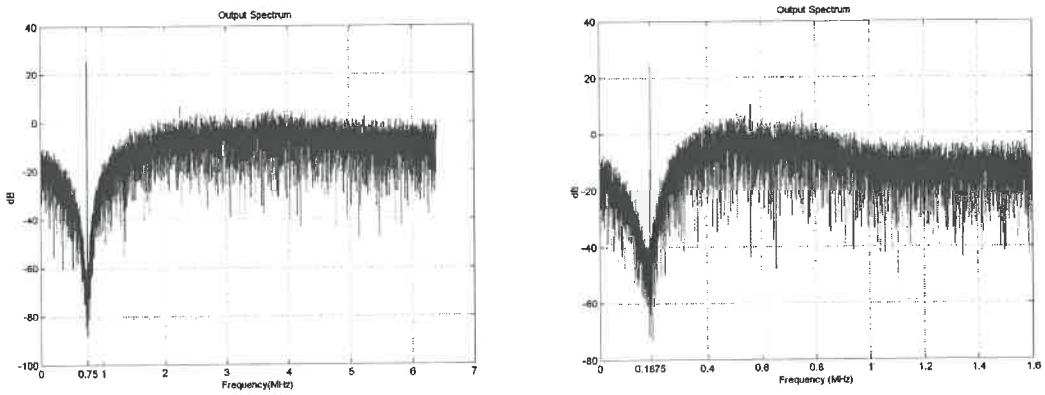
(a)



(b)

Figure 10: Modulateur avec une fréquence centrale de (a) 5 MHz; et (b) 12 MHz

Le design proposé du modulateur de 4ième ordre a été fabriqué en technologie CMOS 0.18 µm offerte par la compagnie Taiwan Semiconductor Manufacturing (TSMC). Les simulations post-layout du modulateur sont obtenues par le simulateur de SpectreS de Cadence.



f_c = 750 kHz; f_S = 12.8 MHz; Vc = 50 mV f_c = 187.5 kHz; f_S = 6.4 MHz; Vc = 12.5 mV

Figure 11: Modulateur programmé par ajustements fins de Vc

Le SNR obtenu de ce modulateur est 78 dB (voir Figure 12). Les résultats de mesure sont effectués avec des spécifications pliées par 4 fois obtenues par l'ajustement de la tension Vc. Avec une fréquence d'échantillonnage de 12.8MHz (un quart de 51.2 MHz originale), le modulateur fonctionne avec une fréquence centrale de 750 kHz et une largeur de bande de 50 kHz. Le spectre mesuré de rendement de ce modulateur plié par 4-fois est illustré à la Figure 13. Dans cette figure la fréquence centrale du signal est de 750 kHz et le SNR est de 58 dB.

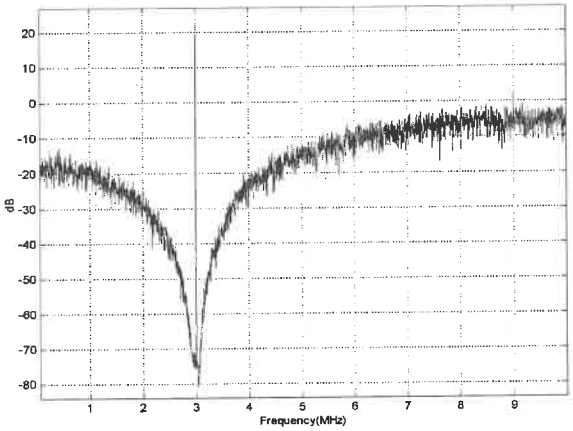


Figure 12: Sortie fréquentielle du modulateur simulé dans Cadence

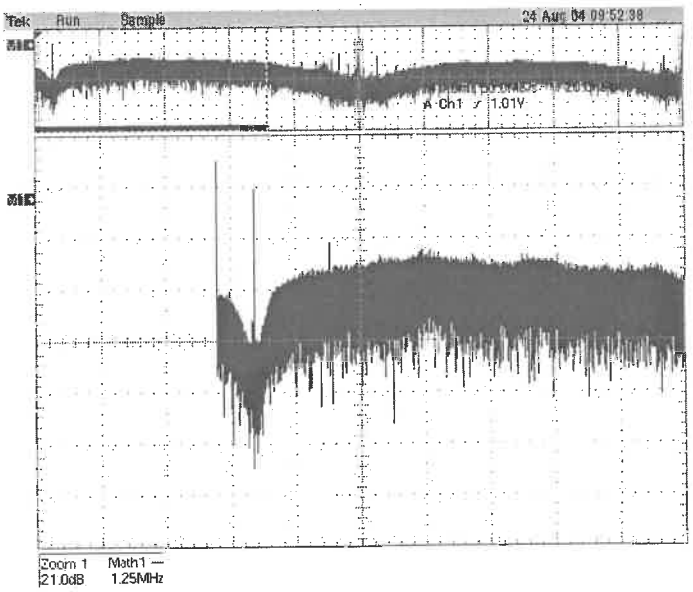


Figure 13: La sortie fréquentielle du modulateur mesurée.

VI. CONCLUSION

Un modulateur Σ-Δ de bande passante centré à 3 MHz est présenté. Le filtre de boucle se compose de deux filtres identiques du type Gm-C de 2ième ordre. Le modulateur de 4ième ordre réalise une gamme dynamique de 78 dB dans une largeur de bande de 200 kHz. Le modulateur peut être ajusté pour différentes fréquences centrales. Le circuit

fabriqué est examiné sous des caractéristiques pliées 4 fois. Implémenté en utilisant la technologie standard du CMOS 0.18μm, le modulateur consomme 2.5 mW puissance d'une tension d'alimentation de 1.8V.

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LIST OF ABBREVIATIONS AND SYMBOLS

ABBREVIATIONS

A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
BW	Bandwidth
CMFB	Common Mode Feedback
C	Capacitor
CMOS	Complementary Metal Oxide Semiconductor
CT	Continuous time
DAC	Digital-to-analog converter
DEM	dynamic element matching
DSP	Digital signal processing
DT	Discrete time
EDA	Electronic Design Automation
Gm	Transconductantor value
Gm-C	Transconductor-capatior circuit
HF	High frequency
LC	Inductance-capacitance
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MASH	Multi-stage noise shaping

$N_{TF}(z)$	Noise transfer function
OSR	Oversampling Ratio
R	Resistor
ΣΔ	Sigma-Delta
SNR	Signal to Noise Ratio
SOC	System-On-Chip
$S_{TF}(z)$	Signal transfer function
TGC	Time gain compensation
TLA	True logarithmic amplification
UHF	Ultra-high frequency
VLSI	Very Large Scale Integration

SYMBOLS

C_{ox}	Gate capacitance per unit area
f_B	Frequency bandwidth
f_{Nyq}	Nyquist rate frequency
$f_Q(x)$	Probability density function
f_S	Sampling frequency
g_m	Transconductance of MOSFET transistor
i_{CM}	Common mode current
i_D	Drain current of MOSFET transistor
K_{DS}	Factor of dynamic scaling
L	Length of MOSFET transistor
μ	Channel mobility of MOSFET transistor
ω_0	Central frequency
Q	Quality Factor
r_{ds}	Drain-source resistance of MOSFET transistor
r_{out}	Transistor output resistance
R_{out}	Transconductor output resistance
V_{CM}	Common mode voltage
VDD	Positive supply voltage
V_{DS}	Drain-source voltage of MOSFET transistor
V_{gs}	Gate-source voltage of MOSFET transistor
V_Q	Quantization error

V_{ref}	Reference voltage
VSS	Negative supply voltage
V_{th}	Threshold voltage of MOSFET transistor
W	Width of MOSFET transistor

CHAPTER 1

INTRODUCTION

Motivation

Ultrasound techniques are widely used for medical diagnostics. With ultrasound it is relatively convenient to get information in the body. Therefore, ultrasound techniques are one of the most commonly adopted medical imaging facilities to identify body abnormalities. Nevertheless, by contrast to their popularity, traditional ultrasonic systems significantly limit their applications inside hospitals by their inherent inconveniences, which mainly come from their bulkiness and high-power consumption.

With the continuing progress in microelectronics technology, the miniaturization of ultrasonic systems or even hand-held device has become feasible and thus attracts great academic and industrial interests. The miniaturization of ultrasonic systems provides not only good density, facility and light weight, but also low power consumption, low noise and high resolution [7]. The block diagram of a state-of-the-art hand-held ultrasound system is illustrated in Figure 1.1, which is proposed by our research team. Ultrasound beams are transmitted and then the attenuated echoes are acquired by the front-end stage. The received beams are successively converted, focused and summed by the digital beamformer for subsequent digital signal processing (DSP). At last, the output of the DSP block is scan-converted and displayed on a LCD. [46]

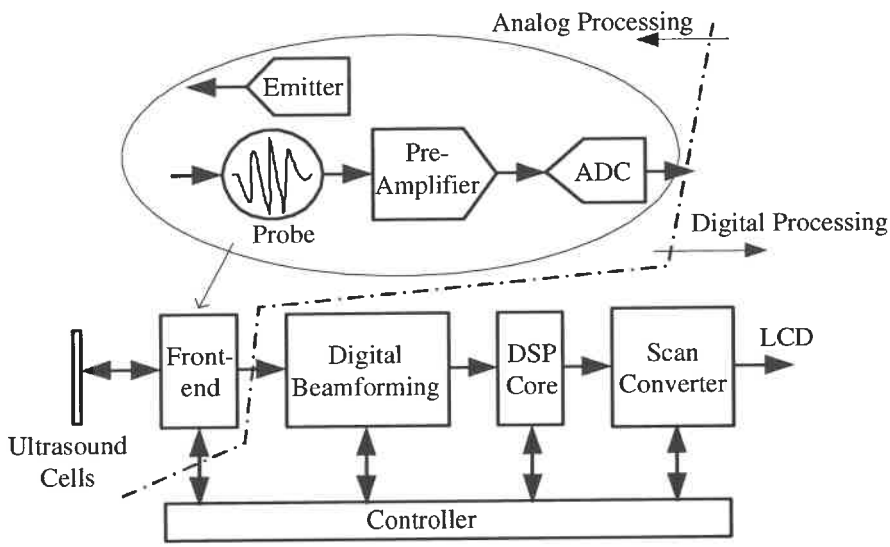


Figure 1.1: Block diagram of the global ultrasonic system

The foregoing signal processing is accomplished through two different procedures, namely analog signal processing and digital signal processing, and the interface is particularly depicted in Figure 1.1 by a dashed-dot line. The multi-channel emitter and receiver in the front-end contribute the most functions of the analog circuit, as shown within the ellipse in Figure 1.1. The probe senses the reflection of ultrasound beams and the attenuated signals are amplified and time-compensated by the pre-amplifier. The analog-to-digital converter (ADC) samples the amplified signals and converts them into digital form for subsequent digital processing. While the digital design benefits tremendously on its speed and calculation capability from the relentless scaling-down of device dimensions, the analog counterpart cannot take the advantage of such progresses easily, or even worse, may suffer more constraints because of short-channel effects. Specifically, the system bottleneck is often located at the ADC, which acts as the interface collecting outside analog signals before postly digital circuits.

Generally, ADCs are classified into Nyquist-Rate Converters and Oversampling Converters according to their sampling frequency. Examples of Nyquist-Rate converters include successive-approximation converters, flash converters and pipelined converters. With the advantage of lower sampling frequency and larger signal bandwidth, Nyquist-Rate converters demand much higher precision on the analog components to reach higher resolution, which inevitably demands substantial efforts on the design and fabrication of analog circuitry. Satisfaction of this demand becomes extremely difficult with short channel devices when a single-chip solution is desired to integrate both the analog and digital circuits together. Besides, performing the A/D conversion with a high-resolution full Nyquist-Rate ADC would be very power inefficient when the channel bandwidth is relatively narrow [43], and thus not an optimum choice for hand-held systems.

On the other hand, oversampling converters relax the accuracy constraints on the analog circuits and higher resolution is still achieved by more complex digital processing. This tradeoff becomes especially attractive for the handheld ultrasonic system where a complete system-on-chip (SoC) solution is highly preferred. Furthermore, quantization noise in oversampling converters from the less accurate analog part can be shaped out of the relevant signal band and thus extra resolution can be obtained. The combination of oversampling and noise shaping is commonly referred to as sigma-delta ($\Sigma\Delta$) modulation and is very popular for applications where high resolution is desired within relatively narrow band. An often referenced qualitative bandwidth and resolution tradeoff of some of these ADC techniques is shown in Figure 1.2 [2].

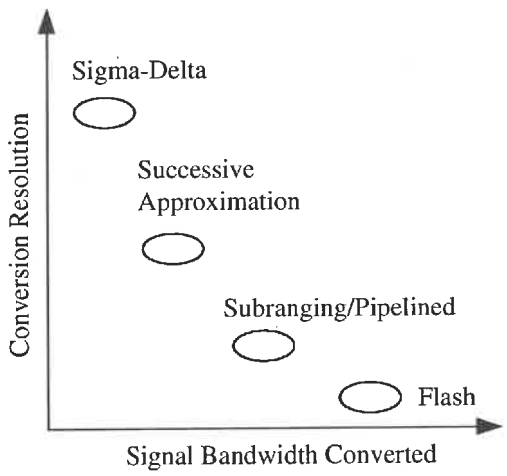


Figure 1.2: Bandwidth resolution tradeoffs

Research Goals

The primary objective of this master thesis is to design a high resolution CMOS Sigma-Delta modulator for ultrasonic receiver dedicated to hand-held ultrasonic system front-ends. According to the system requirement, the modulator has a Signal-to-Noise Ratio (SNR) of more than 72 dB over a bandwidth of 200 kHz and can be programmed with 3, 5, 7, 12 and 20 MHz central frequencies for different applications. So, facilities for programmability are taken into account in the modulator structure and circuit level design. It must be quite power-efficient to serve in hand-held systems. These performances are realized in standard 0.18 μm CMOS process to enable full integration of both analog and digital circuits on a single chip. Such a single chip solution is essential, not only to reduce the system size, but also to simplify the communication between analog and digital circuits and benefit both system speed and power dissipation. Besides, the properly selected modulator architecture should demonstrate adequate robustness

against transistor mismatches aroused by process parameter tolerances and temperature gradients, so that it can be of practical values both in its present research and future industrial production phases.

Master Thesis Organization

Following this introduction chapter, the fundamental theories of quantizing and ΣΔ modulation will be introduced in Chapter 2. Starting from the characteristics of the quantization noise of Nyquist ADC, effective performances of oversampling and noise shaping on the ADC resolution are unfolded step by step.

Architecture level considerations of ΣΔ modulator are given in Chapter 3. High level descriptions and/or simulations of various ΣΔ modulator structures are detailed. After careful comparison and analysis of different potential candidates of modulator realization, such as low-pass vs. bandpass, single-bit vs. multi-bit, discrete-time vs. continuous-time and cascaded vs. interpolative topologies, conclusions are made and the system level parameters and characteristics are settled.

This master thesis also includes the article "A 1.8V CMOS Fourth-Order Gm-C Bandpass Sigma-Delta Modulator Dedicated to Front-end Ultrasonic Receiver", which was submitted for publication. The article is presented in Chapter 4 in which detailed circuits realization and analysis are made. Conclusive results of the verification and test of the fabricated modulator for 3 MHz application are also given in Chapter 4. In Chapter 5, the programmability of the proposed modulator topology for other application frequencies, such as 5, 7, 12 and 20 MHz, are analyzed and developed. Simulations of the

programmability on schematic level by Electronic Design Automation (EDA) tools are detailed in this Chapter. Conclusions and future work are presented at the end of this thesis.

CHAPTER 2

FUNDAMENTAL THEORIES OF ΣΔ MODULATION

2.1 Introduction

Sigma-Delta modulation has been widely adopted as a valuable choice for high-resolution and relatively low speed ADC applications. The main advantage is that this high resolution is achieved by rather low accurate analog circuit or sometimes even one-bit quantizers. Even though one-bit quantizers generate significant quantization noise, such noise can be greatly attenuated by oversampling and further be shaped out of the desired signal band.

In this chapter, characteristics of the quantization noise from quantizer are first introduced. After effects of sampling on the signal and the drawbacks of Nyquist ADC are briefly analyzed, the performance of oversampling on increasing ADC resolution is analyzed in section three. In section four, ΣΔ configuration is described by introducing feedback and loop-filter into the oversampling system, followed by theoretical calculates of ideally achievable SNR. Then, an important issue of modulator stability, which practically limits the modulator SNR are examined in section 5. Conclusions are made in the last section.

2.2 Characterization of Sampling and Quantization

All ADC modulators perform basically two functions: sampling the signal at well defined and fixed time intervals; and quantizing the amplitude of sampled signals and

representing them in the form of digital word streams [2]. Supposing the signal to be treated is located at base-band and is band-limited within f_B. Sampling the signal with a frequency f_S replicates the base-band signal spectrum in the frequency domain, at multiples of f_S. This procedure is illustrated in Figure 2.1, where the spectrum replicas are shown in dashed lines.

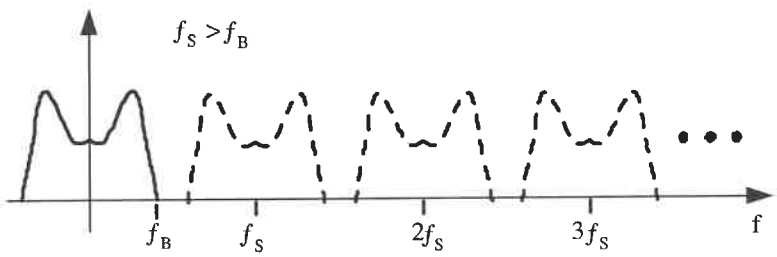


Figure 2.1: Sampling effect on signal spectrum

If a replica overlaps with the base-band signal, the signal is damaged, or aliased. To avoid any aliasing during sampling, the signal should be band limited to $f_S/2$, or equivalently, the sampling frequency should be greater than Nyquist rate f_{Nyq}, which is defined as

$$f_{Nyq} = 2f_B. \tag{2.1}$$

The sampled signals V_{in} are then quantized into N bits words representing 2^N different levels. This procedure can be modeled as:

$$V_{in} + V_Q = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \cdots + b_N 2^{-N}), \tag{2.2}$$

where b_1, b_2, ..., b_N denote the output word, the reference voltage V_{ref} defines the relationship between a voltage value and its digital representation. V_Q is defined as the quantization error and exists even for an ideal ADC, because a continuous-amplitude

signal is represented by a step signal with only 2^N levels and in general there is a difference between the two. If we define the V_{LSB} to be the voltage represented by one Least Significant Bit (LSB) change, that is,

$$V_{LSB} = \frac{V_{ref}}{2^N}, \tag{2.3}$$

and if the quantizer is not overloaded, or in other words, the amplitude of the input signal to the quantizer is well bounded by

$$-\frac{1}{2}V_{LSB} \leq V_{in} \leq 2^N V_{LSB}, \tag{2.4}$$

V_Q is apparently limited by

$$|V_Q| \leq \frac{1}{2}V_{LSB}. \tag{2.5}$$

Under the assumption that the sampled signals are varying rapidly such that V_Q becomes a random variable uniformly distributed between the range of $\pm\frac{V_{LSB}}{2}$, the probability density function $f_Q(x)$ of the error process is a constant value of $\frac{1}{V_{LSB}}$ within the same range and is zero otherwise. Thus, V_Q can be defined as a zero mean variable [2, 30], and the power of which is calculated as

$$P_Q = \int_{-\infty}^{\infty} x^2 f_Q(x)dx = \frac{1}{V_{LSB}}\int_{-V_{LSB}/2}^{V_{LSB}/2} x^2 dx = \frac{V_{LSB}^2}{12}. \tag{2.6}$$

According to equation (2.6), P_Q is independent of the sampling frequency. For sinusoidal inputs with an amplitude of $\frac{V_{ref}}{2}$, the amplitude range satisfies equation (2.4) and so an

ADC subjected to this input is not overloaded. The SNR for N-bit ADCs can be calculated by

$$\mathrm{SNR} = 10\log\left(\frac{P_{in}}{P_Q}\right) \tag{2.7}$$

$$= 10\log\left(\frac{V_{ref}^2/8}{V_{LSB}^2/12}\right)$$

$$= 10\log\left(3\times 2^{2N-1}\right)$$

$$= 6.02\mathrm{N} + 1.76,$$

showing the best performance that a N-bit Nyquist ADC can achieve on its SNR.

To simplify calculations while being reasonably accurate, the quantization noise is assumed to be a white and statistically uncorrelated, which has been shown to be reasonable under the conditions that the quantizer is not overloaded, N is large and the successive signal values are not excessively correlated [5][23]. In the frequency domain, the power of such a white noise, which is expressed in (2.6), are folded into the frequency band $-f_S/2 \le f \le +f_S/2$ with a constant spectral density therein as

$$S_Q^2(f) = \frac{V_{LSB}^2}{12}\frac{1}{f_S}; \quad -f_S/2 \le f \le +f_S/2 \tag{2.8}$$

If f_S is adopted as Nyquist frequency, the total noise power falls into the signal band [24][30].

2.3 Performance of Oversampling

High resolution Nyquist rate converters are heavily dependent on the accuracy of the implementation which is getting much more difficult in deep-submicron VLSI circuits. Another practical drawback of sampling at Nyquist rate is due to the difficulty of realizing an anti-aliasing filter with very sharp cutoff performance. Practically, in order to strictly limit the input signal power within $f_S/2$, Nyquist rate converters normally operate at 1.5 to 10 times the Nyquist rate to relax the constraints on the anti-aliasing filter [30].

Further increasing the sampling frequency to a much higher rate than Nyquist rate not only relaxes the performance requirement on the anti-aliasing filter, but also largely decreases the in-band quantization noise. If the input signal is band limited by $-f_B \leq f \leq +f_B$, the in-band quantization noise power is equal to

$$P_Q = \int_{-f_S/2}^{f_S/2} S_Q^2 df = \frac{2f_B}{f_S}\frac{V_{LSB}^2}{12} = \frac{V_{LSB}^2}{12}\left(\frac{1}{OSR}\right), \tag{2.9}$$

where OSR is defined as the ratio of sampling frequency to Nyquist rate frequency:

$$OSR = \frac{f_S}{2f_B}. \tag{2.10}$$

As illustrated in Figure 2.2, the power of the quantization error of a Nyquist rate ADC is focused within the signal band. While for an oversampling ADC, the same amount of error power is extended over greater frequency range and only one part of the power falls into the signal band, hence, the achievable SNR within the signal band is significantly increased. The SNR performance of an oversampling ADC is then

$$\text{SNR} = 10\log\left(\frac{P_{in}}{P_Q}\right) = 10\log\left(\frac{V_{ref}^2/8}{\frac{1}{OSR}V_{LSB}^2/12}\right) = 10\log\left(2^{2N-1}\cdot 3\right) + 10\log(OSR), \qquad (2.11)$$

or

$$\text{SNR} = 6.02\text{N} + 1.76 + 10\log(OSR). \qquad (2.12)$$

That is, every doubling of OSR contributes 3 dB improvement to the SNR of the ADC. This effect can also be intuitively examined in Figure 2.2.

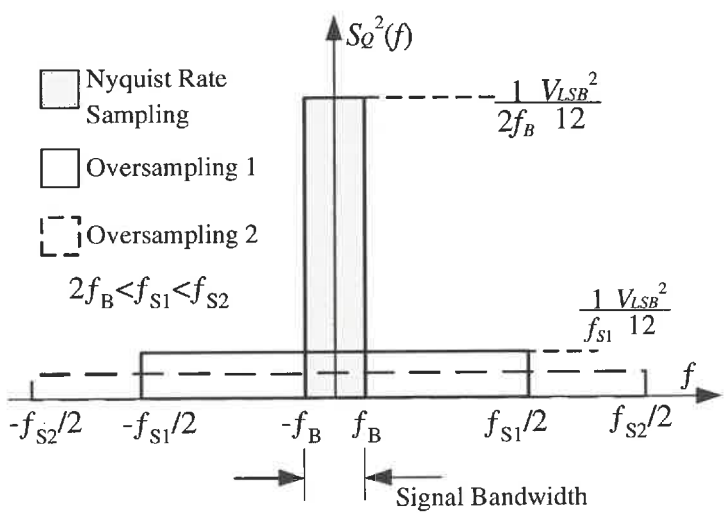


Figure 2.2: Oversampling effect on noise spectral density

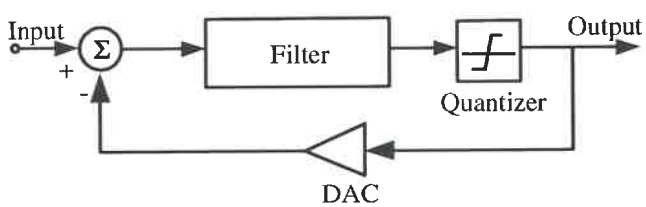
The noise power outside the signal band can be greatly attenuated with a digital low-pass filter after the modulator. It leaves only the high resolution narrow-band signal at the oversampling ADC output.

2.4 Sigma-Delta: Oversampling plus Noise Shaping

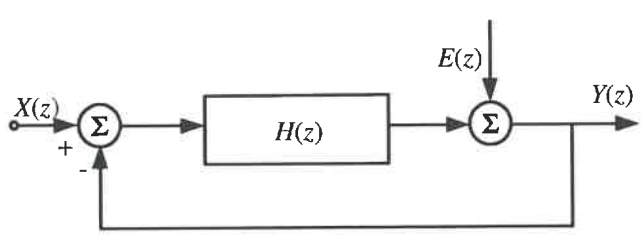
Oversampling ADC trades speed for the high resolution, i.e., extra resolution is achieved by an increase of system sampling rate. However, asking for extraordinary SNR

for higher resolution calls for either small signal band or high f_S. Sometimes, requirement of the system on its signal band can lead to extremely high f_S that exceeds the maximum attainable speed supported by the system or the technology used to implement the ADC. To relax the requirement of extremely high sampling frequency, noise shaping is adopted to achieve extra resolution beyond the capability of an oversampling ADC.

As shown in Figure 2.3 (a), noise shaping technique makes use of feedback from the quantizer output to the modulator input and incorporates a filter on the feed-forward loop. If the filter has a high gain at the signal band, a deep negative feedback is formed and the output spectrum is forced to approximate that of the input within the signal band. Thus, even though the output is rather noisy out of the relevant frequency band, high resolution can be achieved within the signal band.



(a)



(b)

Figure 2.3: Sigma-Delta modulator and its linear model

(a) modulator structure (b) linear model in Z form

In Figure 2.3 (b), the effect of quantization noise is considered as white noise source as what is done in section 2.2 and shown in its Z domain form as E(z). From this model, the signal transfer function STF(z) and the noise transfer function NTF(z) can be derived:

$$S_{TF}(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)}, \tag{2.13}$$

$$N_{TF}(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)}, \tag{2.14}$$

and

$$Y(z) = S_{TF}(z)X(z) + N_{TF}(z)E(z). \tag{2.15}$$

If $H(z)$ has pole(s) located in the signal band and its magnitude is large enough within the bandwidth, $S_{TF}(z)$ approximates to unity and $N_{TF}(z)$ to zero from equations (2.13) and (2.14). Thus in the output shown in equation (2.15), the signal is almost unaffected and quantization noise is largely attenuated.

When the quantization noise is subjected to a 1st-order Noise Transfer Function, its spectral density is

$$S_{Q-1}^{2}(f) = S_Q^{2}(f)\left|1-e^{-2j\pi f/f_S}\right|^2 = \frac{V_{LSB}^{2}}{12}\frac{1}{f_S}\left[2\sin(\pi f/f_S)\right]^2. \tag{2.16}$$

The in-band quantization noise power becomes

$$P_{Q-1} = \int_{-f_B}^{f_B} S_{Q-1}^{2}\,df = \frac{V_{LSB}^{2}}{12}\frac{\pi^2}{3}\left(\frac{2f_B}{f_S}\right)^3 = \frac{V_{LSB}^{2}}{12}\frac{\pi^2}{3}\left(\frac{1}{OSR}\right)^3. \tag{2.17}$$

Thus the achievable SNR of a first order noise shaping modulator is given by

$$\text{SNR} = 10\log\left(\frac{P_{in}}{P_{Q-1}}\right) = 10\log\left(\frac{V_{ref}^{2}/8}{\frac{V_{LSB}^{2}}{12}\frac{\pi^2}{3}\left(\frac{1}{OSR}\right)^3}\right)$$

$$= 6.02N + 1.76 - 5.17 + 30\log(OSR). \quad (2.18)$$

Compared to equation (2.12) where an oversampling ADC gets an extra 3 dB accuracy for every doubling of *OSR*, here a 1st-order ΣΔ modulator can get an extra 9 dB, in which 6 dB is contributed by 1st-order noise shaping.

Similarly, for a second order ΣΔ modulator, the maximum SNR is given by

$$SNR = 6.02N + 1.76 - 12.9 + 50\log(OSR), \quad (2.19)$$

and for Lth-order modulator

$$SNR=6.02N + 1.76 - 20L\log(\pi) + 10\log(2L+1) + 10(2L+1)\log(OSR). \quad (2.20)$$

The performance of noise shaping is illustrated in Figure 2.4 by comparing it with the performance of oversampling ADCs [30]. From the figure, it is clearly depicted that higher order modulator has more ability to push quantization noise out of the frequency band of interest.

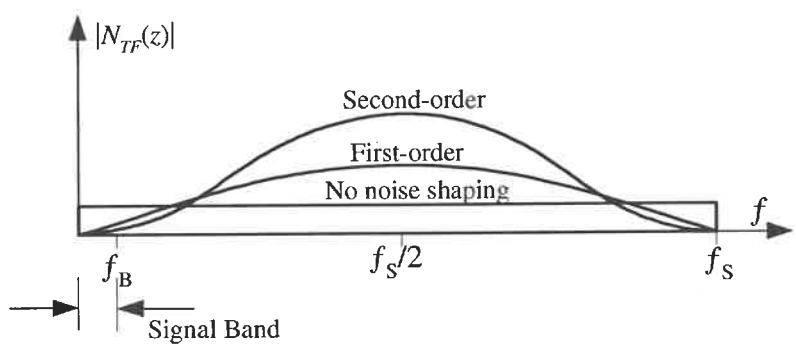


Figure 2.4: Noise-shaping effect of ΣΔ modulator

2.5 Modulator Stability

Like other systems comprising feedback loop, the system stability of ΣΔ modulator is a significant issue that requires much attention. A stable modulator is defined as one in which the inputs to the quantizer remains bounded such that the quantizer is not overloaded [30].

Because of the highly nonlinear feature of the quantizer, the analysis of the modulator stability becomes extremely difficult. Quite a lot of work was devoted to examine, analyze and explain the stability issue [1] [25] [47]. A broadly adopted rule of thumb for a stable modulator is proposed in [6] as

$$|N_{TF}(z)| \leq 1.5\,, \tag{2.21}$$

that is, the maximum out-band gain of the Noise Transfer Function can not be too high. Lower maximum gain gives a more stable modulator with the trade-off of lower SNR performance as less noise power is pushed out of the signal band. Higher maximum gain explores more space for achievable SNR but at the risk of driving the modulator into unstable state.

The stability issue can be reflected by the limit on the maximum amplitude of the input signal. When the input signal power increases from a relatively small quantity, the SNR increases linearly according to equation (2.7), and is limited by the in-band noise. When the modulator input approaches its full scale, the high gain of the loop filter causes the input to the quantizer to be so large that the quantizer is overloaded. The full scale input is defined as one whose magnitude is equal to the maximum magnitude of the

quantizer feedback [9]. Such an overload noise manifests itself as harmonic distortion tones for sinusoidal inputs [39] and the signal harmonics within the signal band begin to damage the SNR. As a result, the increase of SNR appears to be saturated instead of a linear increase. Further, when the increase of the power of harmonics exceeds that of the input, the SNR indeed decreases. Eventually extremely high input power drives the modulator into an unstable state.

The process is illustrated in Figure 2.5 where the SNR is plotted against input amplitude referenced to full scale in dB. Before input amplitude reaches –15 dB, the modulator SNR increases linearly at 1dB/dB. After that, the quantizer begins to be overloaded and SNR increases at a slower rate and at last the modulator reaches its maximum SNR of 86.3 dB when input is –4 dB. This is the point where the increase of the input power is totally counteracted by the increase of harmonics power caused by an overload of the quantizer. Further increasing of input amplitude leads to decreasing of SNR as harmonics power dominates the input power. It is also noticed in Figure 2.5 that system SNR reaches 0 dB when signal magnitude is –88 dB. This 88 dB is defined to be the modulator Dynamic Range, which is equivalent to the resolution of the modulator as an ADC. Thus, the modulator with the performance shown in Figure 2.5 has a equivalent accuracy of 14.6 bits.

2.6 Conclusion

We introduced in this chapter the features of quantization noise and then theoretically examined the performance of oversampling ΣΔ ADCs. It is demonstrated that even with

coarse analog components, high resolution can be achieved within the narrow signal band owing to oversampling and noise shaping. At last, modulation stability issue was discussed and its influences on the maximum input amplitude and on the maximum achievable SNR were reviewed.

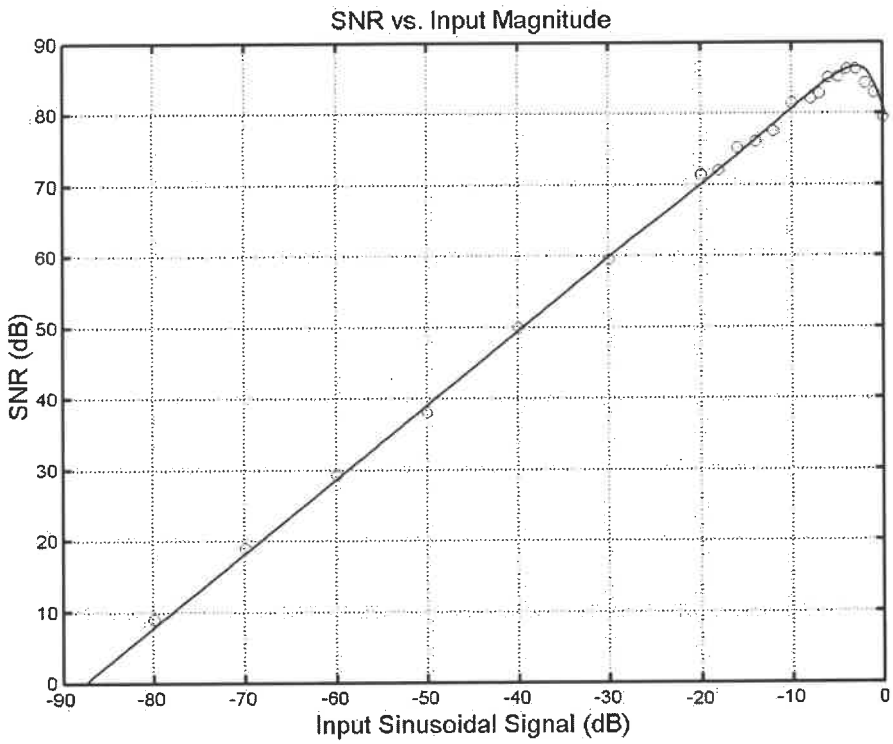


Figure 2.5: Dynamic range plot for an ideal 4th-order bandpass ΣΔ modulator

CHAPTER 3

ARCHITECTURE LEVEL CONSIDERATION OF THE ΣΔ MODULATOR DESIGN

3.1 Introduction

Internal quantizer resolution (N), oversampling ratio (OSR) and noise-shaping order (L) are the three parameters that give plenty of possible candidate modulator architecture for a given resolution. Careful analysis should be made between trade-offs in order to set up the modulator architecture which is most favorable to the targeted design.

We elaborate in the next section our system requirements. In Section 3.3, a theoretical achievable modulator SNR is defined, giving enough margin to overcome the effects of circuit imperfections. Then, possible candidates for the targeted modulator SNR are listed, intensive analysis of the tradeoffs is performed between single- and multi-bit quantizers, low- and high-order noise-shapings, and the features of the modulator will be specified. In section 3.4, possible circuit architectures will be discussed. Then the difference between low- and band-pass concepts, discrete and continuous time domain realization methods are presented, together with their associated advantages and disadvantages. At last, a comparison is made between two high order modulator structures, i.e. interpolative and MASH topologies.

3.2 System Requirements

The targeted resolution of this modulator is 12 bits which corresponds to a SNR of 72 dB, within a signal bandwidth of 200 kHz. The signal carrier can be tuned at the following frequencies: 3, 5, 7, 12 and 20 MHz, which are dedicated to different applications. The circuitry is compatible with a complete system integration in a standard 0.18 μm CMOS process. To be embedded in a SoC of a handheld instrument, the modulator power consumption must be limited within the scale of milliwatts.

3.3 Parameters Specification

According to Equation (2.21), the theoretical accuracy of a Σ-Δ modulator depends on the resolution of its quantizer and extra resolution contributed by oversampling and noise shaping. For system stability concerns, the maximum input signal is limited to be much less than the full-scale input whose magnitude equals the maximum magnitude of the quantizer feedback [9]. Besides, the system realization also suffers from various circuit imperfections such as amplifier finite gain, circuit mismatch or non-accuracy, excessive loop delay and clock jitter. As a result, the achieved resolution is significantly degraded compared with the theoretical result. Table 3.1 summarizes the main published Σ-Δ modulators. It is observed that the achieved SNRs have an average degradation of 30 percent compared with the achievable SNRs. Therefore, to reach our targeted converter resolution which is 72 dB by measure of SNR, the theoretically achievable modulator SNR should be not less than 100 dB. Table 3.2 illustrates different orders of noise shaping combined with different quantizer resolutions and sampling frequencies, and in

last column the achievable maximum SNR. Among all the modulator specifications that lead to achievable SNR over 100 dB, we can find modulators with higher OSR, lower L and/or less N, together with modulators with lower OSR, higher L and/or larger N. The tradeoffs between these candidates will be examined carefully in the following section before final decision on the most desirable OSR, L and N is made.

Table 3.1. Main Published Works

Signal Band	Sampling Frequency	OSR	Modulator Structure	Resol. Achieved	Resol. Achievable	Ref.
500 Hz	128 kHz	128	4th order 1 bit / LP	120 dB	167 dB	[32]
4 kHz	4 MHz	500	1st order 1 bit / LP	78 dB	84 dB	[34]
20.5 kHz	5.25 MHz	128	2nd order 4 bits/LP	96 dB	118 dB	[45]
40 kHz	10.24MHz	128	2nd order 1 bit/LP	84 dB	100 dB	[39]
250 kHz	32 MHz	64	4th order 1 bit / LP	84 dB	140 dB	[40]
200 kHz	280 MHz	700	2nd order 1 bit/BP	42 dB	88 dB	[26]
1.1 MHz	35.2 MHz	16	3rd order 5 bit / LP	84 dB	95 dB	[54]
276 kHz	53 MHz	96	2nd order 3 bit/LP	82 dB	106 dB	[19]
1.25 MHz	80 MHz	32	8th order 1 bit / BP	75 dB	113 dB	[44]

3.3.1 Internal Quantizer Resolution

According to Table 3.2, multi-bit quantizer increases the modulator resolution by 6 dB per extra bit. Furthermore, multi-bit quantizer also potentially offers better modulator

stability. Because of the inherently non-linear nature of the quantizer, the stability analysis of the overall modulator becomes rather complicated. As multi-bit quantizers have better linearity than single-bit ones, the behaviour of multi-bit ΣΔ modulators more closely follow that predicted by the linearized model in Figure 2.3. Therefore, the stability of the modulator is better predicted [2].

However, a multi-bit quantizer necessitates the use of a multi-bit DAC to feed the output digital words back to the modulator input in analog form. The non-linearity of the DAC can be modeled as a noise source, but this noise cannot be filtered out like the quantization noise. Therefore, the DAC linearity is requested to be comparable to the accuracy of the modulator. In our case, implementing a DAC of 12 bits linearity necessitates extra techniques such as dynamic element matching (DEM) [22] or adaptive error compensation techniques [53]. The demand for high performance circuits runs in the opposite direction to the motivation of adopting Sigma-delta modulation, which is to relax the demand of high accuracy analog circuit.

On the other hand, single-bit DAC has only two output levels and as two points define a straight line, single-bit DAC is inherently linear and thus highly linear converter can be implemented [30]. In fact, the inherent linearity has contributed to make single-bit DAC to dominate most sigma-delta modulator applications [26] [40] [44]. Besides, as the single-bit format is compatible for serial data transmission and storage systems, and its processing is reduced to few logic operations, the post-modulator data treatment in the digital domain is simplified [6].

Corresponding to single-bit DAC, a comparator is used as a two-level quantizer. If the oversampling ratio and/or the order of noise shaping of the modulator is high enough, an overall high resolution and high linear modulator can be realized.

3.3.2 Noise-shaping Order and OSR

As shown in Table 3.2, high resolution of more than 100 dB SNR can be realized by 1-bit internal quantizer under first, second and third order noise shaping and the corresponding least oversampling ratio. Compared with first order noise shaping, the second one demonstrates its advantage as it relaxes both the oversampling ratio and the sampling frequency. Even though third or higher order noise shaping can further reduce the sampling frequency, unfortunately, it tends to suffer from instability [15].

Avoiding the complex issue of stability in high order modulator, the second-order noise shaping modulator with one-bit internal quantizer and 51.2 MHz sampling frequency at last demonstrates itself as a good compromise for this project.

3.4 Architecture Level Consideration

3.4.1 Choice of Bandpass against Low-pass ΣΔ Modulator

The transfer function of a low-pass ΣΔ modulator offers an adequate high DC gain so that the resulting noise transfer function can push the quantization noise away from DC. By contrast, in the case of a bandpass ΣΔ modulator, its loop filter must be a narrow bandpass one to offer a high gain around the carrier frequency. Thus, high resolution can be achieved around the carrier frequency in the same way as in the low-pass case

(Chapter 2), except that the quantization noise is shaped out within the interested signal band instead of around DC.

The disadvantage of low-pass Σ-Δ modulator in this project is straightforward. The modulator resolution depends on OSR (Equation (2.21)), and OSR is inversely proportional to f_B (Equation 2.11). For low-pass modulator, f_B is the highest in band signal frequency. For an application around 20 MHz, f_B is the central frequency plus half the bandwidth of 200 kHz, which is 20+0.2/2= 20.1 MHz. As the denominator in Equation (2.11) becomes such a big value, the system sampling frequency can be nonrealistic in order to achieve an adequate OSR and further the targeted system resolution. For example, an OSR of 50 will lead to a sampling frequency over 2 GHz.

On the other hand, in bandpass ΣΔ modulation, f_B is the signal bandwidth and independent of the carrier frequency. Thus, high OSR can be easily achieved with an acceptable sampling frequency. In our case where the signal bandwidth is 200 kHz, a sampling frequency of 20 MHz can easily lead to an OSR of 50. Comparing to the low-pass one with 2 GHz sampling frequency, bandpass modulation demonstrates a significant advantage.

It is important to note that, a 2N-th order bandpass ΣΔ modulator is equivalent to a N-th order low-pass ΣΔ modulator to the effect of noise shaping capability. In the 2nd-order low-pass case (Figure 3.1a), the loop filter offers two 2 poles at DC and thus the noise transfer function has 2 zeros at DC level which contribute to noise shaping. In the 4th-oder bandpass case, it is assumed that $f_c = f_s/4$ without loss of generality. The narrow

bandpass loop filter offers 4 poles and hence corresponding noise transfer function offers 4 zeros at $e^{\pm j\pi/2} = \pm j$. Mapped to z-plane in Figure 3.1b, two real zeros are located at $f_s/4$ and two imaginary ones are at $3f_s/4$, forming 2 conjugate pairs. Apparently, only the two zeros at $f_s/4$ contribute to shape the quantization noise away from the signal band which is assumed to be around $f_s/4$. As a result, 2N-th order bandpass Σ-Δ modulator gives N-th order noise shaping. In this project where the noise-shaping is decided to be 2nd-order, a 4th-order bandpass noise-shaping should be realized.

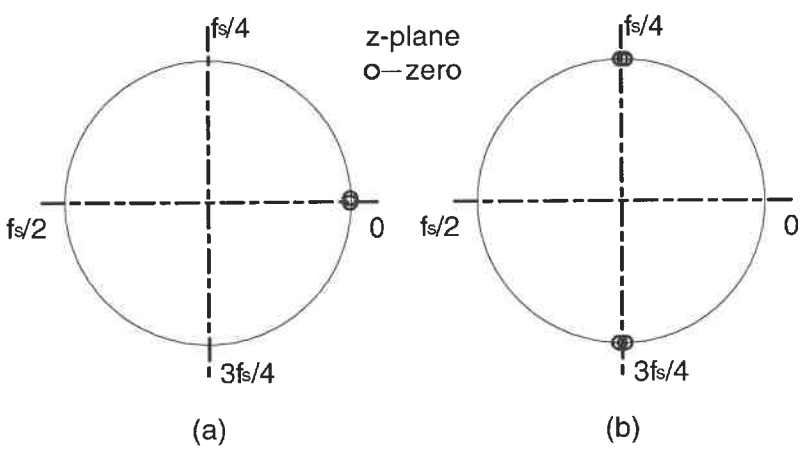
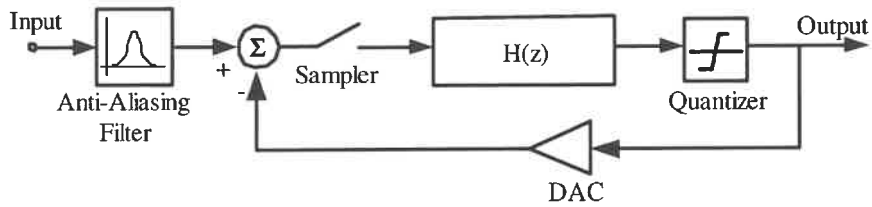


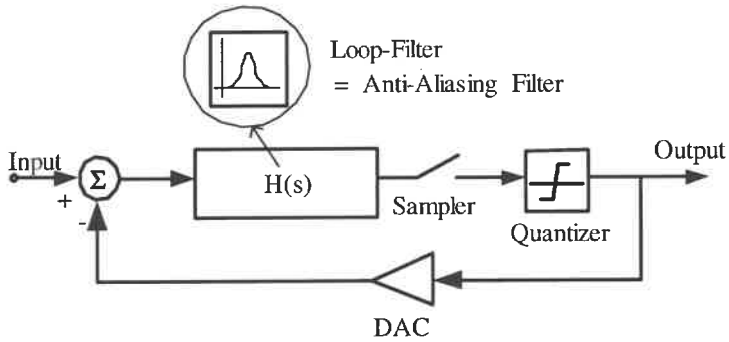
Figure 3.1: Noise Shaping Capability: (a) 2nd-order low-pass; (b) 4th-order bandpass

3.4.2 Choice of Continuous-Time Realization Against Discrete-Time Realization

The loop filter of the modulator can be implemented in either discrete or continuous time techniques and the sigma-delta modulators are referred to accordingly as discrete-time and continuous-time modulator (Figure 3.2).



(a)



(b)

Figure 3.2: Type of Modulators: (a) Discrete-Time Modulator;

(b) Continuous-Time Modulator

Discrete-time modulators, mostly implemented by switched-capacitor techniques, usually dominate the delta-sigma ADC applications, due to their robustness and the intuitive matching between the mathematical model and circuitry implementation [14, 27, 36, 41, 50]. However, this technique significantly suffers from the settling problem. In fact, the integration is realized by charging and discharging capacitors through operational amplifiers, and the unity-gain bandwidths of the amplifiers must usually be at least five times the clock frequency. This not only limits the operating frequency but also

leads to high power consumption. By contrast, continuous-time modulators totally relax the settling constraint and thus can sample the signal at much higher frequency and in turn can increase the modulator resolution and/or bandwidth.

Besides, as sampling of the input to the modulator and of the output of feedback DAC are conducted at the input of the first integrator, switched-capacitor modulator is quite sensitive to circuit nonidealities at the input. As a result, the required integrator's performance must have an accuracy comparable to the overall targeted modulator precision, which inevitably increases the complexity and power consumption of the circuit [4][49]. For continuous-time modulator, the sampling is conducted between the loop-filter and quantizer and thus inside the noise-shaping loop. Any effect of sampling nonidealities, such as quantization errors, can be largely shaped out of the signal band of interest.

Furthermore, unlike the switched-capacitor modulator where sampling is performed at the input node of the modulator and an anti-aliasing filtering should be conducted on the input signal before the input node (Figure 3.2a), the continuous-time modulator performs its sampling after the loop filter (Figure 3.2b). Thus, the signal to be sampled is already filtered by the loop-filter with an equivalent effect of anti-aliasing filtering. Thus, in continuous-time modulator, intrinsic anti-alias filtering is conducted at no cost of circuitry and power [9][49].

Continuous-time modulators can be realized by either Gm-C or LC resonators. Even though LC resonators generally promise a simpler modulator structure [20], the traditional off-chip inductors complicate the design process [28] [51]. The availability of

monolithic inductors in recent years has introduced many totally integrated LC continuous-time ΣΔ modulators with good resolution [10][20][29]. But as monolithic inductors typically have poor quality factors below about 1 GHz, the technology only becomes practical for HF or UHF applications and in advanced technologies [20]. In contrast, Gm-C modulators offer both complete integrated system and design freedom for medium or lower speed applications. It is thus the best choice for our application.

3.4.3 Interpolative or Mash Approach for Higher-order Modulator

Higher-order modulators are generally realized through two approaches, namely interpolative and MASH. The former one is typically constructed by a high-order loop-filter with the modulator in the general form like in Figure 3.2(b), where quantized signal is fed back to the modulator input. The latter approach of MASH consists of a cascade of lower-order modulators, where the latter modulators are used to cancel the noise errors introduced by the earlier modulators (Figure 3.3) [30].

MASH (Multi-stage noise shaping) was first introduced in [52] and was named in [35]. Since then, it has been widely adopted for higher order ΣΔ modulators [14] [18] [33]. The basic idea of MASH is to feed the quantization error of the first stage modulator into the second stage one. The output bit-streams of the two modulators are then post-filtered properly and combined together in such a way that the quantization error of the first stage modulator is canceled and that of the second stage modulator experienced another noise shaping by the post-filter in the digital domain. Since lower-order modulators tend to be

more stable, the higher-order modulators obtained as a cascade of lower-order ones with the MASH approach behave much better performance in terms of stability.

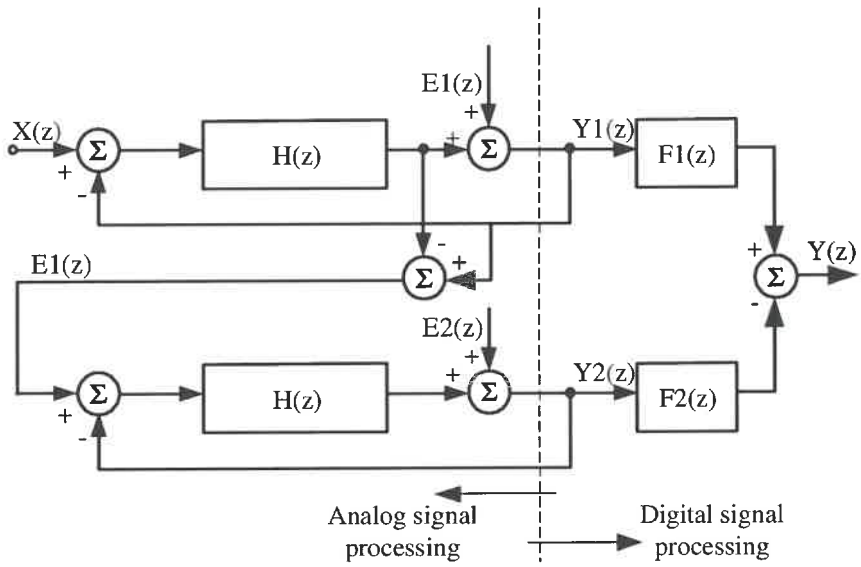


Figure 3.3: Two-stage MASH modulator

By a loop filter with a transfer function of H(z), the first stage lower-order modulator output can be expressed as

$$Y1(z) = S_{TF}(z)X(z) + N_{TF}(z)E1(z), \tag{3.1}$$

where $S_{TF}(z)$ and $N_{TF}(z)$ are defined in Equation (2.14) and (2.15) unaffected. As the quantization noise of the first stage is fed into the second stage, the output of the later is

$$Y2(z) = S_{TF}(z)E1(z) + N_{TF}(z)E2(z). \tag{3.2}$$

And the output of the cascaded modulator is

$$Y(z) = F1(z)Y1(z) - F2(z)Y2(z) \tag{3.3}$$

$$= F1(z)S_{TF}(z)X(z) - F2(z)N_{TF}(z)E2(z) + [F1(z)N_{TF}(z) - F2(z)S_{TF}(z)]E1(z). \tag{3.4}$$

If it is deliberately designed to have

$$F1(z) = S_{TF}(z) \tag{3.5}$$

and

$$F2(z) = N_{TF}(z), \tag{3.6}$$

then (3.4) becomes

$$Y(z) = S_{TF}^2(z)X(z) - N_{TF}^2(z)E2(z) \tag{3.7}$$

Thus, higher-order modulator is made out of two lower-order ones.

In our application, we take the 3 MHz carrier frequency as an example. Two 2nd-order modulators can be cascaded to construct the targeted 4th-order modulator. By [48], a 2nd-order modulator centered at 3 MHz with f_S of 51.2 MHz and bandwidth of 200 kHz, the noise transfer function is

$$NTF(z)=\frac{z^2+1.866z+1}{z^2-1.138z+0.4389} \tag{3.8}$$

The corresponding $H(z)$ and $STF(z)$ are deduced to be

$$H(z)=\frac{0.728z-0.5611}{z^2-1.866z+1}, \tag{3.9}$$

and

$$STF(z)=\frac{0.728z-0.5611}{z^2-1.138z+0.4389}. \tag{3.10}$$

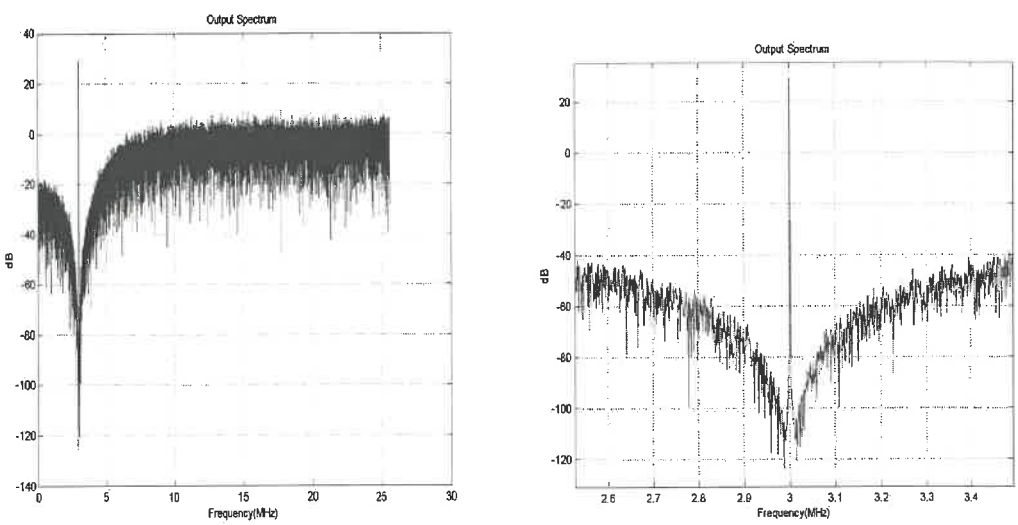
When Equations (3.5) and (3.6) hold, the 4th-order modulator output is

$$Y(z)=\left[\frac{0.728z-0.5611}{z^2-1.138z+0.4389}\right]^2 X(z) - \left[\frac{z^2+1.866z+1}{z^2-1.138z+0.4389}\right]^2 E2(z) \tag{3.11}$$

Figure 3.4 is the output spectrum of the modulator represented by Equation(3.11). The calculated SNR is 86 dB when the magnitude of the input sinusoidal signal is 50 percent of the maximum feedback signal magnitude.

The Gm-C circuit can be extracted from the MASH model (Figure 3.3) with discrete-time loop filter H(z) replaced by the continuous-time one H(s). The equivalent H(s) of H(z) in equation (3.9) can be given by MATLAB (command "d2cm"), and expressed by Equation (3.12):

$$H(s)=\frac{0.6593(\frac{s}{f_S})-0.1688}{(\frac{s}{f_S})^2+0.1355} \tag{3.12}$$



(a) (b)

Figure 3.4: Output spectrum of two-stage MASH modulator:

(a) overview; (b) close view around the signal band

This transfer function is realized by the topology in Figure 3.5, expressed mathematically as

$$H(s)=\frac{Out(s)}{In(s)}=\frac{\frac{Gm3}{C2}s+\frac{Gm1\cdot Gm2}{C1\cdot C2}}{s^2-\frac{Gm2\cdot Gm4}{C1\cdot C2}} \tag{3.13}$$

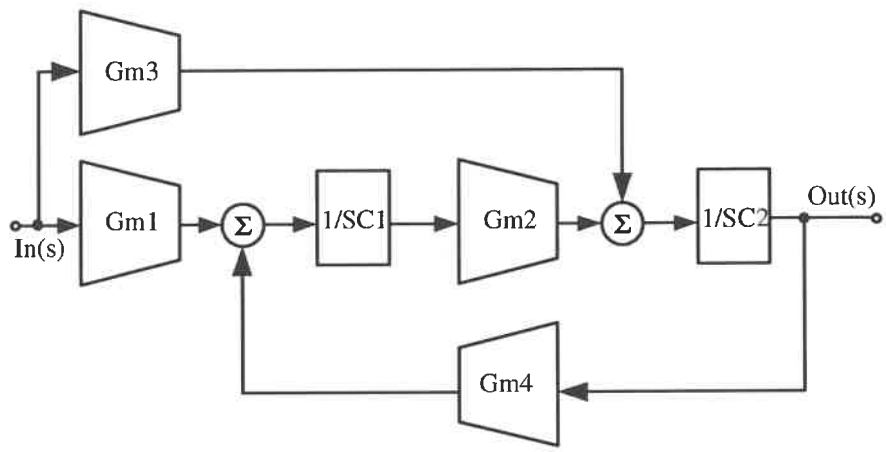


Figure 3.5: Model of Gm-C Filter

With system sampling frequency f_s = 51.2 MHz, it can be calculated that Gm1=6.554e-6, Gm2=Gm3=16.879e-6 and Gm4=-5.262e-6 is one set of Gms that satisfies equation (3.12) when C1=C2=1pF.

However, MASH modulators are sensitive to the mismatches between individual lower order modulators, which result from process parameter tolerances and temperature gradients. Such mismatches result in a leakage of the earlier stage quantization noise to the output of the MASH modulator and hence significantly degrades the dynamic range performance [19][21][30][41][42]. To alleviate such noise leakage, MASH modulator

calls for high accuracy analog building blocks, which conflicts with the motivation for $\Sigma\Delta$ converter.

This drawback of MASH modulator on the dynamic range performance is simulated and demonstrated in MATLAB. For a filter with the transfer function given by Equation (3.13), its center frequency is

$$\omega_0 1 = (Gm2Gm4)^{1/2} \tag{3.14}$$

Without loss of generosity and to simplify the analysis, it is supposed that there is a mismatch of transconductance value between the two Gm4 of the two cascaded modulators, and all the other Gms and Capacitances are kept at there original values. After careful simulations, it is concluded that the system SNR and dynamic range are degraded in proportion to the magnitude of mismatch (Figure 3.6). In this Figure δGm is the difference between values of the two Gm4 in the modulator, and the SNR degradation is intuitive. With 5 and 10 percent of mismatches, the degradation of the SNR is 24dB and 30dB which corresponds to 4-bits and 5-bits respectively. Figure 3.7 illustrates the outputs spectrums when mismatch is 5 and 10 percent.

In contrast to MASH topology, interpolative modulator are robust against circuitry inaccuracy. An interpolative modulator structure proposed by the author is shown in Figure 3.8 and the 4th-order loop filter is enclosed in dashed line.

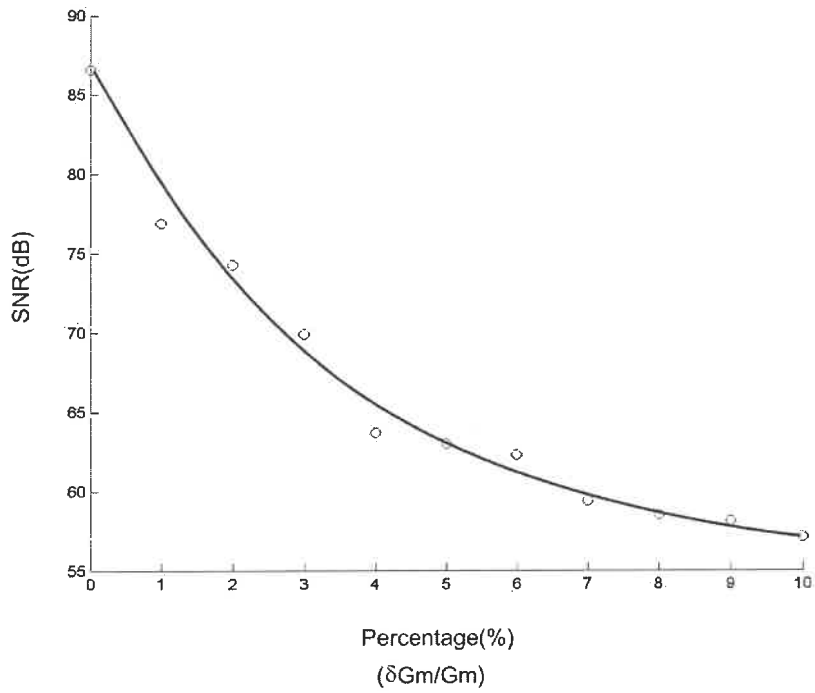
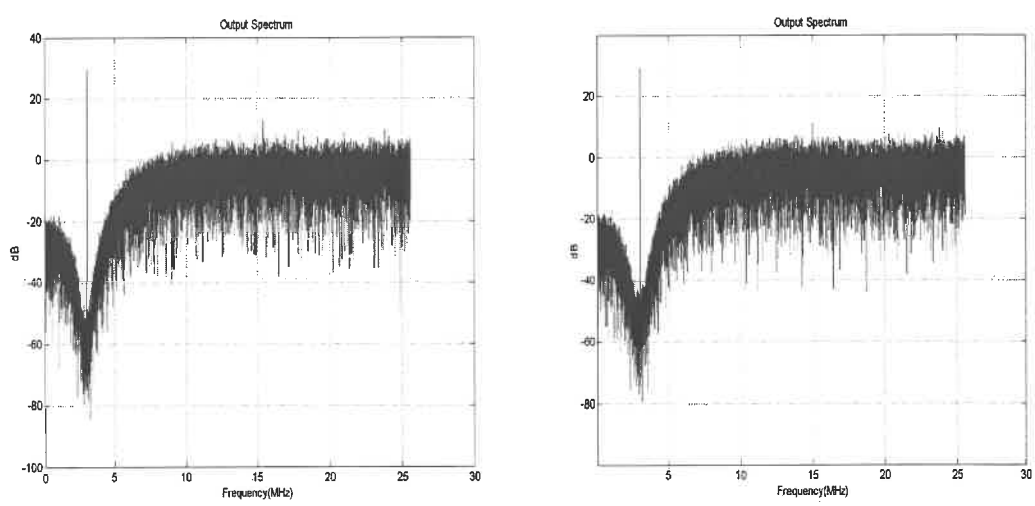


Figure 3.6: Estimated SNR degradation with respect to Gm mismatch percentage



(a) (b)

Figure 3.7: Effects of Gm mismatches: (a) 5%; (b) 10%

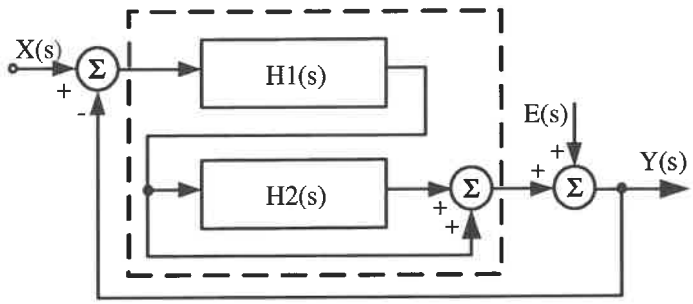


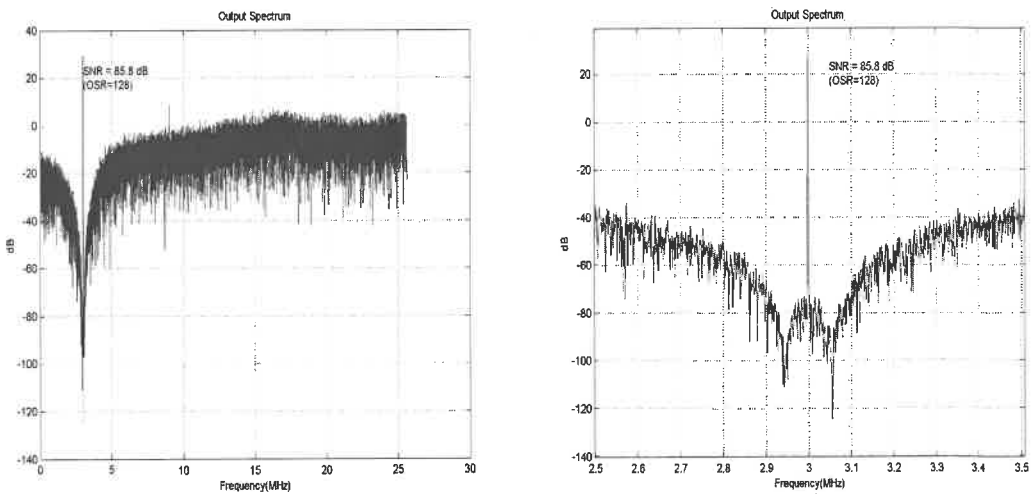
Figure 3.8: Proposed interpolative modulator structure

The 4th-order loop filter is cascaded by two 2nd-order filters of the same structure as in Figure 3.5. Unlike in MASH, where the two 2nd-order filters have the same pole in the center of the signal band, the cascaded two 2nd-order filters have different poles which are distributed within the signal bandwidth. Figure 3.9 gives the output spectrum of the interpolative ΣΔ modulator. From the close view around signal band in Figure 3.9b, the two poles of the 4th-order filter form the two notch of sampling noise, which are located at 2.95 MHz and 3.05 MHz.

The distributed poles not only increase the potential achievable modulator SNR, but also increase the modulator robustness against circuitry inaccuracy [6][16]. Like what is done for MASH modulator, the influence of mismatch between the transconductances of Gm4 in the filters of H1(s) and H2(s) is evaluated in MATLAB.

Simulations of mismatch are conducted in four directions: (a) Both Gm4 are 10 percent greater than designed values; (b) Both Gm4 are 10 percent less than designed values; (c) Gm4 of H1(s) is 10 percent greater and Gm4 of H2(s) is 10 percent less than designed values: (d) Gm4 of H1(s) is 10 percent less and Gm4 of H2(s) is 10 percent greater than designed values. The resulting output spectrums and SNRs are shown in

Figure 3.10. The worst case of the modulator SNR degradation happens when the two filter poles deviate apart (Figure 3.10(d)). In this case, the modulator SNR is traded off for wider bandwidth (400 kHz). It is noted that the resulting modulator SNR of this worst case is 71.8 dB. By comparison in MASH modulator, a mismatch of Gm4 of 10 percent leads to a modulator SNR of 57.1 dB, which is more than 14 dB less than that of the interpolative modulator.



(a) (b)

Figure 3.9: Simulated performances of the interpolative modulator:

(a) overview; (b) close view

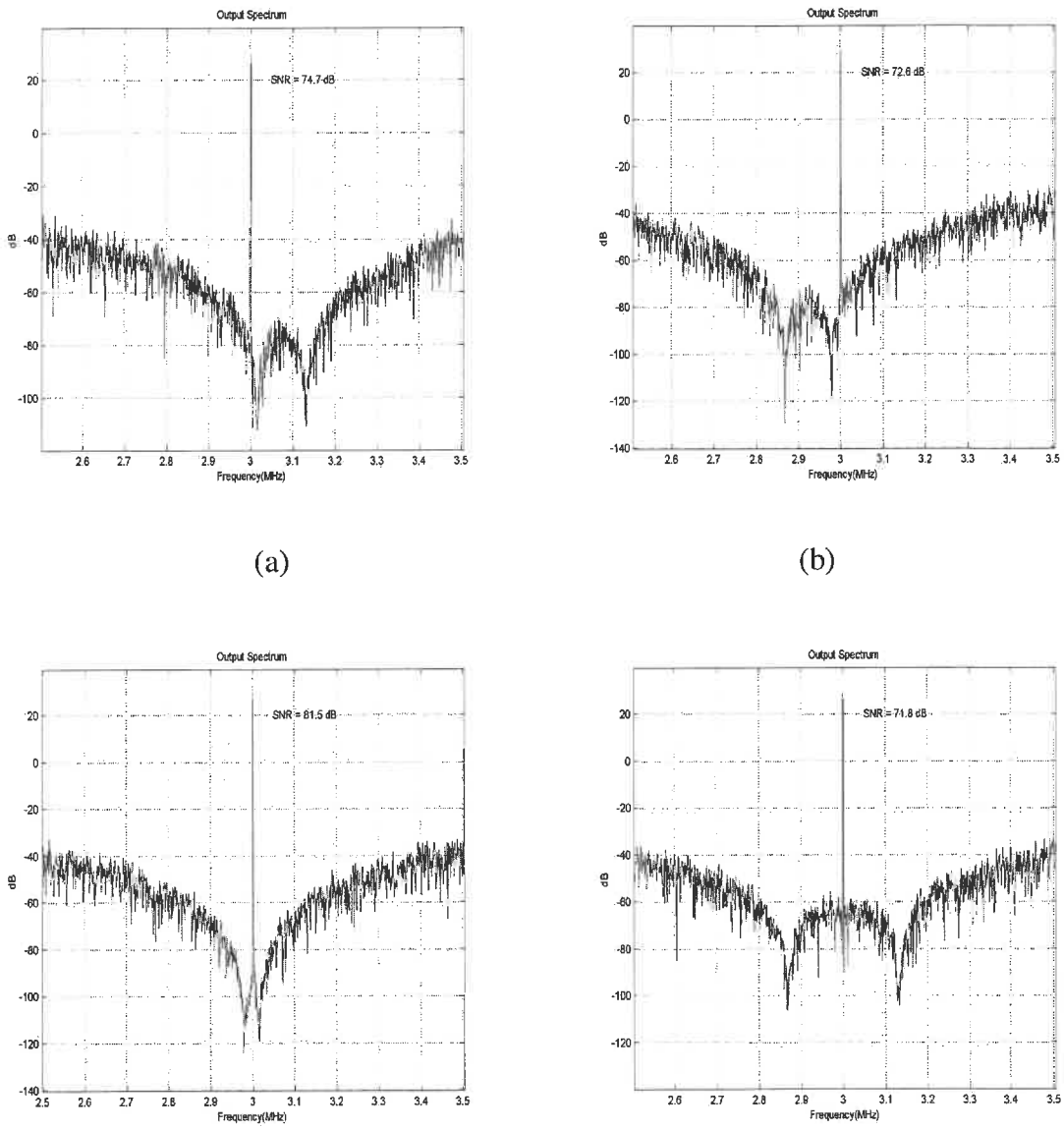


Figure 3.10: Evaluation of mismatch influence on the proposed interpolative modulator structure: (a) poles deviate right; (b) poles deviate left; (c) poles deviate towards signal band center; (d) poles deviate apart

3.5 Conclusion

In this chapter, specifications of the targeted ΣΔ modulator are defined and the modulator architecture is set up. Through theoretical calculation, extensive overview of past works and careful simulations with MATLAB, a 4th-order bandpass single-bit ΣΔ modulator with an oversampling ratio of 128 is defined. Subsequent analysis further excludes the discrete-time domain realization and recommends instead the Gm-C continuous-time domain realization. At last, a quantitive comparison on the modulator SNR is made between MASH and interpolative structures. It is proved that the proposed interpolative structure demonstrates more robustness against parameter tolerances and component mismatches.

CHAPTER 4

REALIZATION AND VALIDATION OF ΣΔ MODULATOR FOR 3 MHz APPLICATION

4.1 Introduction to the Submitted Journal Manuscript

Constituting the main part of this master thesis, this chapter includes the article "A 1.8V CMOS Fourth-Order Gm-C Bandpass Sigma-Delta Modulator Dedicated to Front-end Ultrasonic Receiver", which was submitted for publication.

In this article, theoretical analysis of a novel design approaches to the ΣΔ modulator are discussed. The realization of the modulator for 3 MHz application are detailed both at circuit and system levels. Conclusive results of the verification and test of the fabricated modulator are also given. Besides, primary idea about the modulator programmability are introduced.

4.2 Article "A 1.8V CMOS Fourth-Order Gm-C Bandpass Sigma-Delta Modulator Dedicated to Front-end Ultrasonic Receiver"

4.2.1 ABSTRACT

A 4th order bandpass Σ-Δ modulator for ultrasound applications is presented. By cascading 2 second-order identical Gm-C bandpass filters, a 4th-order modulator was designed with high power-efficiency, stability, tunability and programmability. The modulator is dedicated for application of 3 MHz IF frequency with 200 kHz bandwidth

and implemented in a standard 0.18 μm CMOS technology. Post-layout simulation gives a dynamic range of 78dB. Chip measurements are reported after successfully tuning the modulator to operate at 1/4-scaled of its folded specifications. The final SNR achieves 58 dB at 0.75 MHz with 50 kHz bandwidth. The modulator consumes 2.5 mW from 1.8V power supply. In addition a programming method is introduced and corresponding circuit is designed to change the central frequency of the modulator between 3 and 20 MHz. Even though the 200 kHz bandwidth limits the modulator only for Dobbler technique, the effective facilities of programmability are valuable assets to expand this application to other wide band applications in future.

Keywords: Ultrasonic-Receiver, analog-to-digital converter (ADC), Sigma-Delta, bandpass, programmable, Gm-C

4.2.2 INTRODUCTION

Ultrasound technique has been proved to be one of the most popular and efficient non-invasive methods in medical diagnosis. With the ultrasound waves, which refer to high-frequency sound waves above the human auditive limit (around 20 KHz), the information about the structure and nature of body tissues and organs can be collected and further visualized by imaging technique. Together with other medical imaging facilities such as X-rays, ultrasound techniques are widely adopted to identify tumors and other abnormalities [7] [46].

The traditional ultrasonic systems not only are bulky but also often consume a significant amount of power. The inconveniences greatly limit their application to

bedside within clinics and make them far from the satisfaction of market demand. Like in all the other instrument areas, the design, fabrication and application of the ultrasound techniques have also been significantly influenced by the continuing progress in microelectronics. With the increasing level of integration afforded by CMOS processes, handheld ultrasonic systems are not only theoretically feasible but also practically realizable. While such portable devices begin to emerge on market, higher precision and lower power consumption are required for most applications. A fully integrated portable ultrasonic system was recently introduced by our team [46], and the proposed architecture of the front-end ultrasonic receiver is shown in Figure 4.1(a). It consists of a stage of true logarithmic amplification (TLA) placed in series with a stage of time gain compensation (TGC) and ends with an analog-to-digital converter (ADC) [15].

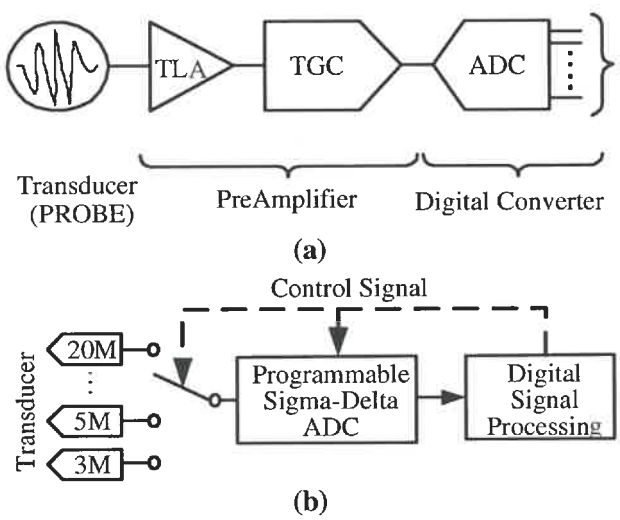


Figure 4.1: Front-end of handheld ultrasonic receiver:(a) Typical; (b) Proposed

The ADC plays a critical role in such signal processing chain. It determines the structure and characteristics of the receiver. Nyquist-rate pipelined ADCs are widely

adopted in ultrasonic applications. However, high-resolution pipelined ADCs are proved to be power-hungry. Many researches have been conducted for power optimization and great success has been achieved to reduce the power consumption from a few watts [13] to less than 100 mW [11][12][15][31][37]. This progress makes it possible to integrate the ADCs with other DSPs on a single chip. But still, the latest result of 20 mW per scan channel [31] is not convenient for a handheld system. Recently, Σ-Δ ADCs have become popular for high-resolution applications and more particularly in ultrasonic systems. On one hand, this kind of converter takes advantage of oversampling to relax the constraints on the analog circuit complexity for high resolution and to eliminate the need of an input sample-and-hold circuit. On the other hand, the use of noise shaping techniques further pushes the quantization noise away from the band of interest. Realizing Σ-Δ modulators is usually done by two approaches, namely in discrete time (DT) domain and in continuous time (CT) domain. Though a straightforward mapping between the DT system mathematics and the circuit-level implementation makes for the prevalence of DT modulators, the settling-time issue largely limits the maximum clock rate and thus the oversampling ratio. By contrast, its continuous time counterpart relaxes this restriction and further provides a free inherent anti-aliasing filter, which is essential for DT implementation [2][15] [38].

To enable power-efficient handheld ultrasound transceivers implementation and its complete system on chip (SoC) solution, digitizing the analog signal as early as possible is highly preferable. Moving the analog-digital interface towards the transducer side trades the analog circuitry for more complex digital one. Such trade-off is getting more

economically advantageous as the relentless scaling down of transistor dimensions are most optimized for digital circuitry. Therefore the transceivers would benefit both the simplicity and power efficiency on the analog side and robustness and flexibility on the digital side.

Enlightened by the foregoing analysis, bandpass Σ-Δ ADC is the best choice for a handheld ultrasonic application. While the published literatures [17, 38] deal with specific RF frequencies, a novel structure of ultrasonic receiver is proposed based on a programmable Σ-Δ ADC as shown in Figure 4.1(b). The target design is a low power, high-resolution programmable handheld ultrasonic receiver. This design is limited only for Dobbler technique (narrow band) and further extension to other wideband techniques will be included in future work. The receiver should be programmed to operate at frequencies of 3, 5, 7, 12 and 20 MHz, while maintaining resolution above 72 dB within a narrow bandwidth of 200 kHz. This is essential to make the receiver adaptable for several kinds of piezoelectric cells used for scanning different regions of the body. The programmability dictates the conventional ADC to be of wide bandwidth to digitize data from multiple channels. Such a 20 MHz wide band could be a stringent challenge for the target modulator. In fact, in the digital output, total useful signal bands only occupy 5*200kHz/20MHz=5% of the entire bandwidth and for each particular application only 1%. This is not simply an issue of waste of signal band but also waste of power and increasing complexity for post-ADC digital processing. To take advantage of the narrow band nature of each application, a narrow bandwidth bandpass Σ-Δ modulator with programmability of its central frequency is preferable. Resolution of delta-sigma

converter is generally determined by its loop filter, the quantizer resolution, and the oversampling ratio (OSR). For a bandpass converter, the OSR is defined by

$$OSR = \frac{f_S}{2 \cdot BW} \tag{4.1}$$

where f_S is the sampling frequency and BW is the signal bandwidth. Because the signals are of the same bandwidth, a single sampling frequency f_S=51.2 MHz is adopted for all applications. Though the resulting SNR could vary from one frequency to another but generally such variation is insignificant. As it is shown in Figure 4.2, the bandpass Σ-Δ modulator can be programmed between the applications from 3 MHz to 20 MHz and eventually covers all applications within 20 MHz band. A uniform OSR of 128 is achieved within each 200 kHz signal band.

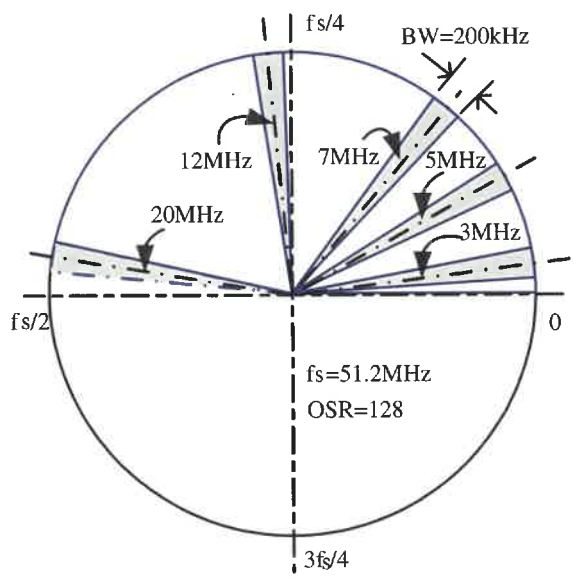


Figure 4.2: Z plane for band-pass Σ-Δ modulators

This paper is organized as follows: Description of the structure of the fourth-order modulator is given in Section II. In Section III, the main circuit building blocks are reported. Simulation and experimental results of the modulator with f_C of 3 MHz are presented in Section IV. Finally, conclusions are summarized.

4.2.3 FOURTH-ORDER ΣΔ MODULATOR

The general structure of the fourth-order Σ-Δ modulator is shown in Figure 4.3. It consists of a fourth-order loop filter, an one-bit quantizer, and an one-bit digital-to-analog converter (DAC). The latter are chosen for the sake of their linearity and simplicity.

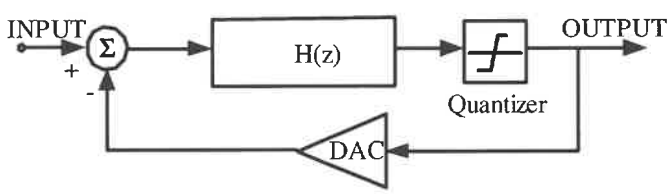


Figure 4.3: Block diagram of a 4th-order Σ-Δ modulator

4.2.3.1 Discrete-Time to Continuous-Time Transformation

The initial discrete-time domain Noise Transfer Function *NTF(z)* of the modulator is achieved using Matlab tool "Delta Sigma Tool Box" [48]. The Signal Transfer Function of the loop filter for a 3 MHz central frequency is then derived by Equation (4.2), in discrete-time domain,

$$H(z)=\frac{1-NTF(z)}{NTF(z)}=\frac{0.7610z^3-1.9295z^2+1.7347z-0.5556}{z^4-3.7320z^3+5.4819z^2-3.732z+1} \tag{4.2}$$

Impulse invariant transformation [9] is then used to get its continuous time equivalent. Impulse invariant transformation is expressed as,

$$h(nT)=[NRZ(t)*h(t)]\Big|_{t=nT} \tag{4.3}$$

where *NRZ(t)* is the non-return-to-zero waveform of the DAC, h(n) and h(t) are the impulse responses of the discrete-time and continuous-time loop respectively, and $T=1/f$. As *NRZ(t)* remains constant within T, the impulse response of Equation (4.3) can be expressed by:

$$h(t)=\left(\int_{-\infty}^{\infty} NRZ(\tau)\cdot h(t-\tau)d\tau\right)\Bigg|_{t=nT}$$

$$=\begin{cases}\int_0^t h(t-\tau)d\tau & 0\le t<T\\ \int_0^T h(t-\tau)d\tau & t\ge T\\ 0 & t<0\end{cases} \tag{4.4}$$

Note that a N-th order continuous-time filter can be presented with the following general form

$$H(s)=\sum_{k=1}^{N}\frac{a_k}{s-s_k}\ . \tag{4.5}$$

Substituting Equation (4.6), which is the impulse response of Equation (4.5), into Equation (4.4),

$$h(t)=\sum_{k=1}^{N}a_k e^{s_k T}\,u(t)\ . \tag{4.6}$$

the z-domain equivalent filter can be derived as

$$H(z)=\sum_{k=1}^{N}\frac{a_k}{-s_k}(1-e^{s_kT})\frac{z^{-1}}{1-e^{s_kT}z^{-1}} \tag{4.7}$$

From Equations (4.5) and (4.7), the discrete-time transfer function of Equation (4.2) is transformed to its continuous-time counterpart

$$H(s)=\frac{0.6638(\frac{s}{f_s})^3+0.2092(\frac{s}{f_s})^2+0.1470(\frac{s}{f_s})-0.0109}{(\frac{s}{f_s})^4+0.2711(\frac{s}{f_s})^2+0.018341}. \tag{4.8}$$

The 4th-order filter with a transfer function of Equation (4.8) offers two poles located on both sides of the central frequency and are kept 100 kHz apart for a 200 kHz bandwidth, as shown in Figure 4.4.

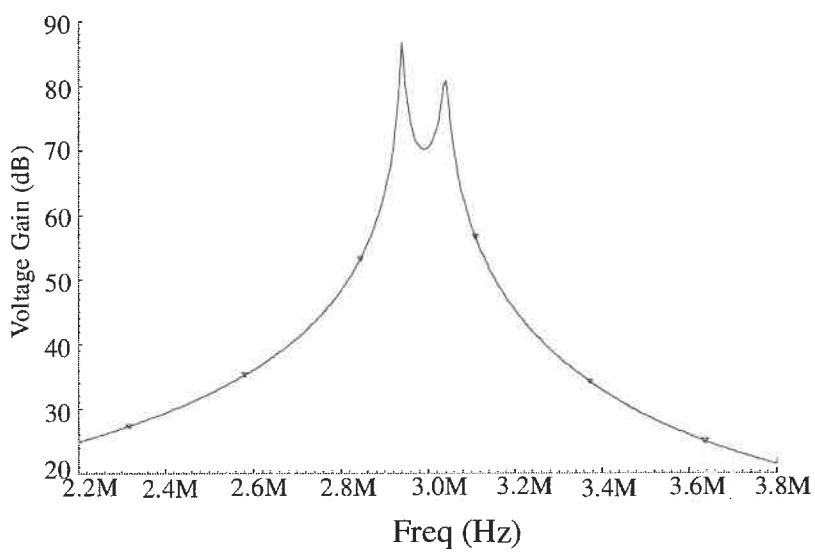


Figure 4.4: Frequency response of the 4th-order bandpass loop filter

4.2.3.2 Loop-Filter Topology

For the operation flexibility of the modulator, it is desirable to tune each pole separately and conveniently. Therefore we propose a 4th-order filter cascaded by two

identical 2nd-order filters $H1$ and $H2$ as shown in Figure 4.5. Each of the two 2nd-order filters contributes one pole. When the outputs of $H1$ and $H2$ are added together, a global transfer function can be obtained. Not only the poles position but also Q factors of the two filters can be programmed separately, and more flexibility is achieved. Furthermore, when the output signal from the filter $H2$ is eliminated from the Adder, the 4th-order modulator in Figure 4.5 can be used as a 2nd-order one, which increases the resolution programmability and enables its use in power saving mode.

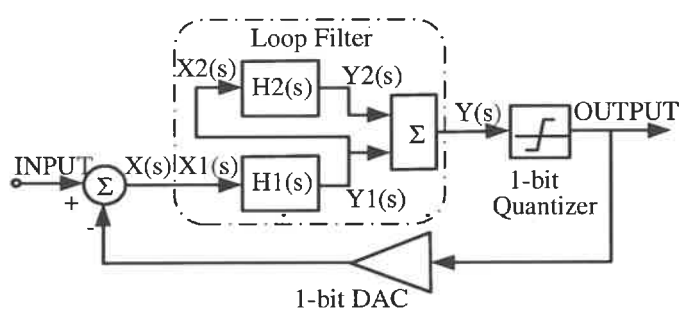


Figure 4.5: Block diagram of a 4th-order Σ-Δ modulator

The structure of the 2nd-order filter is shown in Figure 4.6, with tuning resistors $R1$ and $R2$ added to the topology presented in [26].

To quickly set up the desired transfer function on the circuit level, the transconductor output impedances, and resistors $R1$ and $R2$ are temporarily neglected. Thus, the corresponding transfer function of $H1$ becomes:

$$H1(s)=\frac{Y1(s)}{X1(s)}=\frac{\frac{Gm3}{C2}s+\frac{Gm1\cdot Gm2}{C1\cdot C2}}{s^2-\frac{Gm2\cdot Gm4}{C1\cdot C2}} \tag{4.9}$$

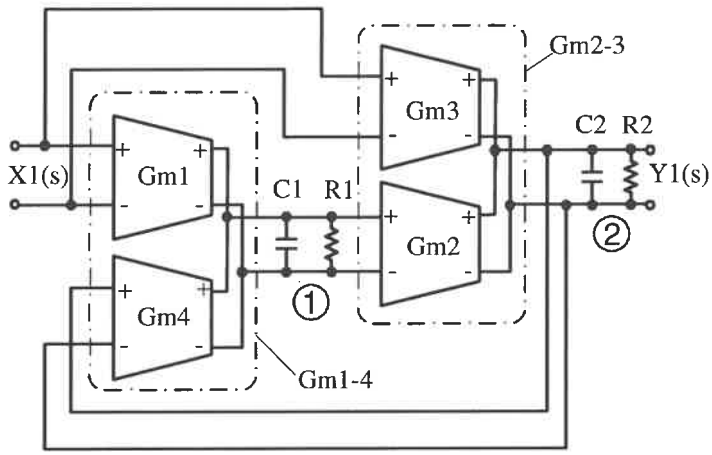


Figure 4.6: Block diagram of the 2nd-order H1 Filter

Similarly for the other 2nd-order filter ($H2$), if Gm1 to Gm4 are renamed as Gm5 to Gm8 accordingly and C1 and C2 as C3 and C4, the transfer function of $H2$ will be:

$$H2(s)=\frac{Y2(s)}{X2(s)}=\frac{\frac{Gm7}{C4}s+\frac{Gm5\cdot Gm6}{C3\cdot C4}}{s^2-\frac{Gm6\cdot Gm8}{C3\cdot C4}} \tag{4.10}$$

With the adder, the outputs of $H1$ and $H2$ are added, and the transfer function of the loop filter can be expressed as

$$H(s)=H1(s)+H1(s)H2(s)=\frac{Y(s)}{X(s)} \tag{4.11}$$

where

$$X(s)=s^4-\left(\frac{Gm2\cdot Gm4}{C1\cdot C2}+\frac{Gm6\cdot Gm8}{C3\cdot C4}\right)s^2+\frac{Gm2\cdot Gm4\cdot Gm6\cdot Gm8}{C1\cdot C2\cdot C3\cdot C4} \tag{4.12}$$

and

$$Y(s)=\frac{Gm3}{C2}s^3+\left(\frac{Gm1\cdot Gm2}{C1\cdot C2}+\frac{Gm3\cdot Gm7}{C2\cdot C4}\right)s^2$$

$$+\left[\frac{Gm1\cdot Gm2\cdot Gm7}{C1\cdot C2\cdot C4}+\frac{Gm3\cdot Gm6\cdot(Gm5-Gm8)}{C2\cdot C3\cdot C4}\right]s$$

$$+\frac{Gm1 \cdot Gm2 \cdot Gm6 \cdot (Gm5 - Gm8)}{C1 \cdot C2 \cdot C3 \cdot C4} \tag{4.13}$$

From Equations (4.11), (4.12), (4.13) and (4.8), a set of Gm values can be determined as shown in the left column of Table 4.1. Nevertheless, this set of values is selected arbitrarily. Even thought the value of Gm3 can be settled down directly by comparing the coefficient of cubed-s term in Equations (4.8) and (4.13), the values of other Gms are not so obvious. In fact, this set is achieved by equating Gm2 to Gm3 and Gm6 to Gm7 simply for the calculation convenience. It is just one of possible sets of values in accordance with the relationship of Equation (4.8) but not necessarily the best.

Table 4.1: Summary of Circuit Parameters

	Value before DS(μA/V)	Value after DS(μA/V)
Gm1	4.147	14.300
Gm2	51.200	9.338
Gm3	51.200	32.201
Gm4	-6.677	-36.608
Gm5	13.515	12.791
Gm6	11.992	17.519
Gm7	11.992	16.580
Gm8	-30.744	-21.045
C1,C2,C3,C4	1 pF	
f_c/f_s	3 MHz/51.2 MHz	

* DS=Dynamic scaling

By simulation, it is observed that the maximum signal amplitudes at each Gm input and output node vary a lot. Some of the nodes are subjected to very small signal. There are also some nodes suffering large signals with amplitude beyond the Gm linear range. As shown in Figure 4.7(a), the magnitude of the upper wave from node ① of Figure 4.6 is less than one-sixth of the magnitude of the lower wave drawn from node ② of the same figure.

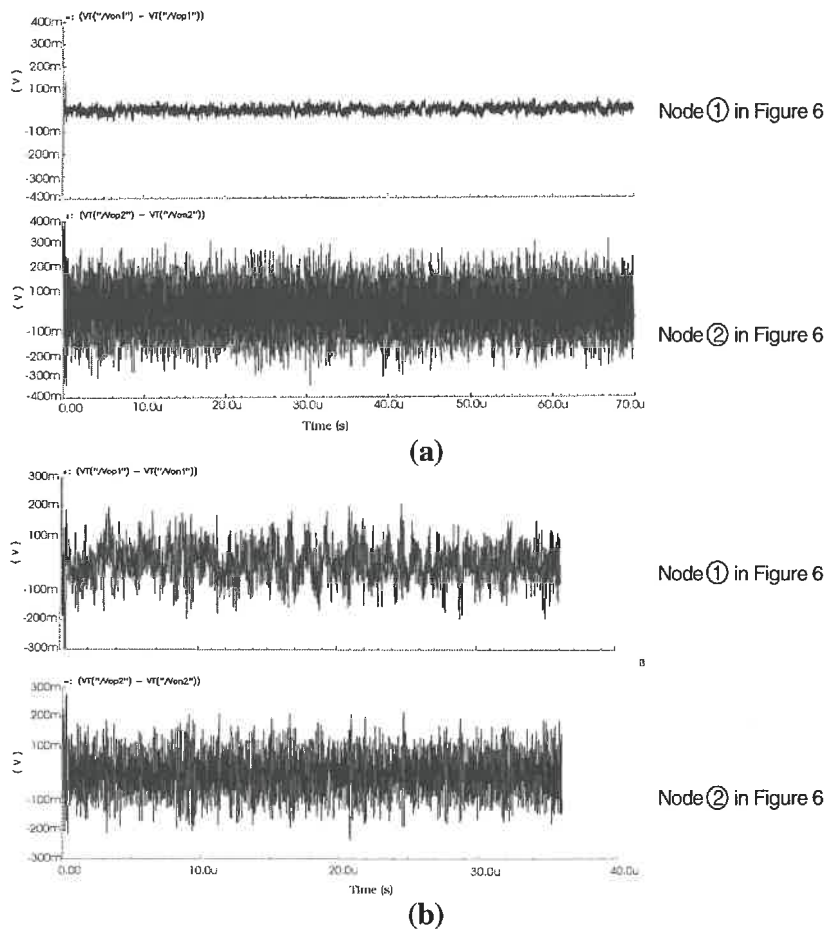


Figure 4.7: Circuit nodes amplitudes comparison:

(a) before and (b) after Dynamic Scaling

Small signal variation not only wastes the linear range but also asks for higher sensitive transconductor. On the other hand, large variation is also not preferable as nonlinear Gm generates more noise. Therefore Dynamic Scaling (DS) is performed. For example, to scale down the input signal by a factor of K_{DS} at the input node of Gm2 in Figure 4.6, the values of Gm1 and Gm4 should be scaled down by this factor. If the value of Gm2 is scaled up by the same factor of K_{DS}, the signal amplitude at the input node of Gm2 is scaled successfully without changing the transfer function of the filter. Dynamic scaling is performed from the input to the output throughout the filter and an optimised set of Gm values is obtained in the right column of Table 4.1. In Figure 4.7(b), it is noticed that the two amplitudes are quite comparable after dynamic scaling. As to the effect of dynamic scaling on the total modulator, it is noticed through simulation in Cadence that the output SNR is increased by 5 dB. In Table 4.1, all capacitors are predetermined to be 1 pF. This significantly simplifies the circuit complexity when the system is programmed between different applications.

4.2.3.3 Tuning of Filter

Taking into account the transconductor output impedances and resistors $R1$ and $R2$, the transfer function of the second order $H1$ filter is now modified as

$$H1(s)=\frac{\frac{Gm3}{C2}s+\left[\frac{Gm1\cdot Gm2}{C1\cdot C2}+\frac{Gm3}{(R_{14}//R1)C1\cdot C2}\right]}{s^2+\left[\frac{1}{(R_{14}//R1)\cdot C1}+\frac{1}{(R_{23}//R2)\cdot C2}\right]s+\left[\frac{1}{(R_{14}//R1)\cdot(R_{23}//R2)\cdot C1\cdot C2}-\frac{Gm2\cdot Gm4}{C1\cdot C2}\right]} \quad (4.14)$$

where R_{14} denotes the equivalent output impedance of Gm1 paralleled with that of Gm4 ($R_{14}=R_{out1}//R_{out4}$), and similarly $R_{23}=R_{out2}//R_{out3}$. As explained in next section, the

transconductor output impedances are much greater than resistors $R1$ and $R2$ and therefore can be neglected. With C1=C2=C, Equation (4.14) is simplified as

$$H1(s)=\frac{\frac{Gm3}{C}s+\frac{1}{C^2}\cdot\left(Gm1\cdot Gm2+\frac{Gm3}{R1}\right)}{s^2+\frac{1}{C}\cdot\left(\frac{1}{R1}+\frac{1}{R2}\right)s+\frac{1}{C^2}\cdot\left(\frac{1}{R1\cdot R2}-Gm2\cdot Gm4\right)} \tag{4.15}$$

The central frequency $\omega_0 1$, quality factor $Q1$ and bandwidth $BW1$ thereof are derived as

$$\omega_0 1=\sqrt{\frac{1}{R1\cdot R2}-Gm2\cdot Gm4} \tag{4.16}$$

$$Q1=\frac{\omega_0 1}{\frac{1}{C}\cdot\left(\frac{1}{R1}+\frac{1}{R2}\right)} \tag{4.17}$$

$$BW1=\frac{1}{C}\cdot\left(\frac{1}{R1}+\frac{1}{R2}\right) \tag{4.18}$$

The dependence of $\omega_0 1$, $Q1$ and $BW1$ on $R1$ and $R2$ shown in Equations (4.16), (4.17) and (4.18) gives us much facility to tune the characteristics of the filter. Furthermore, a much simpler relationship can be adopted if $R1$ is cancelled, in other words, $R1>>0$. Apparently, this simplicity is at the cost of tunability of central frequency. With $R1>>0$, expressions (4.16), (4.17) and (4.18) are rewritten as

$$\omega_0 1=\sqrt{Gm2Gm4} \tag{4.19}$$

$$Q1=C\cdot R2\cdot\omega_0 1 \tag{4.20}$$

$$BW1=\frac{1}{C\cdot R2} \tag{4.21}$$

Similar tuning ability is also hold for the 2nd-order filter $H2$. Figure 4.8 shows the Q-tuning of the filters $H1$ and $H2$, together with the resulted 4th-order loop filter.

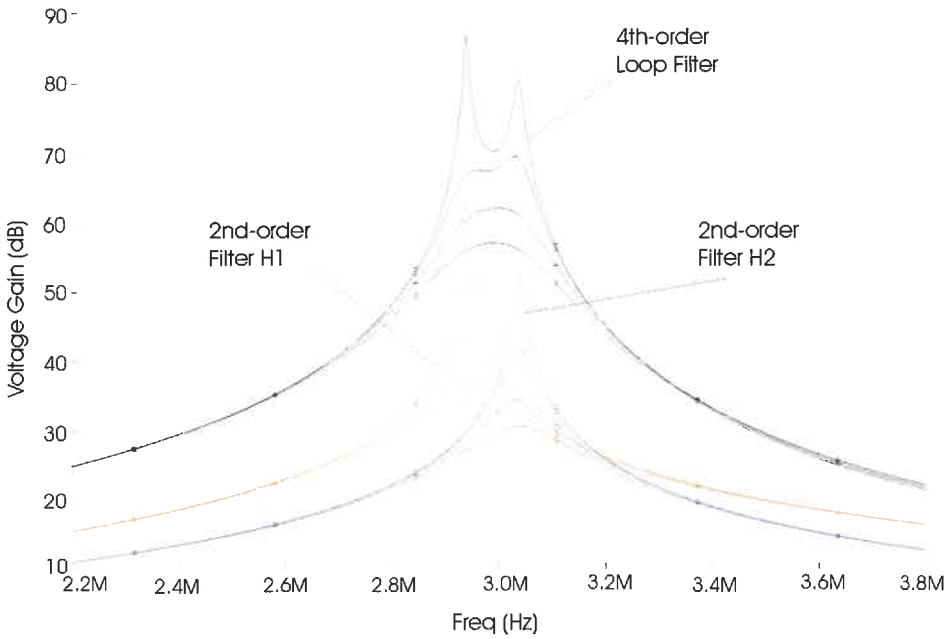


Figure 4.8: Q-tuning of the 2nd-order filters and 4th-order filter

4.2.4 CIRCUIT IMPLEMENTATION

4.2.4.1 Gm-Cell

A Gm-cell is composed of Gm-core and its auxiliary opamps. The implementation of the Gm1-4 is illustrated in Figure 4.9 [20]. Gm1-4 integrates Gm1 and Gm4 together as shown in Figure 4.6 by dashed line. In Figure 4.9, transistors M1 to M4 contribute to Gm1, and the parallel ones in dot-line contribute to Gm4. For simplicity of calculation, we temporarily just consider the Gm1 therein.

Transistors M1 to M4 are biased in the triode region. For a classical transistor model in triode region, the drain current is given by,

$$i_D = \mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{in} + V_{CM} - V_{th}\right)V_{DS} - \frac{V_{DS}^2}{2}\right], \tag{4.22}$$

where V_{in} and V_{CM} denote the AC and DC components in the input signal accordingly. Using opamps to drive the gates of M5 to M8, deep negative feedbacks are formed and the source voltages of M1 to M4 are set to be a constant voltage Vc. Thus the current in equation (4.22) is linearized as,

$$i_D=\mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{in}+V_{CM}-V_{th}\right)V_C-\frac{V_C^2}{2}\right]$$

$$=\mu_n C_{OX}\left(\frac{W}{L}\right)V_{in}V_C+\mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{CM}-V_{th}\right)V_C-\frac{V_C^2}{2}\right] \tag{4.23}$$

Defining

$$i_{CM}=\mu_n C_{OX}\left(\frac{W}{L}\right)\left[\left(V_{CM}-V_{th}\right)V_C-\frac{V_C^2}{2}\right] \tag{4.24}$$

which is the dc component of i_D due to V_{CM}, V_{th} and the squared V_C in Equation (4.24).

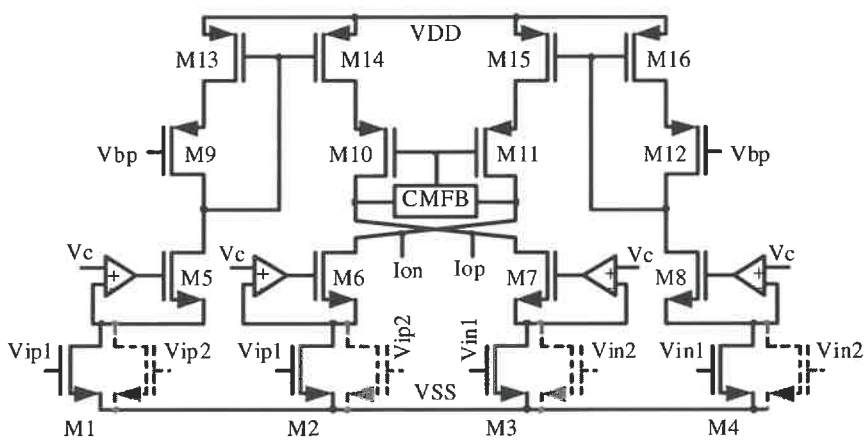


Figure 4.9: Schematic of Gm1-4 circuit

The current mirrors and the cross-coupling connection further cancel the i_{CM} term at the outputs of I_{op} and I_{on}. Ignoring second-order effects, a highly constant Gm-cell value is given by,

$$Gm = \frac{i_D}{V_{in}} = 2\mu_n C_{OX}\left(\frac{W}{L}\right)V_C \tag{4.25}$$

By simulating in Cadence, the linearity range of this Gm is shown in Figure 4.10 between –250 and 250 mV of input voltage at which the value of the Gm deviates by 1 %. Figure 4.10 also gives the simulation results of the Gm tunability controlled by Vc.

To stabilize the output DC voltage level, a common-mode feedback (CMFB) circuit is implemented between the two output nodes. In addition, two-stage opamps are used (Figure 4.11). Miller Capacitance Cc and lead-compensation transistor M50 are included between the input and output node of the second stage amplifier in order to enforce the stability of the opamp. Vbp5 and Vbp6 are used to bias transistors M46, M49 and M45

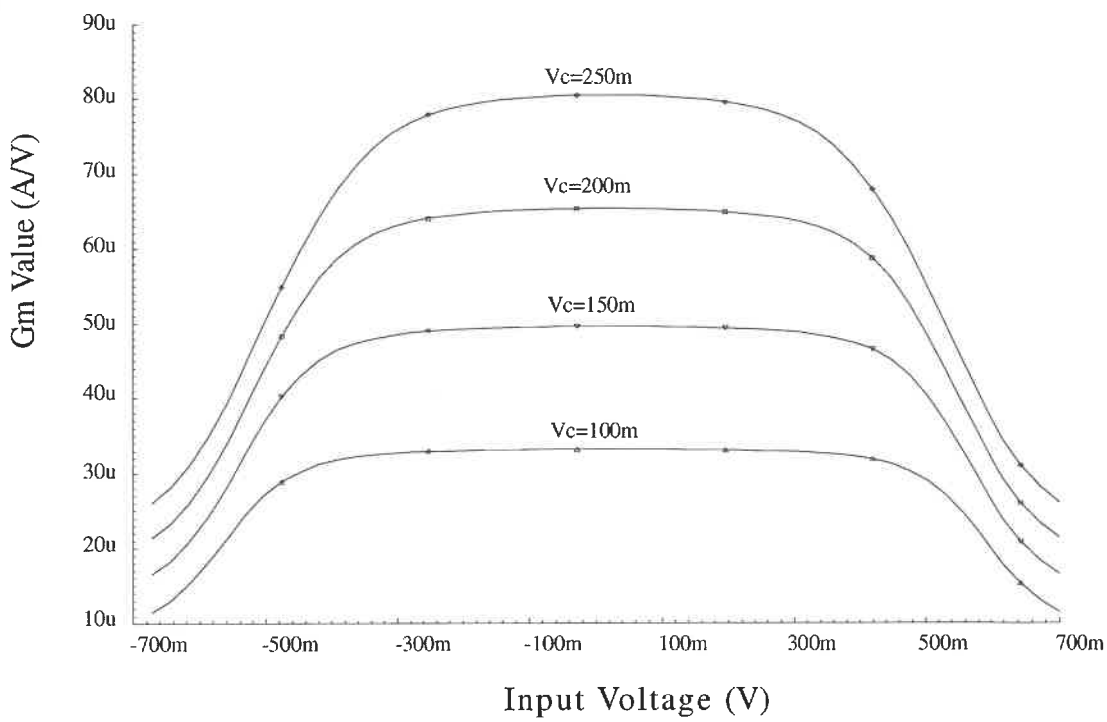


Figure 4.10: Linearity range and tunability of Gm

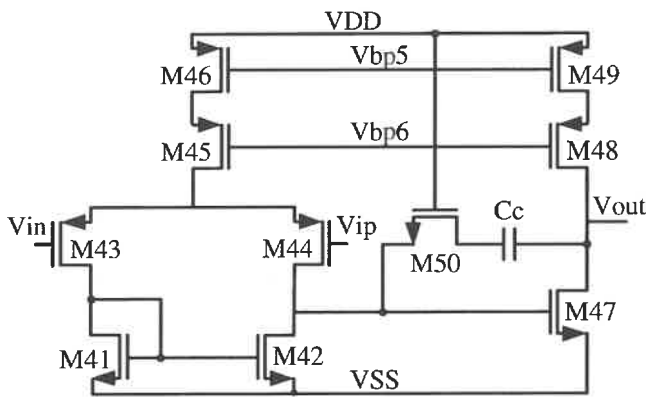


Figure 4.11: 2-stage opamp

and M48 respectively. The power consumption of the opamp is a major concern as each Gm-cell contains four similar opamps. Each opamp is used only to drive the gate capacitance of the load transistor, so the required driving capacity is not large. Noting that the gain of the first stage is

$$A_{v1} = g_{m41}(r_{ds42} \parallel r_{ds44}) \tag{4.26}$$

where

$$g_{m41} = \sqrt{2\mu_p C_{OX}\left(\frac{W}{L}\right)_{41}\frac{I_{bias}}{2}}$$

and

$$r_{ds42} = \frac{2}{\lambda_{42} I_{bias}}$$

which similarly also holds for r_{ds44}. With I_{bias} decreasing, r_{ds42} and r_{ds44} increase inversely while g_{m41} decreases in the power of one-half. As a result decreasing I_{bias} not only saves the power consumed but also increases the gain of the opamp, both are in favor of the

design. Similar result is also obtained from the second stage. In fact, the proposed opamp only consumes 24 μW while its DC gain is above 60 dB.

On the other hand, a high transconductor output impedance is achieved. In fact, the output impedance r_{out14} is amplified by a factor of $gm_{10}r_{out10}$, thus $r_{equ1}= gm_{10}r_{out10}r_{out14}$ (Figure 4.9). Similarly M6 amplifies the output impedance of M2, and the proposed circuit further boosts the amplified value by $(1+A_V)$, where A_V denotes the gain of the opamp. That is,

$$r_{equ\,2} = (1 + A_V)\, g_{m6} r_{out\,6} r_{out\,2} \tag{4.27}$$

The overall output impedance is derived as

$$r_{out} = r_{equ\,1} \parallel r_{equ\,2} = g_{m10} r_{out\,10} r_{out\,14} \parallel (1 + A_V)\, g_{m6} r_{out\,6} r_{out\,2} \tag{4.28}$$

4.2.4.2 Adder

The Adder is also constructed by means of transconductors, as shown in Figure 4.12(a). The output voltages of the two second-order filters are first converted into currents by Gm11 and Gm12. The currents are inherently added together as they are fed into the same node. Another transconductor is employed as a resistive load to convert the resulting current back to voltage for the subsequent quantizer use. The output voltage of the adder is given by Equation (4.29).

$$V3 = \frac{Gm\ 1}{Gm\ 3} V1 + \frac{Gm\ 2}{Gm\ 3} V2 \tag{4.29}$$

It is important to note that it is not necessary to use three independent Gm-cells to build the adder. In fact, a much less complex adder circuit can be implemented on the basis of

transistors instead of on Gm-cells. The needed function of the transconductors Gm11 and Gm12 in Figure 4.12(a) is performed by M21 and M22 in Figure 4.12(b), and summing is inherently accomplished at the drains thereof. At last, M23 acts as Gm13 by connecting its gate to the output node where the summed voltage is achieved.

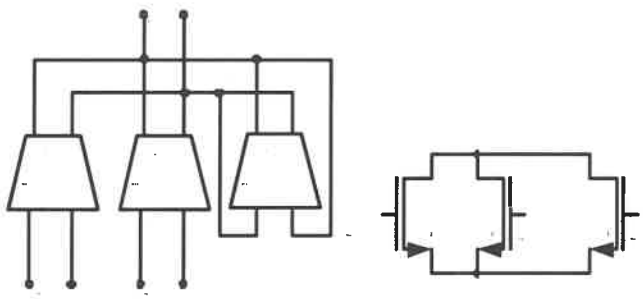


Figure 4.12: Adder implementation: (a) Transconductors based, (b) Transistors based

This transistors-based adder is integrated with active loads in the same way how the Gm-cell is constructed for high linearity. While the general structure is similar to Figure 4.9, one of the four circuit branches is illustrated in Figure 4.13. All the performances of V-to-I, summing and I-to-V are finished with the same complexity as a Gm-cell. This modification not only simplifies the required area but also avoids signal attenuation and speed degrading.

Same analysis applies also to Gm1-4 and Gm2-3 which integrate Gm1 with Gm4 and Gm2 with Gm3 together. Furthermore, the purpose of the DAC in Figure 4.5 is to feed the ADC output back to its input and to perform a voltage addition at the input node even though with negative effect. More profitably, such a one-bit DAC can be integrated into the input Gm cell in the same way as Gm4 into Gm1 forming Gm1-4.

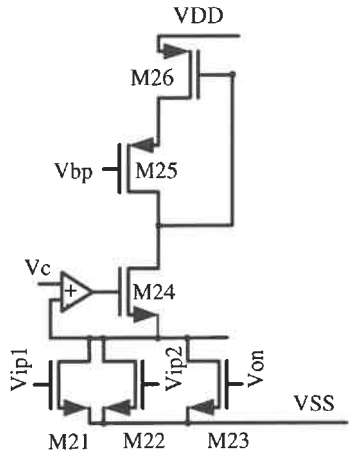


Figure 4.13: Transistor based adder with active load

4.2.4.3 Quantizer

The Quantizer consists of a conventional latched comparator and RS latch as shown in Figure 4.14 [55]. During the precharge phase with φ being low, the outputs of the comparator are charged to VDD. The RS latch holds the result of last comparison. When φ goes to high, the comparator enters into the comparison phase. Pairs of M32-M33 and M38-M39 positively regenerate and greatly amplify the input signal difference to digital signal scale at the comparator output. Resulted signals drive the following RS latch which memorizes this result until the next comparison.

4.2.4.4 Global View of the Programmable Modulator

For the programmable modulator, the central frequency is programmed between 3, 5, 7, 12 and 20 MHz. From Equation (4.19), the central frequency of the 2nd–order filter H1 is given by Gm2 and Gm4, and similarly for H2, its central frequency depends on Gm6

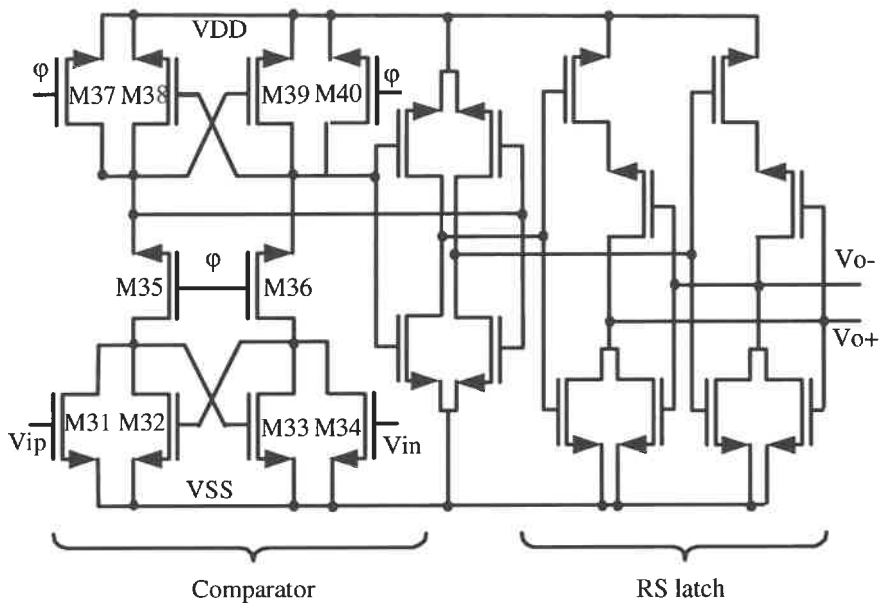


Figure 4.14: Quantizer structure

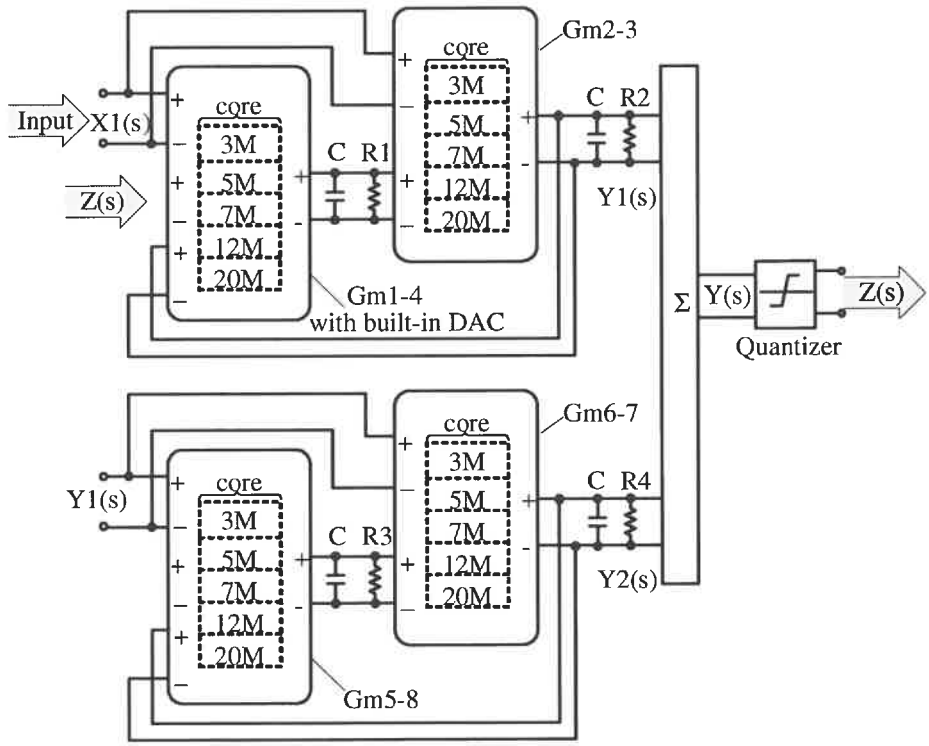
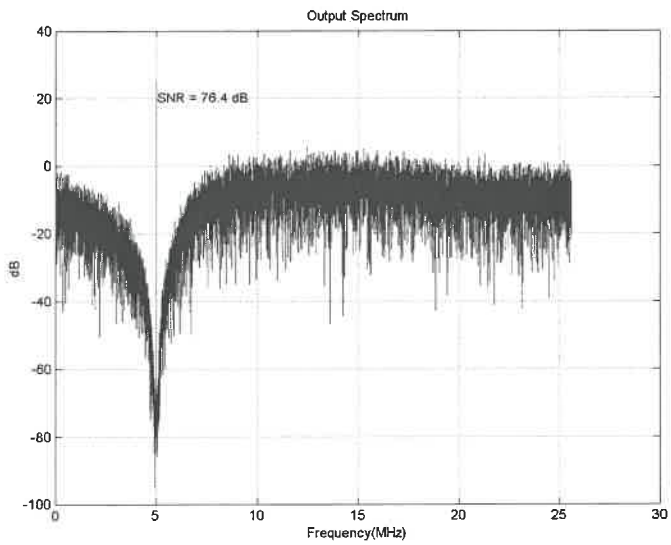


Figure 4.15: Global view of the programmable modulator

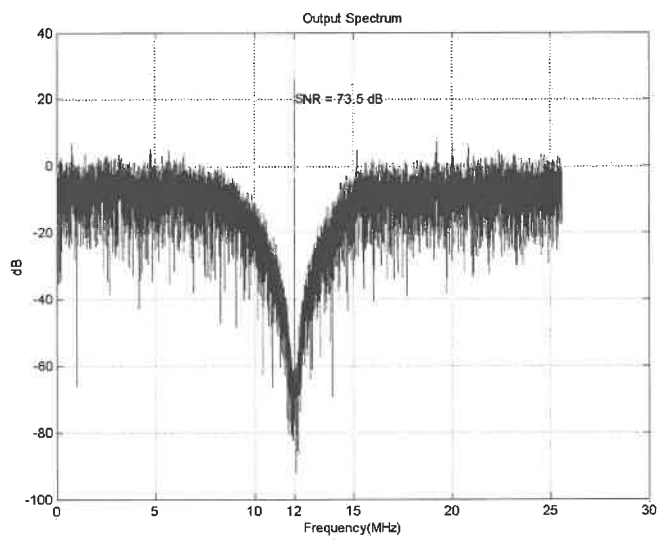
and Gm8. Thus programming the values of Gm2, 4, 6 and 8 is essential. Furthermore, to make a stable modulator at all target frequencies, it is also necessary to program the values of the other Gms. As depicted in Figure 4.15, the cores of all the Gm-cells, as shown in dashed line, contribute to the programmability. All other building blocks, such as quantizer, adder, opamps, capacitors and resistors, form the non-programmable frame of the modulator. According to out application request, only one set of Gm-cores dedicated to that particular frequency is put into operation and, in conjunction with the frame, forms a Σ-Δ modulator for the particular application. Thus, the programmable modulator covers all the applications frequencies from 3 to 20 MHz while consuming the same power as a modulator fixed to one frequency if the power consumed by the auxiliary circuit to switch between different sets of Gm-cores is neglected. Figure 4.16 gives out the simulation results while the system is programmed between applications of 5 and 12 MHz.

4.2.5 SIMULATION AND EXPERIMENTAL RESULTS

The presented 4th-order Σ-Δ modulator for 3 MHz application has been implemented and fabricated in 0.18 μm CMOS technology offered by Taiwan Semiconductor Manufacturing Company (TSMC) (Figure 4.17). The post-layout simulation results are obtained by SpectreS simulator from Cadence. Figure 4.18 shows an output SNR of up to 78 dB at the 3 MHz central frequency. The summary of the simulation results of the modulator is shown in Table 4.2.



(a)



(b)

Figure 4.16: Modulator programmed for applications of (a) 5 MHz; (b) 12 MHz

Because the total capacitive loads summing at the modulator output is around 40 pF, which is contributed by pads, chip package, wires and instrument probes, and is quite larger than what is expected, the fabricated chip cannot work properly at the 3 MHz IF with 51.2 MHz sampling frequency. So, testing of the chip is conducted by tuning the

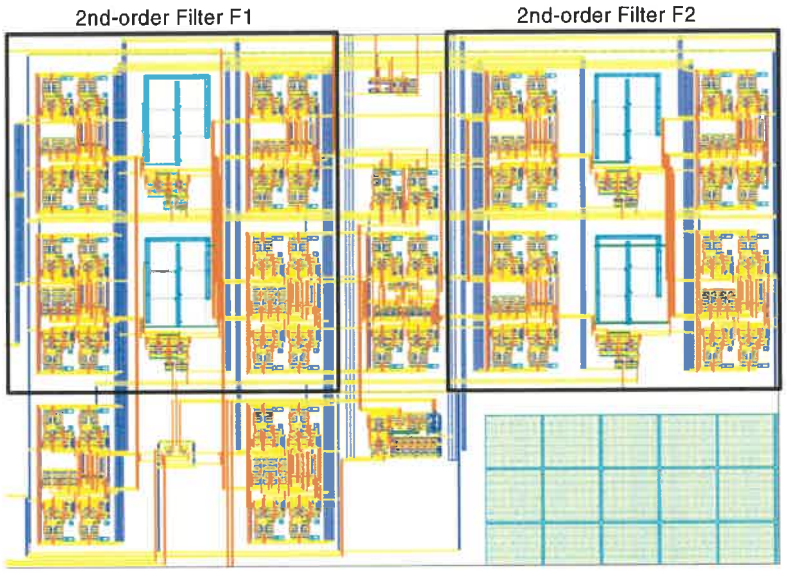


Figure 4.17: Layout of 4th-order Σ-Δ modulator

Table 4.2: Post-layout simulation result of the 4th-order Modulator

Technology	0.18 μm 1.8 V CMOS	
Central Signal Frequency	3	MHz
Signal Bandwidth	200	KHz
Sampling frequency	51.2	MHz
SNR	78	dB
Power consumption	2.5	mW
Layout core area size	400 × 300	μm^2

modulator to its 1/4-scaled specification. With Vc of each Gm-cell being one-fourth of the original designed value, each Gm value is tuned to be 4-times folded. Thus the frequency response feature of the loop filter is 4-times folded from the original designed one (Figure 4.8). With a sampling frequency of 12.8MHz (one-fourth of the original 51.2

MHz), the modulator is working at a central frequency of 750 kHz and with a bandwidth of 50 kHz. The measured output spectrum of this 4-times folded modulator is illustrated in Figure 4.19. Within the folded signal band around 750 kHz, the SNR is 58 dB. Simulation results in Cadence with the same 4-times folded specification and 40 pF capacitive load is also given in Figure 4.20 for comparison. The accordance between the chip measurement and simulation results concludes both the functionality and tunability of the modulator.

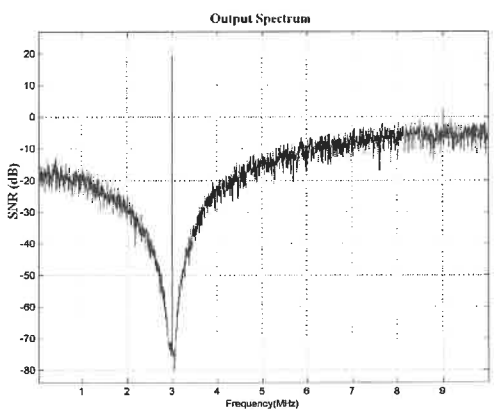


Figure 4.18: Spectrum of the modulator output in Cadence

4.2.6 CONCLUSION

A bandpass Σ-Δ modulator centered at 3 MHz is presented. With the loop filter which consists of two second-order Gm-C filters with identical structures, the fourth-order modulator achieves a 78 dB dynamic range in a 200 kHz signal bandwidth. Tunability of the modulator is demonstrated while the fabricated chip is tested under 4-times folded specifications. Implemented in a standard 0.18 μm CMOS technology, the modulator consumes 2.5 mW from 1.8V power supply.

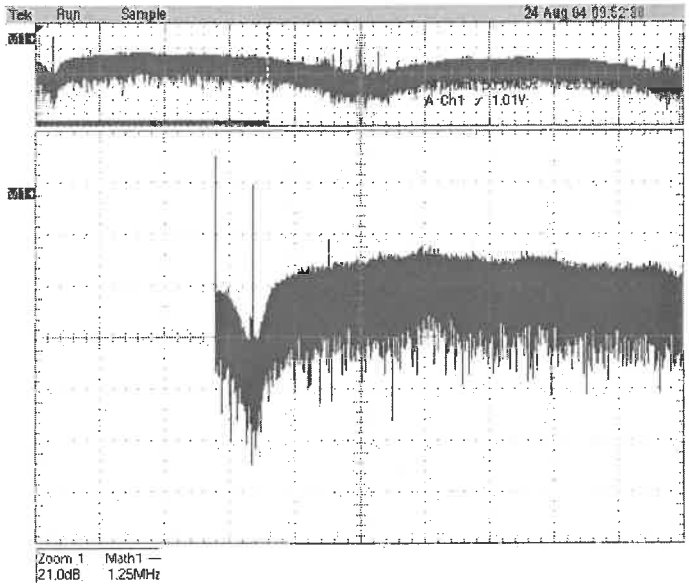


Figure 4.19: Measured output spectrum with 4-times folded specification

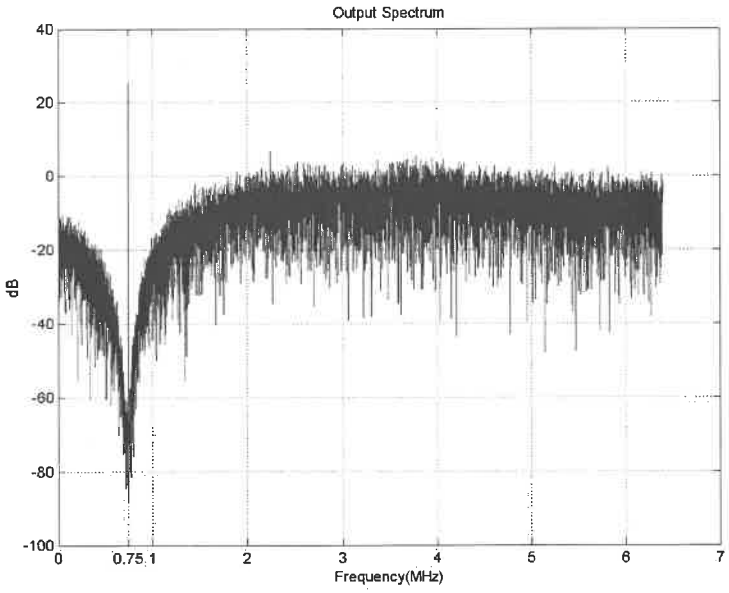


Figure 4.20: Simulation result with 4-times folded specification

4.2.7 ACKNOWLEDGEMENT

The authors would like to express their thanks to the Natural Sciences and Engineering Research Council of Canada (NSERC), Micronet and the Canadian Microelectronics Corporation (CMC) for their financial supports, the chip design tools and fabrication service during this project.

CHAPTER 5

SYSTEM PROGRAMMABILITY

5.1 Introduction

As stated in Chapter 1, the ultimate goal of the project is to realize a programmable ΣΔ modulator to cover the frequencies of 3, 5, 7, 12 and 20 MHz. The design and validation of the 3 MHz application has been detailed in Chapter 4. The programmability of the ΣΔ modulator to other frequencies will be discussed in this chapter.

In Section 5.2, the programmability of the modulator is analyzed. The transfer functions of the required filter and associated circuit parameters for all application frequencies are deduced. The tunability of the Gm value which guarantees the programmability of the filter is discussed in Section 5.3. Limitation of the tunability is pointed out and its alternative amendment is given. Finally, simulation results on the schematic level are illustrated in Section 5.4.

5.2 Programmable Loop Filter

The essence of ΣΔ modulation is to filter the white quantization noise to form a noise notch around the signal band. While it is rather noisy out of the signal band, the Signal – to-Noise Ratio within the signal band is greatly increased. In order to program the modulator to different carrier frequencies, the noise notch should be programmed to be around the targeted frequencies. Figure 5.1 illustrates the presumed frequency responses of the noise transfer functions for all the application frequencies. The response of the

validated noise transfer function for 3 MHz application is shown in solid line, responses of all the other intended noise transfer functions are shown in dashed line.

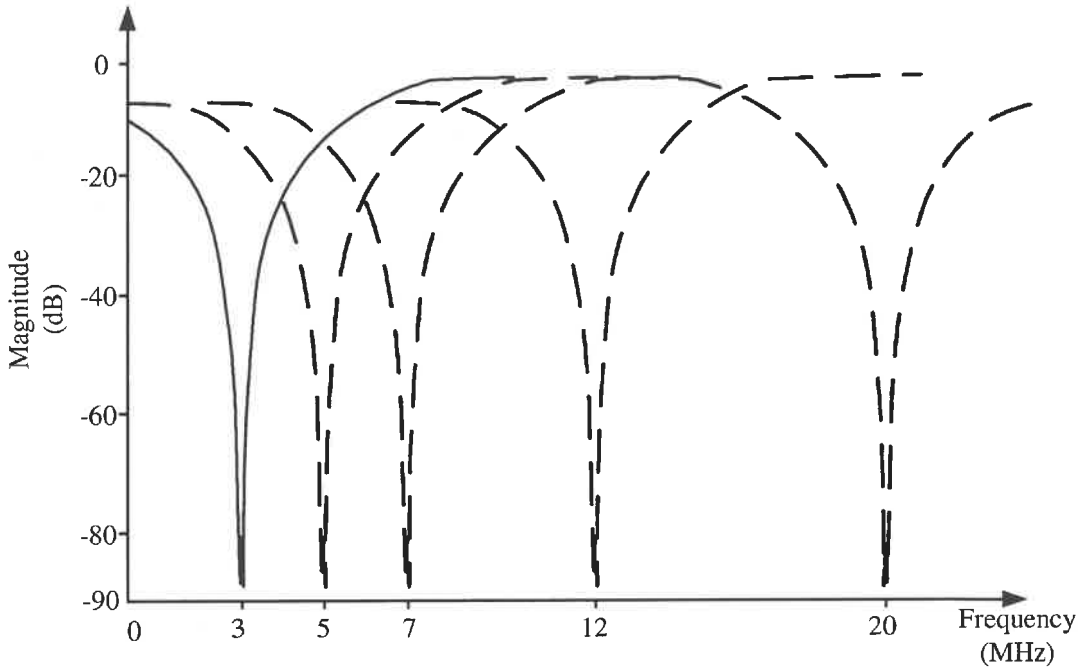


Figure 5.1: Targeted noise transfer functions for the programmable modulator

With the loop filter structure shown in Figures 4.5 and 4.6, the position of the noise transfer notches or zeros on the frequency axis are determined by Gm2 and Gm4 in the 2nd-order filter $H1$, and Gm6 and Gm8 in $H2$, according to Equation (4.19). As a result, to program the notches to other frequencies, transconductors Gm2, Gm4, Gm6 and Gm8 should be programmed to proper values. In the mean time, the transfer function poles, which are determined by transconductors Gm1-Gm3, should also be programmed to maintain the optimum stability and bandstop nature of the noise transfer function.

In the same way that the noise transfer function for 3 MHz application is acquired, all the other transfer functions are derived and listed below, where the index to the *NTF* indicates the application central frequency (f_c):

$$NTF_3(z)=\frac{z^4-3.732z^3+5.4819z^2-3.732z+1}{z^4-2.971z^3+3.5524z^2-1.9973z+0.4444} \tag{5.1}$$

$$NTF_5(z)=\frac{z^4-3.27z^3+4.6732z^2-3.27z+1}{z^4-2.597z^3+3.0153z^2-1.7525z+0.4444} \tag{5.2}$$

$$NTF_7(z)=\frac{z^4-2.613z^3+3.7068z^2-2.613z+1}{z^4-2.0719z^3+2.3703z^2-1.401z+0.4443} \tag{5.3}$$

$$NTF_12(z)=\frac{z^4-0.392z^3+2.0382z^2-0.392z+1}{z^4-0.3101z^3+1.2526z^2-0.2097z+0.4425} \tag{5.4}$$

$$NTF_20(z)=\frac{z^4+3.092z^3+4.39z^2+3.092z+1}{z^4+2.455z^3+2.8275z^2+1.6581z+0.4444} \tag{5.5}$$

According to Equation (4.2), the loop filter transfer functions can be deducted:

$$H_3(z)=\frac{0.761z^3-1.9295z^2+1.7347z-0.5556}{z^4-3.732z^3+5.4819z^2-3.732z+1} \tag{5.6}$$

$$H_5(z)=\frac{0.673z^3-1.6579z^2+1.5175z-0.5556}{z^4-3.27z^3+4.6732z^2-3.27z+1} \tag{5.7}$$

$$H_7(z)=\frac{0.5411z^3-1.3366z^2+1.212z-0.5557}{z^4-2.613z^3+3.7068z^2-2.613z+1} \tag{5.8}$$

$$H_12(z)=\frac{0.0819z^3-0.7856z^2+0.1823z-0.5575}{z^4-0.392z^3+2.0382z^2-0.392z+1} \tag{5.9}$$

$$H_20(z)=\frac{-0.637z^3-1.5625z^2-1.4339z-0.5556}{z^4+3.092z^3+4.39z^2+3.092z+1} \tag{5.10}$$

With the discrete-time to continuous-time transformation, the loop filter transfer functions expressed in continuous-time form are:

$$H_3(s)=\frac{0.6638(\frac{s}{f_S})^3+0.2092(\frac{s}{f_S})^2+0.1470(\frac{s}{f_S})-0.0109}{(\frac{s}{f_S})^4+0.2711(\frac{s}{f_S})^2+0.018341} \tag{5.11}$$

$$H_5(s)=\frac{0.6486(\frac{s}{f_S})^3+0.1272(\frac{s}{f_S})^2+0.2796(\frac{s}{f_S})-0.0245}{(\frac{s}{f_S})^4+0.7534(\frac{s}{f_S})^2+0.1419} \tag{5.12}$$

$$H_7(s)=\frac{0.6243(\frac{s}{f_S})^3-0.0024(\frac{s}{f_S})^2+0.4484(\frac{s}{f_S})-0.1575}{(\frac{s}{f_S})^4+1.4755(\frac{s}{f_S})^2+0.5441} \tag{5.13}$$

$$H_{12}(s)=\frac{0.517(\frac{s}{f_S})^3-0.5378(\frac{s}{f_S})^2+0.8986(\frac{s}{f_S})-1.5592}{(\frac{s}{f_S})^4+4.3374(\frac{s}{f_S})^2+4.7028} \tag{5.14}$$

$$H_{20}(s)=\frac{0.0511(\frac{s}{f_S})^3-2.0504(\frac{s}{f_S})^2-0.3221(\frac{s}{f_S})-12.0893}{(\frac{s}{f_S})^4+12.0483(\frac{s}{f_S})^2+36.2885} \tag{5.15}$$

With a sampling frequency f_S of 51.2 MHz for all applications, and C1-C4 of 1 pF, Equations (5.11) – (5.15) are compared to Equation (4.11) – (4.13) separately, and thus Gm values are obtained for all applications. The results are shown in Table 5.1, which are the primary values before Dynamic Scaling is conducted.

For each transconductor in Figure 4.14, if its value can be programmed to the values listed in corresponding columns in Table 5.1, the modulator can be programmed to be suitable for intended application frequencies. Simulations with MATLAB validate the above design and output spectrums are shown in Figure 5.2.

Table 5.1: Gm values deduced before Dynamic Scaling

	Gm1	Gm2	Gm3	Gm4	Gm5	Gm6	Gm7	Gm8
3 MHz	4.147	51.2	51.2	-6.677	13.514	11.991	11.991	-30.744
5 MHz	4.257	51.2	51.2	-18.849	12.661	14.297	14.297	-70.627
7 MHz	15.879	51.2	51.2	-37.164	10.645	15.682	15.682	-125.317
12 MHz	70.323	51.2	51.2	-109.967	0.976	17.060	17.060	-336.446
20 MHz	2.070	51.2	51.2	-306.647	35.156	15.392	15.392	-1.031

As it is stated early, the sets of Gm values in Table 5.1 are not optimised. The somewhat arbitrarily based values may cause serious overload at the filter internal nodes. To eliminate the adverse effect of overload on system SNR, Dynamic Scaling should be conducted. Independent modulator prototypes for each application are set up in Cadence in accordance with each row of Gm values in Table 5.1. In every case of applications, transient simulations are performed to record the voltage signal ranges at each filter internal node. Based on the recorded data, careful dynamic scaling is performed in the same way as it is stated in Chapter 4. Table 5.2 summarizes the resulting optimised Gm values after dynamic scaling.

In Table 5.2, each column of values represents a set of transconductances between which a specific transconductor should be programmed. For example, Gm1 should be programmed to the following values 14.3, 2.077, 5.611, 18.313 and 30.994 μA/V in order

to enable the modulator being programmed for centre frequencies of 3, 5, 7, 12 and 20 MHz.

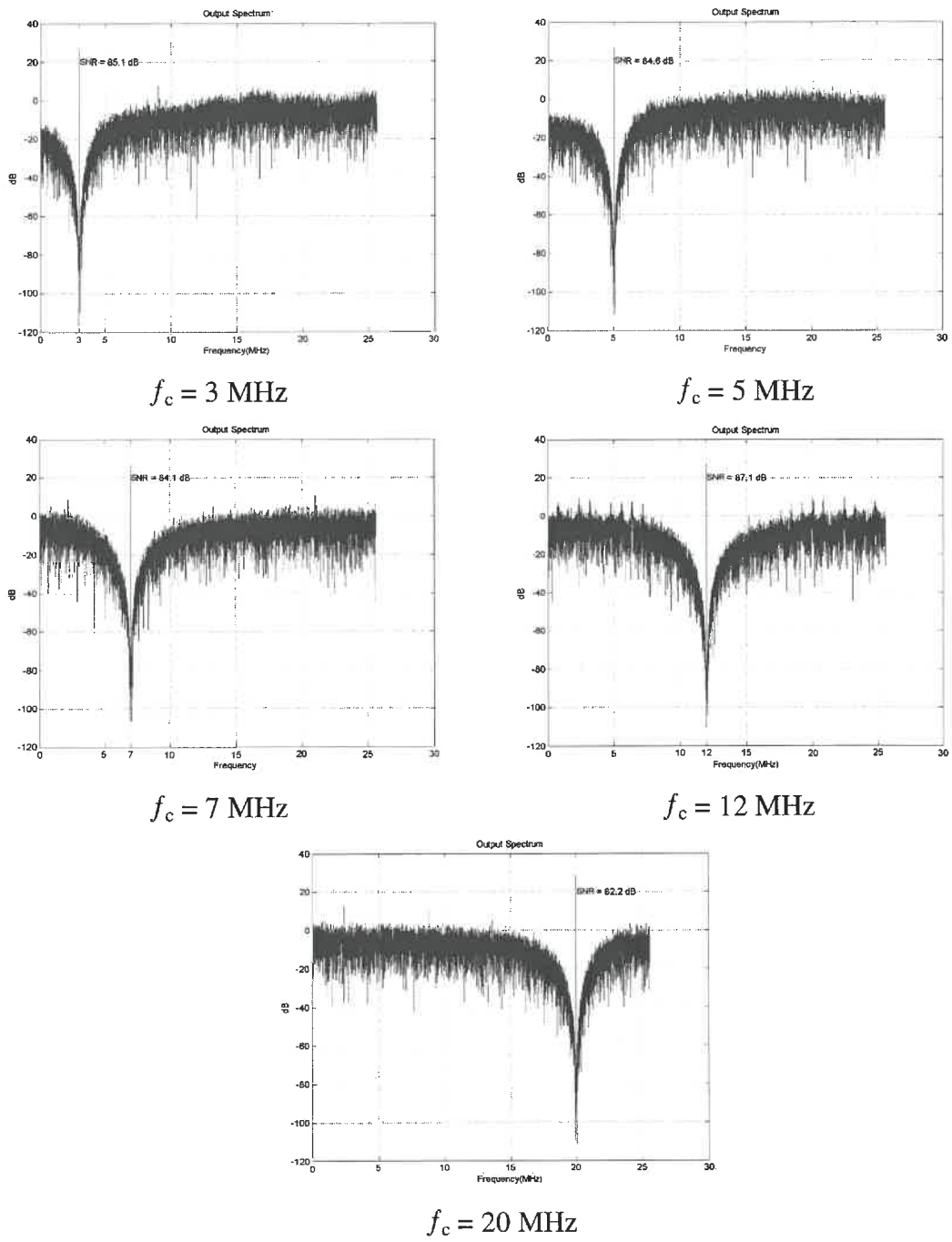


Figure 5.2: MATLAB results of output spectrums of the programmable Modulator

Table 5.2: Gm values deduced after Dynamic Scaling

	Gm1	Gm2	Gm3	Gm4	Gm5	Gm6	Gm7	Gm8
3 MHz	14.3	9.338	32.201	-36.608	12.791	17.519	16.58	-21.045
5 MHz	2.077	51.98	25.347	-18.574	8.171	29.442	19.001	-34.298
7 MHz	5.611	57.958	20.48	-32.83	5.824	47.461	25.964	-41.407
12 MHz	18.313	72.282	18.824	-79.41	2.974	83.571	33.525	-67.372
20 MHz	30.994	99.659	1.462	-160.768	6.856	135.513	25.94	-119.51

5.3 Tunability of Tranconductor

As it is concluded in last section in Table 5.2, the programmability of the targeted modulator is made possible by the tunnability of the transconductance cell.

According to Equation (4.25), restated here for convenience,

$$Gm = 2\mu_n C_{OX}\left(\frac{W}{L}\right)V_C \tag{5.16}$$

This transconductance can be finely tuned by Vc and coarsely tuned by W/L.

In Figure 4.10 the effect of Vc on the transconductance is illustrated. With Vc increasing gradually, the Gm value increases accordingly. If step of Vc variation is small enough, the Gm value can be tuned in a continuous manner. This feature of tuning is validated by simulation in Cadence and the result is shown in Figure 5.3. It is clear that when Vc is small, there exits a clear linear relation between Gm value and Vc defined by

Equation (5.16). The nonlinearity relationship between Gm value and Vc is caused by two factors. The first one comes from the power 2 of Vc existing in Equation 4.23. When Vc is small, the second order effect of Vc is negligible. When Vc is greater, the faster increase of second order effect of Vc tends to decrease the Gm value. At the same time, when Vc is greater than 400 mV, the transistors M1-1 to M1-4 and/or M4-1 to M4-4 in Figure 4.9 begin to leave their triode region and enter their active region. Further increase of Vc drives the transistors in the current mirrors out of their active region and the Gm cell can not function properly any more. The maximum Vc for a properly functioning Gm cell apparently decides the maximum tunable Gm value for a fixed W/L ratio. If a greater transconductance is wanted, W/L ratio of the transistors M1-1 to M1-4 and/or M4-1 to M4-4 in Figure 4.9 has to be changed properly and at the same time the dimensions of the current mirror transistors are modified according to the circuit bias current. Figure 5.4 illustrates the Gm tuning concept integrating both coarse tuning by W/L and fine tuning by Vc. On one hand, different ratios of W/L can give a set of discrete transconductance values as shown by real line. For example, the ratio of W1/L1 with a fixed Vc leads to a transconductance of gm1 and W2/L2 with the same Vc leads to gm2. On the other hand, based on each discrete transconductance value defined by W/L, Vc finely controls the transconductance to fill the value gaps between the discrete values. For example, continuous lowering of Vc gradually can decrease the transconductance from gm2 and at last arrives at gm1. This fine tuning course is shown in dashed line.

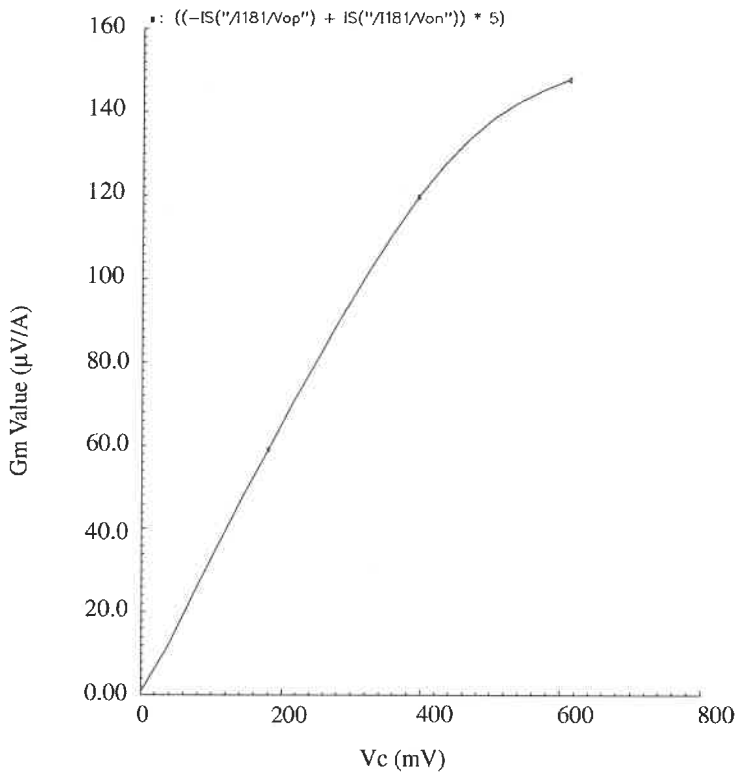


Figure 5.3: Fine tuning of tranconductance by Vc

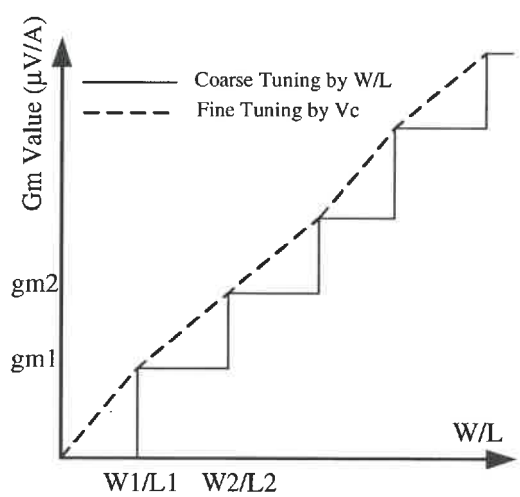


Figure 5.4: Wide range transconductance tuning by coarse plus fine tunings

5.4 Validation of Modulator Programmability

As the transconductance tunability can be achieved by two means, namely coarse tuning by W/L and fine tuning by Vc, the validation of the ΣΔ modulator programmability is done separately with these two means.

5.4.1 Validation of Modulator Programmability through Coarse Tuning

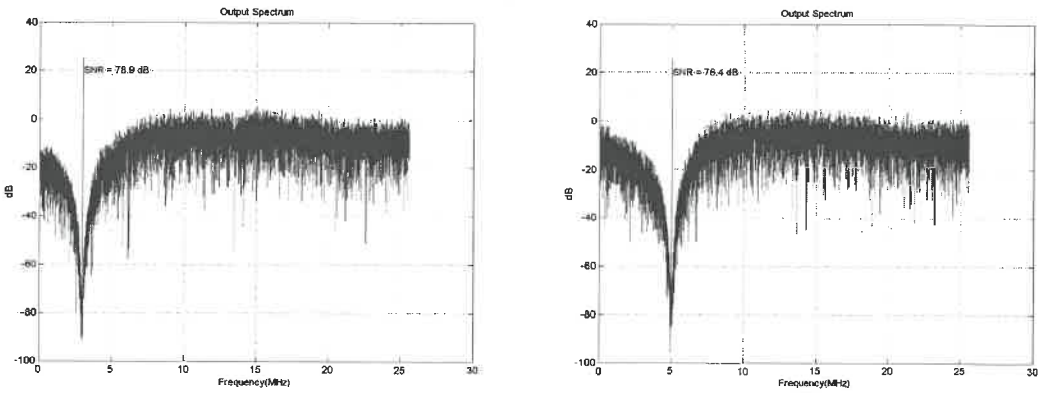
The concept of programming the central frequency of the ΣΔ modulator is illustrated in Figure 4.2 and stated in Section 4.2.3.3. For validating this concept, a set of Gm-cores of Gm1 to Gm8 for 5 MHz application was build up in Cadence. The Gm values are equal to those of the row of 5 MHz shown in Table 5.2.

When the modulator works in 3 MHz application, all the Gm-cells from 1 to 8 select 3 MHz Gm-core accordingly, and the output spectrum is illustrated in Figure 5.5 (a). When it is desired to program the modulator to 5 MHz one, all the Gm-cells switch their Gm-cores from 3 MHz application to 5 MHz application, and the output spectrum is illustrated in Figure 5.5(b). For each application, the sampling frequency remains 51.2 MHz and Vc remains 200 mV for all Gm-cell.

5.4.2 Validation of Modulator Programmability Through Fine Tuning

Fine tuning of transconductance by Vc can be applied to Gm-cells from 1 to 8 according to the values listed in Table 5.2. However, as each column of Gm values in Table 5.2 demands a tunable Vc source, eventually eight independent tunable voltage

sources become indispensable. Such a large number of tunable voltage sources largely increases the complexity of the validation circuitry.



$f_C = 3$ MHz $f_C = 5$ MHz

Figure 5.5: Modulator programmed through coarse tuning by W/L

In this project, a novel validation concept is devised to offer a concise and practical validation method. We take the validated 3 MHz application for example. Noise Transfer Function of Equation (5.1) defines two notches to be around 3 MHz. In z-plane as illustrated in Figure 5.6, the two notches (zeros) are located on both sides of the line which represents the frequency of a steady relationship 3/51.2 with the sampling frequency f_S. As it is validated, when the system sampling frequency is 51.2 MHz, the NRF zeros are located around 3 MHz. If the f_S is scaled down, the central frequency of the system will be scaled down proportionally. For example, when f_S is halved to 25.6 MHz, the central frequency of the modulator is moved from 3 MHz to 1.5 MHz. This result goes directly to the discrete-time modulator without changing anything to the loop

filter as the filter is realized in z-domain. For a continuous-time modulator of our case, following necessary work should be done before this frequency scaling can be applied.

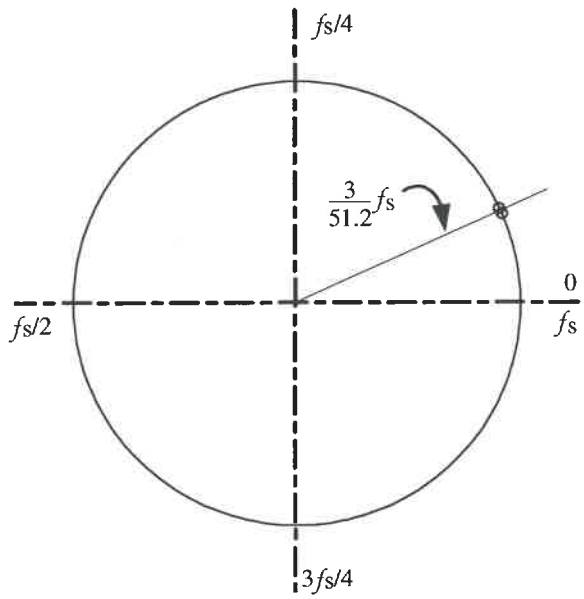
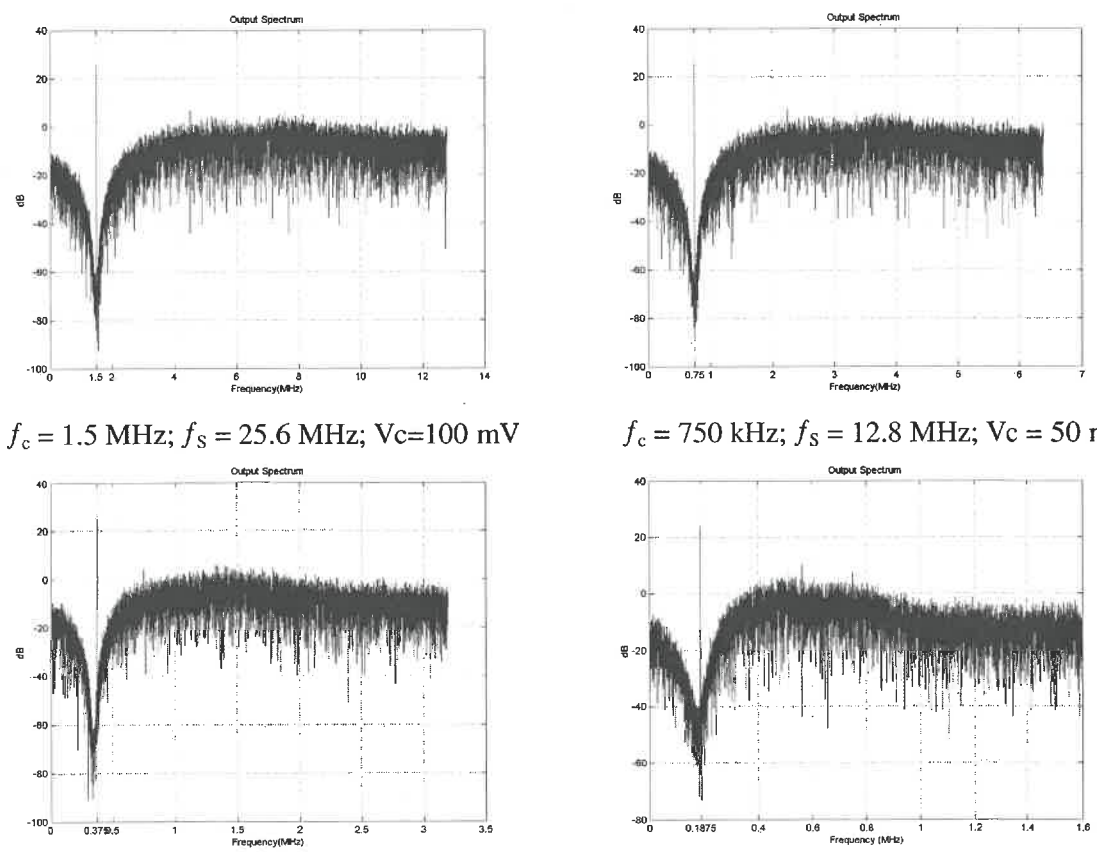


Figure 5.6: z-plane equivalent of Equation (5.1)

The loop filter transfer function in z-domain, Equation (5.6), is derived from Equation (5.1). After discrete-time to continuous-time transformation, the loop filter transfer function in s-domain is stated as Equation (5.11), from which it is clear that the transfer function highly depends on the sampling frequency. Not like in discrete-time case, simply scaling the frequency without changing the circuit parameters can only spoil the continuous-time transfer function. According to Equations (4.11) – (4.13), when the sampling frequency is scaled down, the only way to keep the coefficients in Equation 5.11 as constants is to scale down the values of Gm1 to Gm8 proportionally. For example, when f_S is halved to 25.6 MHz, all the Gm values should be halved, and then the central frequency of the modulator can be moved from 3 MHz to 1.5 MHz, resulting the same

effect as for discrete-time modulator. As all the Gm values are tuned in the same scale, only one tunable voltage source is needed to control Vc for all Gm-cell. As it is shown in Table 5.3, f_S begins from 51.2 MHz and Vc begins from 200 mV with Gm1 to Gm8 having the original values for f_c (central frequency) of 3 MHz. With f_S and Vc being gradually scaled down, Gm values and f_c are scaled proportionally. Simulations were performed in Cadence with different f_S and Vc and the output spectrums are reported in Figure 5.7.



f_c = 1.5 MHz; f_S = 25.6 MHz; Vc=100 mV

f_c = 750 kHz; f_S = 12.8 MHz; Vc = 50 mV

f_c = 375 kHz; f_S = 6.4 MHz; Vc = 25 mV

f_c = 187.5 kHz; f_S = 6.4 MHz; Vc = 12.5 mV

Figure 5.7: Modulator programmed to be scaled down through fine tuning by Vc

Table 5.3: Sets of Gm values for scaled-down modulator specifications

f_c (MHz)	f_S (MHz)	Gm1	Gm2	Gm3	Gm4	Gm5	Gm6	Gm7	Gm8	Vc (mV)
3	51.2	14.3	9.34	32.20	-36.61	12.79	17.52	16.58	-21.05	200
1.5	25.6	7.15	4.67	16.10	-18.31	6.40	8.76	8.29	-10.53	100
0.75	12.8	3.58	2.34	8.05	-9.16	3.20	4.38	4.15	-5.27	50
0.375	6.4	1.79	1.17	4.03	-4.58	1.60	2.19	2.08	-2.64	25
0.1875	3.2	0.89	0.58	2.02	-2.29	0.80	1.1	1.04	-1.32	12.5

5.5 Conclusion

We analysed the facilities for transconductance tuning. By integrating coarse and fine tunings together, the usable tuning range is greatly maximized. The flexibility of transconductance tuning guarantees the tunability of the ΣΔ modulator. On the schematic level, simulations are conducted to validate the performance and effectiveness of the proposed tuning technique.

CHAPTER 6

CONCLUSION

According to the system level requirements for a hand-held ultrasound transceiver front-end, this master thesis makes extensive and in-depth analysis and research between the multi-dimensional trade-offs that exist from the system level down to the circuit level during the design process of ADC modulator. ΣΔ modulation takes advantage of the narrow band nature of the application. Continuous-time realization relaxes the sampling speed limit on its discrete-time counterpart. Gm-C filter technique guarantees the integrity of SoC. Proposed novel loop-filter topology together with the transconductance structure offer an optimum programmability. This programmability combined with the bandpass nature of the modulator satisfies the wide-band requirement of the transceiver front-end and the modulator consumes only the same amount of power as narrow-band ones.

We propose in this master thesis a Gm-C band-pass ΣΔ modulator. Playing a critical role at the interface between analog and digital signal processing, this ADC modulator manifests itself with high-resolution, high power-efficiency, robustness against circuitry imperfection and flexible programmability. Theoretical analysis, implementation and realization of a modulator for 3 MHz application were described in detail. Schematic and chip level validation are conducted. In addition, simulations on schematic level were performed to validate modulator programmability and tunability. Accordance between

the simulation and chip measurement results demonstrates the functionality and tunability of the design.

To further improve the performance of the ΣΔ modulator, possible future work can be reviewed as follows:

First, to improve the fine tuning ability to even wider range, the input-range of the auxiliary opamps in the Gm-cell should be increased. In the mean time, current mirrors in the Gm-cell should be improved for wider signal swings in order to guarantee its functionality within the whole desired tuning range.

Second, this thesis is only dedicated to the narrow-band mode application of the ultrasound transceiver. The wideband application imposes much more difficulties on the modulator design. In the wide-band mode, not only the central frequency varies, but also the bandwidth changes a lot. For example, a common configuration of wideband application asks for 1.5 MHz signal band at 3 MHz IF, 2.5 MHz band at 5 MHz, 3.5 MHz band at 7 MHz, 6 MHz band at 12 MHz and 10 MHz band at 20 MHz. To accommodate the worst case which requires 10 MHz bandwidth, the oversampling ratio can not be high in order to limit the sampling frequency to an acceptable value. In this case, higher-order noise-shaping such as 8th or 10th order becomes necessary. However, such a higher order is apparently a waste of resources for the narrow bandwidth like 1.5 MHz. So another flexibility to program the modulator between large ranges of noise shaping order will be preferable. As a result, a novel loop filter structure can be designed to offer not only the central frequency and bandwidth programmability, but also to facilitate to programming the order of such filter.

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