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UNIVERSITÉ DE MONTRÉAL

LINC TRANSMITTER FOR LINEAR AMPLIFICATION SYSTEMS

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To my husband Shi, Jiang chuan

And my son Shi, Bo wen

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ABSTRACT

This project is dedicated to develop and implement a practical linear amplification with nonlinear components (LINC) transmitter for modern wireless communication systems. Several aspects of design for the digital signal component separator (DSCS) and high performance high efficiency power combiner are presented in this thesis.

A crucial function of LINC is the signal component separator (SCS). A modern version, using a standard DSP device, was first evaluated. It has two major disadvantages: low bandwidth and high power consumption. Next, a new digital signal separation (NDSCS) architecture, based on an FPGA (Field-Programmable Gate Array), is presented and used to enhance the flexibility and the speed of the signal processing. An FPGA provides a means of arranging the arithmetic blocks and registers to fit the algorithms, and to choose an arbitrarily word length so as to significantly reduce power consumption and increase bandwidth. Two effective solutions were implemented: a one-dimensional look-up table and a square-root function block. Both were designed using an Altera Quartus II FPGA kit, which uses a pipelining technique that improves speed. The equivalent designs were also simulated in MATLAB's Simulink. These simulations provide design verification. The experimental results demonstrate that this new architecture is effective and efficiently combines flexibility and performance. Also shown is that the LUT method used is more precise but has less speed than the square-root function block.

Next, a new combiner is proposed. Two of the basic power combiners' (isolated

and non-isolated) voltage / current models are analyzed and a variable reactive termination combiner (VRTC) is proposed, developed and implemented. The proposed model's load impedance, presented to the power amplifiers, is varied according to the amplitude of the input signal in a way that optimizes the LINC transmitter's efficiency. With this new power combiner, unlike most past designs, it is possible to obtain high power-added efficiencies (PAE) at the full dynamic output power range of the amplifier. The prototype is constructed with a balun transformer and two reactive terminations in which the shunt susceptance is varied parametrically with the degree of phase shift in the modulation. It is shown that this approach can improve the overall efficiency in the LINC system.

Agilent's advanced design system (ADS) software is used to compare this new combiner's effect on linearity and efficiency with three other classical power combiners. A two-tone signal and an IS-95 signal were used for the comparison. The results indicate that the new combiner is more effective than the others in improving the efficiency and does so with a lesser degradation in linearity. Using a transmitter with class AB power amplifiers having 23.5% efficiency at 2.14 GHz, the overall average efficiency of LINC system using the new combiner is 17.6%, whereas it is only 9.1% using a Wilkison combiner. The linearity was more intact with some of the classical, but less efficient, combiners, but the best compromise between efficiency and linearity was struck with this design. Suggestions for future work on this subject is also described.

RÉSUMÉ

Ce projet est consacré au développement d'un transmetteur LINC et à son implantation dans les systèmes modernes de communication sans fil tels que le IS95, le WCDMA et le CDMA2000. Plusieurs aspects de la conception du diviseur de signal (SCS) numérique, ainsi qu'un combineur de puissance à rendement élevé et à haute performance sont présentés dans cette thèse.

L'élément clé du transmetteur LINC est le diviseur de signal (SCS). La technologie de traitement du signal numérique (DSP) utilisée dans le diviseur de signal du transmetteur LINC s'avère le meilleur choix. Tout d'abord une version moderne du diviseur de signal utilisant un dispositif DSP standard a été évaluée. Ce dernier dispositif comporte deux désavantages importants: une faible largeur de bande et une consommation d'énergie élevée. Ensuite, un nouveau diviseur de signal numérique a été développé. Celui-ci comprend un FPGA (Field-Programmable Gate Array), qui améliore la flexibilité des algorithmes, augmente la vitesse du traitement des signaux et réduit la consommation d'énergie. Il représente une solution efficace pour réaliser le diviseur de signal numérique. Il nous donne la possibilité de manipuler les blocs et les registres arithmétiques pour mieux adapter les algorithmes, et permet de choisir une longueur de mot pour répondre à nos spécifications. L'apport en termes d'économie d'énergie et d'augmentation de la largeur de bande, est significatif.

Deux designs ont été implantés au FPGA (un Altera Quartus II FPGA kit) ; le premier comprend une table unidimensionnelle (look-up-table) et le seconde, un bloc de

fonction de racine carrée. La technique "pipelining" est employée dans les deux designs pour améliorer le temps de calcul. Elle a été utilisée fréquemment dans les systèmes nécessitants des calculs intensifs. Les simulations faites dans Simulink de Matlab ont servies à vérifier ces deux designs.

Le diviseur de signal numérique (FPGA) a été réalisé avec la carte de développement APEX DSP d'Altera. Les mesures de ce signal démontrent que cette nouvelle architecture est plus flexible, précise et performante qu'une conception utilisant un dispositif DSP. En plus, la version du 'look-up-table' était plus précise mais moins rapide que celle du bloc de fonction de racine carrée.

Ensuite, deux catégories de combineurs de puissance, (isolée et non isolée) ont été comparées selon une analyse de voltage / courant. L'impédance de charge, vue de l'amplificateur de puissance, varie en fonction de l'amplitude du signal. La valeur de réactance de shunt du nouveau combinateur s'adapte aux signaux pour améliorer l'efficacité énergétique pour tous les niveaux de puissance sortant du transmetteur. Par conséquent, l'efficacité du système est maximisée. Le combineur a été élaboré en utilisant un transformateur "balun", qui a un faible coût et de petites dimensions. Deux terminaisons réactives ont été réalisées avec des circuits LC où la valeur de la susceptance de shunt varie en fonction de la phase modulée.

La simulation des quatre différents combineurs a été exécutée avec ADS (Advanced Design System) d'Agilent, en utilisant un signal à deux fréquences et un signal IS-95. Les résultats obtenus indiquent que le nouveau combineur, contrairement au trois autres, améliore davantage l'efficacité sans dégrader pour autant la linéarité.

Deux amplificateurs de puissance de classe AB ayant une efficacité de 23.5% (fréquence centrale 2.14 GHz), ont été utilisés. Avec le nouveau combineur, une efficacité de system moyenne de 17.6% est atteinte pour une linéarité équilibrée, comparée à 9.1% en utilisant un combinateur classique de Wilkinson. Le meilleur compromis entre l'efficacité énergétique et la linéarité du signal a été obtenu avec ce nouveau combinateur.

Les travaux futurs sur ce sujet sont décrits.

CONDENSE EN FRANÇAIS

TRANSMETTEUR LINC POUR LES SYSTÈMES D'AMPLIFICATIONS LINÉAIRES

0.1 Introduction

Les systèmes de communication modernes exigent des techniques efficaces telles que des types de modulation sophistiqués, des algorithmes complexes de démodulation et une détection des erreurs d'une très haute qualité. Ainsi, il est possible d'obtenir des canaux de transmission à rendement élevé et sans perte. Cependant, ces types de modulation sophistiqués génèreront des signaux d'enveloppe variable et de crête sensiblement plus élevée que la moyenne de sorte qu'un amplificateur de puissance RF linéaire est requis. Il est donc nécessaire de linéariser un amplificateur de puissance non-linéaire pour rencontrer à la fois les exigences de haute linéarité et de faible consommation de puissance.

Bon nombre de techniques de linéarisation sont disponibles pour les applications commerciales. Certaines de ces techniques visent les systèmes à bande étroite tandis que d'autres, tel que la post-compensation, sont prometteuses pour les systèmes à large bande. Il n'est pas encore possible d'identifier des solutions économiques ayant toute les caractéristiques requises mais de telles solutions viendront dans le futur.

Les techniques appropriées de linéarisation sont la boucle cartésienne, la boucle polaire, la prédistortion adaptative en bande de base, la technique d'élimination et de

restauration de l'enveloppe (EER), l'amplification linéaire par technique d'échantillonnage (LIST), le modulateur universel combiné à boucle verrouillée (CALLUM), et l'amplification linéaire par composants non-linéaires (LINC) qui fait d'ailleurs l'objet de cette thèse. Les techniques de pré- et post-compensation peuvent opérer sur de larges bandes. Cependant, à ce jour aucune technique ne permet d'atteindre à la fois les exigences de linéarité et d'efficacité sur une bande de fréquence suffisamment large.

La technique LINC est l'une des techniques par sommation de vecteurs permettant de réaliser des amplificateurs de puissance RF à efficacité élevée tout en ayant, en théorie, une très bonne linéarité. Le principe consiste à prendre une forme d'onde modulée et de la décomposer en deux signaux à enveloppe constante, mais déphasés, qui alimentent ensuite des amplificateurs de puissance non-linéaires très efficaces. Il n'y a alors pas de distorsion d'intermodulation en raison de l'amplitude constante de ces signaux. En conséquence, des amplificateurs efficaces, mais non-linéaires, peuvent être utilisés pour remplacer les amplificateurs linéaires de d'autres architectures. Suite à l'amplification et la recombinaison, une version amplifiée du signal d'entrée est obtenue en sortie.

0.2 Séparation des composants du transmetteur LINC

Le transmetteur LINC permet d'obtenir une grande efficacité énergétique et les signaux indésirables sont réduitsde l'ordre de 30-60 dBc. Cependant, il est limité par la sensibilité du processus de conception pour obtenir deux amplificateurs parfaitement balancés. Cette sensibilité est principalement provoquée par le composant séparateur de

signal (Signal Component Separator) qui divise le signal de la source en deux signaux constants modulés en phase. La mise en application du SCS a été un des problèmes principaux dans le transmetteur LINC. Un premier article a suggéré une solution complètement analogique qui n'a pas eu un réel succès. Il est aujourd'hui possible d'implanter le SCS au niveau logiciel par les techniques de traitement numérique des signaux et l'utilisation d'un dispositif DSP standard permettant une précision suffisante au prix de contraintes de largeur de bande et de consommation de puissance. Cette solution est supportée par des conceptions fondées sur un processeur de signal numérique (DSP) ayant des restrictions dues au temps de calcul, au temps de conversion des convertisseurs A/N et N/A, au bruit de quantification et au coût.

Puisque la plupart des fabricants fournissent des logiciels d'aide à la conception pour leurs propres puces, la conception initiale, le coût et le délai d'arrivée sur le marché sont réduits et flexibles. Le FPGA (Field-Programmable Gate Array) est le meilleur choix pour les applications flexibles car il permet d'apporter des changements à la conception sans exiger de changements physiques au circuit imprimé, et ce aussi longtemps que les fonctions révisées sont compatibles avec l'espace disponible sur la même puce programmable. Dans ce projet, une nouvelle architecture numérique de séparation des composants du signal à base de FPGA permet d'avoir une architecture, une structure de bus et une mémoire adaptée aux besoins spécifiques de chaque utilisateur, et ce, à moindre coût et pour de bonnes performances. Le dispositif à haute vitesse FPGA qui remplace le DSP standard traitera tous les algorithmes avec plus de flexibilité. Nous

pouvons améliorer la largeur de bande et réduire la consommation d'énergie si nous choisissons des convertisseurs A/N et N/A avec un taux d'échantillonnage élevé.

0.3 Techniques de combinaison du transmetteur LINC

Simultanément, la réalisation d'un combineur pouvant atteindre une efficacité de puissance ajoutée (PAE) élevée est un autre facteur pivot pour obtenir une efficacité élevée avec une bonne linéarité.

Deux catégories de combineurs de puissance, isolés et non isolés, peuvent être utilisées dans les transmetteurs LINC. Le combineur de puissance isolé, tel le combineur Wilkinson, a une faible efficacité énergétique car la partie non utilisée du signal est dissipée par une charge passive. Même si des amplificateurs très efficaces étaient utilisés, une efficacité globale supérieure à 10% serait difficile à atteindre. Le combineur non isolé, tel le combineur à terminaison réactive variable, présenté dans ce travail, améliore l'efficacité puisque la variation de l'impédance dans le temps altère la consommation de puissance DC lorsque la puissance de sortie varie. Donc, l'efficacité globale de l'amplificateur LINC reste suffisamment élevée sur la majeure partie de la plage de puissance de sortie. Il y a une grande opportunité pour accroître significativement l'efficacité si les erreurs de phase et d'amplitude produites par cette approche peuvent être suffisamment bien contrôlées.

Pour réaliser la modulation de la charge en fonction du niveau de puissance de sortie désiré, les vecteurs doivent être des signaux représentant le courant ou la tension.

Un système LINC fondé sur des sources de tension idéales peut être quelque peu indépendant du niveau de puissance de sortie et de l'efficacité. Ce travail fournit un moyen qui optimise l'efficacité du transmetteur LINC en fonction des statistiques de modulation d'amplitude. Il est démontré que l'ajout d'une susceptance parallèle à la source de tension améliore grandement le ratio d'efficacité crête à la moyenne. L'efficacité moyenne de plusieurs signaux modulés en amplitude est déterminée en fonction de la réactance parallèle. La sélection de la réactance parallèle correspondant aux signaux permet de maximiser l'efficacité à une puissance de sortie donnée. Ce combineur est utilisé pour générer une porteuse modulée en amplitude en combinant deux porteuses de même fréquence, modulées en phase et d'enveloppe constante. De plus, il peut être construit en utilisant des éléments purement réactifs de sorte qu'aucune énergie n'est dissipée.

Typiquement, les systèmes déphasés Chireix [19] représentés par un circuit sommant coupleur-transformateur et un coupleur en ligne de transmission avec une réactance parallèle, permettent d'appliquer des variations conjuguées de charge aux amplificateurs de puissance non linéaires. Cependant, le maximum d'efficacité est atteint pour un niveau de sortie spécifique car la valeur de la réactance parallèle est fixe. Par conséquent, un des objectifs majeurs est d'implanter une nouvelle architecture de recombinaison pour obtenir une efficacité énergétique plus élevée aux sorties. Ce circuit peut être construit avec un transformateur d'impédance et des terminaisons réactives variables. En choisissant de façon appropriée la valeur de la réactance parallèle, il sera possible au combineur LINC d'atteindre son efficacité énergétique maximale. De plus, la

réactance peut être optimisée pour rencontrer à la fois les critères d'efficacité et de linéarité. Pour augmenter l'efficacité moyenne de modulation ayant un haut ratio crête par rapport à la moyenne, la terminaison réactive et le circuit de combinaison sont appliqués pour atteindre à la fois une efficacité élevée et une bonne linéarité.

0.4 La mise en application d'un transmetteur LINC

Ce travail de recherche développe et réalise un transmetteur LINC pratique fondé sur des techniques de traitement de signal numérique et des technologies efficaces de combinaison. Des améliorations de ces deux technologies fournissent des solutions pour le compromis difficile entre efficacité et linéarité élevée du transmetteur LINC.

0.4.1 Nouveau séparateur numérique de composants

Le séparateur de composants du signal décompose le signal source S(t) en deux signaux d'amplitude constante modulés en phase et décalés de $\pm\theta$, $S_1(t)$ et $S_2(t)$. Ces signaux modulés sont le signal en phase $I_1(t)$ / $I_2(t)$ et le signal en quadrature $Q_1(t)$ / $Q_2(t)$. Ils permettent d'obtenir l'enveloppe constante des signaux modulés en phase et en quadrature.

Un nouveau séparateur numérique de composants du signal (NDSCS) basé sur la technologie FPGA nous fournit une solution pour sélectionner arbitrairement la longueur des mots et minimiser le taux d'échantillonnage de sorte à rencontrer nos critères de conception. En effet, par rapport au processeur DSP, le FPGA devient la solution de

choix pour réaliser un séparateur numérique des composants d'un signal pour un transmetteur LINC en raison de la personnalisation de la conception.

Le NDSCS est mis en application sur une carte de développement Altera APEX DSP. Elle permet d'éviter les longs mots peu pratiques, les faibles taux d'échantillonnage, et les lents temps d'exécution lors du traitement du signal. Elle fournit également une architecture polyvalente pour accélérer les performances en plus d'avoir davantage de puissance de traitement des données brutes qu'un processeur DSP standard. Une réalisation matérielle peut être modélisée avec Simulink de MATLAB pour l'analyse et la vérification du concept. Le choix d'un dispositif FPGA qui s'adapte à tous les algorithmes permet d'obtenir rapidement un prototype. En outre, il est nécessaire de choisir des convertisseurs analogique-numérique (A/N) et numérique-analogique (N/A) ayant des taux d'échantillonnage suffisant. Ainsi, les exigences des conceptions des systèmes de traitement de signal à haut débit sont satisfaites.

Autant les méthodes utilisant le principe des tables unidimensionnelles (Look-Up-Table) que celles utilisant des blocs de fonctions en racine carrée ont été conçues dans Quartus II, le logiciel de conception du FPGA. Une LUT unidimensionnelle sans mémoire, qui est adressée I-carré plus Q-carré ($I^2 + Q^2$) avec des mots de 14 bits, stocke 26 bits de données calculées dans une mémoire à accès aléatoire (RAM). Deux bascules « flip-flops » paramétrables de type D sont employées comme blocs à délai temporel pour synchroniser les données afin d'obtenir la sortie correspondante.

Une méthode alternative est de créer en VHDL (Very High Speed Integrated circuit Hardware) un bloc de fonction dédié en racine carrée qui aurait un temps

d'exécution faible et présenterait de bonnes performances. La technique dite de "Pipelining" est nécessaire pour améliorer les performances. La combinaison de l'architecture registre-amélioré et de la connaissance du délai est une alternative attrayante aux FPGAs pour la mise en application de conceptions canalisées complexes dans des CPLDs, et avec de meilleures performances. Toutes les conceptions ont été simulées avec Simulink de Matlab pour valider le concept.

De plus, des mesures expérimentales démontrent que ce nouveau séparateur numérique de signal peut minimiser la longueur des mots avec une précision acceptable de sorte à réduire la consommation d'énergie et augmenter la largeur de bande.

0.4.2 Combineur à terminaison réactive variable

Le combineur à terminaisons réactives variables consiste en un transformateur d'impédance et deux éléments variables en parallèle sur deux branches. En comparaison avec un système à déphasage Chireix, ce modèle a deux susceptances parallèles, +Bv et – Bv, pour optimiser l'efficacité globale au lieu de la susceptance de compensation fixe ±B.

Le choix de la valeur des suceptances correspondant aux signaux peut améliorer l'efficacité à une amplitude de sortie donnée. L'impédance des éléments réactifs varie alors selon le décalage en phase, θ, entre les deux signaux S_1 et S_2. Donc, la tension de sortie peut être en phase avec le courant. La satisfaction de ce critère est le meilleur choix pour la combinaison LINC.

Le combineur pratique est construit à l'aide d'un transformateur d'impédance non isolé et d'éléments purement réactifs de sorte qu'aucune énergie ne soit dissipée. Les

terminaisons réactives sont alors réalisées en combinant des condensateurs variables et des inductances fixes en parallèle. L'admittance est variée avec le décalage en phase θ en changeant la valeur du condensateur ou de l'inductance. Un transformateur balancé à non balancé (balun) miniature, à faible coût et de performance suffisante est utilisé pour convertir l'impédance du port balancé au port non balancé en sortie. Ce combineur LINC amélioré n'utilise que des éléments réactifs et présente une charge n'ayant aucune partie imaginaire aux deux amplificateurs d'enveloppe constante pour tous les niveaux de la sortie modulée. Ainsi, le courant et la tension sont en phase au niveau de la charge.

Les éléments réactifs du circuit LC ont respectivement une susceptance capacitive +jBv et inductive –jBv. Ils ajustent le courant lorsque les signaux sont recombinés dans le combineur non isolé suivit de la charge désirée R_L. Si la réactance de la terminaison est choisie de façon appropriée, le courant sera additionné au courant de sortie de sorte que le courant total i_1/i_2 sera en phase avec la tension.

La réactance X est fonction de la phase modulée θ. Lorsque $X(\theta)$ est négatif, -X indique un élément capacitif et sera infini si θ est égale à zéro ou 90°. Pour le cas où θ=45°, X aura une réactance capacitive ($-k*R_L$).

Lorsque $X(\theta)$ devient positif, +X indique une réactance inductive ($+k*R_L$) à θ=45° et sera infinie si θ égale 0° ou 90°.

Les circuits réactifs peuvent être ajustés pour obtenir des valeurs de réactance allant de l'infini à $\pm k*R_L$ (inductif or capacitif). Nous considérons que les inductances L_1 et L_2 ont la même valeur et que les condensateurs C_1 et C_2 peuvent être ajustés selon l'écart de phase θ. Les circuits sont ajustés pour résonner à la fréquence porteuse ce qui

produit une réactance infinie. Lorsque la valeur du condensateur surpasse le point de résonance, le circuit devient capacitif. Inversement, lorsque la valeur du condensateur se situe sous la valeur de résonance, le circuit devient inductif.

Le module 3W525 de Anaren (fréquence 1.8-2.5 GHz) est utilisé en tant que transformateur d'impédance non isolé dans ce combineur. Il s'agit d'un transformateur « balun » mince dans un boîtier « surface-mount » ayant des impédances non balancée et balancée de 50Ω et de 25Ω, respectivement. Le combineur à terminaisons réactives variables permet, en théorie, 100% de modulation d'amplitude du signal à la charge de sorte que l'efficacité peut être maximisée en tout temps. Ces résultats de validation ont été obtenus par simulation dans ADS.

0.5 Conclusion

Le transmetteur LINC composé d'un nouveau séparateur numérique de composants du signal (NDSCS) et d'un nouveau combineur peut être utilisé comme amplificateur linéaire pour les modulations GSM, CDMA et WCDMA. Dans ce projet, deux contributions majeures ont été apportées dans la fabrication d'un transmetteur LINC. Premièrement, un nouveau séparateur numérique de composants du signal a été conçu et réalisé en utilisant une trousse de développement FPGA de Altera selon deux méthodes : la table unidimensionnelle (Look-Up-Table) et le bloc de fonction racine carré. Ces deux méthodes minimisent la longueur de mot tout en permettant une précision acceptable, ce qui réduit la consommation de puissance et accroît la largeur de bande.

Deuxièmement, un nouveau combineur à terminaison réactive améliore substantiellement l'efficacité de puissance ajoutée.

Le prototype du transmetteur LINC a été fabriqué et simulé avec un signal d'entrée IS-95 de largeur de bande 1.2288 MHz, un canal inférieur ACPR -89.4 dBc et un décalage de 885 kHz entre les canaux supérieur et inférieur. Le ratio global de la valeur crête par rapport à la moyenne était de 9.340dB.

Les résultats expérimentaux montrent que l'efficacité de ce transmetteur LINC est en moyenne de 17.6% pour des amplificateurs de puissance fonctionnant en classe AB et ayant une efficacité de 23.5% à la fréquence centrale 2.14 GHz. La sélection de la susceptance parallèle appropriée ±Bv peut donc optimiser l'efficacité et la linéarité tel que le démontre les résultats ci-dessous :

- L'efficacité moyenne est de 15.5% en utilisant un combineur à terminaison réactive variable avec susceptance parallèle. Le ACPR est de -57 dBc à 885 kHz de décalage. En ce qui concerne le niveau de puissance global de sortie, le ratio crête à la moyenne est de 8.3 dB.
- L'efficacité moyenne est de 13.6 % en utilisant un combineur à déphasage Chireix. Le ACPR est de -61 dBc à 885 kHz de décalage. Le ratio crête à la moyenne est de 8.6 dB.
- L'efficacité moyenne est de 10.2 % en utilisant un combineur en T sans susceptance. Le ACPR est de -63 dBc à 885 kHz de décalage. Le ratio crête à la moyenne est de 9.2 dB.

- L'efficacité moyenne est de 9.1% en utilisant un combineur Wilkinson. Le ACPR en sortie est de -65 dBc à 885 KHz de décalage. Le ratio crête à la moyenne est de 9.3 dB.

En conclusion, le combineur isolé, tel le Wilkinson, ne permet pas une impédance de charge variable et la puissance du signal en quadrature entraîne une consommation de puissance. Donc, l'amplificateur n'atteint son maximum d'efficacité d'opération qu'à la puissance maximale de sortie. Son efficacité décroît alors linéairement avec la diminution de la puissance de sortie. Ce comportement de l'efficacité est similaire à celui des amplificateurs en classe A qui ont une faible efficacité globale. Un combineur isolé avec pertes peut cependant préserver la linéarité de la puissance RF de l'amplificateur.

Un combineur non isolé est plus efficace qu'un combineur isolé mais souffre d'une moins bonne linéarité. La terminaison réactive parallèle est une méthode puissante selon laquelle un combineur non isolé peut améliorer l'efficacité énergétique. Cependant, l'utilisation de ces terminaisons réactives variables entraîne une erreur de gain ou de phase dans les deux branches et, conséquemment, une dégradation de la linéarité. Il est donc nécessaire de balancer l'efficacité et la linéarité en sélectionnant une valeur appropriée de réactance parallèle de sorte à maintenir le meilleur compromis entre l'amélioration de l'efficacité et la dégradation de la linéarité.

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ABBREVIATIONS AND ACRONYMS

3G	third generation mobile system
ACPR	adjacent channel power ratio
ADC	analog to digital converter
AHDL	Altera's hardware description language
ASDSP	application specific digital signal processing
CALLUM	combined analogue locked-loop universal modulator
CDMA	code division multiple access
CDMA2000	code division multiple access 2000
CPLDs	complex programmable logic devices
DAC	digital to analog converter
DSCS	digital signal component separator
DSP	digital signal processing
EER	envelope elimination and restoration
FPGA	field-programmable gate array
GSM	global system for mobile communications
HDL	hardware description language
IEEE	Institute of Electrical and Electronics Engineers
IMD	inter-modulation distortion
IP	intellectual property
IS-95	digital cellular standard IS-95

LEs	logic elements
LINC	linear amplification with non-linear components
LIST	linear amplification by sampling techniques
LO	local oscillator
LUT	look-up table
MAC	multiply accumulate
NCO	numerically controlled oscillator
NDSCS	new digital signal component separator
PA	power amplifier
PAE	power-added efficiency
PEP	peak output Power
PLLs	phase locked loops
QAM	quadrature amplitude modulation
RAM	random access memory
ROM	read only memory
PCS	personal communication system
RF	radio frequency
SCS	signal component separator
SOPC	system on a programmable chip
SRFB	square-root function block
VHDL	very high speed integrated circuit hardware description Language

VRTC	variable reactive termination combiner
WCDMA	wideband code division multiple access

CHAPTER 1
INTRODUCTION

1.1 RF Linearization techniques

For cellular mobile, wireless and other modern communication systems, more spectral efficient techniques are required to accommodate high-rate data transmission in a limited bandwidth. Various modulation schemes such as QAM, CDMA2000 and WCDMA have been introduced to improve spectral efficiency for different applications. However, these advanced modulation schemes generate non-constant envelope signals which often have high peak-to-average ratios which require very linear RF power amplifiers. Traditionally, class A amplifiers were operated with very high back-off, resulting in very poor efficiency. Hence a more efficient power amplifier is desired to replace the traditional class A amplifier. But due to the inherent non-linearity of these more efficient RF power amplifiers that generate significant in-band intermodulation distortion and out-of-band interference, they need to be linearized to meet today's stringent requirements for high linearity and low power consumption.

The aim of the various linearization techniques is to eliminate undesired in band distortion components and to avoid interference in adjacent channels. These techniques are challenging and complicated. They have been developed in areas such as multi-carrier base-stations, fixed point-to-point microwave radio links, satellite communications, etc.. Whatever the application, the goal is the same: to suffiently improve linearity while sacrificing the least amount of efficiency.

The wide-range of the linearization techniques can be divided into a number of approaches [1]. Figure 1.1 shows graphically how the various linearization techniques are related.

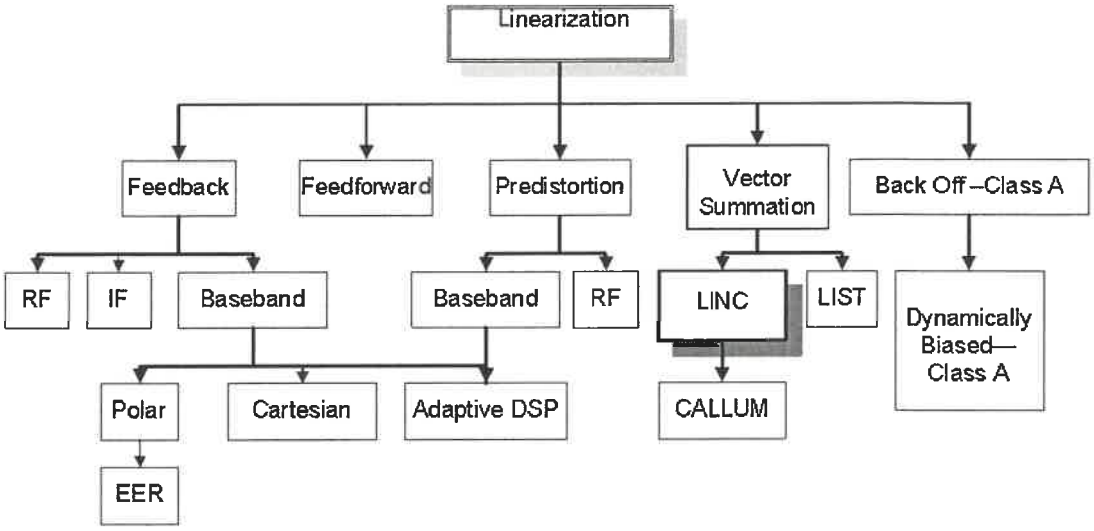


Figure 1. 1 RF amplifier linearization techniques

A number of linearization techniques are available for commercial applications, some for narrowband systems, and others, such as the feedforward technique, are promising for the broadband systems. It is not yet possible to find economical solutions to cover all the requirements. Appropriate linearization techniques include Cartesian loop, polar loop, Adaptive baseband predistortion, Envelope Elimination and Restoration (EER), **LI**near Amplification with **N**onlinear **C**omponents (**LINC**) which is studied in this project, and Combined Analogue Locked-Loop Universal Modulator (CALLUM), LInear amplification by Sampling Techniques (LIST). They are the most suitable techniques for narrow band applications, while feedforward and predistorsion techniques can operate over wider bandwidths. However, there is no technique so far

that can promise both high efficiency and very good linearity simultaneously over a sufficiently wide band.

LInear amplification using Non-linear Components (LINC) is a vector summation technique [2] for achieving a highly efficient RF power amplifier with very good linearity [3]. In this technique two constant envelope but varying phase signals are produced that are amplified and added (combined) to reform the desired varying envelope and varying phase signal at the output. For amplification of constant envelope signals it is not necessary to use a very linear amplifier; hence, more efficient amplifiers can be used to replace the linear (and less efficient and more expensive) amplifiers. The LINC transmitter can be applied to today's complex base station and portable applications. It takes the envelope modulated bandpass waveform and resolves it into two "out-phased" constant envelope signals, which are then applied to two highly efficiency and nonlinear power amplifiers. No intermodulation distortion is produced because the amplitudes of the signals handled by the two amplifiers are constant. After recombination (vector summation), a linearly amplified input signal is obtained at the output.

1.2 Literature review and background for LINC transmitter

The LINC radio frequency (RF) power amplifier was derived from the outphasing modulation technique developed in 1935 by H. Chireix [4]. Two power amplifiers were driven by a phase-modulated carrier and combined to produce a highly linear and efficient AM transmission at the carrier frequency. In 1974, Donald Cox first

proposed the "LINC" amplifier concept [5] which became the well- known acronym 'LInear amplification with Nonlinear Components', in which the input signal is decomposed into two phase-modulated signals. Then narrow-band linear amplification is achieved using efficient constant amplitude nonlinear amplifiers.

There were two major challenges in LINC transmitter systems: component signal separation and recombination. Many previous papers concentrate on LINC transmitters such as a VHF implementation of a LINC amplifier [6][7], an inverse-sine modulator for use in a decomposition circuit [8], an in-phase/quadratic processor for LINC [9], a broad-band combiner for LINC [10], a digital signal processor for LINC component separation, and the effect of imbalances and modulation on LINC performance [11]. They mainly consist of two solutions: analog or digital .

1.2.1 Analog solutions in LINC transmitters

Outphasing modulation can be used to obtain an AM signal by the use of counter-phase modulation and vector summation of two RF signals, which was marketed by RCA under the trade name "Ampliphase"[12]. This technique used two class C RF power amplifiers in parallel, fed by a phasing network that uses the envelope of the drive signal to control the relative phase of the RF signal fed to each amplifier. At low signal amplitudes, the power amplifiers are fed limited versions of the input signal that are nearly 180 degree out of phase, so they nearly cancel out at the amplifier output. At high signal amplitudes, the amplifiers are fed nearly in phase signals.

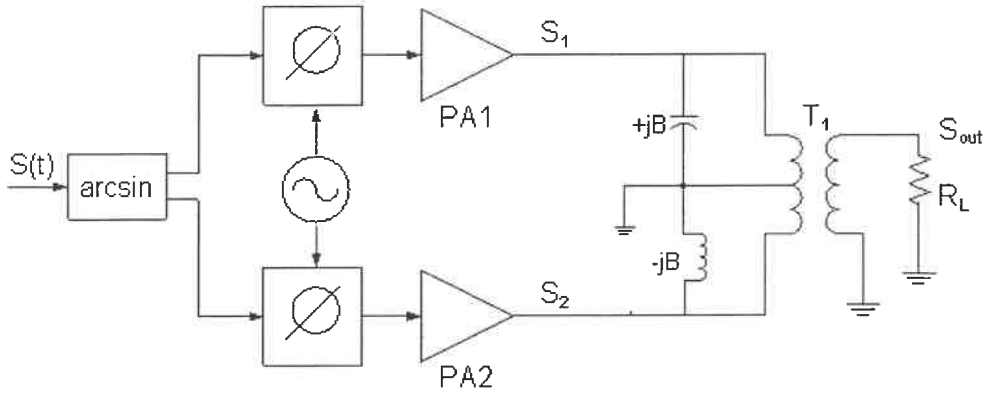


Figure 1. 2 Analog LINC transmitter

An outphasing transmitter produces an amplitude modulated signal by combining two constant envelope signals with different time-varying phases in the analog modulation. The inverse sine of the envelope S(t) produces the phase modulation $+\phi$ and $-\phi$ for the two PAs, shown in figure1.2. Basically, the phase modulation causes the instantaneous vector sum of the two PA outputs to follow the desired signal amplitude [5][9].

Cox achieved this complete analogue solution for component separation, but it suffered from bandwidth limitations and distortions that were caused by factors, in the phase modulator, limiter and envelope detector. For broad-band applications, system complexity prevented this analog technique from becoming widely accepted [13][14].

1.2.2 Digital solutions in LINC transmitters

Today, digital signal processing techniques make it possible to implement the signal component separator (SCS) in a standard DSP device with software which can provide sufficient accuracy [15][16]. However, it suffered from some constraints in

terms of bandwidth and power consumption. This solution executed by digital signal processor based designs which have some limitations in processor computing-time, A/D, D/A conversion time, quantization noise and price [17].

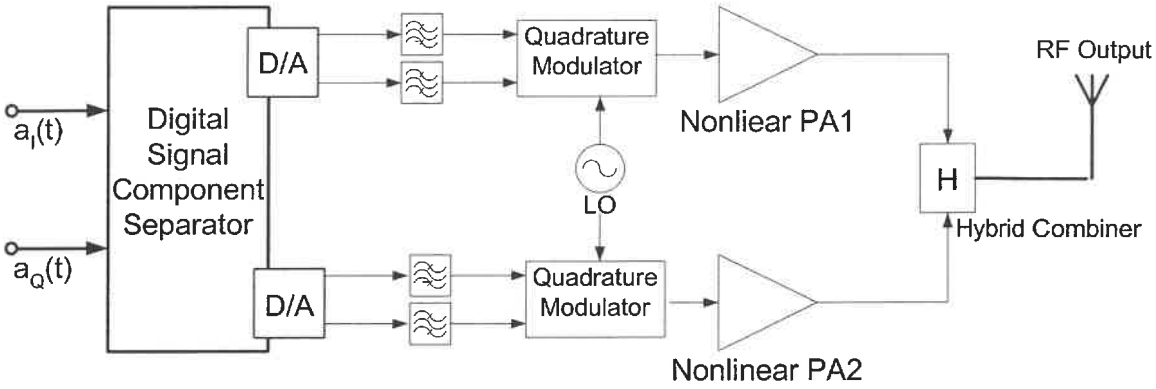


Figure 1. 3 LINC transmitter with digital signal component separator

With this scheme all processing is executed at baseband. See figure 1.3. The digital signal component separator generates two constant-envelope phase-modulated signals which are up-converted by a pair of quadrature modulators to translate the baseband signals to the desired carrier frequency. They are then amplified by two well-matched non-linear amplifiers, and then summed in the combiner. All undesired out-of-band components of the complex signals are in antiphase and therefore cancel at the output.

The difficulties with this method are in the production of the complex phase-modulated signals, the design of two well-matched amplifiers and the combination of the two high-power signals from the amplifiers.

1.3 Research goals

LINC technology is proposed to improve the linearity of power amplifier and enhance the power efficiency. There are many papers reporting clever implementations that have been studied and developed in the past years. The improvements of both efficiency and linearity were stated, but the inherent tradeoffs between these two parameters remain unresolved.

This research work develops and implements a practical linear transmitter for today's complex base station and portable applications. Improvements in digital signal processing and combining are providing solutions for the difficult task in achieving both high efficiency and linearity. A practical LINC transmitter is based on applying digital signal processing techniques, efficient combining technology and highly efficient non-linear power amplifiers such as class AB, B, C , as well as the switch-mode class E and class F. See figure 1.4.

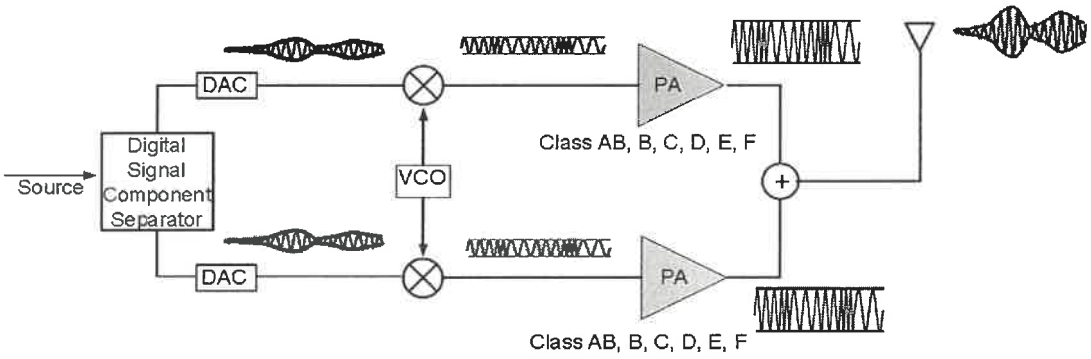


Figure 1. 4 LINC transmitter using DSP technique

This linear transmitter can achieve high efficiency and its spurious performance can be reduced in the order of 30-60 dBc [18]. However, one of its limitations is the sensitivity of the design to the balance between the two amplifiers. This is mainly caused by signal component separator (SCS) that splits the source signal into the two individual constant envelop phase-modulated signals. The implementation of the SCS has been one of the major problems in the LINC transmitter.

A new digital signal processing architecture based on FPGA (Field-Programmable Gate Array) allows the design to have a customized architecture, bus structure and memory in a cost-effective, high-performance digital signal processing scheme. High-speed FPGA devices process all algorithms more flexibly than a standard DSP device so that we can improve the bandwidth and reduce the power consumption. A/D and D/A converters having a significantly high sampling rate should also be selected.

In order to obtain high efficiency and good linearity performance simultaneously, the implementation of combiner that can achieve a high power-added efficiency (PAE) is a pivotal factor. Typically, Chireix outphasing systems [19] which has a transformer coupler summing circuit with shunt reactances result in conjugate output load variations applied to the nonlinear power amplifiers. But it only achieves the maximized efficiency at one specific output level because of the fixed shunt reactances. Hence, another major objective is on on implementing a new recombination architecture with variable shunt susceptance in order to obtain high power efficiency at variable output levels. It can be constructed with an impedance transformer and reactive terminations with tuning

elements as shown in figure 1.5. Dynamically and accurately selecting the shunt reactances would make it possible for the LINC combiner to achieve maximum efficiency for all output levels.

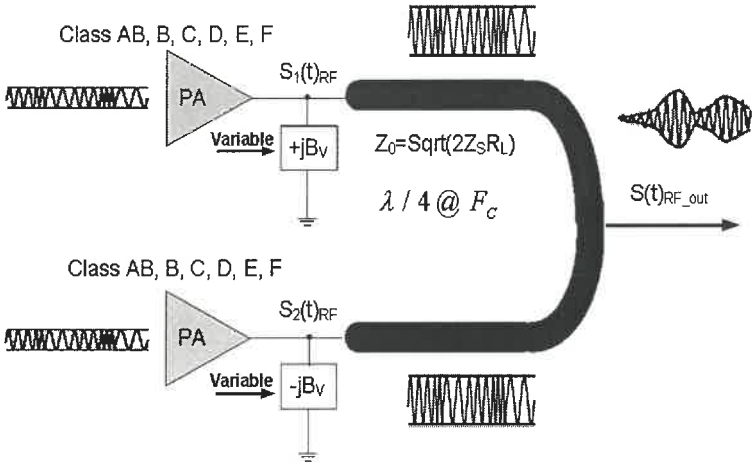


Figure 1. 5 Variable reactive termination combiner

1.4 Thesis organization

The remainder of this thesis is organized as described below.

In Chapter 2, the principle of the signal component separator (SCS) is analyzed in detail. The essential elements of our approach with an in-depth analysis is discussed. Moreover, it presents key techniques needed to implement this signal component separator. The new digital signal component separator (NDSCS) is based on an FPGA device which has been designed to achieve a higher performance of digital signal processing. All of the designs and experimental measurements using a Quartus II platform are validated by simulations in MATLAB's Simulink.

Chapter 3 analyzes LINC combination technologies and its voltage/ current model. The discussions and comparisons of the two main combiner types, represented in

four classical models, are analyzed in detail. The new combiner architecture is constructed using a balun transformer and variable reactive elements and is optimized for obtaining a suitable balance between efficiency and linearity. ADS simulations suggest that variable reactive terminations increase the efficiency significantly with only a reasonable loss of linearity.

The final chapter summarizes the major contributions of this work. Possible future work is suggested.

CHAPTER 2
THE SIGNAL COMPONENT SEPARATOR AND ITS IMPLEMENTATION

LINC is a technique that uses signal processing to produce linear amplification of bandpass signals with nonlinear components. The most two important signal processing functions of LINC are: 1) forming two constant envelope phase-modulated signal components from a band limited input signal. 2) recombinating the amplified components to produce an amplified replica of the input signal. Hence, the signal component separator is a significant objective of this research. It will be analyzed theoretically, and its practical and theoretical implementations will be described in this chapter and then some conclusions will be presented.

2.1 Introduction

The basic principle of the LINC transmitter is shown in figure 2.1 [3][13][14][16][17][18][19]. The source signal S(t) is decomposed by the signal component separator (SCS) into two constant amplitude phase modulated signals, $S_1(t)$ and $S_2(t)$. The constant amplitude signals are separately translated from baseband to RF by a carrier frequency in the quadrature modulators and then amplified by the nonlinear power amplifiers. After amplification the signals are recombined to form an amplified replica of the source signal. Since the amplitude of the two signals are constant, and therefore no distortion will be generated, the amplifiers can be nonlinear. Ideally the LINC transmitter is insensitive to nonlinear characteristics of the amplifiers.

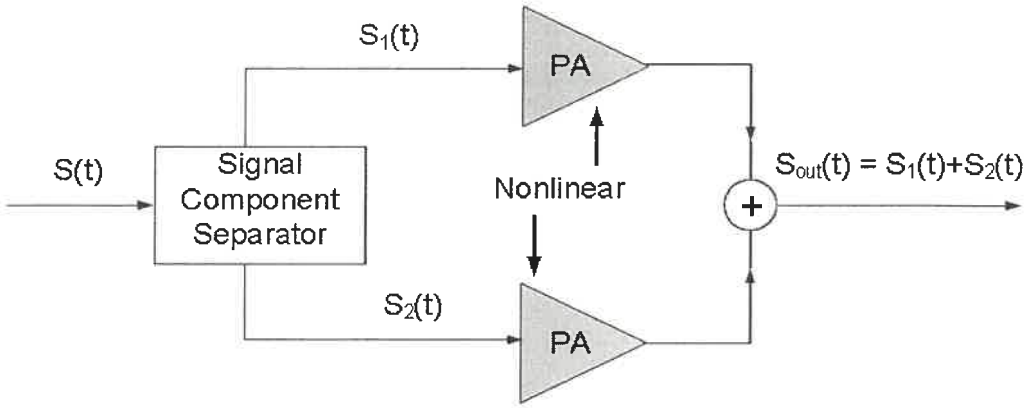


Figure 2. 1 Basic schematic diagram of the LINC transmitter

2.1.1 Basic analysis of the SCS

The source signal translated from baseband [20], can be representated as

$$S(t) = r(t) * e^{j\phi(t)} \quad ; \quad 0 \le r(t) \le r_{\max} \tag{2.1}$$

This input signal with envelope r(t) and instantaneous phase variation $\phi(t)$ can be split into two signals, $S_1(t)$ and $S_2(t)$, having modulated phases and constant amplitudes:

$$2 * S(t) = S_1(t) + S_2(t) \tag{2.2}$$

$$|S_1(t)| = |S_2(t)| = r_{\max} \tag{2.3}$$

where $S_1(t)$ and $S_2(t)$ are composed of the in-phase and quadrature phase components as shown in figure 2.2.

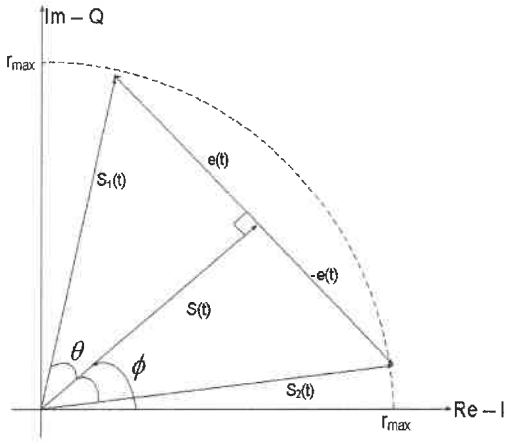


Figure 2. 2 Decomposition of signals in the signal component separator

Both phasors $S_1(t)$ and $S_2(t)$ can be obtained by summing the input signal with the vector +e(t) and –e(t) [15][20][21][22][23].

$$S_1(t) = S(t) + e(t) = r_{\max} e^{j[\phi(t)+\theta(t)]} \tag{2.4}$$

$$S_2(t) = S(t) - e(t) = r_{\max} e^{j[\phi(t)-\theta(t)]} \tag{2.5}$$

where $\theta(t) = \cos^{-1}\left[\frac{r(t)}{r_{\max}}\right]$ phase offset (0°- 90°) (2.6)

$r_{\max}$ is the maximum value of r(t), and e(t) is a signal that is in quadrature to the source signal S(t). Its equation is:

$$e(t) = j * S(t) * \sqrt{\frac{r^2_{\max}}{r^2(t)} - 1} \quad , \qquad |e(t)| \le r_{\max} \tag{2.7}$$

The quadrature signal e(t), is calculated and added / subtracted from S(t) respectively so as to obtain two constant envelope signals. When the separated signal components are recombined after amplification, the source signal part of each component is added in-phase, whereas the wideband signals cancel each other out.

It can be easily understood from (2.4), (2.5) that if the two signal branches are

perfectly matched, e(t) will ideally cancel its anti-phase counterpart, - e(t), and leave only the amplified source signal at the transmitter output. A small gain and/or phase imbalance would make this cancellation imperfect and result in IMD products. To attain high linearity in LINC transmitters, there must be a high degree of gain and phase matching between the two branches [20][21].

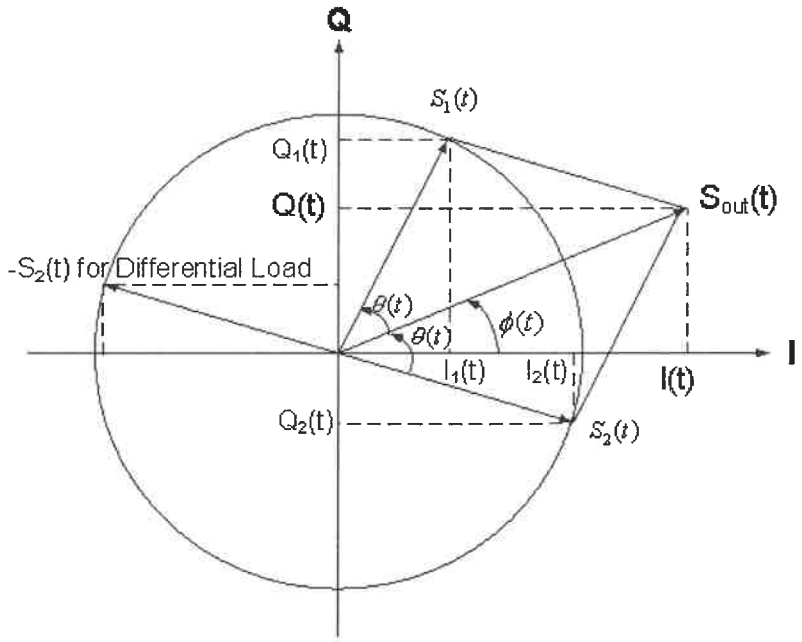


Figure 2. 3 Vector diagram illustrating relationship between components

2.1.2 LINC vectors in the Cartesian coordinate system

We can also analyze the LINC signal component vectors in a Cartesian system [23][24]. Figure 2.3 is a vector diagram illustrating the signal separation. The desired signal S(t) is decomposed into two equal amplitude signals $S_1(t)$ and $S_2(t)$.

$$S_1(t) = I_1(t) + j * Q_1(t) \tag{2.8}$$

$$S_2(t) = I_2(t) + j * Q_2(t) \tag{2.9}$$

$$S_{out}(t) = I(t) + j*Q(t) = [I_1(t) + j*Q_1(t)] + [I_2(t) + j*Q_2(t)] \quad (2.10)$$

Two modulated signals consist of the in-phase components $I_1(t)$ / $I_2(t)$ and the quadrature components $Q_1(t)$ / $Q_2(t)$. Their relationship is described below:

$$I_1(t) = I(t) - Q(t)\sqrt{\frac{1}{I^2(t)+Q^2(t)} - 1} \quad (2.11)$$

$$Q_1(t) = Q(t) + I(t)\sqrt{\frac{1}{I^2(t)+Q^2(t)} - 1} \quad (2.12)$$

$$I_2(t) = I(t) + Q(t)\sqrt{\frac{1}{I^2(t)+Q^2(t)} - 1} \quad (2.13)$$

$$Q_2(t) = Q(t) - I(t)\sqrt{\frac{1}{I^2(t)+Q^2(t)} - 1} \quad (2.14)$$

There is a common part in equations (2.11) to (2.14), named here as SR_Part.

$$SR\_Part = \sqrt{\frac{1}{I^2+Q^2} - 1} \quad (2.15)$$

It allows a means to obtain the constant envelope, phase modulated signals represented by their in-phase and quadrature phase components.

2.1.3 Unsolved problems in SCS

Previous analog approaches [5][9][13], where the SCS works at an intermediate frequency (IF) or at a carrier frequency, suffered from system complexity. Although various feedback [25][26] techniques were proposed to overcome these problems, there were bandwidth limitations due to the loop delay. Digital signal processing techniques were later introduced to produce the SCS in baseband using a standard DSP device [14][15][26]. Look-up tables were used which simplified SCS implementation.

However, two serious limitations in this type of DSP solution were : bandwidth and power consumption.

The first is because the word-lengths in DSP devices cannot be chosen arbitrarily and are either 16 or 32 bits, which are longer than required by the SCS. The second is because the sampling rate must be appropriately considered because the power consumption is proportional to the clock frequency. Hence, reduced bandwidth and increased power consumption occurred when a high speed DSP and D/A converters are used.

By minimizing the sampling rate we can minimize the clock frequency of the DSP described in [21], and by adapting a topology of registers and arithmetic function bocks to fit the algorithms, the word-length can be reduced. Therefore, for a standard DSP device, which typically operates using long word-lengths some constraints occur in terms of the bandwidth due to how well the algorithms suit the DSP architecture. And, in using high performance DSP devices to alleviate this, the power consumption rises.

On the basis of these problems, this work presents a new digital signal component separation architecture on FPGA which can improve bandwidth and reduce power consumption. The accuracy of signal separation processing which is taken into account also meet the requirement of SCS.

2.2 New digital signal component separator (NDSCS)

A new DSCS based on FPGA (Field-Programmable Gate Array) technology gives us a solution to choose a word length arbitrarily and to minimize the sampling rate

so as to meet our requirements.

2.2.1 Advantages of an FPGA device

Many digital signal processing applications can be implemented by DSP devices, but its hardware architectures are not flexible. Although DSP processors are programmable with software, they are limited by a fixed hardware architecture such as bus performance variation, memory, the number of multiply accumulate (MAC) blocks and hardware accelerator blocks, and as well as having a fixed data-width. For certain applications, such as customized digital signal implementation, like an SCS, a fixed hardware architecture is not advantageous.

An FPGA provides us with a reconfigurable solution for implementing digital signal processing applications [28]. It also has more power than DSP processors as far as raw data processing goes. At the same time, the FPGA can be reconfigured in hardware. It offers complete hardware customization for different applications. The customized architecture, bus structure, memory, hardware accelerator blocks, and a variable number of MAC (Multiply ACcumulate) blocks all can be implemented in FPGA devices which are an advantage when creating customized designs.

This flexible hardware which can implement the hardware design using a suitable hardware description language (HDL), such as VHDL or Verilog HDL, can implement the complete system inside a high-density FPGA. Furthermore, it can use the embedded silicon to form embedded memory, DSP blocks, and embedded processors. At the same time, accumulation, addition/subtraction, and summation blocks which are commonly

used for the arithmetic operations are offered in a digital signal processing block library.

A DSP processor can supply only a limited number of multipliers. The most important factor in the overall bandwidth limitation of digital signal processing is the multiplier bandwidth- FPGA devices offer much higher multiplier bandwidths than DSP processors. For example, Altera's FPGA device can deliver 70 GMACS of digital signal processing throughput and DSP processors only deliver maximum 4.8 GMACS. Altera FPGAs also have 10 Mbits of embedded memory to meet large amounts of data processing.

Embedded processors in the FPGA provide integration and flexibility for many digital systems. We can implement the system's software components in the embedded processors and implement the hardware components in the FPGA's general logic resources. The Nios embedded processor used in this FPGA provides us with a means to decrease the complexity of some inherently complicated arithmetic operations.

To sum up, it is difficult for DSP processors to trade-off the size and performance when they choose a variable bus on the chip. And DSP performance is limited by the predefined hardware accelerator blocks. However, FPGA devices can accelerate performance functions in hardware under a flexible platform. Hence, FPGAs become the best choice to implement a digital signal component separator in LINC transmitters, rather than a DSP processor, because of their ability for accommodating customized designs. They achieve the best performance due to hardware acceleration.

2.2.2 Basic NDSCS design

FPGA devices consist of logic elements (LEs) and memory that can be configured to operate in different modes according to functionality. The new DSCS configuration on the FPGA device processes all vector arithmetic. See figure 2.4.

First of all, it is important for us to know how accurate the SCS has to be when we choose a FPGA device. Moreover, the bandwidth of the phasors are substantially larger than that of the original input signal. FPGA devices and A/D, D/A converters operate with sampling rates at least 15-20 times the bandwidth of the input signal.

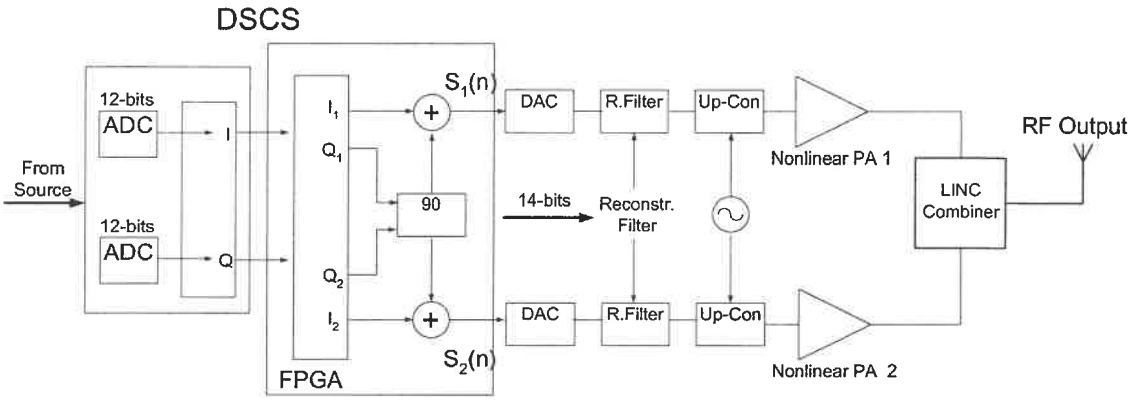


Figure 2. 4 LINC implementation with a new DSCS architecture

The source signal S(t) at baseband is decomposed during demodulation into I(t) and Q(t) components which are applied to the inputs of two A/D converters. Both 12-bit binary data I(n) and Q(n) after A/D conversion are then transmitted to the FPGA for digital arithmetic processing. Then two pairs of binary digit data, in-phase components $I_1(n)$ / $I_2(n)$ and quadrature components $Q_1(n)$ / $Q_2(n)$ are obtained in the FPGA. The components $I_1(n)$ / $I_2(n)$ are added to $Q_1(n)$ / $Q_2(n)$ which have been 90° phase shifted,

to form $S_1(n) / S_2(n)$.

$$S_1(n)=I_1(n)+jQ_1(n) \quad (2.16)$$

$$S_2(n)=I_2(n)+jQ_2(n) \quad (2.17)$$

Subsequently, the resulting constant amplitude digital signals $S_1(n)$ and $S_2(n)$ are converted to analog by two D/A converters. The outputs of the D/A converters pass through low-pass filters to remove unwanted high-frequency components. The signals are then translated to RF by two up-converters having the same local oscillator (LO). Finally, the RF signals are amplified by two non-linear high efficiency power amplifiers and summed in the LINC combiner to obtain a linear amplified RF signal at the output.

2.2.3 Challenges in the NDSCS design

The most difficult part is in the realization of a square root block that includes division and the square root arithmetic calculation for $SR\_Part = \sqrt{\frac{1}{I^2+Q^2}-1}$ (2.15). These operations are usually avoided, when possible, because they are very time-consuming. Previous digital techniques used two-dimensional look-up tables to realize SR_Part. It was addressed by the real and imaginary parts of the input signal [21][22] and have large table sizes. This was a unique solution implementing the square root function block this past year.

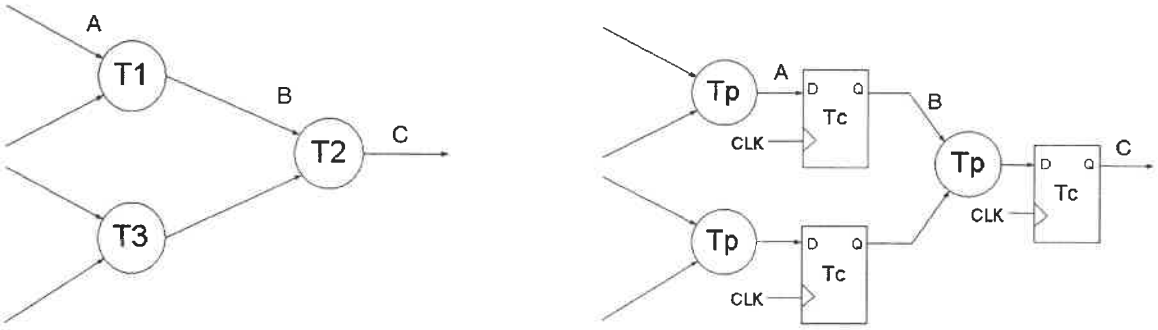
Clock synchronization is another important factor for data processing. Every arithmetic block inherently causes a clock delay, which can result in data asynchronization in the various calculation stages. In order to obtain correct data, it is

necessary to synchronize the clock so as to ensure that all required data are acquired during the same clock period in each processing stage.

Two techniques are introduced to solve this problem: pipelining and delay blocks. Implementing SR_PART (2.15) in the FPGA using pipelining techniques reduces the table size and increases the processing throughput. Delay blocks make it possible to synchronize data at each stage.

2.2.3.1 A key in NDSCS design --- pipelining technique

In a computational system, pipelined design techniques are used when building a functional block for CPLDs (Complex Programmable Logic Devices) [28] in different digital applications. To Pipeline a design, registers are inserted in every stage of the circuit. A K-stage pipeline is an acyclic circuit having exactly K registers (one register for every stage of the path) from input to output.



(a) Before adding the registers **(b) After adding the registers**

Figure 2. 5 A combinatorial design and a pipeline design

Figure 2.5 shows a combinatorial design that includes two stages and a pipelined design. In figure 2.5 (a), where T_1 or T_3 are the delay for the first stage, T_2 for the

second stage. The maximum T_1 or T_3 plus T_2 will form the propagation delay obtained from a computation result.

In the pipelined design, see figure 2.5 (b), the sum of T_1 or T_3 and the T_c (clock to output time) of the register is the total delay for the first stage. The second stage of registers has a similar delay of T_2 and T_c.

- (T_1 or T_3) + T_c = delay of the first stage
- T_2 + T_c = delay of the second stage

The overall clock period of the pipelined design will be the maximum sum of $[\max(T_1,T_3)+T_c]$ and (T_2+T_c).

- $[\max(T_1,T_3)+T_c]+ (T_2 + T_c)$ = overall delay of the pipelined design

The advantage of pipeline design is the increased throughput. However, it takes two clock cycles here to obtain the very first computation result. The initial clock cycles required to obtain the first result is called the latency. The propagation delay, T_p is assumed the same for T_1, T_3 and T_2. Hence, $2*T_p$ is the delay for the combinatorial design and the sum of T_p and T_c is for the pipelined design.

The latency is the amount of time for the initial or longest path. Throughput is the amount of time required after repeated operation. In the case of a combinatorial design, the latency and throughput will be the same at $2*T_p$. But for the pipelined design, the latency and throughput are different at $2*(T_p+T_c)$ and (T_p+T_c) respectively. If T_c is faster than T_p, determined by the CPLD hardware, then the pipelined design will have a faster throughput than the combinatorial design.

In order to implement a high performance, complex, and pipelined design in CPLDs, a register-rich architecture having predictable delays, available in FPGAs, offers a desirable solution.

From the above analysis, pipelining technology is key to increasing throughput, and thus performance. Furthermore, available register-rich architectures makes it possible to implement computationally intensive functions.

2.2.3.2 Another key in NDSCS design --- delay technique

We also have to pay close attention to the cycle times which determine the maximum delay through a given pipelined segment; and also to the processing-delays of the arithmetic function blocks. Delay blocks can be used to realize synchronous functions and to avoid undesirable asynchronous affects.

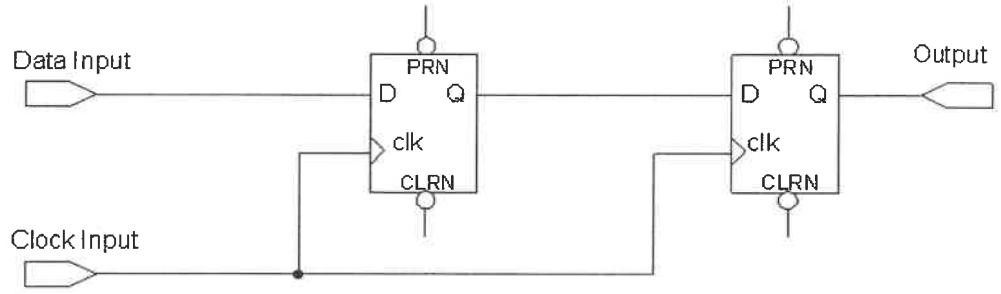


Figure 2. 6 Multiple-stage synchronizer

Designing a delay block is presented in two ways. The first is implemented using D-type flipflops. Several parameterized D-type flipflops are operated as timing-delays to synchronize the data and obtain the correctly timed output data. In figure 2.6, two D-type flipflops are cascaded to form two stages in a synchronizer to delaying the timing by two cycles.

A D-type flip-flop, also called a D-type bistable, is a subsystem having two stable states. Using appropriate input signals, we can trigger the flip-flop from one state to the other. The logic state at the DATA input is transferred to the Q output on the rising edge of the CLOCK signal. Hence, it can be used to delay timing cycles.

The second way is in coding a delay block in Very high speed intergrated circuit Hardware Description Language (VHDL), to synchronize the processing data. Function block LPM_DFF is coded to operate as the frame of the delay block. Inside of LPM_DFF, some parameters, such as width, determines the size of the input and output , and the depth, which presents the delay time that can be selected by the designer, depending on the design needs. See appendix A.

2.3 Design Details for NDSCS

2.3.1 Analysis of two methods for implementing SR_Part

This work presents two methods for implementating SR_Part (2.15). A simple but powerful one-dimension look-up-table (LUT) can store the data output of the square-root result which is addressed by the square of I(n) plus the square of Q(n). Hence, it results in a low-memory size LUT to realize accurate data processing instead of using a two-dimensional look-up-table which has an extremely large memory requirement [29]. In doing this, two important factors have to be ensured: that the table is long enough for storing the calculated data and that the values in the LUT have enough precision to accomplish the required linearity of the output signal. This means, for one, that little or no envelope ripple presides in the separated component signals. Therefore, selecting a

reasonable LUT size with enough memory is very important in DSCS design.

The alternative method is in realizing the SR_Part directly by implementing a square-root function block. A typical square root block can be commercially acquired from Atera's intellectual property (IP) block library for Quartus II version 2.0. But it uses more processing time than any of the other arithmetic blocks such as the adder, subtractor and multiplier. In fact, DSP designers can not use this IP block because it is only built by a simple base frame, and lacks many details and design codes.

For up-to-date techniques, Altera provides parameterized megafunctions that are optimized for Altera device architectures [30]. In order to increase design complexities, Altera released a square-root megafunction named ALTSQRT in September 2004. It must be run in Quartus II version 4.1 or later, especially for Stratix and Cyclone family devices.

The ALTSQRT megafunction also supports the APEX 20K family devices which is used in this project. It is an efficient way to implement a square root function in the Altera FPGA. Extra latency that the designer selects reduces the delay along the critical path and can increase the overall function's performance. However, the output bus width of ALTSQRT is merely half of the input width (W/2). Although the width of the remainder port is equal half of the input width plus one [(W/2)+1], it does not present the fractional part- it comes from the remain-bit of data processing. The result is that the square of output data is not equal to exactly the input data- it is only an approximate value. Hence, the accuracy of ALTSQRT is a weak point.

If it were possible to design a customized square root function block with higher

overall performance and accuracy, the NDSCS performance would be improved in this second method.

Coding an effective square-root function block called SRFB in VHDL is introduced to meet our design goal. This function block belongs to a base-level design and is coded in VHDL where we can flexibly select the output size, and code the pipeling registers into the programmed block. See appendix B. Thus, it can process the complicated square-root arithmetic with high processing speed and improved accuracy.

2.3.2 Design environment

An Altera APEX DSP development board (professional version) is employed to implement the digital signal component separator. It is a development platform providing us with an economical solution for hardware verification [31], which consists of an APEX EP20K1500E-1X device in a 652-pin package, two 12-bit 65MHz analog-to-digital (A/D) converters, two 14-bit 125 MHz digital-to-analog (D/A) converters, 512 Kbytes of 10-ns asynchronous SRAM in the memory subsystem and digital/analog I/O connectors. This functional development board gives us an efficient method to construct a digital signal processing system. The customized designs are implemented by this board combined with DSP intellectual property (IP) and "megafunctions" to achieve many different arithmetic tasks. Altera Quartus® II 2.0 version design software supports this FPGA design, synthesis, place-and-route, verification, and device programming.

2.3.3 Method 1--- LUT implementation

The less memory intensive approach uses a one-dimensional look-up table which

is addressed by I-square plus Q-square (I^2+Q^2). In figure 2.7, two 12-bit / 65 MSPS analog to digital converters convert two input analog signals, I and Q, into binary digit data. The output format to each A/D converter is a 12-bit two's complement number, which is signed, and a fractional part. The two's complement signed fractional numbering system uses an N.M binary digit format, N represents the binary integer portion and M represents the binary fractional portion. It must have the radix point '.' which determines the portion of integer and fraction in arithmetic operations. Also, the numbers are padded with zeros and a sign-extension to obtain the result.

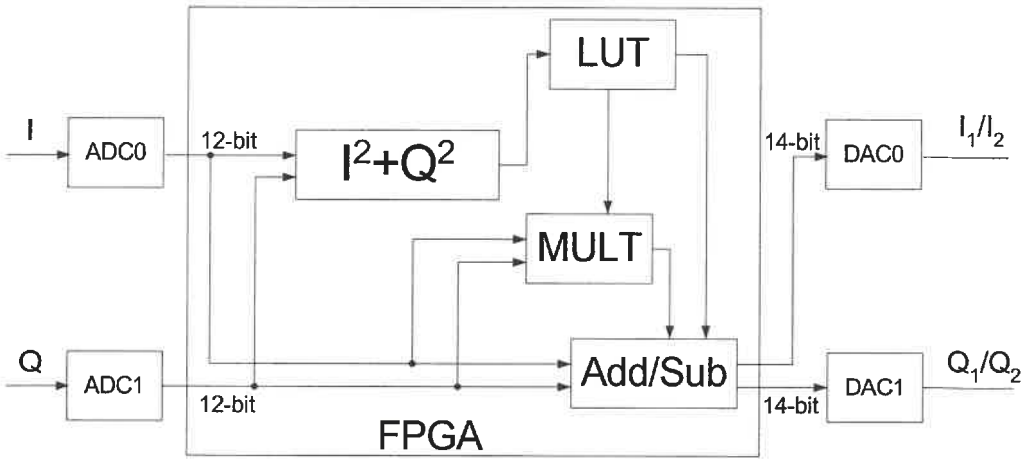


Figure 2. 7 Method 1 ---LUT design block diagram

In Quartus II 2.0, two 12-bit input data are multiplied by two parameterized multipliers (LPM_MULT) residing in Altera's arithmetic library, and then added by a parameterized adder to obtain the 24-bit data (I^2+Q^2). By extracting 14-bit of data from the adder's 24-bit of output, it operates as a LUT input address so as to obtain a 16384 ($=2^{14}$) bit look-up-table. All of the calculated data for SR_Part (2.15) are then stored as 26-bit data (N=12, M=14) in the parameterized dual-port random access memory (RAM)

which is megafunction block. The 26-bit output of the LUT is multiplied again by LPM_MULT, and then add/subtracted to produce the digital signal components, $I_1(n)$ and $Q_1(n)$. The detail design inside the LUT blocks, are described below.

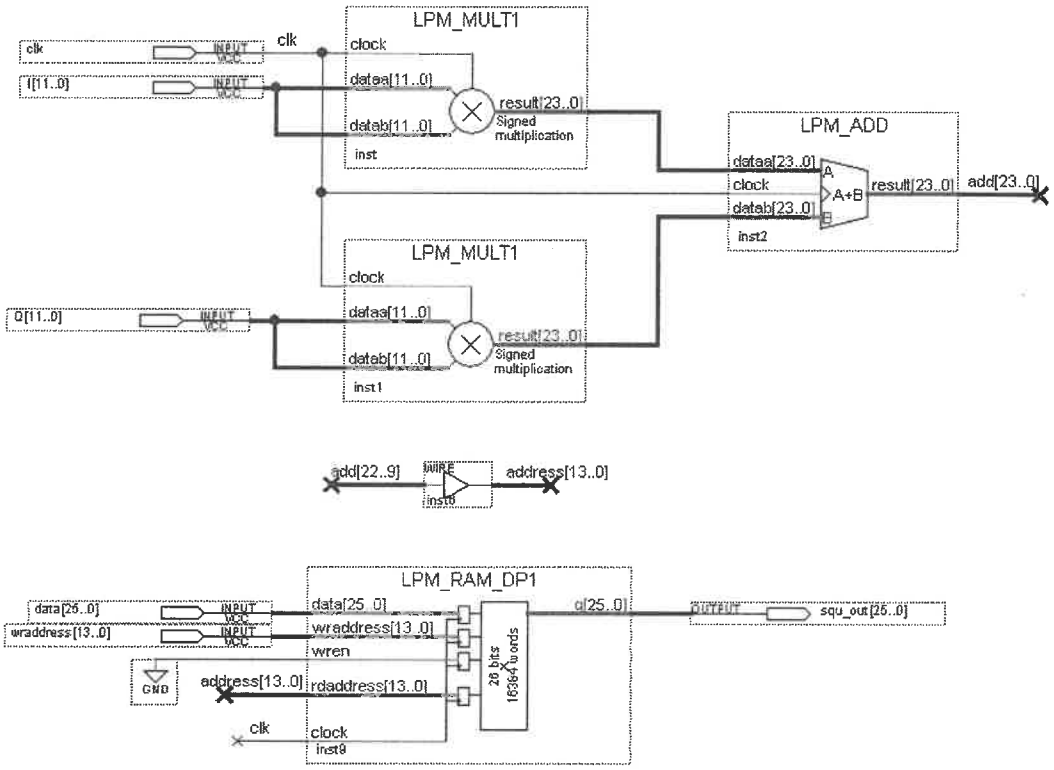


Figure 2. 8 LUT 16384 design block in Quartus II 2.0

It is strongly recommended to use a multiple-stage synchronizer to obtain the correct output data. This design uses a multiple-stage synchronizer where two or more flipflops are cascaded to form a synchronization circuit to delay the data two or more clock cycles. Figure 2.9 is a three-stage delay block which is designed in the Quartus II 2.0 and delays three timing cycles. A Four or more stage delay block is similar to the three-stage block.

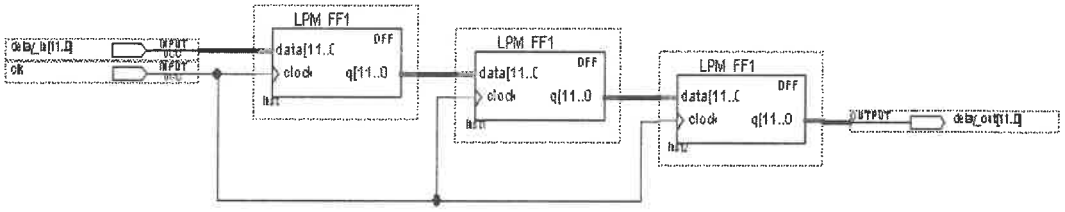


Figure 2. 9 Three LPM_FF block for a three clock cycle delay

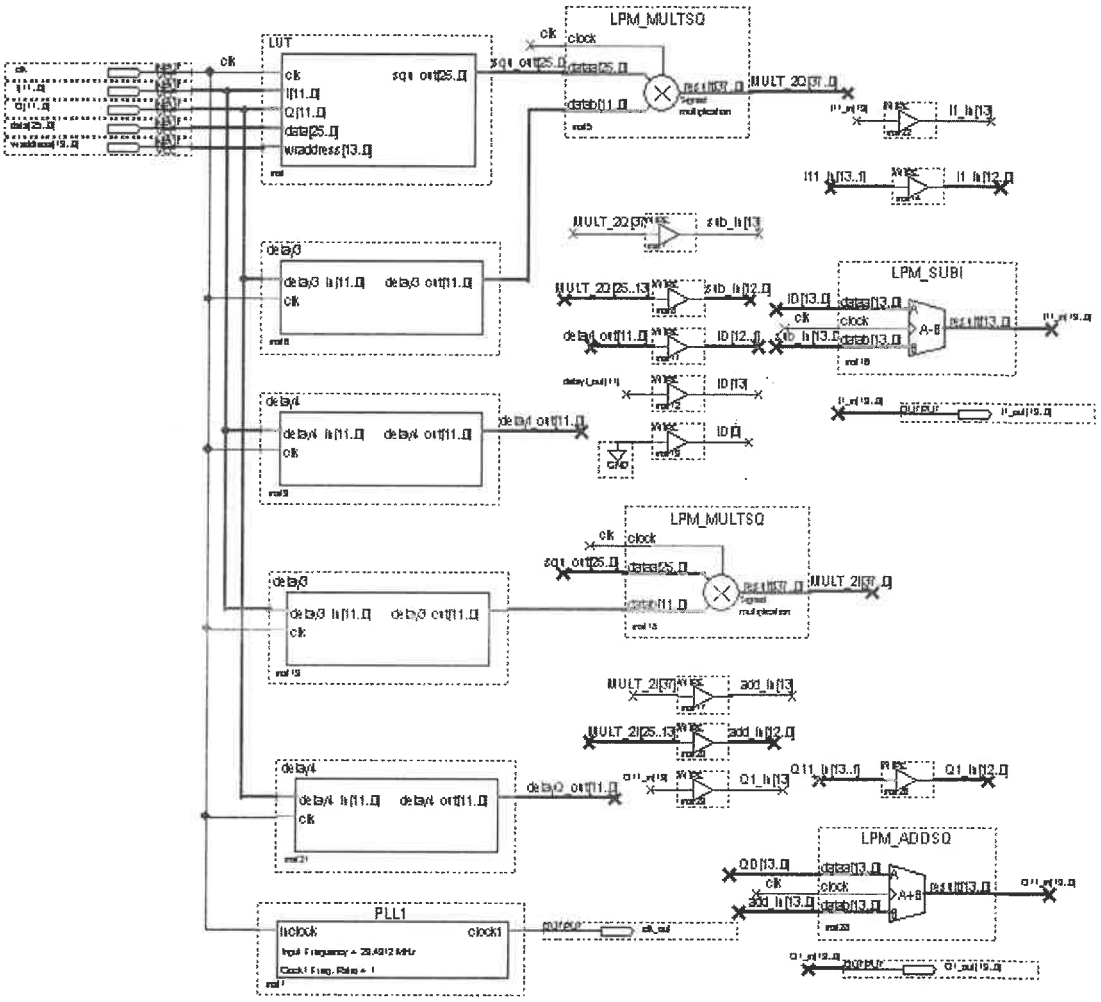


Figure 2. 10 Top level design for I_1 (n) & Q_1(n) with LUT in Quarus II 2.0

In the method 1 design, each arithmetic block is available in the Altera DSP library. They are processed during one timing cycle. Even though pipelined cycles can be chosen in the design, we still know how many integral timing cycles are interleaved. Therefore, D-type flipflop delay blocks are adequate for the method 1 design.

In figure 2.10, three-stage delay blocks, are implemented by cascading three D-type flipflops to delay the timing by three timing cycles, and four-stage delay blocks are operated to delay the timing by four timing cycles.

2.3.4 Method 2 --- square root function block (SRFB)

The second method is realized by a square-root function block (SRFB), coded in VHDL. See appendix B. It achieves the square-root arithmetic with in less time while still maintaining enough accuracy. The pipelining technique that inserts registers in every stage is also coded into the SRFB block using VHDL. Its advantage is the increased throughout and performance as compared to a functionally equivalent combinatorial design. In addition, the design must add a delay block at every stage especially when pipelining is used. The programmed delay blocks with different depth values are applied to this SRFB method. See appendix A.

In figure 2.11, inside of the square-root block is : [1/(I*I+Q*Q)-1]. A divider and an effective square-root block are used to calculate the data directly with more speed. In the practical design, 10-bit constant unit that represents one (2^{10}=1024) is the numerator of the divider, and an 8-bit data extracted from the fractional portion M of (I^2+Q^2) is input to the denominator. The quotient of divider has the same word-length as the

numerator, 10-bit digit [9..0], and the remainder is leaved as 8-bit [7..0]. Furthermore, pipelining the function with the output latency of 4 clock cycles is used to increase the processing speed in the divider.

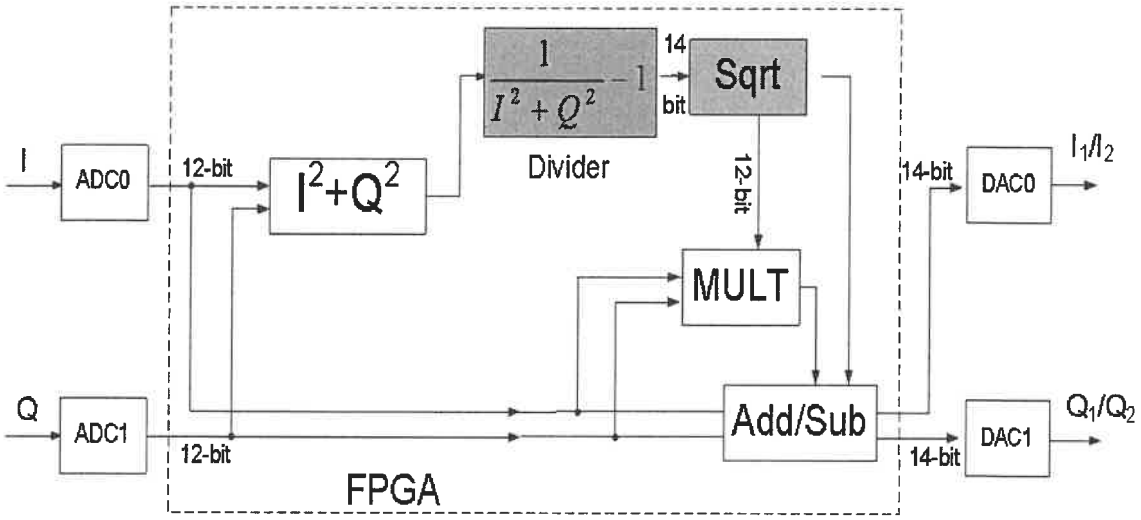


Figure 2. 11 Method 2 - Square-Root Function Block design diagram

Subsequently, the 10-bit portion of the quotient is subtracted by one, and contributes to the high ten-bits of the 14-bit square-root input [13..4]. In the meantime, the high 4-bit of the remainder becomes the low 4-bit of the square-root input [3..0]. So a combination of the 14-bit data becomes the input of the square root, and results in a 12-bit square root output.

In this new SRFB, the output of square root achieves a large bus width, having only 2-bits less width than the input (W-2). Compared with the ALTSQRT (output_q=W/2), it is easy to see that the new SRFB has more accuracy than ALTSQRT due to its larger bus size at the output, when the same bus width is used at the inputs.

The detail design for implementing the SR_Part function block in the Quartus II

2.0 is shown in the following diagram:

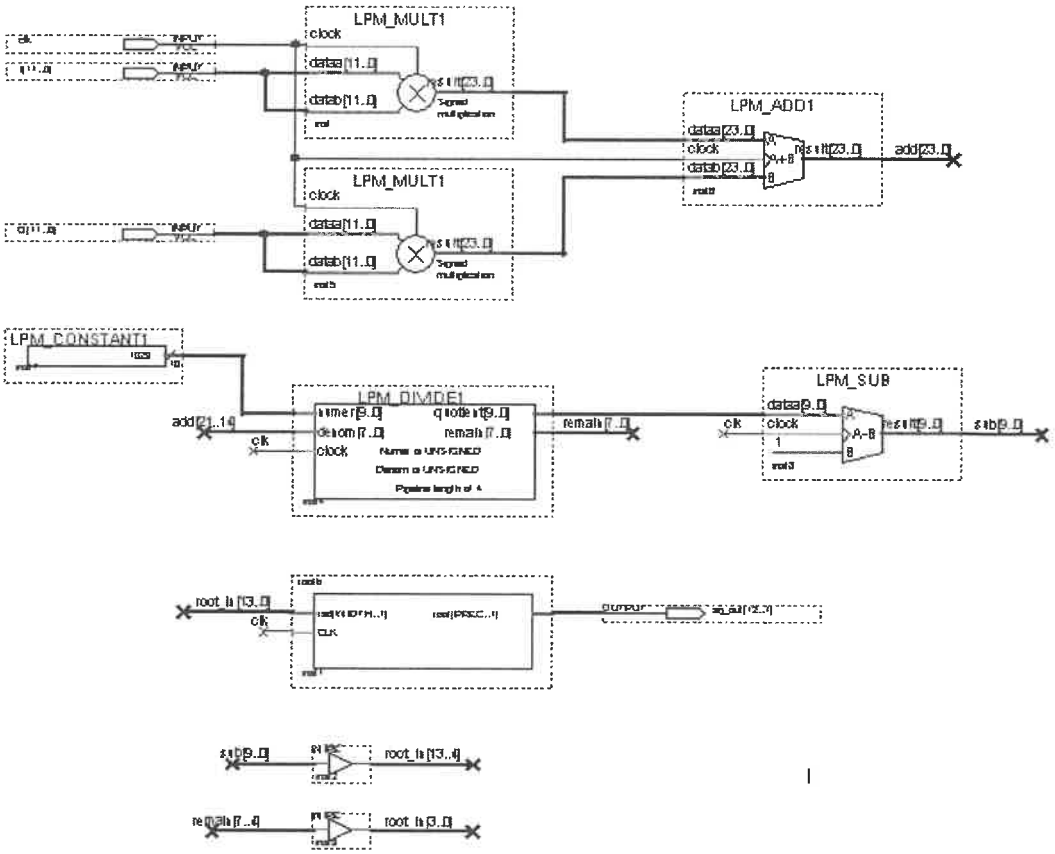


Figure 2. 12 SR_Part implementation of SRFB in the Quartus II 2.0

In Quartus II 2.0, a new SRFB is used to realize the customized square root function. However, it produces more delay than the other blocks due to the programmed pipelining segment, and it leaves non-integral timing cycles. So it is better to use a programmed delay block (appendix A) instead of a flip-flop delay block because its depth value can be adjusted arbitrarily by the program code. Two delay blocks with a 22 and 29 value depth are used so that synchronization is achieved in the overall design. See figure 2.13.

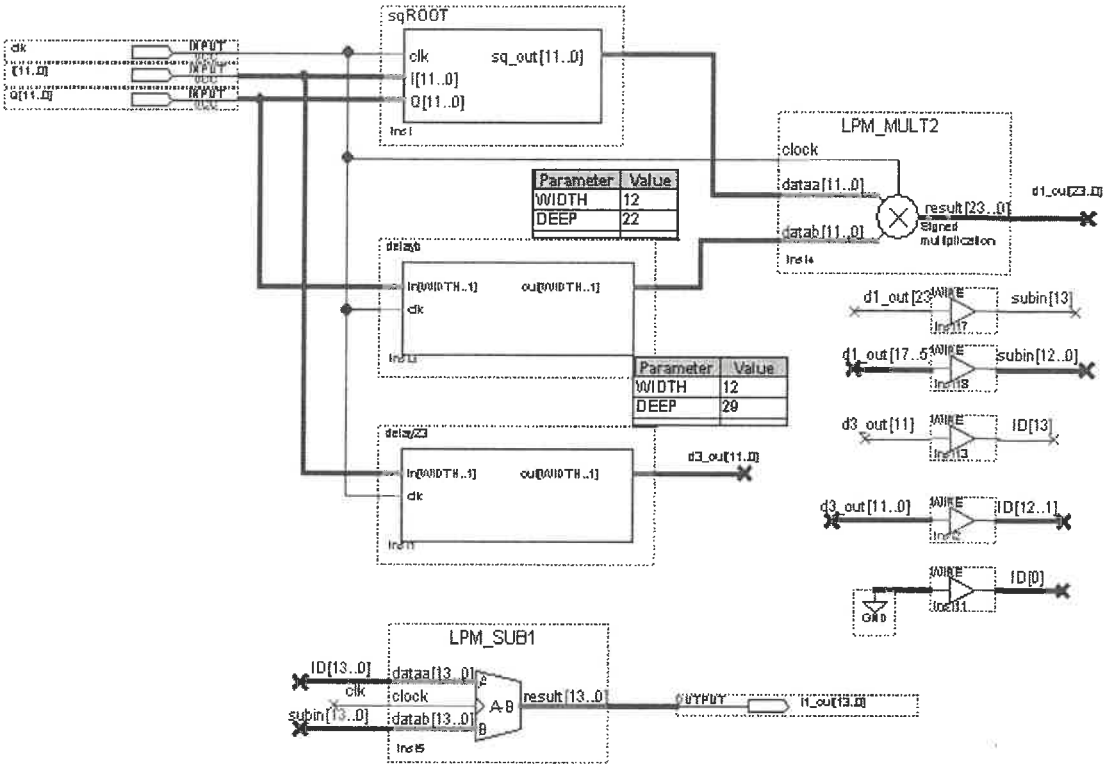


Figure 2. 13 Top level design for $I_1(n)$ with SRFB in the Quartus II 2.0

2.3.5 Combination in baseband

Digital components $I_1(n)$ / $I_2(n)$ and $Q_1(n)$ / $Q_2(n)$ are obtained by the two design methods in the Quartus II 2.0. Two D/A converters are employed to convert the digital components to analog components. A numerically controlled oscillator (NCO) that generates a digital representation of sine and cosine waves can be used as the local oscillator to modulate $I_1(n)$ / $I_2(n)$ and $Q_1(n)$ / $Q_2(n)$ into $S_1(n)$ / $S_2(n)$ in baseband.

2.4 Design in Simulink of MATLAB

Altera's DSP builder development tools integrate algorithm development, simulation, and verification capabilities of MATLAB. MATLAB's Simulink, a system-level design tool, is used for synthesis, evaluation and simulation. The accurate Simulink blocks, which cover basic operations such as arithmetic or storage functions, are applied in the different designs.

In order to verify the two designs in Quartus II, we build the same designs in Simulink having the same input and output bus widths. Subsequently, simulations in Simulink can prove the design in Quartus II to be correct or not.

The digital signal component separator (DSCS), using our two methods of look-up-table and square-root function, is implemented by an arithmetic block design model in Simulink. The input I and Q, which come from the SMIQ and AMIQ instruments used, are saved as two *.txt files, and are imported to the MATLAB workspace by 2-D array matrix format files with one array of signal values, and the other array of time steps. The functional arithmetic blocks such as adder, subtractor, multiplier and divider etc, are available in the Simulink block library (that include all the Altera DSP blocks). Design details are described below.

2.4.1 Method 1--- LUT implementation

The embedded memory in the Simulink library, such as ROM, can be used to read out pre-loaded data, so that it operates as a one-dimensional look-up table, addressed by (I^2+Q^2), to store all of the calculated results. In addition, the ROM block is

read as an intel-format hexadecimal file (*.hex). Thus, the following steps need to be done: First, the program code edited as an M-file in MATLAB, used to calculate all the data, converts the data from decimal to hexadecimal. Second, a hex file is generated with hexadecimal data in Quatus II and downloaded into LROM. Third, two models for I_1 and Q_1 are built by arithmetic blocks and the LUT, which have the properly chosen word-length for the input address. Finally, the complex output signal ($S_1 = I_1 + j* Q_1$) is formed by a real-to-image complex block. All data processing is achieved at baseband.

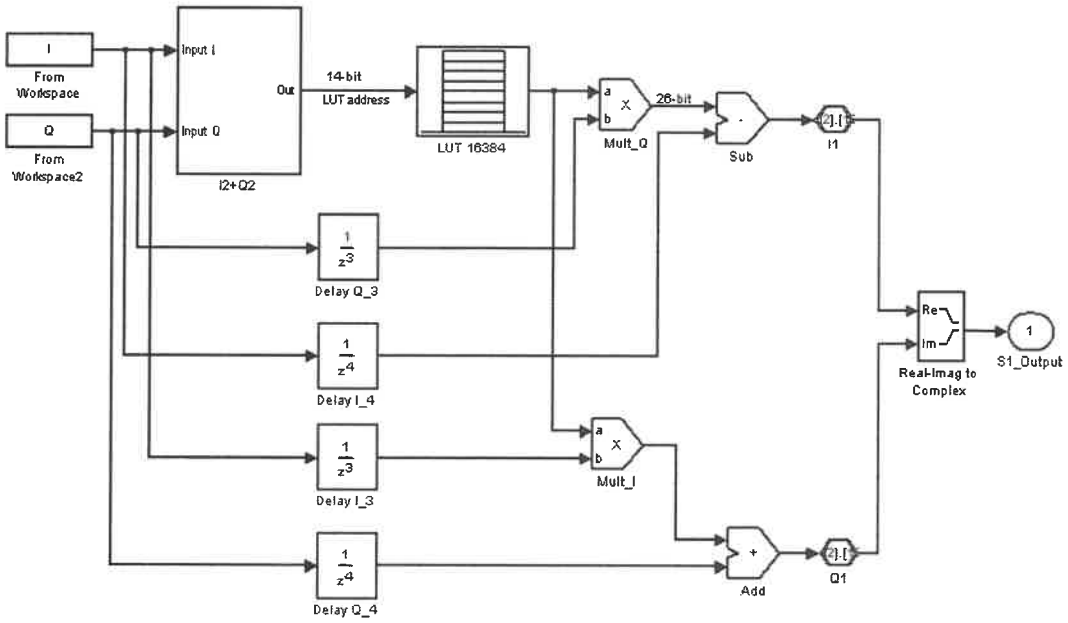


Figure 2. 14 Top level design for S_1 in Simulink ---- method 1 LUT

Note: The S_2 design in Simulink is similar with the S_1design.

2.4.2 Method 2 --- Square Root Function Block

In the Simulink library, there are many arithmetic operators available such as

adder/subtractor, multiplier/divider, logical operators, mathematical functions and a specified expression function block specified in C language. In our example, we need to use a square root function block to calculate data. Simulink can implement a complicated arithmetic function more easy than some other options. The square root block is implemented by a Simulink expression "Fcn" block which applies the square root function.

Figure 2.15 shows S_1 design in Simulink with method 2 --- SRFB.

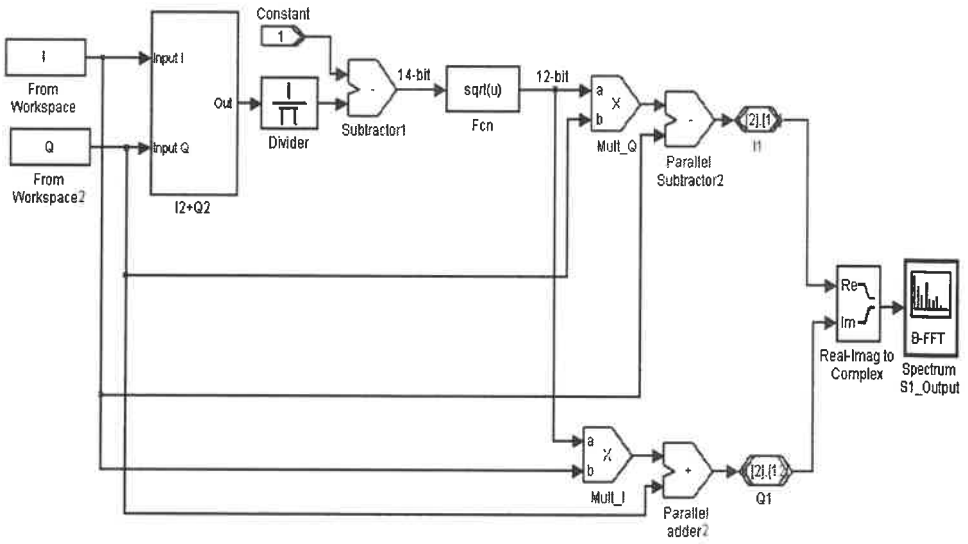


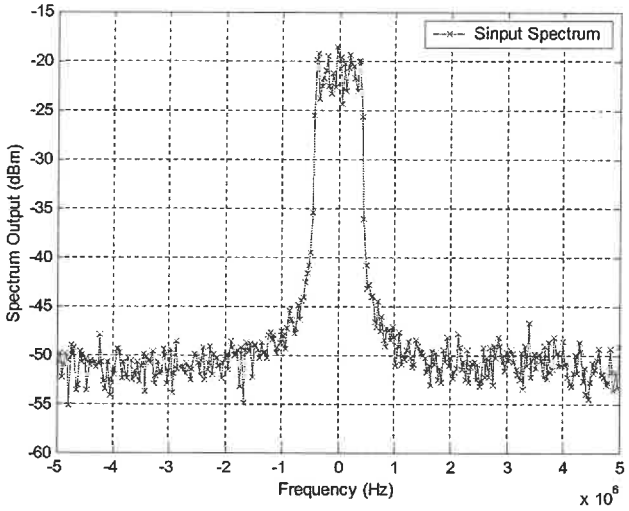
Figure 2. 15 Top level design for S_1 in Simulink ---- method 2 SRFB

Note: The S_2 block diagram in Simulink is similar with the S_1 design.

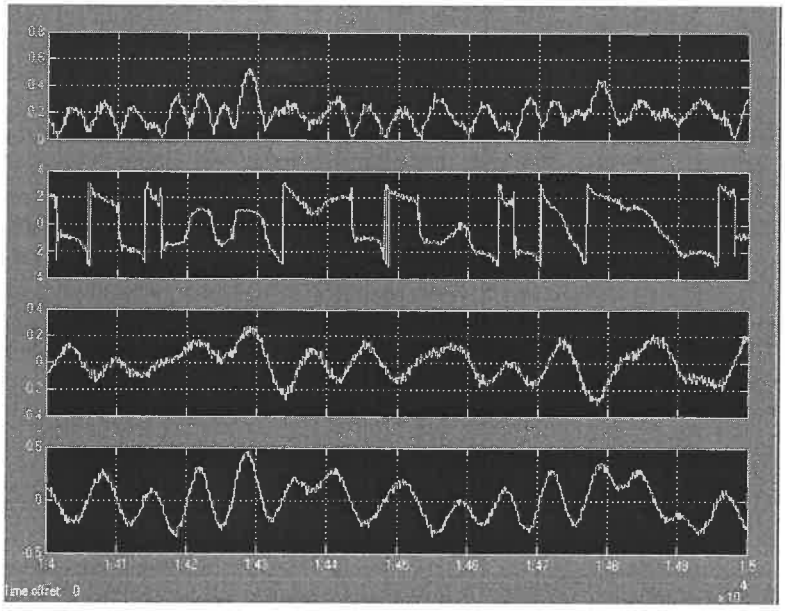
2.5 Simulation results in Simulink

2.5.1 Input signal in Simulink

The input signal consists of the real part I and the imaginary part Q that are generated from the I/Q modulation generator AMIQ and signal generator SMIQ. In this work, we use an IS-95 input signal. The following figure shows the IS95 signal.



(a) Input IS95 signal in frequency domain



(b) Input IS 95 signal in time domain

First axis: magnitude of S_input(t)

Second axis : phase of S_input(t)

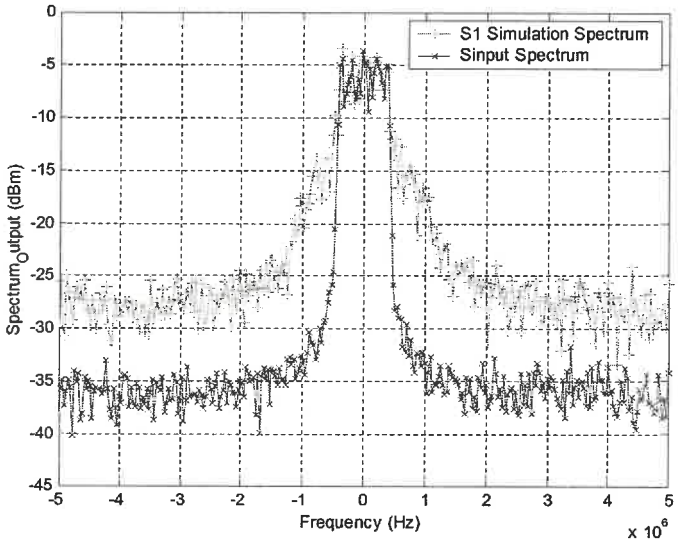
Third axis: I -- real part of S_input(t)

Fourth axis: Q -- image part of S_input(t)

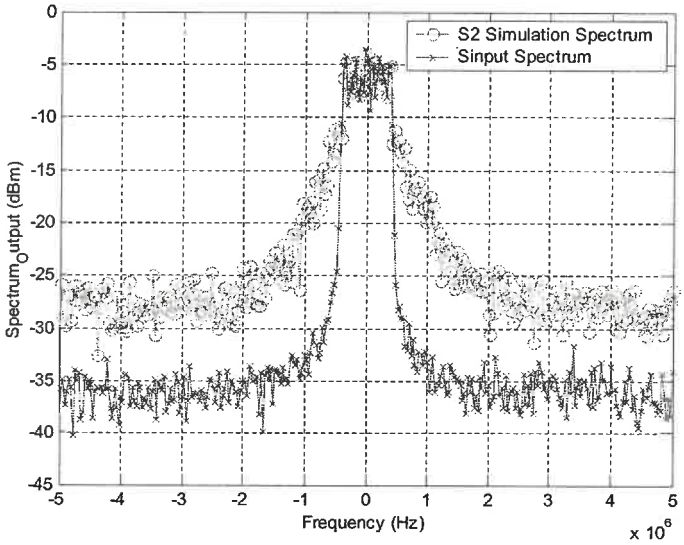
Figure 2. 16 IS95 input signal

2.5.2 Spectrum of constant envelope phase modulated signals in Simulink

In the simulation parameter set-up, after selecting the start-time and stop-time, Simulink can run the simulation automatically. The set up details are as follows: "Altbus" is bus block in the Simulink digital library, it can operate as ADC or DAC with a 12-bit signed fractional type, (1-bit integer, 11-bit fraction) is input, and the 26-bit data (12-bit integer, 14-bit fraction) is stored in the LUT to obtain the output of the square-root ($\sqrt{\frac{1}{I^2+Q^2}-1}$). The 14-bit data of I_1 / Q_1 (2-bit integer, 12-bit fraction) is then output to form the complex $S_1(t)$ and $S_2(t)$.



(a) S_1 and input signal S in Simulink

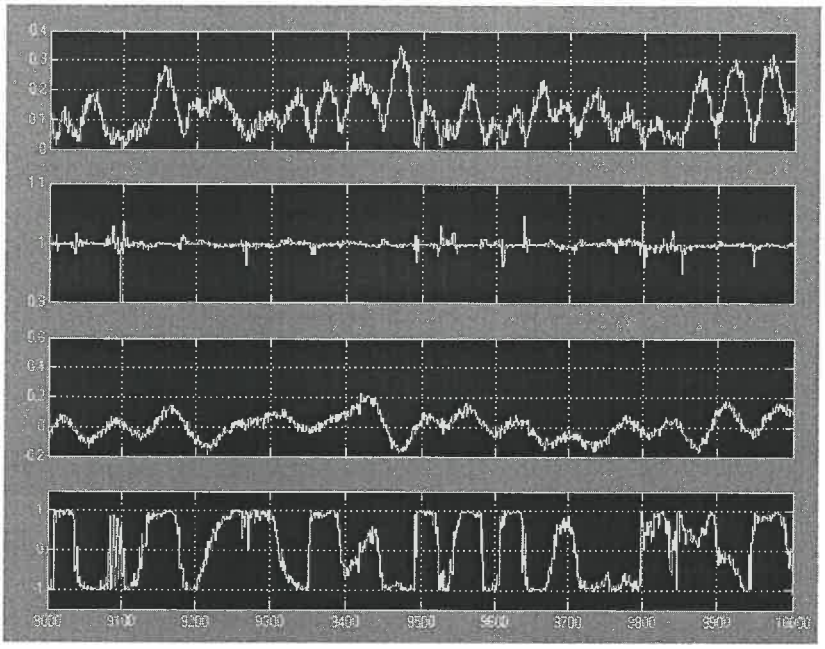


(b) S_2 and input signal S in Simulink

Figure 2. 17 Simulation results in Simulink

2.5.3 Constant envelope phase modulated signal in time domain

The simulation results in the time domain are displayed below. The magnitude of the input signal is mag(S). mag(S_1) represents the magnitude of S_1 signal. The real part is I(t) and I_1(t), the imaginary part is Q(t) and Q_1(t). It is demonstrated that S_1(t) has a constant envelope while input signal S(t) has a non-constant one.



1^{th} **axes ---- mag(S)**

2^{th} **axes ---- mag(S_1)**

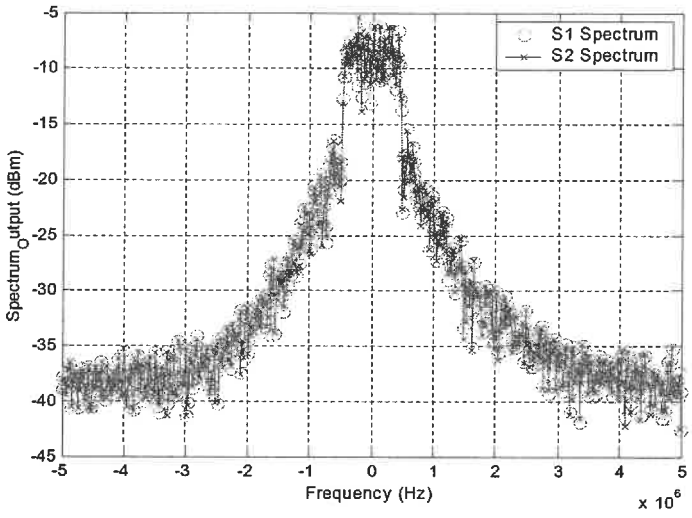
3^{th} **axes ---- real(S)=I(t)**

4^{th} **axes ---- real(S_1)=I_1(t)**

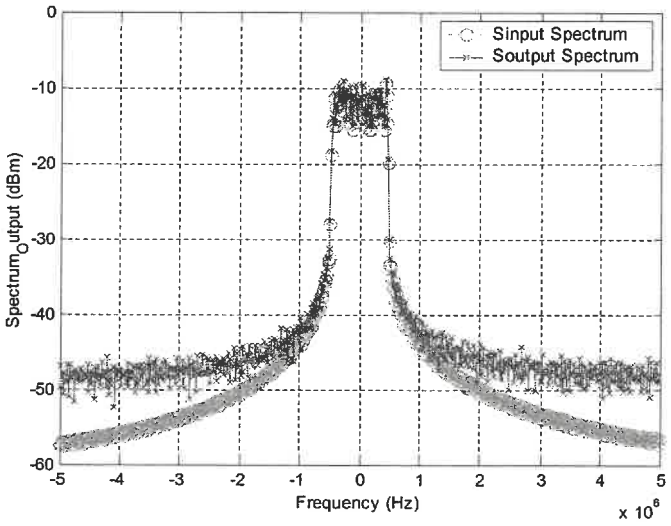
Figure 2. 18 S and S_1 in time domain of Simulink

2.5.4 S_1 and S_2 combination at baseband in Simulink

Finally, we recombine the two constant envelope phase modulated signals S_1 and S_2 into S_{output} in baseband. The resultant signal S_{output} is the desired replica of the original source signal.



(a) Constant envelope phase modulated signals S_1 and S_2



(b) LINC output S_{output} and input signal S_{input}

Figure 2. 19 Recombination spectrum in Simulink

2.5.5 Two methods comparison in Simulink

Both the one-dimensional look-up table (LUT) and the square-root function

block (SRFB) methods are compared in the Simulink simulations. In figure 2.20, the curve marked by the "x" is the look-up table solution. It is addressed by 14 bits of data ($2^{14} = 16284$ RAM memory), and the output of the LUT is 26 bits (12-bit integer, 14-bit fraction).

The other one shows the output spectrum using the SRFB. This method takes more time for data processing, so it is important to carefully limit the input and output data lengths while still meeting the accuracy requirement. Therefore, in this design we could choose only a 12-bit (7-bit integer, 5-bit fraction) data length for the output of the SRFB (Sqrt Fcn) as being a reasonable compromise between word-length and accuracy.

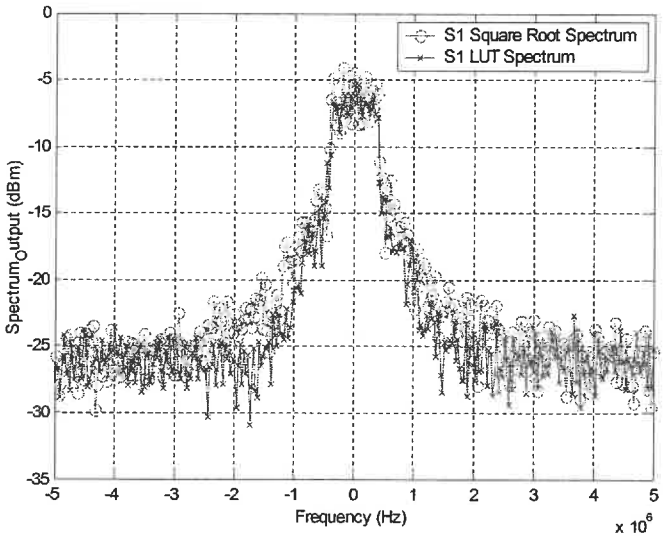


Figure 2. 20 S_1 spectrum comparison between LUT and SRFB

Therefore, this clearly shows that the LUT method is more accurate than a customized square-root function block solution in Simulink. In the results the output spectrums are slightly different. Comparing the output spectrum results, the LUT

spectrum has a better result than the SRFB spectrum because its out of band spurious spectrum is lower.

2.6 Experimental results for verifying Quartus II design

2.6.1 Measurement setup

A ROHDE & SCHWARZ arbitrary waveform / vector signal generator SMIQ, I/Q modulation generator AMIQ, and the Simulation Software WinIQSIM™ are used together to form the generation of the I/Q signals. SMIQ provides a convenient generation of high-precision signals of CDMA 2000 and IS-95 digital standards. The AMIQ is a dual-channel modulation generator which consequently has an I/Q source. It can be programmed by the software WinIQSIM™ to output an I/Q signal at baseband. These two pieces of equipments are used as signal generators for the measurement.

The Altera APEX DSP development board with the APEX™ EP20K1500E-1X device works as the digital signal component separator. It contains two 12-bit 65-MHz analog-to-digital (ADC0/ADC1) converters and two 14-bit 125-MHz digital-to-analog (DAC0/DAC1) converters. The measurement set-up is shown in figure 2.21.

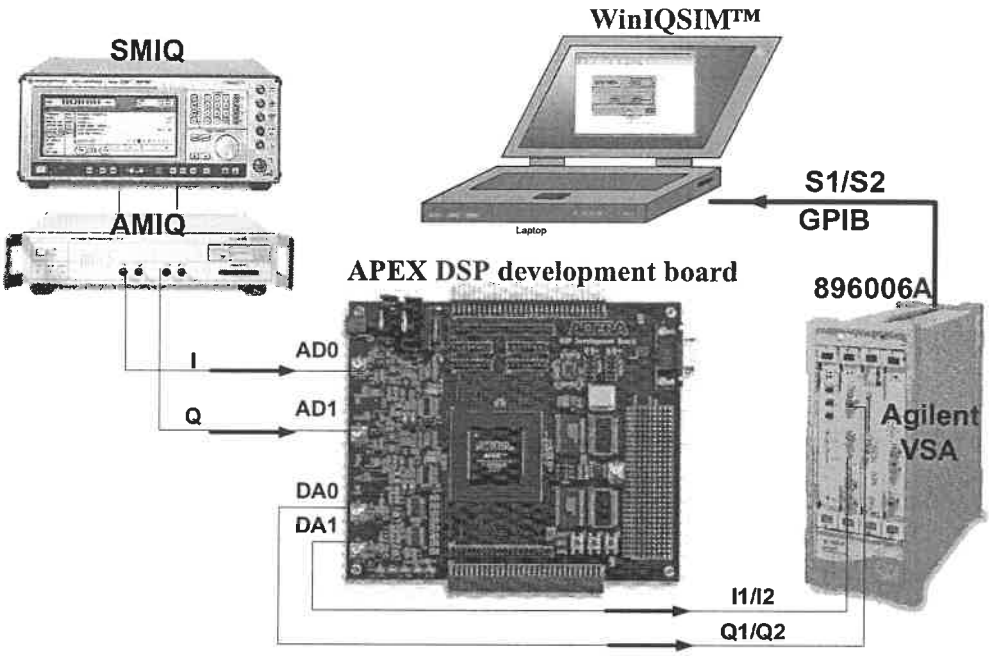
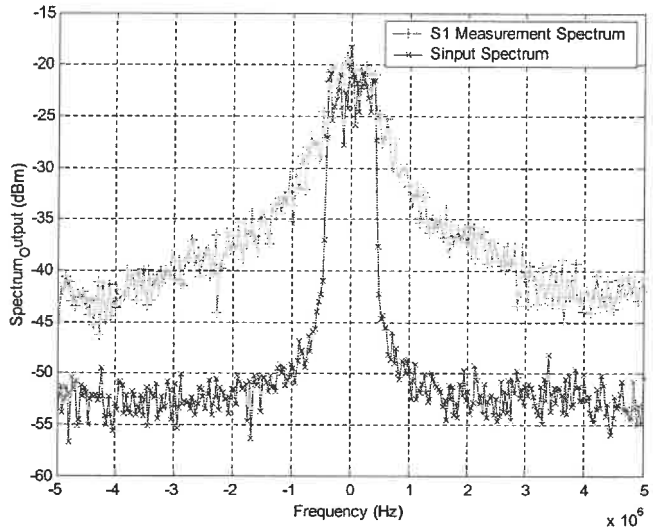


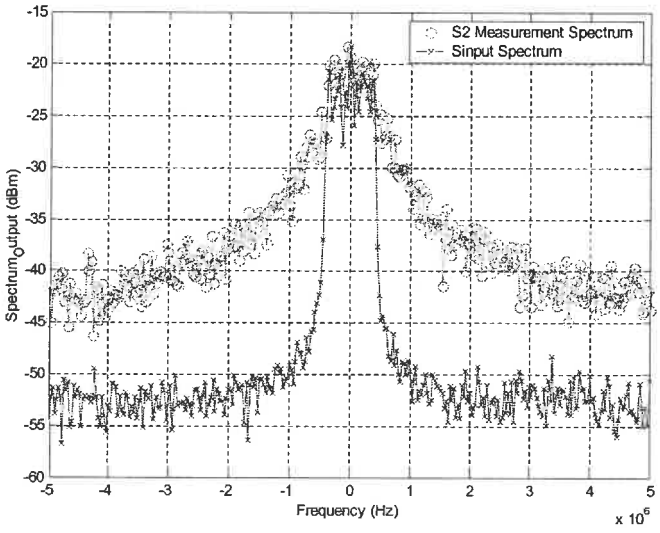
Figure 2. 21 Measurement set-up

2.6.2 Measurement results for S_1 and S_2

The compilation file *. sof generated in the Quartus II is downloaded into the P20K1500E-1X device by the ByteBlasterMV cable via its RS-232 serial port. The Agilent 89600 series vector signal analyzer (VSA) and PC are linked with via a GPIB card to complete the measurement set-up. Two equal amplitude but phase modulated signals $S_1(t)$ / $S_2(t)$ are obtained separately from this setup and are shown in figure 2.22.



(a) S_1 and S_input from measurement



(b) $S_2(t)$ and S_input from measurement

Figure 2. 22 Output and input spectrum from measurement

2.6.3 Two methods comparison from measurement

The comparison of results in figure 2.23 concludes that the method of square-root functional block, SRFB, had achieved the high processing speed (see table 2.1), but with a lower accuracy than the LUT approach, due to its limited word-length .

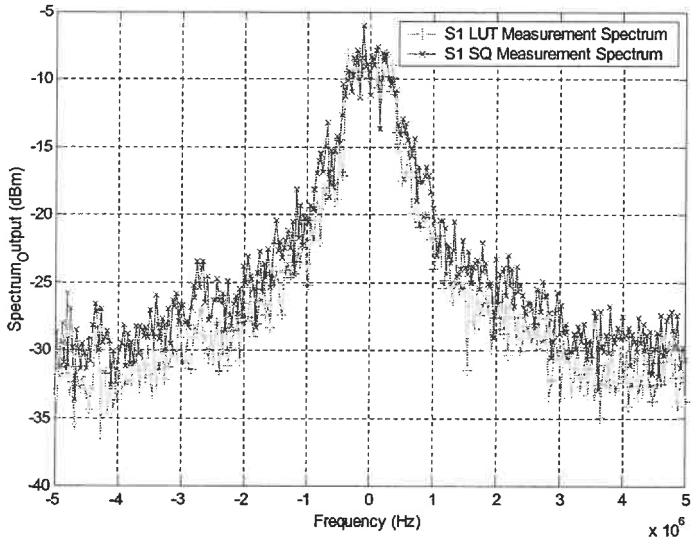


Figure 2. 23 S_1 spectrum between LUT and SRFB from measurement

Consequently, the same result is obtained from measurement: LUT method is more accurate than SRFB method, and LUT spectrum has a better result than the SRFB spectrum due to its lower spurious spectrum.

2.7 Comparison between simulation and measurement

The designs in the Quartus II have been evaluated by Simulink simulations and validated by the experimental measurement. The comparison result between simulation and measurement is shown in below.

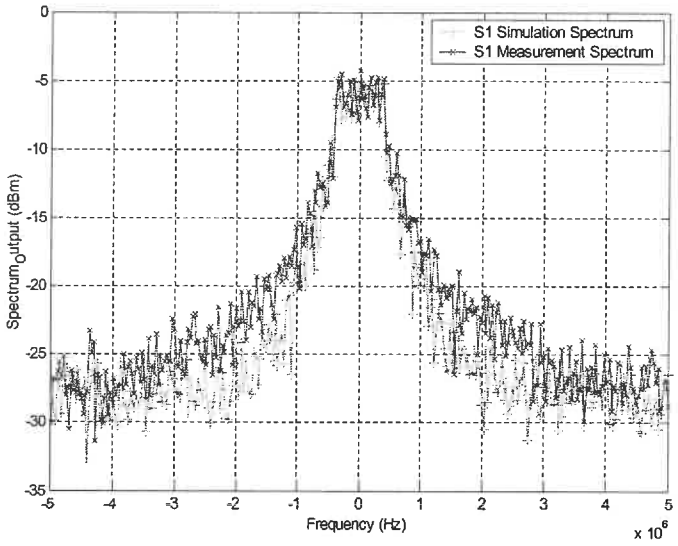


Figure 2. 24 Spectrum comparison between simulation and measurement

In figure 2.24, two curves represent the output signal $S_1(t)$ from simulation and the output signal $S_1(t)$ from measurement. It shows that the simulation has more accuracy than the measurement because the simulation in Simulink can generate perfect data without a loss in the data processing. But the errors generated in the practical implementation and measurement are degraded by overall accuracy.

2.8 Conclusions

In conclusion, the DSP implementation of a digital signal component separator (DSCS) based on an FPGA device is a challenging but effective solution.

Both methods, one-dimensional look-up-table (LUT) and a square-root function block (SRFB), can implement DSCS on an FPGA. They can minimize the word length while still providing acceptable accuracy which reduces the power consumption and

increases the bandwidth.

The LUT method has more accuracy than the SRFB method due to its larger size bus architecture, but its processing time is longer. In contrast, the SRFB method achieves a higher overall throughput performance due to its pipelining techniques; but its output result is not as good as the LUT method due to its lower bus width.

From the compilation report in Quartus II, the overall actual maximum output frequency (f_{max}) represents the system processing speed.

LUT method achieves an actual 59 MHz overall frequency. The maximum output frequency goal is set at 100 MHz. The SRFB method accomplishes more than a 65 MHz frequency with the same frequency goal. The overall speed of this, the high-consumption SRFB, had improved by more than 40 MHz. This takes into account that the general square root block available in the Quartus II 2.0 library only achieves a 18 MHz f_{max}.

All the comparison results, including the Altera square root megafunction ALTSQRT, are shown in table 2.1.

Table2. 1 Processing speed and accuracy comparison from the Quartus II 4.2

	Overall Actual Frequency f_{max} (MHz)	Single Block Actual time tpd (ns)	Data-error (%)
16384 LUT (26-bit)	59.53	15.84	0.0536
Coded SRFB with pipelining (12-bit)	69.78	13.28	0.115
ALTSQRT with pipelining q=7-bit, remainder=8-bit	72.36	12.95	0.204
Square-root without pipelining in Quartus II 2.0 library	18.69	50.25	N/A

With this DSP scheme, all of the signal processing has been achieved at baseband, and then converted into analog waveforms by digital-to-analog converters (DAC). Finally, the processed analog signals are translated to the desired RF frequency by up-converters.

All the designs have been simulated in Simulink of Matlab for validation. Moreover, the experimental measurements are performed to demonstrate that these two solutions can be implemented in an FPGA and become the new digital signal component separator (NDSCS) for today's LINC transmitter.

CHAPTER 3

COMBINER TECHNIQUES IN LINC TRANSMITTERS

Power efficiency of a mobile transmitter is crucial in wireless communications because the mobile end is usually battery powered. The output stage of a transmitter is also the largest consumer of power; hence improvement at this stage is very important for overall efficiency. Combiner technology is the biggest contributor to an efficient LINC transmitter. Implementing efficiency in the output signal combiner is necessary to achieve an overall high power-added efficiency (PAE) in the LINC RF transmitter [32] because RF power is not wasted.

There are two main problems in building a vectorial signal combiner [33]. The first problem, has to do with the power dissipation in the combiner itself. If the combiner can be built to consist of mainly reactive components the power disipation will be minimized. The second is in making the combiner present the proper load to the two constant envelope signals for all levels of the modulated output. If this load represents an impedance that has no imaginary part, it will maximize the overall power efficiency by having the voltage and current in phase at the load. Therefore the impedance at the input of the combiner should be a function of the modulated phase between the constant amplitude amplifier outputs to maintain this phase relationship between the voltage and current.

Unfortunately, the linearity of the LINC system will be degraded when achieving its maximum power efficiency [34]. Hence, the compromise between efficiency and

linearity in the LINC transmitter is studied and becomes an optimization goal. There is no previous work in constructing a LINC combiner that satisfies these two requirements. The closest combiner to this is the Chireix outphasing combiner [19] which has two reactive elements and contains a large impedance transformer. However, the reactive terminations bring the phase error into the signal combiner so as to degrade the linearity significantly as the average efficiency is increased. The goal is to optimize efficiency, without scarifying too much linearity. In this chapter, the effect of optimising efficiency of two combiner types are analyzed and presented. Then, a new structure of combiner having variable reactive elements and a "balun" (anonym of balance to unbalance transformer) chip, is implemented to achieve the efficiency optimization. It presents the balance between linearity and efficiency for different classical combiner models and demonstrates the results using ADS simulations.

3.1 Efficiency definitions

Efficiency, like linearity, is a critical factor in PA design. Three definitions of efficiency are commonly used. Drain efficiency is defined as the ratio of RF output power to DC power dissipation [35] [36][37]:

$$\eta_{drain} = \frac{P_{out}}{P_{dc}} \tag{3.1}$$

The 3G wireless standards such as wideband CDMA and WCDMA demand more strict requirements on the power amplifier's linearity performance. Hence, linear power amplifiers require a substantially higher quiescent current than that used for constant

envelope applications. This characteristic, coupled with the requirement that linear power amplifiers cannot be driven into deep saturation, is the reason why linear power amplifiers show lower efficiency than those for constant envelope applications. One related problem is that the DC-to-RF amplifier efficiency generally drops sharply as the RF input drive power is ''backed-off'' from the maximum rated power level. The power-added efficiency (PAE) of a typical amplifier is a measure of the conversion efficiency of all sources of input power (both from the power supply and the input signal) to the output [32], and is given by

$$PAE = \frac{P_{RF_{out}} - P_{RF_{in}}}{P_{dc}} \times 100\% \tag{3.2}$$

where P_{RFout} is the desired output power of the amplifier in the band, P_{RFin} is the RF input power and P_{dc} is the average DC input power supplied to the circuit. If the gain of the circuit is relatively high, then the RF input power is much smaller than the dc power, and the PAE is a measure of the conversion efficiency from the battery to the transmitted signal.

A useful measure of performance is then the average efficiency, which is the ratio of the average output power to the average DC-input power:

$$\eta_{AVG} = \frac{P_{out\_AVG}}{P_{dc\_AVG}} \tag{3.3}$$

In a LINC transmitter, the average efficiency is dependant on the modulation scheme used and is expressed by the following if the combiner is lossless [36].

$$\eta_{LINC} = \eta_a \eta_m = \eta_a \frac{\bar{r}^2}{r_{\max}^2} = \eta_a \frac{\int_0^{r_{\max}} P_m(r) r^2 dr}{r_{\max}^2} \tag{3.4}$$

where

η_a is the efficiency of the amplifiers

η_m is the efficiency of the modulation scheme

$P_m(r)$ is the probability density function of the modulation scheme

r is the normalized amplitude of the input signal

r_{max} is the maximum amplitude of the input signal

The overall the efficiency of LINC transmitter taking the combiner efficiency into account [37]:

$$\eta_{total\_LINC} = \eta_a \eta_m \eta_c = \eta_a \eta_c \frac{\bar{r}^2}{r_{\max}^2} = \eta_a \eta_c \frac{\int_0^{r_{\max}} P_m(r) r^2 dr}{r_{\max}^2} \tag{3.5}$$

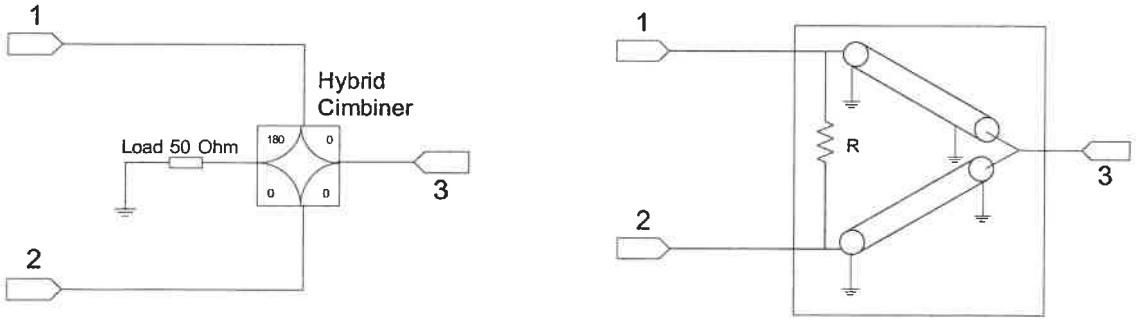
where all are the same as in (3.4), except ηc is the efficiency of the combiner that represents the loss in the combiner itself. The numerical average to peak power ratio of the modulation method is used for calculating its efficiency. This value is then multiplied by the efficiency of the nonlinear RF power amplifiers in each branch to determine the composite LINC efficiency. The degradation of the total efficiency is dependant on the magnitude of the modulated signal.

3.2 Different combiner structures

Combiner technologies have many architectures such as impedance transformers, hybrid couplers, Wilkinson combiners, baluns, transmission line combiners and Lange couplers [35]. All of these constructions fall into two main categories: power combiners with isolated input ports that are lossy, and lossless combiners with input ports that are not isolated from each other.

3.2.1 Category 1 ---- The isolated combiner

A passive matched hybrid coupler with four ports is an isolating device, where the power is split equally from one port to another pair of output ports, the remaining input port being isolated. It provides high isolation between input ports to obtain an undistorted signal combination [15][35][36][37]. It isolates the two power amplifiers from each other, even allowing one to continue operating after the other one has failed. See figure 3.1.



(a) Hybrid combiner **(b) Wilkinson combiner**

Figure 3. 1 Model 1: isolated combiner

Another isolated combiner is a three port Wilkinson combiner [38]. It is actually a type of hybrid with a built-in termination that uses quarter-wavelength transmission lines. Its phase and amplitude balance depend primarily upon circuit symmetry and thus it is broadband.

A practical hybrid has a limited bandwidth. There are effects on isolation, phase/amplitude balance and loss. For this model combiner which has high isolation between input ports, the distortion in the output signal are caused by phase and /or gain imbalances between the two RF paths and signals. As the summation ports are terminated in matched loads, a constant impedance of 50 Ω is offered to the output of the high efficiency amplifiers. This assures that the amplifier's operating conditions remain constant even though the constant envelope signals have large phase variances. Power is lost in the process of recombining the constant envelope signals. Because this isolated combiner prevents the variable load impedances being presented back to the power amplifiers due to its fixed 50 Ω load, and the power of the quadrature signals turn into a 'consume' state. As a result, the amplifier only achieves its peak operating efficiency at maximum output power, and its efficiency decreases linearly as the output power decreases. This is disadvantageous in modulation schemes, such as CDMA, that have high peak to average power ratios.

This efficiency behaviour is similar to that of a Class A amplifier which has a very poor overall efficiency, but attain their best efficiency at high output powers. Therefore,

the isolated model combiner can preserve the linearity of LINC transmitter, but at a significantly reduced efficiency.

3.2.2 Category 2 ---- The unisolated combiner

Alternatively, unisolated combiners, like the Wilkinson without the isolation resistor between two balance ports in figure 3.4 [36], contain no internal power consuming terminations.

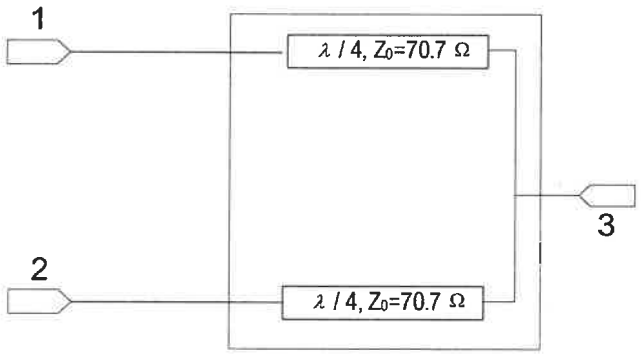
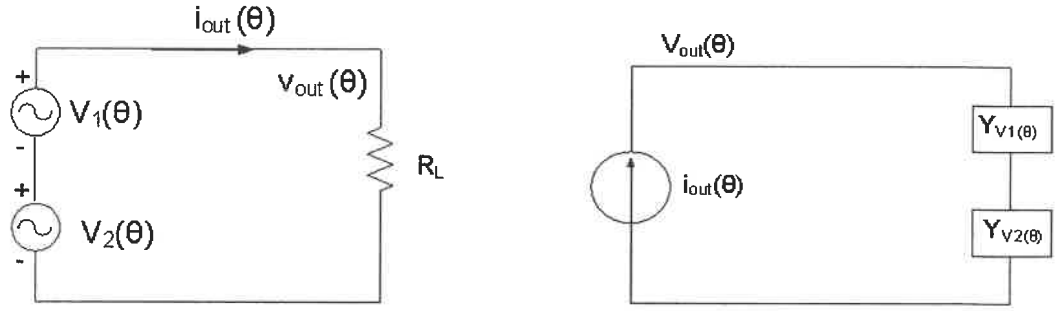


Figure 3. 2 Model 2: unisolated combiner

Therefore, the unisolated combiner is first considered as the model in the LINC transmitter for achieving this high efficiency performance. Two simplified voltage sources added in series , see figure 3.3, provide us with a short cut for analyzing and optimizing the efficiency of LINC transmitter. This exercise is independent of the class of amplifier used because we are mainly interested in the effectiveness of the combiner in combining the signals coming from the amplifiers. The reactive termination is simplified as a reactive source for optimization purposes.

3.2.2.1 Simplified voltage /current source model in unisolated combiner

The LINC power amplifier efficiency can be analyzed and optimized by analyzing the impedance or admittance of the input and output ports of the LINC combiner. The average efficiency using various amplitudes is determined as a function of input port admittance for different types of combiners. It is important to study the impedance/admittance in the LINC signal combination process.



(a) Realized as voltage sources **(b) Current source**

Figure 3. 3 LINC combiner realized voltage / current sources

It is known that two phase-modulated constant phasor signals in LINC system are defined as [32]:

$$V_1(\theta) = k * e^{j\theta} = \frac{r_{\max}}{2}(\cos\theta + j\sin\theta) \tag{3.6}$$

$$V_2(\theta) = k * e^{-j\theta} = \frac{r_{\max}}{2}(\cos\theta - j\sin\theta) \tag{3.7}$$

$$V_{out}(\theta) = V_1(\theta) + V_2(\theta) = k * (e^{j\theta} + e^{-j\theta}) = r_{\max}\cos\theta \tag{3.8}$$

$$i_{out}(\theta) = \frac{V_1(\theta) + V_2(\theta)}{R_L} = \frac{k * (e^{j\theta} + e^{-j\theta})}{R_L} = \frac{r_{\max}\cos\theta}{R_L} \tag{3.9}$$

$V_1(\theta)$ provides a constant voltage signal modulated by θ and $V_2(\theta)$ provides a constant voltage signal modulated by $-\theta$, where θ is varied between 0 to 90°. The output is summed as $V_{out}(\theta)$ which is applied to the output load R_L which generates the current $i_{out}(\theta)$. See figure 3.3. Voltage and current models in series are formed by two phase-modulated constant voltage sources.

Where the load is defined as the admittance $Y_{V_1(\theta)}$ and $Y_{V_2(\theta)}$ [32]

$$Y_{V_1(\theta)} = \frac{i_{out}(\theta)}{V_1(\theta)} = \frac{2\cos\theta}{R_L e^{j\theta}} \tag{3.10}$$

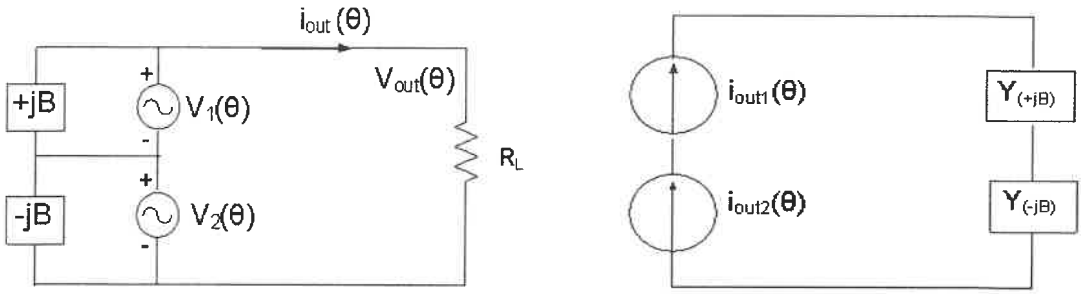
$$Y_{V_2(\theta)} = \frac{i_{out}(\theta)}{V_2(\theta)} = \frac{2\cos\theta}{R_L e^{-j\theta}} \tag{3.11}$$

The identical approach for optimization of efficiency is performed using two shunt susceptances, which are simplified by making the reactive sources voltage / current models. All analysis and equations are then taken into account. This leads to relational expressions between the impedance and the modulated phase offset. Also included are the parameters of output voltage / current, time varying admittance B expressions and the efficiency calculation.

3.2.2.2 Simplified Reactive Sources Model

When the power is not dissipated in the load R_L there is no reactive loading in the termination, therefore the equal real values impedance lead to achieve maximum efficiency. Two additional shunt susceptances, which are conjugate to each other, can be

applied in parallel and across the two voltage sources resulting in reducing the susceptance in the simplified voltage / current model.



(a) Series voltage sources **(b) Current source**

Figure 3. 4 Voltage and current models with shunt susceptances

The model with shunt conjugate elements is shown in figure3.4 (a) where two parallel susceptances +jB and –jB are added to the voltages sources and the modeled current sources is in (b). These shunt conjugate components can be optimized at a particular output power level other than the peak output power for the efficiency [32].

The admittance of load are redefined as:

$$Y_{(+jB)} = \frac{2\cos^2\theta - j\sin 2\theta}{R_L} + jB \tag{3.12}$$

$$Y_{(-jB)} = \frac{2\cos^2\theta + j\sin 2\theta}{R_L} - jB \tag{3.13}$$

A key value B in (3.12) and (3.13) can be obtained by setting the imaginary part equal to zero. This leads to the following relationship:

$$B = \frac{\sin 2\theta}{R_L} \tag{3.14}$$

This expression allows us to get the modulated phase θ where maximum efficiency occurs in the combiner for a given load and shunt reactive element. At the same time, evaluating the LINC efficiency for different shunt reactance, B, is important to construct a good combiner.

3.3 Different models analysis of unisolated combiner

3.3.1 Lossless tee combiner

A lossless tee combiner, which belongs to the unisolated combiner category, produces significant interactions between input port 1 and 2. This leads to distortion and a reduction in efficiency in a practical circuit. The analysis is shown in figure 3.5. With two input ports coupled, the constant envelope signal entering port 1 will be split into two components: one passes through the combiner to the output and the other goes to the input port 2. This component in port 2 will interact with the output of amplifier PA2, and reflected back to the combiner. The reflected signal will be split again between the original input and the combiner's output. When constant envelope signals are transmitted through both branches, a large standing wave will be obtained at the two input ports.

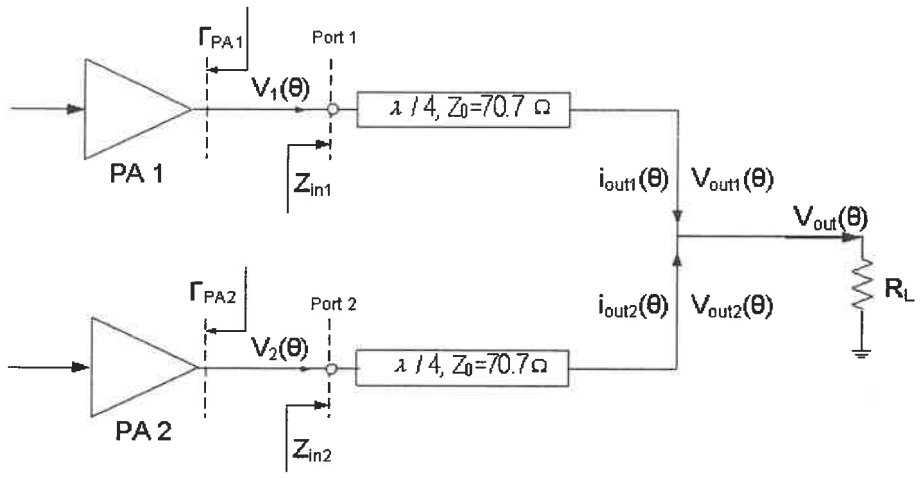


Figure 3. 5 Lossless combiner analysis

To simply the analysis, we assume that there is no phase or gain imbalance between the two paths, and that the time delay is small. Then the signals at the junction to the load are [36]:

$$V_{out1}(\theta) = V_1(\theta) + \frac{V_1(\theta)s_{21}s_{12}\Gamma_{PA2}(1+\Gamma_{PA1})}{1-s_{21}s_{12}\Gamma_{PA1}\Gamma_{PA2}} + \frac{V_2(\theta)s_{12}(1+\Gamma_{PA1})}{1-s_{21}s_{12}\Gamma_{PA1}\Gamma_{PA2}} \tag{3.15}$$

$$V_{out2}(\theta) = V_2(\theta) + \frac{V_2(\theta)s_{21}s_{12}\Gamma_{PA1}(1+\Gamma_{PA2})}{1-s_{21}s_{12}\Gamma_{PA1}\Gamma_{PA2}} + \frac{V_1(\theta)s_{21}(1+\Gamma_{PA2})}{1-s_{21}s_{12}\Gamma_{PA1}\Gamma_{PA2}} \tag{3.16}$$

where s21 and s12 are the S-parameters between the port1 and port 2. The load voltage is $V_{out} = V_{out1}(\theta) + V_{out2}(\theta)$. Γ_{PA1} is the output reflection coefficient of upper branch from power amplifier PA1 and Γ_{PA2} is the output reflection coefficient of the lower branch from power amplifier PA2 [39].

For the matching condition of $\Gamma_{PA1} = \Gamma_{PA2} = 0$ then,

$$V_{out1}(\theta) = V_1(\theta) + V_2(\theta)s_{12} \tag{3.17}$$

$$V_{out2}(\theta) = V_2(\theta) + V_1(\theta)s_{21} \tag{3.18}$$

When reflection coefficient $\Gamma_{PA1} = \Gamma_{PA2} = -1$, the output impedance of the amplifiers will be a short, we obtain

$$V_{out1}(\theta) = V_1(\theta) \tag{3.19}$$

$$V_{out2}(\theta) = V_2(\theta) \tag{3.20}$$

Therefore, the LINC transmitter with a tee combiner is equal, or more efficient, than an isolated combiner such as a Wilkinson.

3.3.2 The Chireix outphasing combiner

Reactive terminations made with shunt susceptances form a Chireix combiner and is a very useful unisolated combiner which can improve the power efficiency [19]. The average efficiency for various power levels is determined as a function of shunt reactance. Selecting the right value of shunt reactance to fit the signal level will maximum the efficiency at that one output power level.

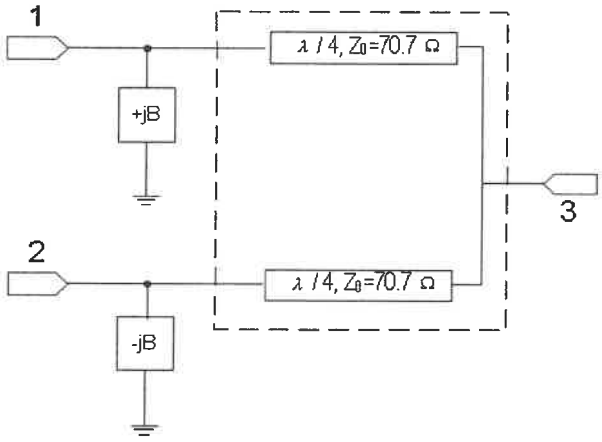


Figure 3. 6 Chireix outphasing system with shunt susceptances

Based on the lossless tee combiner, the Chireix combiner structure consists of λ/4 transmission lines in each branch which operates as a impedance transformer to translate the impedance from the balanced port to the unbalanced port. The two reactive elements are added symmetrically in the two input branches of the lossless tee combiner.

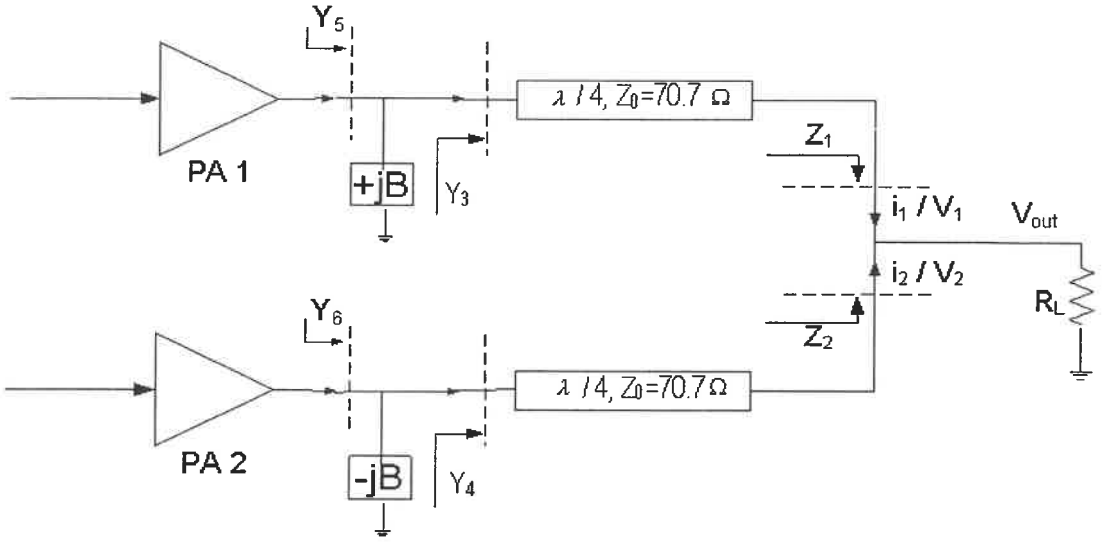


Figure 3. 7 Chireix outphasing system analysis

In figure 3.7, the impedance Z_1 and Z_2 are

$$Z_1 = \frac{V_{out}}{i_1} = 2R_L \cos\theta(\cos\theta - j\sin\theta) \tag{3.21}$$

$$Z_2 = \frac{V_{out}}{i_2} = 2R_L \cos\theta(\cos\theta + j\sin\theta) \tag{3.22}$$

The corresponding admittance Y_3 and Y_4 can be obtained by $Z_1 Z_3 = Z_0^{\,2}$ and $Z_2 Z_4 = Z_0^2$.

$$Y_3 = \frac{1}{Z_3} = \frac{2R_L \cos\theta(\cos\theta - j\sin\theta)}{Z_0^2} \tag{3.23}$$

$$Y_4 = \frac{1}{Z_4} = \frac{2R_L \cos\theta(\cos\theta + j\sin\theta)}{Z_0^2} \tag{3.24}$$

The admittance Y_5 and Y_6 at the output of the amplifiers can be aquired after adding the shunt susceptances +B and –B.

$$Y_5 = \frac{2R_L \cos^2\theta}{Z_0^2} - j(\frac{R_L^2}{Z_0^2} * \frac{\sin 2\theta}{R_L}) + jB \tag{3.25}$$

$$Y_6 = \frac{2R_L \cos^2\theta}{Z_0^2} + j(\frac{R_L^2}{Z_0^2} * \frac{\sin 2\theta}{R_L}) - jB \tag{3.26}$$

The shunt susceptances B and -B equal:

$$B = K * \frac{\sin 2\theta}{R_L} \tag{3.27}$$

The choice of B produces a phase shift in the current i1 or i2 so that i1 or i2 can be in phase with V_1 or V_2. The selection of a particular value of B will increase the efficiency at one output voltage but it will decrease the efficiency at all other values. It is necessary to calculate the average efficiency of the Chireix-outphasing combiner and amplifier.

The efficiency of LINC transmitter with Chireix-outphasing combiner can be maximized at a specific output amplitude by selecting the shunt susceptance properly. However, in the circuit, B has a fixed value, independent of the output power level, so optimal efficiency can occur at only one particular choice of B. It shows that ideal efficiency is not obtainable over the full range of output power, it is optimized at only one particular power level. In addition, the best selection of power level to optimize the

combiner depends on the characteristics of the signals to be amplified and particularly the probability distribution of the output power over time.

3.3.3 Variable reactive termination combiner (VRTC)

The variable reactive termination combiner consists of an impedance transformer and a variable shunt susceptance elements in each branch. Compared to a Chireix outphasing combiner, this model has two variable shunt susceptance elements, +Bv and – Bv, for optimizing efficiency instead of two fixed elements.

Dynamically selecting the correct value of shunt susceptance to fit the signal can improve the efficiency at any instantaneous amplitude output, it is therefore possible to obtain the maximum efficiency at all output levels. The admittance of the shunt suseptance elements vary with the modulated phase θ so that the voltage stays in-phase with the current. The variable reactive termination combiner becomes the best choice for LINC combination to satisfy the optimization requirements.

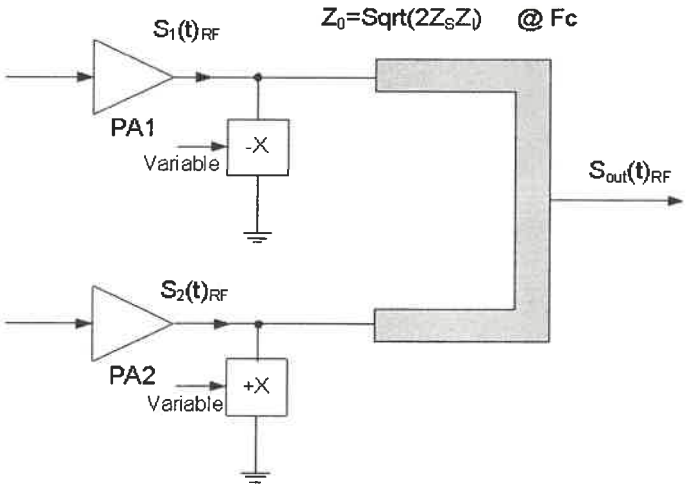


Figure 3. 8 Variable reactive termination combiner

3.3.3.1 VRTC implementation

The practical combiner is constructed with two purely reactive elements, so that it does not dissipate energy, and an impedance transformer. The two reactive elements are implemented with the parallel combination of a variable capacitor and a fixed inductor. The shunt admittance is varied with modulated phase θ by changing the value of the capacitor or inductor. A small, low cost, but high performance balun chip is used to transfer the impedance [33].

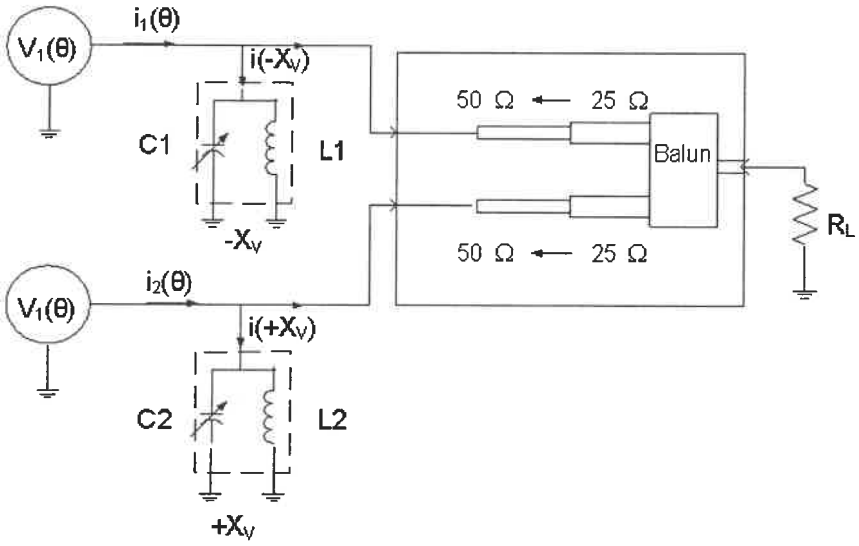


Figure 3. 9 Implementation of variable reactive termination combiner

The reactive elements in the LC shunt circuit have the capacitance +Xv and inductance –Xv in two branches respectively, as shown in diagram 3.9 which adjust the current when the signals are combined at the desired load R_L.

3.3.3.2 Reactance Xv analysis in VRTC

In the following discussion, we suppose that the instantaneous phase variation $\Phi(t)$ is neglected because it represents only a small fraction of the carrier frequency, and because it is applied to both $V_1(\theta)$ and $V_2(\theta)$ equally [33].

If reactance ± Xv is chosen properly, current $i_{(-Xv)}$ and $i_{(+Xv)}$ will add to the output current so that the total current i_1 and i_2 will be in phase with $V_1(\theta)$ and $V_2(\theta)$ respectively, see figure 3.9. Otherwise $i_{(-Xv)}$ and $i_{(+Xv)}$ will be out of phase with $V_1(\theta)$ and $V_2(\theta)$ respectively and will therefore cancel and this lowers the efficiency.

The reactance in this model is, therefore, calculated from the shunt susceptance Bv, called X_1 and X_2 .

$$jX_1 = \frac{1}{+jB_v} = -jX_V \tag{3.29}$$

$$jX_2 = \frac{1}{-jB_v} = +jX_V \tag{3.30}$$

Consequently, the explicit expression of X_V is a function of the modulated phase θ.

$$X_V(\theta) = \frac{k * R_L}{\sin(2\theta)} \tag{3.31}$$

When $X_V(\theta)$ is a negative value, $-X_V$ denotes a capacitive element. It will be infinite when θ is equal to zero or 90°. In the other case, it becomes a capacitive reactance ($-k*R_L$).

When $X_V(\theta)$ becomes a positive value, $+X_V$ is an inductive reactance ($+k*R_L$) and it becomes infinite as θ is equal to 0° or 90° .

3.3.3.3 Variable capacitors in VRTC

The reactive circuits can be tuned to have reactance values ranging from infinite to k*RL, inductive or capacitive. We assume that L_1 and L_2 have the same inductances. The capacitors C_1 and C_2 are be adjusted according to the signal's phase offset. The circuits are tuned to resonate at the carrier frequency which it leads to an infinite reactance. When the capacitor is increased above the resonance value, the circuit becomes a capacitive and when the capacitor is decreased below the resonant value the circuit becomes inductive.

In this combiner, the proper choice of the value of C_1 and C_2 depend on the following expressions used to trade-off efficiency and linearity [33].

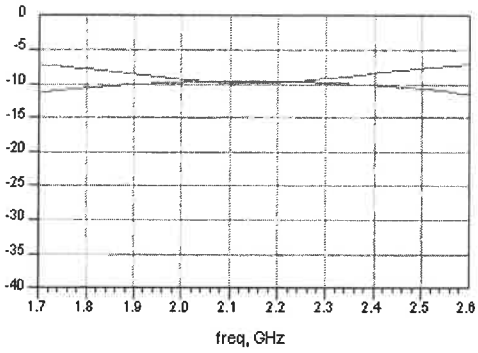
$$C_1 = \alpha * \left[1 + \frac{\omega L}{X_1}\right] = \alpha * \left[1 - \frac{\sin[2\theta]}{\beta}\right] \tag{3.32}$$

$$C_2 = \alpha * \left[1 + \frac{\omega L}{X_2}\right] = \alpha * \left[1 + \frac{\sin[2\theta]}{\beta}\right] \tag{3.33}$$

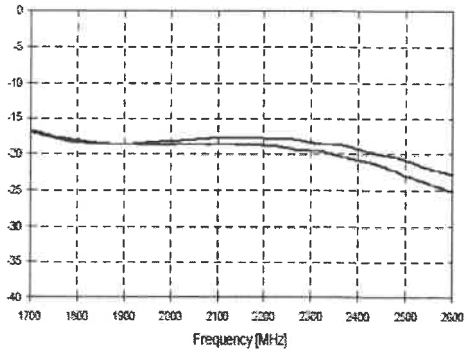
Where α is the value of C_1 and C_2 which resonates with L at the carrier frequency ω, and $\beta = K*(R_L/\omega L)$. This combiner is described in terms of adjusting the capacitors, but the inductors L_1 and L_2 may also be adjusted.

3.3.3.4 Implementation of impedance transformer in VRTC

Anaren's 3W525 (frequency 1.8-2.5 GHz) is implemented into the design to work as an unisolated combiner. It is a low profile balanced to unbalanced balun transformer in a surface mount package which has an unbalanced port impedance of 50Ω and balanced port impedances of 25Ω. The minimum 15 dB return loss and maximum 0.30 dB insertion loss are shown below.

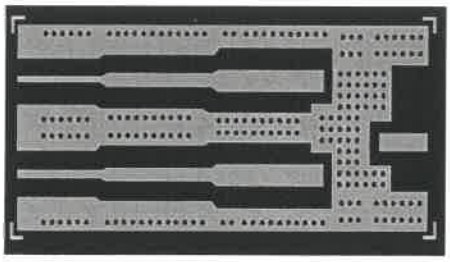


(a) Tee combiner return loss

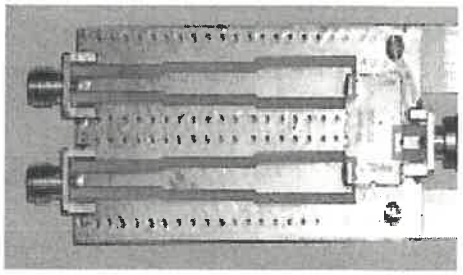


(b) 3W525 return loss

Figure 3. 10 Combiner return loss



(a) Layout diagram



(b) Circuit board

Figure 3. 11 Enhanced unisolated combiner design in ADS

The following prototype is constructed with Anaren's 3W525 chip. The balanced ports are designed to transfer the impedance from 25Ω to 50Ω.

3.3.3.5 Advantage of variable reactive termination combiner

This new model of combiner, with variable reactive elements, presents a load that has no imaginary part for all values of θ. It is possible to achieve very high efficiency for amplitude modulation of the signal.

The improved VRTC uses only reactive elements and a small size impedance transformer. Two variable reactive elements (±Xv) cancel the imaginary parts in output impedances so that the two constant envelope amplifiers have no imaginary part for all levels of the modulated output. Hence, VRTC places the voltage in phase with the current at the load. The efficiency is increased obviously.

On the contrast, if two variable reactive elements (±Xv) are removed from VRTC, the two constant envelope amplifiers will have the imaginary part in the load. It results that the power of quadrature components turn into consumption state. The power will be lost in these imaginary portions. As a result, the efficiency can not be maximum at all output power level because no reactance is used to fit the signal level.

3.4 Simulations in ADS

The validation of the results are obtained using simulations in Agilent's Advanced Design System (ADS) software. The overall LINC transmitter system was simulated. The efficiency of the LINC transmitter using different models of combiners was obtained by a two-tone input signal and an IS95 CDMA input signal having a bandwidth of 1.2288 MHz.

3.4.1 Efficiency results using two-tone signal

Motorola's RF power field effect transistor MRF 21045, a class AB power amplifier which has 23.5% efficiency at 10 watts average output power and 15 dB gain is used to act as the RF power amplifier in each branch.

The power-add-efficiency (PAE) of the LINC transmitter can be obtained by the simulation with classical combiners and our variable reactive termination combiner respectively. Two-tone signal is used as input signal, and MRF 21045 is operated as power amplifier in each branch. The PAE is then calculated from simulation in ADS.

Three simulation curves in figure 3.12 show PAE comparison results. The first curve is the efficiency of LINC system using the new variable reactive termination combiner and achieves the maximum efficiency. The second curve shows the efficiency of LINC system with the same model of combiner but making some trade off of efficiency for linearity. The variations of efficiency are realized by adjusting the reactive elements in the new LINC combiner The third curve represents PAE of the LINC system using a classical tee combiner without reactive elements.

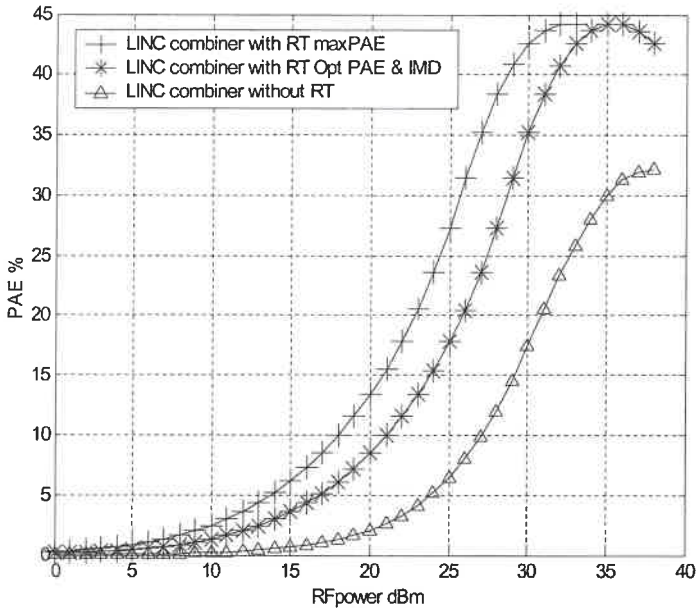


Figure 3. 12 PAE η (%) vs Pin (dBm) with two-tone signal

The instantaneous efficiency are 42.6%, 35.2% and 17.5% respectively with 30 dBm of input power.

3.4.2 Efficiency results using CDMA IS95 input signal

The CDMA IS95 source signal in ADS can generate a digitally-modulated signals that have base station like modulation characteristics. It does not contain any framing characteristics. It is recommended that the simulation time step is equal to 0.25/1.2288 MHz with four samples per bit. Shown are four simulation curves obtained with an IS-95 input signal.

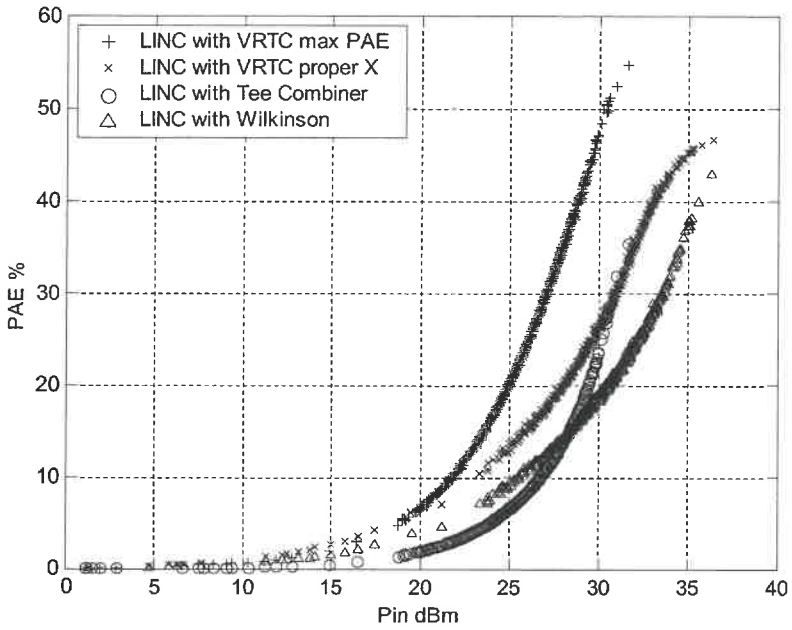


Figure 3. 13 PAE curves with IS95 signal

Comparing with different LINC combiners, a Wilkinson combiner, a lossless tee combiner, and our variable reactive termination combiner (VRTC), it demonstrates that a lossless combiner has similar or better efficiency performance than a Wilkinson combiner. A careful choice of shunt reactance in the variable reactive termination combiner makes the best compromise between the efficiency and the linearity.

3.4.2.1 Average combiner efficiency using IS95 input signal

Different combiners produce different average efficiency when they operate in the same LINC system separately. Table 3.1 shows average combiner efficiency achieved in ADS with IS95 reverse signal of 5 dB peak-to-average ratio.

Table 3. 1 Average combiner efficiency

	Wilkinson Combiner	Tee Combiner	Chireix Outphasing Combiner	VRTC
Combiner Efficiency η (%)	48.77	54.96	72.83	94.37

The overall average efficiency for LINC system with various amplitude-modulated signals are determined as a functions of shunt reactance. It is obtained by the peak efficiency of the saturated power amplifier ηa multiplied by the efficiency of the modulation scheme ηm , then multiplied by the average combiner efficiency ηc. In a LINC amplification system, ηa and ηm keep the same value as using different combiners. Hence, different average combiner efficiency result overall average efficiencies having variable values.

Four simulation results of overall average efficiency of LINC of system are:

- Maximum average efficiency is achieved at 17.6% with VRTC
- Average efficiency is 13.6% with Chireix outphasing combiner
- Average efficiency is 10.2 % with tee combiner
- Average efficiency is 9.1 % with Wilkinson combiner

As a result, the overall efficiency of LINC system with an unisolated combiner is higher than with an isolated combiner.

3.4.3 Linearity results using IS95 input signals

Achieving the maximum efficiency brings about non-linearity because the shunt susceptance increases the amount of phase imbalance, especially for the modulation schemes having high peak-to-average ratios, such as CDMA.

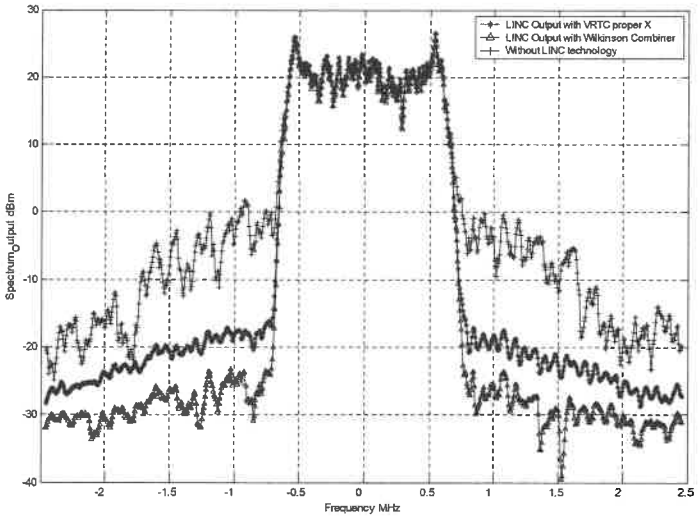
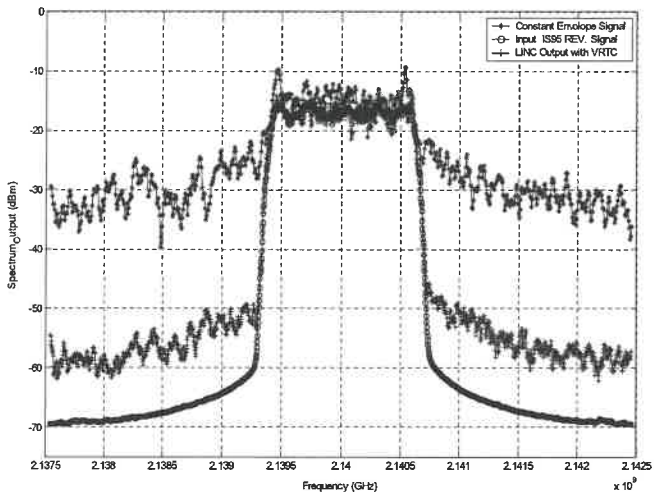


Figure 3. 14 LINC output spectrum using an IS95 REV signal

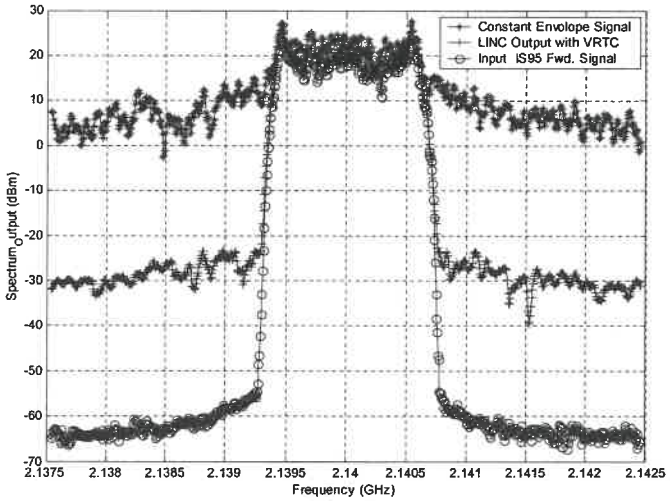
The output spectrum in figure 3.14 indicates that the linearity is improved by LINC technology. Moreover, isolated combiners, such as Wilkinson combiners, achieve better linearity than unisolated combiners such as the variable reactive termination combiner, but variable this combiner brings about high efficiency performance with not so much of a loss in linearity when careful value of shunt reactances are chosen to meet requirements.

Two types of IS95 CDMA input signals, are used for the input source in the simulation: a reverse link signal with a 5 dB peak-to-average ratio and a forward link

signal with a 9 dB peak-to-average ratio. The first spectrum on the 3.15 (a) is constant envelope phase modulated signal, S_1/S_2. The second one is a LINC output spectrum and the third one is the IS95 input signal.



(a) IS95-Reverse link CDMA signal



(b) IS95-Forward link CDMA signal

Figure 3. 15 Spectrums using IS95 signal

In figure 3.15 (b) using IS95 forward link signal, the acceptable LINC output spectrums are obtained by properly choosing the shunt reactance value in the variable reactive termination combiner. The linearity on ACPR at 885 KHz offset is achieved at minimum –56.9 dBc. See table 3.2.

3.4.4 Linearity and efficiency using IS-95 input signal

The LINC transmitter is simulated using an IS-95 forward link signal with 1.2288 MHz bandwidth, and an ACPR of –89.4 dBc at 885 KHz offset. The peak-to-average ratio is 9.34 dB.

The results show that the maximum average efficiency of this practical LINC transmitter is 17.6% with class AB power amplifiers having 23.5% efficiency at the center frequency of 2.14 GHz. Properly selecting the shunt reactance ±Xv can appropriately trade off efficiency and linearity. When a 'compromise' solution is taken, the shunt reactance value of 15.5% for efficiency and –57 dBc for ACPR (885 KHz offset, 8.3 dB peak-to-average ratio at output) is obtained.

All the results are shown in table 3.2.

Table 3. 2 Comparison results : overall_PAE , ACPR, Peak-to-ave ratio

	Lower Channel ACPR (dBc)	Upper Channel ACPR (dBc)	Peak-to-Ave (dB)	Overall Ave_PAE %
Input Signal	-89.370	-89.451	9.340	
Wilkison Combiner	-64.928	-65.698	9.327	9.1
Tee Combiner	-63.435	-63.385	9.268	10.2
Chireix Outphasing Combiner	-60.568	-61.613	8.621	13.6
VRTC without X	-61.128	-60.446	8.603	11.9
VRTC with X Max_PAE	-35.231	-34.264	8.195	17.6
VRTC with proper X	-56.888	-57.601	8.303	15.5

CHAPTER 4

CONCLUSIONS

4.1 Project Conclusions

LINC is a feasible RF linearization technique, It has an integrated transmitter architecture with high efficiency and good linearity and achieves the longest battery life. In this thesis, two contributions in implementing a practical LINC transmitter have been accomplished: a new digital signal component separator (NDSCS) and a variable reactive termination combiner (VRTC).

The new digital signal component separator (NDSCS) avoids common DSP problems such as unsuitable word-lengths, low sampling rates and poor signal processing performance. FPGAs provide a flexible architecture which accelerates performance, as well as having a high DSP throughout. Its raw data processing power is greater than that of a standard DSP processor. Selecting a suitable FPGA device that easily accommodates all necessary algorithms makes for quick prototyping. It is also necessary to choose suitable analog-to-digital (A/D) converters and digital-to-analog (D/A) converters with sufficiently high sampling rates to meet the high speed signal processing needs.

Two NDSCS designs were implemented into a Quartus II FPGA: a one-dimensional look-up-table (LUT) and a square-root function block (SRFB). The one-dimensional LUT was memory-less and addressed by I-square plus Q-square (I^2+Q^2) using a 14-bit word-length. It stored 26-bits of calculated data in a random access

memory (RAM). Two or more parameterized D-type flipflops are used as timing-delay blocks to synchronize the data so as to obtain the correct data at the output. An alternative method is to create a customizing square-root function block in VHDL, which is less time-consuming and has higher performance. It is necessary to use pipelining techniques to synchronize the data which also increases the throughput, thereby improving performance. The combination of register-rich architecture and the predictable delays make it an attractive alternative to FPGAs for implementing complex pipelined designs. It had higher speed due to its pipelining design, but it had less accuracy than the LUT method due to shorter word-length.

All of designs were verified using simulations in Matlab's Simulink. The experimental results indicate that this new digital signal component separator, based on the FPGA, can minimize word length while still maintaining acceptable accuracy, increased bandwidth and reduced power consumption.

In the second part, the two main power combiner categories, isolated and unisolated, are analyzed. It was indicated that the isolated power combiner, such as a Wilkinson, has low efficiency because the unused signal power is dumped into a passive load. Even if highly efficient amplifiers are used, an overall efficiency of higher than 10% is difficult to achieve.

The unisolated power combiner, such as the proposed variable reactive termination combiner obtains improved efficiency. It has been shown that varying the combiner's input impedance according to the output power level decreases the DC power consumption over the output dynamic power range. Thus, the LINC amplifier's efficiency

can increase significantly, especially if the phase and amplitude errors in the two paths can be adequately controlled.

To achieve this load modulation as a function output power, the vectors analysed were voltage and current signals. An LINC system based on ideal voltage sources has some independence from the parameters of output power and efficiency . An approach has been developed to optimize the LINC transmitter efficiency as a function of the amplitude modulation statistics. It shows that adding appropriate shunt admittances across the voltage sources in the model greatly improves the peak-to-average efficiency. The average efficiency with various amplitude-modulated signals is determined as a function of shunt reactance. Selecting the shunt reactance to fit the signal can maximize the efficiency at a desired output.

The LINC transmitter with its new digital signal component separator and power combiner can be operated as an efficient linear amplifier for both GSM and CDMA type modulations. The LINC transmitter had been simulated using a two-tone signal and an IS-95 signal (1.2288 MHz bandwidth, 885 KHz channel offset ACPR –89.4 dBc 9.34 dB output peak-to-average ratio).

The experimental results show that the maximum average efficiency obtained is 17.6% using 23.5% efficiency class AB power amplifiers at 2.14 GHz. By properly selecting the value of the shunt susceptance, some linearity can be traded-off for efficiency. An average efficiency of 15.5% was held while the ACPR improved to –57 dBc. The same combiner without a shunt reactance obtained 11.9 % with a linearity of -60.5 dBc. A Wilkinson combiner had a much lower efficiency with the least degradation

of linearity. Thus, the new combiner has the best compromise between efficiency and linearity.

4.2 Future Works

First, the implementation of an ideal voltage or current source may become workable proposal for an LINC application. Once ideal signal source implementations are incorporated in a low-cost high-linearization LINC system, this independent modulation technology could become the preferred transmitter architecture of future multi-mode communication systems.

Second, the LINC transmitter is best implemented by a DSP technology. Therefore, the recommended future work should be focused on improving the data processing at baseband and implementing a digital intermediate frequency (IF) architecture. Digital up-converting the component signals from baseband to an intermediate frequency will remove any effects that non-ideal quatrature modulators may add to the two amplifier branches in an LINC system. Moreover, digital signal processing with high performance will not only increase the data rate but also raise the IF component signal frequency. A higher IF frequency requires less stringent filtering and fewer up-conversion stages.

Finally, synthesizing a linear, digital power combiner can also be introduced into the research area. The reactive termination combiner may be realized by automatic tuning elements. Since many DSP technologies are available for various applications, a microchip is a low-cost and low-size device which can act as look-up-table for

calibration data to operate the variable reactive termination. Moreover, testing software can also be designed to realize an automatic calibration interface.

In a word, all of these future works are feasible and therefore recommended and should be given a greater priority.

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APPENDIX A

DELAY BLOCK IN VHDL

```
FUNCTION  lpm_dff (data[LPM_WIDTH-1..0], clock, enable, shiftin, shiften, sclr, sset,
sconst, aclr, aset, aconst)

        WITH (LPM_WIDTH, LPM_AVALUE, LPM_SVALUE)
        RETURNS (q[LPM_WIDTH-1..0]);

 PARAMETERS
 (
  WIDTH = 12,
  DEEP = 29
  );

subdesign delay23
 (
  in[WIDTH..1]    : INPUT;
  clk             : INPUT;
  out[WIDTH..1]   : OUTPUT;
 )

VARIABLE
   p[WIDTH..1][DEEP..0] : node;

 BEGIN

  p[WIDTH..1][0] = in[WIDTH..1];
  FOR n IN 0 TO (DEEP-1) GENERATE
     p[WIDTH..1][n+1] = lpm_dff(p[WIDTH..1][n], clk,,,,,,,,)
                  WITH(LPM_WIDTH = WIDTH);

END GENERATE;

  out[WIDTH..1] = p[WIDTH..1][DEEP];

 END;
```

APPENDIX B

SQUARE ROOT FUNCTION BLOCK WITH PIPELINING IN VHDL

```
FUNCTION lpm_add_sub (cin, dataa[LPM_WIDTH-1..0], datab[LPM_WIDTH-1..0],
add_sub, clock, aclr)

  RETURNS (result[LPM_WIDTH-1..0], cout, overflow);

FUNCTION DFF (D, CLK, CLRN, PRN)
  RETURNS (Q);

FUNCTION lpm_dff (data[LPM_WIDTH-1..0], clock, enable, shiftin, shiften,
    sclr, sset, sconst, aclr, aset, aconst)
  WITH (LPM_WIDTH, LPM_AVALUE, LPM_SVALUE)
  RETURNS (q[LPM_WIDTH-1..0]);

PARAMETERS
(
WIDTH = 12,
PREC = 10
);

constant pw = 2*PREC;
constant odd = ((floor(WIDTH DIV 2)) == (ceil(WIDTH DIV 2))) ? 0:1;
constant inwidth = width+odd; -- if odd, internal width is 1 greater

subdesign rootb
(
rad[WIDTH..1] : INPUT;
clk         : INPUT;
root[PREC..1] : OUTPUT;
)

VARIABLE

 inrad[inwidth..1] : node;
 nrad[inwidth..1][PREC..1] : node;

 stone[2..1] : node;
```

```
  top[PREC..2][pw..1] : node;
  etop[PREC..2][pw..1] : node;
  bot[PREC..2][pw..1] : node;
  st[PREC..2][pw..1] : node;

  dummy[(pw-4)..1], dumst[pw..1] : node;

  preroot[PREC..1] : node;
  eroot[PREC..1][PREC..1]  : node;


BEGIN

    ASSERT (WIDTH>5)
        REPORT      "Parameter WIDTH must be at least 6"
        SEVERITY ERROR;
    ASSERT (PREC >= (ceil(WIDTH DIV 2)))
        REPORT      "Parameter PREC must be at least (WIDTH/2)"
        SEVERITY ERROR;

 IF (odd == 1) GENERATE
   inrad[] = (GND,rad[]);
 ELSE GENERATE
   inrad[] = rad[];
 END GENERATE;

   dummy[] = 0;

   (stone[],,) = lpm_add_sub (VCC, inrad[inwidth..(inwidth-1)], (GND,VCC),,clk,)
                                WITH (LPM_WIDTH = 2, LPM_DIRECTION = "SUB",
LPM_PIPELINE=1);

   preroot[PREC] = DFF((inrad[inwidth] # inrad[inwidth-1]), clk,,);

   eroot[PREC][1] = preroot[PREC];
 FOR n IN 1 TO (PREC-1) GENERATE
   eroot[PREC][n+1] = DFF (eroot[PREC][n], clk,,);  --root[PREC] delay (PREC-1)
clk
 END GENERATE;


    nrad[(inwidth-2)..(inwidth-3)][1] = lpm_dff(inrad[(inwidth-2)..(inwidth-3)],
```

```
clk,,,,,,,,,)
                        WITH(LPM_WIDTH = 2);
  top[2][pw..(pw-3)] = ( (stone[] & preroot[PREC]), nrad[(inwidth-2)..(inwidth-3)][1]);
  bot[2][pw..(pw-3)] = ( 0, preroot[PREC], 0, 1);

  (st[2][pw..(pw-3)],,) = lpm_add_sub (VCC, top[2][pw..(pw-3)], bot[2][pw..(pw-
3)],,clk,)
                                                WITH (LPM_WIDTH = 4,
LPM_DIRECTION = "SUB", LPM_PIPELINE=1);

   top[2][(pw-4)..1] = top[2][(pw-4)..1] # dummy[(pw-4)..1];
   bot[2][(pw-4)..1] = bot[2][(pw-4)..1] # dummy[(pw-4)..1];
   st[2][(pw-4)..1] = st[2][(pw-4)..1] # dummy[(pw-4)..1];

   preroot[PREC-1] = !st[2][pw];

   eroot[PREC-1][2] = preroot[PREC-1];
  FOR n IN 2 TO (PREC-1) GENERATE
   eroot[PREC-1][n+1] = DFF (eroot[PREC-1][n], CLK,,);  --root[PREC] delay
(PREC-2) clk
  END GENERATE;



  FOR k IN 3 TO PREC GENERATE

   etop[k-1][pw..(pw+3-(k*2))] = lpm_dff(top[k-1][pw..(pw+3-(k*2))],clk,,,,,,,,)
                        WITH(LPM_WIDTH = ((k*2)-2));
   top[k][pw..(pw+3-(k*2))] = (st[k-1][pw..(pw+3-(k*2))] & preroot[PREC+2-k]) #
                                                        (etop[k-1][pw..(pw+3-(k*2))] &
!preroot[PREC+2-k]);

  IF (k<=(inwidth DIV 2)) GENERATE


   nrad[(inwidth+2-(k*2))..(inwidth+1-(k*2))][1] = inrad[(inwidth+2-
(k*2))..(inwidth+1-(k*2))];
  FOR n IN 1 TO (k-1) GENERATE
   nrad[(inwidth+2-(k*2))..(inwidth+1-(k*2))][n+1] = lpm_dff(nrad[(inwidth+2-
(k*2))..(inwidth+1-(k*2))][n], clk,,,,,,,,)
                        WITH(LPM_WIDTH=2);
  END GENERATE;
   top[k][(pw+2-(k*2))..(pw+1-(k*2))] = nrad[(inwidth+2-(k*2))..(inwidth+1-(k*2))][k];
```

```
  ELSE GENERATE
   top[k][(pw+2-(k*2))..(pw+1-(k*2))] = (GND,GND);
  END GENERATE;

 FOR j IN 1 TO (k-1) GENERATE
  bot[k][pw+1-j] = GND;
 END GENERATE;

 FOR j IN 1 TO (k-1) GENERATE
  bot[k][pw+2-k-j] = eroot[PREC+1-j][k-1];
 END GENERATE;

  bot[k][(pw+2-(k*2))..(pw+1-(k*2))] = (GND,VCC);


  (st[k][pw..(pw+1-(k*2))],,) = lpm_add_sub (VCC, top[k][pw..(pw+1-(k*2))],
bot[k][pw..(pw+1-(k*2))],,clk,)
                                                    WITH (LPM_WIDTH =
(k*2), LPM_DIRECTION = "SUB", LPM_PIPELINE=1);

  preroot[PREC+1-k] = lcell(!st[k][pw]);  -- make sure that MP2 doesnt build huge carry
chain

 IF (k<PREC) GENERATE
  eroot[PREC+1-k][k] = preroot[PREC+1-k];
 FOR n IN k TO (PREC-1) GENERATE
  eroot[PREC+1-k][n+1] = DFF (eroot[PREC+1-k][n], clk,,); --root[PREC+1-k]
delay (PREC-k) clk
 END GENERATE;


  top[k][(pw-(k*2))..1] = top[k][(pw-(k*2))..1] # dummy[(pw-(k*2))..1];
  bot[k][(pw-(k*2))..1] = bot[k][(pw-(k*2))..1] # dummy[(pw-(k*2))..1];
  st[k][(pw-(k*2))..1] = st[k][(pw-(k*2))..1] # dummy[(pw-(k*2))..1];
 END GENERATE;

END GENERATE;
 root[1] = preroot[1];
 root[PREC..2] = eroot[PREC..2][PREC];


 dumst[] = st[PREC][pw..1] # dumst[];
 END;
```