Titre: Title:	A Wireless, High-Voltage Compliant, and Energy-Efficient Visual Intracortical Microstimulator
Auteur: Author:	Md Hasanuzzaman
Date:	2016
Type:	Mémoire ou thèse / Dissertation or Thesis
Référence: Citation:	Hasanuzzaman, M. (2016). A Wireless, High-Voltage Compliant, and Energy-Efficient Visual Intracortical Microstimulator [Thèse de doctorat, École Polytechnique de Montréal]. PolyPublie. https://publications.polymtl.ca/2245/

UNIVERSITÉ DE MONTRÉAL

A WIRELESS, HIGH-VOLTAGE COMPLIANT, AND ENERGY-EFFICIENT VISUAL INTRACORTICAL MICROSTIMULATOR

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THÈSE PRÉSENTÉE EN VUE DE L'OBTENTION
DU DIPLÔME DE PHILOSOPHIÆ DOCTOR
(GÉNIE ÉLECTRIQUE)
JUIN 2016

UNIVERSITÉ DE MONTRÉAL

POLYTECHNIQUE MONTRÉAL

Cette thèse intitulée :

A WIRELESS, HIGH-VOLTAGE COMPLIANT, AND ENERGY-EFFICIENT VISUAL INTRACORTICAL MICROSTIMULATOR

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en vue de l'obtention du diplôme de : Philosophiæ Doctor
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DEDICATION

To my parents, grandparents, sisters, brother-in-laws, nephews, uncles, aunts, and cousins.

. . .

ACKNOWLEDGMENTS

All praise and glory for our Creator, The Almighty God (Allah (subhanu ta'ala)) for granting me life. I have the deepest gratitude to Him for bestowing me with pure knowledge without which I would not be able to read, write, and learn. Then I have my heartfelt gratefulness to my supervisor Dr. Mohamad Sawan for giving me the opportunity to pursue my Ph.D. program under his supervision, mentoring and helping me in research throughout my journey to achieve my goal in Polytechnique Montreal. I would also like to express my gratitude to him for entitling me in his team to work on an exciting and promising project. My heartfelt gratitude also goes for my co-supervisor Dr. Rabin Raut for his counsel and help in my endeavor.

I express my sincere thanks and gratitude to Dr. Yvon Savaria, Dr. Frédéric Lesage, Dr. Yong Lian, and Dr. Julien Cohen-Adad for agreeing to be members of the examination board of my Ph.D. thesis.

Several people in the Polystim Neurotech team have been of invaluable assistance at one time or another for a long time. I specially thank LASEM laboratory co-ordinator Laurent Mouden for his technical help in the assembly of my developed system. Next, I thank Rejean Lepage, Jean Bouchard, Jacques Girardin, and Brian Tremblay for their technical supports. I thank the secretaries, especially Marie-Yannick Laplante and others of the Electrical Engineering Department for their cooperation.

I also thank Faycal Mounaim, Goutam Chandra Kar, Bahareh Ghane-Motlagh, Meghan Watson, Ahmad Hassan, Aref Tregui, Moez Bouali, Sreenil Saha, Sami Hached, Arash Moradi, Ghazal Nabovati, and others. I thank my other friends in laboratories M-5304, M-5306, M-5308, Polystim, and GR2M for being kind to me.

I earnestly want to express my deepest gratitude to my parents, grandparents, sisters and their families, my uncles, and aunts for their encouragements in my higher education.

I also would like to acknowledge the financial support from the Canada Research Chair in smart medical devices, the National Science and Engineering Research Council (NSERC) of Canada, and Fonds de la recherche québécoise sur la nature et les technologies (FRQNT), without which I could not accomplish my research and study.

In the end, my thank goes for CMC Microsystems for supporting me with their design tools and integrated circuits manufacturing facilities.

RÉSUMÉ

L'objectif général de ce projet de recherche est la conception, la mise en œuvre et la validation d'une interface sans fil intracorticale implantable en technologie CMOS avancée pour aider les personnes ayant une déficience visuelle. Les défis majeurs de cette recherche sont de répondre à la conformité à haute tension nécessaire à travers l'interface d'électrode-tissu (IET), augmenter la flexibilité dans la microstimulation et la surveillance multicanale, minimiser le budget de puissance pour un dispositif biomédical implantable, réduire la taille de l'implant et améliorer le taux de transmission sans fil des données. Par conséquent, nous présentons dans cette thèse un système de microstimulation intracorticale multi-puce basée sur une nouvelle architecture pour la transmission des données sans fil et le transfert de l'énergie se servant de couplages inductifs et capacitifs.

Une première puce, un générateur de stimuli (SG) éconergétique, et une autre qui est un amplificateur de haute impédance se connectant au réseau de microélectrodes de l'étage de sortie. Les 4 canaux de générateurs de stimuli produisent des impulsions rectangulaires, demi-sinus (DS), plateau-sinus (PS) et autres types d'impulsions de courant à haut rendement énergétique. Le SG comporte un contrôleur de faible puissance, des convertisseurs numérique-analogiques (DAC) opérant en mode courant, générateurs multi-forme d'ondes et miroirs de courants alimentés sous 1.2 et 3.3V se servant pour l'interface entre les deux technologies utilisées. Le courant de stimulation du SG varie entre 2.32 et 220μA pour chaque canal.

La deuxième puce (pilote de microélectrodes (MED)), une interface entre le SG et de l'arrangement de microélectrodes (MEA), fournit quatre niveaux différents de courant avec la valeur maximale de 400μA par entrée et 100μA par canal de sortie simultanément pour 8 à 16 sites de stimulation à travers les microélectrodes, connectés soit en configuration bipolaire ou monopolaire. Cette étage de sortie est hautement configurable et capable de délivrer une tension élevée pour satisfaire les conditions de l'interface à travers l'impédance de IET par rapport aux systèmes précédemment rapportés. Les valeurs nominales de plus grandes tensions d'alimentation sont de $\pm$10V. La sortie de tension mesurée est conformément 10V/phase (anodique ou cathodique) pour les tensions d'alimentation spécifiées. L'incrémentation de tensions d'alimentation à $\pm$13V permet de produire un courant de stimulation de 220μA par canal de sortie permettant d'élever la tension de sortie jusqu'au 20V par phase. Cet étage de sortie regroupe un commutateur haute tension pour interfacer une matrice des miroirs de courant (3.3V /20V), un registre à décalage de 32-bits à entrée sérielle, sortie parallèle, et un circuit dédié pour bloquer des états interdits.

Les deux puces ont été conçues et fabriquées avec les technologies IBM CMOS 0.13μm et Teledyne DALSA 0.8μm 5V/20V CMOS/DMOS avec des surfaces de silicium de 1.75 x 1.75mm^2 et 4 x 4mm^2 respectivement. Les budgets d'alimentation consommés par les puces basse et moyenne tensions ont été mesurées à 2.56 et 2.1mW consécutivement.

Ajoutons qu'un nouveau protocole de transfert bidirectionnel sans fil de données par le biais d'une liaison capacitive, qui est basée sur le principe de position spatiale de modulation par impulsion (SPPM). Cette liaison a été proposée par Polystim team pour transmettre des données à 10Mbps au microstimulateur à travers la peau. Le microstimulateur récupère l'énergie sans fil via une autre liaison inductive, accordée sur une porteuse à une fréquence de 13.56MHz. Le module de microstimulation (MS), combinant le SG et le pilote de microélectrodes, à une architecture modulaire et a été interfacé avec un arrangement de microélectrodes en format pyramidal développé par Polystim team pour atteindre différents niveaux de neurones dans le cortex visuel primaire. L'ensemble du système proposé a été validé par des tests in vitro dans une solution saline (NaCl 0.15M) et les résultats expérimentaux démontrent l'efficacité du prototype complété.

ABSTRACT

The general objective of this research project is the design, implementation and validation of an implantable wireless intracortical interface in advanced CMOS technology to aid the visually impaired people. The major challenges in this research are to meet the required high-voltage compliance across electrode-tissue interface (ETI), increase flexibility in multichannel microstimulation and monitoring, minimize power budget for an implantable biomedical device, reduce the implant size, and enhance the data rate in wireless transmission. Therefore, we present in this thesis a multi-chip intracortical microstimulation system based on a novel architecture for wireless data and power transmission comprising inductive and capacitive couplings.

The first chip is an energy-efficient stimuli generator (SG) and the second one is a high-impedance microelectrode array driver output-stage. The 4-channel stimuli-generator produces rectangular, half-sine (HS), plateau-sine (PS), and other types of energy-efficient current pulse. The SG is featured with low-power controller, current mode source- and sink-digital-to-analog converters (DACs), multi-waveform generators, and 1.2V/3.3V interface current mirrors. The stimulation current per channel of the SG ranges from 2.32 to 220μA per channel.

The second chip (microelectrode driver (MED)), an interface between the SG and the microelectrode array (MEA), supplies four different current levels with the maximum value of 400μA per input and 100μA per output channel. These currents can be delivered simultaneously to 8 to 16 stimulation sites through microelectrodes, connected either in bipolar or monopolar configuration. This output stage is highly-configurable and able to deliver higher compliance voltage across ETI impedance compared to previously reported designs. The nominal values of largest supply voltages are $\pm$10V. The measured output compliance voltage is 10V/phase (anodic or cathodic) for the specified supply voltages. Increment of supply voltages to $\pm$13V allows 220μA stimulation current per output channel enhancing the output compliance voltage up to 20V per phase. This output-stage is featured with a high-voltage switch-matrix, 3.3V/20V current mirrors, an on-chip 32-bit serial-in parallel-out shift register, and the forbidden state logic building blocks.

The SG and MED chips have been designed and fabricated in IBM 0.13μm CMOS and Teledyne DALSA 0.8μm 5V/20V CMOS/DMOS technologies with silicon areas occupied by them 1.75 x 1.75mm^2 and 4 x 4mm^2 respectively. The measured DC power budgets consumed by low-and mid-voltage microchips are 2.56 and 2.1mW consecutively.

On the other hand, a new capacitive link-based bi-directional wireless data transfer protocol,

which works on spatial pulse position modulation (SPPM) principle, has been implemented to transmit data at 3Mbps to the microstimulator through skin. Power is recovered wirelessly through an inductive-link, which is tuned at 13.56MHz carrier frequency. The microstimultion module (MS), combining the SG and MED, is modular in architecture and has been interfaced with a newly developed, by Polystim team, platinum coated pyramidal shaped microelectrode array (MEA), which can reach the different levels of neurons in the primary visual cortex. The multichip system has been successfully validated through in-vitro tests in 0.15M NaCl saline and the experimental results confirm the efficacy of the completed prototype.

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LIST OF ABREVIATIONS

GRM	Groupe de Recherche en Microélectronique
LASEM	Electronic Microsystems Assembly and Encapsulation Laboratory
GR2M	Microelectronics and Microsystems Research Group
NSERC	National Science and Engineering Research Council
FRQNT	Fonds de la recherche québécois sur la nature et les technologies
CMC	Canadian Microelectronics Corporation
CMOS	Complimentary metal-oxide-semiconductor
DMOS	Double diffused metal-oxide-semiconductor
SG	Stimuli generator
ETI	Electrode-tissue interface
MED	Microelectrode driver
MEA	Microelectrode array
HS	Half-sine
PS	Plateau-sine
DAC	Digital-to-analog converter
ADC	Analog-to-digital converter
SAR	Successive approximation
SPPM	Spatial pulse position modulation
MS	Microstimultion module
WHO	World Health Organization
FES	Functional electrical stimulation
DBS	Deep brain stimulation
CNS	Central nervous system
CIC	Charge injection capacity
GSA	Geometric surface area
AIROF	Activated iridium-oxide film
SIROF	Sputtered iridium-oxide film

UIEA	Utah intracortical electrode array
PPy	Poly(pyrrole)
PEDOT	Poly(3,4-ethylenedioxythiophene)
SOI	Silicon on insulator
LGN	Lateral geniculate nucleus
AMD	Age related macular degeneration
RP	Retinitis pigmentisa
ASIC	Application specific integrated circuit
LSU	Local stimulation unit
IEEE	Institute of Electrical and Electronics Engineers
PDMS	Polydimethylsiloxane
RF	Radio frequency
FSK	Frequency shift keyed
LC	Inductive-capacitive
IM	Interface module
SM	Stimulation module
MVG	Monash Vision Group
OSHC	Original scientific hypothesis of contributions to research
SIPO	Serial-in parallel-out
SISO	Serial-in serial-out
FF	Flip-flop
FPGA	Field programmable gate array
FSLC	Forbidden state logic circuit
LS	Level shifter
DMOS	Double diffuse MOSFET
LDMOS	Lateral double diffuse MOSFET
TG	Transmission gate
ISM	Industrial-scientific-medical
LDO	Low-drop out regulator
ASK	Amplitude Shift Keying
SPPM	Spatial pulse position modulation
MIMO	Multiple-Input and Multiple-Output
SNR	Signal-to-noise ratio
SPPM	Spatial pulse position modulation

AEM	Amplitude-engraving modulation
CSP	Chip scale package
BGA	Ball grid array
PCB	Printed circuit board
HDI	High density interconnect
MUX	Multiplexer
SEM	Scanning electron microscope

LIST OF NOTATIONS

I_{th}	The current required to reach threshold
I_{th}	Rheobase current
t_c	Chronaxie time
τ_m	Membrane time constant
Z_w	Warburg impedance
R_{CT}	Charge transfer resistance
Z_{CPA}	Non faradic pseudo capacitance
R	Resistance
V	Voltage
t	Time
T	Pulse-width
$E(t)$	Instantaneous energy
$P(t)$	Instantaneous power
$V(t)$	Instantaneous voltage
$I(t)$	Instantaneous current
T_s	Pulse-width
$Z(t)$	ETI impedance
M_n	Transistor
V_T	Thermal voltage
C	Capacitance
Ihsine	Half-sine current pulse
S_n	TG based CMOS switch
Rs_{ON}	Switch-on resistance
$g_{ds_{ON}}$	Switch-on transconductance
D_i	Digital data

CHAPTER 1

INTRODUCTION

In recent past, the field of biomedical engineering has proved to be a very promising to restore physiological functions. A substantial growth of research in biomedical engineering has been experienced in recent decades. Implantable medical devices have been found to be one of the major applications where scientists, engineers, and physicians have shown great enthusiasm. The pacemaker and cochlear implant have become commonly used prosthetic devices to restore vital functions. However, power and area miniaturization of implantable microelectronics circuits are still considered to be major challenges, that the researchers, nowadays, are trying to solve.

Scientific community has shown great interest for a long time to blindness, a serious physiological dysfunction, in which approximately 39 million blind people around the world are likely to be affected (World Health Organization [WHO], 2014). According to the study carried by WHO, in case of a significant number of patients such blindness cannot be treated following normal surgical procedure. To deal these cases, considered to be irreversible, a group of researchers have been studying functional electrical stimulation (FES) technique and employing it in microelectronic based prosthetic devices with an aim to enable visually impaired patients to recover functional vision. The performance of such systems are affected by the technical specifications related to the physical constraints, such as the energy efficiency of needed stimulation system and the required data rate to run an implant dedicated to such stimulation.

Authors presented different solutions addressing difficulties of the visual implants. However, these solutions are generally contemplated with a specific goal and have a limited perspective. Consequently, fundamental and technical considerations are omitted, and the results are not representative of solutions to complete systems in all respects.

The relevant recent publications of the most respected and advanced teams in this field have developed implants that allow sufficient stimulation and parallel data transfer rate capabilities, but present several drawbacks such as power consumption well beyond the authorized budget [1], [2], [3]. Owing to the limited power budget for the implantable biomedical devices, and in order to ensure the safety of biological tissues and for a long battery life, a transcutaneous inductive-link can not assuredly provide such amount of energy continuously to the implant [4]. Some solutions to optimize the energy transfer are also proposed, but can

not guarantee that the power of the implant is unduly affected by the activity of the latter [5], [6]. The high-voltage compliance, needed at the output stage of the device, is a major issue and it requires the use of high-voltage CMOS/DMOS process. On the other hand, minimizing power consumptions is also necessary. Therefore, a compromise between the use of low-power and high-voltage technologies, and complexity can be made to satisfy these two divergent requirements.

Therefore, the research team at the Polystim neurotech laboratory at the Polytechnique Montreal has launched the Cortivision project in this context. The purpose is to build a visual prosthetic implant to stimulate the visual cortex area. To achieve this goal, a functional prototype was built and successfully validated through in-vivo experiments on rats [7]. The power needed for the implant was derived from an external battery and was transmitted through a wireless inductive-link. It is essential to limit power dissipation of the implant for long battery life, as the microstimulator in daily application is used several hours per day. Therefore, for any implantable device, power consumption is a primary concern and an important constraint. The high impedance of the electrode between the electrode and the physiological tissue is the second design constraint for an intracortical microstimulator. This high-impedance necessitates the use of high voltages in the output-stage of a microstimulator for typical stimulation current of about 100μA. Implementing the output-stage in low voltage CMOS process to satisfy the need of high-voltage is quite unreliable, as the generated high-voltage would stress the low-voltage transistors and make the system unreliable. Enhanced flexibility in the output-stage is also required for maximum channel count and delivering stimulation currents to neural sites using charge-balanced monopolar and bipolar stimulation. The third constraint is the multichannel monitoring of stimulation sites prior to, during, and after injecting excitation current to prevent the damage of the device and release of toxic ions in the tissues. Research teams have estimated that 625 to 1000 phosphenes in the visual field are needed to create useful vision [8]-[12]. For a wirelessly controlled microstimulator, data-rate of about 10Mbps is required to stimulate such large number of sites and the detailed calculation is provided in Chapter 6.

The primary goal of this research project is to build an intracortical microstimulator keeping energy savings, required data-rate and voltage-compliance across the electrode-tissue interface (ETI), enhanced flexibility in multichannel stimulation and monitoring in mind, when compared to the previously designed prototypes ([7], [13]). To accomplish our objective, new category of potential energy-efficient stimulation pulse types have been generated and delivered through a highly-configurable high-voltage compliant output-stage, named as microlectrode driver (MED). The new stimulation pulse patterns are introduced to minimize power consumption by some fraction both in the device as well as across ETI, when a large

number of neural sites are excited. The other objective of this thesis is to design and implement a wireless high data-rate (at least 10Mbps) communication module to maximize the stimulation channel count and capability in the device and therefore, neural sites through high density microelectrode array (MEA). Assuredly, characterization and validation of the newly developed prototype through in-vitro or in-vivo experiments are also within our objectives. However, such successful experiments do not endorse entirely the efficacy and safety of the device unless tested on human subjects. Therefore, the long term goal is to design the prototype, with an objective to implant and verify on human subjects.

1.1 Organisation of the thesis

This Ph.D. thesis includes eight chapters. The first chapter (this chapter) discusses the motivation behind this research and organization of this thesis. The second one discusses the basic principle and parameters of electrical stimulation, physiological concepts needed to understand the specifications of and build an intracortical microstimulation system, and essential elements required to create an interface between the former and neural tissues. In the beginning we discuss how different stimulation parameters affect the process of stimulation. Secondly, we proceed to different types of waveforms which can be employed in FES. Thirdly, an essential interface, the MEA, its working principle and types are addressed. Next, we proceed to discuss the different physiological aspects, such as visual system, different regions of visual cortex, neuron basics and its working principle, and generation of action potential and its propagation.

The third chapter deals with a review of the literature. We have categorized the visual prosthetic implants based on the location along the visual pathways. At first, we have presented an overview of architectures of different retinal implants designed by prominent research groups. Secondly, works and systems for optic nerve stimulation have been presented. Thirdly, we have discussed various visual intracortical implants, designed by renowned research groups. We have investigated the specifications and performances of the built prototypes. Their technical limitations, which have not been addressed and need to be solved, have been identified from global perspective. We have formulated the research questions to resolve the technical limitations or challenges in the existing intracortical architectures presented in the second chapter. Based on this, we have set up our general and specific objectives, and developed our hypotheses (original scientific hypothesis). Finally, we have proposed the new architecture of visual intracortical microstimulator satisfying the specifications derived from the research questions and objectives. The novel items related to the original contributions are presented in chapters 4 to 7.

The fourth chapter presents the proposed system and microstimulation module (MSM), and deals with the design and implementation of the energy-efficient stimuli-generator (SG). We begin with investigation on various types of excitation efficient pulse patterns and selecting those concluded to be the most energy-optimum for implementation. Next, the architecture of the SG, working and design principles of different functional blocks, and the experimental results of the fabricated chip are presented.

In the fifth chapter, we include the architectures of the microelectrode driver, discuss their configurability issues, design specifications and working principles of the building blocks. The experimental results are presented in the end.

The sixth chapter discusses the data and power recovery units. At first, we summarize the main published architectures of energy and power recovery units for biomedical devices. Next, we presented the configuration of the proposed subsystems, design and working principles of different circuits, and achieved results.

The ETI voltage monitoring unit; the central controller; and the assembly techniques of all the chips fabricated for this project, including MEA, and the additional discrete components are presented in chapter seven. At first, we have illustrated the ETI voltage monitoring unit and the associated experimental results, and next, discussed the configuration of the central controller. The in-vitro experimental results are also presented supporting the performance and validation of the complete prototype.

Finally, in chapter eight, we summarize all the work done, our contributions, and achievements in this thesis. Necessary steps to be taken for further improvements on the present design are also recommended here. This conclusion also presents the future direction as an extension to the current research.

CHAPTER 2

MICROSTIMULATION BASICS

2.1 Introduction

The origin of electric therapy dates back to the ancient time when a freed slave, Anthero, of the Roman Emperror Tiberius Claudius Nero Caesar (ruler of the ancient Rome from AD 14 to AD 37), stepped on a torpedo fish accidentally while walking by a seashore. Anthero was suffering from gout and the electric shock from the torpedo fish, which can reach sometimes about 100-150 volts (DC), worked as the electric therapy for him [14]. The ancients also used amber and magnetic rings for electric treatments. These properties of amber and magnetic rings were further studied in the medieval Europe by Italian mathematician and physician, Gerolamo Cardano (1501-1576). The first electric therapy was performed in 1744 by Christian Gottlieb Kratzenstein, a physician and Professor of Medicine at Halle, on a female patient to free her contracted little finger. The increase in the heart rate was also first observed by him while performing electrification on another patient. In the eighteenth and nineteenth centuries, further development was achieved due to Volta's battery, Galvanism, electrostatic machine, introduction of Newton's theories of matter. It was not until twentieth century, electric therapy has been termed as functional electrical stimulation and modernized with the development of miniaturized microelectronic devices. Generally, stimulation can be defined as the action of different stimuli on muscles, nerves, or sensory end organ. The impulse signals are produced in the nerve tissues in response to the applied stimulation signals, which can be chemical, electrical, or optical in nature, and activities are evoked in those biological body parts. The scope of this chapter is to focus on functional electrical stimulation and its applications to rehabilitation.

2.2 Functional electrical stimulation

The principle, Functional Electrical Stimulation (FES), was first applied by W.T. Liberson and named it as Functional Electrotherapy [15]. The term FES was first introduced by Moe and Post, who defined it as the process of "pairing the stimulation simultaneously or intermittently with a functional task" [16]. As mentioned earlier, history says that this procedure, used for rehabilitation purpose is not new, and dates back in 1790 when Italian anatomist and physician Luigi Galvani observed motion in the leg muscles of a frog after applying elec-

trical currents. In 1831, Michael Faraday claimed that nerves can be stimulated by injecting electrical currents to them to create active movement [17]. Applications of FES are numerous, such as, pacemaker, deep brain stimulation (DBS) for Perkinson diseases, epilepsy [18], cochlear implant [19], motor nerves stimulator [20], bladder implant [21], retinal and visual intracortical implants [22] and so on.

During microstimulation, irrespective of applications, the net quantity of charge delivered to muscle or nerve tissue should be zero at the end of microstimulation period to prevent the electro-chemical reactions in the of biological tissue and for the safety of the patient. This can be achieved by providing charge-balanced biphasic waveforms. The associated parameters, which are amplitude and width of applied pulse, stimulation frequency and period, inter-pulse duration, type of waveforms etc. should be carefully chosen to receive optimum microstimulation effects. Electrical stimulation can be performed using voltage or current signals or in the form of delivered charge quantity. An integral part of the microstimulation system, microelectrode array, delivers the microstimulation signals to the stimulation sites. The microelectrode-tissue interface impedance, which can reach up to few Mega Ohms depending on the coating material used to coat the electrode tip, plays a vital role to define the compliance voltage needed for the microstimulation system.

2.2.1 Category of FES

Functional electrical stimulation can be categorized as voltage-mode and current-mode [23].

Voltage-mode stimulation

The stimulation signal in the voltage-mode stimulation is voltage, which is converted into current when the stimulation signal is applied to the electrode. The magnitude of the converted current or the quantity of delivered charge which is directly proportional to the applied current is not constant and affected by electrode-tissue interface, nerve and inter-electrode impedances. This method is applicable only when the information on the range of the change of electrode-impedance over time is available. Therefore, this method of microstimulation does not allow the precise control of the exact amount of charge to be passed to the microstimulations sites. An excessive amount of charge will cause irreversible Faradic electro-chemical reactions in the tissues and damage them. A number of voltage controlled microstimulator has been discussed in [24] – [26].

Current-mode stimulation

On the contrary, current-mode stimulation has the feature of controlling the charge quantity meticulously. This advantage of current-controlled stimulator over the voltage-mode has made it preferable for implementation in most of the stimulators. The output current is usually controlled by current-mode source or sink digital-to-analog converters (DACs). This method is appropriate when there is a possibility of wide variations of electrode-tissue interface impedance. The stimulator provides constant level of current, as long as the stimulation parameters are kept constant and provided that wave-forms other than the rectangular pulse are not applied. In this regard, it is worth to mention that there are other types of wave-forms which can be used for microstimulation for energy saving purpose and it will be discussed shortly. A wide variety of current mode stimulators have been developed so far, and two of such systems are reported in [22] and [27].

2.2.2 Parameters of FES

The efficiency of electrical stimulation can be optimized by customizing the associated stimulation parameters, illustrated in Figure 2.1. It is also necessary to ensure the safety and comfort of patient. The stimulation parameters are pulse width, amplitude and shape; interpulse duration; stimulation frequency and duration; duty cycle; type of stimulation waveform; phase of the pulse; number of pulse trains within stimulation duration etc.

Amplitude/Intensity

The strength of the stimulation current, I, is determined by its magnitude (also the total quantity of charge delivered) in μA or mA. The type of the electrode also plays a significant role on the requirement of the intensity level of the current. Implantable penetrating electrodes require less current (up to few hundred microamperes) due to the proximity of the target area. On the contrary, surface mode stimulation which is a non-invasive technique, requires larger current, generally in the order of milliampere. The current with higher amplitude has the stronger depolarizing effect on the nerves. But, the intensity of the current is also restricted by the maximum tolerable heat dissipation limit in the tissue, and to prevent the damage to the nerve or muscle fibres and corrosion of electrode surface.

Pulse-duration/width

The pulse-duration or width, t is defined as the time span of a single pulse. The width of a single pulse for both monophasic and biphasic waveforms vary depending on the amplitude

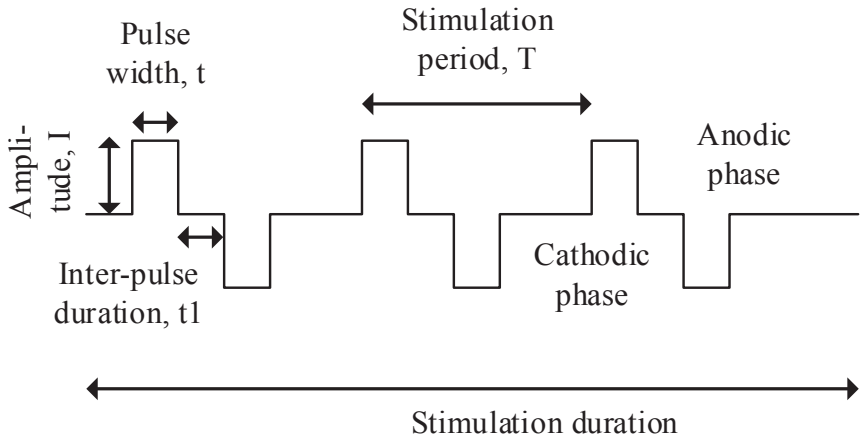


Figure 2.1 Typical constant current stimulation waveforms showing various stimulation parameters.

of the current and the net quantity of charge to be applied to the stimulation site. In [28], Cameron C.M. et al. applied monophasic and biphasic waveforms with pulse durations of 10μS – 1mS to excite central nervous system (CNS) neuron populations. The objective was to identify the optimum stimulus and electrode geometry. In [29], Thomas J. F. et al. performed an investigation on different waveforms in order to identify their advantages over conventionally used rectangular waveforms for deep brain stimulation. Pulse width, in this case, was varied from 50μS to 2mS. However, they also have mentioned the rectangular pulse of width 100μS as the "gold standard" for neurostimulators. It is better to use narrow pulse width to minimize electrochemical reactions that may occur on the surface of the electrode.

Inter-pulse duration

Inter-pulse duration is defined by the distance between anodic and cathodic pulses within one complete stimulation period. Usually, a charge-balanced biphasic waveform is preferred to prevent the tissue damage. While performing stimulation, in some cases, irreversible reactions occur, leading to the development of positive potential (with respect to the pre-pulse potential) at the end of anodic phase. This electrochemical process causes electrode corrosion, may suppress an action potential and increase the stimulation threshold for a biphasic stimulation compared to monophasic case. These undesirable effects can be minimized by introducing an interphase delay between cathodic (stimulating) and anodic (reversal) phases. In [30], it has been suggested that an interphase (or inter-pulse) delay of about 100μS is effective enough to prevent the action potential suppression while keeping the products of electrochemical reactions in the acceptable range.

Stimulation frequency

Stimulation frequency is the inverse of the stimulation period, T as shown in Figure 2.1. T is the distance between two successive anodic or cathodic pulses for monophasic and biphasic stimulation. Stimulation frequency is application dependent and can range from 50 to 4000Hz.

Stimulation pulses

Stimulation waveforms are usually two types, monophasic and biphasic as shown in Figure 2.2.

Monophasic waveforms are unidirectional and consist of either positive or negative pulses. In practical cases, a number of repetitive cathodic (negative) pulses are applied to construct this unidirectional waveform. This kind of stimulus pattern is used generally in surface electrode stimulation. The one directional current causes electrode deterioration (corrosion, electrode tissue-interface impedance change) and polarization, and changes the ionic distribution in the biological medium, which in turn causes tissue damage. These undesirable effects can be minimized using biphasic waveforms, provided that those are charge-balanced.

Biphasic waveforms consist of repeating pulse pattern, composed of cathodic (negative) pulse followed by anodic (positive) pulse. Cathodic pulse generates action potentials in the neural tissue by depolarizing the axons. The charge accumulated during this phase can damage the tissues due to the Faradic electro-chemical reaction. The succeeding anodic pulse of equal quantity of positive charge is applied to negate the residual negative charge accumulated in the preceding phase. The biphasic waveforms can be either symmetric or asymmetric as shown in Figure 2.2, where in both cases they should be charge-balanced. In most of the stimulators, charge-balanced waveforms are rectangular in shape, but waveforms with other pulse shapes can also be applied as long as they have the similar effect as of the former one on the nerve or muscle tissue. Usually, the primary pulse has rectangular-shape, and the secondary pulse can have either rectangular or exponentially decaying shape, known as active- and passive-discharging phase respectively. The quantity of charge delivered during any phase, Q(t), is the total area under that pulse. Q(t) is equal in both phases for charge-balanced waveforms irrespective of the symmetry in two phases.

Electrode-configuration/Microstimuation-strategy

Electrodes can be configured either in monolpar, or bipolar, or tripolar or hexagonal arrangement. In monopolar case, as shown in Figure 2.3(a), stimulation current is passed through

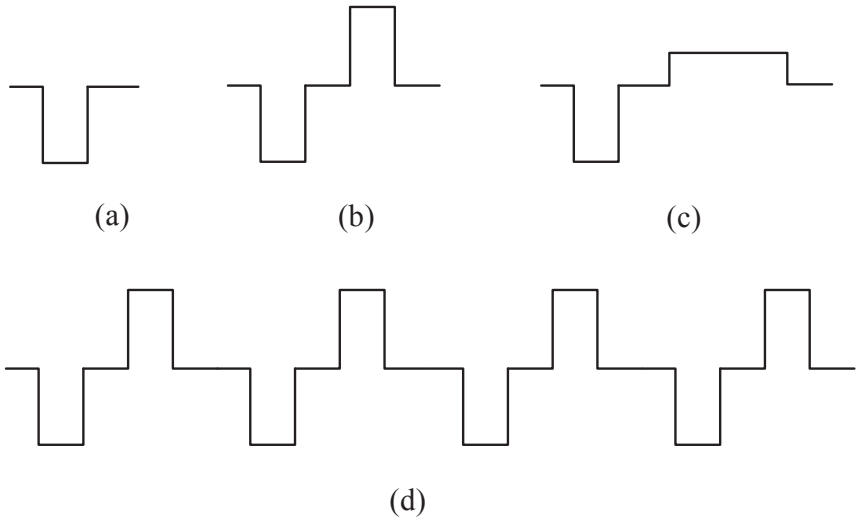


Figure 2.2 Various types of constant current pulses: (a) monophasic, (b) biphasic (symmetric), (c) biphasic (assymmetric), and (d) pulse train (charge-balanced).

the active electrode which is also known as working electrode and a return (or counter) electrode, located near or far, is provided for the outgoing (return) current. The return electrode also works as a reference electrode in this case. Charge is balanced with the aid of a capacitor discharge circuit, resulting in a cathode leading monophasic and capacitive coupled waveform. In bipolar configuration, presented in Figure 2.3(b), two working electrodes are used for stimulation and current direction is altered to provide biphasic stimulation currents, conventionally beginning with the cathodic phase for physiological purpose. Potentials of both working and counter electrodes may fluctuate, which is measured with respect to the third electrode potential, kept at the reference point (usually ground) [30]. A various patterns of biphasic current waveforms can be applied and have been illustrated with their effects on stimulation efficacy, tissue damage and electrode corrosion in [30]. In tripolar mode, current, applied to two working electrodes, is evenly distributed among them and returns through the counter electrode.

2.2.3 Stimulation waveforms

The rectangular pulse waveform has been used for microstimulation for long time because of its superior charge injection capacity over other types of pulse waveforms. The charge quantity per pulse, as mentioned earlier, is defined by the amplitude and duration of the pulse, and defines the strength of that pulse.
The relation between the amplitude of the current needed to generate an action potential and

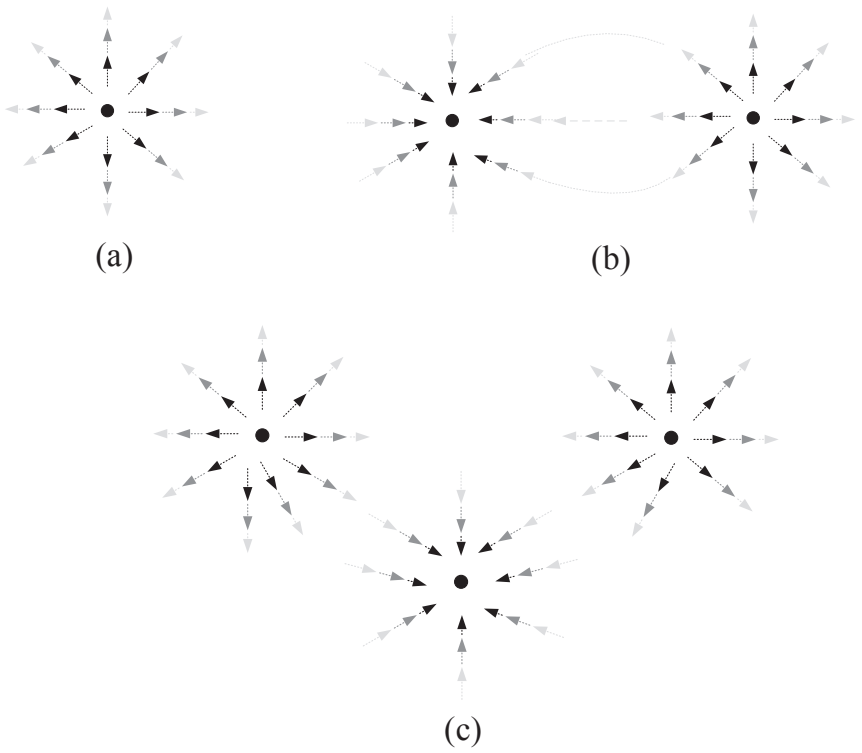


Figure 2.3 Modes of electrode configuration for stimulation: (a) monopolar, (b) bipolar, and (c) tripolar.

the pulse duration was first described by the strength-duration curve formulated by Lapicque [31], [32]. The strength-duration curve is presented in Figure 2.4. The required stimulation current decreases with the increase in the pulse-width and is minimum for infinitely wide pulse. Two important parameters of this curve are the Chronaxie time (t_c) and Rheobase current (I_{rh}). Rheobase current, (I_{rh}) corresponds to the current magnitude required for a pulse of infinite duration. The pulse width corresponding to twice of the rheobase current is the Chronaxie time tc. The strength-duration curve, shown in Figure 2.4, represents generally for a typical excitable tissue. However, the Rheobase current is empirical and its value is affected by the factors, such as the distance between the target neuron tissue and electrode and electrode geometry. The relation between the current required to reach threshold, (I_{th}) and (I_{rh}) can be well understood from the following equation

$$I_{th} = \frac{I_{rh}}{1 - e^{\frac{-W}{\tau_m}}} \tag{2.1}$$

Where, τ_m is the membrane time constant and W is the pulse width.
In the literature, most of the strength-duration curves are defined for rectangular pulse.

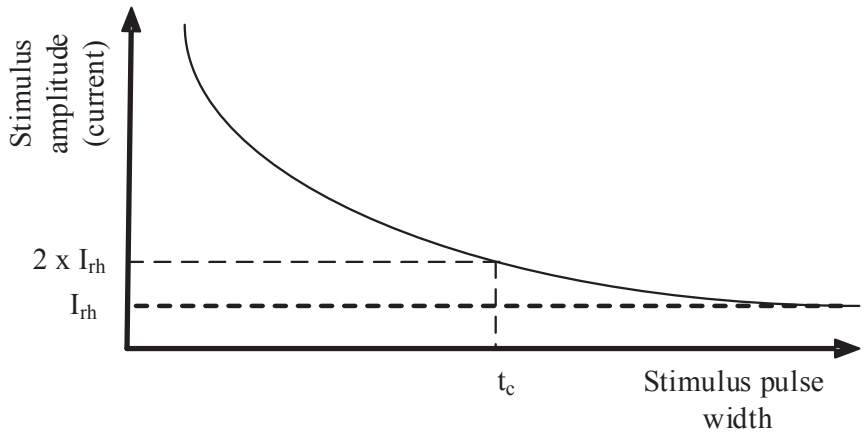


Figure 2.4 Strength–duration curve for activation of an action potential. (I_{rh}) is the Rheobase current and (t_c) is the Chronaxie time.

2.3 Microelectrodes

An integral part of a neural stimulator is microelectrodes which are used to deliver the stimulation signals to the neural sites. Applications can be bladder prostheses, brain-stem and cochlear prostheses, deep brain stimulation (DBS) for treating Parkinson's diseases, epilepsy and vagus nerve stimulation for epilepsy. Microelectrodes for neural stimulation can be classified into two types based on their functional properties, surface electrodes and penetrating electrodes [33]. The first type of electrodes have the geometric surface area (GSA) of about 100,000 μm^2 and are placed on the surface of the stimulation sites [34]. They have low-charge density thresholds and high-charge/phase thresholds. Therefore, high current in the range of mA is required for stimulation using the surface electrodes. On the other hand, penetrating electrodes have high-charge density and low-charge/phase thresholds, and GSA of about 10,000 μm^2. A large number of electrodes can be implanted in a smaller area providing better selectivity and spatial resolution. Another advantage is the needed smaller magnitude of current in the order of approximately 100μA which reduces power consumption and increases the life span of the microstimualtor.

2.3.1 Working principle of stimulation microelectrodes

Electro-chemical reaction occurs at the microelectrode-tissue interface due to the charge injection during microstimulation [34]. This reaction can be either capacitive or Faradic. Charging and discharging occur across the electrode-electrolyte double layer capacitors and reactions can be electrostatic or electrolytic in nature. Electrostatic capacitive charging

involves purely double-layer ion-electron charge separation and electrolyte dipole orientation. On the other hand, electrolytic reaction involves storing charge across a thin, high-dielectric-constant oxide at the electrode-electrolyte interface. Faradaic reactions involve the transfer of an electron across the electrode-electrolyte interface and require that some species, on the surface of the electrode or in solution, undergo a change in valence, i.e., are oxidized or reduced (oxidation-reduction process).

Surface electrodes

This type of electrode is non-invasive and attached to the skin [33]. Stimulation with surface electrodes has some disadvantages. Due to the high resistance of skin, stimulus voltage needs to be high enough for generating required tissue current. The necessity for large current is met also by making the electrode surface area large. Skin can be damaged at the high conductive areas due to the local current density. Surface electrodes are not a good choice for stimulation if nerves are located in the deep.

Percutaneous electrodes

Percutaneous electrodes are fine wire electrodes, placed close the nerves percutaneously, to provide stimulation current pulses in smaller magnitude in comparison to that for surface electrodes [33]. Monopolar stimulation currents are passed through the working electrodes and currents are returned through a common surface electrode, called return electrode.

Implantable electrodes

Implantation of these types of electrodes to the locations requires surgery [33]. However, this invasive technique has several advantages over non-invasive techniques. Electrodes can be placed almost precisely to the desired stimulation sites, spreading of current through surrounding tissues can be minimized, and required stimulation current is considerably reduced due to the proximity of electrodes to the nerves or muscle tissues. Examples can be peripheral nerve cuff electrode, wraparound electrode, monopolar epimysial electrode, intrathecal nerve root electrode, spinal stimulation electrodes, deep brain electrode, Michigan array, 3D Utah array and so on. With the advances in micromachining and microfabrication techniques a wide range of microelectrodes have been designed, fabricated and tested for various clinical applications such as cochlear-, visual intracortical-, bladder- and retinal implants, epilepsy, and Alzheimer diseases. Silicon based microelectrodes will be discussed in brief in the next section.

Silicon based microelectrode array

These types of microelectrodes are made on silicon substrate and materials such as platinum, iridium, iridium-oxide, activated iridium-oxide (AIROF), sputtered iridium-oxide (SIROF)

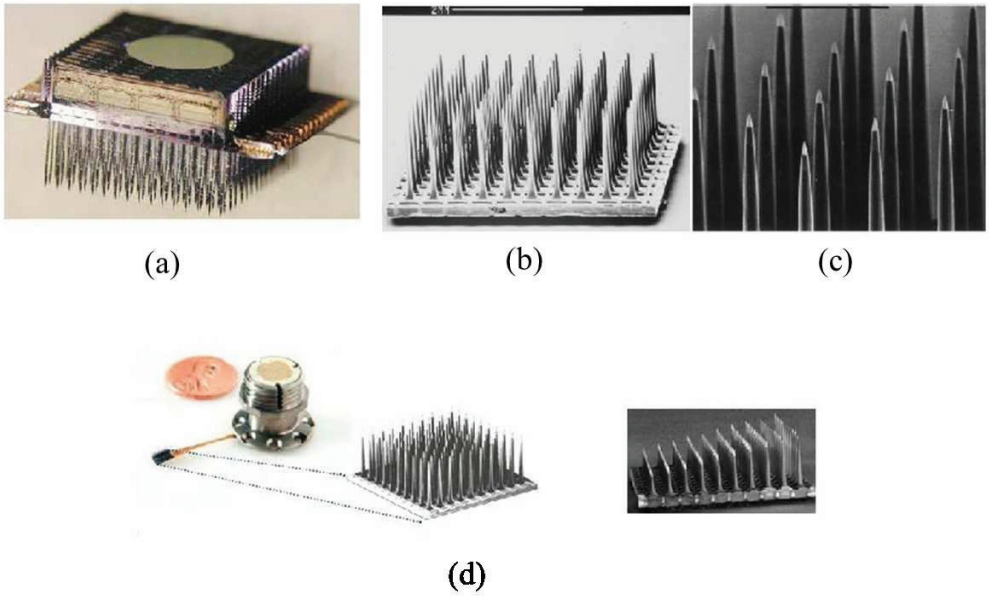


Figure 2.5 Slicon based microelectrode arrays: (a) A 3-D 128 channel 1024 site michigan array, (b)-(c) Utah MEA [36], and (d) MEA from Blacrock Microsystems [37].

[34] or carbon nanotube are used to coat the tips of electrodes. Silicon substrate is doped with boron in case of Michigan array and electrodes are made of 4 mm long on average. Utah intracortical electrode array (UIEA) are made from a single silicon wafer of 0.2mm thickness. 1.2mm long electrodes are of needle shaped and the chemically etched sharp tips are layered with platinum, titanium-tungsten and platinum. This coating works as an electrical interface between the electrode surface and the surrounding biological tissues and provides impedance in the range of 80 - 150kΩ [35]. Access to the electrodes are provided through the gold contact pads in the back of each electrode. Figure 2.5 - Figure 2.6 show different types of silicon-based microelectrode array (MEA) fabricated by various research groups and companies [36], [37], [38].

There are also some other types of electrodes made of silicon substrate and thin film conductor based probes. Recent studies show that materials such as poly(pyrrole) (PPy) and poly(3,4-ethylenedioxythiophene) (PEDOT) have better biocompatibility than the conventionally used noble metals. Through the use of electrochemical polymerization process, PPy and PEDOT are deposited on the microelectrode sites [36], [39]. Figure 2.7 presents silicon

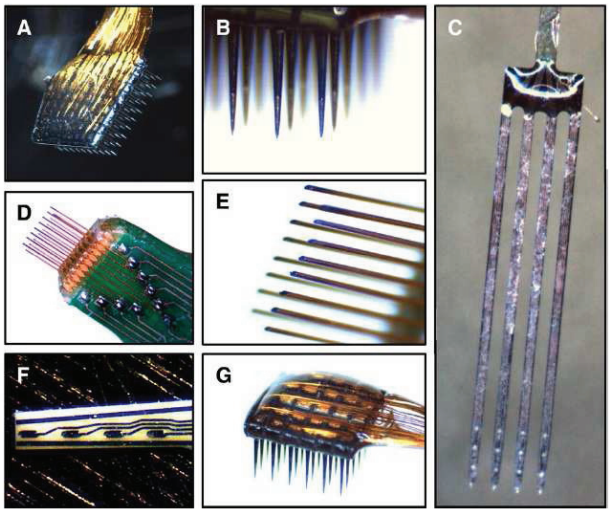


Figure 2.6 Silicon based microelectrodes from Cyberkinetics [38].

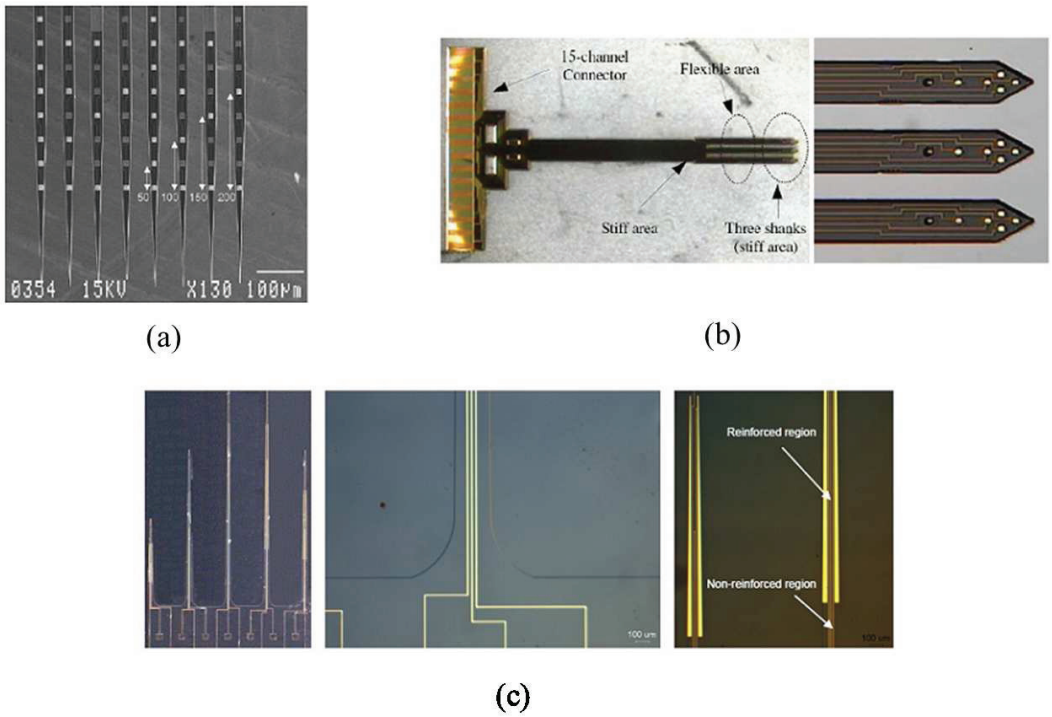


Figure 2.7 (a) Silicon on insulator (SOI), (b) Polymar based and (c) Micralyne MEAs [36].

on insulator (SOI), polymar based and Micralyne MEAs.
For our system, we have used a novel high-density silicon based platinum-coated microelectrode array designed by one of the Polystim Laboratory team members [40].

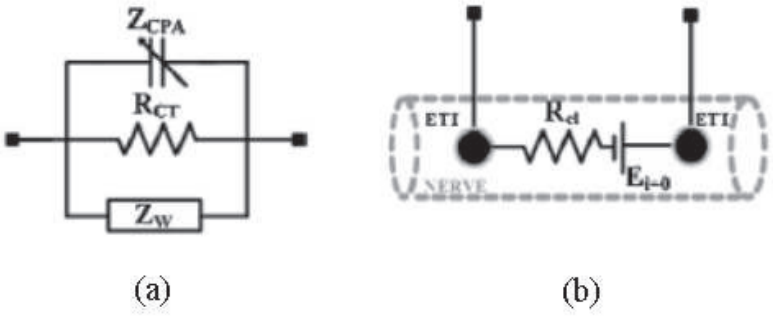


Figure 2.8 Equivalent circuit models for electrode-tissues interface (ETI) and ETI contacts: (a) ETI model, and (b) model of two ETIs and tissue contact. [41] © J. Biomedical Materials.

2.3.2 Equivalent circuit of electrode

The typical ETI model consists of the Warburg impedance (Z_w), a charge transfer resistance (R_{CT}), and a non faradic pseudo capacitance (Z_{CPA}), connected in parallel as presented in Figure 2.8(a) [41]. The Warburg impedance (Z_w) represents the diffusion of ionic components at the ETI interface and is expressed as follows:

$$Z_w = \frac{\sigma}{\sqrt{\omega}}(1 - j) \tag{2.2}$$

where σ is the diffusion coefficient, which is determined by the ion specie concentrations resulting from oxidation-reduction reactions close to ETI interface and the effective contact area.
The second component, R_{CT}, in the ETI model represents the exchanged current near the ETI. It is a function of the injected stimulation current magnitude through the electrode and the developed voltage across the ETI interface. This component has been included in order to take the DC current through the interface into account.
Also, Z_{CPA} indicates the inhomogeneous area of contact:

$$Z_{CPA} = \frac{1}{(j\omega C_{dl})^{\beta}} \tag{2.3}$$

where ω is the angular frequency, β is the deviation index from a pure capacitance, and C_{dl} is the double layer capacitance.
Figure 2.8(b) shows the case, when two ETI models are in contact with tissue. Here, in between two ETI models, an electrolytic resistance, R_{el} is connected in series with an electrode potential E_i. Where, R_{el} is the electrolyte resistance of the tissue. E_i is 0 due to same area for the two contacts and the same materials used for them.
While performing in-vitro test, usually 0.9 % NaCl solution is used to represent the tissues and R_{el} is substituted by ohmic resistance R_Ω.

2.4 Visual system

The complex visual system in humans extends from the retina to the visual cortex, a part of the cerebral cortex of the brain, located in the back of the brain. The anatomy of human visual system is presented in Figure 2.9 [22]. At the beginning, the visual information is processed by the retina, located at back of the eye. Retina is primarily composed of three layers, photoreceptors, bipolar neurons and ganglion cells, each of which has specific functions. Light information propagates from the photoreceptors to the bipolar cells and passed on to the ganglion cells. In the end, light is converted into nerve spikes. The axons of retinal ganglion cells meet together at a point, called the optic disc which is the beginning of the optic nerve. All axons of retinal ganglion cells exiting the optic disc form the optic nerve. Most of the (90%) of the axons in the optic nerve reaches the lateral geniculate nucleus (LGN) cells in the thalamus. Some axons carry information to the superior colliculus in the midbrain to control eye movements, called saccades [42] and other motor responses.
The next part of the visual pathway is the optic chiasm, located at the base of the hypothalamus of the brain. At this point, two optic nerves (from both eyes) cross each other, information propagating from two eyes is merged and next, segregated based on the visual field. The information from the right visual field is carried through the left optic tract and information from the left visual field is transmitted through the right optic tract. Both optic tracts end to the LGN cells.
In human, the LGN is composed of six layers, 1-6. Layers 1, 4, and 6 project information from the temporal visual field (nasal retina), and layers 2, 3, and 5 project information from the nasal visual field (temporal retina). The neurons in it relay the visual image to the primary visual cortex (V1) through projections called optical radiation. The LGN also processes received reciprocal innervation from the visual cortex, and reciprocal input from the cortical and subcortical layers.

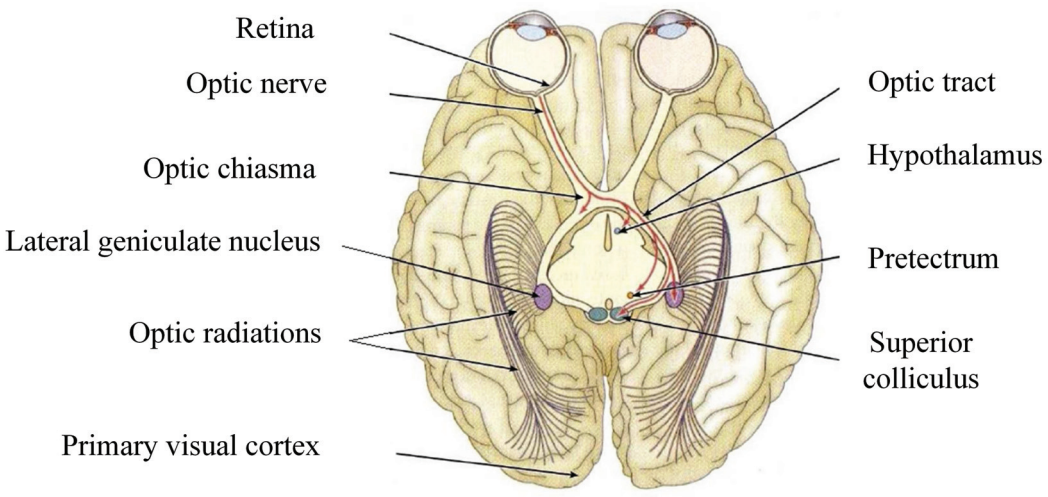


Figure 2.9 Modified version of the anatomy of the human visual system [22].

2.5 Primary visual cortex

The visual cortex is composed of several dozen areas which perform treatments such as spatial positioning, cognitive and associative recognition of objects or simple treatments, such as the analysis of color and orientation. We consider here only the primary visual cortex, called striate cortex or V1.

V1 area has a total thickness of 2 mm and is the entry point which accomplishes the complex processing of visual information [43]. Being located in the posterior occipital lobe, the primary visual cortex consists of different types of neurons such as pyramidal cells and stellate. V1 area is partitioned into six layers, where each one has a distinct structure and functions. Study of the neuronal connections among these layers and between other areas shows that the signals originated from the LGN cells enter the visual cortex through layer 4 of area V1. The sub-layer 4C of this layer has the significant role in the treatment and progression of visual information. Afterwards, the processed information is projected to layers 2, 3 and 5, furthermore, feedback is also provided to the LGN. To perform more advanced information processing, these layers retransmit the signals to the neighbouring areas.

Figure 2.10 shows this arrangement of columns in the primary visual cortex. The layer 4C, the ocular dominance columns are evenly segmented forming alternating bands of about 0.5 mm wide. Next, in the direction orthogonal to that of the ocular dominance column, the orientation columns are spread. Neurons in each orientation columns are electrically excited depending on the orientation of the light stimulation. It has been validated experimentally

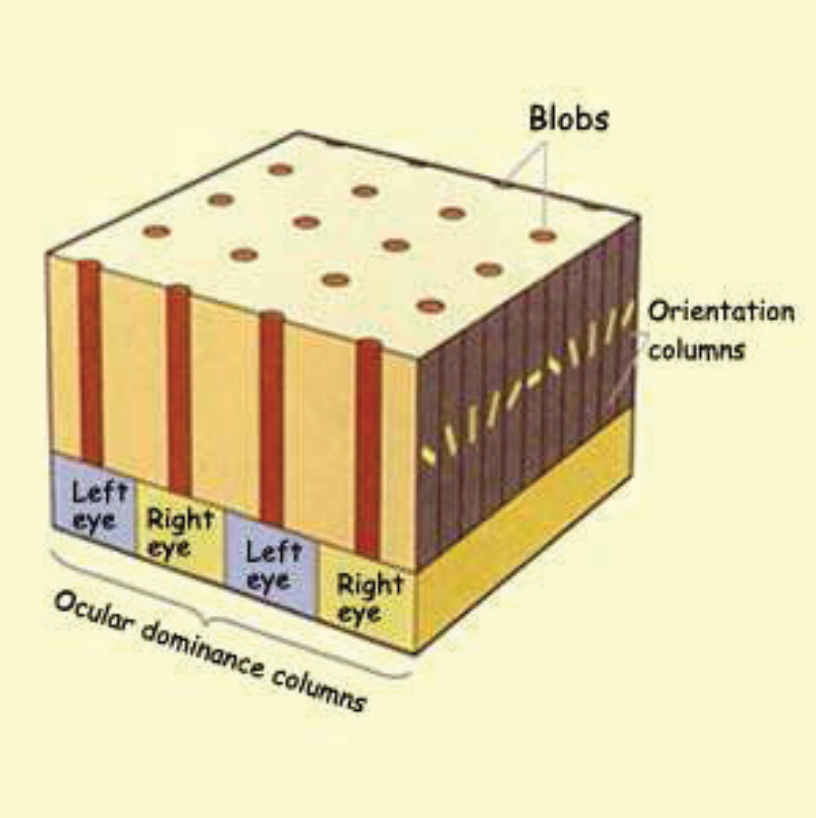


Figure 2.10 Organization of the columns in the primary visual cortex (Cortical module) (McGill University, 2009) [43].

that 1 mm on average covers 180° orientation. In the end, stains which are the cylindrical pillar shaped column elements, gather and process color related information. The schematized cortical module, presented in Figure 2.10, illustrates a block of 2 mm x 2 mm which includes four ocular dominance columns covering orientation range of twice of 180° and 16 cylindrical stains.

2.6 Neuron

The anatomy of a typical neuron, the primary element of the nervous system, is shown in Figure 2.11 [44]. Nerve spike, called the action potential, is generated in it and propagates within itself as well as to the neighbouring neurons.

Each neuron consists of dendrites, soma, axon, nucleus cytoplasm, myelin sheath, ranvier nodes, and terminal buds. The dendrites receive nerve impulses, which is transmitted through axon. The terminal buds, located on the other end, transmit nerve pulses to other neurons.

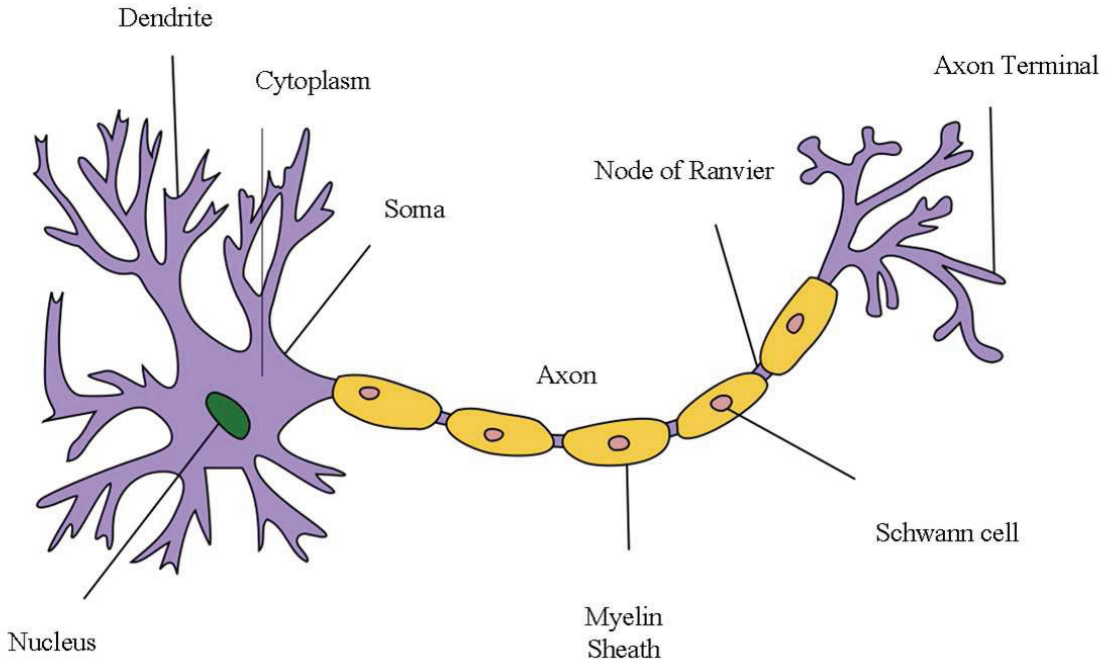


Figure 2.11 The anatomy of a neuron (modified version). © [44]).

Neurons communicate with each other through synapses. However, this synaptic connection between two neurons is a narrow space. Signals from one neuron to the next is transmitted through this narrow space in the form of biochemical agent, called neurotransmitters. On the arrival of nerve impulses, neurotransmitters are released by the terminal buttons of the first neuron. Upon collection of neurotransmitters by the dendrites of the receiving neuron, nerve pulses are regenerated and converged to soma, which is the center of the receptor neuron. Afterward, soma transmits the nerve pulses through the axon. Some neurons have myelin insulating sheaths, composed of glial cells, surrounding their axons. Action potentials travel faster in myelinated axons compared to unmyelinated axons of the same diameter. The myelin sheathing travels around the axon and is segmented in a number of sections of about 1 mm long. Between each section, the axon is uncovered, which is called nodes of Ranvier.

2.7 The cytoplasmic membrane

In generating and propagating the nerve pulses, cell membrane of the neuron plays a significant role. Like other cells in the body, it consists of a double layer of phospholipids, ions and low permeability layer molecules. Nonetheless, proteins that act as channels (protein channel) and as ion pumps, surface protein, integral protein, globular protein, glycoprotein

and peripheral protein travel across it. These proteins control the selective transport of ions between the extracellular and intracellular environments, allow smoother dissemination and secure self-regulation of the cell. Major ions which participate in this bioelectric process are Na+, K+, Ca2+, and Cl-. The intracellular medium contains a higher concentration of potassium ions, whereas the extracellular medium generally contains a higher concentration of sodium ions and chlorine when the equilibrium is reached. Due to variation of concentrations of different types of ion in the extracellular and intracellular environments, a difference in electric potential is developed across the sides of the cytoplasmic membrane. This transmembrane potential is typically about -70 mV. Conventionally, it is known as equilibrium potential or neuron resting potential. A specific value of membrane potential defines the number of open or closed gates of various ion channels. Thus, this membrane voltage, and the mechanism of opening and closing of ion gates facilitate the generation of action potentials.

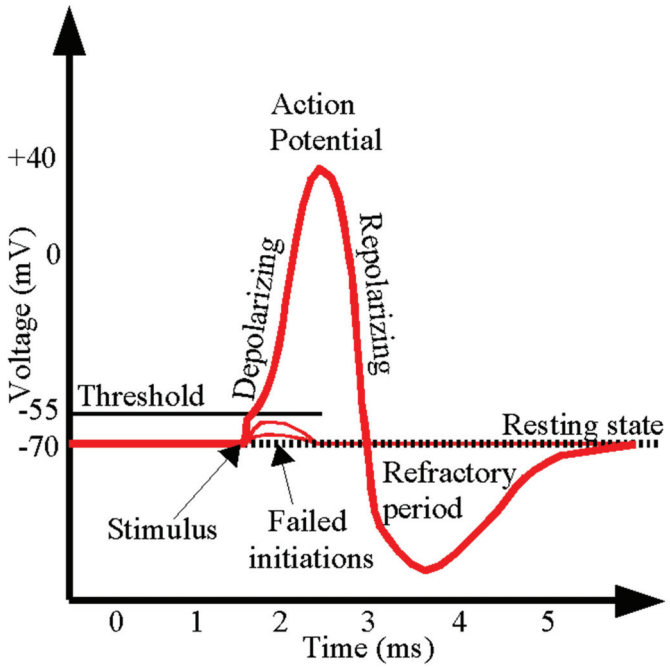


Figure 2.12 Principle of generating an action potential: Variation of the membrane potential with time © [44].

2.8 Action potential

The electrical potential balance of the neuron can be disturbed by some factors. Regarding sensory neurons, changes in parameters such as light, pressure and temperature alter the physical environment, causing fluctuation of internal potential. A nerve impulse, received from a neighboring neuron, causes disruption of internal potential as well. An external electrical stimulation, applied to the neurons, gives rise to a local variation of extracellular potential.

The electrochemical imbalance in neural cell developed by aforementioned factors changes transmembrane potential. The regular excitation threshold is about -55mV. No excitation occurs, if the transmembrane potential is kept below the threshold value, that is to say that the process of ion transportation and diffusion remains in equilibrium condition. On the contrary, spike is triggered or action potential is generated, if membrane potential exceeds the threshold value. The magnitude and width (duration) of the action potential do not depend on the intensity of the stimulus.

The trigger mechanism of an action potential is presented in Figure 2.12 [44]. In the first phase, the membrane potential is of -70 mV and the neuron is in equilibrium condition (phase 1 or initial phase) as illustrated in Figure 2.12. A subsequent injection of a stimulation signal increases the membrane potential above the threshold value. Next, local depolarization of the membrane of the neuron begins, which leads to the second phase (phase 2). In this stage, the opening of the gates of sodium channels allows a large amount of Na+ ions to influx inside the cell, causing a sudden rise in the transmembrane potential. Next, the repolarization phase (phase 3) begins when the action potential reaches its peak value of about 35 mV. A large volume of K+ ions outflows to the extracellular medium as one of two gates of the sodium channels closes and the gates potassium channels open. Consequently, the membrane potential drops in this phase. The final phase (phase 4) is hyperpolarization of cell membrane, when membrane potential decays below its equilibrium value. During this period, the internal membrane potential of the neuron is balanced by pumping out Na+ and pumping in K+ ions.

The rate at which an action potential is triggered is called its firing frequency which has a limit. The membrane remains insensitive to extracellular potential for a certain period, called refractory period, shortly after the onset of an action potential. This mechanism prevents the generation of second action potential immediately after the first spike owing to the hyperpolarization phase of the membrane. This mechanism of ion channels in a membrane cell while triggering an action potential is presented in Figure 2.13.

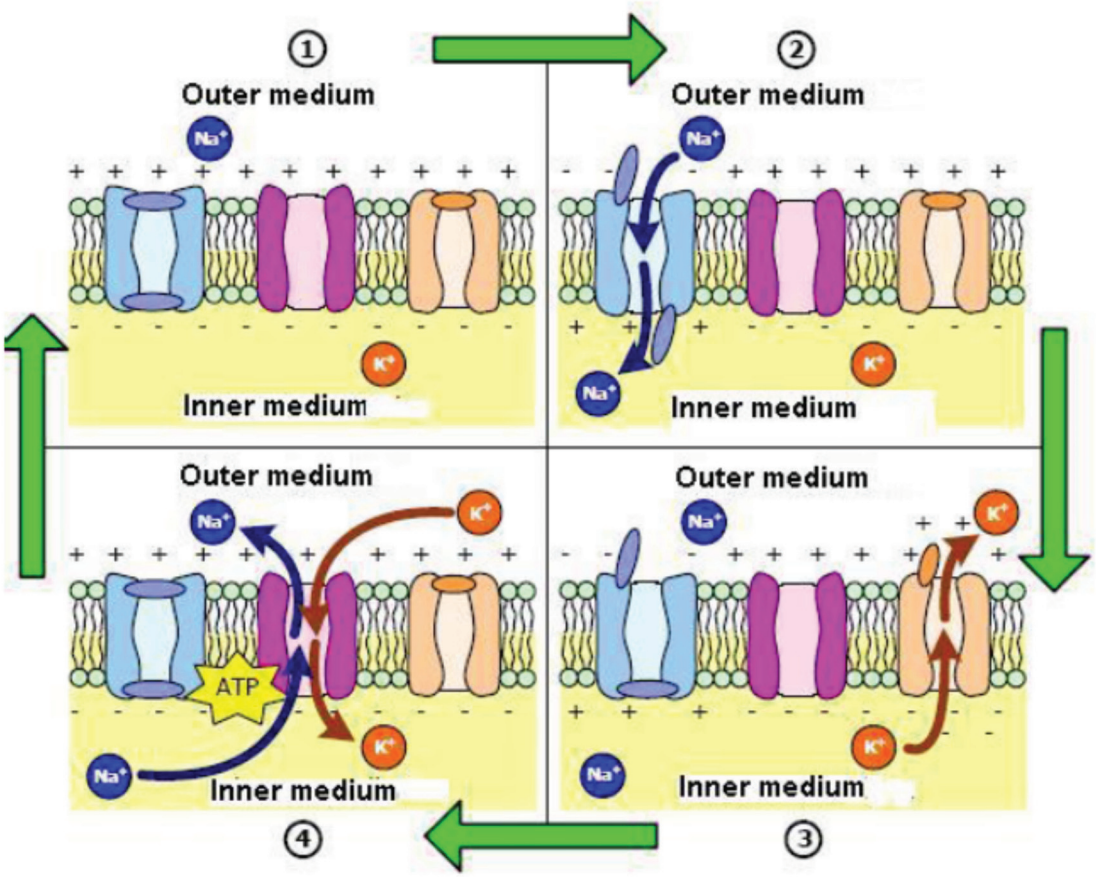


Figure 2.13 Mechanism of ion channels in a membrane cell while triggering an action potential © [44].

2.9 Propagation of an action potential

Upon generation, the action potential needs to traverse through the nervous system to perform the desired task. The propagation of the action potential along the axon, shown schematically in Figure 2.14, can be explained by the theory of the cable [45]. In brief, ionic current is controlled by the intra- and extracellular environments. The membrane potential at a point A is changed, once the action potential is triggered there. During depolarization, intra- and extracellular ionic currents flow from point A to point B due to the potential difference between these points. During this process, membrane B is depolarized by these ionic currents. Another action potential is triggered at point B if the intracellular potential reaches its threshold value. Membrane C also experiences this phenomenon, which continues throughout the axon.

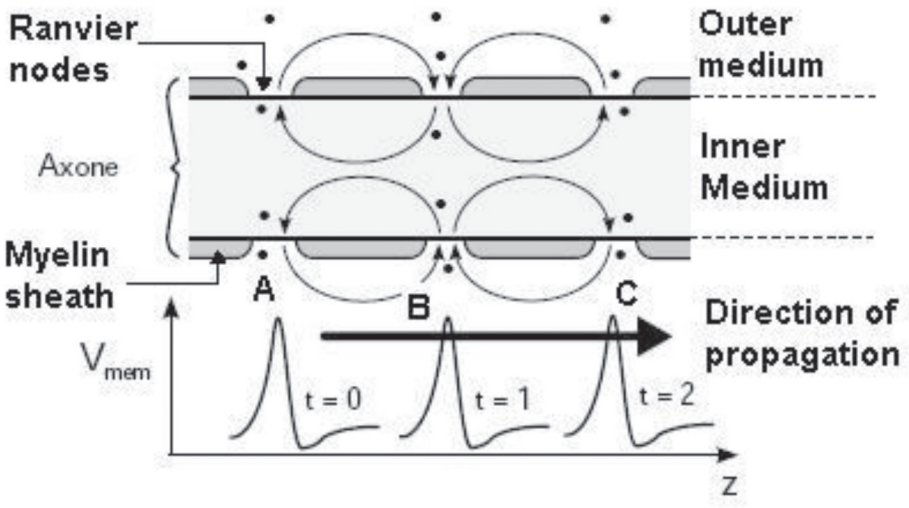


Figure 2.14 Action potential propagation along the axon of a myelinated neuron © [44].

2.10 Conclusion

In this chapter, we discussed the principle of FES and the associated parameters, different types of interfacing device (electrodes) to apply the stimulation signal, and physiological basics required to investigate the specifications and accordingly, to build an intracortical microstimulation system.

CHAPTER 3

LITERATURE REVIEW AND OVERVIEW OF THE PROPOSED VISUAL PROSTHESIS

3.1 Introduction

In this chapter, we present related works on the state of the art in stimulating different locations of visual pathways. We, next, illustrate relevant works previously done by various research groups to build a functional visual prosthetic device. Emphasis is given mainly on simple and advanced existing intracortical visual prosthetic devices. However, a brief summary of implants built to stimulate other locations in visual system is included here as well. We rationalized the pros and cons of each developed system from implementation and application perspectives. Next, on the basis of the literature review and performance comparison of the previously developed prototypes, the research questions are formulated, accompanied by the general and specific objectives, and original research contribution. The schematic of the proposed system is presented in the end of this chapter.

3.2 FES based prosthetic approaches to restore sight

Blindness is a serious dysfunction that may be caused by some diseases that affect the ocular structures, such as age related macular degeneration (AMD), glaucoma, and retinitis pigmentisa(RP) rendering eyes insensitive to light. In RP and AMD, blindness results from the total destruction of photosensitive cell layer keeping the rest of the other cells in the retina and the remaining part of the visual pathways alive. The visual function can be restored partially using microelectronic-based prosthetic devices. Until now, most of the visual prosthetic devices use electrical microstimulation through an array of microelectrodes for generating phosphenes in the form of perception of light in the visual field. The locations for effective restoration of sight are the retina, the optic tract, the optic nerve, the optic radiation, the dorsal lateral geniculate nucleus (LGN) of the thalamus, and the primary visual cortex [22]. Each of these approaches has some advantages and drawbacks. Two widely projected techniques to restore vision are retinal- and intracortical- implants.

3.3 Retinal implant

Retinal implants [46] are used to treat only those diseases where the optic nerve and the central visual pathways remain undamaged. Research shows that visual sensation can be produced through electrical stimulation of retinal bipolar and ganglion cells. Henceforth, patients suffering from RP and AMD can benefit from this implant [46], [47], [48], and [49]. Figure 3.1 shows two approaches of retinal visual prostheses (Epi- and Sub-Retinal implants)

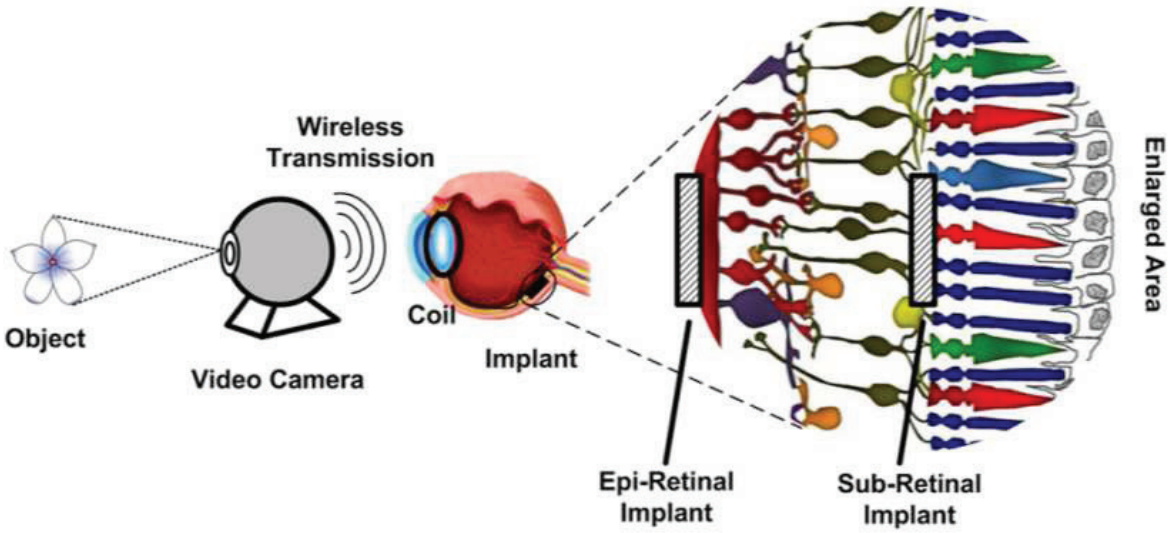


Figure 3.1 Epi- and Sub-Retinal visual prostheses [50]. © Journal of Ophthalmic and Vision Research.

[50]. However, retinal approach, irrespective of its type, has some general disadvantages. This procedure imposes weight restrictions on implanted device to prevent any damage at the retina caused by the large acceleration forces due to the eye movements, lacks high resolution because of the limited space available for the implant, requires complex connection to energy- and data- system, and has binding problem. The advantages are: the surgery procedure for this approach is entirely extracranial and there is an even mapping of retinal surface to the visual space.

In retinal prostheses, artificial means are used to elicit phosphene in the visual field. Light energy is detected and transformed into an electrical signal, which is applied to the retinal neurons other than photoreceptors. Two major retinal stimulators are the epi-retinal and sub-retinal implants depending on the location of stimulating electrodes [51]. However, electrodes can also be placed inside the optic nerve head and suprachoroidally. To lay the foundation for an implantable retinal microstimulator, all approaches, other than the sub-

retinal approach, began short-term (acute) stimulation, involving temporary insertion of a stimulating electrode in the eye of blind test subjects. On the other hand, an acute placement of electrodes for sub-retinal stimulation was not carried out due to the complex surgical procedures required for accessing the sub-retinal space.

3.3.1 Epi-retinal implant

The advantages of the epi-retinal implant are: (1) uncomplicated implantation procedure and deployment of the implant on epi-retinal surface does not segregate the retina from choroid and retinal pigment epithelium. (2) heat from the microelectronic device can be dissipated to the vitreous [52], [53]. Disadvantages of this approach include: (1) need of surgical procedure to attach the implant to the inner retina for extended period of time [54], [55], and (2) advanced image processing algorithm emulating retinal function is required to stimulate at the output of the retina (ganglion cells) [56].

Weiland et al. designed one of the epi-retinal prosthetic device to interface 1000 individual

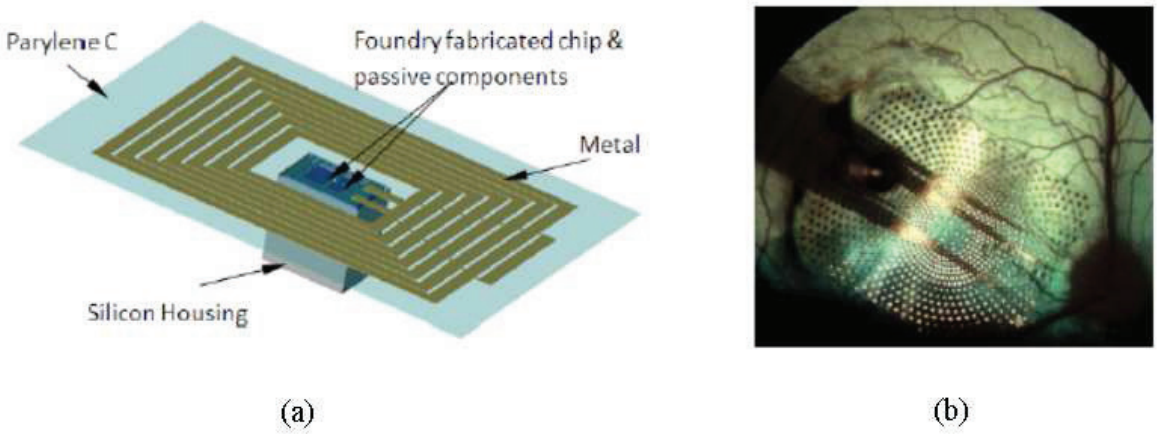


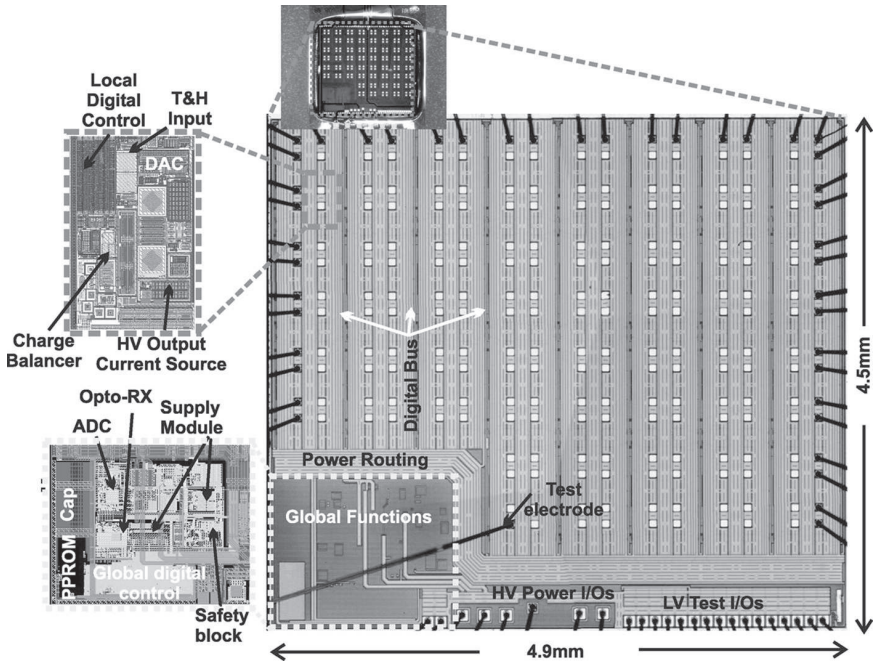
Figure 3.2 (a) Diagram of coil and chip packaged using CL-I2. (b) Implanted 1000 electrodes with Parylene substrate on retinal surface. Area of electrode array is 5mm x 6mm [57]. © IEEE.

electrodes to restore visual function of blind individuals [57], [58], [59]. Dual band telemetry system was employed to transmit power and data via inductive links [57]. The receiver coils, with dimension of 2cm x 2cm each, are positioned in the front half of the eye; the ASIC module was placed in the vitreous cavity; and an electrode array was implanted on the epi-retinal surface, located at the back of the eye. To control the implant, an external system, consists of an image acquisition device (camera), image processing hardware, data

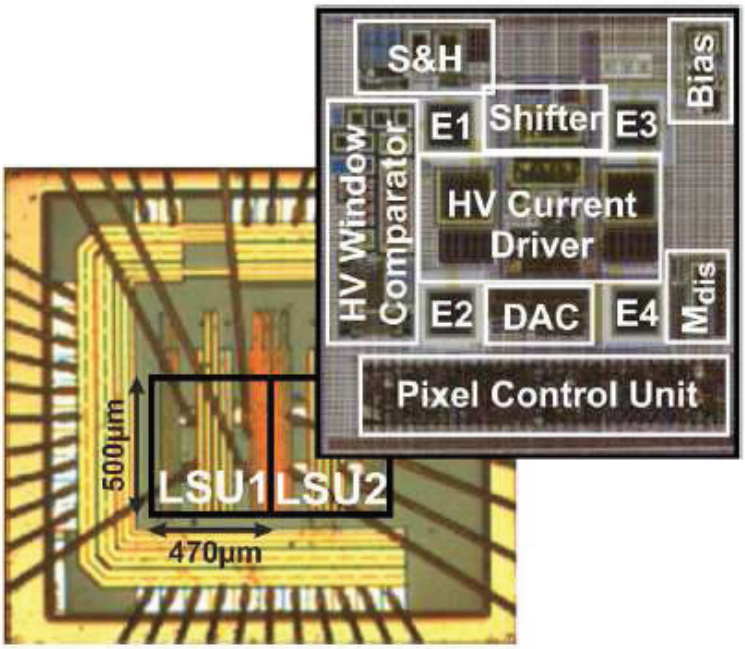
modulation scheme, and a power amplifier were included. The authors' have stated the need for compliance voltage of 9V for monophasic and 18V for biphasic stimulation across microelectrode. However, they did not provide adequate information on the technology, used to design the implant. Moreover, to block the DC voltage level across microelectrode-tissue interface, no biphasic supply rails were used in the output stage. Figure 3.2 shows (a) the diagram of packaged chip and coil, and (b) implanted 1000 electrodes on retinal surface.

M. Ortmanns et al. and recently E. Noorsal et al. designed two stimulators for epiretinal stimulations [60], [61]. The first one was featured with 232 channels with a maximum of 116 parallel stimulations and the latter stimulator is intended to stimulate 1024 electrodes. In both cases, they considered Platinum black electrode with impedance of about 10kΩ. They considered optical data transmission to transmit data at 1 and 2Mbps respectively in two cases. However, the power was transmitted over the inductive-link with the carrier frequency of 13.56MHz. The maximum stimulation current per output channel was 1mA. The stimulators were designed in AMS 0.35μm HV CMOS process to solve the high-voltage compliance required in the output stage, which is 20V for the specified ETI impedance and stimulation current. Nonetheless, a single HV supply which is greater than 20V was used in both designs rather than using biphasic supplies and biphasic stimulation was performed around a common-mode voltage. The drawback of this design is their use of additional charge balancing techniques to cancel the developed DC offset at the ETI interface. These techniques serve the purpose but consumes extra power. Moreover, the data rate in the later case is limited to 2Mbps only. Figures 3.3(a) and 3.3(b) show the fabricated chips for epi-retinal stimulation by this group.

One most recently designed microstimulator for retinal visual prosthesis is reported in [62]. The authors presented the design of a stimuli-generator, along with a high-voltage output stage, in IBM 130-nm 1.2/3.3V CMOS technology up to the post-layout simulations. No specific information is provided regarding the number of channels. This system is featured with a flexible current-mode stimuli such as constant, and rising- and falling-exponential pulses. The maximum deliverable stimulation current was $\pm$96μA with voltage headroom capability of $\pm$3V in the output stage, to cope with the needed voltage across ETI interface of only 30kΩ. Pelliconi charge pump circuit was used to up convert 1.2V to $\pm$3.3V on-chip. The positive features are: (1) the design is fully integrated and (2) the system is equipped with on-chip DC-DC up converter. However, the drawbacks are: (1) rising and falling exponential pulses have been found to be not energy-efficient in later studies, (2) integration to electrode is not addressed, and (3) the system has not been validated through experimental results.



(a)



(b)

Figure 3.3 (a) Photograph of the retinal stimulator chip: Assembled ASIC on polyimide foil, layout of local stimulation pad cell designed for two electrodes, and layout of the global stimulator. (b) Local stimulation unit (LSU): Chip photograph and floor plan [61]. © IEEE.

3.3.2 Sub-retinal implant

The second category of retinal implant, sub-retinal implant, benefits of remaining close proximity to bipolar cells, the next surviving layers of neurons in the visual pathway [50], [63], [64]. A significant retinal processing in order to generate useful neural response can be achieved through stimulation at the bipolar cell level. Regarding stability in placement, attaching an implant in the sub-retinal space might be better choice than securing it to the epi-retinal surface. This approach also allows the retina to hold the electrode [63]. The drawbacks of this method are: (1) probability of thermal damage to neurons, due to the nearness of the retina to the electronics, hence restricting the thermal budget of the implant, (2) tight sub-retinal space to fix the device, (3) tethering effect on the cable passed across the sclera, in case, only an electrode array is implanted in the sub-retinal space keeping the electronics outside the eye [65], and (4) chance of sub-retinal hemorrhage and local or total retinal detachment due to this cable.

Kelly et al. have designed a wirelessly controlled, hermetically encased, and miniaturized subretinal implant and performed preclinical studies in the Yucatan minipig [46]. The implant included a 15-channel stimulator chip and discrete circuit components, contained in a hermetic titanium case and a microelectrode array, microfabricated from thin-film polyimide array of sputtered iridium oxide film (SIROF). The various parts of the implant are shown in Figure 3.4. The stimulator chip was connected to the electrode array in the subretina, and to secondary data and power receiving coils on the eye via feedthroughs in the case. To

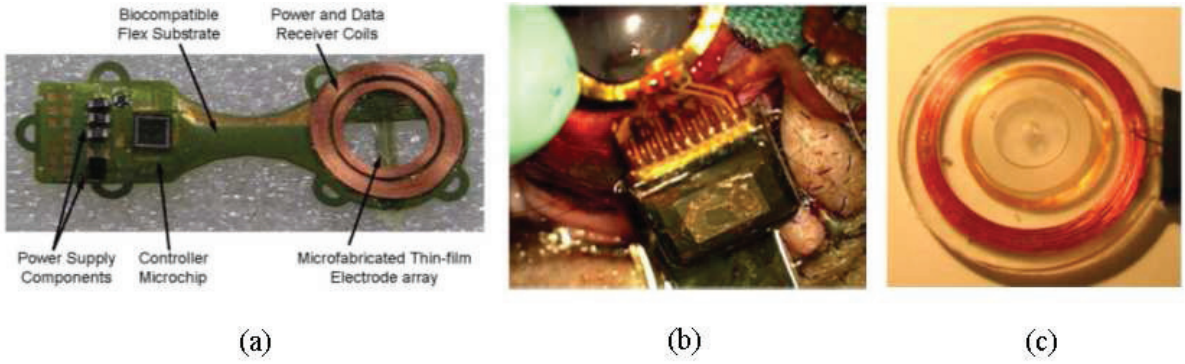


Figure 3.4 (a) Developed first-generation retinal prosthesis by [46]. (b) An actual hermetic prosthesis implantation onto a minipig eye through surgery. (c) PDMS potted primary coils. © IEEE.

nullify the DC voltage level across microelectrode-tissue interface, the rectified supply voltage was set to ±2.5V. The achieved driving voltage across electrode was 0.85 ± 0.03V owing to

low resistive impedance of employed SIROF coated electrodes. The wireless operation of the system was validated through in-vitro tests in physiological saline using custom primary coils and a RF transmitter. Chronic implantation of the retinal implant in two pigs was performed for up to five and a half months to verify the system.

Another category of sub-retinal approach emulates the function of degenerated photoreceptors by implanting a microchip designed using photodiode array under the transparent retina. The photodiodes convert the incident light into electrical current, which is delivered to the retina [49]. The major advantages of this approach, compared to two previous cases, are: (1) no need for additional image and data processing electronics circuitries, (2) fewer components, and (3) easy placement. The disadvantages are: (1) insufficient current generated by photodiodes to stimulate the neighboring neurons using only the incident current and (2) damage of the retina in terms of obstruction of blood flow from the retina or pigment epithelium separation from the placement of photodiode array.

In summary, compared to other types of visual prosthesis, retinal implant approach is less invasive [66]. However, this method can not be used to treat the major diseases of the retina and optic nerve, when both of them are completely or significantly damaged [66], leaving no choice other than using visual intracortical approach.

3.4 Optic nerve microstimulation

The optic nerve with diameter of about 1–2 mm contains all the visual information. Activation of a large section of the visual field can be expected through electrical stimulation of a small area of the optic nerve [67]. As presented in Figure 3.5, usually, electrical stimulation current is delivered via a cuff electrode surrounding the optic nerve. Capturing real-time

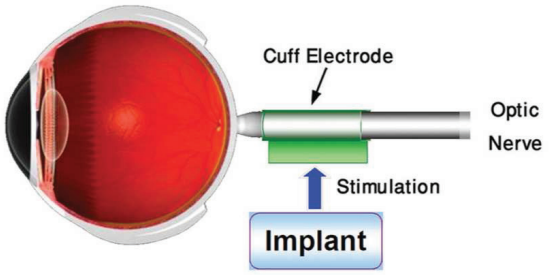


Figure 3.5 Visual prosthesis using optic nerve stimulation [50]. © Journal of Ophthalmic and Vision Research.

image and processing it, and transmitting data and power through a telemetry link to the electronic implant are required in this approach. It is extremely challenging to achieve focal

stimulation and high resolution, as the electrodes are placed around a very densely packed nerve, containing about 1.2 million fibers [68]. Compared to retinal approaches, more secure and straightforward implantation can be performed in this case. This method of generating specific vision pattern is still unclear due to limited information on the functionality of each individual fibre within the optic nerve and technical challenge in achieving focal stimulation [69]. Veraart et al. applied this approach on a blind volunteer with retinitis pigmentosa in an effort to justify their reasoning of using optical nerve stimulation for the design of a visual prosthetic device [67], [70].

3.5 Visual prosthesis using cortical microstimulation

The third approach, based on cortical microstimulation, encompasses a large number of diseases to treat and this advantage has made this approach attractive in visual prostheses. Stimulation can be performed either at the surface of the cortex, called cortical stimulation or at a specific depth in the primary visual cortex with penetrating electrodes, called intracortical stimulation.

3.5.1 Early works on visual cortex and intracortical microstimulation

It is known, since the 1960s, that injecting electrical stimulation locally to the visual cortex elicits phosphenes. Many research teams, such as Brindley and Dobelle were drawn to the concept of developing a visual prosthetic device to facilitate reading and travelling for the blind individual [71], [72]. They, first, characterized the generated phosphenes through the locations of the electrodes on the occipital lobe and the applied stimulation parameters. The inception of visual prostheses research began from their pioneering work. Their investigations found the major restrictions of this approach, specifically surface mode stimulations, such as (i) the minimum threshold current required to generate phosphenes, which is of the order of mA, (ii) precise focal stimulation due to diffusion of current to the neighboring neuron, and (iii) difficulty in control.

In case of intracortical implants, a large number of electrodes can be implanted in the primary visual cortex due to its large physical extent, thus allowing the restoration of a very high resolution visual function. Intracortical implants also provide high tolerance for the chronic low-grade heating effects while performing microstimulation. Two major difficulties are the complex implantation surgery due to the location of primary visual cortex and uneven mapping of the intracortical microstimulation pattern to the visual field.

Advanced experiments with penetrating microelectrodes were performed on sighted subjects [73] and a blind about 22 years old [74], more than two decades later. Their discoveries

showed that the required amplitude of threshold current to give rise to phosphenes are 10 to 100 times lower than that with surface level stimulation, of the order of few tens of microamperes. Moreover, the phosphenes were well shaped and more stable. Schmidt, besides quantifying the effect of stimulation parameters, also observed continuous phosphenes from the injection of pulse trains. The standard of spacing of 500 μm between two electrodes to exhibit two distinct phosphenes in the visual field is also established by Schmidt et al. Their experiments and analyses of the results on the effects of stimulation parameters on elicited phosphenes in a blind human subject remain one of the main references [74].

3.5.2 Progress in physiological experiments

The effects of chronic implantation of a large number of microelectrode arrays in the striate cortex of V1 area were not considered in previous studies. A sequence of experiments with a 10 x 10 microelectrodes array (MEA), spaced 400 micron from each other, were performed on cats by Normann's team at the University of Utah [66], [75]. This biocompatible microelectrode array used for these experiments is illustrated in Figure 3.6. The MEA is made of silicon and tips of microelectrodes are coated with platinum. Investigation of the cortex of

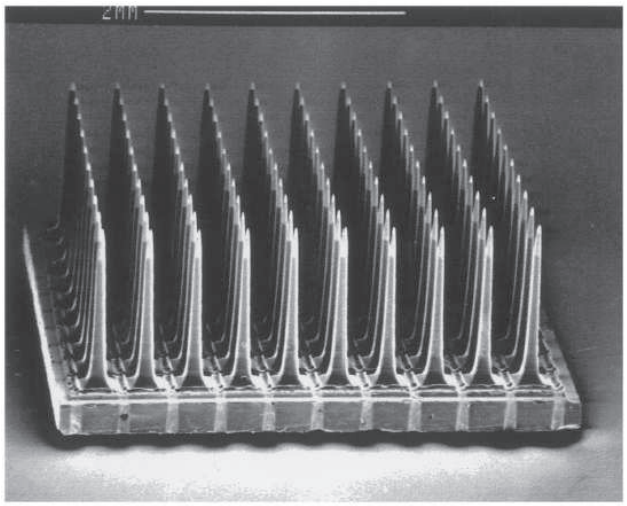
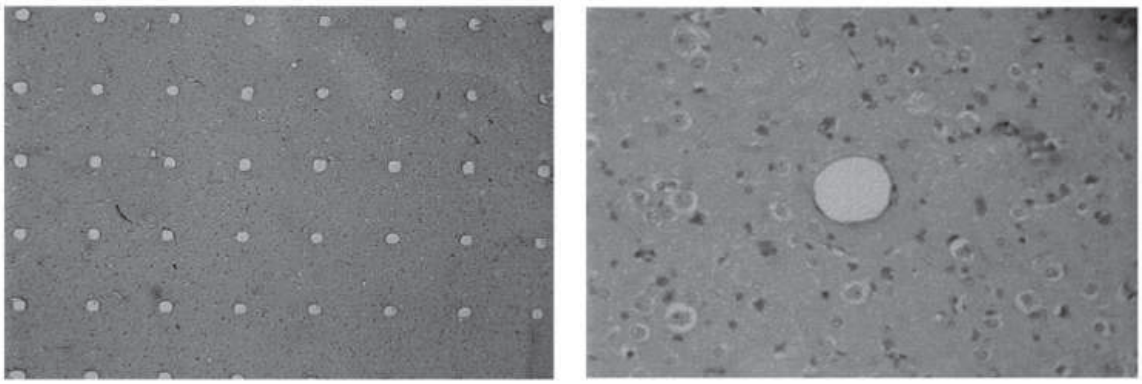


Figure 3.6 Silicon-based Utah electrode array, which includes 100 electrodes with length of 1.5-mm each and inter-electrode space of 400-micron. [66]. © Vision Research.

cats, after six months of implantation of MEA, showed deposition of fibrous tissue and gliosis at all implantation sites as presented in Figure 3.7. Electrodes were stressed and electrical impedance increased as a result of the reaction between tissues with the electrodes. In spite of this incidence, most of the implanted electrodes were yet able to stimulate and record for a period of up to three years [66].



(a) (b)

Figure 3.7 (a) Sections of visual cortex, stained with eosin and Hematoxylin and implanted for 6 months with a MEA. (b) Magnified version of one track. [66]. © Vision Research.

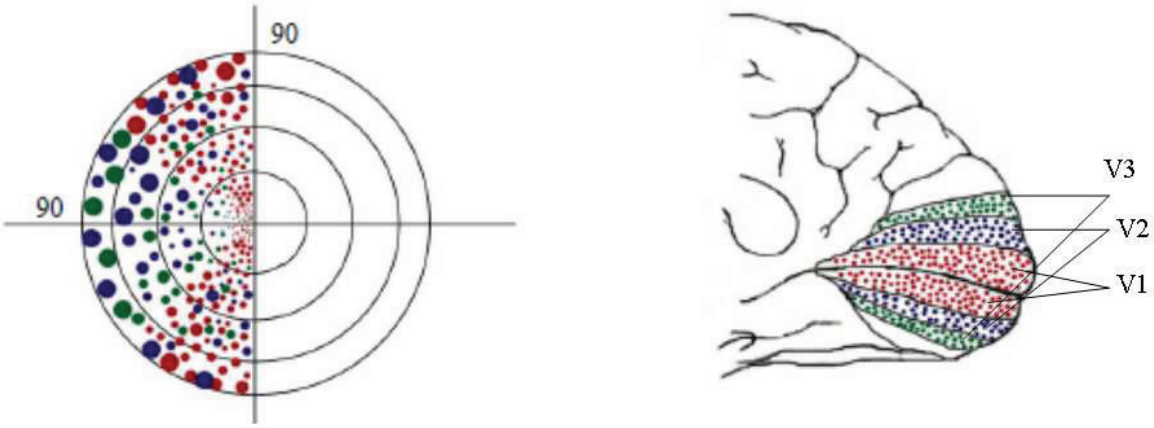


Figure 3.8 Expected visual map: when electrodes are implanted on V1, V2, and V3 areas. Corresponding phosphenes in red, blue, and green colours are shown on the visual space [78]. © IEEE.

Researchers also have studied the visiotopic mapping between the stimulation sites and the phosphene positions in the visual field [76]. Troyk at the Illinois Institute of Technology carried out in-vivo tests on monkeys and focused to locate the phosphenes in the visual field [77], [78]. The objective was to find the relationship between stimulation sites in the primary visual cortex and the location of generated phosphenes in the visual field. Figures 3.8 and 3.9 show expected visiotopic mapping of visual cortex. Their qualitative conclusions were very

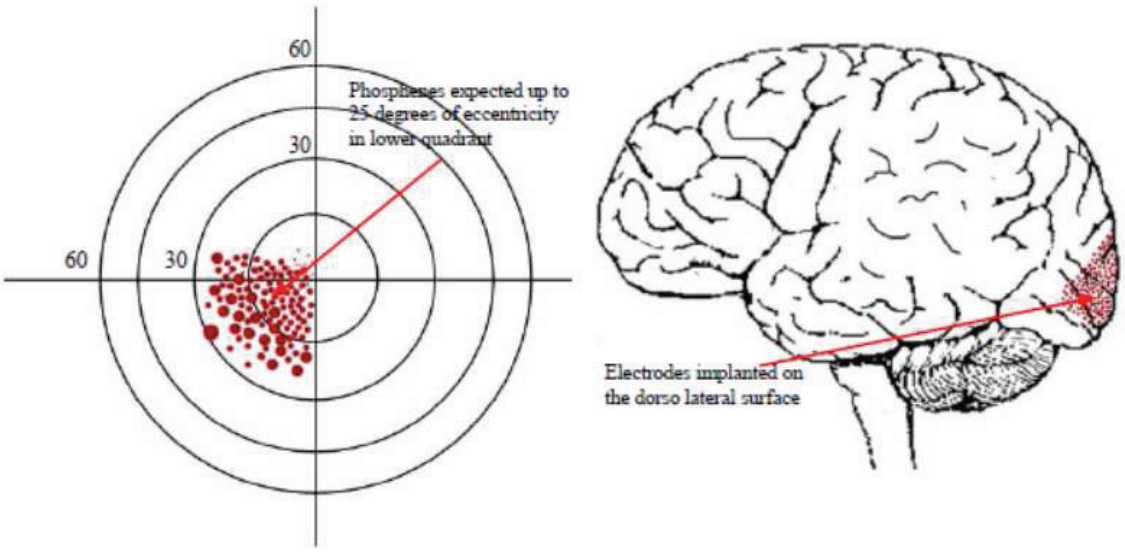


Figure 3.9 Expected visual map: when electrodes are implanted on the lateral surface area and within a radius of 3 cm from the occipital pole [78]. © IEEE.

encouraging, however, still more experiments and analyses are needed for complete understanding of this visiotopic mapping.

In spite of these progresses, there remain some disadvantages in visual intracortical prosthesis. Firstly, implanting this type of prosthetic device is invasive, reaching the V1 area of primary visual cortex is difficult and surgery may be complicated. Secondly, the quality of the perceived image can be limited as a certain amount of the natural processing of the visual stimuli is ignored. Thirdly, the visuotopic mapping for each blind subject may differ and therefore, this mapping for each user needs to be confirmed through in-vivo experiments. Because of the plasticity property of the brain, as some studies show in case of blind people, senses, such as hearing tend to retrieve from some areas of the occipital cortex. It is the plasticity of the brain for which visuotopic mapping can be changed as time passes.

3.6 General architecture of the visual intracortical implant

The outcomes of these investigations and progress in leading-edge microelectronic technologies have motivated several research teams to design the integrated microsystems with an aim to stimulate the visual cortex through wireless communication. Irrespective of the differences in different architectures with their own specifications, the fundamental functional blocks and their working principles are quite similar.

The typical architecture of an implantable visual intracortical microstimulator is presented

in Figure 3.10. Images are captured by a camera and the capturing frequency depends on

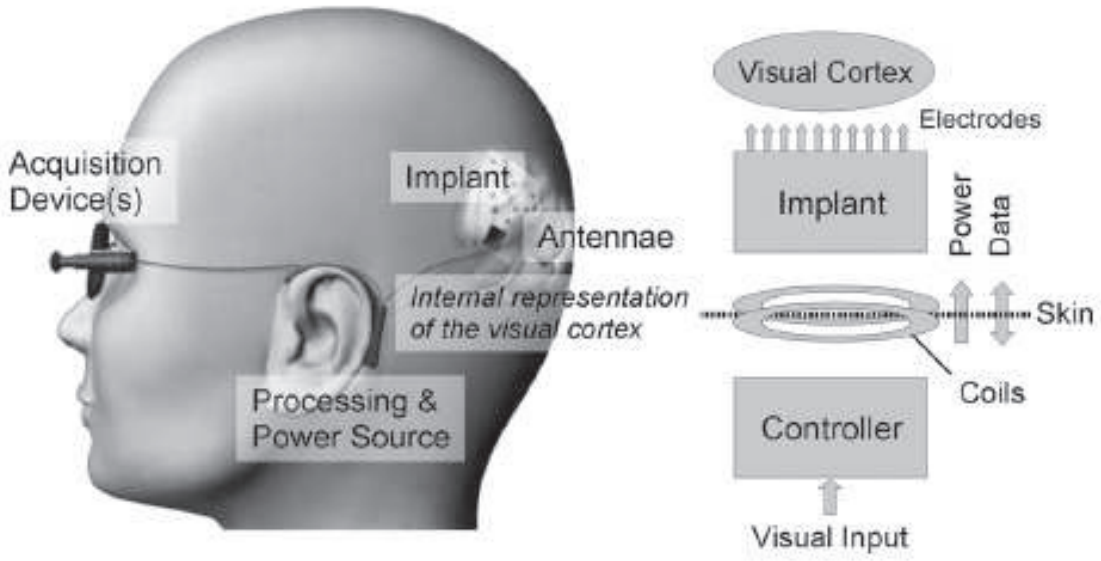


Figure 3.10 General architecture of a visual intracortical prosthetic device [22]. © IEEE.

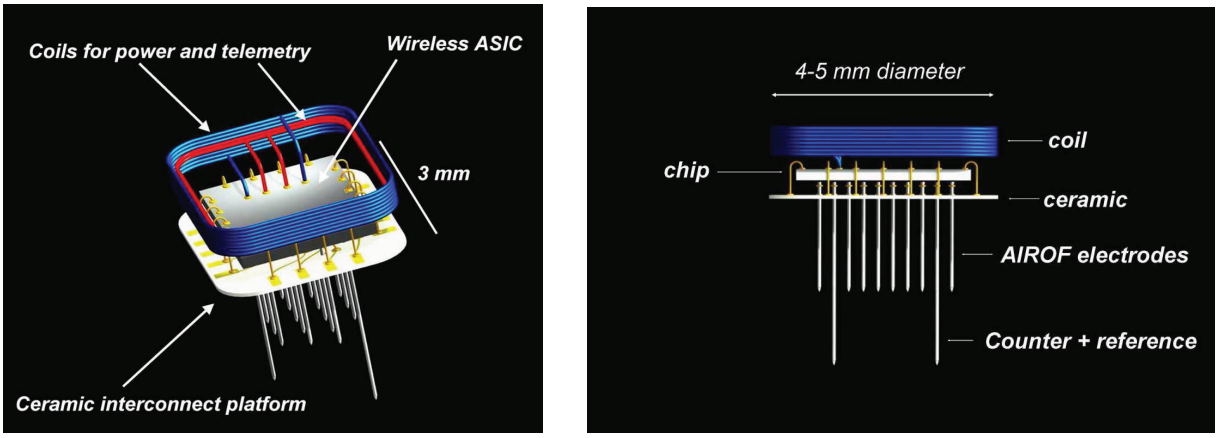
the consecutive processing time of the camera. A battery-powered external controller translates the acquired image frames into stimulation commands. In summary, the purpose is to simplify the image and retain only useful information which is comprehensible to the user. However, correlation between stimulation control commands and stimulation strategy in the V1 area needs to be established from visiotopic mapping.

An external transmitter modulates and transmits data through a wireless link to the receiver of the implant. The energy to power the implant is also transmitted through wireless link. In general, inductive RF wave is used to send both data and power. The RF link is needed to eliminate wired connections which can cause mechanical stress to the implant and infections to the skin. The receiver located in the implant recovers power (supply voltages) and demodulates the data. The internal controller receives and interprets the data, and controls microstimulators according to the received stimulation parameters and instructions. Microstimulator, usually, generates charge balanced biphasic current pulses, which are injected to the stimulation sites through microelectrodes, implanted in the primary visual cortex.

Several custom built architectures for intracortical microstimulation have been reported by various research groups. We review the most renowned systems from architecture perspective, and discuss their features, advantages, and limits in the following sections.

3.6.1 Implant developed by Troyk's team at the Illinois Institute of Technology

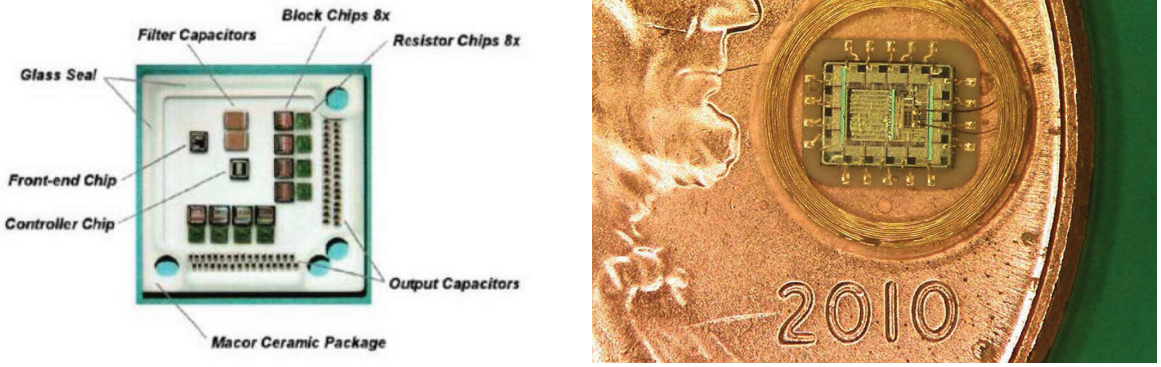
The first prototype, built by Troyk's team, was a 96-channel microstimulator to drive activated iridium oxide (AIROF) microelectrodes [79]. The system was designed to maximize the charge-injection capacity without jeopardizing the microelectrodes. However, all blocks of this system were designed using off-the-shelf components.
In a later version of their design, the team followed more integrated approach. In synchrony with their in-vivo experiments, they developed a 64-channel implant to stimulate 1024 neural sites [80], [81], [82]. The complete system was sub-divided into four identical implants, each one connected to 256 microelectrodes. Each implant was comprised of four sub-modules of 64 channels each. The amplitude of biphasic stimulation current ranged from 0 to 64μA with pulse duration of 0 to 750 microseconds. It is necessary to mention that only constant current pulse was considered in this design. The measured access resistance of employed AIROF microelectrodes were 71.4kΩ and 78.5kΩ while measuring their charge injection capacity through in-vitro and in-vivo tests respectively [83]. The output compliance voltage was within -0.6 and 0.8V with respect to Ag|AgCl reference electrode potential [84]. Wireless power and data communication were carried out via inductive link [85], and the circuits for data and power recovery units were implemented on a different stimulation chip. The different parts of the implant are shown in Figures 3.11 [81], 3.12 [81], and 3.13 [82]. From the



(a) (b)

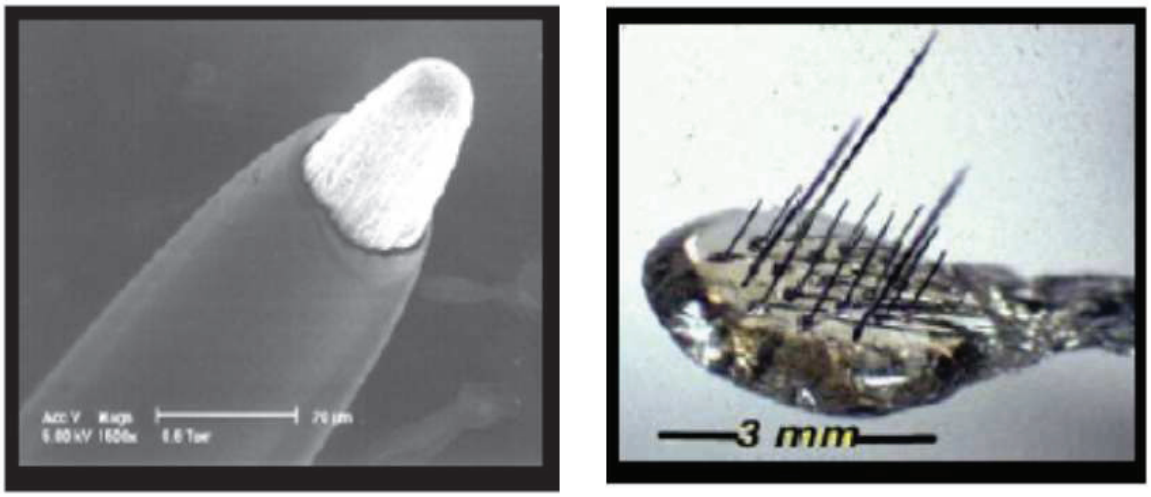
Figure 3.11 3D model of the implant: (a) top view and (b) side view. © [81].

perspective of architecture, the generated currents are very limited in amplitude. They also did not discuss about energy efficiency of a microstimulator considering other pulse types. The output compliance voltage was limited. However, needless to say that the stimulation they performed in the visual cortex is a pioneering work, which can always be a fundamental reference in the intracortical visual prosthesis research domain.



(a) (b)

Figure 3.12 Implant designed by the Illinois Institute of Technology's group: (a) Encapsulated 64-channels implant with various modules within it. (b) Real floating microelectrode array scaled with penny. © [81].



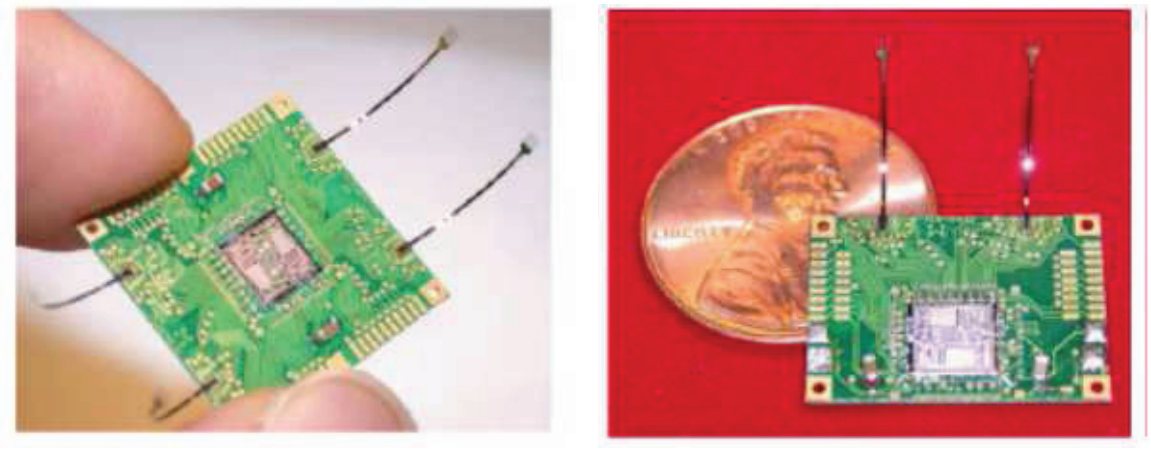
(a) (b)

Figure 3.13 (a) SEM image of one microelectrode tip. (b) Array of 16 microelectrodes [82]. © IEEE.

Recently, Troyk's team has proposed a new intracortical vision prosthetic device to collect an image which will be processed in realtime for generating stimulation patterns [86]. These patterns will be applied to the implanted microelectrodes to regenerate phosphene patterns in the visual field. In order to achieve this, they have developed some phosphene mapping methods with the aid of simulated phosphenes in sighted individuals [87]. Nonetheless, this exploration is still underway and no device has been realized yet to implement the concept.

3.6.2 System designed by Ghovanloo and Najafi at the University of Michigan

Ghovanloo and Najafi at the University of Michigan developed a 64-site microstimulator chip, called Interestim-2B [8], [88]-[91]. This chip consists of 16 current drivers, capable of supplying 270μA full-scale constant current from a 5-bit digital-to-analog converter (DAC). The 5-bit DAC has the output impedance of 100 MΩ. The voltage compliance in each output channel reaches within 150 and 250 mV of the 5 V supply and ground rails, respectively. The chip was made flexible to generate different types of constant current waveform and perform a number of monopolar and bipolar stimulations. The chip was featured with in situ site impedance and site potential measurement capabilities to identify faulty sites or site characteristic variation during chronic stimulations. Figure 3.14 shows the 64- and 32-site IS-2B chips assembled on two platforms. Inductive coupling was used to receive 50 mW



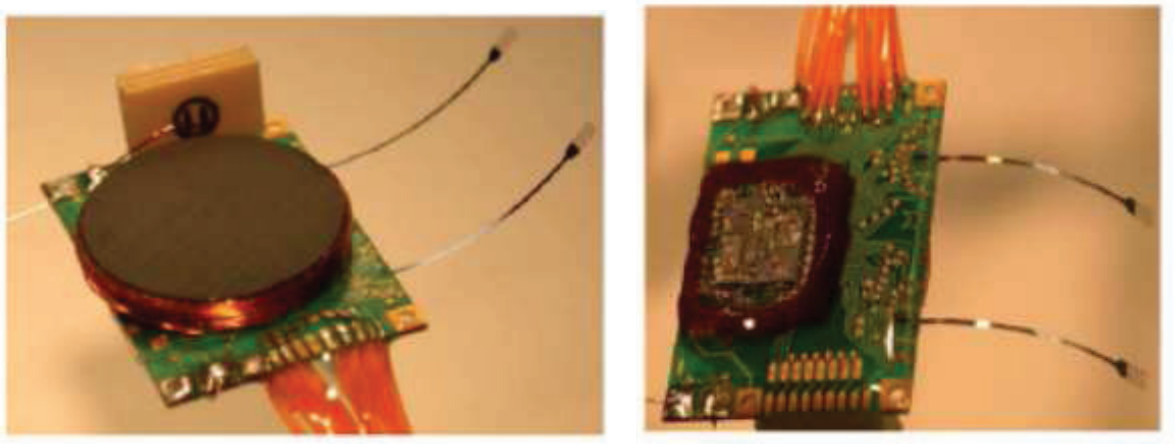
(a) (b)

Figure 3.14 Microassembly of Interestim-2B based wireless microstimulator implants: (a) 64-site IS-2B assembled on an 18 mm x 18 mm PCB platform, (b) 32-site IS-2B assembled on an 18 mm x 13 mm platform, compared with a US penny [8]. © IEEE.

power and 2.5 Mb/s data through a 5/10 MHz frequency shift keying (FSK) carrier. This data communication principle was chosen to generate up to 65800 pulses/s. However, the inductive-capacitive (LC) tank circuit to tune at carrier frequency and the capacitive low-pass filter to reject the ripples were discrete component based circuits.

The Interestim-2B chip is modular in architecture, which allowed 32 chips to be included in the prototype implant to stimulate a total of 2048 neural sites. The implant was able to address each of these chips separately and operate them in parallel. The end size of the prototype implant along with the test connectors was 19mm x 14mm x 6mm. The performance of the implant was verified through in-vitro experiments and conducting in-vivo tests in rats [8]. The inductor coil, Omnetics-Nano test-point access connectors, and hermetic

packaging of this system are presented in Figure 3.15. It is worth to mention that, being



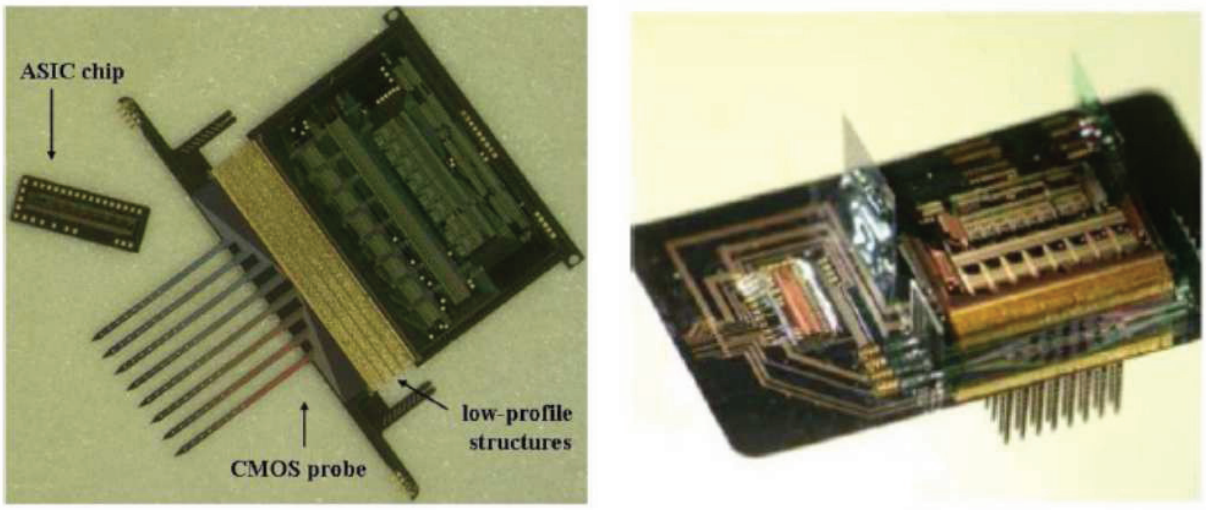
(a) (b)

Figure 3.15 (a) The inductor coil (L) is assembled on the backside of the PCB platform together with Omnetics-Nano test-point access connectors, and (b) Temporary hermetic packaging of IS-2B implant, encapsulated in silicone and coated with epoxy, to be used for acute experiments. [8]. © IEEE.

among one of the earliest prototype implants for visual intracortical prosthesis, it included many advanced features, yet was limited by the output compliance voltage.

3.6.3 System developed by Wise's team at the University of Michigan

A three-dimensional micro-compact implant was developed by Wise and Najafi at the University of Michigan for stimulation and biosignal acquisition [92], [93]. The main feature of the implant is its complex and dense assembly. Special type of low-profile 3-D microelectrode array, named Michigan array, was micromachined for this system. The array comprised of multiple planar complimentary metal–oxide–semiconductor (CMOS) probes for microstimulation and other components assembled in 3-D structure. On the end part of electrode, called shank, a plurality of stimulation points were created along its length to support stimulation at different depths. As presented in Figure 3.16(a), eight of such electrodes were grouped together to form an 8-channel. The height of the Michigan array above the cortical surface was reduced folding the backends of the probes. This process was accomplished using Parylene-encapsulated gold beams along with etch-stopped silicon braces in the backends. These probes were micromachined on a silicon platform and then integrated to an ASIC chip, capable of stimulating 64 sites. Four of such probe were combined to form 256-site 3-D arrays, which operate from ±5V supply. Simultaneous stimulation to 32 sites can be carried



(a) (b)

Figure 3.16 (a) Photograph of a 64-site eight-channel low-profile stimulating probe and a platform ASIC chip. (b) Picture of a microassembled four-probe 3-D low-profile array [92]. © IEEE.

out with maximum currents of $\pm 127\mu$A. At maximum operating condition, with pulse widths of 100μs and at 500 Hz frequency, the average power dissipation per-channel is 97μW. The developed prototype was tested on the auditory cortex of a guinea pig model as shown in Figure 3.17.

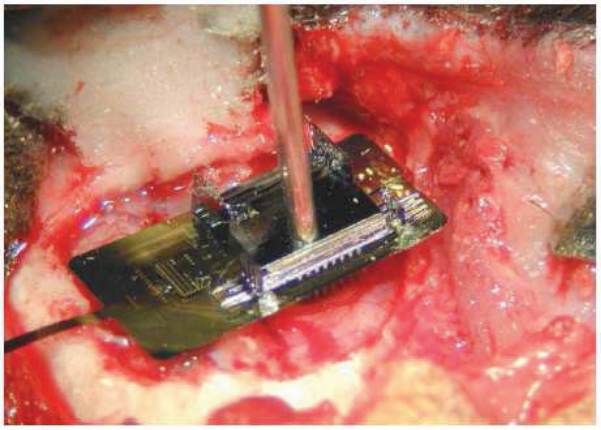


Figure 3.17 Photograph of a low-profile 3-D array inserted into the auditory cortex of a guinea pig model. [92]. © IEEE.

3.6.4 Cortivision project led by Sawan's team at the Polytechnique Montreal

Sawan's team at the Polytechnique Montreal, one of the prominent groups on this field, took an initiative to build a visual intracortical implant in his Polystim Laboratory.
To achieve their goal, various members of Polystim team worked on different parts of the implantable intracortical system, such as, the stimulation controller [94], wireless link [95], and microelectrodes [96]), and the non-implantable external controller [97] and image sensor [98]. The highly-flexible microstimulation platform designed by Coulombe et al. uses an external image sensor, an external controller, inductive-link for data and power transmission, an interface module and an implant [7]. This system was verified through in-vivo experiments on rats. The conceptual modular architecture proposed by Coulombe et al. is presented in Figure 3.18. The schematic of interface and microstimulation modules (IM and SM) are illustrated in Figure 3.19. The system also includes inductive link based wireless communication to recover data and power. The image acquisition device captures images

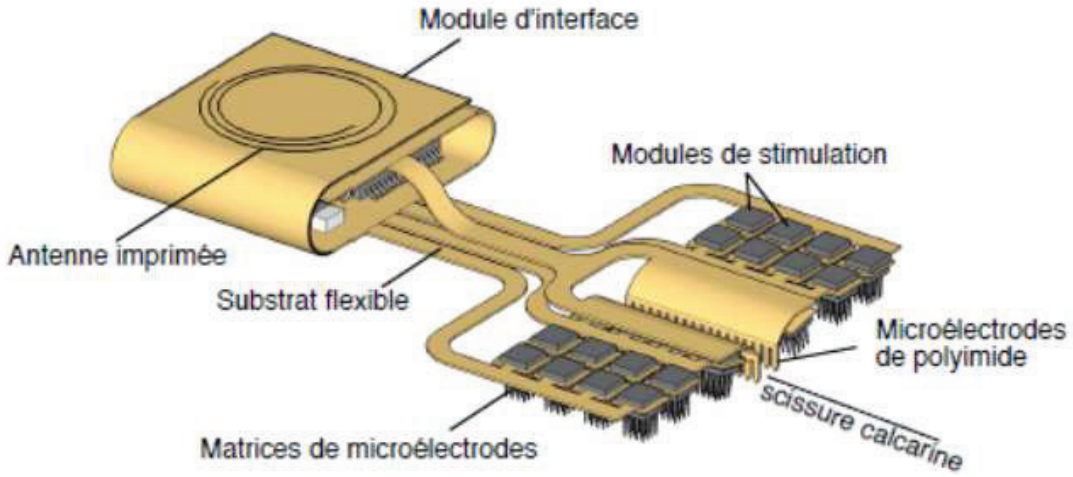


Figure 3.18 Sawan's team system: conceptual diagram of the modular architecture of the implant with flexible substrate. © [22].

and the external controller transmits them wirelessly to the interface module. The recovered power-supplies are 1.8 V and 3.3 V, and biphasic stimulation with a maximum current of 140μA is delivered from the microstimulation module. The stimulation module is compatible to perform stimulation to all 16 output channels, connected to an array of microelectrodes composed of 4 x 4 microelectrodes. However, these channels are divided into four groups so as to stimulate only four neural sites simultaneously by the stimulation module. To provide higher flexibility and security, electrode-tissue interface voltage monitoring circuit was also

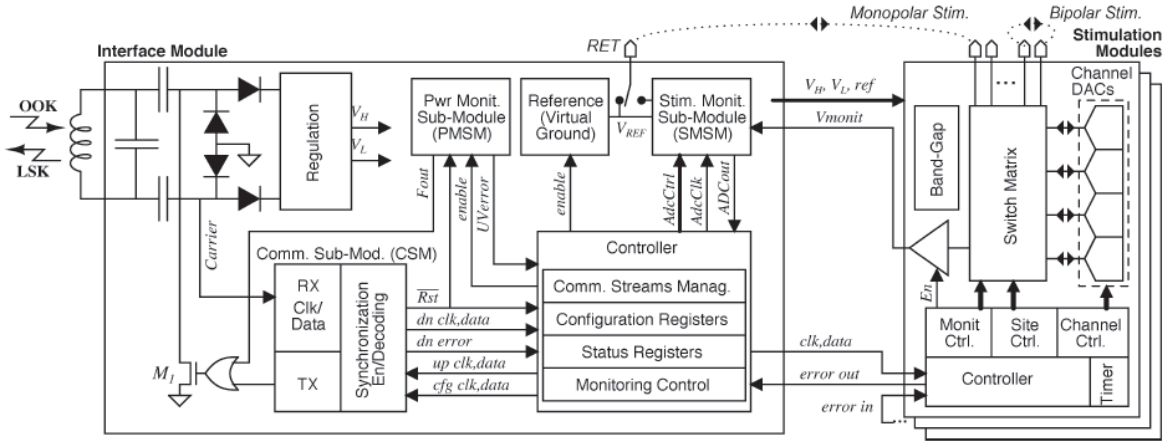
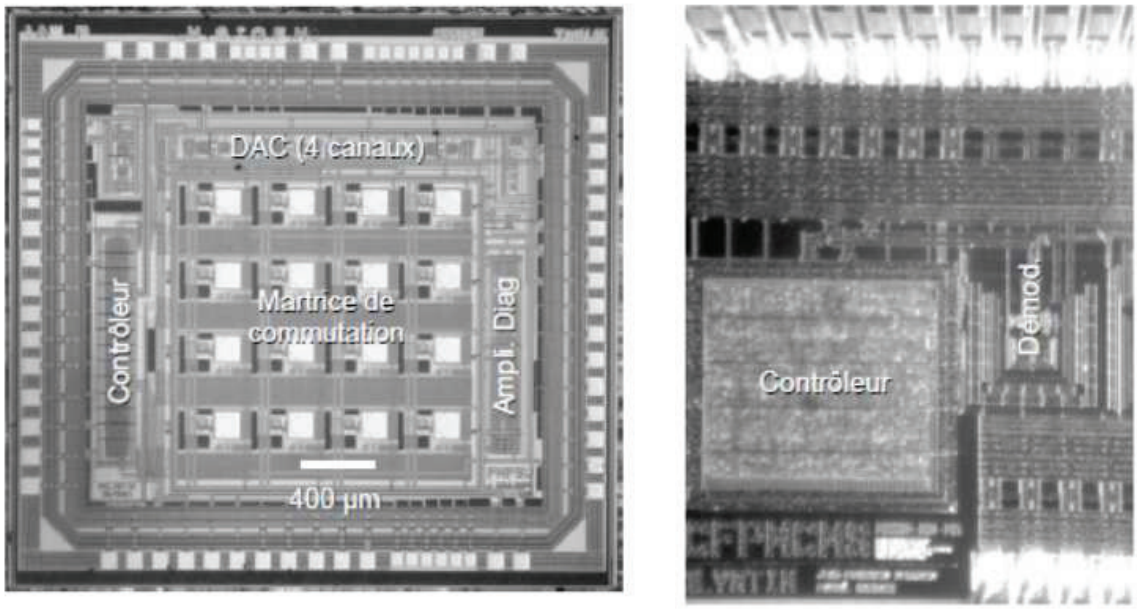


Figure 3.19 Sawan's team system: schematic diagram of the interface and stimulation modules [7]. © IEEE.

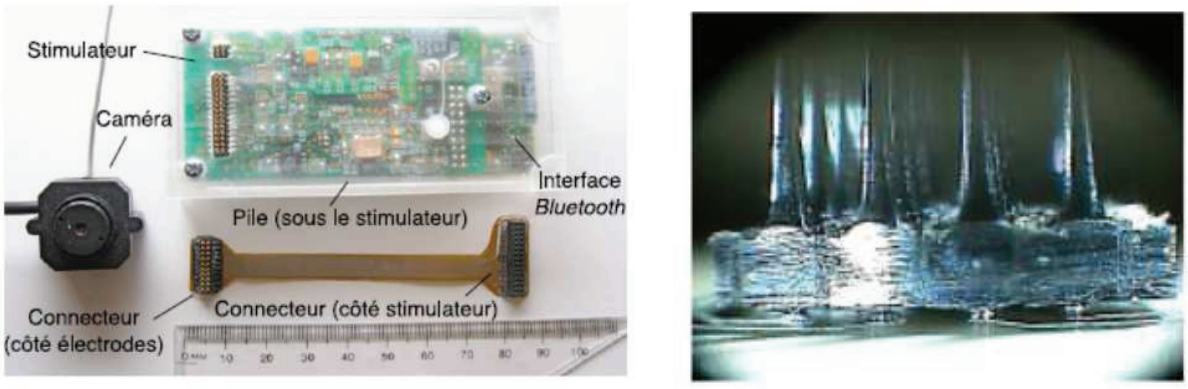


(a) (b)

Figure 3.20 Microphotographies of (a) the stimulation module, (b) the communication circuit. © [22].

in the stimulation module. The integrated version of the 16-channel stimulation module and communication circuit is illustrated in Figures 3.20(a) and (b). The interface module is modular in architecture, that is to say, 64 of such modules is able to cover a total of 1024 neural sites to stimulate entire visual cortex area. The drawback is that the integrated version of the stimulation circuitry was unable to deliver the required higher compliance

voltage to high-impedance microelectrodes. Therefore, the compliance voltage was raised by 9 V using external discrete components in the output stage while performing in-vivo tests [22]. The complete microstimulator, its accessories, the image of microelectrode array, the experimental setup with a rat, and the insertion of microelectrode array in rat's brain are presented in Figures 3.21 and 3.22. Before going to discuss about the next system developed



(a) (b)

Figure 3.21 (a) Portable stimulator for experiments with other accessories (microelectrode array assembled with the connectors and camera). (b) Photograph of a microelectrode matrix assembled on the flexible substrate before encapsulation by adhesive and silicon. © [22].

(a) (b)

Figure 3.22 (a) Photography of a freely moving rat mounted with the stimulator and the camera. (b) Microelectrode array before and after insertion. © [22].

by this group, it is necessary to mention that, in case of commercially fabricated electrodes, electrode-tissue interface impedance can reach up to 400kΩ [99]. All the previously reported

microstimulators are unable to provide the required high-voltage compliance in the output stage. The approach used by Coulombe et al. was limited to only 9V and was not integrated as well [22]. Moreover, none of these microstimulators considered to employ energy-efficient stimulation waveforms. Therefore, Sawan's team introduced the next version of the intracortical microstimulation system to solve those issues.

Both high-voltage compliance requirement and energy-optimum stimulation waveform have been considered in the design by Ethier and Sawan for high-impedance microstimulation [13], [27]. The architecture was built on dual-chip concept using two different technologies. The low-voltage 1-channel chip, a stimuli-generator which is designed in 0.18μm CMOS technology, is capable to produce constant current, rising-exponential, and half-sine pulses. It is reported from the experimental results that the rectangular pulse (constant current) ranges from 1.6 to 167.2μA and the maximal dynamic range of the generated rising exponential current extends up to 34.36 dB when the stimulation current reaches its full scale value. The stimuli-generator chip dissipates a maximum of 21.48μW and 88.3μW while generating constant and full-scale exponential currents respectively. The area occupied by this chip is 1.01mm x 1.01mm.

The 1-input channel and 4-output channel microelectrode-driver output-stage, designed in Teledyne DALSA 0.8μm CMOS/DMOS process, is fully integrated. The idea was to generate the high-voltage supplies, which are $\pm$9V, on-chip from 3.3V to substantially increase the needed voltage-compliance across high-impedance electrode-tissue interfaces for stimulation. Pelliconi charge pump architecture was used for its high efficiency and small required area [100] for both positive and negative charge pumps. Experimental results show that the generated high-voltage supplies were 8.95 and -8.46 V, which provided 13.6 V (anodic and cathodic phases together) swing for a resistive load as high as 100kΩ. The reported quiescent DC power consumed by the microelectrode driver is 51.37mW with no load, however, increases to 54.91mW when delivering a stimulation current of 200μA. The occupied silicon area by this high-voltage chip is 2.87mm x 2.92mm. Figure 3.23 shows the microphotograph of two ICs. The complete system was controlled by an external controller, implemented using a Xilinx Spartan 3E FPGA evaluation board, which was interfaced with two microchips externally.

The prototype, although, was able to solve the high-voltage compliance issue and implemented with some energy-efficient waveforms, yet has some drawbacks. The rising-exponential pulse has been found to be not energy-efficient stimulation current pulse in later studies. Two ICs and the controller are not fully integrated on a single PCB platform. Moreover, the output-stage also consumes high power budget due to the on-chip DC-DC converter, which does not satisfy the power consumption standard of implantable biomedical devices.

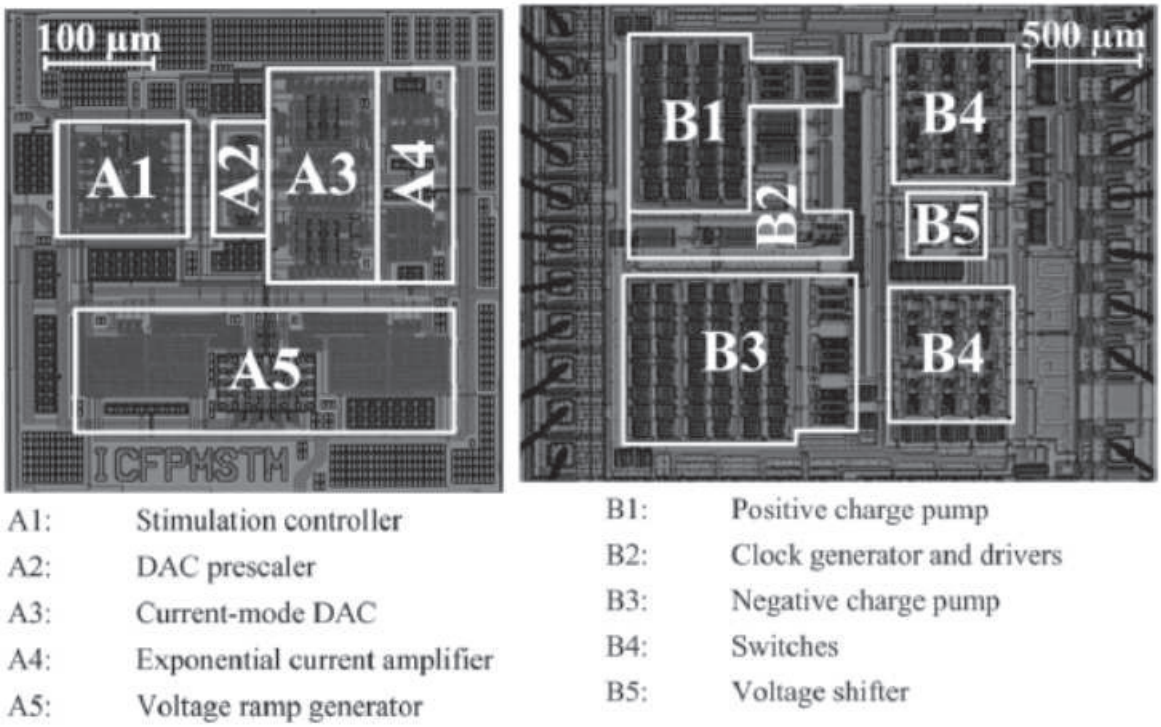


Figure 3.23 Microphotographs of the fabricated ICs for the reported system: (a) The stimuli-generator, implemented in 0.18μm CMOS process and with occupied silicon area of 1.01mm x 1.01mm, produce exponential and rectangular current pulses according to the stimulation parameters [13]. (b) The microelectrode-driver output-stage generates biphasic high-voltage supplies (8.95 and -8.46 V) to enhance the compliance-voltage swing across the load. This chip has been designed in Teledyne DALSA 0.8μm CMOS/DMOS technology [13]. © IEEE.

Wireless data transmission and power recovery were not considered either. The system was not validated using real microelectrodes through in-vitro tests or performing experiments on animals.

3.6.5 Monash Vision Group

Monash Vision Group (MVG) is collaborating with other groups from Monash University, (MiniFAB, Alfred Health, and Grey Innovation) with a long term plan to develop bionic based medical prosthetic devices to restore vision. Their target is to build an implantable cortical prosthetic device, which can be controlled wirelessly. They have studied visual field in the primary visual cortex [101], the response properties of neurons in this area [102], characterized impedance of annulus electrodes, and investigated stimulation performance of a chronic cortical implant [103]. Each implant consists of four electrodes made of 20% iridium and 80% platinum, each 2–2.25mm long and 125μm in diameter [103]. The reported electrode

impedance varied between 39.9±8.3kΩ (in saline and before implantation) to 182.4±27.8kΩ (after chronic implantation in rats) depending on pre- and post-implantation scenarios. The applied stimulation current window was 75-100μA, with charge density range 48-128μC^{cm-2} to evoke motor behaviour. Figure 3.24 shows the array of four electrodes pre- and post-implantation during in-vivo tests, sketch showing an approximate insertion location of the array into rat's brain, and the rat with chronic implant.

From architecture perspective, likewise a generic visual intracortical microstimulator, MVG

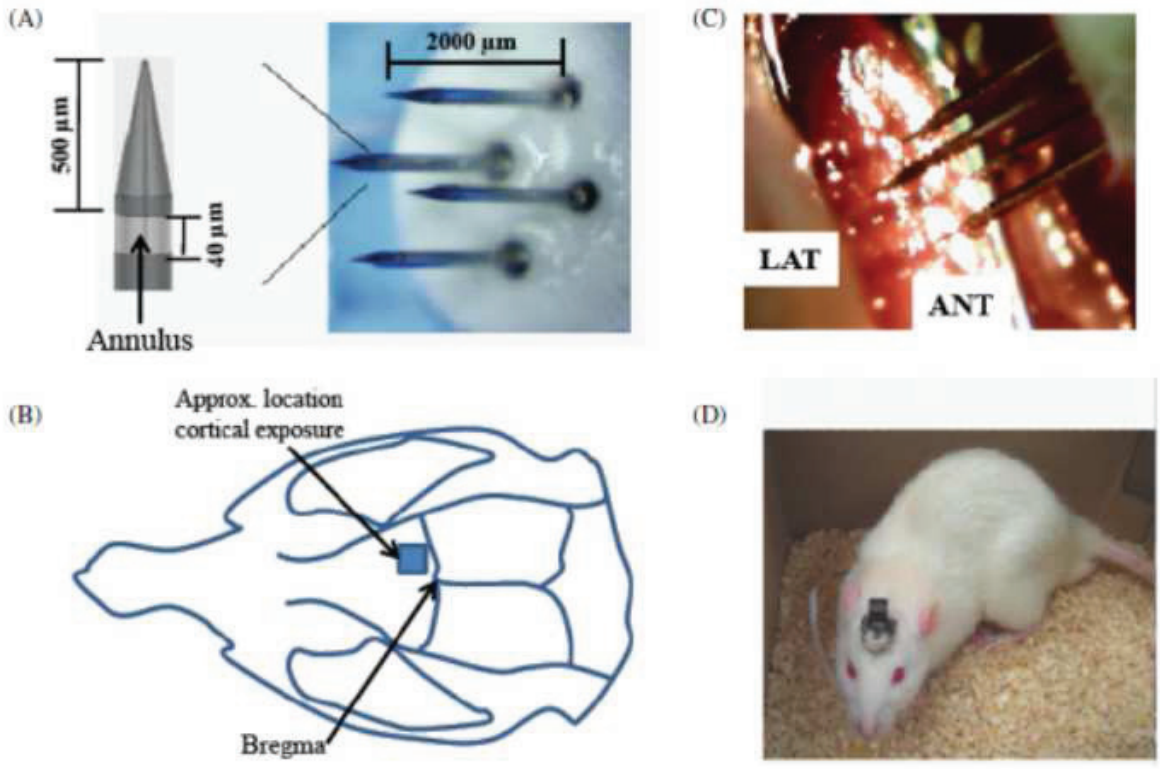
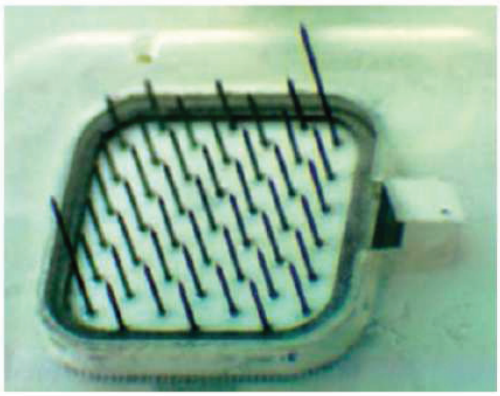


Figure 3.24 (A) An array of four electrodes used for the in-vivo tests. (B) Drawing to illustrate the estimated insertion location of microelectrode arrays with respect to bregma. (C) Photograph of microelectrode-array prior to transdural implantation into primary motor cortex of the rat. (D) Rat (post-recovery) with chronic implant. [103]. © Journal of Neural Engineering.

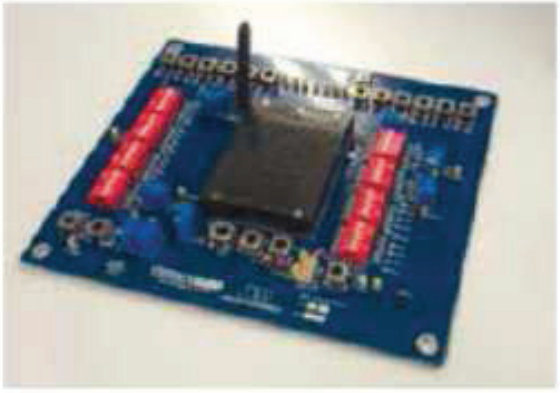
stimulator is comprised of image capturing and processing device, a wireless link, and the implant. The latter consists of 10-12 tiles to cover the V1 area of the visual cortex. An ASIC and other electronics on each tile of an area of 8mm x 8mm are hermetically encapsulated by a ceramic package, and are integrated to 45 penetrating electrodes [104], [105]. To date, the team has designed several ASICs, named ASIC1, ASIC1B, ASIC2, and ASIC3 with various features. Figure 3.25 presents the photographs of 43-electrode implant designed by the MVG,

wireless ASIC1B on its test board, and brain tissue implanted with implant Tiles.

Not much technical details have been published in the literature on the design and im-



(a)



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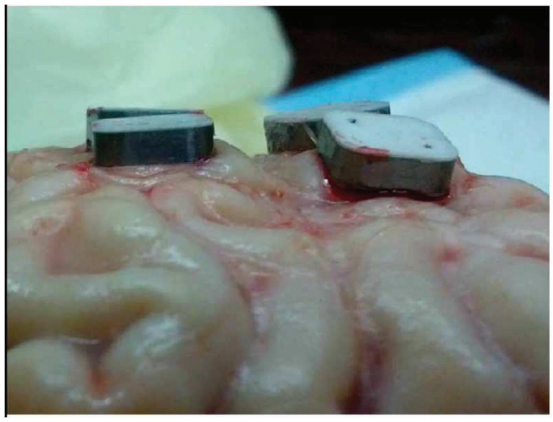
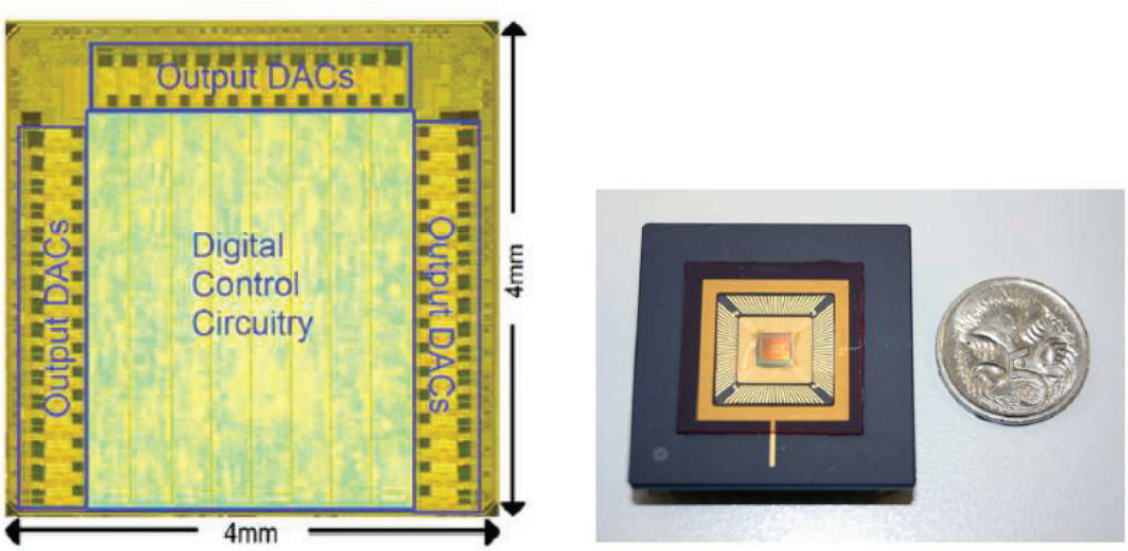


(c)

Figure 3.25 (a) A 43-electrode implant designed by the MVG for preclinical investigation. (b) ASIC1B (wireless) test board designed by the MVG. (c) Brain tissue implanted with implant Tiles. [104], [105]. © MVG.

plementation of these ASICs, except the earlier wired version reported in [106], which is a an integrated electrode driver designed in OnSemi I3T50 0.35μm high-voltage CMOS process. Two major features are the achieved (a) high-voltage compliance which is reported to be 17.3V and (b) reduced data band width. The latter has been implemented by pre-programming stimulation patterns, called wave tables, on the chip. However, from visual inspection, the delivered biphasic signals appear to be charge imbalanced and do not reach up to 17.3V [106] . The chip photograph along with its dimension is presented in Figure 3.26.



(a) (b)

Figure 3.26 (a) Layout view of the integrated neural stimulator showing its dimension. (b) Packaged version of the fabricated microchip [106]. © Elsevier Microelectronics Journal.

3.6.6 Research Group at the University of Duke

Hanson et al. at the University of Duke have developed a 15 channel intracortical microstimulator, although not intended for visual prosthesis rather for motor and sensory cortices stimulation [107]. This stimulation system was built using biploar transistor components capable to withstand 185V or higher, supplied with 50V source. Two high power 1W dc-dc converters were used to provide the required high voltage across high-impedance microelectrode arrays, made of tungsten or stainless steel microwires with teflon, SML, or HML insulation, and for the 5V voltage mode DACs. The complete system was sub-divided into four PCBs, each featuring four bipolar channels. Based on the DAC output scaling, the system was capable of delivering current with a range of 0–400 or 0–800 μA. The device was calibrated applying stimulation currents with the amplitudes of 50, 75, and 100μA through 97, 120, 180, 240, 270, 330, and 470kΩ resistors. No wireless protocol was used to transfer stimulation control parameters as well as power. The prototype was validated performing in-vivo tests on a Rhesus Monkey, which was chronically implanted with tungsten microelectrode arrays in sensory and motor cortices. The photograph of the 4-channel stimulator is presented in Figure 3.27.

The major advantageous feature of this device is its capability of handling very large compliance voltage. However, the microstimualtor is very large in dimension compared to an implantable device owing to the use of discrete components on PCB. Moreover, the system is not integrated with wireless data and power transfer capability.

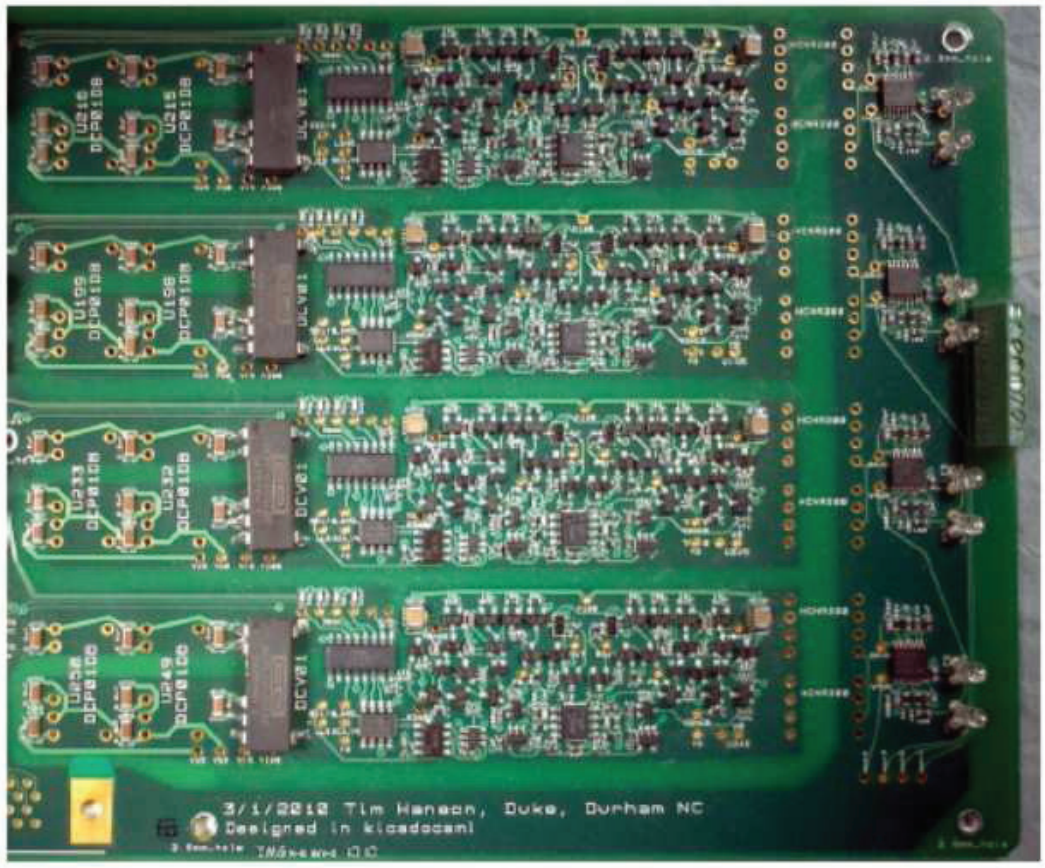


Figure 3.27 Photograph of the 4-channel high-side current controlled bipolar microstimulator implemented on a PCB. © [107].

3.7 Architectures' comparison of visual prosthetic implants

We provide, in this section, a comparison of the main parameters based on the stimulators' performances (Table 3.1). This table is presented to identify the specifications, that need to be fulfilled in this thesis. It is important to note that the stimulator in [108] is not specifically designed for visual prosthesis application, but is included here as its output-stage generates biphasic supplies required for the high-impedance microstimulation.

Table 3.1 Comparison of main visual intracortical implants.

Parameters Publication year	[80] 2006	[108] 2006	[7] 2007	[8] 2007	[92] 2007	[13] 2011	[61] 2012
Technology (μm)	0.18[a]	0.18[b]& 0.8[c]	0.18[b]	1.5[b]	3.0[b]	0.18[b]& 0.8[c]	0.35[c]
Power supply (V)	N/A	1.8, 3.3	1.8, 3.3	5	$\pm$5	1.8, 3.3	3.3, 20
Compliance Voltage (V)	VDD – 0.5	8.25	2.98[d]	0.15-5[e] 0-4.75[f]	< 10	13.7[d]	20
Max. stim. current (μA)	64	2000	140[d]	$\pm$270	127	1.6-167.2	1000
Consumed quiescent power (mW)	N/A	N/A	0.88	16.5	0.78	27.2	1.16
Area (mm^2)	2.0x2.0	9 (Includes DC-DC converter)	3.2x2.8 (Stim. module)	4.6x4.6 (Complete stim. module)	5.7x4.0	1.01, 2.9x2.9 (Stim. module and DC-DC converter)	0.2[g] (LSU)
No. of stim. sites	16	N/A	16	32	64	4	4
Load (kΩ)	71.4, 78.5	9.125	10	210 & 45	N/A	100 & 150	1, 10
Data-rate (Mbps) (wireless)	1.2	N/A	1.5	2.5	N/A	N/A	2
Power tran. carrier freq. (MHz)	4.8	N/A	13.56	5/10	N/A	N/A	13.56
Application	Intracortical	N/A	Intracortical	Intracortical	Intracortical	Intracortical	Epiretinal

[a] BiCMOS, [b] CMOS, [c] HV CMOS, [d] Source and sink [e] Source, [f] Sink [g] Per four output channels

3.8 Hypothesis and research contributions

Following the literature review, we formulate the research questions for this project. We also identify our general and specific objectives, which are itemized in the following sections. Next, the original scientific hypotheses of this thesis contributions, justification of their originalities, and refutability have been provided. Then, the proposed system is introduced briefly.

3.8.1 Research questions

1. (a) How the high-voltage compliance across the microelectrode-tissue interface impedance can be met using the available technologies?

   (b) How can the high electrode-tissue voltage be monitored using available integrated circuit technology?

2. What is the most energy efficient signal for visual intracortical microstimulation?

3. What is an optimum wireless data-communication scheme and the technical challenges to implement it for a wireless visual intracortical microstimulator?

4. What are the technical challenges to minimize size, and dynamic and static power consumptions of the intracortical implant?

3.8.2 Objectives

The general objective of this research project is the design of an implantable wireless microstimulation platform in advanced CMOS and CMOS/DMOS technology for visual intracortical prosthesis meeting the following specific objectives:

1. Design a high-impedance microelectrode driver (MED) in Teledyne DALSA 0.8μm CMOS/DMOS process with the following specifications and to meet high-voltage compliance developed while injecting stimulation current to the high-impedance microelectrode-tissue interface:

   (a) Highly flexible to perform monophasic and biphasic stimulations when electrodes are configured either in monopolar or bipolar arrangement.

   (b) Ability to perform charge-balanced microstimulation using either current source, sink or both.

   (c) Efficient to control stimulation current amplitudes precisely.

(d) Configurable to inject various levels of stimulation current.

(e) Robust to prevent distortion while delivering different stimulation current pulses.

(f) Capable of performing multi-channel stimulation simultaneously.

(g) Capable of monitoring electrode-tissue interface voltage and digitize it.

2. (a) Investigate and characterize different types of energy-efficient stimulation waveform through simulations and use the energy-optimum waveforms for microstimulation.

   (b) Design of the stimuli-generator in CMOS process to minimize the power consumption and area, and to implement the energy-optimum stimulation waveforms.

3. Implement a 10Mbps data-rate compliant bidirectional transmission protocol to evoke high-resolution phosphene pattern in the visual field.

4. Design a wireless power-transmission unit satisfying the standard of implantable biomedical devices.

5. Test and analyze the performance and limitation of each module.

6. Assemble different parts of the prototype on PCB platforms; and minimize the device size, and dynamic and static power consumptions.

7. Assemble the microstimulator with a novel microelectrode-array and validate the performance of the microstimulator through in-vitro or in-vivo tests.

3.8.3 Scientific hypothesis of contributions

Hypothesis 1: Implementing high-impedance microelectrode driver (MED) in Teledyne DALSA 0.8μm CMOS/DMOS process allows to provide the necessary compliance voltage across microelectrode-tissue interface high-impedance.
Justification of the originality: Original contributions are the high-configurability, satisfying all the specifications mentioned in 1, low-power consumption meeting the standard of implantable biomedical devices, highest voltage compliance, and on-chip switch control ability.
Refutability: The hypotheses will be refuted if the implementation of the MED in Teledyne DALSA 0.8μm CMOS/DMOS process cannot meet the specifications.
Hypothesis 2: The investigated stimulation waveforms are able to save energy when they are delivered to the stimulation sites, and the implemented stimuli-generator consumes low-power by itself and dissipates less energy in the intracortical tissues.

Justification of the originality: The novelty of the stimuli-generator lies within its capability of generating energy-optimum waveforms, producing less heat in biological tissues, and consuming less power from supply.
Refutability: The hypothesis will be refuted if the stimuli-generator is unable to satisfy the power consumption and heat dissipation limits of implantable biomedical devices.
Hypothesis 3: The proposed 10Mbps bidirectional data-communication protocol satisfies the required data-rate, which is able to generate high-resolution phosphene pattern in the visual field.
Justification of the originality: The concept of integrating a multichannel and high data-rate bidirectional capacitive-link communication protocol to satisfy the phosphene resolution is novel.
Refutability: The hypothesis will be refuted if the proposed capacitive-link based data-transmission scheme fails to perform the desired task.
Hypothesis 4: Assembly of the designed integrated circuits (ICs) and novel Pt-coated MEA on miniature PCB platforms optimizes the prototype size and facilitates integration; and validating the complete system through in-vitro tests justifies the efficacy of both the microstimulator and MEA in real environment.
Justification of the originality: Solving technical details for the assembly of the multi-chip based stimulator and the complicated procedure of MEA interfacing, and validating the complete system through in-vitro tests are major contributions.
Refutability: The technical procedure to assemble various parts and MEA needs to be optimized or changed to minimize the prototype dimension, in case, the end size becomes large and the stimulator, along with the MEA, becomes non implantable.

3.9 An overview of the proposed system

A brief overview of the proposed system is presented in Figure 4.1 meeting the desired objectives of this thesis. The system consists of hybrid wireless data and power transmitter and receiver blocks to transmit stimulation control parameters and deliver power to N number of energy-efficient and high-voltage compliant microstimulation modules (MSMs). Each MSM is modular in architecture and delivers stimulation current to 16 output channels, interfaced with a novel Platinum-coated microelectrode array. The system is presented and discussed in detail in the following chapters.

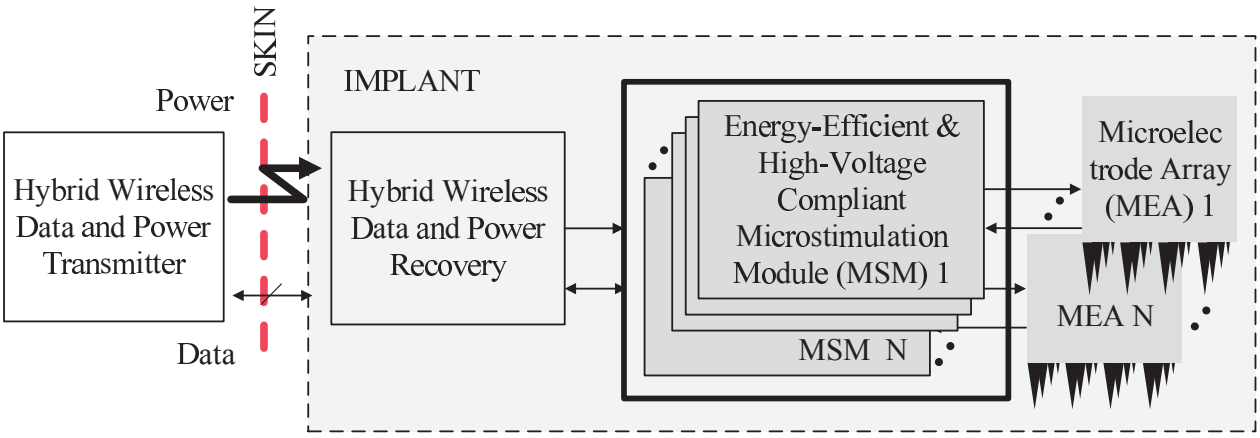


Figure 3.28 An overview of the architecture of the proposed visual intracortical microstimulator.

3.10 Conclusion

In this chapter, we presented various microelectronic device based prosthetic techniques to treat blindness. We primarily emphasized on intracortical approach and studied early physiological experiments performed by the pioneers in this research domain. Next, the literature review on custom built prototypes is presented and their performance has been compared in tabular form. The technical limitations in the mentioned architecture have been analyzed, research questions emerged from this investigation have been formulated and our objectives as answers to these questions have been presented. An overview of the architecture of the new wireless visual intracortical microstimulator meeting the objectives of this thesis has been presented at the end of the chapter.

CHAPTER 4

THE PROPOSED SYSTEM AND THE ENERGY-EFFICIENT STIMULI-GENERATOR

4.1 Introduction

We present in this chapter, the proposed system, microstimulation module (MSM), and an energy-efficient stimuli generator (SG) dedicated for visual intracortical microstimulation. We elaborate the design principle and implementation of 4-channel stimuli-generator, which produces constant current (rectangular), half-sine, plateau-sine and some other types current pulse waveforms, and delivers them to the output-stage (MED) of the microstimulator. The post-layout simulation and experimental results of the stimuli generator are presented in the end of this chapter.

4.2 The proposed system

To achieve our objectives and fulfil the original scientific hypothesis of this thesis contributions, we have proposed a new highly-configurable microstimulation system, which is presented in Figure 4.1. The system consists of four major building blocks: (i) microstimulation module (MSM), (ii) high data-rate transceiver, (iii) power recovery unit, and (iv) central controller.

4.2.1 Microstimulation module (MSM)

Figure 4.2 illustrates the proposed microstimulation module (MSM). This is a multi-chip interface between the central controller and the microelectrode array. The MSM consists of a high-voltage output-stage or microelectrode driver (MED), an energy-efficient and multi-waveform stimuli generator (SG), an electrode-tissue interface voltage monitoring unit, and an analog-to-digital converter (ADC) to convert the monitored voltage into digital signal. The high-impedance microelectrode driver (MED) is designed in Teledyne DALSA 0.8μm 5V/20V CMOS/DMOS process to provide the required compliance voltage across the selected microelectrodes [109], [110]. To reduce the power consumption, the stimuli generator (SG) is implemented in IBM 0.13μm 1.2V/3.3V CMOS process [110], [111]. Discrete components have been utilized to design the monitoring unit and the ADC.

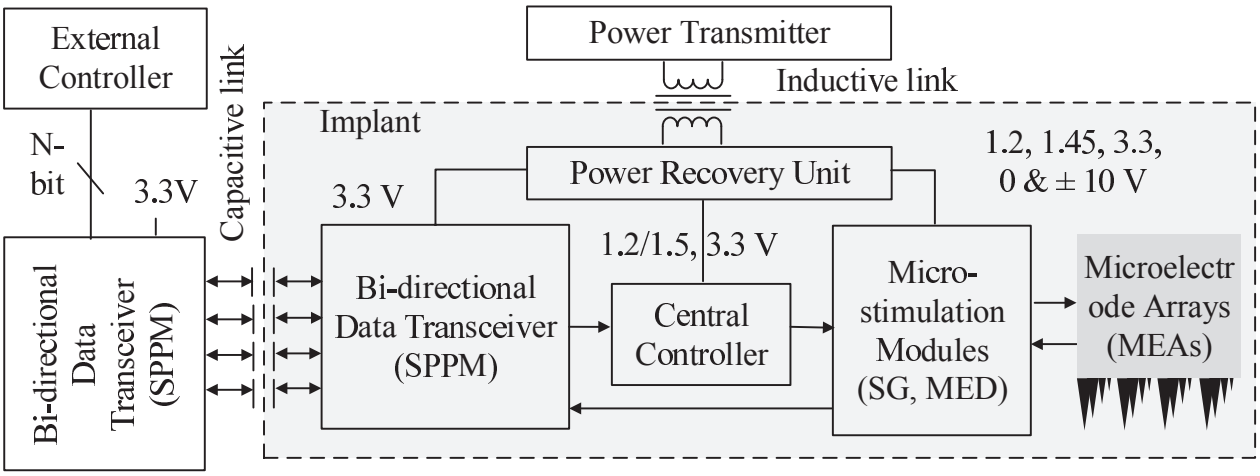


Figure 4.1 Architecture of the proposed visual intracortical microstimulator. Each stimulation module is designed to drive an array of 16 microelectrodes. 1.2 to 3.3V supplies are for the low-voltage analog and digital components used in two microchips, designed in IBM 0.13μm and DALSA 0.8μm 5V CMOS technologies, and central controller. $\pm$ 10 supplies are for the high-voltage sections included in the output stage, realized in 0.8μm 20V DMOS process.

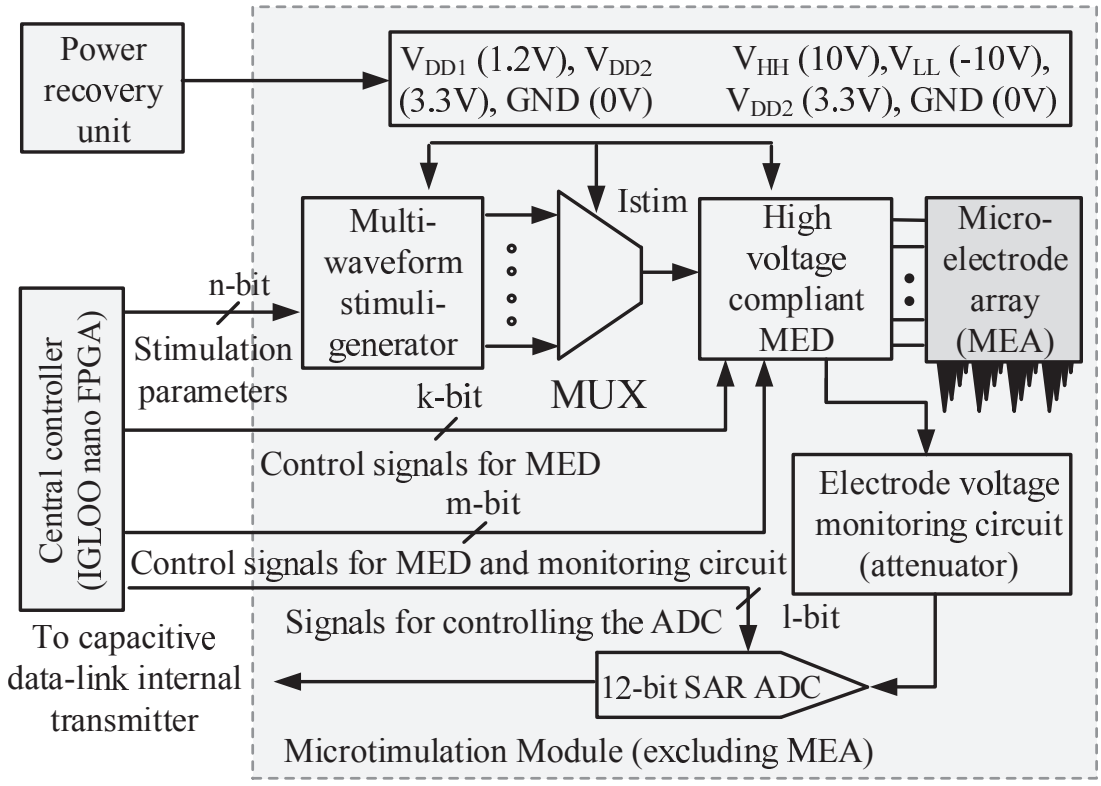


Figure 4.2 Architecture of the proposed microstimulation module along with its building blocks. Electrode array is not part of this design but connected to the MSM.

The microelectrode driver, high data-rate transceiver, power recovery unit, central controller, and assembly of the microstimulation module (MSM) are presented in the subsequent chapters. The design principle of the stimuli generator (SG) along with its post-layout simulation and measurement results are presented in the following sections.

4.3 The energy-efficient and multi-waveform stimuli-generator

4.3.1 Introduction

Regardless of applications and designs, all microstimulators must execute charge balanced stimulation to prevent the discharge of toxic ions in the stimulation sites produced by irreversible Faradic electrochemical reactions [30]. This essential condition can be met through proper choice of stimulation current amplitude, inter- phase and pulse durations, frequency, and direction of stimulation pulses precisely. Current-mode stimulation allows to control the delivered charge quantity meticulously, thereby, maintaining charge balanced stimulation. The threshold of action potential and elicited phosphene features (size, duration, and intensity) [74] are also modulated by the aforementioned stimulation parameters.

Most of intracortical microstimulators are implemented with rectangular waveform for monophasic and biphasic stimulations. This constant current pulse, compared to other pulse types, delivers maximum charge quantity and is easy to generate [113]. However, energy-efficiency is a prime concern for both the safety of the biological tissue and medium. This can be achieved by limiting the heat dissipation, reducing power consumption of the stimulators, especially those which are implantable, and increasing battery-life. Recently some researchers are paying attention to alternative waveforms and the growing interest among them is to determine the energy-optimum waveforms for microstimulation. The effects of stimulus pulse shapes on the strength-duration curve and their charge injection capacity (CIC) are being studied. Sahin et al. applied some waveforms composed of non-rectangular pulses to a computer simulated local membrane model [114]. The objective was to determine the maximum charge injection capacity (CIC) and the minimum required neural activation threshold to generate the action potentials. The waveforms, under their investigation, were rectangular, rising and decaying exponential, linear increase, and decrease, sinusoidal and Gaussian. These waveforms were injected to titanium nitride microelectrodes to measure their charge injection capacity. Their study found exponential and linear decaying, and Gaussian pulses to be the most energy-efficient; and the linear decaying pulse with the highest charge injection capacity for pulse widths from 20 to 500μS.

In [115], authors used genetic algorithm to determine the energy-optimal neural stimulation signal. The algorithm was applied to the computational model of a mammalian myelinated

axon. The resulting energy-optimal signal, obtained from the progression of this algorithm, was truncated Gaussian signal that closely resembles half-sine pulse. This waveform was applied on a cat sciatic nerve during in vivo experiments, and it outperformed in both energy- and charge-efficiency over other regular waveforms conventionally used in neural stimulation. Another investigation was made by Foutz et al. to explore and compare the neural activation energy of different waveforms, which are rectangular, triangular, exponential, sinusoidal, and Gaussian [29]. Computer model simulation was performed for both intracellular and extracellular stimulations. The specific application was deep brain stimulation (DBS) and the waveforms were applied through DBS electrode. They concluded that centered-triangular pulse with duration of 1ms can save energy consumption by 64% and 10% compared to rectangular pulse of durations 100μs and 1.25mS respectively.

Applying the principle of least action to functional electrical stimulation (FES), a criterion can be formulated to construct an energy-optimum stimulation-current waveform [116]. The most recent research on this energy-optimal criterion of neural stimulus was carried out by Krouchev et al. [113]. In their investigation, single-compartment cortical neuron model was used in computer simulation and monophasic waveforms with rectangular, half-sine, rising and decaying quarter-sine, rising and decaying exponential, triangular, and rectangular-decaying exponential pulse shapes were applied to that model. Their computational results suggest that for short stimulation pulse, T $\leq$ 1mS, rectangular pulse outperforms the others. However, as the pulse width increases, the sine-like pulses, tend to reach the energy-efficiency of rectangular pulse and surpasses for longer pulse duration, T $\geq$ 5 mS. A summary on the preliminary investigation on these waveforms have been reported in section 4.3.2.

All the analyses, performed by different groups, were affected by their applications, algorithms for computation, computation of neuron model, type of electrodes used during experiments, distribution of capacitive and resistive parts in the equivalent electrode model, stimulation frequency on the equivalent model of electrode, stimulation pattern (monophasic or biphasic) etc. The conclusions of three major groups suggest the half-sine pulse, a close approximation of truncated Gaussian pulse, to be the energy-optimal current stimulation pulse, especially for long pulse duration. Moreover, a deep investigation into the research conducted by Grill's team reveals that stimulation current pulses are energy-optimum for pulse widths of 20 to 200μS, when their shapes take the form of a truncated Gaussian pulse with a constant base current, which we call plateau-Gaussian. Krouchev et al. reached almost to the same conclusion, but for pulse duration of 5mS [117]. Irrespective of the pulse width, it is evident that there remains a constant current at the base of truncated Gaussian or half-sine energy-efficient pulse. This plateau-Gaussian (or plateau-sine) pulse is nothing but a linear summation of rectangular and Gaussian (or sine) pulse. Therefore, it is highly

desirable to design a stimuli-generator which is capable to produce constant, half-sine, and plateau-sine current pulses for efficient stimulation of neural tissues saving some energy.
Most of the commercially available and custom designed stimulators, to-date, generate rectangular pulse waveforms. To the authors' knowledge, three custom microstimulators have been designed with energy-optimum waveforms for visual neuroprosthetic application (microstimulation). The first one is designed to provide rectangular, rising-exponential, and half-sine [13]. The second stimulator is able to deliver rectangular, and rising and falling (decaying) exponential pulse waveforms [62]. In this thesis we discuss how to implement a low-power stimuli-generator capable of producing rectangular, half-sine, plateau half-sine, and some other types of energy-optimum waveforms.
The operation and design principles of building blocks for the multi-waveform stimuli-generator are presented in section 4.3.3. Section 4.3.4 illustrates the post-layout simulation and measurement results of different functional units and the complete stimuli-generator chip. Technical issues related to the expected and obtained measurement results have been addressed in the conclusions.

4.3.2 Exploration of energy-efficient waveforms

Investigation performed by N. I. Krouchev et al. on exploring various energy-efficient stimulation waveform to elicit action potentials in a single-compartment membrane model is summarized here [113]. To achieve our objective, we have analyzed some new energy-efficient wave shapes. The waveforms we considered are:

1. Rectangular pulse
2. Half- and quarter-sine pulses
3. Half-rectangular and half-exponentially decaying pulse
4. Rising- and decaying- exponential pulses
5. Decaying-exponential pulse
6. Symmetrical triangular pulse
7. SCP-S, SCP-E, SCP-HF, SCP-HL, SCP-L pulses,

Where SCP = Scalable centered-plateau, S = Rising and decaying sine, E = Rising and decaying exponential, F=Flat, H=Half, and L=Linear.
All of the waveforms listed above are shown in Figures 4.3 and 4.4. Each of the waveforms

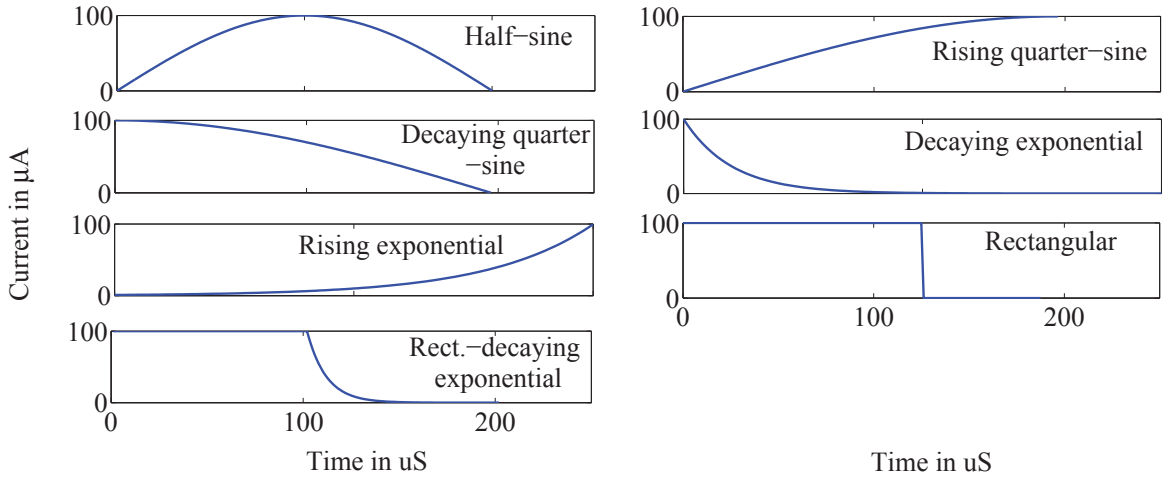


Figure 4.3 Waveforms used for efficiency analysis: first group.

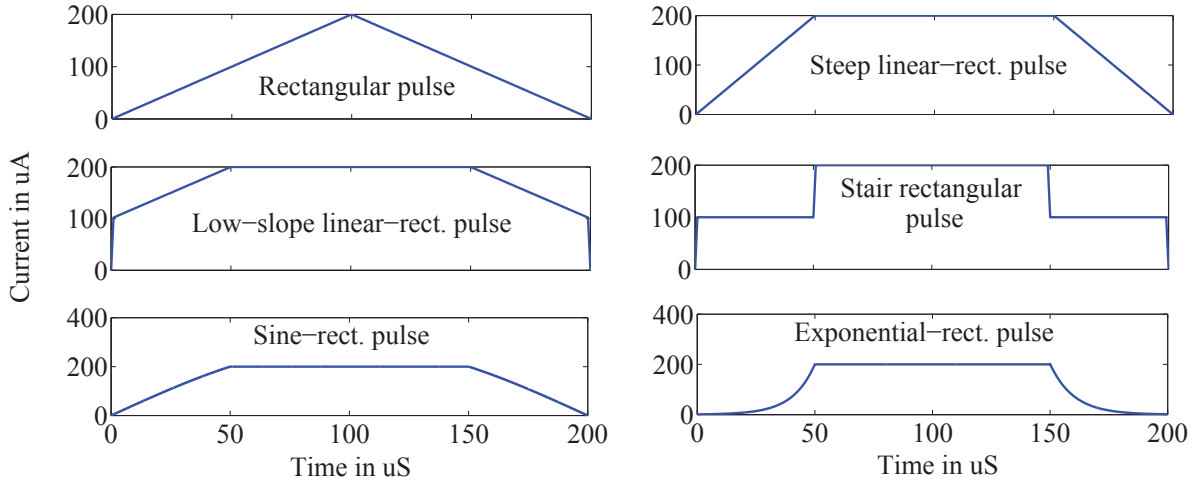


Figure 4.4 Waveforms used for efficiency analysis: second group.

has been applied to a model of a single axon for generating action potential, and the strength-duration curves and total-charge vs pulse duration curves have been plotted to identify the charge-optimum waveform.

The strength-duration and total charge quantity vs pulse duration curves, plotted in Figures 4.5 -4.7 for pulse widths of 0.1, 0.2, 1, 2, and 5 mS, reveal that rectangular waveform delivers the highest amount of charge with the lowest amplitude of stimulation current compared to other waveforms. The energy efficiency takes into account both the energy dissipated across the electrode-tissue interface impedance as well as the energy consumed by the implant. An waveform can be energy efficient iff the energy saved by that waveform compared to the rectangular waveform surpasses the energy consumed by that stimuli gener-

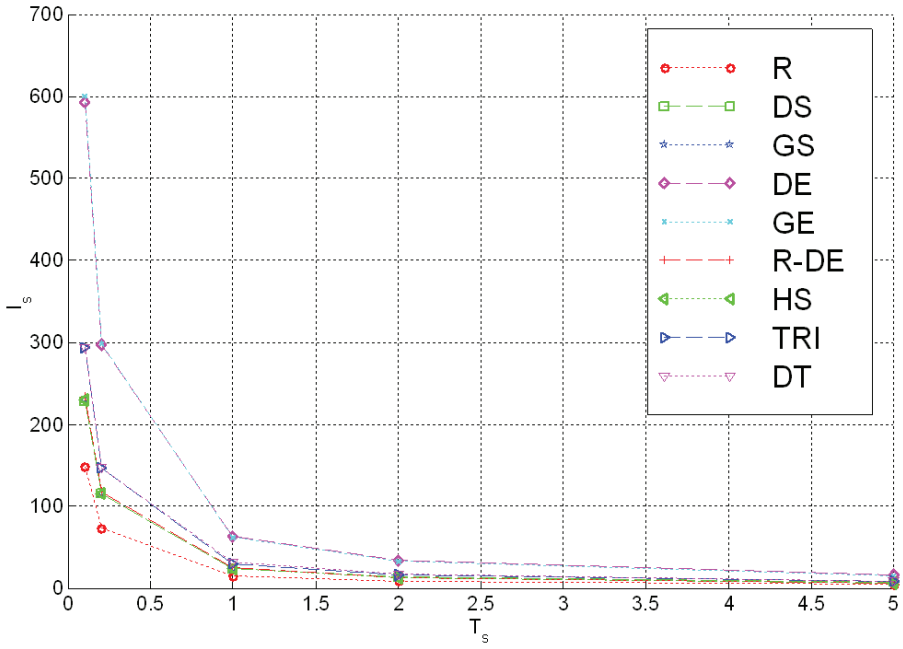


Figure 4.5 Strength-duration curves for first group of waveforms. The units for T_s and I_s are mS and μA respectively. © [113].

ator. The energy dissipated across the electrode-tissue interface impedance can be calculated according to the following formula

$$\begin{aligned} E(t) &= \int_0^{T_s} P(t)dt \\ &= \int_0^{T_s} V(t)I(t)dt \\ &= \int_0^{T_s} I^2(t)Z(t)dt \end{aligned} \tag{4.1}$$

where

$E(t)$ = Instantaneous energy consumed by the electrode-tissue interface impedance

$P(t)$ = Instantaneous power dissipation across the electrode-tissue interface impedance

$V(t)$ = Instantaneous voltage across the electrode-tissue interface impedance

$I(t)$ = Instantaneous current through the electrode-tissue interface impedance

T_s = Pulse width, and

$Z(t)$ = Electrode-tissue interface impedance

The easiest waveform to generate is the rectangular waveform which requires only a simple current- or voltage- mode DAC. Therefore, the design complexity of the stimuli generator for the new energy-optimum waveforms must be taken into consideration as the new circuits may

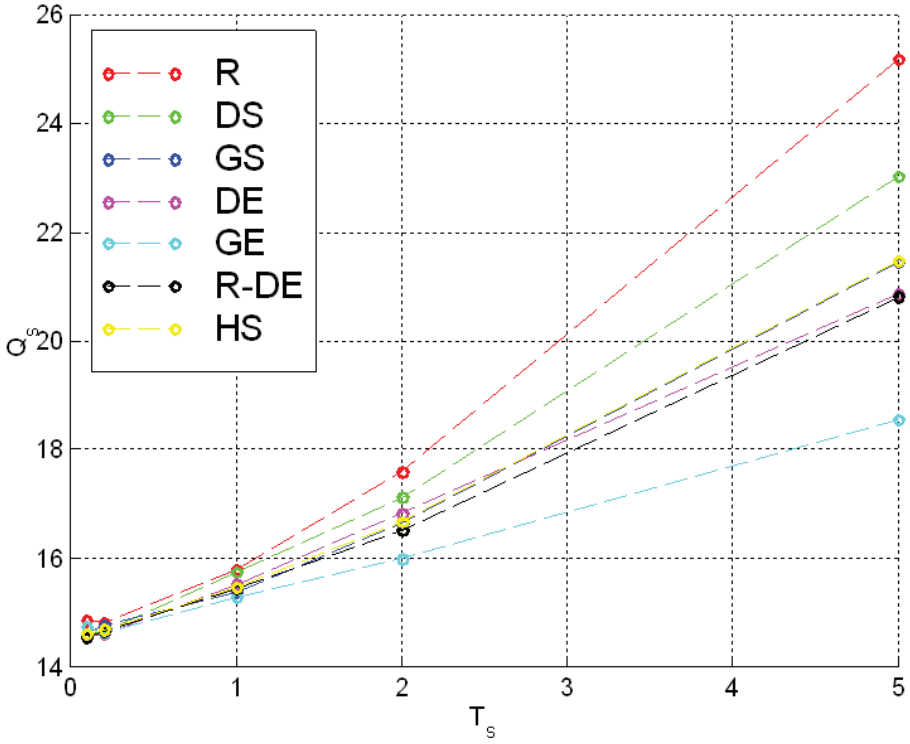


Figure 4.6 Total charge delivered Vs pulse width: first group of waveforms. The units for T_s and Q_s are mS and nC respectively. © [113].

dissipate more power than a simple current-mode DAC. To mitigate the design complexity of novel stimuli generator, we aimed to analyze some other pulse shapes which are based on the sinusoidal frequency components of the rectangular pulse and might be less complex to implement. These new category pulses are shown in Figure 4.8. However, we did not apply these sine-pulse harmoic based waveforms to the neuron model to find their charge delivering capabilities compared to the rectangular and other previously stated waveforms.

In this energy efficiency analysis, some other parameters such as polarity of stimulation, stimulation frequency, electrode's equivalent circuit, and type of electrode will also play significant roles. Injecting and investigating the effects of sine-pulse harmonic based waveforms to neurons, and analyzing the effects of these parameters on the energy efficiency of stimulation waveforms were beyond the scope of this project. Therefore, this research field still remains open to future exploration.

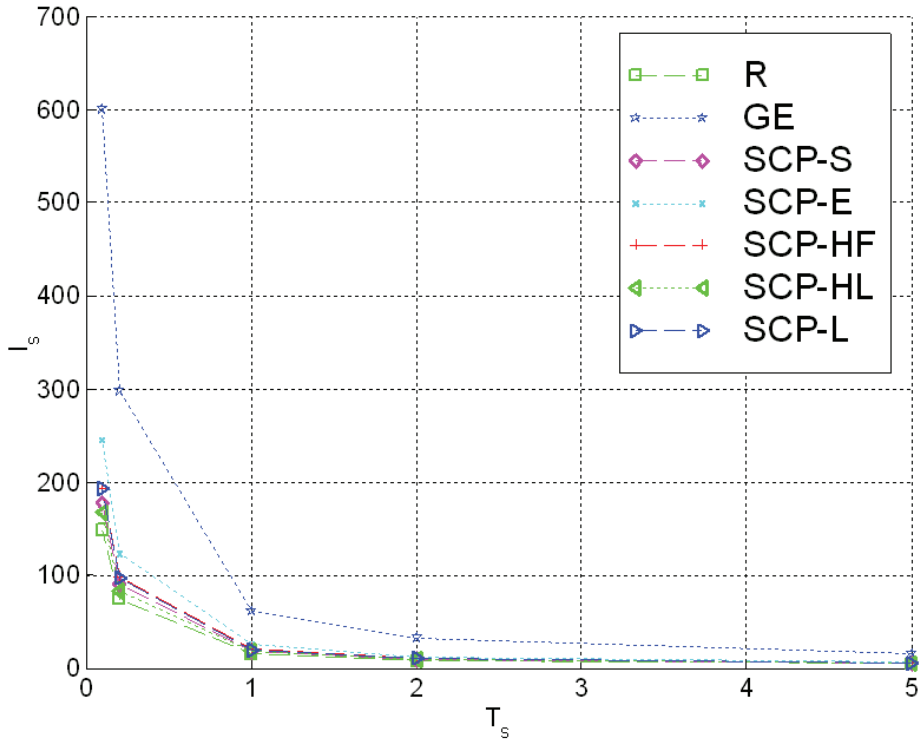


Figure 4.7 Strength-duration curves for second group of waveforms. The units for T_s and I_s are mS and μA respectively. © [113].

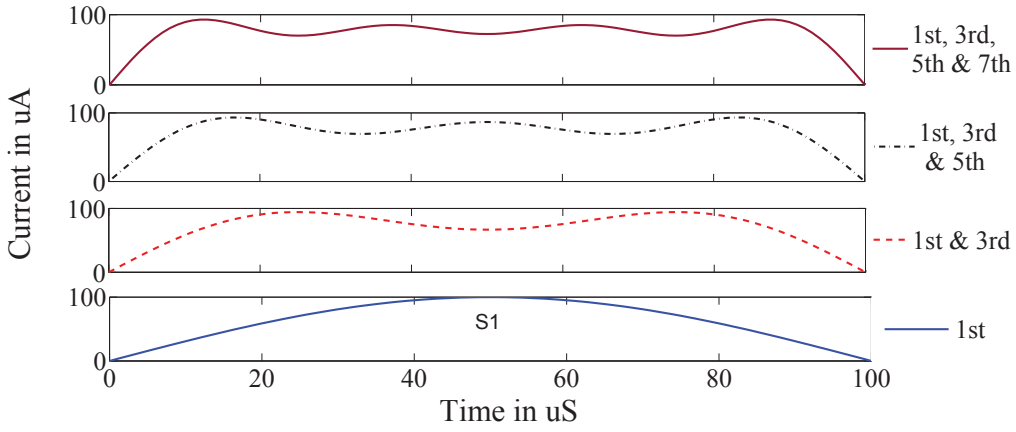


Figure 4.8 Waveforms to be used for efficiency analysis: third group.

4.3.3 The proposed stimuli generator (SG)

The four channel stimuli-generator (SG) delivers energy-efficient pulse patterns through the high-impedance microelectrode driver output-stage (MED) to the microelectrode array. The stimuli-generator, illustrated in Figure 4.9, consists of a digital controller, bias voltage and

reference current generator, ramp voltage generator, current-controlled source and sink DACs,

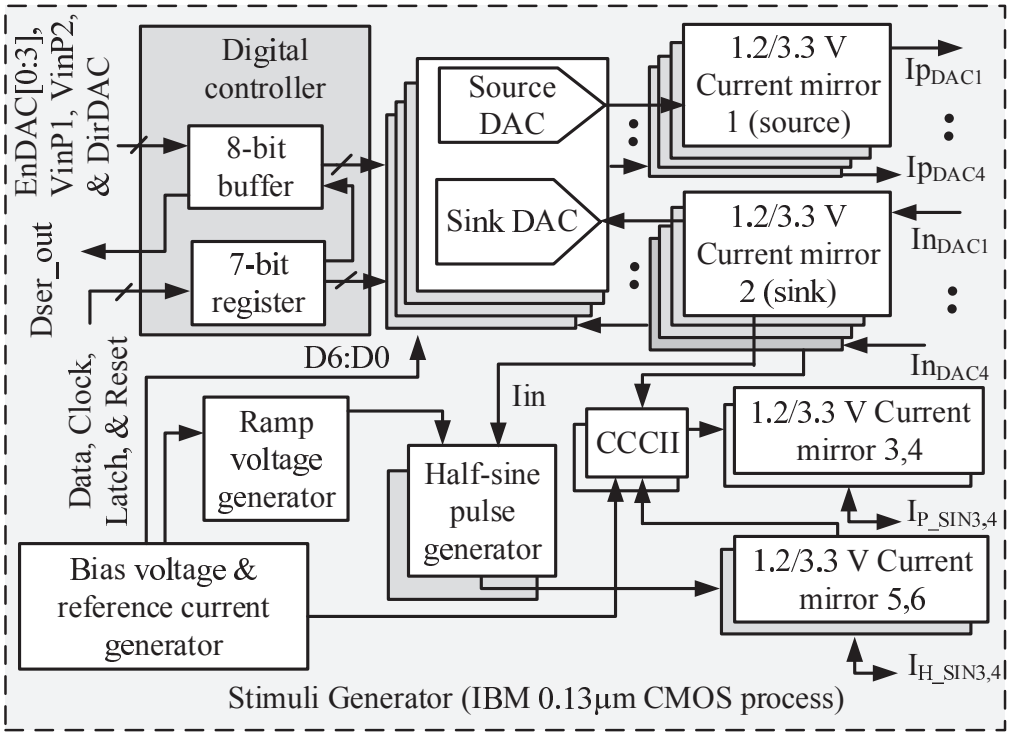


Figure 4.9 Illustration of the architecture of the stimuli generator with different functional blocks within it.

half-sine (HS), plateau-sine (PS) and mixed-type pulse generators, and 1.2V/3.3V current mirrors. The stimuli generator (SG) is implemented in IBM CMOS 0.13μm 1.2V/3.3V process [110], [111] to reduce the power consumption in this current waveform generator.
The realization and working principles of different functional blocks are described in the following sections.

Digital controller

The digital controller, presented in Figure 4.10, receives signals Data, Clk, Latch, Reset, DirDAC, VinP1, VinP2, and EnDAC[0:3] from the central controller to regulate the control parameters, such as stimulation current magnitude, direction of stimulation (anodic or cathodic), pulse-width, inter-pulse duration, and type of waveform. EnDAC[0:3] selects the stimulation current channel and DirDAC decides its phase. Serial data is applied to the 7-bit serial-in parallel-out (SIPO) shift register. Signal Dser_out is the internal serial data passed at the output of the 7-bit serial-in parallel-out (SIPO) shift register.

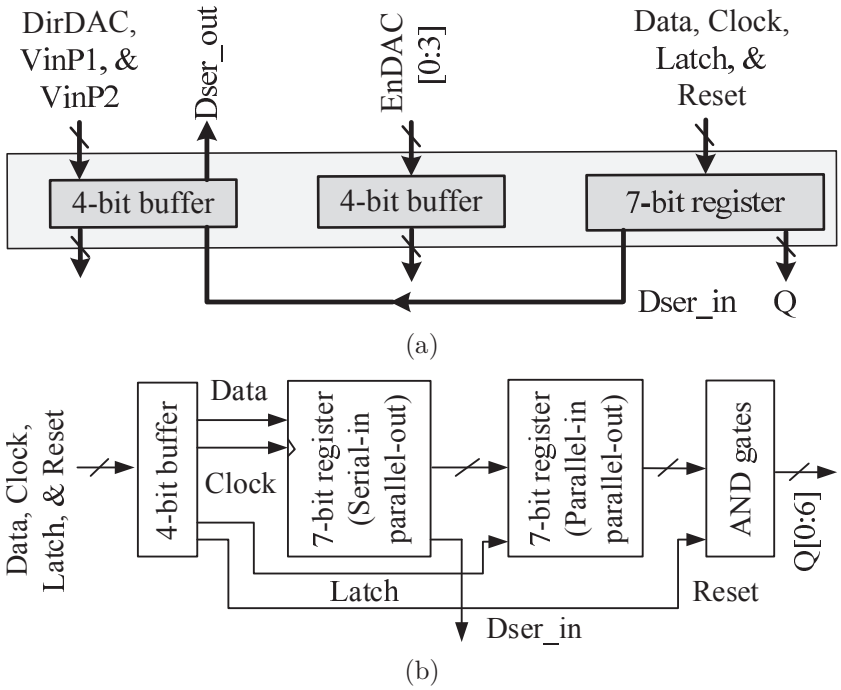


Figure 4.10 (a) Configuration of the digital controller of the stimuli generator. (b) Architecture of the 7-bit serial-in parallel-out shift register.

Current mode DAC

Each stimuli-generator is designed to support stimulation currents in four channels. A small area current mode DAC, incorporated with mixed multibias [118] and thermometer code techniques [119], is dedicated for each channel. This mixed topology has been selected to reduce the area without sacrificing the linearity of the DAC. The maximum stimulation current per source and sink DAC is 221μA. The resolution of each DAC is set to 7-bit to meet the specified current limit. The current-mode source DAC is illustrated in Figure 4.11 with different functional blocks [110], [111]. There are four source DACs each of which is dedicated for each channel and enabled by EN signal. DIR signal, which selects either source or sink DAC, controls the direction of current. D6-D1 are thermometer decoded and segmented into three groups (D6-D5, D4-D3 and D2-D1) to reduce the number of row-column decoders and hence, the area of the DAC. For the LSB, D0, three inverters have been added to match the delay to those of thermometer decoded signals. The first two, D6-D5, define three values for the reference current, Iref, to define three stimulation current ranges. Within each range, the amplitude of current depends on the bit values of D4-D0. The sleep mode operation of the DAC is enabled when the DAC is not in operation and has been implemented to reduce the static power consumption. Transistors are inserted between the power supplies for digital parts, VDD and analog parts, VDA and the respective blocks.

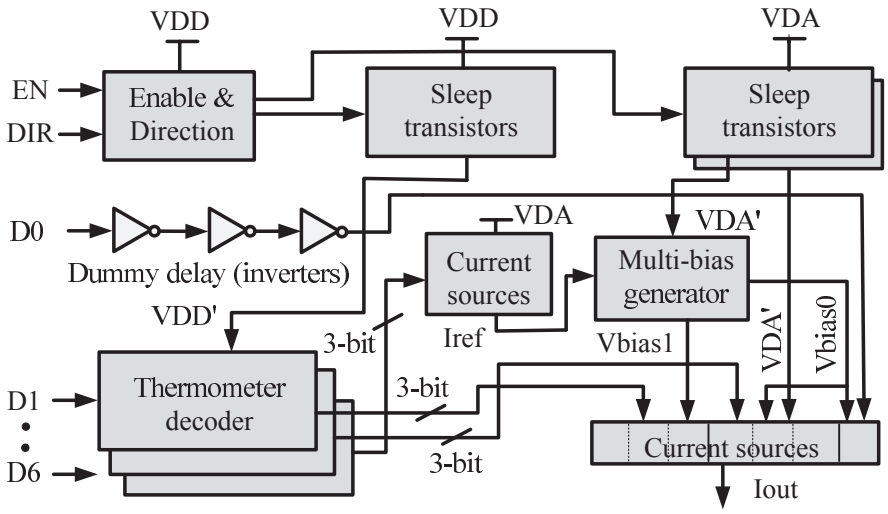


Figure 4.11 Block diagram representation of the source DAC.

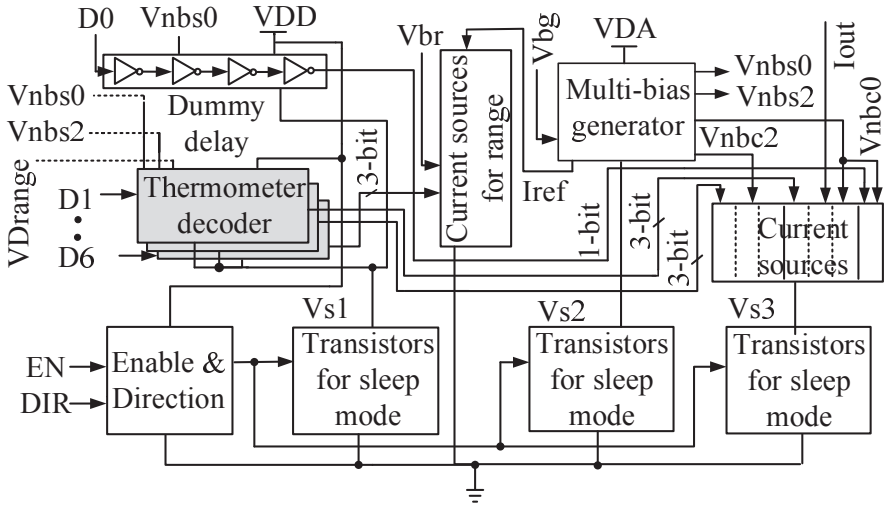


Figure 4.12 Architecture of the sink DAC.

The design principle of the sink DAC, as shown in Figure 4.12, follows the similar approach used in the source DAC. The DIR and EN signals select the direction and channel of the current (source or sink) respectively. Bits, D1-D6, are divided into three groups, D6-D5, D4-D3 and D2-D1, and thermometer decoded. This principle minimizes the number of row-column decoder and the transistor counts per decoder, hence, the area of each DAC. An inverter chain, consists of four inverters, matches the delay of D0 to those of D1-D4. The DAC operates in three maximum full-scale currents, 73.67, 147.33 and 221μA, which are set by the three levels of Iref. A small DAC, controlled by D6-D5, establishes the value of Iref and D4-D0 determine the main DAC current. Transistors for sleep mode operation are inserted between the respective analog and digital blocks, and supply ground to disable the

DAC when microstimulation is not performed. The required current magnitudes of half-sine and plateau half-sine pulses during anodic and cathodic phases are also set by these DACs.

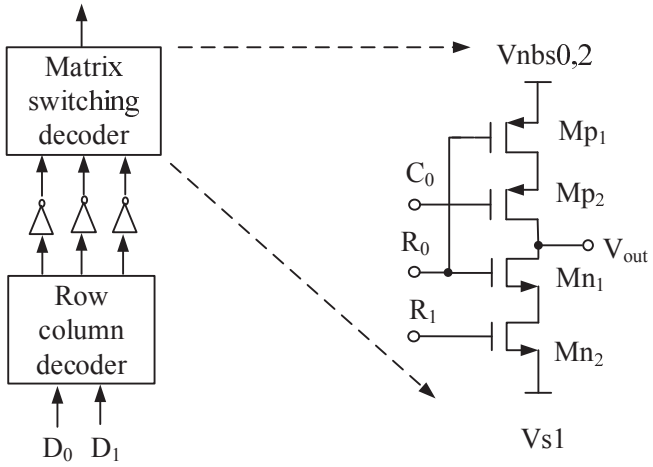


Figure 4.13 Block diagram representation of the thermometer decoder used in DAC realization and the modified matrix switching decoder.

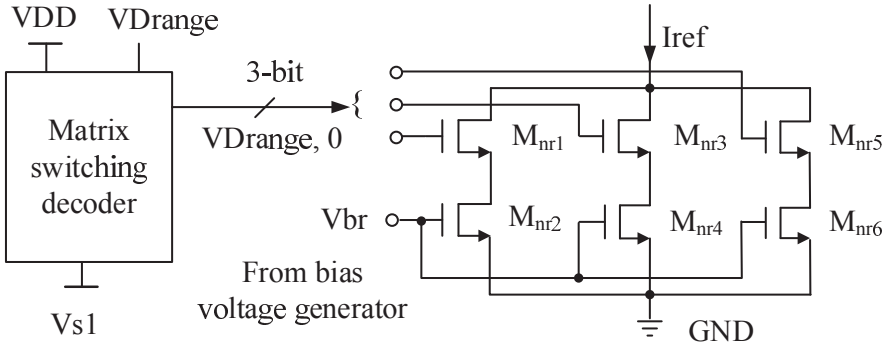


Figure 4.14 The 2-bit source DAC that sets 3 ranges of Iref for the 5-bit source DAC.

Figure 4.13 (shown on left) shows the architecture of the thermometer decoder used for switching the current sources in the DAC. In our segmented 2-bit thermometer decoder case, two transistors in the original matrix switching decoder, used in [119], have been found to be redundant. Therefore, the previous circuit has been modified to a 4-transistor model, which is presented in Figure 4.13 (shown on right). The 2-bit DAC, illustrated in Figure 4.14, is controlled by a 2-bit thermometer decoder and sets 3 different values of Iref, i.e., 19, 38, and 57μA. The transistors in each branch are connected in cascode configuration to increase the output resistance given by the following equation [120], [121]:

$$\begin{aligned} R_{out} &\equiv r_{nr1} + r_{nr2} + (g_{m_{nr1}} r_{nr1}) r_{nr2} \\ &\cong (g_{m_{nr1}} r_{nr1}) r_{nr2} \end{aligned} \tag{4.2}$$

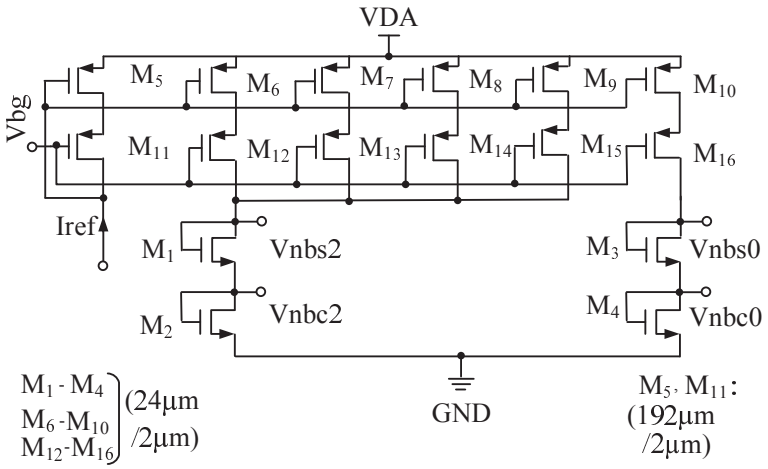


Figure 4.15 Transistor level representation of the multibias generator used to generate the needed voltages for current sources.

The multbias generator, presented in Figure 4.15, is biased by the reference current, Iref and generates the needed bias voltages, Vnbc0, Vnbc2, Vnbs0, and Vnbs2 for the current sources, shown in Figure 4.16 [118]. Transistors, M_5 and M_{11} with the reference bias current, Iref form wide swing cascode current mirrors with PMOS transistors, connected in cascode configuration in the parallel branches [120], [121]. All the NMOS and PMOS transistors are made of equal size for matching purpose, except M_5 and M_{11}, which are eight times bigger than the other transistors. Transistors, M_1 - M_4, M_6 - M_{10}, and M_{12} - M_{16} are equal and matched in dimension to those used in current sources.

Figure 4.16 demonstrates the circuit and block diagrams for 1LSB, 2LSB and 8LSB current

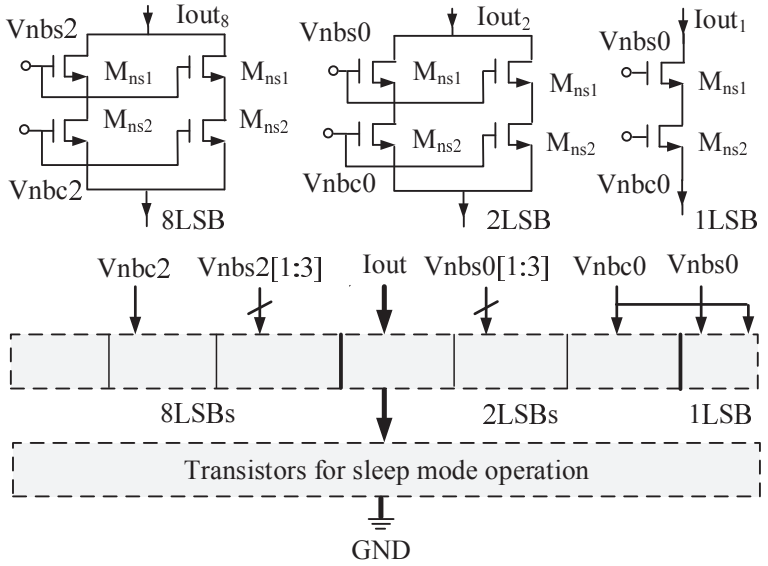


Figure 4.16 Circuit diagram of current sources used for sink DAC.

sources implemented in the 5-bit sink DAC Figure 4.12. Transistors in each branch are cascoded to increase the output impedance of current sources presented earlier. The total DAC output current is set by equation 4.3:

$$\text{Iout} = \text{I}_{8\text{LSB}}(2^0 b_6 + 2^0 b_5 + 2^0 b_4) + \text{I}_{2\text{LSB}}(2^0 b_3 + 2^0 b_2 + 2^0 b_1) + \text{I}_{1\text{LSB}} 2^0 b_0 \tag{4.3}$$

where,

$$(\text{b}_6, \text{b}_5, \text{b}_4) = f(\text{D4}, \text{D3}, \text{Vnbs2}, \text{Vnbc2}) \tag{4.4}$$

$$(\text{b}_3, \text{b}_2, \text{b}_1) = f(\text{D2}, \text{D1}, \text{Vnbs0}, \text{Vnbc0}) \tag{4.5}$$

$$\text{b}_0 = f(\text{D0}, \text{Vnbs0}, \text{Vnbc0}) \tag{4.6}$$

For Iref $= 57\mu$A, $\text{I}_{1\text{LSB}}$ becomes $\frac{\text{Iref}}{2^3}$, which is 7.125μA. For this $\text{I}_{1\text{LSB}}$, the generated full scale DAC current is $\text{I}_{1\text{LSB}}.(2^5 - 1) \approx 221\mu$A.

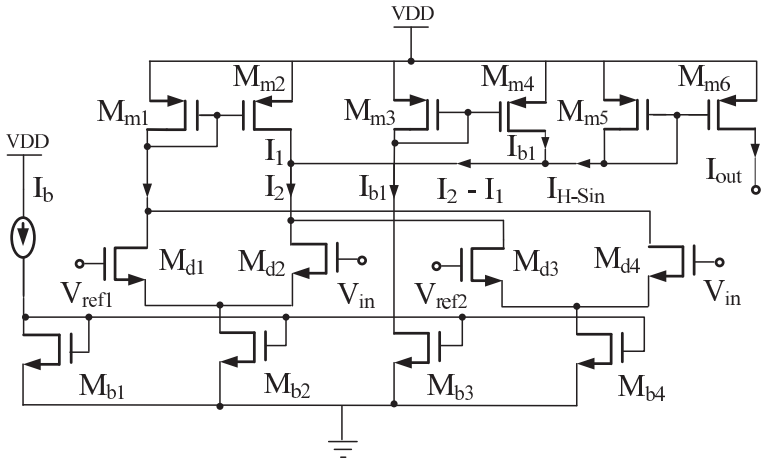


Figure 4.17 The schematic representation of the half-sine generator.

Half-sine pulse generator

The half-sine pulse generator, presented in Figure 4.17, follows the functional principle of the Gilbert cell [122]. The differential pair transistors, M_{d1}-M_{d4}, are biased in the subthreshold region to generate an approximate half-sine pulse according to the following equation [13].

$$\text{Ihsine} \propto \tanh(\frac{V_{in} - V_{ref1}}{2nV_T}) - \tanh(\frac{V_{in} - V_{ref2}}{2nV_T}) \tag{4.7}$$

where V_{in} is the ramp voltage input, which is common to two differential pairs and ranges between 720 to 920mV in our case, V_{ref1} and V_{ref2} are the fixed voltage levels, 720 and 920mV respectively, applied to the remaining inputs to the differential pairs, n is the slope factor, and V_T is the thermal voltage.

Ramp voltage generator

The width of the half-sine pulse, described previously, is modulated by the variation of the slope of the ramp voltage, $\frac{dV}{dt}$. The charging property of a capacitor, according to $\frac{dV}{dt} = \frac{I}{C}$ relation, has been utilized to generate such increasing ramp voltage. Setting dV and C to 200mV and 20pF respectively, the charging current needed for pulse duration dt of 20μS to 2mS ranges from 2 to 200nA. The circuit, demonstrated in Figure 4.18, meets this specification to generate nano scale currents, where the slope of the ramp, $\frac{dV}{dt} = \frac{I}{C}$, is programmable by varying, Iprog and output capacitor Cprog. At the beginning of generating the voltage ramp, Cprog is pre-charged to 720mV closing the switch, S_2, controlled by VinP2. This voltage increases linearly to 920mV when VinP1 closes the switch, S_1, and allows the nano-scale current, Icharge, to charge the capacitor. Icharge is generated subtracting, I_1 and I_2, the scaled versions of Iprog. A 2-bit thermometer decoder, switched by D7-D8 or D9-D10 and a 2-bit DAC set 3 different values of Iprog.

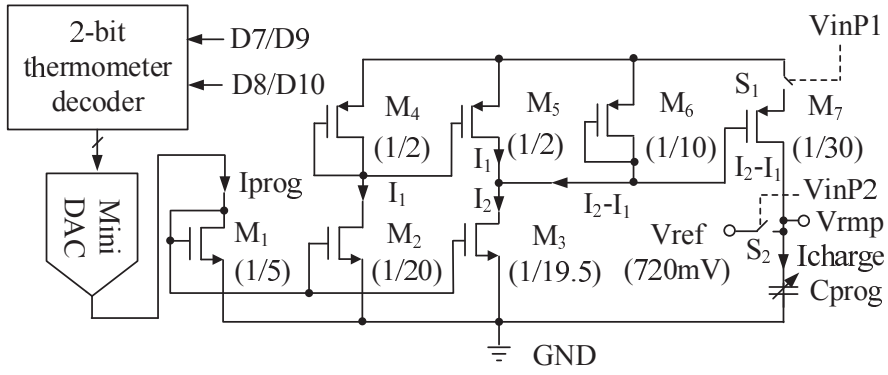


Figure 4.18 The circuit for programmable ramp voltage generator to generate increasing ramp voltage required to set the durations of half-sine and plateau half-sine pulses. In channel-3 and 4, a 20pF capacitor is integrated, and additional capacitors can be added externally to modulate the pulse width.

Plateau half-sine pulse generator

The compliance voltage for currents from DAC and half-sine pulse generator is increased to 3.3V using 1.2V/3.3V current mirror. The constant current from the DAC and the half-sine

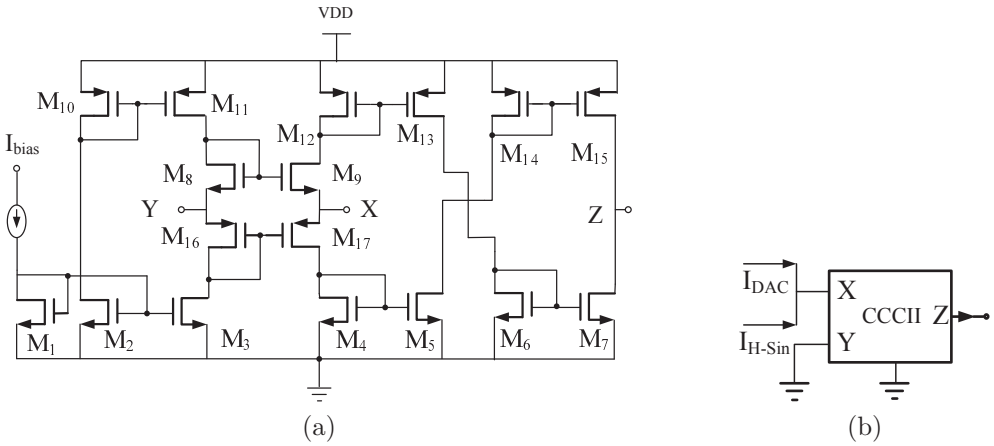


Figure 4.19 (a) Circuit for the second generation current conveyor before configuring as a current adder, and (b) block diagram representation of plateau half-sine pulse generator.

current pulse from the half-sine pulse generator in channel-3 and -4 are added using a second generation current conveyor [123], as presented in Figure 4.19(a), to obtain a plateau half-sine current pulse. The mixed translinear loop made of transistors M_8-M_9 and M_{16}-M_{17} works as the input cell. The output port is implemented using two cross coupled pairs of current mirrors, made of M_6-M_7 and M_{12}-M_{13}, and M_4-M_5 and M_{14}-M_{15}. The current that flows through port X is copied to port Z. For our application, currents from DAC and half-sine pulse generator are applied to port X as illustrated in Figure 4.19(b). The input port Y is connected to the ground. The generated plateau half-sine pulse is available at port Z. Mathematically,

$$\text{Ipsine(t)} = \text{Irect.(t)} + \text{Isine(t} - \text{t1)} \tag{4.8}$$

where t1=0 results in the perfect plateau-sine pulse with duration of T. However, shifting the relative position of the Isine(t-t1), where $-\frac{3T}{4} \leq \text{t1} \leq \frac{3T}{4}$, generates various waveforms which can be used in neural microstimulation to investigate an energy-optimum pulse.

1.2V/3.3V current mirror

1.2V/3.3V source- and sink-current mirrors, have been added in the output stage of each channel for supplying constant (DAC), half-sine, plateau-sine and other types of current waveform to the MED. Input stage of each of these cascode current mirrors [120], [121] is implemented using 1.2V transistors, and output stage is realized with 3.3V transistors and

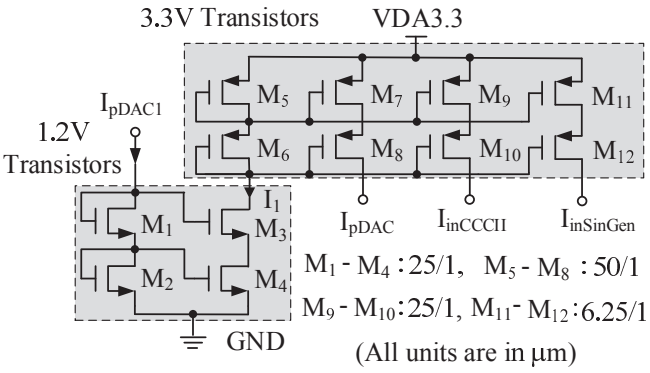


Figure 4.20 Circuit diagram of the 1.2V/3.3V source current mirror, connected in the output stage of each source DAC.

supplied with 3.3V to provide the required compliance voltage to the input stage of 3.3V/20V current mirror in the MED. Figure 4.20 illustrates the circuit diagram of the 1.2V/3.3V source current mirror added to the output of each source DAC. In the saturation region, all transistors in this design follow equation 4.9, which is shown below

$$I_{DS} = \frac{\mu_n C_{ox} \frac{W}{L}}{2}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{4.9}$$

Where, the symbols have their usual meanings. The relation among the branch currents I_{pDAC1}, I_1, I_{pDAC}, $I_{inCCCII}$, and $I_{inSinGen}$ is established by the following equations

$$\frac{I_{pDAC1}}{I_1} \approx \frac{(W/L)_2}{(W/L)_4} \qquad \frac{I_1}{I_{pDAC}} \approx \frac{(W/L)_5}{(W/L)_7}$$

$$\frac{I_1}{I_{inCCCII}} \approx \frac{(W/L)_5}{(W/L)_9} \qquad \frac{I_1}{I_{inSinGen}} \approx \frac{(W/L)_5}{(W/L)_{11}}$$

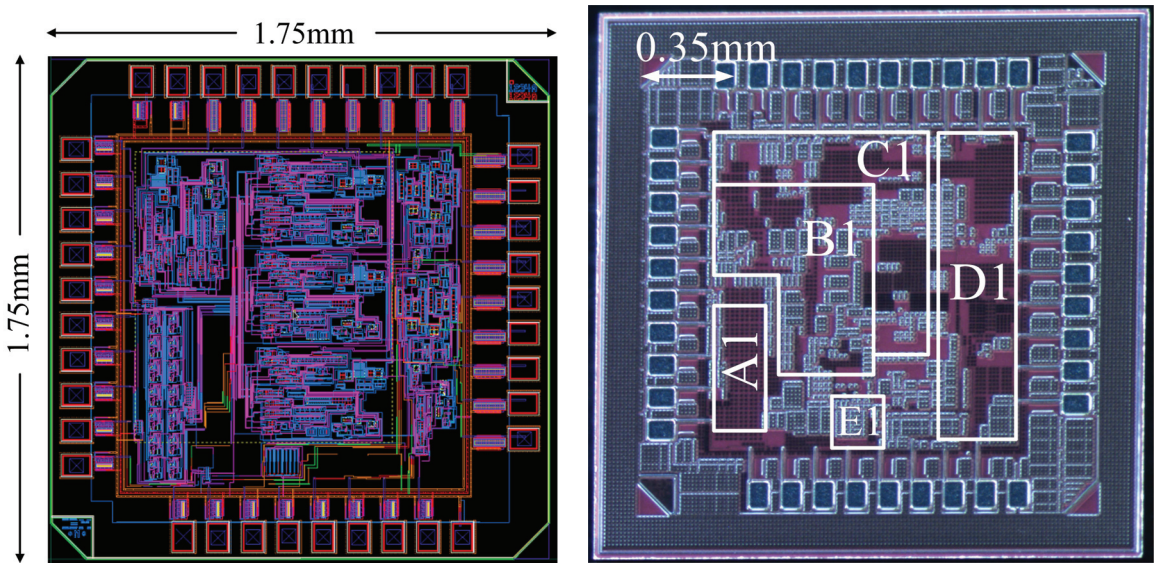
Where, I_{pDAC} is the exact copy of the DAC current I_{pDAC1}; $I_{inCCCII}$ is the scaled down DAC current by half, which is applied to the X port of the CCCII and added with the half-sine current pulse to generate plateau half-sine current pulse; and $I_{inSinGen}$ is the reference current (I_b in Figure 4.17) for the half-sine current pulse generator.

Modified versions of this current mirror of both source and sink types have been added at the outputs of sink DACs, plateau half-sine (CCCII) and half-sine (Gilbert) current pulse generators, and in-between the latter.

4.3.4 Post-layout simulation and measurement results

The layout and the microphotograph of the fabricated waveform generator (ICGPMSTG) are shown in Figure 4.21. While laying-out the chip, good layout design rules such as multi-gate fingering, inter-digitized style, multiple contacts etc. have been followed throughout the whole layout of the chip, especially for matching transistors in analog blocks. The digital parts have been implemented using 1.2V transistors to minimize the power consumption.

The nominal voltages VDD, VDA, VDD33 for the SG were set to 1.2, 1.2, and 3.3V re-



(a) (b)

Figure 4.21 The ICGPMSTG chip: The (a) layout and (b) microphotograph of the fabricated chip with floor plan: A1-Digital controller; B1-DACs and reference generator; C1-Current mirrors; D1-Ramp voltage generators (RMPGs), half-sine pulse generators (HSGs), plateau-sine generators (PSGs - CCCII), and current mirrors; and E1-20pF capacitors and 2-bit DACs.

spectively while performing post-layout simulation. Results show that the full-scale currents in each channel for constant (DAC current), half-sine, and plateau-sine pulse waveforms are 221, 221, and 203μA respectively. The DNL and INL of each DAC from the post-layout simulations are 0.29 and 0.75 LSB respectively. The half-sine and plateau-sine pulses, plotted in Figure 4.22, were generated for different values of charging current, (Icharge in Figure 4.18) which are 20.51, 50, and 167nA for Cprog of 20pF integrated capacitor, dV of 200mV, and dt of 195, 80, and 24μS respectively. These results clearly verify the theoretical relation $\frac{dV}{dt} = \frac{I}{C}$.

The post-layout simulation results also prove that the widths of both pulses are inversely proportional to the charging current and directly proportional to the output capacitor. The

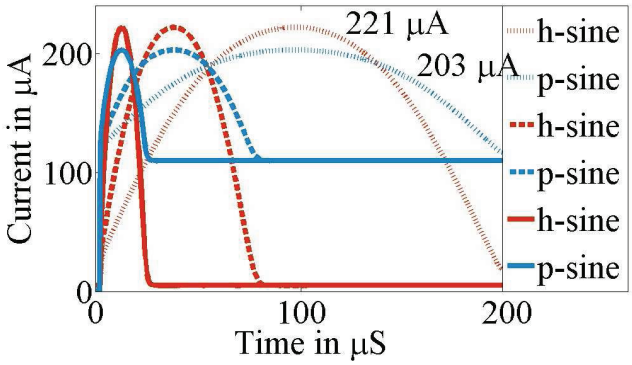


Figure 4.22 Variation of half-sine (h-sine)- and plateau-sine (p-sine)- pulse widths with different charging currents of the capacitor in the ramp generator.

Table 4.1 Charge quantity (nC) delivered by the half-sine and plateau-sine pulses for their respective full scale currents.

Pulse-type	Rectangular			Half-sine			Plateau-sine		
Full-scale current (μA)	221			221			203		
Pulse-width (μS)	24	80	195	24	80	195	24	80	195
Charge (nC)	5.3	17.7	43.1	3.38	11.26	27.44	4.07	13.57	33.07

charge quantities of these pulses for different pulse-widths and their respective full-scale currents are illustrated in Table 4.1.

Experimental results show that the measured quiescent and dynamic power consumptions of the stimuli-generator chip are 1.92 and 0.64mW respectively. Clock frequency of 50kHz was applied during experiments and measurements. Control signals were applied from the Tektronix 714 logic analyzer and the IGLOO nano FPGA board. Figure 4.23 shows the control signals used for generating various waveforms at the outputs of the stimuli-generator. The full-scale DAC current of 210μA was obtained for VDA of 1.45V. Investigation shows that the reference generator circuits are unable to provide the required voltages and currents, when VDA is set to 1.2V. While generating constant, half-sine, plateau-sine and various waveforms from the stimuli-generator, resistors of 1kΩ were used as loads. Pulse widths were modulated varying the charging currents and capacitances in Ch3 and Ch4 respectively. Higher pulse width of up to 500μS was obtained connecting external capacitors in parallel with the integrated 20pF capacitor/channel. Current for the half-sine pulse was adjusted to 200, 175, 140 and 122 μA (approx.) in the first case, but kept constant at 110μA in the second case. Figure 4.24 illustrates the oscilloscope graphs of half-sine pulse-width variations measured across 1kΩ resistors for various charging currents and capacitances.

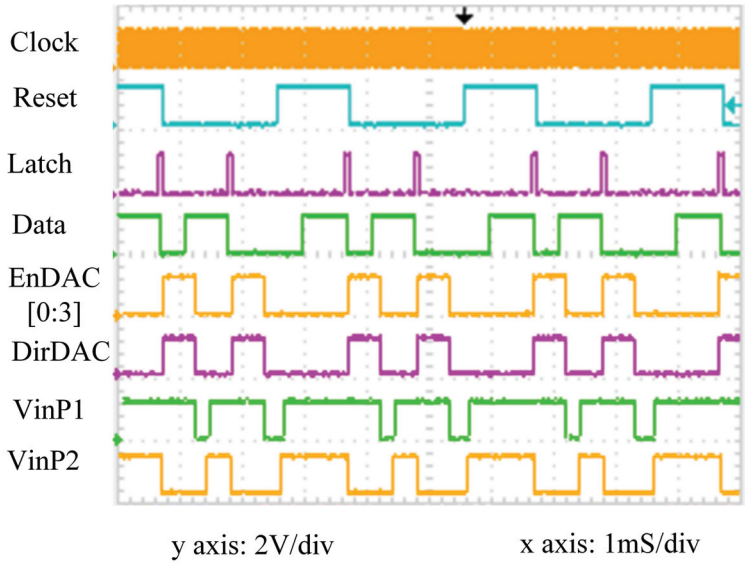


Figure 4.23 Control signals applied to the stimuli-generator chip for generating source constant current (from DAC), half-sine and plateau-sine pulses.

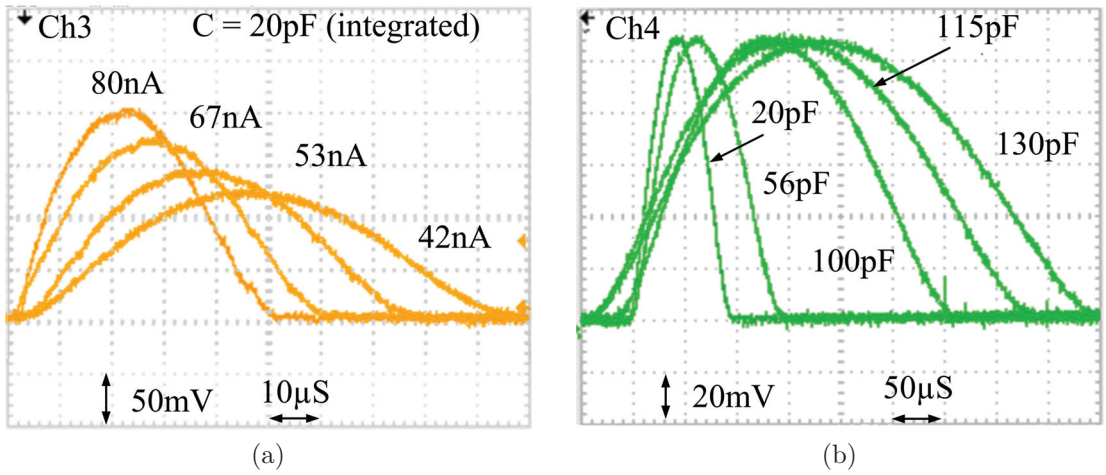


Figure 4.24 Oscilloscope graphs of pulse-width variations of measured HS pulses: (a) for multiple charging currents and (b) for various capacitances.

Plateau-sine pulses in Ch3 and 4 were generated, following the similar approach as in HS pulse case. The oscilloscope graphs of the measured plateau-sine pulses, presented in Figure 4.25, elucidate the pulse-width variations for several capacitances. The amplitude of each generated I_{PS} pulse, measured across a 1kΩ resistor, was 132μA.

In addition to the constant current, half-sine, and plateau-sine pulses, stimuli-generator is also able to produce some other types of waveform, exhibited in Figure 4.26, shifting the position and changing the pulse-width of the half-sine pulse relative to the rectangular (con-

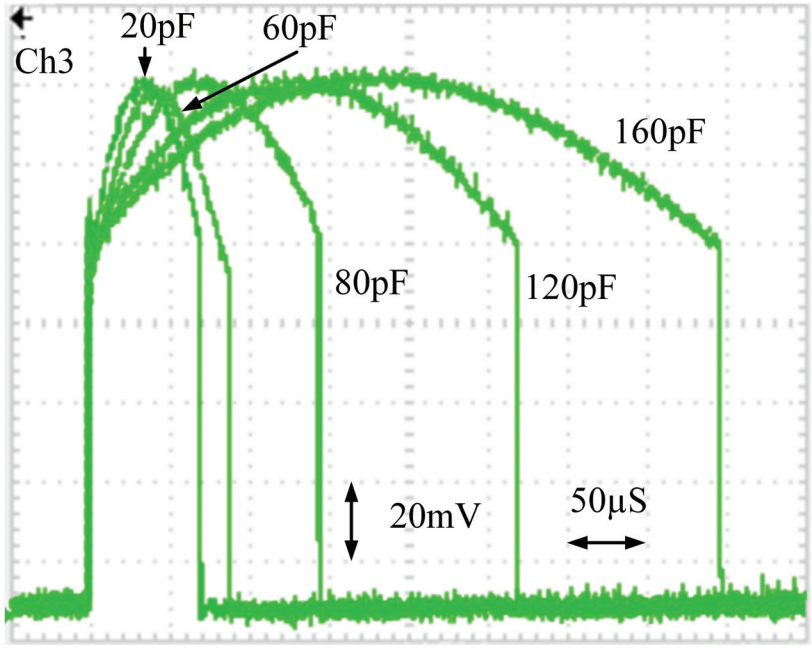


Figure 4.25 Pulse-width variations of the measured PS pulses in Ch3 of the SG for different capacitances.

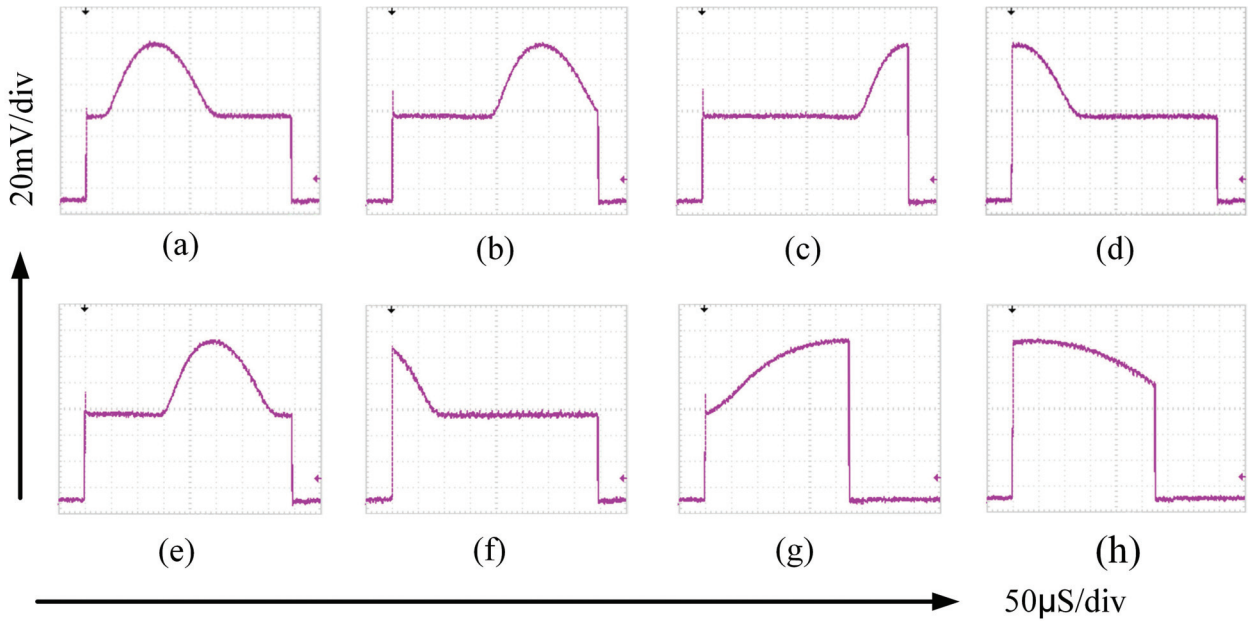


Figure 4.26 Oscilloscope traces of the various forms of current signals, measured across 1kΩ resistors, in Ch3 and 4 of the stimuli-generator chip.

stant current) pulse.

Table 4.2 summarizes the performance of the presented stimuli-generator in terms of post-

Table 4.2 Specifications and performance results summary.

Device	Stimuli-generator	
Parameters	Post-layout simulation results	Experimental results
Technology	IBM 0.13μm 1.2V/3.3V CMOS	
V_{DD}, V_{DA}, V_{DD33}, GND	1.2, 1.2, 3.3 and 0V	
Current waveform type	Rect., HS, PS, and others[a]	
ASIC die area	1.75 X 1.75mm^2	
Avg. quiescent power dissipation	2.37mW	1.92[b]and 3.66mW[c]
Dynamic power dissipation	-	0.64[b] and 1.54mW[c,d]
DNL and INL	0.29 and 0.75LSB	-
Current per channel (source/sink)	2.32 - 221μA[d,e]	$\leq$ 210μA[c,d]

[a] Figure 4.26.
[b,c] V_{DA} = 1.2 and 1.45V respectively.
[d] Constant current only and the amplitude is 210μA for other waveforms.
[e] f_{clock} = 50kHz.

layout simulation and experimental results. The measured quiescent power consumption, which is 1.92mW for the nominal value of VDA of 1.2V, is less than that calculated in the post-layout simulation. However, this measured value increased to 3.66mW, when VDA was increased to 1.45V to obtain full-scale DAC current, the measured value of which is 210μA. Power dissipation per channel is 3.66/4 = 915μW, and half-sine and plateau-sine pulse generators consume about 140μW power per channel, which is $\frac{140}{915}$x100 or 15.3% of total power consumed under no load condition. On the other hand, these two waveforms save 36% and 19% of the energy respectively compared to the rectangular pulse, considering the total areas under the curves. According to Robillard et al., half-sine pulse is able to save up to 44.8% [124] energy. Therefore, taking the additional power consumption to generate these waveforms into account, 3.7 to 29.5 % energy saving is possible, which, however, can vary depending on the design of circuits. Thus, a high-data rate compatible stimuli-generator, capable to stimulate hundreds of neural sites and implemented with these waveforms, can be a very effective solution to low-power implantable stimulator.

4.4 Conclusion

We presented in this chapter the proposed system, microstimulation module (MSM), and a novel 4-channel stimuli-generator (SG), which is designed to supply multiple energy-efficient

waveforms to the high-impedance microelectrode driver output-stage. This sub-system (SG) is fully integrated and designed in IBM 0.13μm 1.2V/3.3V CMOS process. The functionality of the stimuli-generator has been verified through both post-layout simulation and post-fabricated experimental results. The experimental results show that this unit is able to perform its target task. The reduced full-scale DAC currents issue, when the low-voltage analog parts are supplied with 1.2V (VDA), can be solved easily by adjusting the sizes of some transistors in the reference generator (RG) circuits.

However, some design considerations need to be addressed here. Power has been minimized at the design level, where the digital, mixed-signal, and most of the analog components are supplied with 1.2V. Moreover, we used one 7-bit register to upload data to all DACs and disable any channel which is not used for stimulation to save power. In addition to the power saving, we also implemented mixed multibias and thermometer coded topology to save area. A separate reference voltage generation circuit is added for every DAC in each channel, in our case, to avoid the risks. More area and power can be saved dedicating one bias circuit for all DACs, as in the case of original design of the multibias bias DAC. However, owing to the area limitation as well as to limit the power consumption, pulse types other than the rectangular pulse are implemented only in Ch3 and Ch4. Flexibility is achieved using both source and sink current sources in all 4 channels, and providing external terminals to Ch3 and Ch4 to connect additional off-chip capacitors for varying widths of non-rectangular pulse forms. The fabricated SG chips were tested to validate the functionality before the assembly of the MSM.

CHAPTER 5

HIGH-VOLTAGE COMPLIANT MICROELECTRODE DRIVERS

5.1 Introduction

Microelectrode array is an essential interface to apply the microstimulation current from the microstimulator to biological tissues. The impedance of the microelectrode is highly variable; complex in nature; and depends on the electrode-geometry and materials used to fabricate it and coat the exposed tip area. This impedance is also affected by the stimulus parameters, such as stimulation frequency, due to the double layer capacitance formed between the electrode surface and the surrounding medium. Various research groups reported that the impedance of a Silicon-based microelectrode can range between 70 kΩ to 400kΩ for intracortical microstimulation [40], [41], [99], [125]. Stimulation current of about 150μA [7] for intracortical sites through microelectrode of such high-impedance justifies the necessity of large-voltage compliance across microelectrodes, which may reach up to 15 V [13]. This required amount of voltage can be delivered from the output stage of a microstimulator, namely microelectrode array driver (MED). For the safety of biological tissues and long life of the microstimulator, it is also necessary to limit the power and heat dissipations of the implantable device and across the electrode-tissue impedance. As a possible solution, low-power standard CMOS technologies can be used to design the MEA. However, the drawback is that the deliverable voltage to the electrodes-tissue interface is also limited by the maximum breakdown voltages of available transistors used in these technologies. Moreover, generated high-voltage using low-voltage CMOS process stresses the transistors, which can cause device failure and make the system unreliable for chronic implantation. Therefore, mixed low- and high-voltage CMOS/DMOS technologies (called mid-voltage) can be a proper choice for this application, where digital circuitries can be designed using low-voltage transistors to limit power dissipation and high-voltage across the output microstimulation channels can be met utilizing high-voltage transistors.

A charge balanced biphasic stimulation is necessary to prevent the release of toxic ions in the biological tissues caused by irreversible Faradic electrochemical reactions [30]. Current-mode stimulation is usually preferred due to its direct control capability over the amount of charge delivered.

The functionality of the microstimulator can be greatly enhanced making the MED highly configurable to perform various types of microstimulations. This configurability is related

to: (i) the precision of amplitudes and ranges of stimulation current, (ii) the capability of delivering monopolar and bipolar stimulations, (iii) types of stimulation waveform to be provided, (iv) deliverable compliance voltage across microelectrode-tissue interface impedance, (v) charge-balanced microstimulation, (vi) the ability to use either current source or sink, and (vii) monitoring voltage across microelectrode-tissue interface.

Several microstimulators have addressed the compliance-voltage issue. Coulombe et al. have designed and implemented a highly-flexible microstimulation system, but it lacks high-voltage compliance [7]. The prototype with high-output impedance developed by Ghovanloo et al. allows 5V compliance voltage at the output channels [8]. Ethier and Sawan have solved this high-voltage compliance issue but the system consumes high power due to the on-chip DC-DC up converter included in the output stage [13]. Recently, Louis et al. have developed a multi-chip neurostimulator based on two-wire protocol for visual prosthesis [126]. But, the authors have generalized the application and considered electrode impedance up to 60kΩ only. The wireless microstimulation prototype for retinal prosthesis, designed by Cihun et al., used electrode impedance of 10kΩ only [127].

For our proposed microstimulator, we have designed and fabricated two new high-impedance microelectrode array drivers. The original contributions are their low power consumptions, high-flexibilities, enhanced voltage compliances, and on-chip switch control abilities. Flexibility has been achieved fulfilling the criteria mentioned in this section previously, except the types of stimulation waveform to be provided, which belongs to stimuli-generator functionality. Switch-matrices, included into MEDs, allow maximum simultaneous monopolar or bipolar microstimulations. MEDs are integrated with on-chip switch control mechanism which reduces the number of external pads and the chip dimension. Digital circuitries or the switch controllers, implemented using 5V components, are supplied by 3.3V to reduce the power consumption. High-voltage switch arrays and cross-coupled current mirrors are realized with 20V transistors to obtain high voltage compliance (10V/phase, 20V (anodic and cathodic phases)). The functional blocks of these output stages (MEDs) [109]-[112] are detailed with their performance analyses in section 5.2. Post-layout simulation and experimental results are presented in section 5.4. Finally, we conclude with a summary and suggestions for future works.

5.2 Proposed microelectrode drivers

The first high-impedance microelectrode array driver (MED1) is presented in Figure 5.1. It delivers one microstimulation current level to high-impedance microelectrode array with required compliance voltage.

The major building blocks, shown in Figure 5.1, are two 3.3V/20V current mirrors, a 32-bit high-voltage level shifter, an array of 32 high-voltage switches (called switch-matrix), and a 32-bit serial-in parallel-out shift register. The switch-matrix connects any microelectrode

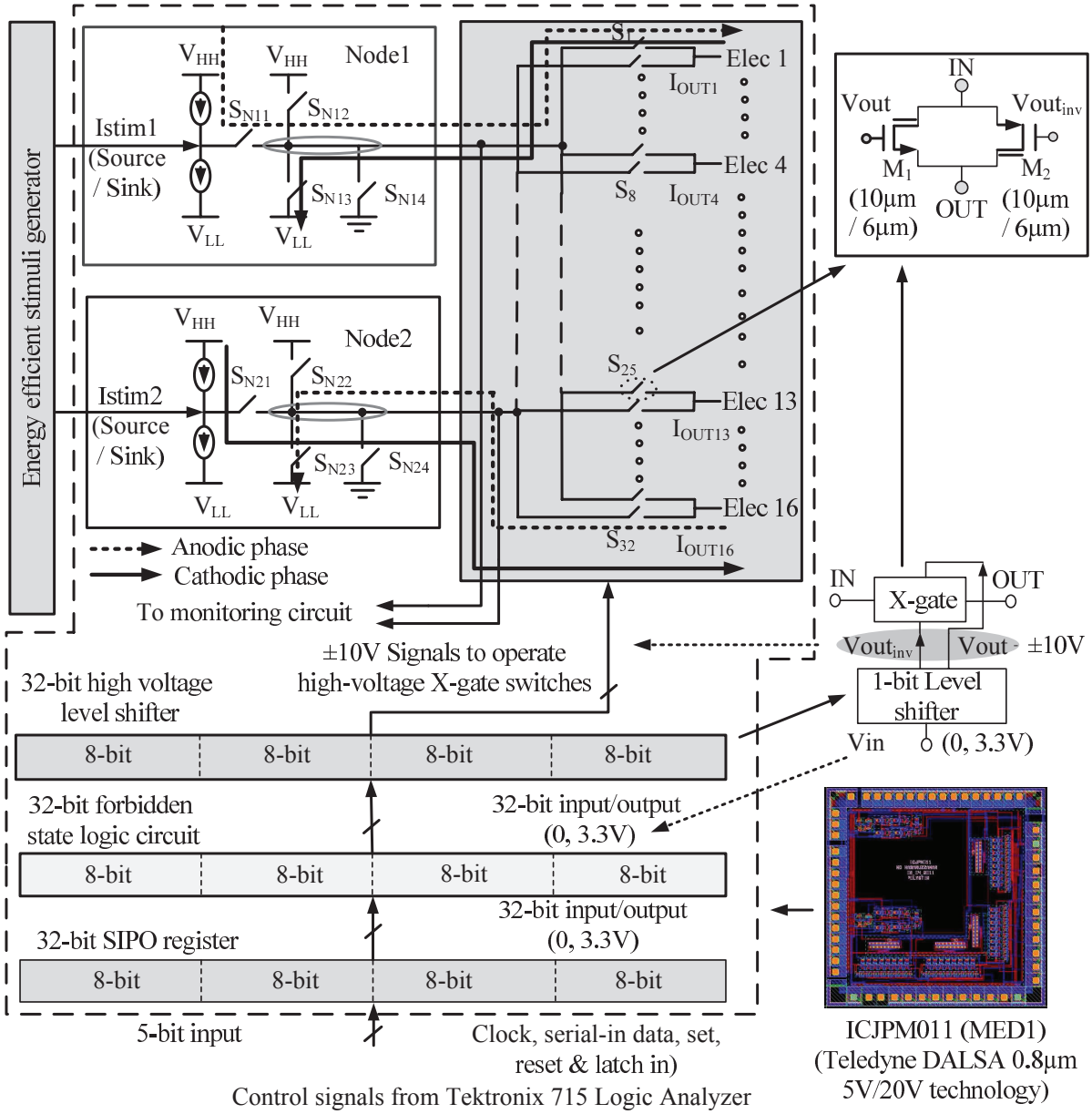


Figure 5.1 Architecture of the first high-impedance microelectrode driver. The 32-bit register and the forbidden state logic circuits are implemented using low-voltage digital components. The other functional blocks are analog.

to any of two nodes, defined as Node1 and Node2 in the figure. Switches, S_{N11}...S_{N24} connect each of these nodes to the power supplies, V_{HH}, V_{LL}, and GND or input stimulation current source (or sink), (Istim1, 2). Charge-balanced biphasic stimulation is achieved using

the positive- and negative- supply rails. This principle also rejects DC offset voltage across electrode-tissue interface impedance and avoids the use of output capacitors. An independent inductive-link front end power recovery unit along with DC-DC step-up converter has been designed to generate these supply voltages. The switch-matrix is driven through 32 high-voltage level shifters and control signals are applied from a 32-bit serial-in parallel-out shift register. Between the register block and 32-bit high-voltage level shifter, forbidden state logic circuits are included to prevent the electrodes from connecting to both of the nodes simultaneously. All low voltage digital circuits are supplied by 3.3V to reduce the power consumption and this supply voltage reduction from 5V to 3.3V does not deteriorate their performances. The microelectrode driver can deliver only one amplitude of current from one node to all electrodes.

The second version of this module (MED2), illustrated in Figure 5.2, is comprised of similar building blocks used in the first MED. The superiority of the second MED over the first one is the enhanced ability to perform simultaneous microstimulation to sixteen electrodes with four different levels of current. To accomplish this task, 32 switches are segmented into four different groups, where each group is dedicated for connecting four microelectrodes of a row or a column. Number of input stimulation current channels has been increased to four (Istim1....Istim4). Monitoring differential voltage across any electrode is performed by selecting two nodes (such as, Node1 and Node2) from the respective group.

$Vout$ and $Vout_{inv}$ are two outputs of each 1-bit high-voltage level shifter presented in Figure 5.6.

Both MEDs, demonstrated in Figures 5.1 and 5.2, are designed, laid-out, and fabricated in Teledyne DALSA $0.8\mu m$ 5V/20V CMOS/DMOS technology. The working principles of the functional blocks are illustrated in Figure 5.3 - Figure 5.13 with the corresponding circuit diagrams and the post-layout simulation results. The specifications of two MEDs are presented in Table 5.2. Post-layout simulation and measurement results of the fabricated microchips are included in section 5.4.

5.2.1 32-bit serial-in parallel-out shift register

The 32-bit serial-in parallel-out (SIPO) shift register sends control signals to the high-voltage switch-array through 32-bit high-voltage level shifter. The 32-bit SIPO register consists of D-type Flip-Flops (FFs) and is divided into four 8-bit SIPO shift registers to increase the data rate. Figure 5.3(a) presents the architecture of the 8-bit SIPO register. Data is provided serially and separately to each of these 8-bit register blocks. The first stage of each 8-bit register functions as an 8-bit serial-in serial-out (SISO) shift register. The control signals to drive this stage, i.e., clock, reset, set, and serial-in data can be applied externally to the chip

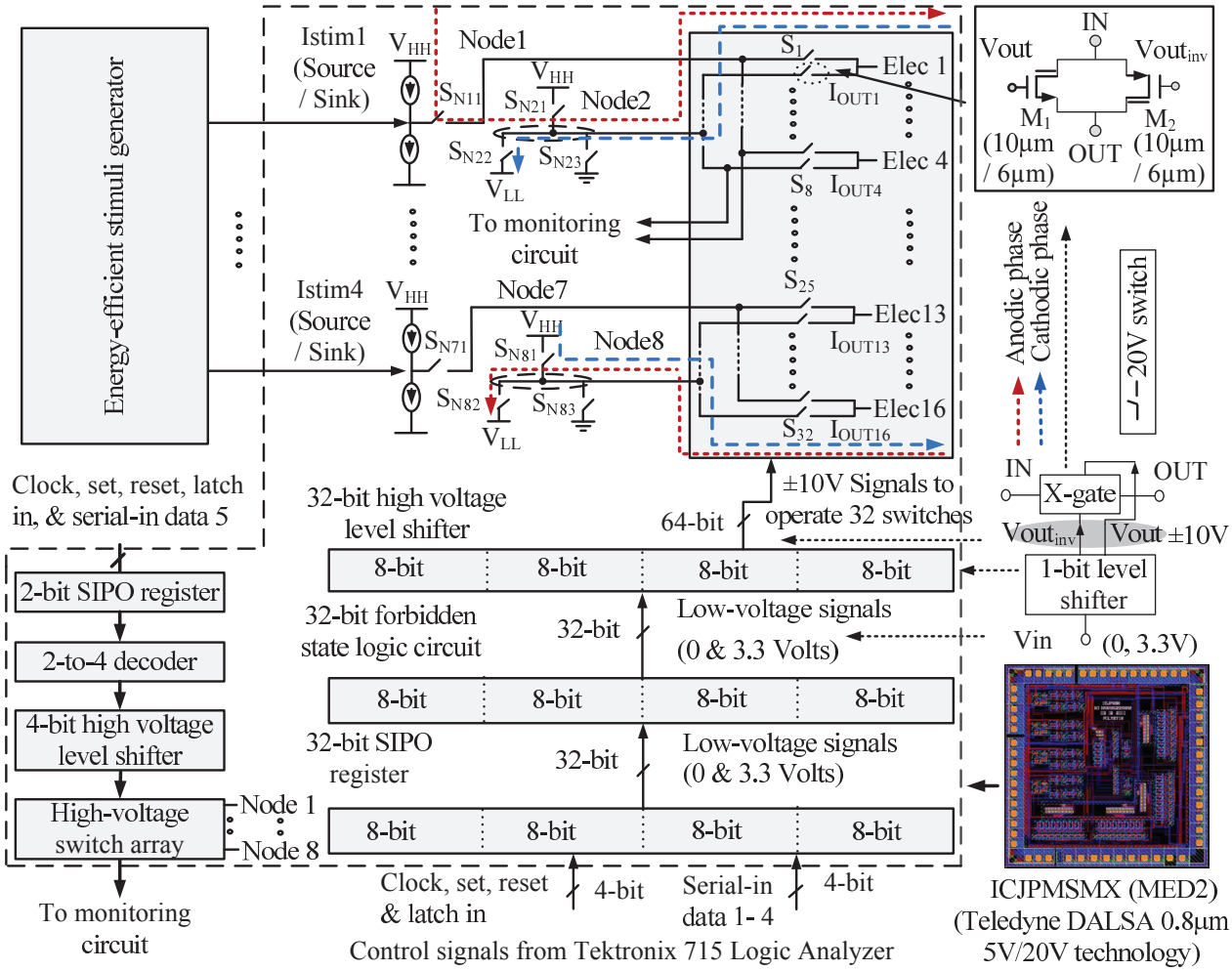


Figure 5.2 Architecture of the second high-impedance microelectrode driver. This MED can deliver four different stimulation current levels simultaneously.

from any commercial instrument, such as Tektronix 715 Logic Analyzer or an any controller, such as a field programmable gate array (FPGA). In this stage, data is transferred from one FF to the next one at the rising edge of each clock signal and the first set of data is available at the output of last FF after eight clock pulses. The second stage operates as an 8-bit parallel-in parallel-out shift register and at the rising edge of a latch signal which appears after eight clock signals, data from the previous stage is transferred to the output of each FF. These two-stages function as an 8-bit serial-in parallel-out (SIPO) shift register.

5.2.2 Forbidden state logic circuit

Any one of the stimulation current sources or sinks (Istim1, 2) (Istim1 - Istim4 in MED2); or the power supplies ±10V (V_{HH}, V_{LL}) and 0V (GND) can be connected to two nodes defined

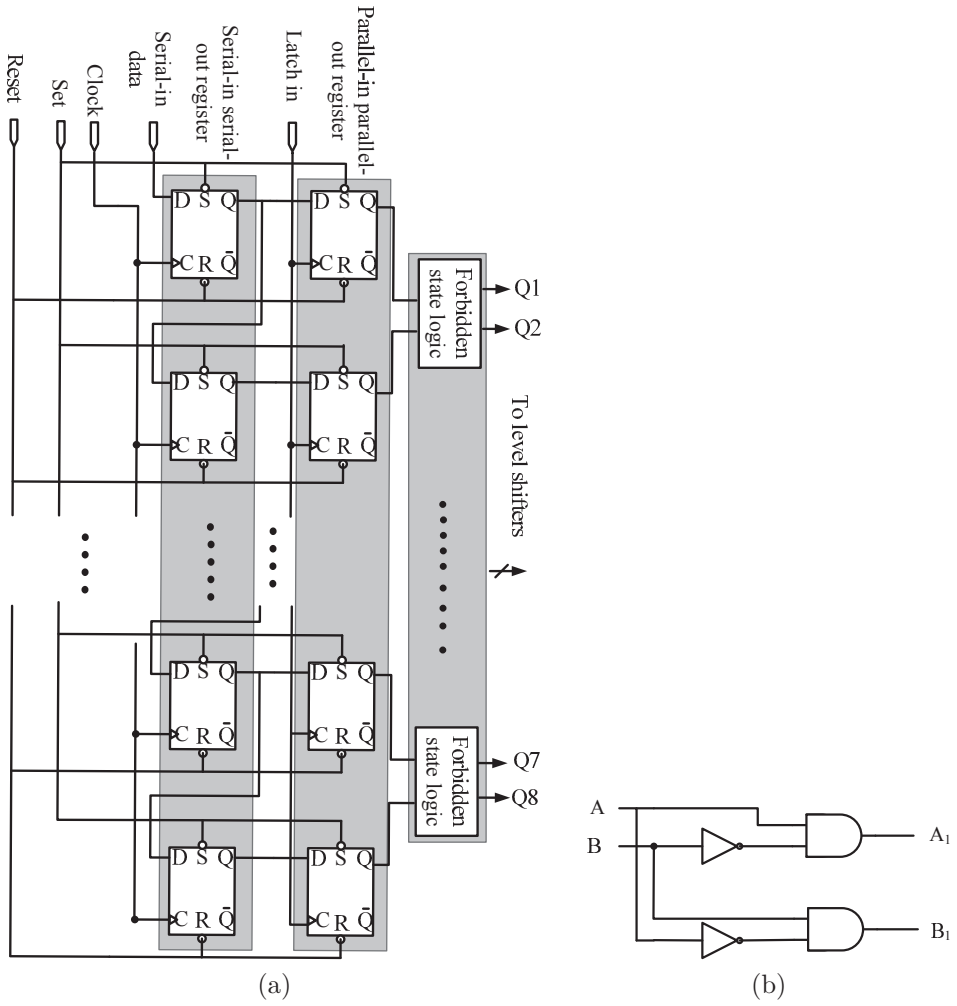


Figure 5.3 (a) Block diagram of 8-bit serial-in parallel-out shift register. The forbidden state logic circuits are added to the output stage of the register. (b) Circuit diagram of forbidden state logic circuit.

as, Node1 and Node2 in Figure 5.1 (Node1- Node8 in MED2 as illustrated in Figure 5.2), engaging switches S_{N11}...S_{N24} (S_{N11}...S_{N83} in MED2). In the switch-matrix array, each two consecutive switches (from the top or bottom) are assigned for connecting a microelectrode of the 4 by 4 electrode-matrix to any one of two nodes. The precision of the stimulation current level through the high electrode-tissue interface impedance, while performing monopolar- or bipolar-stimulation, can be secured through proper operations of these two switches. Enabling them simultaneously causes a short circuit between the highest to the lowest potentials resulting in a large amount of current to flow and this accidental improper operation needs to be avoided. Addition of the forbidden state logic circuits (FSLCs) at the output stage of the 8-bit register prevents this hazard. Post-layout simulation and measurement results manifest that, in case of logic high to both inputs of the FSLCs, stimulation currents do not

pass through corresponding switches and outputs remain unaffected in case of bit-error. The implementation and working principle of the FSLC are illustrated in the circuit diagram and the truth table, shown in Figure 5.3(b) and Table 5.1 respectively.

The performance of 8-bit SIPO register (building block for the 32-bit register) and the

Table 5.1 Truth table for forbidden state logic circuit.

A Input1	B Input2	A_1 Output1	B_1 Output2
0	0	0	0
0	1	0	1
1	0	1	0
1	1	0	0

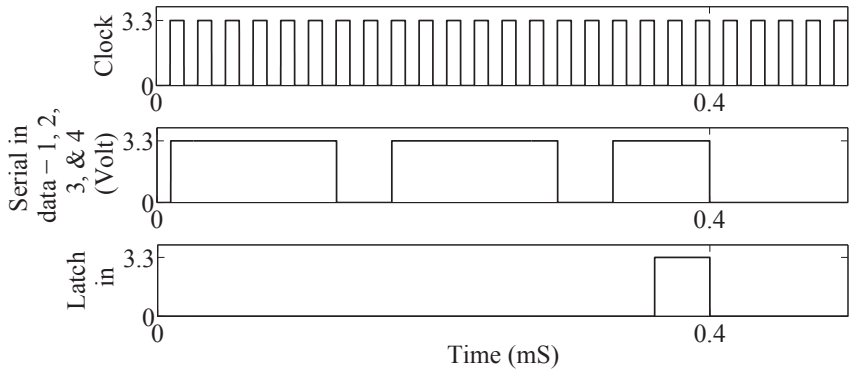


Figure 5.4 Input control signals: Clock, serial-in data and latch-in to 32-bit serial-in parallel-out shift register. Each signal is of amplitude 3.3V.

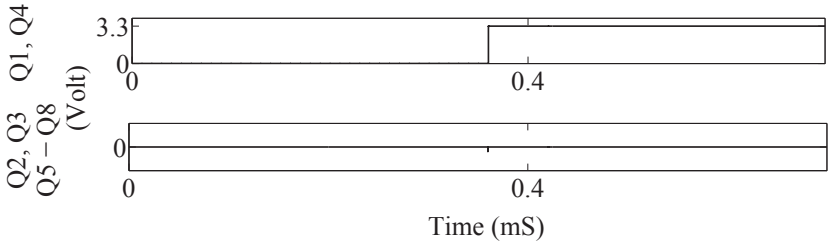


Figure 5.5 Signals from each 8-bit serial-in parallel-out shift register for controlling 32 high-voltage switches in the switch matrix.

forbidden state logic circuits have been verified through post-layout simulations before microfabrication. The 8-bit shift register is able to operate with maximum clock frequency of

250kHz. Figure 5.4 presents the control signals applied to four 8-bit serial-in parallel-out shift registers with clock frequency at 50kHz. Serial-in data-1, 2, 3, & 4 are input data signals to four 8-bit SIPO registers. Similitude in four serial data stream has been maintained for sending logic high (3.3V) to Q1 and Q4 of each 8-bit SIPO registers keeping the rest of the outputs (Q2, Q3 and Q5 - Q8) low for 0.7mS (Figure 5.5). This maneuver connects Node1 to I_{OUT1}, I_{OUT5}, I_{OUT9}, and I_{OUT13}; and Node2 to I_{OUT2}, I_{OUT6}, I_{OUT10}, and I_{OUT14} disabling other outputs. Data become available at the outputs of all registers when latch in signal was applied to the second stages of all registers as illustrated in Figure 5.3. Signals Q1 - Q8 are the final outputs from the forbidden state logic circuits. Selection of outputs (I_{OUT1},...I_{OUT16}) and their connectivity to different nodes (Node1-Node2 in MED1 and Node1-Node8 in MED2) can be updated by changing serial-in data pattern.

5.2.3 High-voltage level shifter

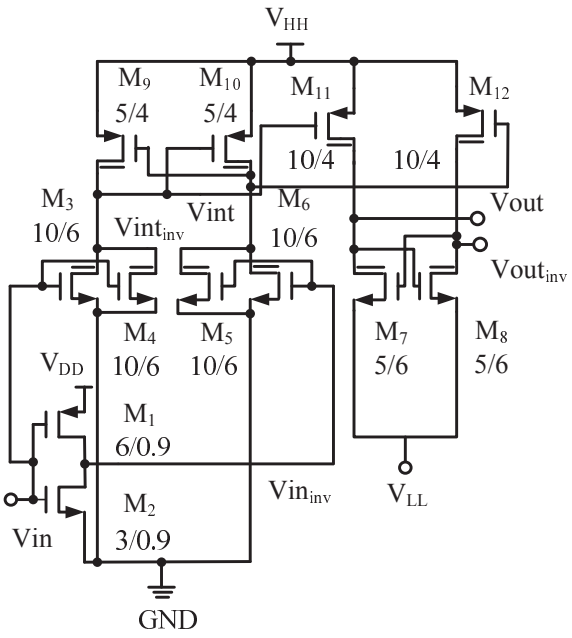


Figure 5.6 High-voltage level shifter implemented using 5V transistors, M_1-M_2, 20V single-side (drain) extended NMOS transistors, M_3-M_8, and PMOS transistors, M_9-M_{12}. The dimensions of all transistors are in μm / μm.

The level shifter [13], demonstrated in Figure 5.6, has been added at each output of the 32-bit forbidden state logic circuit for DC-DC up conversion of low-voltage signals. Ignoring the inverter at the input stage, the next two stages are required to convert 3.3 and 0 Volts to $\pm$10 Volts in two different steps. To enhance the output swing and switching speed, conventional cross-coupled architecture with positive feedback [128] has been used. This

circuit is comprised of 5V transistors (M_1-M_2), and 20V single-side drain extended transistors (M_3-M_{12}) [129]. The isolated bulks of the high-voltage NMOS transistors are connected to their respective source terminals. These 3-terminal transistors have gate lengths of 6μm and are made in deep N-well. On the other hand, the high-voltage PMOS transistors are 4-terminal devices, and their bulks are not isolated and need to be connected to the highest potential of the circuit. This circuit converts 3.3 and 0 Volts to the respective high-voltage levels, $\pm$10 Volts, to provide connection between two nodes (eight nodes in MED2) and the microelectrodes. This level-up shifter has also been used to operate the high-voltage switches, S_{N11}...S_{N24} (also the respective switches at Node1-Node8 in MED2), dedicated for connecting Node1 and Node2 in Figure 5.1 to input stimulation current source (or sink), (Istim1, 2) and power supplies, V_{HH}, V_{LL}, and GND. Three steps are required to convert low-level signals, 3.3 and 0 Volts into $\pm$10 Volts. The inverter made up of transistors M_1-M_2 in the first stage, inverts low-voltage signals, 3.3 and 0 Volts, in the first step of the conversion process. These inverted signals, in the second step, are then converted to 10 and 0 Volts respectively by the second stage, consists of transistors M_3-M_6 and M_9-M_{10}. The last stage, constructed by transistors M_7-M_8 and M_{11}-M_{12}, generates $\pm$10 Volts from 10 and 0 Volt signals respectively.

Figure 5.7 illustrates the transient post-layout simulation in Cadence of the high-voltage

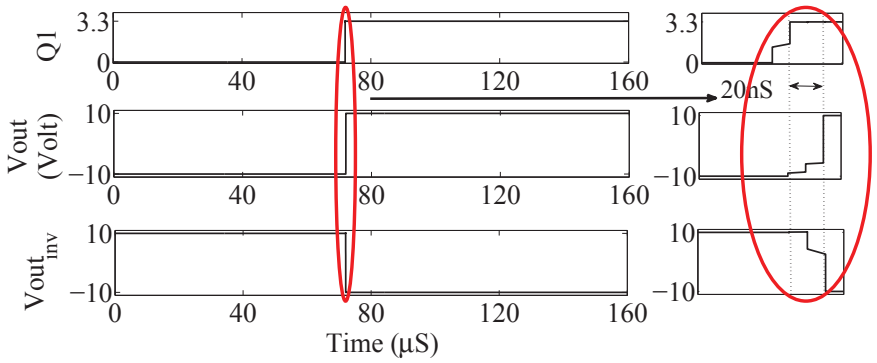


Figure 5.7 The post-layout transient simulation results: output signals from the high-voltage level shifter for 160 μS. The input signal (Q1) is provided from the first output of an 8-bit serial-in parallel-out shift register (including the forbidden state logic circuit).

level shifter for 160μS, which verifies the functionality of this level shifter. Signal from the first output of an 8-bit serial-in parallel-out shift register, Q1, is directly applied to the input of the level-shifter. Q1 remains low till 72μS switching M_2-M_4 off, and M_1 on. The output of the first stage, $V_{in_{inv}}$ goes high and turns on transistor, M_5-M_6, which in turn brings the node voltage of second stage, V_{int} down to 0V. The high-voltage pull-up PMOS transistor, M_9 is turned on by this low level signal and the node voltage $V_{int_{inv}}$ increases to 10V, which switches off PMOS transistor, M_{10} reinforcing V_{int} to 0V. M_{12} and M_{11} are switched on and

off states by V_{int} and $V_{int_{inv}}$ respectively until Q1 goes high. The third stage is supplied by ±10 Volts rather than 10 and 0 Volts and follows similar functional principle of the second stage. Till 72μS, the node voltages, V_{out} and $V_{out_{inv}}$ in the third stage remain -10 and 10 Volts respectively. The signals of all internal and external nodes reverse the polarities as soon as Q1 switches to 3.3V and remain in the same states till 160μS. Enlarged view of these transitions depicts the delay, which is 20nS, between Q1 and V_{out}. The level shifter has been realized keeping its speed in conformity with that of the register.

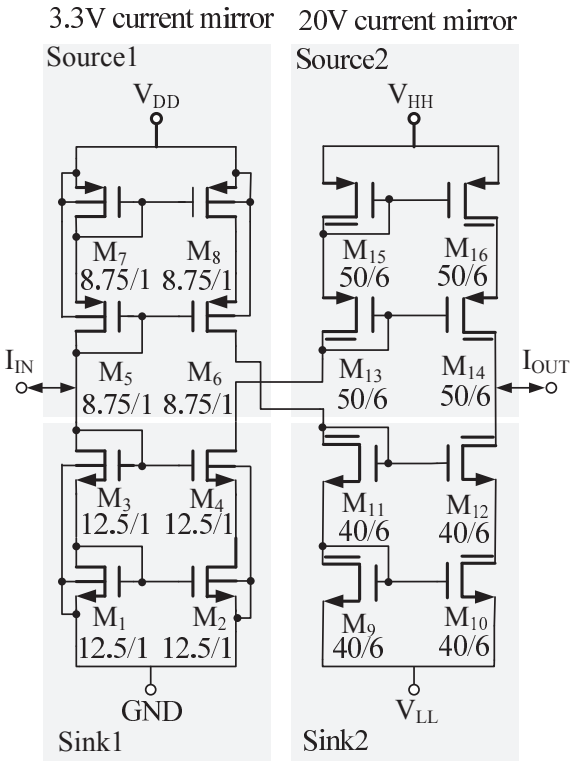


Figure 5.8 3.3V/20V current mirror circuit designed using 5V transistors, M_1-M_8 and double-side (source and drain) extended 20V transistors, M_9-M_{16}. The units for the dimensions of all transistors are μm / μm.

5.2.4 3.3V/20V current mirror

The current mirror is configured to support both source and sink currents to comply with the specification and enhance the flexibility of the microstimulator. The 3.3V/20V current mirror, depicted in Figure 5.8, is an interface between low-voltage, CMOS 0.13μm and high-voltage, 0.8μm DALSA 5V/20V technologies. Double cascode current mirror has been chosen because of its high-output impedance, and efficacy to maintain good linearity between input and output currents by diminishing the effect of channel length modulation [120]. Albeit,

this linearity is achieved sacrificing output swing by some extent compared to that of wide swing cascode and wide swing enhanced output impedance cascode current mirrors [121], the latter group requiring additional reference currents. Our mixed-voltage current mirror is comprised of four cross coupled double cascode current mirrors and two of these circuits are realized with 20V transistors. Generating reference currents for all current mirrors would increase power and area consumptions, and make their implementation complex.

The whole circuit is a two stage cascode current mirror [13], where each stage is composed of one source and one sink cascode current mirrors.

The 3.3V current mirror is designed using 5V transistors and is supplied with 0 and 3.3V. The sink current mirror is made of NMOS transistors, M_1-M_4, and the bias current in M_1 and M_3 is delivered by the PMOS transistors, M_5 and M_7, which together also work as the active current source load for the low-voltage sink current mirror. On the other hand, transistors M_2 and M_4 are cross connected to the left branch of high-voltage source current mirror and bias current is drawn from 20V PMOS transistors, M_{13} and M_{15}. Low voltage transistors, M_1 and M_3, and 20V NMOS transistors, M_9 and M_{11} work as current sink loads for the low-voltage source current mirror, comprised of PMOS transistors M_5 to M_8. All transistors in the low-voltage (3.3V) current mirror follow the characteristics of long channel CMOS transistor. The analytical design equations related to this current mirror is presented in APPENDIX A. This low-voltage current mirror works as an interface between the external stimulation current source and 20V current-mirror stage.

The high-voltage current mirror has been integrated to increase the output compliance voltage swing across electrode-tissue interface impedance. This second stage current mirror is realized with 20V transistors, i.e., high side drain and source extended MOS transistors [129] and driven by $\pm$10V supplies. The source current mirror is constituted by PMOS transistors M_{13} to M_{16} which are biased by the active current sinks made of low-voltage NMOS transistors, M_2 and M_4 and high-voltage NMOS transistors, M_{10} and M_{12}. The sink current mirror is designed of high-voltage NMOS transistors, M_9 to M_{12} and biased by transistors M_6, M_8, M_{14}, and M_{16}. The high-voltage transistors are basically DMOS (double diffuse MOSFET) [130]-[131], more specifically LDMOS (lateral double diffuse MOSFET) in our case, and do not follow the same traits as of low-voltage transistors. The electrical equivalent circuit of an LDMOS is comprised of more than one simple MOS transistor.

The dimensions of all low- and high-voltage transistors have been optimized to limit the quiescent current consumption to only 4μA and operate them in the saturation region for the input stimulation current (I_{IN} in this circuit) up to our target value of 400μA. The objective was to make I_{IN} equal to I_{OUT} and henceforth, transistors utilized in the same source or sink current mirrors are not scaled. However, some minor deviations between input

and out currents may arise because of process variations.

The stimulation current, applied externally to this chip, can be either source or sink or both to aid monophasic and biphasic stimulation. Custom integrated chips or commercially available current sources can be used to supply the microstimulation current. In our case, the novel stimuli-generator implemented with various energy-efficient waveforms and described in Chapter 4 serves this purpose.

5.2.5 High-voltage switching

The high-voltage switches are one of the fundamental components of the microelectrode drivers and it is necessary to characterize the implemented switches for different stimulation current levels. All switches in two MEDs are made of transmission gate (TG) owing to its rail-to-rail swing capability and low overall transconductance. The transconductance of TG switch is given by the following equation [132]:

$$\begin{aligned} g_{ds_{ON}} = \mu_n C_{ox}\left(\frac{W}{L}\right)_n [V_{DD} - V_{thn}] - \mu_p C_{ox}\left(\frac{W}{L}\right)_p \\ . |V_{thp}| - \left[\mu_n C_{ox}\left(\frac{W}{L}\right)_n - \mu_p C_{ox}\left(\frac{W}{L}\right)_p\right] V_{in} \end{aligned} \tag{5.1}$$

The ON resistance Rs_{ON} of the switch is the reciprocal of its transconductance, $g_{ds_{ON}}$ and expressed by the following equation:

$$Rs_{ON} = \frac{1}{g_{ds_{ON}}} \tag{5.2}$$

According to Eq. 5.1, the transconductance of TG switch varies depending on input signal level. In the standard procedure to calculate Rs_{ON}, a sinusoidal voltage signal is applied at the input of a switch which is operated by the gate control voltage. The measured voltage across the switch is divided by the current passing through it for a given load-impedance. In our case, the input signal is stimulation current rather than a voltage signal. In our proposed MEDs, the main switch-matrix has 32-high-voltage switches which are configured to be connected directly to electrodes. A number of such switches are also located in each node (Node1 to Node2 in MED1, and Node1 to Node8 in MED2) within both MEDs. The output impedance of each group of switch is different from another group, depending on their locations within the system and output loads. Two different scenarios have been considered, where the node voltage at the input of each switch (such as V_1 for the switch S_{N11} in Figure 5.9 and Figure 5.10) is V_{in} according to Eq. 5.1.

First scenario

In this scenario, as shown in Figure 5.9(a), only two switches in the switch matrix, S_1 and S_2 are connected to the electrical equivalent model of two electrodes, which is presented in Figure 5.9(c), for one microstimulation site.

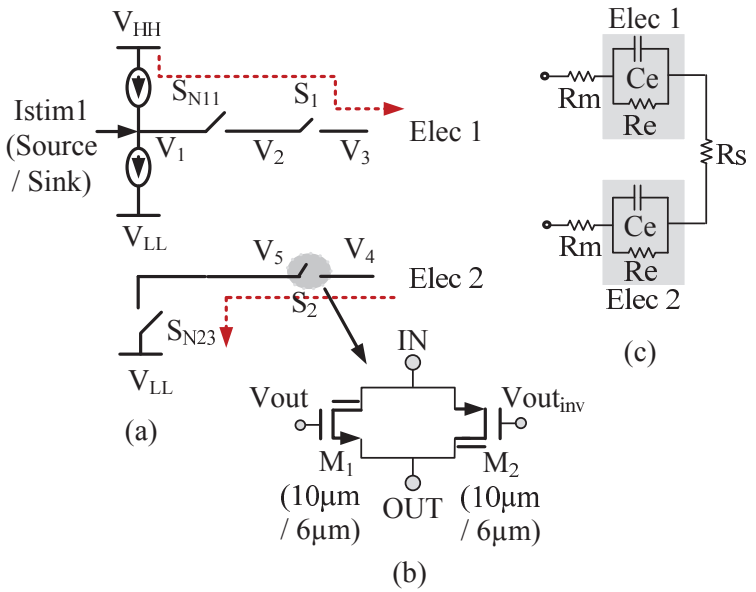


Figure 5.9 Schematic diagrams for (a) calculating the ON resistance of different switches in the first scenario (one monopolar or bipolar stimulation), (b) high-voltage transmission gate, and (c) equivalent circuit of two electrodes.

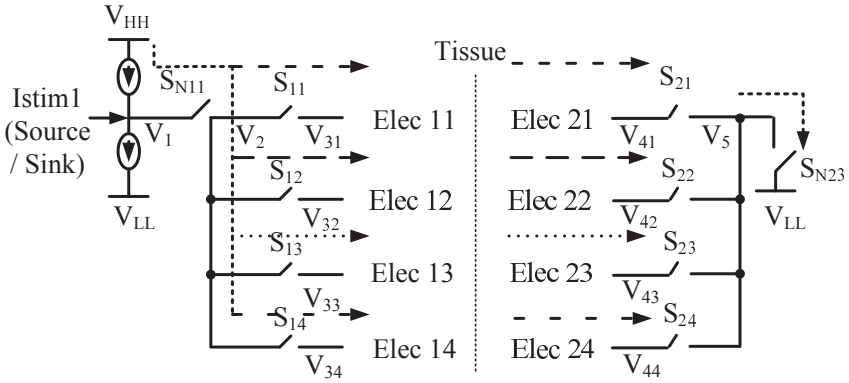


Figure 5.10 Schematic diagram for calculating the ON-resistance of switches in the second scenario (4 monopolar or bipolar stimulation).

Second scenario

In the second scenario, eight switches in the switch matrix, S_{11} to S_{24}, presented in Figure 5.10, have been configured for four microstimulation sites. Between each pair of switches,

the same electrical equivalent model of the microelectrode has been used.
In both scenarios, Node1 switch S_{N11}, allocated for connecting Istim1, 2 and Node2 switch S_{N23}, dedicated for connecting V_{LL} (considering MED1 only) have been taken into account for simplicity. Switch ON resistances for different groups of switches have been calculated on the basis of the applied different stimulation current values.
$V_{S_{N11}}$, $V_{S_{N23}}$, V_{S_1}, and V_{S_2}, shown in Figure 5.11, are the control signals applied to the switches used in the first scenario in section 5.2.5. The stimulation current, Istim1, was varied from 20μA to 130μA. To calculate the ON-resistance of the switches, node voltages, V_1 to V_5 were measured, subtracted, and divided by the specific stimulation current. Figure 5.12 reports the variation of ON-resistance for different stimulation currents. These results show that these resistances vary between 3.5kΩ to 7.5 kΩ. The stimulation current frequency was unchanged throughout this experiments, resulting in a constant equivalent impedance of two electrodes with an average value of 111.5kΩ. Similar steps were taken in the second scenario but the stimulation current was increased up to 400μA owing to the low equivalent impedance of four branches of electrodes (28kΩ (approx.) for eight electrodes) and switches (between 1 to 1.6kΩ for each switch, S_{11} to S_{24}, within the switch matrix) connected in parallel. Nonetheless, the ON-resistance of node switches varied between 3.7 to 7kΩ in this case.

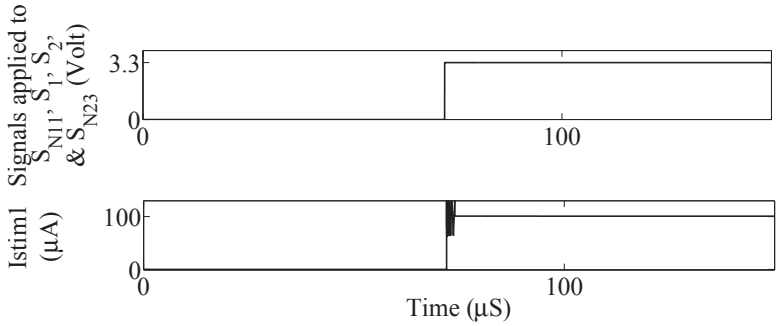


Figure 5.11 Signals for controlling the switches during measuring ON-resistance of switches (top). Stimulation current from 3.3V/20V current mirror when Istim1 was set to 100μA during first scenario.

5.3 Microelectrode model

Figure 5.9(c) presents the simplified electrical equivalent model for the electrode [133], used for post-layout simulations and characterizing fabricated microchips. The electrode model is comprised of passive elements, R_e and C_e, where R_e is the leakage resistance created due to the charge carriers crossing the double-layer and C_e is the double-layer capacitance at the electrode-electrolyte interface [134]. Both of these parameters are frequency dependent. In

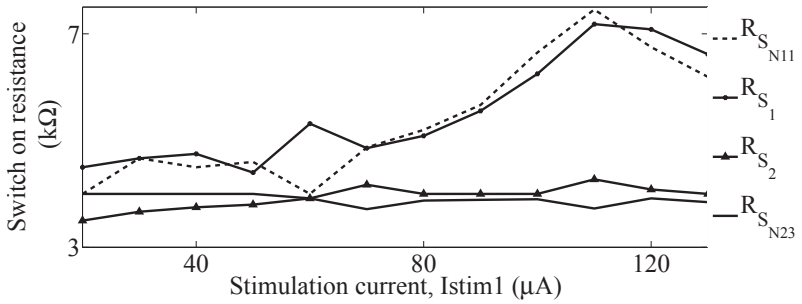


Figure 5.12 First scenario: variation of switch ON-resistance due to the change in applied stimulation current.

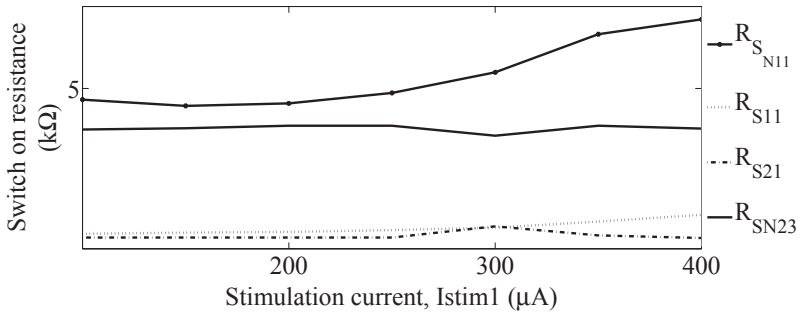


Figure 5.13 Second scenario: effect of delivered stimulation current change on switch ON-resistance variation.

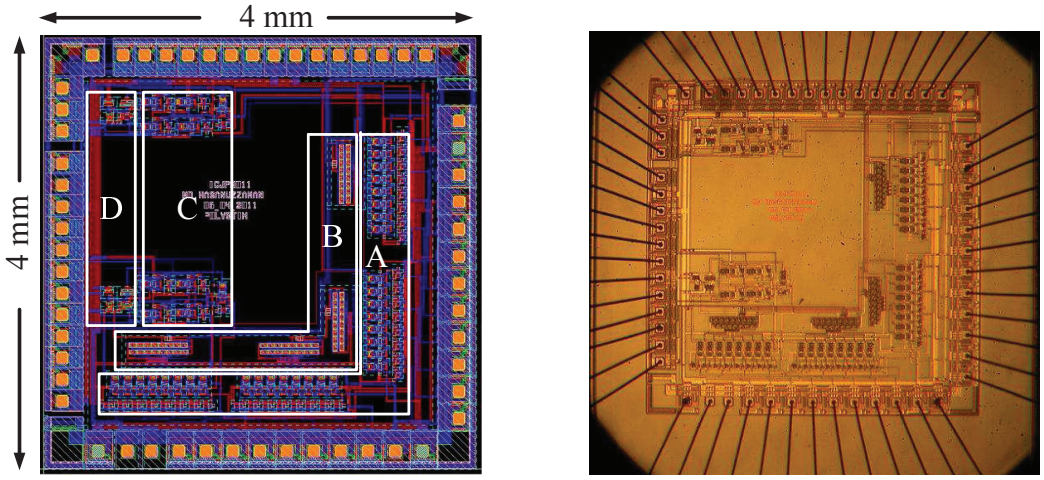
[133] the reported values of R_e and C_e are 140kΩ and 1.14nF respectively. For our post-layout simulations and measurements, the value of R_e was approximated to 46kΩ to comply with iridium-oxide coated silicon microelectrode from Blackrock Microsystems (50kΩ per electrode), and a 1.2nF capacitor was chosen for C_e. R_m is used to replicate the resistance of microelectrode metallic part between the back of the microelectrode and the microelectrode driver, and R_s represents the saline spreading resistance. The values of R_m and R_s are set to 1.5Ω and 11.7kΩ respectively [133].

A novel micromachined platinum (Pt) coated 3D microelectrode array, fabricated in our Polystim Laboratory, has also been used for in vitro characterization of the second microelectrode array driver and the complete microstimulator. A summarized description on this new MEA and the associated in vitro experimental results will be provided in Chapter 7.

5.4 Results

The layouts and the microphotographs of the fabricated microchips are presented in Figures 5.14 and 5.15. The empty space in the first microchip was reserved for the monitoring unit. Good layout design rules, such as common centroid, multi-gate fingering, inter-digitized

style, multiple contacts etc., have been used while laying-out of two microchips. Special attention was paid for matching transistors in current mirror circuits. The digital building blocks available in Teledyne DALSA 0.8μm C08E technology library were utilized to implement the 32-bit serial-in parallel-out shift register and forbidden state logic circuits. This technology



(a) (b)

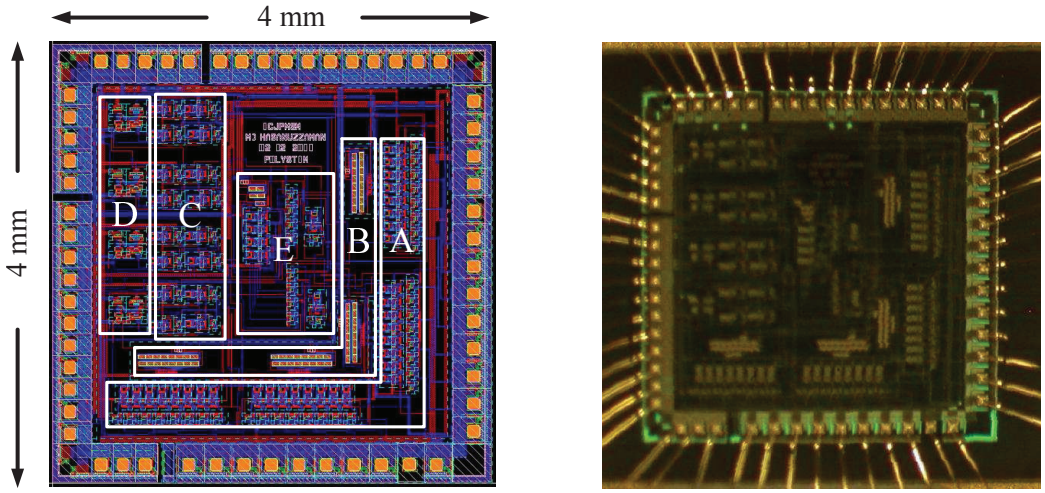
Figure 5.14 The fabricated ICJPM011 chip: (a) Layout view with floor plan: A and C - high-voltage level shifters and switches, B - 32-bit serial-in parallel-out shift register, and D - 3.3V/20V current mirrors. The empty space is for the electrode-tissue interface voltage-monitoring circuit. (b) The microphotograph of this chip.

has the common ground irrespective of low or high-voltage analog pads used for GND or 0V and the lowest potential (-10V or V_{LL} in our case). Therefore, the high-voltage V_{LL} pads were modified and substrate contacts from P-epitaxy layer were removed to prevent the latch-up between GND and V_{LL} pads. 68PGA ceramic packaging assemblies have been used for the post-fabrication testing and characterization purpose. Bare chip die of the second MED has been wire-bonded on the custom-designed PCB for building the microstimulator prototype (Chapter 7).

The features of the MEDs are summarized in Table 5.2. The test setup to characterize the MEDs is presented in Figure 5.16. Indeed, ICJPM011, shown in this figure, was replaced by ICJPMSMX during its characterization. The post-layout simulation and measurement results are illustrated in the following sections.

5.4.1 Post-layout simulation results

The post-layout simulation results, presented in Figure 5.17, show that the microelectrode drivers maintain linear relation between the applied input and received output stimulation



(a) (b)

Figure 5.15 The fabricated ICJPMSMX microchip: (a) Layout view with floor plan: A and C - high-voltage level shifters and switches, B - 32-bit serial-in parallel-out shift register, D - 3.3V/20V current mirrors, and E-circuitry for monitoring microelectrode voltage. The empty space in ICJPM011 is for the electrode-tissue interface voltage-monitoring circuit. (b) The microphotograph of the chip.

currents for the desired range, 0 to 400μA. Beyond this range, the output current level through each impedance saturates. However, this current saturation does not limit the MEDs to perform the desired microstimulation. The explanation is that there are six 20V transistors on the way of the stimulation current and almost 10V, which is half of the total compliant voltage of the global system (20V, as V_{HH} and V_{LL} were set to $\pm$10V), is dropped across these transistors. The value of electrode-tissue interface impedance, the global compliance voltage levels ($\pm$10 Volts), and sizes of 20V transistors in current mirrors and switches also largely affect the stimulation current range. The possible solution to extend the input stimulation current range is to increase the voltage levels of V_{HH} and V_{LL} or the dimensions (width) of transistors in the current mirror circuits and transmission gates or to reduce the electrode-tissue interface impedance. However, increment of supply voltages beyond 20V may stress the high-voltage transistors. In MED1, four trains of biphasic current pulses with amplitude of 96μA each, plotted in Figure 5.18, were generated with cathodic first through resistors, Z_3 and Z_7, and anodic first through resistors, Z_1 and Z_5. In all pulse trains, pulse-width and inter-pulse duration (t) are 100μS, and period of the biphasic pulse (T) is 400μS. These parameters can be adjusted by varying the Serial-in data1-4 and other stimulation control signals. Istim1 and Istim2 were set to 400μA each. Results in Figure 5.18 prove that the microelectrode driver is able to produce charge balanced biphasic stimulation current pulse with almost zero offset current. The control signals to the 32-bit register inputs are portrayed

Table 5.2 Specifications for ICJPM011 (MED1) and ICJPMSMX (MED2).

Parameters	Value
Technology	DALSA 0.8 μm 5V/20V CMOS/ DMOS process
V_{DD}, V_{HH}, V_{LL} and GND	3.3V, 10V, -10V and 0
Type of microstimulation	Current
Maximum stimulation current per input channel	400 μA
Stimulation current range per output channel	0 - 100 μA (nominal)
No. of simultaneous current level amplitude	1 (MED1), 4 (MED2)
No. of simultaneous monopolar and bipolar stimulations	16 and 8
No. of electrodes to drive	16
Electrode selectivity	Any
Power consumption (quiescent)	0.316 mW (MED1), 0.735 mW (MED2)
No. of input and output pads	56 (MED1), 58 (MED2)
Type of package	68PGA
Dimension of the chip	4 X 4 mm^2

in Figure 5.4. To model the iridium-oxide coated silicon microelectrode from Blackrock Microsystems and investigate the microstimulation capability of our system in practical case, resistors of 50kΩ (charge transfer resistance) were connected in parallel with 1.14nF capacitors (double layer capacitance). The generated biphasic current signals were similar to those in Figure 5.18 except transients at the beginning of each positive and negative-pulse.

It is necessary to mention that the threshold voltage of all high-voltage PMOS transistors (PXE) was increased by 0.6V from the nominal value of -0.985V as a result of the process variation during fabrication of the first MED. This increment in the threshold voltage affected the high-voltage analog subsystems (switches, current mirrors, and level shifters) of the global system and therefore, overall performance of the microchip severely. This technology does not allow performing Monte-Carlo simulation in "Cadence Analog Environment Window" for investigating process variation and mismatch analysis. We, therefore, pursued an alternative approach to inquire the effect of V_T on high-voltage PMOS transistors. In the spectre model file, V_{T0} for this technology was raised from the nominal value -0.985V to -1.585 to consider the 0.6V increment into effect. No change was noticed in the stimulation current range up to 350μA, as illustrated in Figure 5.19. For the new V_{T0}, the nonlinearity

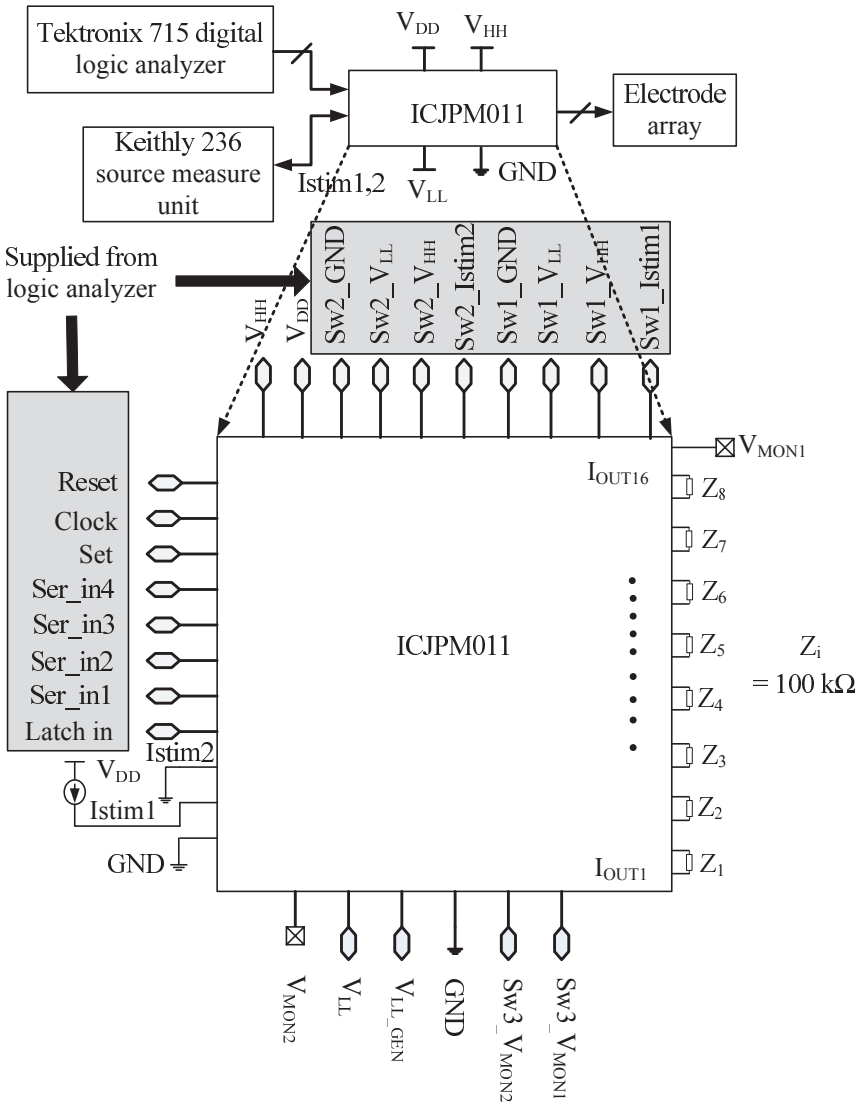


Figure 5.16 Test bench for the post-layout simulations and measurement of the chips ICJPM011 and ICJPMSMX. Z_1 . . Z_8 represent microelectrode-tissue interface impedances and connected in bipolar microstimulation configuration. ICJPM011 was replaced by ICJPMSMX in the second phase of testing. Microstimulation current is supplied by Istim1 or Istim2 in MED1 and Istim1 to Istim4 in MED2.

in the output current from the ideal value arises beyond input current of 350μA.

Post-layout simulations were carried out also to inspect the effect of temperature variation on the effectiveness of two MEDs. The variation of total stimulation current for the temperature range of 20 °C to 45 °C is presented in Figure 5.20. Current drops at 90nA/ °C for the temperature range of 23 °C to 38.5 °C. The stimulation current value at 37.5 °C, the temperature of biological medium, is 397.1μA. This minor deviation in total stimulation current will not impose serious challenge on the precision level of the delivered charge quantity to the tissue.

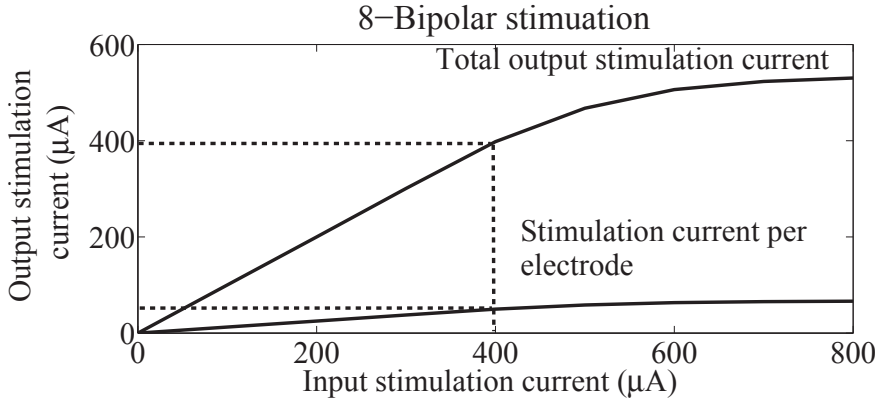


Figure 5.17 Post-layout simulated result showing the range of the linearity per input channel and per microelectrode in the output channel of microelectrode drivers.

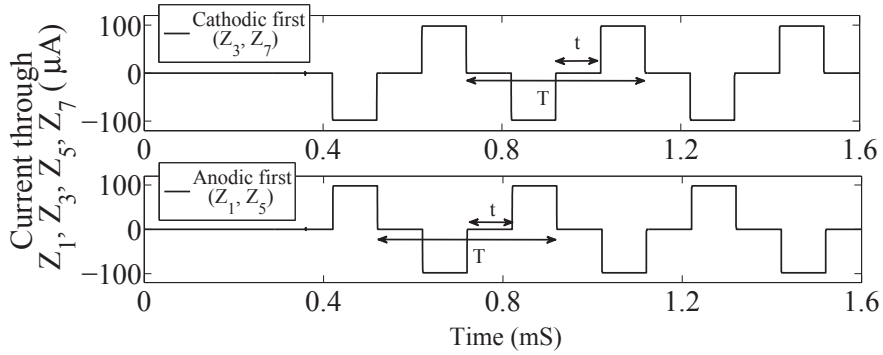


Figure 5.18 Trains of biphasic current pulses generated through resistors Z_1, Z_3, Z_5 and Z_7 during post-layout simulations of ICJPM011. Both pulse trains have the peak values, $\pm 96\mu$A.

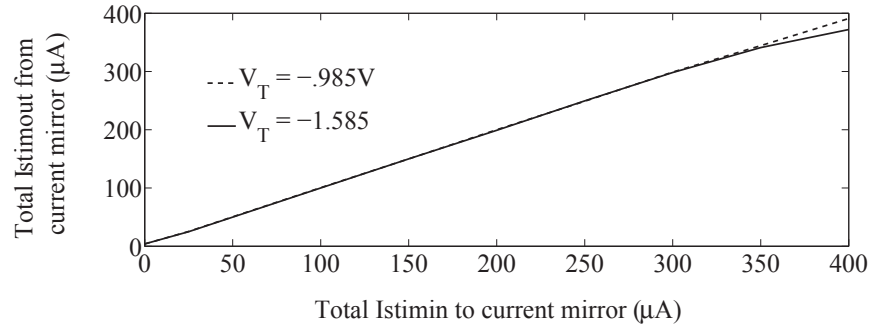


Figure 5.19 Plot of the incremental effect of V_{T0} on the total stimulation current.

5.4.2 Measurement results

For the measurements of first MED, the control signals, clock, reset, serial-in data and latch in, illustrated in Figure 5.21(a), were generated from a Tektronix 715 digital logic analyzer. These signals were applied externally to the 32-bit register to operate the switches in the switch-matrix. Two other control signals, to turn on the switches S_{N11} and S_{N23}, were applied

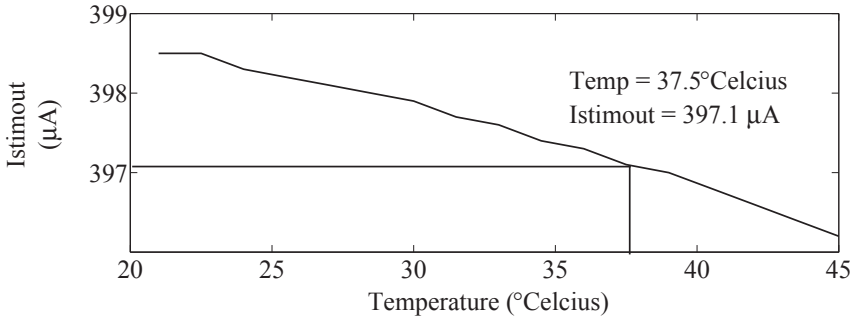


Figure 5.20 Gradual change in the stimulation current due to the fluctuation of temperature.

directly from the digital logic analyzer. To model the electrode-tissue interface impedances, eight 100kΩ resistors were used, where only the resistive parts were considered for simplification. The stimulation current, Istim1, supplied from a Keithly 236 source measure unit, was varied from 0 to 800μA. The second stimulation current source, Istim2 dedicated for Node2, was disabled during these experiments. Only the switches dedicated for the terminals, connected to the resistors Z_1, Z_3, Z_5, and Z_7, were closed to allow stimulation currents. Figure 5.21(a) shows latch signal which enabled the current signals to pass through these resistors with a certain delay. The oscilloscope trace of the voltage stimulus measured across resistor Z_1 is illustrated in Figure 5.21(b). The measured voltage levels were unaffected by the variation of input stimulation current, but pulse width, inter-pulse duration, and frequency

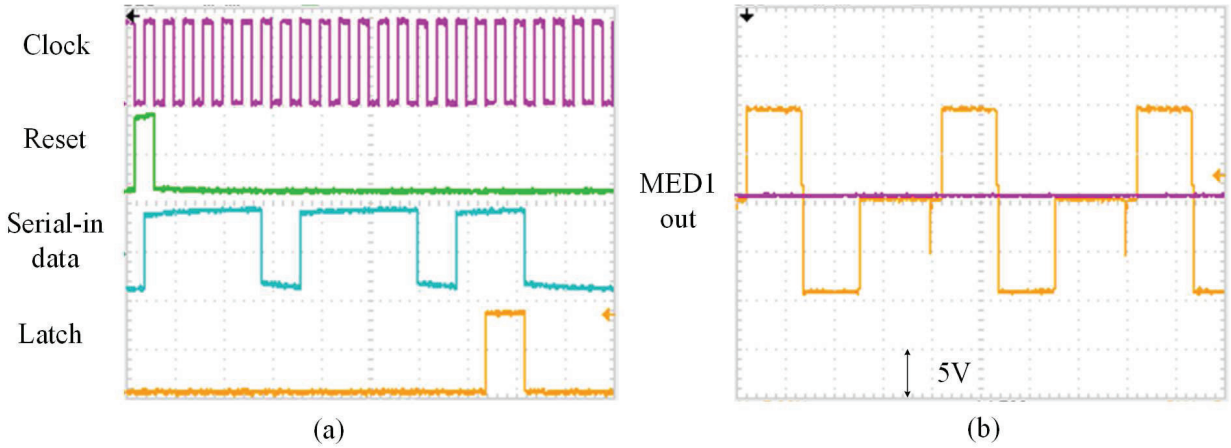


Figure 5.21 Experimental results of MED1: the (a) control signals from Tektronix 715 digital logic analyzer and (b) biphasic voltage pulse across resistor, Z_1.

were being modulated by the control signal parameters. These observations summarize that, in MED1, the low voltage digital parts are functional whereas the 20V analog and digital blocks are inoperative. This partial malfunction of MED1 can be attributed to the fabrication fault in high-voltage PMOS transistors (V_T increment).

In case of MED2, stimulation current from Keithly 236 source measure unit was applied to four channels, Istim1 .. Istim4 separately. Control signals for the switches in Node1 to Node8; and clock, reset, serial-in data-1-4 & 5 and latch in signals to the 32-bit and 2-bit SIPO registers were delivered from Tektronix 715 digital logic analyzer. The nominal values for V_{DD}, V_{HH}, and V_{LL} were set to 3.3, +10, and -10 Volts respectively.
Linear stair source and sink current signals were applied to Istim1 - Istim4 individually to verify the linearities at the outputs of both 3.3V/20V current mirrors and MED2. For testing the range of each current mirror, the input stimulation current signals ranged from 0 to $\pm 400\mu$A with an increment (or decrement) of $\pm 50\mu$A in each step. All the switches in the switch array remained closed. External connections to Node1 .. Node8 were established by providing control signals to 2-bit SIPO register, and current signals available to these nodes were measured. A resistor of 23kΩ was added between two nodes from each group of nodes (Node1 & Node2....or Node7 & Node8). During anodic phase, switches S_{N11} and S_{N22} (.....or S_{N71} and S_{N82}) were closed. For cathodic phase, switches S_{N21}, S_{N41}, S_{N61}, and S_{N81} were turned on. Figure 5.22(b) presents the control signals for operating these switches. Differential voltage signals measured across the 23kΩ resistor for Istim1 up to $\pm 400\mu$A are

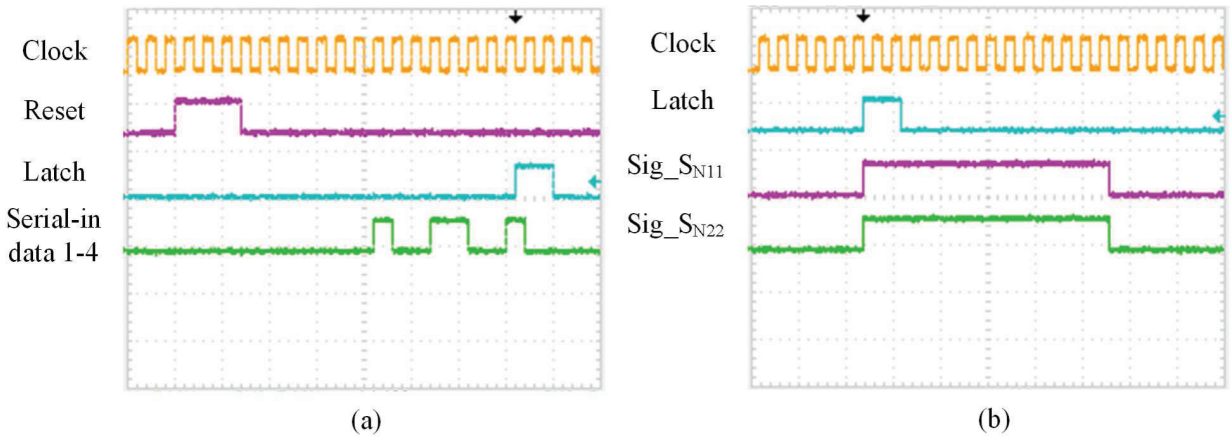


Figure 5.22 Experimental results of MED2: 3.3V signals from Tektronix 715 digital logic analyzer applied (a) to the 32-bit SIPO register for controlling the high-voltage switch array, and (b) to the switches in Node1 to Node8 dedicated to connect Istim1 – 4, V_{HH}, and V_{LL} (bottom two signals only).

plotted in Figure 5.23(a), which exhibits strong linear relation between applied input stimulation currents and output voltage signals until Istim1 reaches $\pm 380\mu$A. In the absence of input stimulation current, an undesirable amount of current flows at the beginning of anodic and cathodic phases for a very short duration (shown as spikes), when switches are closed. But, the potentials developed across load-impedance owing to these currents are cancelled during biphasic stimulation and therefore, do not contribute to develop net charge at the stimulation

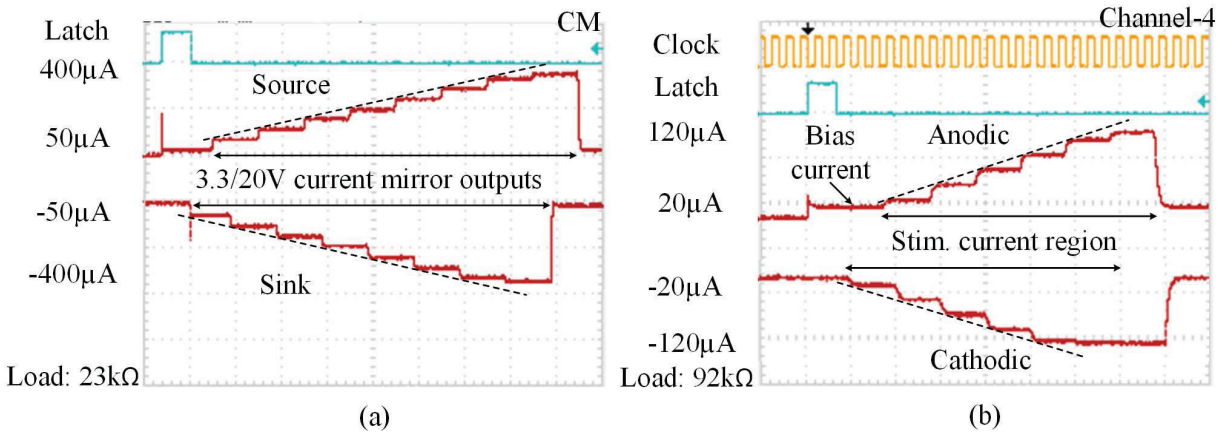


Figure 5.23 Measurement results of MED2: (a) Oscilloscope graphs of voltage waveforms at the output of 3.3V/20V current mirror showing its range of linearity for positive and negative linear stair input current signals. (b) Measured signals across an equivalent resistor of 92kΩ connected between I_{OUT1} and I_{OUT2} for anodic and cathodic linear stair input current waveforms.

sites after a complete stimulation cycle. Figure 5.23(b) presents results measured across a 92kΩ resistor connected between I_{OUT1} and I_{OUT2}, when linear stair source and sink currents, ranged between 0 to ±120μA, were supplied to Istim1. Evidently, stimulation current per output channel could not exceed ±110μA for the specified load and compliance voltage limit across it (10V).

Constant DC currents spanning between 0 to ±120μA, were applied to four channels, Istim1 .. Istim4, to perform bipolar monophasic stimulation for both anodic and cathodic phases. Control signals to the switch matrix, presented in Figure 5.22(a), were delivered to the 32-bit SIPO register. During anodic phases, switches S_{N11} and S_{N22} for channel-1, and other similar positioned switches in the rest of the channels were operated applying signals as illustrated in Figure 5.22(b). In cathodic phases, microstimulations were carried out providing connections between V_{HH} and even numbered nodes. The first two consecutive outputs within each channel, such as, I_{OUT1} and I_{OUT2} in channel-1 to I_{OUT13} and I_{OUT14} in channel-4 were selected, and two resistors of 46kΩ each were connected in series between two outputs of each channel. Figure 5.24(a) and Figure 5.24(b), respectively, present the developed differential voltages across these resistors owing to different input stimulation current levels in channel-1 and -2. Stimulation output waveforms measured in two other channels (not presented here) were closely resemble of those observed in channel-1 and -2.

Emulated model of microelectrode was used to analyze the effect of double layer capacitance on bipolar monophasic stimulation. While performing stimulation, a 1.2nF capacitance was connected in parallel with a 46kΩ resistor and two of such models were implemented in series.

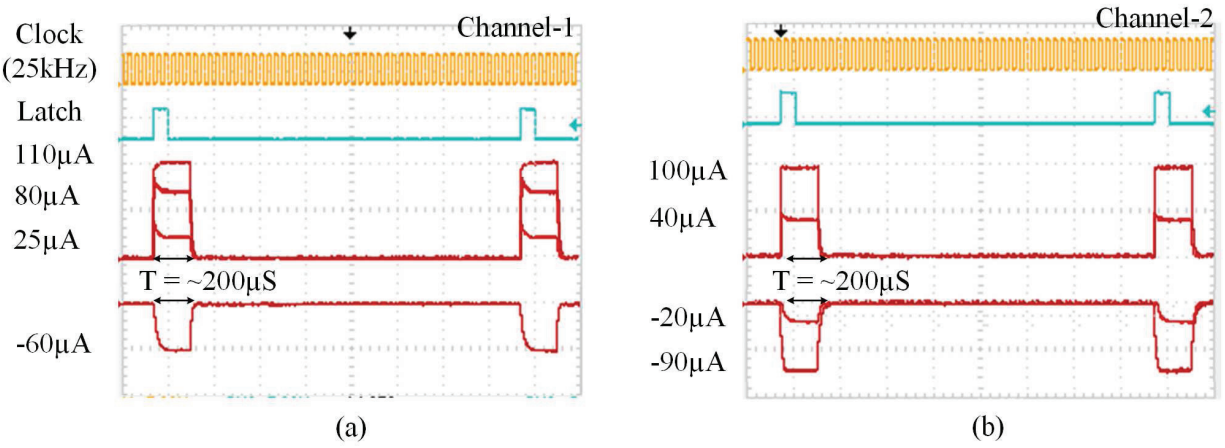


Figure 5.24 Experimental results of MED2: (a) Variation of pulse amplitudes across a 92kΩ equivalent resistor for multi-level anodic and cathodic stimulation currents in channel-1. The resistor was connected between I_{OUT1} and I_{OUT2}. (b) Anodic and cathodic voltage pulse variations across an equivalent resistor of 92kΩ for several current ranges in channel-2. Current was delivered through I_{OUT5} and I_{OUT6}.

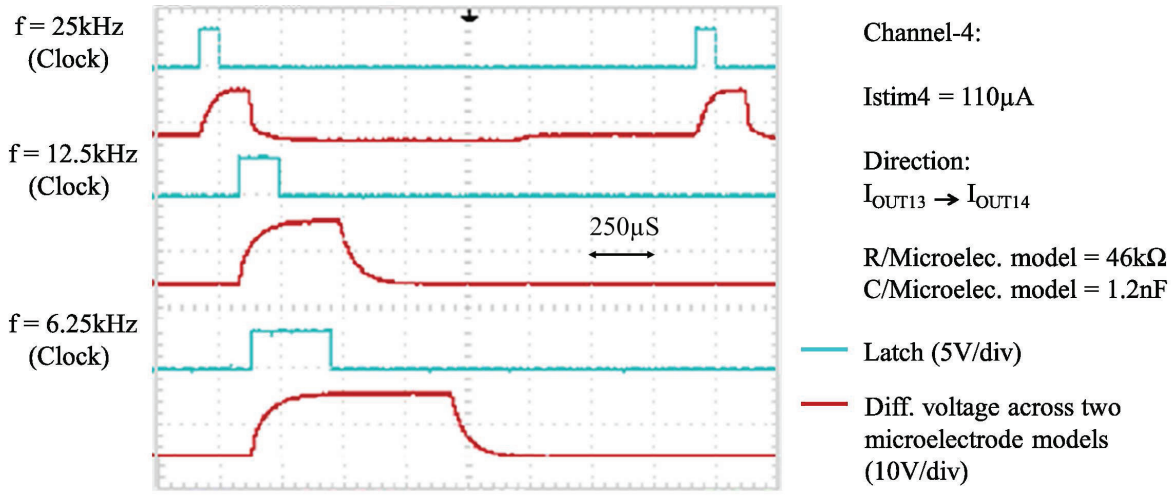


Figure 5.25 Experimental results of MED2: Effect of double layer capacitance for different clock frequencies on bipolar monophasic stimulation. Signals were extracted across two emulated models of microelectrode inserted between I_{OUT13} and I_{OUT14} of channel-4. Stimulation current level was set to 110μA.

The measured waveforms in channel-4 outputs (between I_{OUT13} and I_{OUT14}) for 100μA source stimulation current are presented in Figure 5.25. For various frequencies, capacitive nature is prominent, caused by the finite charging and discharging times of two capacitors.
Increasing V_{HH} and V_{LL} to ±13 Volts enhances compliance voltage to 20V per anodic or ca-

thodic phase at the output of MED2. The measured potential waveforms across the output channels I_{OUT9} and I_{OUT10}, when 230μA stimulation current was applied to Istim3, are shown in Figure 5.26. Impedance of each imitated microelectrode model is also stated in the figure. Table 5.3 summarizes the performance indices of these MEDs and those reported in [8], [13],

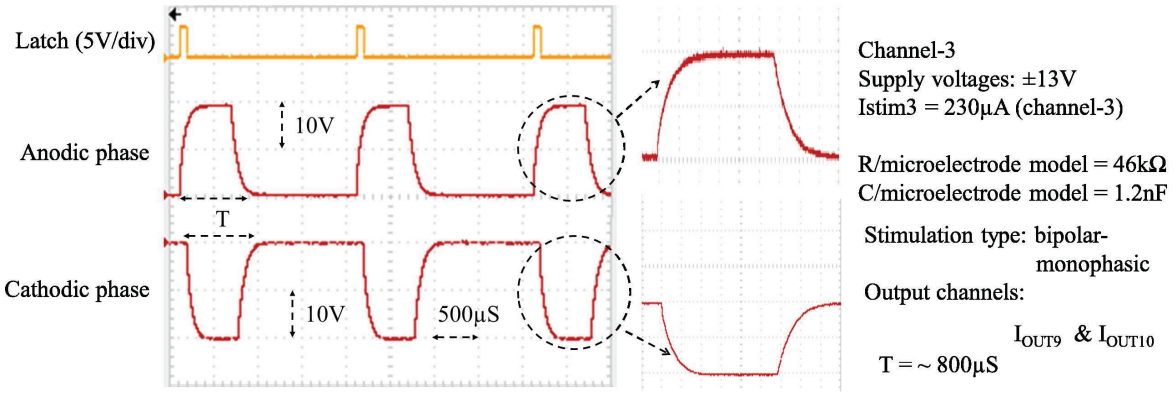


Figure 5.26 Experimental results of MED2: The maximum compliance voltage (20V per phase) measured across two imitated models of microelectrode connected between I_{OUT9} and I_{OUT10}. Stimulation current, Istim3, in input channel-3, was set to 230μA. V_{HH} and V_{LL} were increased to $\pm$13V.

[108], [135]. On the basis of their capabilities and the technologies used to implement them, a fair comparison between our designs and other works has been made. The system in [13] includes an on-chip high-voltage DC-DC converter in the output stage and it exceeds the minimum allowable static power dissipation limit for implantable biomedical devices. The microstimulator in [135] is designed in low-voltage process, and therefore, it occupies the lowest area and consumes very small power while rendering low voltage swing in the output stage. The proposed output stages are integrated with needed on-chip switching control. In addition, our systems provide higher compliance voltage and stimulation current per channel which meet the desired specifications. The proposed MEDs are highly configurable to perform monopolar or bipolar charge balanced bipasic stimulation using either source or sink or both current sources. The microelectrode drivers have large areas as these are designed to drive 16 microelectrodes and a differential voltage across electrode-tissue interface impedance monitoring circuit is included in MED2. The quiescent power consumptions, which are 0.316 and 0.735mW in these systems, are much lower and satisfy the power budget for the implantable biomedical devices.

Table 5.3 Comparison with other works.

Parameters	This work	[13]	[108]	[8]	[135]
Technology	0.8μm	0.8μm	0.8μm	1.5μm	0.35μm
Compliance Voltage (V)	10[a], 20[b] (Source) 10[a], 20[b] (Sink)	13.7 (Source and sink)	8.25	0.15-5 (Source) 0-4.75 (Sink)	2.6
Stimulation current (μA)	0-100 / Output channel[a] 0-220 / Output channel[b] 0-400 / Input channel	1.6-167.2	2000	$\pm$270	10-250
On-chip switch control	Yes	No	No	Yes	N/A
Consumed quiescent power (mW)	0.316 (MED1)[a] and 0.735 (MED2)[a]	27.2	N/A	8.25	0.0026
Area (mm^2)	4 X 4 (Each microelectrode driver)	2.9 X 2.9 (Includes DC-DC converter)	9 (Includes DC-DC converter)	4.6 X 4.6 (Complete stimulation) module	0.02 (Includes DAC and MUX)
No. of stim. sites	16	4	N/A	32	N/A
Load (kΩ)	23, 46, 50, 92, and 100	100 and 150	9.125	210 and 45	10

[a] V_{HH} and V_{LL} were set to $\pm$10V.
[b] V_{HH} and V_{LL} were set to $\pm$13V.

5.5 Conclusion

We presented in this chapter two fully configurable high-impedance microelectrode array drivers, integrated with on-chip switch control circuitries and dedicated for visual intracortical microstimulation. The proposed architectures are highly-flexible for all types of microstimulations, fully integrated, and designed in Teledyne DALSA 0.8μm 5V/20V CMOS/DMOS technology to meet the required high-voltage compliance across electrode-tissue interface high-impedance. The first device is able to deliver the same stimulation current to all sites. However, the fabrication fault prevented us to present the full-scale capability of the fabricated microchip. The second version of the design has been fabricated to support different currents in different electrodes' interfaces simultaneously. The second MED has been assembled with the other parts of the microstimulator and the experimental results of the complete microstimulator are included in Chapter 7. Because of higher compliance voltage capability, the device can drive microelectrodes with impedance of up to 200kΩ, when stimulated with 100μA. The ETI voltage monitoring circuit was not included within this chip due to the lack of space in the reserved silicon area and to meet the design submission deadline. We tested and characterized 7 packaged chips out of 10, wire-bonded 2 chip dies on PCB, and all of them are found to be functional.

CHAPTER 6

THE POWER AND DATA RECOVERY UNITS

6.1 Introduction

In this chapter, we propose the architectures of the energy and data recovery systems. The specific methodologies to design and implement each of them are justified and explained in detail. Performance of each system is verified through experiments and measurement results are presented in the end.

6.2 Power recovery unit

In most inductively-coupled wireless powered biomedical devices, minimizing the power consumption is necessary to limit the generated heat in the biological tissue, to prevent tissue damage, and to enhance device and battery lives. In general, minimizing inductive voltage and to improve the inductive link power efficiency are preferred goals. In visual intracortical microstimulation, the high value of electrode-tissue interface (ETI) impedance requires high-voltage compliance across it and this voltage can reach more than 15V [13] depending on the microstimulation current level. Moreover, biphasic high-voltage supplies are needed to prevent the DC level across ETI impedance and eliminate the use of DC blocking capacitors, while performing microstimulation. In addition to this, low voltage supply is necessary to reduce power dissipation in digital and the majority of analog circuitries. A conventional approach to satisfy all these requirements is to restrict the recovered inductive voltage to a low value and, then, generate a HV supply by adding a step-up DC-DC converter [108], [136]. Restricting the recovered voltage to a low value is required to keep the compliance of low-voltage ICs within their maximum operating limits and, therefore, to prevent the damage of the overall system from exceedingly large inductive voltages. One solution is to provide a low impedance path to ground. Two off-chip approaches to limit the voltage can be (i) using shunt regulators or Zener diodes, and (ii) controlled transistors as shunting devices. Various voltage clamp techniques with diodes fall among the on-chip approaches [136]-[142]. But, such system architectures published in [143]–[145], where a shunt regulator limits the rectified voltage to 3.3 or 5V are generally not energy efficient.

The principle and theories of inductive-link energy transmission is explained in APPENDIX A. In such case, an external controller (power transmitter) transmits energy to the implant

by coupled spiral antennas. The parallel LC network, resonated at a carrier frequency of 13.56 MHz, recovers energy. This industrial-scientific-medical (ISM) radio band frequency is chosen so as to keep the coupling attenuation through the skin tissues within the acceptable range, when antennas of 4-cm diameters are used [146]. Next, the received voltage is rectified and filtered with the capacitor, which also serves as the energy storage device for the implant. The reason behind choosing the shunt regulator is, in a discrete implementation approach, the former provides a simple voltage limiting option within a small space. However, as the inductive voltage is limited, any excess amount of inductive power, not used by the system will be dissipated as heat by the shunt regulator owing to the flow of excessive current to ground. Additionally, the 3.3V or 5V supply is found to be inadequate for high-impedance microstimulation, where the multichannel output stage delivers stimulation currents to multiple sites and this necessitates supply voltages as high as ±10 Volts. The remaining parts of the system can still operate at 3.3V or lower supplies to minimize power consumption.
However, it is not a simple task to select the most appropriate topology [147] on which the total efficiency of the system depends. This system efficiency is affected by parameters such as the efficiencies of shunt regulator and the rectifier, the inductive-link secondary equivalent source resistance (Rs), the load current on each supply, and the efficiencies of converters. In applications such as visual intracortical microstimulation, up to 2mA current from ±10 Volts, 1mA from 3.3V and 2mA from lower supplies (1.2 to 1.5V), can be consumed during stimulation phase, thus, confining the power budget within 50mW and satisfying the standard for the implantable biomedical devices. This power requirement is also affected by the system specifications, architecture, design consideration, and technology used. Considering our needs, the step-down approach turned out to be more advantageous.

6.2.1 Proposed power recovery unit

The architecture of this unit is shown in Figure 6.1. The electro-magnetic energy to the implant is transmitted from an external power transmitter through a spiral antenna. The parallel LC resonant circuit is tuned at 13.56MHz frequency which is within the industrial-scientific-medical (ISM) radio band. The inductive voltage is rectified using a full-wave bridge rectifier which is designed in Teledyne DALSA 5V/20V CMOS/DMOS technology [146], [148]. It is worth to mention that the rectifier chip was designed by F. Mounain et al. specifically for the bladder neurostimulator [146] and is being reused for visual intracortical microstimulator. A 20V off-chip Zener diode limits the rectified voltage to 20V which is the maximum possible value for the used technology. C_{filter} removes the effect of ripple in the rectified voltage. The rectified voltage is adjusted to 5V using a variable resistor load. The generated 5V signal is applied to a charge pump based DC-DC up converter to generate ±10V,

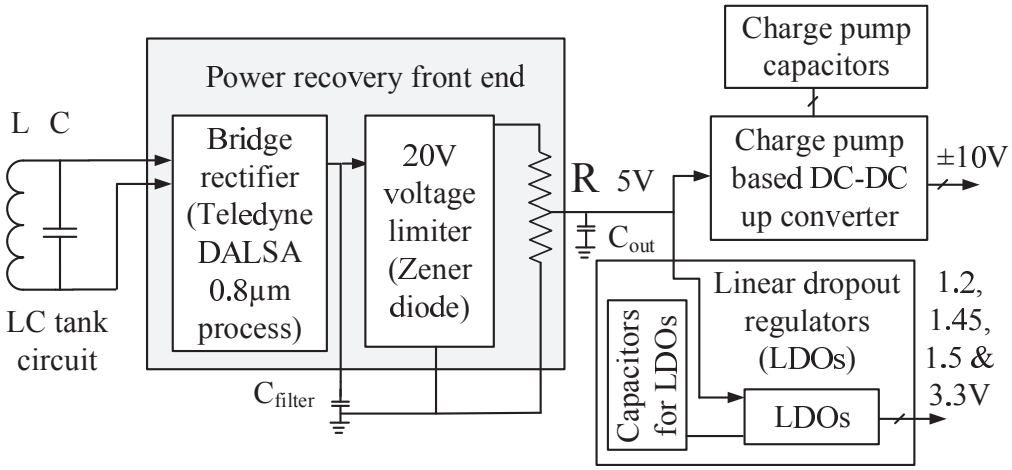


Figure 6.1 Schematics of the power recovery unit. The power recovery front end is a custom integrated circuit. The LDOs and the charge pump based DC-DC converter are low-power discrete components.

required for the biphasic microstimulation performed by the high-voltage output stage of the microstimulator. A number of low-drop out regulators (LDOs) have been used to generate 1.2, 1.45, 1.5 and 3.3 Volts needed by the rest of blocks of the implant. The LDOs and the charge pump based DC-DC up converter are realized using off-the-shelf components. The authors' contribution here is to assemble the rectifier chip and the other discrete components on a single miniature PCB, and experimental validation of the energy recovery unit.

6.2.2 Full-wave bridge rectifier

The detail description and implementation strategy of this circuit are presented in [146], and this thesis does not contribute to the design of this chip, except reusing it. However, for the convenience of the readers, the functional principle and design method will be summarized here.

The main rectifier, presented in Figure 6.2, consists of the transistors (N11, N12, P11, P12) where (P11, P12) are connected in cross-coupled manner and (N11, N12) are diode-connected with Vth canceling technique. With a large resistance R_N, a small current biases the diode-connected transistor N3. The resulting voltage at the terminal of N3 is maintained by the capacitor C_N and is applied to the gates of the transistors (N11, N12). This gate voltage allows to virtually cancel their threshold voltages. The transistors (N21, N22, P21, P22) form a secondary rectifier which, thanks to the integrated capacitors C_H and C_L, generates the higher voltage V_H and the lower voltage V_L. These voltages are applied to the substrates

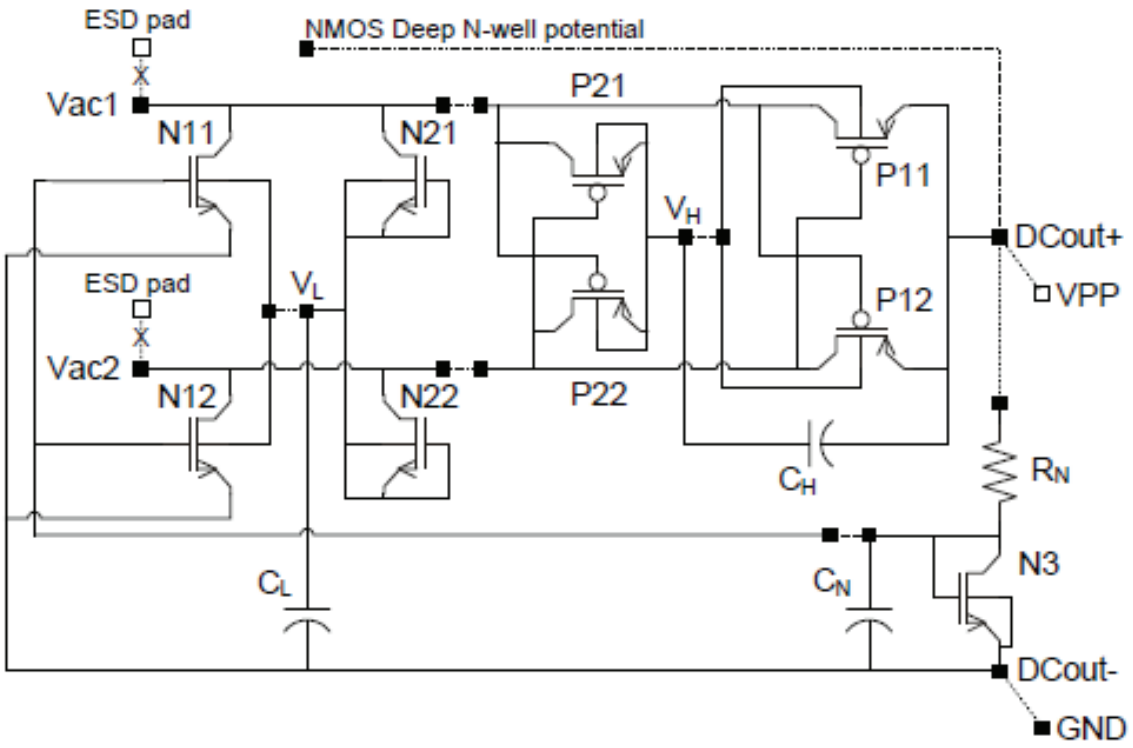


Figure 6.2 Circuit diagram of the rectifier chip © [146].

of the PMOS and NMOS transistors respectively. The secondary rectifier, not carrying high currents, is much smaller but protects the main rectifier of a possible clamping and prevents leakage current to the substrate when the output current increases. Moreover, the rectifier is optimized for maximum power efficiency at a load of 3mA to 5mA. For testability and investigation purposes, the chip was designed with many external connections from the outside as shown by broken lines in Figure 6.2. This design procedure not only allows access to certain internal nodes for measurements but also permits to apply external voltages to verify the impact on the performance of the rectifier. Thus, among others the nodes which can be accessed are the the common gate and common substrate of the transistors (N11, N12), and the common substrate of the transistors (P11, P12).

6.2.3 Experimental results

The layout view and fabricated microchip for the rectifier (ICJPMFMZ) are presented in Figure. 6.3. The characterization and the measurement results of the chip ICJPMFMZ are already presented in [146], and therefore, will not be repeated in this thesis as it does not count to the original contribution. However, contributions are added to assemble the rectifier chip and the discrete components. A 6-layer and 2-sided PCB of dimension 25mm x 25mm

is designed with different power planes (0, 1.45, 1.5, 3.3, and ±10 Volts) in multiple layers.

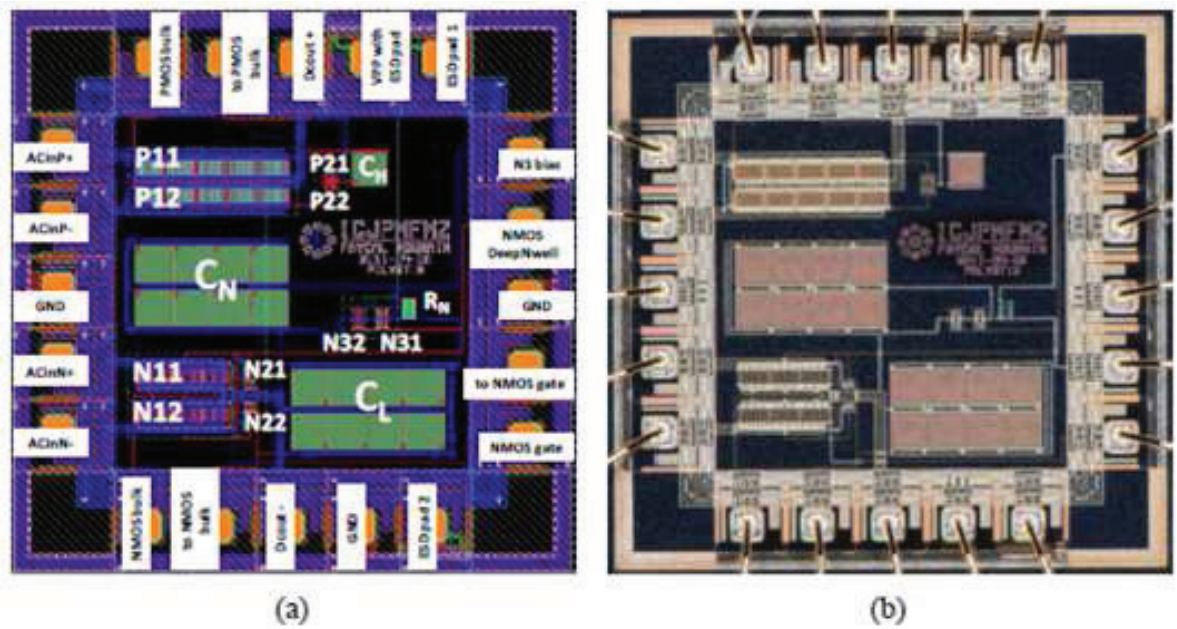


Figure 6.3 Power recovery front end rectifier chip, ICJPMFMZ: (a) Layout view, (b) the fabricated chip. © [146].

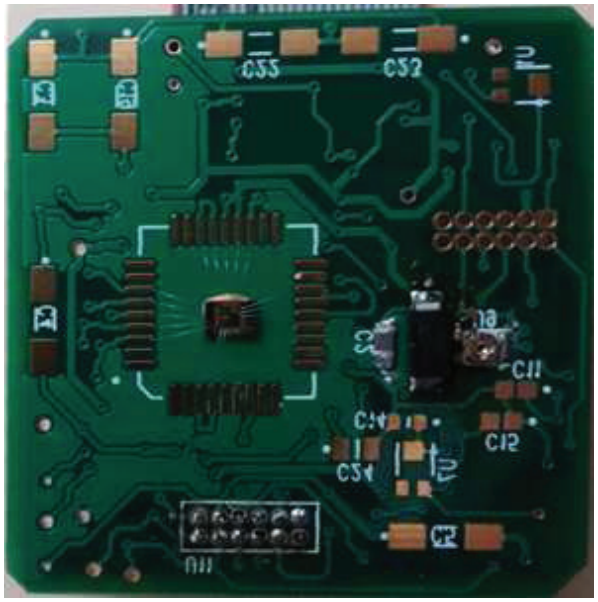


Figure 6.4 The power recovery unit assembled on a miniature PCB.

The rectifier chip is wire-bonded on the top layer of the PCB and the other surface mount components are soldered on both sides of it. The photograph of the assembled PCB is shown in Figure 6.4. To validate the performance of this unit, we transmitted RF signal at 13.56MHz

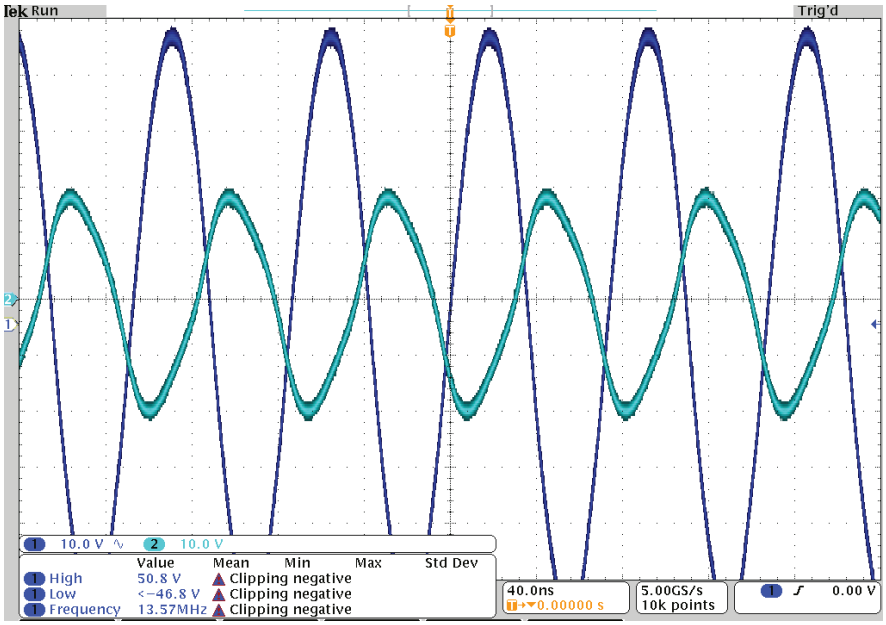


Figure 6.5 Oscilloscope graphs of the transmitted and received RF signals at 13.56Mhz frequency.

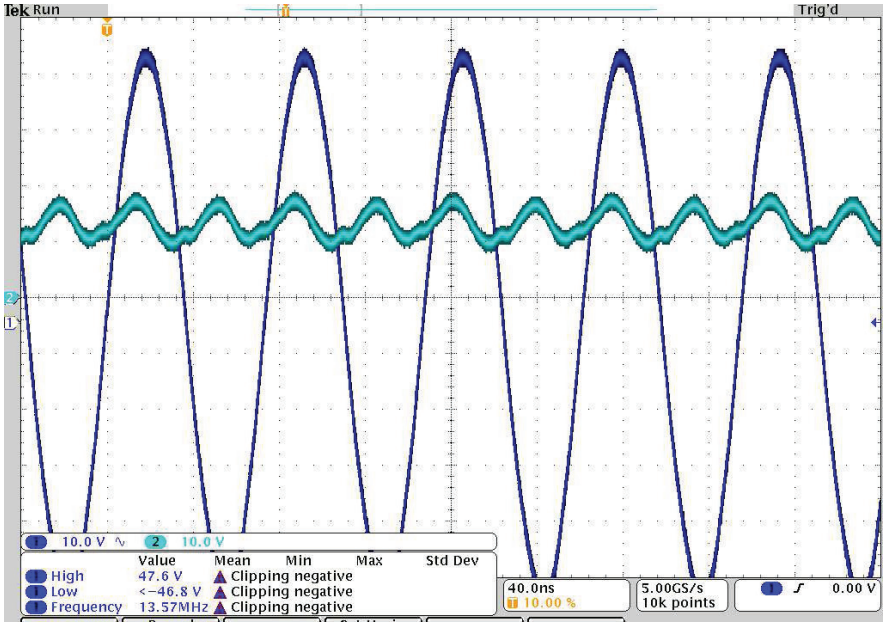


Figure 6.6 Measurement results showing the transmitted signal and output of the rectifier.

from a custom built power transmitter [149]. Two 4-turn inductive coils were place at about 6mm distance with air medium between them. The LC tank circuit consisting of the receiver coil and a variable capacitor was tuned at 13.56 MHz to receive 40V peak-to-peak AC signal

at the rectifier input terminals. Figure 6.5 illustrates the 13.56MHz transmitted and received RF signals measured on oscilloscope. The resulting rectified filtered signal is presented in Figure 6.6. The functionalities of the DC-DC up converter and regulators have also been verified. However, the biphasic ±10V signals drop slightly, when connected to the output stage of the microstimulator (MED).

6.3 Capacitive-link based data transceiver

In case of biomedical implants, most of wireless data transmission protocol uses inductive coupling to transfer uni-directional or bi-directional data between the external system and implantable devices. The limited amount of power that can be delivered through human tissue imposes a major challenge thereto. By far, amplitude modulation (Amplitude Shift Keying - ASK) is the most employed due to the simplicity of its demodulator [150]-[156]. However, researchers have put efforts to investigate several other types of modulation schemes which are OQPSK, DPM and DPSK [157]-[159]. Nonetheless, the disadvantage of widely used inductively coupled circuits is the electromagnetic interference. The neighboring microelectronics circuits in the implant are affected by the electro-magnetic induction, in terms of spreading of magnetic flux around the coils. Moreover, 3D structures of cylindrical coils make it unsuitable and difficult to fabricate high quality coil in planar technology, which is employed to design and implement microelectronics based integrated circuits. These technical challenges have motivated a group of researchers to use the capacitive link in biomedical applications [160]. This principle uses two capacitor plates; the first one is placed outside the body, connected to the data transmitter; and the second plate, physically aligned with the external plate, is located beneath the skin of human body and connected to the internal data receiver of the implant. Both the transmitter and receiver can be placed on the opposite sides of their respective capacitor plates. This configuration is for the down-link data transmission. The location of transmitter and receiver can be reversed for up-link data communication (implant to external). Bidirectional transmission can be established using transmitters and receivers on both sides. Data is transmitted through coupled capacitors via electric field carrier, rather than magnetic flux. Owing to the confined nature of electric flux between two plates, parallel multi-channel data transmission is possible to increase the bandwidth, which is required to stimulate hundreds of neural sites. This approach increases the possibility of widening the area coverage in the visual cortex region. Needless to mention that the fringe charge on the sides of capacitor plates can cause some interferences between adjacent channels but not to the degree caused by the magnetic flux induced in inductive-link. Additionally, contrary to the inductive coupling, capacitive-coupling, due to its high-pass nature, does not restrict the

upper cut-off frequency value.

The capacitive-link data transceiver works based on spatial pulse position modulation (SPPM), presented in [161]. It works following the functional principle of Multiple-Input and Multiple-Output (MIMO) [162] communication systems. The system in [161] was designed in IBM 0.13μm CMOS process and had been verified through post-layout simulations, which showed the data-rate of 200Mbps. This transmission rate, although satisfies our need, yet has been found to be extremely high for down-link transmission. In addition to it, the experimental results of the fabricated chips could not exhibit desired performance. The hardware implementation of this original system [161] using discrete components could not provide satisfactory results either, when tested with sheep skin, placed between two capacitor places. Sheep skin was used for its close proximity of thickness and hair density compared to human brain skin, which was unavailable during these experiments.

It is required to mention that the data transmission rate depends on the total number of

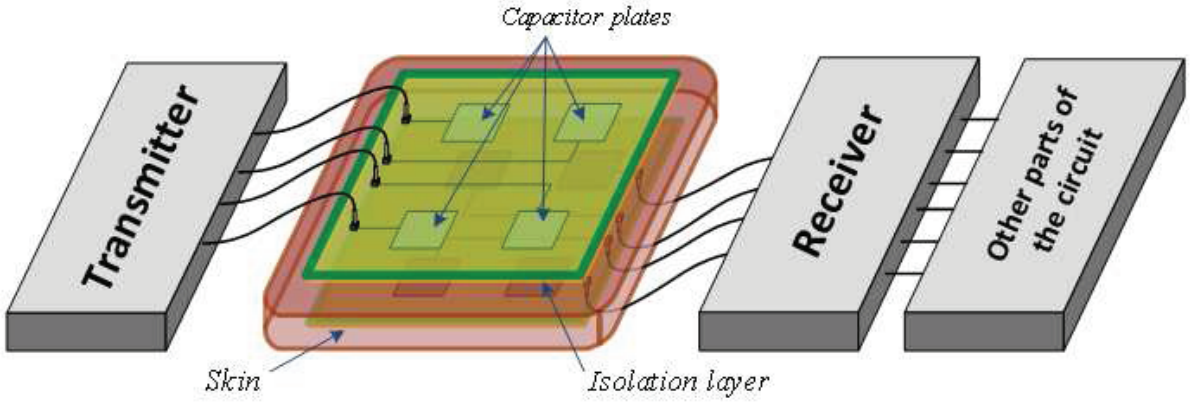


Figure 6.7 Conceptual representation of the proposed multichannel capacitive-link [163]. © IEEE.

neural sites in the visual cortex to be excited, number of simultaneous stimulation in a single microelectrode array, and the parameter used to configure the central controller, which is the length of the serial-in parallel-out (SIPO) shift register in our case. The microstimulation module (MSM) in the newly developed microstimulator is modular in architecture and each MSM is able to support a microelectrode array of 16 (4 x 4) electrodes. Due to the modular architecture, a large number of electrodes, multiple of 16, can be controlled. In the present architecture, each MSM is operated at 50kHZ. Down-link data transmission at 10Mbps through a single capacitive-link data line using SPPM communication scheme allows to control $\frac{\text{10Mbps}}{\text{Lx50kHz}} = 12.5$ microelectrode arrays, where L =16, the length of the SIPO shift register used to convert serial data, received from a single data line, to parallel data sent to each MSM. Increasing the number of data channels to 4 or 8 will allow to stimulate 800 (4

x 12.5 x 16) or 1600 (8 x 12.5 x 16) microelectrodes (stimulation sites) respectively. This calculation is based on the assumption that columns of electrodes in a microelectrode array are stimulated sequentially, not simultaneously. Therefore, 10Mbps data rate per channel is needed for efficient image transmission to the implant with a clock frequency of 10MHz. Accordingly, the previous system was modified to build a new and simpler configuration to meet the specifications of the intracortical vision stimulation project [111], [163]. The conceptual architecture is comprised of a transmitter delivering data to the receiver through four capacitive-links as shown in Figure 6.7. The COMSOL modeling of capacitive-link has been carried out and discussed, and the crosstalk among the adjacent channels have also been investigated.

6.3.1 Modeling of capacitive skin

Transmission capacity of capacitive link

The maximum data rate that can be effectively transmitted over a capacitive channel, called capacity of the link (C), is determined by the following equation according to the Shannon–Hartley theorem [164]:

$$C = B.\log_2(1 + SNR) \tag{6.1}$$

Where, B is the data bandwidth and SNR is the signal-to-noise ratio (S/N) of the data sent over the link. The high-pass nature of the capacitive link sets the lower cut-off frequency of the channel which is determined by the values of resistance and capacitance of the link. According to [165], the bandwidth is inversely proportional to the area of the plate. That is to say, capacitance ↑, lower-cutoff frequency ↓, bandwidth ↑. The SNR is proportional to the the distance between two plates, i.e., the larger is the separation between two plates in the adjacent channels, the less is the signal interference between them.

Characterization of capacitive link using COMSOL modeling

COMSOL modeling was done in two cases, which are for two overlapping and non-overlapping plates [163]. Figure 6.8(a) shows the geometric models of the plates in both cases with the plates' dimensions of 3.5mm x 3.5mm. Each plate was attached to an insulation material with thickness of 1μm and relative permittivity of 3. Skin was represented by a 3.5 mm thick material, inserted between two plates. The simulation results of electric potential and electric field distributions, presented in Figures 6.8(b) and 6.8(c) respectively, prove that the electric

field is constrained within the insulation material. These results also support that the model

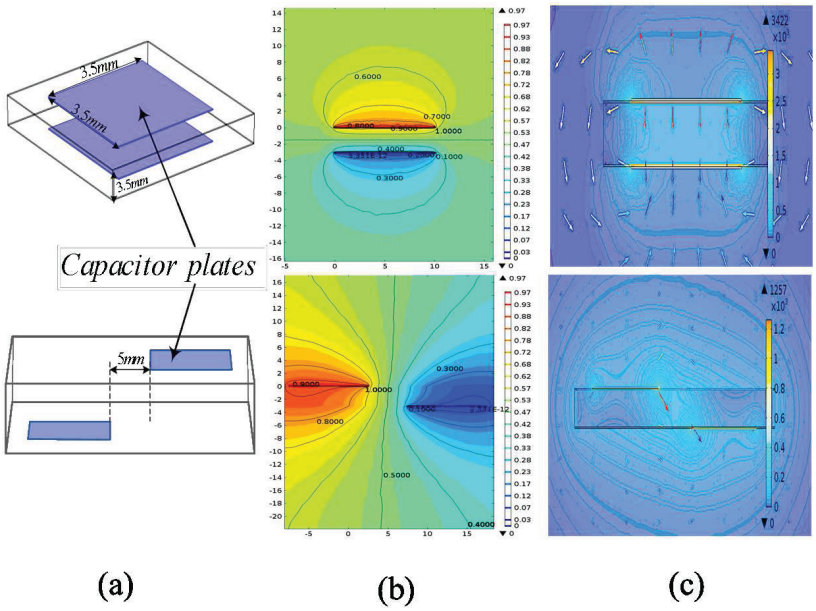


Figure 6.8 Modeling of capacitive-link in COMSOL and simulation results of two overlapping and non-overlapping capacitive plates: (a) Geometric features of the models, (b) distribution of electric potential, (c) distribution of electric field [163]. © IEEE.

is comprised of two dominant capacitors: (1) the first one is created between the upper plate and the skin, and (2) the second capacitor is created between the skin and the lower plate, with the insulation as dielectric for both capacitors. In case of non-overlapping plates, which were separated from each other by a distance of 5mm, electric field distribution remained same, however, charges were concentrated on the inner sides of the plates (Figures 6.8(b) and 6.8(c)). Simulation results show that for plate dimension of 10mm x 10mm, the generated equivalent capacitances in overlapping and non-overlapping cases were 146.8 pF and 38.4 pF respectively.

Characterization of sheep skin: equivalent electrical circuit

M. Takhti et al. have studied the modeling of a capacitive link and presented it in [165]. For our experiments, we used fabricated copper plates on PCB and insulated the former with 1μm thick biocompatible material, Parylene, to prevent any DC current to cross the skin. This thin layer of Parylene raises the capacitance value and thereby, shifting the cutoff frequency of the equivalent high-pass filter to a lower value. The sheep skin, used for this experiment, was characterized at 20 MHz using an impedance analyzer. The magnitude and phase responses of measured impedance of sheep skin are shown in Figures 6.9(a) and 6.9(b)

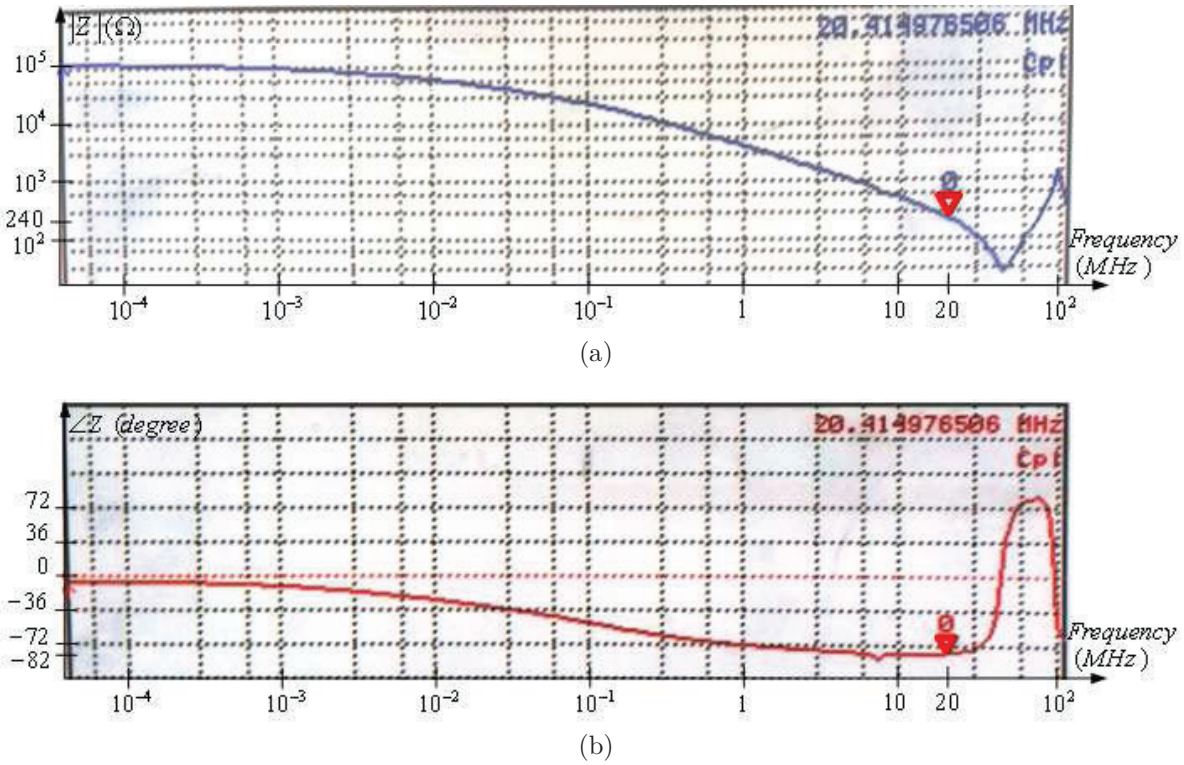


Figure 6.9 Characterization of sheep skin at 20MHz: (a) Magnitude of impedance, (b) phase of impedance [163]. © IEEE.

respectively. Using the derived parameters of the skin, the dielectric properties of Parylene, and the proposed model for the capacitive link in [165], the calculated capacitance between the plates and skin, skin resistance and capacitance have been found to be 2.6nF, 4.2$k\Omega$, and 150pF respectively at 20 MHz.

6.3.2 Proposed data transceiver

The previous system presented in [161] was modified to build a new, simple and stable configuration with the building blocks: spatial pulse position modulation (SPPM) transmitter, skin interface, clock-recovery, and data-recovery [111], [163]. The proposed data transceiver is presented in Figure 6.10.

SPPM transmitter

Two input data lines, A and B, fed to the transmitter inputs, are decoded by a 2-to-4 decoder and passed through clocked AND-gates (Figure 6.10). The decoder and clocked AND gates ascertain that, during any single clock interval, only one out of the four channels in space (spatial) is selected and remains active to transmit the data from two data lines. This method

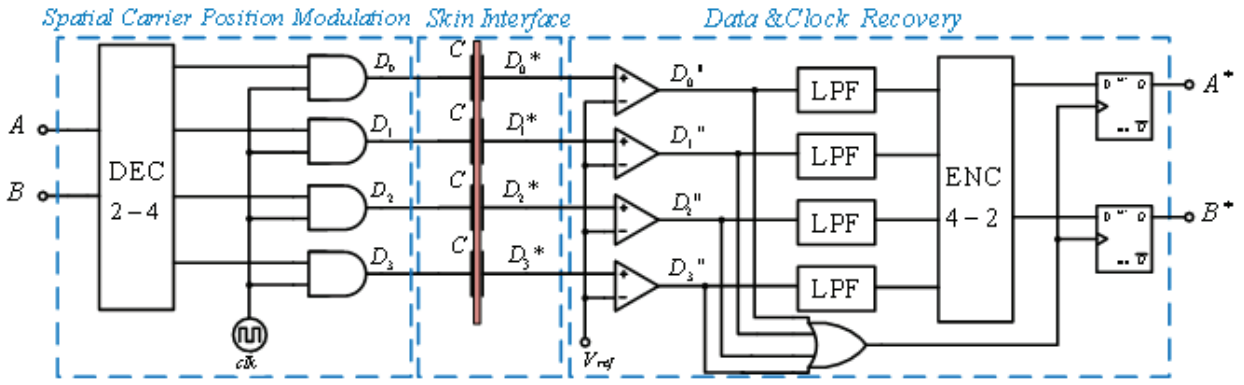


Figure 6.10 SPPM transmitter and receiver used in data transmission for the microstimulator and realized using low-power discrete components [163]. © IEEE.

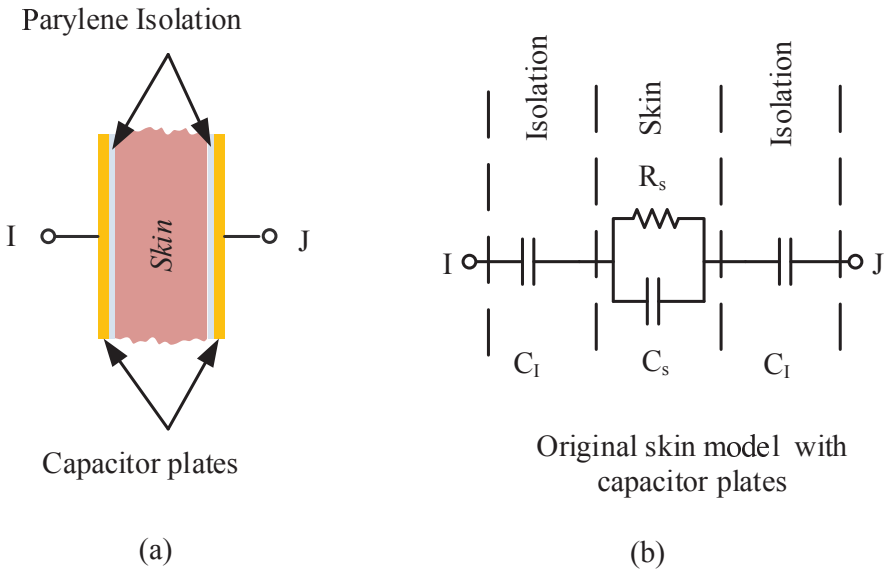


Figure 6.11 (a) Two capacitor plates isolated by Parylene insulation and skin between them, (b) the equivalent circuit of original skin model.

of data transmission implies reduction in the power consumption of the whole system.

Skin model and the interference among the channels owing to skin conductivity

The skin can be considered as a lossy capacitor, which is formed by two parallel plates and the skin between them. The plates and skin are separated from each other by an isolation material, as shown in Figure 6.11(a), which is Parylene in our case. Capacitive link modeling has been studied and investigation shows that the equivalent circuit in Figure 6.11(a) can be represented as in Figure 6.11(b) [165].

In the proposed 2-input system (Figure 6.10), four data lines coming from the transmitter

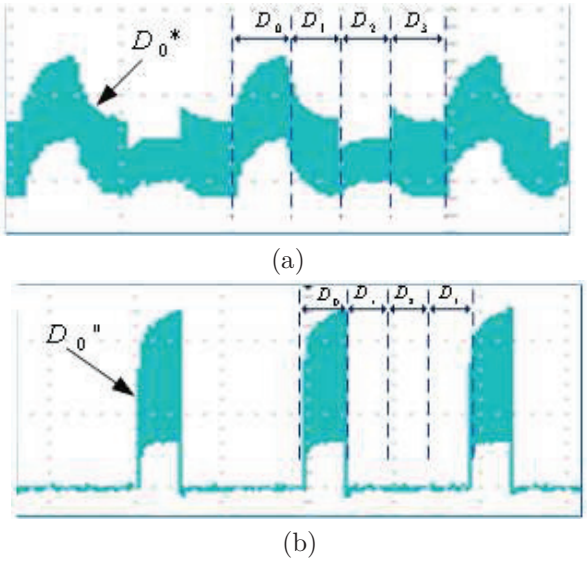


Figure 6.12 Effect of crosstalk between non-overlapping plates on D_0^*: (a) Before the comparator, (b) after the comparator [163] © IEEE.

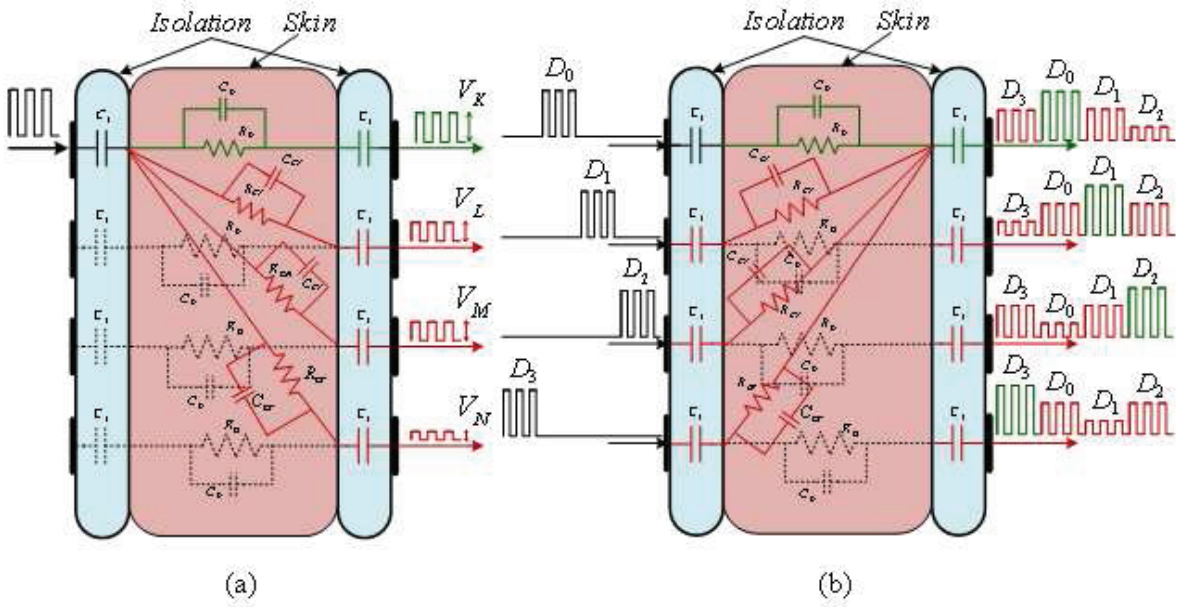


Figure 6.13 Effect of crosstalk among all capacitive-channels: From (a) one input and (b) all inputs [163]. © IEEE.

circuit are connected to the first group of four capacitor plates on the transmitter side. The opposite four plates, forming the second group, are connected to the receiver sides. These insulated plates are placed on both sides of the skin. It was expected to have crosstalk between the non-overlapping plates of communication channels owing to the high conductive

nature of skin. While performing experiments, a high interference between channels was observed due to propagation of the signal, which was applied to one of the transmitting plates. Figure 6.12(a) illustrates this interference. Thus, as shown in Figure 6.13 (left), all the receiving plates experience attenuated version of the original input signal, when it is applied to one plate only. The difference among these signals arises due to the resistances R_{CN} and R_{CF}, and capacitances C_{CN} and C_{CF}, which are directly proportional to the distance between the contact plates. Therefore, each of the received output signals will be corrupted by the signals coming from the non-overlapping plates, when the modulated data D_0, D_1, D_2, and D_3 are applied to the transmitter plates as shown in Figure 6.13 (right). Hence, capacitive plates need to be designed more carefully.

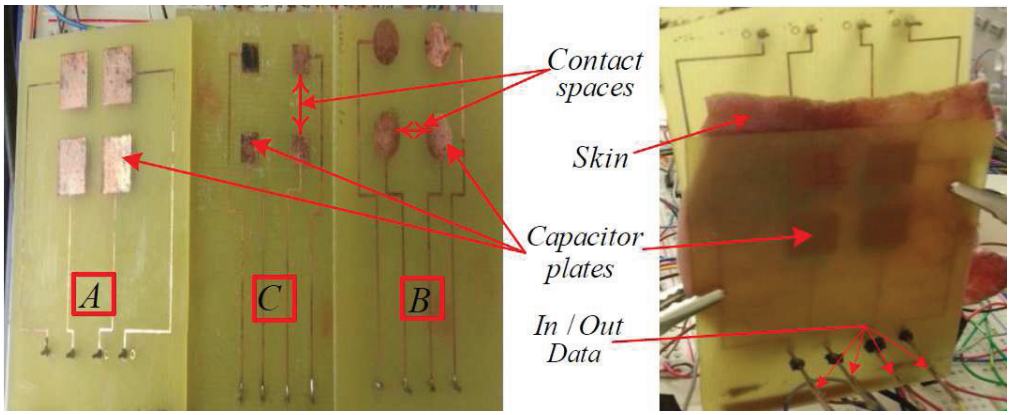


Figure 6.14 Fabricated capacitor plates: (a) Three categories of 4-capacitor plates with different dimensions, (b) 3.5 mm thick sheep skin between emitting and receiving plates [163]. © IEEE.

Table 6.1 Received signals for different sizes of capacitor plates [163]. © IEEE.

Plate name	Plate area (cm^2)	Plate spacing (cm) (adjacent channels)	V_K(V)	V_L(V)	V_M(V)	V_N(V)
A	1	0.5	2.5	1.9	1.9	1
B	0.56	0.75	1.8	1.1	1.1	0.6
C	0.25	1	1	0.2	0.2	0.1

Figure 6.14 shows the various types of capacitor plates (A, B and C) with different sizes, which are reported in Table 6.1. The dimensions of these plates and inter-plate distances are adopted and designed in order to confirm the presence of appreciable difference between the voltage levels of the overlapping and non-overlapping receiving plates. Table 6.1 demonstrates that

the overlapping plate voltage V_K increases, when the plate dimension is larger. On the other hand, the non-overlapping voltages (V_L, V_M, and V_N) decrease simultaneously for wider inter-plate space. Plate A, among all the designed plates for the presented system, favours most to conserve a strong received voltage (V_K) with relatively weaker non-overlapping voltages.

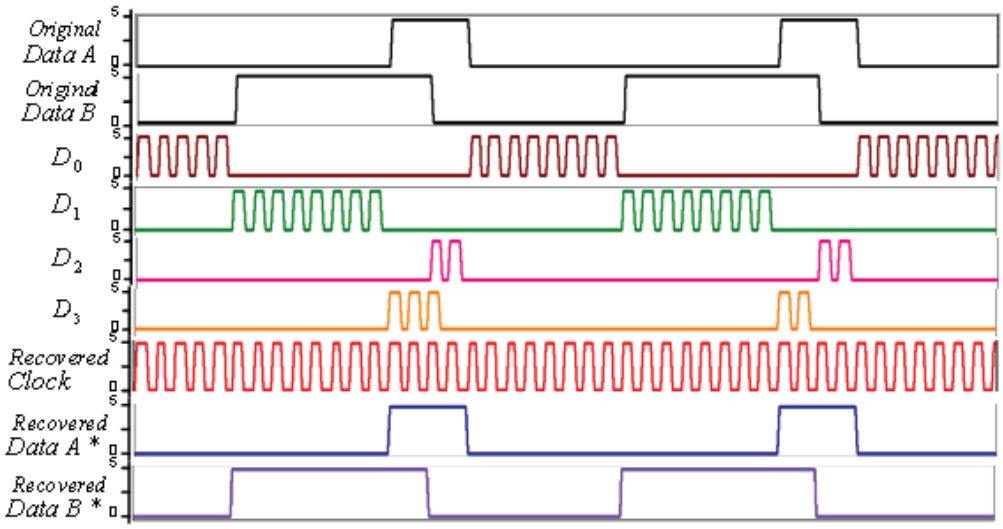


Figure 6.15 Recovered data and clock from simulation results [163]. © IEEE.

Data recovery

Four baseband modulated signals are applied to the inputs of four comparators, which compare the received signals (D_0^*, D_1^*, D_2^*, and D_3^*) from the second plate of each capacitor with V_{REF} to reject the interferences from the other channels and amplify the main signal (Figure 6.10). In the current design, V_{REF} is the average value of the signal in the active channel and second largest signal, which appears to the non-active adjacent channel owing to the interference. A calibration circuit receives signals from four capacitive-links as feedbacks and determines the value of V_{REF}. The outputs of the comparators, (D_0'', D_1'', D_2'', and D_3''), as illustrated in Figure 6.10, are provided as inputs to the low pass filters to eliminate the clock from the modulated data and encoded to recover the original data signals (A & B). At the end of the receiver, the retrieved data, (A^* & B^*) and clock are synchronized by adding two clocked D-flip-flops .

Clock recovery

A 4-input OR-gate adds all the clocked signals, D_0'', D_1'', D_2'', and D_3'', from the outputs of the comparators and generates a clean recovered clock (Figure 6.10).

Figure 6.15 illustrates the simulation results of the transceiver, which include the original and modulated signals, the recovered data and clock.

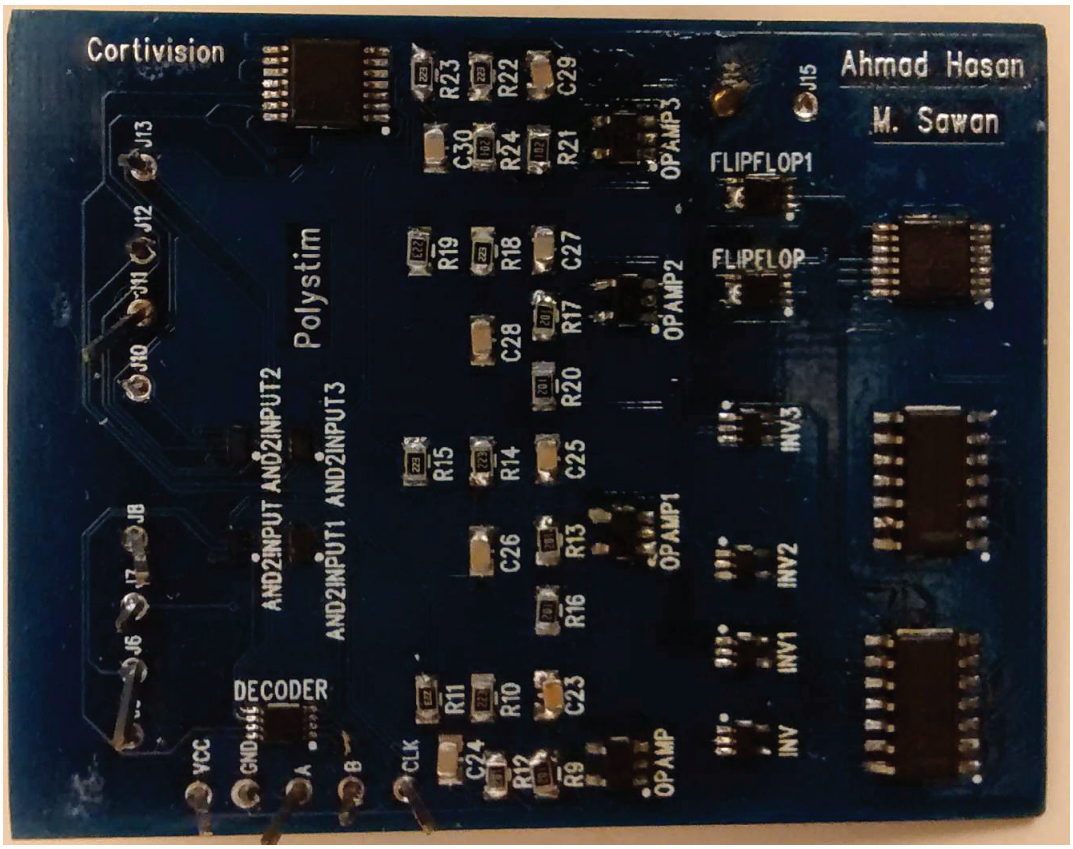


Figure 6.16 Experimental results: Discrete component based SPPM transmitter and receiver assembled on a PCB.

6.3.3 System implementation, experimental results, and comparison

This data-link transceiver is implemented using low-power surface mount discrete components, presented in Figure 6.16 and its functionality has been verified with 3.5 mm thick sheep skin, inserted between capacitor plates. The capacitor plates are fabricated with copper plates of various dimensions and shapes, as mentioned in section 6.3.2, printed on PCB and coated with 1μm thick Parylene insulation material. The optimum experimental results were obtained for the capacitor plates of dimension 10mm x 10mm and 5mm separation. Although, our system is proposed to transmit data stream at a bit rate of 10Mbps per channel with the clock frequency of 10MHz, the recovered data rate, which is 3Mbps, is lower than our expectation value due to the band-width limitation of the surface mount comparators

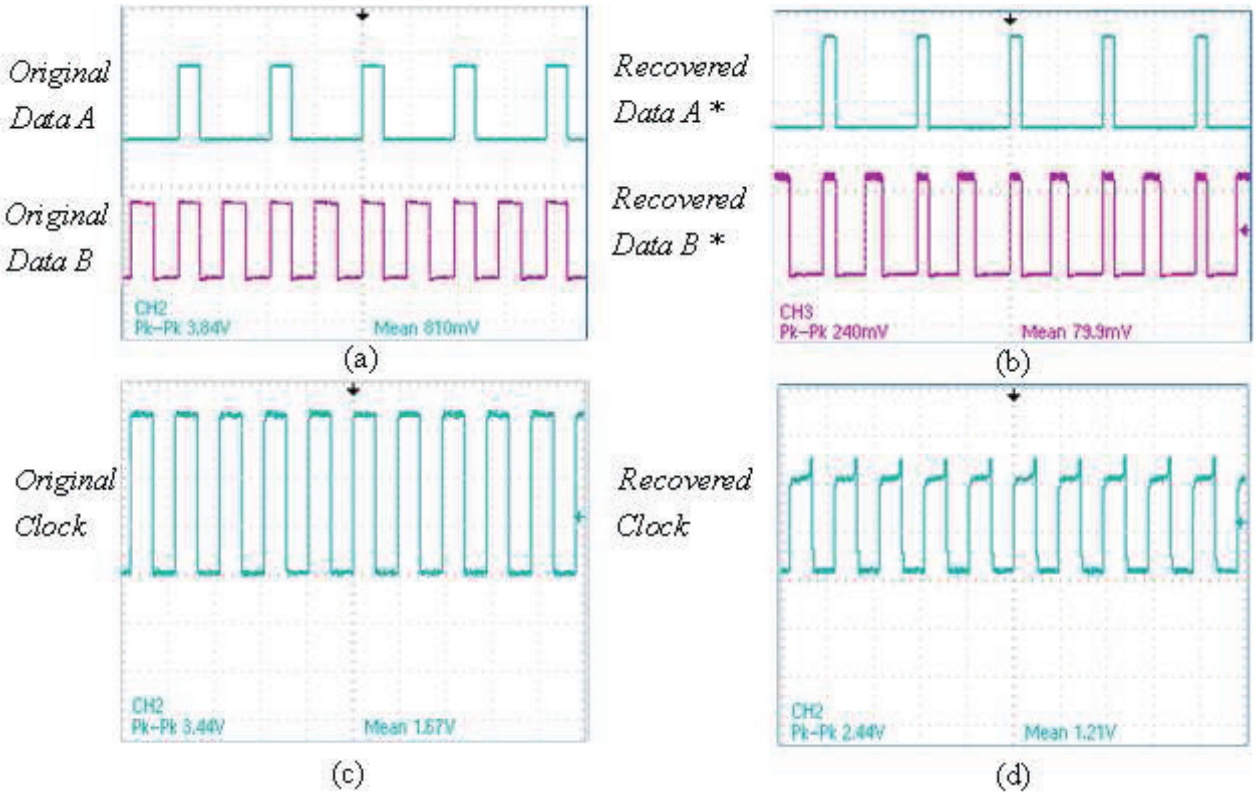


Figure 6.17 Experimental results: (a) Input data A & B, (b) recovered data A* & B*, (c) input clock signal, (d) recovered clock signal (modified version from [163]).

used in the design. Figures 6.17(a) and 6.17(b) show the applied input and recovered data signals (A & B) and (A* & B*) respectively. The original and recovered clocks are presented in Figures 6.17(c) and 6.17(d) consecutively.

Table 6.2 shows a general comparison between the recently reported data-transceivers primarily designed for biomedical implants and our implemented design. The system in [158] used inductive coupling approach, where the data rate carrier frequency is restricted to 13.6 MHz and they used air as the medium for experiments; whereas our system has been tested with real sheep skin. The capacitive-link based approach implemented in [161] achieved the highest data rate of 200 Mbps and low power consumption of 3.75 pJ/bit, but these results were obtained by post-layout simulations of the customized integrated circuit (IC) and without any experimental validation. The system developed with the Amplitude-Engraving Modulation (AEM) and presented in [166] was not validated with the experimental measurements as well. Mohammadi et al. approached with a new capacitive-link based design, however the power consumption is very high [167]. Moreover, the technical challenge for a multichannel data transmission, such as crosstalk among the data channels, was not clearly

Table 6.2 Results comparison with recently published data transceivers.

Reference	[158]	[161]	[166]	[167]	This work
Link	Inductive	Capacitive	Capacitive	Capacitive	Capacitive
Modulation	PDM	SPPM	AEM	SPI	SCPM
Carrier(MHz)	13.6	Baseband	Baseband	Baseband	Baseband
Data Rate(Mbps)	13.6	200	2	10	3
Consumption(PJ/bit)	1122	3.75	-	4560	150
Experimental medium	Air	-	-	Chicken skin	Sheep skin

investigated and analyzed in all the presented capacitive-link based designs. The data-rate of the proposed system is limited to only 3Mbps owing to the bandwidth limitation of the discrete components and can definitely be enhanced to higher than 20Mbps following the custom integrated circuit approach. The proposed system has also been verified through experiments with sheep skin and custom fabricated capacitor plates. We also investigated the crosstalk issue among the channels. New robust multichannel data communication schemes are being explored by one of the Polystim team member and the most suitable one to resolve the crosstalk problem will be employed in the future version of this transceiver. An integrated version of this system with the new communication scheme, optimum power consumption and our specified data-rate will be laid-out, and the post-layout simulation and experimental results will be presented in the future articles.
Bi-directional communication channels can been realized using a secondary transceiver unit, and switching the positions of the transmitter and receiver compared to the primary transceiver unit.

6.4 Conclusion

This chapter dealt with the design and validation of the proposed inductive-link based energy recovery unit and capacitive-link based data transceiver. We investigated (i) the technical challenges, such as crosstalk to identify specifications relating multichannel capacitive-link based data transmission, and (ii) specifications for integrated circuit based wireless energy-recovery units. Regarding the inductive energy recovery unit, the rectifier was solely designed for the bladder implant [146] and optimized to deliver power at load of 3 mA to 5 mA. This load current was dedicated for the regulators and DC-DC converter implemented in the chip ICJPMFMS [148], [146]. In our case, the load current is delivered to the commercial charge-pump based DC-DC up converter and LDOs. Additionally, we have higher requirement considering the generation of -10V. From implantation perspective, the data-receiver is located within the implant and is also supposed to derive supply voltage from the power

recovery unit. Therefore, considering all these cases, optimization is needed in the design of and requirement from this unit. A complete integrated approach can be followed which will include also a power management unit to control power for the micostimulator, central controller, and the data-receiver.

CHAPTER 7

THE ETI VOLTAGE MONITORING UNIT, CENTRAL CONTROLLER, ASSEMBLY, AND IN-VITRO VALIDATION OF THE MICROSTIMULATOR

7.1 Introduction

In this chapter, we present the ETI voltage monitoring unit and the central controller. We also discuss the assembly strategy of different parts of the microstimulator; i.e., the microelectrode array driver and stimuli-generator microchips, SAR ADC, components for the monitoring unit, microelectrode array, and analog multiplexers (MUXs). A brief description of the assembled microeletrode array has also been presented. Procedures for the in vitro tests have been discussed. The experimental results, involving biphasic stimulation for different types of stimulation waveform, have been included in multiple cases, such as (i) RC model (equivalent circuit of microelectrode) and (ii) fabricated Pt-coated microelectrode array. The assembly of the microstimulation module is described in section 7.4 and the experimental results are presented in section 7.5.

7.2 Monitoring unit

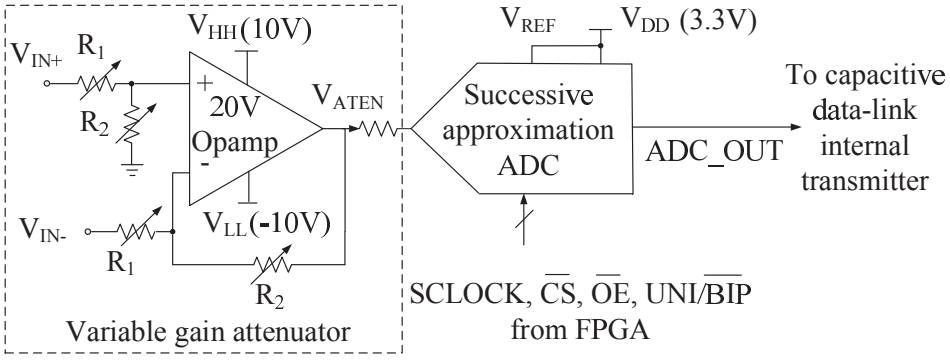


Figure 7.1 The ETI-voltage monitoring unit: Variable gain attenuator and the 3.3V SAR ADC.

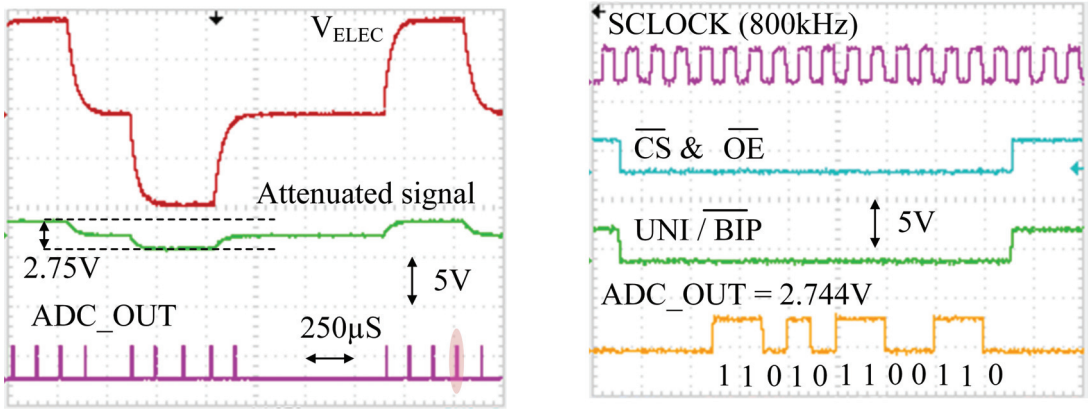
Figure 7.1 shows the circuit diagram for the electrode-tissue interface (ETI) voltage monitoring circuit [169]. For stimulation current of about 100μA through two microelectrodes, configured in bipolar arrangement, the maximum electrode voltage reaches up to $\pm$10V. The

input stage of the monitoring circuit is designed to withstand this high voltage. The 20V operational amplifier, along with four resistors, is configured as a variable gain attenuator, where the attenuation factor is determined by the ratio of R_1 and R_2. The output voltage is defined according to the following equation [168]:

$$V_{ATEN} = (V_{IN+} - V_{IN-}).\frac{R_2}{R_1} \tag{7.1}$$

Where, V_{ATEN} is the amplified or attenuated (attenuated in our case) signal from the differential input signals, V_{IN+} and V_{IN-}, which are the measured potentials across the electrodes. Both V_{IN+} and V_{IN-} contain the DC and AC potentials built up across electrodes during stimulation phase. The ratio of R_1 and R_2 is set to 1: 6.67 to attenuate the peak value of the monitored biphasic voltage and bring it within the conversion range of the successive approximation (SAR) analog-to-digital converter (ADC).
The 12-bit SAR ADC is supplied by 3.3V and for clock frequency of 3MHz, the conversion rate can be up to 312.5ksps. The reference voltage, V_{REF} is set to 3.3V to facilitate maximum input voltage swing. The ADC is configured to digitize biphasic analog signal received from the attenuator. The converted bit stream is applied to the internal secondary transmitter of the capacitive-link for wireless monitoring purpose.

7.2.1 Experimental results



(a) (b)

Figure 7.2 Oscilloscope traces: (a) The biphasic stimulation signal in channel-1 output of the MED (top), attenuated signal (middle) and ADC output (bottom). (b) The control signals to the ADC and zoomed view of the resulting binary output.

Constant current amplitude of 110μA was delivered from the microstimulator to perform biphasic stimulation and to verify the functionality of the assembled monitoring unit. Two

RC models of microelectrode, where R = 46kΩ and C = 1.2nF, were connected in series between I_{OUT1} and I_{OUT2} (MED outputs) during the course of microstimulation in channel-1 of the MED. The attenuation factor was set to 6.67. The applied clock frequency to the ADC was 800kHz. The digitized value from the ADC, which is 2.774V, closely approximates the attenuated stimulation signal value, which is 2.75V. The measured stimulation signal at the output of the MED, attenuator output and the signal converted by the ADC are shown in Figure 7.2(a). The other control signals to the ADC and the binary value of the ADC output (zoomed) are presented in Figure 7.2(b).

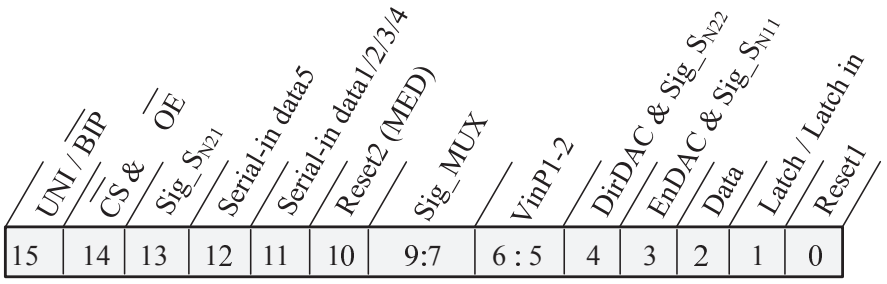


Figure 7.3 The 16-bit data stream containing stimulation parameters for the stimuli-generator and microelectrode driver chips, multiplexers, and the successive approximation (SAR) ADC.

7.3 Central controller

The central controller receives recovered data A* & B* serially as the stimulation control parameters from the internal capacitive-link data receiver, and stores the data in a 16-bit serial-in parallel-out (SIPO) shift register [169]. The information bits of the register are presented in Figure 7.3. Bit[0, 2, 5: 9] program the stimuli-generator chip and three multiplexers, bit[1, 3: 4] control both stimuli-generator and MED chips, bit[10: 13] provide stimulation parameters to the MED, and bit[14: 15] program the SAR ADC. A "Reset" signal clears the output of the register in the first clock pulse and data starts to load from the rising edge of the second clock pulse. The 16-bit control signal is delivered to different parts of the microstimulator after 17 clock pulses with the rising edge of the "Load" signal. The central controller is realized with a 9 x 9 pin ball grid array (BGA) and chip scale package (CSP) IGLOO nano field programmable gate array (FPGA) chip. The small area of 5mm x 5mm and ultra low profile pitch of 0.5mm allow the miniaturization of the microstimulator.

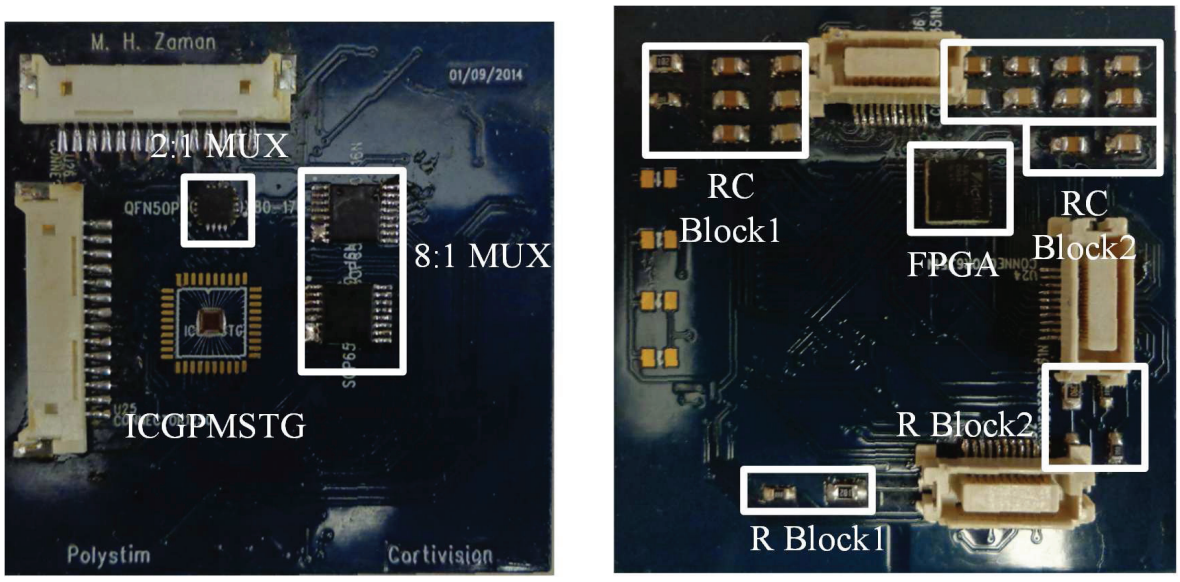
7.4 Assembly of the microstimulation module

We have designed and fabricated three high density interconnect (HDI) printed circuit board (PCB), namely PCB1-PCB3, to assemble different parts of the microstimulation module and interface with the newly fabricated microelectrode array.

PCB1, a 4-layer PCB with the thickness of 0.8mm, contains the wire-bonded stimuli-generator chip die, and two 2-to-1 and two 8-to-1 MUXs on its top side as shown in Figure 7.4(a). The stimuli-generator chip die is, at first, glued on the surface of the PCB and then, wire-boded to the dedicated surrounding PCB pads. All the MUXs are surface mount discrete components and soldered to the associated PCB pads. An ultra small 81-pin ball grid array (BGA) packaged IGLOO nano FPGA chip with the dimension of 5mm x 5mm has been chosen as the central controller. The FPGA chip, and the associated capacitors and resistors are soldered at the bottom side of this PCB (Figure 7.4(b)). This PCB is made of 4-layer to access the pins located in the internal columns (rows) of the BGA package using micro-vias of 10mil diameter.

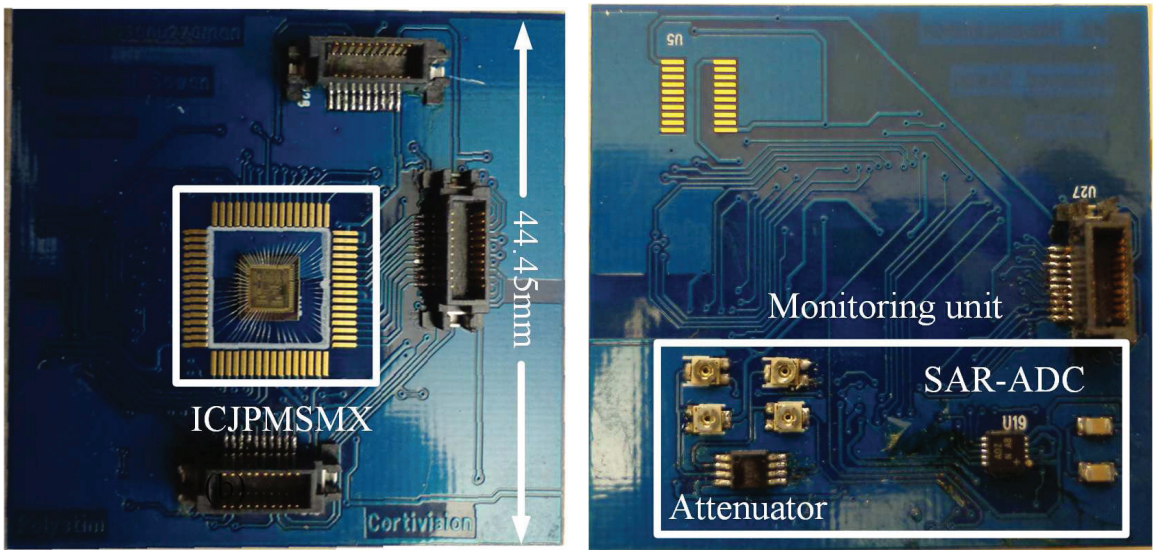
PCB2 is a two layer PCB of thickness 0.5mm. The MED chip die is wire-bonded to the top side of PCB2 as presented in (Figure 7.5(a)). The surface mount components for the monitoring circuit; and 20V operational amplifier and the associated variable resistors, and the SAR ADC for the monitoring unit; are soldered at the bottom side of this PCB as illustrated in Figure 7.5(b). The end dimension of PCB1 and PCB2 is 44.45 x 44.45mm^2 each. PCB1 and PCB2 are stacked on top of each other by surface mount ultra-low profile Molex 20-pin connectors of 0.635mm pitch (Figure 7.6(a)). The end height of the stacked PCBs is 9mm.

To interface with the microelectrode array, PCB3, a two layer PCB of thickness 0.5mm, has been used. A square sized opening (hole) of 3.5mm x 3.5mm has been created in the middle of PCB3 to access the pads which are located on the back side of the MEA. When microfabricated, the MEA substrate was extended on 4 sides to support itself under PCB3. As shown in Figure 7.7(a), the extended MEA substrate has been glued to the bottom side of PCB3 using H20E epoxy. 24 rectangular pads, 6 pads on each side of the opening of the PCB, are positioned to connect the MEA pads through wire bonding (Figure 7.7(b)). Compared to two other PCBs, the dimension of PCB3 has been made smaller to fit it with that of the MEA. PCB2 is interfaced with PCB3 with a ribbon cable, connected to the wire bonded pads on PCB3.



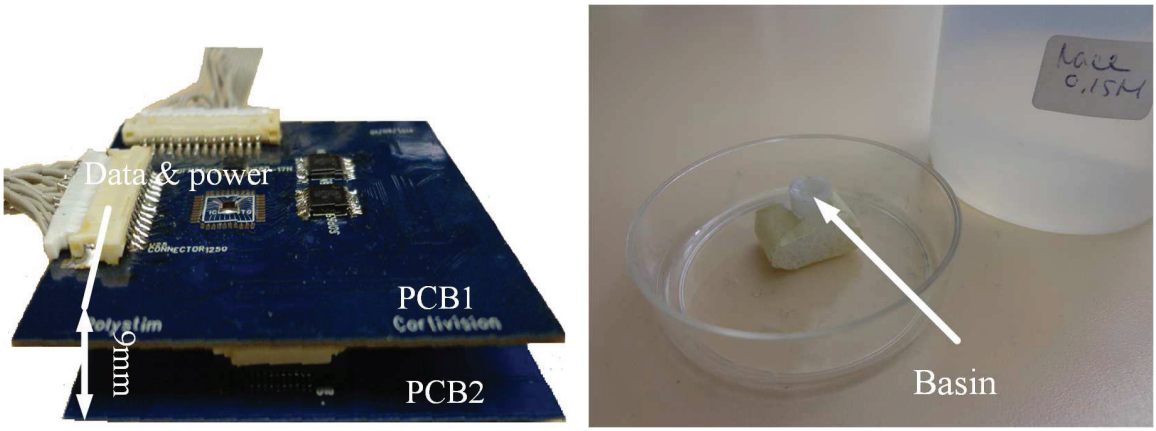
(a) (b)

Figure 7.4 The assembled microstimulator prototype: (a) Top view of PCB1 containing the wire-bonded stimuli-generator chip die, 2:1 and 8:1 MUXs and connectors; (b) the assembled FPGA chip, the associated resistors and capacitor, and connector on the bottom side of PCB1.



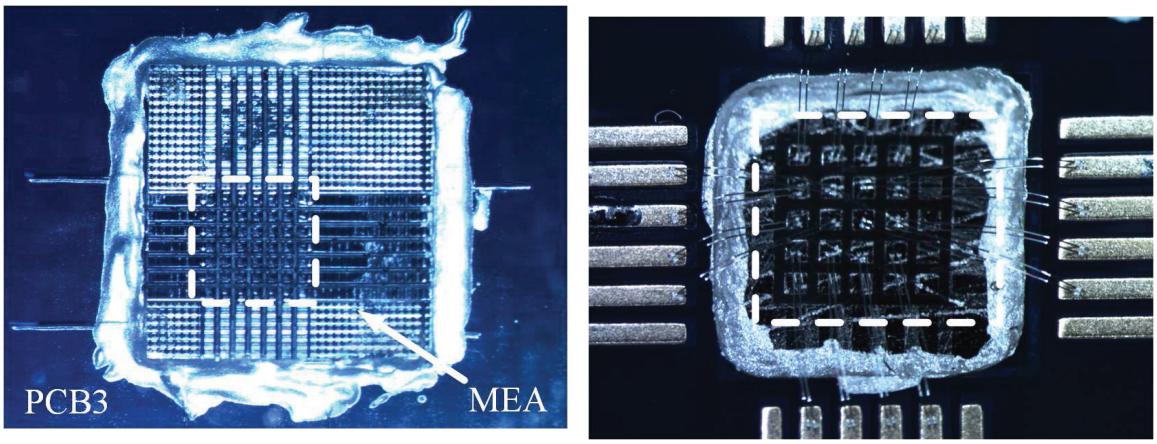
(a) (b)

Figure 7.5 The assembled microstimulator prototype: (a) Wire-bonded MED2 chip die and connector on the top side of PCB2; (b) the monitoring unit (the attenuator and ADC).



(a) (b)

Figure 7.6 The assembled microstimulator prototype: (a) Vertically stacked PCBs; (b) basin filled with 0.15M NaCl solution for in-vitro test.



(a) (b)

Figure 7.7 The assembled microstimulator prototype: (a) MEA, glued underneath the opening in PCB3; and (b) MEA pads, wire-bonded to PCB3 pads.

7.5 Experimental results

The experimental setup to validate the microstimulation module and the MEA is presented in Figure 7.8. From the stimuli-generator, half- and plateau-sine pulse, and constant currents with the range 11.6 to 120.64μA, were applied to four channels, Istim1 .. Istim4, to generate both monophasic and biphasic stimulations. In channel-1, while generating charge-balanced biphasic stimulation signals between I_{OUT1} and I_{OUT2}, control signals were applied to the

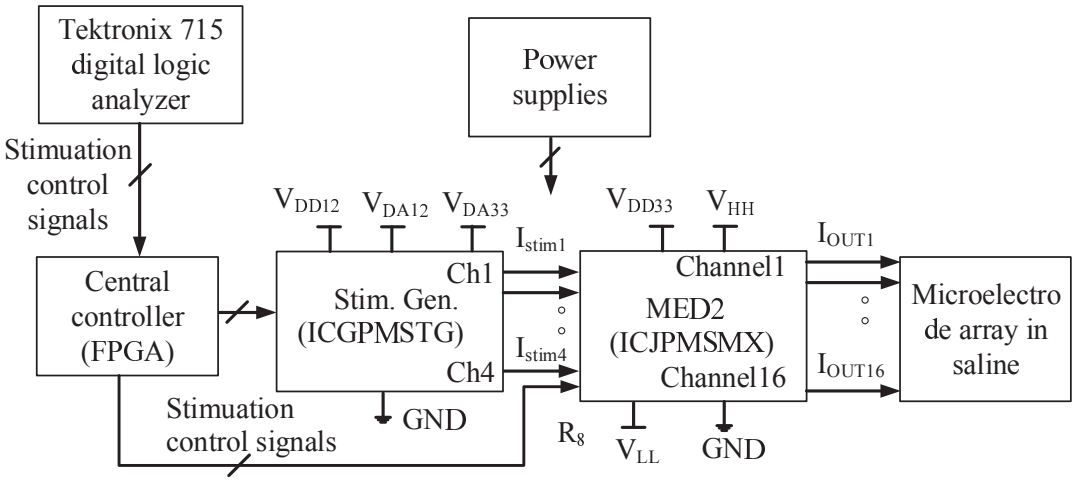


Figure 7.8 The experimental setup for validation of the microstimulation module and the MEA.

switches, S_{N11}, S_{N22}, and S_1 - S_4. Two microelectrode models, emulated by a resistor of 46kΩ for each, were connected in series between these outputs. Similar procedures were followed for channel-2 to channel-4.

In Ch3, plateau-sine source current with amplitude of ±120μA and in Ch4, half-sine source current with magnitude of ±110μA were employed for cathodic first and anodic first stimulations in succession. The generated waveforms across two 1kΩ resistors for PS and HS current pulses from the SG are shown in Figure 7.9(a)(top) and Figure 7.9(b)(top) successively. The corresponding measured waveforms across 92kΩ (equivalent) resistors, connected at the outputs of the MED, are presented at the bottoms of Figure 7.9(a) and (b).

Figure 7.10(a) illustrates the oscilloscope graphs of the measured differential voltages across the resistive loads of 92kΩ, connected in four channels, for various input constant current amplitudes, pulse-widths, inter-pulse durations, and stimulation frequencies.

7.5.1 Microelectrode array

We have interfaced a novel 3D microelectrode array (MEA) [40] with our microstimulator for performing in-vitro tests. This MEA was designed and fabricated for this project by one of the previous Polystim Neurotech Laboratory members. Therefore, the design and fabrication of this MEA do not count to the contribution of this thesis. However, contribution in this thesis has been made in interfacing the microstimulator with the MEA, and characterization of both systems through in vitro experiments. A brief description on the design and

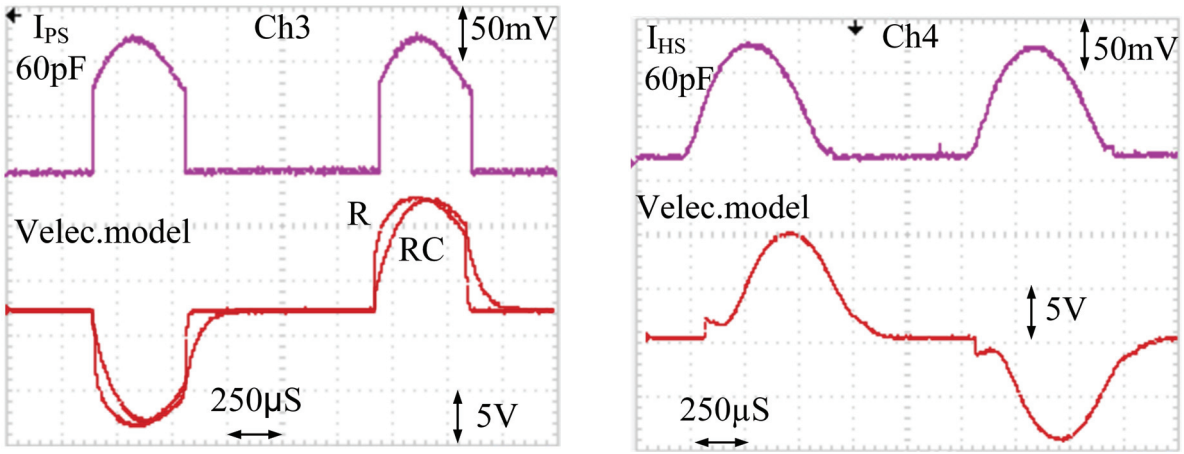


Figure 7.9 Experimental results: Generated waveforms due to (a) PS and (b) HS current pulses from the SG (top) and, the corresponding stimulation signal at the output of the MED (a) and (b) (bottom).

fabrication techniques has been provided here for the ease of understanding of the readers. The high-density silicon-based MEA was designed and fabricated following micromachining techniques. Geometrical features of these electrodes allow more contacts between the electrodes and targeted neural tissues. To electrically isolate the electrodes, the polish side of the wafer was cut, filled with glass, and polished. To achieve 3D structure, the other side of the substrate was cut with variable depths. As a result, a 5 x 5 electrode array with variable heights of 1.45, 1.55, and 1.65mm was obtained. The thickness of the electrodes was 200μm at the base and less than 2μm at the tip with 100μm spacing. The front side of the arrays was coated with Parylene-C to encapsulate and improve the biocompatibility of the electrodes. A new masking method was used to remove Parylene-C from the tips of the 3D electrode array. This method enhanced a uniform tip-exposure [40]. The active sites of the electrodes were sputter-deposited with thin-film of Platinum (Pt) to facilitate charge transfer from electrode to neural tissues. Biostat VMP-300 electrochemical impedance system was used for performing electrochemical impedance spectroscopy (EIS). The instrument was operated under the computer control with EC-Lab software. A solution of 0.9% PBS was used as the electrolyte in a three-electrode cell, consists of a Ag/AgCl reference electrode and two others as a counter and a working electrodes. At 1kHz sinusoidal input voltage signal, the average impedance of Pt-coated electrodes was 70kΩ. Figure 7.11 illustrates the SEM images of the MEA.

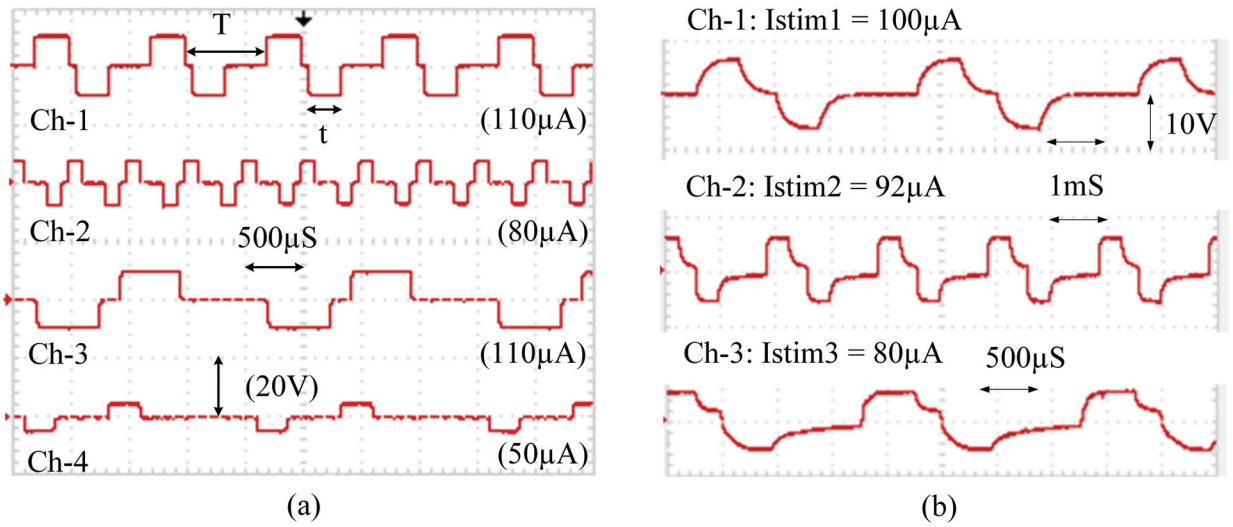


Figure 7.10 (a) Measured stimulation signals in four output channels of the MED for resistive loads and different constant current levels. (b) In vitro experimental results obtained using Pt-coated MEA.

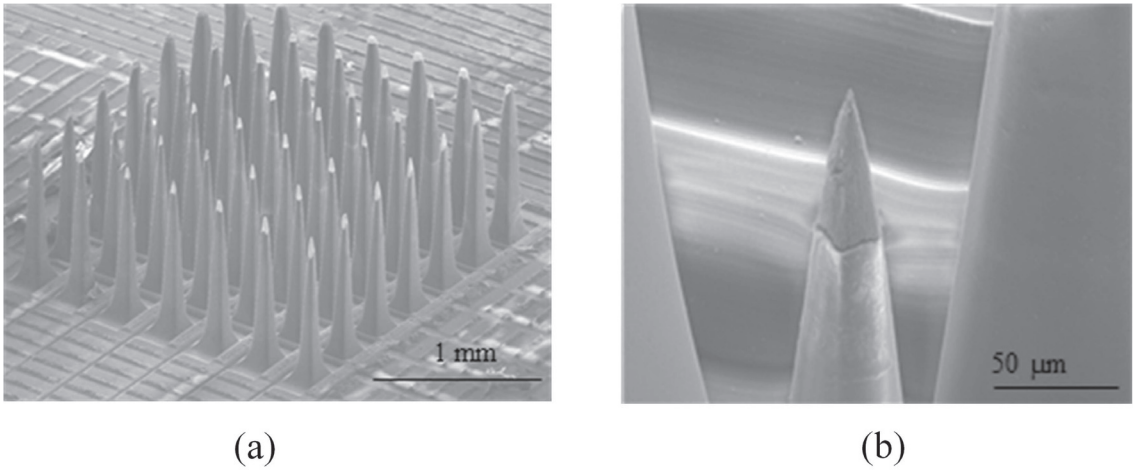


Figure 7.11 SEM images of the MEA: (a) 3D penetrating microelectrode array, (b) the tips of the electrode sputter-deposited with Pt. © [40].

7.5.2 In vitro tests

Before carrying out the microstimulation, the MEA was immersed in 0.15M NaCl solution, poured in a basin with the depth of 4.0mm and diameter of 3.5mm, as presented in Figure 7.6(b). Constant current was varied between 11.6 to to 110μA and injected to different pairs of electrodes, connected in bipolar configuration in multiple sites. This experiment shows an average impedance of the microelectrodes, located on the sides of the MEA, of

65 to 70kΩ. Figure 7.10(b) demonstrates the in vitro test results, showing the variation of biphasic stimulation current amplitudes, pulse-widths, inter-pulse durations, and stimulation frequencies in the output channels-1, 2, and 3 of the microstimulator. In the results, the effects of double-layer capacitances at the electrode-electrolyte interfaces are very prominent. In all cases, charge-balanced and biphasic stimulations were carried out. The obtained maximum compliance voltage across the loads was 10V per phase or 20V per anodic and cathodic phases. However, this compliance voltage rises to 20V per phase when V_{HH} and V_{LL} are increased to ±13V.

7.5.3 Performance comparison

A comparison between our design and other microstimulators, reported in [61], [7], [13], [108], [8], [80], and [92] has been presented in Table 7.1. This table is the duplicate version of that presented in Chapter 3, with the exception of inclusion of this work. The MSM, in our proposed microstimulator, consumes 4.66mW quiescent power, which is much lower compared to the system in [13]. The latter design includes an on-chip high-voltage DC-DC converter, which consumes high-power and causes it to exceed the minimum allowable quiescent power dissipation limit for the implantable biomedical devices. The microstimulators in [7], [92] consume less power as their designs are implemented in a single chip using one CMOS technology and are not integrated with the output stages to deliver the required high-voltages across the high-impedance of ETI. The system in [61] is limited to 4 channel only and therefore, less power consumption compared to our case is reasonable. To the authors' knowledge, the achieved compliance-voltage of this microstimulator is the highest among the reported custom integrated microstimulators. This compliance voltage increases up to 20V per phase, when the high-voltage supplies (V_{HH} and V_{LL}) in the output stage (MED) are increased to ±13V. The new types of stimulation current waveform, in addition to the constant, HS and PS current pulses, facilitate exploring their efficiencies in exciting neural tissues and energy saving capabilities. The stimulation current level, although, not maximum compared to the other designs, is yet sufficient to meet our demand. However, the total area, in this case, is greater compared to those in [61], [7], and [8] owing to two different technologies used and the electrode voltage monitoring feature, and that in [13] due to the increased number of channels. Besides, this system has been assembled with a novel pyramidal shaped MEA and the functionality of the complete system has been validated through in vitro tests. The data and power recovery units were tested separately and not employed to the MSM. Therefore, their performance is presented separately. The achieved data rate was 3Mbps due to the bandwidth limitation of the discrete components and the wireless power budget has been limited to 50mW to satisfy the standard of biomedical devices.

Table 7.1 Performance comparison of the microstimulators.

Parameters	[61]	[7]	[13]	[108]	[8]	[80]	[92]	This work
Technology (μm)	0.35[a]	0.18[b]	0.18[b], 0.8[a]	0.18[b], 0.8[a]	1.5[b]	0.18[c]	3.0[b]	0.13[b], 0.8[a]
Nom. power supply (V)	3.3, 20	1.8, 3.3	1.8, 3.3	1.8, 3.3	5	N/A	$\pm$5	1.45, 1.5, 3.3, $\pm$10
Compliance Voltage (V)	20	2.98[d]	13.7[d]	8.25	0.15-5[e] 0-4.75[1]	VDD–0.5	< 10	20[h]
Max. stim. current (μA)	1000	140[d]	1.6-167.2	2000	$\pm$270	64	127	220
Consumed DC power (mW)	1.16	0.88	27.2, 54.91[i]	N/A	16.5	N/A	0.78	2.1[i], 2.56[j]
Area (mm^2)	0.2[g]	3.2x2.8	2.9x2.9[i], 1.01[j]	9	4.6x4.6	2.0x2.0	5.7x4.0	4x4[i], 1.75x1.75[j]
No. of stim. sites	4	16	4	N/A	32	16	64	16
Load (kΩ)	1, 10	10	100, 150	9.125	45, 210[k]	71.4, 78.5	N/A	70[l], 92

[a] HV CMOS, [b] CMOS, [c] BiCMOS, [d] Source and sink,
[e] Source, [f] Sink, [g] Per four output channels, [h] Combining anodic and cathodic phases, and this value increases up to 40V, when V_{HH} and V_{LL} are increased to $\pm$13V,
[i, j] Output-stages and stimuli-generators respectively,
[k] Iridium/Iridium-oxide coated microelectrode, [l] Platinum coated microelectrode

Table 7.2 Performance comparison of the data and power recovery units.

Parameters	[61]	[7]	[13]	[108]	[8]	[80]	[92]	This work
Data-rate (Mbps) (wireless)	2[m]	1.5[n]	N/A	N/A	2.5[n]	1.2[n]	N/A	3[o]
Power tran. carrier freq. (MHz)	13.56	13.56	N/A	N/A	5/10	4.8	N/A	13.56
Application	R[p]	I[q]	I[q]	N/A	I[q]	I[q]	I[q]	I[q]

[m] Optical coupling, [n] Inductive coupling, [o] Capacitive coupling,
[p] R = Retinal, and [q] I = Intracortical.

7.6 Conclusion

In this chapter we presented the ETI voltage monitoring unit and the architecture of the central controller. We have elaborated also the assembly methodology of the microstimulator and the MEA, and presented in vitro experimental results. The microstimulator is highly-integrated and dedicated for visual intracortical microstimulation. The proposed architecture is configurable for all types of microstimulation and featured with various types of energy-efficient waveform. The MS module is modular in architecture and can be duplicated to cover the large V1 area. However, the end size of the integrated MS module has been retained to be large because of the functional verification purpose and can be reduced for the implantation.

Concerning the implementation of the central controller, the supplies of three I/O banks among four of the FPGA, are set to 3.3V and the last I/O bank is connected to 1.5V, which is also the FPGA core voltage. The reason is that majority of the I/O banks are connected to the digital blocks of the second MED chip and the multiplexers (used at the output of the ICGPMSTG chip), which are supplied by 3.3V. The 800kHZ clock frequency, fed to the 16-bit SIPO shift register, is reduced to 50kHz required for the microstimulator. The current drawn from the 3.3V increases to 16mA, when the FPGA is operated at 800kHz. This current can be brought down using smaller length such as 4- or 8-bit registers, requiring low input clock frequency. Further power can be saved connecting I/O banks to the corresponding supplies (3.3V or 1.5V) only during microstimulation.

The most challenging task of this project was to assemble all the components for the microstimulation module (MS), MEA, and power recovery unit, and functional validation of the prototype. In addition to the custom integrated circuits, low-power, low-cost, and industrial standard commercially available components were used to build this prototype. However,

the individual component reliability does not guarantee reliability of the complete prototype. The complexity of the PCB was increased due to the use of 81 pin BGA package for the FPGA chip. Indeed, the 0.5mm pitch between the connection balls is very small, requiring a PCB with a plurality of layers, a complex routing, and various types of blind and buried inter-layer via. The complicated nature of the designed PCB increased the cost of fabrication, because such a realization is also a challenge for PCB manufacturers that offer such technical facilities. Moreover, establishing various connections between multiple PCBs via ultra-low profile connectors, serial-to-parallel data conversion for generating parallel control signals and delivering them from the FPGA to the MED and stimuli-generator chips, multiplexers, and ADC were extremely cumbersome, where failing to synchronize among the stimulation parameters results in the malfunction of the complete system. In addition to this, gluing the MEA beneath the opening of PCB3 and realizing the wire-bonding between MEA pads and the PCB pads required very sophisticated procedure, which was not easy at all. All these complex techniques lead to multiple debugging steps of the assembled PCBs, each time either a surface mount component was soldered, or a chip die or a MEA was wire-bonded.

CHAPTER 8

CONCLUSION

We summarize our work and results derived from it in this final chapter. Additionally, we enlist the contributions and achievements, provide recommendations to improve the design, and accordingly direct the research toward future directions through next steps to be taken.

8.1 Summary of work

We have formulated the research questions and direction of this work from a biomedical problem perspective, and accordingly, in this thesis, we have proposed a plausible solution to develop a visual intracortical prosthetic device solving different technical challenges related to the field of neurostimulation and microelectronics.

After an introduction to the basic stimulation parameters and visual neurophysiology in Chapter 2, we presented a thorough literature review on microelecronics device based visual prosthetic approaches in Chapter 3. We have raised the research questions from this investigations and presented FES based neurostimulation as a promising therapeutic option. Among different visual prosthesis approaches, intracortical one has been chosen owing to its diversity of treating various types of diseases causing blindness. However, there are many technological hurdles to develop a device for this application and to date, no commercially available or custom designed microstimulator successfully dealt with all the existing technical impediments. Therefore, the questions formulated at the end of Chapter 3, involve the search for a solution to this predicament.

Thus, the general objective described by the end of Chapter 3 has been derived from the formulated research questions, and is to develop a wireless and implantable device dedicated for visual intracortical multichannel microstimulation and monitoring purpose. Indeed, as explained in the literature review in Chapter 3, there are a number of custom built neurostimulators differing in characteristics for this application. Among them, the differences rely on the architecture and specifications of the neurostimulator, location of implantation in the visual pathways, number and types of electrode used for validation, power and data transfer capabilities, mode of stimulations etc.. Although the aforementioned research groups developed some systems solving some technical challenges, yet, their proposed approaches necessarily do not agree with our strategy. Moreover, they ignored some major technical issues, such as (i) the required voltage compliance at the ETI impedance when commer-

cial high-impedance electrodes are used for microstimulation, (ii) the use of various types of energy-efficient pulse patterns in stimulation to save power, and (iii) increasing the rate of data transmission over multichannel.

At this stage, we note that there are two types of development. The first type being the realization of discrete prototypes using only commercially available components, facilitates cost-effective implementation and allows to conduct short-term experiments on animals. But, they prove to be quite bulky, power-hungry and are not implantable on small animals to carry on chronic experiments. Moreover, these devices suffer from limited performance and flexibility. On the other hand, the majority of research groups on neurostimulation are motivated to the on-chip integration approach which allows increasing the number of stimulation channels, reduction in power consumption, miniaturization of the implant, adding additional functionality and chronic implantation. The integrated approach allows either using multiple chips on a single platform or in the extreme case, the neurostimulator can be implemented on a single chip leading to a fully integrated miniature solution requiring only a small number of passive components.

In this context, implementation of the system in a specific integrated circuit, the choice of manufacturing process, and multi-chip implementation need to be justified. On one hand, the cost of manufacture in a given process depends upon its industrial popularity. CMOS manufacturing processes are widely used for example and several generations of technology coexist. The least expensive generations are widely adopted in the consumer industry. On the other hand, these processes operating at low supply voltage are not suitable for easily full integration of a visual intracortical microstimulator which requires high stimulation voltages. There are some designs, demonstrating techniques to interface with high voltages using a low-voltage CMOS technology. But, in the field of neurostimulation, the trend is rather to use a high voltage version of the CMOS manufacturing process for the concerned reliability. A HV CMOS process, therefore, allows full integration of the neurostimulator. But, it would be realistic to implement in low-voltage CMOS process to minimize power and save the silicon area. Therefore, a multi-chip implementation using two CMOS and HV CMOS/DMOS technologies seems technically viable. All low-voltage digital and analog functional blocks can be integrated in CMOS process to minimize power consumption and save the silicon area. Only blocks such as stimulation output-stage, requiring high voltages can be implemented in HV CMOS/DMOS technology, increasing reliability of the system. However, this multi-chip approach also increases the complexity of assembly and miniaturization procedure. In the process of our investigation, some technical matters are still under exploration and remained unsolved. Therefore, the proposed system is more hybrid, combining a partial integration covering the microstimulation back-stage and wireless energy recovery unit; and discrete sys-

tems for the controller and data transmission unit.
In view of aforementioned justification, we have proposed and developed a new visual intracortical microstimulator to overcome the addressed technical limitations. To this end, we made several integrated circuits for the microstimulation subsystem and power recovery unit, which are discussed in Chapters 4-6. The corresponding experimental results validating their functionalities have also been presented. In Chapter 6 we also discussed the discrete system designed for the capacitive-link based transceiver, investigated the crosstalk among the adjacent channels, and provided experimental validation of the data transceiver. The assembly of the various parts along with the MEA, which poses the most challenges, is detailed in Chapter 7 with successful in vitro experimentation. Although, the microstimulator is built using several custom designed integrated chips, a commercial FPGA chip, and some other discrete components, yet, it shows the possibility of full integration through a few passive components such as some capacitors and a single inductor coil.

8.2 Contributions

Our major contributions to develop this new wireless microstimulator are as follows:

- We have conducted in-depth investigations on the energy-efficiencies of various types of stimulation waveform [C5] and based on this analysis, we have designed a low-power and multichannel stimuli-generator, which is implemented with the selected energy-optimum pulse patterns for power-efficient microstimulations. The detail descriptions and experimental validations of the stimuli-generator chip are presented in Chapter 4, and preliminary results are published in [C2], [C3], and [C6]. The experimental results of this chip are also included in the article [J1], which is in preparation (section 8.5).

- We have designed a low-power, 16-channel, and highly configurable output-stage, called MED, to satisfy the need of high-voltage compliance required at the ETI interface, and for multichannel monitoring of ETI voltage; and have evaluated the performance of the MED through experiments. The design procedure and experimental validation are described in Chapter 5, and a number of articles have been published in [J2], [C2], [C3], and [C4] (section 8.5).

- Proposed a new wireless architecture for recovering data and power, combining capacitive and inductive links [C2], [C3] (section 8.5). The capacitive-link based data transceiver has been introduced and implemented to transfer data at 10Mbps as a solution to stimulate hundreds of neural sites in the visual cortex. Both the inductive-link based energy recovery and capacitive-link based data communication systems have

been implemented on to two separate platforms, discussed and validated through experiments, which are presented in Chapter 6. The experimental results of the capacitive link data transceiver have been published in [C1] (section 8.5).

- Assembled the microstimulation module on two stacked HDI PCBs, designed the interface between a novel MEA and the microstimulator, and validated the prototype through in vitro experiments. These are detailed in Chapter 7 and presented in the article [J1] (section 8.5).

8.3 Achievements

Our main accomplishments are listed below and the resulting publications from this research are separately presented before the BIBLIOGRAPHY section.

- Tested and characterized all fabricated micorchips in the Polystim Neurotech test laboratory.
- Conducted in-vitro experiments to characterize the assembled prototype microstimulator and its multichannel stimulation and monitoring capabilities, and verified ETI impedance characterizing the assembled MEA in collaboration.
- Carried out and collaborated experiments to validate the functionality of the capacitive-link based multichannel data transmission unit with sheep skin.
- Performed experiments to substantiate the efficacy of the assembled inductive-link based energy-recovery unit.
- Designed and fabricated two chips in Teledyne DALSA 0.8μm 5V/20V (mid-voltage) CMOS/DMOS process with the fabrication code names ICJPM011 and ICJPMSMX, and tested them:
  - ICJPM011 is the first version of the MED and is able to deliver one stimulation current level simultaneously to sixteen stimulation sites through sixteen electrodes. This chip includes a high-voltage switch-matrix, 3.3V/20V current mirrors, an on-chip 32-bit SIPO register, and FSLCs.
  - ICJPMSMX is the second version of the MED and was upgraded to four input channels. Consequently, this highly-configurable chip is able to deliver four different current amplitudes independently and simultaneously to 16 output channels.

The basic building blocks remaining same, it additionally includes node selection circuitries for ETI voltage monitoring purpose.

- Implemented and fabricated the 4-channel stimuli-generator chip in IBM 0.13μm 1.2V/3.3V CMOS process with the fabrication code name ICGPMSTG. This chip delivers multiple energy-efficient current pulses to the input stage of the second MED.

- ICVPMMON is a high-voltage chip, which includes a rail-to-rail operational amplifier with differential inputs and is configured as an attenuator for monitoring ETI voltage. This chip is implemented in AMS 0.35μm 5V/20V CMOS/DMOS technology. This chip has been validated to be completely functional through testing and measurements, when supplied with up to 11V. But, the chip consumes much higher (about 20mA) than the anticipated current (1mA) when the power supplies are increased to $\pm$10V, which are the nominal supply voltages for the output stage (MED and monitoring unit). Therefore, this integrated version of the monitoring unit has not been assembled in the microstimulation module.

- Designed four HDI PCBs; and assembled ICJPMSMX, ICGPMSTG, ICJPMFMZ [146], MEA [40], and additional discrete components to build the final microstimulator prototype.

- The capacitive-link based data transceiver is designed on a miniature PCB using commercially available discrete components to identify the needed specifications for a multichannel high data-rate ($\geq$10Mbps) transceiver [C1]. Elimination of cross-talks among the channels due to the conductive nature of skin, as mentioned in Chapter 6, still remains challenging. The optimum dimensions of fabricated capacitors (10mm x 10mm), although found to be effective in data transmission, yet, are large from implantation perspective. Therefore, more investigations need to be done to solve these technical issues and accordingly, the design of this block using integrated circuit approach is not justified at this stage.

8.4 Recommendations

To meet the future objectives of departure, this section presents recommendations for the next steps to be taken in the short, medium or long term for the design and validation of an implantable visual intracortical system.
The long term goal of this project is to build an implantable wireless microstimulator and its

functional validation through in vivo experimentation on animals, before implantation in the visual cortex of any human subject. Certainly, there is a long way to go and the recommendations here are listed to accomplish this objective. The microstimulator, we have built, has three separate blocks, which are the microstimulation module (MSM), capacitive-link based data recovery unit, and inductive-link based power recovery unit. So far, we have assembled one MSM prototype and validated through in vitro tests. The PCBs to assemble the MSM were designed to be large for the benefit of functional verification, and as a result of this, the assembled prototype is not suitable for implantation. Therefore, we can begin with the functional improvements and miniaturization of this module. As a first step, the design of the stimuli-generator can be updated so as to obtain full-scale DAC current, which is 220μA in our case, for the nominal supply voltage of 1.2V for the low-voltage analog section. The multiplexers (MUXs) at the output of the stimuli-generator chip are used to select the source and sink current channels. These 3.3V MUXs were not included in the stimuli-generator chip because of limited silicon area dedicated for this IC and can be integrated in the future version of this IC to save area. The efficiencies of the last group of pulses, which have not yet been theoretically verified, are worth to investigate. This can be achieved delivering these pulses on cultured neuron cells and recording the resulting action potentials.

The second step is to upgrade the second MED for increasing number of stimulation channel and integrate the discrete component based monitoring unit. Pads can be inserted at the centre of the chip for flip-chip bonding with the MEA. The 3.3V/20V current mirror or the complete architecture can be redesigned to prevent the additional voltage drop across six high-voltage transistors, while delivering stimulation current. In this context, we need to mention that an integrated version of the ETI voltage monitoring circuit has also been designed and fabricated in AMS 0.35μm CMOS/DMOS process using 5V and 20V transistors. The core component of this chip is a 20V rail-to-rail operational amplifier (opamp) with fully differential inputs. The reference bias generator circuit implemented in the same chip was not connected to the opamp and external pads were added for this purpose. The opamp was designed to function for 1mA bias current from the reference circuit, when supplied with 20V. Experimental validation shows that this current increases to higher than 20mA, which causes the opamp to malfunction for the specified supply. However, the desired performance is achieved, when the supply is reduced to 11V. Investigation shows that the change of the high-voltage guard rings around the 20V transistors from the nominal 50V to 20V causes the latch-up. As a remedy to this problem, we used commercial 20V opamp and 3.3V SAR ADC for the monitoring unit, discussed in Chapter 7.

The central controller can remain be FPGA based, which will ease the debugging while performing functional validation of the stimulator. The advantage is that it is reprogrammable

and allows to update the controller as needed, even after assembly of the device. There are now a variety of options that provide greater flexibility and many advantages in terms of capacity and functionality. However, this option requires the design of a complex PCB to assemble the FPGA chip and to interface it with the other chips. Therefore, another choice is to integrate the controller within the stimuli-generator chip.

Thirdly, the stimuli-generator can be assembled with the MED chip via TSV (through silicon via) process or die-stacking (wire-bonding) technique, and each of such assembled MSM needs to be tested to verify if it meets the desired specifications. But if that does not really provide a significant gain in terms of area and power minimization, flexibility in stimulation, and in general overall performance, then it would be better to implement the entire system in HV CMOS/DMOS process. We recommend to use either Teledyne DALSA 0.8μm or AMS 0.35μm process which are proved to satisfy our high-voltage needs. Alternatively, for greater miniaturization, low-voltage CMOS process would be even more advantageous, if the ETI impedance can be brought down considerably so as to keep the compliance voltage across this impedance within the maximum nominal supply voltage range. For example, IBM 0.13μm CMOS process would be a good choice for a higher density. As for the integration, the MEA has to be assembled via flip-chip bonding to the MED pads, followed by the encapsulation of the complete MSM.

The fourth step is to perform in-vitro experimentations with several encapsulated MSM. Satisfactory performance from these tests will lead to in vivo experiments on animal subjects.

Concerning the wireless power recovery, all the components used to design this unit as mentioned earlier in Chapter 6, can be integrated in a single chip except the coil and tuning capacitor. The good choice is to dedicate one power recovery unit for multiple MSM to save area and power. A power management unit (PMU) is required, in this case, to optimize power consumptions during idle, power-up, and stimulation periods. This PMU will also be responsible to control the power of the implanted data receiver. Power can be optimized globally using an adaptive inductive power recovery module, which could be implemented in order to switch from one approach to another depending on the operation of the system conditions. Thus, this module could not only be used in variable operating conditions, but also be in several applications. This will also improve the energy efficiency of the entire neurostimulation system.

A number of steps can be undertaken to improve the design and functionality of the data transceiver. On one hand, the 10mm x 10mm area of the capacitor plates, although found to be the most effective in our case to transmit data, yet, is quite large and not implantable. On the other hand, miniaturization of these plates allows higher density which would increase the data-rate, but would also degrade the signal quality as the SNR drops. For bidirec-

tional communication, low-noise-amplifiers (LNAs) can be used on both sides of the plates to amplify the received weak signals cancelling the background noise. This approach seems interesting and it is worth to investigate the feasibility of its implementation. Noise cancellation techniques can be studied and the one suitable for the transdermal data communication needs to be implemented for cancelling cross-talks. The integrated approach can be followed for miniaturization of this unit and a single multichannel data transceiver can be assigned to control several MSM.

The monitored stimulation signals, digitized by the ADC, can be send to the internal controller for power management and to the external controller for updating the stimulation parameters, which will allow closed-loop control of the global system.

Finally, we would say, through this research, we intend to contribute to further improvements in the energy efficiency and the miniaturization of wireless and implantable neurostimulators. We also wish to contribute to the improvement of intracortical and in general, other prosthetic options based on neurostimulation for the partial restoration of visual functions of blind individuals.

To date, most of microelectronic based neural prosthetic devices are designed either with only microstimulation or bio-signal acquisition (recording) capability. Recently, a new generation of prosthetic device, featured with both microstimulation and recording functionalities on the same platform to perform closed-loop operation, is emerging [170]. Design of such a device for intracortical visual prosthesis is becoming a necessity, and would allow reliable and efficient treatment method. We initiated to design such a device towards the end of this program, but this extended work was found to be beyond the scope of this project as the remaining work of the microstimulator (assembly) had to be completed within the time limit of this program. Therefore, a very interesting future direction on this work can be the realization of a novel microstimulator-recording system with the ability to perform microstimulation and bio-signal acquisition tasks simultaneously, analyze the recorded data, and provide feedback to the stimulator on the basis of the analyses using closed-loop control principle.

8.5 Publications[1]

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[J2] M. Hasanuzzaman, R. Raut, and M. Sawan, “High-voltage compliant microelectrode

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APPENDIX A

THEORIES AND ANALYTICAL EQUATIONS FOR THE DESIGNED CIRCUITS

A.1 3.3V/20V current mirror used in the MEDs (Chapter 5)

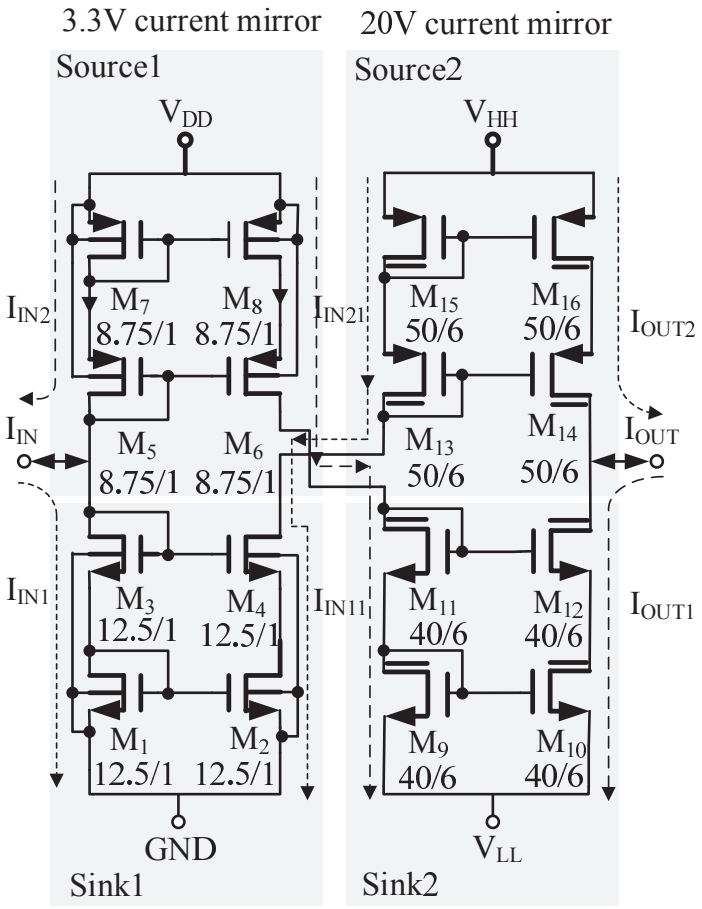


Figure A.1 3.3V/20V current mirror circuit designed using 5V transistors, M_1-M_8 and double-side (source and drain) extended 20V transistors, M_9-M_{16}. The units for the dimensions of all transistors are μm / μm.

The transistors in the low-voltage (3.3V) double cascode current mirror, presented in Figure A.1, follow the characteristics of long channel MOSET transistor. In saturation region

(when $V_{DS} \geq V_{GS}$ - V_{th}), the drain current of M_1 to M_4 can be expressed as [120], [121]

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}) \tag{A.1}$$

For the p-channel transistors, M_5 to M_8, the above equation can be rewritten as

$$I_{SD} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p (V_{SG} - |V_{th}|)^2 (1 + \lambda V_{SD}) \tag{A.2}$$

where, μ_0 is the surface mobility of the channel, $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ is the gate oxide capacitance density, W is effective channel width, L is the effective channel length, V_{th} is the threshold voltage, and λ is the channel length modulation parameter. The relation between the branch currents I_{IN1} and I_{IN11} of sink current mirror1 can be expressed by the following equations [120], [121]

$$\begin{aligned} \frac{I_{IN1}}{I_{IN11}} &\approx \frac{(W/L)_1}{(W/L)_2} \\ &\approx \frac{(W/L)_3}{(W/L)_4} \end{aligned}$$

Again, the ratio of I_{IN2} to I_{IN21} of source current mirror1 can be expressed according to the following equations [120], [121]

$$\begin{aligned} \frac{I_{IN2}}{I_{IN21}} &\approx \frac{(W/L)_5}{(W/L)_6} \\ &\approx \frac{(W/L)_7}{(W/L)_8} \end{aligned}$$

The 20V high-voltage transistors used to design the output stage of the current mirror, shown in Figure A.1, are basically DMOS (double diffuse MOSFET) [129], [130], [131], more specifically LDMOS (lateral double diffuse MOSFET) in our case, and they do not follow the same characteristics as of low-voltage MOSFET transistors. The electrical equivalent circuit of an LDMOS consists of more than one simple MOS transistor.

On the basis of V_K concept, the EKV compact modeling of DMOS long channel transistors expresses the normalized drain current in the saturation region [131], which is

$$I_{Dsat} = I_0\left(\left(\frac{V_p}{2U_t}\right)^2 + \left(\frac{V_p}{2U_t}\right)\right) \tag{A.3}$$

where, I_0 is the EKV *specific current* and expressed as

$$I_0 = 2n(V_p)C_{ox}\mu_0(U_t)^2\frac{W}{L_{CH}} \tag{A.4}$$

and, V_p is the EKV $pinch - off$ *voltage*, which is defined as follows

$$V_p = \frac{V_G - V_T}{n(V_p)} \tag{A.5}$$

The mathematical relations between $\mathrm{I_{IN11}}$ and $\mathrm{I_{OUT2}}$, and $\mathrm{I_{IN21}}$ and $\mathrm{I_{OUT1}}$, can be described as [120], [121]

$$\begin{aligned}\frac{\mathrm{I_{IN11}}}{\mathrm{I_{OUT2}}} &\approx \frac{(\mathrm{W/L})_{13}}{(\mathrm{W/L})_{14}} \\ &\approx \frac{(\mathrm{W/L})_{15}}{(\mathrm{W/L})_{16}}\end{aligned}$$

$$\begin{aligned}\frac{\mathrm{I_{IN21}}}{\mathrm{I_{OUT1}}} &\approx \frac{(\mathrm{W/L})_{9}}{(\mathrm{W/L})_{10}} \\ &\approx \frac{(\mathrm{W/L})_{11}}{(\mathrm{W/L})_{12}}\end{aligned}$$

A.2 Theories related to the inductive link (Chapter 6)

The elements of an inductive link enabling the transmission and recovery of energy are presented in Figure A.2. The AC carrier signal for power transmission is generated by an oscillator. This signal is amplified by the power amplifier and the current circulating in an external coil (primary) induces a magnetic field, which is captured by the inner coil (secondary). The tuning filter (a parallel LC circuit) selects the carrier frequency and the induced AC voltage is then converted to constant voltage (DC) by a rectifier. This voltage is stabilized by the regulators, which in turn generate different constant voltage (DC) levels required by the implant. We need to mention that it is essential to avoid any momentary drop in supply DC voltage. Indeed, such a fall can lead to a decrease in stimulation current for one of the stimulation phases and may result in a damage to the stimulated tissue.
Ideally, the inner and outer coils are each connected to at least one capacitive element, and their values are set in a way that their respective resonance frequencies are identical and match that of the the magnetic field carrier wave (f_{Carr}). In accordance with the generic

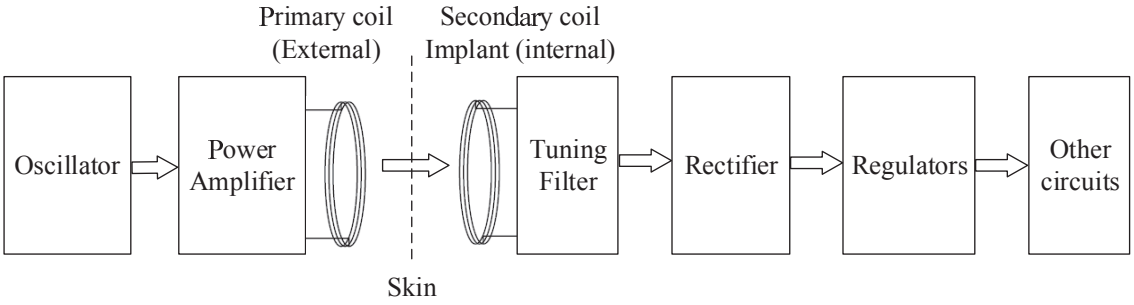


Figure A.2 The basic elements of an inductive link energy transmission and recovery for implantable biomedical devices.

model of an inductive link as presented in Figure A.3,

$$w_0 = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}} = 2\pi f_{Carr} \tag{A.6}$$

Note that, in the model, R_1 represents the parasitic resistance in primary side and in the

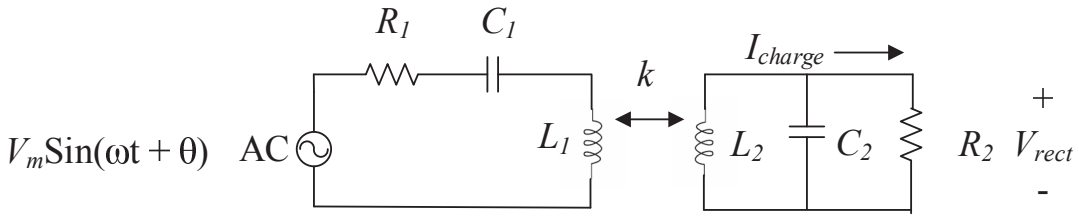


Figure A.3 The generic model of a transcutaneous inductive link for energy transmission.

secondary side, R_2 is the load or the equivalent input impedance of the implant experienced by the rectifier voltage. If the total current consumed by the implant is I_{charge}, then $R_2 = (V_{rect} \ / \ I_{charge})$.

From [171], we know that the gain of the transfer function of such a link at the resonance frequency and considering ${R_2}^2{C_2}^2 \gg L_2 C_2$

$$\frac{V_{rect}}{V_m} = k\sqrt{\frac{C_1}{C_2}}\left(\frac{R_1 C_1}{R_2 C_2} + k^2\right)^{-1} \tag{A.7}$$

Where, k is the coupling coefficient between the antennas, which is determined by their physical characteristics, material, geometry, distance between them, and relative orientation. The gain $\frac{V_{rect}}{V_m}$ is maximum when the coupling is said critical, which is

$$k = k_{crit} = \sqrt{\frac{R_1 C_1}{R_2 C_2}} \tag{A.8}$$

The overall efficiency of the system (η) is largely determined by the efficiency of the power amplifier. Usually, a class E amplifier is used. This choice is especially justified considering the very high energy efficiency (theoretically 100%). Also, the Vrect - Vdc voltage drop, contributes to a significant deterioration of the efficiency. Practically, the efficiency is usually in the range of 10% to 30%, with a maximum theoretical value of 50% [172].

APPENDIX B

ICJPM011 AND ICJPMSMX: THE MED CHIPS

The schematic and layout views of the MED chips designed in Teledyne DALSA 0.8μm CMOS/DMOS technology are presented below:

B.1 Layout view of the chips ICJPM011 and ICJPMSMX

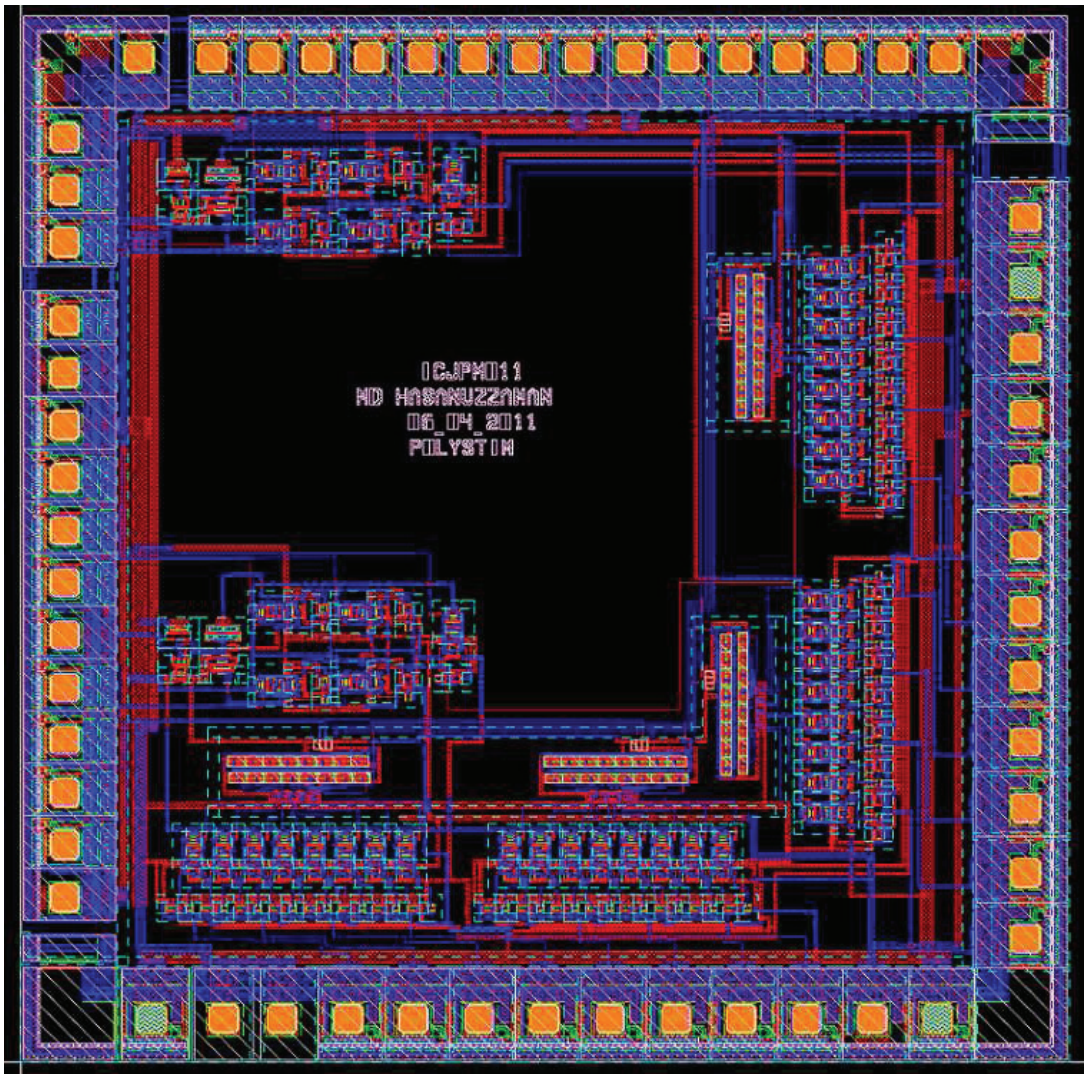


Figure B.1 The layout view of the first MED, ICJPM011, designed in Teledyne DALSA 0.8μm CMOS/DMOS technology.

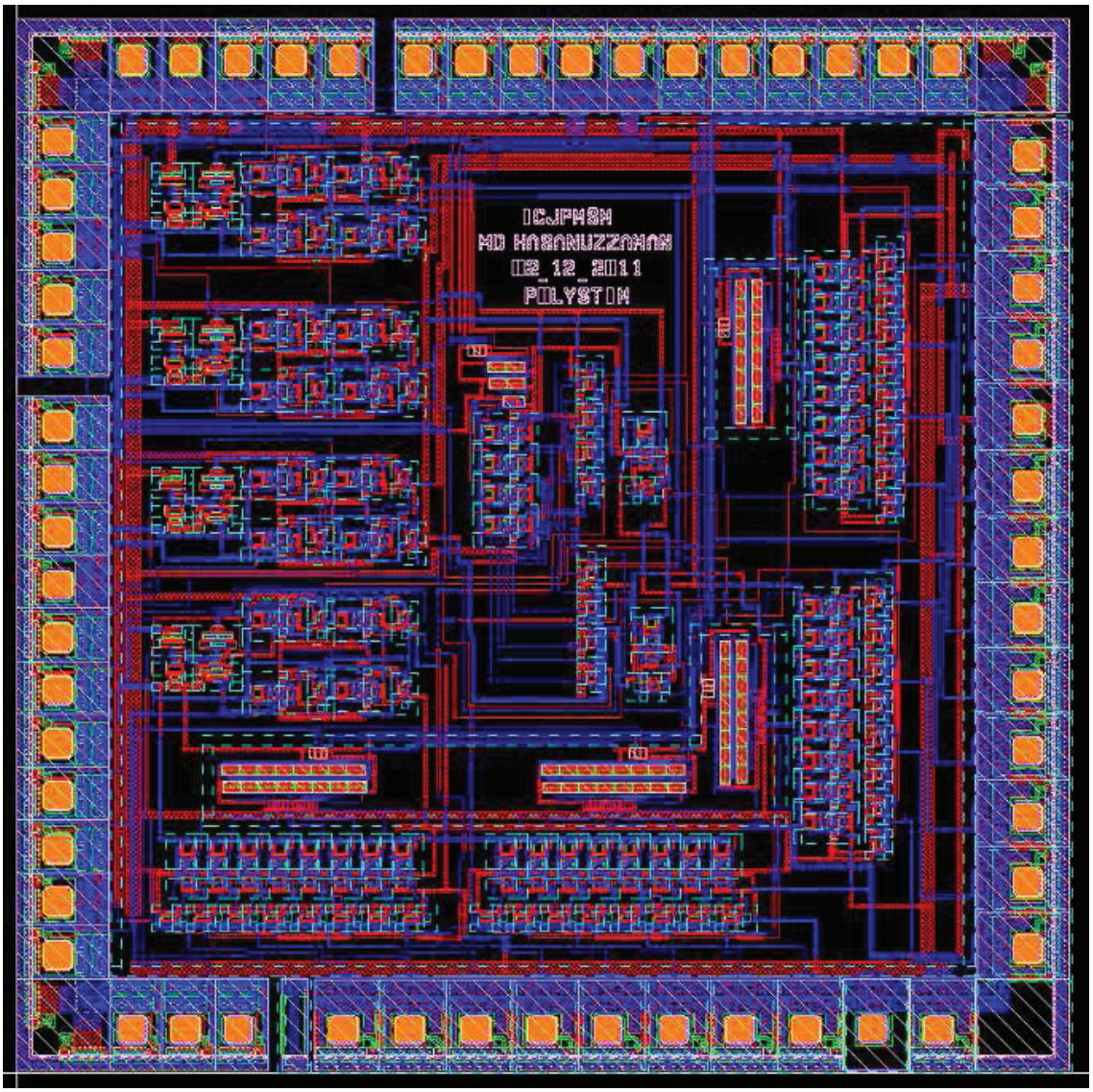


Figure B.2 The layout view of the second MED, ICJPMSMX, designed in Teledyne DALSA 0.8μm CMOS/DMOS technology.

B.2 Design level (ICJPM011 and ICJPMSMX)

B.2.1 3.3V/20V current mirror

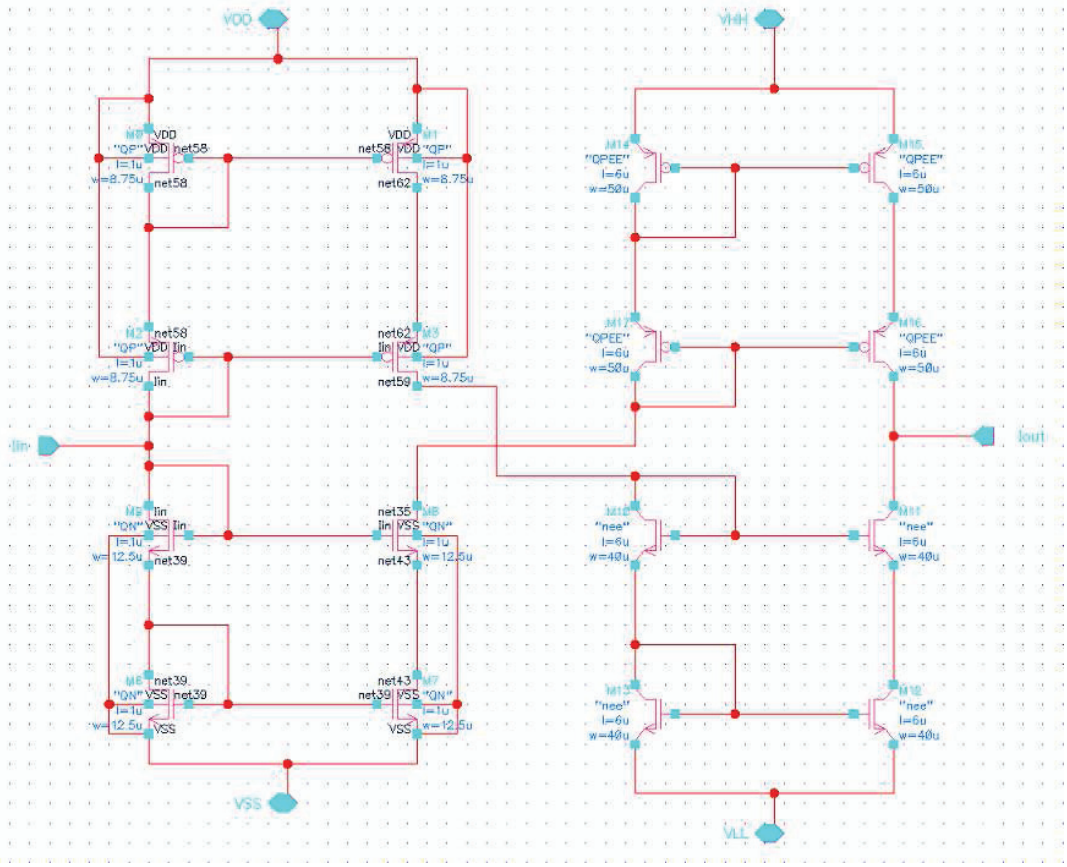


Figure B.3 The schematic diagram of the 3.3V/20V current mirror.

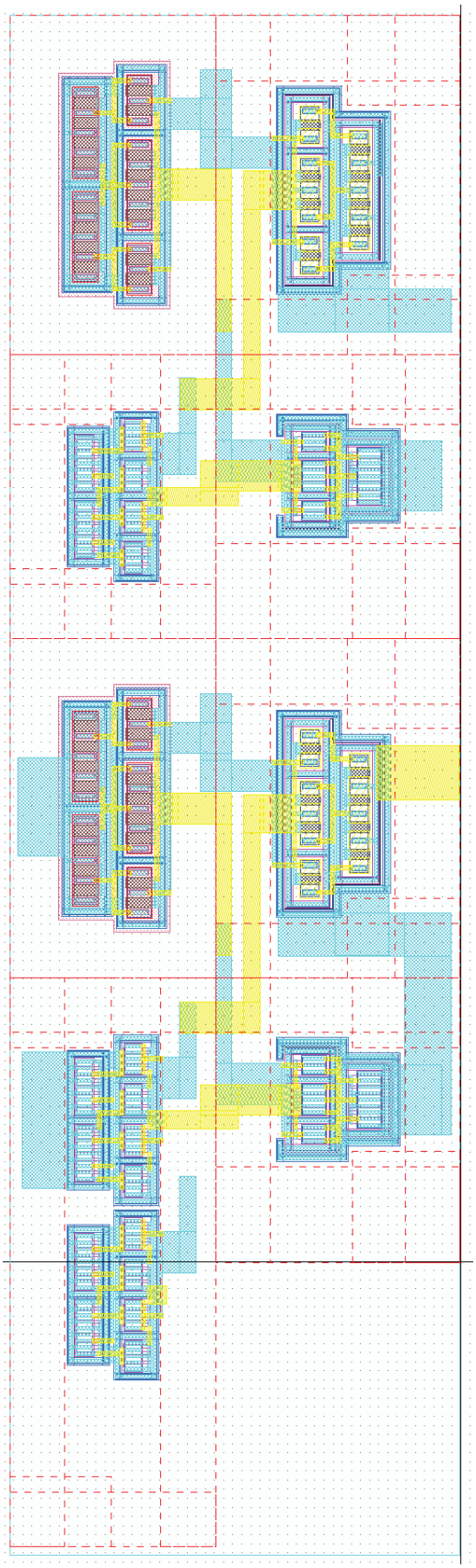


Figure B.4 The layout view of the 3.3V/20V current mirror.

B.2.2 3.3V/20V high-voltage level-shifter

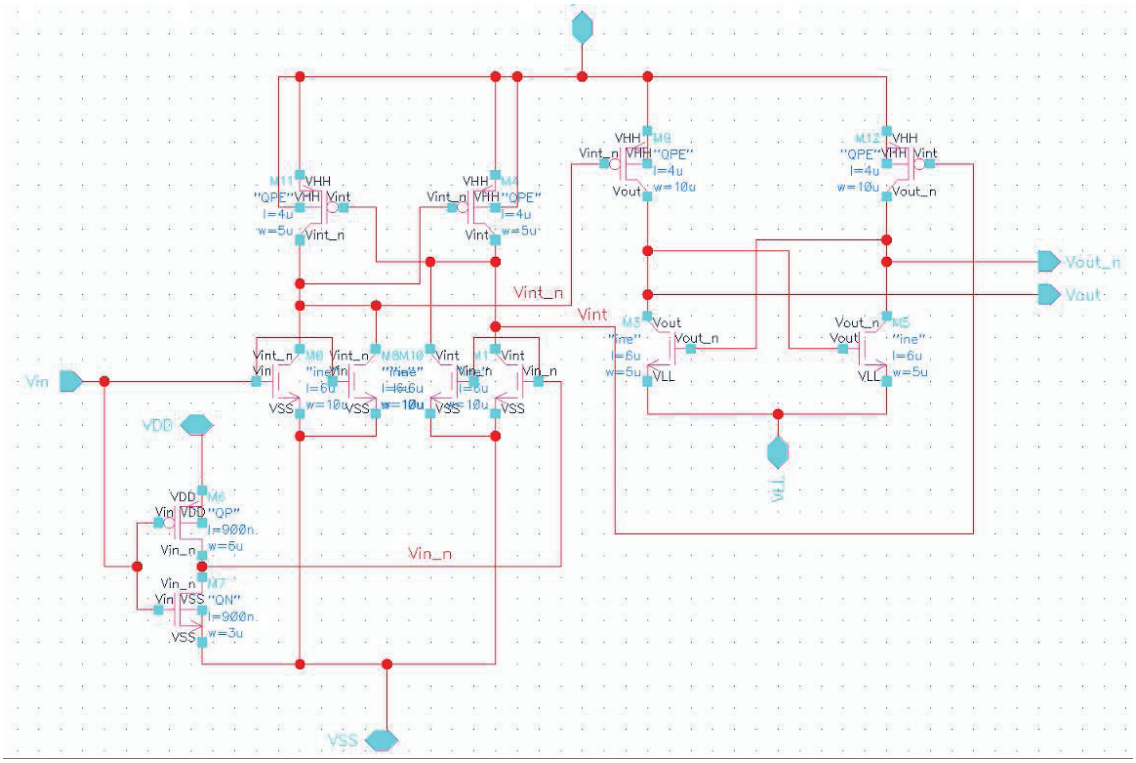


Figure B.5 The transistor level circuit diagram of the 3.3V/20V high-voltage level-shifter.

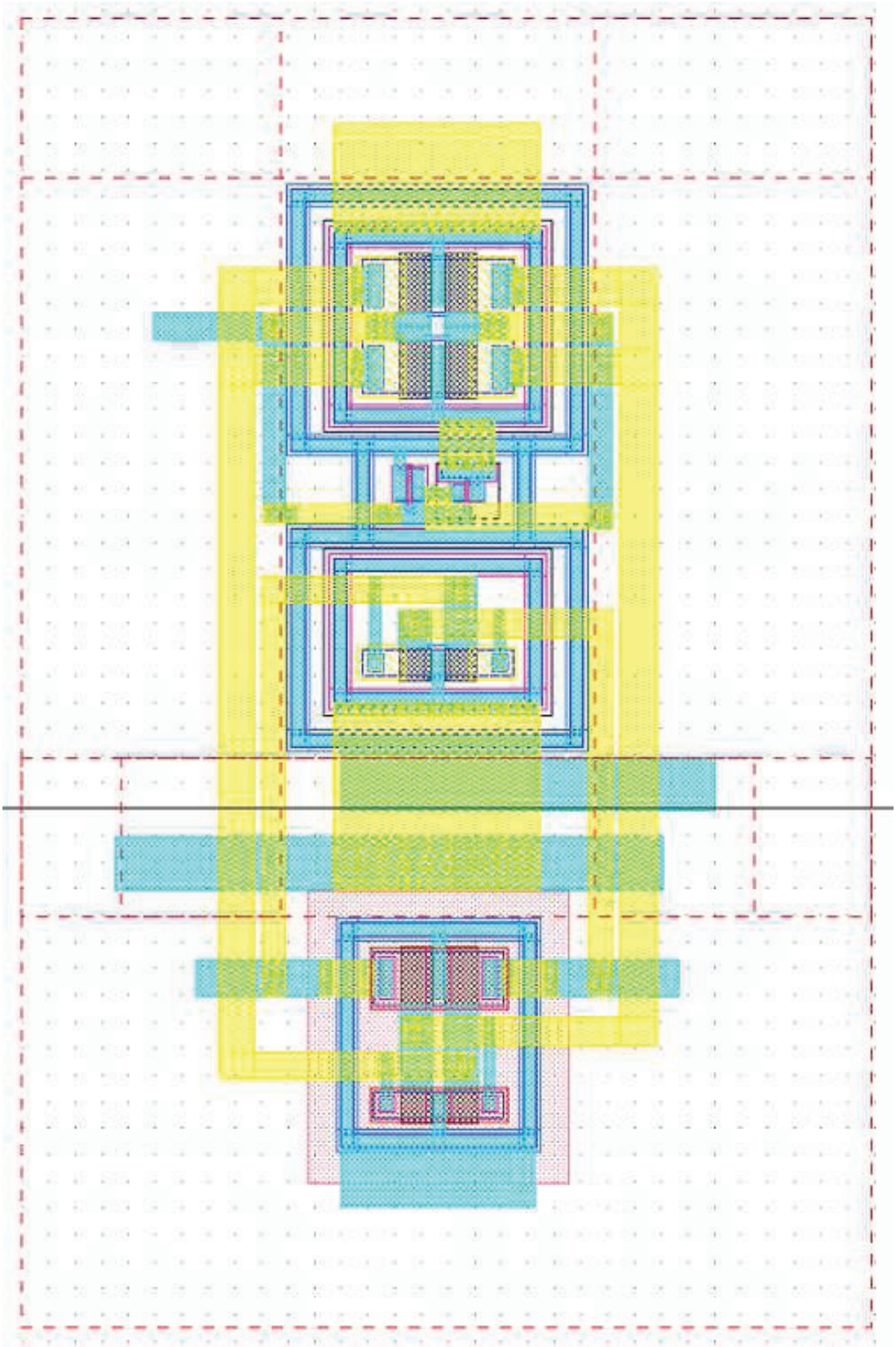


Figure B.6 The layout view of the 3.3V/20V high-voltage level-shifter.

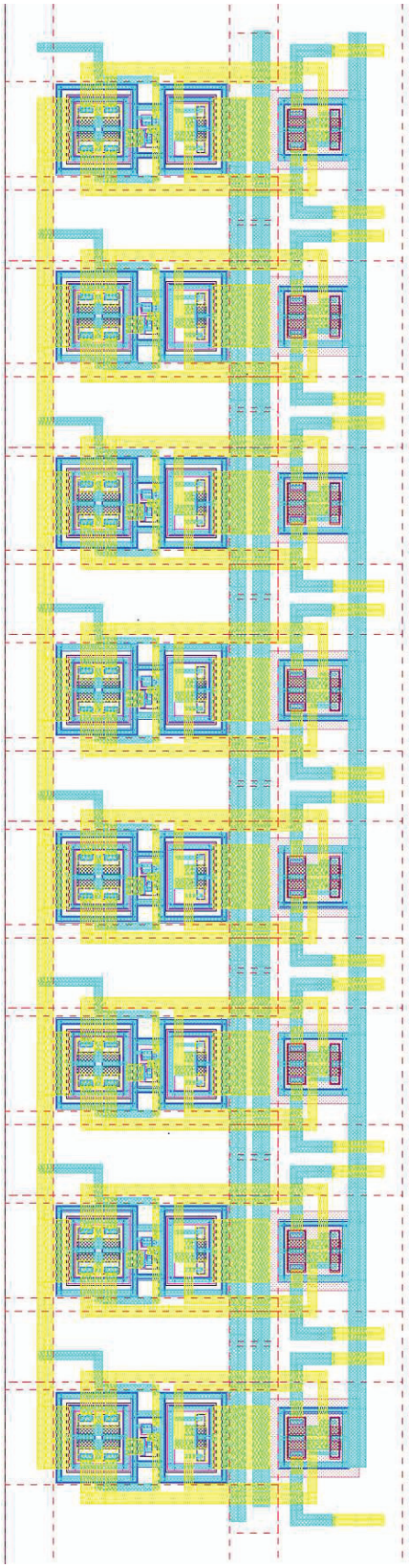


Figure B.7 The layout view of the block of eight high-voltage level-shifters.

B.2.3 8-bit low-voltage (3.3V) register

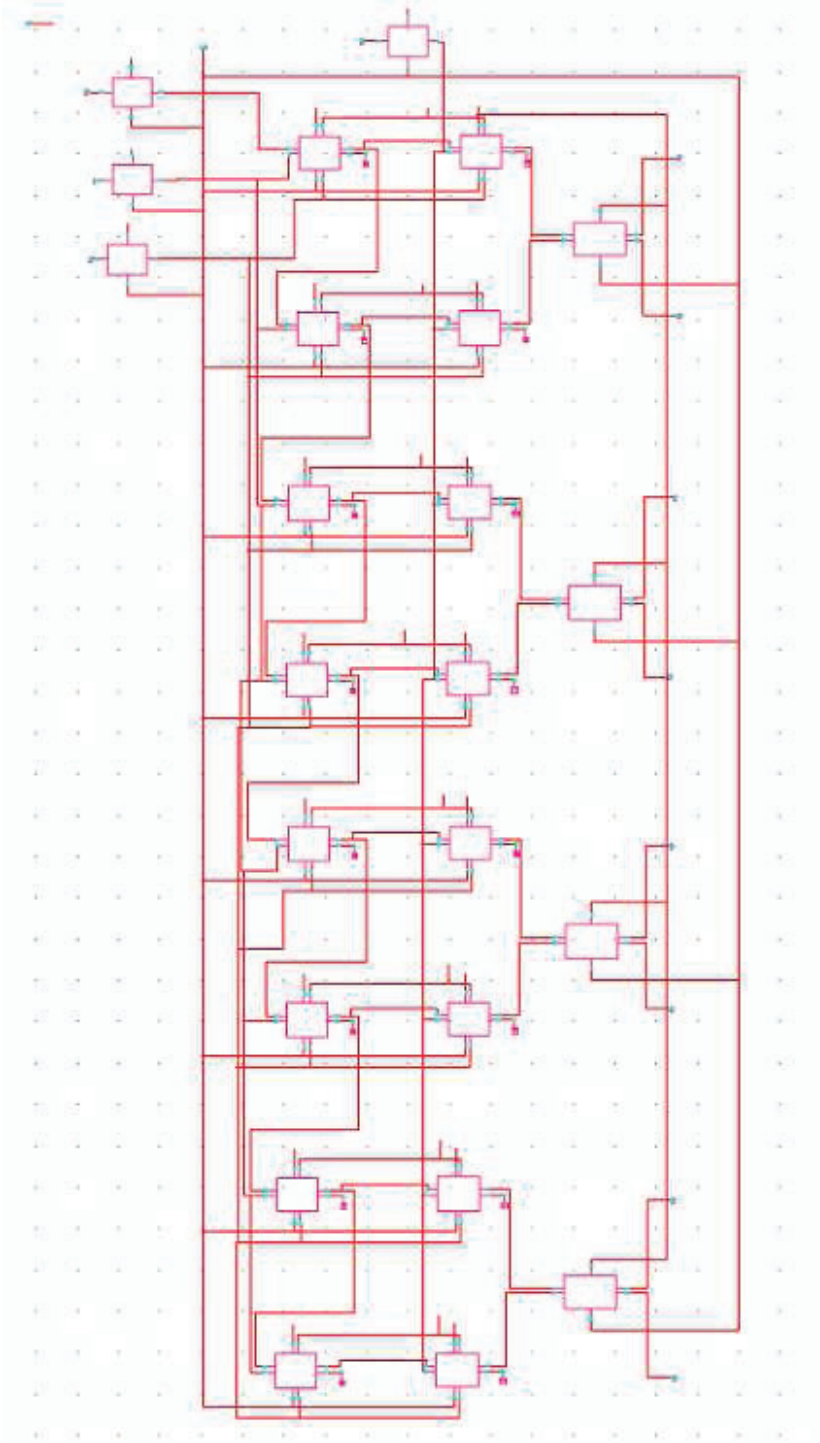


Figure B.8 The schematic diagram of the 8-bit low-voltage register.

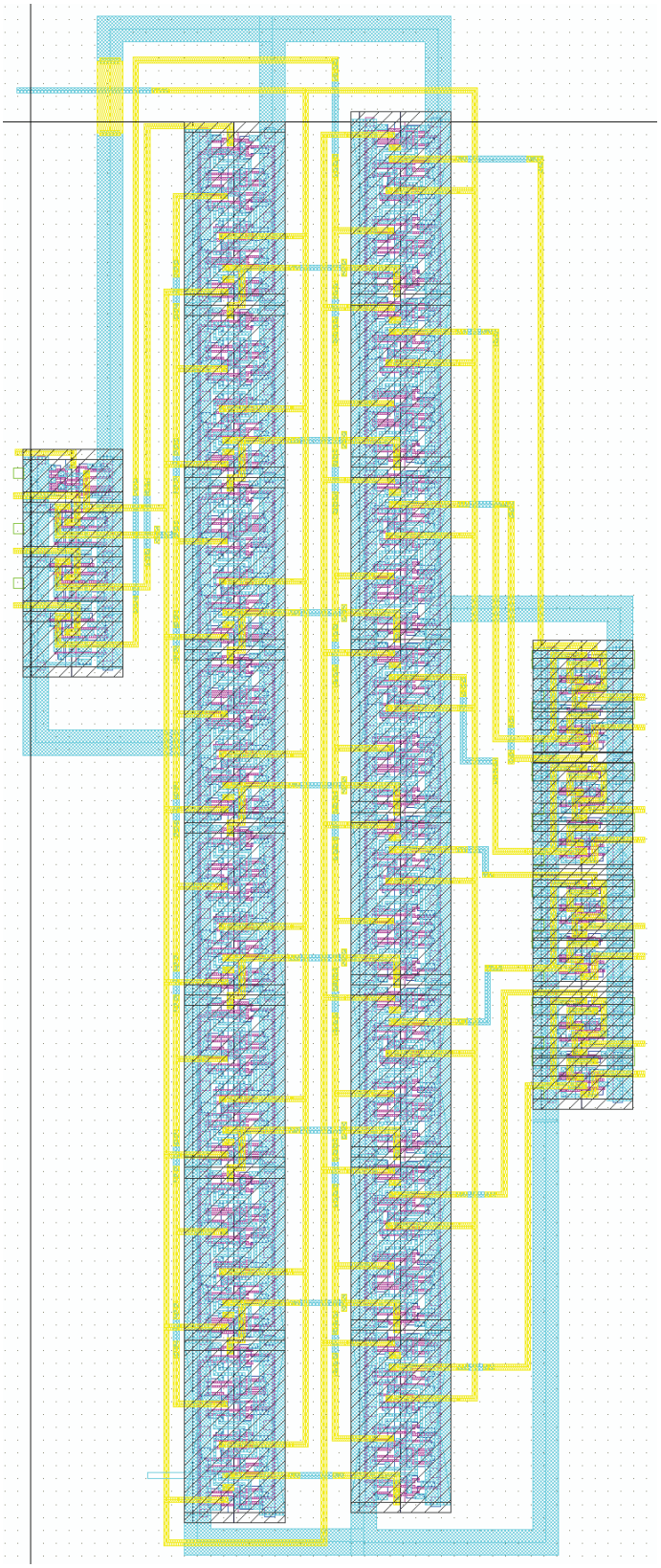
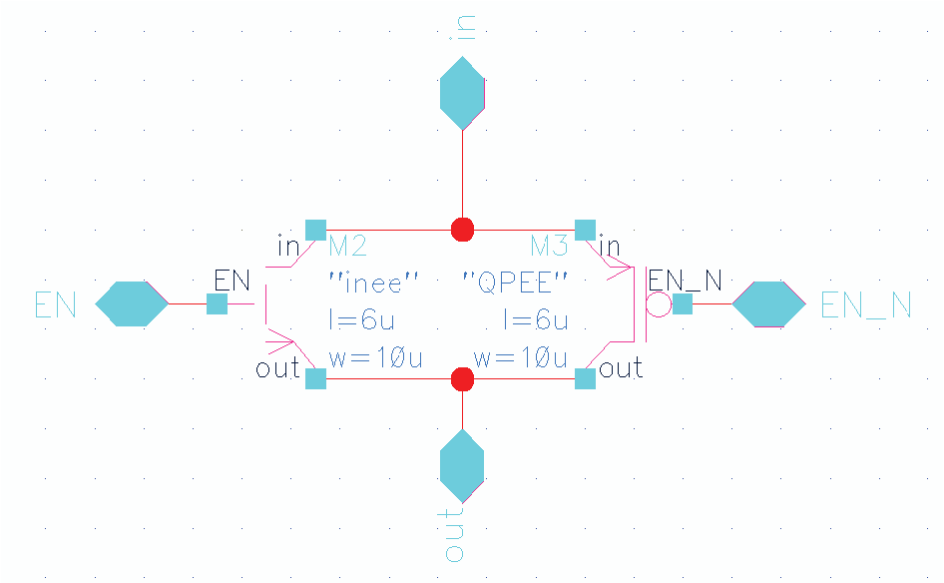
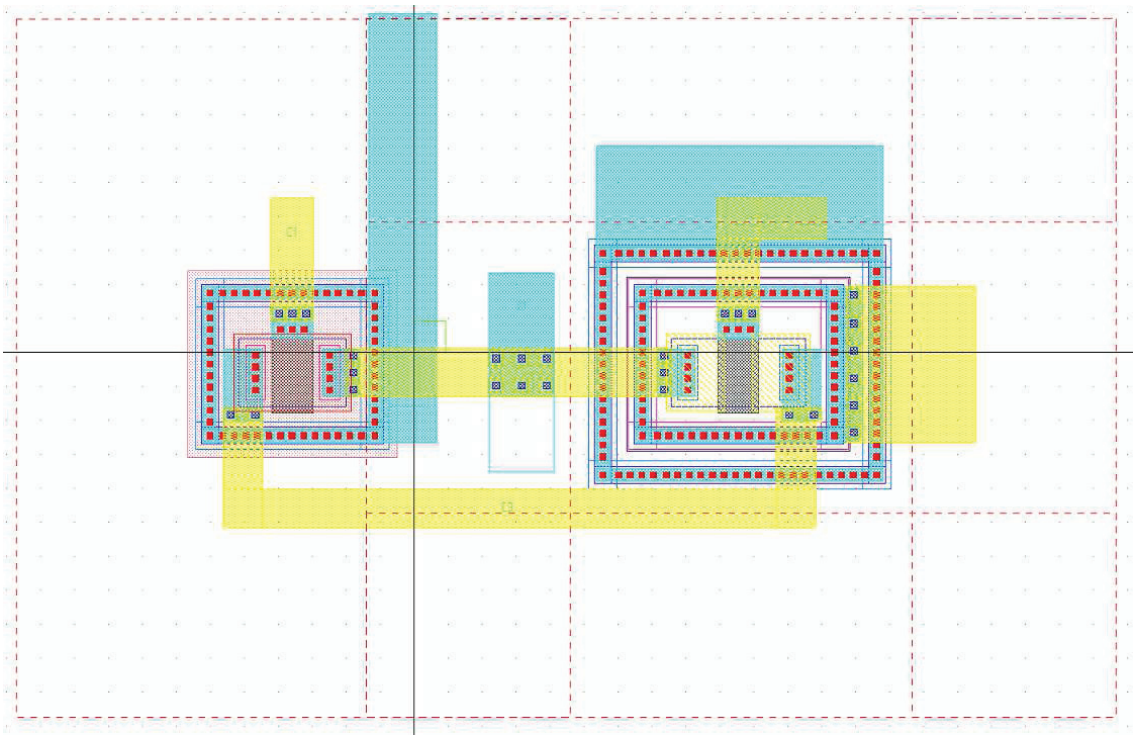


Figure B.9 The layout view of the 8-bit low-voltage register.

B.2.4 Transmission gate based high-voltage switch



(a)



(b)

Figure B.10 (a) Transistor level schematic diagram of a high-voltage switch and (b) layout view of the switch.

APPENDIX C

ICGPMSTG: THE STIMULI-GENERATOR CHIP

The schematic and layout views of the stimuli-generator chip designed in IBM 0.13μm CMOS technology are presented below:

C.1 The schematic and layout views of the chip ICGPMSTG

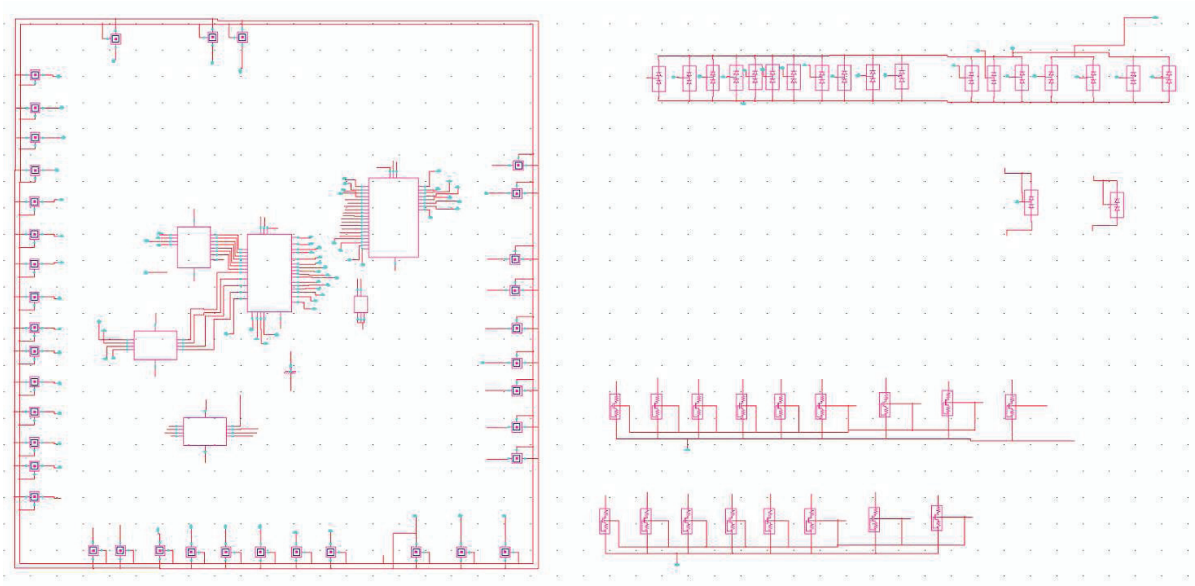


Figure C.1 The schematic view of the stimuli-generator chip, ICGPMSTG, designed in IBM 0.13μm CMOS technology.

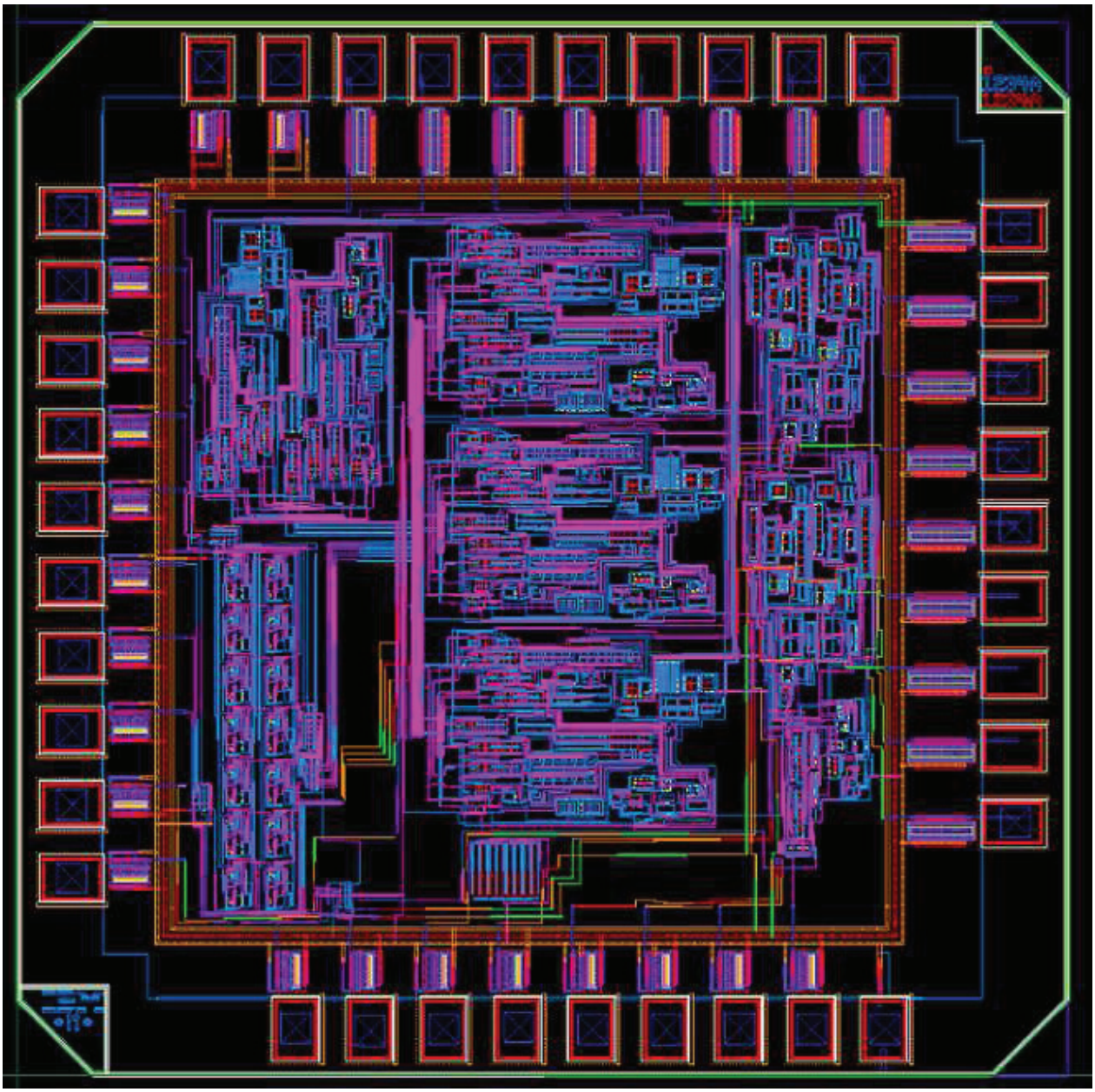


Figure C.2 The layout view of the stimuli-generator chip, ICGPMSTG, designed in IBM 0.13μm CMOS technology.

C.2 Design level (ICGPMSTG)

C.2.1 Source and sink DACs

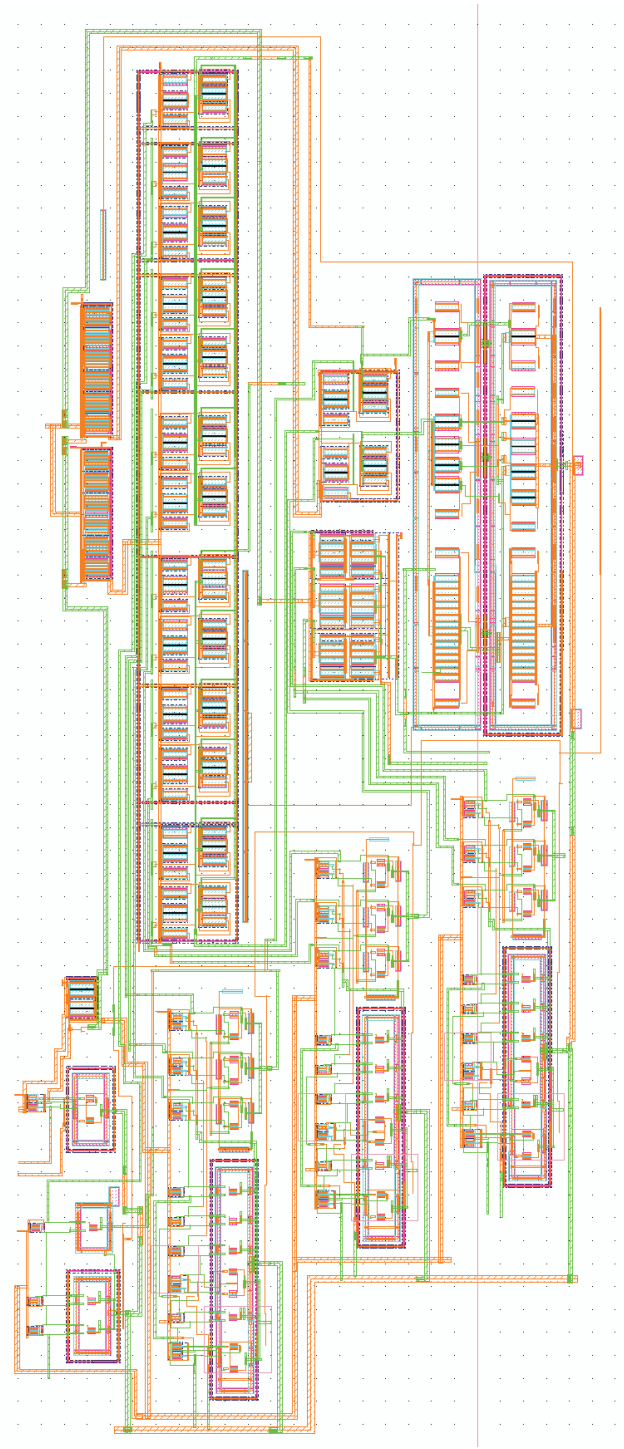


Figure C.3 The layout view of the source DAC.

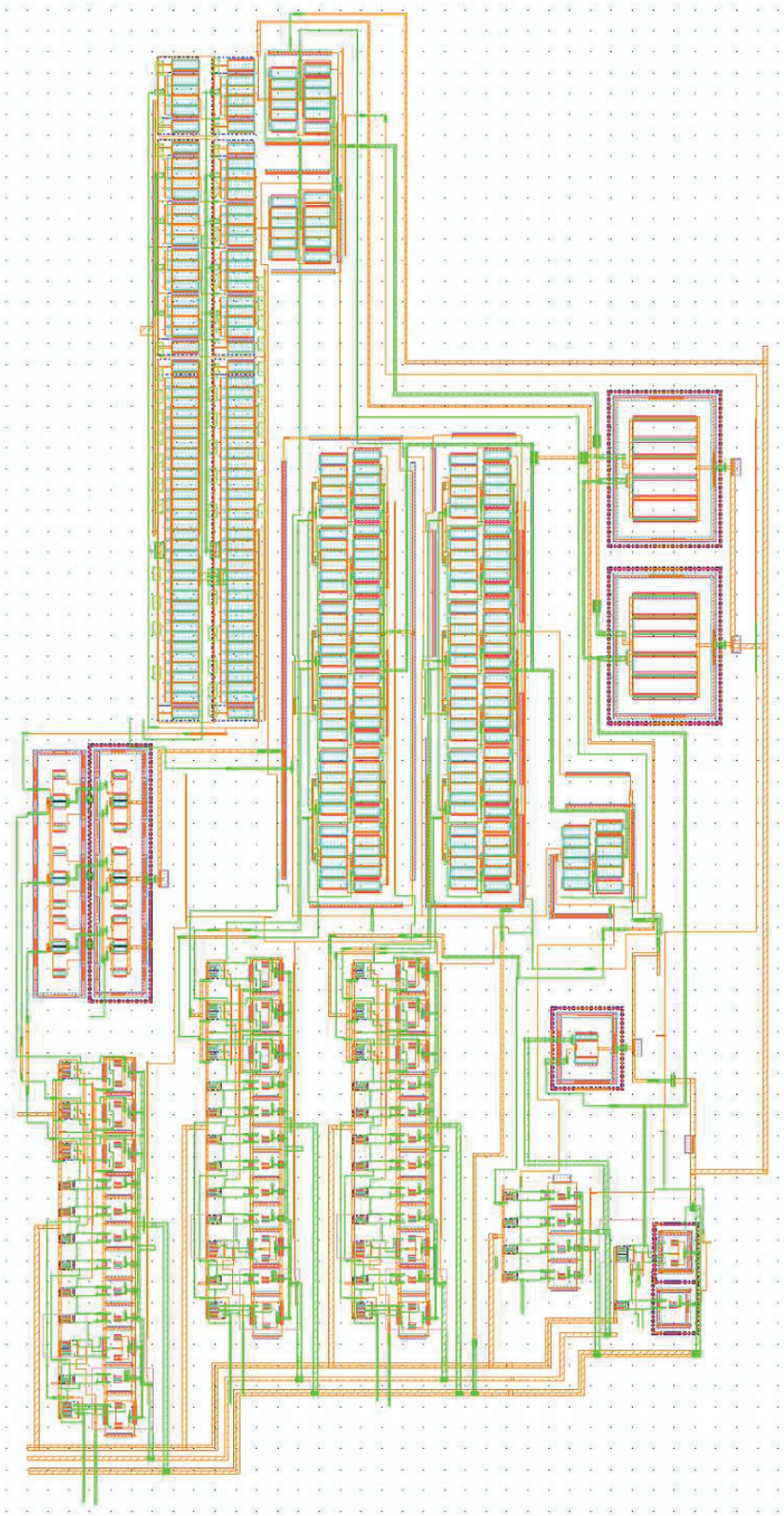


Figure C.4 The layout view of the sink DAC.

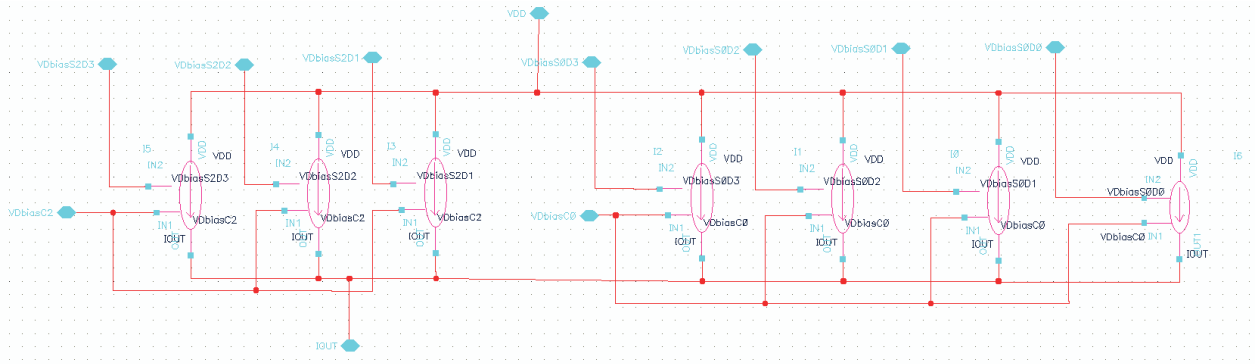


Figure C.5 The schematic view of current sources in the source DAC.

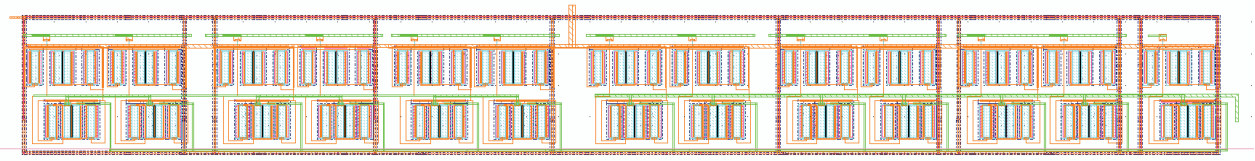


Figure C.6 The layout view of current sources in the source DAC.

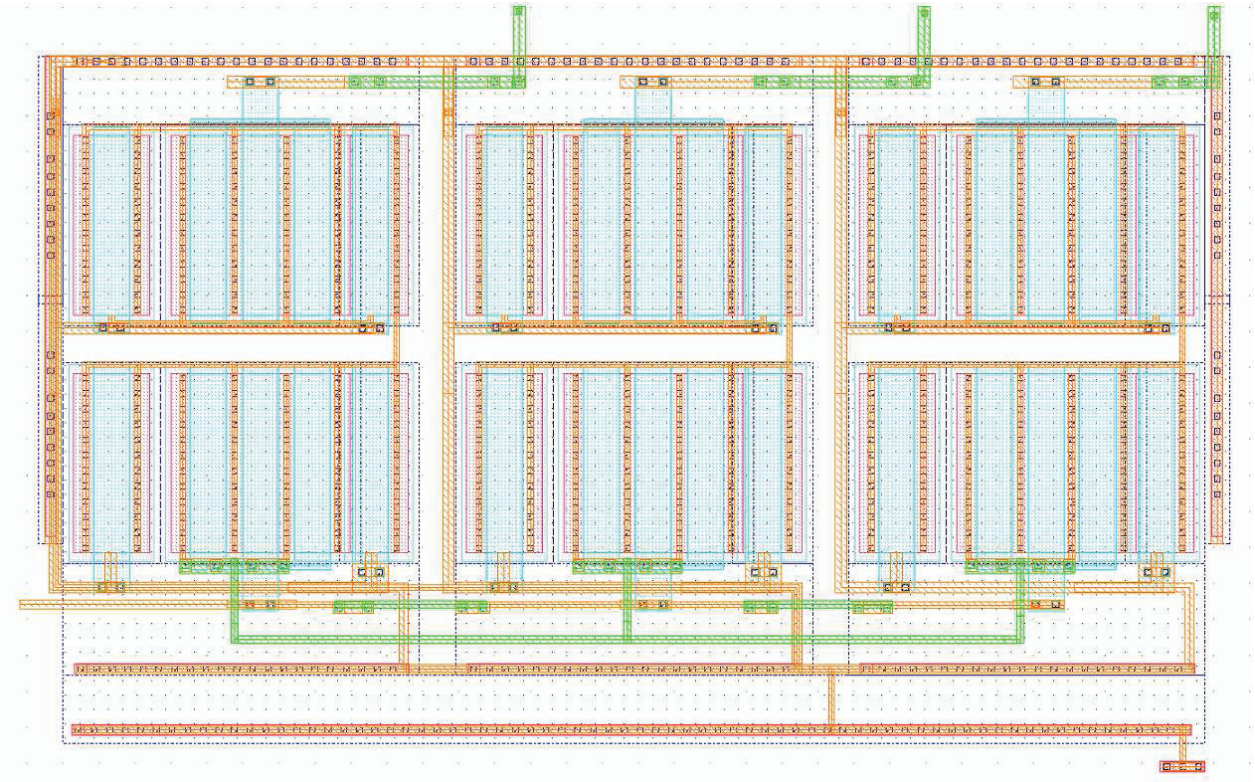


Figure C.7 The layout view of current sources defining the range of source DAC.

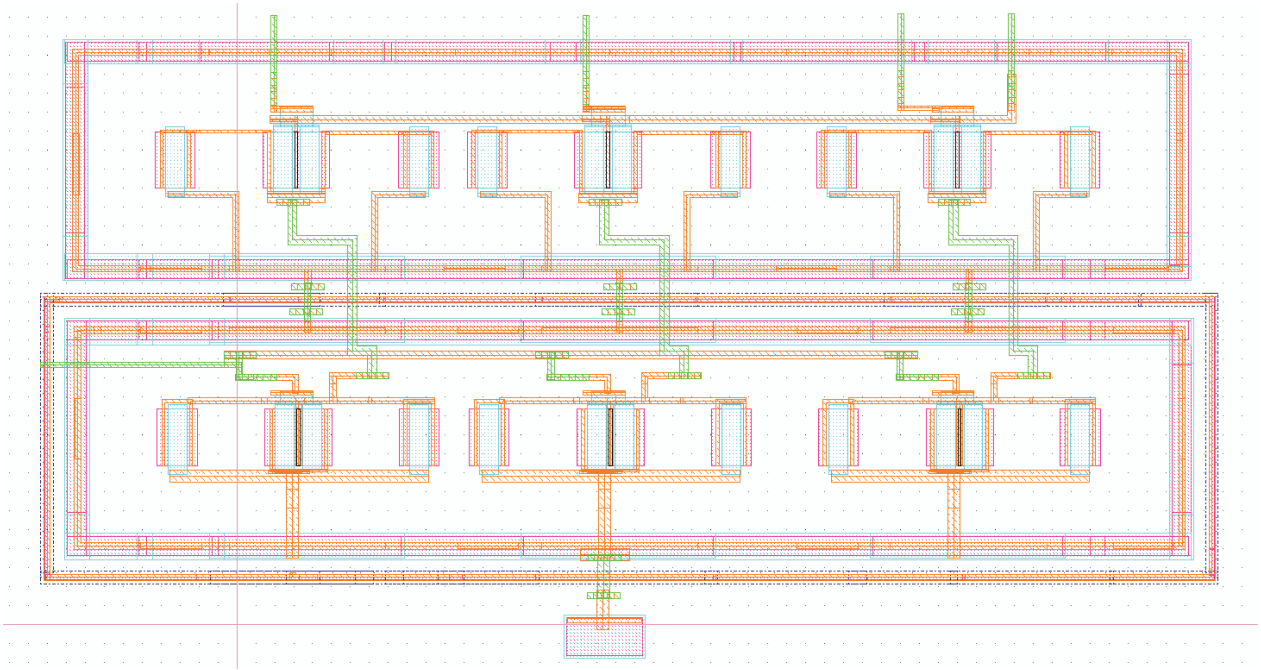


Figure C.8 The layout view of current sources defining the range of sink DAC.

C.2.2 Thermometer decoder

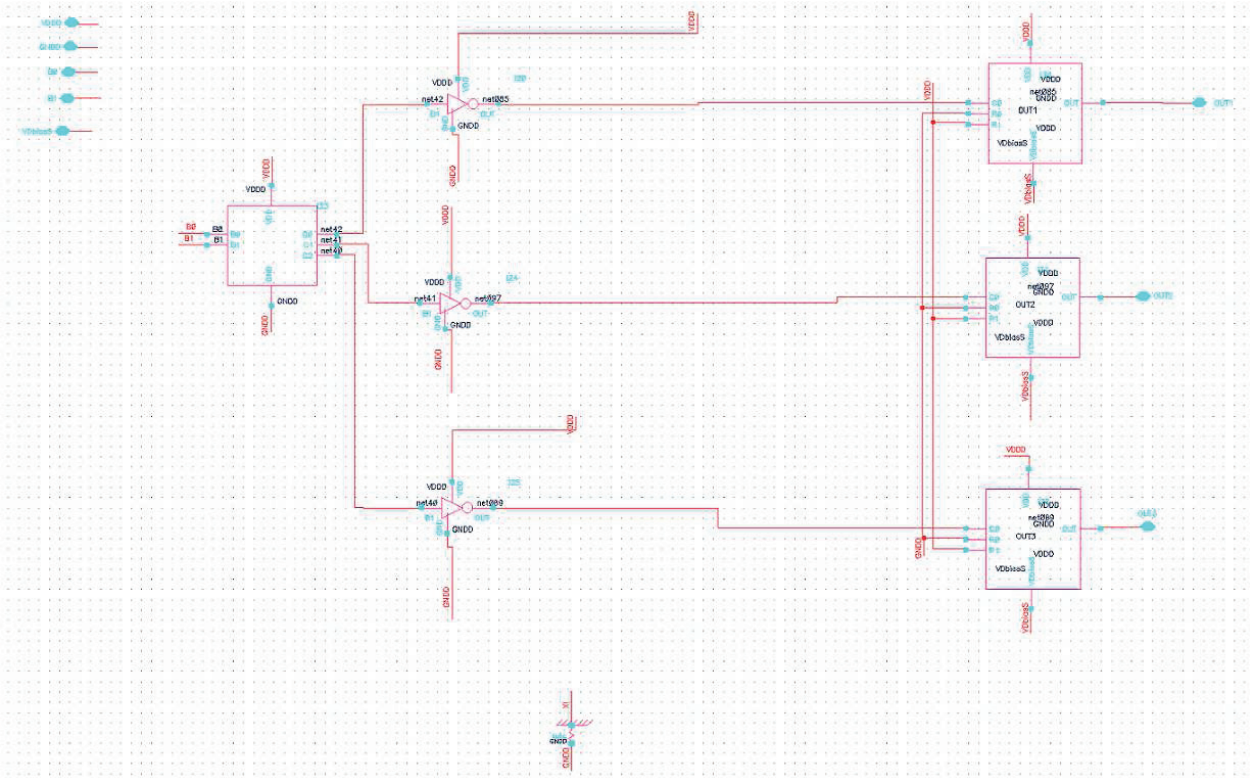


Figure C.9 The schematic diagram of the thermometer decoder.

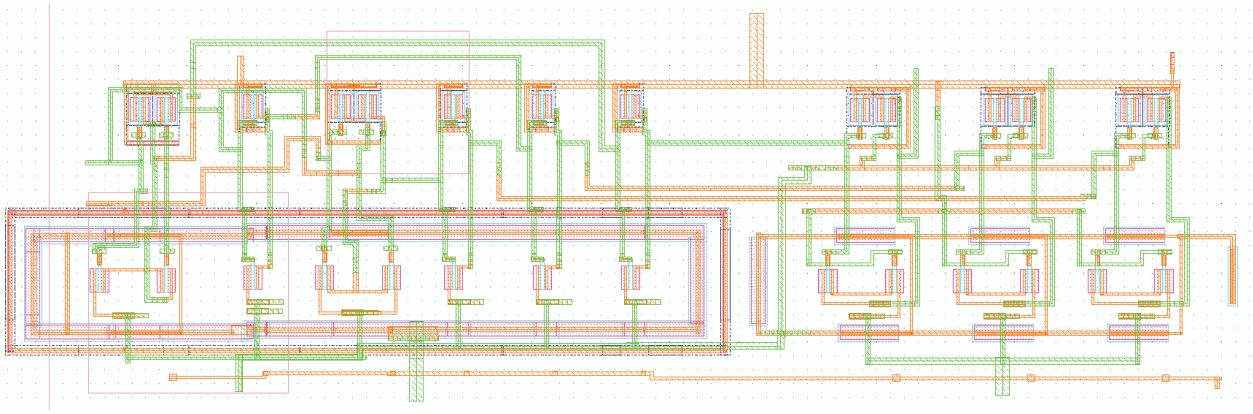


Figure C.10 The layout view of the thermometer decoder.

C.2.3 Reference voltage and current generator

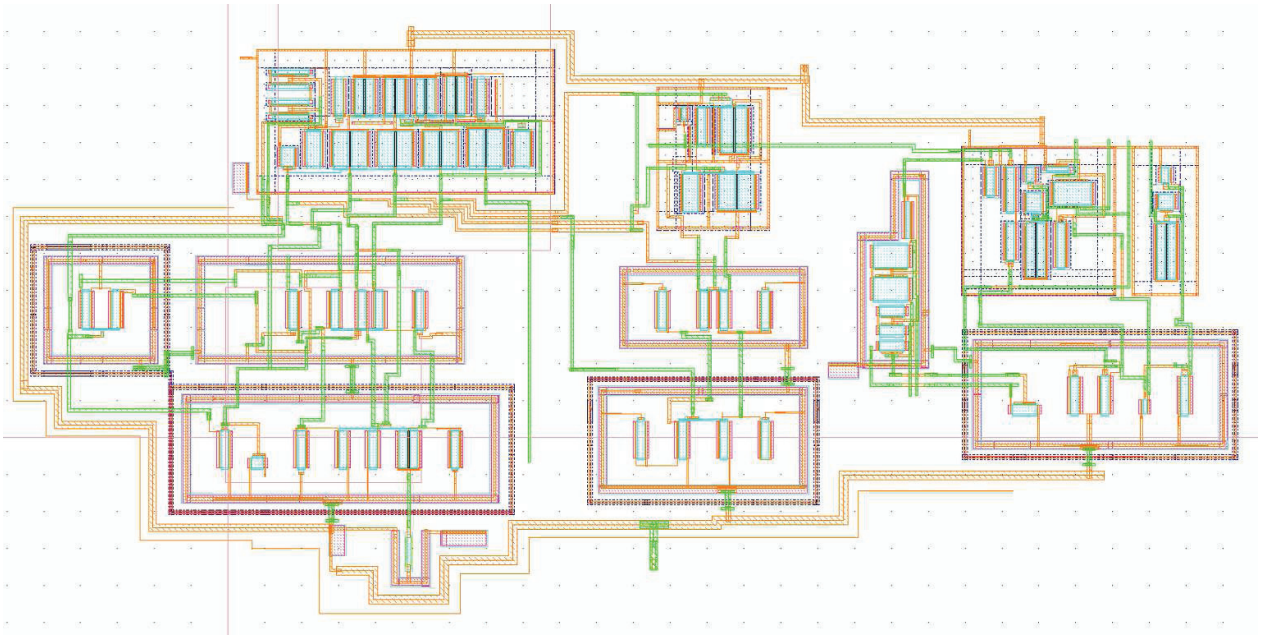


Figure C.11 The layout view of the reference circuit for the DAC.

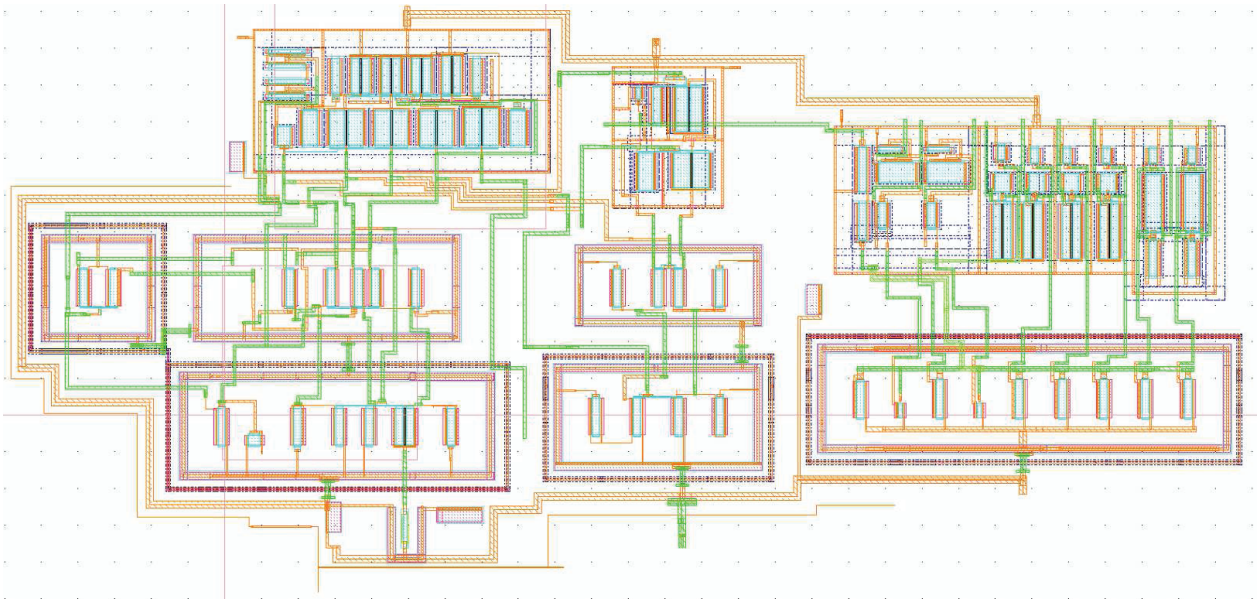


Figure C.12 The layout view of the reference circuit for HS, PS and other pulses.

C.2.4 Ramp voltage and half-sine pulse generators

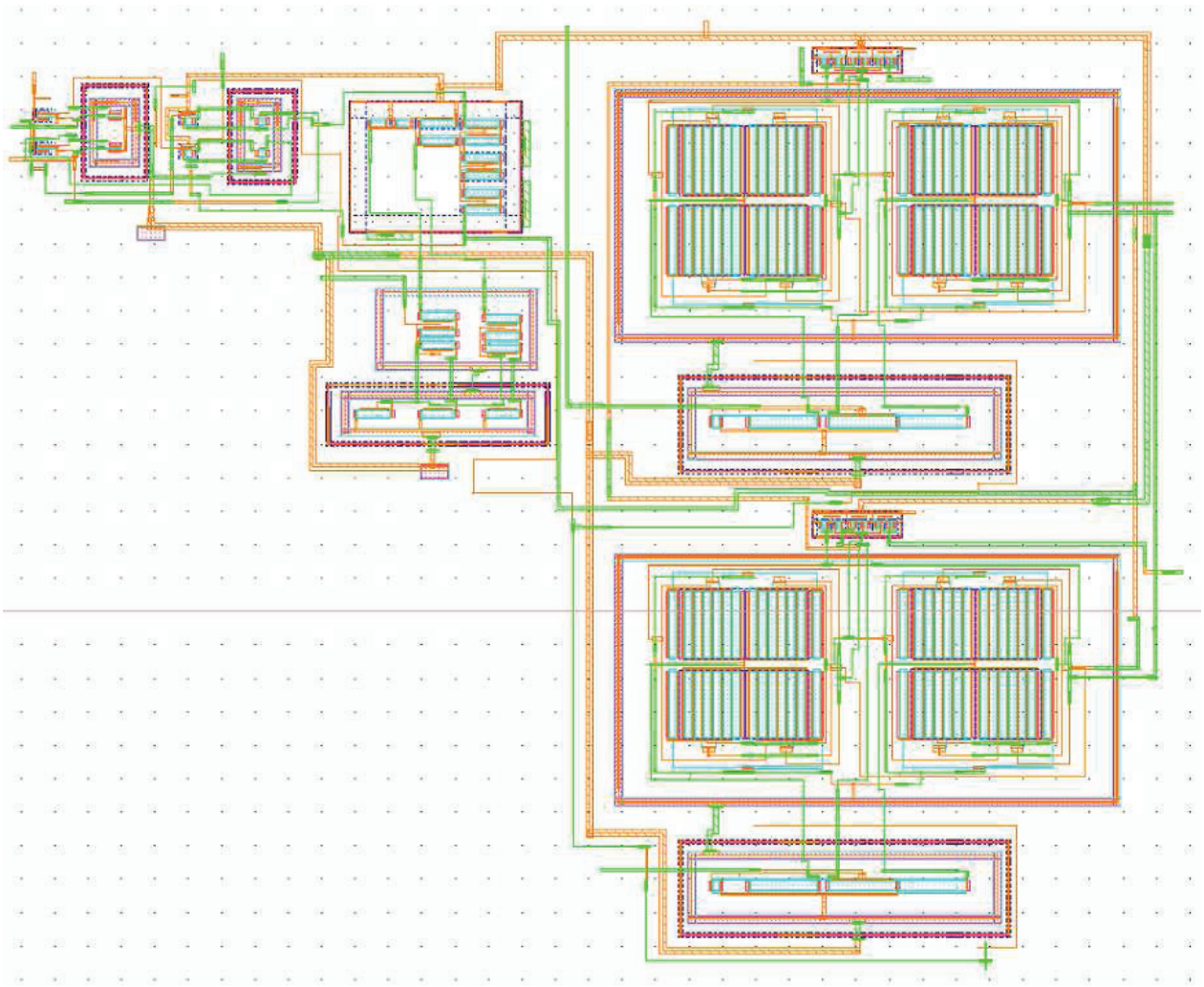


Figure C.13 The layout view of ramp voltage and HS pulse generators.

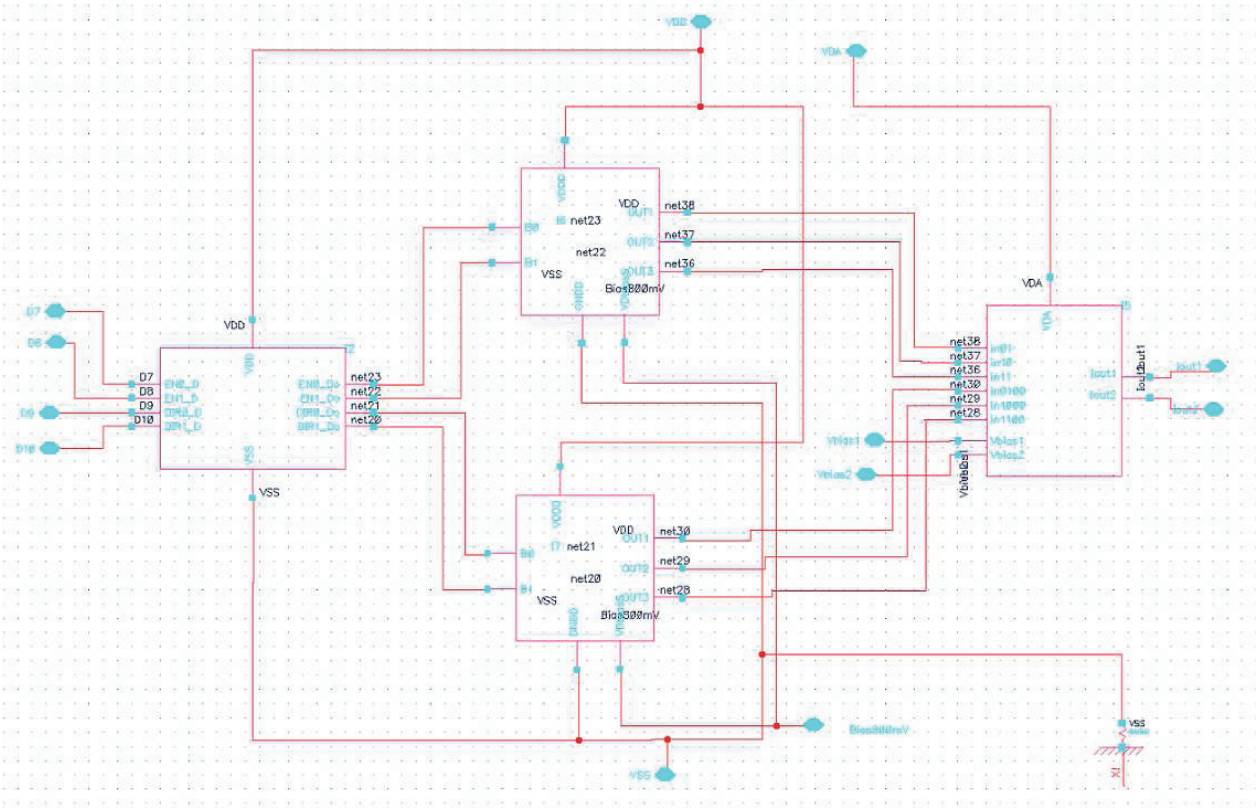


Figure C.14 The schematic diagram of Iprog current sources.

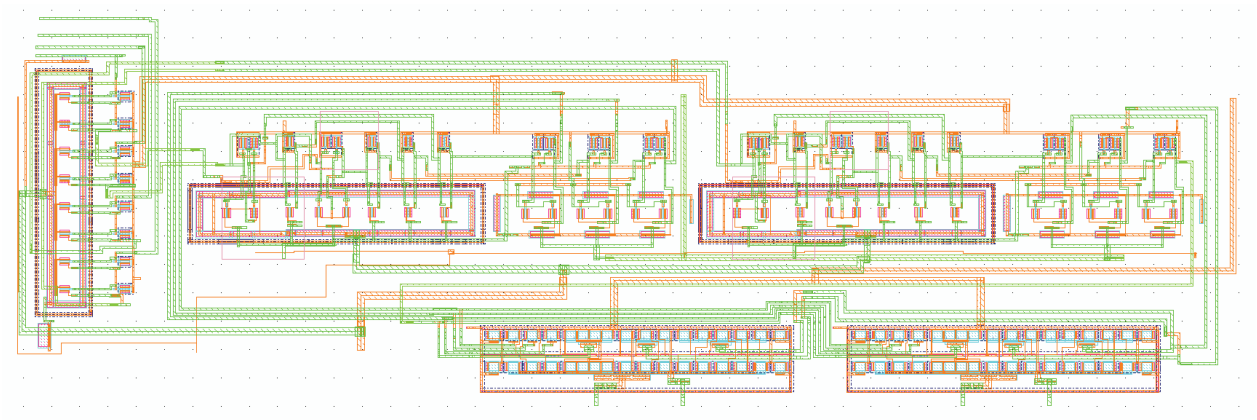


Figure C.15 The layout view of Iprog current sources.

C.2.5 On-chip controller

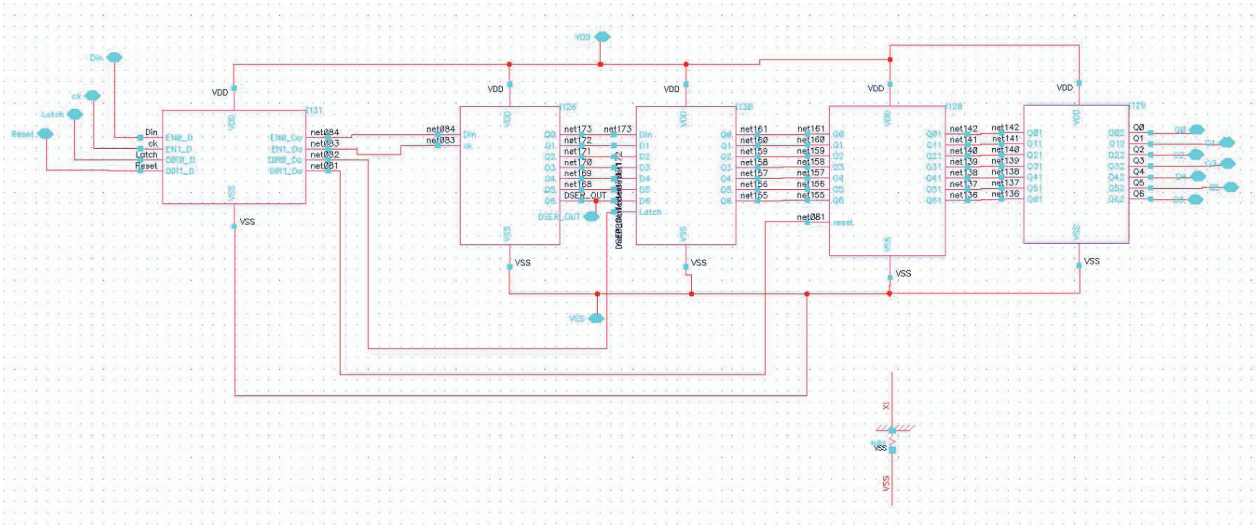


Figure C.16 The schematic diagram of the on-chip controller.

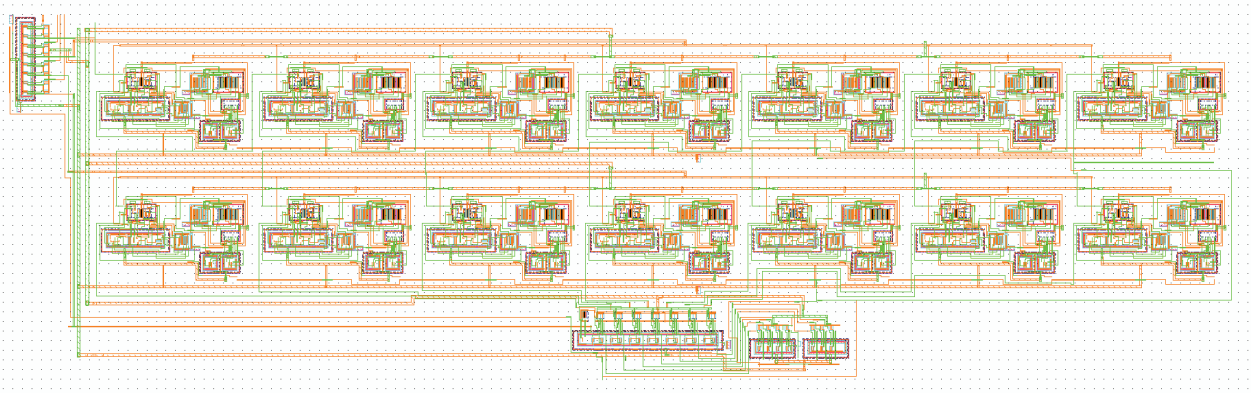


Figure C.17 The layout view of the on-chip controller.

C.2.6 Plateau-sine and other forms of pulse generator

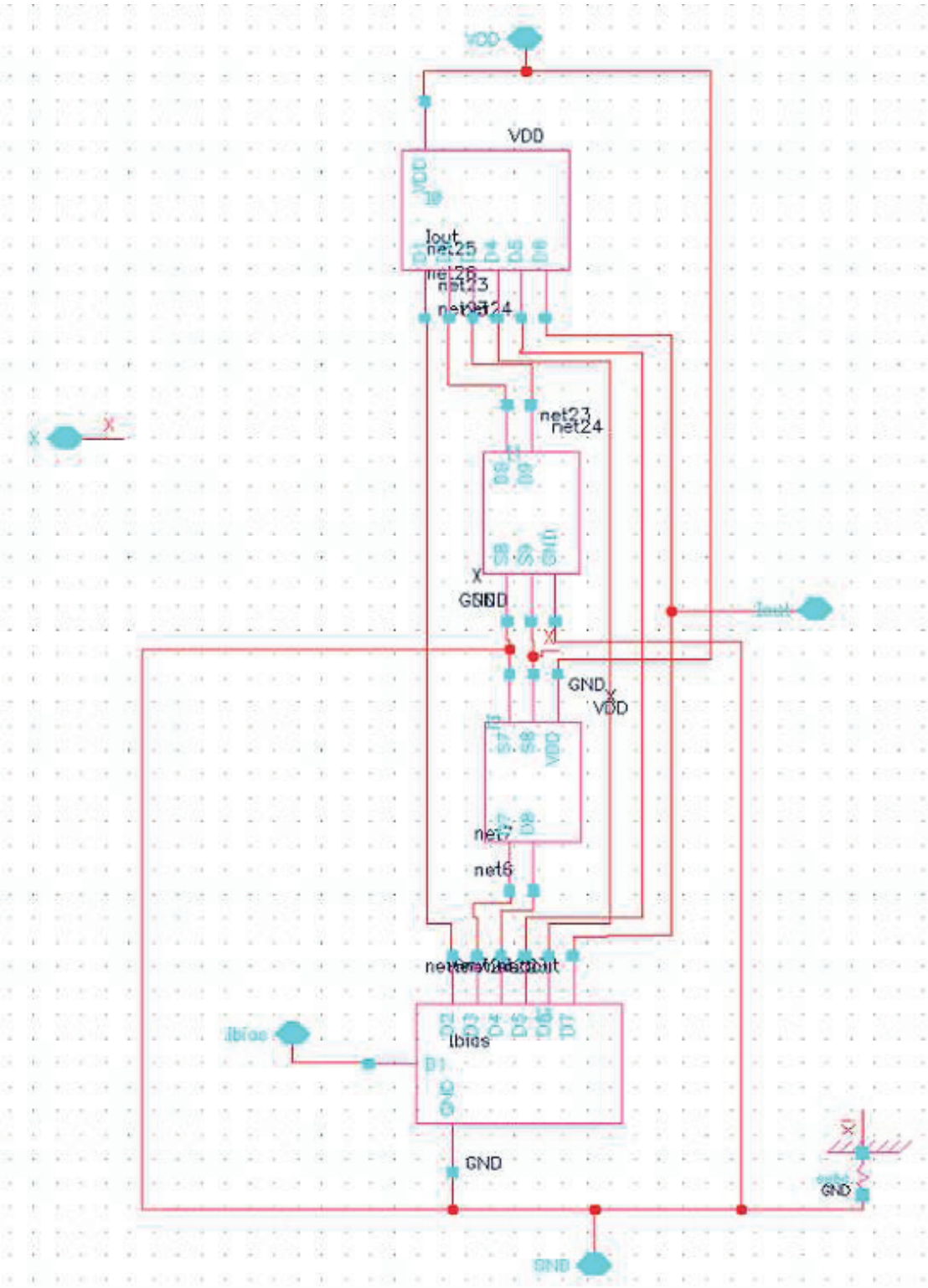


Figure C.18 The schematic diagram of HS and other pulse types.

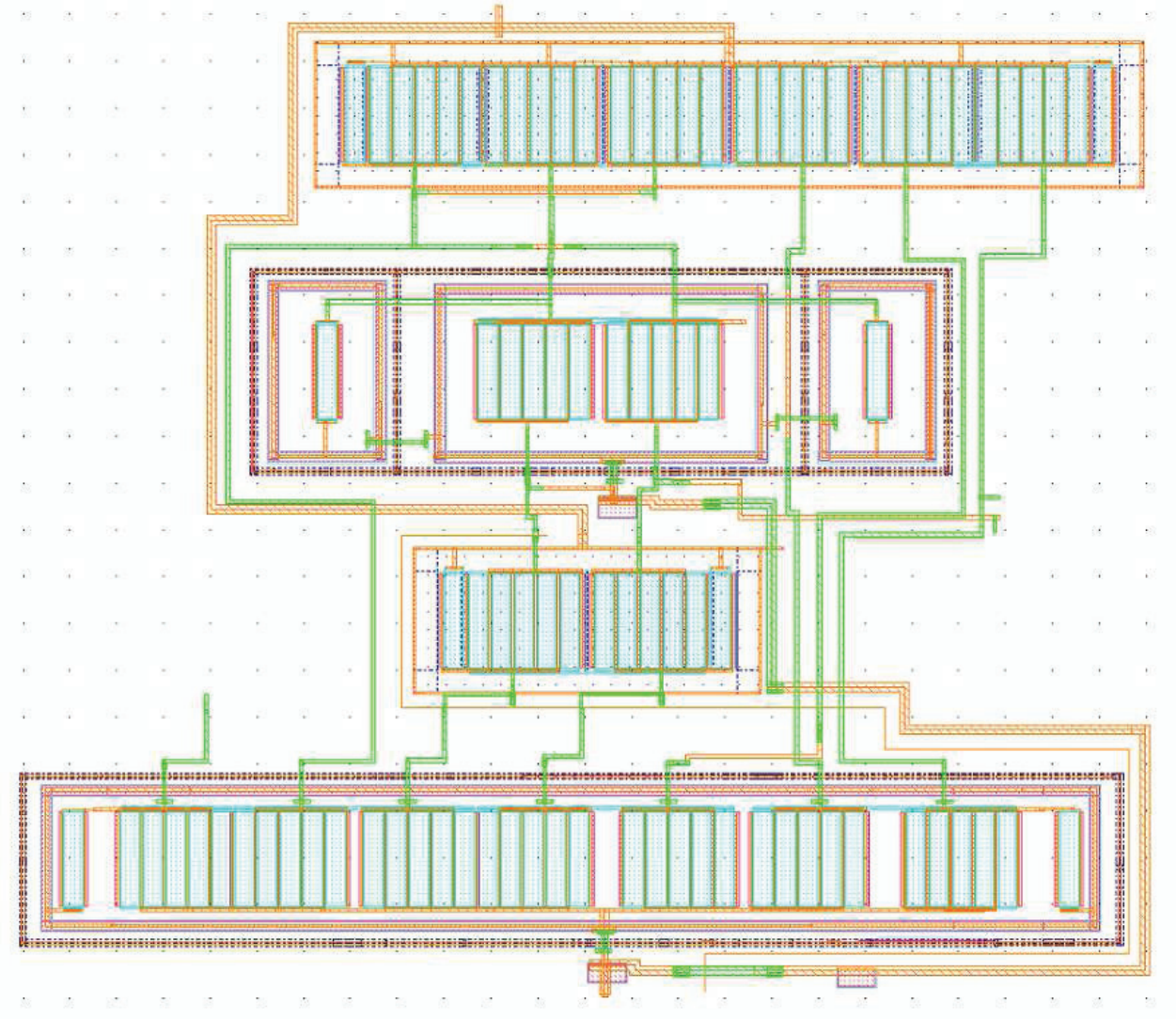


Figure C.19 The layout view of HS and other pulse types.

C.2.7 1.2V/3.3V current mirrors

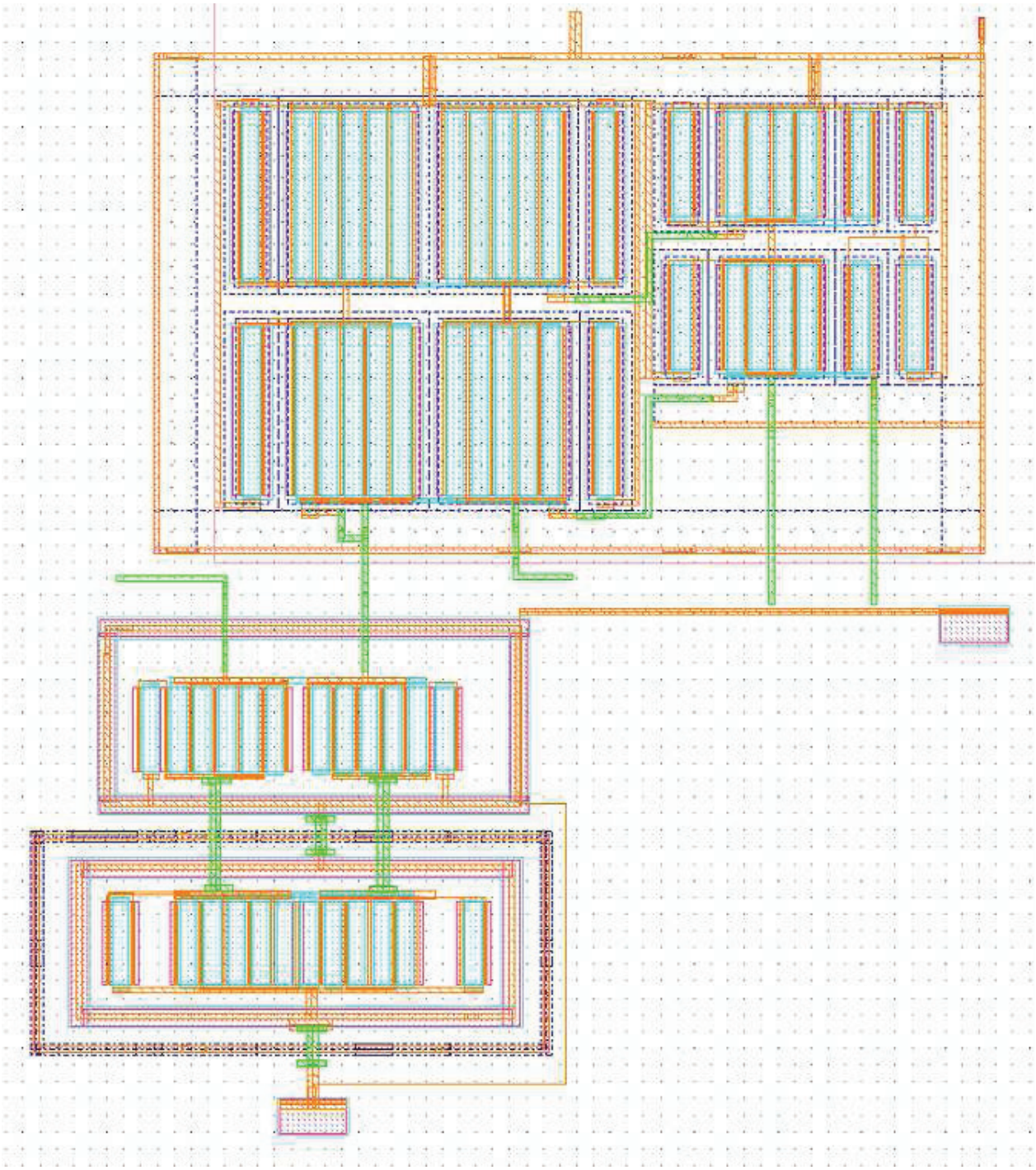


Figure C.20 The layout of the 1.2V/3.3V current mirror1 at the output of each source DAC.

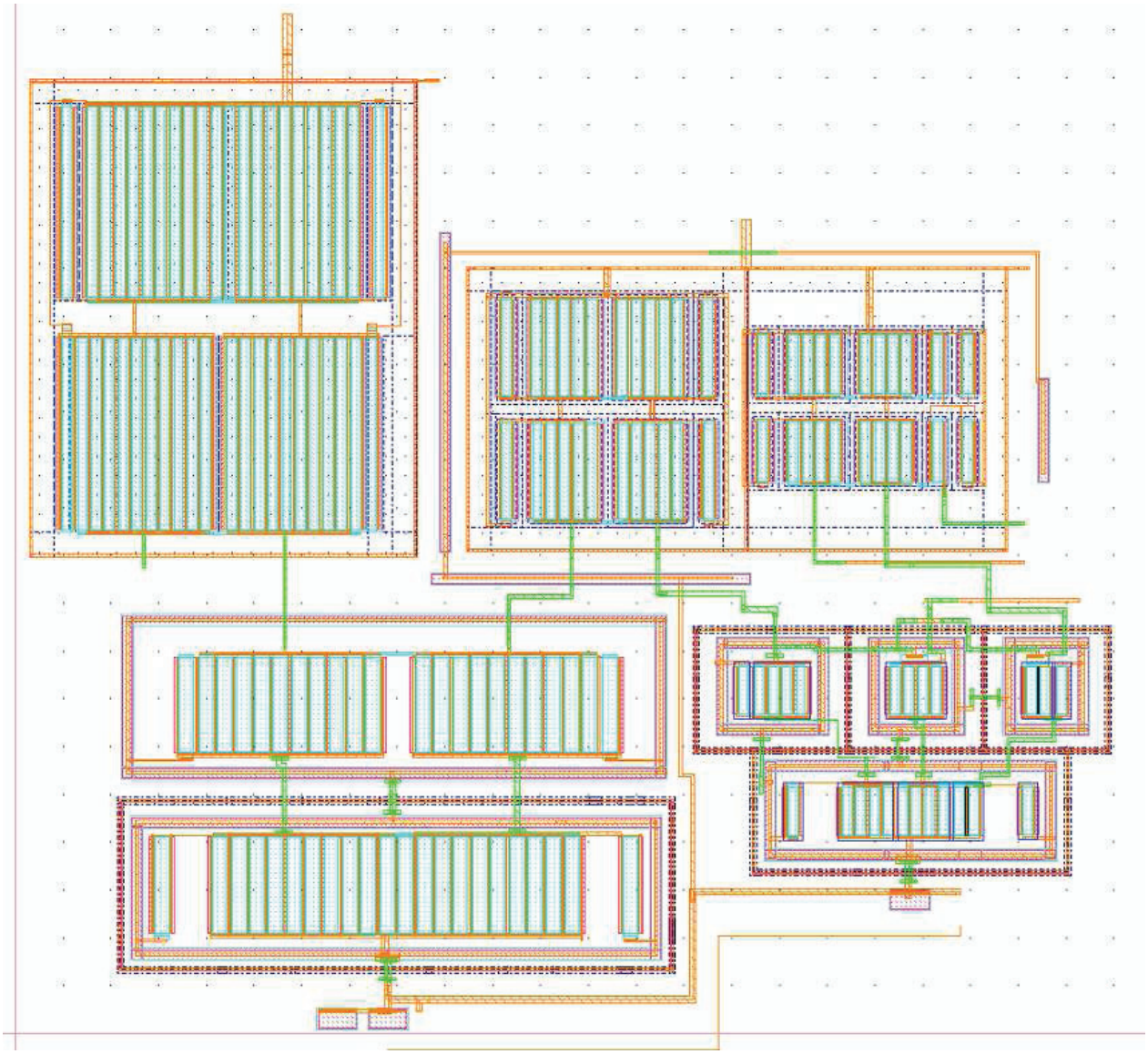


Figure C.21 The layout of the 1.2V/3.3V current mirror1 at the output of each sink DAC.

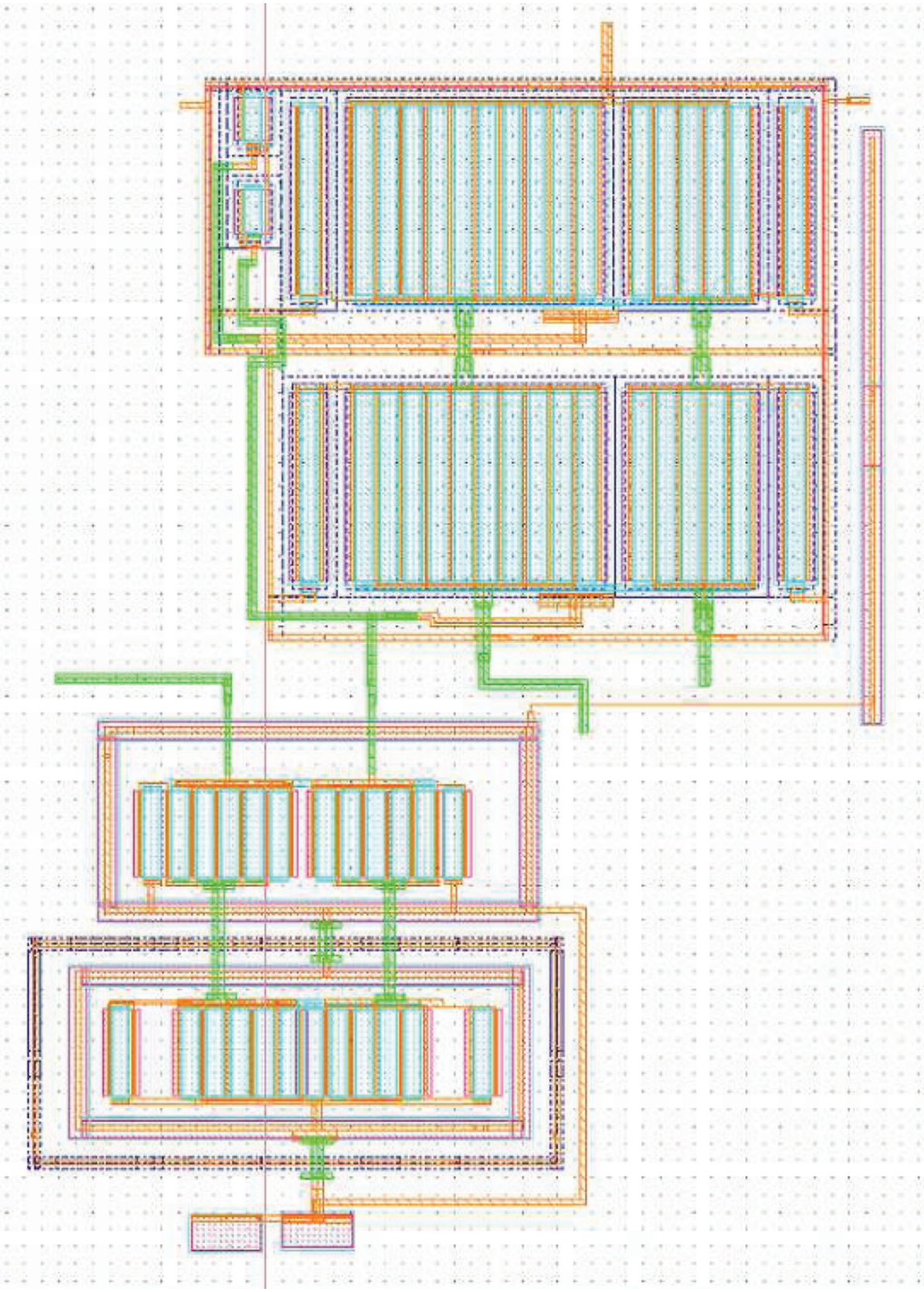


Figure C.22 The layout of the 1.2V/3.3V current mirror2 at the output of each source half-sine pulse generator.

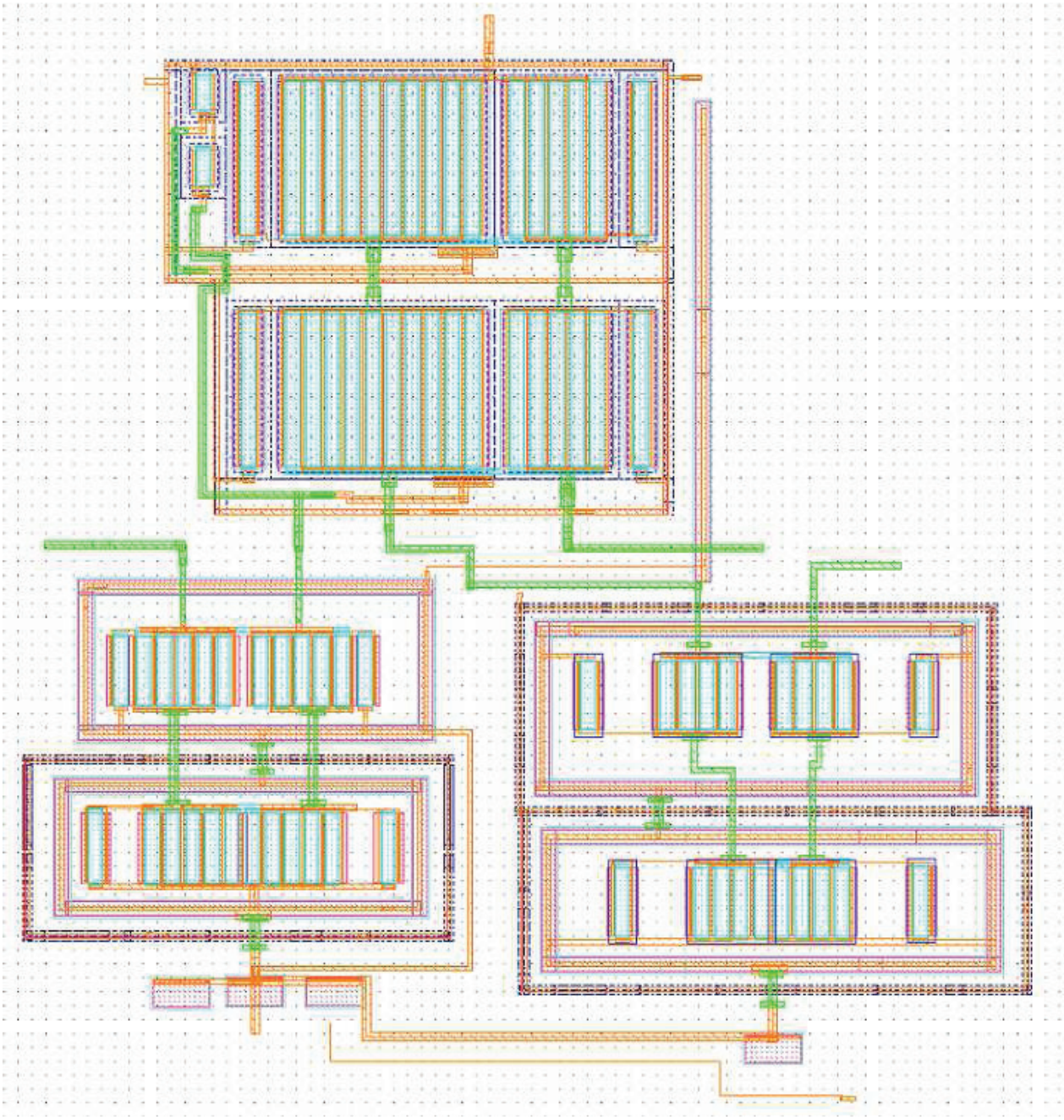


Figure C.23 The layout of the 1.2V/3.3V current mirror2 at the output of each sink half-sine pulse generator.

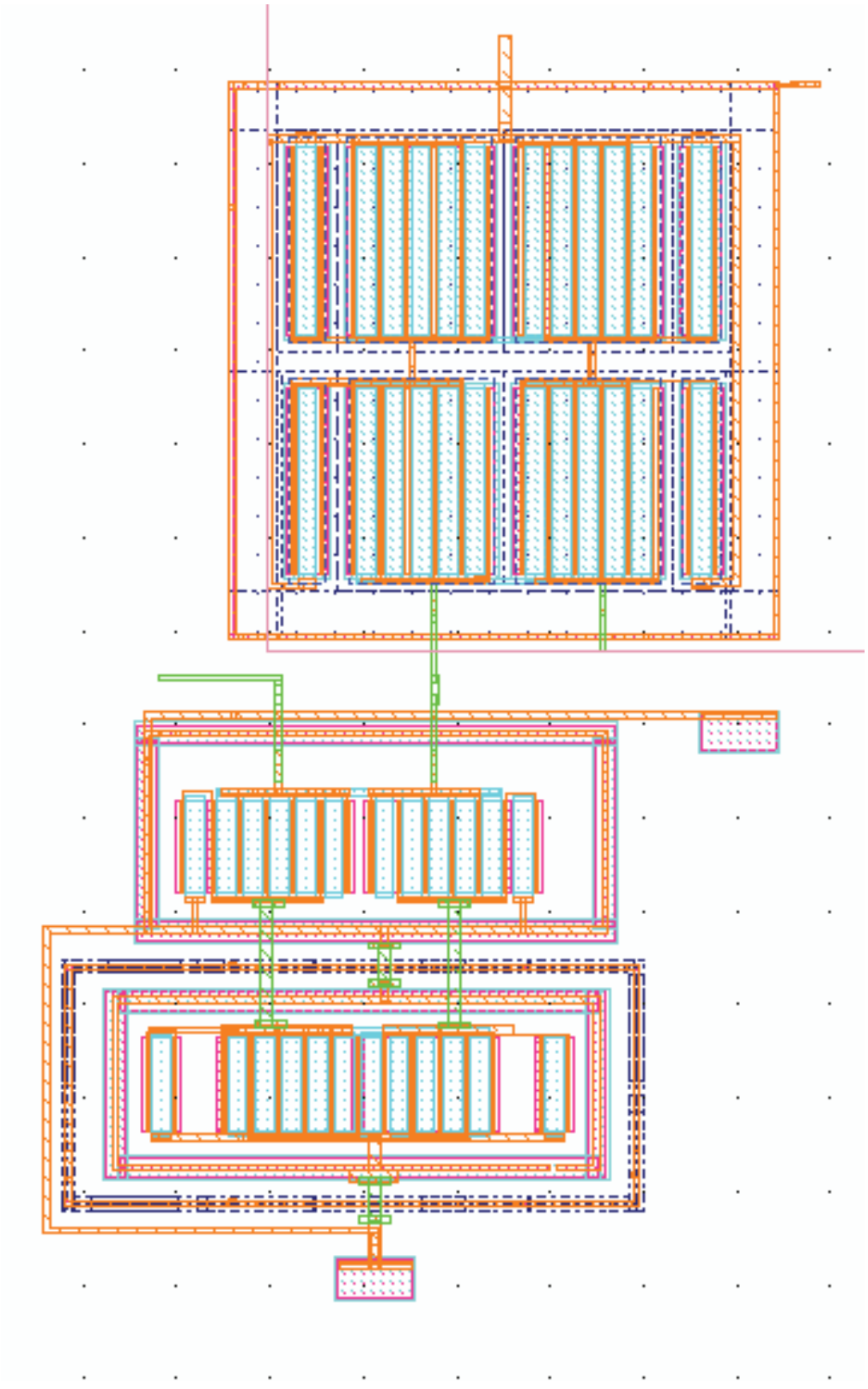


Figure C.24 The layout of the 1.2V/3.3V current mirror3 at the output of each source plateau-sine and other pulse generators.

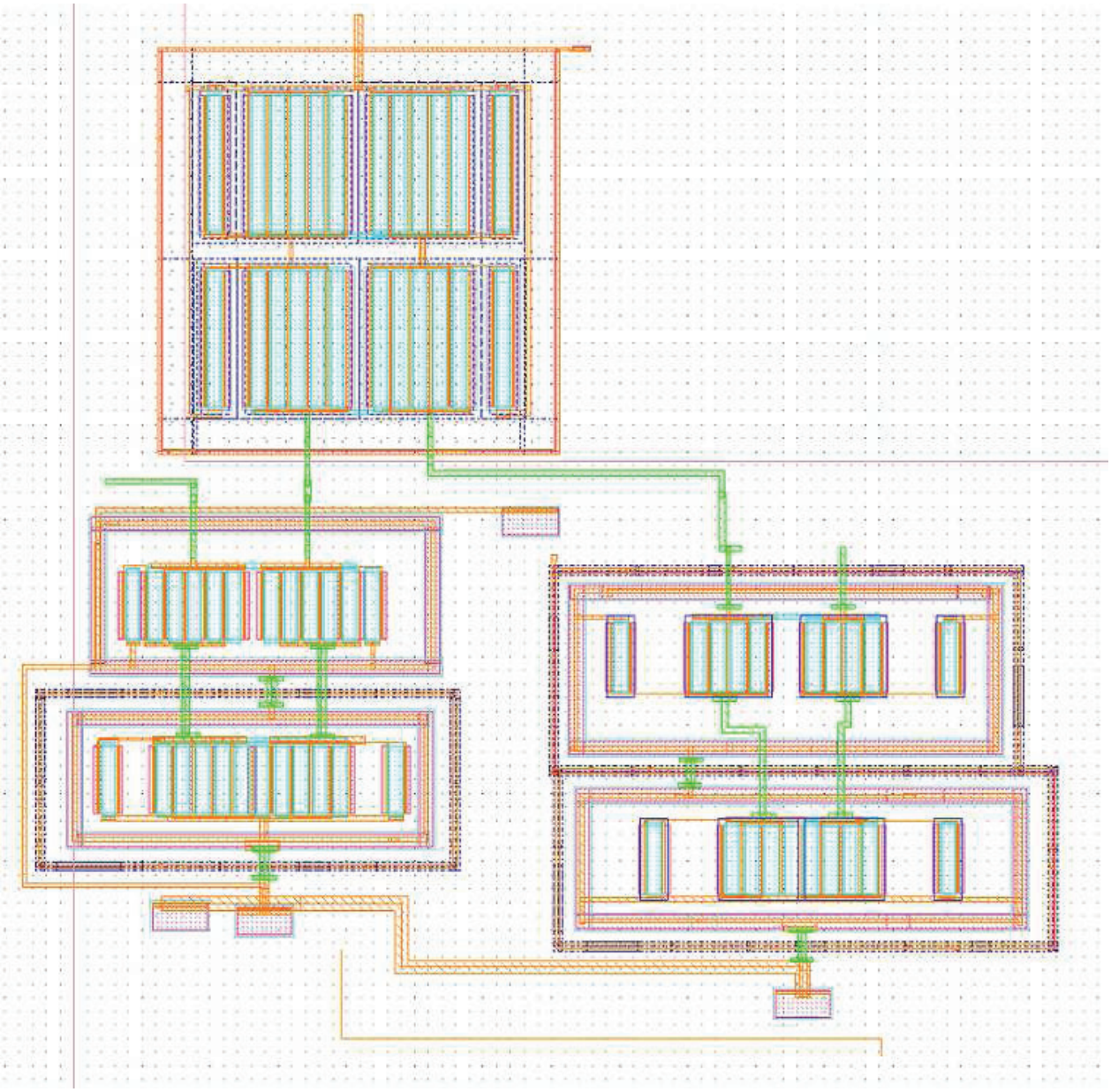


Figure C.25 The layout of the 1.2V/3.3V current mirror3 at the output of each sink plateau-sine and other pulse generators.

APPENDIX D

ICVPMMON: THE ETI VOLTAGE MONITORING UNIT CHIP

The schematic and layout views of the ETI voltage monitoring unit chip designed in AMS 0.35μm HV CMOS/DMOS technology are presented below:

D.1 Layout and schematic view of the chip ICVPMMON

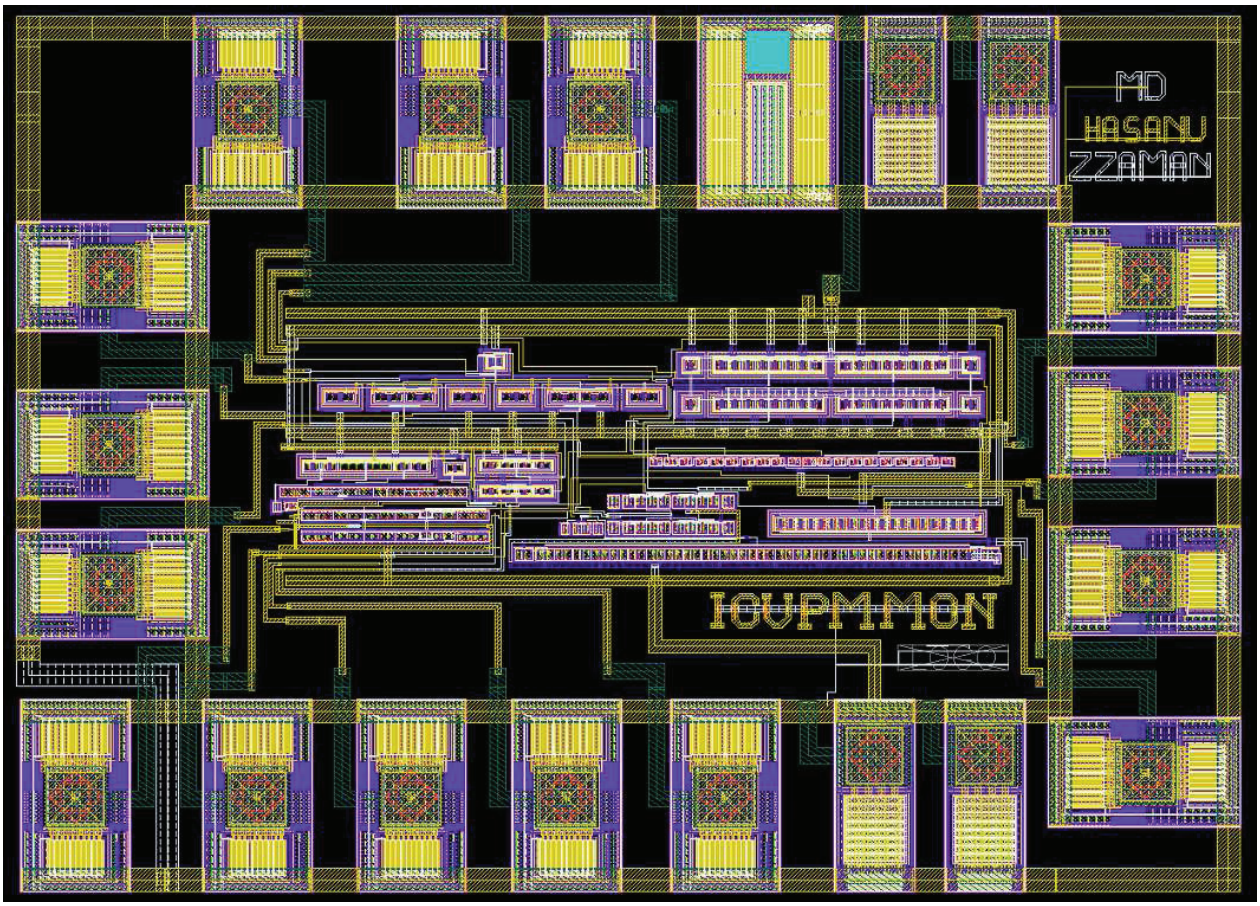


Figure D.1 The layout view of the ETI voltage monitoring unit chip ICVPMMON.

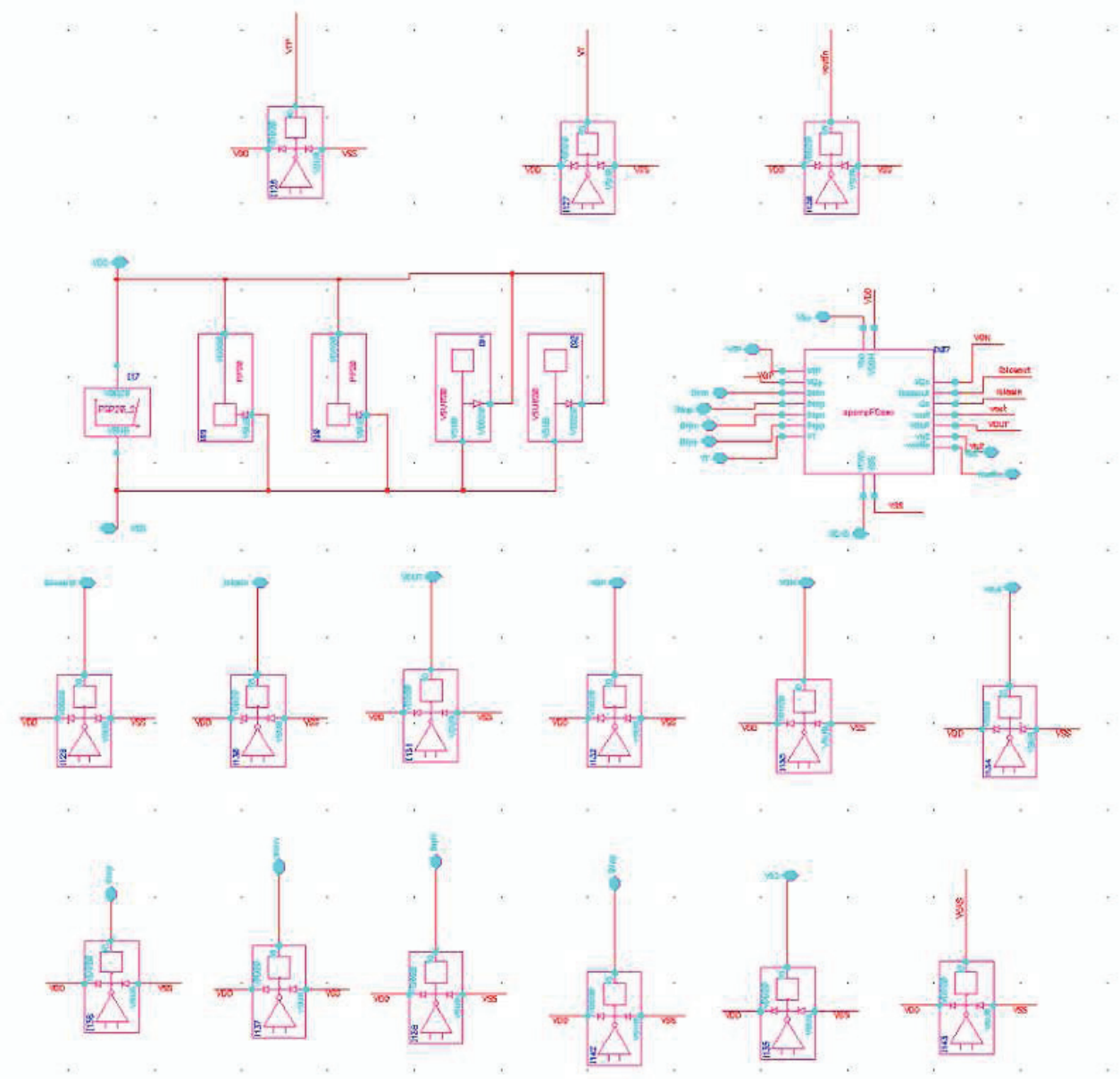


Figure D.2 The schematic view of the ETI voltage monitoring unit chip ICVPMMON.

D.2 Design level of the chip ICVPMMON

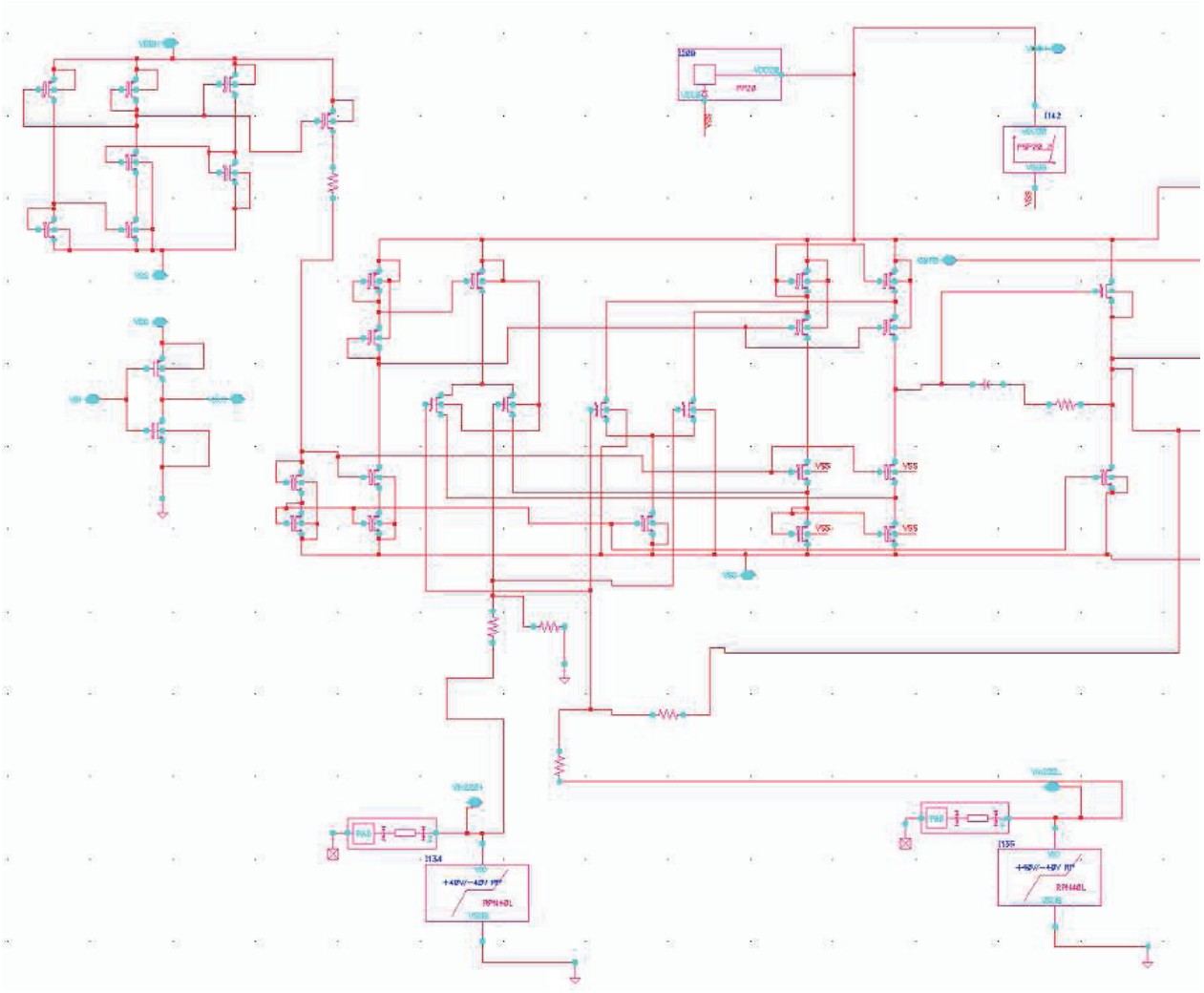


Figure D.3 The schematic view of the high-voltage rail-to-rail operational amplifier with differential inputs.