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UNIVERSITÉ DE MONTRÉAL

LOW-POWER HIGH DATA-RATE WIRELESS TRANSMITTER FOR MEDICAL IMPLANTABLE DEVICES

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Cette thèse intitulée :

LOW-POWER HIGH DATA-RATE WIRELESS TRANSMITTER FOR MEDICAL IMPLANTABLE DEVICES

présentée par : MORADI Arash

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DEDICATION

To my parents…

for their never-ending love and support.

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I am dedicating my thesis to my parents for their endless love and support along the way and I am thankful of my siblings, Simindokht, Amir and Sima, for their non-stop encouragement towards higher achievements. At last but not the least, I would like to thank my friends, primarily Mahsa Golkar for her inspiring and caring attitude as well as Kian Jalaleddini, Mina Ranjbaran and Omidreza Ghasemi, who kept their amiable company with me in the ups and downs during my stay in Montréal and

RÉSUMÉ

Les émetteurs-récepteurs radiofréquences (RF) sont les circuits de communication les plus communs pour établir des interfaces home-machine dédiées aux dispositifs médicaux implantables. Par exemple, la surveillance continue de paramètres de santé des patients souffrant d'épilepsie nécessite un étage de communication sans-fil capable de garantir un transfert de données rapide, en temps réel, à faible puissance tout en étant implémenté dans un faible volume. La consommation de puissance des dispositifs implantables implique une durée de vie limitée de la batterie qui nécessite alors une chirurgie pour son remplacement, a moins qu'une technique de transfert de puissance sans-fil soit utilisée pour recharger la batterie ou alimenter l'implant a travers les tissus humains.

Dans ce projet, nous avons conçu, implémenté et testé un émetteur RF à faible puissance et haut-débit de données opérant à 902-928 MHz de la bande fréquentielle industrielle-scientifique-médicale (ISM) d'Amérique du Nord. Cet émetteur fait partie d'un système de communication bidirectionnel dédié à l'interface sans-fil des dispositifs électroniques implantables et mettables et bénéficie d'une nouvelle approche de modulation par déplacement de fréquence (FSK). Les différentes étapes de conception et d'implémentation de l'architecture proposée pour l'émetteur sont discutées et analysées dans cette thèse. Les blocs de circuits sont réalisés suivant les équations dérivées de la modulation FSK proposée et qui mènera à l'amélioration du débit de données et de la consommation d'énergie. Chaque bloc est implémenté de manière à ce que la consommation d'énergie et la surface de silicium nécessaires soient réduites. L'étage de modulation et le circuit mélangeur ne nécessitent aucun courant continu grâce à leur structure passive.

Parmi les circuits originaux, un oscillateur en quadrature contrôlé-en-tension (QVCO) de faible puissance est réalisé pour générer des signaux différentiels en quadrature, rail-à-rail avec deux gammes de fréquences principales de 0.3 à 11.5 MHz et de 3 à 40 MHz. L'étage de sortie énergivore est également amélioré et optimisé pour atteindre une efficacité de puissance de ~ 37%. L'émetteur proposé a été implémenté et fabriqué à la suite de simulations post-layout approfondies. Les résultats de simulations et de mesure sont discutés et comparés avec ceux des émetteurs modernes démontrant ainsi la contribution de ce travail dans ce domaine de recherche

très populaire. Le facteur-de-mérite (FOM) a été amélioré impliquant essentiellement l'augmentation du débit de données et la réduction de la consommation d'énergie du circuit. L'émetteur est implémenté en utilisant une technologie CMOS de 130 nm alimentée par une tension 1.2 V. Avec 1.4 mA de consommation de courant, un débit de données de 8 Mb/s a été mesuré résultant en une consommation d'énergie de 0.21 nJ/b. L'émetteur fabriqué occupe une surface active de silicium inférieure à 0.25 mm^2.

ABSTRACT

Wireless radio frequency (RF) transceivers are the most common communication front-ends used to realize the human-machine interfaces of medical devices. Continuous monitoring of body behaviour of patients suffering from Epilepsy, for example, requires a wireless communication front-end capable of maintaining a fast, real-time and low-power data communication while implemented in small size. Power budget limitation of the implantable and wearable medical devices obliges engineers to replace or recharge the battery cell through frequent medial surgeries or other power transfer techniques.

In this project, a low-power and high data-rate RF transmitter (Tx) operating at North-American Industrial-Scientific-Medical (ISM) frequency band (902-928 MHz) is designed, implemented and tested. This transmitter is a part of a bi-directional transceiver dedicated to the wireless interface of implantable and wearable medical devices and benefits from a new efficient Frequency-Shift Keying (FSK) modulation scheme. Different design and implementation stages of the proposed transmitter architecture are discussed and analyzed in this thesis. The building blocks are realized according to the equations derived from the proposed FSK modulation, which results in improvement in data-rate and power consumption. Each block is implemented such that the power consumption and needed chip area are lowered while the modulation block and the mixer circuit require no DC current due to their passive structure.

Among the original blocks, a low-power quadrature voltage-controlled oscillator (QVCO) is achieved to provide differential quadrature rail-to-rail signals with two main frequency ranges of 0.3-11.5 MHz and 3-40 MHz. The power-hungry output stage is also improved and optimized to achieve power efficiency of ~37%. The proposed transmitter was implemented and fabricated following deep characterisation by post-layout simulation. Both simulation and measurement results are discussed and compared with state-of-the-art transmitters showing the contribution of this work in this very popular research field. The Figure-Of-Merit (FOM) was improved, meaning mainly increasing the data-rate and lowering the power consumption of the circuit. The transmitter is implemented using 130 nm CMOS technology with 1.2 V supply voltage. A data-rate of 8 Mb/s was measured while consuming 1.4 mA and resulting in energy consumption of 0.21 nJ/b. The fabricated transmitter has small active silicon area of less than 0.25 mm^2.

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LIST OF ACRONYMS AND ABBREVIATIONS

ADC	Analog to Digital Converter
BFSK	Binary Frequency-Shift-Keying
BPF	Band-Pass Filter
BSN	Body Sensor Network
CMOS	Complementary Metal-Oxide-Semiconductor
DCO	Digitally-Controlled Oscillator
IF	Intermediate Frequency
ILFD	Injection-Locked Frequency Divider
ISM	Industrial-Scientific-Medical
EEG	Electroencephalography
ESD	Electrostatic Discharge
fNIRS	Functional Near-Infrared Spectroscopy
FOM	Figure-Of-Merit
FSK	Frequency Shift-Keying
GFSK	Gaussian Frequency-Shift-Keying
LC	Inductor-Capacitor
LO	Local Oscillator
MI	Modulation Index
OOK	On-Off-Keying
PA	Power Amplifier
PCB	Printed Circuit Board

PPF	Poly-Phase Filter
PSK	Phase Shift-Keying
QFN	Quad Flat No-lead
QVCO	Quadrature Voltage-Controlled Oscillator
RF	Radio Frequency
RFID	Radio Frequency Identification
RMS	Root Mean Square
Rx	Receiver
SNR	Signal-To-Noise Ratio
TRX	Transceiver
Tx	Transmitter
WSN	Wireless Sensor Network

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CHAPTER 1

INTRODUCTION

1.1 RF transceivers in medical applications

Medical applications of implantable and wearable body sensors keep short-range wireless communication as a challenging and hot research topic for monitoring and detection of various health parameters, such as temperature, pressure, oxygenation, seizures and other signs of diseases. For instance, the continuous monitoring of oxygen level of the blood for patients suffering from epilepsy may help locating, treating and even preventing the emerging of seizures. Even monitoring the behaviour of freely-moving animals, where free-running circuits are demanded, offers the chance to extract medical information in realistic conditions, thanks to wireless technologies. However, all requirements of a medical interface have to be considered and implementing such wireless communication interface remains challenging in many aspects.

Thanks to CMOS technology, the small size of the implemented front-ends helps to get rid of external bulky components. Among all challenges to realize the link between the implanted device and the external processing base station, the main challenge in addition to the size is in reducing the power consumption of the communication front-end for transferring information. Since the implanted devices have limitation over power storage, different circuits and systems design techniques have to be employed [1-4]. Radio Frequency (RF) transceivers, as the wireless communication front-end of body sensors, have the role of transmitting (Tx) and receiving (Rx) information (Figure 1.1) and usually they sink more than 90% of consumed power in emerging bio-devices. Data modulation is necessary to transmit the digital or analog data and to efficiently use the limited electrical bandwidth. Specific frequency ranges are allocated to be used as the electrical frequency bandwidth for the mentioned transceivers, mostly North-American Industrial-Medical-Scientific (ISM) frequency band (902-928 MHz) and European Medical-Implant-Communication-Service (MICS) frequency band (402-405 MHz). Consequently, the transceiver architecture and the employed modulation directly affect the performance of the target transmitter in terms of size, power consumption and data-rate.

Wireless sensor networks show their importance in communication for remote and inaccessible locations including inside the human body. Wireless transceivers are usually the most critical blocks in sensors in terms of power consumption. In addition to power consumption, the size, communication data-rate and, in total, designing high-efficiency wireless transceivers have been an interesting topic in circuit and system designs.

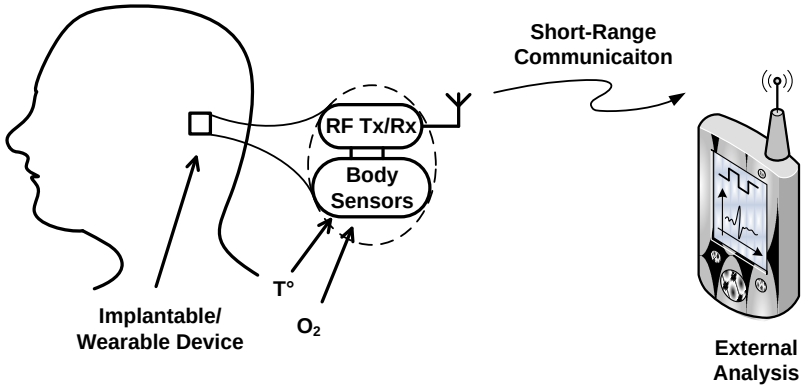


Figure 1.1: RF Transceivers used for human-machine wireless interface

In general, the transmitter power may be reduced to less than 1 mW in short-range communication application to relax the total current budget [5]. As an example, in the 400 MHz transmitter [6], the output power level is reduced to -59 dBm when the transmitter consumes less than 0.5 mW for transmitting each bit of data for a 1 m communication distance. As another example for monitoring freely-moving animals, a 900 MHz transmitter [7] consumes 1 mW to maintain the communication in ~2 m range. Power harvesting techniques may be used to power up the device, but, managing the collected power is a great challenge itself. The related reported front-end circuits in the literature and their performance are summarized and discussed in the following chapter.

In total, in addition to the current budget, the number of needed external components and maximum data-rate still remain challenging issues in implantable/wearable wireless communication devices. In practice, the medical sensor node is used to detect and monitor the target information from body using a number of channels, such as in electroencephalography (EEG) recordings. After the biomedical signal acquisition, the signal is digitized by an analog-to-

digital converter (ADC) with a specific sampling rate and reasonable precision. Finally, the extracted data can be processed (compressed for example) before the transmission starts with a high data-rate RF transmitter operating in range of few Mb/s [8].

The electrical bandwidth together with the signal-to-noise ratio, according to the well-known Shannon-Hartley theorem, defines the maximum communication channel capacity. Signal power level is usually defined according to the application and can be lowered in low-power applications to reduce energy consumption. In practice, the power level may be at least 30 to 40 dB higher than noise level and the attenuation caused by the working environment has to be considered. On the other hand, modulation is necessary to wisely use the limited electrical bandwidth and to physically transmit the digital or analog data. When the information signal is digital and the amplitude is varying according to the digital data, the Amplitude Shift-Keying (ASK) modulation, such as OOK, is used. Similarly, when the information is integrated into the frequency or phase, the modulation is called FSK and Phase Shift-Keying (PSK), respectively. In the following, characteristics of the FSK and OOK modulation schemes are briefly discussed and compared. Then, advantages and disadvantages of the common RF transmitter architectures, heterodyne and direct-conversion, are reviewed towards low-power implementation. In the next chapter, an overview on the architectures, behaviour, advantages and disadvantages of the low-power ISM-band transmitters is presented. The literature review is narrowed down to 915 MHz Binary FSK (BFSK) transmitters concluding that a high data-rate and low-power integrated design is mandatory for emerging medical devices.

1.1.1 Modulation: FSK vs. OOK

Proper choice of architecture results in how efficient the system can operate [9]. In order to have a low-power transceiver, the modulation scheme has to be as simple as possible. As reported in literature [10-19], the modulation schemes of FSK and OOK are widely used in transmitter (Tx) and receiver (Rx) building blocks, respectively, since they are phase independent and can be detected by non-coherent architectures. Implementing a data modulator with low-power consumption in wireless transceivers is of interest as the power budget is limited especially in implantable devices where long-life batteries are required.

In general, carrying information in the amplitude requires a highly linear power amplifier and the signal would be more susceptible to noise. In implantable and low-power consumption applications, where the level of signal is intentionally reduced, the information is more likely to be carried in the frequency. When the signal level is low, a linear power amplifier is needed in OOK modulation while FSK modulation has constant envelope with continuous phase and can be realized using non-linear power amplifiers [4, 20, 21]. In practice, the frequency content of the information is shifted up using a carrier frequency (f_c) to reduce the effect of noise and disturbance from surrounding instrument and, hence, a Local Oscillator (LO) is necessary. In OOK, the biasing point of the transmitter circuit and the oscillator have to settle in less than a single bit period and this may limit the data-rate. Due to discontinuity in phase, the power spectrum of the binary PSK has larger side lobes than that of the binary FSK. As a result, FSK modulation is the best candidate in the implantable side while the OOK modulation is used in the external side. In FSK modulation, which is generally simpler than PSK in terms of detection, the center frequency is shifted to two close frequencies and this can be considered as sending the data of '1' and '0', as shown in Figure 1.2. The minimum bandwidth for FSK modulation is approximated as $B=2(\Delta f+f_d)$, where B is the channel bandwidth, Δf is the shifting frequency and f_d is the data-rate. In definition, Modulation Index (MI) for FSK modulation can be defined as the frequency deviation over the data-rate and the frequency deviation can be chosen due to bandwidth availability or data-rate requirement. Large modulation index of 2 in an FSK modulation, for example, can help relaxing the precision requirement [4] which means less deviation from the constellation points and, hence, smaller FSK error is expected.

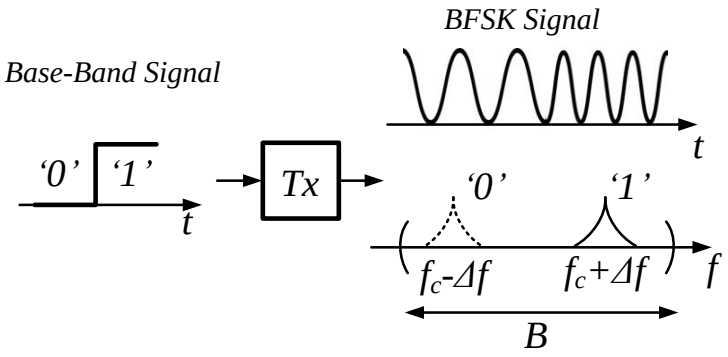


Figure 1.2: Generation of FSK signal from baseband data

1.1.2 General RF Transmitter Architectures

Performance of any RF transmitter in terms of total power consumption and data-rate depends on its architecture and the employed modulation [22]. As reported in a survey in [9], which reviews the transceivers reported from 1997 to 2007 in IEEE Solid-State forums, Zero-IF architecture is a first choice for Rx path as well as Direct-Up Conversion for Tx path in most communication standards. Expensive and bulky heterodyne architectures with their high-power consumption are not acceptable for mentioned applications. Also, image-reject architectures suffering from first and secondary images need a high I/Q matching and even a two-step-up conversion still suffers from image problem. Low cost, high integration level, simplicity and having no image problem make the Zero-IF/Direct-Up Conversion architectures suitable for implantable transceivers.

A transceiver has both transmitter and receiver parts which may share one or more circuitries. RF modules are used for high speed data-transmission and they may be implemented with both analog and digital circuits. Since digital circuits may consume less power, in particular cases, and give advantage of scalability, it is preferable to bring the digital domain closer to the antenna which can be very challenging. Passive components may also be used to reduce the power consumption. Simplicity, data-rate and power dissipation as well as number of external components are the primary criteria in choosing transceiver architecture. Depending on the application and the required specifications, different architectures may be used to develop a transmitter. Practically, the goal is to modulate the data by varying one or more properties such that the transmission or reception would be beneficial in terms of speed and power consumption.

The RF transmitter performs modulation, up-conversion and power amplification. The two main transmitter architectures, Heterodyne and Direct-Conversion, are discussed in the following.

1.1.2.1 Direct-Conversion transmitters

To achieve a highly integrated and low-power consumption transceiver, direct-conversion method is used which can replace the heterodyne architecture. In this architecture, the baseband data is quadrature modulated while the I and Q signals are up-converted using a local oscillator

(ω_c), as shown in Figure 1.3. Simplicity of this architecture makes suitable for implantable and low-power applications. Also, the image-rejection is no more a problem in the receiver side for direct down-conversion. In total, avoiding the problem of image-rejection and having less current consuming building blocks are two main benefits of this architecture [23]. Also, Direct-Up Conversion architecture needs a simple frequency plan for multi-standard designs [9].

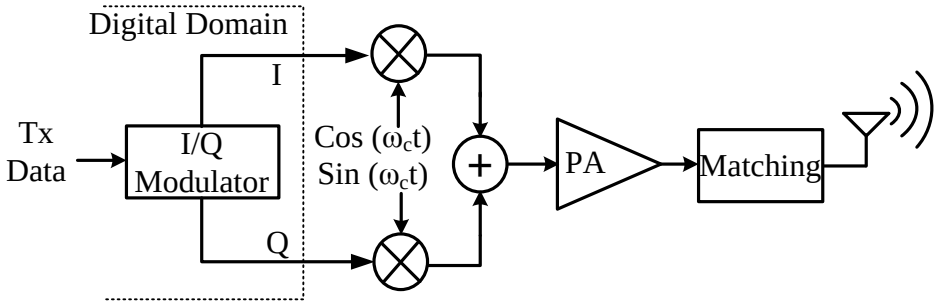


Figure 1.3: General direct-conversion transmitter architecture

Notice that the baseband signals generated in the transmitter side are sufficiently strong and noise of mixers is not critical such as in receivers [22]. However, the leakage of PA output to the oscillator is still an issue since the output of the PA is a modulated waveform with high signal power and a spectrum centered around the LO frequency. Due to imperfection of shielding, injection pulling is inevitable and the noisy and amplified output of PA corrupts the spectrum of the oscillator. Moreover, phase and amplitude mismatch of I/Q signals in addition to DC offset and 1/f noise may lead to large error in constellation diagram and have to be minimized.

1.1.2.2 Two-Step transmitters (Heterodyne)

A heterodyne transmitter (Figure 1.4) is the reverse operation of a heterodyne receiver [1, 24]. Two-step up-conversion gives the advantage of having less severe issues with injection pulling as the baseband signal is up-converted in at least two steps using two oscillators (ω_1 and ω_2). As illustrated in Figure 1.4, the output frequency is far from the frequency of each oscillator. However, more filtering is needed and the band-pass filter (BPF) has to reject the unwanted sideband by large factor since the second up-converting mixer generates wanted and unwanted sidebands with equal magnitudes [22]. The necessity of off-chip passive components in filters

limits the integration aspect. Also, the additional oscillator circuit brings more complexity and power consumption to the architecture. In total, heterodyne architectures have a more reliable performance with a flexible frequency plan at the expense of being bulky and consuming more power than the direct-conversion based circuits.

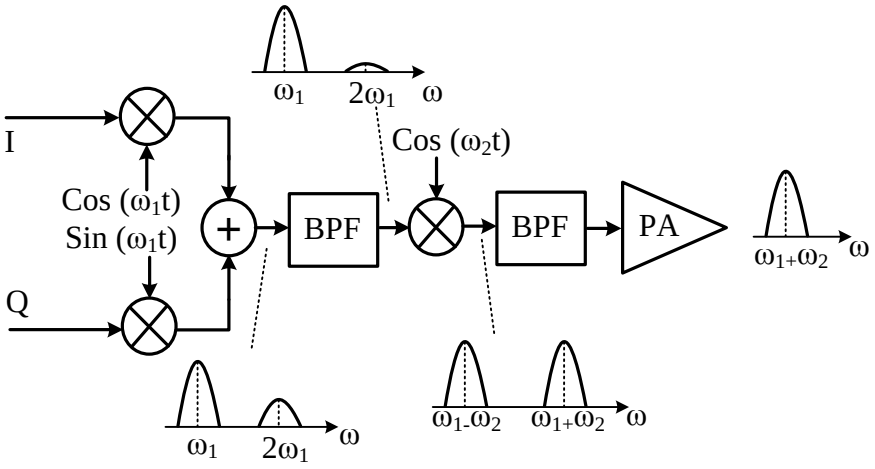


Figure 1.4: Two-step up conversion transmitter architecture

Generation of RF signal, its modulation and driving it into an antenna are the basic functions of any RF transmitter [4, 22]. Direct-Up conversion architecture is chosen to avoid image-rejection problem. FSK modulation is also chosen to realize the transmitter side since OOK is strongly susceptible to interference and a linear power amplifier (PA) is required. In practice, two desired frequencies corresponding to data '1' and '0' are generated by the transmitter. The frequency deviation depends on the available channel bandwidth which is essential in narrow-band applications.

To sum up, the principles of the FSK modulation in comparison with OOK modulation were reviewed and it was conferred that the FSK modulation is more suitable and common for implantable transmitter section of a bidirectional transceiver while OOK modulation is more used for the receiver section. Then, the basic transmitter architectures, Direct-Conversion and Two-Step, were reviewed concluding that the Direct-Conversion architecture is more fit to integrated and low-power applications.

1.2 Motivation

Continuous monitoring and detection of health parameters of patients' body is practicable these days using new implantable and wearable biomedical sensors. Indeed, human-machine direct interaction can be minimized by using such wireless sensors and the patients do not need to be connected permanently (or for long period of time) to monitoring equipment. High energy-efficient circuits and systems design techniques are demanded to realize smart medical devices where low-power consumption, size and speed of communication are the priorities [25]. Different wireless sensor network (WSN) platforms may be used for health monitoring where wearable and implantable wireless circuits are needed. Such medical devices can have electrode-tissue interface or an implanted sensor and they may be used for detection of different body parameters such as temperature or drug delivery.

As depicted in Figure 1.1, Radio Frequency transceivers as the communication interface of wireless sensor networks (WSNs) are required in several biomedical applications such as monitoring brain activities for patients with brain diseases (Epilepsy). Such implanted devices have to consume very low power; otherwise, the battery cell of these devices has to be recharged through frequent medical surgeries. In general, the goal is to keep the implantable transmitter as simple and low-power as possible. Instead, the external receiver can be more complex.

The implemented transmitter in this thesis is dedicated to a target EEG-fNIRS brain monitoring sensor for patients suffering from Epilepsy, similar to [26]. In this research, the goal is to transfer the extracted information from blood to predict the seizure using up to 32 channels of EEG and 128 channels of fNIRS with 320 and 20 Hz needed sampling rate, respectively. A 16-bit analog-to-digital convertor (ADC) is also considered for digitization. The approximate required data-rate for real-time monitoring is then estimated by channels × sampling rate (Hz) × bits (ADC) resulting in about 500 kb/s of data-rate in the communication front-end. However, the data needs to be encoded and the necessary communication protocols have to be applied, which mean a throughput rate of 3 or 4 times higher in Mb/s range is necessary. One may use a novel encoding technique to lower the total needed power such as in [27], but the power-hungry analog front-end is usually the center of attention when low-power and high data-rate communication is of interest.

As a result, a much higher data-rate in range of few Mb/s is needed for real-time monitoring while the integrated front-end consumes as low power and small area as possible. In practice, a new modulation and architecture can be implemented to realize a low-power and high data-rate communication interface. Then, circuits of the composing building blocks in the designed architecture need to be carefully designed and implemented to minimize current consumption and area. Finally, the corresponding prototype has to be tested and verified according to the target requirements.

1.3 Research objectives and contributions

The RF integrated transmitter section of a power-efficient bidirectional communication front-end in the implantable side (Figure 1.5) is the target of this research. The transmitter section has to be carefully and separately investigated and implemented such that it is able to efficiently communicate with its external counterparts.

The goal of this research is to design and implement a binary Frequency-Shift-Keying (FSK) based integrated wireless transmitter section of the target transceiver, such as in Figure 1.6, operating at North American ISM frequency band with center frequency of 915 MHz. The main objectives for designing such RF transmitter are low-power consumption, high data-rate and small silicon area, as addressed in this thesis.

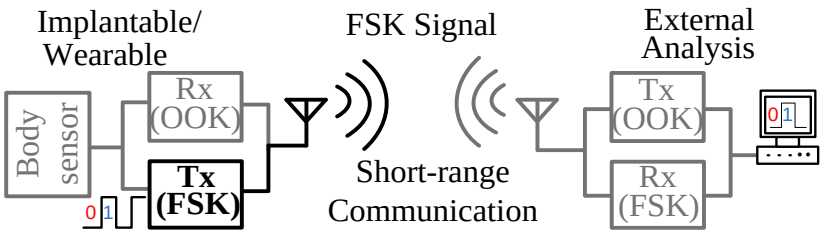


Figure 1.5: Target FSK transmitter in the communication front-end

In this project, a new FSK modulation scheme is introduced and developed using the basic modulation principles and the mathematics background. Reduction in total current consumption was the first advantage of the presented architecture and the corresponding block

diagram and initial implementation simulation results were published in a conference, CCECE 2011, titled as "*A New FSK-based Transmitter Dedicated For Low-Power Wireless Medical Transceivers*" [28].

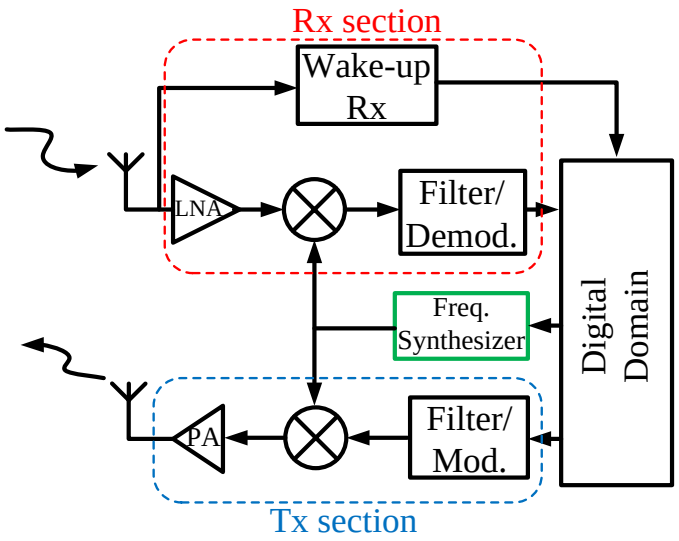


Figure 1.6: General architecture for RF transmitters and receivers

The proposed transmitter architecture was implemented and optimized for high data-rate performance and the post-layout simulation results were published in a second conference paper, ICECS 2012, titled as "*A 20 Mb/s 0.084 nJ/bit ISM-band Transmitter dedicated to medical sensor networks*" [29]. The performance of the presented transmitter and its characteristics were also published in NEWCAS 2013, titled as "*A 0.084 nJ/b FSK Transmitter And 4.8 μW OOK Receiver For ISM-band Medical Sensor Networks*" [30].

The proposed FSK modulation scheme and the corresponding transmitter architecture were further investigated and characterized. The alternatives for applying the modulation block as well as the sensitivity over phase and amplitude discrepancies were studied.

The circuits of the composing building blocks of the proposed transmitter architecture are adopted, designed and optimized towards low-power, high data-rate integrated transmitter. A new quadrature voltage controlled-oscillator (QVCO) was implemented to provide differential rail-to-

rail quadrature signals with tunable frequency from 300 kHz to 11.5 MHz with very small current consumption of 0.5 to 160 uA, respectively. This QVCO is in important building block in the proposed transmitter architecture to avoid additional external reference frequency. The interesting design point for this oscillator is the frequency of 2 MHz with current consumption of 5.5 uA. The results were published in the IET Electronics Letters, titled as "*A New Differential Rail-To-Rail Voltage-Controlled Quadrature Ring-Oscillator For Low-Power Implantable Transceivers*", 2014. Moreover, as an alternative frequency tuning range, the proposed QVCO oscillates at a frequency varying between 3 and 40 MHz with a current consumption of 3 to 117 uA, correspondingly. The related results are summarized and reported in chapter 5 of this thesis.

The layout of the designed transmitter was implemented for fabrication using the 130 nm CMOS technology to test and confirm the performance. Thanks to high frequency measurement setup, the experimental results were compared with state-of-the-art and similar related RF transmitters. The implemented transmitter prototype provided a data-rate of up to 8 Mb/s with 2.13% average FSK error while consuming 1.4 mA from a 1.2 V voltage supply and relatively small active silicon area of 0.25 mm^2. The achieved measurement results were submitted to a journal paper, Analog Integrated Circuits and Signal Processing, titled as "*An Energy-Efficient High Data-Rate 915 MHz FSK Wireless Transmitter for Medical Applications*", 2014. The related simulation and measurement results as well as the developed test-setup are reported in chapter 5.

1.4 Thesis outline

In Chapter 2, the two widely-used data modulation schemes for low-power transceivers, FSK and On-Off-Keying (OOK), as well as two main transmitter architectures, Direct-Conversion and Two-Step, are reviewed and compared. A technical overview of low-power RF transceivers is presented. The transceivers are intended for the communication interface of medical implants where the size, power consumption and data-rate are the main challenges. The focus is narrowed down to integrated transmitters operating at ISM frequency band (915 MHz) and the design constraints and parameters as well as Figure-Of-Merit (FOM) are discussed.

In Chapter 3, a new efficient FSK modulation scheme is introduced and corresponding mathematical equations are presented towards realizing the block diagram of the target

transmitter. Characteristics and behaviour of the proposed modulation scheme, such as sensitivity, is then discussed. Finally, the proposed transmitter architecture is presented.

In Chapter 4, the building blocks in the proposed transmitter architecture are implemented in circuit- and layout-level. Alternative design and implementation choices for each block and their behaviour are briefly discussed. A novel low-power rail-to-rail differential QVCO, which can be tuned in different frequency ranges, is introduced and implemented. Special attention was paid to design the output stage of the transmitter, the Power Amplifier (PA), including its optimization. The final layout of the fabricated transmitter is also presented.

Post-layout simulation and measurement results of the integrated QVCO and the energy-efficient RF transmitter are presented in Chapter 5. Different parameters of the implemented QVCO and transmitter are investigated in simulation and measurement. The achieved performance of the proposed transmitter in this work is then compared with State-Of-The-Art showing the improvement in size, power consumption, data-rate and FOM.

Summary and conclusion of this dissertation are brought in Chapter 6, where the contributions of the overall work are outlined and benefits of this work are discussed. The possible future work is then discussed and a few related circuits are recommended to be designed and implemented.

In the Appendices, the related system-level test-bench and layouts of the implemented QVCO are shown.

CHAPTER 2

LOW-POWER ISM-BAND RF TRANSMITTERS: A REVIEW

2.1 RF transmitters in medical applications

As mentioned earlier, implantable wireless Microsystems for human bodies may be used to detect and transfer different information such as Oxygen level of the blood for treatment of different diseases [31]. Low-power CMOS RF transmitters have been always an interesting challenging research topic, such as the 915 MHz transmitter [32] published in 1996 with up to 160 kb/s and relatively large power consumption. The reported ISM-band low-power transmitters and their energy efficiencies are discussed in the following section. As a recent example of body implantable devices, a CMOS transceiver is presented in [33] for telemetry services. In [33], the transmitter side communicates at 400 MHz frequency range with a data-arte of 500 kb/s with an output power of -2.87 dBm while consuming 22 mW which is relatively high. The corresponding energy consumption is 44 nJ per transmitting bit. The power consumption has to be reduced by using less complex circuits or by improvement in data-rate which is directly affected by the architecture and the employed modulation. As another example, the Bluetooth module of [34] is produced in 2013 for communication with a data-rate of 186 kbps and energy efficiency of 13 nJ/b. Alternatively in [35], the battery-powered and wirelessly-powered RF body sensors are reported to be useful for monitoring of temperature and blood behaviour, for example, but the data-rate of the emerging methods is around 100 kb/s with a short period of operating time. In total, the goal is to come up with an energy-efficient communication front-end which consumes low power for transmitting each bit of data.

New medical experiments such as monitoring a given animal's activity is feasible with light and tiny medical devices, such as battery-free RFID sensing tags on freely-behaving insect and small animals in [36] and [37]. Experiments on freely-moving rats are also very interesting where the micro-size integrated sensors are promising. For example, the telemetric system for recording EEG activity in freely-moving rat in [38] uses an implantable transmitter which communicates a sampling rate of 500 b/s with the external receiver via radio transmission over a short distance (less than 3m) similar to Figure 2.1. In this system the data-rate is reported 115.2

kb/s when 1.6 mA is drawn from two batteries of 1.55 V (~ 5 mW) for only 14 hours of measurements.

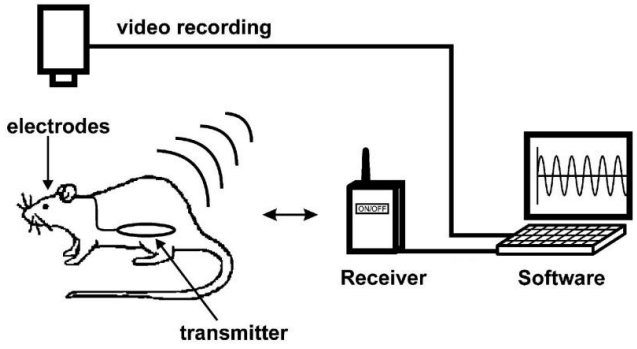


Figure 2.1: Continuous monitoring of freely-moving rats using implanted transmitter [38]

2.2 Case studies of low-power 915 MHz transmitters

In this section, the main FSK-based ISM-band transmitters are reviewed and studied. The state-of-the-art transmitters from literature, simulated and fabricated using CMOS technology, are summarized. The target range of current consumption is around 1 mA and the typical supply voltage is between 1.2 and 1.8 V depending on the used technology and the circuit design. Moreover, a few off-the-shelf transmitter chips are also reviewed to understand the level of performance in the market.

Comparing customized integrated RF transmitters is not an easy task due to the fact that each one is designed and optimized for a specific application with specific power level or frequency range and bandwidth. Consequently, similar designs with similar specifications have to be investigated to have a fair comparison.

Figure 2.2 shows the power consumption of recent low-power 915 MHz binary FSK transmitters. Each of the mentioned transmitters in this graph is discussed in the following as well as other related transmitters. In this figure, the trend in power consumption and data-rate is summarized while the dashed lines shows the constant lines of consumed energy per transmitting bit. Other concerning parameters, such as size, simplicity and suitability for implantable medical devices, are also discussed in the following sections. Also, notice that the technical overview on the performance of the related ISM transmitters brought in this dissertation is actually based on

what the authors have reported in their work. Not everyone reports and discusses all parameters in their published work and, therefore, important parameters are basically discussed here. In addition to the absolute value of current consumption, simplicity and size, the main focus is to compare the commonly-used FOM of the low-power ISM band transmitter, which is the consumed energy per transmitting bit (J/b).

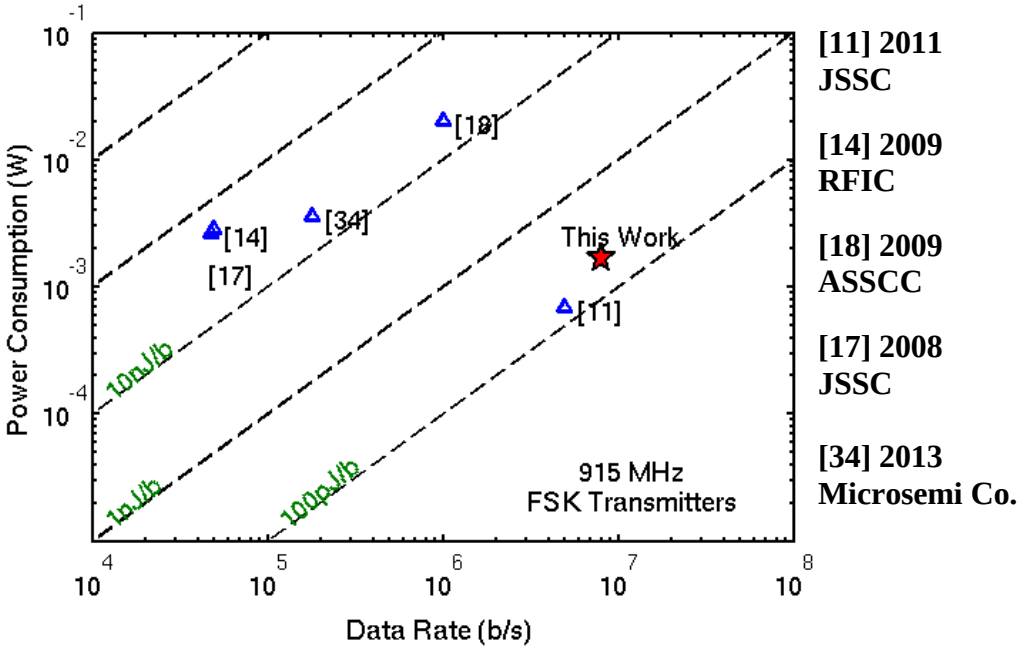


Figure 2.2: Trend in recent energy-efficient binary FSK 915 MHz transmitters

One of the best reported transmitters was published in the JSSC [11] in 2011, which is an energy-efficient 915 MHz FSK-based transceiver for wireless body sensor network (BSN) applications. It is implemented in 0.18 um CMOS technology with 0.7 V supply. The architecture is based on injection-locked frequency divider (ILFD) for the low-energy consumption. In the receiver, the ILFD in the signal path converts the received FSK signal to amplitude-modulated signal which is applied to the next envelope detector. In the transmitter, the ILFD is used as digitally-controlled oscillator (DCO) which directly modulates the FSK signal with digital data. This is, indeed, one example of sharing components in both receiver and transmit path to reduce the total needed chip area. Also, the DCO is claimed to replace the frequency synthesizer to

eliminate the crystal oscillator to reduce power consumption and cost. The active chip area is around 0.35 mm^2 while 5 off-chip inductors are used. The transmitter consumes 700 uW at -10 dBm output power with a data rate of 5 Mb/s, resulting in the energy consumption of 0.14 nJ per transmitted bit. The transmitter efficiency of 15 % is reported when the output power is set to -10 dBm. The 5 MHz bandwidth is used to provide a data-rate of 5 Mb/s with the modulation index of 1.

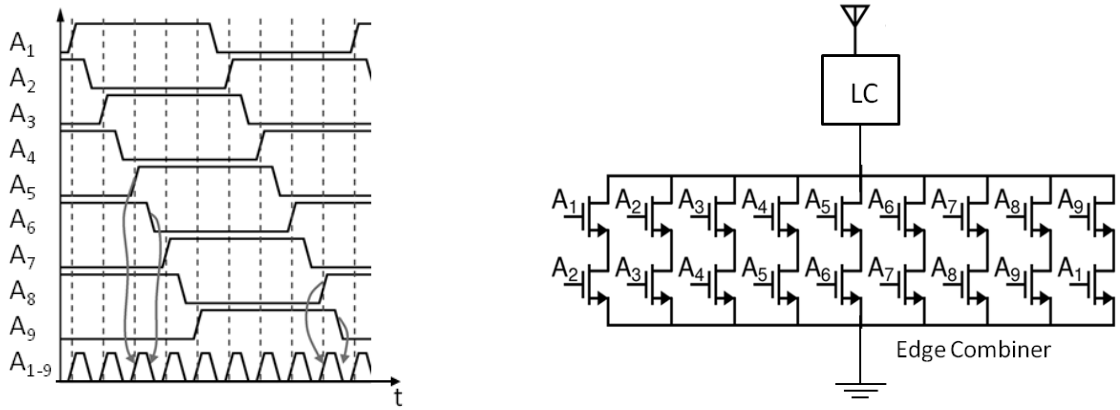
The reported current and energy consumption is one of the best leading designs in the literature; however, there are still few issues to consider. The transceiver has to detect whether injection locking occurs or not, and needs to calibrate the frequency drift of DCO over temperature variation. The calibration process requires a complicated additional circuitry where a frequency bandwidth of 5 MHz is necessary. This is actually not vey suitable when many channels are needed for narrowband RF communication. Moreover, three different LC tanks for matching, harmonic filtering and oscillation are needed in the transmitter path in addition to the capacitor bank which is used to tune the desired frequency.

In total, the published architecture has shown good performance in terms of data-rate and energy efficiency. The total current consumption and, hence the energy consumption are low in spite of the need for 5 off-chip inductors for higher quality factor and the required process of calibration. In other words, the required area needs to be reduced to make it more suitable for implantable devices where frequent surgeries for calibrations are not feasible.

Similarly, an ultra low power 400 MHz transmitter also uses FSK as the modulation scheme and its oscillator requires being periodically calibrated [39]. In practice, it is claimed that a ring-type oscillator has been considered instead of LC-type as it reduces the buffer's power consumption immediately following the oscillator. A switch is used in order to disconnect the frequency calibration unit and to turn on the PA after the channel frequencies have been calibrated. According to simulation results, the transmitter is claimed to work from a data rate of 250 kb/s to 1 Mb/s. It draws an average current of 180 μA from a 1.6V supply to provide an output power of -16 dBm achieving a very low current consumption for a transmitter designed at the 400 MHz band and allowing for multichannel operation. The transmitter is not tested yet and the inductor is off-chip with very high quality factor of 50 in the simulations.

The minimum required power for transmission is generally a function of the operating frequency and distance as well as receiver sensitivity and losses of the path. As reported in [24], for a transmission range of about 2 m, a 1 GHz communication system requires about -18 dBm of transmission power with a sensitivity of -60 dBm in the receiver side. Also, according to the modeling and optimization methods for different carrier frequencies shown in [40] an optimal transmission frequency and antenna size can be found such that a 1 Mb/s of data-rate over a 1-m wireless link with a transmitter power consumption of 10 uW is achievable which is very much challenging to realize. In [40], the power consumption for two data-rates of 10 kb/s and 1 Mb/s is studied and it is also shown that the difference in needed power consumption for the two data-rates is much larger at higher frequencies of 2.4 and 5 GHz comparing with 400 and 915 MHz. In other words, for data-rate communication, the needed power consumption at higher frequencies (2.4 and 5 GHz) is much larger than that at lower frequencies (sub-1 GHz). As a result, in spite of the smaller antenna size for higher frequencies, sub-1 GHz frequencies are more common as the carrier frequency of the communication front-ends in low-power applications.

The BFSK-based transmitter in published in JSSC, 2011, which has injection-locking oscillator, has lowered the output power to -17 dBm (20 uW) with 22% transmitter efficiency to achieve the energy efficiency of 0.45 nJ/b with a data-rate of 200 kb/s [13]. In this transmitter, the injection-locking oscillator generates low-frequency signals of $A_{1\text{-}9}$ in Figure 2.3a and the edge-combiner circuit of Figure 2.3b combines the received pulses to generate the high-frequency signal in the output node before the LC matching circuit. The nine received phases from the oscillator are, in fact, combined to generate the 400 MHz output frequency. The edge-combiner is acting as a multiplier, indeed. In this way, the high-frequency node is shifted toward the antenna.



(a) (b)

Figure 2.3: The frequency multiplication used in [13]: (a) $A_{1\text{-}9}$ phases from the oscillator and (b) schematic of the edge-combiner to multiply the frequency by 9

The maximum data-rate in this work is dependent on the behaviour of the employed external Crystal oscillator. In practice, a part of the loading capacitor of the Crystal oscillator is switched on and off using the input digital data to distinguish between data '1' and '0'. The switching time for this capacitor is limited and cannot provide a high data-rate. Also, the value of the loading capacitance is also limited and cannot have a wide frequency tuning range. Moreover, for 915 MHz frequency generation the number of transistor branches is doubled and more mismatch and harmonics will be introduced. In total, the power consumption is reduced significantly.

In some transmitters, the baseband data is used to directly control the behaviour of the transmitter. The transmitter published in [12] (ISSCC 2013) is a multichannel one that supports different FSK modulations to provide up to 5 Mb/s for high-bandwidth channels. In this 400 MHz transmitter, the baseband data is used to directly control the synthesizer inputs using a pulse-shaping filter and it achieves various FSK modulations, such as BFSK and Gaussian FSK (GFSK). In GFSK, the baseband waveform passes through a filter to smooth the transitions and limit the spectral width. Off-chip matching network is used to improve the output efficiency. The reported BFSK error for this work is about 12% when the data-rate is 5 Mb/s with modulation

index of ~0.5. The produced output power is -8 dBm when 2.35 mA is consumed. The related FOM for this work is 0.11 nJ/b and it is considered as one of the best energy-efficient 400 MHz multichannel transmitters.

The low-power FSK transmitter presented in [41] uses a direct VCO modulation scheme where the LC-based VCO is directly modulated to change the tank capacitance. It is dedicated for body area network applications with carrier frequency of 2.4 GHz. The FSK synthesizer consumes 600 μW. A few buffers drive the power amplifier (PA) where the output stage is a differential class-E stage and a differential transformer is required for antenna matching resulting in a large consumed area. The load impedance seen by the PA is 840 Ω and an integrated step-up transformer is used to up-convert the antenna impedance. The circuits are integrated in a 0.13-μm CMOS technology. The overall transmitter consumes 8.9 mA to deliver +1.9 dBm to the antenna with a total power efficiency of 17.4%. The reported RF output power of -5.7 dBm with power efficiency of about 7% in this work is due to the current of 3.7 mA from 1 V supply. The data-rate is reported 1 Mb/s resulting in the FOM of 3.7 nJ/b. The FSK modulation index for this work is also 0.5±10% and the FSK error is not reported. In total, the proposed direct VCO modulation technique is proved to be novel, simple and functional; however, the total current consumption is high which makes it not suitable for implantable devices.

Several transmitters in literature with relatively larger current consumption are also notable to understand the range of concerning parameters in non-recent transmitters. For example, 14 mA is drawn from a 2.7 V supply in the 915 MHz BFSK transmitter of [42] (reported in 2003) to provide 0 dBm of output power and 115.2 kb/s data-rate with an energy efficiency of 328 nJ/b. The size of the chip is also reported 5.4 mm^2 using 0.35 um technology which is relatively large. Similarly, the large current of 32.3 mA from 1.2 V supply in [43] (reported in 2005) gives an energy efficiency of 387 nJ/b when the data rate is 100 kb/s with FSK modulation index of 2. Also, in the off-the-shelf BFSK 915 MHz transmitter chip of [44] (reported in 2006), a data-rate of 76.8 kb/s with modulation index of ~1.7 is reported. In this chip, 8.6 mA is consumed to provide an output power of -20 dBm giving an energy efficiency of ~335 nJ/b. As another example, the 900 MHz transmitter in [19] (reported in 2007) consumes 16 mA from a 1.8 V supply to provide an output at 0 dBm. The reported FSK error is 6.3% for 40 kb/s data-rate resulting in an energy efficiency of 720 nJ/b. The die size is also reported 2.16 mm^2 using 0.18 um CMOS technology.

Several ISM-band transmitters are available in the market and each one has its own specifications in terms of current consumption and data-rate. A few of the related low-power ISM-band integrated transmitters are summarized and compared here. In general, the commercial transmitters have many supporting blocks and features, such as control units for programmable outputs, selectable modulations, ADCs, integrated switches, power management blocks, etc. Therefore, the range of reported current consumption in the data-sheet of these products is usually higher unless specified.

Table 2.1 summarizes the specifications of the transmitter section of the selected related off-the-shelf ICs. Notice that the reported values in this table are due to the FSK-mode performance of the transmitter sections. As predicted, the total power consumption of these transmitters is relatively large and, hence, the Figure-Of-Merit (FOM), which was defined as consumed Energy per transmitting bit (J/b), remains large. In practice, FOM is calculated by dividing the DC power consumption ($VDD \times I_{DC}$) by the data-rate. As highlighted in Table 2.1, only the integrated circuit of ZL70250 [34] has a relatively small current consumption resulting in the best and lowest FOM of 19.35 nJ/b. For this case, FSK modulation is used to provide the data-rate of 186 kb/s and modulation index of ~0.5.

The presented FSK transmitters in Table 2.1 operate at 915 MHz. However, the off-the-shelf transmitters in 400 MHz range have similar performance. For example, the 433 MHz version of the integrated chip, ZL70101 [45] can provide up to 256 kb/s data-rate with 5 mA current consumption and 35 nJ/b of energy consumption. Also notice that the commercialized integrated circuit are likely to use higher voltages (~3 V) for the supply for more compatibility with other chip such as the microcontroller. This is another reason why the total power consumption is still high. In the integrated transmitter circuit of TRC103 produced by Murata Co. [46], both OOK and FSK modulations are used to provide up to 200 kb/s of data-rate and up to +11 dBm transmit power from 3.6 supply voltage.

As shown in Table 2.1, the range of the reported data-rates are less than 500 kb/s which is mainly due to the general requirement of applications. More importantly, the reported current consumptions are very large that is an interesting research area. Speaking of low-power implantable devices, a low-power RF transmitter is consequently required.

Table 2.1: Summary of selected off-the-shelf low-power integrated ISM-band (915 MHz) transmitters

IC [Ref] (year)/ Company	Modulation	Maximum Data-Rate	Tx Current/ VDD	FOM Energy/bit (nJ/b)	Output power	Related Applications
TRC103 [46] (2012)/ Murata	OOK/FSK	200 kb/s	– /3.6 V	-	> 11 dBm	- General Applications
AT86RF212 [47] (2010)/ ATMEL	BPSK	40 kb/s	17 mA/3.6 V	1530	5 dBm	- General Applications
	QPSK	200 kb/s		306		
ZL70250/70101 [34] (2013)/ Microsemi	FSK (MI:~0.5)	915 MHz: 186 kb/s	2 mA/1.8 V	19.35	-13 dBm	- Body-Area Network - WSN
		433 MHz: 400 kb/s	5 mA/2.8 V	35	-4.5 dBm	
ADF7020 [48] (2012)/ Analog Devices	FSK/GFSK	200 kb/s	14.8 mA/3.6 V	266	-20 dBm	-Low cost wireless data transfer
CC1150 [49] (2009)/ Texas Inst.	BFSK/GFSK/MSK	500 kb/s	15.2 mA/3 V	91	0 dBm	- Low power telemetry - WSN
MICRF405 [50] (2006)/ Micrel	ASK/FSK	200 kb/s	9.6 mA/3 V	144	-7 dBm	- Remote control systems - Wireless security systems

One common way to reduce the current consumption and area is to share few blocks in the architecture of the transceiver as is reported in literature. An example of sharing building blocks is the energy-efficient transmitter-receiver of [51]. A configurable and energy-efficient transceiver architecture is introduced in [51], 2009 and is operating at 2.4 GHz using PSK modulation. Active mode power consumption is reported to be 11 mW and 14 mW in receive and transmit modes, respectively, on a 1.6 V supply in 0.18 μm technology. In this transceiver, in addition to the mixer, the LNA circuitry is also shared for both transmission and reception. The

transceiver is designed for the short range wireless sensors but complexity of the proposed structure is still one of its drawbacks. In this work, the LNA is used in a loop such that it also functions as the VCO for both paths, Tx and Rx. However, the loop and the total Rx/Tx paths are still complicated and many blocks are involved. Moreover, the number of on- and off-chip inductors makes it not fit for implantable devices.

Another example in which the LNA and the PA stages are reconfigurable to save silicon area is reported in [52]. In this work, the LNA and PA stage are combined to realize a reconfigurable antenna interface. The transmitter uses BFSK modulation with modulation index of ~1 to provide 100 kb/s of data-rate while consuming 1.6 mW to produce an output power of -5 dBm. The energy consumption then becomes 28 nJ/b. Notice that a differential transformer is used in addition to the inductor of the LC tank and more area is consumed. In total, the presented transmitter has shown a fairly efficient performance as a result of trade-off between power consumption, data-rate and silicon are.

Simplicity of the architecture directly leads to a high performance transmitter if the blocks are carefully optimized and implemented. For instance, the transmitter in [20] is implemented using 0.5 μm CMOS technology and uses direct-conversion architecture. It operates at 434 MHz frequency band and uses FSK modulation to maintain a data-rate of 25 kb/s. The initial proposed Tx architecture seems to be very simple as shown in Figure 2.4, but, the complexity of each block is a disadvantage.

In this transmitter, the I/Q signals with the deviation frequency are determined by a digital baseband modulator based on an analog oscillator circuit and the absolute value of the frequency is controlled by the Δf Ctrl signal. When the input data changes, the settling time for the new deviation frequency may limit the data-rate. This modulator has several blocks, including several OTAs and active mixers resulting in a large required chip area. The reported power consumption is 0.5 mW for an output of 10 dBm with overall efficiency of 38% from a 1.2 V supply voltage. Also, the power amplifier is composed of three-stage class-A preamplifiers with 7 mW power dissipation and an output class-B stage with 8 mW power dissipation. Moreover, the matching circuit is realized using off-chip inductors and capacitors.

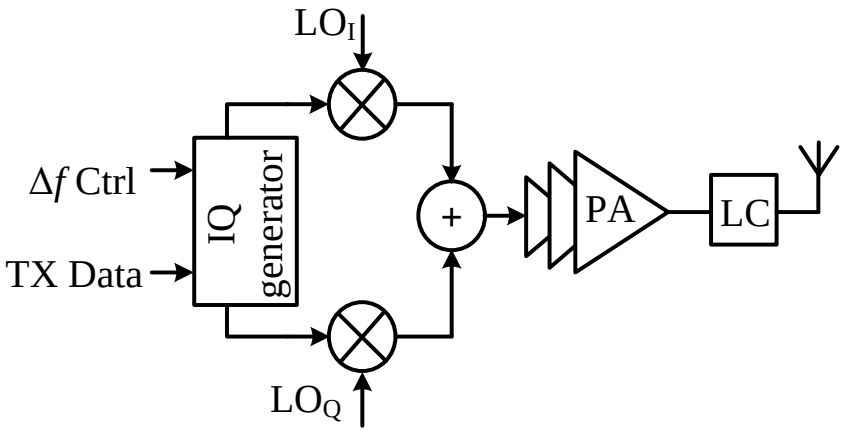


Figure 2.4: Simplified FSK-based Tx diagram reported in [20]

In total, the presented Tx architecture is simple but requires a large area and the complexity of several blocks has increased the total power consumption to 25 mW which makes inappropriate for low-power implantable applications. It is shown later in the following chapters and the proposed transmitter architecture benefits from its simplicity while the building blocks are implemented with less complexity to lower the total current and area.

The BFSK transmitter in [14] operates at 868/915 MHz and was implemented using 0.13 μm CMOS technology in 2009. Zero-IF architecture is used to implement the transceiver. The simplicity in [14] is an advantage where the number of blocks (Figure 2.5) is low and, hence, the current consumption is supposed to be at a low level. However, an additional block of divide-by-2 is used to divide the output frequency from the synthesizer and to bring it to 915 MHz. Binary FSK modulation is used to realize a 45 kb/s data-rate. In total, the reported current consumption of the transmitter is 1.8 mA from a 1.5 V supply voltage to generate an output of -6 dBm. The power amplifier is a class-AB which is reported to be very suitable for low-power output, but, it requires three different supply voltages in addition to several resistors and capacitors.

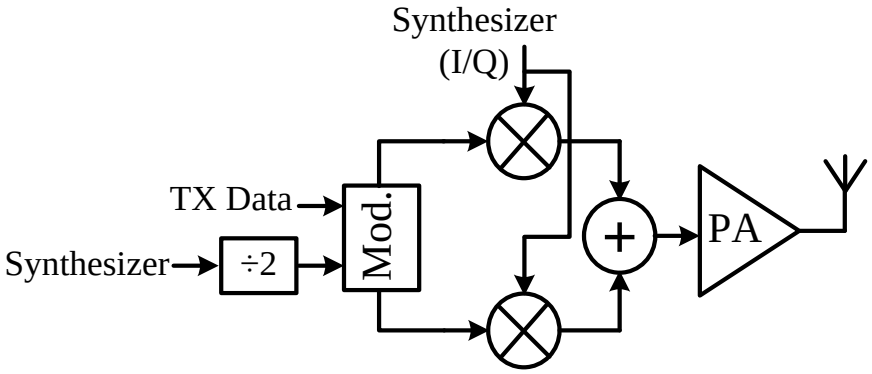


Figure 2.5: Simplified TX architecture in [14]

One of the most interesting circuits in [14] is the modulator circuit which is implemented using digital circuits, as shown in Figure 2.6. In this configuration, the TX data, the quadrature signals with deviation frequency and the quadrature signals from the synthesizer are the inputs. The TX data chooses between the I and Q signals with the deviation frequency to get mixed with the LO signals through multiplexers. The output FSK signal is generated through the logic gates. In this modulator, multiplication is replaced by an XOR function while the summation function is replaced by AND/NOR functions. However, the current consumption is 110 μA. The output frequency is $f_{LO}+\Delta f$ for Tx D='1' and $f_{LO}-\Delta f$ for Tx D='0'.

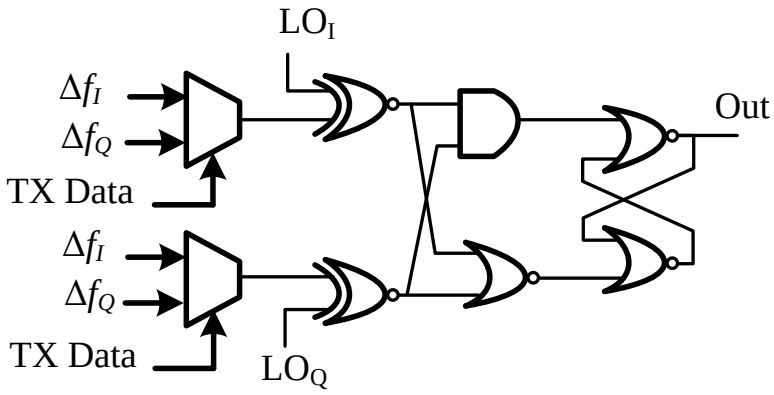


Figure 2.6: The digitally implemented modulator in [14]

The current consumption of this modulator in addition to the PA stage is reported as more than 1.14 mA. The maximum overall efficiency of the PA stage is 32.4 % when delivering -4 dBm. However, the digital FSK-modulator is claimed to be functional but has sub-optimum performance when combined with the PA. In total, using digital components has reduced the total power consumption and the transmitter is implemented with a simple architecture. In the following chapters, a proposed FSK modulation scheme is implemented with small current consumption where the main modulation block consumes no DC current.

Reviewing all the mentioned ISM-band transmitters, it is notable that implementing an energy-efficient transmitter suitable for implantable and wearable devices has many issues to address, more importantly current consumption, data-rate and chip area. As a result, a new RF transmitter is proposed to realize the wireless communication interface of medical devices. This transmitter is the subject of next chapters.

2.3 Summary

Medical application of RF transmitters for human-machine interactions and freely-moving animals were discussed. A technical overview on several related published low-power ISM-band transmitters for short-range communication was given while focusing on their performance in terms of size, power consumption, maximum data-rate and, in total, energy efficiency. Several related low-power off-the-shelf components were also listed and their performances were compared in spite of higher level of needed power consumption.

The strength of the presented transmitter in this work is the energy efficiency to provide a high data-rate, simplicity of the employed FSK modulation and the small size. Moreover, low complexity is a benefit when the low-power transmitter circuit is implemented. The proposed FSK modulation scheme and the corresponding architecture are presented in the next chapter.

CHAPTER 3

PROPOSED BFSK 915 MHZ TRANSMITTER

3.1 Target ISM-band transmitter

This transmitter is a part of a bidirectional target transceiver operating at the license-free North American Industrial-Scientific-Medical (ISM) frequency band (902-928 MHz) and as the communication front-end. It is dedicated to wireless interface of medical body sensors to avoid using discrete external off-the-shelf components and shrink the total size of the sensor. The center frequency of 915 MHz is usually used to address this frequency band. Other frequency bands may also be used in other regions with their own design constraints, such as antenna restrictions or availability of frequency bandwidth. However, the circuits may be redesigned for other frequency bands, such as European frequency band (434 MHz) with less available bandwidth or worldwide frequency band (2.4 GHz or 5.7 GHz) with circuits with generally higher power consumption and more sensitive to parasitic components.

Performance of any wireless transmitter as a power-hungry communication front-end is significantly dependent on the employed modulation. More importantly the power consumption and data-rate can be improved by careful selection of the signal modulation while meeting other design constraints such as area, simplicity, and integration. Both transmitter and receiver circuits of the target transceiver are to communicate in the mentioned frequency band with a limited bandwidth with high data-rate and low-power characteristics. In general, some blocks can be shared to minimize the power and area, such as the local oscillator (LO). In the target transceiver, the high quality LO's In- and Quadrature-phase (I and Q) signals are generated by a very low-power fully integrated integer-N frequency synthesizer which was previously implemented and reported in [53]. It is designed to allow the selection of different channels equally spaced in the 902–928 MHz ISM frequency band while offering differential, quadrature versions of the carrier. It consumes 600 µA from 1 V supply while showing good phase noise immunity, large tuning range and fast settling time.

The proposed transmitter in this work benefits from an efficient FSK modulation scheme which has the main advantages of being a high data-rate, low-current design with small needed

area. It is shown in the following sections how the required signals with the frequencies corresponding to the transmitting data are produced and results in high data-rate communication. The corresponding circuit implementation allowed realizing the transmitter with low-power consumption.

3.2 Proposed FSK modulation scheme

The modulation principle of a binary FSK modulation is shown in Figure 3.1. The signal spectrum gets shifted up and down to distinguish between data '1' and '0', respectively. Indeed, data='1' is realized by shifting the center frequency to f_c+f_s and data='0' is realized by shifting the center frequency to f_c-f_s. Here, f_c is considered as the center frequency while f_s (or Δf) is the shifting frequency (or deviation frequency).

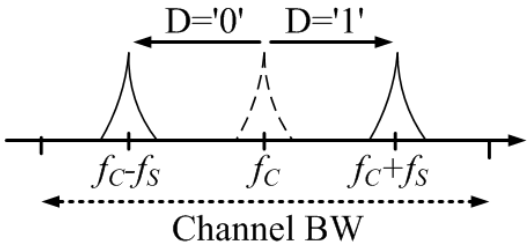


Figure 3.1: FSK modulation principle

In this research, the FSK signals are generated using the mathematical trigonometric equations towards realizing the final simplified equations.

In the first scenario, consider the trigonometric signals with frequency of f_c+f_s, meaning $cos(\omega_c t + \omega_s t)$ and $sin(\omega_c t + \omega_s t)$, as shown in Eqs. (3.1) and (3.2).

$$cos(\omega_c + \omega_s)t = cos(\omega_c t)\, cos(\omega_s t) - sin(\omega_c t)\, sin(\omega_s t) \tag{3.1}$$

$$sin(\omega_c + \omega_s)t = sin(\omega_c t)\, cos(\omega_s t) + cos(\omega_c t)\, sin(\omega_s t) \tag{3.2}$$

Combining the above equations Eq. (3.3) can be obtained. The sinusoidal terms in Eq. (3.3) are then replaced by the following terms in Eq. (3.4).

$$V_{f_c+f_s} = \sqrt{2}\left\{sin(\omega_c t)cos\left(\omega_s t + \frac{\pi}{4}\right) + cos(\omega_c t)sin\left(\omega_s t + \frac{\pi}{4}\right)\right\} \quad (3.3)$$

$$V_{f_c+f_s} = V_{f_c,Q} \times V_{f_s,I} + V_{f_c,I} \times V_{f_s,Q} \quad (3.4)$$

In the above equations, $V_{f_c,I}$ and $V_{f_c,Q}$ are the In- and Quadrature-phase (I and Q) signals with frequency of f_c (the frequency of the local oscillator) and $V_{f_s,I}$ and $V_{f_s,Q}$ are the I and Q signals with frequency of f_s (the shift frequency or deviation frequency). It is worth remarking that as long as the sinusoidal terms with frequency of f_s keep the 90 degrees phase-shift they will be considered as I and Q signals and, in other words, the $\pi/4$ delay for both terms in Eq. (3.3) can be ignored when generating the signals. The factor of $\sqrt{2}$ is not also the concern at this step.

Similarly, in the second scenario, the signal with frequency of f_c–f_s can be produced by changing ω_s to $-\omega_s$ in Eq. (3.3) resulting in Eq. (3.5).

$$V_{f_c-f_s} = \sqrt{2}\left\{sin(\omega_c t)Cos\left(\omega_s t - \frac{\pi}{4}\right) - cos(\omega_c t)Sin\left(\omega_s t - \frac{\pi}{4}\right)\right\} \quad (3.5)$$

Notice that in this equation the sinusoidal terms containing f_s are still I and Q signals with 90 degrees phase difference. Therefore, one can simply replace terms similar to Eq. (3.4) to obtain the output signal with frequency of f_c–f_s, which is shown in Eq. (3.6).

$$V_{f_c-f_s} = V_{f_c,Q} \times V_{f_s,I} - V_{f_c,I} \times V_{f_s,Q} \quad (3.6)$$

It can be seen that the only change in the output generated terms containing frequency of f_c+f_s and f_c–f_s is that one of the signals, here $V_{f_c,I}$ or $V_{f_s,Q}$, changes its sign. In other words, the polarity of the mentioned signal is inverted, when differentially implemented. Therefore, the output generated frequency can be switched between f_c+f_s and f_c–f_s, the two desired FSK frequencies. Indeed, the negative sign can be applied to any of the sinusoidal terms. It can even be applied to the product of the two signals before the sum operation. However, in this work,

changing the polarities of a signal with frequency of f_s was considered for applying the negative sign summarizing all the equations to Eq. (3.7).

$$V_{out} = V_{f_c \pm f_s} = V_{f_c,Q} \times V_{f_s,I} + V_{f_c,I} \times (\pm 1) \times V_{f_s,Q} \tag{3.7}$$

The block diagram of the above obtained simplified equation is realized in the following towards realizing the proposed transmitter architecture.

3.3 Proposed Transmitter Architecture

3.3.1 Block Diagram

The simplified equation to generate the desired FSK signals, Eq. (3.7), consists of the sinusoidal terms, sum and multiplication operations. Figure 3.2 shows the conceptual block diagram of the mentioned equation. The sinusoidal terms are the inputs, the multiplication and sum operations are realized by mixer and adder, respectively.

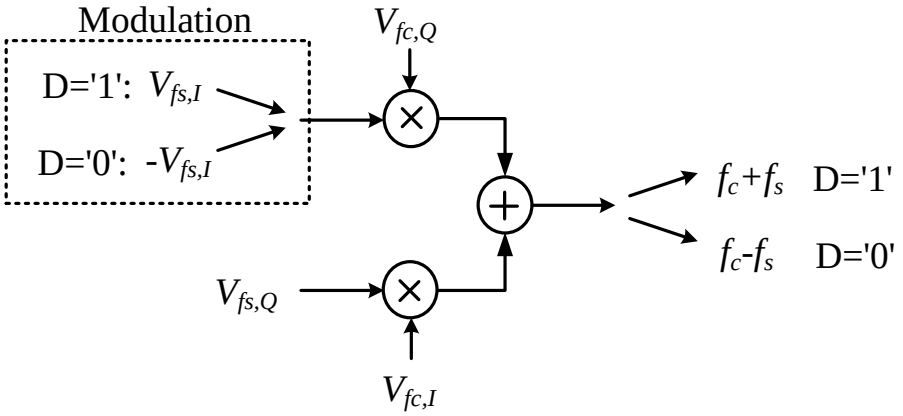


Figure 3.2: Conceptual diagram of the proposed FSK Modulation

In practice, the signals are usually implemented differentially to lower the noise and avoid third harmonic distortions, especially for high-frequency circuits. The adder is usually followed by an amplifier, here called Power Amplifier (PA), to increase the signal amplitude to a higher level in order to avoid mixing the generated desired signal with the unwanted distortion generated by

other surrounding instruments. Figure 3.3 shows a more complete diagram of the proposed FSK modulation. $V_{f_c,I}$ and, $V_{f_c,Q}$ the I and Q signals from the Local Oscillator (LO) are renamed as LO-I and LO-Q, respectively, to easily distinguish between the carrier signal and the one with the deviation frequency. The modulation block, which is controlled by the input data, has the task of changing the polarities of its input, here $V_{f_s,I}$, in order to switch between the two desired scenarios, as mentioned earlier. The PA is also controllable by V_{ctrl} to adjust the output amplitude and current consumption.

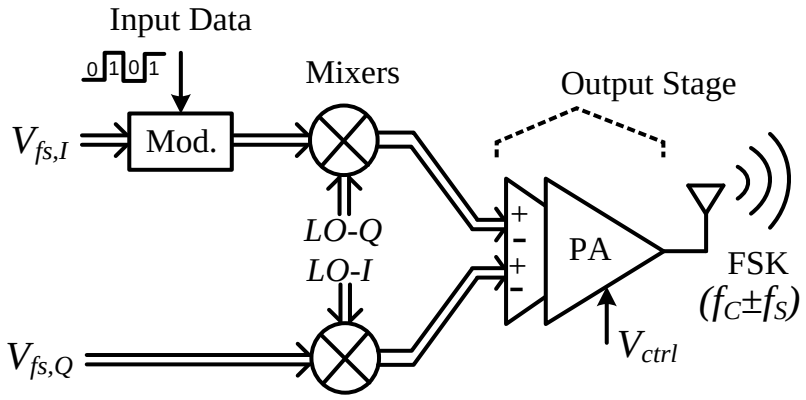


Figure 3.3: Simplified diagram of the proposed transmitter architecture

As a result, changing the polarities of only one of the signals is interpreted as changing the transmitting data from '1' to '0' or from '0' to '1' and the short needed switching time helps increasing the data-rate. This, in fact, is one big advantage of the proposed modulation technique which results in high data-rate and is another major contribution of this work in addition to the reduction in power dissipation and size. Notice that the proposed transmitter is different from conventional ones in principles and achieved performance and the simplicity of this design makes it very suitable for implantable and wearable medical devices.

Figure 3.4 shows the global block diagram of the proposed BFSK-based transmitter architecture. In this architecture, the signals containing the deviation frequency are provided by an integrated low-power differential QVCO, when enabled by EN signal. Alternatively, the Poly-Phase Filter (PPF) stage is used to generate the required I and Q signals. Both integrated and external choices to provide the signals with frequency deviation ($V_{f_s,I}$ and $V_{f_s,Q}$) were considered.

The poly-phase filters itself can also be on- or off-chip. Notice that all signals are differential except the output of the PA stage, which goes the 50-Ohm antenna.

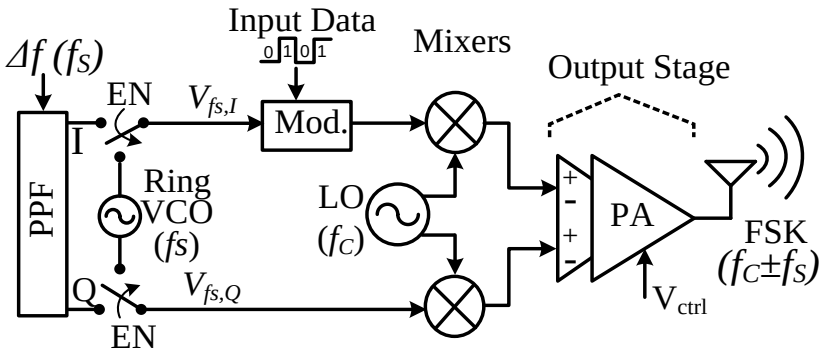


Figure 3.4: Proposed Transmitter Architecture

3.3.2 Alternative spots for applying the modulation

As discussed, the proposed FSK modulation is realized by changing the polarities of a signal when producing the transmitter output voltage. The generated output signal is toggling between Eq. (3.4) and Eq. (3.6). Referring to Eq. (3.7), changing the polarities of the sinusoidal term $sin(\omega_s t)$ was the basis of the presented modulation. However, the presented technique can be applied not only on one sinusoidal term but also on the product of them, here, $sin\ (\omega_c t)\ cos\left(\omega_s t + {}^{\pi}/_{4}\right)$, or $V_{f_c,I} \times V_{f_s,Q}$. Figure 3.5 shows the possible choices (1, 2 and 3) for applying the modulation within the FSK signal path. Spot number 3 is, in fact, inside the adder due to its symmetrical differential circuit implementation. Notice that the modulation blocks are practically differential CMOS switches used to change the polarities of its input signal.

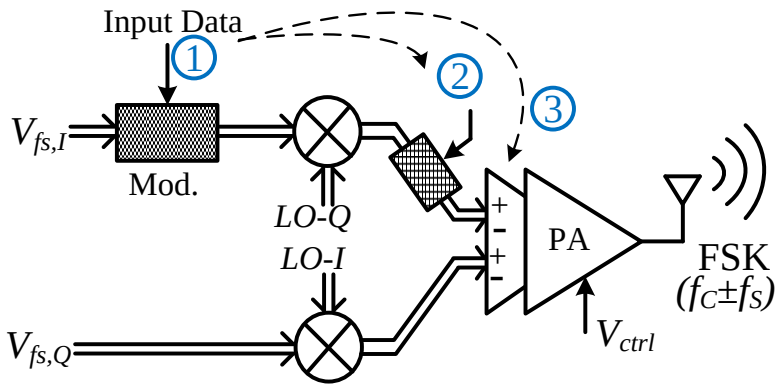


Figure 3.5: Choices for applying the modulation in the proposed transmitter architecture

The propagation time from the modulation block to the antenna may be shorter which results in a faster circuit. But, on the other hand, the low-frequency input node of the mixer is easier to access once fabricated. The input signals of the mixers were considered to be fed both internally and externally for testing purposes. According to the simulation results for comparing the propagation time for the three mentioned modulation spots, the delay difference was negligible. As a result, the modulation block was chosen to be located before the mixer due to easiness of dealing with low-frequency circuits.

3.3.3 Sensitivity over variation in phase and amplitude

Sensitivity of the generated output signal in Eq. (3.7) is studied in this section. The output generated signal is observed by considering a small variation in phase and amplitude of the I/ Q signals. Eq. (3.8) shows the output signal as a function of and the variation in amplitude and phase, respectively.

$$V_{out}(\Delta a, \Delta\varphi) = sin(\omega_c t)cos(\omega_s t - \Delta\varphi) + (1 + \Delta a)cos(\omega_c t)sin(\omega_s t + \Delta\varphi) \qquad (3.8)$$

Considering the error signal of V_{ERR} in Eq. (3.9), sensitivity of the output signal is interpreted by calculating the rms value of the error signal, $V_{ERR,rms}$ in Eq. (3.10).

$$V_{ERR}(\Delta a, \Delta\varphi) = V_{out}(\Delta a, \Delta\varphi) - V_{out}(0,0) \qquad (3.9)$$

$$V_{ERR,rms}(\Delta a, \Delta\varphi) = \sqrt{\frac{1}{T}\int_0^T {V_{ERR}}^2\, dt} \tag{3.10}$$

Figure 3.6 shows the 3D demonstration of the error signal ($V_{ERR,rms}$) to observe the sensitivity over both phase and amplitude generated in MATLAB environment. In Figure 3.6, the value of $V_{ERR,rms}$ reaches its maximum when phase variation between the I and Q signals is close to 90 degrees (or $\Delta\varphi = 45$ in Eq. (3.8)). Assuming an amplitude of 1 V for each sinusoidal term in Eq. (3.8) and 90 degrees phase discrepancy results in $V_{ERR,rms}$ of 1 V and may increase by larger amplitude discrepancies. The error reaches zero for the ideal case where there exists no discrepancy in phase and amplitude. Notice that for frequency variations close to 180 degrees, the value of $V_{ERR,rms}$ drops to zero again, but, in fact, such unacceptable phase discrepancy is so large that the output desired frequency changes from one frequency to another. The time-domain behaviour of $V_{ERR,rms}$ is shown in Figure 3.7.

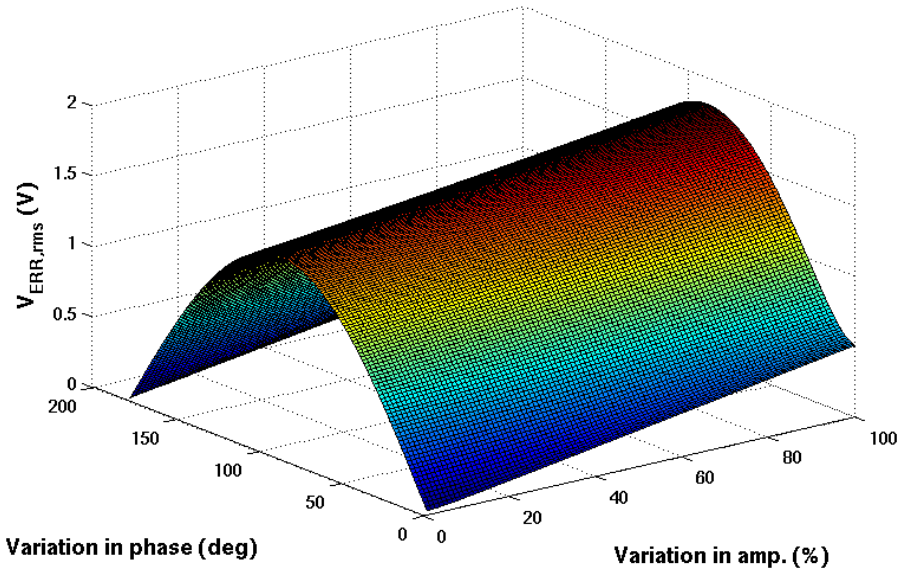


Figure 3.6: Output sensitivity over amplitude and phase discrepancy

The error resulting from the detection of the output FSK frequency is also displayed in Figure 3.8, where the correct FSK frequency (915 MHz + 500 kHz for data='1') gets shifted down to 915 MHz – 500 kHz resulting in an incorrect detection of data. As mentioned earlier and

according to Figure 3.8, the maximum error occurs when the two I and Q signal have become in opposite phases where Δφ for each sinusoidal term is 45 degrees. For Δφ larger than 45 degrees, every bit of data (‘1’ or ‘0’) will be incorrectly detected.

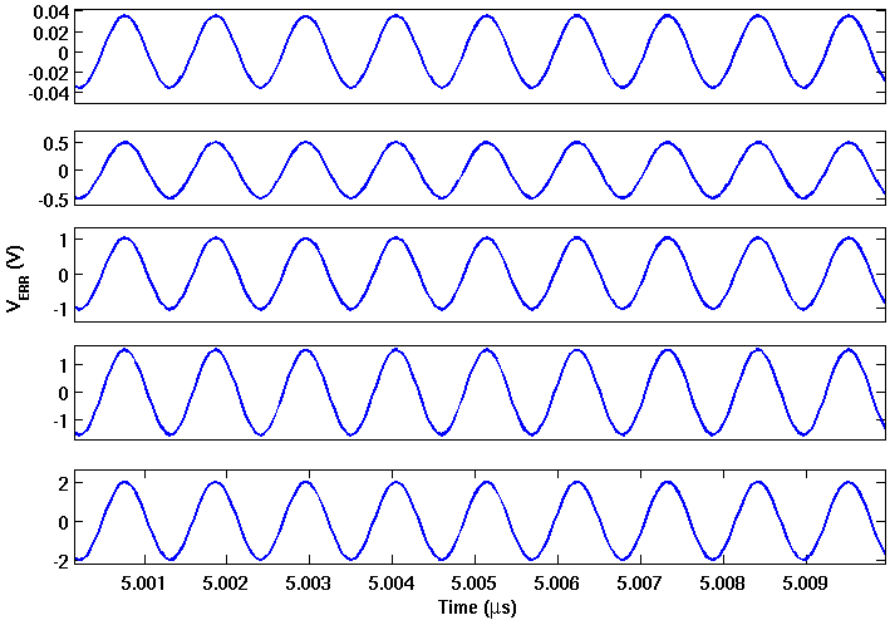


Figure 3.7: Variation of V_{ERR} for Δφ =1, 22, 45, 77 and 90 degrees when Δa=0

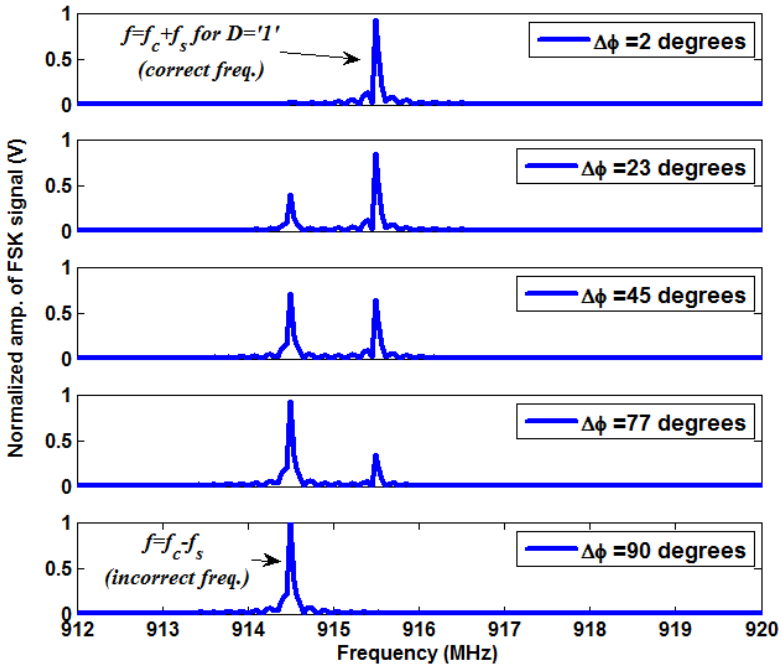


Figure 3.8: Frequency domain behavior of $V_{out}(\Delta a,\Delta\varphi)$ for $\Delta\varphi$ =2, 23, 45, 77 and 90 degrees when Δa =0

As a conclusion, minimizing the effect of discrepancy in phase is more important than in amplitude, however, both should be carefully dealt with. A few degrees of phase discrepancy might be tolerable but it has to be minimized to reduce the error. In practice, the phase discrepancy directly increases FSK error as it was observed during the measurements. Therefore, a quadrature oscillator with small amount of phase discrepancy between I and Q signals should be used. The system-level verification of the presented architecture was also done in ADS environment (Figure 3.9). Figure 3.10 also shows the generated output FSK signals when data=’1 and ‘0’ that verifies the proposed modulation scheme. Notice that the frequency of 1 GHz was used in the simulations for simplicity. The frequency deviation is also chosen to be 100 kHz in Figure 3.9 where the phase of the 100 kHz signal is shifted up and down by 45 degrees to generate the I and Q signals. The power amplifier is not shown in this figure.

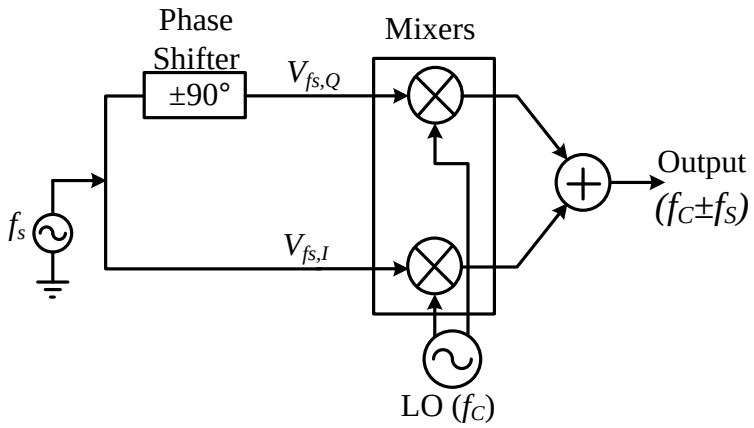
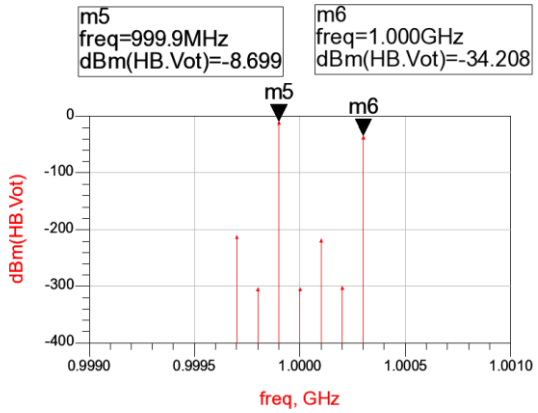


Figure 3.9: Simplified block diagram of the test-bench for system-level verification of the transmitter architecture in ADS software (See Appendix A)

Data=’0’:

$f_{out}=f_c - f_s$=1 GHz - 100 kHz



Data=’1’:

$f_{out}=f_c + f_s$=1 GHz + 100 kHz

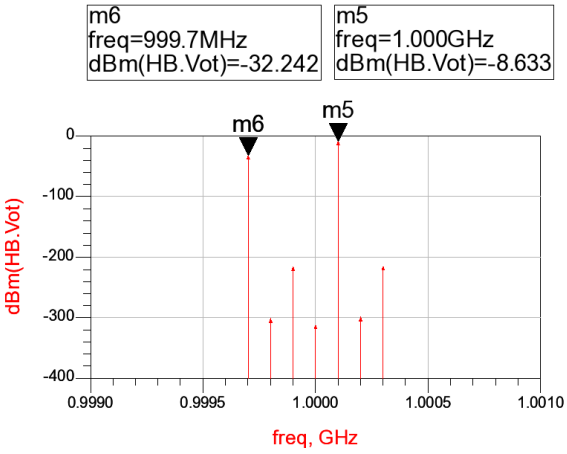


Figure 3.10: Output generated FSK signal in ADS when data='1' and '0'

3.4 Summary

In this chapter, the background theory of the proposed FSK modulation scheme was described and the methodology of realizing the corresponding target transmitter architecture was presented. It was shown that the proposed FSK modulation leads to a low complexity transmitter and can theoretically provide a high data-rate due to the short needed time to generate the output FSK signal as input data varies. The supporting mathematical equations were discussed along with sensitivity analysis over phase and amplitude discrepancy and system-level verification. It was shown that the phase and amplitude discrepancies can result in error in the desired output FSK signal. Alternative configurations for applying the needed modulation were also discussed. The building blocks intended to implement the proposed transmitter can be achieved through low-power circuits described in next chapter.

CHAPTER 4

CIRCUIT DESIGN AND IMPLEMENTATION

In this chapter, circuit-level design of the building blocks of the proposed transmitter architecture (Figure 3.4) is described. The composing building blocks were initially introduced in [28] and developed in [29] and [30]. The proposed transmitter can be realized using different implementations which may result in different performances for either customized or general applications. A fully integrated design is targeted towards a low-power prototype, however, some off-chip design choices are also considered. Building blocks of the proposed radio frequency transmitter were simulated using two CMOS technologies of TSMC 90 nm and IBM 130 nm showing similar performance. The results due to IBM 130 nm technology are presented in this thesis.

4.1 Differential Quadrature Voltage-Controlled Oscillator (QVCO)

Implantable biomedical sensors require very small and low-power communication front-ends and wireless radio frequency transceivers are the most challenging blocks to maintain the data communication. Design of crystal-less and inductor-less Voltage-Controlled Oscillators (VCOs) helps to implement the fundamental building blocks in implantable communication and VLSI systems with different frequency ranges as demonstrated by several reported literatures such as in [54-56]. As mentioned earlier, in widely-used binary FSK-based transceiver architectures, the carrier frequency gets shifted up and down by the frequency deviation to distinguish between ‘1’ and ‘0’. Such frequency deviation is usually defined by differential quadrature signals which can be generated by cascaded flip-flops acting as a frequency divider fed by an external reference clock or crystal oscillators. However, crystal oscillators may not be suitable for integrated sensors. The frequency may also vary depending on the application and the available channel bandwidth.

In this section, a new low-power differential rail-to-rail quadrature voltage-controlled oscillator (QVCO) is presented. The proposed CMOS QVCO in this work is a 2-stage ring-

oscillator and consumes small area, which is suitable for implantable devices with low-voltage and low-power circuits. The generated quadrature signals in this work are targeted to operate with a frequency between 500 kHz and 2 MHz to modulate the carrier signal (915 MHz) and to realize the binary FSK modulation in the target radio frequency transmitter architecture. The frequency of the presented QVCO can be tuned between 300 kHz and 11.57 MHz by varying the control voltage from 0.35 to 0.9 V by consuming a current between 0.5 and 160 uA. As discussed in the following, the related parameters can be varied to obtain another range of frequency. Here, the frequency range of 3-40 MHz was also achieved while consuming a current of between 3 and 117 uA. The simulation results for both cases are shown in this section.

4.1.1 QVCO's Block Diagram

This voltage controlled quadrature oscillator was designed and implemented to generate differential quadrature signals, I+, I-, Q+ and Q-. Notice that the generated I and Q signals are, in fact, the $V_{fs,I}$ and $V_{fs,Q}$ signals in the transmitter architecture in Figure 3.4. Figure 4.1 shows the block diagram of the designed quadrature oscillator including two delay cells and a start-up block. This structure can be considered as a ring oscillator where no external clock signal is required and facilitates the integration of the oscillator. However, the start-up circuit still needs to take care of initiating the oscillation.

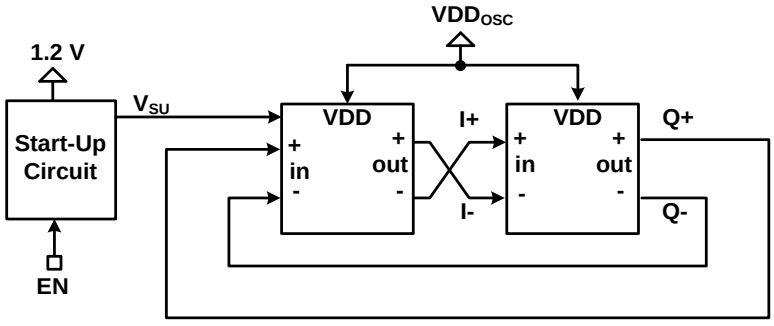


Figure 4.1: Block diagram of the 2-stage tunable quadrature oscillator including 2 delay cells and start-up

Once enabled by EN signal, the start-up circuit sends the start-up signal, V_{SU}, to the oscillator block to initiate the oscillation and after a specific delay the start-up circuit

automatically gets disconnected from the oscillator circuit by floating the node of V_{SU}. The external supply voltage, VDD_{OSC}, is also used to tune the frequency of the quadrature signals. No inductor is necessary to save chip area for the target frequency range. Notice that the start-up block is fed by the 1.2 V supply and consumes relatively negligible current.

4.1.2 QVCO's Circuit

Figure 4.2 shows the circuit-level implementation of the delay cells of the oscillator blocks. Each delay cell is similar to a bi-stable circuit triggered by the rising edge of its inputs and provides differential outputs. The NMOS transistors, $M_{n5\text{-}8}$, are the input transistors while transistors $M_{n1\text{-}4}$ and $M_{p1\text{-}4}$ form the output inverters. Each I and Q nodes are, in fact, the outputs of the CMOS inverters that can be powered up by a low supply voltage to reduce the power consumption. The voltage variations on both terminals of the capacitors, C_t, are concurrent. As shown in the following, the total current of this oscillator is less than 6 uA when generating quadrature differential signals with frequency of 2 MHz.

Alternatively, the PMOS transistors can be used as input transistors, where the delay cells are sensitive to the falling edge of the inputs. The symmetrical layout of the proposed QVCO implemented using IBM 130 nm CMOS technology in Cadence Environment is shown in Appendix B. Capacitors are in practice consuming the largest area.

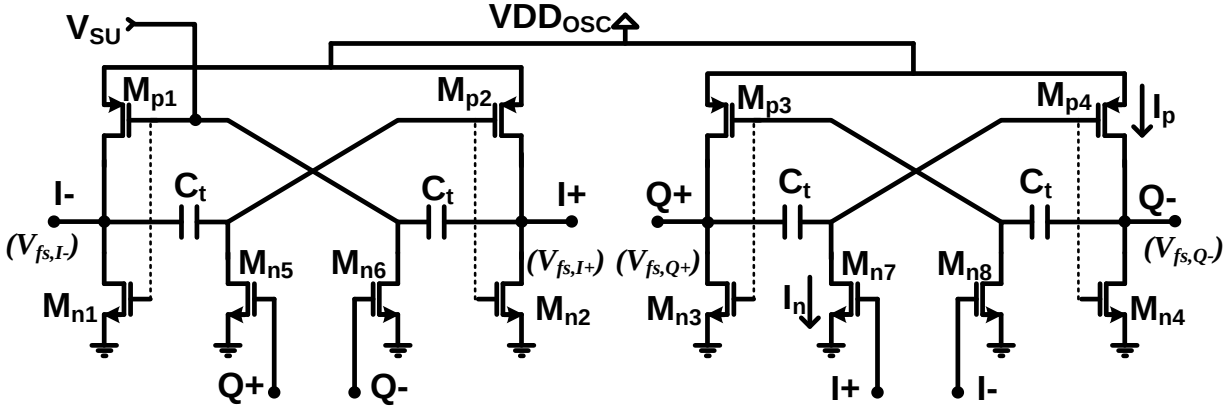


Figure 4.2: Proposed 2-stage quadrature voltage-controlled oscillator

The transient behaviour of I and Q signals is shown in Figure 4.3, where T_{np} is the delay from the rising edge of the input of one delay cell to the next rising edge occurring at the input of the other delay cell. This interval includes the propagation of signal through two NMOS and PMOS transistors. Notice that in practice the falling and rising time for NMOS and PMOS transistors can be different depending on their width and length. Here, both falling and rising time of the nodes are assumed to be close and the symmetrical behaviour of differential signals will be kept.

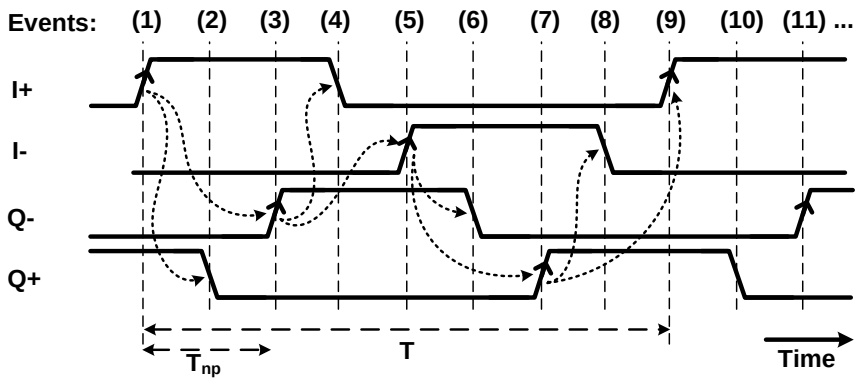


Figure 4.3: Time-domain behaviour of I and Q signals showing the sequence of events in one period of T

For instance, the propagation of the signal from *I*+ to *Q*- is described here. Assuming a large enough voltage of VDD_{OSC} to power up the transistors, the voltage of *I*+ is raised using the rising edge of a pulse produced by the start-up circuit that is the starting point, event (1) in Figure 4.3. Then, the rising edge propagates through M_{n7} to *Q*+ as a falling edge due to I_n occurring at event (2) followed by the rising edge of *Q*- due to I_p at event (3). Therefore, T_{np} can be estimated as follows:

$$T_{np} \approx \frac{C_{p1}\left(V_{High} - V_{Low}\right)}{I_n} + \frac{C_{p2}\left(V_{High} - V_{Low}\right)}{I_p} \tag{4.1}$$

In Eq. (4.1), C_{p1} and C_{p2} are the total capacitance at the gate of PMOS transistors and the output nodes, respectively, which can be considered equal and replaced by C_{tot}. V_{High} - V_{Low} can

be replaced by VDD_{OSC}. I_p and I_n, which are also functions of VDD_{OSC}, are the current of the PMOS and NMOS transistors, respectively, and can be considered equal. Consequently, the total period, T, can be estimated by Eq. (4.2).

$$T = 4 \times T_{np} \approx \frac{8 \times C_{tot} \times VDD_{OSC}}{I_{n,p}} \tag{4.2}$$

The presented quadrature structure can be used as a digitally-controlled oscillator either by controlling an additional capacitor-bank in parallel with C_t or by adding parallel transistors to change the current capacity and, hence, the frequency. Here, the supply voltage of the proposed oscillator's circuit, VDD_{OSC}, is used to tune the frequency and to realize the VCO. The current consumption and frequency range of the generated differential I and Q signals of the proposed structure may vary according to the chosen parameters and the target application (here low-power implantable transceivers). The maximum frequency is limited by the required settling time for each output voltage after its transition from High to Low levels and vice-versa. There is a trade-off between the slew-rate and the current budget. The achieved frequency range and corresponding current consumption are shown in the results section in the following chapter.

4.1.3 QVCO's Start-Up Circuit

The goal of this start-up circuit is to generate a pulse with a rising-edge to change V_{SU} (the gate voltage of the PMOS transistor M_{p1} in Figure 4.2) to a non-zero value and to initiate the oscillation as described earlier. As initial conditions in the start-up circuit of Figure 4.4*a*, V_{b2} is zero when EN is still zero. The non-zero value of V_{b1} forces V_p to stay at zero. The stack of diode-connected NMOS transistors are used to provide the two voltages of VDD_S and V_{b1} such that $VDD_S > V_{b1}$ while consuming less than 0.4 µA.

The conceptual transient behaviour of the nodes of the presented start-up circuit is illustrated in Figure 4.4*b* and can be explained in three steps. In the first step, by enabling the oscillator and the start-up circuit, the voltages VDD_S and V_{SU} reach their non-zero values. In step two, the voltage V_{b2} starts rising due to the charges accumulating in C_d until V_{b2} becomes larger than V_{b1} by a delay proportional to the inverse of C_d. In step three, the voltage V_p changes from

'0' to '1' and disconnects VDD_S and V_{SU} by turning off the corresponding PMOS transistor, M_{PSU}, leaving the oscillator disconnected from the start-up circuit. The simulated time-domain behaviour of the mentioned nodes is shown in Figure 4.5 which is following the behaviour of nodes explained in Figure 4.4*b*. Layout of the implemented start-up circuit using 130 nm CMOS technology is also shown in Appendix C.

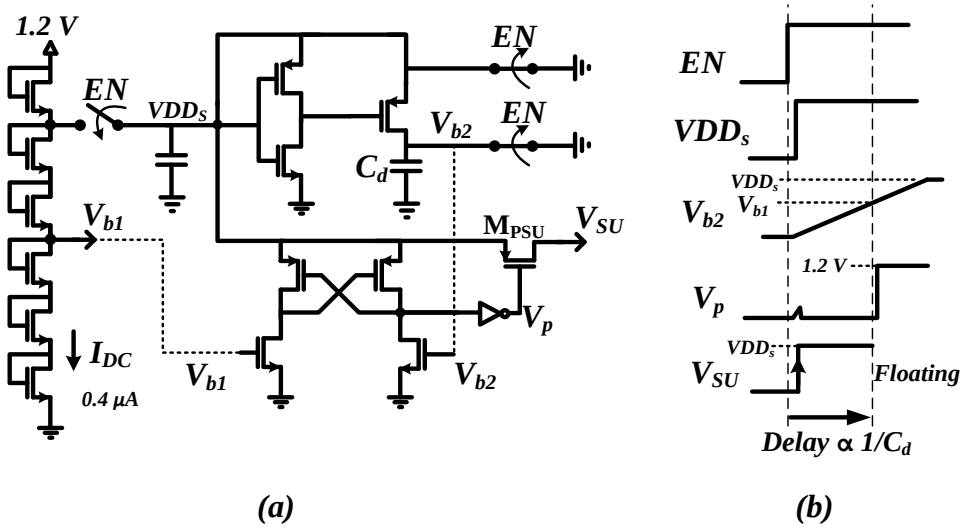


Figure 4.4: Start-up circuit: a) Schematic, and b) Transient behavior of its nodes

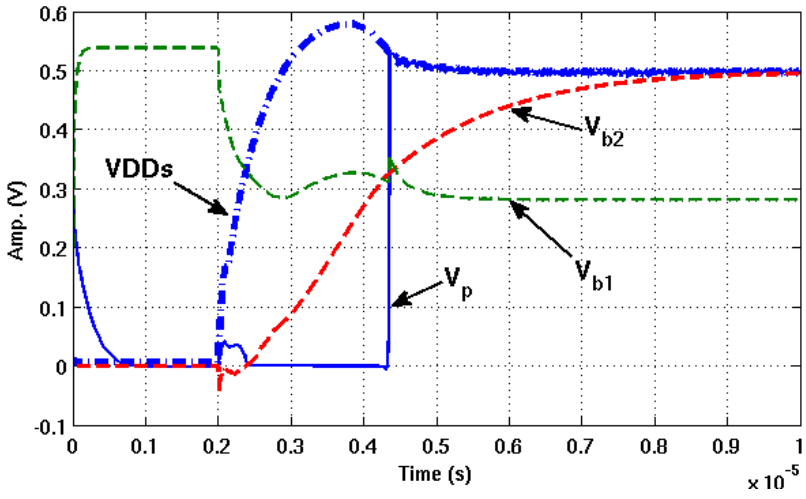


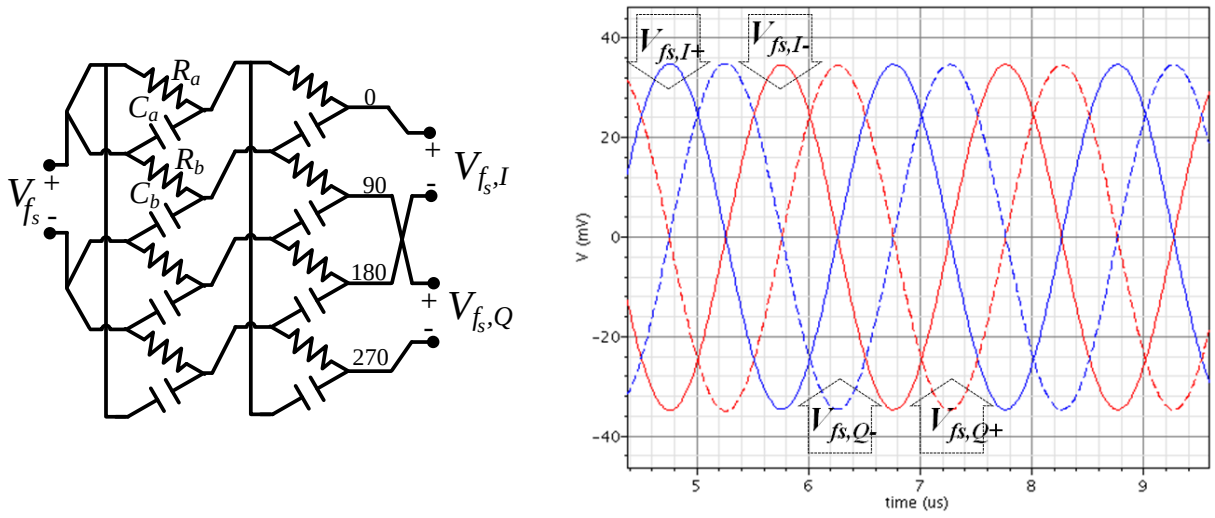
Figure 4.5: Simulated time-domain behavior of the nodes in start-up circuit

The circuit of the proposed QVCO was simulated and fabricated using IBM 130 nm technology in Cadence environment. The simulation and measurement results of the proposed QVCO are reported in chapter 5.

4.2 Poly-Phase Filter (PPF)

As discussed earlier, the frequency deviation of an FSK signal is defined mainly by the available channel bandwidth. Once the desired frequency deviation is defined, the differential I/Q signals are generated correspondingly for the presented transmitter architecture. To generate I/Q signals a passive poly-phase filter (Figure 4.6*a*) was implemented to avoid DC current consumption. The poly-phase filter is a symmetric RC network with inputs and outputs symmetrically disposed in relative phases. The target frequency of such structure is defined by $1/2\pi fRC$. Notice that all resistors have equal values as well as the capacitors.

The detailed characteristics of the PPF structure was analyzed in [57] with more details. Here, some characteristic of this filter is studied. Layout of each resistor was implemented with multiple fingers in an interleaved pattern to further reduce the effect of process variation and mismatch (Figure 4.7). Since the on-chip passive resistors and capacitors take relatively large die area, PPF is more suitable for implementing test prototypes of circuits operating at higher frequencies (several MHz and higher). However, on the other hand, active poly-phase generators may add more current consumption and complexity. The new designed VCO in this thesis can be also replaced to save chip-area.



(a) ***(b)***

Figure 4.6: 2-stage PPF: a) Schematic, b) Simualted quadrature signals with f_s=500 kHz

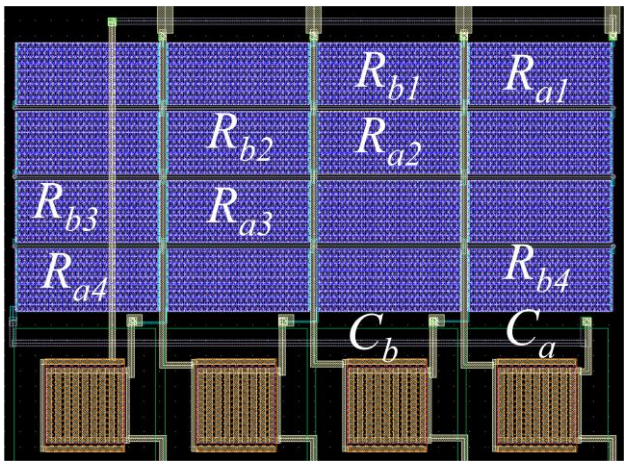
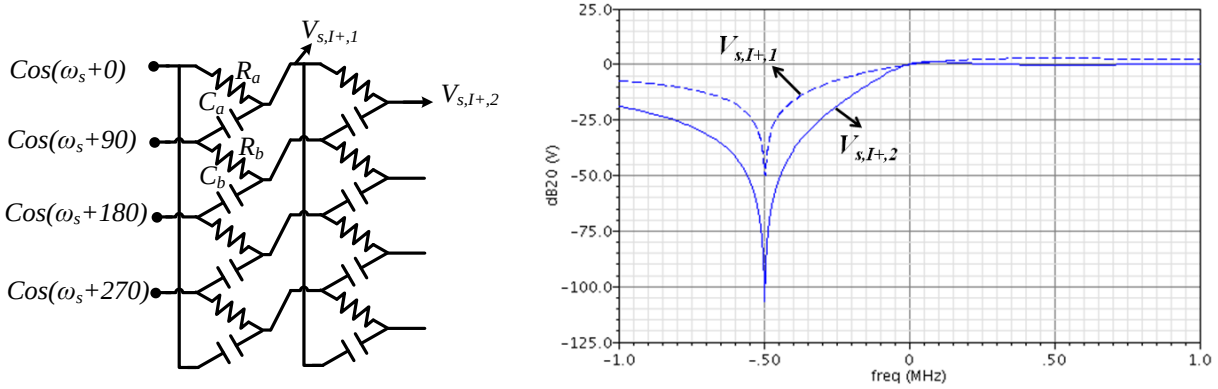


Figure 4.7: One stage of PPF layout with interleaved-shaped resistors to minimize mismatch. $R_{a1\ldots4}$ form R_a in Figure 4.6

According to Authors of [57], one way to study the performance of such PPF is to input it with four signals with 90 degrees phase-shift, similar to Figure 4.8*a*. This configuration is actually the case for the second stage in a 2-stage cascaded PPF. In this way, the attenuation of the image signal can be observed. According to the performed Monte-Carlo simulations in this

research, two stages of PPF may be used to decrease the effect of mismatch and process variation and to improve the quality of the generated I and Q signals by further weakening the image signal. Using 100 iterations in Monte-Carlo simulation showed that by using 2 stages of PPF the attenuation of the image signal at $-f_s$ (f_s=500 kHz, for example, in Figure 4.9) remains around 20 dB for 30% variation in the center frequency while for one stage of PPF the attenuation is only 6.7 dB for the same variation in the center frequency. In other words, when the center frequency of the PPF stage varies due to mismatch and process variation, the image signal remains low enough.

As a result, two stages of PPF were considered in this design to lower the effect of mismatch and process variation. The layout was also designed in Cadence environment using interleaved configuration to further minimize the effect of mismatch and process variations. Larger number of stages may results in better image-reduction but losing more die area.



(a) ***(b)***

Figure 4.8: Image reduction in PPF: a) Inputs configuration with f_s=500 kHz, b) Outputs of the first and second stages in frequency domain

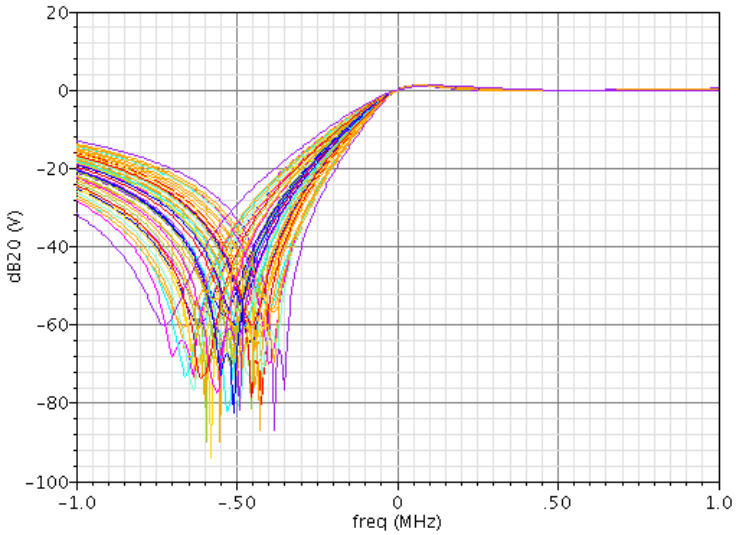


Figure 4.9: Effect of mismatch and process variation on quadrature signals due to 100 iterations of Monte-Carlo simulation

4.3 Passive Mixer

Multiplication of sinusoidal terms in Eq. (3.7) and, hence, up-conversion is realized using the well-known linear passive CMOS mixers of Figure 4.10. They draw no dc current from the voltage supply that is suitable choice for low-power designs. However, port-to-port isolation could be a challenge and may result in LO feed-through [1]. Passive mixer layout design has to be done very carefully to avoid any mismatch between transistors. One may use an active mixer, such as Gilbert cells [1] to minimize the signal attenuation in expense of more complexity and current. The current-driven mixer in [58] also requires large current consumption.

In this mixer, I and Q signals with the deviation frequency (or shifting frequency), f_s, are mixed with the Local Oscillator signals, $V_{fc,I}$ and $V_{fc,Q}$, with frequency of f_c referring to Eq. (3.5). Therefore, the sum expression will be $cos(\omega_c+\omega_s)t+sin(\omega_c+\omega_s)t$ with frequency of f_c+f_s, while the sub expression is $cos(\omega_c-\omega_s)t+sin(\omega_c-\omega_s)t$ with frequency of f_c-f_s. The input data has already determined which output is to be generated.

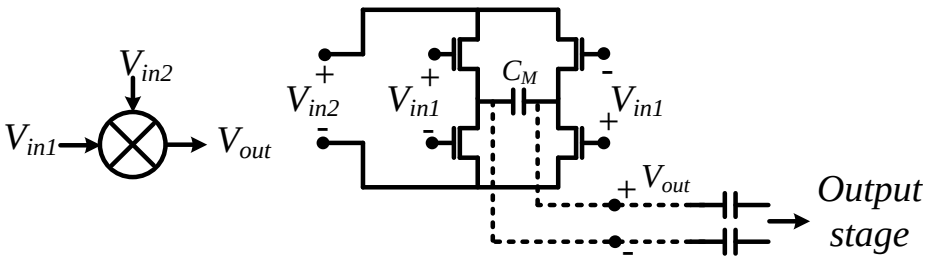


Figure 4.10: Differential CMOS passive mixer

Figure 4.11 shows the simulated differential output signals of the two mixers in the I and Q paths in the transmitter architecture. In the related test-bench, the low-frequency input, V_{in1}, has amplitude of 100 mV with frequency of 500 kHz, which is the deviation frequency, f_s. The high-frequency input, V_{in2}, has amplitude of 200 mV with frequency of 1 GHz, which is the carrier frequency, f_c. The DC voltage of the above signals are considered zero. Decoupling capacitors are used to avoid any dc path between the local oscillator and its following blocks. Also, the outputs of the mixer are passing through series capacitors (~200 fF) before reaching the output stage. The capacitor, C_M, has also value of 20 fF for this simulation. The width and length of the transistors are chosen to be 7/0.12 um/um to maintain a trade-off between the total parasitic capacitance and minimum dc on-resistance and largest output.

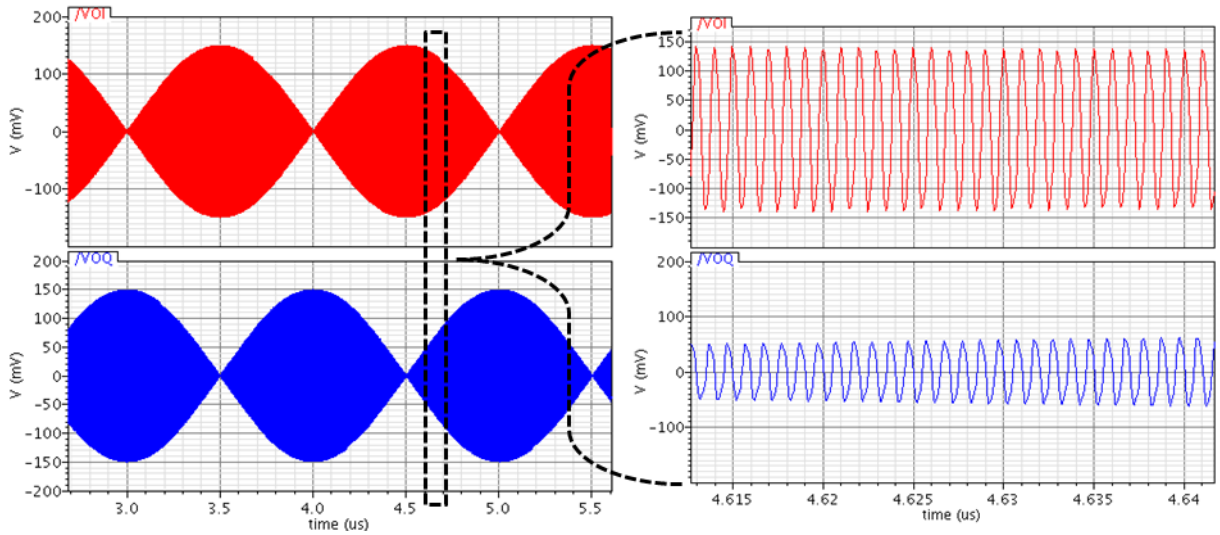


Figure 4.11: Simulated mixers' outputs

4.4 Transmitter's Output Stage

Depending on the target transmission distance, the output stage of the transmitter needs to provide an adequately large signal due to the existing losses, noise and disturbances from other instruments nearby. The required signal amplitude is usually smaller in implantable devices to lower the current dissipation while the current budget is more relaxed in wearable devices with higher power efficiencies. However, there is always a trade-off between the PA's current consumption and the provided output power to the antenna. The output stage in this architecture was considered for both low-power implantable and high-efficiency wearable applications.

The Power Amplifier is known to be the most power-hungry block in RF transmitters. Its job is to amplify the generated transmitting signal before reaching the antenna. The main challenge in addition to the power efficiency is the size of the inductors for biasing or matching. Efficiency (η) of the power amplifier is usually calculated as P_{out}/P_{DC} in percentage. P_{out} is the generated and delivered output power to the 50-Ohm antenna. P_{DC} is the total DC power consumption which is the total current consumption multiplied by 1.2 V, the supply voltage. The PA stage is optimized in terms of efficiency to provide high-output power when it is used for applications with wearable devices. As shown in the following, the tuneable driver as adjusts and reduces the current and the output amplitude. The inductor is also integrated to have less external components, although better signal quality is expected if external LC matching network is used.

4.4.1 Output stage in the fabricated Tx

Figure 4.12 shows the block diagram of the implemented output stage in the fabricated transmitter chip. Figure 4.13 also shows the transistor-level implementation of the output stage of the integrated transmitter. The two differential signals from the mixers (V_1 and V_2) are added up through a single-ended adding amplifier. This single-pole signal, V_{o1}, which is the generated FSK signal, contains the desired information and needs to be fed to the antenna. Transferring large signal amplitude from such CMOS circuit to the 50-Ohm antenna would be challenging and inefficient unless a power amplifier with matching circuit is used.

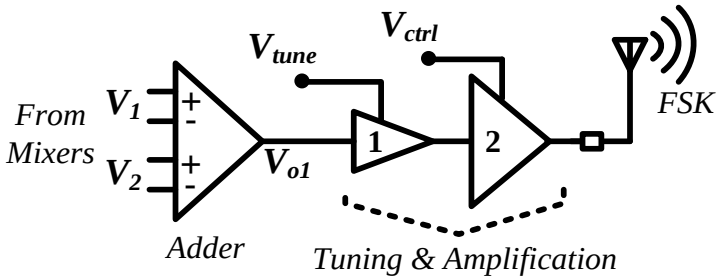


Figure 4.12: Block diagram of the integrated transmitter's output stage including the 2-stage PA

The circuit of the power amplifier has 2 stages of tuning and amplification where the control voltages (V_{tune} and V_{ctrl}) are considered to control the current consumption, signal amplitude and power efficiency. Alternatively, as specified in Figure 4.13, the gate voltages of the cascode transistors in the output branch, $V_{ctrl,R}$ and $V_{ctrl,LC}$ are considered to further control current for integrated and off-chip matching scenarios, respectively.

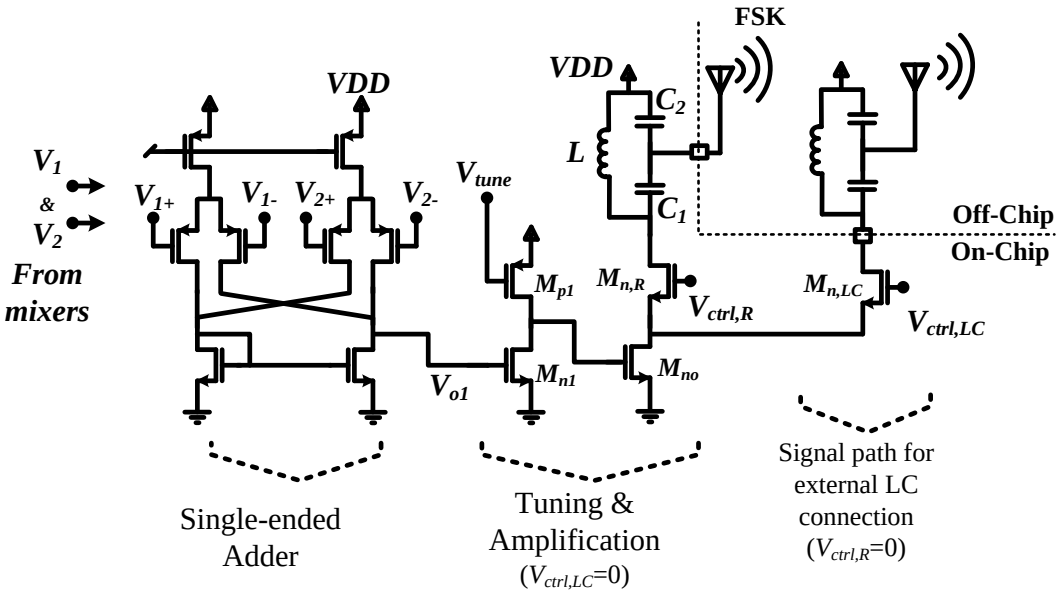


Figure 4.13: Transmitter's output stage (fabricated chip)

In this output stage, V_{o1} is amplified through 2 different stages. The first stage consists of M_{n1} and M_{p1}. M_{n1} is chosen small to lower the loading capacitance of the adding amplifier and to

lower the signal loss at high frequency. The gate voltage of M_{p1}, V_{tune}, is considered for tuning the DC voltage at the gate terminal of M_{no} in the second stage. In this way, the effect of process variation on M_{n1} or M_{p1}, which may change the DC voltage of the gate terminal of M_{no}, can be adjusted. Another benefit of this tuning voltage is to control the current of M_{no} in the output branch. This current is also controlled by the gate voltage of the cascode transistor, $M_{n,R}$, which changes from ~400 mV to 1.2 V. Notice that the gate terminal of $M_{n,LC}$ is always set to zero unless external LC matching circuit is to be used. In such scenario, the gate terminal of $M_{n,R}$ will be set to zero and the control voltage is $V_{ctrl,LC}$.

Both $M_{n,R}$ and $M_{n,LC}$ may be removed to avoid their drain-source voltage drop, leaving V_{tune} the only control voltage. In this case, increasing the current of the output branch by increasing W_{no}, the width of M_{no}, results in maximum efficiency of 9 % while consuming 2.7 mA to generate -5 dBm of output power (Figure 4.14). As a result, this output stage was modified to improve the efficiency.

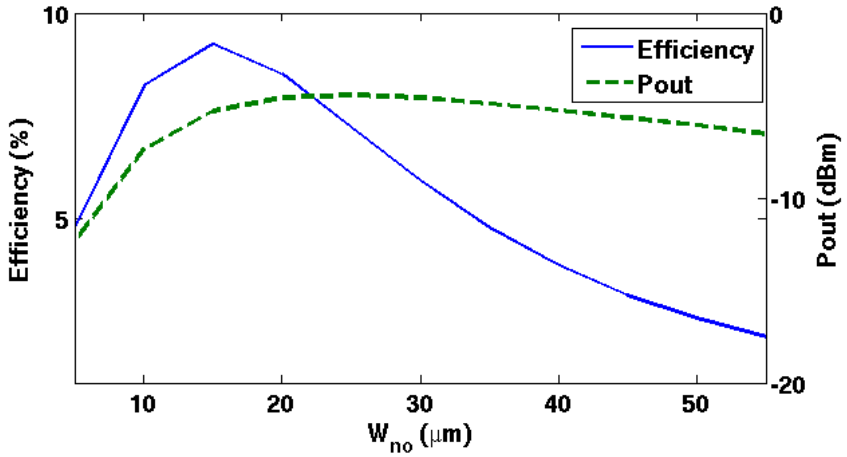


Figure 4.14: Efficiency and P_{out} vs. W_{no}, the width of M_{no} in output branch of Figure 4.13

4.4.2 Modification and optimization of PA

The presented circuit of the power amplifier was modified in order to increase the power efficiency of the output stage of the target transmitter by adding an inverter stage consisting of M_{n2} and M_{p2} (stage 2 in Figure 4.15). This inverter enhances the total gain while consuming a small current. The goal is to find the best range for V_{tune}, the best sizing for transistors and the

corresponding matching circuit. The approach is to come up with a low gain for the first and second stages and higher gain for the third stage. As mentioned before, the width of M_{n1} in stage 1 should be considered small to minimize the loading capacitance to the adder stage.

As the first step, Figure 4.16 shows the efficiency versus width of M_{n2} and M_{p2}, $W_{2,}$ where W_2= 3 µm gives the best efficiency. For simplicity, W_{p2} and W_{n2} were considered equal (W_{n2}=W_{p2}=W_2) and the lengths are the minimum length. By varying V_{tune}, the gate voltage of M_{p1}, the total current and, hence, the output power and efficiency are varied. In this case, V_{tune}=674 mV gives the highest efficiency of 36.3% while the output power is 3.3 dBm and $I_{DC,tot}$ 4.88 mA. The value of V_{tune}, which give the maximum efficiency, is then used to re-adjust the size of M_{n3}, the NMOS transistor in the output branch. The maximum efficiency reaches its maximum with W_{n3}=50 µm. Notice that the power added efficiency (PAE), which is (Pout-Pin)/P_{DC}, takes the input power into consideration and follows the behaviour of Efficiency (η).

The final optimized widths of transistors in Figure 4.15 are shown in Table 4.1. Notice that values of the inductor, L, and capacitors, C1 and C2, are accordingly tuned when different widths of M_{n3} are used. As mentioned before, the integrated inductor, L, is also the current path of the output branch. The inductor was taken from the library of IBM 0.13 um CMOS technology for simulations in Cadence environment. Inductance of the bonding-wires was also included in the simulations. The inductor is around 10 nH and the capacitors are around 5 pF in the used matching circuit.

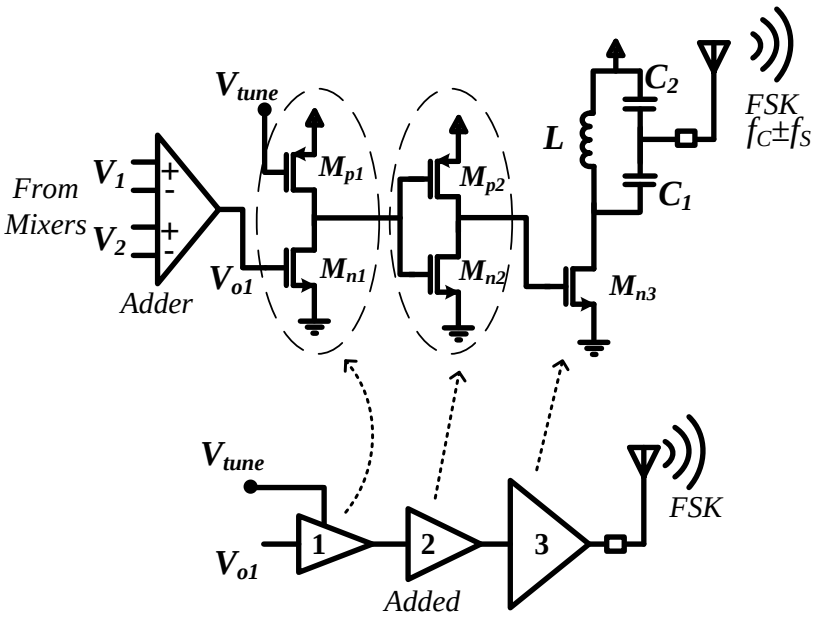


Figure 4.15: Modified and optimized power amplifier

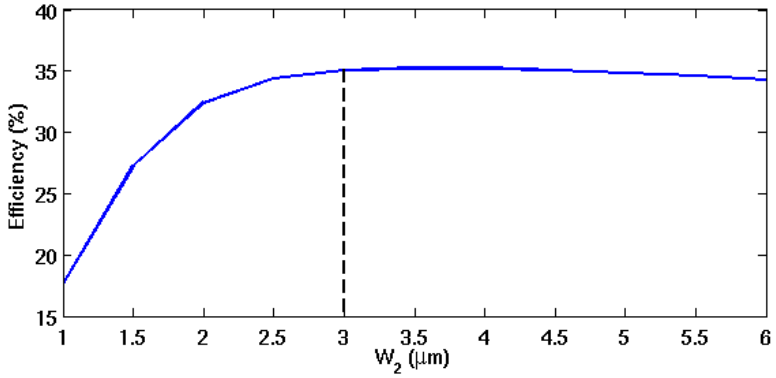


Figure 4.16: Efficiency vs. W_2, transistors' width in the added inverter

Table 4.1: Transistors sizing of the optimized PA

	M_{n1}	M_{p1}	M_{n2}, M_{p2}	M_{n3}
W/L (um/um)	4/0.2	8/0.2	3/0.2	50/0.2

Figure 4.17 shows the characteristics of the final design of the optimized PA as a function of V_{tune}. In this case, for V_{tune}=676 mV the highest efficiency is 37.3% while the output power is 3.7 dBm and $I_{DC,tot}$=5.2 mA. As another operating point, considering a current budget of 0.8 mA, P_{out} reaches -12.6 dBm with an efficiency of 5.8 %.

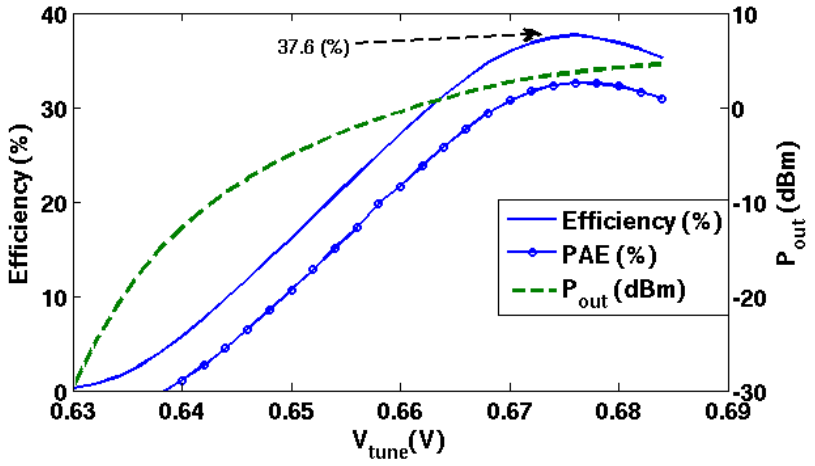


Figure 4.17: Efficiency, P_{out} and total current vs. V_{tune} after optimization

The simulation results for the designed PA are summarized in Table 4.2 and compared with other related PAs. Notice that PA designs are usually customized according the required specifications in different applications and it is not easy to compare their respective FOMs. In addition to the efficiency, the size of the implantable and even wearable devices is also one of the main issues to deal with. On-chip inductors take a huge portion of the die area and implementing a high performance front-end with less number of inductors is an advantage. Therefore, power efficiency has to be considered as a FOM while taking other parameters into account, such as the die-area and number of external components. According to simulation results, the optimized power amplifier of this work has shown a relatively good and comparable performance among other similar designs, as shown in Table 4.2. For wearable applications, where higher value of current is allowed, V_{tune} may be set such that the maximum efficiency is achieved. On the other hand, for implantable applications with limitation on current consumption, V_{tune} can be adjusted to lower the current. Moreover, an additional NMOS transistor could be used in parallel with M_{n3} in Figure 4.15 with a smaller width to provide lower current when M_{n3} is switched off.

Alternatively, in order to perform the future tests on the OOK receiver, V_{tune} can be also controlled by a digital signal to generate the OOK outputs signals to be transmitted to the receiver, which was not the focus of this research.

Table 4.2: Comparison of similar CMOS power amplifiers

PAs	P_{out}	$I_{DC}(P_{diss})$	η (%)	VDD (V)	Tech. (um)	Freq.	Level of integration
[20] (2001)	10 dBm (10 mW)	12.5 mA	38 %	1.2	0.5	430 MHz	External matching
	0 dBm (1 mW)	5.56 mA	15 %				
[59] (2004)	4.1 dBm (2.6 mW)	-	35 % (PAE: 26 %)	1.2	0.13	1.9 GHz	Bond-wire & off-chip for matching
[60] (2005)	6.5 dBm (4.5 mW)	11 mA	(PAE: 28 %)	1.4	0.18	2.45 GHz	Integrated
[14] (2009)	-6 dBm (0.25 mW)	1.8 mA	9.2 %	1.5	0.13	915 MHz	External matching
[61] 2009	-16 dBm (0.025 mW)	0.27 mA	~ 20 %	0.7	0.18	403 MHz	External matching (2 inductors)
[13] (2011)	-17 dBm (0.02 mW)	-	22 %	1	0.13	400 MHz	External matching
[11] (2011)	-10 dBm (0.1 mW)	0.7 mA	~ 25 %	0.7	0.18	920 MHz	External matching
This Work (wearable)	3.7 dBm (2.34 mW)	5.22 mA	37.6 % (PAE: 33%)	1.2	0.13	915 MHz	Fully Integrated
This Work (integrated)	-12.6 dBm (~0.55 mW)	0.8 mA	~ 6 %				

In summary, the circuit of the fabricated PA was shown in this section followed by the modified version and its optimization. In this power amplifier, only one on-chip inductor is used for both biasing and matching. The circuit of power amplifier was then optimized for maximum efficiency and the amplitude of the output signal is adjustable. The results were finally summarized and compared with similar circuits.

4.5 Transmitter Layout and Packaging

Figure 4.18 shows the transmitter circuit which was fabricated and tested to prove the functionality, efficiency and characteristics of the proposed transmitter. The reported measurement results in the following sections are, in fact, based on this implementation while the first version of the power amplifier was integrated. The layout of this proposed transmitter was implemented using IBM 130 nm CMOS technology under Cadence environment. For this technology, the typical VDD is 1.2 V with minimum transistor length of 120 nm.

Layouts of all transistors were instantiated from IBM 130 nm package with MA metallization option. Notice that the dummy layers are not shown in Figure 4.19. Table 4.3 lists the input and output ports briefly describing the role of each terminal. In the layout, the VDD terminal of the output branch (consisting of M_{no}, $M_{n,R}$ and L in Figure 4.13) is separated from that of the driver stage for test purposes. Also, the I/O pads are tried to be located as far from the integrated inductor as possible to lower any possible parasitic capacitors ad resistors from the high-frequency output signal to other nodes.

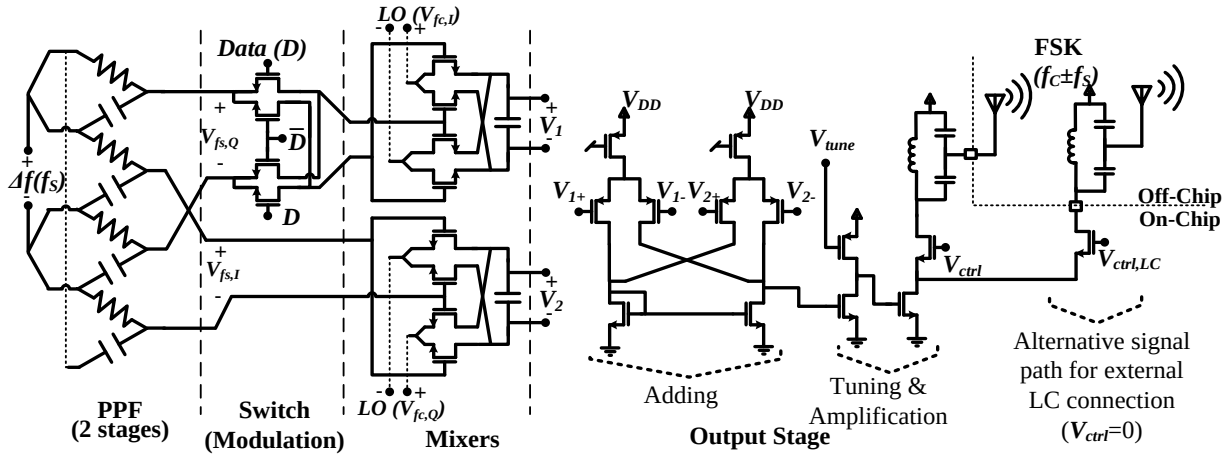


Figure 4.18: Transmitter circuit (fabricated chip)

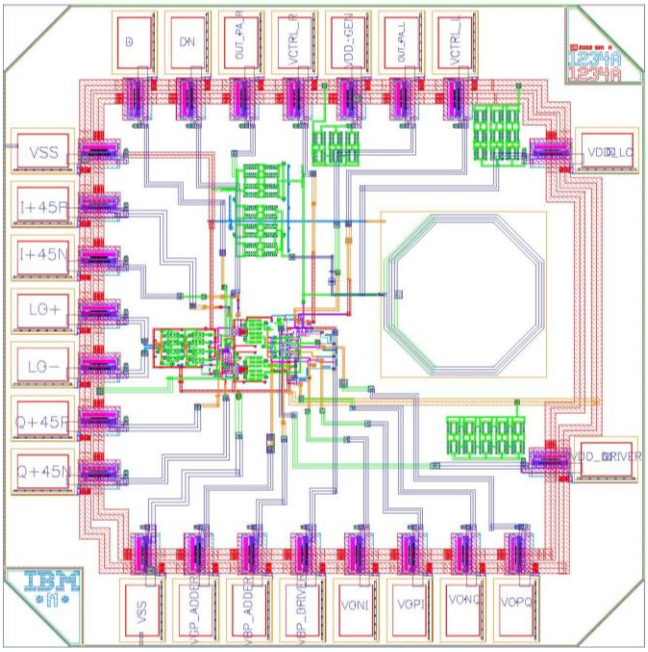


Figure 4.19: Transmitter layout (1.2×1.2 mm^2)

Table 4.3: Port definition of the integrated circuit

Ports	**Function**
VDD_GEN	General VDD terminal of the chip
VDD_LC	VDD terminal of the last branch in PA
VDD_PA (VDD_DRIVER)	VDD terminal of the driver stage
VSS	Ground terminal
VGP_ADDER, VBP_ADDER, VBP_DRIVER	Biasing signals for testing purposes
D, DN	Input Data (‘1’ and ‘0’)
I_P (I+45P) & I_N (I+45N) Q_P (Q+45P) & Q_N (Q+45N)	External I/Q signals containing the frequency deviation
LO+, LO-	Carrier inputs containing f_c
OUT_PA_R	Output of the transmitter going to the antenna
VCTRL_R	Control signal to control the current when OUT_PA_R is used
OUT_PA_LC	Output of the transmitter going to the external LC matching before the antenna
VCTRL_LC	Control signal to control the current when OUT_PA_LC is used. Otherwise it is set to zero.
VOPQ, VONQ, VOPI, VOPI	Monitoring points within the circuits

The layout of the transmitter was fabricated through CMC Microsystems and MOSIS by IBM, and the resulting die was packaged using Quad-Flat No Lead (QFN) package with 28 pins. This type of packaging is suitable for high-frequency tests as the unwanted parasitic capacitance and resistance of the leads are eliminated. Figure 4.20 shows the packaged chip with 1.44 mm^2 total die area including the ESD-protection pads and test circuits with relatively small active area (~0.2 mm^2).

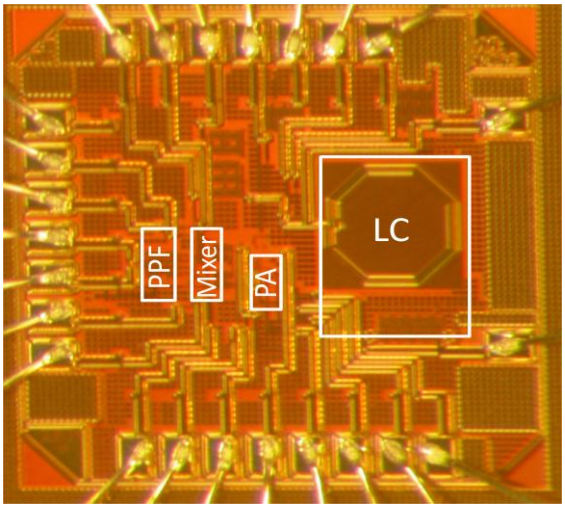


Figure 4.20: Chip microphotography of the fabricated transmitter (1.2×1.2 mm^2)

4.6 Summary

In this chapter, circuit-level implementation of the building blocks of the proposed transmitter diagram was presented. The novel design of the differential quadrature VCO (QCVO) was also shown along with the start-up circuit. The introduced QVCO provides two ranges of frequency tuning, 0.3-11.57 MHz and 3-40 MHz and the corresponding ranges of current consumption are 0.5-160 uA and 3-117 uA, respectively. The circuit of the poly-phase filter (PPF) was discussed including the Monte-Carlo simulations and layout considerations. Mixers and the output stage were also implemented following by optimization of the power amplifier and comparison with similar designs. The layouts of the presented circuits were then demonstrated and discussed followed by summary on description of the packaged chip and the developed test setup. As a conclusion, the circuit of the proposed transmitter was implemented with small area

and low-current consumption as will be shown in the next chapter, where the simulation and measurement results are reported and discussed.

CHAPTER 5

SIMULATION AND MEASUREMENT RESULTS

5.1 Fabricated Tx chip: Test-setup and general considerations

The fabricated layout of the implemented transmitter is used to confirm functionality and to compare the simulation results with the corresponding experimental performance. In particular, current consumption, capability of generating the desired FSK signals, and measuring the data-rate are priorities. The achieved transmitter was implemented using IBM 130 nm CMOS technology and supply voltage of 1.2 V, as mentioned earlier. The post-layout simulation results of the designed transmitter using 90 nm and 130 nm CMOS technologies for the same transmitter were similar, as reported in [28-30]. In this chapter, the simulation and measurement results due to IBM 130 nm CMOS technology are reported and used for comparison.

Simplified diagram of the test-setup used for measurements is shown in Figure 5.1 an RF signal generator was used to replace the local oscillator signal, which was converted to a differential signal through an external transformer (balun). A Spectrum Analyzer was used to observe and measure the characteristics of the generated FSK signal including the variation of output captured frequency over time, extracting modulated bits from analog signal and the FSK error in the constellation diagram. Also, for the implemented QVCO, an Oscilloscope was used to capture the differential I and Q signals when enabled by EN signal.

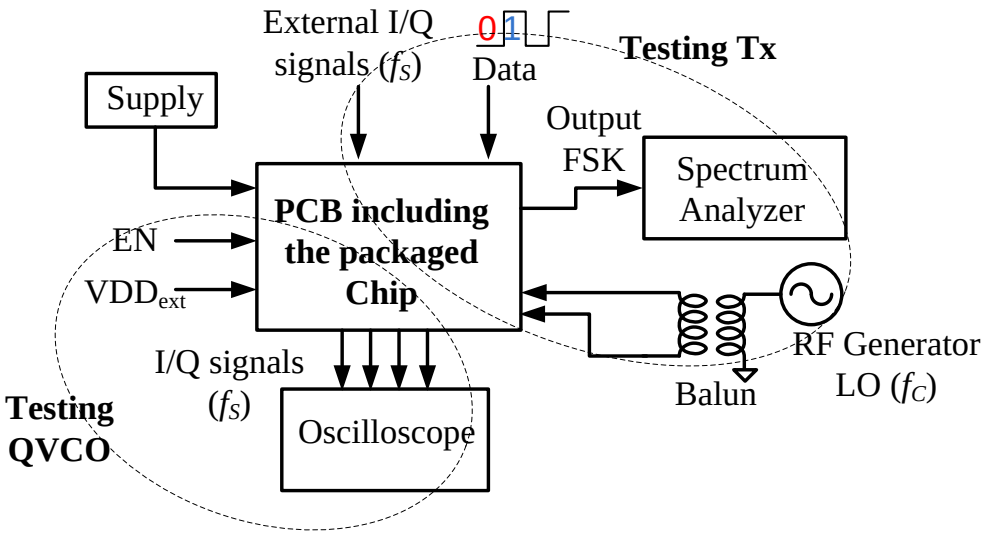


Figure 5.1: Simplified diagram of the setup used for testing the fabricated chip

The Printed-Circuit Board (PCB) is also shown in Figure 5.2 with the mounted packaged chip in the middle. The inputs, output, the external transformer (balun) and the input matching circuit are shown.

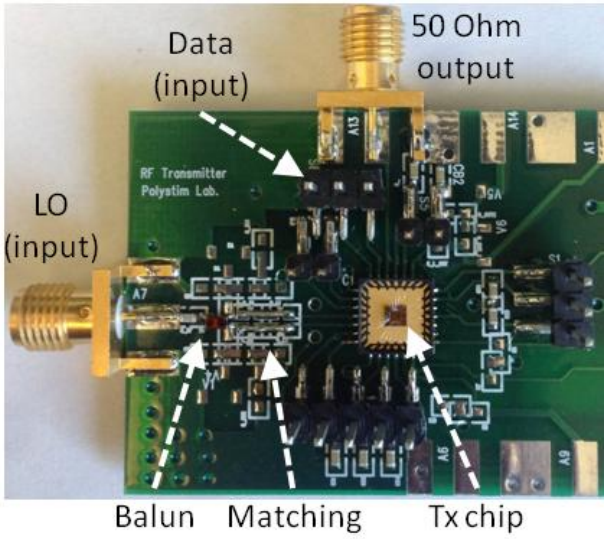


Figure 5.2: The developed Printed Circuit Board (PCB) for measurement

In general, preparing the test setup for high-frequency measurements is a time consuming process and interfacing has usually issues to resolve during the measurements. In this chapter, the post-layout simulation and measurement results are reported and discussed, and the achieved performances of the fabricated transmitter are reported and compared.

5.2 QVCO: Simulation and measurement results

The circuit of QVCO was implemented using IBM 130 nm CMOS technology and a control voltage (VDD_{OSC}) of less than 1.2 V. According to the post-layout simulation results, the frequency can be tuned from 300 kHz to 11.57 MHz by varying the control voltage from ~0.35 to ~0.9 V for a set of parameters (Table 5.1). Figure 5.3 shows the $I+$ and $Q+$ signals of the oscillator with the frequency of 11.5 MHz using the supply voltage of 0.89 V. Figure 5.4 also shows the achieved frequency range and the corresponding current consumption as VDD_{OSC} varies. As mentioned earlier, this oscillator is dedicated to generate differential quadrature signals to define the frequency deviation and to realize the FSK modulation in very low-power RF transceivers. Notice that the oscillator's delay cells are fed through a PMOS transistor and a small voltage drop on this additional transistor is inevitable.

Table 5.1: Parameters of the delay cells for generating the frequency range of 0.3-11.57 MHz

Component	**Size**
M_{p1-4}	30/0.4 (µm/µm)
M_{n1-4}	8/0.4 (µm/µm)
M_{n5-8}	0.5/4 (µm/µm)
C_t	1.4 pF

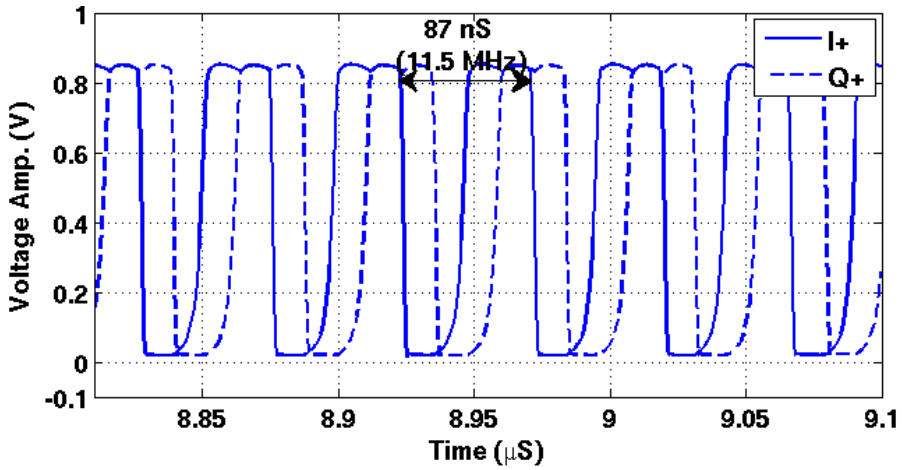


Figure 5.3: Time-domain I and Q signals (related to frequency of 11.5 MHz when VDD_{OSC} is 0.89 V) using the parameters of Table 5.1

An interesting point of this design is highlighted in Figure 5.4 where only 5.5 µA is consumed to generate 2 MHz differential quadrature signals used to define the frequency deviation in FSK modulation for low-power implantable transceivers. Notice that this level of current consumption is actually very important to keep the total current consumption of the transmitter low.

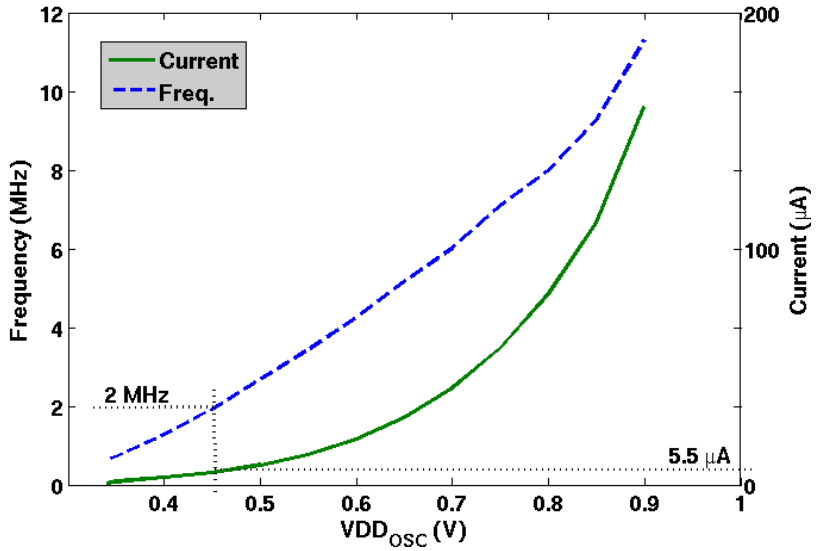


Figure 5.4: Frequency and current consumption of the proposed QVCO vs. VDD_{OSC} related to parameters of Table 5.1

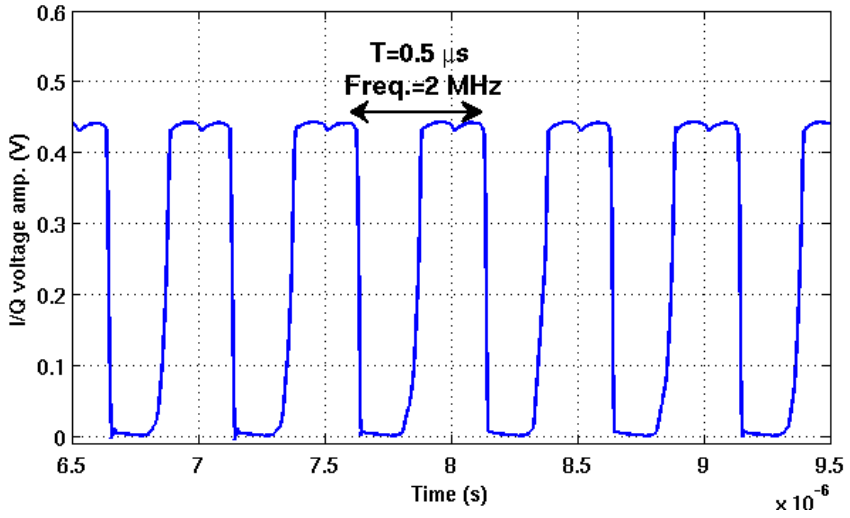


Figure 5.5: A 2 MHz I/Q signal generated by the proposed QVCO with VDD_{OSC}=0.45 V using paramters of Table 5.1

This VCO is not only providing one range of frequency by tuning its control voltage but also can be controlled by other parameters. The capacitance and the transistors' sizing may be changed to achieve another range of frequency. Using the parameters shown in Table 5.2, the frequency range of 3 to 40 MHz can be achieved while consuming a current between 3 and 117 uA, as summarized in Figure 5.6.

Table 5.2: Parameters of the delay cells for generating 3-40 MHz

Component	**Size**
M_{n1-4} & M_{p1-4}	10/0.4 (µm/µm)
M_{n5-8}	0.5/1 (µm/µm)
C_t	0.3 pF

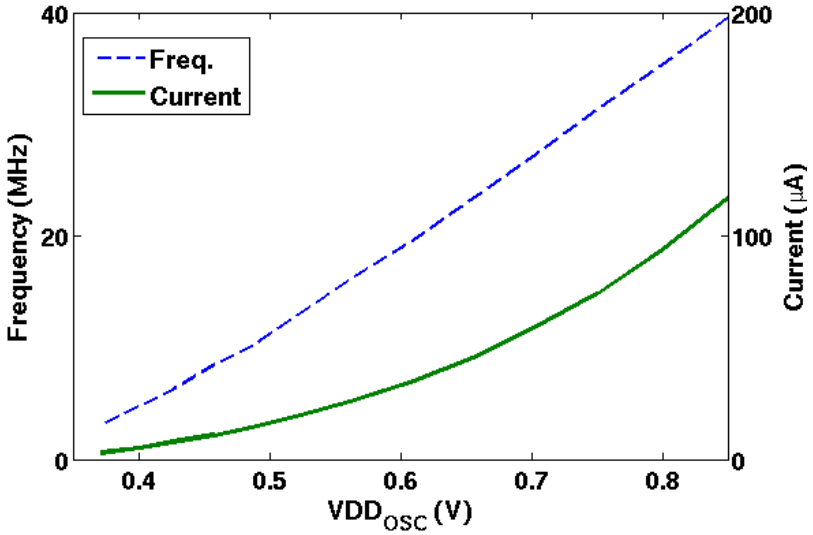


Figure 5.6: Frequency and current of the oscillator vs. VDD_{OSC} using parameters of Table 5.2

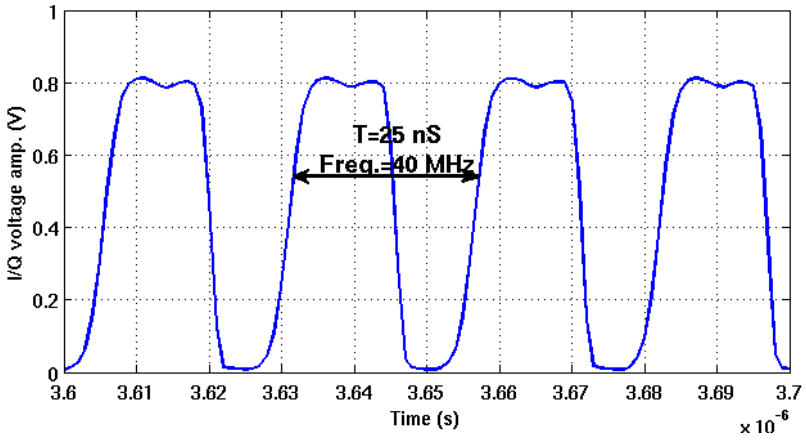


Figure 5.7: 40 MHz I/Q signal generated by the proposed QVCO with VDD_{OSC}=0.45 V using parameters of Table 5.2

The external voltage supply is provided through a PMOS transistor in this design and the sharp rising and falling edges of I and Q signals cause small ripples at their High level due to the existence parasitic capacitors. This effect can be reduced by enlarging the capacitance at the VDD terminal of the VCO in expense of losing some area or using a voltage regulator.

To sum up, a novel low-power rail-to-rail voltage-controlled quadrature oscillator is designed and presented in this section. Eliminating the use of external reference frequency, the

generated differential quadrature signals were used to provide the differential signals with deviation frequency for the FSK-based implantable RF transmitter. The proposed QVCO and its start-up circuits were implemented using IBM 130 nm CMOS technology. According to post-layout simulation results the frequency can be tuned from 300 kHz to 11.57 MHz by varying the supply voltage from 0.35 to 0.9 V while consuming a current between 0.5 and 160 µA. Alternatively, using another set of parameters, the frequency can be tuned from 3 to 40 MHz by varying VDD_{OSC} from 0.37 to 0.85 V and consuming a current from 3 to 117 uA.

To study the effect of the process variation on the oscillation frequency, Monte-Carlo simulation was used with 100 iterations. In addition to the fact that oscillation happens at all iterations, Figure 5.8 shows that the variation in the frequency of the QVCO when parameters of Table 5.1 are used. Histogram of the obtained frequencies is also shown in Figure 5.9.

Monte-Carlo simulation with 100 iterations was also used to verify the effect of process variation on the target signals in the start-up circuit. Figure 5.10 shows the generated voltage of V_p in the start-up circuit for 100 iterations. The corresponding produced delays are shown in Figure 5.11 with the corresponding histogram in Figure 5.12. The delay is, in fact, the time interval from enabling moment of the start-up circuit to the moment that the start-circuit is disconnected from the oscillator blocks.

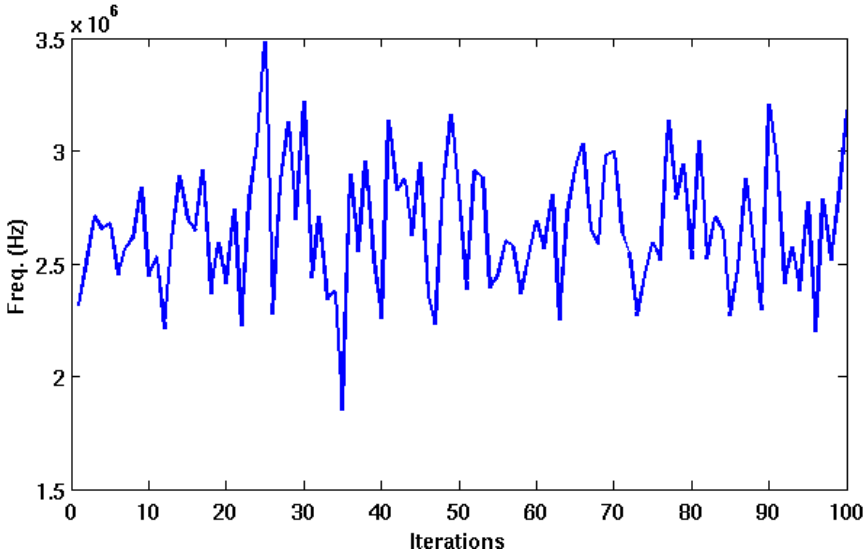


Figure 5.8: Variation in oscillation frequency for 100 iterations of Monte-Carlo simulation for a set of parameters in Table 5.1 when VDD_{OSC}=0.5 V

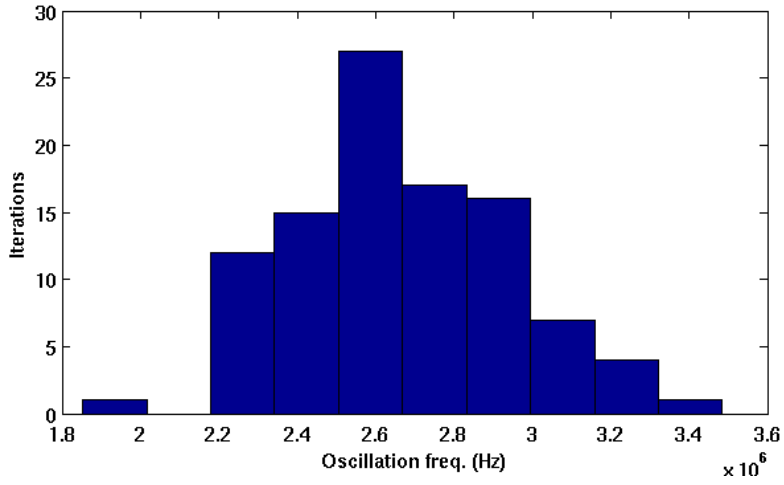


Figure 5.9: Histogram of the oscillation frequencies due to 100 iterations of Monte-Carlo simulation

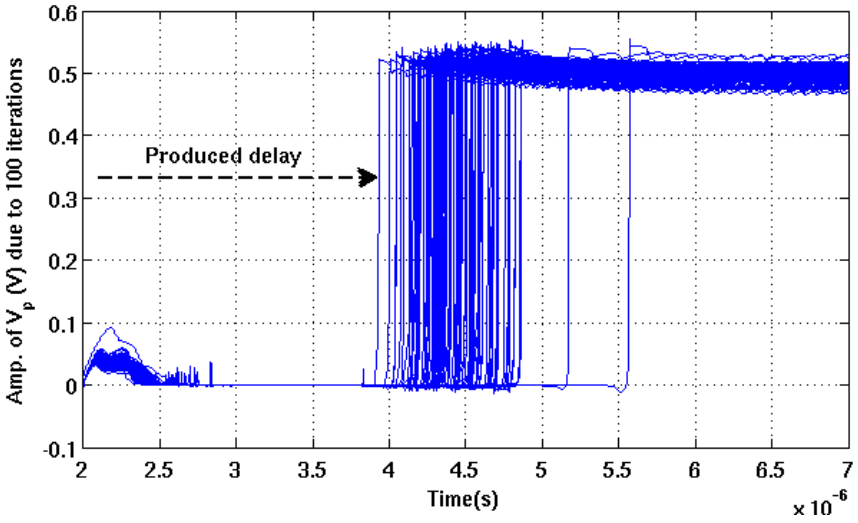


Figure 5.10: Produced signal of V_p in the start-up circuit due to 100 iterations of Monte-Carlo simulation

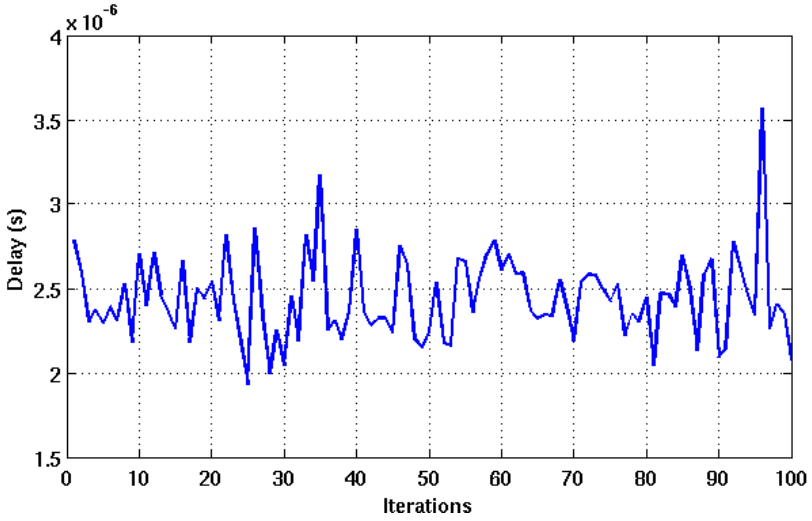


Figure 5.11: Produced delay due to signal of V_p in the start-up circuit due to 100 iterations of Monte-Carlo simulation

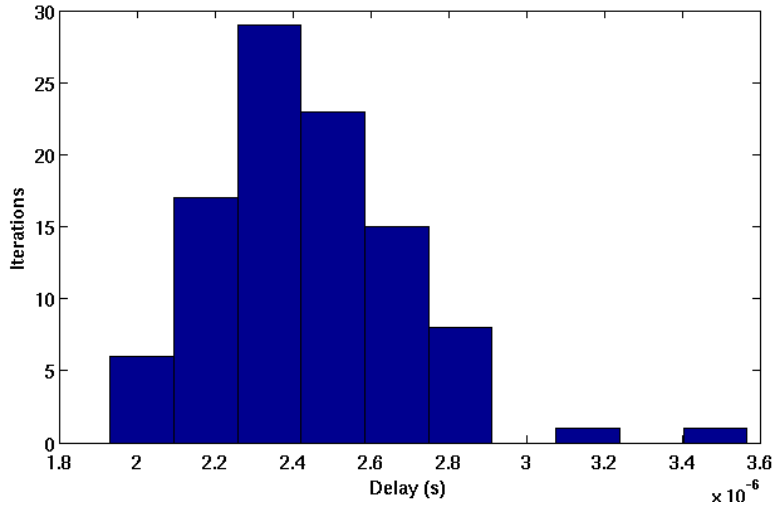


Figure 5.12: Histogram of the produced delays in the start-up circuit due to 100 iterations of Monte-Carlo simulation

Finally, the proposed QVCO was fabricated for testing and verification. Figure 5.13 shows the captured differential I/Q signals on the oscilloscope. In this figure, the frequency is ~250 kHz and the amplitude is ~0.615 V (~1.23 V differentially) when VDD_{ext}=0.75 V. To consider the effect of the parasitic of test setup, capacitive and resistive loads have to be considered in simulations. The measured frequency range is different from the one in simulation

results which is mainly due to the parasitic capacitance of the test-setup. The difference between the current range in measurement and simulation results is also due to the voltage drop on the parasitic resistance. These additional loading capacitance and resistance are actually replacing the capacitance and resistance due to bonding-wires, package, PCB traces, connector headers, external cables and the probes. The small difference between the captured I and Q signals are mainly due to the mismatch, process variation and asymmetrical traces of the test-setup. In practice, to observe the effect of the loading capacitance and resistance of the test-setup a parallel 70 pF capacitor at the output nodes and a series 500 Ohm resistor at the VDD_{ext} terminal were used in simulation. Figure 5.14 shows the measured frequency and current range as a function of the control voltage (VDD_{ext}) in comparison with those from simulations.

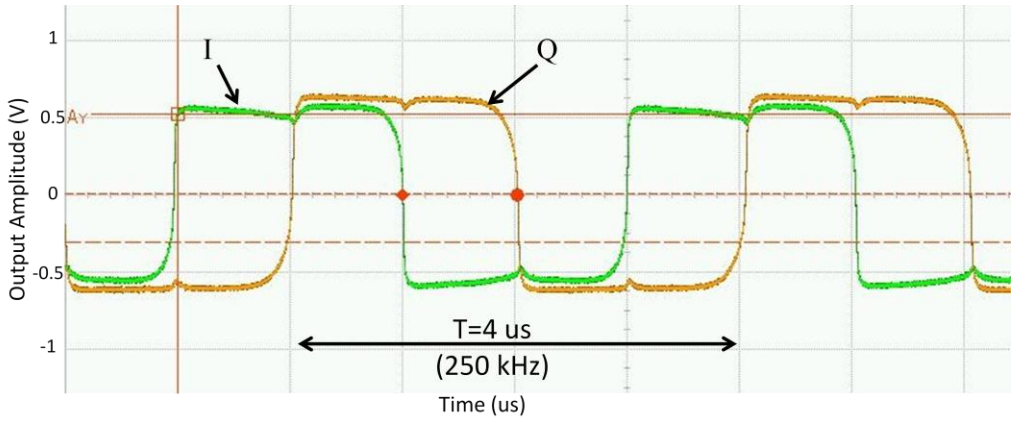


Figure 5.13: Captured differential I and Q signals generated by the fabricated QVCO

As a result, the new QVCO circuit was designed and implemented to provide the differential quadrature I/Q signals. Monte-Carlo simulations also showed that the oscillation will start even if the process variation exists. The simulation and experimental results confirmed the functionality of the proposed QVCO. The effect of the test-setup was considered in simulation in order to compare with measurement results.

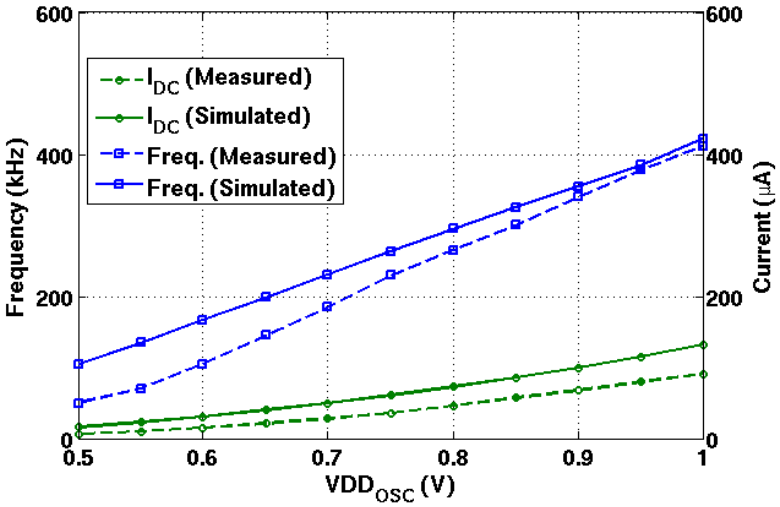


Figure 5.14: Simulated and measured frequency and current consumption of the implemented QVCO considering the external capacitive and resistive loads

5.3 DC simulation and measurements of the fabricated Tx

The DC current consumption of the fabricated transmitter was measured for different samples with negligible variations in the measured values. In total, 5 samples were used in the test setup, where 4 of them were biased as expected and one last sample failed to be biased with zero current drawn from the supply. In practice, a few of the packaged chips were damaged in different steps of the measurements, such as applying larger voltage than VDD to some nodes, and the following reported results are due to 4 available undamaged chips. Prior to the process of wire-bonding, the short-circuit tests were done on each unpackaged die. The effect of inductance of bonding-wires was already considered in simulations. Figure 5.15 shows the simulated and measured total current consumption with the same set of inputs as a function of V_{ctrl}, the control voltage at the gate terminal of the output transistor ($V_{ctrl,R}$ in Figure 4.13). Notice that only small amounts of current are of interest due to the low-power application. According to simulation and measurement results, the maximum current reaches 1.5 mA when V_{ctrl}=1.2 V. Setting V_{ctrl} to a very small value turns off the output branch and the total current, which is the nearly constant, is due to the driver stage. The small drop in the slope of the measured current may be due to the parasitic resistance from the I/O pads to the actual voltage supply. Also, the low voltage drop on the inductor makes the cascode NMOS transistor approaching its triode region when its gate

voltage is at maximum. The highlighted point on the I-V curve is an interesting point of operation with 0.8 mA which is reported together with 0.6 mA considered for the local oscillator.

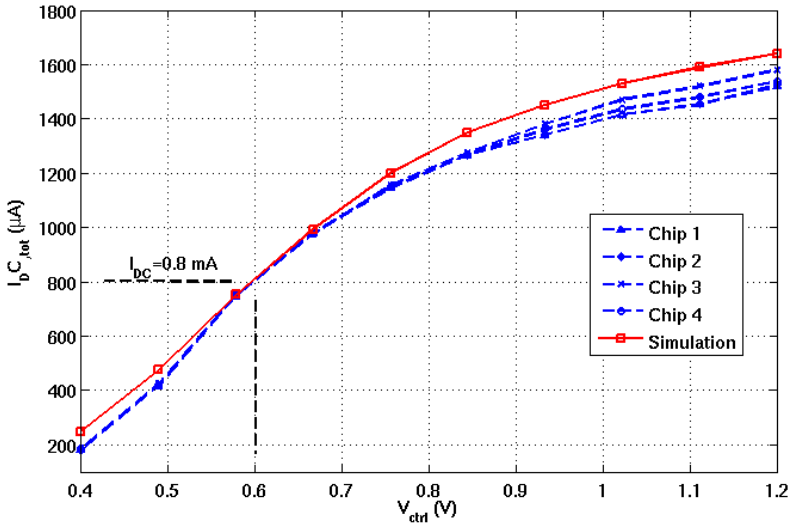


Figure 5.15: Simulated and measured current consumption

Concerning the simulation results due to the design using 90 nm technology, the amounts of current are similar and only the sizing of transistor is varied according to the minimum value for the length of transistors.

5.4 High-frequency simulation and measurements of the fabricated Tx

The simulated time-domain behaviour of the output generated FSK signal is shown in Figure 5.16 where data is varying between ‘1’ and ‘0’ with a rate of 4 Mb/s. Since the frequency is relatively high the envelope can be seen from Figure 5.16 rather than the sinusoidal signal itself and, therefore, the magnified version of the signal is shown. In practice, the envelope of the input signal containing the frequency deviation affects the envelope of the output generated signal. This is obviously due to the fact the inputs of the adding amplifier is coming from the mixers which are controlled by the inputs containing the shifting frequency (V_{fs}). It is not easy to observe that the shifting frequency is mixed with the carrier frequency in time-domain analysis.

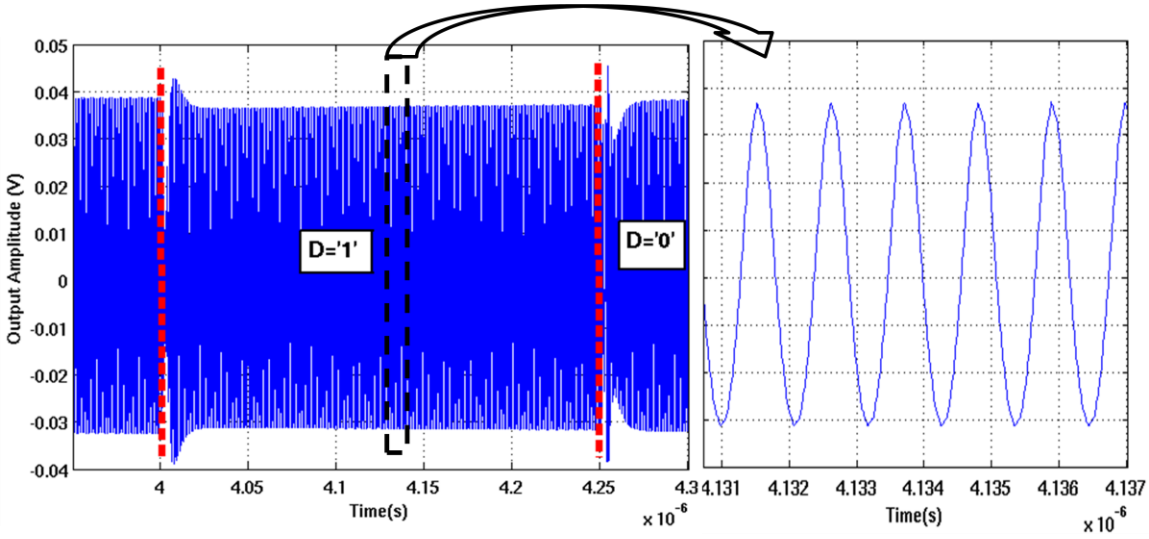


Figure 5.16: Simulated FSK signal when data varies between '1' and '0' with 4 Mb/s rate related to the implemented transmitter using 130 nm technology

In practice, when the low-frequency signals (Data or V_{fs}) have a square-wave shape, the sharp rising and falling edges would propagate through the parasitic capacitances of the mixer and the output stage. The short signal propagation time from the input data to the output node when the data is changed results in a fast settling time, which means the data-rate can go even higher. For instance, the transient behaviour of the output generated FSK signal is shown in Figure 5.17 for data-rates of 8, 10 and 20 Mb/s. In this figure, it can be seen that the settling time starts to be vital as data-rate reaches 20 Mb/s. Notice that, similar to Figure 5.16, the graphs are high frequency signals and the envelope of the output generated signals can be observed. However, the bandwidth is limited in most applications and sampling of the captured high data-rate signal in the spectrum analyzer will be also more difficult.

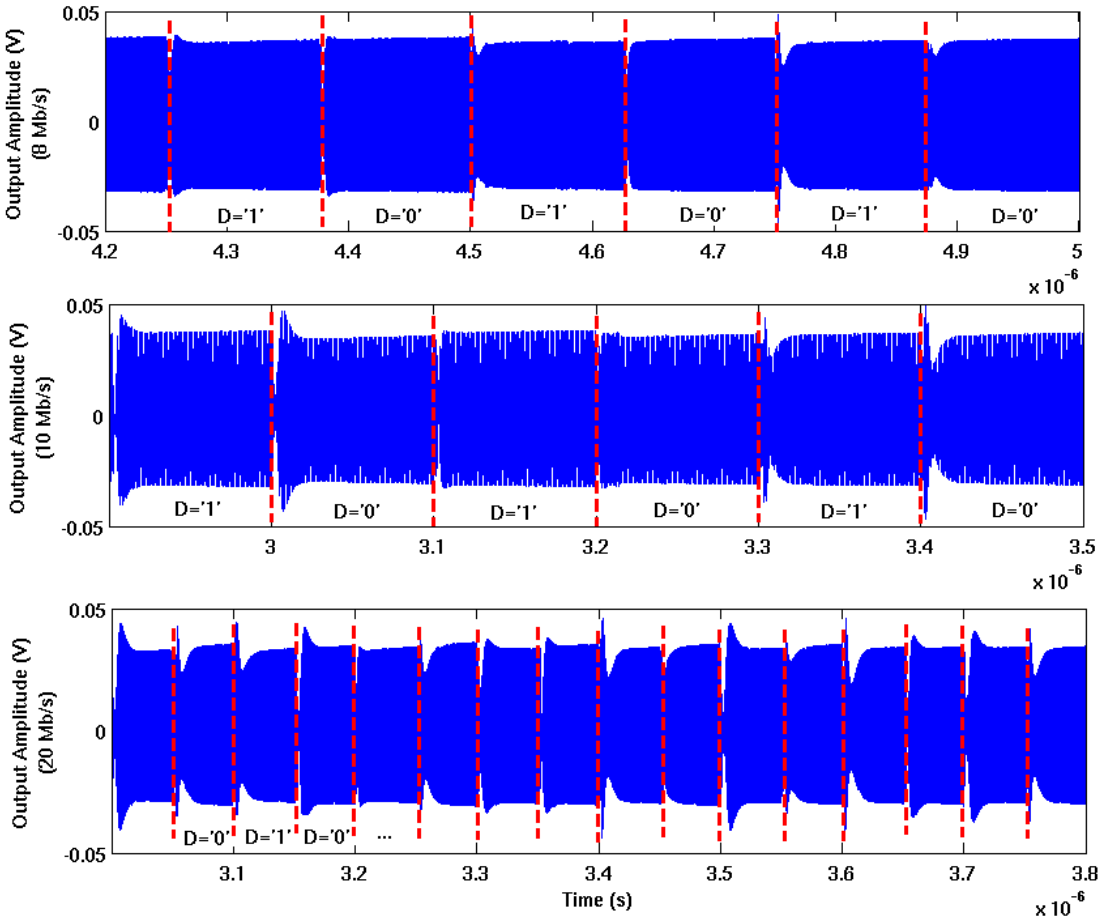


Figure 5.17: Simulated output FSK signal when data varies with 8, 10 and 20 Mb/s rates

Figure 5.18 shows the simulated frequency content of the FSK signal and confirms the existence of the desired frequencies. Notice that in this figure the center frequency was set to 1 GHz for simplicity. As described before, the upper frequency (f_c+f_s=1 GHz + 500 kHz) is generated when the input data is '1' and the lower frequency is for data='0'.

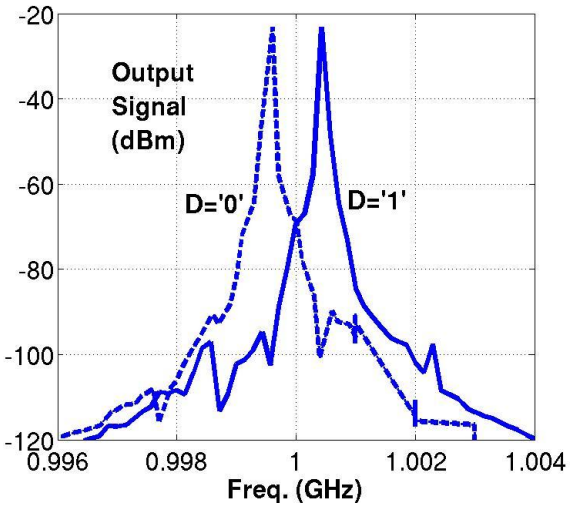


Figure 5.18: Simulated output FSK signals when data='1' or '0' when Δ*f*=0.5 MHz

The output of the fabricated chip was captured using the Spectrum Analyzer (Figure 5.19) for two scenarios of data=’1’ and ‘0’ which is similar to what we had in simulation in Figure 5.18. The noise level of the Spectrum Analyzer is in the range of -80 dBm and the tails of the simulated FSK signals in Figure 5.18 can be partially displayed.

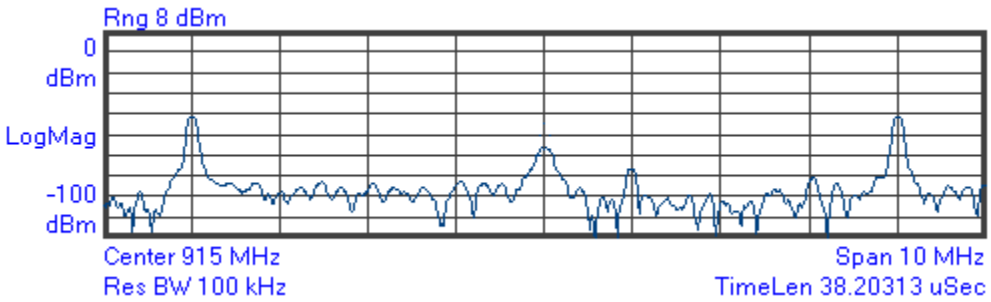


Figure 5.19: Captured output FSK signals when Δ*f*=4 MHz

Characteristics and demodulation properties of the captured FSK signal in Figure 5.19 are discussed in the following. One important phenomenon in the captured FSK signal in the Spectrum Analyzer is the appearance of the unwanted signal with the frequency of 915 MHz, the local oscillator. This is mainly due to LO signal passing through the mixer and appearing in the output node. In other words, any mismatch due to the transistors of the mixers and weak input

matching can increase the amplitude of the unwanted signal. Moreover, radiating the input signal from anywhere in the test-setup to the output node is also helping this phenomenon. Consequently, the receiver or the Spectrum Analyzer has more difficulty in extracting the bits from FSK-modulated signal.

As discussed earlier, the current consumption and the output amplitude can be adjusted by the control signal and in different biasing conditions. Figure 5.20 also shows the output amplitude (P_{out}) as a function of V_{ctrl} for a set of inputs in both simulation and measurement due to 0.13 um CMOS tehcnology. In this case, $P_{out} = 10\log\frac{(V_{out}{}^2)/50}{1\,mW}$ where V_{out} is the RMS value of the output signal. The difference between the simulation and measurement curves is mainly due to the imperfect matching circuit which was very challenging at the time of preparing the test-setup. Notice that this first prototype was implemented to have low current consumption and the PA stage was not optimized for high-output power and high efficiency. Optimization of the PA stage was described in chapter 4.

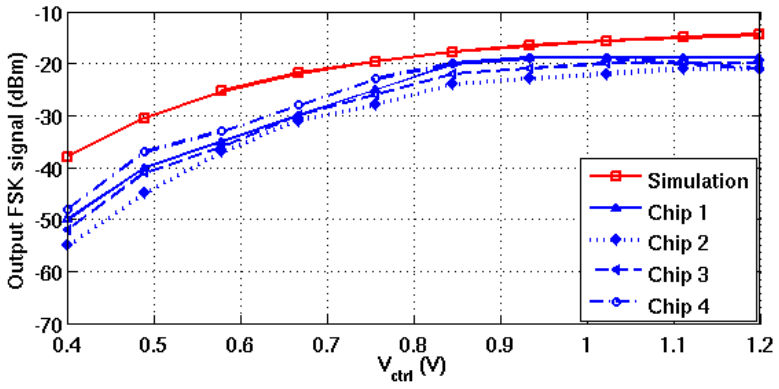


Figure 5.20: Measured and simulated amplitude of the generated output signal (P_{out})

As mentioned earlier, the packaged chips showed expectedly similar results with only difference in the amplitude of the output generated signal which can be adjusted by tuning the consumed current using the control voltages. One other sample also failed in biasing level with zero current drawn from the voltage supply. Figure 5.20 shows the measured output amplitude due to the 4 characterized chips.

The captured FSK signal was characterized by investigating the demodulation properties on the Spectrum Analyzer. The constellation diagram, which shows the possible symbols

generated by the FSK modulation scheme, was observed for the demodulated FSK signal in the Spectrum Analyzer. The deviation from the constellation points is the FSK error, which is an important parameter when comparing the FSK transmitters.

One way of showing the demodulated FSK signal is by showing the variation of the frequency of the captured FSK signal over time. The captured frequency variation over time for data-rates of 100 kb/s, 1, 2 and 4 Mb/s are shown in Figure 5.21, Figure 5.22, Figure 5.23 and Figure 5.24, respectively. These graphs also present the demodulation of the stream of input bit, thanks to the Spectrum Analyzer. Notice that due to the limitation on the channel bandwidth and, hence, the sampling rate, the number of data points on the graphs has decreased as data-rate increases. The captured frequency variation over time for the data-rate of 8 Mb/s is not shown, however, other demodulation properties of the 8 Mb/s FSK signal are shown in Figure 5.25 and discussed.

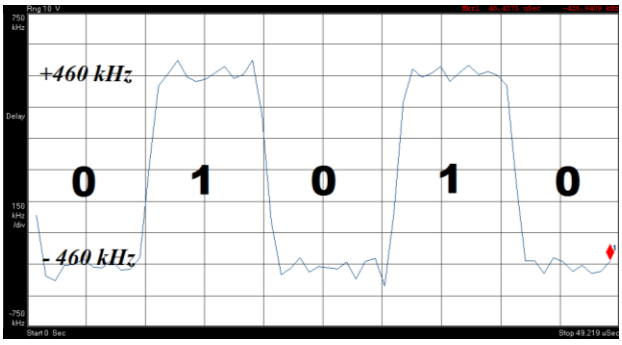


Figure 5.21: Captured frequency variation vs. time for data-rate=100 kb/s and Δf=460 kHz

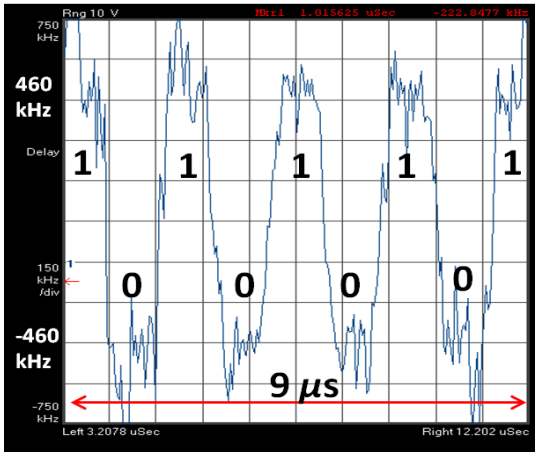


Figure 5.22: Captured frequency variation vs. time for data-rate=1 Mb/s and Δf=460 kHz

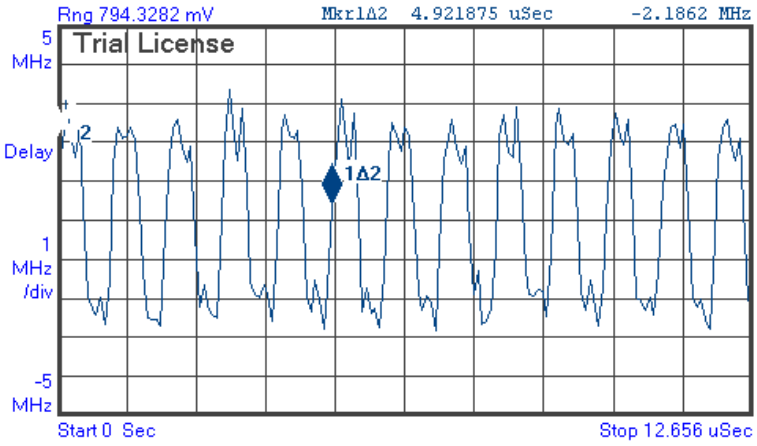


Figure 5.23: Captured frequency variation vs. time for data-rate=2 Mb/s and Δ*f*=2 MHz

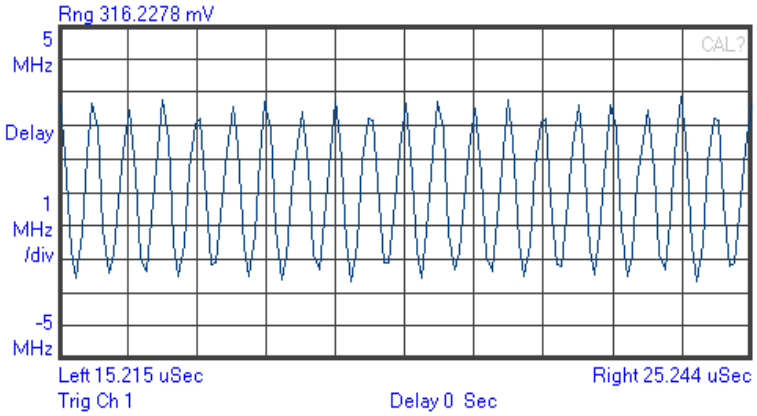
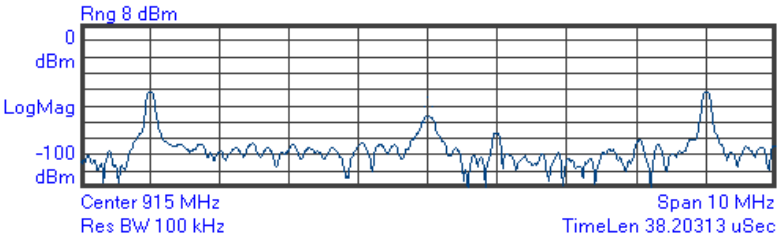


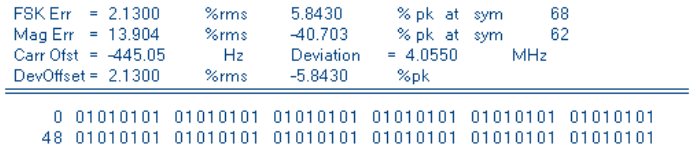
Figure 5.24: Captured frequency variation vs. time for data-rate=4 Mb/s and Δ*f*=2 MHz

As shown in the above figures, limitation in the sampling rate as well as appearance of the unwanted signals in the considered bandwidth does not allow obtaining a sharp square-wave graph, especially for Figure 5.24. However, other demodulation properties presented in Figure 5.25 help understanding the characteristics of the captured 8 Mb/s FSK signal. Larger FSK errors were observed, as expected, at higher data-rates which are not acceptable.

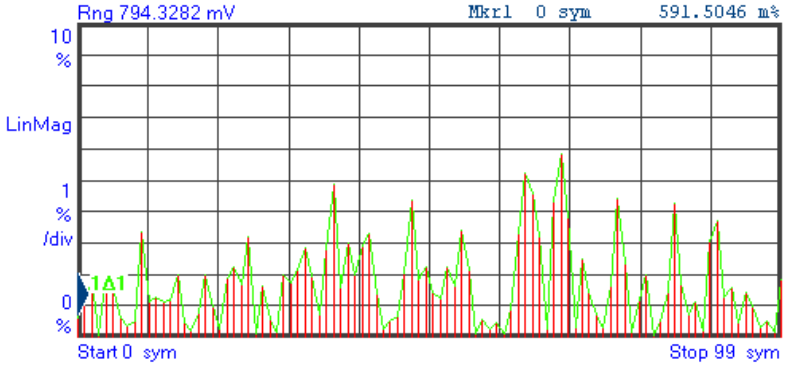
Captured 8 Mb/s FSK signal by Spectrum Analyzer



Extracting 100 bits with an average FSK error of 2.13% when f_s=4 MHz



FSK error for 100 bits



Constellation Diagram

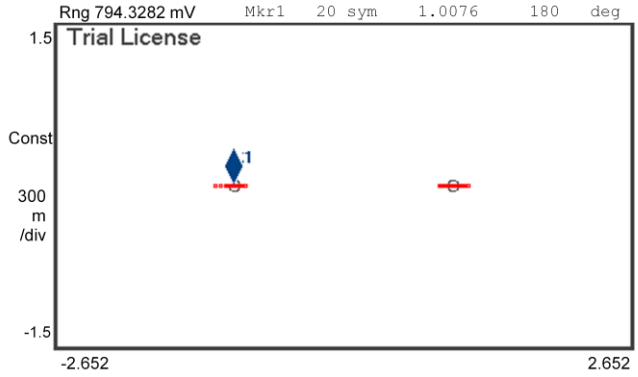


Figure 5.25: Demodulation properties of the captured 8 Mb/s FSK signal with frequency deviation of 4 MHz showing an average FSK error of 2.13% for 100 extracted bits

As observed on the Spectrum Analyzer, the measurement suffers from the jitter issue and the triggering mode was used to lower the effect of jitter by synchronizing the demodulator and the input data. In practice, the demodulator in the receiver, here the Spectrum Analyzer, can easier distinguish between the received frequencies when the two frequencies are farther. But, on the other hand, it has a limited channel bandwidth and, hence, limited sampling rate that means larger error is inevitable at higher data-rates. Here, the maximum bandwidth of the Spectrum Analyzer is 10 MHz which allows having a deviation frequency less than 5 MHz. This is why the shifting frequency of 4 MHz was used in measurements to achieve 8 Mb/s of data-rate. However, more harmonics and interferences will be captured in a wider BW. As mentioned earlier, the approximate required bandwidth is B=2(Δf+DR), where Δf is the shifting frequency (same as f_s) and DR is the data-rate. Therefore, for the channel bandwidth of <10 MHz and the shifting frequency of 2 MHz, data-rate of 3 Mb/s is considered to show very small FSK error. For instance, a small FSK error of 0.64% for 100 extracted bits (Figure 5.26) was observed when f_s=1 MHz and data-rate =1 Mb/s. Consequently, as data-rate is increased larger FSK error is expected which is similar to the achieved measurements.

Average FSK error=0.64%
(f_s=1 MHz &
data-rate =1 Mb/s)

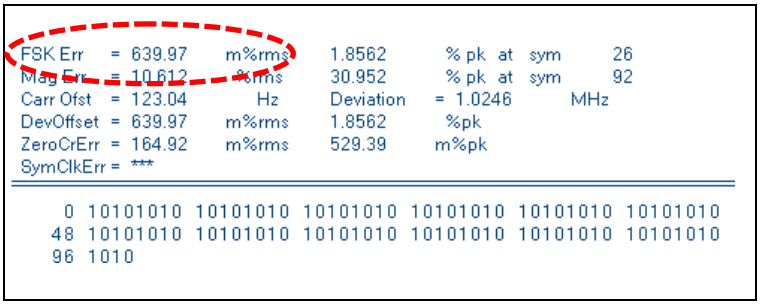


Figure 5.26: Demodulation properties of the captured 1 Mb/s FSK signal with frequency deviation of 1 MHz showing an average FSK error of 0.64% for 100 extracted bits

Testing and measurements issues are also challenging parts of RF circuit implementations and verifications. Providing high quality inputs to the developed testing board might be challenging such as generating the carrier signal in differential mode with exactly 180 degrees phase shift. In this work, the single-pole output from the RF Generator was converted to differential waves using discrete off-chip balun, which can cause a few degrees of phase discrepancy. Moreover, the cross-talk of the high frequency routes before reaching the die is inevitable. The input data (D and DN) may not be perfect square-waves and can suffer from

overshoot when the frequency (data-rate) goes higher resulting in unwanted harmonics. In total, preparing and debugging such high frequency test-setup requires good care and effort and is a time consuming process.

5.5 Comparison and discussion

In this section, the results of the designed binary FSK-based 915 MHz transmitter are compared with other similar transmitters followed by discussion on different parameters and the Figure-Of-Merit (FOM).

Table 5.3 summarizes important parameters of the measurement results of the mentioned transmitters. The typical supply voltage of 1.2 V is used when 130 nm is the fabrication technology. As discussed earlier, comparison of these kinds of transmitters is possible only if all parameters and characteristics are considered. Current Consumption, data-rate with small FSK error and area were mentioned as the main constrains when reporting performance of RF transmitters. As frequently reported, the consumed energy per transmitting bit (J/b) was considered as FOM while simplicity and size must be taken into consideration when making a comparison. In the following, the achieved performance and parameters of the implemented transmitter are discussed and compared with the similar FSK transmitters.

The amount of current consumption is 1.4 mA including 0.6 mA for the local oscillator (implemented in [53]) and 0.8 mA for the presented building blocks of the implemented transmitter, mainly the output stage. As described before, QVCO, mixer, PPF stage and modulation block, have negligible contribution in current consumption. Besides, the reported current consumption (~0.8 mA) and the corresponding output power (-20 dBm) are due to the implemented PA in the fabricated prototype which was optimized later to -12 dBm (Table 4.2). However, the presented transmitter in this work is still competitive with other transmitters.

Table 5.3: Comparison of recent 915 MHz binary FSK transmitters

Ref.	Tech. (um)	VDD (V)	P_{out} (dBm)	Tx Current (mA)	Freq. Deviation	Data Rate	FOM (Energy/bit) nJ/b	Die area (mm^2)
[17] JSSC (2008)	0.13	1.2	-10	2.37	50 kHz	50 kb/s	56.9	16 (Total die)
[18] ASSCC (2009)	0.18	1.8	-14.5	11.5	714 kHz – 3.2 MHz	1 Mb/s (FSK Error: 14.68%)	20.7	3.04 (Total die)
[14] RFIC (2009)	0.13	1.5	-6	1.8	190 kHz	48 kb/s	56.25	1.5 (Total die)
[11] JSSC (2011)	0.18	0.7	-10	1	5 MHz	5 Mb/s*	0.14	0.35 (Active area) (5 off-chip inductors)
[34] Microsemi Co. (2013)	–	1.2 – 1.8	-13	2	450 kHz	180 kb/s	11.7	–
This work	0.13	1.2	-20	1.4$	4 MHz	8 Mb/s (Avg. FSK Error: 2.13 %)	0.21	LO: 0.25# TX: 0.2# (Active area)

* Requires 5 MHz bandwidth for calibration

Estimated from figure including 1 on-chip inductor

$ Including 0.6 mA for the synthesizer [53] and 0.8 mA for the presented Tx

As shown in Table 5.3, the presented transmitter of this work has improved the data-rate and, hence, FOM. The achieved data-rate of 8 Mb/s with an average FSK error of 2.13 % is proving the great performance of the presented modulation scheme and the developed transmitter. This data-rate is high enough to maintain a data communication when a specific protocol with control bits is applied. More than 1 Mb/s was estimated as the needed data-rate for a medical sensor channel. Besides, the reported typical FSK error is around 15% [18] which means the achieved FSK error of this transmitter is in the acceptable range. The data-rate of the transmitter in [11] is up to 5 Mb/s but it has to deal with calibration in a wide frequency locking range and, hence, channel bandwidth of minimum 5 MHz is needed. It also requires several off-chip inductors. The die area was reduced in this work by using less number of external components

and on-chip inductors. The total chip area of the implemented transmitter prototype was 1.4 mm^2 including ESD protection pads with the guard-rings, test circuits and one inductor. The estimated active area of the presented FSK transmitter was around 0.25 mm^2 which is relatively small. However, the area of the previously designed local oscillator should not be neglected. In total, the needed area was considerably reduced and this makes this work suitable for implantable devices.

The reported energy consumption per transmitting bits (FOM) for the recent 915 MHz FSK transmitters of Table 5.3 are alternatively demonstrated and compared in Figure 5.27 where the inclined dashed lines show the constant values of FOM (consumed energy/ transmitting bit). Note that, as another advantage of this work, area was further saved with less number of external components and on-chip inductors. Finally, the measurements showed the functionality and the efficiency of the proposed transmitter up to 8 Mb/s with small FSK error and power consumption. The impacts from the measurement setup will be diminished when the target FSK transmitter is integrated with the digital counterparts in the sensor node and when less external components are involved.

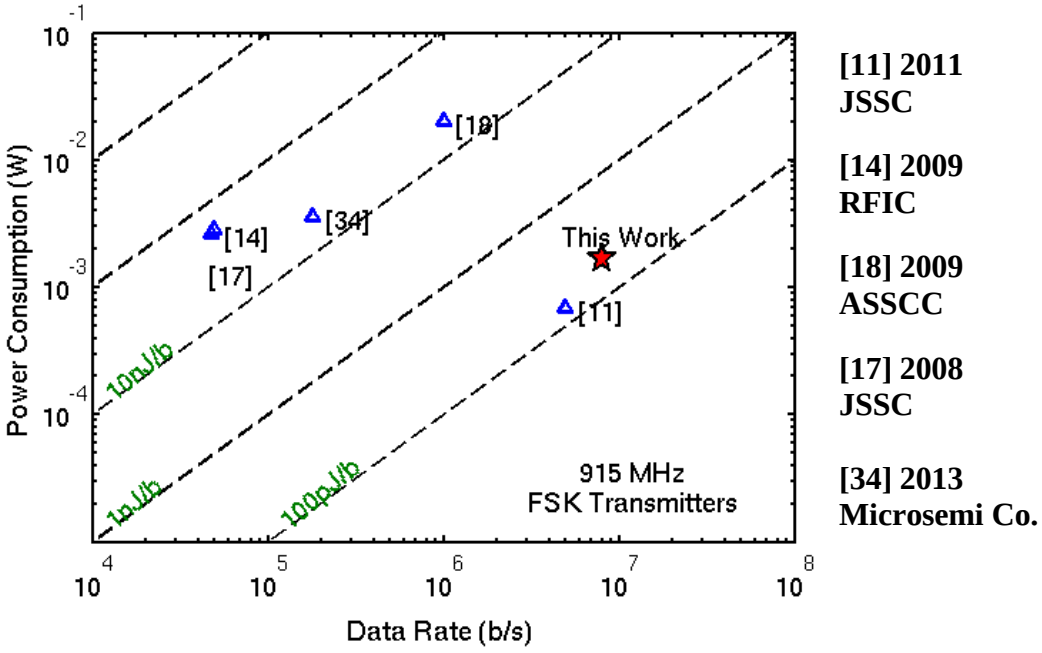


Figure 5.27: Comparison of recent energy-efficient 915 MHz FSK transmitters

5.6 Summary

In this chapter, the DC and high frequency simulation and measurement results of the fabricated chip were presented and discussed. The measured current consumption and output power were compared with the simulation results. The time- and frequency-domain simulation results of the implemented transmitter showed the settling-time as limiting factor of maximum data-rate. The trend of the effect of the settling time for different data-rates and possibility of achieving a data-arte of up to 20 Mb/s depending on the available bandwidth were discussed.

In the measurements, the constellation diagram and extracted bits were reported to show the characteristics of the 8 Mb/s FSK signal with 2.13 % for average FSK error. To further investigate the characteristics of the implemented FSK transmitter, frequency variation over time was observed for different data-rates to demonstrate the demodulation behavior of the FSK signal and FSK error was reported accordingly. Using the high frequency test equipment, the developed test-setup was used to test the fabricated chips and measurement issues were also briefly discussed. The achieved performance of the implemented transmitter was compared with similar state-of-the-art transmitters showing the significant improvement in the concerning parameters and characteristics, meaning current consumption, size and data-rate. In the following chapter, the presented work in concluded and a few recommendations are discussed as future work.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Conclusion

In this research, a radio frequency ISM-band transmitter is designed and implemented. This transmitter is a part of a transceiver dedicated to the interface of wireless and wearable medical implants. It benefits from a new efficient FSK modulation scheme that improves the data-rate, power consumption and size. Different design and implementation stages were studied and presented including the proposed architecture, circuit and layout design and implementation. Simulation and measurement results were discussed and compared with similar transmitters showing the contribution of this work in the field by improving the Figure-Of-Merit, meaning mainly increasing the data-rate and lowering the power consumption. The fabricated transmitter prototype was tested and main parameters were measured using adequate equipment.

The transmitter operates at North-American ISM frequency band (902-928 MHz). The integrated circuits were simulated using IBM 130 nm CMOS technology with 1.2 V supply voltage. The architecture of the proposed transmitter was discussed and analyzed. The building blocks were designed and implemented according to the developed mathematical equations of the proposed FSK modulation scheme, which intended to improve the data-rate and power consumption. Here, the design choices in implementing the circuit of each building block of the transmitter architecture play an important role to achieve a low-power design. Cautious design and implementation of every single circuit in this work directly affect the performance of the target RF transmitter. Implementing the circuits with passive configuration, such as in the poly-phase filter and the mixer, reduced the needed current consumption.

The introduced architecture, the proposed FSK modulation scheme and circuit implementations were initially published in 3 different conference papers, titled as "*A new FSK-based transmitter dedicated for low-power wireless medical transcievers*", 2011 [28], "*A 20 Mb/s 0.084 nJ/bit ISM-band transmitter dedicated to medical sensor networks*", 2012 [29] and "*A 0.084 nJ/b FSK transmitter and 4.8 uW OOK receiver for ISM-band medical sensor networks*", 2013 [30]. Each block was implemented and optimized such that the power consumption and needed chip area is lowered while the modulation block and the mixer require no DC current.

As a novel design, a new quadrature voltage controlled oscillator (QVCO) was introduced to provide differential quadrature signals with very low current with adjustable frequency to realize the required frequency deviation in the FSK architecture. This oscillator is designed to avoid using external reference signal or Crystal oscillators and minimize the number of external components. The results of designing this oscillator was accepted in IET journal, titled as "*A New Differential Rail-To-Rail Voltage-Controlled Quadrature Ring-Oscillator for Low-Power Implantable Transceivers*", 2014. This journal was also selected to be featured in IET magazine. As a result of this design, the related parameters for two ranges of frequencies, meaning 0.3-11.5 MHz and 3-40 MHz, were obtained. For the two mentioned cases, a tuning voltage controls the frequency while the current consumption lies in the ranges of 0.5-160 uA and 5-117 uA, respectively.

The power-hungry output stage was improved, where the power amplifier of this stage was optimized to achieve a power efficiency of ~37%. This output stage was optimized for high output power wearable devices, with high efficiency. The amplitude of the generated FSK signal was decreased for short distance transmission to further reduce the energy consumption in implantable devices.

The layout of the designed transmitter was then prepared for post-layout simulation and fabrication using IBM 130 nm CMOS technology. According to the measurement results of the fabricated chip, a maximum data-rate of 8 Mb/s with 2.13 % average FSK error for 100 extracted bits was measured. The current consumption for the presented building blocks in this work is in a small range of ~ 0.8 mA (for modulator, mixer, QVCO and PA). Considering all concerning parameters, the results were compared with similar 915 MHz FSK transmitters and the Figure-Of-Merit of 0.21 nJ/b (consumed energy per transmitting bit) was achieved. The achieved measurement results were also submitted to Analog Integrated Circuits and Signal Processing (AICSP) Journal, titled as "*An Energy-Efficient High Data-Rate 915 MHz FSK Wireless Transmitter for Medical Applications*", 2014.

This transmitter is dedicated to continuous brain monitoring for patients suffering from Epilepsy. Such implantable transmitters are highly demanded to realize the communication frond-end of biomedical implants. The proposed transmitter in this research is beneficial in any low-power wireless application where an integrated energy-efficient high data-rate wireless

communication interface is needed. The battery cell has a limited life and frequent medical surgeries to replace or recharge the battery are not welcome by the patients, even if other techniques for battery recharging are used. The implemented transmitter in this thesis reduces the total power consumption and, in fact, the rate of data transfer is greatly increased while the required power for transmitting each bit is reduced.

Besides, shrinking the size of the transmitter itself helps to perform more monitoring on patients. For example, patients suffering from Epilepsy require real-time monitoring devices and such integrated transmitter is beneficial to maintain a high data-rate data-communication with an external base station. Performing tests on animals' behaviour is also doable thanks to light and small wireless implants, such as in freely-moving-rat projects. In total, the designed and implemented RF transmitter is contributing in biomedical monitoring and treatments which are hot topics in today's life.

Finally, it is worth mentioning again that different levels of design, implementation and testing of the presented work in this thesis, which were done in Polystim Neurotechnologies laboratories at Polytechnique Montreal, required huge amount of time, effort and hard work. For instance, implementing the designed circuits in layout level is an important engineering task such that a separate team of engineers is only responsible for the layout implementation in most industrial microelectronics jobs. Preparing the necessary and high-quality test-setup to perform precise experiments on the implemented circuits presented in this thesis was very challenging. It was a lengthy process to optimize and improve the test-setup for reducing its effect on the performance of the integrated circuits. Consulting with a few Polygrames members at Polytechnique Montreal, the needed test-setup was further analyzed to improve the quality of the experimental results when capturing and recording the produced signals by the implemented circuits. More than 20 different PCBs, for example, were developed to assess the performance of the designed circuits and to reduce the effect of parasitic components on the quality analysis of the integrated circuits. The reported results in this thesis, which were compared with state-of-the-art, are indeed due to the latest versions of the test-setup which were improved according to the gained experience.

6.2 Recommendations For Future Work

To further reduce the power consumption of the target transceiver design, a high frequency ring oscillator could be implemented to replace the existing local oscillator. In practice, in order to achieve a highly integrated transceiver node, the small area and current consumption of a new ring oscillator may be traded with the phase immunity and programmability of the former designs. Therefore, a new low-power ring-oscillator could further complete the target low-power implantable transceiver. Alternatively, as the next prototype, the transmitter and receiver and the frequency synthesizer should be integrated on a single chip with the same technology to verify the characteristics of the target integrated transceiver.

As another recommended work on generating an ISM-band signal, the new designed QVCO may be modified in order to directly generate the desired FSK signal by adding a multiplier block. In this way, no frequency synthesizer and potentially no external Crystal oscillator are needed. However, the programmability and phase-noise immunity have to be investigated.

In general, the digital domain circuitry in architecture are likely to be implemented as close to the antenna as possible in order to get rid of power-hungry blocks and to benefit from scalability. Analog circuit design techniques require relatively higher attention as each design is customized for different applications. Digital implementation of few blocks may also help reducing the time-to-market. Accordingly, a control unit needs to be developed in order to control the communication protocol between each block such as their power management, etc.

As another difficulty in implementing RF communication front-ends, the size of the antenna has been always an issue for implantable circuits. Some new structures of antenna should be developed to come up with small size of antenna while having a high efficiency power transmission. On-board traces and inductors forming the antenna might be good options for this concern. Especially that inductive-links used in power transfer techniques have the same structure and could share the same inductor with some circuit modifications although they operate at different frequencies. In this way, the area can be further reduced.

The presented architecture in this thesis benefits from passive mixers followed by analog amplifier. A new configuration of adder combined with modulation and mixer stages would help reducing the total size and current consumption. It might be possible to realize the adding stage

using switched capacitors; however, the maximum data-rate might be affected due to needed charge-discharge time.

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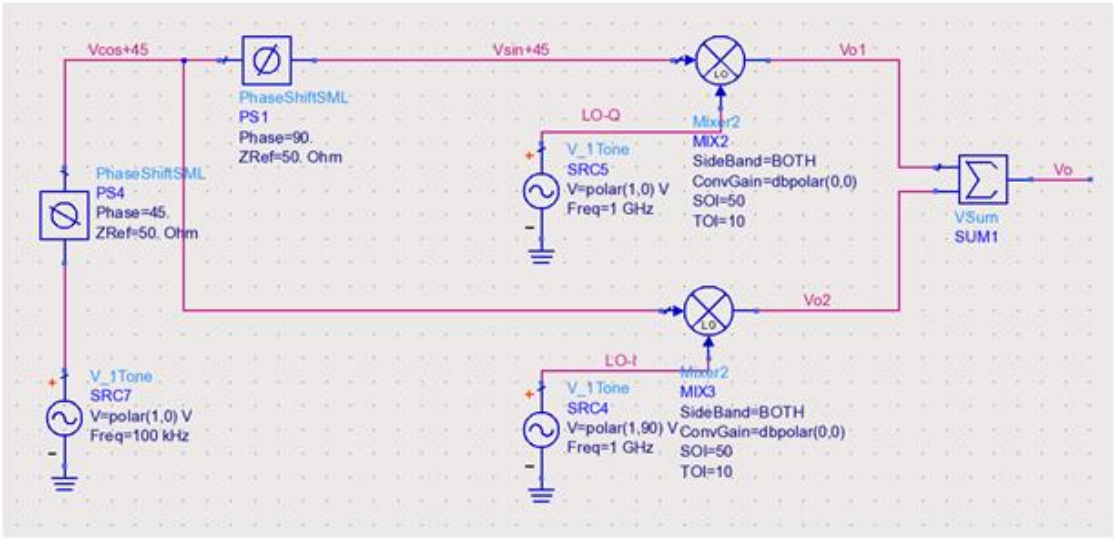
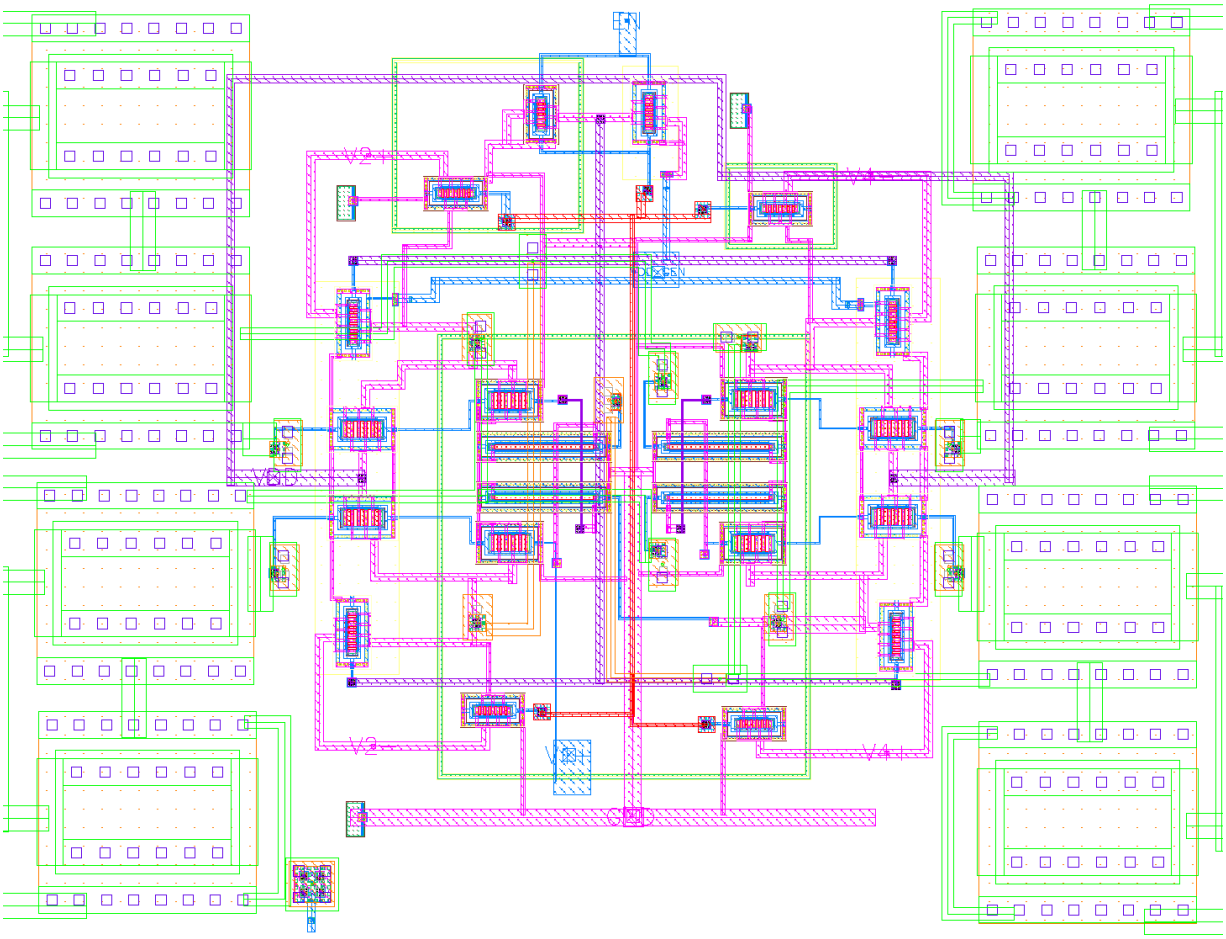
Appendix A Test-bench in ADS

Test-bench used in ADS environment for system-level simulation:



Appendix B QVCO Layout

Layout of the delay cells in the novel QVCO (140 um × 110 um)



Appendix C QVCO's Start-Up Layout

Layout of the start-up circuit used in the novel QVCO (100 um × 60 um)