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SIMULTANEOUS WIRELESS POWER TRANSMISSION AND DATA COMMUNICATION

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DEDICATION

To my parents

To Farshad

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RÉSUMÉ

Le développement rapide des systèmes électroniques sans fil de faible consommation de puissance a conduit à d'innombrables activités de recherche dans le cadre de la faisabilité d'une alimentation à distance ou sans fil de ces systèmes. Par conséquent, la transmission d'énergie sans fil (WPT), qui est développé comme une technique prometteuse pour alimenter les appareils électroniques à longue distance et permettre la conception et le développement de systèmes auto-alimentés, est devenue un centre d'intérêt depuis de nombreuses années. Les antennes de redressement connues sous le nom de rectennas, sont les éléments les plus importants de transmission à longue portée d'énergie sans fil. L'efficacité de rectennas dépend essentiellement de leurs antennes et les circuits redresseurs associés. Par conséquent, pour concevoir une antenne redresseuse à haut rendement qui garantit la qualité d'un système WPT, plus d'attention devrait être concentré sur l'étude, l'analyse et le développement des antennes à gain élevé et redresseurs à haute efficacité de conversion RF-DC. Dans la littérature, différentes configurations de circuit antenne redresseuse, opérant principalement à basse fréquence tels que 2,45 GHz et 5,8 GHz, ont été largement étudiés. Cependant, il existe quelques études rapportées à la fréquence à ondes millimétriques, bien que les avantages de plus petite taille et l'efficacité du système global plus élevée pour la transmission à longue distance peuvent être obtenus à la fréquence à ondes millimétriques.

D'autre part, les circuits rectennas peuvent tout simplement récupérer l'énergie, mais ils ne peuvent pas décoder le signal transmis à des fins de communication. Cependant, la transmission de données est une condition essentielle dans les systèmes de communication sans fil. Par conséquent, si la capacité de détection et de traitement du signal peut être ajoutée à une architecture de rectenna, alors, un récepteur de communication sans fil transmettant simultanément de l'énergie et de données peut être réalisé. La réalisation d'un tel système peut être considérée comme une approche prometteuse pour la prochaine génération de systèmes de communication auto-alimentés.

Cette thèse de doctorat vise à examiner et à démontrer un système de transmission d'énergie sans fil et également un récepteur avec la capacité de récupérer l'énergie et de données de communication simultanément fonctionnant aux fréquences à ondes millimétriques. Pour atteindre ces objectifs, différentes structures de circuit redresseurs sont étudiés, conçus et mesurés expérimentalement. Aussi, différentes antennes sont étudiées et les facteurs requis pour une

antenne WPT sont spécifiés. En outre, cette étude porte sur la conception et les contraintes d'un rectenna fonctionnant à 24 GHz, qui est développé pour démontrer la faisabilité de techniques de récupération et de transmission d'énergie sans fil à ondes millimétriques. La structure proposée comprend un réseau compact d'antennes SIW cavity-backed à polarisation circulaire intégré avec un redresseur auto-alimenté utilisant des diodes Schottky. L'antenne et le redresseur sont individuellement conçus, optimisés, fabriqués et mesurés. Ensuite, ils sont intégrés dans un circuit afin de valider l'architecture rectenna. Le rendement de conversion maximal et la tension continue mesurés sont 24% et 0,6 V, respectivement, pour une densité de puissance de $10 \text{ mW} / \text{cm}^2$. Au meilleur de nos connaissances, l'efficacité mesurée à ce niveau de puissance RF et à cette fréquence de fonctionnement, est le maximum rapporté à ce jour.

En outre, plusieurs architectures de récepteurs sans fil sont étudiées afin de concevoir et démontrer un récepteur de communication sans fil transmettant simultanément de l'énergie et de données. Compte tenu des caractéristiques souhaitables pour récepteurs sans fil tels que faible consommation de puissance, structures simples, compacte et faible coût, les récepteurs-multiports (six-port) représentent une approche appropriée pour concevoir un tel récepteur. Pour ce faire, diverses structures d'une jonction de six-ports sont étudiées et une configuration appropriée basée sur la structure micro-ruban fonctionnant à 24 GHz est réalisée. Un module spécial à haute efficacité de détection, capable de diviser une tension continue avec un rapport spécifique, est conçu et relié au six-port pour réaliser le récepteur. Enfin, la simulation ADS du récepteur six-port capable de récolter l'énergie sans fils et de recevoir les données de communication est présentée, ainsi que les performances en termes de points de constellation et BER comparés au modèle conventionnel.

ABSTRACT

The rapid development of low power wireless electronic systems has led to countless research activities in connection with the feasibility of a remote or wireless powering of those systems. Therefore, wireless power transmission (WPT) has become a focal point of interest since many years, which is being developed as a promising technique, for powering electronic devices over distance and for enabling the design and development of self-powered systems. The rectifying antennas known as rectennas are the most important elements in long-range wireless power transmission. The efficiency of rectennas mainly depends on their antennas and the related rectifier circuits. Therefore, to design a high-efficiency rectenna that guarantees the quality of a WPT system, more focus should be concentrated on the investigation, analysis and development of high-gain antennas and performance-driven rectifiers with reference to high RF-to-DC conversion efficiency. In the literature, different configurations of rectenna circuit, mainly operating at low frequency such as 2.45 GHz and 5.8 GHz, have been widely investigated. However, there are just a few reported studies at millimeter-wave frequency although the advantages of more compact size and higher overall system efficiency for long distance transmission can be obtained at millimeter-wave frequency.

On the other hand, rectenna circuits can just scavenge energy and they cannot decode the transmitted signal for communication purpose. However, the data transmission is an essential requirement of wireless communication systems. Therefore, if the ability of signal detection and processing can be added to a rectenna architecture then a receiver with simultaneous wireless power transmission and data communication can be realized. The realization of such a system can be considered as a promising approach for the next generation of self-powered communication systems.

This PhD dissertation aims to investigate and demonstrate a system of wireless power transmission and also a receiver with the capability of simultaneous wireless energy harvesting and data communication operating at up-microwave and millimeter-wave frequency. To achieve these goals, different structures of rectifier circuit are studied, designed and experimentally measured. Also various antennas are investigated and the required factors for a WPT antenna are specified. Moreover, this study addresses design and implementation issues of a 24 GHz rectenna, which is developed to demonstrate the feasibility of wireless power harvesting and transmission techniques

towards millimeter-wave regime. The proposed structure includes a compact circularly polarized substrate integrated waveguide (SIW) cavity-backed antenna array integrated with a self-biased rectifier using commercial Schottky diodes. The antenna and the rectifier are individually designed, optimized, fabricated and measured. Then they are integrated into one circuit in order to validate the studied rectenna architecture. The maximum measured conversion efficiency and DC voltage are respectively equal to 24% and 0.6 V for an input power density of 10 mW/cm^2 . To the best of our knowledge, the measured efficiency is the maximum reported to date at this level of input RF power and the operation frequency.

Furthermore, several architectures of wireless receiver are studied to design and demonstrate a receiver for simultaneous wireless power transmission and data communication. Considering the underlying desirable features for developing wireless receivers such as low-power consumption, simple structure, compact-sized and low-cost structures, the multiport (six-port) interferometer receivers are selected as a proper approach to design such a receiver. To do so, various structures of a six-port junction are investigated and an appropriate configuration of microstrip six-port junction operating at 24 GHz is designed and prototyped using our in-house miniaturized hybrid microwave integrated circuit (MHMIC) technique. In continue a special high efficiency detector module with ability of dividing DC voltage with a specific ratio is designed and connected to the six-port junction to realize the six-port receiver. Finally, the ADS simulation of the six-port receiver with feature of power harvesting and data detection is presented and its performance in terms of constellation points and BER are compared to the conventional counterpart.

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LIST OF ACRONYMS AND ABBREVIATIONS

AGC	Automatic Gain Control
BPSK	Binary Phase Shift Keying
CMOS	Complementary Metal–Oxide–Semiconductor
CP	Circularly Polarized
EM	Electromagnetic
ESD	Electrostatic Discharge
HB	Harmonic Balance
ISM	Industrial-Scientific-Medical
LHCP	Left-Hand Circularly Polarized
LNA	Low Noise Amplifier
LO	Local Oscillator
LP	Linearly Polarized
MHMIC	Miniaturized Hybrid Microwave Integrated Circuit
MPT	Microwave Power Transfer
MTCE	Maximum Theoretical Conversion Efficiency
PCB	Printed-Circuit-Board
PLF	Polarization Loss Factor
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RFID	Radio Frequency Identification
RG	Ritz-Galerkin

SHC	Sample-and Hold Circuit
SIW	Substrate Integrated Waveguide
SNR	Signal to Noise Ratio
SoC	System on Chip
VNA	Vector Network Analyzer
WEH	Wireless Energy Harvesting
WIT	Wireless Information Transmission
WPT	Wireless Power Transmission

CHAPTER 1 INTRODUCTION

Presently, a large number of power-constrained wireless communication systems are used in various applications from portable entertainment systems to health care devices and wireless infrastructures. These systems are typically powered by batteries that have a limited operation time and they have to be replaced or recharged in order to guarantee the operation of a network for a certain period of time. However, the procedure of battery replacement or recharging may create an undesired expenditure and sometimes is not practical or readily unavailable (e.g., implant devices inside human bodies or for sensors embedded in building structures). Hence, harvesting energy wirelessly from the environment can be a promising solution in providing long-lasting energy supplies for energy-constrained power-limited wireless communication systems. Usually, solar and wind are the well-known renewable energy sources for energy harvesting which may not be available continuously according to the environment, location and weather conditions. Therefore, scavenge energy from ambient RF signals can be a potential alternative in generating clean and renewable power source. Therefore, harvesting RF energy can be a viable new source for wireless power charging and battery-free solutions in many existing and emerging applications such as RF identification (RFID) and wireless sensor networks (WSN) [1].

On the other hand, it is well known that one of the most important concerns in communication systems is their power consumption so that extensive researches are being focused to reduce the required power level of wireless communication systems through the design of low-power receiver techniques. Moreover, to develop wireless communication systems, simple structure, compact-sized, low-cost and wideband transceivers are also points of interest. Considering those mentioned requirements, multipoint receiver techniques based on the principle of interferometer are more practical compared to the other existing receiver configurations since their simple architectures can address most of the above-mentioned issues [2].

Besides, RF techniques have been instrumental for wireless information transmission (WIT). Therefore, since these signals that carry energy can at the same time be used as a vehicle for transporting information, simultaneous wireless power transmission (WPT) and data communication becomes an interesting new area of research that attracts increasing attention toward the development of self-powered receivers. Consequently, in this thesis we have conducted research on the far-field WPT and developed rectennas and wireless receivers with the capability

of energy harvesting and data at the same time in such a way to use the same transmitted electromagnetic (EM) wave to transport both energy that is harvested at the receiver, and information that is decoded by the receiver.

1.1 State-of-the-art of the wireless receiver capable of energy harvesting

1.1.1 Far-field wireless power transmission

Wireless power transmission is considered as a three-dimensional means of transferring electrical power from one place to another. In general, there are three basic wireless powering techniques, namely; short-range induction technique, mid-range magnetically coupled resonance technique and long-range far-field rectification technique [3]. The short-range induction technique is normally used at the maximum distance of a few centimeters. In this technique, the electric current through a primary coil generates a magnetic field which on a secondary coil results in generating a current therein. Two coils are electrically isolated from each other and the transfer of energy takes place by electromagnetic coupling through a process known as mutual induction (non-resonant induction). Over greater distances and when the coils are placed a few meters apart, the non-resonant induction technique is inefficient and wastes much of the transmitted energy just to increase range. An efficient power transmission in this case can happen if the electromagnetic fields around the coils resonate at the same frequency (coupled resonance) which transfer a stream of energy from the transmitting coil to the receiving coil. This technique is a non-radiative energy transfer since it involves stationary fields around the coils rather than fields that spread in all direction.

The long-range wireless power transmission is completely different from the two previous methods and this thesis work focuses on this method of energy transfer. This technique is mostly related to the development of rectennas. The rectenna, the rectifying circuit integrated with an antenna, is the most important module in long-range WPT, whose development has been reviewed in [1], [4]-[6]. The overall performance of a WPT system is normally determined by the efficiency of both the antenna and the related rectifier circuit. Then, it is essential to design high-efficiency rectennas to guarantee the quality of the WPT system.

Until now, most rectenna elements and rectenna arrays have been developed for frequencies below 10 GHz, especially for the ISM (Industrial-Scientific-Medical) bands. Various configurations of wireless rectennas operating at low microwave frequencies; such as 915 MHz and 2.45 GHz, are widely available in the literature [7]-[9]. In general, wireless rectennas are studied from two points of view, namely; operating frequency and RF-to-DC conversion efficiency. For example, a rectenna with 85% and 82% RF-to-DC conversion efficiency operating at 2.45 and 5.8 GHz, respectively, was presented in [7]. The rectennas operating at low frequencies normally aim at harvesting the ambient energy from abundant Wi-Fi and other wireless signal sources. For low-frequency operation, the antenna structure may be limited by its physical and aperture size although ambient electromagnetic power density is relatively high at commonly used wireless frequencies due to its wide-spread deployment for commercial applications and its relatively low-cost wireless power source generation.

So far, only a few rectennas have been reported for the millimeter-wave operation and most of them have focused on single element performances. A rectenna operating at 10 GHz and 35 GHz with respective 60% RF-to-DC conversion efficiency at 140 mW input power and 39% RF-to-DC conversion efficiency at 120 mW input power were presented in [10]. Recently, some studies have been done at 24 GHz [11]-[14]. For instance, [12] describes a rectifier with 54% of efficiency driven by 130 mW input power and 41% with 50 mW. Although the state-of-the-art efficiency of rectennas reported so far is still low at millimeter-wave frequency, the advantages of absolute size reduction and potential high-power density make them more attractive in terms of overall system efficiency for pin-point long-distance wireless power delivery. The development of millimeter-wave harvesters is also driven by ever-decreasing cost and increasing popularity of millimeter-wave technologies and applications including CMOS developments [15] and [16]. A CMOS rectenna operating with efficiency of 53% at 35 GHz and 37% at 94 GHz was reported in [15].

1.1.2 Multiport technique

The multiport interferometer technique was first analyzed in the 1970s by Engen and Hoer in order to propose an accurate power measurement setup [17], [18]. Shortly after its initial publication, the principle was expanded to the characterization of voltage, current, impedance, and phase, resulting in an alternative network analyzer approach [18]. Based on these concepts, a

variety of different applications has been proposed which proves the universal nature of the basic multiport concept [19].

1.1.2.1 Multiport applications

As mentioned above, the multiport circuit technique can be used in microwave network measurements, since it is capable of providing a low-cost measurement of amplitude and phase. Besides, the multiport, in addition to network parameters, can realize power measurements. Using the multiport technique provides a simultaneous power flow and impedance measurement with no need of phase measurements. A detailed description of microwave network measurement could be found in [20] and [21]. Moreover, the multiport technique has many other applications in microwave and millimeter-wave systems where measuring the phase and amplitude of the signal is required such as directional finder, reflectometer and antenna measurement. Multiport reflectometer for measuring the reflection coefficient of a load has been described in [17]. Also, there is a great potential in radar application especially in the automobile industry where low-cost and high performance radar is needed [22]. Furthermore, since the multiport architectures feature low-cost, long-term stability, dynamic range of up to 50 dB, they appear to be suitable for antenna measurement including the near field and polarization [23], [24]. The multiport technique is also used to perform non-destructive permittivity measurements. This technique is appropriate for measuring relatively high-loss dielectric liquids [25]. In addition, the multiport technique has applications in optical systems. The early investigation on the use of a six-port architecture in optics was an optical reflectometer used for measuring optical complex reflection coefficients [26]. An important advantage of this architecture compared to other techniques is the capability to handle high-power signals, enabling the setup of large-signal analysis systems for power amplifier or semiconductor circuits [27].

1.1.2.2 Multiport receiver

The concept of multiport receiver was first introduced in 1994, which has stimulated an important development in wireless receiver design [28]. The underlying multiport receiver principle of operation is related to the additive mixing or coherent interference of radio frequency (RF) and local oscillator (LO) signals through a passive network with a couple of controlled relative phase and amplitude outputs for a direct down conversion through diode power detectors or power

reading. Therefore, the multiport receiver allows increasing the upper frequency limit and decreasing the required power because of the utilization of power detectors instead of mixers.

Professors R.G. Bosisio, Ke Wu and S. O. Tatu who are the pioneers in developing the multiport technique, introduced the up-microwave and millimeter-wave applications of six-port demodulator in connection with homodyne and heterodyne receivers [29]. Since then, the multiport technique has been widely studied and used as an alternative for direct conversion transmitter and receiver for modulating and demodulating signals in different modulation schemes, such as, binary phase shift keying (BPSK), quadrature phase shift keying (QPSK), and quadrature amplitude modulation (QAM).

1.1.2.3 Comparison between multiport receivers and conventional receivers

The six-port receiver has several advantages over its conventional counterpart. First of all, the broadband specifications can be easily obtained by building passive elements. Moreover, the homodyne technique based on the power detection ensures relatively low power consumption because of a relatively low driving power level. In addition, its hardware architecture is simple and cost-effective. Therefore, the multiport based receivers are an expedient enhancement to the group of the available receiving topologies. Especially for high frequencies and large bandwidths, they have been demonstrated as an excellent alternative to the common architectures [30]. To enable a serious validation of the multiport technology, a benchmark has been done between the six-port receivers and the existing receiver architectures from several points of view [31], [32].

1.1.2.4 RF performance

Phase accuracy: In conventional receivers, the phase noise of the local oscillator (LO) is directly converted to the phase noise in the complex baseband. This phase noise leads to a neighbor channel interference, caused by reciprocal mixing, and thus reduces the selectivity of the receiver. In the case of the direct conversion receiver and six-port receiver, an additional phase inaccuracy is introduced because of the inaccurate calibration. With this unavoidable phase imbalance, a phase distortion is generated [33].

Noise figure: The noise figure is usually defined by the LNA stage of a receiver. If no LNA is used in the structure of the receiver, the noise of a mixer is comparable to the noise of a power detector. For frequencies beyond 50 GHz, both are usually built up using Schottky diodes. The

noise figure for diode mixers is close to its conversion loss which is typically about 7 dB [34]. Simulations on microwave power detectors using a beam lead GaAs Schottky diode have shown that the noise figure can be lower than 4.8 dB for input power smaller than -20 dBm.

LO power: For most mixers, to obtain a good conversion loss, the LO power should be in the range from 0 to 10 dBm [34]. In the six-port receivers, a suitable condition is a LO power in the area of the receiver input power which is much lower in practical applications (less than -10 dBm).

In-band dynamic range: The dynamic range of six-port receiver is mainly determined by the accuracy of calibration and detector sensitivity. First trials have shown a dynamic range of 40 dB [35], [36]. It must be noticed that the calibration limits the linearity of the receiver. The dynamic range of mixer based receiver is limited by the linearity and 1 dB compression point of -10 dBm to 10dBm. This results in a dynamic range of about 90 to 100 dB for a signal bandwidth of 10 MHz. The dynamic range of the receivers can be improved up to 70 dB using an AGC inserted within the LNA [29].

Self-mixing effects: Direct coupling and external reflections can cause a DC offset in the direct conversion receivers and six-port receivers since the desired baseband signal as well as the unwanted DC offset are both centered at DC, therefore they cannot be separated by filtering. The six-port receivers are less sensitive to the DC offset because this problem is mitigated by the calibration procedure, but the direct conversion receivers contain some signal processing unit to cope with this effect [32].

1.1.2.5 Constraints

Size: Major part of a mixer-based receiver is occupied by active components and filters which are large in size and cannot be integrated on the chip while the usual size of a six-port is about $\frac{3}{4} \lambda$ in square, and for V, W and D band applications, it is possible to integrate the six-port on a chip.

Cost: The cost of a direct conversion receiver depends on the frequency range. At high frequencies especially in D and W band, mixers are expensive and in some cases they are rare whereas power detectors are available for higher frequencies. For millimeter-wave signal generation, usually a lower frequency LO is followed by a frequency multiplier, which produces a

small LO power. The six-port receivers will have a cost advantage by reducing the LO power requirements.

According to the above comparisons and discussions, it is clear that the six-port receiver is a suitable and cost-effective alternative to the existing systems, especially for millimeter-wave applications. At millimeter-wave frequencies, the neighbor channels interference are negligible so the reduced dynamic range is acceptable. In addition, it has been proved that the six-port receiver architecture is less sensitive to LO power variations and phase errors than the antiparallel diode receivers [32].

1.2 Motivation and research objectives

Therefore, according to the above-mentioned backgrounds, the need for a high efficiency rectenna operating at millimeter-wave frequency as well as a proper architecture of low-power wireless receiver design have motivated our research to realize a quality receiver for simultaneously wireless power transmission and data communication.

The overall objective of this thesis is to develop a wireless receiver for simultaneous wireless power transmission and data communication using the multiport technique. To be more specific, there are three main objectives as follows:

1. To investigate different configurations of a rectifier circuit and to propose a simple architecture with high RF-to-DC conversion efficiency operating at up-microwave and millimeter-wave frequency under low/medium RF power level;
2. To determine specifications required for antenna selection in regards to WPT applications and to design a high gain millimeter-wave rectenna array;
3. To propose a new structure for the six-port receiver in order to present an innovative receiver with the capability of simultaneous wireless power transmission and data communication.

1.3 Methodology

To achieve the objectives of this thesis, we have taken the following steps:

1. The required conditions to design the rectifier circuits (using Schottky diode) with high RF-to-DC conversion efficiency are examined in terms of appropriate diode selection and circuit design. It is well known that the maximum efficiency of Schottky diode rectifiers is limited by the maximum operating frequency and the loss of the system. Therefore, the internal analysis of Schottky diodes dealing with rectifying element characteristics as well as the external analysis considering the component modeling and matching effects are investigated in detail.
2. Various architectures of rectifier are studied from the points of view of the required RF power and operating frequency. Then, the common structures of rectifiers are modified to make them operational at up-microwave and millimeter-wave frequency. Consequently, three different structures of high efficiency rectifier operating at 24 GHz and 35 GHz are designed and their performance are examined experimentally.
3. Different antenna configurations are investigated with regards to the required specification for WPT applications such as gain, polarizations, weight and fabrication techniques. Since, in a WPT system, an antenna plays an important role in receiving RF power, then its performance is a critical factor in determining the overall efficiency of the system.
4. Considering the required criteria for a WPT antenna, a proper structure of WPT antenna array operating at 24 GHz is designed and experimentally tested. Then, it is integrated into the designed low-power rectifier to realize the WPT rectenna.
5. To validate the idea of a system with the capability of simultaneous wireless power transmission and data communication, different configurations of wireless receiver are studied. Considering the desirable requirements of a wireless receiver such as low-power consumption, compact-sized and low-cost, the use of a multiport technique is an appropriate solution that addresses all the above-mentioned concerns. Figure 1.1 shows the flowchart of the proposed system to provide wireless power transmission and data communication at the same time using the six-port technique. Since it is shown in Figure 1.1, the detector module of the six-port receiver, should have a special design which can

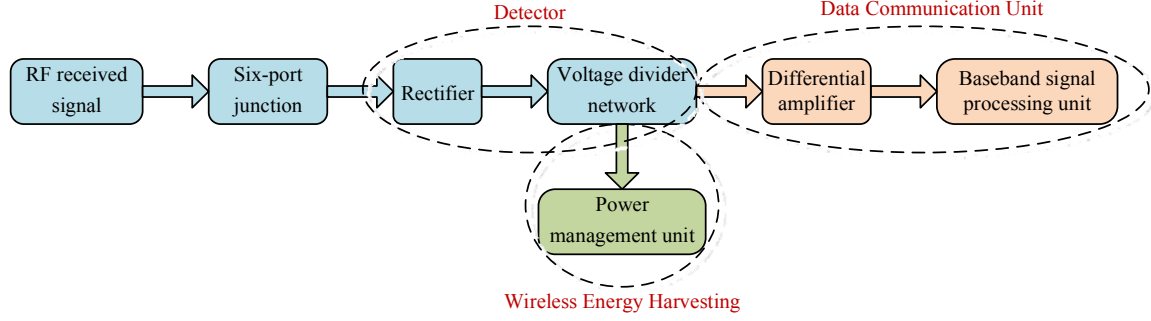


Figure 1.1: Flowchart of simultaneous wireless energy harvesting and data communication.

split the generated DC voltage with a specific ratio in order to harvest the energy and perform the data detection.

6. Since the designed six-port junction is used in a power harvesting structure, it has to have the minimum passive loss to transfer as much as possible RF power to detectors. To do so, one with the lowest loss is selected among the different configurations of six-port junction, designed and optimized to operate at the desirable frequency (24 GHz in this case).
7. The detector of interest has to generate more DC power, therefore it should act as a rectifier with a high RF-to-DC conversion efficiency. This rectifier is designed considering the required conditions such as low-power (maximum power of 10 dBm), operating at up-microwave frequency (24 GHz) with the ability of dividing the generated DC power with a specific ratio.
8. After the detection module, some part of the DC voltage is transferred to the differential amplifiers to realize the I and Q data detection (analog signal detection [37]) while the rest is harvested.

1.4 Original contributions

The original contributions of this thesis can be summarized in the following:

- A self-biasing technique is presented as an efficient approach to reduce the required power of rectifiers and design low-power rectifier circuits. To justify the claim, a 24 GHz self-biased rectifier is designed and prototyped. The measurement results

show that the self-biased rectifier is more efficient than the conventional designs when the available RF power density is low.

- In order to increase the efficiency of the rectifiers, an original idea is put forward to harvest harmonics generated by the nonlinear rectification process in the millimeter-wave rectifier. To validate the proof of concept, a 35 GHz harmonic harvester rectifier is designed, fabricated and experimentally tested. The measured efficiency has the maximum value compared to the conventional rectifiers (without harmonic harvesting or recycling) reported in the literature.
- A robust investigation of up-microwave and millimeter-wave rectennas is presented to maximize the harvested DC power. Consequently, a 24 GHz compact rectenna is developed to demonstrate the feasibility of wireless power harvesting and transmission techniques towards millimeter-wave regime. To the best of our knowledge, the designed rectenna has the highest efficiency reported to date compared to the previous studies.
- An original idea of simultaneous wireless power transmission and data communication is presented. The proposed system is based on the six-port technique in connection with a special architecture of rectification circuit which acts as a detector and also a rectifier both to achieve data extraction and high efficient RF-to-DC rectifying functions.

In summary, this thesis addresses all the design issues from system-level analysis to component-level design, from CAD simulation to experimental validation and from original idea to prototype implementation.

1.5 Thesis outline

This thesis details research works performed on planar modeling of Schottky diode and fabrication procedure, nonlinear rectifier circuit analysis, rectenna design issues for applications of wireless energy harvesting, and finally a system of simultaneous wireless power transmission and data communication. The thesis is organized as follows:

Chapter 2 provides a general description of the Schottky diode technology. It initiates with the basic diode operating principle, and further discusses the issues specifically related to the planar diode structure. At the end, the diode design, optimization and fabrication principles for rectifier applications as well as the simulation and measurement results are presented.

Chapter 3 develops an analysis of nonlinear rectifiers and derives the required conditions to achieve a maximum efficiency rectification. It begins with a review of different configurations of rectifier and then explains the design steps to realize an up-microwave/millimeter-wave rectifier with a maximum RF-to-DC conversion efficiency. A 24 GHz voltage doubler rectifier is designed and experimentally tested. The self-biased technique is presented as a method to reduce the required input RF power and consequently design a low-power rectifier. A self-biased rectifier is developed and prototyped at 24 GHz to justify the claim. Finally, the harmonics generated through the rectification process are investigated using some analytical approach based on Ritz-Galerkin (RG) technique. It is shown that some parts of power are wasted in harmonics which are normally filtered out by some DC-pass filtering after passing through the Schottky diode, then the idea of harmonic harvesting is introduced to increase the overall efficiency. To validate the idea, a 35 GHz harmonic harvester rectifier is designed, optimized and fabricated.

Chapter 4 addresses the integration issues between rectifiers and antennas to realize rectennas for wireless powering. Various configurations of antennas are studied considering WPT applications. Subsequently, two rectennas are designed and experimentally demonstrated on the example of a linearly polarized SIW slot array with a voltage doubler rectifier and a circularly polarized SIW cavity-backed in connection with a self-biased rectifier. Calibration, circuit validation, impedance matching to nonlinear impedances, DC collection circuit design and integrated rectifier-antenna characterization are all presented in detail.

Chapter 5 presents the idea of a simultaneous wireless energy harvesting and data communication system based on the multiport interferometer technique. This chapter begins with a brief review of different configurations of wireless receiver and it explains the reason of choosing the multiport technique to design such a system. Consequently, different structures of a six-port junction are studied and their related s-parameters are extracted. A proper configuration of six-port junction operating at 24 GHz is designed and prototyped using our in-house miniaturized hybrid microwave integrated circuit (MHMIC) technique. The designed six-port is used to build up the

receiver. Then, the design process of a special detector module with high RF-to-DC conversion efficiency is explained. Next, the designed detector is connected to the six-port outputs to realize the receiver. Finally, the ADS simulation of the six-port receiver featuring both power harvesting and data detection is presented and its performance in terms of constellation points and BER are compared to the conventional counterpart. The simulations start with the ideal component models provided in ADS and end up with much more realistic models obtained in EM simulations and measurements.

Chapter 6 summarizes the thesis work with a concise conclusion and gives some future directions of our research in this interesting area of microwave engineering.

CHAPTER 2 PLANAR SCHOTTKY RECTIFIER DIODES

Generally, a Schottky diode can be used in designing mixer, detector or rectifier circuits. However, the required features for a mixer Schottky diode differ from the required specifications for a rectifier Schottky diode. Moreover, microwave rectification using Schottky diode has been widely discussed in the context of energy harvesting and WPT. Therefore, in this chapter we intend to have a closer look at rectifier Schottky barrier structure by itself, to understand about the nature of rectification. Even though, the commercial Schottky diodes have been used in our fabricated WPT systems.

In 1904, the first practical semiconductor device was introduced and in fact it was a metal-semiconductor contact which showed a certain rectifying behavior. In 1938, Schottky suggested that the rectifying behavior could arise from a potential barrier [38]. This was later named as Schottky diode. Since Schottky diodes play an important role in the development of high frequency electronics as rectifier especially for millimeter-wave rectification, this chapter provides an overview of the Schottky diode operation. Therefore, general physics of the metal-semiconductor interface forming a Schottky barrier and the corresponding diode equivalent circuit model are discussed briefly. Consequently, the diode operation as a rectifier is described and the design parameters for rectifier and performance optimization are given. Furthermore, some initial results of our in-house fabricated prototypes of a planar rectifier Schottky are presented.

2.1 Summary of Schottky diode operation

When a metal makes contact with a semiconductor, a barrier is formed at the metal-semiconductor interface. The fundamental operation of a Schottky diode is regarded to carrier transport mechanism over a Schottky barrier. This barrier is responsible for controlling the current conduction as well as its capacitance behavior. The metal-semiconductor interface and the corresponding diode terminal notation is presented in Figure 2.1.

In designing the Schottky diodes, both n-type and p-type semiconductors can be used. In n-type Schottky barriers, the forward current results from electron movement from the n-type semiconductor into the metal while in p-type Schottky, the forward current drives from holes movement from p-type semiconductor into the metal.

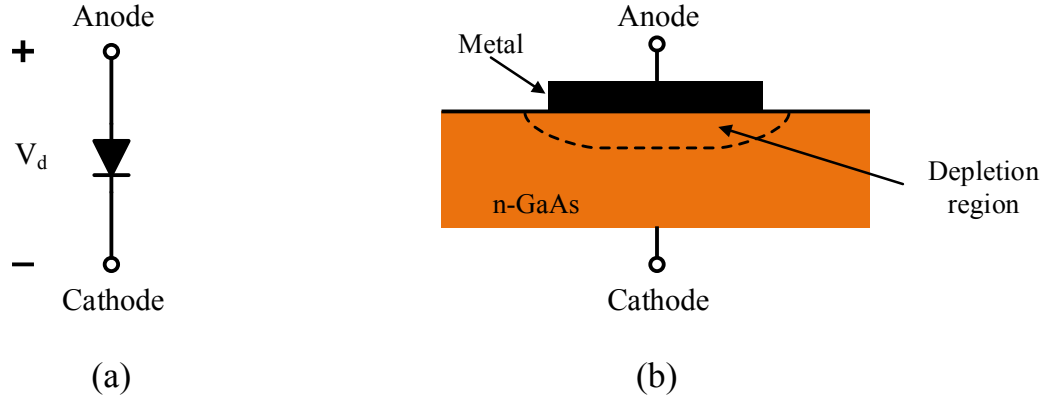
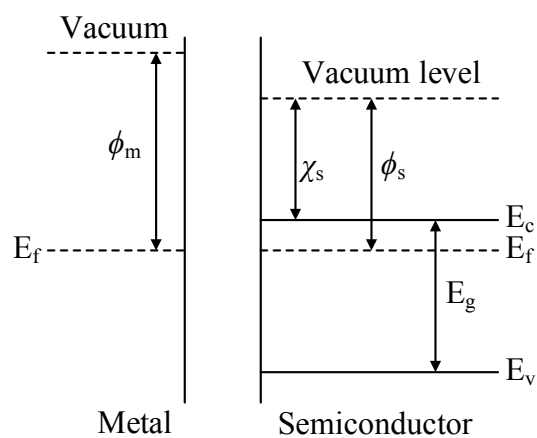


Figure 2.1: (a): Symbol of a diode; (b): Metal-semiconductor interference in a Schottky diode.

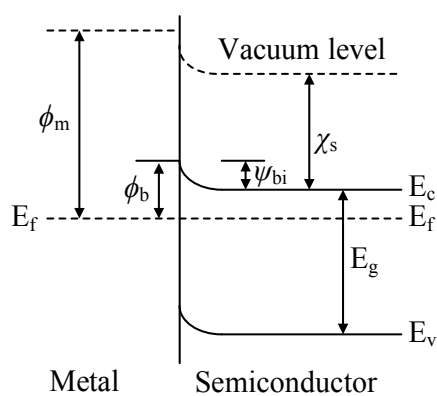
Since in Schottky diodes only one type of semiconductor (n-type or p-type) exists, therefore slow and random recombination of n-type and p-type carriers does not happen. For this reason, Schottky diodes are much faster in conduction and unlike junction diodes, they do not have any delay effect due to the charge storage. It means that, in Schottky diodes, when the forward voltage is removed, the current flow stops instantly and reversed voltage is established in a few picosecond [38].

2.1.1 Metal-semiconductor contact [38]

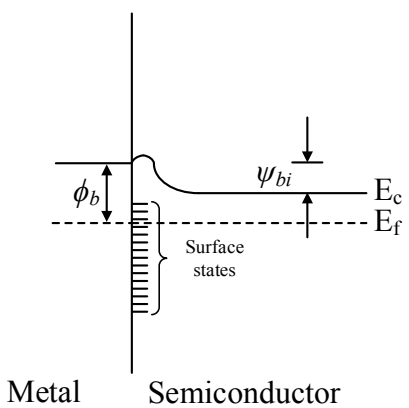
According to Figure 2.2, when the metal and the n-type doped semiconductor are separated from each other, the metal-semiconductor band diagram looks completely different from the band diagram of the time they are in contact. In an intimate contact, electric charge will drift from the semiconductor to the metal and a thermal equilibrium is established. The Fermi level on both sides will line up. Relative to the Fermi level in the metal, the Fermi level in the semiconductor is lowered by an amount equal to the difference between the two work functions. This band diagram is explained in detail in [38]. In the thermal equilibrium condition, the semiconductor region next to the metal contact is depleted of electrons and electron movement from the semiconductor to the metal is blocked by an energy barrier, identified as built-in-potential, ψ_{bi} . By changing the potential between the metal and semiconductor, i.e., when an external bias is applied over the diode terminals, the width of the depletion layer $\omega_d(V_j)$ as well as the built-in potential is changed.



(a)



(b)



(c)

Figure 2.2: Energy band diagram

For an ideal contact, a barrier height ϕ_b is calculated as the difference between the metal work function ϕ_m and semiconductor electron affinity χ_s . ϕ_b is an important factor as it determines the LO power required to bias the diode in its nonlinear region. In many millimeter-wave applications, the LO power is at premium and, therefore, low barrier Schottky diodes are desired. In practice, the barrier height dependency on metal work function is weak compared to the ideal case. Experimental characteristics showed that the estimation of a practical barrier height is rather complicated [39]. The physics of the metal-semiconductor system can be found in the literature [40]-[46].

Table 2.1 shows some experimental values of barrier height of different Schottky diodes ranging from 0.15 to 0.9 V [47].

Table 2.1: Experimental values of metal-semiconductor barrier height in volts

Metal	ϕ_b Si (n-type) (111) (V)	ϕ_b Si (p-type) (111) (V)	ϕ_b GaAs (n-type) (100) (V)
Au	0.81		0.9
Ni	0.3	0.8	
Mo	0.6		
Ti	0.35,0.5	0.61	
W	0.69		
Ag	0.69		0.88
Pt	0.85		0.86
Pt-Ni Alloy	0.6		
Pd	0.72	0.15-0.25	
Au-Ge 300°C			0.27
Au-Ge 200°C			0.35

2.1.2 Schottky diode material

Schottky barrier diodes are generally fabricated from n-type silicon (Si) or n-type gallium arsenide (GaAs) epitaxial layer. For up-microwave and millimeter-wave applications, n-doped GaAs is more desirable due to its high electron mobility ($8000 \text{ cm}^2/\text{V.s}$ for doping concentration of 10^{18} cm^{-3}), relatively low current leakage through the Schottky barrier, ready availability, wide bandwidth and room temperature operation. Also, there has been a considerable interest in using some of the other, even higher mobility, III-V compounds, but there have been practical difficulties in deploying them. One of the most promising materials is indium antimonide (InSb) with mobility nine times higher than GaAs. According to the literature, some Schottky barrier diodes were fabricated on InSb, showing an enormously high series resistance in addition to a relatively low shunt resistance [48]-[49]. One of the drawbacks of InSb is its low band gap requiring that it be cooled to produce a rectifying barrier. The other common semiconductors used in the fabrication of Schottky diodes are gallium nitride (GaN), silicon carbide (SiC), indium phosphide (InP) and indium gallium arsenide (InGaAs). Examples of metals used for the Schottky anode contacts are titanium (Ti), platinum (Pt), chromium (Cr), tungsten (W), molybdenum (Mo), and various alloys. The typical metal (ohmic) contact is an alloy of Ge, Au and Ni since they decreases contact resistance to n-GaAs. The choice and processing of materials result in a low series resistance along with a narrow spread of capacitance value for close impedance control.

Moreover, the epitaxial layer to be used must have the following main important properties:

1. The correct crystallographic orientation (100) for GaAs and (111) for Si in order to avoid the uncertainties and patchy result characteristics of using a polarized crystal face,
2. A very low crystallographic imperfection density in order to ensure the minimization of avalanche noise,
3. Excellent surface morphology to allow for submicron device dimension,
4. The correct epitaxial layer doping level, abrupt interface and thickness to ensure the lowest possible device series resistance and the highest possible cutoff frequency.

In addition to the correct epitaxial layer properties mentioned above, the epi-layer thickness should not be greater than 2000 \AA for the optimum device design, since it effects on the series resistance and forward voltage drop of the diode. Also the resistivity of the substrate needs to be

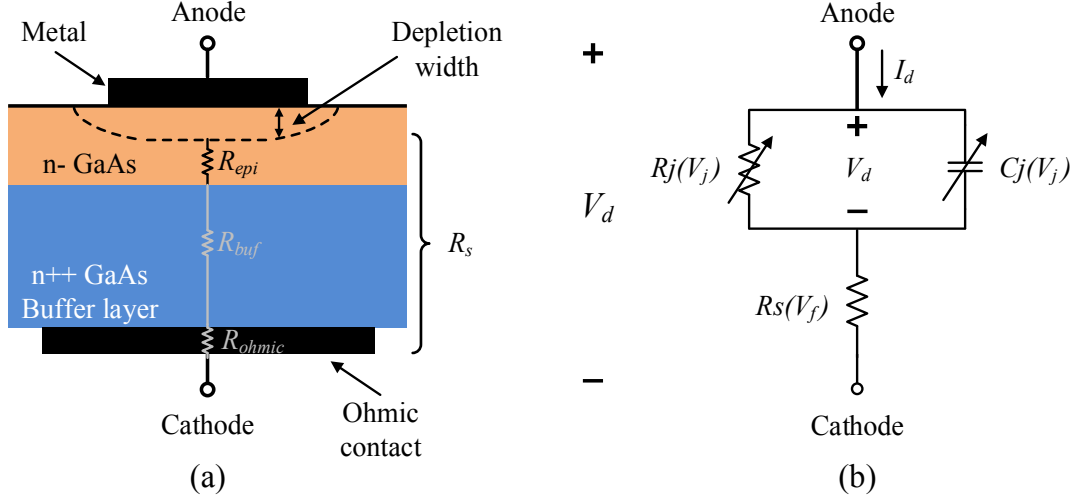


Figure 2.3: (a): Cross-section view of a GaAs Schottky diode; (b) Equivalent circuit model.

as low as possible, more desirable less than $0.001 \Omega cm$, to minimize the contribution of substrate series resistance R_s , which is explained in the sequel.

2.1.3 Schottky diode circuit model

A cross-sectional view of a GaAs Schottky diode shown in Figure 2.3 contains three main layers; the epi-layer, the buffer layer and the ohmic contact. Normally, the buffer layer is made of a high doped GaAs (with doping concentration more than $10^{18} cm^{-3}$) to ease the current flow from the epi-layer to the ohmic contact. The current flow between the semiconductor and the external circuit is made through the ohmic contact.

The equivalent circuit model of the Schottky diode shown in Figure 2.3 (b) consists of a voltage-dependent current source, $I_j(V_j)$ charge source, $Q_j(V_j)$ and a series resistor R_s . The diode essential properties are dependent on junction voltage, V_j . The series resistor, V_j , is the sum of the resistance due to the epitaxial layer, R_{epi} the resistance due to the current spreading through the buffer layer, R_{buf} and the resistance due to the semiconductor-ohmic contact, R_{ohmic} . But the major contribution comes from R_{epi} and R_{buf} . The series resistance in the epitaxial layer and the buffer depends on the junction geometry, frequency, and to a lesser extent, on the applied voltage. Therefore, R_s is given by

$$R_s(V_j, f) \approx R_{epi}(V_j, f) + R_{buf}(f) \quad (2.1)$$

where

$$R_{epi} = \frac{\rho}{A} = \frac{2w}{(q\mu_e N_d)A} \quad (2.2)$$

$$R_{buf} = \frac{\rho}{2d} = 2\rho_{buf} \sqrt{\frac{A}{\pi}} \quad (2.3)$$

in which ρ is the epitaxial layer resistivity, w is the epitaxial thickness, A is the size of the Schottky contact, μ_e is the electron mobility of the epitaxial layer (this assumes the layer is n-type), and N_d is the donor density in the epitaxial or active layer. ρ_{buf} is the buffer resistivity and d is the active junction diameter (in case of having a circular Schottky contact $d = 2\sqrt{\frac{A}{\pi}}$).

However, R_{epi} is a voltage-dependent parameter, but its voltage-dependency is not strong and the series resistance is normally considered as an extrinsic element.

2.1.4 Current-voltage characteristic

Under a forward bias condition, thermionic emission, recombination in the space charge region and recombination in the neutral region occurs in the current transport mechanism [50]. For a good quality metal-semiconductor contact, the majority of the carrier transport is caused by thermionic emission. Thermionic emission in a Schottky contact has been discussed in detail in [40] and [43]. The current-voltage (I-V) equation of a Schottky diode is described by

$$I_d(V_j, T) = I_s (e^{\frac{qV_j}{\eta k_B T}} - 1) \quad (2.4)$$

where

$$I_s(T) = AA^{**} T^2 e^{-\frac{q\phi_b}{k_B T}} \quad (2.5)$$

in which I_d is the diode junction conduction current, I_s is the saturation current, V_j is the junction voltage, η is the ideality factor of the diode, q is the electron charge (1.6×10^{-19} Coulomb), k_B is

Boltzmann's constant ($1.37 \times 10^{-23} J/K$), T is the absolute temperature, A is the Schottky contact area, A^{**} is the effective Richardson's constant ($8.2 A cm^{-2} K^{-2}$ for GaAs) and ϕ_b is the barrier height.

In the forward condition when the thermionic emission dominates the electron transport mechanism, the ideality factor is close to unity. But in the practical scenario, this is not the case and the ideality factor depends on the doping concentration and the temperature as well [51]. Therefore, the ideality factor is described by

$$\eta = \frac{1}{k_B T \left(\frac{\tanh(\frac{E_{00}}{k_B T})}{E_{00}} - \frac{1}{2E_B} \right)} \quad (2.6)$$

$$E_{00} = 18.5 \times 10^{-12} \sqrt{\frac{N_d}{m_e^* \epsilon_r}} \quad (2.7)$$

where E_{00} is the material constant in eV , E_B is the band bending, m_e^* is the electron effective mass in unit of free electron mass, N_d is the epi-layer doping concentration in cm^{-3} and ϵ_r is the semiconductor relative permittivity.

Under the reverse-biased condition, the semiconductor area under the metal contact is depleted of electrons and the ionized donors occupy this region. When the diode junction goes under a reversed-biased, the electric field across the junction increases and the electron conduction current decreases. In theory, under reverse-biased condition $V_j \rightarrow -\infty$, $I_d \rightarrow -I_s$. While in reality, a high reverse-bias voltage causes a high electric field across the junction resulting the junction to breakdown. The breakdown voltage, V_{br} , is estimated as

$$V_{br} = 60 \left(\frac{E_g}{1.1} \right)^2 \left(\frac{N_d}{10^{16}} \right)^{-\frac{3}{4}} \quad (2.8)$$

where E_g is the band gap energy in eV and N_d is the epi-layer doping concentration in cm^{-3} [38].

2.1.5 Capacitance-voltage characteristic

While the depletion region is emptied of electrons, using Poisson's equation can determine the diode capacitance-voltage (C-V) relation as

$$Q_j(V_j) = -2C_{j0}\psi_{bi}\sqrt{1 - \frac{V_j}{\psi_{bi}}} \quad (2.9)$$

$$C_j(V_j) = \frac{dQ_j(V_j)}{dV_j} = C_{j0}\sqrt{\frac{\psi_{bi}}{\psi_{bi} - V_j}} \quad (2.10)$$

where, C_{j0} is the zero-biased junction capacitance given by [52]

$$C_{j0} = A\sqrt{\frac{q\epsilon_s N_d}{2\psi_{bi}}} \quad (2.11)$$

in which ϵ_s is the semiconductor dielectric constant.

On the other hand, a diode can be considered as a parallel plate capacitor where the distance between two plates is the width of depletion region, $w_d(V_j)$, which is controlled by the junction voltage.

$$C_j(V_j) = \frac{A\epsilon_s}{w_d(V_j)} \quad (2.12)$$

while

$$w_d(V_j) = \sqrt{\frac{2\epsilon_s(\psi_{bi} - V_j)}{qN_d}} \quad (2.13)$$

The mentioned equations are valid in the condition of absence of electron in the depletion area. Under a forward-biased condition, the conduction current of electron increases which affects the carrier distribution. Therefore, under such a condition, the diode junction capacitance is calculated using a numerical solution of semiconductor transport equations [53].

2.2 RF Schottky rectifier design criteria

The optimal design of high-performance Schottky rectifiers requires an understanding of the dominant device mechanisms that affect Schottky rectifier performances. The key performance parameters of Schottky rectifiers are breakdown voltage, forward voltage drop, power dissipation and switching time. Depending on applications, different parameters become more or less important relative to others. Each of these performance parameters are affected by one or more physical mechanisms. As mentioned before, a typical Schottky rectifier consists of a metal contact deposited on an epi-layer, a substrate (buffer-layer) and a backside ohmic contact. The main device design variable that affects Schottky rectifier characteristics is the contact metal work function which affects the barrier height, the epi-layer doping concentration, the epi-layer thickness and the device edge termination. Hence in the sequel, the above-mentioned criteria and their impacts in Schottky rectifier performance are elaborated.

2.2.1 Breakdown voltage

The breakdown voltage of a Schottky rectifier depends on the semiconductor critical field, epi-layer doping, and epi-layer thickness. For rectification purpose, a high breakdown voltage is desirable. To provide that, the selected epi-layer should be thin with a high doping concentration [54].

2.2.2 Forward voltage drop

The forward voltage drop is the function of the Schottky barrier height and the series resistance. In the Schottky rectifier, the forward voltage should be as small as possible to have sensitivity at low power level. The forward voltage drop is

$$V_F = \frac{nk_B T}{q} \ln\left(\frac{J_F}{A^{**} T^2}\right) + n\phi_b + R_{ON} J_F \quad (2.14)$$

where n is the ideality factor, k_B is Boltzmann's constant, T is the absolute temperature, A^{**} is the effective Richardson's constant, ϕ_b is the barrier height, J_F is the forward current density and R_{ON} is the resistance calculated by

$$R_{ON} \approx \rho_{epi} t_{epi} = \frac{t_{epi}}{q \mu_N N_D} \quad (2.15)$$

in which ρ_{epi} is the epi-layer resistivity, and μ_N is the epi-layer mobility.

2.2.3 Power dissipation

The power dissipation, P_D , of a Schottky rectifier depends on the forward voltage, the reverse leakage current and the breakdown voltage, according to (2.16) [54],

$$P_D = (\%ON)(V_F J_F) + (1 - \%ON)(V_B J_L) \quad (2.16)$$

where $\%ON$ is the on duty cycle.

Considering the power dissipation, there is a tradeoff in selecting the best metal for a Schottky rectifier. A metal that forms a small barrier will reduce the forward voltage drop, but increase the reverse leakage current which is not desirable. Conversely, a metal that forms a large barrier will increase the forward voltage drop and decrease the reverse leakage current. Therefore, it is necessary to consider the duty cycle, the required forward current, and the required breakdown voltage before selecting the Schottky contact metal.

2.2.4 Switching time

A good Schottky rectifier has a fast switching time. The switching time depends on the dominant forward current mechanism. The forward current in a typical Schottky rectifiers is dominated by thermionic field emission which guarantees a fast switching time. According to the above-mentioned discussion, a high quality Schottky rectifier needs to have high breakdown voltage, low forward voltage drop, low power dissipation and fast switching time. To achieve these characteristics, the following conditions should be satisfied:

- The barrier height of the Schottky rectifier should be as small as possible to detect low RF power, therefore the work function of the selected metal has to be close to electron affinity of the selected semiconductor.
- A high-doped semiconductor needs to be selected as epi-layer (in the range of 10^{18} cm^{-3}).

- The selected semiconductor needs to have a high electron mobility.

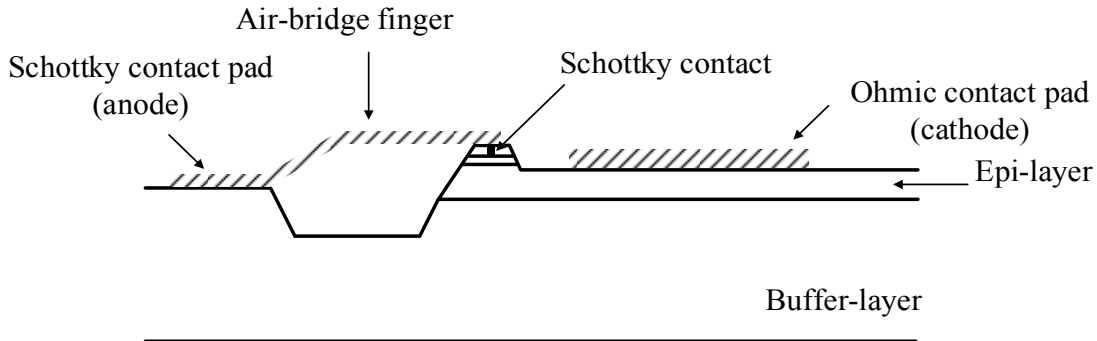


Figure 2.4: Structure of a planar Schottky diode

2.3 Planar structure Schottky diode

Different techniques are available for the design and fabrication of Schottky diodes. For many years whisker technique was widely used for fabrication of millimeter-wave Schottky rectifiers [55]. In 1987, a planar structure Schottky diode technology was introduced [56]. Nowadays, this technique has been well accepted as a promising solution for millimeter-wave and THz applications, compared to the whisker contacted diode structure. Figure 2.4 shows the planar structure of the diode in which the anode contact is formed by depositing a metal contact on the epi-layer. By etching through the epi-layer to the buffer-layer, the ohmic contact is made at a distance of a few micrometers away from the anode contact. A narrow metal connection, known as the air-bridge finger, is shaped across the surface-channel to connect the Schottky anode to a large anode contact pad. The semiconductor beneath the air-bridge finger is removed in order to isolate the anode and cathode pads. The semi-insulating substrate serves as a supporting structure for the diode, whereas the silicon dioxide (SiO_2) or silicon nitride layer passivates the top semiconductor surfaces to increase the isolation between the anode and cathode.

2.3.1 Design and fabrication of a rectifier planar Schottky diode

In this section, we explain the design and fabrication process of a planar based Schottky diode for rectifier applications. First, we choose proper materials for our design. Considering the above-mentioned discussion, a $3\text{ }\mu\text{m}$ thickness n-type GaAs with doping concentration of 10^{18} cm^{-3} and crystallographic orientation of (100) is selected as the main substrate (epi-layer). Since

Table 2.2: Selected metals for Schottky contact.

Metal	Work function
Silver (Ag)	4.26
Aluminum (Al)	4.28
Chromium (Cr)	4.55

we are interested in low barrier height, we choose metals with work functions close to the electron affinity of GaAs (4.07 eV). Therefore, metals listed in Table 2.2 are selected to form Schottky contact. Also a thin layer of an alloy of Ge/Au/Ni is used to make the ohmic contact, since it is found to significantly decrease the contact resistance to n-type GaAs.

To make the ohmic contact, resistance contacts of (280°A of Ni, 680°A of Au and 330°A of Ge) is deposited by magnetron sputtering. The fabrication process consists of cleaning semiconductor wafers in dissolvent and wet etching in order to remove the native oxide layer.

Then the samples are loaded into a vacuum chamber and the metallic layers deposited. Before the sputter deposition, the targets of GaAs are pre-cleaned by four different processes including etching by Ar^+ ions and wet etching. Samples are then annealed in a gas flow furnace in the temperature range from 400°C to 450°C to increase the thermal-stability. To increase the conductivity of the ohmic layer, a thin metallic layer of gold (100 nm) is deposited on the semiconductor, then the ohmic is made on this layer. To make the Schottky contact, the same process is repeated. First, a thin layer of gold is made then the Schottky metal is deposited on. The Schottky contact of first samples is a square of $50 \mu\text{m} \times 50 \mu\text{m}$. Figure 2.5 and Figure 2.6 show the first prepared mask and the fabricated samples of the Schottky barrier, respectively.

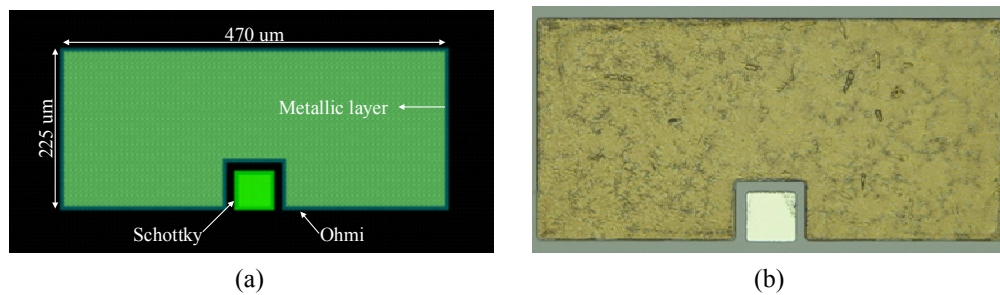


Figure 2.5: (a): The mask of the designed Schottky diode; (b): The fabricated prototype of Schottky diode.

The forward I-V curves of the first samples with different Schottky materials are measured and then compared to results obtained from theory using (5.4) and a commercial Schottky rectifier, MA4E1317. Figure 2.6 depicts results of the Schottky contact made with silver. Results show that the forward voltage of the Schottky made with silver is around 0.6 V for a current of 0.2 mA. The measured breakdown voltage is 4.8 V.

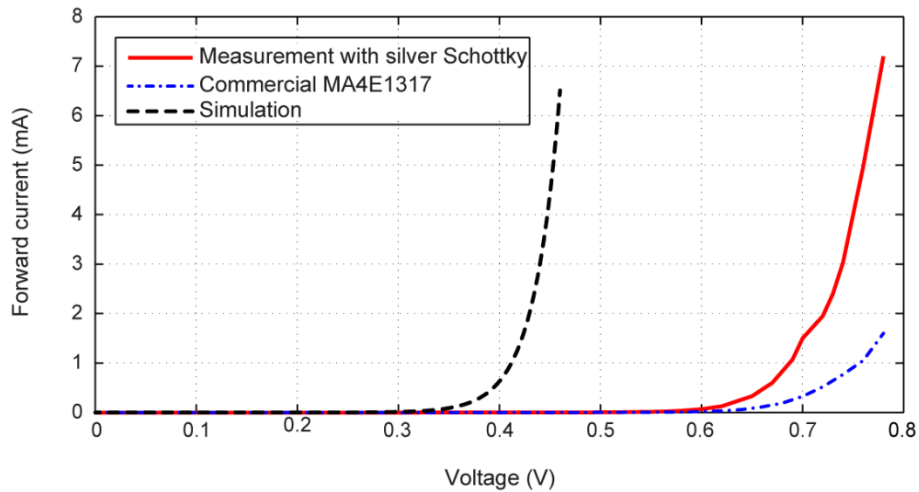


Figure 2.6: The forward I-V curve of the silver Schottky diode.

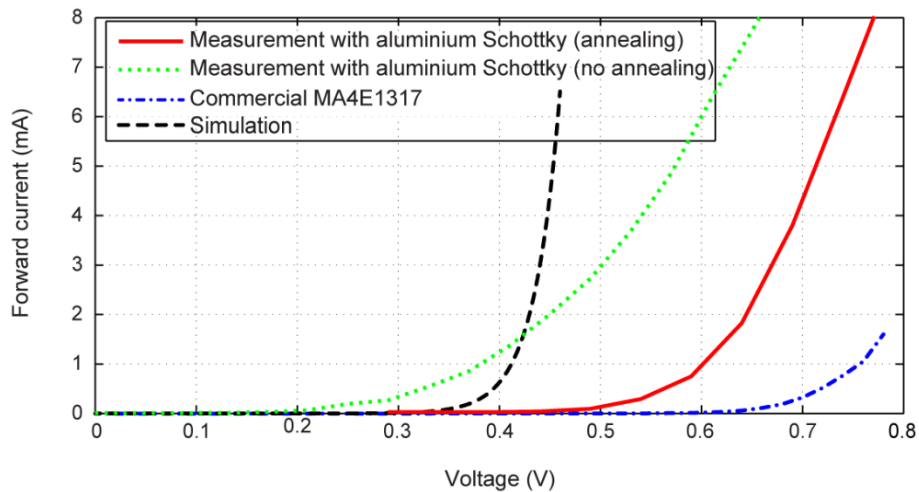


Figure 2.7: The forward I-V curve of the aluminum Schottky diode.

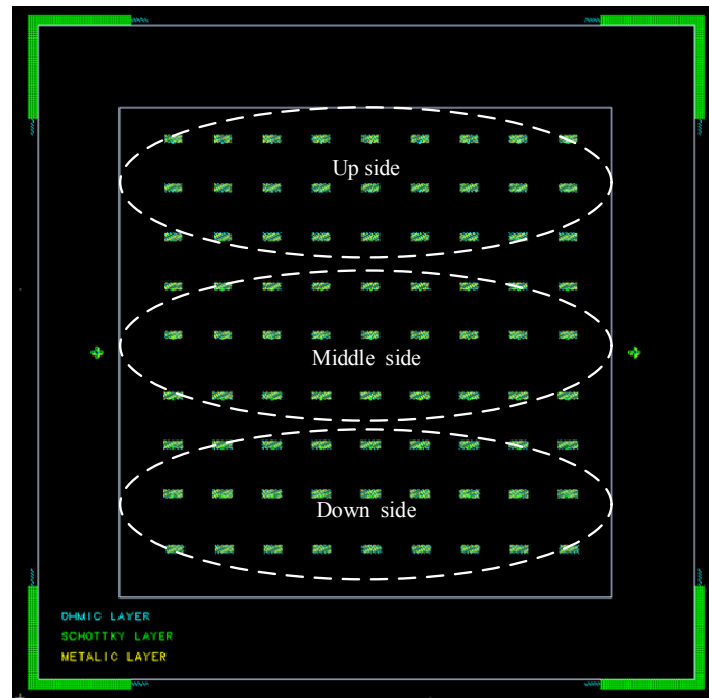


Figure 2.8: The designed Schottky diodes on a single wafer of GaAs.

Another Schottky contact is made using aluminum. Two samples are made; one with annealing and one without annealing. Figure 2.7 shows that the forward bias voltage for the aluminum prototypes is 0.3 V without annealing and 0.5 V with annealing. The measured breakdown voltage for both samples is 5 V. It can be seen that the measured DC characteristics of the fabricated aluminum Schottky diodes have a superior performance compared to the commercial counterpart, MA4E1317. It is good to mention that in each wafer there are 100 Schottky diodes (Figure 2.8). We need to measure at least half of the diodes to make sure about the quality of the fabrication process (They need to have similar I-V curves). Figure 2.9 shows the I-V curves of the Schottky diodes placed at different side of the wafer. Close I-V behaviors demonstrates the precision of the fabrication process. The last sample of Schottky diodes are made on chromium. To do that, two different size of Schottky contacts, $50\text{ }\mu\text{m} \times 50\text{ }\mu\text{m}$ and $20\text{ }\mu\text{m} \times 20\text{ }\mu\text{m}$, are fabricated. It is known that, reducing the size of the Schottky contact leads to the cutoff frequency increment. The forward DC measurement (I-V curve) is done and the results is presented in Figure 2.10. The measured forward bias voltage and breakdown voltage of the chromium Schottky diode are 0.4 V and 3.8 V, respectively.

The comparison result among different Schottky diodes (Figure 2.11) shows that the aluminum is a better choice for making the Schottky contact, since the aluminum Schottky contacts have less forward bias voltage and more breakdown voltage. Therefore, aluminum is selected as the proper metal for making the Schottky contact for the rest of the fabrication.

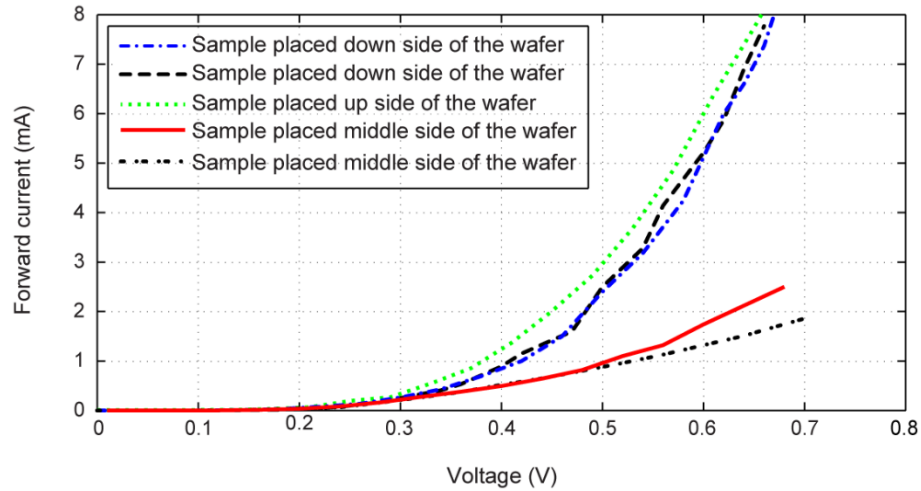


Figure 2.9: DC characteristics of Aluminum Schottky diodes placed at different side of the GaAs wafer.

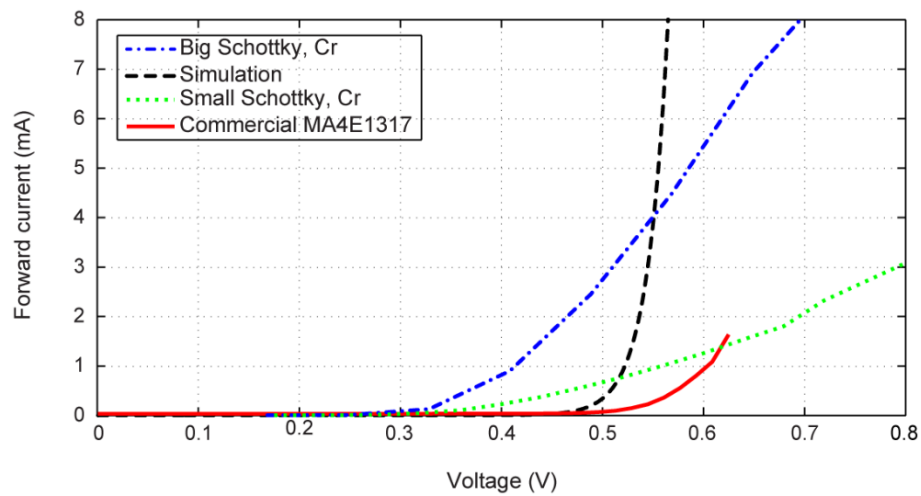


Figure 2.10: The forward I-V curve of the chromium Schottky diode.

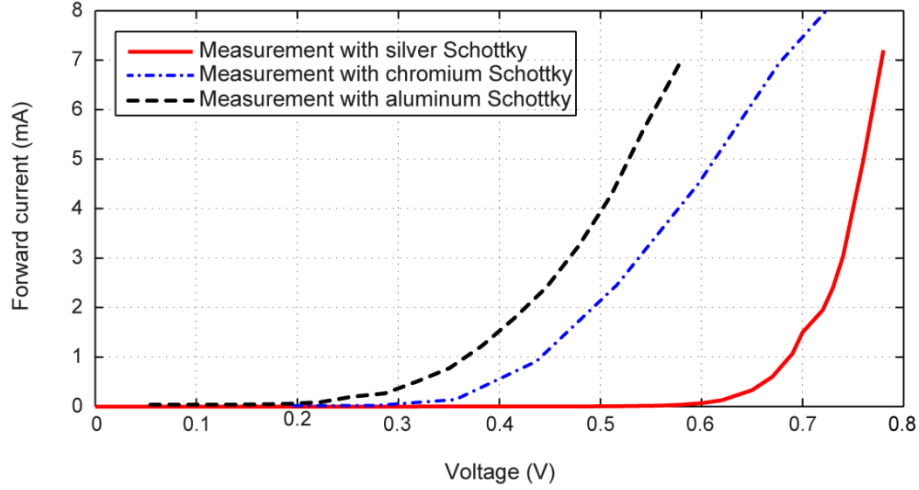


Figure 2.11: Comparison among different Schottky diodes.

Moreover, it is worth to mention that the fabricated sample of aluminum Schottky contact provides a better performance in terms of sensitivity to low voltage compared to the commercial Schottky rectifier. In the sequel, we should measure the RF performance of the designed Schottky diode to evaluate the rectification behavior. To do so, we need to fabricate the air-bridge finger to provide a connection between the Schottky pad and Schottky contact and make the two-port measurement using a VNA.

The layout and the fabricated prototype are shown in Figure 2.12. The Schottky contact is a square of $10\text{ }\mu\text{m} \times 10\text{ }\mu\text{m}$. The thickness of the epi-layer is $4\text{ }\mu\text{m}$. The air-bridge is made using a thin layer of Aluminum (the same material as the Schottky contact), $2.6\text{ }\mu\text{m}$.

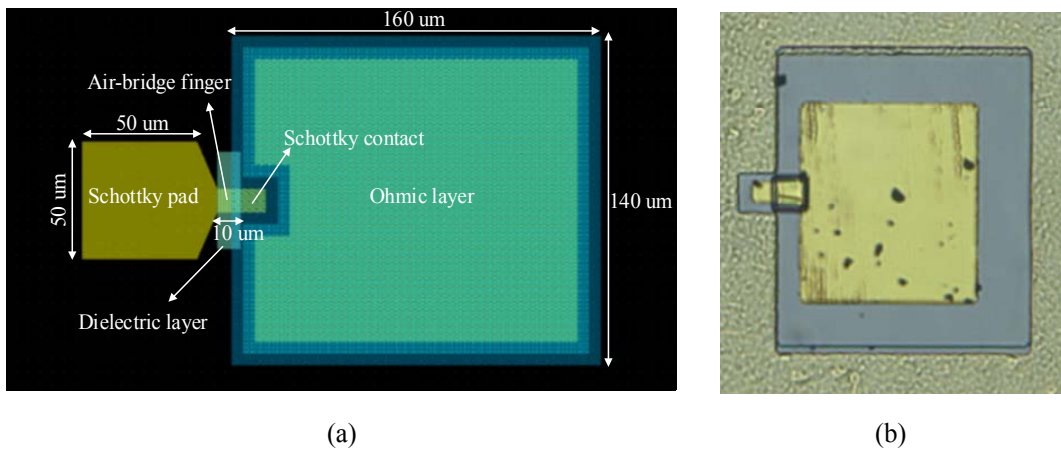


Figure 2.12: (a): Mask of the designed planar Schottky diode; (b): Fabricated prototype of the planar Schottky diode.

The required steps for the fabrication of the Schottky diode shown in Figure 2.12 are as following:

- First the mesa layer is generated.
- The ohmic layer is deposited on mesa.
- The dielectric layer which is a kind of photoresist material (AZ 1518) is used to make an isolation between the Schottky pad and the ohmic layer (Figure 2.13 (b)). The Curing process at 175 °C is done to stabilize the dielectric layer on top of the mesa (Figure 2.13 (c)).
- Then the Schottky contact is deposited.
- Next the air-bridge is fabricated to connect the Schottky pad to the Schottky contact.

Figure 2.13 shows the process of air-bridge formation. The key challenge here is the development of reliable processes allowing for suspended metallic bridges on GaAs. Unfortunately, our experimental results for fabrication of the air-bridge was not successful. Since

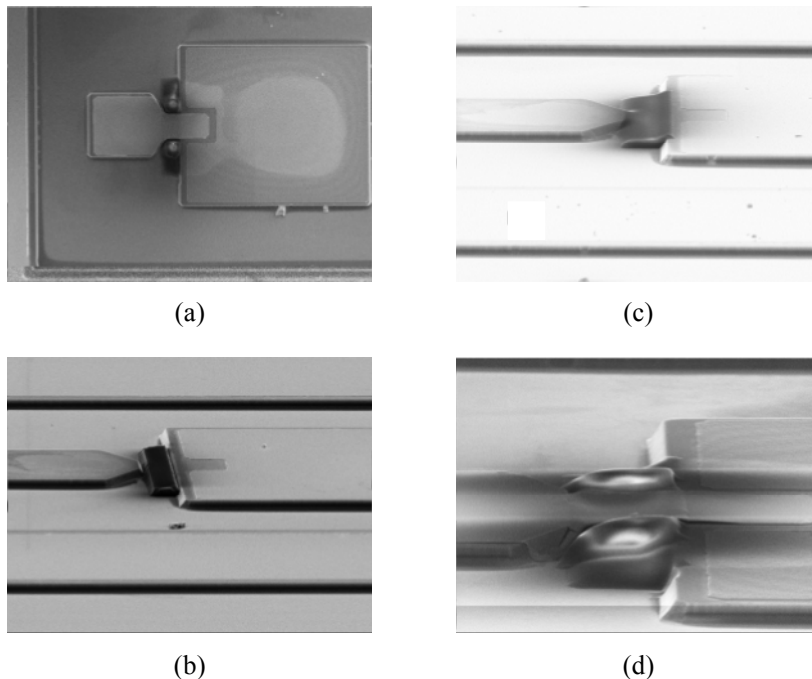


Figure 2.13: (a): Planar Schottky diode; (b): Photoresist deposition; (c): Stabilizing the photoresist layer; (d): Expansion of the photoresist layer which causes the disconnection of the air-bridge.

the photoresist layer had some reaction to Acetone (the material used for lift-off process) and expanded after the lift-off process (shown in Figure 2.13 (d)). This expansion caused the air-bridge to get disconnected from the Schottky pad.

2.4 Conclusion

This chapter has briefly reviewed the concept of a Schottky barrier diode, its performance as a rectifier and required specifications for rectifier applications. To realize a high efficiency rectifier, a key factor is developing low-loss diodes with high saturation current. To design these diodes, low-junction capacitance is required, since the high junction capacitance shorts the video resistance (which models the RF-to-DC conversion efficiency) and high junction impedance reduces the transferred DC power. Moreover, the utilization of low-loss diodes can reduce the input impedance of the rectifier, which results in easily designing a broadband matching circuit. Then, the design process of a planar Schottky diode was studied and some preliminary results of the fabricated Schottky rectifier were presented.

CHAPTER 3 UP-MICROWAVE AND MILLIMETER-WAVE RECTIFIER CIRCUITS

Microwave rectification has been widely used and discussed in the context of energy harvesting and wireless power transmission (WPT) using rectenna (rectifying antenna). A rectenna, consisting of a receiving antenna and a rectifier circuit, is the most vital module in long-range wireless power transmission. The overall performance of a WPT system is normally determined by the efficiency of the antenna and the related rectifier circuit. Therefore, it is essential to realize high-efficiency rectennas or rectifier circuits to guarantee the quality of the WPT system. Since this study is concerned with the up-microwave and millimeter-wave rectenna, this chapter discusses about the rectification process and the design of millimeter-wave rectifier circuits. The main goal of this chapter is to assess various rectifier configurations in terms of optimal RF-to-DC conversion efficiency for realistic diodes at up-microwave and millimeter-wave frequencies.

3.1 Rectifier circuit

A general rectifier block diagram (Figure 3.1) includes five main sections, namely, input filter in the form of a low-pass or band-pass, the impedance matching network before the rectifying element, DC-pass output filter and finally a load.

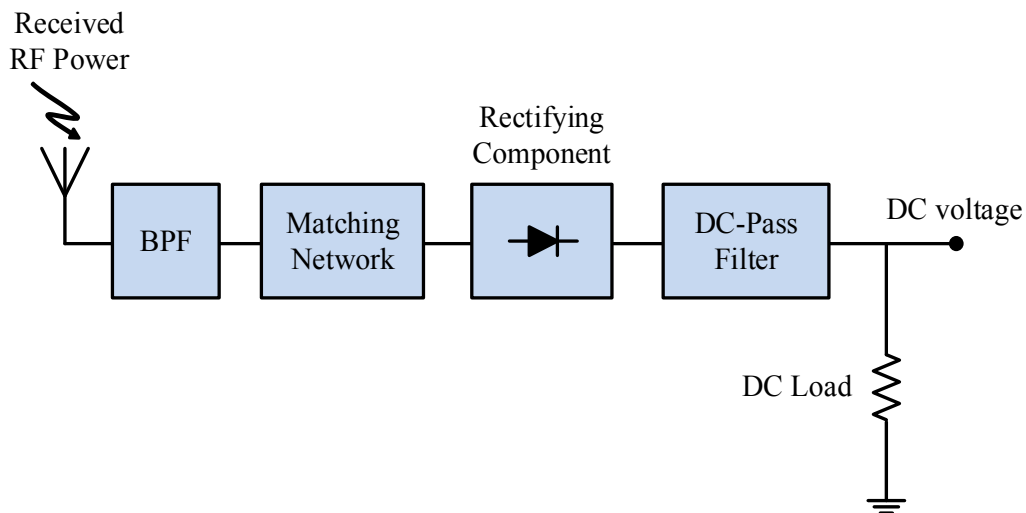


Figure 3.1: General block diagram of a rectifier circuit.

Rectifier circuit can have different topologies, depending on the configuration of the rectifying diodes (Figure 3.2). Single series and shunt mounted diode (Figure 3.2 (a) and (b)) are half-wave rectifiers which theoretically offer the advantage of minimizing the diode loss, which is proportional to diode junction resistance. Since these structures (single series and shunt mounted diode) are dedicated to low power levels (below 1 mW or 0 dBm), power-handling capabilities can be traded for high sensitivity. Voltage doubler (Figure 3.2 (c)) is a full-wave topology which is normally used for medium power levels (up to 100 mW or 20 dBm) which can generate higher DC voltage levels for the same input power compared to a single diode configuration, in the detriment of a power conversion efficiency. Bridge topology (Figure 3.2 (d)) is widely used for low frequency rectification [57]. In the bridge topology, a full-wave rectification is used where both positive and negative half-waves have to overcome two diode threshold voltages. This is the reason why the bridge configuration is not adapted for low power levels. It presents, however, high power-handling capabilities (higher than 100 mW or 20 dBm), if high breakdown voltage diodes are considered. Designers are often confronted with the choice of compromise between high output voltage and good conversion efficiency. Hence, according to the desirable specification of the voltage doubler rectifier in terms of required RF power and the level of the generated DC voltage in the sequel we use this configuration.

3.1.1 Voltage doubler rectifier

Although in most of power harvesting applications the level of received RF power is low ($P_{RF} \leq 0 \text{ dBm}$), the full operating DC voltage must be provided to the load integrated circuit (IC). This would be very challenging since typical ICs at least require 0.5 or 1 V to run and this has to be squeezed out of an antenna that is itself providing only about 0.2 V at a distance of few meters away from a microwave transmitter. This problem will be sensed more at up-microwave and millimeter-wave applications since the path loss is more considerable.

A very common approach to generating higher voltage is to use a voltage doubler configuration. In Figure 3.2 (c), an equivalent circuit is described for the voltage doubler. The operation of the voltage doubler is as follows. When the RF signal is in the negative cycle, the first diode (D_1) is on (Figure 3.3 (a)). Current flows from the ground node through the diode, causing electrical charges to accumulate on the input capacitor (D_1). At the negative peak, the voltage across the capacitor is the difference between the negative peak voltage and the voltage on the top

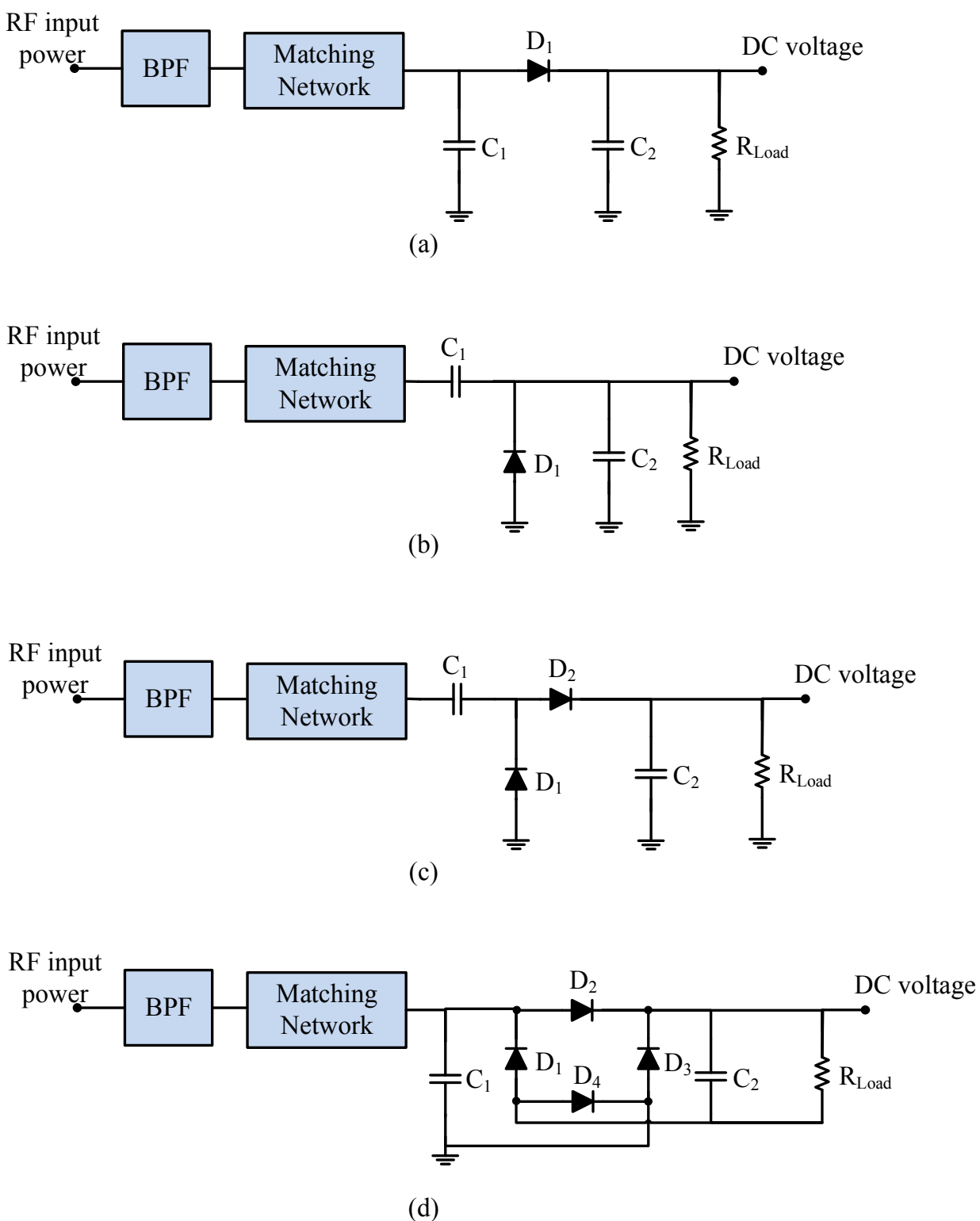


Figure 3.2: Rectifier circuit topologies. (a) Single series-mounted diode. (b) Single series-mounted diode. (c) Voltage doubler. (d) Bridge diode.

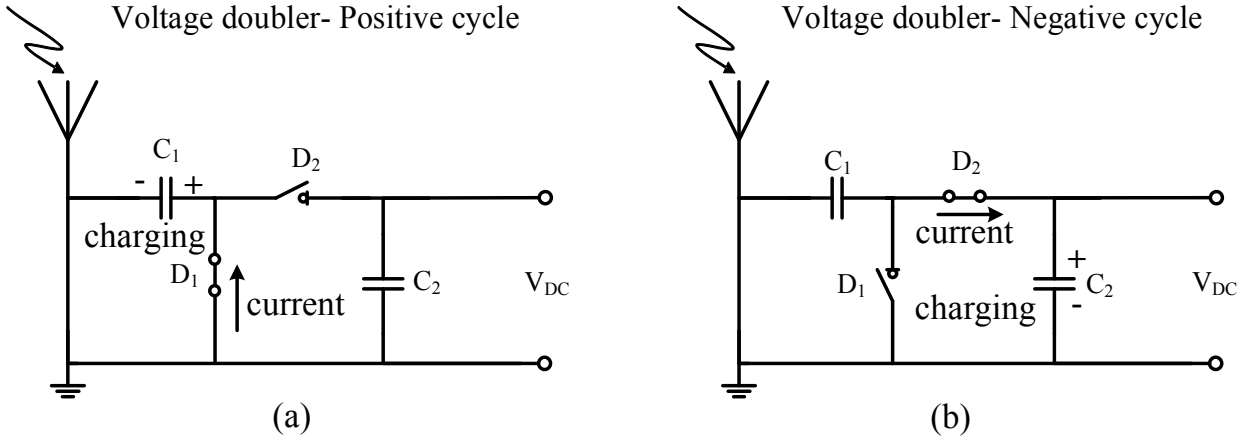


Figure 3.3: Operation of voltage doubler rectifier.

of the diode. At this time, the output of the capacitor is more positive than the RF input. When the RF input becomes positive, the first diode turns off and the second one (D_2) turns on (Figure 3.3 (b)). Electrical charges were collected on the input capacitor (C_1) pass through the output diode toward the output capacitor (C_2). The peak voltage is achieved by adding the voltage across the input capacitor, to the peak positive RF voltage and subtracting the turn-on voltage of the output diode. The actual output voltage depends on the amount of current drawn out of the storage capacitor during each cycle, which is optimized by the value of the load resistance, R_{Load} .

3.1.2 Rectifier input and output filters

As shown in Figure 3.1, in most rectifier circuits an input filter in the form of a low-pass or band-pass is considered to suppress the unwanted higher-order harmonics generated by the diode through rectification process. At up-microwave and millimeter-wave applications, this filter is normally made from open circuit and series stubs. Also, the output filter in a conventional rectifier is generally made up of a capacitor at a distance of quarter wavelength in connection with the operating frequency from the diode.

3.1.3 Matching circuit

Providing a high quality matching network guarantees the maximum energy transfer and minimizes the transmission loss. Different techniques are available to determine the input impedance of a rectifier and design the related matching circuit. For example, the equivalent circuit model of a diode used in the analysis and simulation process, can be obtained based on the diode parameters mentioned in the respective datasheet of the candidate diode. This technique is straightforward and accurate at low frequency (< 2.45 GHz). Since the circuit models obtained from datasheets are not accurate enough to contain all parasitic and packaging effects, this technique is not recommended for high frequency design. Another technique for designing a matching network, is to obtain the parameters of a single diode through measurement and extract its real circuit model considering all the parasitic and packaging parameters. Then, the constructed model is used to design the initial matching network by using Large-Signal S-Parameter (LSSP) simulation controller from Advanced Design System (ADS). At millimeter-wave frequency, circuit models of lumped components similar to diode models, do not include real physical and parasitic effects. While at millimeter-wave frequency, the development of an accurate model of diodes and lumped components should be considered in the simulation. Nevertheless, the measured and simulated resonances will occur at different frequencies and the fabricated prototype will have some frequency shift. Therefore, the recommended method to determine the input impedance and design the matching circuit, is based on the experimental characterization of lumped components as well as diodes.

3.1.4 Selection of rectifier Schottky diode

To design high efficiency rectifiers, the selection of appropriate diode is important because in a rectifier circuit, diodes are the main source of loss and their performance determines the overall circuit performance. A closed-form equation for the diode conversion efficiency has been derived in [10]. According to [10], the power conversion efficiency of a rectifier depends on three parameters of diode; namely, zero-bias junction capacitance (C_{j0}) which determines the oscillation of harmonic currents through a diode, the series resistance (R_s) which causes the ohmic loss and restricts the circuit efficiency and the breakdown voltage (V_{br}) which confines the power handling capability of a rectifier.

An appropriate rectifier diode has low junction capacitance, low series resistance and high breakdown voltage, which are very difficult to get satisfied simultaneously because of the physical mechanism of diodes and those inter-correlated parameters. Also for rectification purpose it is necessary to choose a diode with the capability of a high speed switching to follow a high frequency input signal with low cut-off voltage to operate at low input RF power. Besides, since this study focuses on millimeter-wave frequency design and more specifically 35 GHz, the nominated rectifying Schottky diode needs to support this frequency band. According to the above-mentioned features, commercial Schottky diode MA4E1317 from MACOM with $R_s = 4 \Omega$, $C_{j0} = 0.02 \text{ pF}$ and $V_{br} = 7 \text{ V}$ is selected and used in this study.

3.2 Up-microwave and millimeter-wave rectifier design

The conversion efficiency of millimeter-wave rectennas compared to microwave rectennas is low, but the advantage of size reduction and longer transmission distance overcome the low device conversion efficiency. Therefore, it can be concluded that for the same size of antenna and rectenna, the overall system efficiency of the millimeter-wave rectennas is higher over long distance transmission [10]. However, till now only a few studies have been dedicated to up microwave frequency and millimeter-wave frequency bands [8]-[11]. To the best of our knowledge, most of the previous investigations and designs were assumed to operate at a very high RF power level (higher than 100 mW) and there have been a few reported works for medium and low power range in the literature. Following sections are dedicated to different design of low and medium up microwave and millimeter-wave rectifier circuits.

3.2.1 24 GHz voltage doubler rectifier for wireless power transmission

Over up-microwave and millimeter-wave frequency range, the common configuration of rectifiers suffers from Electrostatic Discharge (ESD) and imperfect output filter drawbacks. Therefore, Figure 3.4 shows the modified configuration of a voltage doubler rectifier operating at 24 GHz. As observed, a lossy path including a high value resistor ($R_{ESD} = 200 \text{ k}\Omega$) in the proposed design) is considered just after charging capacitor (C_l). This resistive path protects the diodes from ESD and prevents them from being burnt out by providing a DC path for accumulated electrical charges [11].

Also, as mentioned before, the output filter of a traditional rectifier circuit normally consists of a capacitor. Since over up-microwave and more specific at millimeter-wave frequency, the impedance of a real capacitor is not zero, then it cannot realize a perfect short circuit. To have a

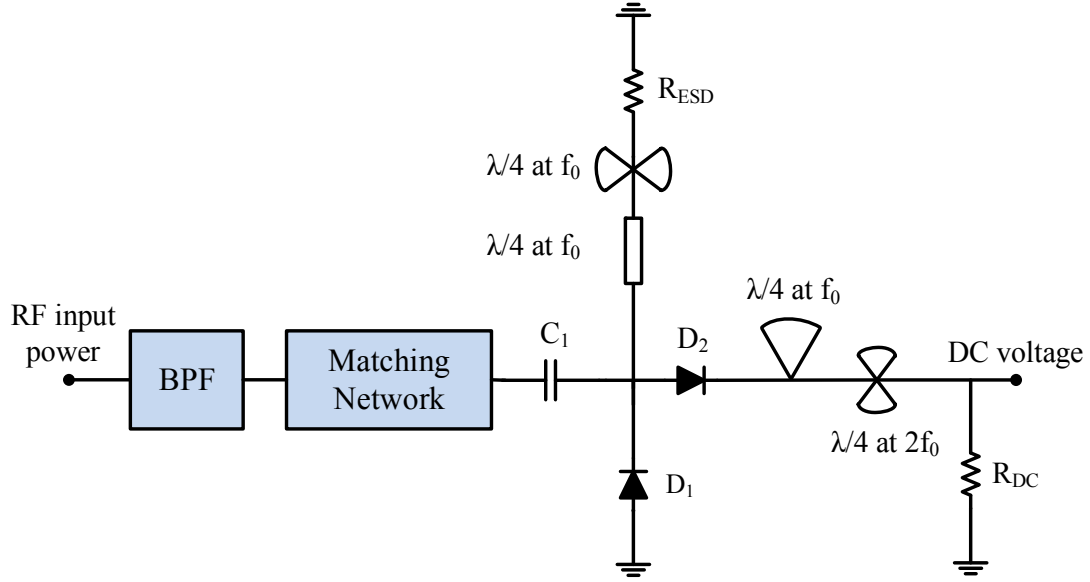


Figure 3.4: Modified configuration of an up-microwave voltage doubler rectifier.

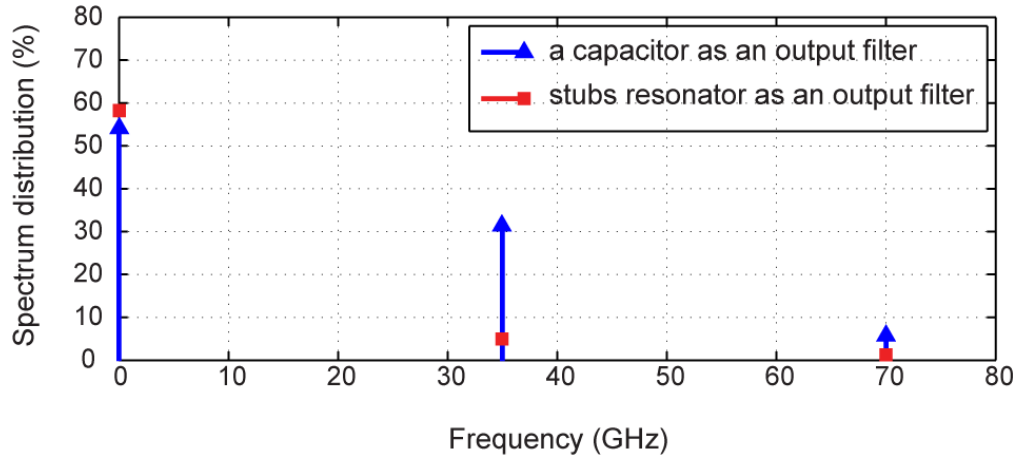


Figure 3.5: Modified configuration of an up-microwave voltage doubler rectifier.

perfect short condition, one solution is using a special quarter wavelength stub resonator instead of a normal capacitor. This stub resonator prevents any RF power from appearing across the resistive load. To do so, the output DC-pass filter is realized using one quarter wavelength open-circuit stub

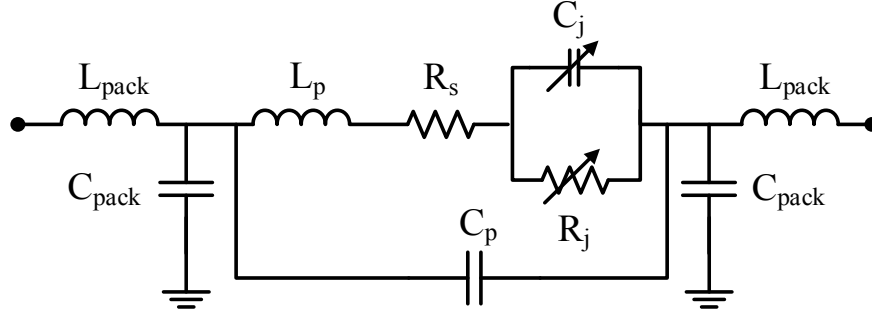


Figure 3.6: Real circuit model of a diode.

resonator at the fundamental frequency as well as the second harmonic. The obtained results depicted in Figure 3.5, justify the resonator structure since it has a superior performance in terms of harmonic suppression compared to a real capacitor.

Designing a high efficiency rectifier circuit depends on the consideration of two important criteria, namely choosing an appropriate rectifier diode and providing quality matching network. As mentioned before, according to the required features for rectification, commercial Schottky diode MA4E1317 from MACOM is selected as rectifying component. To design the matching circuit, the rectifier Schottky diode is firstly measured individually to obtain the parasitic and packaging parameters.

The real circuit model of the Schottky diode is shown in Figure 3.6 where R_s , represents the series resistance, C_j , denotes the junction capacitance, R_j signifies the junction resistance. Also L_p , the lead inductance, and C_p , the parasitic capacitance, are introducing the packaging effect while L_{pack} and C_{pack} are modeling the effect of the diode pads. Normally R_s , and C_j are provided in a component datebook. The parasitic elements and packaging elements of a diode are voltage independent parameters and determined by the small signal measurement explained in [58]. In order to obtain the exact model of the Schottky diode, a microstrip test mount is designed and fabricated for small signal diode measurement. A Thru-Reflect-Line (TRL) calibration kit is also designed for proper calibration (Figure 3.7). The S-parameters characterization is performed using Anritsu 37397C network analyzer from 5 GHz to 40 GHz at different level of input power. The measured frequency range is related to the frequency restriction of TRL calibration kit. For the small signal measurement of the selected diode, the S-parameters in the mentioned frequency range are measured and saved as a S2P file. Then, the diode circuit parameters are obtained through

optimization and tuning process using ADS in order to fit the curves of the diode circuit model to the measured S-parameter data (Figure 3.8). Consequently, L_p , C_p , L_{pack} and C_{pack} are extracted and the model shown in Figure 3.9 is used for initial design simulation of the rectifier.

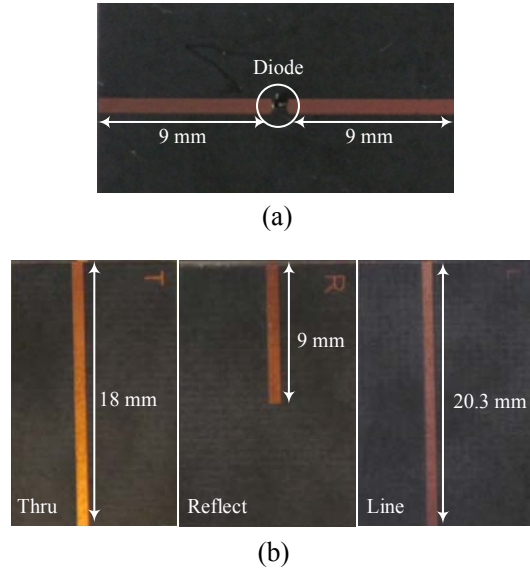


Figure 3.7: (a) Microstrip diode test mount, (b) Microstrip TRL calibration board.

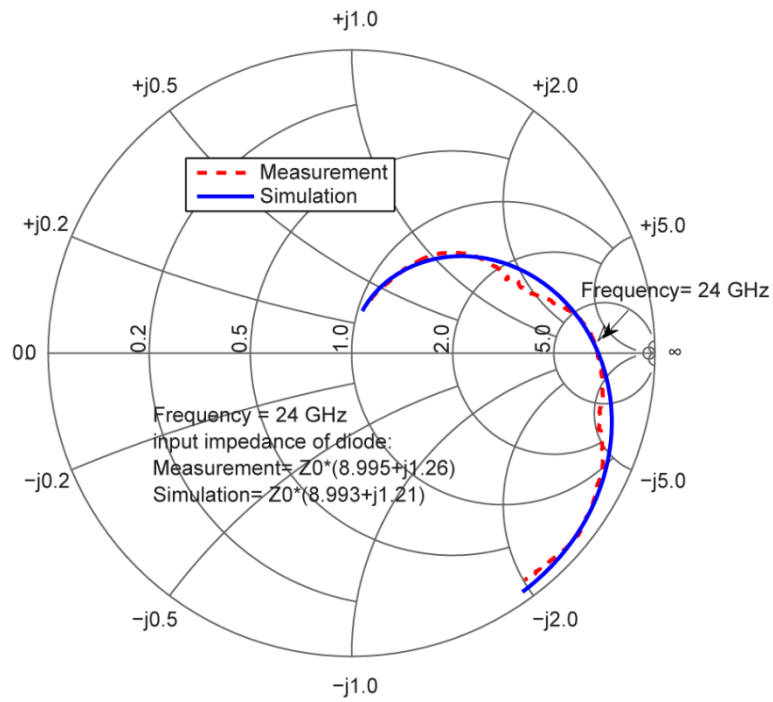


Figure 3.8: Measured and simulated s-parameter (S_{12}). Bias point $V=0$ V.

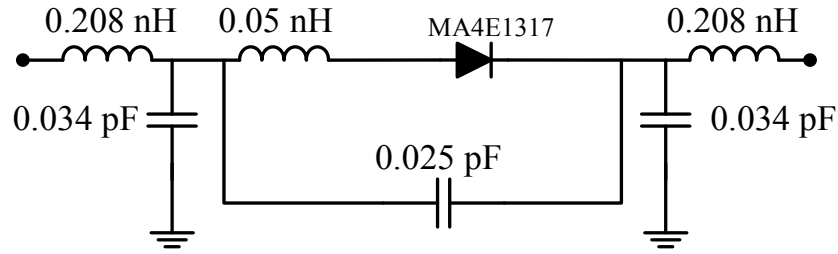


Figure 3.9: Optimized voltage-independent parameter of MA4E1317 Schottky diode.

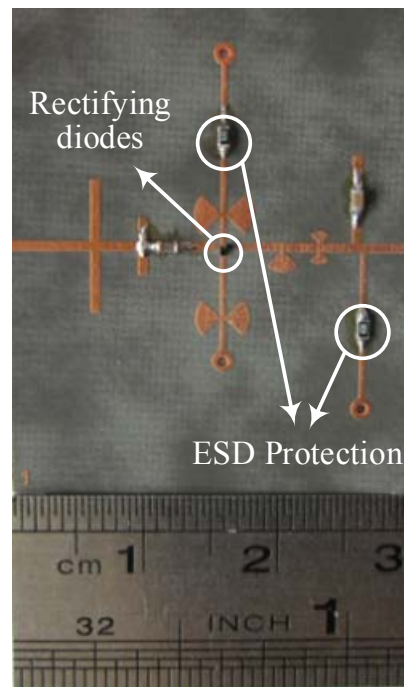


Figure 3.10: Fabricated circuit of the 24 GHz voltage doubler rectifier.

Then the optimization is run to get the maximum efficiency. The optimization is based on the maximum input power and the DC load. Then, the optimized circuit including Schottky diodes, ESD protection resistor, output DC-pass filter and DC resistive load is fabricated on 10-mil-thick high frequency Rogers 5880. The fabricated circuit is shown in Figure 3.10. Simulations have been done on both schematic and layout levels. Layout level simulations were done with the electromagnetic (EM) simulator Momentum in ADS. It should be mentioned that the whole RF circuit, including all passive components, via holes, component's pads and terminations are

simulated individually and as a whole as well. This is important for evaluating the coupling effects among different components at up-microwave and millimeter-wave frequencies. Subsequently, they are brought back to the schematic in order to run the co-simulation process. The co-simulation feature is used to make sure that all designed components show desired performances at operating frequency (24 GHz). Simulated and measured impedance matching conditions of the designed rectifier are shown in Figure 3.11. The measured efficiency is reported at 23 GHz since the fabricated prototype is matched at 23 GHz and it shows better performance at this frequency. The 4% frequency shift, 1 GHz, between simulation and fabricated prototype is acceptable at 24 GHz. Figure 3.12 and Figure 3.13 show the simulated and measured results of achieved output DC power and RF-to-DC conversion efficiency versus the input power. It is necessary to mention that at millimeter-wave frequencies there is some difference between simulation and measurement results of efficiency. This deviation is considered because of the effect of the non-linear junction capacitance of the rectifying diode which becomes dominant at microwave and up microwave frequencies. Because, from the point of view of physic of Schottky diode, at high frequencies, the age of the depletion region is spread and this expansion is changing with time [59]. Therefore, carriers' transportation at the edge of this region can sense velocity saturation effects (because of the expansion and compression of the depletion region) which are time-varying. In the circuit model of the Schottky diode, the depletion region is modeled as junction capacitance. Hence, considering the above-mentioned statement, it can be concluded that the nonlinearity of the Schottky diode is sensed more at higher frequencies, since the effect of nonlinear junction capacitance becomes more dominant. According to Figure 3.13 the conversion efficiency increases gradually when the input power is less than 35 mW then the efficiency drops down rapidly because the diode voltage exceeds the break down voltage. The RF-to-DC conversion efficiency of the rectifier is defined as the ratio of the output DC power to the incident power and is given by:

$$\eta = \frac{P_{DC}}{P_{in}} \quad (3.1)$$

$$P_{DC} = \frac{V_D^2}{R_L} \quad (3.2)$$

where P_{in} is the incident RF power and V_D is the DC voltage on the load, respectively.

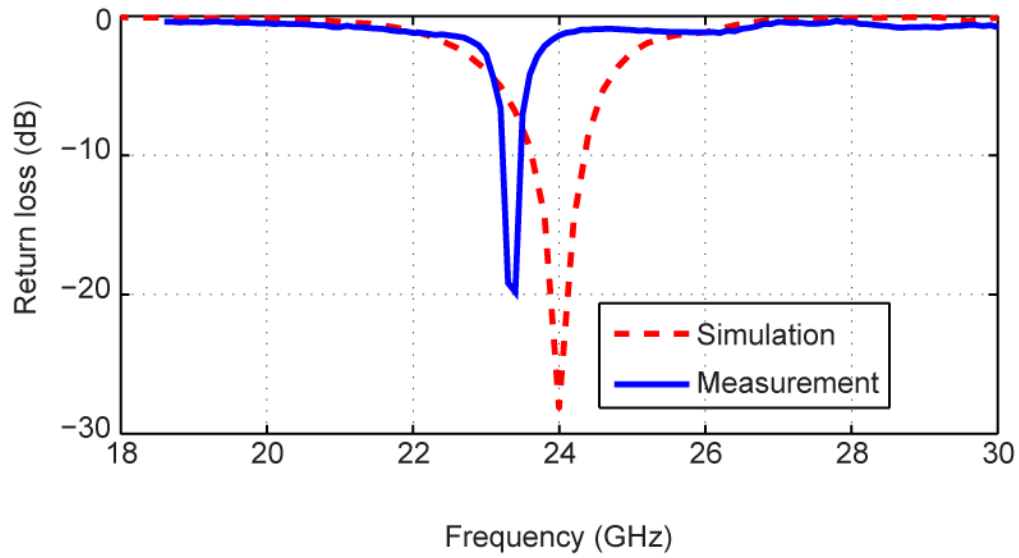


Figure 3.11: Input matching of the 24 GHz voltage doubler rectifier.

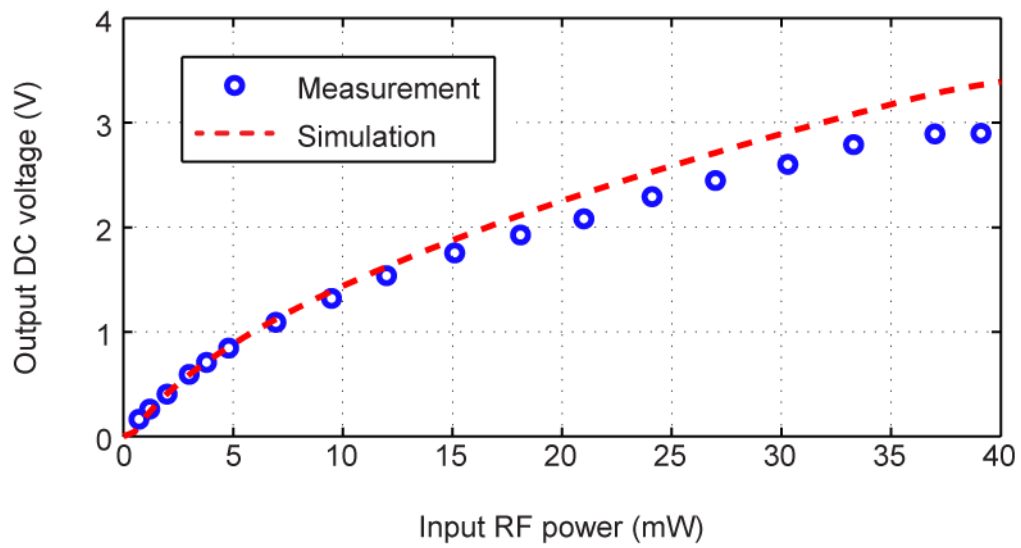


Figure 3.12: Input matching of the 24 GHz voltage doubler rectifier.

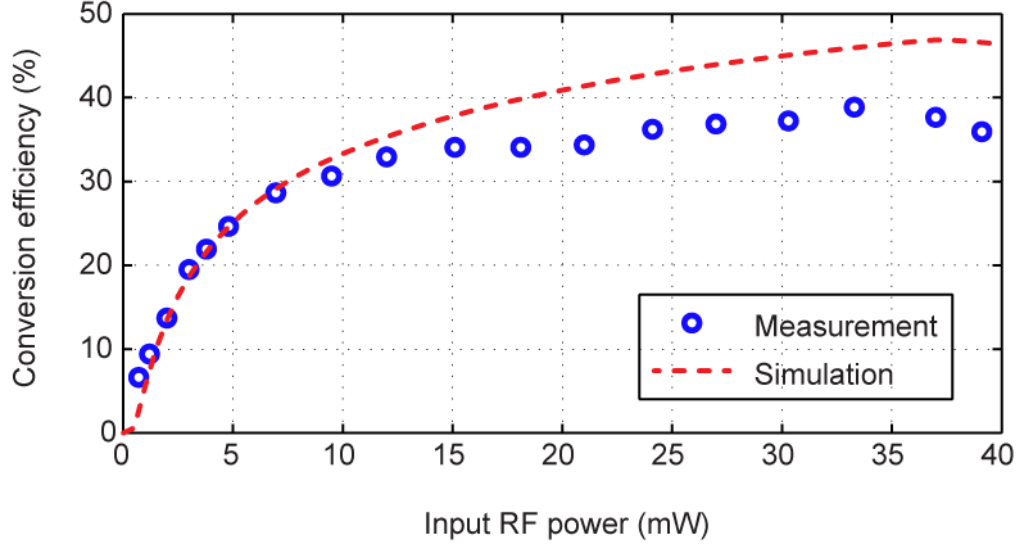


Figure 3.13: RF-to-DC conversion efficiency versus input RF power.

3.2.2 24 GHz self-biased rectifier

In the next step, the design of a low-power rectifier operating at up-microwave frequency is our point of interest. Therefore, deploying a single series configuration (Figure 3.2 (a)) is an appropriate architecture considering the required input RF power (the single series is the best configuration for operating at low level of input power [60]). According to the low-cost technique which is implemented easily, the selected structure is justified. To increase the sensitivity level of a rectifier, one solution is to bias the diode. In order to decrease the required RF power, the necessary voltage for biasing the diode may be provided by using a part of the rectified wave generated from the Schottky diode (self-biased technique [61]). In most of the self-biased rectifiers, the bias path is provided by setting a shunt resistor just before the rectifying Schottky diode as shown in Figure 3.14. This resistor provides the necessary DC return path for the diode's output current. Simulated results shown in Figure 3.15 verify that this structure has the advantage of working at low level of input power (sensitivity level is around -10 dBm). However, the generated output DC voltage does not have thermal stability that is piloted by a variable temperature between -25 °C to 75 °C. The instability of voltage is explained by considering the output DC equivalent circuit of the self-biased rectifier which is modeled by a voltage source in series with junction resistance R_j of the diode [62].

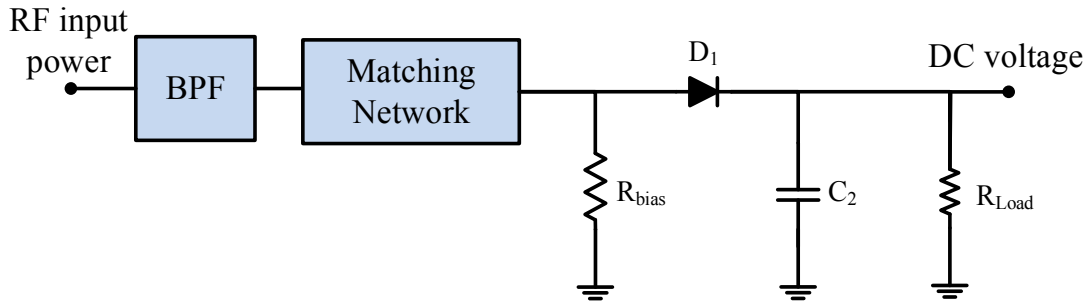


Figure 3.14: Configuration of a self-biased rectifier.

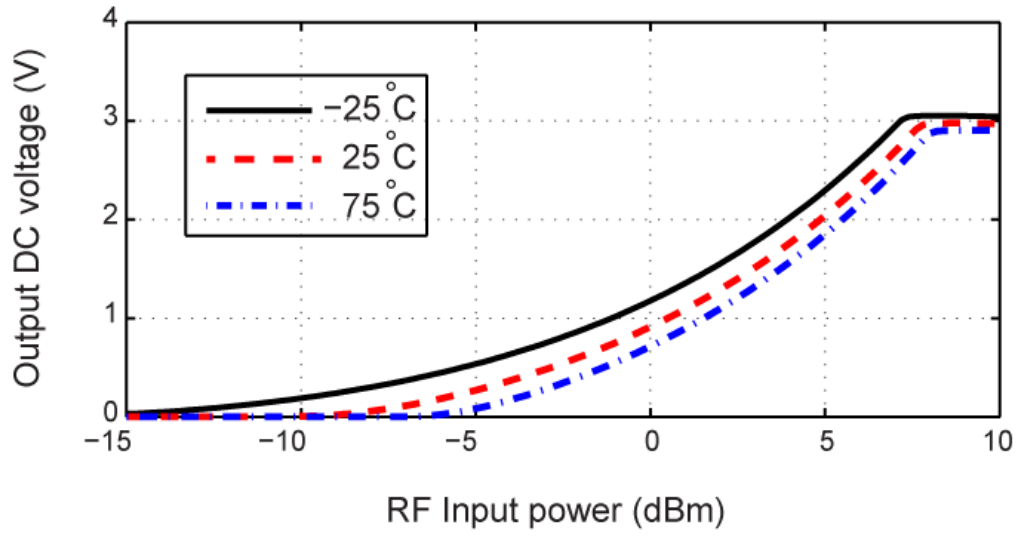


Figure 3.15: Simulated rectified voltage of the self-biased rectifier at different temperature.

Therefore, the defined output DC voltage, V_{out} , is

$$V_{out} = V_{rectified} \frac{R_{Load}}{R_{Load} + R_j} \quad (3.3)$$

Where $V_{rectified}$ is the rectified voltage generated by diode D_1 . The junction resistance of the Schottky diode is defined by

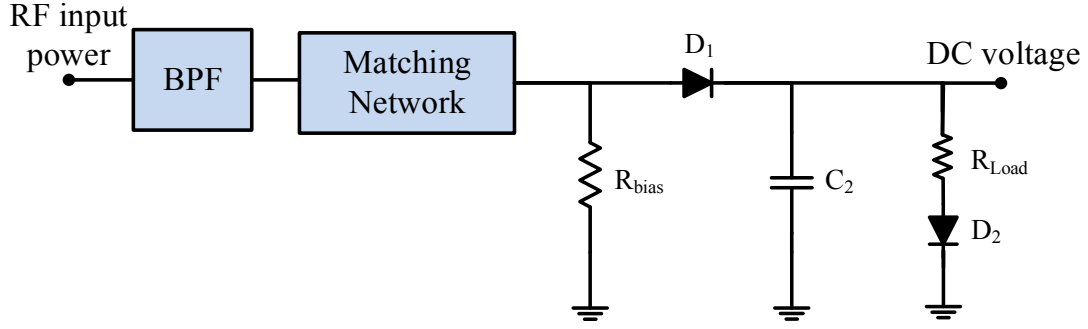
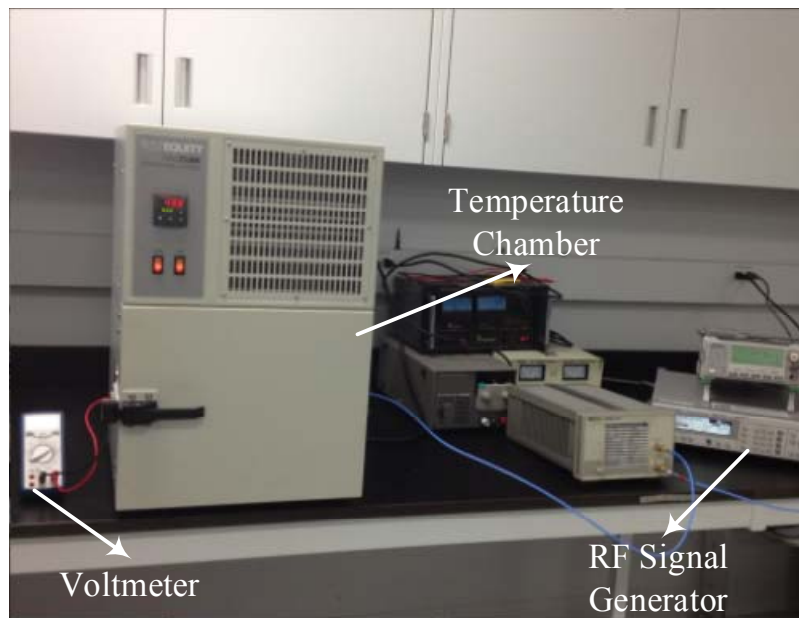


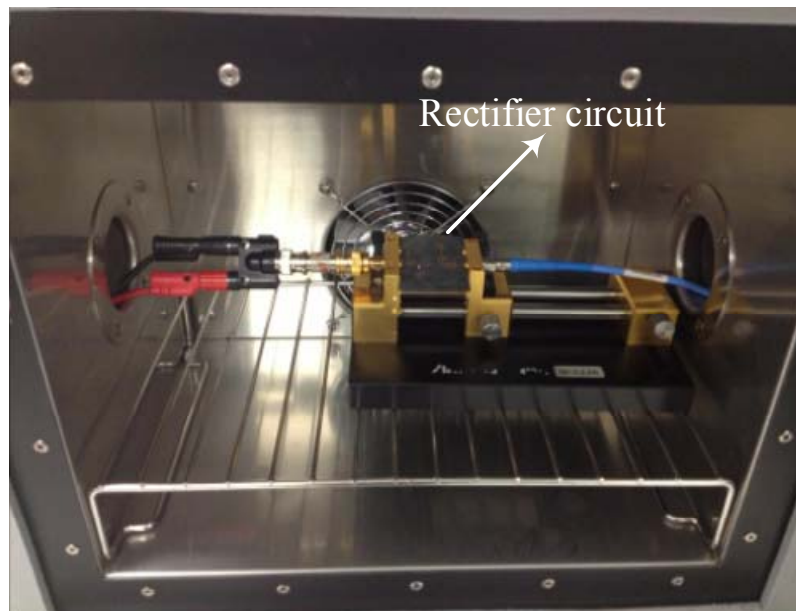
Figure 3.16: Configuration of sensitivity improvement self-biased rectifier.

$$R_j = \frac{nkT}{q(I_s + I_b)} \quad (3.4)$$

where n is the diode ideality factor, k is the Boltzmann constant, T is temperature in Kelvin, q is the electronic charge and I_s and I_b represent the diode saturation current and the external bias current, respectively. Since the junction resistance of the diode is a function of temperature, according to (3.3), the DC output voltage changes with temperature. To provide temperature stability, a modified structure of the self-biased rectifier is needed to overcome this problem. Considering (3.3), if a variable resistance tracking with R_j , which can compensate the effect of R_j , is connected in series to resistive load (R_{Load}) in a way that the value of this resistance alters with rectified current (Figure 3.16), the self-biased rectifier will exhibit temperature stability. The fabricated circuit is measured at different temperature (Figure 3.17) and measurement results justify the temperature stability of the circuit (Figure 3.18). Referring to Figure 3.16, this variable resistance can be made by using the same type of the Schottky diode used as the rectifying component. In this structure, the rectified current obtained by the first diode, D_1 , provides the required bias current of the second diode, D_2 . Consequently, D_2 behaves as a variable resistor because of its current dependence nature in the junction resistance. Results shown in Figure 3.18 prove that this structure has a thermal stability since the measured DC voltage is constant while the temperature fluctuates from -25 °C to 50 °C.



(a)



(b)

Figure 3.17: Measurement setup for the sensitivity improvement rectifier at different temperature.

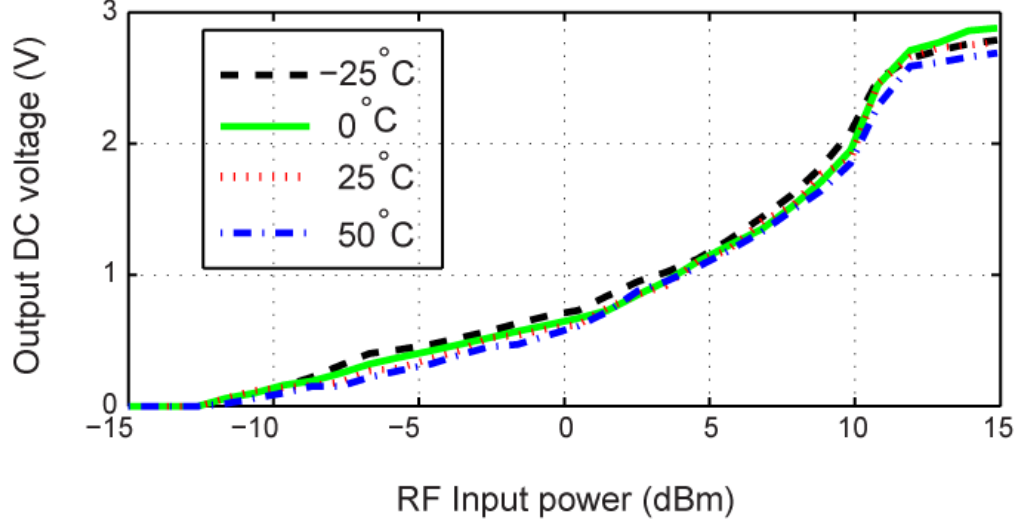


Figure 3.18: Measured rectified voltage of the sensitivity improvement rectifier at different temperature.

The values of R_{bias} and R_{Load} are determined by running optimization using Harmonic-Balance (HB) simulator in Agilent ADS to achieve the maximum DC output voltage and conversion efficiency. For this design, R_{bias} and R_{Load} are set to be $100\ \Omega$ and $160\ \Omega$, respectively since the maximum efficiency is obtained with the mentioned values. After selecting the suitable diode for rectification, and justifying the rectifier configuration, a high-quality matching network is needed. As mentioned before different techniques are available for determining the input impedance of a diode and thus designing the related matching circuit. One direct solution to obtain the input impedance properties is based on experimental characterizations. This technique is more accurate especially at millimeter-wave frequencies since it includes real physical effects of each element used in the circuit. Based on this technique, the entire rectifier circuit (including Schottky diodes, bias resistor, DC-pass capacitor and DC resistive load) without matching part is made, as shown in Figure 3.19. S-parameters of this circuit are measured using Anritsu network analyzer and saved as a S2P file. The obtained result is used as a black box for designing the impedance matching network. Thru-Reflect-Line (TRL) calibration standards (Figure 3.19 (a)) are designed and used to relocate reference planes of the structure (reference plane is point *A* as shown in Figure 3.19.) and remove effects of the microstrip line added to the input of the circuit. This microstrip

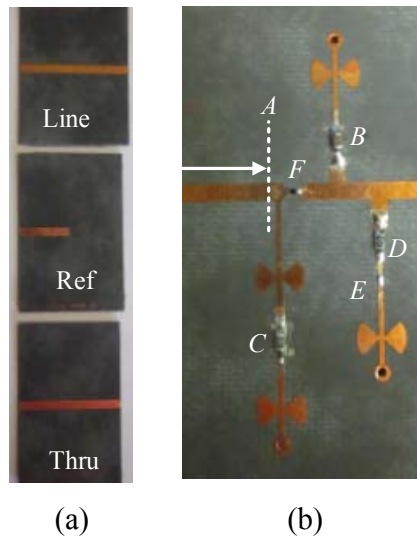


Figure 3.19: (a) TRL calibration kit. (b) Fabricated rectifier without matching used for obtaining the input impedance of the rectifier. (A: reference plane, B: DC-pass capacitor, C: bias resistor, D: resistor load, F and E: Schottky diodes).

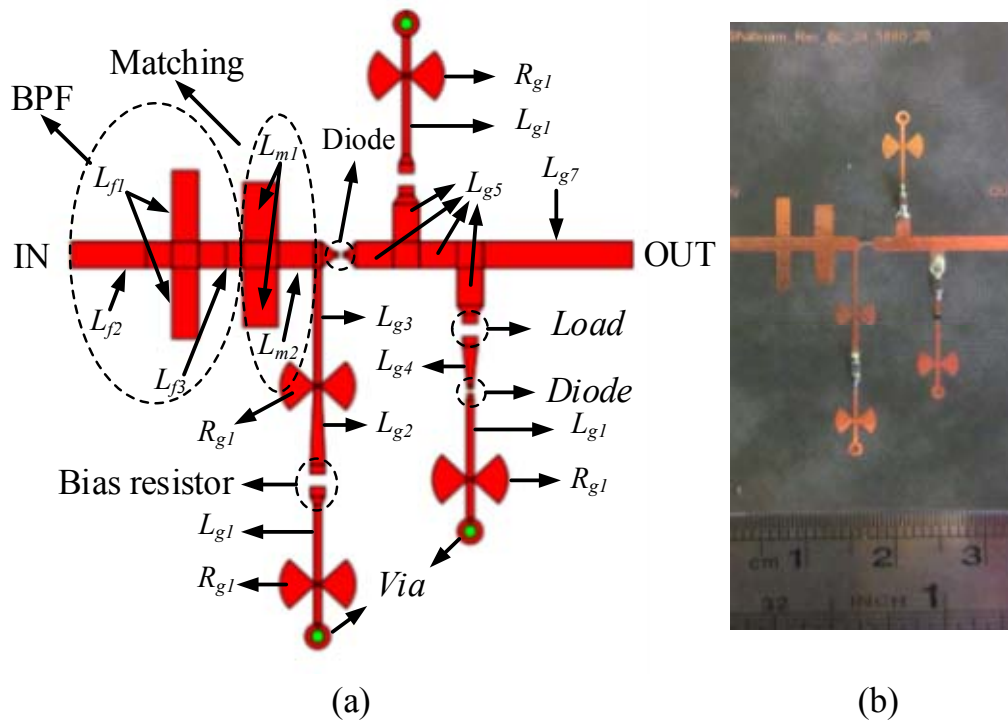


Figure 3.20: (a) Layout of the 24 GHz sensitivity improvement rectifier. (b) Fabricated prototype. Geometry parameters are following: $L_{f1} = 6$, $L_{f2} = 4.24$, $L_{f3} = 2.66$, $L_{m1} = 3.5$, $L_{m2} = 3.3$, $R_{g1} = 2.1$, $L_{g1} = 4.6$, $L_{g2} = 4.55$, $L_{g3} = 6.9$, $L_{g4} = 2.31$, $L_{g5} = 2.24$ (dimensions in millimeters).

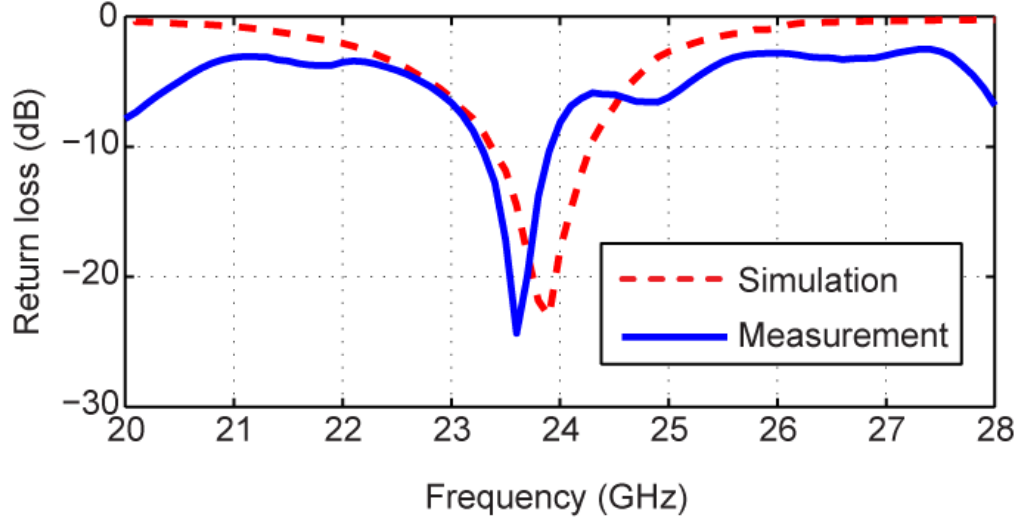


Figure 3.21: Simulation and measurement results of the 24 GHz sensitivity improvement rectifier return loss.

line keeps the circuit in a proper distance (minimum distance of a wavelength at the operating frequency) from connectors of the test fixture. Simulations are carried out at both schematic and layout levels. Layout level simulations are performed using electromagnetic (EM) simulator Momentum in ADS. The designed rectifier is fabricated on 20 mil thick Rogers 5880 (Figure 3.20). Figure 3.21 shows simulated and measured impedance matching conditions of the rectifier. Good agreement between simulation and measurement confirms the accuracy of the method used in determining the diode input impedance.

Considering the fact the conversion efficiency is limited by the diode conduction loss if all other losses are neglected then, the overall efficiency (also it may be called the Maximum Theoretical Conversion Efficiency (MTCE)) is driven by [63], [64]

$$\eta = \frac{I}{I + \frac{V_d}{2V_{out}}} \quad (3.5)$$

where V_{out} is the DC output voltage and V_d is the voltage drop over the conducting diode, $V_d = 0.7$ V in this case. In the proposed rectifier, as it was explained in detail in the previous paragraphs, the output resistive load is not constant and changes with the rectified current. As such, it is more sensible to use (3.5) for calculating efficiency since (3.5) does not include any load [65]-[67]. The

DC output voltage and the MTCE of the fabricated rectifier are measured and compared with simulated counterpart shown in Figure 3.22 and Figure 3.23. The obtained results show a good agreement between simulation and measurement. The results confirm that using the self-biased technique improves the detection sensitivity of the rectifier such that the rectifier starts operating even for a small level of input RF power (RF power less than 1 mW) at 24 GHz. Targeting 1 mW input RF power, the measured overall efficiency or MTCE of 15% is obtained for the designed rectifier which is believed to be the highest efficiency reported to date.

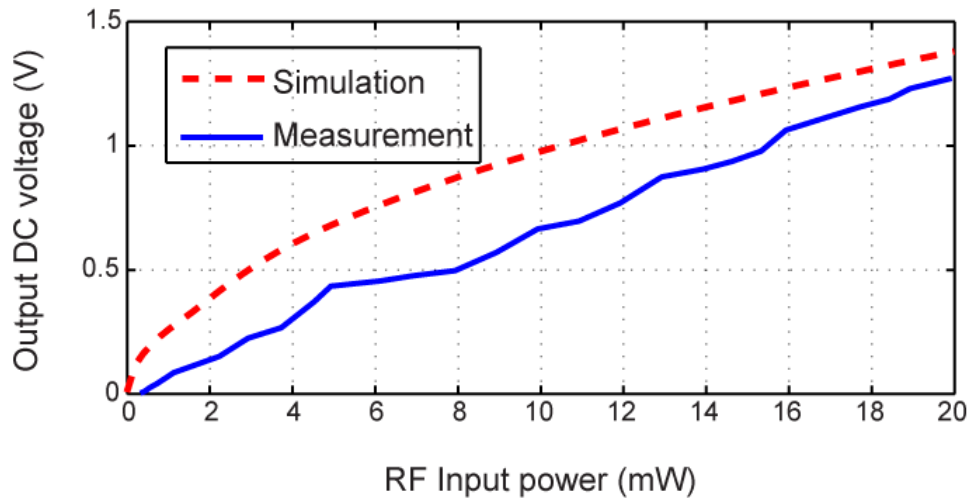


Figure 3.22: DC Output voltage versus input power of the 24 GHz sensitivity improvement rectifier.

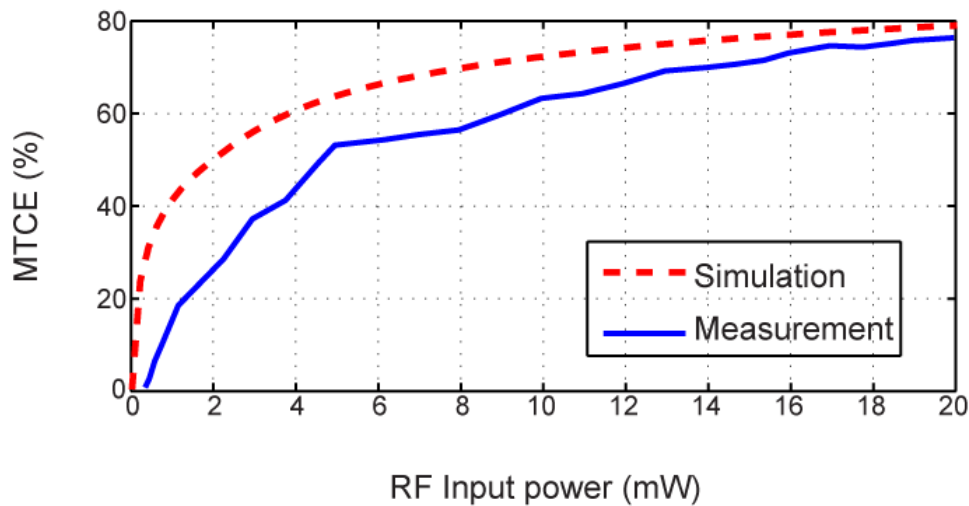


Figure 3.23: Maximum theoretical conversion efficiency (MTCE) versus input power of the 24 GHz sensitivity improvement rectifier.

The RF-to-DC conversion efficiency can also be calculated by using (3.1) and (3.2). To do so, another prototype of the rectifier without diode at the output (Figure 3.14) is fabricated. The output voltage of these two rectifiers, the self-biased rectifier (Figure 3.14) and improved structure of the self-biased rectifier (Figure 3.16), is measured and shown in Figure 3.24. Since these two circuits are similar in terms of generating DC voltage, (the improved structure of the self-biased rectifier has only the advantage of temperature stability) then the rectifier with a fixed resistive load is used to measure the RF-to-DC conversion efficiency (Figure 3.25). According to Figure 3.26, the maximum measured RF-to-DC conversion efficiency of 42% is reported at 18 mW RF power. To the best of our knowledge, the obtained efficiency is the maximum reported to date. For better evaluation, a comparison is given among the documented millimeter-wave rectenna designs (Table 3.1).

Table 3.1: Comparison among previously designed high frequency rectifiers.

Source	Operating Frequency (GHz)	Required RF Power (mW) for Maximum Efficiency	Maximum Measured Efficiency (%)
[10]	35	120	39
[12]	24	130	54
[13]	25.7	6.3	15
[14]	24	210	47.9
[67]	35	25.6	52
Presented design	24	18	42

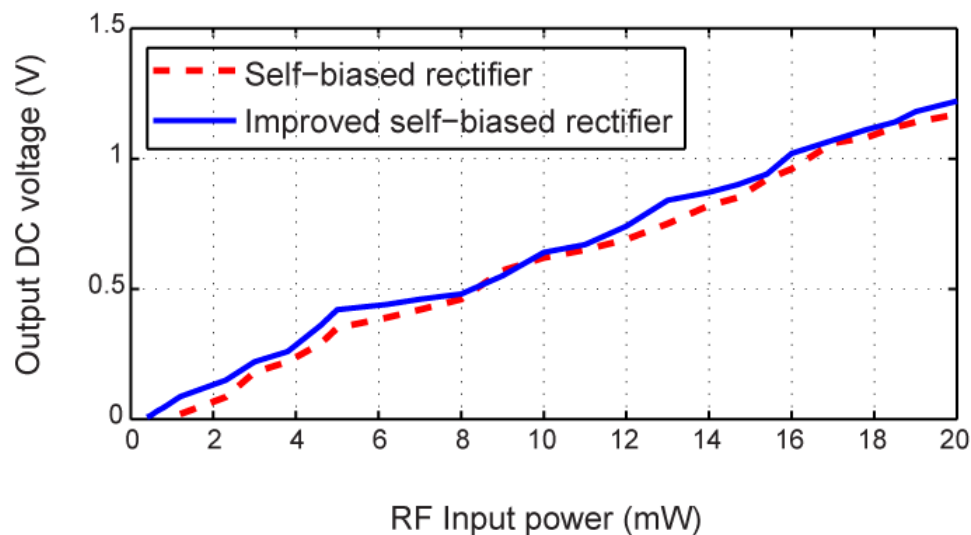


Figure 3.24: Measured output DC voltage from two rectifiers; the self-biased rectifier and the improved configuration of the self-biased rectifier (thermal stability), versus input power.

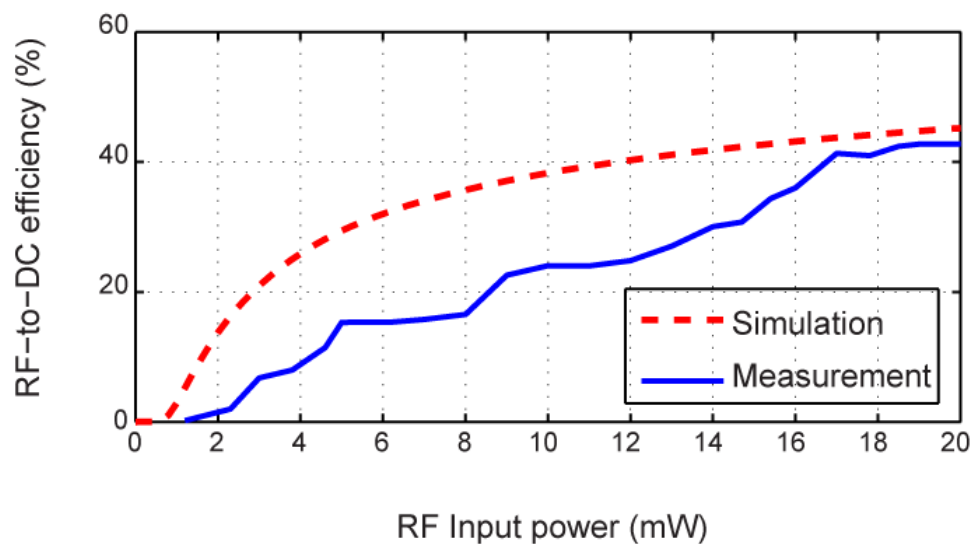


Figure 3.25: RF-to-DC conversion efficiency of the designed self-biased rectifier versus input power.

3.2.3 Analytical analysis of a rectifier diode

The rectification is a nonlinear process, in which the final product is a combination of some resulting DC component plus harmonics. This nonlinearity is mainly pronounced as a function of the input power. Although linear and nonlinear circuit models are both used to predict the rectifier behavior, the nonlinear model has better accuracy, especially at millimeter-wave frequency, since it considers the harmonics oscillation through the nonlinear junction capacitance. Therefore, to yield a better understanding of the rectification process, a closed-form equation describing the nonlinear rectification effects is needed. To obtain a closed-form solution, the analytical analysis of the nonlinear rectification process of a diode has been studied in [68] and [69]. Because of some simplifications made in truncated series of nonlinear functions, obtained results presented in [68] cannot provide an accurate insight into the rectification behavior. In [69], a numerical approach for the complete dynamic range of a rectifier circuit from “square-law” to “linear” is presented. However, in [69] to simplify the mathematical manipulations, only DC component has been considered to study the final outcome of rectification process and generated harmonics has been neglected. To ensure the design accuracy, and also to realize the maximum RF-to-DC conversion efficiency, an accurate diode model considering harmonics is required. This is essential especially for millimeter-wave circuit design where the nonlinear effect of diode junction capacitance, leading to a large leakage current, becomes dominant. The frequency-dependent behavior of diode junction capacitance has been investigated in [58].

In this section, to analyze the contribution of DC component and relevant harmonics generated through the nonlinear effect of a diode, an analytical framework is presented and discussed. To do so, a Schottky rectifier circuit shown in Figure 3.26 is considered, which includes a RF generator, the circuit model of Schottky diode considering diode series resistance (R_s) and junction capacitance (C_j), an external bias path and a resistive load at the output. It is worth noting that in order to simplify the circuit model the parasitic and packaging effect of the diode are ignored. It is assumed that the diode follows an exponential behavior given by

$$i_D = I_s \left(e^{\beta v_D} - 1 \right) \quad (3.6)$$

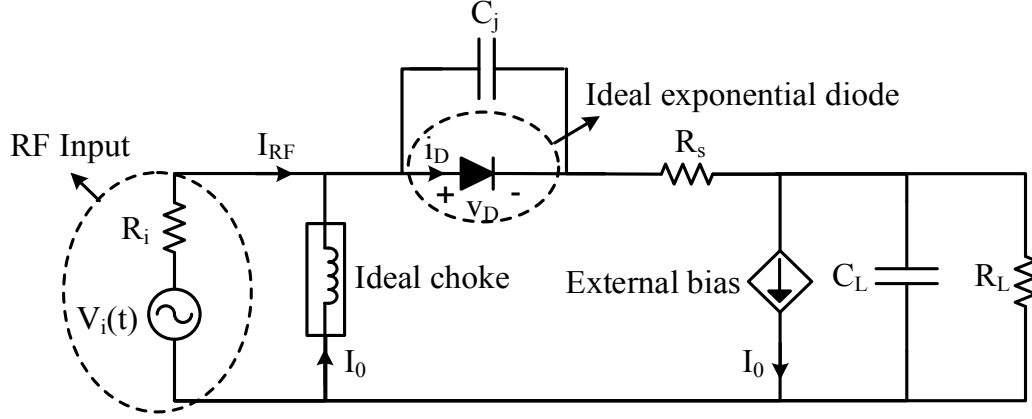


Figure 3.26: Rectifier simplified equivalent circuit.

where i_D is the current through the nonlinear diode, I_s is the saturation current, v_D is the voltage across the nonlinear diode and $\beta = \frac{q}{n k T}$ in which q is the electronic charge, n is the diode ideality factor, k is the Boltzmann constant and T is temperature in Kelvin.

In order to obtain a relationship between the input RF power and output power of the circuit, a differential equation of the circuit shown in Figure 3.26 is presented by

$$a\mu + y + y' = a[\exp\{(x - y) - b(y' + y) - k\mu\} - 1] + c[(x' - y') - b(y'' + y')] \quad (3.7)$$

where $x = \beta v_i$ is the input forcing function and $y = \beta v_{out}$ is the output result, and $a = \beta R_L I_s$, $b = (R_s + R_i) / R_L$ (represents the resistance ratio), $c = C_j / C_L$ (the capacitance ratio), $k = \beta R_s I_s$, and $\mu = I_0 / I_s$ is the bias-current parameter. Primes ' and '' denote $\frac{\partial}{\partial t}$ and $\frac{\partial^2}{\partial t^2}$, respectively, with $\tau = t / R_L C_L$. Since this study is focused on the rectification process for energy harvesting applications at millimeter-wave frequency, the circuit model (Figure 3.26) is simplified to Figure 3.27, by removing the external bias source (i.e. $I_0 = 0$). Therefore (3.7) is rewritten as

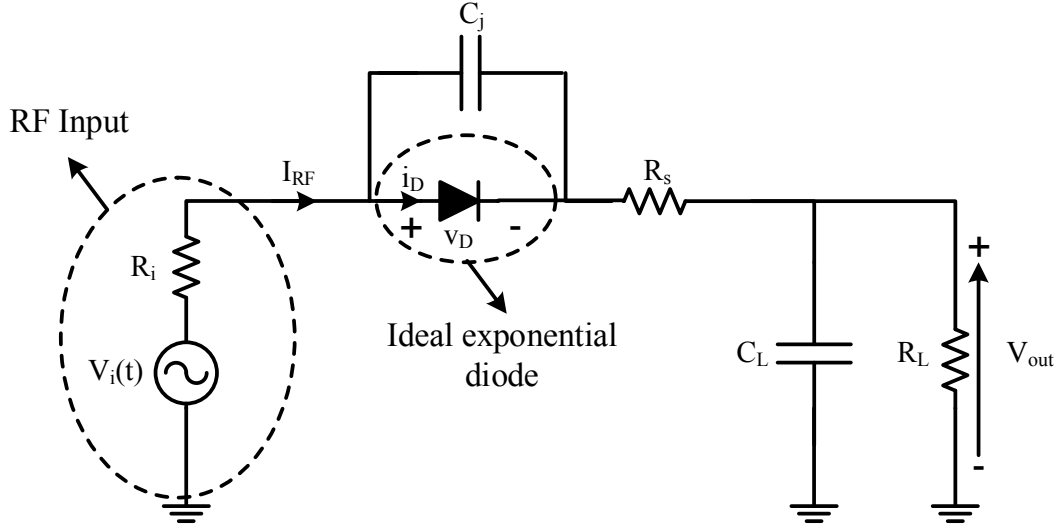


Figure 3.27: Rectifier simplified equivalent circuit.

$$y + y' = a[\exp \{ (x - y) - b(y' + y) \} - 1] + c[(x' - y') - b(y'' + y')] \quad (3.8)$$

Although the output voltage can be calculated from a numerical integration of (3.8), the Ritz-Galerkin (RG) technique presented in [69] is adopted to find the closed-form solution. To apply the RG method, the differential equation (3.8) is represented by

$$\xi \left[x, y, \frac{\partial}{\partial \tau}, \frac{\partial^2}{\partial \tau^2} \right] \equiv 0 \quad (3.9)$$

where ξ is a nonlinear operator. Considering the input signal as

$$x = X \cos(\nu \tau) \quad (3.10)$$

while $\nu = \omega R_L C_L$ and $X = \beta V_i$. Then, the exact output voltage, $y(\tau)$, is approximated by the following basis function sets:

$$\tilde{y}(\tau) = \sum_{k=1}^M Y_k \psi_k(\tau) \quad (3.11)$$

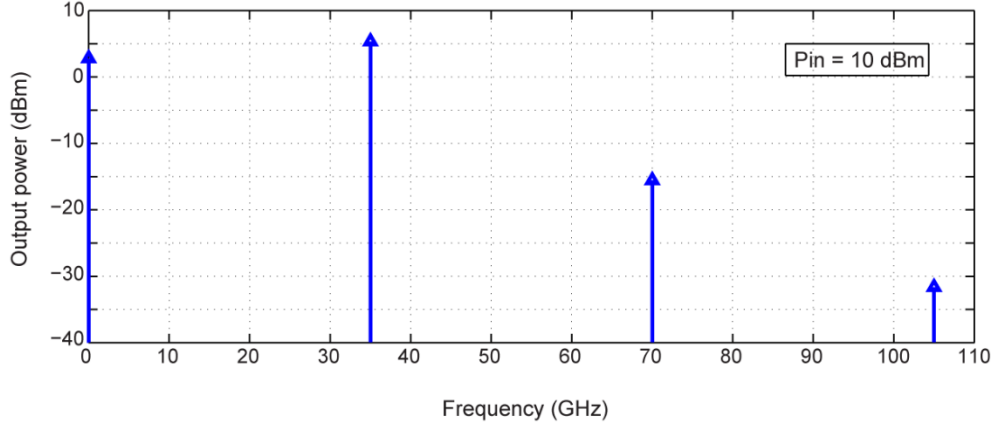


Figure 3.28: Power distribution at the output of the rectifier shown in Figure 3.27.

where $\psi_k(\tau) = \cos(k\nu\tau + \theta_k)$ are M linearly independent functions which represent DC component and different harmonics of the output signal. Also, Y_k signifies adjustable constant coefficients. Since $\tilde{y}(\tau)$ approximates the output voltage, then (3.11) cannot satisfy the differential equation. Therefore, (3.9) can be formulated as

$$\xi \left[x, \tilde{y}, \frac{\partial}{\partial \tau}, \frac{\partial^2}{\partial \tau^2} \right] = \epsilon(\tau) \neq 0 \quad (3.12)$$

where $\epsilon(\tau)$ is called the residual which is a degree of the experienced error. According to [71], the residual is minimized when the Ritz condition of orthogonality is satisfied as

$$\int_{\tau_1}^{\tau_2} \epsilon(\tau) \psi_k(\tau) d\tau = 0 \quad k = 1, \dots, M \quad (3.13)$$

Therefore, unknown coefficients, Y_k , can be found from a system of equations with M equations and M unknown results from (3.13). In order to confine the number of unknown coefficients, the significant harmonics of the rectifier output should be determined. To do so, the circuit shown in Figure 3.27 is simulated for 10 dBm input power at 35 GHz (Figure 3.28). The simulation results are drawn at the output of the Schottky diode without considering the output capacitor (since capacitor C_L is considered as a DC-pass filter). According to the obtained results, it is concluded

that the DC component and the first harmonic (fundamental frequency) carry out 32% and 66% of the output power, respectively, and the second and third harmonics (the spectral components at 70 GHz and 110 GHz) have a very small portion of energy (-15 dBm and -35 dBm). Therefore, $\tilde{y}(\tau)$ in (3.11) is considered as

$$\tilde{y}(\tau) = Y_0 + Y_1 \cos(\nu\tau + \theta_1) \quad (3.14)$$

in which Y_0 represents the DC component and Y_1 is the constant coefficient of the first harmonic. Hence, the residual function is presented by

$$\begin{aligned} \epsilon(\tau) = & a[\exp\{X \cos(\nu\tau) - (1+b)Y_0 - (1+b)Y_1 \cos(\nu\tau + \theta_1) + b\nu Y_1 \sin(\nu\tau + \theta_1)\} - 1] \\ & + (Y_1 \nu (c(1+b) + 1) \sin(\nu\tau + \theta_1) + (cb\nu^2 - 1) \cos(\nu\tau + \theta_1) \\ & - cX\nu \sin(\nu\tau + \theta_1) - Y_0 \end{aligned} \quad (3.15)$$

In order to reduce the algebraic complexity, it is assumed that $\theta_1 = 0$ then the residual function is given by

$$\int_0^{2\pi} \epsilon(\tau) d(\nu\tau) = 0 \quad (3.16)$$

$$\int_0^{2\pi} \epsilon(\tau) \cos(\nu\tau) d(\nu\tau) = 0 \quad (3.17)$$

By casting (3.15) into (3.16) and (3.17) and after some straightforward multiplications, the resulting equation are given by

$$2\pi(a + Y_0) + ae^{-(Y(1+b))} \int_0^{2\pi} \exp((X - Y_1(b+1))\cos(\nu\tau) + b\nu Y_1 \sin(\nu\tau)) d(\nu\tau) = 0 \quad (3.18)$$

$$\begin{aligned} & -\pi(cb\nu^2 - 1)Y_1 \\ & + ae^{-(Y(1+b))} \int_0^{2\pi} \exp((X - Y_1(b+1))\cos(\nu\tau) + b\nu Y_1 \sin(\nu\tau)) \cos(\nu\tau) d(\nu\tau) = 0 \end{aligned} \quad (3.19)$$

The sum of two trigonometric functions can be expressed as a single trigonometric function

to simplify (3.18) and (3.19) as follows

$$-2\pi (a + Y_0) + ae^{-Y(1+b)} \times \int_0^{2\pi} \exp(R \cos(\nu\tau + \varphi)) d(\nu\tau) = 0 \quad (3.20)$$

$$-\pi (cb\nu^2 - 1)Y_1 + ae^{-Y(1+b)} \times \int_0^{2\pi} \exp(R \cos(\nu\tau + \varphi)) \cos(\nu\tau) d(\nu\tau) = 0 \quad (3.21)$$

where

$$R = \sqrt{(X - Y_1(b+1))^2 + (b\nu Y_1)^2} \quad (3.22)$$

$$\varphi = \tan^{-1} \left(\frac{b\nu Y_1}{X - Y_1(b+1)} \right) \quad (3.23)$$

The closed-form solution of the above-mentioned equations can be obtained by employing a modified Bessel function definition as follows

$$-2\pi (a + Y_0) + 2\pi ae^{-Y(1+b)} I_0(R) = 0 \quad (3.24)$$

$$-\pi (cb\nu^2 - 1)Y_1 + 2\pi ae^{-Y(1+b)} I_1(R) \cos(\varphi) = 0 \quad (3.25)$$

where I_0 and I_1 are the modified Bessel function of the first kind of order 0 and 1, respectively.

Therefore

$$I_0(R) = \left(1 + \frac{Y_0}{a} \right) e^{Y(1+b)} \quad (3.26-a)$$

$$I_1(R) \cos(\varphi) = \left(\frac{1}{2} (cb\nu^2 - 1) e^{Y(1+b)} \right) Y_1 \quad (3.26-b)$$

Since (3.26) does not have a closed-form solution, an iterative method is used to find Y_0 and Y_1 . To do so, for a fixed value of the input voltage, X , by iterating the DC component, Y_0 , a

series of first harmonic coefficient, Y_1 , can be obtained from (3.26-a). Then, the final solution, Y_0 and Y_1 , can be found by satisfying (3.26-b). On the other hand, in order to solve (3.26-a), the inverse of the modified Bessel function is needed which does not have a closed-form solution. Therefore, a root-finding algorithm called the Secant method [70] is adopted to find the solution of (3.26-a). The Secant method is an iterative root-finding algorithm which uses a secant line passing through two points of the function $f(Y_1) = I_0(R) - \left(1 + \frac{Y_0}{a}\right) e^{Y_0(1+b)}$ to approximate its root. Hence, considering two approximated points $(Y_1^{(k-1)}, f(Y_1^{(k-1)}))$, and $(Y_1^{(k)}, f(Y_1^{(k)}))$, the Secant algorithm returns an estimate of the function's root as $pk+1$ [70]:

$$Y_1^{(k+1)} = Y_1^{(k)} - \frac{Y_1^{(k)} - Y_1^{(k-1)}}{f(Y_1^{(k)}) - f(Y_1^{(k-1)})} f(Y_1^{(k)}) \quad (3.27)$$

It has been shown that the convergence rate of the Secant method is superlinear with 1.62 [70]. Moreover, it is noted that the Secant algorithm requires two initial points ($Y_1^{(0)}$ and $Y_1^{(1)}$), which have to be determined cautiously. In order to accelerate the convergence to the optimum solution, the signs of $f(Y_1^{(0)})$ and $f(Y_1^{(1)})$ should be different, hence $Y_1^{(0)}$ and $Y_1^{(1)}$ can be obtained satisfying this condition.

Figure 3.29 depicts the simulation and analytical results of the DC component and harmonics of the rectifier output voltage for a 10 mW input RF power at 35 GHz. As observed, there is a good agreement between analytical and simulation results. However, there is a slight difference between the two results which can be traced into the fact that, in simulation, higher order of harmonics are considered which increases the accuracy of the obtained results compared to the analytical method where only one harmonic is considered. It is worth noting that, considering higher order of harmonics in (3.11) leads to more accurate results at the expense of a very high computational complexity.

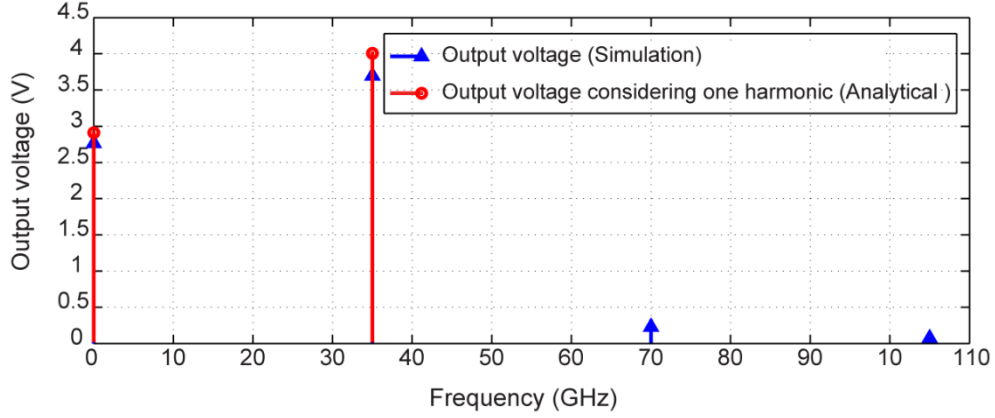


Figure 3.29: Output voltage of the rectifier shown in Figure 3.27.

3.2.4 35 GHz harmonic harvesting rectifier

In the previous section, an analytical analysis was developed using a Ritz-Galerkin method to investigate the nonlinear behavior of rectification process in a rectifier circuit. According to the obtained equations, it was shown that the major portion of energy is carried in the first harmonic and DC component. Then harvesting harmonics can increase the efficiency of the rectifier. To justify the idea of harmonic harvesting technique at millimeter-wave applications, a new structure of full-wave rectifier operating at 35 GHz with the ability of harmonic harvesting is proposed and studied. Subsequently, the performance of the proposed harmonic harvesting structure is compared with the modified voltage doubler configuration.

According to (3.11), the diode's output can be expressed as a summation of the DC part and the harmonics of the fundamental frequency. As explained before, in conventional rectifiers operating at medium range of input RF power (0-100 mW) a substantial portion of energy is wasted in harmonics which normally are trapped by a DC-pass filter to generate a flat output DC voltage. Therefore, harvesting harmonics instead of suppressing them will result in efficiency increment. Figure 3.30 presents a modified voltage doubler rectifier with harmonic harvesting feature. In the proposed structure, diodes D_1 and D_2 realize a full-wave rectification process. At the output of the voltage doubler (test point A shown in Figure 3.30) the DC rectified wave plus some harmonics are available. Capacitor C_2 separates harmonics from the DC part by blocking the DC current. Then, diode D_3 rectifies the harmonics. Figure 3.31 shows the spectrum distribution of the rectified signal at the output of the voltage doubler (test point A, Figure 3.30) and harmonic harvester (test

point B, Figure 3.30). As observed, a significant percentage of the available energy existing in harmonics is rectified. The harmonics rectification will result in increasing the DC level. Furthermore, two DC-pass filters in the form of quarter wavelength resonator stubs are used to reject any RF signals (even though the level of RF signals is very low) and smooth the generated DC voltage.

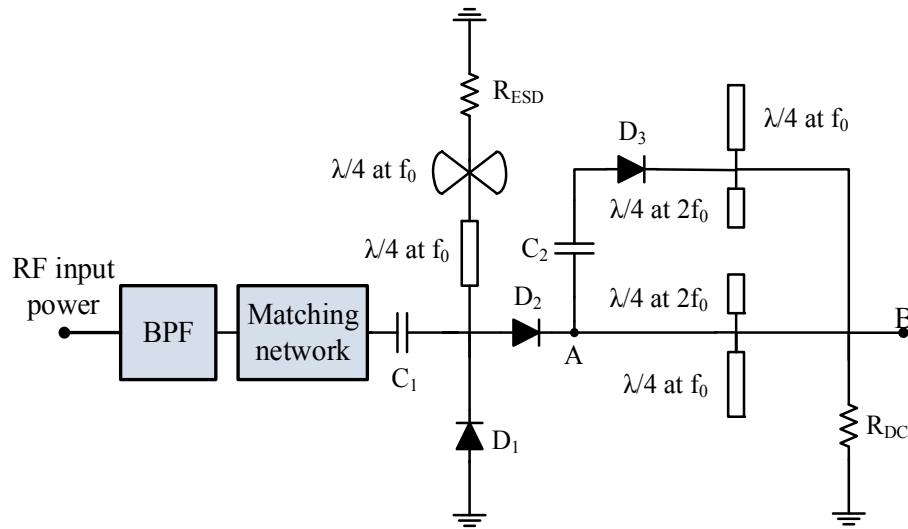


Figure 3.30: Millimeter-wave harmonic harvesting rectifier.

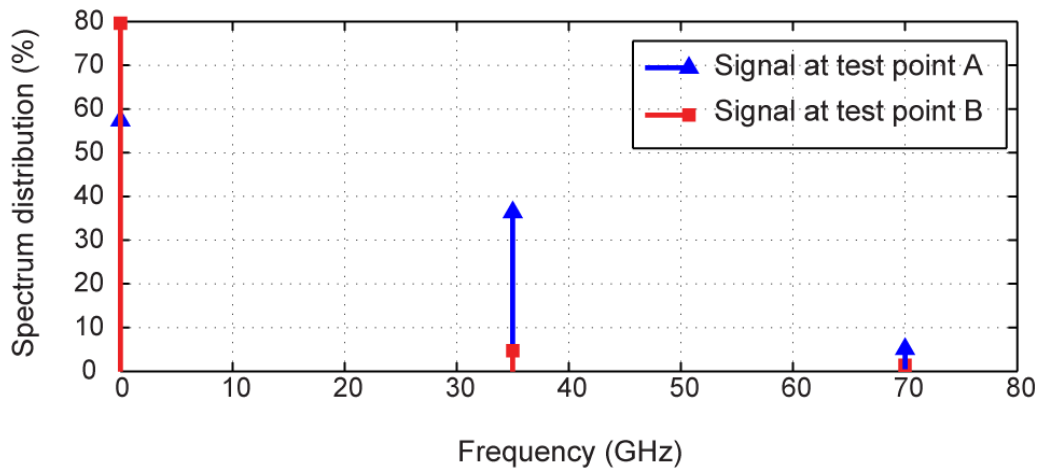


Figure 3.31: Distribution of the rectified signal and harmonics at the output of the voltage doubler (test point A) and harmonic harvesting (test point B).

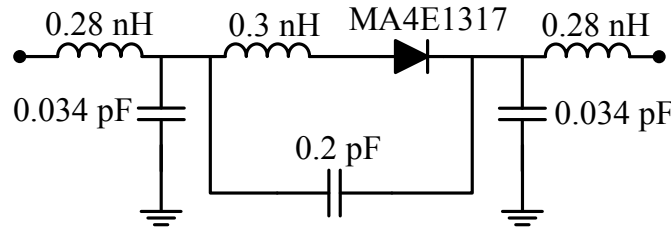


Figure 3.32: Optimized voltage-independent parameter of MA4E1317 Schottky diode.

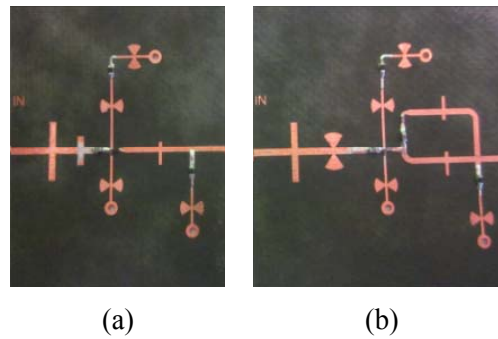


Figure 3.33: (a) Fabricated modified 35 GHz voltage doubler rectifier. (b) Fabricated 35 GHz harmonic harvesting rectifier

The same Schottky diode used in the previous designs (MA4E1317 from MACOM) is considered as rectifying component. Since the design is targeting at millimeter-wave frequency (35 GHz), then the experimental characterization technique is used to determine the input impedance and design the matching circuit. To do so, the rectifier Schottky diode is firstly measured individually to obtain the parasitic and packaging parameters as explained in section 3.2.1. The obtained model shown in Figure 3.32 is used for initial design simulation of the rectifier. In the next step, the rectifier circuit without matching network is designed and the optimization is run to get the maximum efficiency. Then the harmonic harvester rectifier is designed and its performance is compared with a modified structure of a voltage doubler shown in Figure 3.4. Both circuits are operating at 35 GHz. Simulations are carried out on both schematic and layout levels. Layout level simulations are performed using Momentum in ADS. Similarly to the previous designs, the simulated circuit is brought back to the schematic in order to run co-simulation process. The co-simulation feature is needed to reassure that all components show desired performance at 35 GHz. In order to experimentally test and evaluate the system improvement in a real measurement condition, the optimized circuits (the conventional voltage doubler and the harmonic harvester) are

fabricated on a 10-mil-thick high frequency Rogers 5880 ($\epsilon_r = 2.2$, $\tan\delta = 0.0004$ and $17\ \mu m$ copper thickness), (Figure 3.33 (a), (b)).

The simulated and measured results of the impedance matching conditions of the harmonic harvesting rectifier are shown in Figure 3.34. Good agreement between simulation and measurement justifies the accuracy of the method used in determining the diode input impedance and designing the related matching network.

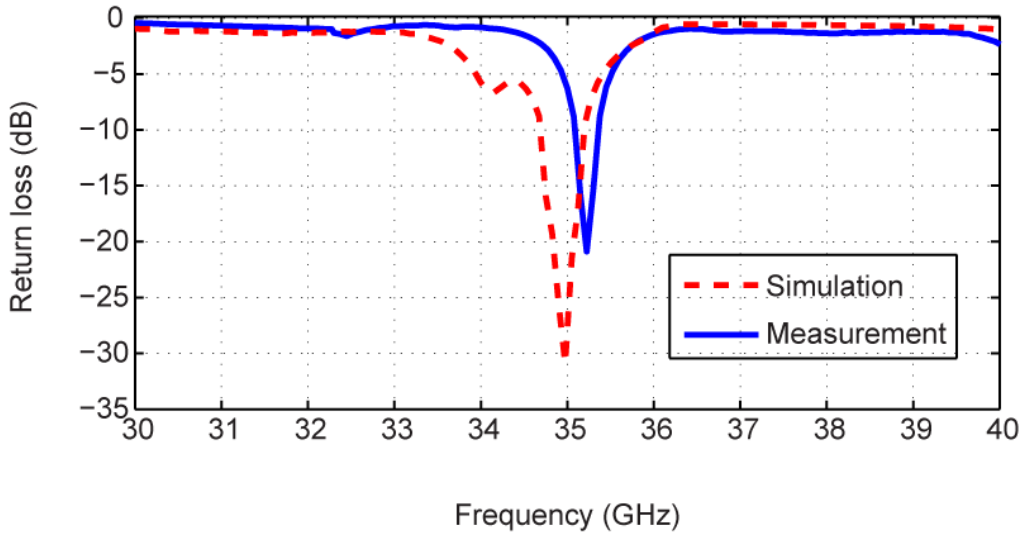


Figure 3.34: Simulation and measurement results of the harmonic harvester rectifier return loss.

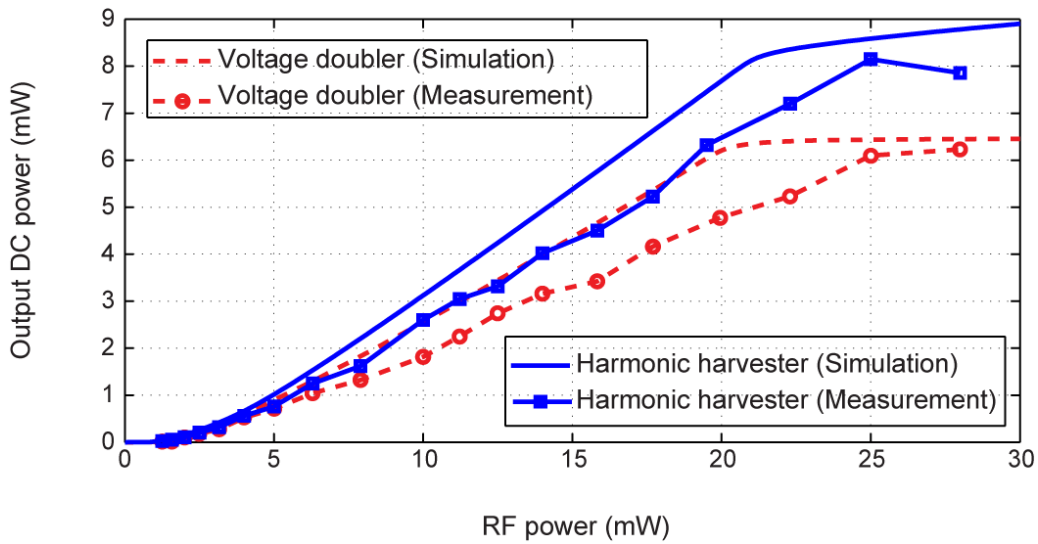


Figure 3.35: Output DC power versus input RF power.

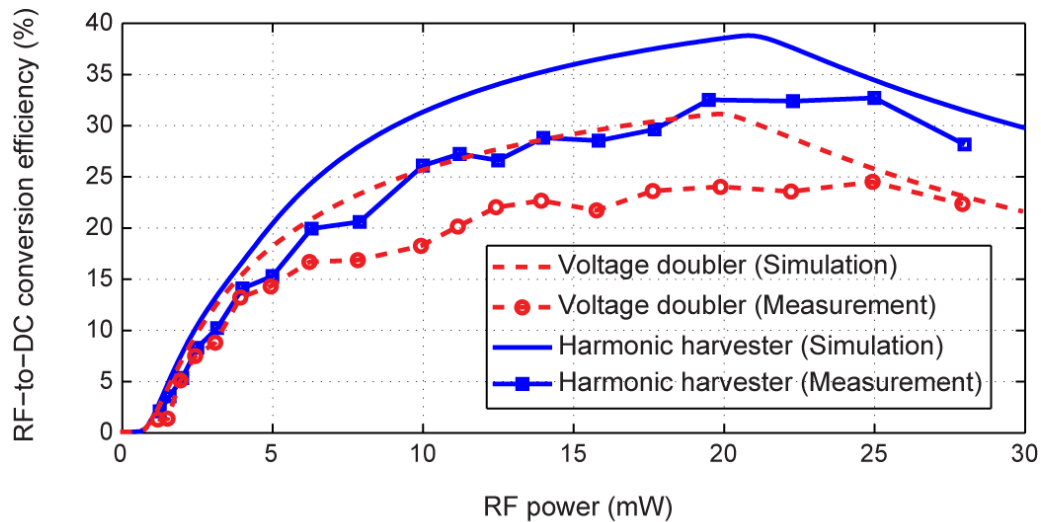


Figure 3.36: Rectifier efficiency versus input RF power.

Table 3.2: Comparison among previously designed high frequency rectifiers.

Source	Operating Frequency (GHz)	RF Power (mW) for Maximum Efficiency	Maximum Measured Efficiency (%)	Rectifier Element
[10]	35	120	38	DMK 6606 Schottky
[15]	35	100	39	0.13- μ m CMOS
[15]	94	1000	29.9*	0.13- μ m CMOS
[58]	35	120	29	GaAs Schottky
[98]	35	60	33	DMK 6606 Schottky
Presented design	35	20	34	MA4E1317 Schottky

*Asterisked efficiencies are related to the rectenna circuits that include antenna effects in their efficiency calculations.

Figure 3.35 and Figure 3.36 show the output DC voltage and RF-to-DC conversion efficiency of rectifiers. The signal generator, E8267D from Agilent Technologies, is used to power both rectifiers. The maximum measured conversion efficiency of 23% at 20 mW input RF power is reported for voltage doubler rectifier while for the harmonic harvesting rectifier the measured conversion efficiency is 34% for the same level of input power. The obtained results verify that the harmonic harvesting configuration increases the conversion efficiency by up to 11%. This shows a significant enhancement in terms of conversion efficiency. According to the state-of-the-art millimeter-wave rectifier reported in the literature, the proposed structure is believed to exhibit the highest conversion efficiency at medium power range. For a better evaluation, a comparison is given among the documented millimeter-wave rectifier designs (Table 3.2). The RF-to-DC conversion efficiency of the rectifier is defined as the ratio of the output DC power to the incident power (3.1).

3.3 Conclusion

This chapter describes the design process of various configurations of up-microwave and millimeter-wave rectifier circuits operating at low and medium level of RF power. The first designed rectifier is a voltage doubler operating at 24 GHz with measured RF-to-DC conversion efficiency of 40% at 35 mW input power. The second prototype is a 24 GHz self-biased rectifier with measured maximum efficiency of 78% at 16 mW input power. The third rectifier is a harmonic harvesting rectifier operating at 35 GHz with measured efficiency of 34% at 20 mW input power. The measurement results of each individual structure justify the proposed configurations. The designed rectifiers can be used in compact rectenna circuits with application of wireless energy harvesting and wireless power transmission.

CHAPTER 4 UP-MICROWAVE RECTENNA USED FOR WIRELESS POWER TRANSMISSION AND ENERGY HARVESTING

As mentioned before, a rectenna consists of a receiving antenna and a rectifier circuit. In chapter 3, various structures of rectifier for up-microwave and millimeter-wave applications are studied and in the sequel different structures of antenna are proposed. During the past years, different structures of antenna such as dipole, microstrip patch, loop, spiral, coplanar patch and parabolic have been used in designing the rectenna [8], [71]-[76]. A proper choice of antenna for wireless power transmission applications needs to have a high gain in order to capture more RF power. Therefore, using a single antenna element, which provides a very limited RF power to the rectifier and results in a lower conversion efficiency level, is generally not appropriate for this type of applications. The use of an antenna array seems to be the most promising solution to provide more RF power [5]. Although antenna array is an effective means of increasing the receiving power but a tradeoff arises between the antenna size and the radiation gain or efficiency. Also it is worth to mention that the rectenna array needs a precise main beam alignment for an efficient power transmission because the main beam of the rectenna array only has a limitedly narrow beam-width. If main beams of the transmitting and the receiving antennas cannot be aligned correctly, the rectenna efficiency would drop significantly. Although many kinds of rectennas have been proposed, most works are focused on the rectenna design using single antenna element without considering the application of the antenna array. Moreover, an appropriate WPT antenna should have an easy and low-loss feed-line. To meet these requirements, single layer planar structure is a viable solution. In terms of polarization, linearly polarized (LP) rectenna, circularly polarized (CP) rectenna and dual polarized rectenna designs can be found in the open literatures. But CP antenna is generally preferred from the point of view of polarization for WPT because it allows for much less sensitive positioning and orientation of transmitter versus receiver or vice-versa [74]-[75]. This scheme is able to offer a constant DC output voltage compared to a linearly polarized configuration. Moreover, an appropriate WPT antenna should have an easy and low-loss feed-line. To meet these requirements, single layer planar structure is a feasible solution.

In this chapter, two different structures of antenna including LP antenna and CP antenna are proposed and studied in array configurations of interest. Consequently, they are integrated to the rectifier circuits presented in chapter 3 and their performance as a rectenna is evaluated. These

rectennas can have wide applications in energy harvesting and wireless power transmission at up-microwave and millimeter-wave frequencies.

4.1 Design of a 24 GHz linearly polarized SIW antenna array

To yield a narrow beam-width high-gain rectenna, a compact structure of a K-band 4×4 antenna array on substrate integrated waveguide (SIW) technology in the form of slot array is proposed. The SIW is considered as an alternative to the widely used microstrip technology in applications where features such as increased isolation and compact size are important. In millimeter-wave frequencies SIW technology is particularly attractive due to the fact that it can present less transmission losses and radiation leakage than its microstrip counterpart [77].

Figure 4.1 shows the schematic of the 4×4 array antenna. The antenna structure and the SIW feed network are designed on a single layer 10-mil-thick high frequency Rogers ($\epsilon_r = 2.2$, $\tan\delta = 0.0004$ and $17 \mu m$ copper thickness). Radiating elements are the longitudinal slots which are etched on the SIW top surface. The slots are placed half a wavelength apart to radiate in phase. To align the slots at peaks of the standing wave along the SIW structure, SIWs are terminated by short circuits that are three quarter wavelengths away from the center of the last slot. The design procedure of the slots is similar to that of the SIW slot array which was presented in [78]-[82]. To connect the antenna array to the designed rectifier, a wideband microstrip to SIW transition is designed and is shown in Figure 4.2. The design procedure of this transition is illustrated in details in [83]-[84]. The simulated $|S_{11}|$ and insertion loss of the transition is shown in Figure 4.3. Three T-type power dividers are used to feed the 1×4 array antennas in phase. Simulated $|S_{21}|$ and $|S_{11}|$ of the T-shaped junctions are presented in Figure 4.3. To reduce the side lobe level of the 4×4 antenna array in H plane, the 1×4 antenna arrays are placed 0.52λ apart each other. Note that dielectric and metallic losses have been considered in the simulation results of the power dividers and the antenna array. Ansoft HFSS version 14 is used to simulate the antenna structure. The simulated gain of the antenna at 24 GHz is 14.7 dB and the simulated radiation efficiency is 87%. Note that dielectric loss decreases the radiation efficiency by 2% while the metallic loss decreases the radiation efficiency by 11%. Metallic loss decreases the gain of the antenna by 0.5 dB while it does not have significant effect on the bandwidth of the antenna. All the dimension of the antenna array and the microstrip to SIW transition is illustrated in Table 4.1.

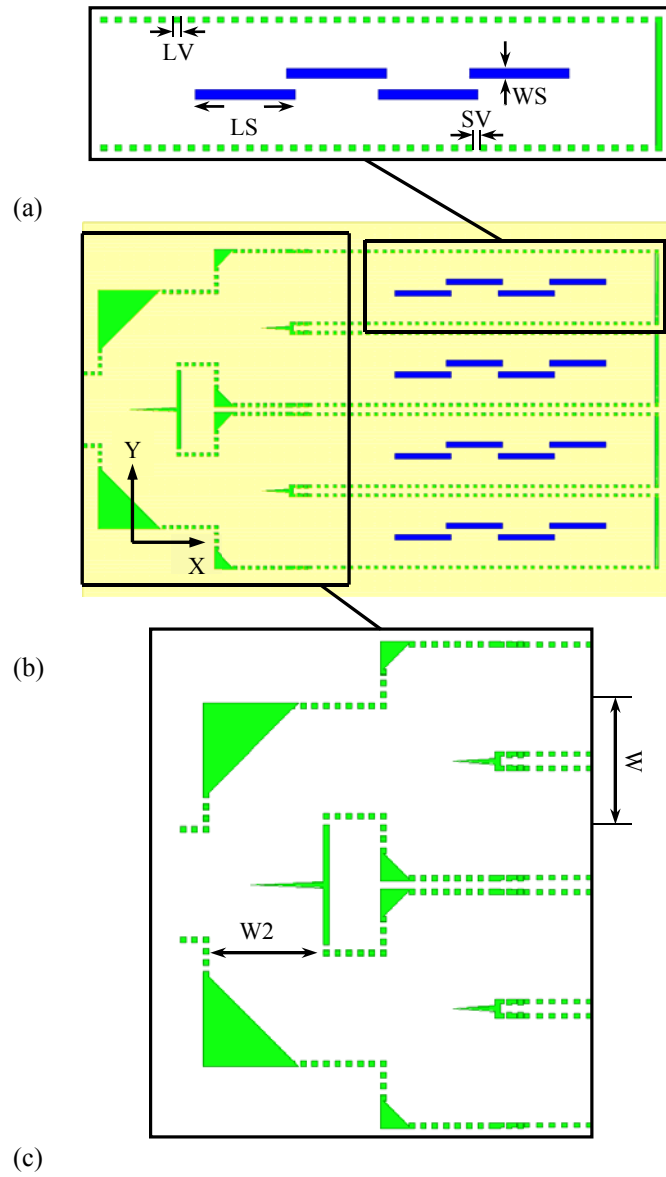


Figure 4.1: Geometry and 3-D view of the (a) 1×4 antenna array, (b) 4×4 antenna array, and (c) power divider.

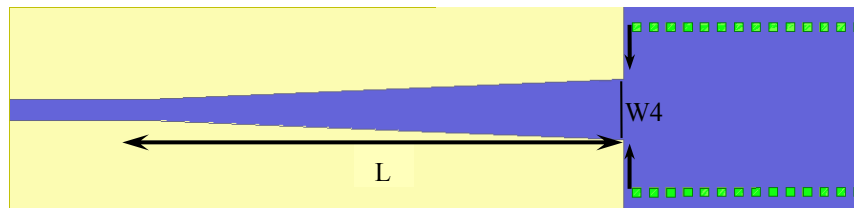


Figure 4.2: Microstrip to SIW transition.

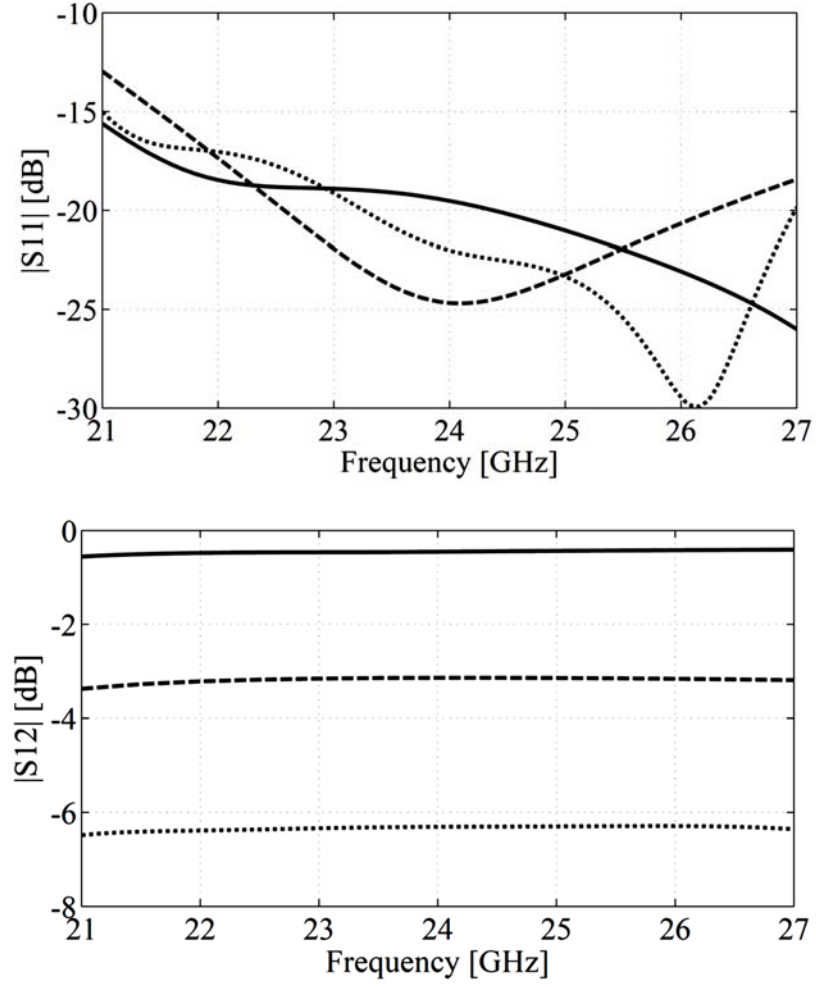


Figure 4.3: Simulated $|S_{11}|$ and $|S_{12}|$ of the solid: microstrip to SIW transition, dashed: 1×2 T shaped power divider, and dotted: 1×4 power divider.

Table 4.1: Dimensions of 4×4 antenna array (unit: mm).

Symbol	Value (mm)
LS	4.5
LV	0.3
WS	0.45
SV	0.36
W	6.5
W1	5.5
W2	6
W3	3.5
W4	2.12
L	16.7

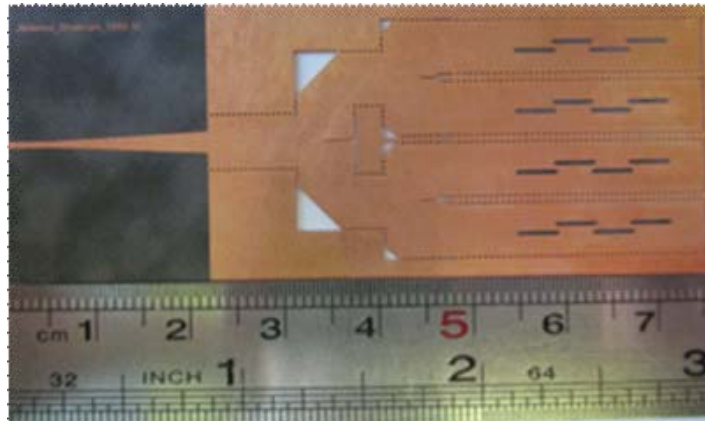


Figure 4.4: Photograph of the fabricated 4×4 SIW antenna array.

4.1.1 Fabrication and measurement results

Low-cost PCB process is used to fabricate the antenna prototype on a 10 mils Rogers/Duroid 5880 substrate with dimension of 70 mm×30 mm. Figure 4.4 shows the photograph of the fabricated 4×4 antenna array. Figure 4.5 shows the simulated and measured $|S_{11}|$ of the antenna array. The measured bandwidth of the antenna array covers the desired frequency range (23.6-24.6 GHz). Figure 4.6 compares the simulated and measured radiation pattern of the antenna array.

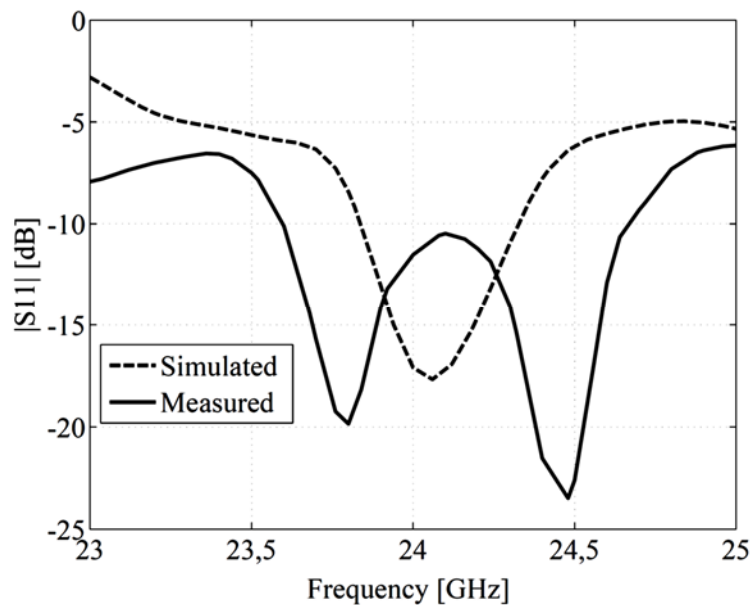
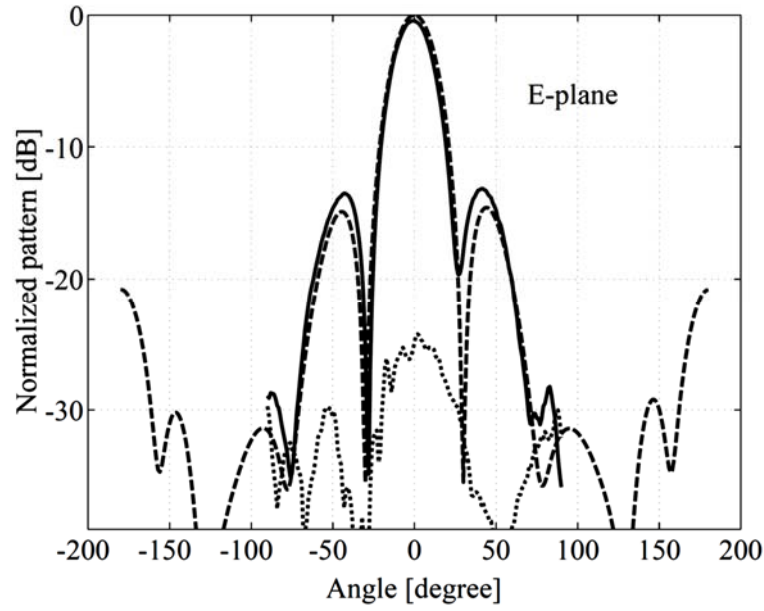
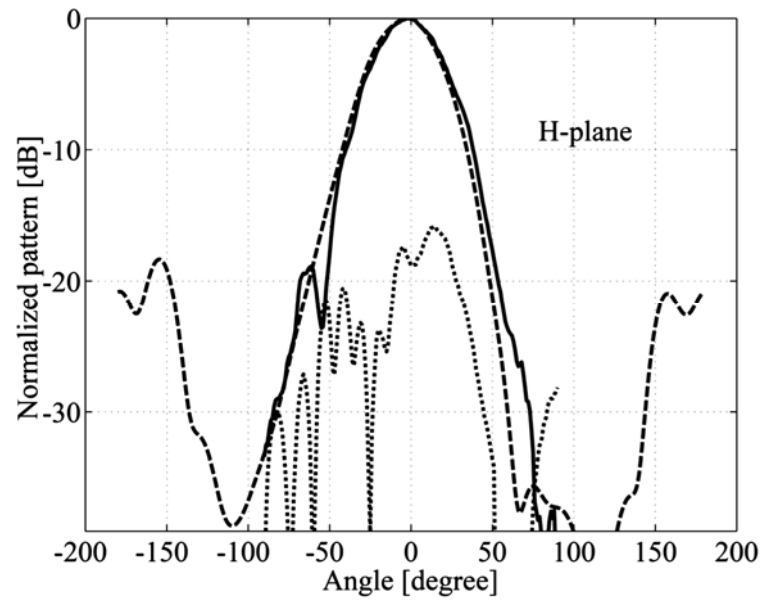


Figure 4.5: Measured and simulated impedances of the 4×4 array of SIW antenna



(a)



(b)

Figure 4.6: Simulated and measured radiation pattern in (a) E plane (YZ plane), and (b) H plane (XZ plane), of the 4×4 antenna array at 24 GHz, Solid: measured, dashed: simulated, and dotted: measured cross-polarization.

Good agreement is obtained between the simulated and measured radiation patterns. Note that effect of the dielectric and the metallic losses, roughness and thickness of the metallic layer have been considered in the simulation of the antenna. The simulated and measured side lobe levels of the 4×4 antenna array are less than 15 dB in both E- and H-planes at 24 GHz. The E-plane measured cross polarization of the antenna array is less than 25 dB (Figure 4.6).

4.2 24 GHz LP rectenna design for energy harvesting and wireless power transmission

To make a LP rectenna, the designed SIW antenna array is connected to the voltage doubler rectifier presented in section 3.2.1. The SIW antenna array is connected to the microstrip rectifier using an SIW to microstrip transition. The designed rectenna is fabricated on the same substrate as antenna (10 mil thickness Rogers 5880) and shown in Figure 4.7.

The measurement setup for measuring the rectenna performance is shown in Figure 4.8. In the transmitter side, 24 GHz RF signal is generated by Anritsu MG3694A signal generator. The generated signal is amplified using an amplifier and transmitted through a linearly polarized K-band horn antenna to power the rectenna array. The received power to the rectenna is calculated by determining the path loss of the system using below equation

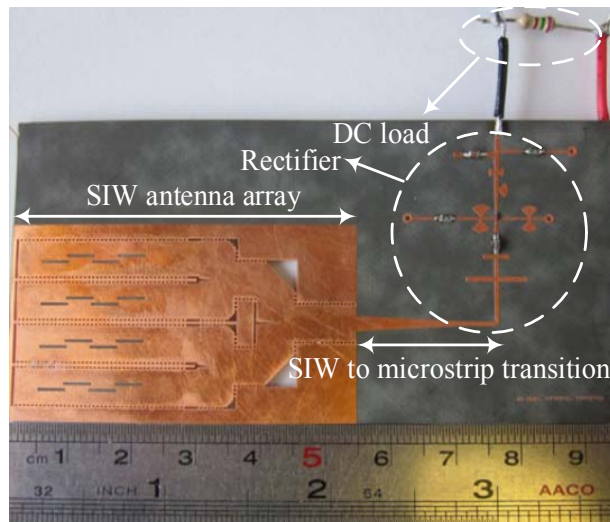


Figure 4.7: Fabricated circuit of the 24 GHz linearly polarized SIW rectenna.

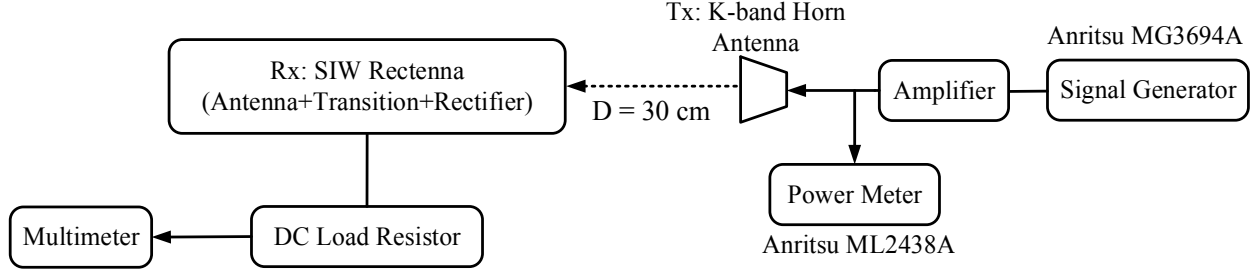


Figure 4.8: Rectenna receiver power measurement setup.

$$Path Loss = -20 \log \frac{4\pi D}{\lambda} \quad (4.1)$$

$$P_{received} (dB) = P_{S.G} + G_{T.A} + Path Loss + G_{R.A} \quad (4.2)$$

Where D is the distance between the transmitter and the receiver, which is 30 cm and is equal to $24 \times \lambda$ at 24 GHz. Using (4.1) the path loss of the system is -49.5 dB. $P_{S.G}$ is the power generated by the signal generator (the maximum achieved power at 24 GHz is 8 dBm) and is amplified by the amplifier (the gain of the amplifier is 8 dB at 24 GHz). $G_{T.A}$ is the transmitter antenna gain (20 dB for the standard horn antenna used in this measurement) and $G_{R.A}$ is the receiver antenna gain (15 dB for the designed SIW array). The maximum generated power at 24 GHz measured at the output of the amplifier is 16 dBm. When all these values are put in (4.2), the injected power to the rectifier is obtained which is 1.5 dBm or 1.4 mW. The measured output DC voltage at the output of the rectenna is 0.37 V. Since the DC load resistor is known (670 Ω for this design since the maximum RF-to-DC conversion efficiency of the rectifier has been reported for this value of the DC load). Then the RF-to-DC conversion efficiency of the rectenna system is obtained using (4.1) and (4.2) which is 14.6% for 1.4 mW RF input power.

4.3 Design of a 24 GHz circular polarization antenna array

In addition to the desirable factors mentioned for the choice of antennas used in WPT systems, these antennas should feature light-weight and portability. Therefore, it can be claimed that microstrip patch antennas present prime candidates due to their attractive advantages such as low profile, light weight and low cost. They can also be realized using both planar and non-planar architectures with various configurations of array depending on particular shape and mode requirements.

4.3.1 Microstrip patch circular polarization antenna array

According to the required specification mentioned before for a proper antenna for WPT applications, a metallic circular patch is chosen to implement the fully planar CP antenna array. A single antenna with microstrip feeding transmission line is characterized first and then used to form an antenna array. The geometry along with parameters of the designed CP patch array is shown in Figure 4.9. Standard low-cost PCB process is used to fabricate the antenna prototype on a 20 mils Rogers/Duroid 5880 substrate with $\epsilon_r = 2.2$. The antenna prototype occupies the total size of $30 \text{ mm} \times 30 \text{ mm}$.

In the proposed array, a circularly polarized characteristic is constructed with two sets of microstrip patches. In each set, two elements are positioned with an angular orientation of 90° to each other and fed with 90° phase difference using an unequal length power divider. The optimum antenna parameters are calculated using the Ansoft simulation software (HFSS). The designed array provides the left-handed CP while the right-handed CP is obtained by mirroring the structure along the X axis. Simulated and measured impedance matching characteristics (return loss) as a function of frequency are compared in Figure 4.10. Antenna impedance (with $|S_{11}| \leq -10 \text{ dB}$) is matched from 24.2 GHz to 25.8 GHz. The deviation of the measurement from the simulation is explained by the effect of the connector soldered on the 50Ω microstrip feed-lines shown in Figure 4.9 (b). The CP array far-field radiation pattern is measured inside a MI technology anechoic chamber.

Antenna radiation pattern in the XZ and YZ planes is separately measured, while transmitting a linearly polarized signal from the transmitting horn antenna. The simulated and measured normalized radiation patterns in the XZ and YZ planes are compared in Figure 4. 11. (a) and (b). The measured CP array gain is 10.3 dBc at 24.8 GHz. The simulated and measured axial ratios (AR) are compared in Figure 4.12. The measured AR value is less than 3 dB from 23.9 GHz to 25 GHz and the minimum of 0.5 dB at 24.3 GHz. Good agreement is obtained between the simulated and measured radiation patterns. Note that the effects of dielectric and metallic losses and thickness of the metallic layer are considered in the simulation of the antenna array. The antenna array has the advantages of compact size, left-hand circularly polarized (LHCP) characteristics and single layer with single feed-line.

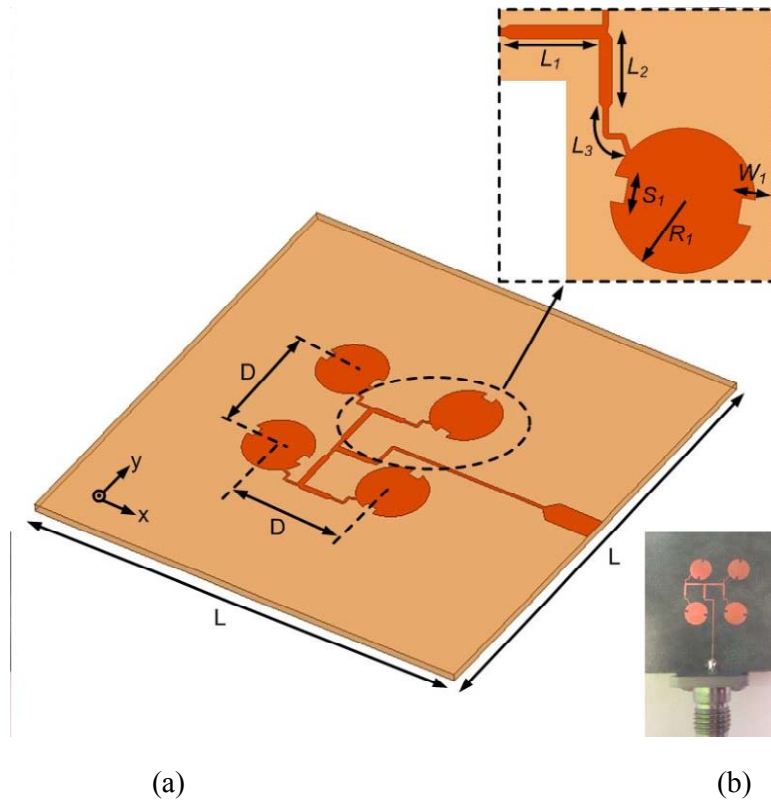


Figure 4.9: (a) CP patch array antenna configuration. (b) Photograph of the fabricated prototype. Geometry parameters are following: $R_1 = 2.2$, $S_1 = 0.65$, $W_1 = 0.45$, $L_1 = 2.45$, $L_2 = 2.35$, $L_3 = 1.75$, $D = 8$, $L = 30$ (dimensions in millimeters).

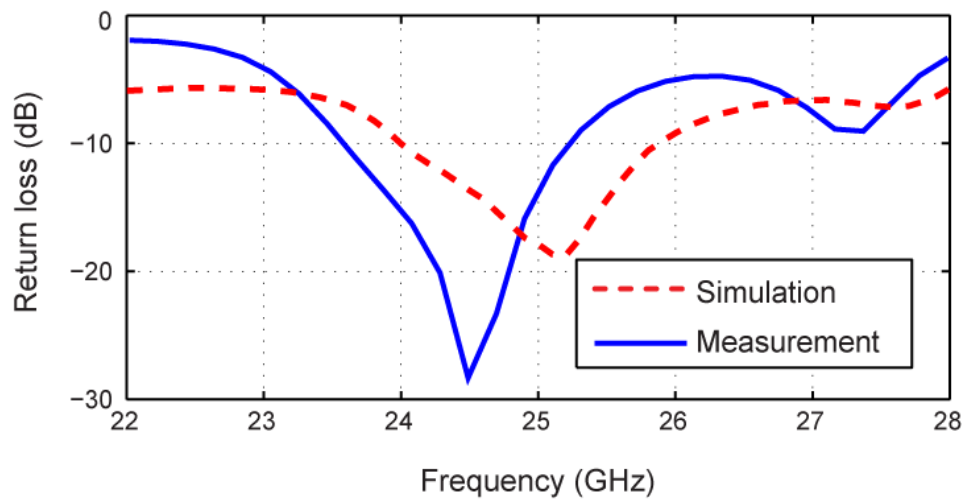
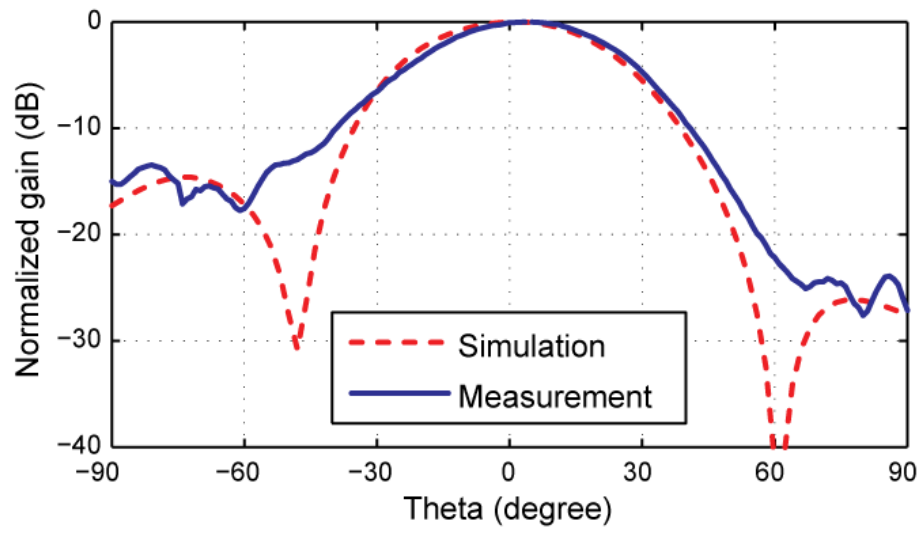
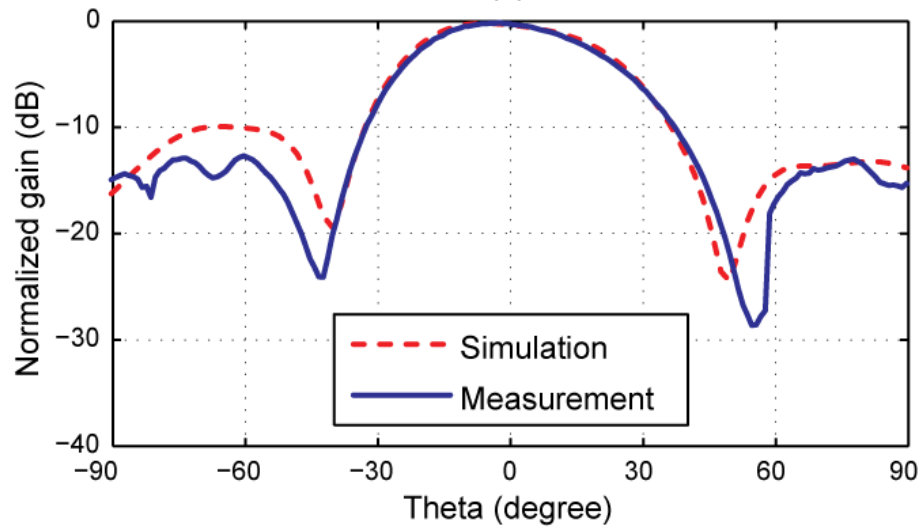


Figure 4.10: Simulation and measurement results of the CP array impedance matching from 22 GHz to 28 GHz.



(a)



(b)

Figure 4.11: Simulation and measurement results of normalized gain pattern of the CP array. (a) XZ plane, (b) YZ plane.

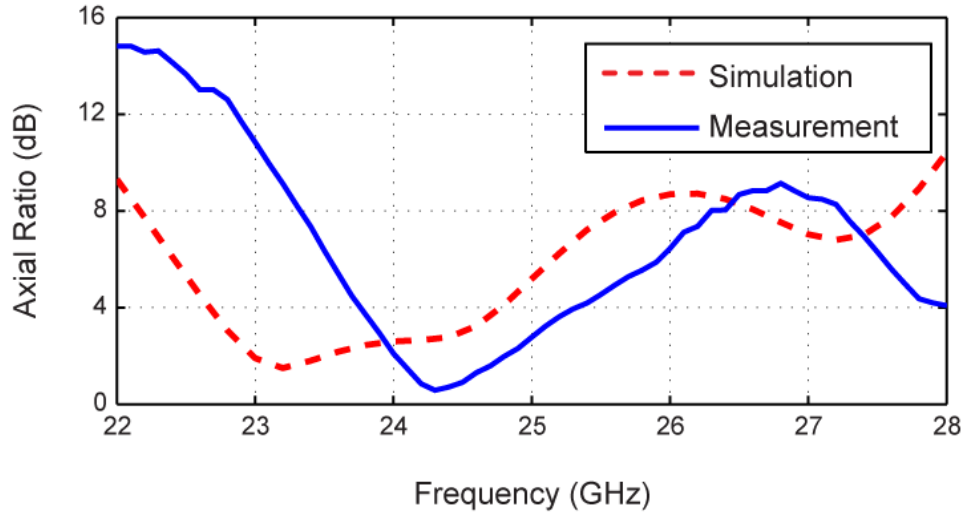
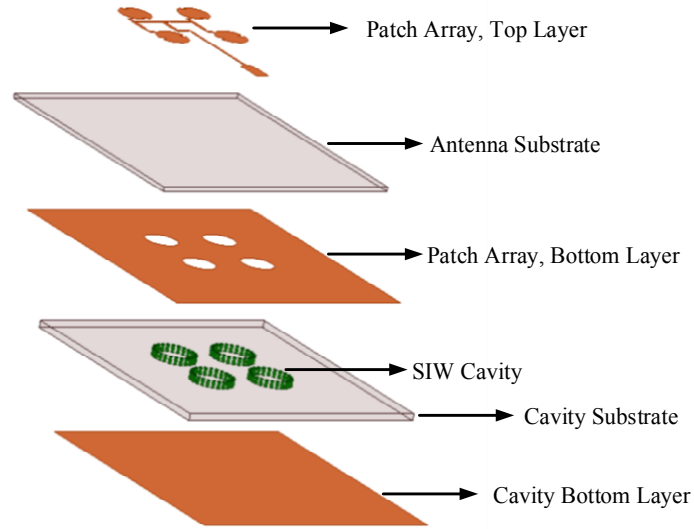


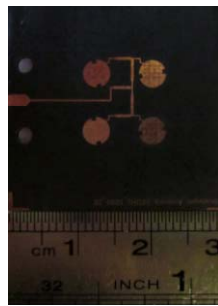
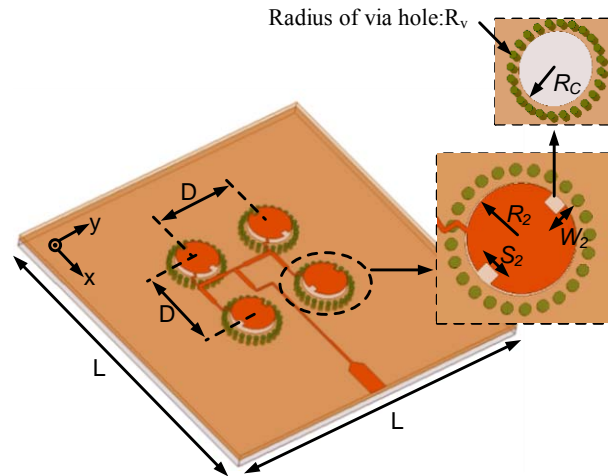
Figure 4.12: Simulation and measurement results of the CP array impedance matching from 22 GHz to 28 GHz.

4.3.2 Circular polarization microstrip antenna array with metallic-cavity backing

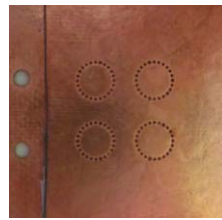
The above-developed planar array shows excellent radiation characteristics, but its impedance and axial ratio bandwidth is narrow. Substrate thickness can be increased to enhance the bandwidth further. However, a major drawback of this technique is degrading the efficiency of the antenna caused by undesired surface wave excitation [85]. Another solution is to add an air cavity beneath the antenna element to suppress surface waves. Therefore, the circular cavity surrounded with metallic vias can reduce mutual coupling between antenna elements and also increase the bandwidth. Normally, SIW cavity-backed patch antennas have superior performance since they can significantly suppress surface waves, reduce coupling and provide better matching and wider scan performances in an array configuration [86]- [88]. The design of this type of antenna needs careful attention to select a proper substrate with appropriate thickness and dielectric constant for the patches and the cavity. The final designed structure of 2×2 array with related dimensions and the fabricated prototype are shown in Figure 4.13.



(a)



(b)



(c)

Figure 4.13: (a) 3D model of the SIW cavity-backed CP array. (b) Front-side of the fabricated prototype. (c) Back-side of the fabricated prototype. Geometry parameters are following: $R_2 = 1.85$, $S_2 = 0.9$, $W_2 = 0.6$, $R_c = 1.9$, $R_v = 0.2$ (dimensions in millimeters).

The antenna prototype consists of two layers. The bottom layer is in support of the SIW cavity and the top layer is related to the antenna design. As mentioned before, in order to minimize the surface wave losses and increase the antenna radiation efficiency, the CP array is designed on a low loss dielectric constant substrate with a relatively thin thickness. According to [86], a proper substrate for the cavity should not have high dielectric constant because this may trap the energy and increase the quality factor of the antenna, which results in decreasing the bandwidth and degrading the radiation efficiency. In addition, the thickness of substrate used in the design of the cavity can be relatively thick to improve the bandwidth. Nevertheless, a very thick substrate is not recommended in order to maintain a light-weight and low-profile structure. Also, using the same material for both patch and cavity substrates preserves the thermal expansion matching between the patch and cavity layers [90]. Therefore, 30 mil thick Rogers 5880 substrate is chosen for the cavity design. To emulate the cavity wall, 24 via holes with radius of 0.2 mm are placed along a circular opening (with radius R_c) and added in the cavity substrate. The designed SIW cavity is added to the above-designed CP patch array to realize an SIW cavity-backed patch array antenna. The fabricated prototype of the antenna array is shown in Figure 4.13 (b) and (c). The HFSS gain optimization is based on cavity radius R_c , patch radius R_2 , width S_2 , and depth W_2 of the perturbation segments. Figure 4.14 compares simulated and measured impedance matching performances of the SIW cavity-backed antenna as a function of frequency. Good agreement is observed from 23 GHz to 26 GHz with $|S_{11}| \leq -10$ dB.

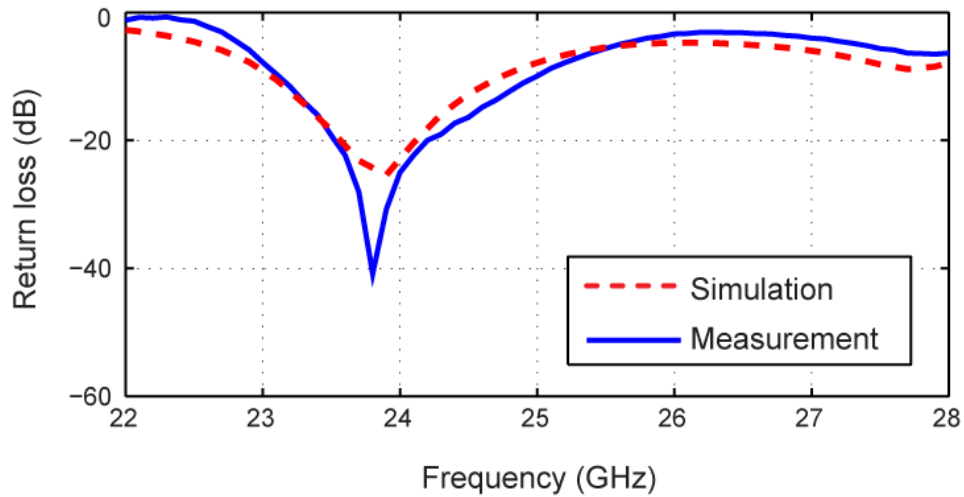


Figure 4.14: Simulation and measurement results of the SIW cavity-backed CP array impedance matching from 22 GHz to 28 GHz.

The far-field measurements of antenna radiation pattern in the XZ -plane and YZ -plane are shown in Figure 4.15 (a) and (b). Simulated and measured axial ratios are compared in Figure 4.16. Measured axial ratios of planar and cavity-backed array are compared in Figure 4.17. Measured 4 GHz (from 22.2 GHz to 26.2 GHz) bandwidth of axial ratio (≤ 3 dB) is obtained for the designed antenna array. The measured CP gain of 12.6 dBi is achieved at 24 GHz. It can be concluded that the SIW cavity-backed structure improves the bandwidth of antenna and shows a superior performance in terms of axial ratio and gain. Therefore, the SIW cavity-backed patch array is selected and used to integrate with the rectifier for WPT at 24 GHz frequency range.

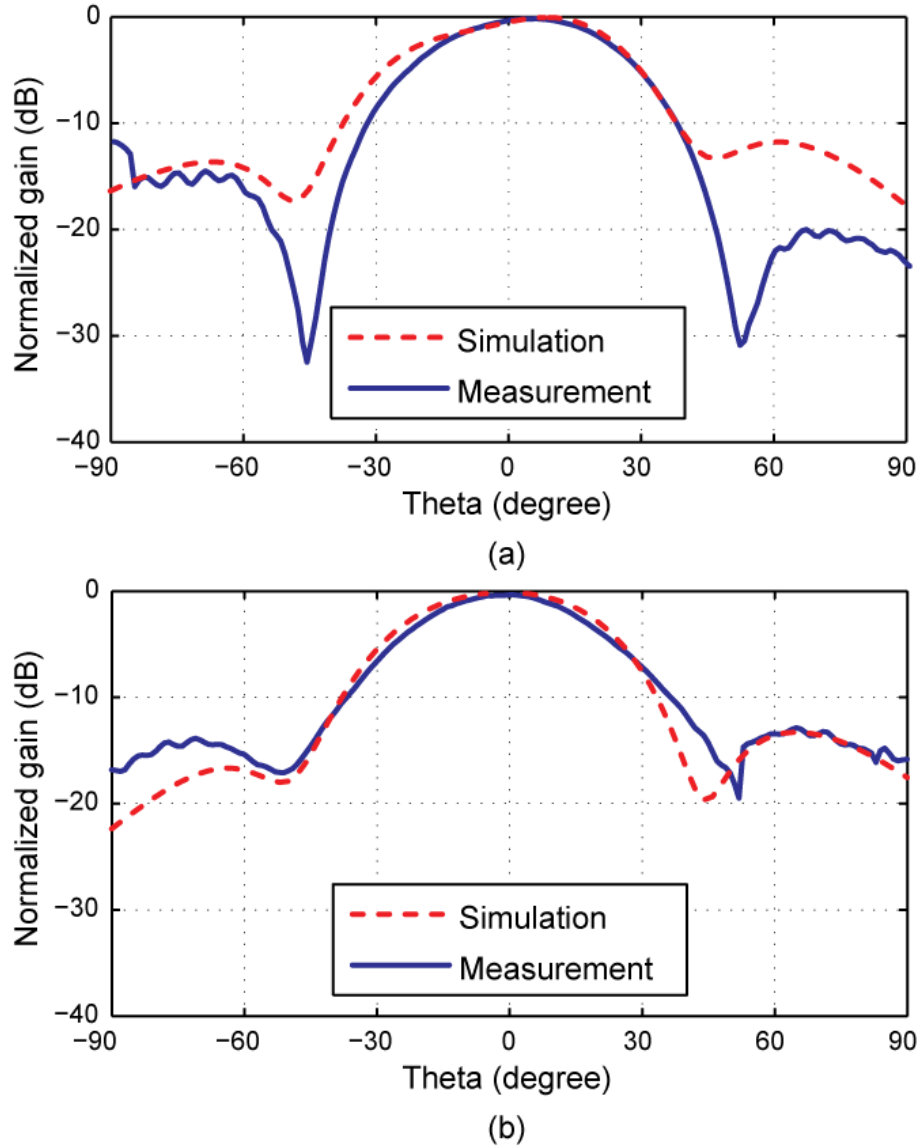


Figure 4.15: Simulation and measurement results of the normalized gain pattern of the SIW cavity-backed CP array. (a) XZ plane, (b) YZ plane.

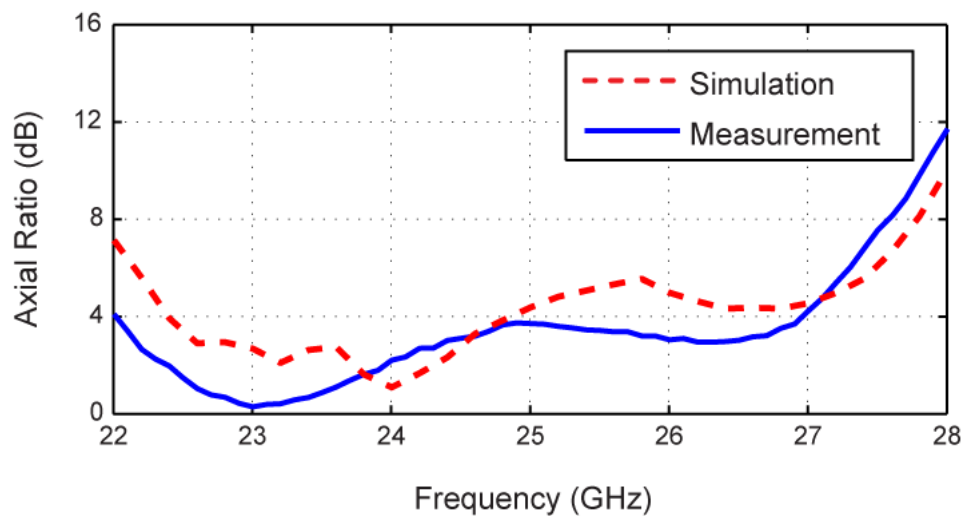


Figure 4.16: Simulation and measurement axial ratios of the SIW cavity-backed CP array.

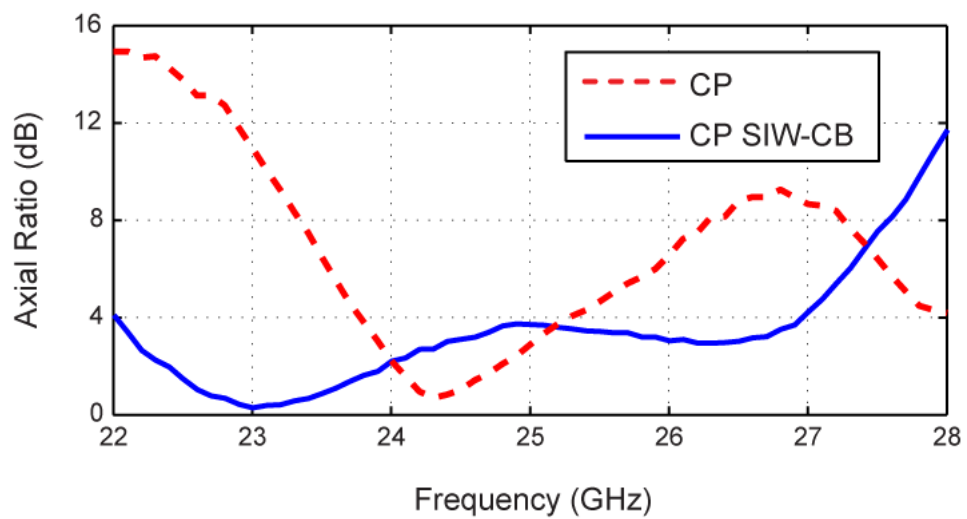


Figure 4.17: Comparison between measured axial ratio of the CP array and the SIW cavity-backed CP array.

4.4 Design of a 24 GHz circular polarization rectenna for energy harvesting and wireless power transmission

Previously, it was shown that the designed SIW cavity-backed CP array presents a superior performance in terms of gain and axial ratio compared to the CP array without cavity backing. Therefore, this antenna array of choice is connected to the improved structure of the self-biased rectifier (discussed in 3.2.1) in order to realize an integrated rectenna. The fabricated prototype and the measurement setup are shown in Figure 4.18 and Figure 4.19, respectively. A standard horn antenna of 20 dBi gain with dimension (D) of 7 cm is used to transmit the RF power at 24 GHz. A 30 dB gain amplifier, Hewlett Packard 8348A, amplifies the power generated by the signal generator Anritsu ML68177. The DC output voltage and the RF-to-DC conversion efficiency are measured as a function of power density derived from the Friis transmission equation [90]. The power density is calculated by

$$P_D = \frac{P_t G_t}{4\pi R^2} \quad (4.3)$$

where P_t is the transmitted power, G_t is the transmitter's antenna gain and R is the distance from the transmitter to the rectenna. In this measurement, R is set to be 1 meter which satisfies the far-field condition at 24 GHz ($R \geq (2D^2 / \lambda) = 78$ cm where D is the largest dimension of the aperture of the antenna and λ is the free-space wavelength at the operating frequency). The transmitter antenna and the receiver rectenna have polarization mismatch represented by the polarization loss factor (PLF). The PLF between the linearly polarized transmitter horn antenna (ρ_t) and the SIW cavity-backed CP antenna (ρ_r) is determined by

$$PLF = |\rho_t \cdot \rho_r|^2 = \left| \hat{a}_x \cdot \frac{1}{\sqrt{2}} (\hat{a}_x - j \hat{a}_y) \right|^2 = \frac{1}{2} \quad (4.4)$$

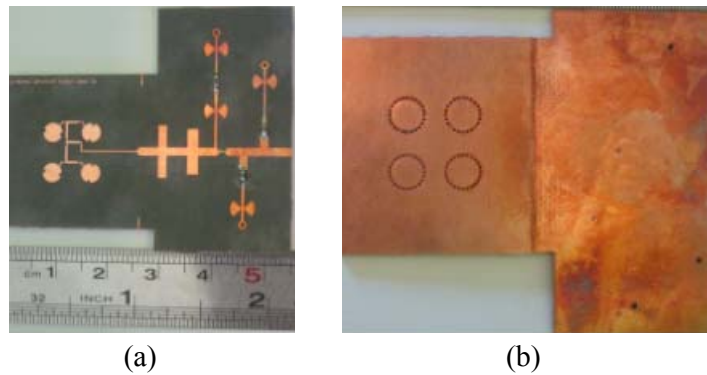


Figure 4.18: (a) Front-side of the fabricated rectenna. (b) back-side of the fabricated rectenna.

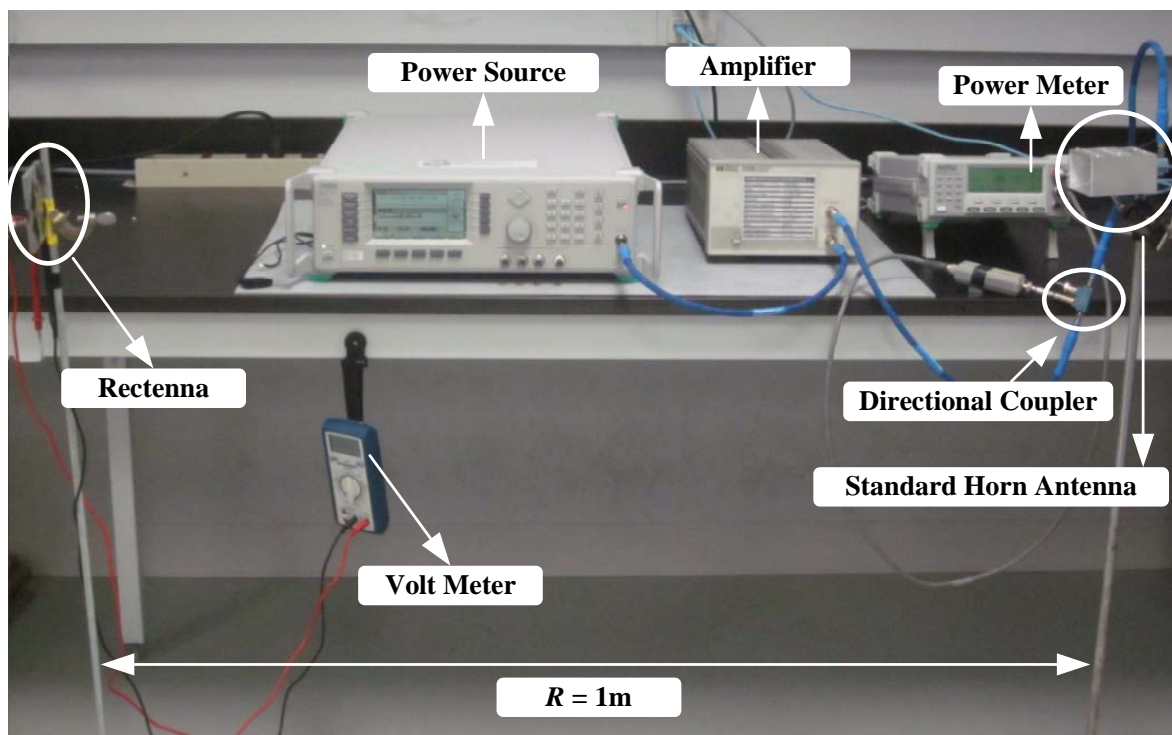
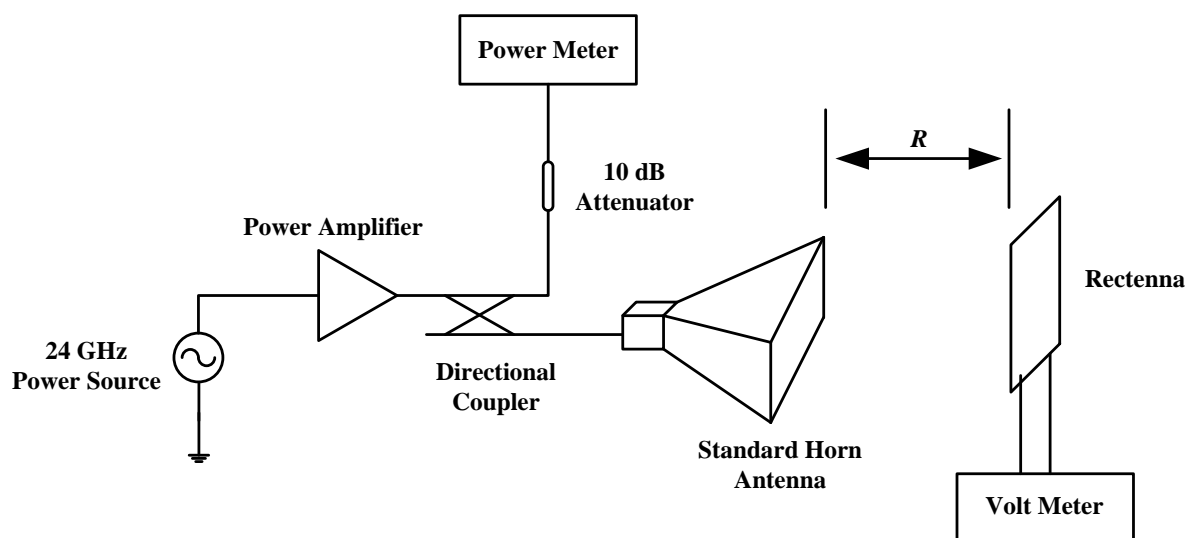


Figure 4.19: Rectenna measurement setup.

The CP rectenna receives only half of the transmitted power because of the polarization mismatch. The transmitted RF power is swept from 1 dBm to 14 dBm and the corresponding DC voltage is measured at the output of the rectifier for different value of power density. The measured DC voltage and efficiency of the rectenna is shown in Figure 4.20. For example, considering (4.3), the obtained power density for 9 dBm RF input power at distance of 1m from the transmitter is 6.31 mW/cm^2 which only a half of it (3.15 mW/cm^2) is considered as the power density at the receiver side taking into account the 3 dB polarization mismatching. The measured DC voltage at the output of the rectenna at this level of power density (3.15 mW/cm^2) is 0.25V while the RF-to-DC conversion efficiency is 15%. The maximum conversion efficiency of 24% is achieved at an incident radiation power density of 10 mW/cm^2 which is the highest recorded voltage obtained at this level of power density compared to previous similar works. Consequently, the designed rectenna presents a significant enhancement in the design of a high efficiency WPT rectenna at high frequencies towards millimeter-wave applications as compared with the state-of-the-art results.

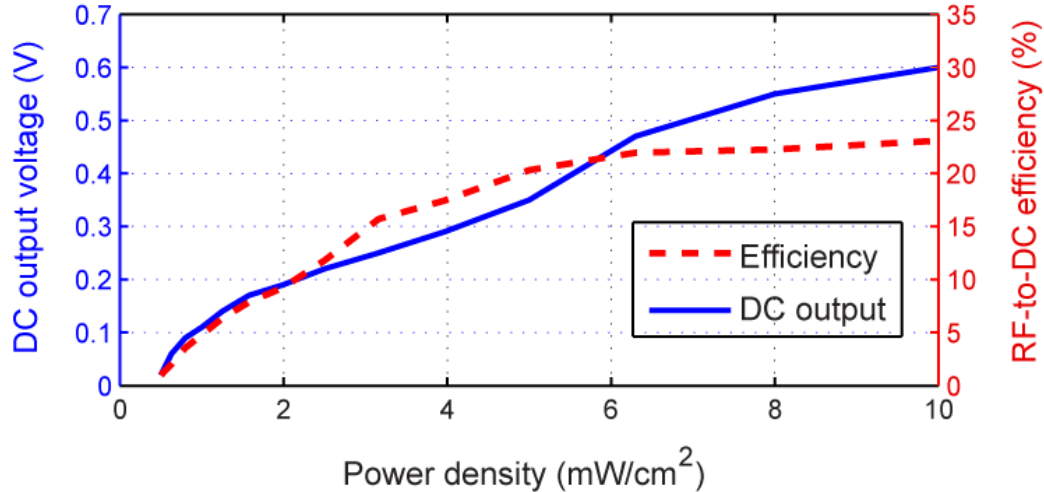


Figure 4.20: Measured DC output voltage and efficiency versus incident power density of the rectenna at distance of 1 m at 24 GHz.

4.5 Conclusion

Required specification for antennas used in WPT systems has been studied in this chapter. Two different antenna configurations; an SIW slot array antenna with LP polarization and a microstrip patch array with CP polarization were designed. The proposed antennas structures were simulated using full-wave software Ansoft HFSS. High gain characteristic was verified by measurement. Consequently, the designed antennas were integrated to the rectifier circuits studied in chapter 2 to perform as a rectenna working at up-microwave. The 24 GHz LP rectenna provided 40% RF-to-DC conversion efficiency at 35 mW input power experimentally while the maximum efficiency of 24% at power density of 10 mW/cm² at 24 GHz was measured from the CP rectenna. The measured efficiency is the maximum reported to date for this level of power density.

CHAPTER 5 SIMULTANEOUS ENERGY HARVESTING AND DATA COMMUNICATION USING SIX-PORT RECEIVER

Microwave power transmission technology has been subject to intensive development in both theoretical and application aspects such as wireless energy harvesting (WEH) and space solar power system (SSPS). Recently, wireless power transmission has become a potential alternative in generating clean energy. With the trend of communication systems consuming lower power and lower voltage, many researchers have been exploring the feasibility of powering these devices through harvesting ambient electromagnetic energy. For this purpose, self-powering systems present special topic of interest. On the other hand, data transmission is omnipresent thanks to the rapid development of wireless communication systems. Consequently, a platform in support of simultaneous energy harvesting and data communication is promising for the next generation of self-powered communication systems (Figure 5.1).

Currently, the power harvesting circuits (rectenna circuits) are not able to decode the transmitted signal and the output of the rectifier may not be used for data detection directly. In order to realize the function of simultaneous energy harvesting and data communication, the most straightforward and simpler manner is to split the received RF signal into two streams which can be used for data detection and energy harvesting (Figure 5.2). As it can be seen, two different approaches may be considered.

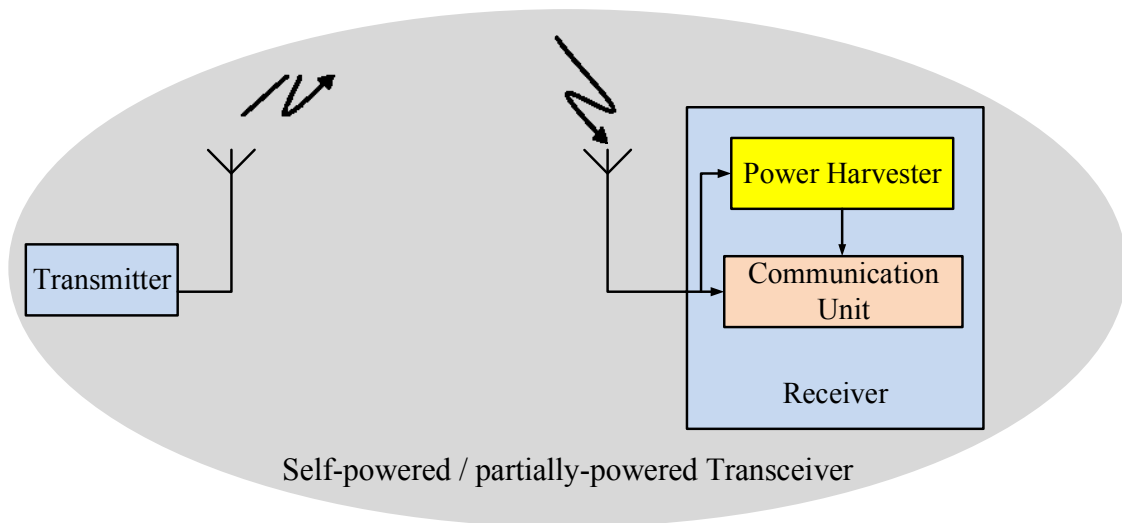


Figure 5.1: General schematic of a self-powered transceiver.

First, we can put a power splitter right after the antenna and send one stream to the energy harvesting circuit (rectifier circuit) and send the other portion to the data detection (demodulation) circuit (Figure 5.2-a). The second approach is to employ a rectifier right after the antenna to convert the entire RF signal to DC plus baseband signals and then use a splitter to accommodate the energy harvesting and information detection circuits (Figure 5.2-b).

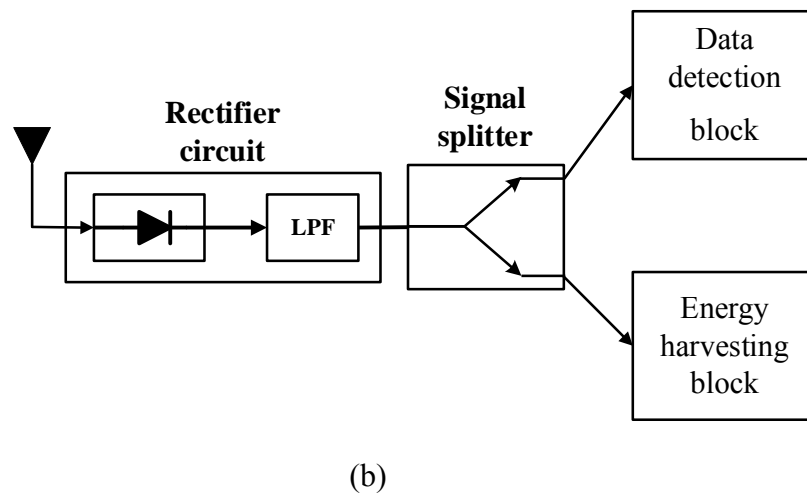
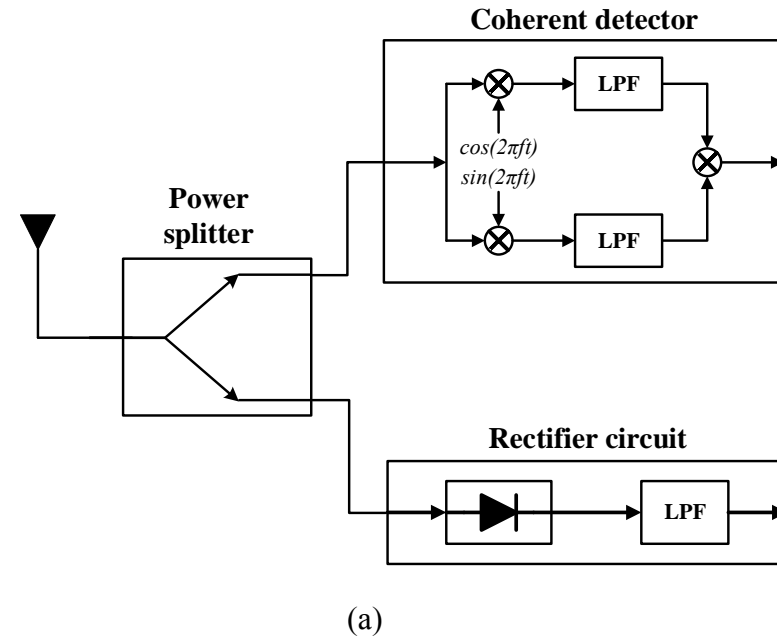


Figure 5.2: Block diagram of a self-powered transceiver.

In order to study the above-mentioned approaches, we analyze the performance of these circuits in terms of noise level and power consumption. Noise level analysis is one of the critical aspects of performance evaluation which can help us to assess the effect of various signal splitting approaches. On the other hand, for energy harvesting systems, power consumption is a vital metric that has to be taken in to consideration, due to the fact that decreasing the power consumption of such systems leads to higher overall power harvesting efficiency. As seen in Figure 5.2 (a), we can consider a coherent demodulation for data detection and ideal signal splitter (without any noise production). There are two noise sources including the thermal noise ($n_T(t)$) and the RF band to baseband conversion noise ($n_{Mix}(t)$) (i.e. mixer noise for RF to IF conversion and quantization noise in analog to digital convertors). Splitting the received signal (transmitted signal plus thermal noise) before the data detection circuit affect the SNR at the output of the coherent demodulator as follow:

$$SNR_{Coherent} = \frac{(1 - \alpha) P_s}{(1 - \alpha) \sigma_{n_T}^2 + \sigma_{n_{Mix}}^2} \quad (5.1)$$

where α is the splitting signal ratio and P_s , $\sigma_{n_T}^2$ and $\sigma_{n_{Mix}}^2$ denote the average transmit power, thermal noise variance and mixing noise variance, respectively. Hence, splitting the received signal would decrease the signal to noise ratio after the coherent demodulator, which may affect the overall performance of the receiver. In addition, the power consumption of the coherent demodulator is a critical design issue (due to the active mixer) for simultaneous energy harvesting and data communication. On the other hand, as seen in Figure 5.2 (b), the received RF signal is first converted to DC signal then gets split into two streams. To this end, besides the thermal noise, we have a noise source from the rectification process ($n_{Rec}(t)$) and the analog to digital converted signal of the rectifier circuit output (rectified signal plus thermal noise and rectifier noise) can be written as

$$\hat{y}(m) = \left(\left| \sqrt{2P_s} A(t) + n_T(t) \right|^2 + n_{Rec}(t) \right) \Big|_{t=m} \quad (5.2)$$

where $A(t)$ is the amplitude of transmitted signal ($s(t) = A(t)e^{j\varphi(t)}$). Therefore, the signal splitter does not affect the signal to noise ratio at the input of data detection block, due to the fact that both received signal and noise terms are multiplied by splitting signal ratio, $(1 - \alpha) \hat{y}(m)$.

Moreover, the power consumption of the circuit in the second design is limited to the power consumed by analog to digital converter which is common to the first design. Consequently, we can see that employing a rectifier circuit to convert the received RF signal to the DC and baseband signals and a splitter to provide the required power for data detection and energy harvesting, presents a promising approach for simultaneous energy harvesting and data communication with lower power consumption and higher signal to noise ratio. Furthermore, it is worth noting that in the use of signal splitters for energy harvesting purposes, we have to consider the minimum required input power at the input of the detector circuit. In the other word, we need to adjust the splitting factor in such a way that the injected signal can driver the data communication circuit (for instance analog to digital convertor circuit).

As mentioned in the introduction, simple structure, low-power consumption, compact-sized, low-cost and wideband transceivers are critical in the development of wireless communication systems. To achieve these desirable specifications and to eliminate the rectification noise in the second approach, we can take advantage of the multiport techniques to convert the received RF power to the DC plus baseband signal. Moreover, it is worth noting that the multiport techniques has drawn significant attention in designing transceivers due to the proven ability to provide simpler circuits in comparison with heterodyne transceivers [92]. Therefore, in the sequel, six-port technique, its applications and the proposed simultaneous energy harvesting and data communication are discussed in detail.

5.1.1 Six-port junction analysis

A six-port junction is a passive component which mainly consists of several couplers and power dividers. They can be made based on various design techniques, such as microstrip line, SIW and CPW. Three common configurations of six-port junction have been proposed and widely used in different designs. These configurations (shown in Figure 5.3) are made using:

Model A: Three hybrid couplers plus one equal power divider [29]

Model B: Four hybrid couplers plus one 90° phase shifter [92]

Model C: Two hybrid couplers plus two equal power dividers and one 90° phase shifter [93]

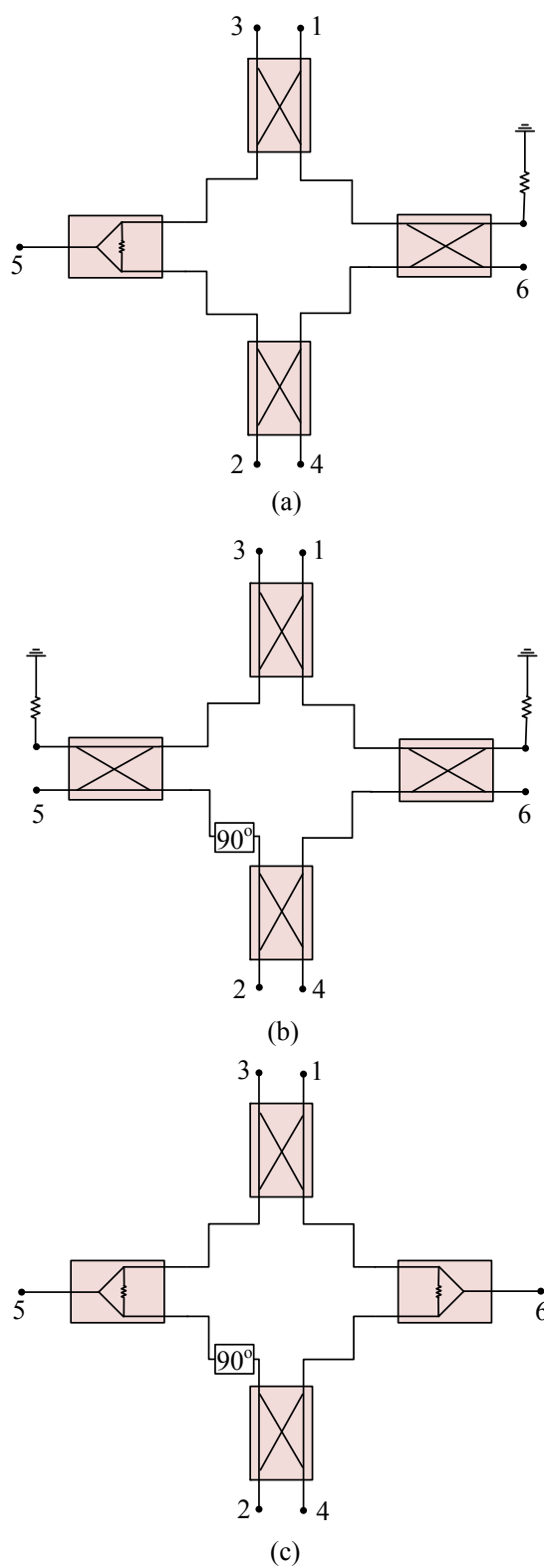


Figure 5.3: Three common configurations of a six-port junction.

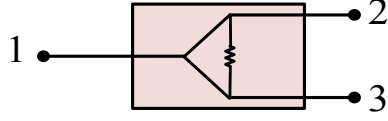


Figure 5.4: Structure of an ideal Wilkinson power divider.

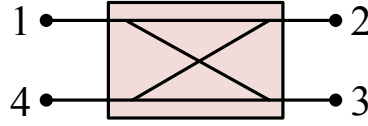


Figure 5.5: Structure of an ideal 90° hybrid coupler.

To obtain the S-parameters of each configuration, the S-parameters of the ideal Wilkinson power divider and the ideal 90° hybrid coupler are considered below

$$S_{Wilkinson} = -\frac{1}{\sqrt{2}} \begin{pmatrix} 0 & j & j \\ j & 0 & 0 \\ j & 0 & 0 \end{pmatrix} \quad (5.3)$$

$$S_{Coupler} = -\frac{1}{\sqrt{2}} \begin{pmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{pmatrix} \quad (5.4)$$

Using some straightforward calculations the S-parameters of each employed configuration A, B or C (Figure 5.3) are obtained as follows

$$S_A = \frac{1}{2} \begin{bmatrix} 0 & 0 & 0 & 0 & j & j \\ 0 & 0 & 0 & 0 & -1 & j \\ 0 & 0 & 0 & 0 & -1 & 1 \\ 0 & 0 & 0 & 0 & j & -1 \\ j & -1 & -1 & j & 0 & 0 \\ j & j & 1 & -1 & 0 & 0 \end{bmatrix} \quad (5.5)$$

$$S_B = \frac{1}{2} \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & j \\ 0 & 0 & 0 & 0 & -j & j \\ 0 & 0 & 0 & 0 & j & 1 \\ 0 & 0 & 0 & 0 & -1 & -1 \\ 1 & -j & j & -1 & 0 & 0 \\ j & j & 1 & -1 & 0 & 0 \end{bmatrix} \quad (5.6)$$

$$S_C = \frac{1}{2} \begin{bmatrix} 0 & 0 & 0 & 0 & j & -1 \\ 0 & 0 & 0 & 0 & -j & j \\ 0 & 0 & 0 & 0 & -1 & j \\ 0 & 0 & 0 & 0 & -1 & -1 \\ j & -j & -1 & -1 & 0 & 0 \\ -1 & j & j & -1 & 0 & 0 \end{bmatrix} \quad (5.7)$$

Considering the relation between the incident waves and reflected waves with respect to the six-port correlator, one can employ the above-mentioned S-parameters to model the behavior of the ideal six-port junction as follows:

$$\mathbf{b} = \mathbf{S}\mathbf{a} \quad (5.8)$$

where \mathbf{a} and \mathbf{b} are incident and reflected wave vectors. The obtained results will be used to derive and analyze the functionality of a six-port receiver.

5.1.2 Design and fabrication of a 24 GHz six-port junction

Since the designed six-port junction will be used in a system for energy harvesting applications, a simple low-loss structure is needed. Model B is a good candidate since it is just made of hybrid couplers and phase shifter with no need of power dividers. However, the six-port junctions made of power divider and couplers can provide more bandwidth (the use of phase shifter generally limits the bandwidth). Then, a six-port circuit is designed at 24 GHz using microstrip technology based on model B. The designed circuit is fabricated by miniaturized hybrid microwave integrated circuit (MHMIC) technology on a 10-mil-thick ceramic substrate with relative permittivity of $\epsilon_r = 9.9$. The layout and fabricated prototype of the circuit with the size of $20\text{mm} \times 20\text{mm}$ are shown in Figure 5.6 and Figure 5.7, respectively. The six-port junction consists of four 90° hybrid couplers connected together using microstrip line of characteristic impedance $Z_0 = 50\Omega$. Two 50Ω loads (made by thin film technology) are used at the output of the unused ports to prevent any reflections. The required 90° phase shift is provided using an extra

three-quarter-wave transmission line. The circuit is designed and optimized using momentum simulator to operate at 24 GHz [99] and [100].

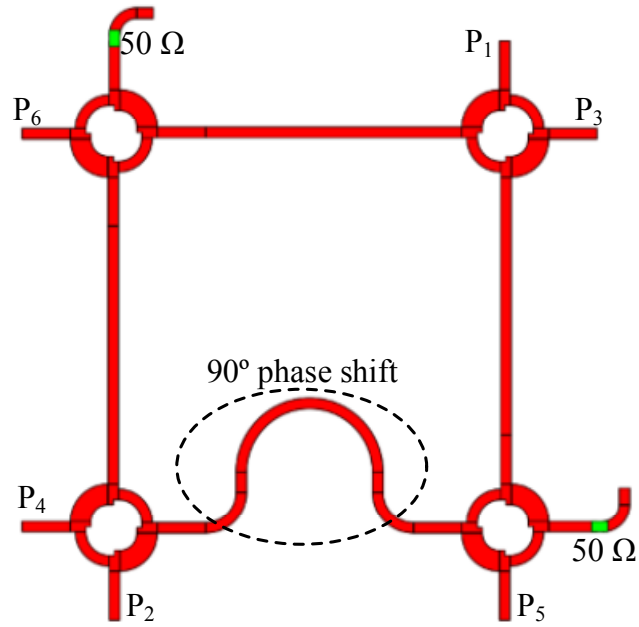


Figure 5.6: The layout of six-port junction.

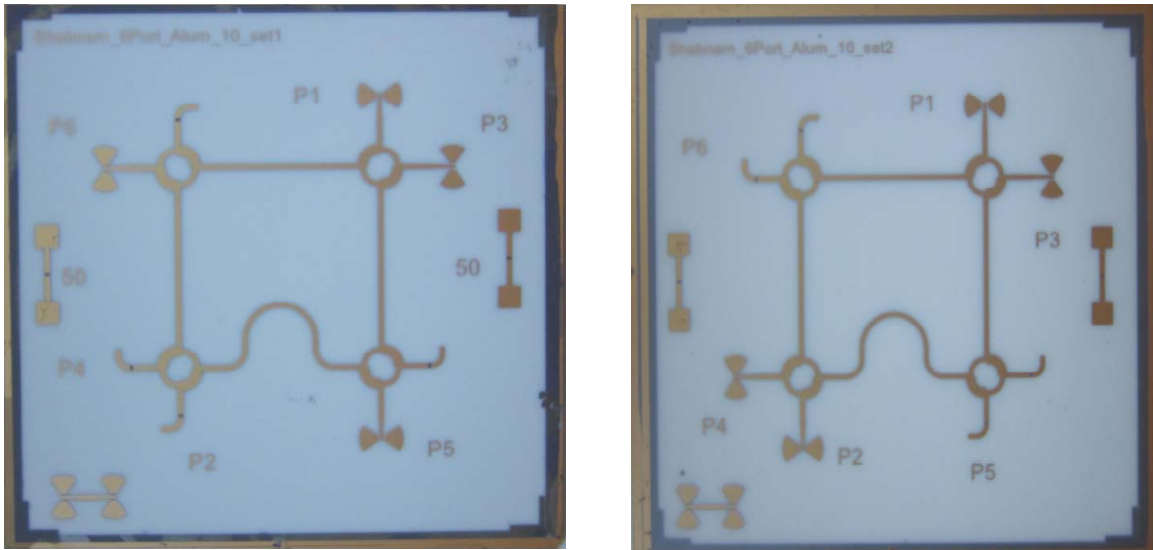


Figure 5.7: The fabricated prototype of six-port junction.

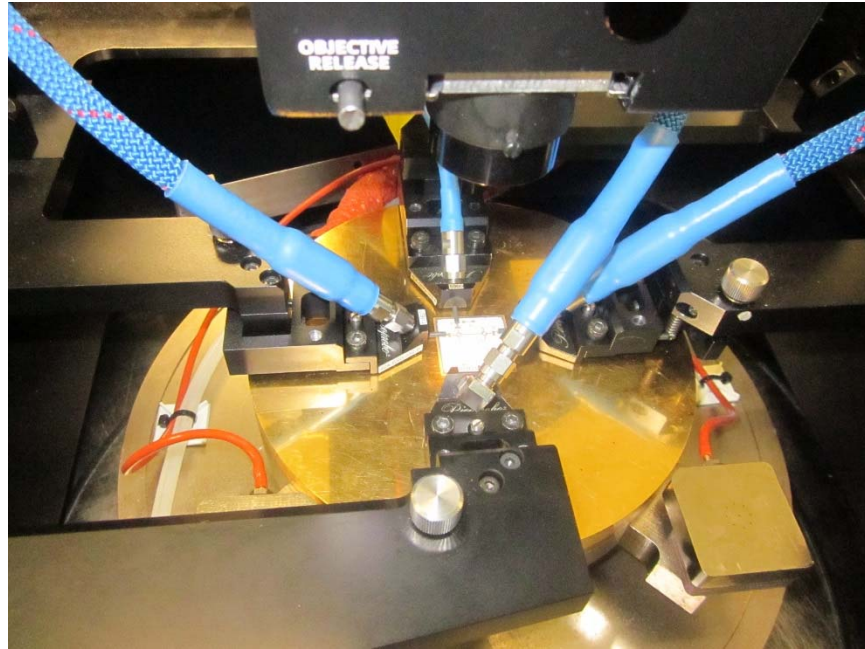
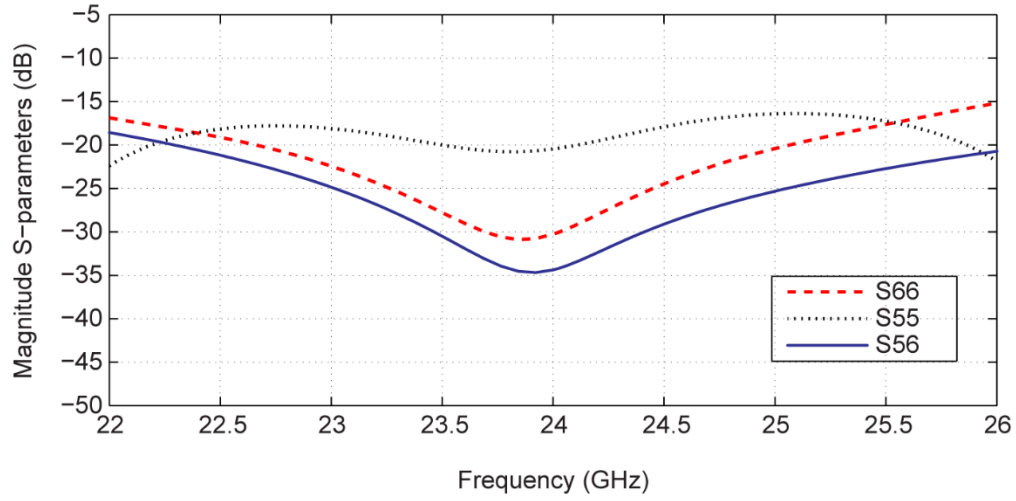


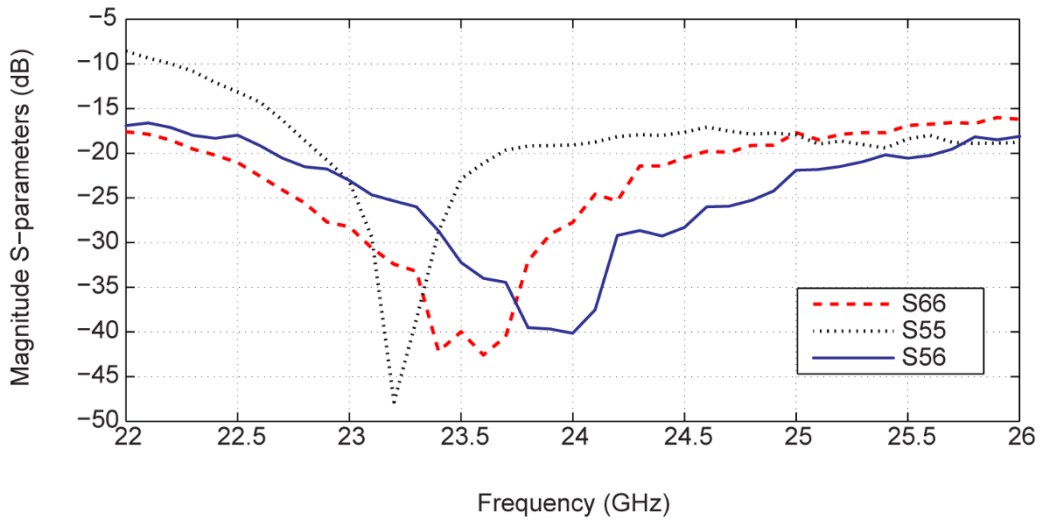
Figure 5.8: Four-port measurement setup.

The S-parameters are measured using a four-port vector network analyzer (VNA). With the four-port measurement setup (Figure 5.8), the S-parameters of four ports of the six-port are obtained at the same time while the two other ports matched to $50\ \Omega$. Since in a six-port junction, the number of ports to be measured is more than that of VNA ports (four-port VNA), two sets of six-port are fabricated in order to have the complete results of measured S-parameters. Also a CPW line is added to the ports (the ones which are going to be measured) to make them compatible with probing station. In the designed six-port, the LO power is injected from port 5 (P_5), while the RF signal comes from P_6 . The other four ports (P_1 to P_4) are considered as output ports. Measurement results are in good agreement with simulations. As shown in Figure 5.9, excellent return losses and isolation between RF and LO inputs are obtained at the 24 GHz operating frequency. Figure 5.10 shows the matching condition of the outputs in such a way that measured -15 dBm is obtained within a 4 GHz bandwidth. Figure 5.11 and Figure 5.12 present the transmission of RF and LO signals to the outputs. Compared to the ideal six-port model (shown in simulation, Figure 5.11 (a) and Figure 5.12 (a)), the measured transmission of RF and LO signals has an additional loss of 0.2 dB (-6.2 dB at 24 GHz) and also some ripples caused by calibration of VNA. Figure 5.13 and Figure 5.14 show the phase of transmission S-parameters between the input signals (RF and LO)

and outputs versus frequency. As it can be seen, the measured 90° phase shift is obtained among the output ports at 24 GHz.

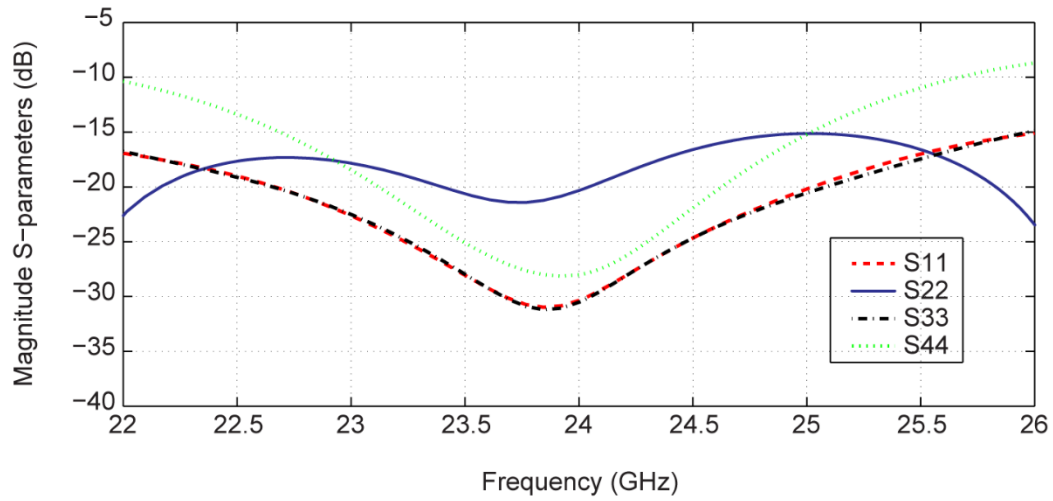


(a)

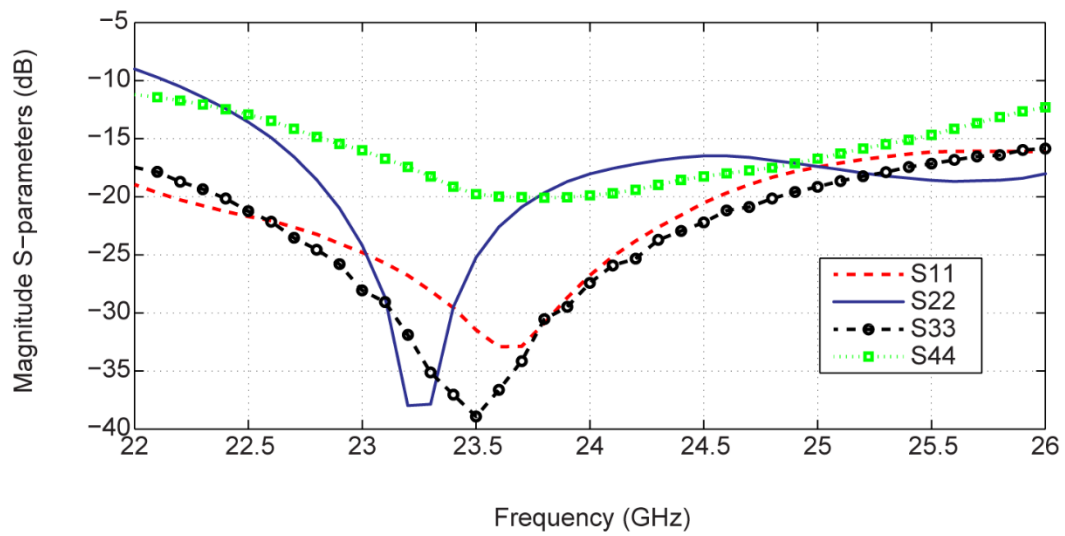


(b)

Figure 5.9: Matching and isolation conditions between RF and LO ports; (a): Simulation, (b): Measurement.

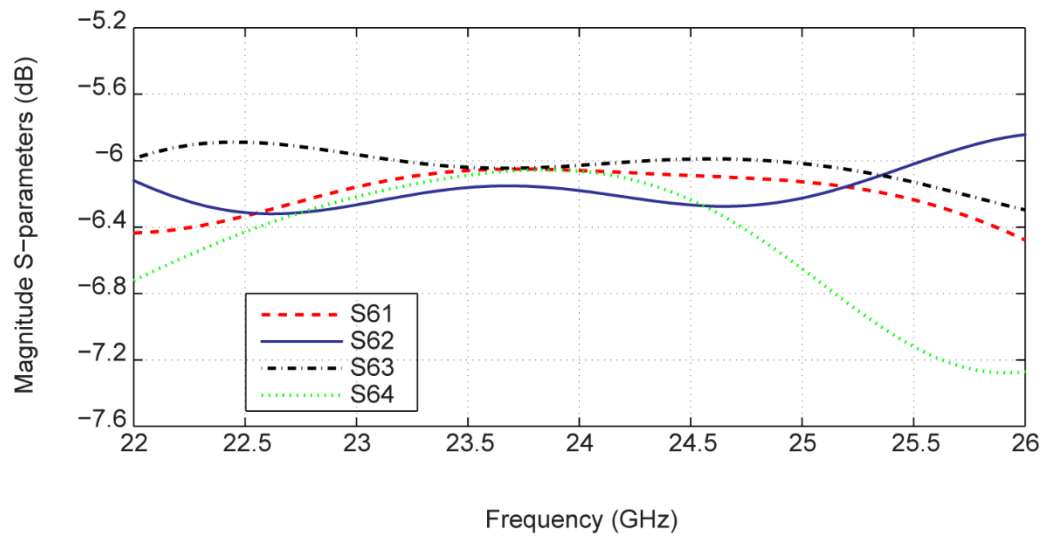


(a)

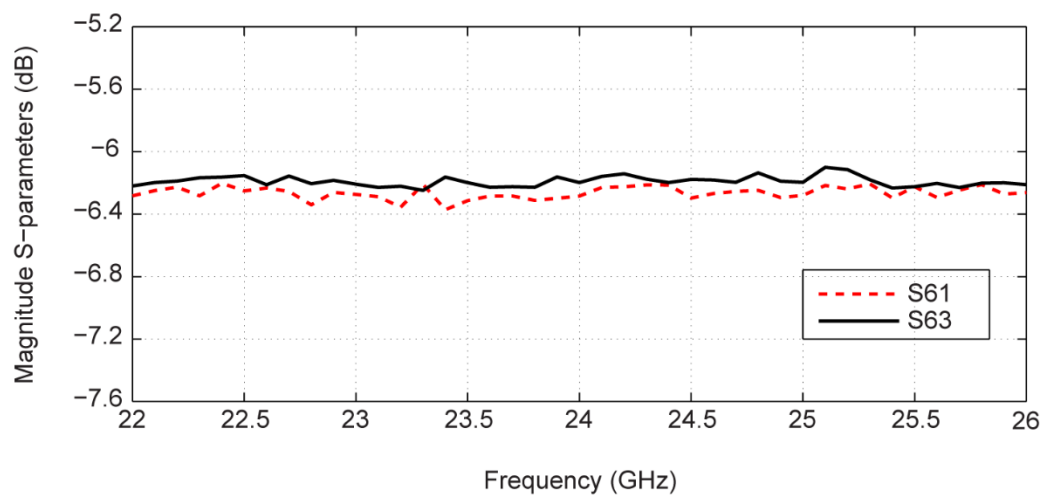


(b)

Figure 5.10: Matching conditions of output ports; (a): Simulation, (b): Measurement.

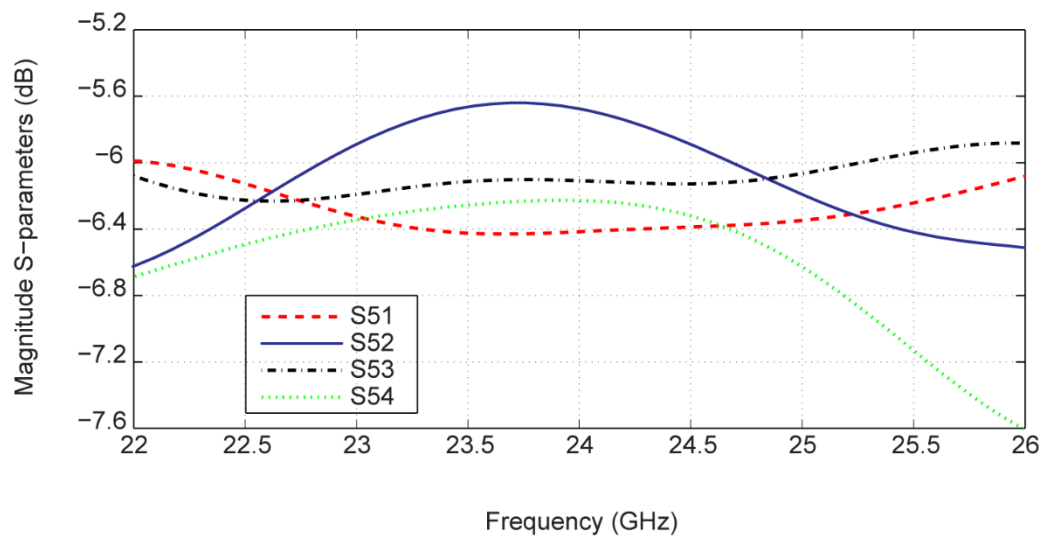


(a)

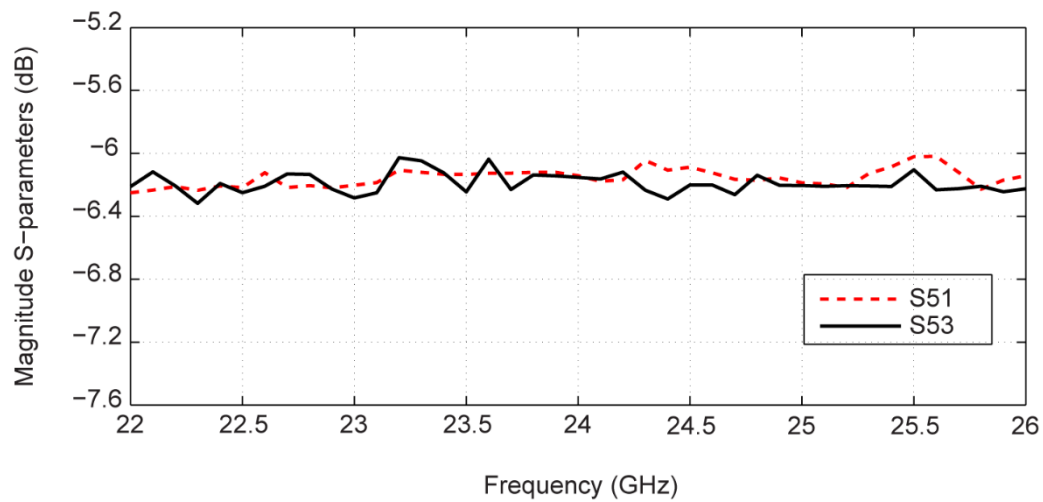


(b)

Figure 5.11: Transmission from RF port to outputs; (a): Simulation, (b): Measurement.

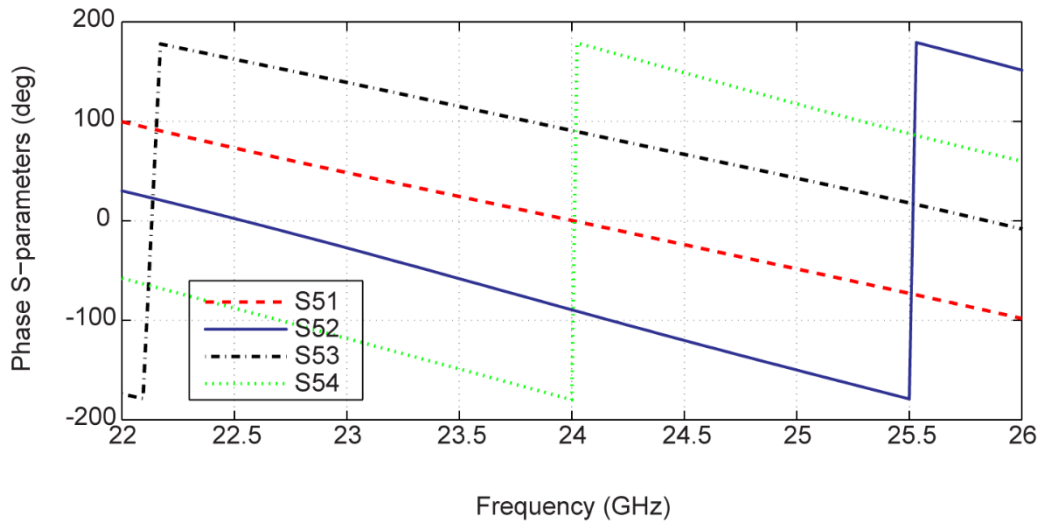


(a)

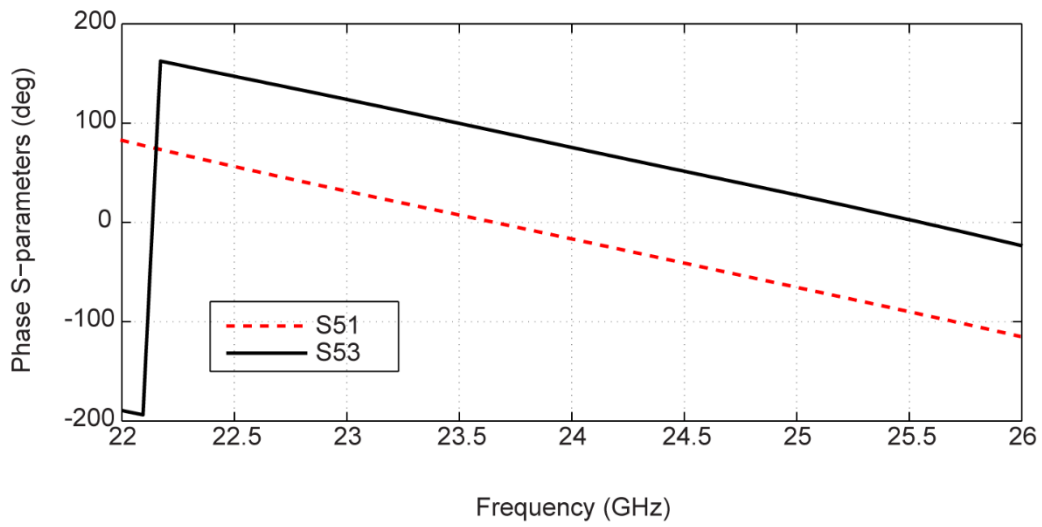


(b)

Figure 5.12: Transmission from LO port to outputs; (a): Simulation, (b): Measurement.

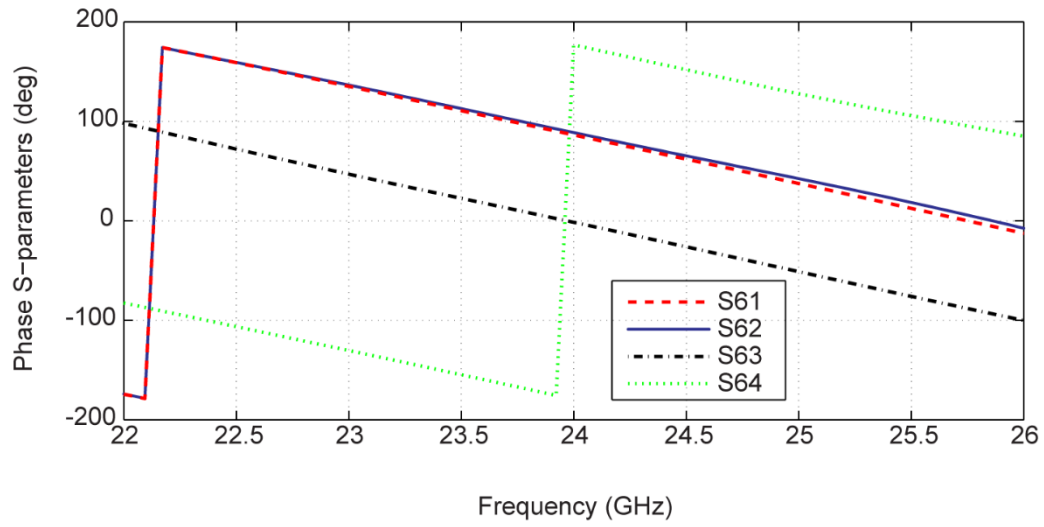


(a)

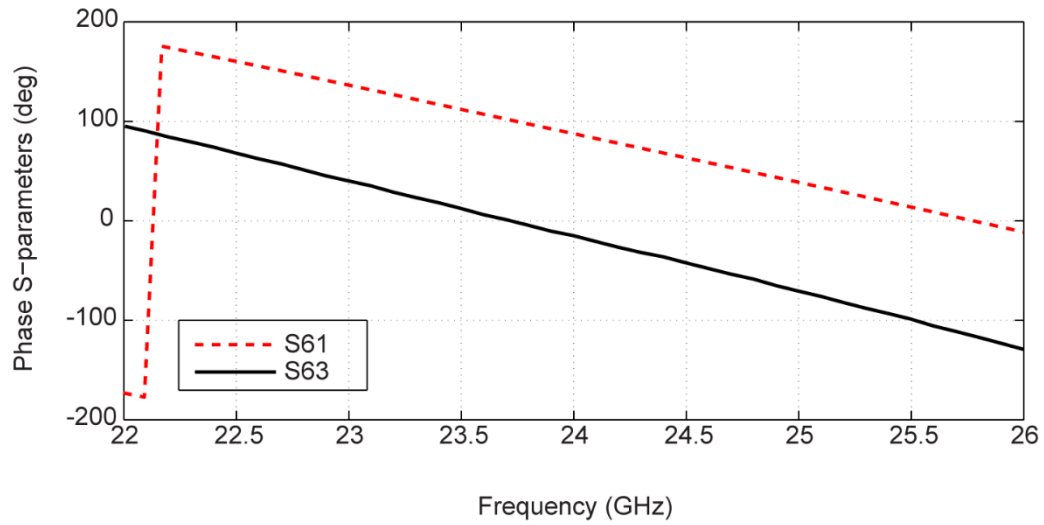


(b)

Figure 5.13: Phase transmission between LO port and outputs; (a): Simulation, (b): Measurement.



(a)



(b)

Figure 5.14: Phase transmission between RF port and outputs; (a): Simulation, (b): Measurement.

5.1.3 Six-port receiver analysis

In the six-port receiver presented by Tatu [37] (shown in Figure 5.15) for demodulation purpose, the six-port junction is used together with power detection to use the nonlinearity characteristics of detection procedure in order to recover the baseband signal [93]-[96] and [29]. The power detection is normally done by using zero bias Schottky diodes, since they can realize high data rate due to their high speed property. To recover the baseband signal, the modulated RF (a_6) and the coherent LO (a_5) are injected to the six-port junction where they are linearly combined together with difference phase shift in accordance with the S-parameters of six-port junction. On the other word, the instantaneous phase shift and the relative amplitude between the unknown received RF signal and the known reference signal (LO), are obtained by output power measurements. The output at ports (a_1 to a_4) is the input to nonlinear device (Schottky diode) for power detection. The nonlinear transfer function of the diode which is a square law transfer function, among other frequencies, generates the demodulated baseband signal.

The phase relations in the six-port junction together with the nonlinear processing allow to separate the I and Q baseband channels. As mentioned before, the DC offset is a serious problem in a direct conversion receiver since it overlaps the desired baseband signal [2] and [97] also it creates a noise problem on the A-D conversion, too. Nevertheless, by taking the difference between the diode's output current on specified ports (using differential baseband amplifier) the DC offset can be effectively suppressed in the detected baseband I and Q channels.

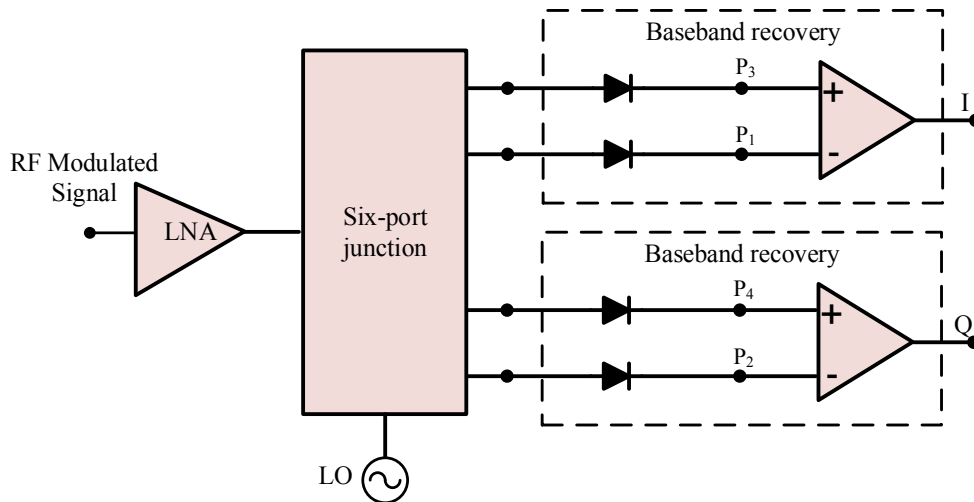


Figure 5.15: Analog front-end of six-port receiver.

To show the demodulation process, the modulated RF and LO signals are described in the complex domain as follows

$$a_5 = A_{LO} e^{j\phi} e^{j\omega t} \quad (5.9)$$

$$a_6 = A_{RF} (X_I + jX_Q) \quad (5.10)$$

where ω denotes frequency, ϕ is the phase difference between the modulated RF signal and LO signal and A_{RF} and A_{LO} represent the RF and LO amplitudes, respectively. X_I and X_Q are the transmitted baseband I and Q data. The combined signal at the output of each port, is expressed by:

$$y_x = S_{x5} a_5 + S_{x6} a_6 \quad (5.11)$$

in which x corresponds to one of the four output port (a_1 to a_4) and S_{nm} is the related forward transmission from port m to n of the six-port junction. Considering an ideal power detector with the square law transfer function described by

$$i_D = k v_D^2 \quad (5.12)$$

where i_D is the diode current, v_D is the applied voltage and k is the constant value. Therefore, after y_x passing through the ideal diode and low-pass filtering can be defined by

$$V_x = LPF\{k Y_x^2\} = k \frac{\overline{y_x y_x}}{2} = k \frac{|y_x|^2}{2} \quad (5.13)$$

while Y_x is the real part of y_x and is calculated as

$$Y_x = \Re\{y_x\} = \frac{y_x + \overline{y_x}}{2} \quad (5.14)$$

By setting $k = 1$ for simplification and doing some straightforward manipulation, the output voltage V_x is obtained as

$$\begin{aligned} V_x = & |S_{x5}|^2 \frac{A_{LO}^2}{2} + |S_{x6}|^2 \frac{A_{RF}^2}{2} (X_I^2 + X_Q^2) + \\ & A_{RF} A_{LO} |S_{x5}| |S_{x6}| X_I \cos(\phi + (\angle S_{x6} - \angle S_{x5})) + \\ & A_{RF} A_{LO} |S_{x5}| |S_{x6}| X_Q \sin(\phi + (\angle S_{x6} - \angle S_{x5})) \end{aligned} \quad (5.15)$$

where

$$|S_x| = |S_{x6}| |S_{x5}| \quad (5.16)$$

$$\angle S_x = \angle S_{x6} - \angle S_{x5} \quad (5.17)$$

$$L_x = |S_{x6}|^2 \frac{A_{RF}^2}{2} \quad (5.18)$$

$$M_x = |S_{x5}|^2 \frac{A_{LO}^2}{2} \quad (5.19)$$

$$N_x = A_{LO} A_{RF} |S_x| \quad (5.20)$$

$$R = X_I^2 + X_Q^2 \quad (5.21)$$

Therefore, the voltage at the each output can be written by

$$\underbrace{\begin{bmatrix} M_1 & L_1 & N_1 \cos \angle S_1 & N_1 \sin \angle S_1 \\ M_2 & L_2 & N_2 \cos \angle S_2 & N_2 \sin \angle S_2 \\ M_3 & L_3 & N_3 \cos \angle S_3 & N_3 \sin \angle S_3 \\ M_4 & L_4 & N_4 \cos \angle S_4 & N_4 \sin \angle S_4 \end{bmatrix}}_G \begin{bmatrix} 1 \\ R \\ X_I \\ X_Q \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} \quad (5.22)$$

where G is the matrix which describes the six-port demodulator and is dependent on the implementation of the six-port junction and its related S-parameters. Considering the B configuration of the six-port junction, according to (5.6), the corresponding G matrix is obtained as follows

$$G = \begin{bmatrix} \frac{A_{LO}^2}{8} & \frac{A_{RF}^2}{8} & 0 & -\frac{A_{RF} A_{LO}}{4} \\ \frac{A_{LO}^2}{8} & \frac{A_{RF}^2}{8} & -\frac{A_{RF} A_{LO}}{4} & 0 \\ \frac{A_{LO}^2}{8} & \frac{A_{RF}^2}{8} & 0 & \frac{A_{RF} A_{LO}}{4} \\ \frac{A_{LO}^2}{8} & \frac{A_{RF}^2}{8} & \frac{A_{RF} A_{LO}}{4} & 0 \end{bmatrix} \quad (5.23)$$

The LO power is assumed to be known. Therefore, only X_I , X_Q and R are unknown while four equations are available and one of the equations is linearly dependent on the others and matrix G is singular. By inspection of (5.24) together with (5.25), it is seen that the data of I channel can be recovered by taking the difference of $V_3 - V_1$, and the detected Q channel by taking the difference of $V_4 - V_2$. Therefore

$$I = \frac{2}{A_{LO}A_{RF}}(V_3 - V_1) \quad (5.24)$$

$$Q = \frac{2}{A_{LO}A_{RF}}(V_4 - V_2) \quad (5.25)$$

As it can be seen from equations (5.24) and (5.25), in this case, the DC offset from LO (M_x) and RF (L_x) as well as the nonlinear distortion (R) are cancelled on the I and Q channels. To recover the baseband I and Q channels with DC offset suppression, equations (5.24) and (5.25) must be implemented by using differential amplifiers or in the FPGA.

5.2 Simultaneous wireless energy harvesting and data communication

Since it was mentioned before, the main idea of this research work is to design a six-port receiver with the capability of simultaneous wireless energy harvesting and data communication. Therefore, we need to redesign the detector circuit of the six-port receiver in order to increase its RF-to-DC conversion efficiency and add the capability of detection and harvesting at the same time. In the sequel, a common configuration of a six-port detector circuit and its drawbacks in terms of energy harvesting are studied, then the proposed architecture is presented.

5.2.1 Common configuration of RF rectifier and detector circuit

To study the detection circuit of a conventional six-port receiver, we refer to (5.15) which describes the output of the power detectors. According to (5.15) the output of the power detector consists of three elements; the desired phase difference between the modulated and the reference signals (N_x), the self-mixing component of the LO signal (M_x) and multiplication of the self-mixing

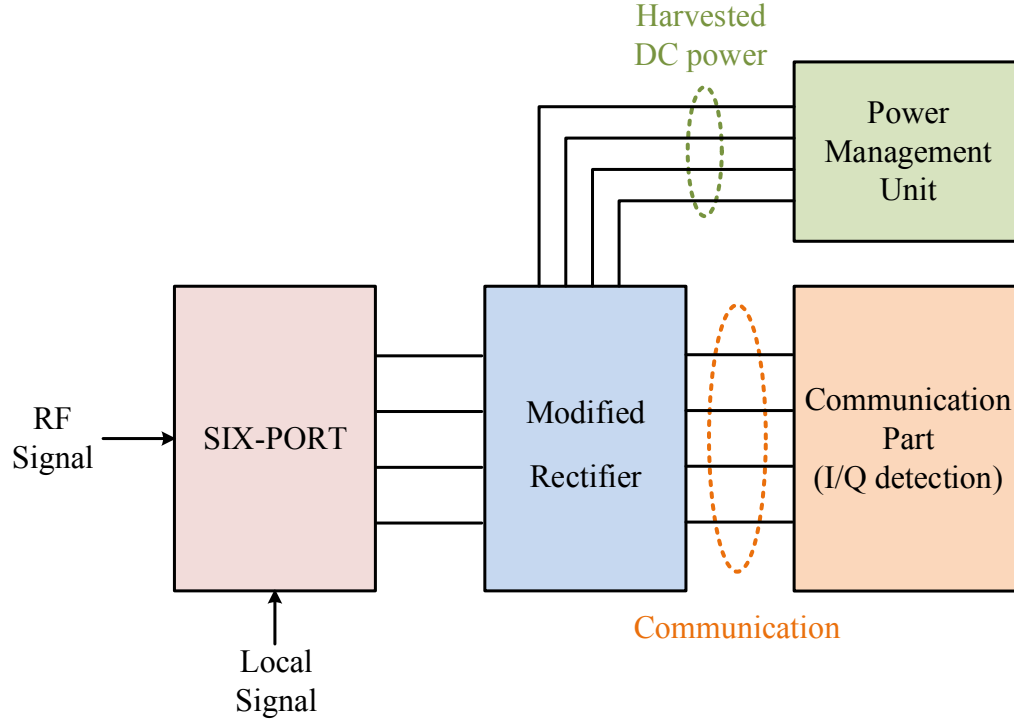


Figure 5.16: System architecture of the proposed power harvester and data communication.

component of the modulated signal (L_x) and the nonlinear distortion (R). As explained in the previous section, in the conventional six-port receiver to recover the I and Q channels, the DC offset from LO as well as the nonlinear distortion (R) should be cancelled out, which leads to the waste of the rectified power. However, since we are interested to harvest the power of the rectified signal, we need to use (M_x) and (L_x) instead of cancelling them out. This can be done by using a different structure of the power detector at the output ports of the six-port junction to have harvesting and detection at the same time. The structure of the proposed six-port receiver is shown in Figure 5.16.

Moreover, the RF-to-DC conversion efficiency of the detector circuit is another important issue which has to be considered. A conventional detector circuit used in a conventional six-port receiver is shown in Figure (5.17). It includes a matching circuit to match the input impedance of the Schottky diode to the six-port outputs (in our case it is matched to $50\ \Omega$), the Schottky diode, a DC-pass filter and a resistive load. The structure of a detector circuit is similar to a rectifier circuit which has been investigated in detail in Chapter 3. The diode that is normally employed in the

detector circuit is not a good candidate for efficient RF-to-DC rectification since it has a high series resistance which causes more loss inside the diode.

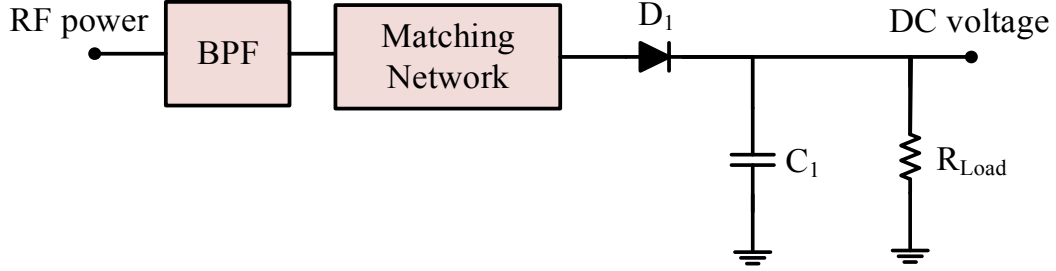


Figure 5.17: Common structure of a detector circuit.

5.2.2 Proposed architecture of detector for simultaneous energy harvesting and data communication

According to the above-mentioned explanations and in order to have the energy harvesting and the data communication at the same time, the detector circuit of the six-port receiver have to be modified to address its low RF-to-DC rectification efficiency because of the improper diode selection and the waste of rectified signal. To this end, the proposed detector circuit is capable of producing a higher DC power as well as supplying a power management and the I/Q detection units (Figure 5.16). In order to improve the RF-to-DC rectification efficiency of the six-port detector, we need to select an appropriate diode. To choose a proper Schottky diode for both detector and rectifier purpose, several Schottky diodes are examined. To do so, we design a simple detector circuit using different Schottky diodes. The performance of each circuit is examined in terms of RF-to-DC conversion efficiency. Eventually MA4E1317 GaAs Schottky barrier diode from MACOM is chosen as detector and rectifier since it shows superior performance as well as the highest RF-to-DC conversion efficiency compared to its counterparts (Figure 5.18). Also, the selected Schottky diode has the cutoff frequency of 80 GHz which supports our design frequency of 24 GHz. The specifications of MA4E1317 are summarized in Table 5.1.

As mentioned before, we are taking the same approach explained in detail in chapter 3 to design the rectifier. The rectifier of interest is a single diode in the series configuration which is designed and fabricated using the same substrate and technique as the six-port junction, a 10-mil-thick ceramic fabricated by MHMIC technology. Since the designed rectifier will be integrated

into the designed six-port junction, it needs to be completely matched to the six-port outputs with $50\ \Omega$. An accurate experimental characterization technique is used to design the matching network (the more detail has been discussed in 3.2.2). To do so, we need to measure the selected Schottky diode individually to extract the packaging and parasitic effects and determine the related real circuit model. Then, the real circuit model of the Schottky diode is used in designing the rectifier.

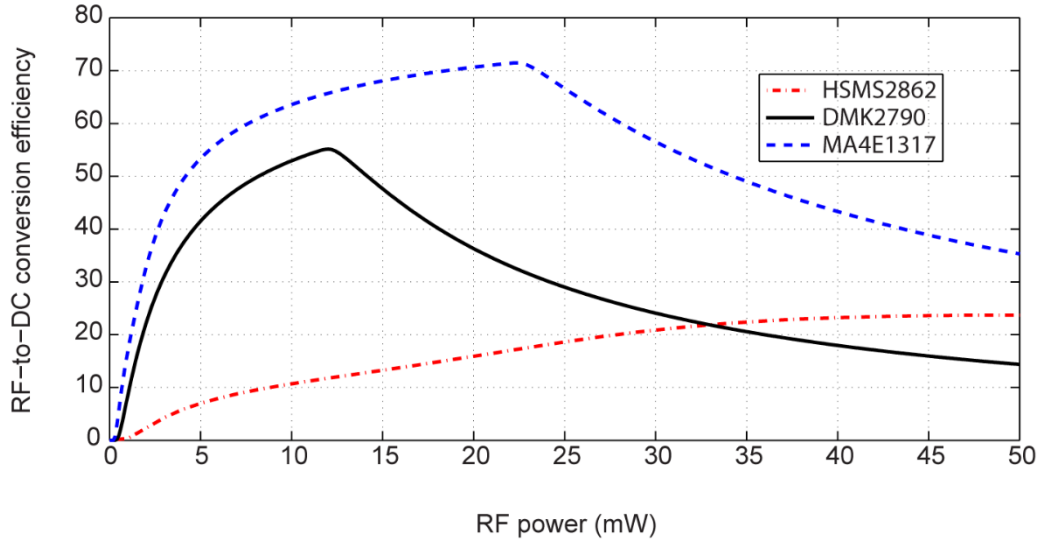


Figure 5.18: RF-to-DC conversion efficiency for different Schottky diodes.

Table 5.1: MA4E1317 Schottky diode specifications.

Parameters	Unit	MA4E1317
R_s	Ω	4
C_{j0}	pF	0.02
N	-	1.08
M	-	0.38
E_G	eV	1.424
IKF	A	0.016
B_v	V	7
V_j	V	0.86

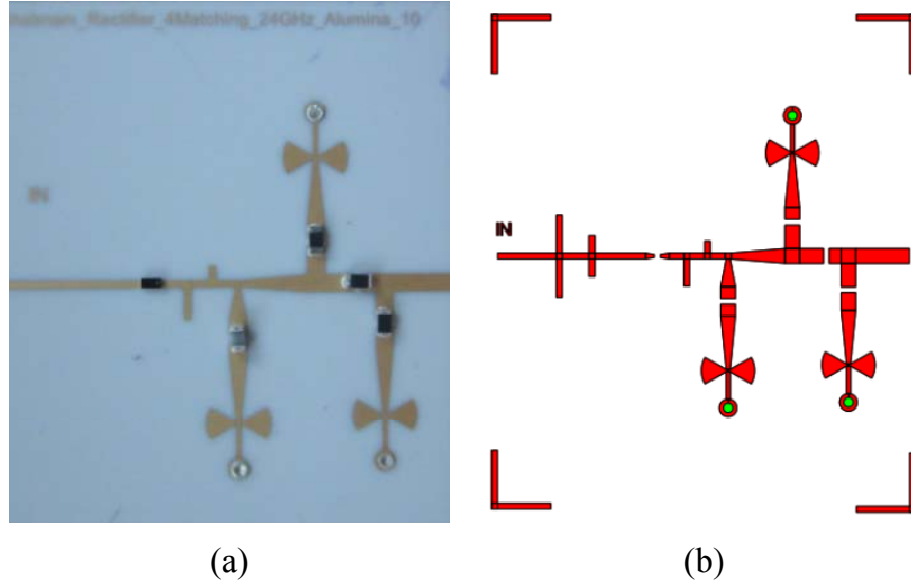


Figure 5.19: (a): Fabricated rectifier used to design the matching network; (b): Layout of the designed rectifier.

Consequently, the rectifier is designed and fabricated with no matching, to obtain its input impedance and the related S-parameters experimentally. Finally the measured S-parameters are used to design a quality matching network. Figure 5.19 shows the fabricated rectifier circuit used to design the matching and the layout of the rectifier plus matching circuit. According to the results shown in Figure 5.20, the input port of the rectifier is completely matched, therefore all the power will be transmitted from the six-port outputs to the rectifiers.

After satisfying a high efficiency rectification, we need to address the issue of cancelling the self-mixing component of the LO signal and multiplication of the self-mixing component of the modulated signal and the nonlinear distortion. To do so, an adaptive voltage divider network including several variable resistors is designed and placed at the output of rectifier circuits. The structure of the modified detector is shown in Figure 5.21. As it is seen in (Figure 5.21), the output voltage at point A can go for harvesting while the output voltage at point B can be transmitted to differential amplifiers to perform the I and Q detection process. Here, R_1 , R_2 and R_3 are the variable resistors which determine how many percent of the rectified wave can be dedicated to the harvesting and detection process.

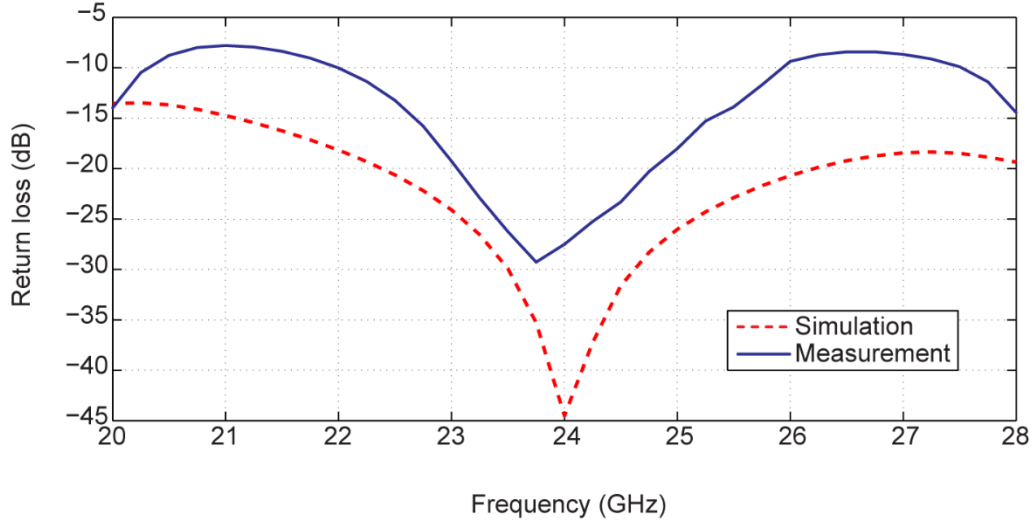


Figure 5.20: Matching condition of the designed rectifier.

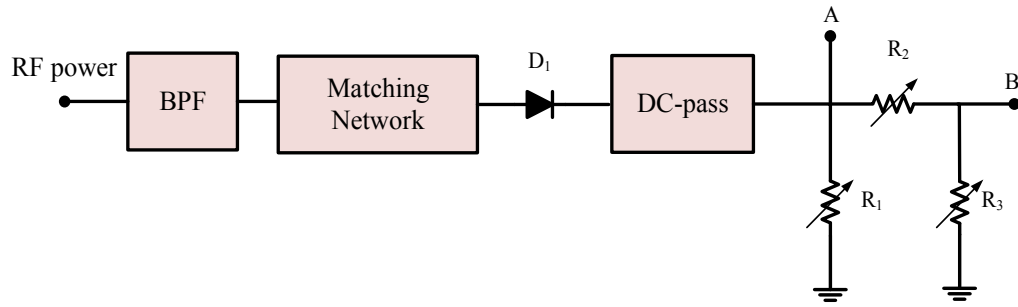


Figure 5.21: Configuration of the modified detector used for simultaneous wireless energy harvesting and data communication.

To design such a detector with the function of detecting and harvesting, two main criteria need to be considered:

1. The minimum required power which guarantees to drive the baseband processing module.
2. Threshold levels (used to detect the transmitted data from the obtained I and Q signals) adjustment.

5.2.2.1 Data communication considerations

The main issue to be considered is the effect of the power splitter on the performance of the data communication circuit. In the other word, the proposed structure may raise an uncertainty about the fact that the use of splitter may change the signal to noise ratio. As mentioned in the

beginning of this chapter, we have two main sources of noise in the proposed receiver including the thermal noise and the rectifier noise. Since the power splitter is placed at the output of the rectifier circuit, the signal to noise ratio (SNR) does not change. It is due to the fact that the useful and noisy parts of the rectified signal are divided by the same factor which does not affect the SNR. Figure 5.22 depicts the effect of power splitter on the amplitude of the rectified signal and the noise term. Obviously, dividing the output signal of the rectifier shrinks the size of constellation, it reduces the size of the clouds (thermal noise plus rectifier noise) around the constellation points which yields the same SNR.

Additionally, two other issues have to be considered. First, the power ratio of the splitter has to be optimized considering the minimum acceptable input voltage of the differential amplifier or analog to digital converter used to detect I and Q streams. The other important issue is to adjust the threshold level used to detect the transmitted data from the obtained I and Q signals, according to the splitter power ratio. First, let us elaborate the effect of splitter power ratio on the constellation of the received signal. As shown in Figure 5.22, for instance, splitting the output of the rectifier for QPSK and 32-PSK modulations leads to constellations with smaller size. Therefore, considering the main concept behind the demodulation of data from the detected I and Q (i.e. comparing the detected I and Q with predefined thresholds), we have to adjust the detection thresholds in order to have a non-erroneous demodulation. For example, considering 32-PSK modulation in Figure 5.22,

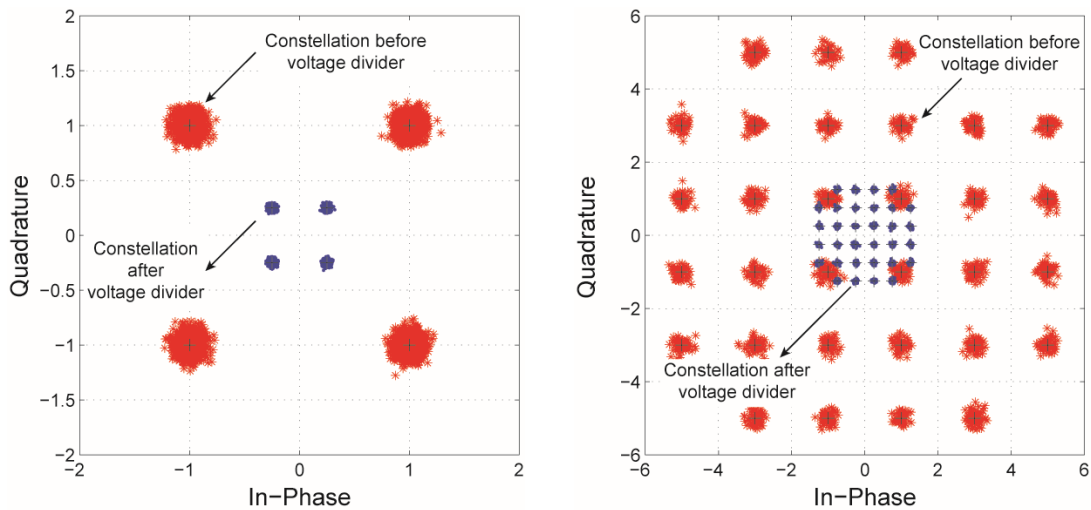


Figure 5.22: Effect of the splitter power ratio on the constellation of the received signal.

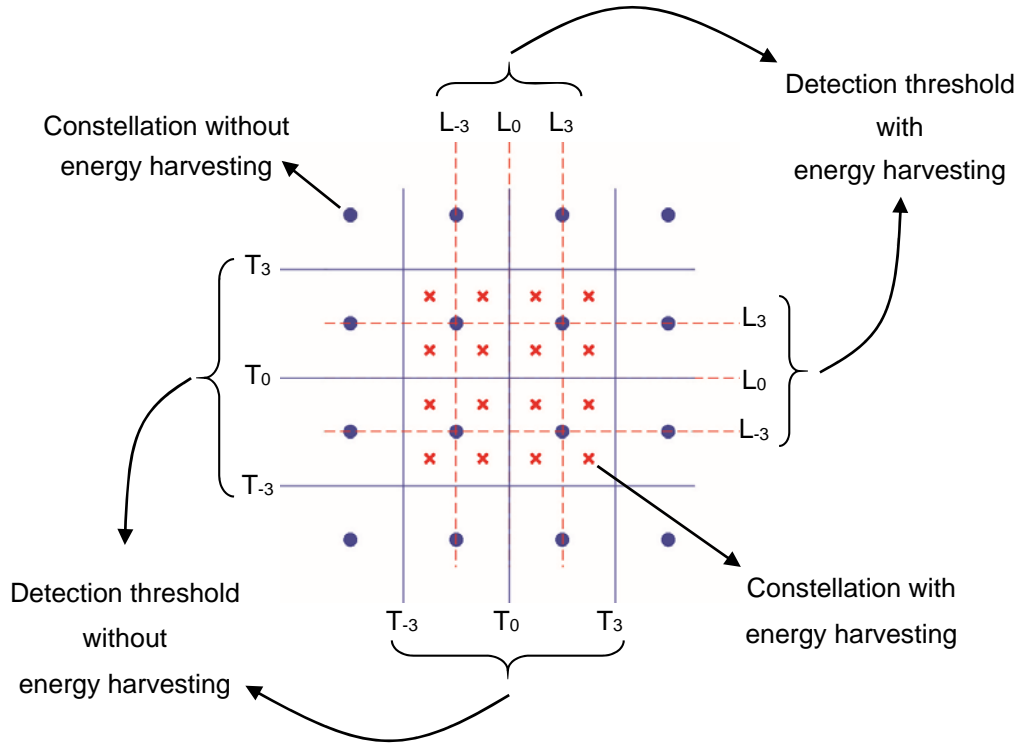


Figure 5.23: Detection thresholds before and after power splitting.

the detection thresholds for a system without power splitter are $\{-4, -2, 0, 2, 4\}$ which are not suitable for the proposed system (i.e. usage of splitter) which leads to an erroneous detection for most of the constellation points. Therefore, for the proposed system, the detection thresholds need to be changed to $\{-1, -0.5, 0, 0.5, 1\}$.

Figure 5.23 shows the constellations of a 16-PSK modulated signal before and after power splitting with their detection thresholds (the constellation of modulated signal before and after splitting represented by dot and cross, respectively). It is obvious that considering the received data stream after splitter, if the demodulator uses the previous detection thresholds (solid line) to detect the transmitted data, only some of the constellation points are detected correctly. For instance, in Figure 5.23, considering a system without energy harvesting, T_{-3} , T_0 and T_{+3} are used to demodulate the detected I and Q streams. However, when we consider a system with energy harvesting, if we compare the constellation points (cross points) with T_{-3} , T_0 and T_{+3} thresholds, only 4 constellation points are detected correctly. Therefore, we have to define a set of new thresholds (L_{-3} , L_0 and L_{+3}) in order to correctly demodulate I and Q streams. Consequently, in the proposed simultaneous

energy harvesting and data communication system, an adaptive signal processing algorithm has to be used to modify and adapt the detection thresholds considering the power splitter factor.

5.2.3 ADS simulation of the six-port receiver with the capability of simultaneous wireless power transmission and data communication

To design a six-port receiver using ADS simulation, the six-port junction and the rectifier circuits are first designed and tested individually to make sure about the required isolation and the matching condition. In order to have accurate results, simulations of the six-port and rectifiers are done on both schematic (HB simulator) and layout levels (Momentum simulator). Then, the co-simulation is run to guarantee the performance of the designed modules. Before analyzing the performance of the designed receivers, we should check the output of the rectifiers as well as the detectors which have been connected to the six-port junction (P₁ to P₄, Figure 5.24 and P₇ to P₁₀, Figure 5.26) to verify the required 90° phase shifts. To do that, the HB simulator is run at the operating frequency (24 GHz) while the phase difference between two RF input signals (RF and LO in this case) is swept from 0° to 360°. Figure 5.25 and Figure 5.27 show the results of the output detected voltages versus the phase difference for both circuits.

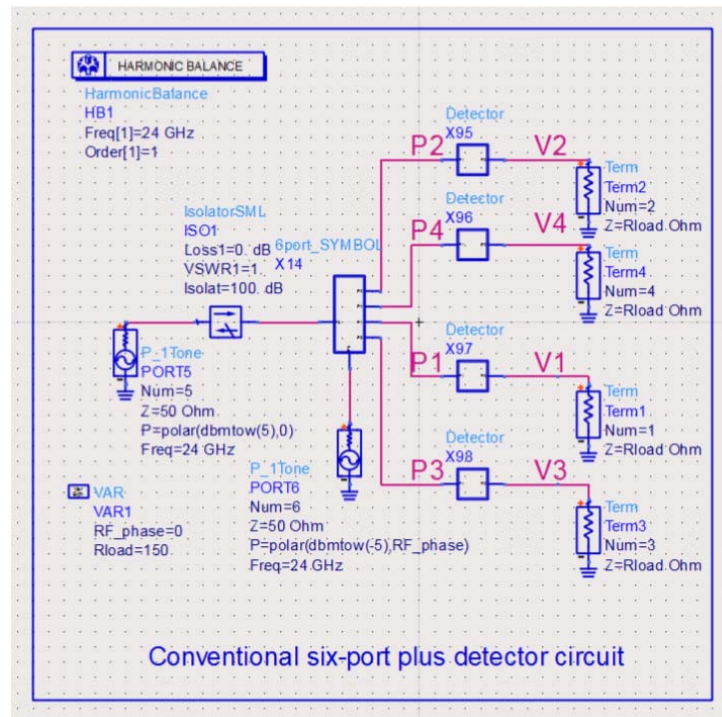


Figure 5.24: ADS simulation of a conventional six-port detector.

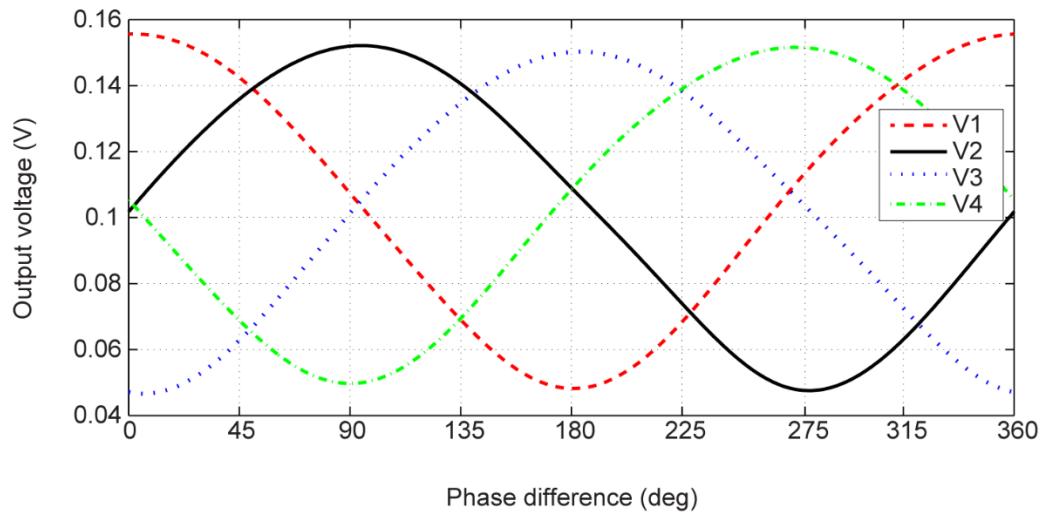


Figure 5.25: Simulation results of DC voltage versus phase difference between the two input ports of a conventional six-port.

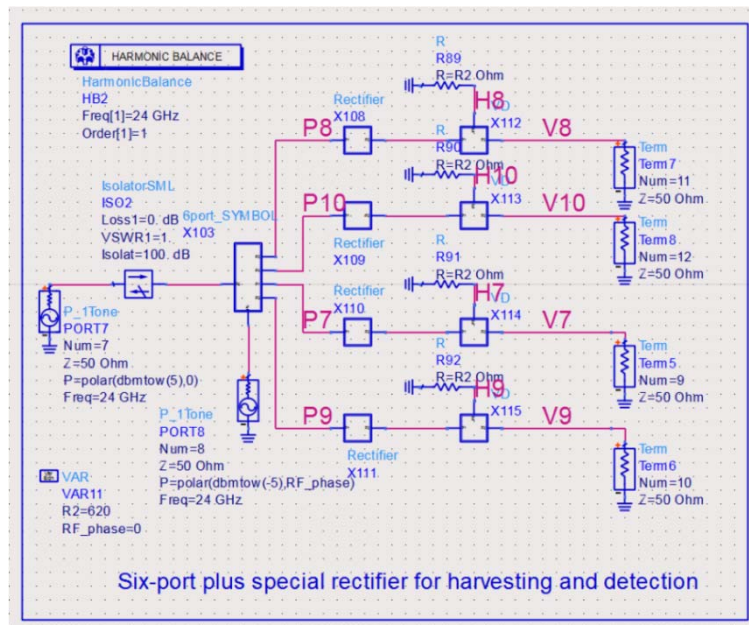


Figure 5.26: ADS simulation of the six-port with the function of harvesting and data communication.

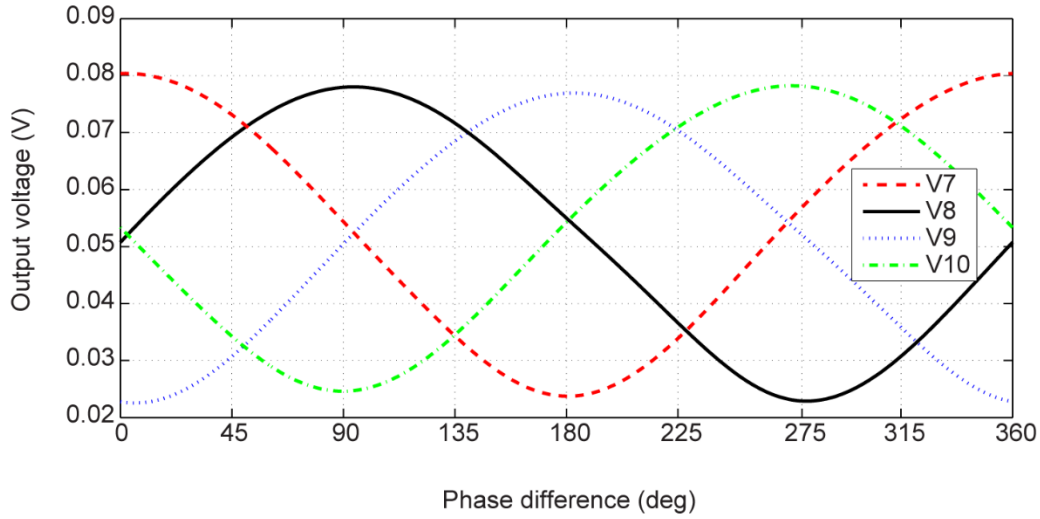


Figure 5.27: Simulation results of DC voltage versus phase difference between the two input ports of six-port with the function of harvesting and detection.

As previously mentioned, the proposed six-port receiver has a rectifier with the special design that provides the capability of harvesting and communication at the same time. To do that, the DC voltage at the output of this rectifier is split by a specific ratio in such a way that some part of DC power goes to the differential amplifiers (V7 to V10, Figure 5.26) to perform the I and Q detection process, while the rest is sent to the harvesting unit (H7 to H10, Figure 5.26). By comparing results shown in Figure 5.25 and Figure 5.27, it can be concluded that, however, the level of DC voltage obtained from the proposed six-port (V7 to V10) is smaller than that achieved from the conventional model (V1 to V4, Figure 5.24); but still the proposed configuration grants the correct phase difference which can guarantee the precision of I and Q detection.

Consequently in order to demonstrate the demodulation capability of the two receivers; the conventional model and the other with the capability of harvesting and data communication, both receivers are simulated using the ADS envelope simulator for different types of modulation schemes (QPSK, 8PSK and 16PSK). The ADS schematics of both six-port receivers are shown in Figure 5.28 and Figure 5.29. As seen in the ADS schematic, for both receivers, the envelop simulation is performed during 100 μ s with time step of 0.2 μ s. The operating frequency is set at 24 GHz, the transmitter is placed at the distance of 5 m from the receiver, the transmitted RF power is set at -5 dBm and the transmitter antennas have a gain of 20 dBi. At the receiver side, the gain

of the input LNA is set at 20 dB and the LO signal is set at 5 dBm. Also, in order to consider a more realistic condition, the simulation is done in the presence of white noise, therefore a noise

generator is added between the receiving antenna and the LNA. Moreover, to obtain a clearly demodulated constellation points, two “sample-and-hold” (SHCs) are considered at the output of differential amplifiers. The output signals change only once at each time clock. Therefore, the constellation is realized by discrete points. Figure 5.30, Figure 5.31 and Figure 5.32 show the related demodulated constellation diagram for each QPSK, 8PSK and 16PSK modulation. As it is seen, all the clusters of demodulated constellations are very well positioned and individualized. In the case of receiver performed simultaneously wireless power transmission and data communication, however, the constellation points are closer together (compared to the conventional receiver), but still the Euclidean distance is granted and the detection can be performed precisely. Since it was explained before, in the simultaneous wireless power transmission and data communication, six-port receiver (Figure 5.29), the collected DC power at points V7 to V10 are dedicated to the detection process and transferred to the differential amplifiers while the generated DC powers collected at points H7 to H10 are considered as the harvested powers. Figure 5.33- Figure 5.36, compare the voltage level of these points versus time for QPSK modulated signal. According to the obtained results, it can be concluded that the designed six-port receiver can realize the energy harvesting and data communication at the same time.

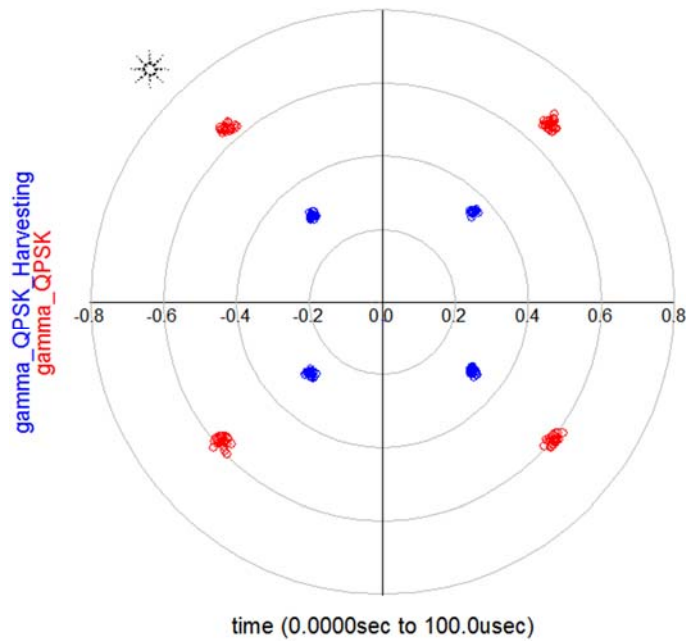


Figure 5.30: Constellation of the demodulated QPSK signal.

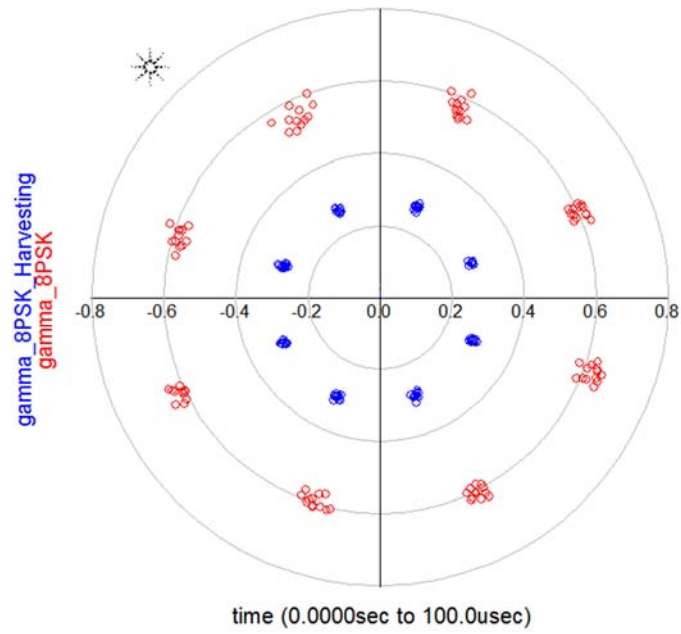


Figure 5.31: Constellation of the demodulated 8PSK signal.

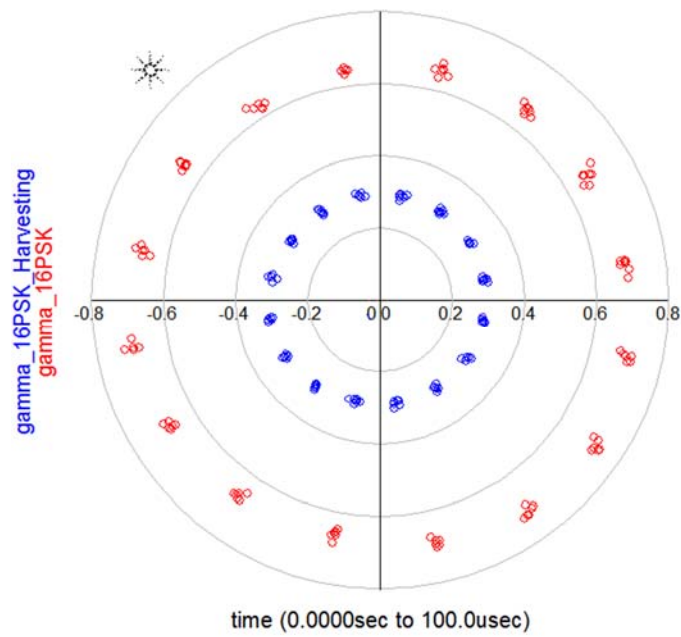


Figure 5.32: Constellation of the demodulated 16PSK signal.

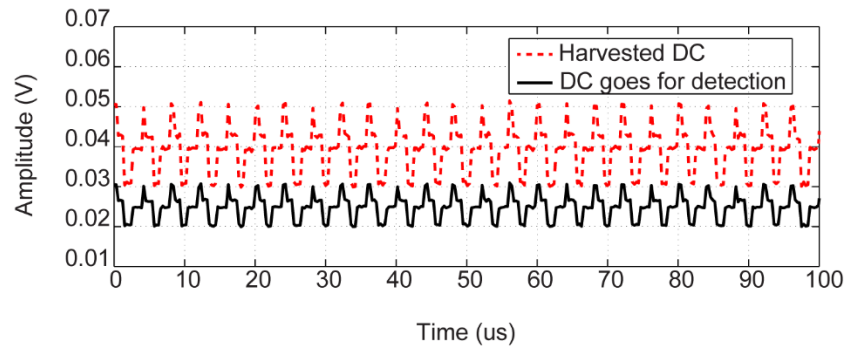


Figure 5.33: Collected DC voltage at points V7 and H7 shown in Figure 5.29.

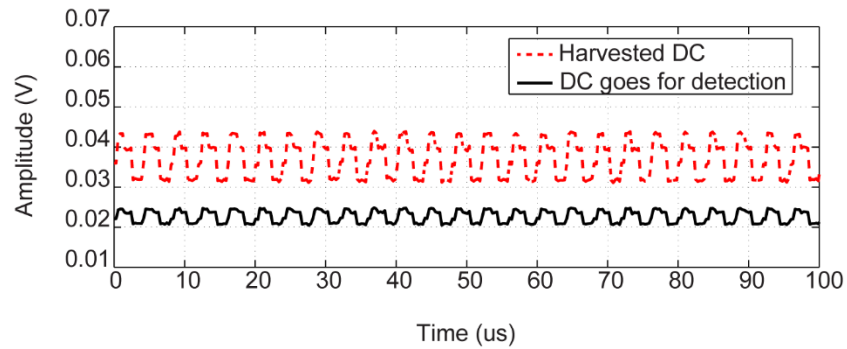


Figure 5.34: Collected DC voltage at points V8 and H8 shown in Figure 5.29.

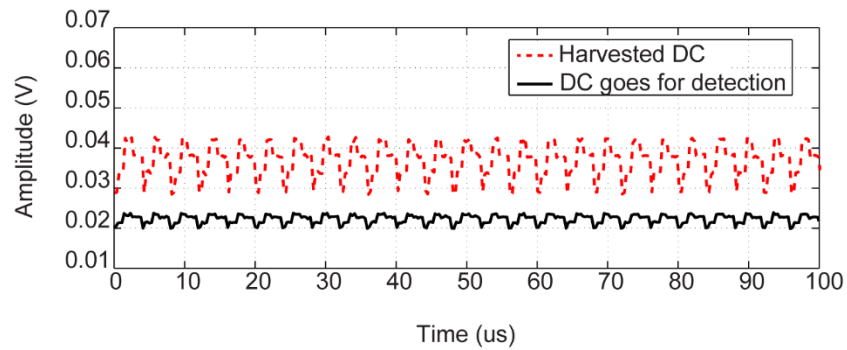


Figure 5.35: Collected DC voltage at points V9 and H9 shown in Figure 5.29.

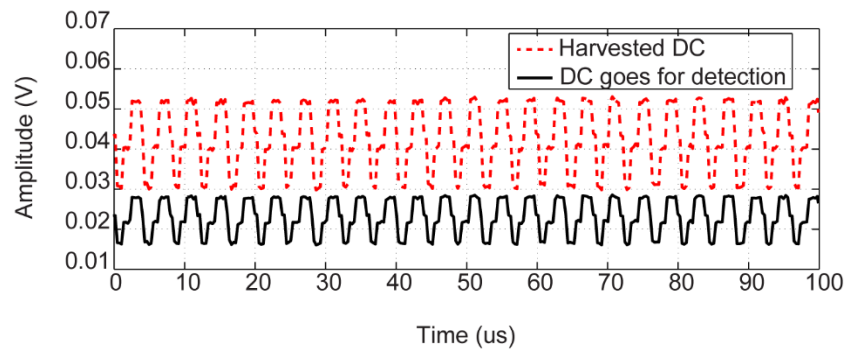


Figure 5.36: Collected DC voltage at points V10 and H10 shown in Figure 5.29.

5.3 BER performance analysis

In order to study the effect of the proposed simultaneous energy harvesting and data communication structure on the performance of the communication part, the BER of the conventional six-port and the proposed structure is compared in Figure 5.37. It is depicted that the use of splitter does not affect the BER of the system, due to the fact that the signal to noise ratio remains constant and the thresholds are properly adjusted.

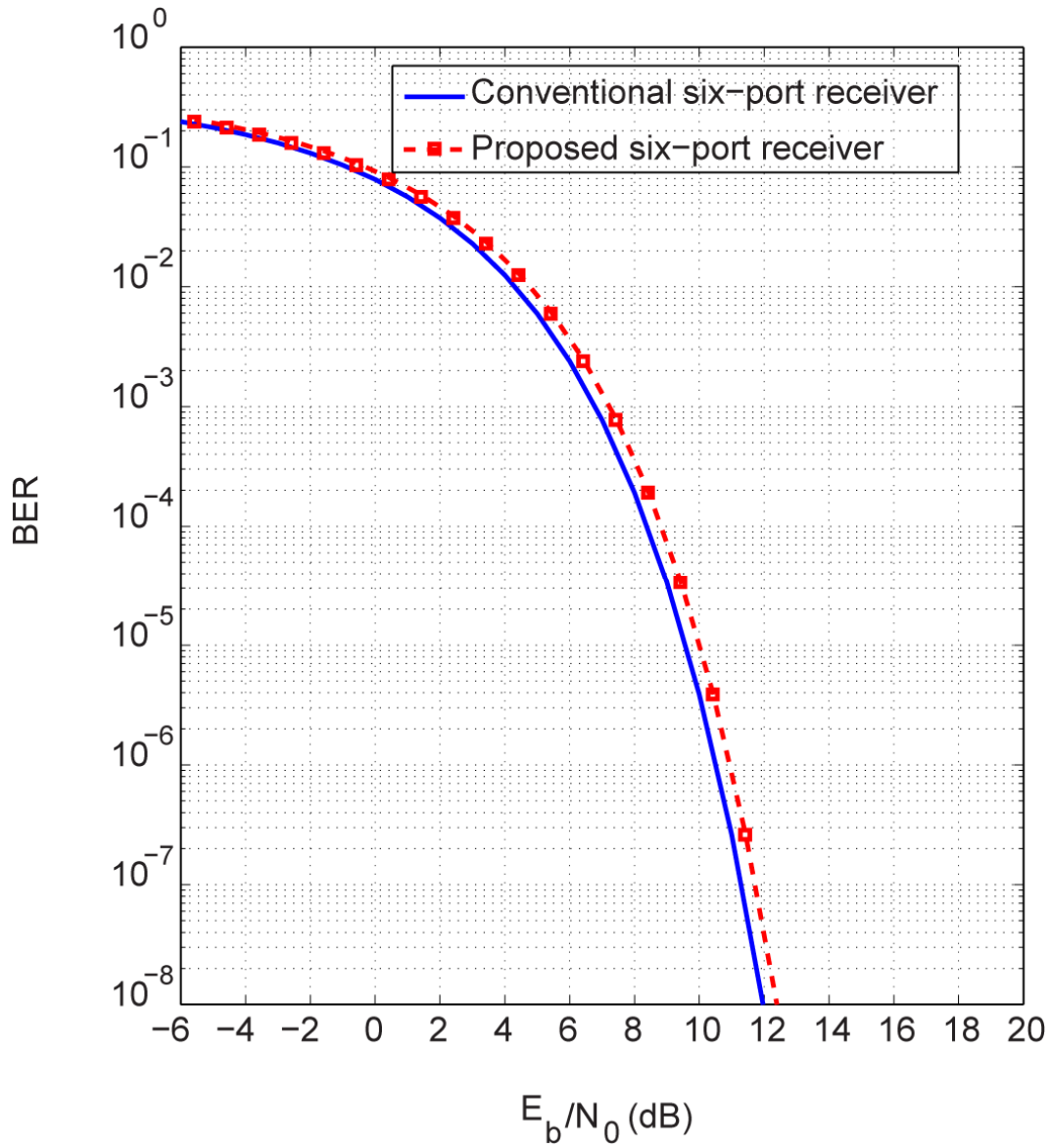


Figure 5.37: BER performance of the ADS simulation for both receivers with QPSK modulation.

5.4 Conclusion

This chapter presents a review of different configurations of six-port junction and extracts the related S-parameters of each configuration. Also, the design and fabrication process of a 24 GHz six-port junction is explained and the measurement results are presented. In the sequel, the idea of a simultaneous wireless power transmission and data communication system using the six-port receiver is presented. To this end, the designed six-port is integrated with a special rectifier that can split the generated DC power with a specific ratio. The ADS simulation of the six-port receiver with the features of power harvesting and data detection is presented and its performance in terms of constellation points and BER are compared to the conventional counterpart.

CHAPTER 6 CONCLUSION AND FUTURE WORKS

6.1 Conclusion

This PhD thesis has established the required procedure for the analysis, design and implementation of integrated rectifier antennas operating at up-microwave and millimeter-wave frequency with optimized efficiency for far-field wireless power transmission. Therefore, the following steps were concluded and demonstrated during this thesis research in order to carry out this framework:

- A rectifier Schottky diode was studied from the points of view of semiconductor physics, and the required factors to design a low-loss diode were defined.
- Different configurations of rectifiers were studied and the design criteria to develop high efficiency rectifiers were defined.
- According to the defined criteria, several rectifiers operating at 24 GHz and 35 GHz were designed, optimized and experimentally measured.
- The idea of self-biased technique was introduced as an effective approach to reduce the required RF power of rectifiers. To validate the idea, a self-biased rectifier operating at 24 GHz, was designed and prototyped.
- The harmonic harvesting method was presented to increase the efficiency of rectifiers. Also, a harmonic harvester rectifier operating at 35 GHz was designed and fabricated to justify the claim.
- The required specifications of antennas for wireless powering were investigated. Considering the mentioned requirements, two different antenna arrays including LP SIW slot array and CP SIW cavity-backed microstrip patch array were designed and prototyped.
- A simple and compact structure of rectenna made of a high gain microstrip patch array in connection with a self-biased rectifier operating at 24 GHz was demonstrated for wireless powering. The maximum output DC voltage of 0.6 V was

observed at power density of 10 mW/cm^2 . To the best of our knowledge, the demonstrated efficiencies are the highest reported for the power levels and frequencies of interest.

Moreover in this dissertation, the original idea of a system in support of simultaneous power transmission and data communication has been explored. To realize the idea, the subsequent steps were performed:

- Different architectures of wireless receivers were studied. Considering the desirable features for a wireless communication system such as compact-sized, low-power consumption and low-cost, the multiport (six-port) interferometer technique was recognized as an appropriate approach to developing a receiver for simultaneous energy harvesting and data detection.
- Various configurations of six-port junctions were studied and their related S-parameters were extracted. Then, a 24 GHz microstrip six-port junction, made of four hybrid couplers, was developed for the direct conversion receiver.
- A special structure of high efficiency rectifier, with the function of dividing the generated output DC voltage, was designed and connected to the six-port junction to realize a six-port receiver.
- A series of ADS envelop simulations were performed for the designed six-port receiver with the features of simultaneous power harvesting and data communication. The performance of the designed receiver in terms of constellation points and BER were compared to the conventional six-port receiver.

6.2 Future works

The research contributions presented in this thesis may be extended in the following ways:

- It is essential to conduct research for commercial and military applications on up-microwave and millimeter-wave rectennas and rectennas arrays by integrating other components and subsystems such as communications, RFID, embedded sensors and recharging vehicles and aircrafts. Plus, the basic rectenna elements (an antenna integrated with a rectifier), a recharging control circuit made of a fixed voltage

regulator is required to deliver a stable and constant voltage or current flowing into the battery.

- The fabrication technique has a significant effect on the performance of the energy harvesting circuit. Therefore, it is preferable to choose the fabrication technique which yields the least parasitic effects and minimizes the effect of components' layout. To achieve small size, circuit integration is a challenge due to the size of the wave correlator. Hence, suitable technologies such as LTCC and MMIC can be utilized to design smaller wave correlator suitable for miniaturized circuit integration. Moreover, "System on Chip" (SoC) can be considered as the recommended fabrication technique which provides a smaller circuit size, a potentially less overall cost and a better system performance, especially for millimeter-wave applications. Also, the fast improvement in CMOS scaling enables designing high speed circuits with small die size.
- Due to the fact that the sensitivity of a data communication receiver is typically much higher than that of an RF energy harvester, the system of simultaneous power harvesting and data communication needs to be improved in terms of sensitivity. Otherwise while this receiver is set at a distance away from an RF transmitter, it may be able only to decode information and fail to extract energy from the received RF signals.
- Because the receiver of simultaneous power harvesting and data communication has a strict operation power constraint, it cannot support high computational algorithms. Therefore, the existing schemes and algorithms for modulation and coding of this kind of receiver, need to be adopted to be energy-efficient and low-power.
- Since at higher millimeter-wave frequencies, such as V-band and W-band, a large number of frequency resources are available and also the atmospheric attenuation of radio waves is low, then, the operation frequency of the proposed simultaneous wireless power transfer and data communication system can be scaled-up to these frequency bands.

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